A High Precision Fully Integrated Accelerometer

by

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Abstract

The design of an integrated accelerometer controller IC is described. The IC is designed to be stitch-bonded to a micromechanical structure to form a closed loop hybrid accelerometer. The micromechanical structure (fabricated as part of a companion project) consists of a silicon proof mass supported by long silicon tethers which act as springs. Fixed electrodes are placed above and below the proof mass to capacitively sense the position of the proof mass. The accelerometer controller includes a capacitance sensor, lead-lag compensation, and a third order Delta-Sigma modulator as components of its main feedback loop. A secondary feedback loop containing a separate proportional-plus-derivative compensation is used to reset the accelerometer when necessary.

The capacitance sensor determines the deflection of the proof mass away from its equilibrium position. A lead-lag compensation network placed at the output of the C-V sensor is used to provide a large DC gain to the loop and provide positive phase shift at the system crossover frequency to ensure stable closed loop operation. The output of the Lead-Lag compensation is passed to the third order Delta-Sigma modulator which converts the analog input voltage into a high frequency bit stream. The digital output from the modulator is used to determine the feedback force to be applied to the proof mass. If the output of the modulator is a "1", the fixed electrodes are charged such that an electrostatic restoring force is placed on the proof mass in the direction of the lower electrode. If a "0" is output from the modulator, the electrodes are oppositely charged and a restoring force is directed towards the upper electrode.

When the proof mass is located more than a certain distance from its center point, the main feedback loop can become unstable as a result of nonlinearities within the loop. When this occurs, a second order reset loop is used to restore the proof mass close enough to its center position to resume higher order operation.

A novel electromechanical tuning method is presented which is used place the poles of the mechanical system near DC. By varying the voltages applied to the fixed electrodes during the C-V sense, the location of the mechanical poles can be adjusted. This can be used to minimize the input referred circuit (thermal) noise from the accelerometer controller. An incremental dynamics analysis is introduced which predicts the new locations of the poles of the mechanical system.

The test system for the accelerometer is documented. Results are presented for functionality of the accelerometer controller as well as the hybrid closed loop system. Ideas for future work are discussed in the conclusion.

Thesis Supervisor: Charles Sodini

Title: Professor of Electrical Engineering

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Table of Contents

CHAPTER 1

Introduction

The full integration of physical sensors was previously limited only by the inability to place mechanical parts on chip. Since the advent of micromachining, there is now a mechanism available on chip which can convert changes in physical parameters such as pressure, acceleration, direction (gyro), gas concentrations, or flow rates into variances in electrical parameters. Once a relationship is established between the physical inputs to a sensor and the sensors's electrical properties, a fully integrated transducer can be realized.

The focus of this research is a fully integrated accelerometer. The mechanical transducer for this accelerometer is a small silicon (proof) mass on springs located between two fixed electrodes. As the proof mass moves up or down, there is a variation in capacitance between the mass and silicon plates. By measuring the change in capacitance, the position of the mass can be determined and in turn, the acceleration force placed on the proof mass can be resolved. Taking this design a step further, the position of the proof mass can be converted to a voltage which is then applied to the top and bottom electrodes. The applied voltages place an electrostatic restoring force on the mass. This closed loop architecture comprises the basic design of the forced-rebalanced accelerometer system used in this research.

Parameter	Target Value
Bandwidth	1.0kHz
Input Range	±2g
Resolution	2.0μg

Table 1.1 Target Specifications for Accelerometer

The overall objective of this research was to design, fabricate, and characterize a fully integrated force-rebalanced accelerometer which includes analog signal processing circuits and an analog-to-digital conversion. The major target specifications for the system are given in Table 1.1. Though no specifications were given for power dissipation and die area, both were kept at a minimum without sacrificing the major target specifications given. The accelerometer was designed from the system level in order to pinpoint critical circuits and fundamental limitations on resolution. From there, circuits were designed and fabricated in order to characterize the accelerometer system. The subcircuits of the system include a precision capacitance-to-voltage converter, low noise amplifier, delta-sigma modulator (ADC), and two compensation networks, all designed specifically for this closed loop system. Charles Hsu fabricated the micromechanical system used in the accelerometer in companion research which focused on optimizing the physical sensor and developing the process.

1.1 Motivation

In recent years, research efforts have been growing steadily in the field of integrated microelectromechanical systems (MEMS). The large demand for integrated sensors has been fueled by the strong economic incentive to replace bulky transducers with a more compact integrated version at a lower cost. Earlier work in microelectromechanical sensors focused mainly on the development of silicon diaphragm pressure transducers [1]. One application for the integrated pressure sensor which emerged from early research is

the monitoring of absolute manifold pressure (MAP) in cars. Today, about 20 million low cost integrated pressure transducers are produced annually for this reason alone [2]. This attests to the success of early research efforts as well as the viability of micromechanical sensors in industrial applications.

Today, with airbags in a large portion of the cars currently manufactured, there is a growing demand for low cost accelerometers for use as collision detectors. By placing several acceleration sensors in different locations throughout a vehicle, a microprocessor can determine when a collision has occurred and whether or not airbags should be deployed. Threshold deceleration for airbag deployment ranges from 20g to 50g, depending on the vehicle [3,4]. In addition to collision detection, automotive applications include antilock breaking systems (ABS), four-wheel steering (4WS), and active suspension systems (AS) [3,4]. ABS uses lateral and longitudinal acceleration combined with wheel speed to determine when a tire is skidding. 4WS uses lateral acceleration along with several other variables (speed, yaw rate, steering wheel angle, etc.) to determine steering angles for front and rear wheels. AS uses longitudinal and vertical hub acceleration along with other variables (speed, yaw rate, etc.) to determine active suspension adjustments. Excluding collision detection, most acceleration sensor applications in cars require an input range of ±2g and a bandwidth of 50Hz [4]. Accelerometer applications outside the automotive industry include railway, industrial, medical, and inertial guidance (spacecraft) applications [4-12].

Two examples of industrial uses for accelerometers are platform stabilization and vibration sensing [5]. In railway systems, accelerometers are used to measure the forces placed on passengers during travel as a means of quantifying passenger comfort [7]. Another railway application which has recently emerged for accelerometers has resulted from the development of magnetically levitated ("MagLev") trains [8]. To maintain the levitated train's position safely above the track, an active suspension system is necessary (and not a luxury as with autos). The suspension system of the train is designed as a low-pass filter in order to reject the high frequency track irregularities yet still follow the (low frequency) changes in the track. The active suspension system has several inputs which

include lateral and vertical position, and lateral velocity (recall that position and velocity can be obtained from an accelerometer through double and single integration, respectively).

Because of the miniaturization of accelerometers, they are well suited for medical applications [9]. Reference 9 cited the specific example of measuring voluntary movements of the hand. Another interesting medical application cited in the literature [10] is the placement of matching accelerometers on opposite sides of the heart to measure heart wall velocities, and relative dimensional changes of the heart (it is not clear to the author that this is the optimal sensing method for this application).

Along with the gyro, the accelerometer forms the sensory basis for inertial guidance systems [11]. In an inertial guidance system, a gyro is used to determine the directions while accelerometers are used to detect applied forces. Using single and double integration as with the MagLev trains, velocity and position are determined. In another aerospace application, an acceleration-feedback control system is used in high performance fighter planes [12]. Spurred by these and numerous other applications, research efforts have generated several different integrated accelerometers. No prior research, however, has been able to combine μg-resolution with a bandwidth greater than a few Hertz using micromachining combined with integrated circuit technology.

1.2 Basic Theory

The structure of the micromechanical accelerometer can be characterized by an inertial mass, a spring, and viscous damping as shown in figure 1.1. This simplified model assumes single-degree-of-freedom operation. The spring models the restoring force provided by the four silicon tethers attached to the proof mass while the dashpot models viscous damping from gas (air) surrounding the proof mass. Summing the forces acting on the inertial mass, a relation between input force and displacement can be derived.

$$F_{acc} = M\ddot{x} + B(x)\dot{x} + K_{sp}(x)x \qquad [1.1]$$

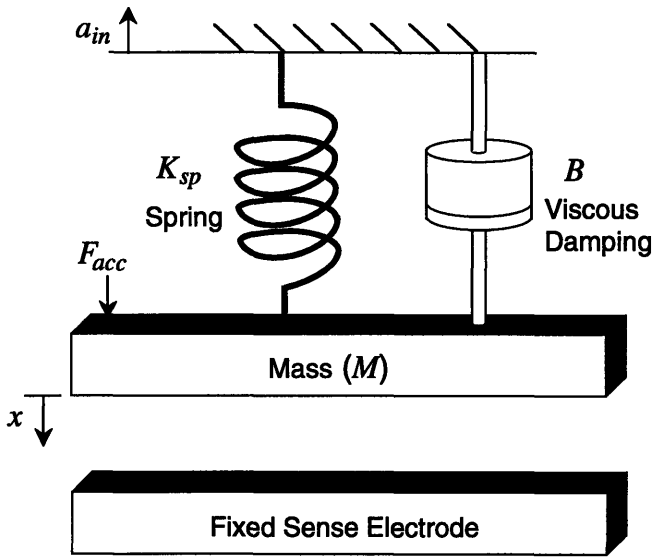


Figure 1.1 Basic mechanical system model

where $F_{acc} = Ma_{in}$[1]. $B(x)$ and $K_{sp}(x)$ represent the viscous damping and spring coefficients, respectively, both of which are nonlinear functions of proof mass deflection. The damping coefficient is approximated by [13]:

$$B(x) = B_o\left[1 + 6\left(\frac{x}{d}\right)^2 + 15\left(\frac{x}{d}\right)^4 \ldots\right] \qquad [1.2]$$

where d is the spacing between the proof mass and sense electrodes. The presence of only even terms reflects the symmetry of the damping about the zero deflection point ($x = 0$). The spring coefficient $K_{sp}(x)$ varies only slightly as a function of x (less than 50ppm nonlinearity [2]) and for now will be modelled as a constant, K_{sp}[2].

The displacement of the proof mass is sensed via the variable capacitance formed between the inertial mass and fixed electrodes. The capacitance sensor can be implemented by either sensing differentially between the upper and lower variable capacitors

1. a_{in} actually refers to the upward acceleration of the inertial reference frame (the chip) to which the silicon tethers are attached. Accelerating the inertial reference frame upward with respect to the proof mass is equivalent to placing a downward force Ma_{in} on the proof mass and holding the inertial reference frame constant (see figure 1.1). When "acceleration force" is used to describe an input to mechanical system, this is the force that is being described.
2. The effects of nonlinearities in damping and spring force as well as secondary resonant modes of the mechanical structure will be addressed later and are omitted here to simplify explanation of the basic system.

or by sensing differentially between the variable sense capacitors and fixed reference capacitors. The reference capacitors are formed by fabricating a structure identical to that of the mechanical system except using very short silicon anchors instead of flexible silicon tethers like the mechanical system. The short silicon anchors hold a reference mass immobile producing a fixed capacitance. Because the structures are fabricated nearly identically, the capacitance values should match well even with process variation.

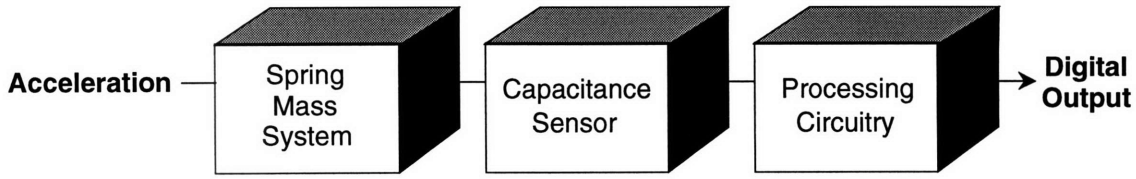


Figure 1.2 Open loop system

As a first pass at implementing the accelerometer, the open loop system shown in figure 1.2 was considered. The position of the mass is determined via a capacitance sensor which is then followed by processing circuitry which outputs the measured acceleration as a digital word. This approach has the benefit of low system complexity but has several drawbacks including limited dynamic range and accuracy.

First, in an open loop system, a fundamental tradeoff exists between sensitivity and dynamic range. Reducing the spring stiffness of the mechanical system will increase the deflection of the proof mass for a given input and thus increase the overall accuracy of the acceleration measurement. However, because a smaller input acceleration causes the proof mass to deflect the full gap distance, the dynamic range will be lowered. In an open loop system, this tradeoff cannot be avoided. Secondly, the accuracy of the open loop system is limited by nonlinearities. Since there is no mechanism to stabilize the proof mass near its equilibrium position, variations in damping and spring force over a large range of proof mass deflections prevent a high resolution measurement. Lastly, there is no simple conversion between deflection of the proof mass and applied acceleration force. Along with the current deflection of the proof mass, the current velocity and acceleration of the proof mass with respect to IC's internal reference frame must also be known to determine

the acceleration force placed on the mechanical system (equation 1.1). Thus, even though the system complexity is low, design of the processing circuitry is quite a task.

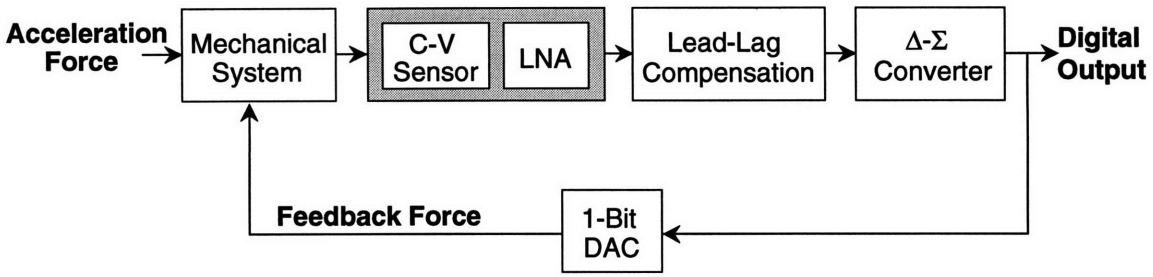


Figure 1.3 Closed loop system

An improved topology for the accelerometer is the closed loop, force-balanced system shown in figure 1.3. The deflection of the proof mass is now given by

$$F_{acc} - F_{FB} = M\ddot{x} + B(x)\dot{x} + K_{sp}x \qquad [1.3]$$

In a perfect closed loop system, F_{FB} exactly cancels F_{acc} forcing the proof mass to remain in its equilibrium position and thereby eliminates all nonlinearities from the system. The actual deflection of the proof mass is reduced by the gain of the loop. Because the proof mass deflection is now decoupled from the input acceleration, the open loop tradeoff between sensitivity and dynamic range is removed.

As with the open loop system, deflection of the proof mass is sensed capacitively. A differential sense is employed between either the two variable capacitors located above and below the proof mass or between the variable capacitors and fixed reference capacitors. Note the LNA in figure 1.3 is not a separate amplifier in series with the capacitance-to-voltage converter, rather it represents the effective gain of the C-V sensor which is used as a mechanism for adjusting the loop gain and thus setting the dynamics of the closed loop system[3].

Lag (pole-zero) compensation is placed in the loop to ensure a high loop gain and minimal movement of the proof mass from its equilibrium position. A large negative

3. The system dynamics are discussed in section 3.2. The implementation of the C-V sensor is detailed in section 4.3.

phase shift from the mechanical system coupled with negative phase shift from other elements in the loop make lead (zero-pole) compensation necessary to maintain a stable closed loop system.

A delta-sigma (Δ-Σ) modulator is used to convert the analog signals coming from the output of the compensation network into a high frequency bit stream. The Δ-Σ modulator is well suited for this system for two reasons: its noise "shaping" characteristic and its binary output. The Δ-Σ modulator places most of the quantization noise (which results from the analog-to-digital conversion) at high frequencies well above the bandwidth of interest while suppressing low frequency noise which would show up in baseband. The high frequency bit stream is then passed through a decimation filter (not shown in figure 1.3) which removes out of band noise. Because the output of the modulator takes on only one of two values, high linearity is ensured in the third order modulator while greatly simplifying the feedback circuitry.

The feedback force necessary to close the loop is generated by the fixed electrodes placed above and below the proof mass as shown in figure 1.4. The twin electrodes are used together to place an electrostatic restoring force on the proof mass as follows: The electrostatic force between two parallel plates of area A and with a differential voltage V is given by

$$F_{ES} = \frac{\varepsilon_o A}{2}\left(\frac{V}{d}\right)^2 = \frac{1}{2}\frac{C}{d}V^2 \qquad [1.4]$$

where d is the separation of the two plates.

Though electrostatic force is a nonlinear function of voltage, the feedback can be approximately linearized by charging the electrodes with a DC bias, V_{DC}, plus a differential voltage, V_{DIFF} [1]:

$$F_{FB} = \frac{\varepsilon_o A}{2}\left(\frac{V_{DC}+V_{DIFF}}{d+x}\right)^2 - \frac{\varepsilon_o A}{2}\left(\frac{V_{DC}-V_{DIFF}}{d-x}\right)^2 \qquad [1.5]$$

where x gives the deflection of the proof mass from its equilibrium position. The output bit stream from the Δ-Σ modulator determines the sign of V_{DIFF} while the magnitude is held constant.

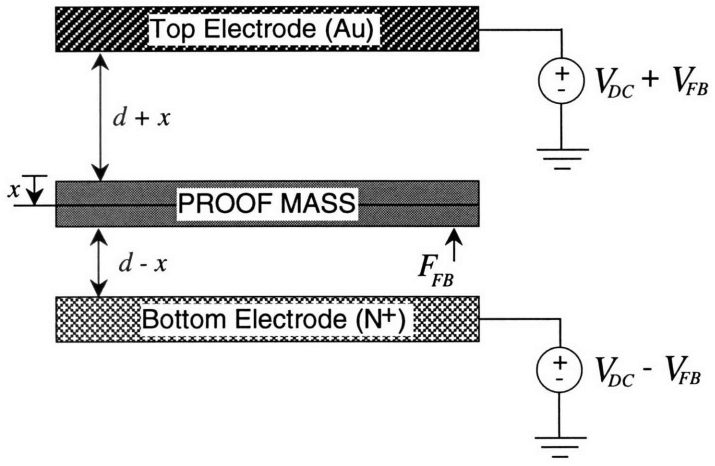


Figure 1.4 Electrostatic force feedback

Taking the Taylor expansion of equation 1.5,

$$F_{FB} \approx \frac{2\varepsilon_o A}{d^2} V_{DC} V_{DIFF} \left[1 - \frac{V_{DC}^2 + V_{DIFF}^2}{V_{DC} V_{DIFF}} \left(\frac{x}{d} \right) + 3 \left(\frac{x}{d} \right)^2 \ldots \right] \qquad [1.6]$$

For small deflections from equilibrium ($x \approx 0$), equation 1.6 can be approximated by

$$F_{FB} \approx \frac{2\varepsilon_o A}{d^2} V_{DC} V_{DIFF} \qquad [1.7]$$

Another possible method of charging the feedback electrodes which was considered was through the use of a "charge dump" [14]. Re-examining equation 1.4:

$$F_{ES} = \frac{\varepsilon_o A}{2} \left(\frac{V}{d} \right)^2 = \frac{1}{2\varepsilon_o A} \left(\frac{\varepsilon_o A}{d} \right)^2 V^2 = \frac{Q^2}{2\varepsilon_o A} \qquad [1.8]$$

Thus, by placing a "fixed packet" of charge on the feedback electrodes instead of a fixed voltage, the positional dependance of the feedback force is removed. The accuracy of this charge-based feedback scheme is, however, limited by the presence of parasitic capacitance in parallel with the top and bottom electrodes as shown in figure 1.5. The parasitic capacitors split the applied charge, Q, with the nominal feedback capacitance which results in an error in the applied force. Moreover, because the sense capacitance varies with deflection of the proof mass, the feedback error is signal dependant. As with any sig-

nal dependant error, harmonic distortion will be seen at the output of the accelerometer. For these reasons, the charge based feedback method was not used.

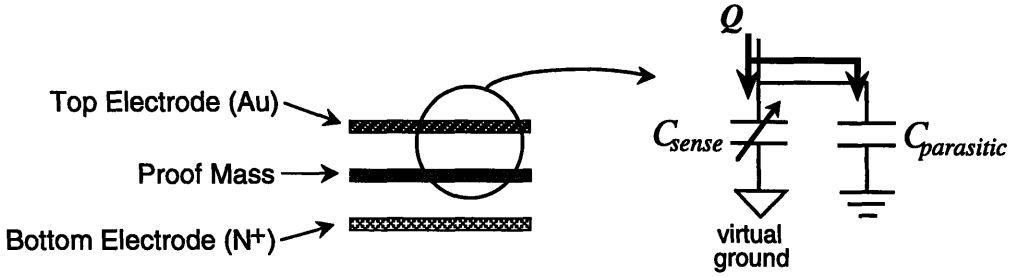


Figure 1.5 Charge-based force feedback

Since the upper and lower electrodes serve the dual purpose of sensing the deflection of the proof mass as well as applying a feedback force to center the mass, the two functions must be time-multiplexed. A two-phase nonoverlapping clock is used to regulate the charging of the fixed electrodes. Since the feedback force is only applied for a fraction of a clock cycle, equation 1.7 must be changed to reflect the average force applied over one clock cycle.

$$F_{FB} \approx \eta(\Phi_1)\frac{2\varepsilon_o A}{d^2}V_{DC}V_{DIFF} \qquad [1.9]$$

where $\eta(\Phi_1)$ is the ratio of time the feedback force is applied (~0.5).

In addition to the feedback loop described above, there is a secondary feedback loop which is necessary to center the proof mass at startup and after out of range input excursions. Upon startup, the proof mass will likely be a relatively large distance from its equilibrium position. When this happens, the linearized model used to design the closed loop system is no longer valid. As a result, nonlinearities[4] in the loop can cause instability. A secondary feedback loop is thus necessary to bring the proof mass close enough to its equilibrium position such that the primary feedback loop can be switched in and assume stable operation[5].

4. A Δ-Σ modulator uses a comparator to generate its output bit stream. A linearized model for this comparator was used to design the Δ-Σ modulator as well as the full closed loop system. This linearized model, however, relies on having only small excursions of the proof mass from its equilibrium position. This is detailed extensively in sections 3.4 and 3.5.

1.3 Previous Work

In response to the large demand for low cost, high precision accelerometers, several integrated sensors have been designed, built, and tested [1,3,5,6,14-16]. Reference 15 implemented a bulk micromachined accelerometer using a flexible bar supporting an inertial (proof) mass between two fixed electrodes. The two electrodes and inertial mass form a capacitive divider which was used for position sensing and the application of electrostatic rebalance force. The accelerometer was configured as an electromechanical delta-sigma modulator, exploiting the high linearity of delta-sigma modulation and the simplicity of digital feedback. Correlated double sampling and an analog calibration algorithm were used to reduce noise and offset. The paper reported a resolution of 15.3 bits (1g, full scale). The system was bandlimited to 5Hz to remove the effects of Brownian noise and thus achieve its high resolution. Reference 5, also utilizing a cantilever beam with capacitive position sense, reported a resolution of better than 1μg but was also highly bandlimited (1Hz). Reference 3, which describes the ADXL50 surface micromachined accelerometer, used an analog servo loop to center its proof mass. Because of its relatively high bandwidth (1kHz) and small inertial mass, this accelerometer proved to be particularly susceptible to the effects of Brownian noise. This was evidenced by the relatively low resolution (0.12g, 50g full scale) of the accelerometer. The mechanical noise could be greatly reduced by bandlimiting the signal to a few Hz as was done in references 5 and 15.

Reference 14 sealed a proof mass in a vacuum to obtain a high-Q resonant mechanical system and eliminate nonlinearities due to viscous damping. The mechanical structure was formed by bonding three 500μm wafers together; The center wafer formed the proof mass and the top and bottom wafers contained sense and feedback electrodes. Though promising results were given for the functionality of the mechanical structure alone, no results were given for the closed loop system

5. See section 3.5.

Along with reference 15, references 1 and 14 also implemented the accelerometer as a second order delta-sigma modulator. The implementation in reference 15 differs from that of references 1 and 14 in that it uses only one mechanical integrator as opposed to the two mechanical integrators used in references 1 and 14. Reference 15 effectively removed one mechanical integrator by heavily overdamping the mechanical system. Thus, one pole of the mechanical system was placed well above the system bandwidth. An electrical integrator was added to the system to replace the mechanical integrator which was effectively removed. The benefit of having only one mechanical integrator is the elimination of the need for compensation to stabilize the closed loop system. The significant disadvantage of this scheme is the Brownian noise associated with the large increase in viscous damping.

Integrated accelerometer systems are not limited to the sensing and feedback schemes described above, reference 6 used a pulse width modulated (PWM) electrostatic feedback to stabilize an inertial mass. Reference 16 (along with many other integrated accelerometers) used no feedback at all.

Along with capacitive transducers, piezoelectric sensors have been frequently used in vibration measurement which requires low sensitivity and high bandwidth [5]. A capacitive sensor, however, is better suited for high accuracy, low bandwidth applications due to its high precision, low drift, and better temperature performance [5,17].

CHAPTER 2

The Sensor

There are three main approaches to fabricating a microaccelerometer, bulk micromachining, surface micromachining, and wafer bonding. Each approach has its advantages and disadvantages. This chapter briefly describes surface micromachining and bulk micromachining, giving the pros and cons of each, then goes on to detail the wafer bonded structure which is used in this research. The process for the accelerometer is given along with its incorporation into a standard IC process flow. This is followed by a discussion of the mechanical properties of the accelerometer. Nominal values are given for the mechanical and electrical characteristics of the sensor along with tolerances and other limitations important to the overall system design.

2.1 Bulk Micromachining

Bulk micromachining uses a backside etch to free a mechanical structure (proof mass and tethers) from the substrate. The inertial mass thickness typically ranges from 10μm to 25μm. An example bulk micromachined accelerometer is shown in figure 2.1.

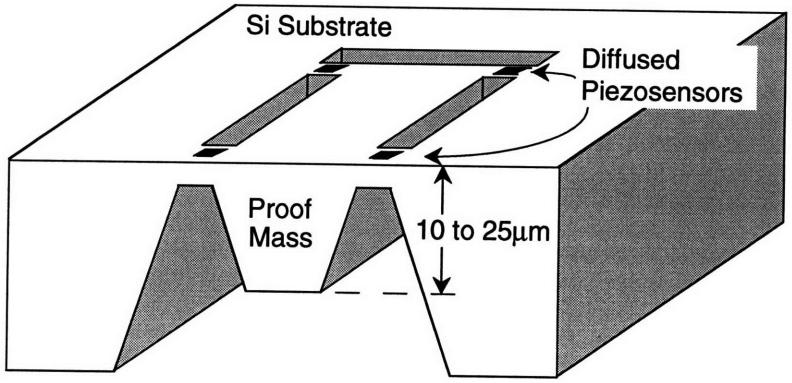


Figure 2.1 Bulk micromachined accelerometer

Here, the acceleration sense in achieved using diffused piezoelectric sensors. The main benefit of a bulk micromachined accelerometer is the use of single crystal silicon, desirable in mechanical structures due to its lack of residual stress. Drawbacks to bulk micromachining include: incompatibility with standard IC process flow, necessary IR alignment and backside etch, processing dependance on wafer thickness, and the large area of silicon required by the sensor (6-16mm^2,typical) [3,18].

2.2 Surface Micromachining

In contrast to bulk micromachining, surface micromachining uses materials deposited on the top surface of the wafer, usually with a low pressure chemical vapor deposition (LPCVD), to form a mechanical structure [1]. To fabricate a surface micromachined accelerometer, the proof mass is first dry etched from a thin film deposition of polysilicon. A sacrificial oxide (or phosphosilicate glass (PSG) [1]), is then wet etched from under the polysilicon to free the inertial mass [3]. The typical thickness of a surface micromachined proof mass ranges from 2μm to 5μm. The side view of a surface micromachined accelerometer is shown in figure 2.2.

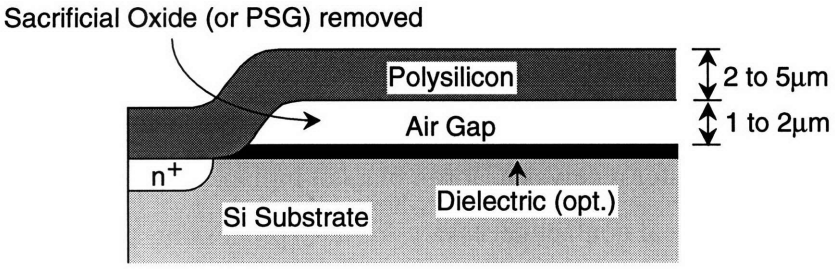


Figure 2.2 Surface micromachined accelerometer

The proof mass and springs (not apparent in the side view) are etched from the polysilicon layer above the air gap. Electrical contact is made with the proof mass at the anchor point to the substrate. The inclusion of a dielectric layer separating the air gap and substrate is optional and varies between accelerometers.

Surface micromachining has many advantages over bulk micromachining. No longer necessary are the IR alignment, backside etch, and large die area needed for bulk micromachining and surface micromachining is fully compatible with a standard IC process flow[6][18]. However, there are some disadvantages to surface micromachining. During the wet oxide etch used to free the proof mass, the mass can stick to the underlying dielectric (or substrate). The residual stress associated with the polysilicon make it difficult to predict the mechanical properties of the film [18].

2.3 The Wafer Bonded Sensor

Wafer bonding combines the advantages of both surface micromachining and bulk micromachining to form a mechanical structure well suited for the accelerometer. The processing for the mechanical sensor is given next followed by the accelerometer's final structure and mechanical and electrical properties[7].

6. Some modification of the CMOS flow must occur.
7. For more information on the process flow and mechanical structure, see references 19, 20, and 21.

2.3.1 Process Flow [18-21]

The processing steps for fabricating the accelerometer are shown in figure 2.3. Processing begins with two wafers, a p-Si handle wafer and a p/n device wafer. The device wafer was formed by growing n-Si epi layer on a p-type substrate to a thickness of 10-11μm. The handle wafer receives a Boron blanket inplant to heavily dope its backside. This ensures good electrical contact necessary for later processing steps. A plasma etch is used to form a 1-2μm trench on the topside of the handle wafer. A diffused junction-isolated electrode is created in the trench using a phosphorous implant with drive-in.

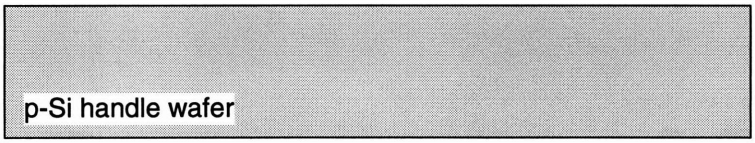
Next, the p-Si handle wafer and p/n wafer are bonded together in a controlled Oxygen ambient forming a p-n-p wafer "sandwich" (figure 2.3d). The upper p-Si (formerly of the p/n wafer) is then removed using a two step process. The wafer is first ground back about 400μm and polished. Afterwards, an electrochemical etchback (KOH) is used to remove the remaining p-Si above the n-Si epi layer.

At this point, the n-epi and p-Si substrate form a sealed cavity wafer. The wafer is now compatible with standard IC processing. Any circuits necessary to implement the sensor could be added at this processing stage[8]. Only low temperature processing steps remain to free mechanical structures from the n-epi layer.

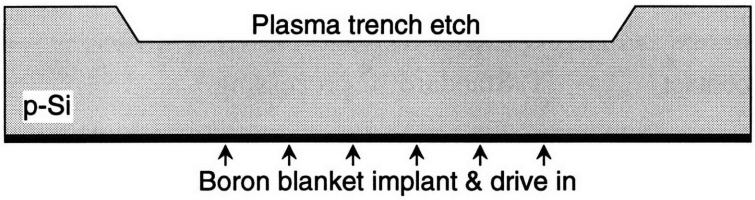
Once the standard IC processing has been completed, the mechanical structures (proof mass and springs) are freed using a deep plasma etch into the n-type silicon. A "capping" wafer, formed from either glass or Si, is attached above the n-Si using a thermocompression bond between Au electroplated on the upper wafer and Au deposited over Cr/SiO_2 on the n-type silicon. The upper wafer is used to position the top electrode above the proof mass.

Wafer bonding has all the benefits of surface micromachining (no backside etch, IC process flow capability, no IR alignment) while it avoids the problem of stiction by using a dry etch to free the inertial mass. Because the mechanical structure is formed with single crystal silicon, the problem of residual stress is also alleviated.

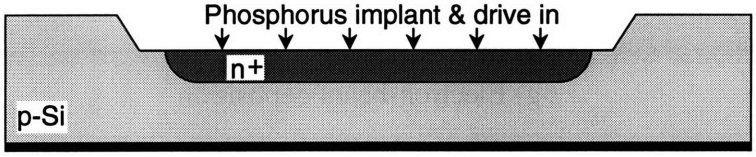
8. In this research, the processing circuits and mechanical sensor were stitch-bonded together side by side in order to test the mechanical structure, electronic processing circuitry, and overall system design. The next goal of continuing this research would be to incorporate mechanical structures and processing circuitry monolithically.



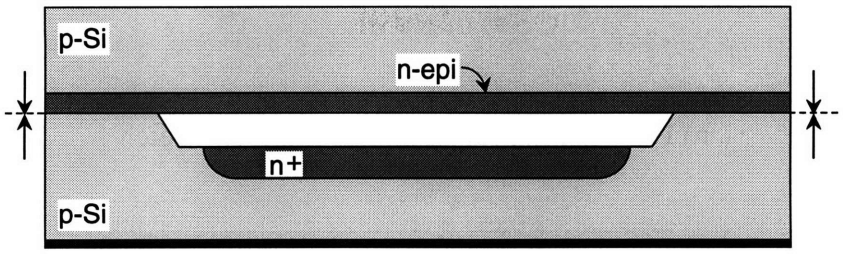
a) p-silicon "handle wafer"



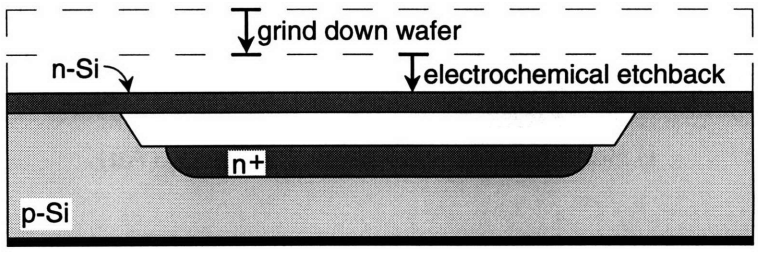
b) Trench etch and backside contact



c) Junction-isolated electrode

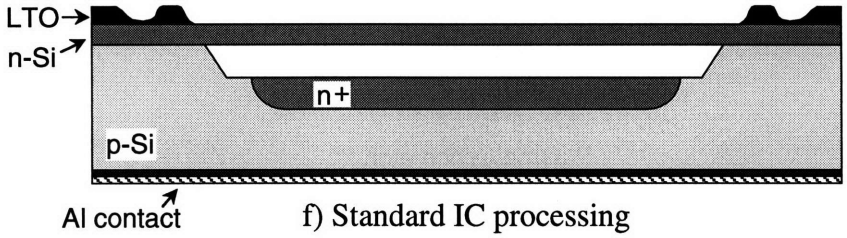


d) Bond device (p/n) wafer to handle (p-Si) wafer

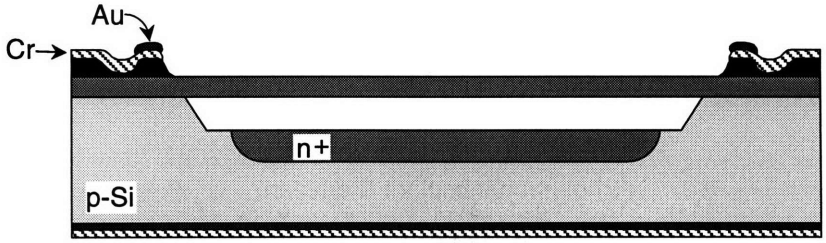


e) Remove p-silicon from device wafer

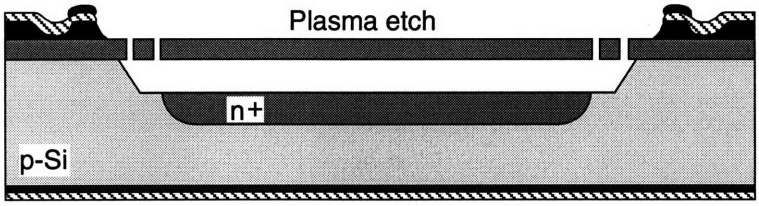
Figure 2.3 Accelerometer process flow



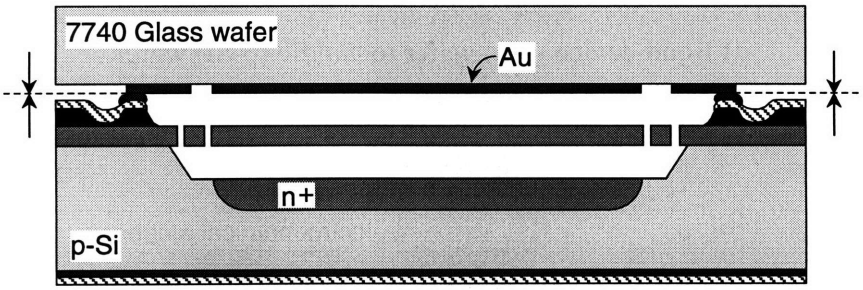
f) Standard IC processing



g) Electron-beam deposition



h) Free mechanical structure with plasma etch



i) Bond glass wafer with top electrode (Au)

Figure 2.3 (cont'd) Accelerometer process flow

2.3.2 The Mechanical Structure

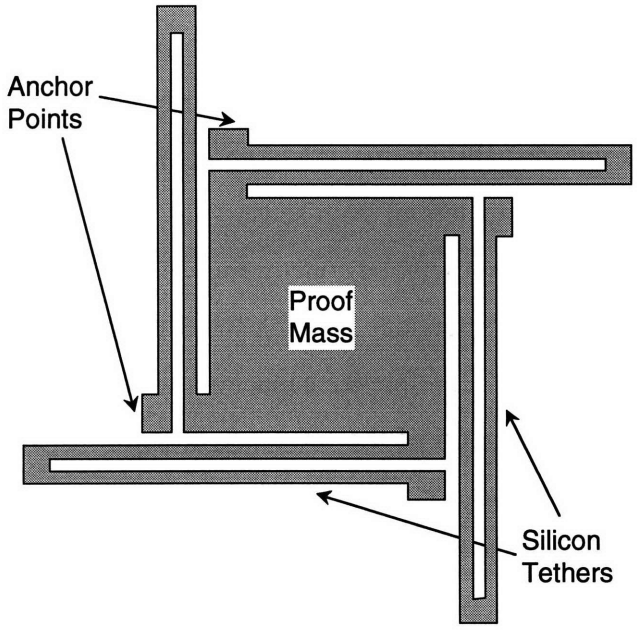


Figure 2.4 Top view of accelerometer

A sideview of the final mechanical structure is shown in figure 2.3i. The sideview shows the proof mass and springs, formed from the n-Si epi layer, and the top and bottom fixed electrodes, formed from metal and diffused n^+ regions, respectively. A top view of the structure, shown in figure 2.4, shows the n^+ region of the mechanical structure comprising the proof mass and springs (silicon tethers). The "pinwheel folded tether" configuration[9] of the silicon tethers (springs) is used for its high linearity (three orders of magnitude better than a simple straight tether design) and reduced device dimensions [2]. The pinwheel configuration also relieves in-plane residual stress [2]. This, however, is not a consideration as single crystal silicon is used to fabricate the proof mass and springs.

9. Though the accelerometer was initially designed as a "folded pinwheel" structure, it was later changed to a "simple pinwheel" structure to optimize the placement of secondary resonance modes of the mechanical system. This is discussed in Chapter 5.

2.3.3 Mechanical and Electrical Properties of the Sensor

Two different mechanical sensors were fabricated for use in the accelerometer, one having a 750μm×750μm×10.8μm proof mass, the other proof mass having dimensions of 500μm×500μm×10.8μm. Other than having different lateral dimensions, the two mechanical structures are virtually identical[10]. The device characteristics which set the mechanical and electrical parameters of both sensors, as well as the tolerances for each, are the same. Thus, they will be discussed concurrently. The target dimensions, mechanical response, and electrical characteristics for each structure are given in table 2.1.

As discussed in section 1.2, reference capacitors were fabricated side-by-side with the mechanical sensor. Fabrication of the reference structure is identical to that of the micromechanical structure except for the use of very short silicon anchors to support the proof mass. The fixed reference capacitors can be thought of as a mechanical structure with an infinite spring constant preventing the proof mass from moving in response to applied acceleration force. The side-by-side fabrication of the structures is done to ensure close matching between the device parameters of the mechanical sensor and reference structure (including parasitics[11]). The "matching" tolerances given in table 2.1 refer to matching between the mechanical sensor and the fixed reference structure.

The tolerances given in table 2.1 can be a major limitation on the accuracy of the accelerometer. Taking each tolerance into account is an important part of the design process both at the system level and at the circuit level. Next, a brief discussion is given of the physical mechanisms which set the tolerances of the sensor along with a more detailed discussion of what mechanical parameters were variables during the system level design.

Structural dimensions

As will be discussed in section 3.3, a large proof mass is always desirable from the system design standpoint. The p/n (epi) device wafers used to fabricate the proof mass were obtained from Motorola and were delivered with an n-epi thickness specified at

10. The mechanical resonant frequencies of the two structures are placed at different frequencies to facilitate electrical resonance tuning which will be described in section 3.3.

11. Matching parasitics are necessary to help cancel substrate noise. See section 4.3.2.

Parameter	Structure 1	Structure 2	Tolerance
STRUCTURAL DIMENSIONS			
Proof mass dimensions	750μm×750μm ×10.8μm	500μm×500μm ×10.8μm	±7.5μm (length) ±0.2μm (10.8μm)
Gap spacing	1.0μm	1.0μm	±0.1μm (absolute) ±100Å (matching)
Electrode dimensions	730μm×730μm	480μm×480μm	±2.0μm (absolute) ±0.5μm (matching)
DYNAMICS			
Resonant Frequency	3.23kHz	6.78kHz	±20%
ELECTRICAL CHARACTERISTICS			
Sense/Feedback Capacitance	4.716pF	2.039pF	±0.54pF (Struct.1) ±0.11pF (matching) ±0.24pF (Struct.2) ±0.05pF (matching)
Parallel Stray Capacitance	<<10fF	<<10fF	
Resistance to Electrodes	<10Ω	<10Ω	
Resistance to Proof Mass	~500Ω	~500Ω	

Table 2.1 Design specifications for the mechanical sensor

10.8μm±0.2μm. Thus, the thickness of the proof mass was not a design parameter. The area of the proof mass was restricted due to concern about warpage of the proof mass as well as the desire to limit the die area of the sensor. During the system level design, it was not known whether a 750μm×750μm proof mass would have significant warpage, however, it was known that a 500μm×500μm proof mass displayed no measurable warpage[12]. For this reason, both sized mechanical structures were fabricated for the accelerometer.

12. Also, less than 300Å surface roughness was measured for the 500μm×500μm proof mass [18].

The ±7.5μm tolerance for the sides of the proof mass are a result of the isotropic etch used to free the mechanical structure.

The lower gap spacing (between the proof mass and diffused n^+ electrode) is set by a plasma trench etch into the handle wafer. Because of the possibility of over or under-etching the trench, the absolute tolerance for the gap was conservatively set at ±0.1μm. The matching tolerance between the mechanical structure and reference is an order of magnitude better (±100Å). The upper gap spacing is controlled by three processing steps: a low temperature oxide (LTO) deposition followed by an electron beam (e-beam) deposition of Cr, then Au. The nominal thickness of the LTO is 5000Å (±200Å with process variations). The thickness of the Cr-Au (combined) layer is also set at 5000Å (±200Å) resulting in a overall tolerance of ±0.04μm for the upper gap spacing. From the system design viewpoint, the gap separation should be minimized to maximize the gain of the C-V sensor[13]. However, because of the tolerances of the gap spacing, a practical limit is set on the minimal gap size. The 1.0μm gap spacing was selected to keep any matching error between the sense capacitors and reference capacitors below 2.5% of the nominal capacitance value.

The accuracy in sizing the lower diffused (n^+) electrode is limited by lateral diffusion during the drive-in step. The upper (Au) electrode is patterned with a single 1× Cr-mask alignment step and will probably exhibit much better control over the electrode dimensions than the ±2.0μm tolerance of the lower diffused electrode. Note that the upper and lower electrodes are sized 20μm smaller on a side than the proof mass. This is done for three reasons. First, by making the electrodes smaller than the proof mass, the capacitance is desensitized to changes in the lateral position of the proof mass. Thus, any undesired lateral resonances or movement in the proof mass will not result in a sense capacitance change. Secondly, because the proof mass area is larger than that of the upper and lower electrodes, it prevents capacitive feedthrough between the two electrodes. Lastly, because the sizing of the upper and lower electrodes can be controlled more precisely than the area of the proof mass, the electrodes should be used to set the values of

13. See section 3.2.3.

the parallel plate capacitances. Thus, the ±2.0μm (per side) tolerance of the electrodes sets the limitations of the capacitance accuracy and not the larger ±7.5μm tolerance of the proof mass.

Dynamics

In section 1.2, the response of the mechanical system to an input force was given as

$$F_{net} = M\ddot{x} + B(x)\dot{x} + K_{sp}x \qquad [2.1]$$

where F_{net} is the acceleration force less any feedback forces applied, and $B(x)$ and K_{sp} are the nonlinear damping and spring force terms, respectively. From a design standpoint, the mechanical system can best be thought of as a low pass filter[14]. Modelling equation 2.1 in the frequency domain, approximating $B(x)$ as a constant:

$$\frac{X(s)}{F(s)} = \frac{1}{Ms^2 + Bs + K_{sp}} = \left(\frac{1}{M}\right)\frac{1}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \qquad [2.2]$$

where $\omega_o = \sqrt{K_{sp}/M}$.

Examining equation 2.2, the response of the mechanical system has two poles which "roll off" the mechanical response above ω_o (the mechanical resonant frequency) at a rate of 40dB/decade. The placement of ω_o, critical in the design of the accelerometer[15], is set by the spring constant, K_{sp}, and mass, M, of the spring-damped-mass system.

The mass, M, can be calculated from the volume of the proof mass and density of silicon (2.33 g/cm^3) with some error resulting from the nonzero mass of the springs. The spring constant, K_{sp}, is set by the length and shape of the silicon tethers. Qualitatively, the predominant mechanism for controlling the spring constant is by varying the dimensions of the two long thin sections of silicon in each tether (figure 2.5, sections 1 & 2). Tether sections 3, 4, and 5 also contribute to the effective spring constant, however, they are all

14. See mechanical sensor dynamics, section 3.2.1.
15. See electrical resonance tuning, section 3.3.1.

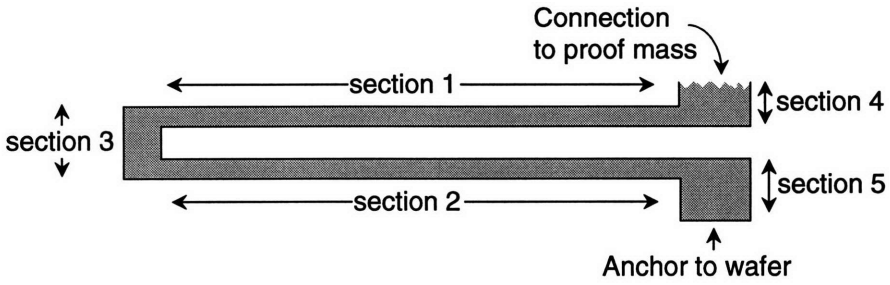


Figure 2.5 Single silicon tether

relatively "stiff" with respect to the long sections of tether. The spring constant for a single straight section of tether is given by [2]:

$$K_{eff} = \frac{4Ebt^3}{l^3} \qquad [2.3]$$

where E is the modulus of elasticity, b is tether width, t is tether thickness, and l is tether length. Though it is a huge oversimplification to calculate the folded pinwheel tether spring constant as just two straight tethers in series[16], equation 2.3 lends qualitative information which justifies the shape of the silicon tethers. To decrease the spring constant, K_{sp}, both the tether width (b) and thickness (t) should be increased while the tether length (l) should be increased. Likewise, to increase the spring constant, increase both b and t and decrease l.

There is a practical limitation on how low the spring constant, and thus, resonant frequency of the mechanical system can be placed which must be taken into account during design of the mechanical sensor. The tether thickness, t, is already set by the n-epi layer (10.8μm) in the device wafer[17]. Decreasing the width of the silicon tethers below a certain point has two practical limitations: First, the proof mass has to be "stiff" to lateral accelerations and second, the electrical connection resistance to the proof mass must be kept below a reasonable value. Both the lateral deflection of the mechanical sensor and the electrical resistance of the tethers are inversely related to the tether width. Increasing

16. See reference 2 for a detailed analysis of the spring constant calculation.
17. Etching the tethers to reduce the width would be impractical because the etch could not be controlled precisely enough to regulate the spring stiffness to within an acceptable tolerance.

the length of the silicon tethers has a practical limitation because of the electrical resistance of the tether. It was decided, due to circuit implementation issues, the electrical resistance of each tether should be limited to 2kΩ providing a 500Ω connection to the proof mass with four tethers in parallel. As a result, resonant frequencies below 2.0kHz were not an option from the system design standpoint.

In the actual design of the mechanical sensor, FEM analysis was used to predict the resonant frequency of the mechanical structure. The measured resonant frequencies of the mechanical sensor displayed matching to within 5% of the FEM calculated values [19]. Thus, the ±20% tolerance used for the system design (table 2.1) was quite conservative.

In equation 2.2, both the spring coefficients, $K(x)$, and damping term, $B(x)$, were approximated by constant terms. As was previously discussed, both the damping and spring force have higher order terms. The spring force is highly linearized by the pinwheel folded tether design shown in figure 2.4. However, there is still a second order nonlinearity on the order of 10ppm for the spring "constant" [2]. This nonlinearity would be much larger (on the order of 50-100ppm) if it were not for the force feedback which greatly limits the deflection of the proof mass. The damping nonlinearity (equation 1.2), like the spring nonlinearity, is kept quite small because of the force feedback stabilization of the proof mass. The effects of the damping and spring nonlinearity on the accelerometer performance are investigated in section 3.4.3.

To this point, the discussion of dynamics has been limited to the fundamental resonance of the mechanical system. Equation 2.2, used to model the second order response of the sensor, models only single degree of freedom movement (up and down in figure 2.3, in and out of the page in figure 2.4). In actuality, the proof mass has several secondary resonances which include responses to torque and lateral acceleration [18,22]. The lateral resonance modes are at very high frequencies and can be ignored for all practical purposes in the system design. The torsion mode resonances[18] are at lower frequencies which can

18. As low as 2.5× the fundamental frequency [18].

affect the performance of the accelerometer. The possible effects of these resonances on system performance are discussed in section 3.6.

The first order gas damping term, B, between two square plates can be calculated analytically using [2]

$$B_o = 0.4217 \frac{\mu L^4}{d^3} \qquad [2.4]$$

where μ is the viscosity of the gas (air) surrounding the plates, L is the plate length, and d is the gap separation. Evaluating equation 2.4 using the viscosity of air at 1 atmosphere pressure, the mechanical system is highly overdamped. From a system design standpoint, it is preferable to have the damping term as small as possible[19] to reduce Brownian noise, as discussed next.

Brownian Noise

Brownian noise, the mechanical equivalent to Johnson (thermal) noise, can be the limiting factor in determining the resolution of a small device geometry sensor. Brownian noise is the direct result of molecular collisions with a gas or liquid surrounding the proof mass [23]. The large discrete accelerometers which preceded the current integrated micromechanical sensors were not limited in resolution by Brownian noise due to their sizable mass. However, as device dimensions have moved to smaller scales, the forces from molecular collisions can no longer be ignored. Using the Equipartition Theorem and Nyquist Relation, input referred Brownian noise force is given by [23]:

$$\overline{F_{brwn}} = \sqrt{4k_B TB} \qquad \text{N}/\sqrt{\text{Hz}} \qquad [2.5]$$

where k_B is boltzmann's constant, T is absolute temperature, and B is the damping coefficient. Solving for the input referred acceleration noise:

$$\overline{a_{brwn}} = \sqrt{4k_B TB}/M \qquad (m/s^2)/\sqrt{\text{Hz}} \qquad [2.6]$$

19. It is, however, more difficult to stabilize the closed loop system with a highly underdamped mechanical system. See section 3.3.1. Also, it is more likely that undesired secondary resonance modes will be excited as damping is decreased.

where M is the mass of the proof mass.

From equation 2.6, the input referred acceleration noise can be decreased either by increasing the size of the proof mass or decreasing the damping. Increasing the size of the proof mass is not a viable option for the aforementioned reasons, thus decreasing the mechanical damping must be investigated.

One possible method for decreasing the damping of the mechanical structure is to perforate the proof mass [2]. Using this approach, the damping coefficient can be lowered to approximately 5μNs/m which corresponds to a slightly underdamped mechanical system. Further perforations necessary to reduce the damping would compromise the integrity of the mechanical structure [18]. Using the proof mass dimensions from table 2.1 and a bandwidth of 1.0kHz, equation 2.6 predicts an input referred acceleration noise on the order of 1.0mg (1×10^{-3}g), about three orders of magnitude above the 2.0μg target resolution of the accelerometer.

To lower the mechanical damping further and keep the same device geometry, it is necessary to vacuum seal the mechanical structure. In a vacuum sealed accelerometer structure, a quality factor, Q, on the order of 50,000 can be attained [13]. In a vacuum, the damping is no longer controlled by the viscosity of the gas (or fluid) surrounding the proof mass. Instead, the damping is controlled by internal damping of the springs and supports.

The damping term in equation 2.6 is meant to apply to only viscous damping. If only the viscous damping term were used to calculate the brownian noise of the proof mass placed in a vacuum, the noise floor would be well below 2.0μg. However, because the mechanisms which control the internal damping of the springs and supports are similar to that of viscous damping, the total damping constant (including the internal damping) is used in equation 2.6 as a conservative estimate. This resulting noise floor is 2.21μg.

Electrical characteristics

In order to facilitate sensing the deflection of the proof mass, the sense capacitance should be as large as possible (see equations 4.28-4.30). Fortunately this coincides with the desire to have the proof mass as large as possible to reduce input referred noise. As previously discussed, the gap spacing was set at 1.0μm to maximize the sense capacitance

without incurring a capacitance matching error greater than ±2.5%. Also recall that the 500μm×500μm and 750μm×750μm proof masses were limited in size to prevent possible warpage of the device wafer. The gap spacing and area constraints combine to define the nominal sense capacitance. Combining the accuracy limitations on the area of the fixed electrodes with the gap matching tolerance, the tolerance of the sense/feedback capacitance was calculated.

Other electrical parameters of interest are the series resistance to the upper and lower electrodes and the previously discussed series resistance to the proof mass (500Ω). Unlike the electrical connection to the proof mass, the connections to the upper and lower electrodes are Au and diffused n^+, respectively, resulting in low contact resistance (<10Ω).

Along with the resistance of the tethers, the mechanical sensor has other undesirable electrical characteristics which must be taken into account. As with any integrated electronics, parasitic capacitances exist at each node, either to ground, to the substrate, or to another node in the circuit. These parasitics are summarized in figure 2.6. Switched capacitor techniques can be used to cancel the effects of the parasitics to ground (C_{p1}, C_{p2}, & C_{p3}) [24]. Similarly, the effects of C_{p6} and C_{p8} can be removed by charging the top and bottom electrodes to ground or virtual ground. In section 4.3, a technique is given to remove the effects of C_{p7}, a parasitic capacitance from the substrate to the proof mass. There is no circuit technique to cancel the effects of capacitors C_{p4} and C_{p5} which are in parallel with the sense/feedback capacitors. C_{p4} and C_{p5} are the result of metal and poly lines crossing which connect to the proof mass, bottom and top electrodes. With careful layout, however, the parasitics can be minimized[20].

One last electrical characteristic which should be mentioned is the reverse leakage current of the diffused lower electrode. Because the n^+ diffused electrode is junction isolated, there is a small reverse bias leakage current associated with the junction (~12.5pA). Though this is a fairly small current, it must be taken into account when designing the

20. Extracting from the layout, both C_{p4} and C_{p5} are estimated to be less than 10fF [18]. Along with the minimal size of the two parasitics, matching between the sensor parasitics and the reference structure parasitics will help cancel the undesired effects.

capacitance sensor. Because reverse bias junction isolation is not used for the upper electrode, there is no associated leakage current.

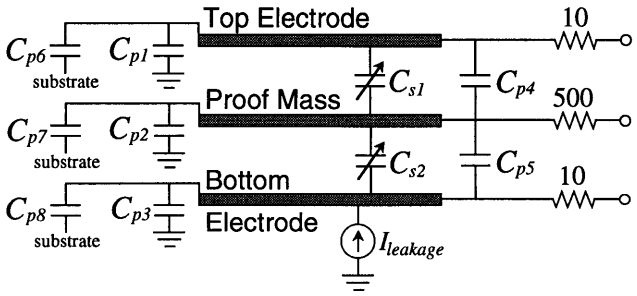


Figure 2.6 Electrical parameters of the sensor

CHAPTER 3

The Closed Loop System

Designing a stable closed loop system using integrated electronics is a fairly straight forward task. Using switched-capacitor circuitry with better than 8-bit matching, the dynamics of an integrated circuit can be predicted with a high degree of accuracy. However, when a control loop is placed around an integrated mechanical sensor with design tolerances as great as 20%, closed loop stability becomes a much larger design issue. In addition, attempting to minimize the effects of noise, cancel parasitics, remove nonlinearities, attain μg resolution, and stabilize a proof mass can present a formidable task. This chapter outlines the design procedure and final system design used to accomplish this goal.

3.1 Design Procedure

The design of the closed loop accelerometer was approached first from the system level. However, as the design proceeded, it became evident that an iterative approach would be necessary to optimize the performance of the closed loop system. All design

decisions were made in an iterative fashion, first exploring ideas from the system level then examining possible limitations of critical circuitry or the mechanical sensor. If circuit or sensor limitations prevented realization of a design, different ideas or adjustments were again explored from the system level. This approach ensured that the capabilities of the electrical and mechanical systems were compatible with the final accelerometer design.

To model the operation of the accelerometer, a custom simulation program, CLASP (**C**losed **L**oop **A**ccelerometer **S**imulation **P**rogram), was written. As the accelerometer design proceeded and implementation choices were made, CLASP was simultaneously updated to accurately model each circuit or mechanical element, including nonlinearities[21]. After extensive design and simulation, the circuit implementation was finalized along with the required mechanical and electrical properties of the sensor (table 2.1). The remainder of this chapter details the final system design and the modelling of its performance.

3.2 Stability and System Dynamics: The Main Loop

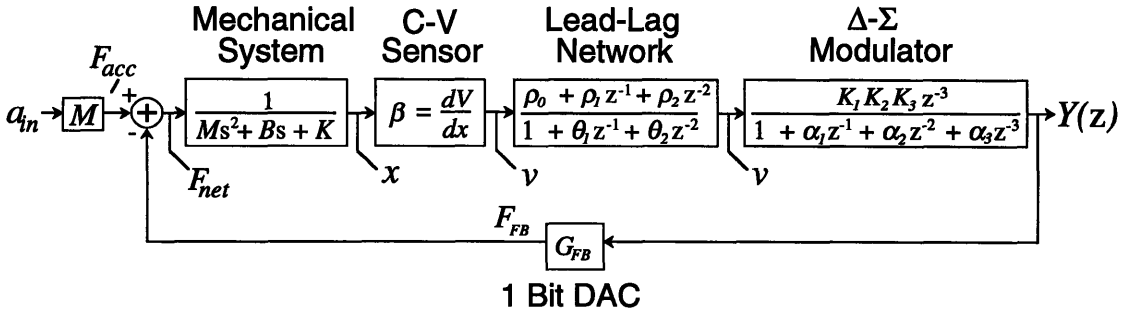


Figure 3.1 The "Gain Block" System Model

With several sources of negative phase shift in the closed loop system including the mechanical system, lag network, and Δ-Σ modulator, stability is a major concern. To accurately predict the dynamics of the closed loop system, each "block" in the system is

21. The final version of CLASP models nonlinearities in damping, spring force, and electrostatic forces placed on the proof mass.

modelled having a gain with associated poles and zeros as shown in figure 3.1. Taylor expansions are used to establish linear gain models for the nonlinear elements within the loop over an incremental operating range.

This section predicts the closed loop dynamics of the accelerometer and examines its stability criterion using the linear analysis described above. Nonlinear behavior of the closed loop system which is not predicted using this simplified linear analysis is detailed in section 3.4.

3.2.1 Stability

The need for compensation can be illustrated by examining the dynamics of the mechanical system and delta-sigma modulator. Both are significant sources of negative phase shift within the loop. As was shown in section 2.3, the inertial mass, spring, and viscous damping of the mechanical system can be accurately modelled as a high-Q low pass mechanical filter with a transfer function given by

$$\frac{X(s)}{F(s)} = \frac{1}{Ms^2 + Bs + K} = \left(\frac{1}{M}\right)\frac{1}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \qquad [3.1]$$

The forward transfer function of the Δ-Σ converter has a third order lowpass characteristic given by [25]:

$$H_X(z) = \frac{K_1K_2K_3z^{-3}}{1 + \alpha_1z^{-1} + \alpha_2z^{-2} + \alpha_3z^{-3}} \qquad [3.2]$$

where the K_i and α_i terms are set in the design of the modulator. Discrete-time (z-domain) representation is used to model the transfer characteristic of the modulator due to its switched-capacitor circuit implementation. The three poles of the modulator are located at approximately 45 kHz.

Figure 3.2 shows the gain/phase plot of a loop comprised of just the mechanical system and third order Δ-Σ modulator[22]. Under the assumption that the C-V sensor provides negligible phase shift, figure 3.2 can be used to approximate the uncompensated

22. In this example, the mechanical resonant frequency is placed at 2kHz.

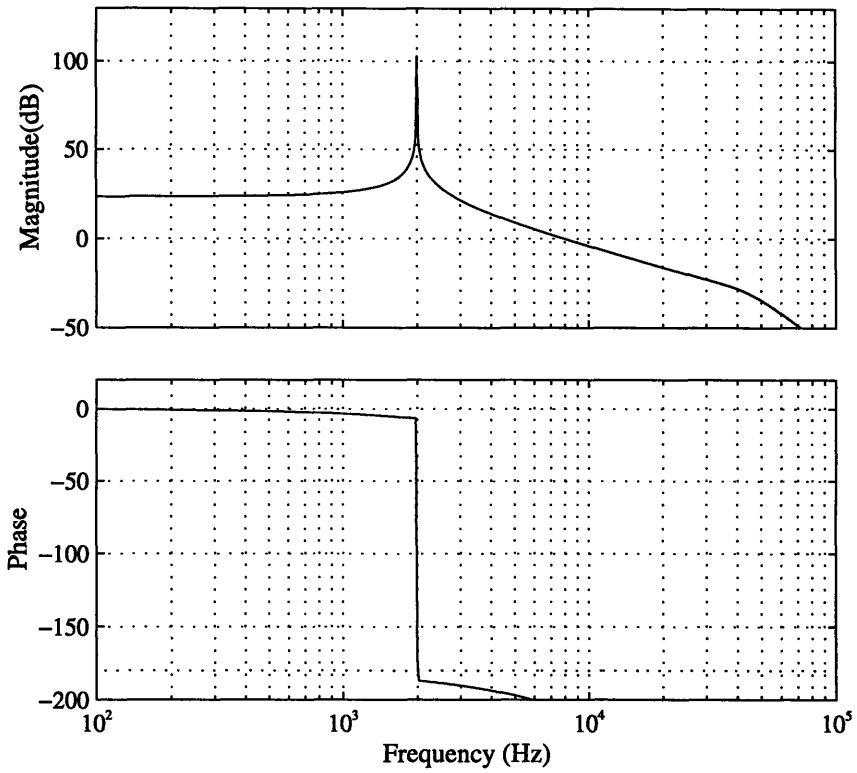


Figure 3.2 Gain/phase plot of mechanical system and Δ-Σ modulator

loop dynamics of the accelerometer. Because of the highly underdamped nature of the sensor (Q≈50,000), the mechanical system alone provides nearly 180° of negative phase shift above its resonant frequency. With no compensation added to the loop, the system crossover frequency must be placed below 2kHz to achieve positive phase margin and thus ensure closed loop stability[23].

As it turns out, placing crossover below the mechanical resonant frequency is undesirable for several reasons. First, because the mechanical resonant frequency has a loose tolerance, 20%, placement of the loop crossover anywhere in the vicinity of resonance will not guarantee a robust system. Secondly, if the system is marginally stable, "ringing" (damped oscillations) will be present near the crossover frequency of the accelerometer. Because this "ringing" is located at a frequency just above baseband, damped

23. Note the system shown in figure 3.2 is unstable. The 8kHz crossover is used here purely as an example. The final system dynamics are detailed in section 3.2.5.

oscillations may be seen at the post-filtered output of the accelerometer unless an extremely sharp "brick wall" decimation filter is used. Lastly, if the bandwidth of the closed loop system is near the decimation bandwidth, a large degree of rolloff will be seen in the baseband signal. Thus, for the aforementioned reasons, it is desirable to place the crossover frequency of the system well above baseband. With crossover placed at or above the resonant frequency of the mechanical system, compensation is necessary to achieve closed loop stability.

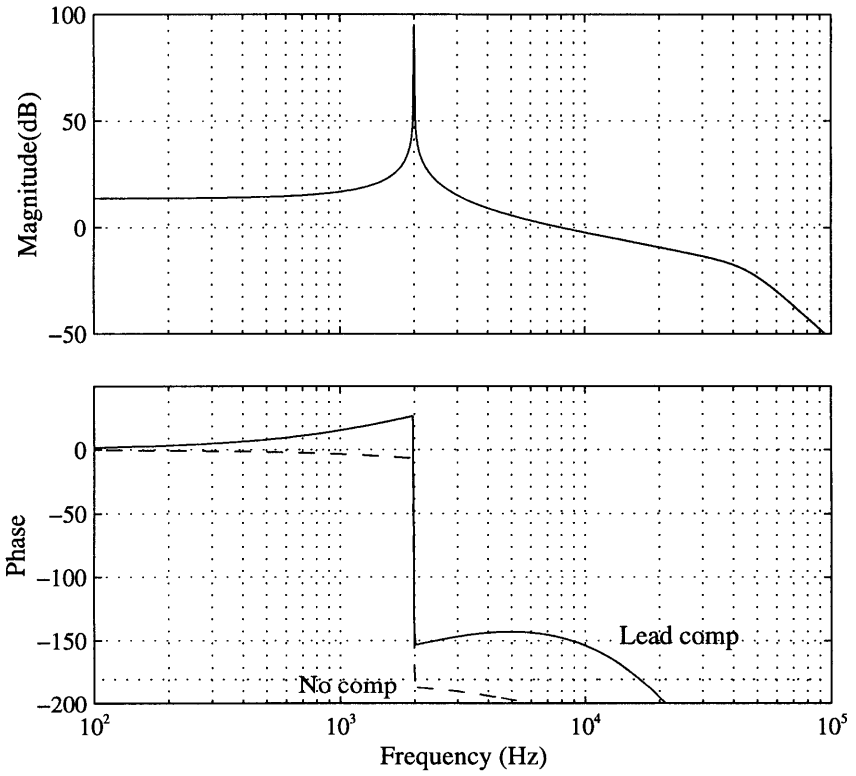


Figure 3.3 Gain/phase of lead compensated system

Figure 3.3 shows the gain-phase plot of the previous loop but with "lead" (zero-pole) compensation added. By placing a zero below crossover and a pole above, positive phase is added to the loop. The uncompensated phase is repeated here to illustrate the added positive phase contributed by the lead network. With the lead compensation as shown, a crossover frequency located between 3kHz and 17kHz results in a stable system

and ensures that the accelerometer's post-decimated output will be free of damped oscillations due to the system's natural response.

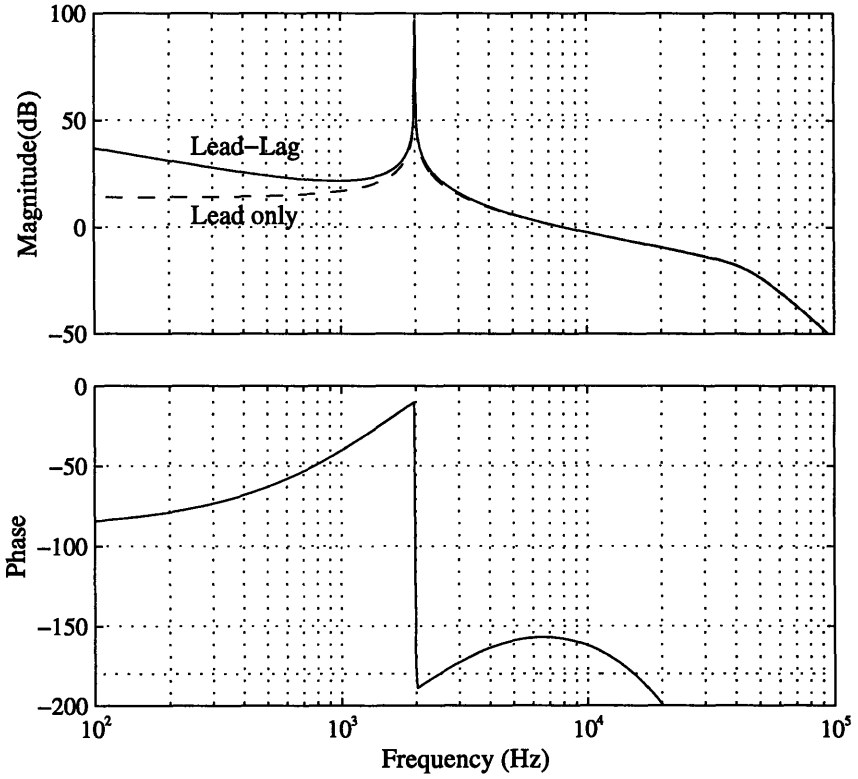


Figure 3.4 Gain/phase of lead-lag compensated loop

Note that in figure 3.3 the low frequency loop gain flattens out below the mechanical resonant frequency. With such a small gain in the low frequency range, the closed loop transfer function of the accelerometer is sensitize to small variations in loop gain. Figure 3.4 shows the gain-phase plot of the system used for figure 3.3 with "lag" (pole-zero) compensation added. To maximize loop gain, the pole from the lag network is placed at DC. The zero from the lead compensation is placed below the system crossover frequency to partially cancel the negative phase shift from the DC pole at crossover. Note the increase in low frequency gain which results from the added lag compensation. Along with desensitizing the closed loop gain of the accelerometer to fluctuations in loop gain, the lag compensation has the added benefit of reducing the input referred noise from the Δ-Σ modulator.

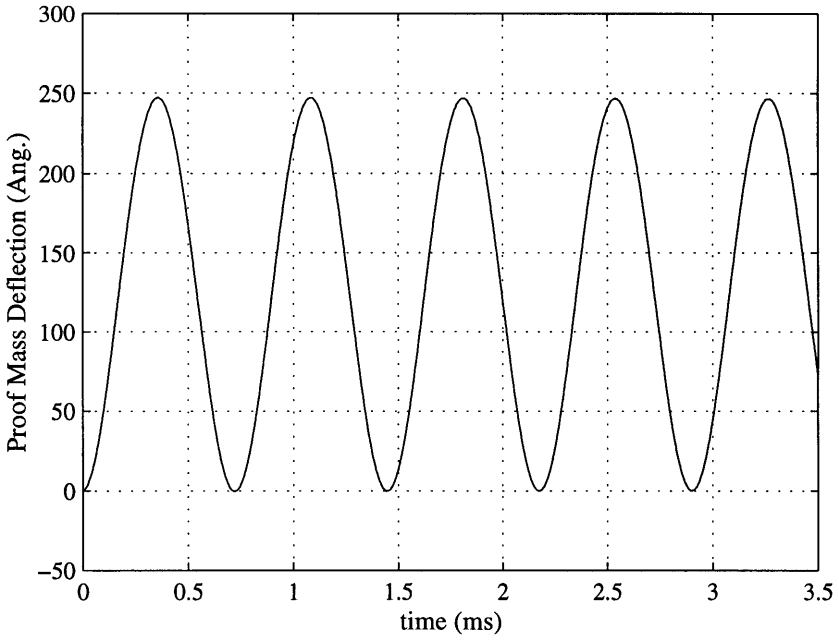


Figure 3.5 Proof Mass deflection with 1.0g step input (no compensation)

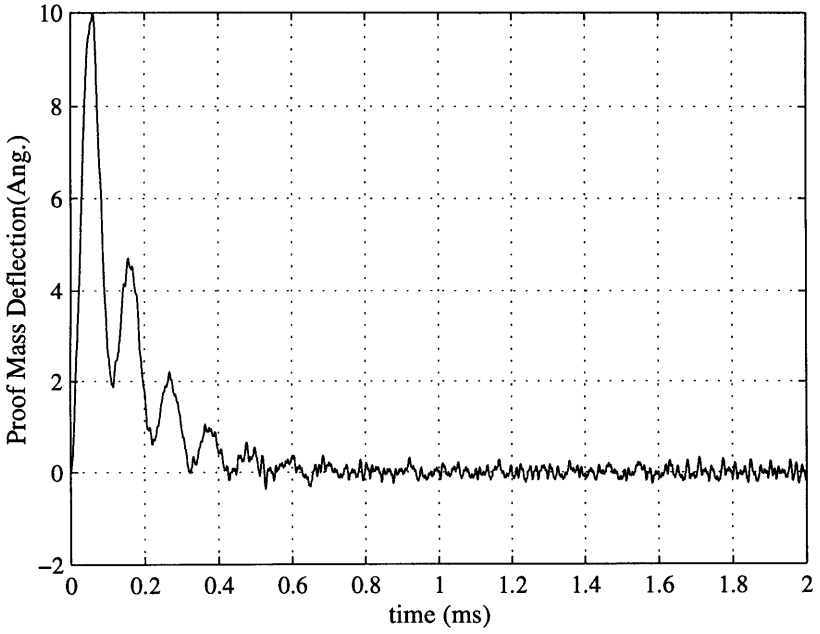


Figure 3.6 Proof Mass deflection with 1.0g step input (lead-lag compensation)

As further example of the added benefits of lead-lag compensation, see figures 3.5 and 3.6. Figure 3.5 shows proof mass deflection of an uncompensated accelerometer in response to a 1.0g step acceleration input. To maintain stability, loop crossover is placed just under 2kHz. In contrast, figure 3.6 shows the proof mass deflection of a lead-lag compensated accelerometer in response to the same 1.0g step input. The uncompensated system exhibits marginal stability illustrated by the extended oscillations in the step response. Also note the relatively large steady state deflection of the proof mass. The compensated system of figure 3.6 exhibits no damped oscillations and settles to a much smaller steady state deflection.

3.2.2 Lead-Lag Compensation

While the need for compensation was explained by applying basic closed loop theory to the transfer functions of only the mechanical system and Δ-Σ modulator, the effective gain and dynamics of all system elements are necessary to accurately predict the closed loop dynamics of the sensor. To model the system as having a forward gain and feedback as shown in figure 3.1, transfer functions must be established for the C-V sensor, lead-lag network, and force feedback. This section examines the lead-lag compensation and its associated transfer function. Linearized models are derived for the C-V sensor and force feedback mechanism in the following two sections. The Δ-Σ modulator is covered in section 3.4.

The lead-lag compensation network was designed first as a continuous time filter, then converted to a discrete-time filter (z-domain) using the bilinear transform. The one-to-one mapping of the bilinear transform between the continuous-time domain and discrete-time domain guarantees stability mapping [26].

The lag network which is used to provide increased gain at low frequencies, places a pole at DC and a zero at 1.5kHz (figure 3.7)[24]. The DC pole placement of the filter provides infinite DC gain to the loop. The zero placed at 1.5kHz is used to partially cancel

24. The pole-zero plots in figure 3.7 illustrate the placements of the poles and zeros for the continuous time filter from which the discrete-time lead-lag network was derived.

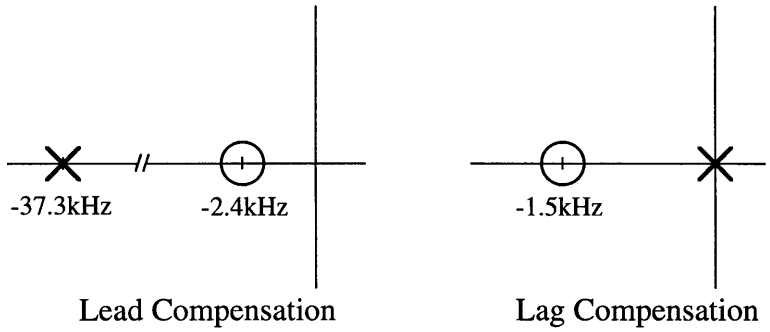


Figure 3.7 Pole-zero plots for the lead and lag compensation

the negative phase shift from the DC pole. The magnitude and phase plots for the lag filter are shown in figure 3.8[25]. Note the residual negative phase shift from the lag compensation extends more than a decade above the zero placement.

The lead network, used to provide positive phase at crossover, is composed of a zero placed at 2.4kHz and a pole placed at 37.3kHz (figure 3.7). The low frequency zero contributes positive phase shift to the loop at crossover. The pole is necessary to rolloff the magnitude of the filter, enabling a realizable circuit implementation. The zero-pole placement of the lead compensation is set such that the maximum positive phase shift of the filter is located at 10kHz. A lower frequency placement of this maximum positive phase shift was prevented by the necessary capacitor ratios in the circuit implementation of the lead lag compensation network. The magnitude and phase plots for the lead filter are shown in figure 3.9[26].

The continuous-time transfer function from which the discrete-time lead-lag compensation was derived is given by:

$$H_{LL}(s) = \beta \frac{(s + 1.5k(2\pi))}{s} \frac{(s + 2.4k(2\pi))}{(s + 37.3k(2\pi))} \qquad [3.3]$$

where β is a scaler multiplier. Using the bilinear transform, the discrete time filter was generated:

25. The magnitude plot is accurate to within a scaler multiplier of the final lag compensation. The importance of the magnitude plot here is to demonstrate the infinite gain at DC and rolloff characteristic of the filter.
26. Again, the magnitude is accurate to within a scaler multiplier.

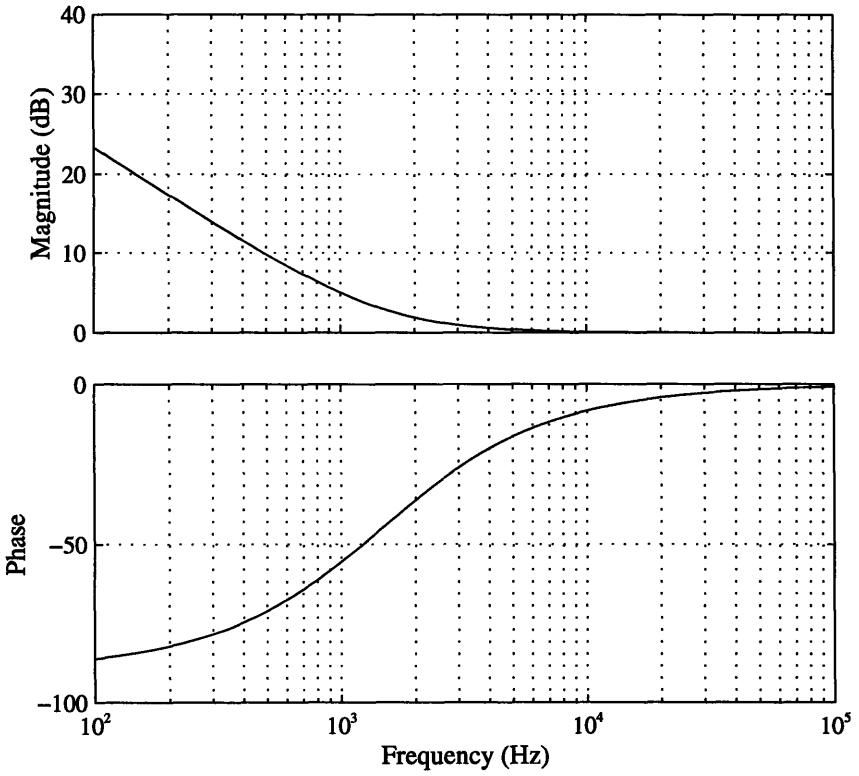


Figure 3.8 Magnitude and phase for the lag compensation

$$H_{LL}(z) = -\frac{7.039 - 13.7z^{-1} + 6.68z^{-2}}{1 - 1.614z^{-1} + 0.614z^{-2}} \quad [3.4]$$

The value of the scaler multiplier was chosen to minimize capacitance ratios in the switched-capacitor circuit implementation of the filter[27].

3.2.3 The Linearized C-V Model

The input to the C-V sensor "block" of figure 3.1 is the deflection of the proof mass, x, and the output is a voltage. In actuality, the C-V sensor measures the sense capacitance, C_X, and the reference capacitance, C_R, and outputs a voltage proportional to the difference between the two capacitors, ΔC[28]. To accurately model the transfer function of

27. The switched-capacitor circuit realization of the discrete time filter requires large capacitor ratios to implement the desired pole and zero locations. The gain of the compensation was selected such that the capacitance ratios were minimized once the pole and zero locations had been set.

28. See section 4.3 for the circuit implementation of the C-V sensor.

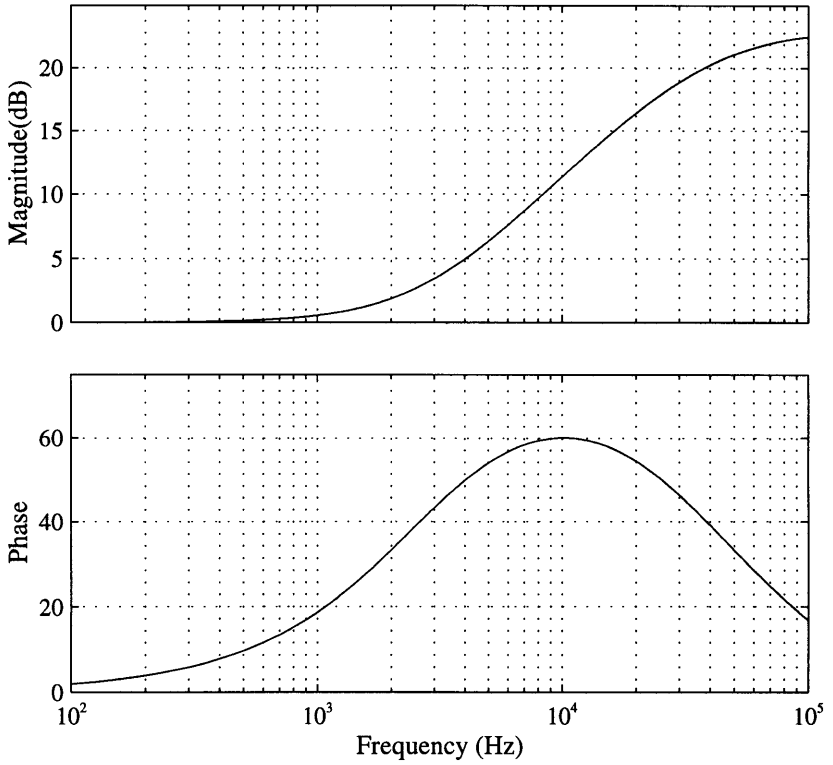


Figure 3.9 Magnitude and phase for lead compensation

the C-V sensor in the form of figure 3.1, a relation must be established between the change in capacitance, ΔC, and deflection of the proof mass, x.

The sensor capacitance, C_X, and reference capacitance, C_R, are given by:

$$C_X = \frac{\varepsilon_o A}{d + x} \qquad C_R = \frac{\varepsilon_o A}{d} \tag{3.5}$$

where d is the nominal gap spacing between the proof mass and fixed electrodes and A is the area of the fixed electrodes. Expanding C_X:

$$C_X = \frac{\varepsilon_o A}{d}\left(1 - \left(\frac{x}{d}\right) + \left(\frac{x}{d}\right)^2 - \left(\frac{x}{d}\right)^3 \ldots\right) \tag{3.6}$$

Combining equations 3.5 and 3.6:

$$\Delta C = C_X - C_R = -\left(\frac{x}{d}\right)\frac{\varepsilon_o A}{d}\left(1 - \left(\frac{x}{d}\right) + \left(\frac{x}{d}\right)^2 - \left(\frac{x}{d}\right)^3 \ldots\right) \tag{3.7}$$

For small proof mass deflections ($x \approx 0$), equation 3.7 can be approximated by:

$$\Delta C \approx -\left(\frac{x}{d}\right)\frac{\varepsilon_o A}{d} = -\left(\frac{x}{d}\right)C_R \qquad [3.8]$$

The effective output of the C-V sensor can now be given by:

$$V_{CVout} = \beta\Delta C \approx -\beta\left(\frac{C_R}{d}\right)x \qquad [3.9]$$

where the gain factor β (Volts/Farad) is determined in the circuit implementation of the capacitance sensor.

3.2.4 The Linear Force-Feedback Model

The last component to be modelled from the closed loop diagram of figure 3.1 is the force feedback element. The input to the feedback "block" is the output bit stream from the Δ-Σ modulator, the output is the restoring force applied to the proof mass. The electrostatic restoring force applied to the proof mass was previously established as:

$$F_{FB} = \eta(\Phi_1)\frac{2\varepsilon_o A}{d^2}V_{DC}V_{DIFF} \qquad [3.10]$$

where V_{DC} and V_{DIFF} are the DC bias and differential voltages, respectively, placed on the feedback electrodes, A is the area of the fixed electrodes, d is the nominal gap spacing, and $\eta(\Phi_1)$ is the duty cycle over which the feedback force is applied(~0.5).

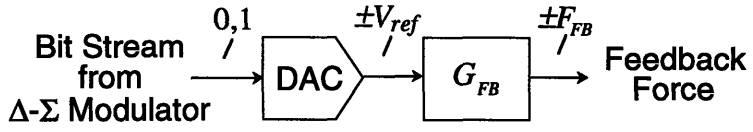


Figure 3.10 Digital-to-analog, voltage-to-force conversion

At first glance, it might seem that the transfer characteristic would be accurately modelled by taking the change in applied force for the change in differential voltage, dF_{FB}/dV_{DIFF} from equation 3.10. This, however, would be incorrect as it does not take into account the analog voltage represented by each bit from the modulator. To simplify mod-

elling the transfer characteristic of the feedback mechanism, the digital-to-analog conversion can be separated from the voltage-to-force conversion as shown in figure 3.10.

A "1" at the output of the modulator represents a $+V_{ref}$ input to the feedback element which results in an output force $+F_{FB}$ fed back to the proof mass. Similarly, if a "0" is output from the modulator, $-V_{ref}$ is encoded and $-F_{FB}$ is the output from the feedback block. Solving for the effective gain of the block:

$$G_{FB} = \frac{\eta(\Phi_1)\frac{2\varepsilon_o A}{d^2} V_{DC} V_{DIFF}}{V_{ref}} \qquad [3.11]$$

where $\pm V_{ref}$ are the feedback levels from the DAC within the Δ-Σ modulator.

3.2.5 Closing the Loop

The linearized transfer functions for the C-V sensor and feedback force can now be combined with the forward transfer functions of the Δ-Σ modulator, lead-lag network, and mechanical system to predict the closed loop dynamics of the accelerometer. In order for all the loop transfer characteristics to be modelled in the discrete time domain, the response of the second order mechanical system is converted from the continuous-time format of equation 3.1 to a discrete-time (z-domain) representation using the bilinear transform[29]. Figure 3.11 updates the accelerometer's system diagram showing the transfer characteristic for each system block[30]. Figure 3.12 shows the corresponding magnitude and phase response of the system.

Several factors were considered in the selection of the crossover frequency of the accelerometer. As previously discussed, the crossover frequency must be located well above the 1.0kHz baseband to avoid rolloff in baseband or "ringing" due to the system's natural response. Probably the most important criterion used for determining the system crossover frequency is loop stability. The crossover frequency must be placed at a high enough frequency to avoid large residual phase shift from the lag network without going

29. As with the leadlag network, the bilinear transform is used for its guaranteed stability mapping between the continuous and discrete time domains.

30. The mechanical system modelled here uses the 750μm×750μm proof mass with a 3.2kHz resonance.

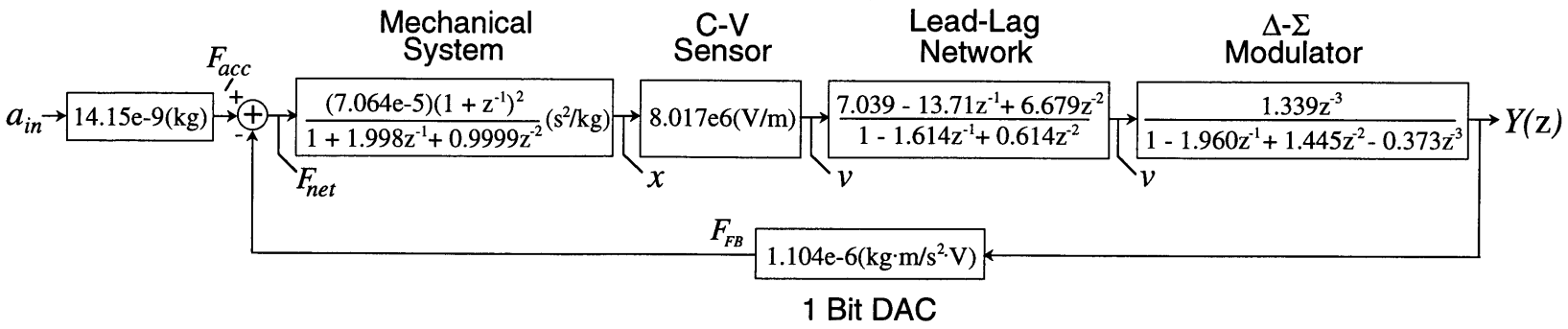


Figure 3.11 Accelerometer System Diagram

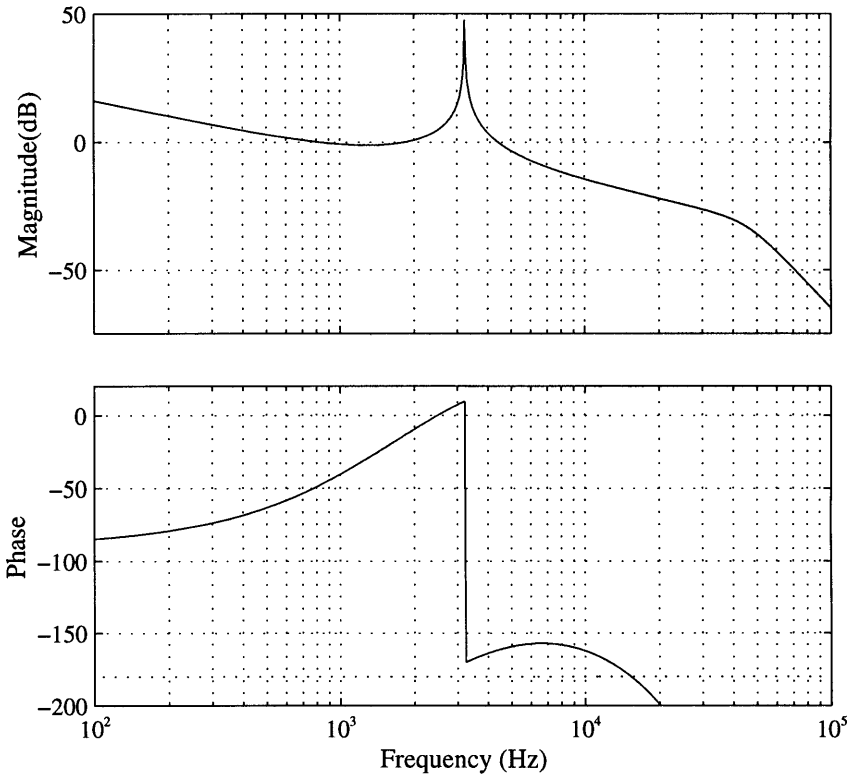


Figure 3.12 Gain phase plot for complete system

to frequencies high enough to incur significant negative phase shift from the Δ-Σ modulator.

In addition to classical linear analysis, stability concerns also arise from circuit noise in the accelerometer. Circuit noise, dominated by the C-V sensor, can be referred to the output of the mechanical system as a positional noise, $\overline{x_n}$, as shown in figure 3.14. Because this noise represents an error in the measured position of the proof mass, the noise causes an incorrect restoring force to be applied to the proof mass. As expected, the effects of this noise are seen at the output of the accelerometer and can limit the resolution of the sensor[31]. In addition, the circuit noise has the potential to cause the loop to go unstable. This occurs when the circuit noise causes the accelerometer to operate outside its linear region of operation. Once outside the linear region, the prior stability analysis no longer holds and the system can become unstable.

31. A full system noise analysis is carried out in section 4.7

The noise tolerance of the loop is inversely related to the bandwidth of the closed loop system. As the system bandwidth is decreased, the response of the loop becomes slower which prevents the system from having time to react to higher frequency noise[32]. The lower system crossover, in effect, increases the stability of the accelerometer by filtering more noise from the closed loop system[33]. Thus, there is additional motivation for a lower system crossover placement. Table 3.1 shows the relationship between the crossover placement in the accelerometer and noise levels which cause the loop to go unstable.

System Crossover Frequency	Noise level, $\overline{x_n}$, which causes instability
4.5kHz	11.6Å
13.75kHz	6.6Å
28.7kHz	0.67Å
57.5kHz	0.3Å

Table 3.1 Noise Tolerance vs. Bandwidth

All data points in table 3.1 were generated with a 0g input acceleration. The accelerometer becomes less stable as its input nears the limits of the sensor's dynamic range. Because of this, a smaller amount of circuit noise will cause instability as the input magnitude increases. Thus, circuit noise which does not cause instability still has the undesired effect of reducing the stable input range to the accelerometer.

The simulated output spectrum of the full system is shown in figure 3.13. The output response shown is for a 1.0g sinusoidal input at 750Hz. Note the notch in the output spectrum at 3.2kHz. This is due to the resonator formed by the highly underdamped mechanical system.

32. This is the case for white noise only. The effects of low frequency noise such as $1/f$ noise would not be significantly reduced by lowering the bandwidth of the system. Circuit techniques are used, however, which remove the effects of $1/f$ noise. See sections 4.2 and 4.3.

33. Note, though the stability of the loop is increased by lowering the system bandwidth, the resolution of the accelerometer is not affected. The baseband (decimation) frequency, still set at 1kHz, would have to be lowered to reduce the total noise present at the output and thus, increase the resolution of the sensor.

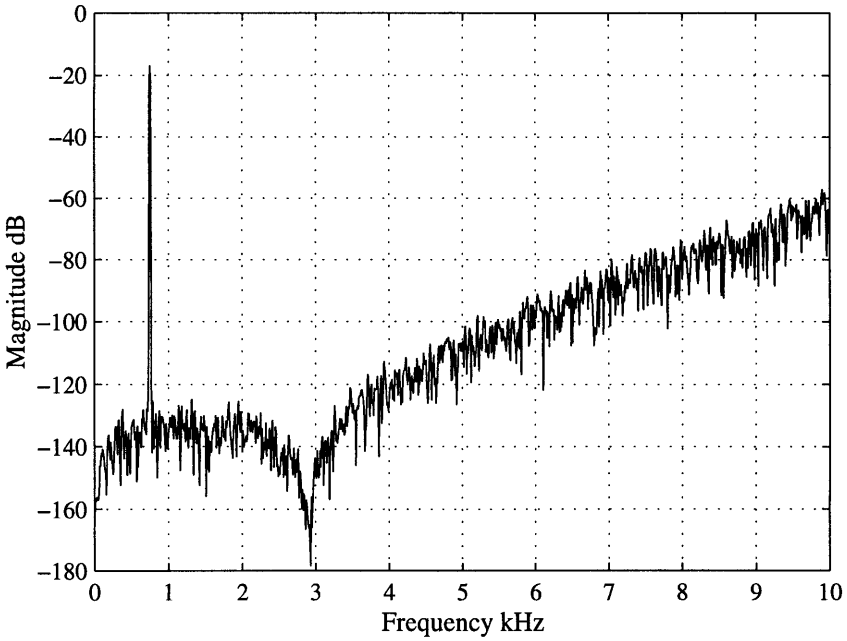


Figure 3.13 Output spectrum for 1.0g sinusoid input @ 750Hz

While the prior linear analysis is an adequate tool for stabilizing the accelerometer and setting the loop bandwidth of the system, two assumptions are made which would lead to a nonoptimal system design if not otherwise taken into account. The first assumption is that the capacitive position sense is noninvasive - that the circuit implementation of the C-V sensor in no way alters the dynamics of the mechanical system. The capacitive sense circuit does in fact affect the dynamics of the mechanical system and can actually be used to greatly reduce the resolution limiting effects of circuit noise. This is examined in the following section. The second assumption is that the system always behaves as a linear system. While this is true under a certain set of limited conditions, the accelerometer design must take into account the fact that the system must sometimes operate outside the incremental region over which the linear analysis is valid. Otherwise, the system may never work at all. A nonlinear analysis of the system is detailed in section 3.4.

3.3 Incremental Dynamics and Resonance Tuning

In section 1.2, a relation was derived between the applied feedback force, the deflection of the proof mass, and the voltages applied to the fixed electrodes above and below the proof mass. This force was approximated as constant and the positional-dependance of the applied force was considered a likely limitation to the overall resolution of the accelerometer. As it turns out, the positional dependance of the electrostatic force which was initially thought to limit the accelerometer's resolution can actually be used to markedly increase the resolution of the sensor. This section examines the interaction between the voltages applied to the fixed electrodes and the dynamics of the mechanical sensor.

3.3.1 The Electric Spring

As was previously established, circuit noise in the accelerometer could be mod-

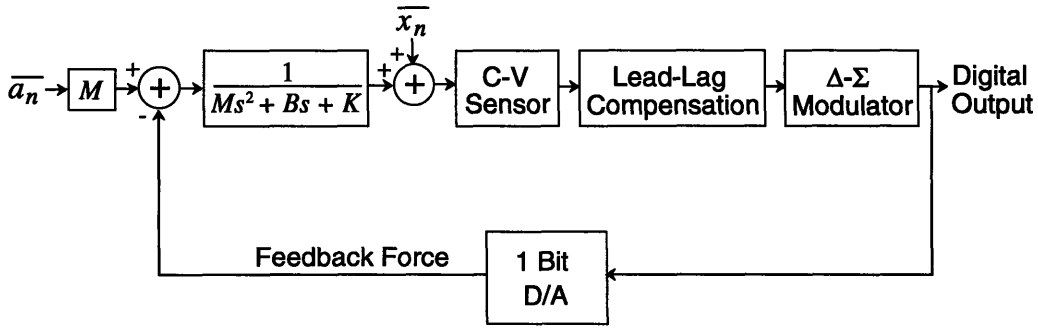


Figure 3.14 Input referred noise

elled as an error in the measured deflection of the proof mass. Figure 3.14 models this error as a positional noise, $\overline{x_n}$. From a circuit design standpoint, noise can be minimized through careful design and layout[34]. From the system design standpoint, the effective gain of the C-V sensor should be maximized to reduce the input-referred noise from the lead-lag circuitry. Once these steps have been taken, all that remains between the posi-

34. Section 4.7 details the circuit noise calculations.

tional noise, $\overline{x_n}$, and the input referred acceleration noise, $\overline{a_n}$, is the effective gain of the mechanical system. From figure 3.14, the input referred circuit noise is given by:

$$\overline{a_n} = \frac{\overline{x_n}}{M\frac{X(s)}{F(s)}} \qquad [3.12]$$

Recall the size of the proof mass, M, is constrained to limit device area and prevent warping in the proof mass. Thus, the last available mechanism with which to reduce the input referred circuit noise is the effective gain of the mechanical system, $X(s)/F(s)$. From equation 2.2, the gain of the mechanical system can be approximated by:

$$\frac{X(s)}{F(s)} \approx \frac{1}{K} \qquad [3.13]$$

at low frequencies. Combining equations 3.12 and 3.13, the input referred circuit noise is approximated by[35]:

$$\overline{a_n} \approx \frac{\overline{x_n}}{M/K} = \omega_o^2 \overline{x_n} \qquad [3.14]$$

where ω_o is the mechanical resonant frequency. Thus to reduce the input referred circuit noise, the resonant frequency of the mechanical system should be lowered. Because the mechanical resonance frequency is limited to being greater than 2.0kHz due to the mechanical and electrical limitations of the sensor, an apparent lower bound was initially thought to exist for the input referred circuit noise. This was thought to limit the overall resolution of the accelerometer.

Returning to the feedback force equation which was derived in section 1.2, the electrostatic restoring force is given by:

$$F_{FB} = \eta(\Phi_1)\frac{2\varepsilon_o A}{d^2} V_{DC} V_{DIFF} \left[1 - \frac{V_{DC}^2 + V_{DIFF}^2}{V_{DC} V_{DIFF}} \left(\frac{x}{d}\right) + 3\left(\frac{x}{d}\right)^2 \ldots \right] \qquad [3.15]$$

35. This approximation begins to break down when the bandwidth of the mechanical system falls below that of the decimation (baseband) frequencies. However, until the mechanical resonance approaches DC, the total input referred circuit noise is still reduced by lowering the mechanical bandwidth.

Originally, this force was approximated by its constant term and the position dependant terms were thought to represent an error in the applied feedback force. Upon closer inspection, the positionally-dependant feedback terms can be used as a means of tuning the mechanical resonance structure. Equation 3.16 gives the first three position-dependant terms of equation 3.15.

$$F(x) = -x\eta(\Phi_1)\frac{2\varepsilon_o A}{d^3}\left[V_{DC}^2 + V_{DIFF}^2 - 3\left(\frac{x}{d}\right)V_{DC}V_{DIFF} + 2(V_{DC}^2 + V_{DIFF}^2)\left(\frac{x}{d}\right)^2 \ldots\right] \quad [3.16]$$

Note that each term is an increasing power of (x/d). For small deflections, only the first order term is significant. The positional dependance of the feedback force can thus be approximated by:

$$F(x) = -\eta(\Phi_1)\frac{2\varepsilon_o A}{d^3}(V_{DC}^2 + V_{DIFF}^2)x = -K_{EL1}x \quad [3.17]$$

Inspection of equation 3.17 reveals that the positional dependance of the electrostatic force can be accurately modelled as a negative spring force. A term similar to K_{EL1} results from voltages applied to the fixed electrodes during the capacitive position sense[36]:

$$K_{EL2} = \frac{\varepsilon_o A}{d^3}[\eta(\Phi_2)V_{tune}^2 + \eta(\Phi_3)V_1^2 + \eta(\Phi_4)V_2^2] \quad [3.18]$$

where V_{tune}, V_1, and V_2 are voltages applied during the C-V sense and $\eta(\Phi_2)$, $\eta(\Phi_3)$, and $\eta(\Phi_4)$ are the duty ratios of the three voltages, respectively. Equations 3.17 and 3.18 are combined to obtain the total effective electric spring constant:

$$K_{EL} = \frac{\varepsilon_o A}{d^3}[\eta(\Phi_1)2(V_{DC}^2 + V_{DIFF}^2) + \eta(\Phi_2)V_{tune}^2 + \eta(\Phi_3)V_1^2 + \eta(\Phi_4)V_2^2] \quad [3.19]$$

Summing the forces acting on the proof mass now including the positional dependence of the feedback force, the net force acting on the proof mass is given by:

$$F_{NET} = F_{acc} - F_{FB} = M\ddot{x} + B\dot{x} + (K_{sp} - K_{EL})x \quad [3.20]$$

36. The full analysis of the electric spring constant is carried out in section 4.3.

The mechanical system is now modelled as having two springs: a mechanical spring, K_{sp}, and an electrical spring, $-K_{EL}$. Figure 3.15 models the mechanical system with the additional spring force.

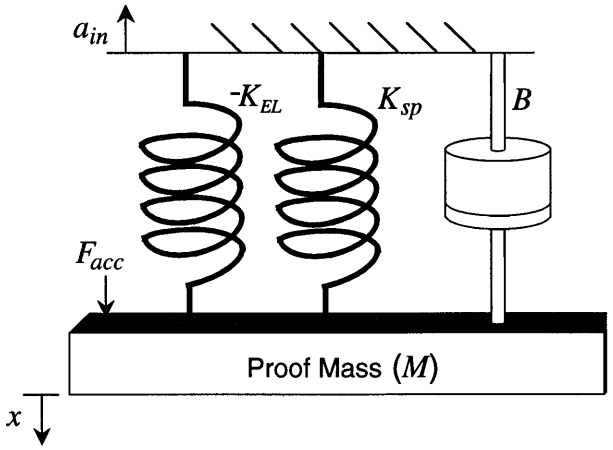


Figure 3.15 The ElectroMechanical System

The adjusted transfer function of the mechanical system is given by:

$$\frac{X(s)}{F(s)} = \frac{1}{Ms^2 + Bs + (K_{sp} - K_{EL})} \qquad [3.21]$$

By carefully controlling the voltages placed on the fixed electrodes during both the C-V sense and feedback cycles, the electric spring constant, K_{EL} can be used to reduce or cancel the mechanical spring constant, K_{sp}. By altering the effective spring force, the pole locations of the mechanical system can be adjusted. Because the adjusted response of the mechanical system is only valid for a small range of proof mass deflections, it is referred to as the *incremental dynamics* of the structure.

As K_{EL} is increased, the net spring force acting on the proof mass is lowered. This, in effect, reduces the resonant frequency of the mechanical system. The effect of lowering the effective spring constant can be seen in figure 3.16. As the effective spring constant of the mechanical system is reduced, the two poles of the mechanical system are brought in towards the real axis. As K_{EL} is increased further, the two poles meet on the negative real axis then split, one heading in the direction of the negative real axis and the other towards the right half plane. When the electric spring constant, K_{EL}, exactly cancels the mechani-

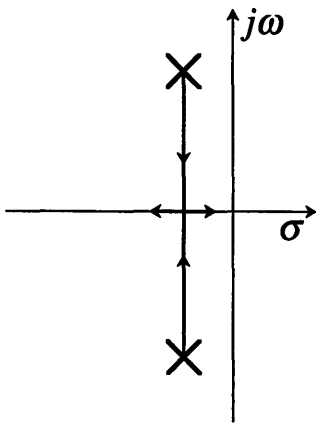


Figure 3.16 Pole-zero plot for the electromechanical system

cal spring constant, K_{sp}, one pole of the mechanical system is placed at DC and the other slightly into the left half plane on the negative real axis. As a practical method of adjusting the mechanical system poles, the C-V sensor is designed such that K_{EL} can be varied by changing the voltages which are applied to the fixed electrodes placed above and below the proof mass[37]. This "resonance tuning" method is used to locate the poles of the mechanical system such that the input referred circuit noise is minimized.

3.3.2 The Updated System

Figure 3.17 shows the output spectrum of the accelerometer with the positional dependance of the electrostatic forces acting on the proof mass fully modelled. The input to the accelerometer is a 1.0g sinusoid at 750Hz, identical to that of figure 3.13. The "tuned" mechanical resonance is placed at approximately 200Hz to minimize input referred circuit noise[38]. Note the "notch" in the output spectrum has been relocated from 3.23kHz to a near DC placement.

Exact adjustment of the low frequency mechanical poles is not always possible. If the electric spring constant, K_{EL}, is set at a value slightly too large, one pole of the mechan-

37. See section 4.3.

38. A DC pole placement of one of the poles of the mechanical system would minimize the input referred circuit noise if the mechanical system were critically damped or overdamped. However, because of the sharp "peaking" in the mechanical system's response due to its highly underdamped nature, the input referred noise is minimized using a pole placement slightly above DC.

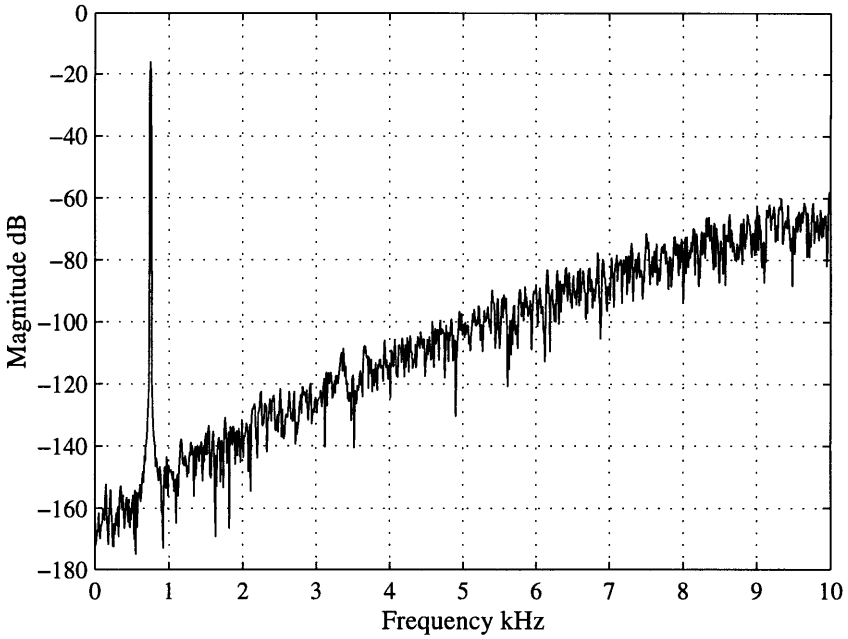


Figure 3.17 Output spectrum with resonance tuning

ical system will slide into the right half plane (RHP). Note that this results in an open loop RHP pole which does not indicate instability as would be the case for a closed loop RHP pole. The phase shift of the mechanical system with and without a pole placed in the right half plane is shown in figure 3.18. If, as designed, both poles of the mechanical system are located in the left half plane, the phase shift from the mechanical system begins at 0° and falls rapidly to -180° just above the mechanical resonant frequency. If, however, one of the poles of the mechanical system is located in the right half plane, the phase of the mechanical system begins at -180° at DC, rises slightly[39], then returns to -180°. In both cases, the phase of the mechanical system is very close to -180° at 4.5kHz, the crossover frequency of the closed loop system. Thus, as 180° of negative phase shift is expected from the mechanical system and was taken into account in the system design, the stability of the closed loop system is not in question if one of the mechanical poles drifts slightly into the right half plane.

39. This slight rise in phase is not apparent in figure 3.18 due to the scale of the figure.

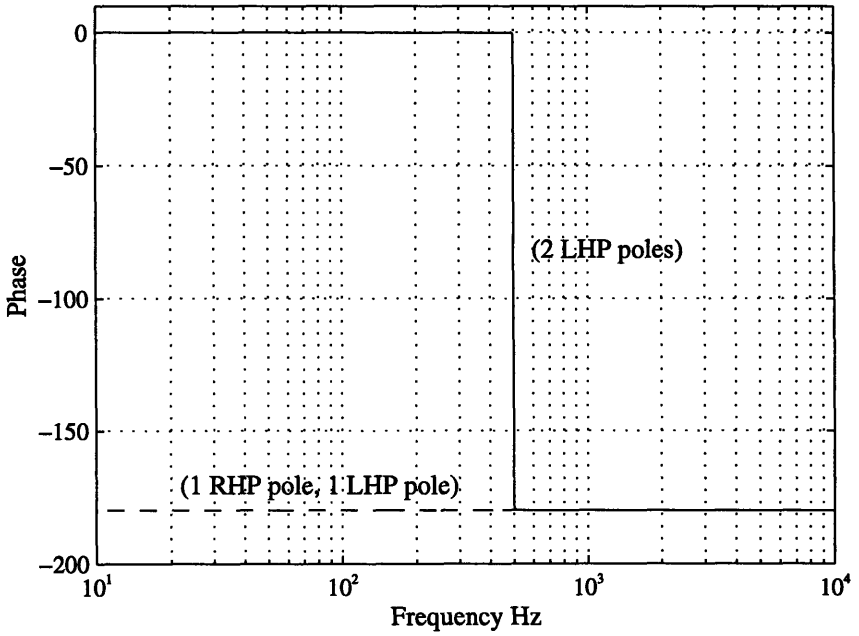


Figure 3.18 Phase shift in the mechanical filter

3.4 Nonlinear Behavior

In section 3.2, the accelerometer was modelled as a linear system in order to predict the dynamics and the linear stability constraints of the loop. While linear analysis is well suited for modelling the dynamics of the accelerometer, much of the system's behavior cannot be predicted using the linear model. As it turns out, the accelerometer is accurately modelled as a 5th order electromechanical Δ-Σ modulator formed from two mechanical integrators and three electrical integrators. Using this fifth order model for the accelerometer, the nonlinear behavior can be predicted using existing Δ-Σ theory and accounted for in the final design. The analysis of the third order Δ-Σ modulator has been saved for this section as an introduction to the fifth order system model.

3.4.1 The Delta-Sigma Modulator

Understanding the function of the Δ-Σ modulator is important not only in the understanding of a single element in the accelerometer and its associated transfer function,

but also in understanding the overall function of the closed loop system. Much of the design methodology used to design the Δ-Σ modulator and predict its behavior can be applied on a larger scale to predict the function of the complete system as well as its limitations. This section describes the design and function of the Δ-Σ modulator and the derivation of its forward and quantization noise transfer functions. The Δ-Σ theory developed to explain the third order modulator is then used to predict nonlinear behaviors which cannot be modelled using the linear analysis of section 3.2.

Theory

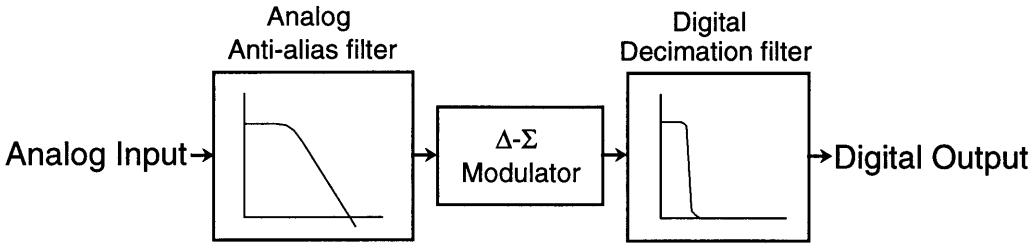


Figure 3.19 Analog-to-digital conversion using a Δ-Σ modulator

As previously discussed, a Δ-Σ modulator converts an analog input into a high frequency bit stream. Along with encoding the input to the modulator, the output bit stream contains errors resulting from circuit noise and quantization noise resulting from the analog-to-digital conversion process. The inherent operation of the modulator places most of the quantization error at higher frequencies well above the signal frequencies of interest. A "sharp" lowpass digital (decimation) filter, placed at the output of the modulator removes most of the quantization noise as well as a large portion of the circuit noise by blocking all frequency components of the output bit stream above baseband[40]. An analog lowpass filter is placed at the input to the modulator to prevent aliasing of frequencies

40. 1/*f* noise is not greatly attenuated by the decimation filtering. A large portion of the 1/*f* noise is placed within the baseband frequency range and is therefore "passed" by the decimation filter. Circuit techniques are used, however, which remove most of the effects of 1/*f* noise as well as offsets. See sections 4.1 and 4.2.

above half the sampling rate of the modulator, f_s. The full conversion scheme is shown in figure 3.19.

As discussed in section 1.2, the Δ-Σ modulator is well suited for implementing the analog-to-digital conversion in the closed loop accelerometer. It is inherently very linear due to its binary feedback [27] and its single bit output greatly simplifies the force feedback implementation. To facilitate explanation of the third-order modulator used in the accelerometer, the operation of first order Δ-Σ modulator will initially be discussed. The first-order Δ-Σ modulator is shown below in figure 3.20.

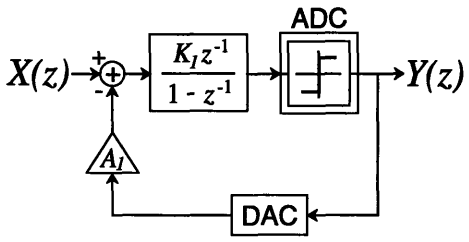


Figure 3.20 First order Δ-Σ modulator

The discrete-time function, $\frac{z^{-1}}{1 - z^{-1}}$, models the discrete-time integrator shown in fig 3.21.

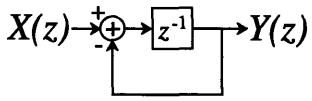


Figure 3.21 Discrete-time integrator

The output of the summing node of the modulator goes in the input of the discrete-time integrator. The comparator, placed at the output of the integrator, performs the analog-to-digital conversion of the modulator outputting a "1" for positive integrator values and "0" for negative values. The DAC, placed in the feedback path of the modulator, outputs $+V_{ref}$ for a "1" input and $-V_{ref}$ for a "0" input.

The input range for a first order modulator extends from $-V_{ref}$ to $+V_{ref}$. For an input voltage outside this range, the DAC reference voltage, V_{ref}, will be too small to offset the input voltage. When this occurs, the output of the modulator is no longer valid. Once the

input voltage returns to the valid input range, the first order modulator gracefully returns to normal operation[41].

During normal operation, the output voltage of the DAC acts to offset the input voltage to the modulator. For DC and low frequency inputs, the average output voltage from the DAC is equal to the input voltage[42]. As an example, if the input voltage to the modulator were 0V, the DAC would output $+V_{ref}$ half the time and $-V_{ref}$ half the time. This corresponds to an output bit stream of half 0s and half 1s from the comparator. Thus, the output bit stream of the modulator is an accurate digital encoding for low frequency inputs. Unlike low frequency inputs, high frequency inputs are greatly attenuated at the output of the modulator. To help see why this occurs, examine the basic first-order continuous time system shown in figure 3.22.

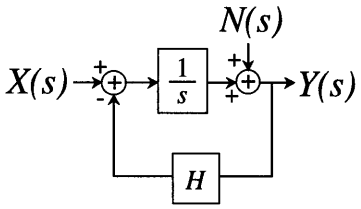


Figure 3.22 First-order continuous time system

Due to the integrator in the forward path, the continuous-time system functions as a low pass filter. The forward transfer function is given as:

$$H(s) = \frac{1}{s+H} = \frac{1}{s+\omega_{co}} \qquad [3.22]$$

At low frequencies, the large gain of the integrator provides enough loop gain to keep the closed loop transfer function approximately constant. At higher frequencies, when the gain of the integrator has declined significantly, the closed loop system reaches its only pole, ω_{co}, and the closed loop transfer function begins first order rolloff. Input signals at

41. This is not the case for third order and higher order modulators as will be discussed later.

42. This is analogous to the use of circuit averaging to model the dynamics of a DC-DC converter [28]. The only difference between the two analyses is that DC-DC converters use pulse width modulation as compared to the pulse density modulation used in Δ-Σ modulator.

frequencies well above ω_{co} are effectively removed from the output due to the decline in gain of the integrator.

Qualitatively this is exactly what happens with the first order Δ-Σ modulator. The discrete-time integrator used in the first order modulator, like its continuous-time counterpart, provides a large gain at low frequencies. Using the previous argument, low frequency signals are passed through the modulator with relatively little attenuation due to the large gain of the discrete time integrator. Similarly, high frequency inputs to the modulator are effectively filtered by the modulator as the gain of the integrator declines significantly.

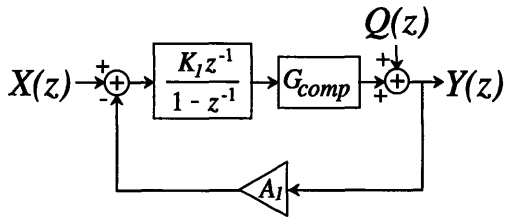


Figure 3.23 Linearized model for the Δ-Σ modulator

Taking this a step further, the modulator's comparator can be modelled as having an effective gain, G_{comp}, as shown in figure 3.23. This effective gain can be obtained numerically [29], however, simulations are more frequently used[43]. The linearized model is used to calculate the forward transfer function of the modulator, $H_X(z)$, given by:

$$H_X(z) = \frac{K_1 G_{comp} z^{-1}}{1 + (A_1 K_1 G_{comp} - 1) z^{-1}} \qquad [3.23]$$

As expected, the forward transfer function of the modulator, $H_X(z)$, has a lowpass characteristic.

In addition to the input signal components seen at the output of the modulator, the output is also comprised of an error signal resulting from the quantization process. This

43. The effective gain of the comparator changes for different inputs to the modulator and likewise, the dynamics of the modulator will change as well. As the input to the modulator increases, the effective gain of the comparator decreases eventually leading to instability when the peak input value is reached. The linearized model is used here to demonstrate the modulator's closed loop characteristics. When using the linearized model as a design tool, care should be taken to simulate function of the modulator over the full input range.

quantization noise results from the discrepancies between the DAC feedback voltages, $\pm V_{ref}$, and the input to the modulator. Returning to the previous example which used a 0V input to the modulator, the DAC oscillates back and forth between $+V_{ref}$ and $-V_{ref}$ to generate the low frequency feedback value of 0V. While the low frequency components from the DAC form a very close approximation to the 0V input, large discrepancies exist between the instantaneous feedback values from the DAC and the input to the modulator. Note in this example, the DAC output is never closer than a voltage V_{ref} to the input voltage. Thus, the instantaneous quantization error is either $+V_{ref}$ or $-V_{ref}$. Because the low frequency gain of the discrete-time integrator ensures close matching between the output of the DAC and the input voltage at low frequencies, the quantization noise must be placed mostly at higher frequencies where the gain of the discrete-time integrator has declined significantly.

To better understand the frequency components of the quantization noise, return to the continuous time system of figure 3.22. The noise signal, $N(s)$, injected at the output of the integrator has the transfer function given by:

$$H_N(s) = \frac{s}{s+H} \qquad [3.24]$$

The highpass characteristic of the noise transfer function is as a result of the large low frequency gain of the integrator in the forward path of the system. The same integrator gain which acts to "pass" low frequency inputs to the continuous time system acts to reject low frequency noise inserted at the output of the filter. The output of the continuous time system is thus desensitized to low frequency noise inserted at the output of the integrator.

In the same fashion that the continuous time system rejects low frequency noise injected at its output, the discrete-time integrator of the Δ-Σ modulator furnishes similar low frequency rejection of the quantization noise inserted at the output of the modulator. Returning to the linearized model of figure 3.23, a relation can be established between the injected quantization noise, $Q(z)$, and its effect at the output of the modulator:

$$H_Q(z) = \frac{1 - z^{-1}}{1 + (A_1 K_1 G_{comp} - 1) z^{-1}} \qquad [3.25]$$

As expected, the transfer function has a high pass characteristic.

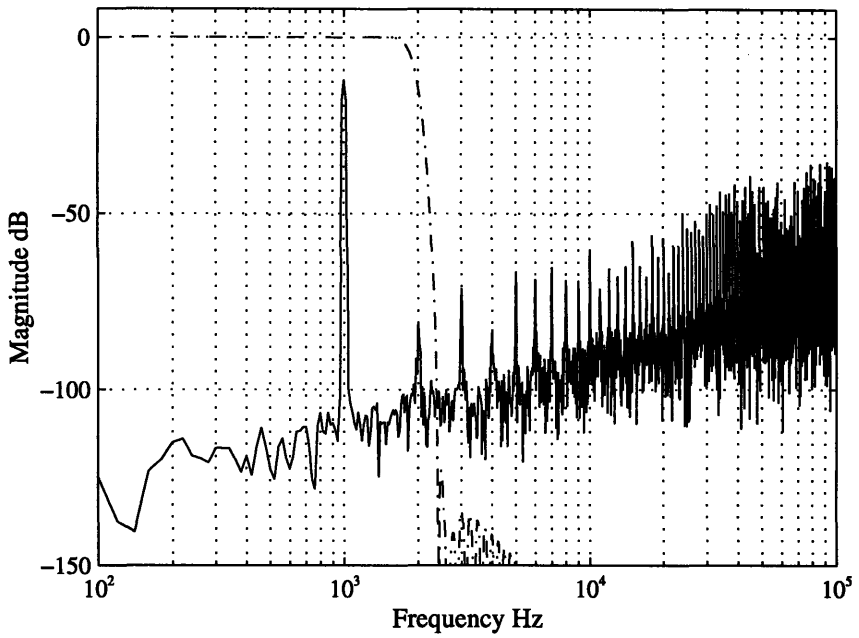


Figure 3.24 Output spectrum of first order modulator

Because the quantization noise is placed mostly at frequencies well above baseband, the decimation filter at the output of the modulator removes all but a small portion of the quantization noise from the digital output. The decimation filter is implemented using a "brick wall" filter which rolls off sharply above baseband in order to minimize noise at the output[44]. Figure 3.24 shows a sample output spectrum from the first order modulator with a low frequency sinusoidal input[45]. The input signal is seen as the "spike" at 1kHz. Quantization noise and tones form the remaining signal components which dominate the spectrum at higher frequencies. A sample decimation characteristic is also shown. The sharp rolloff of the decimation filter at 2kHz rejects all but a small fraction of the quantization noise of the modulator.

44. Typically the decimation filter lowers the data rate from the sampling frequency of the modulator to the Nyquist frequency for the baseband while simultaneously increasing the data stream from 1-bit to the n-bit resolution of the modulator.

45. Here, the modulator is clocked at 1MHz.

The quantization noise present in baseband sets a lower bound on the attainable resolution of the modulator. To determine the quantization noise floor, the total quantization noise power in the baseband, P_B, is calculated [25]:

$$P_B = \int_0^{f_B} |H_Q(f)|^2 |Q(f)|^2 df \qquad [3.26]$$

where f_B is the cutoff filter of the decimation filter and $Q(f)$ is quantization noise. The quantization noise is modelled as an additive white noise source with a magnitude [25]:

$$|Q(f)| = \sqrt{\frac{\sigma}{6f_s}} \qquad [3.27]$$

where f_s is the sampling frequency of the modulator and σ is the quantizer step size[46]. Once the total quantization noise power in baseband has been obtained, the quantization noise floor is calculated by solving for the rms equivalent noise:

$$\overline{q_n} = \left[\int_0^{f_B} |H_Q(f)|^2 |Q(f)|^2 df \right]^{1/2} \qquad [3.28]$$

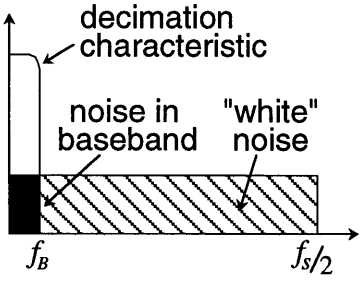


Figure 3.25 Reduction of noise using oversampling

As stated before, quantization noise is not the only noise reduced by the decimation filter. Circuit noise shows up at the output as well[47]. Like quantization noise, a large portion of the circuit noise is removed by the decimation filter. Figure 3.25 illustrates how

46. In the prior example, f_s was 1MHz and σ was $2V_{ref}$.

47. Circuit noise includes thermal noise from the amplifiers and switches as well as deterministic noise which includes feedthrough from the clock, power supply, and substrate.

oversampling reduces the effects of circuit noise. "White" noise such as thermal noise from the amplifiers or kT/C noise is spread across the frequency range from DC to half the sampling frequency of the modulator ($f_s/2$). When the decimation filter rejects all frequencies outside of baseband, only a small fraction of the circuit noise remains in the post-filtered output. For "white" noise, the total noise power is reduced by half the oversampling ratio [27].

It might seem there is no reason for any modulator other than a first order modulator. One can simply increase the oversampling ratio of the modulator until the total noise power in baseband is reduced enough to attain the desired resolution. However, this approach has practical limitations. For any given technology, there will eventually be a speed limitation such that the modulator's sampling frequency cannot be further increased. In addition, a more subtle problem which occurs in first order modulators is the presence of "tones" in the output spectrum. Tones are periodic bit sequences which result from limit cycles in response to certain inputs. If the period of one of these bit sequences is fairly long, a tone can show up at frequencies low enough to be passed by the decimation filter and be erroneously interpreted as part of the input signal to the modulator.

As an example, if 0V were input into the first order modulator, the output would oscillate back and forth between "0" and "1" producing a tone with a period of two cycles. In this case, the tone would show up at half the sampling frequency and be well above baseband. If, on the other hand, the input were $+(1/119)V_{ref}$ (for example), a limit cycle would result with a period of 119 bits (60 "1s", 59 "0s"). The resulting oscillations would show up at 1/119th of the sampling frequency and be passed through the decimation filter[48].

A second integrator in the forward path of the modulator reduces both the quantization noise present in baseband and the likelihood of tones in the output spectrum. By increasing the low frequency loop gain of the modulator, the second integrator reduces the quantization noise transfer function at low frequencies. Accordingly, the quantization

48. The process of "dithering" is sometimes used to remove undesired tones [30]. By adding a small pseudo-random noise to the modulator, the likelyhood of tones can be reduced.

noise present in baseband is reduced from that of the first order modulator operating at the same sampling rate. Thus, a small increase in circuit complexity is traded for reduced quantization noise and a reduced probability of tones in the output spectrum. Tones, however, can still be a significant problem in second order modulators.

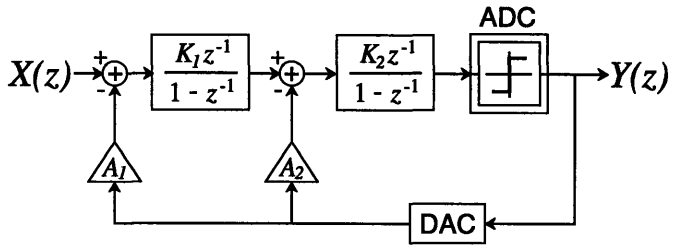


Figure 3.26 Second order modulator

A second order Δ-Σ modulator is shown in figure 3.26. This modulator is said to have a "distributed feedback" topology. The advantage of this topology over most other topologies is the singular feedback to the "critical node". The critical node denotes to the first summing node which is connected to the input. Any noise present at this node is referred directly to the input. The input referred noise from any other node in the modulator is desensitized by the gain of at least one integrator. Other topologies [31,32] may have several feedback paths to the critical node, all of which are possible noise sources.

Like the first order modulator, the output of the second order modulator is valid for all inputs between $+V_{ref}$ and $-V_{ref}$. Likewise, if the input range is violated, the output from the modulator is temporarily invalid until the input voltage returns to within the valid input range.

The second order modulator can be linearized by approximating an effective gain for the comparator in the same fashion as the single order modulator. The quantization and forward transfer characteristics derived from the linear model are given by:

$$H_X(z) = \frac{K_1 K_2 G_{comp} z^{-2}}{1 + (A_2 K_2 G_{comp} - 2)z^{-1} + (1 + K_2 G_{comp}(A_1 K_1 - A_2))z^{-2}} \quad [3.29]$$

$$H_Q(z) = \frac{(1 - z^{-1})^2}{1 + (A_2 K_2 G_{comp} - 2)z^{-1} + (1 + K_2 G_{comp}(A_1 K_1 - A_2))z^{-2}} \quad [3.30]$$

where the integrator coefficients, K_i, and feedback coefficients, A_i, are determined by circuit parameters. A sample second order output spectrum is shown in figure 3.27.

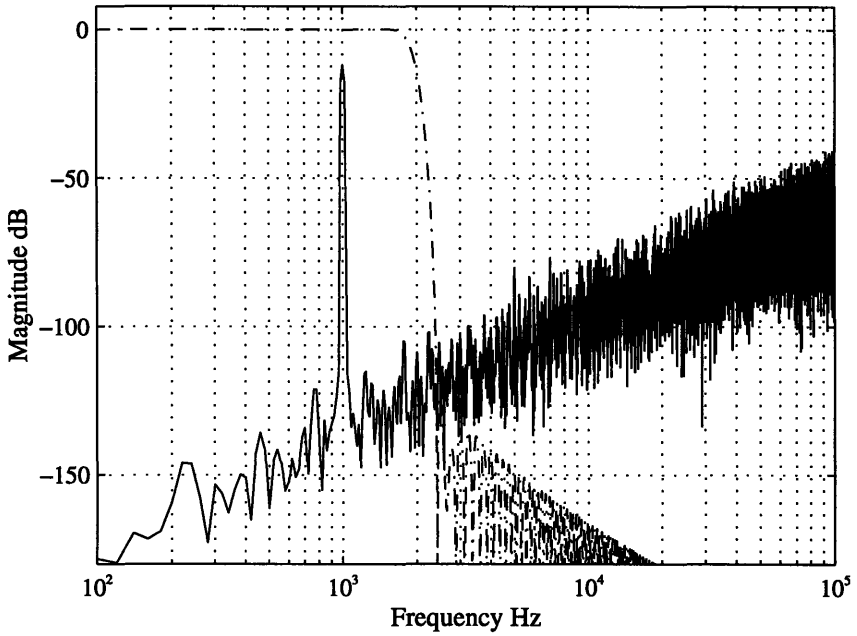


Figure 3.27 Output Spectrum of the second order Δ-Σ modulator

Modulator order	Sampling rate, f_s	Oversampling Ratio (OSR)	Quantization noise, n_{rms}
First	1MHz	200	1.7mV
Second	1MHz	200	167μV
Second	500kHz	100	933μV

Table 3.2 Quantization noise vs. modulator order

As a way of comparing the first and second order modulators, the baseband quantization noise can be calculated for each. As before, the sampling frequency for the modulators is 1MHz and baseband signal, 5kHz. Let σ, the difference in quantizer levels[49], be 10V. Using equations 3.26 - 3.28, the quantization noise in baseband, $\overline{q_n}$, was calculated

49. The following coefficient values were used for the baseband quantization noise calculation:
$A_1 = 0.0834, A_2 = 0.350, K_1 = 0.893, K_2 = 0.300, G_{comp1} = 13.0, G_{comp2} = 10.8.$
The effective comparator gains were determined through simulations.

to be 1.7mV for the first order modulator and only 167μV for the second order modulator. If the sampling rate of the second order modulator is decreased to 500kHz, the quantization noise of the modulator rises to 933μV, still below the quantization noise floor of its first order counterpart. These results are summarized in table 3.2.

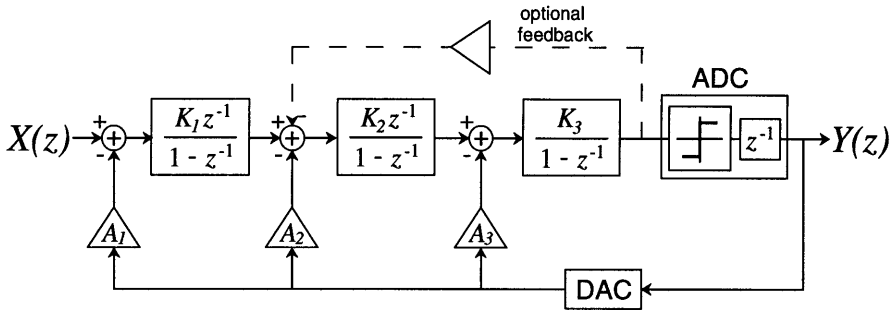


Figure 3.28 Third order Δ-Σ modulator

The third order Δ-Σ modulator selected for use in the accelerometer is shown in figure 3.28 [25]. The third order topology ensures low quantization noise and greatly reduces the likelihood of tones in the output spectrum.

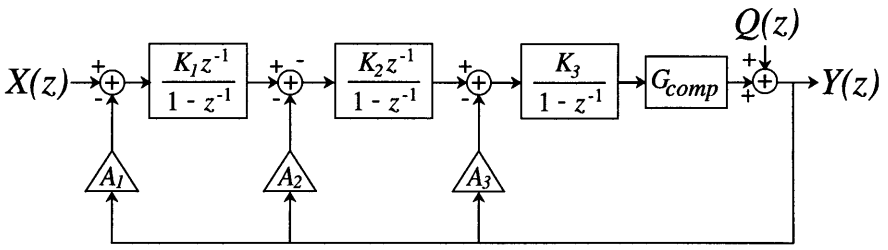


Figure 3.29 Linearized third order model

The linearized model for the third order modulator is shown in figure 3.29. Solving the linearized model as before, the output of the modulator can be expressed as a combination of response to the input, *X(z)*, and the quantization noise injected at the output of the modulator, *Q(z)* [25].

$$Y(z) = H_X(z)X(z) + H_Q(z)Q(z) \qquad [3.31]$$

where

$$H_X(z) = \frac{K_1 K_2 K_3 G_{comp} z^{-3}}{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \alpha_3 z^{-3}} \quad [3.32]$$

$$H_Q(z) = \frac{(1 - z^{-1})^3}{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \alpha_3 z^{-3}} \quad [3.33]$$

$$\alpha_1 = A_3 K_3 G_{comp} - 3 \quad [3.34]$$

$$\alpha_2 = (A_2 K_2 - 2A_3) K_3 G_{comp} + 3 \quad [3.35]$$

$$\alpha_3 = ((A_1 K_1 - A_2) K_2 + A_3) K_3 G_{comp} - 1 \quad [3.36]$$

The integrator coefficients, K_i, and feedback coefficients, A_i, are set by capacitor ratios in the circuit implementation of the modulator.

The forward transfer function of the modulator, $H_X(z)$, has a third order lowpass characteristic and the quantization noise transfer function, $H_Q(z)$, a third order highpass characteristic. The pole locations of $H_X(z)$ and $H_Q(z)$ are determined by the feedback coefficients of the modulator and are selected to optimize performance of the converter.

The three zeros of the noise transfer characteristic are all located at DC. An optional feedback path around the second and third integrators (figure 3.28) can be used to form a resonator in the forward path of the modulator. The optional resonator moves two of the zeros in the noise transfer function away from DC to form a low frequency complex conjugate zero pair. Figure 3.30 illustrates the effect of a complex zero pair placed at 5kHz. Note the notch in the output spectrum resulting from the low frequency resonator. With careful placement of the zero pair, the quantization noise can be further reduced and the rolloff requirements for the decimation filter can be relaxed.

In the final design of the modulator, it turned out to be impractical to implement the low frequency zero pair due to circuit limitations. With a baseband of 1.0kHz and a sampling rate of 500kHz, very large capacitance ratios would have been necessary (>>200) to place the low frequency zero pair at or below 1.0kHz. A complex zero pair placement at frequencies higher than 1.0kHz would result in more baseband quantization noise than with all three zeros placed at DC. For this reason, the DC zero placement was selected.

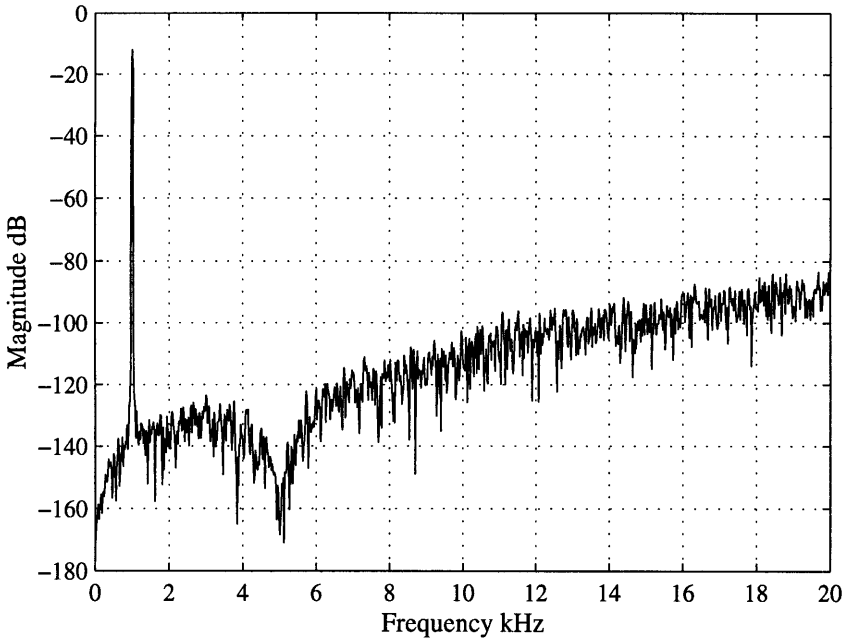


Figure 3.30 Output spectrum with low frequency resonator

Unlike the first and second order Δ-Σ modulators, the output of the third order modulator is not valid over the full $-V_{ref}$ to $+V_{ref}$ input range. Outside of a given input range which usually ranges from 40% to 60% of the DAC output value, the third order modulator goes unstable due to comparator overload. Once this occurs, the modulator cannot return to stable operation on its own even after the input voltage returns to its valid input range. For this reason, the integrators are reset after out of range input excursions and at startup. Thus, the third order modulator trades increased design complexity and reduced input range for lower quantization noise and increased immunity to tones in the output spectrum.

Design of the Modulator

The first step in the design of the modulator is choosing its pole locations. Two types of filters were considered for implementing the transfer function of the modulator, a Butterworth filter and an elliptic (or Cauer) filter. A Butterworth filter is maximally flat in both the passband and stopband. The tradeoff for this maximally flat transfer characteristic is a relatively slow rolloff in the transition band as compared to the elliptical filter. The

elliptical filter sacrifices monotonicity in the passband and stopband to produce a very sharp rolloff in the transition band.

In designing a Δ-Σ modulator for an application such as the open loop data conversion system diagrammed in figure 3.19, issues such as passband ripple could play a significant role in choosing the pole locations, and thus filter type for the modulator. If a maximally flat transfer characteristic were required, the Butterworth filter would be used for the pole placements of the filter. However, because here the modulator is used within a closed loop system, the design issues are somewhat different. The modulator should not be designed as a separate entity with the single function of digital-to-analog conversion, but rather as a minor loop in a larger closed loop system.

Because the poles of the modulator are placed well above the crossover frequency of the accelerometer[50], any passband ripple from the modulator will be placed predominantly at frequencies well above the bandwidth of the closed loop system. Even if the modulator's poles were located near the system crossover frequency, the closed loop effects of a small variance in gain would be negligible due to the large gain of the lag compensation. Thus, passband ripple is not a valid design criterion for choosing between the elliptical or Butterworth filter designs.

In an attempt to minimize the negative phase shift of the Δ-Σ modulator at system crossover, an elliptic filter was chosen to place the poles of the modulator. By placing the poles close to the unit circle, the elliptic filter has a very slow rolloff in phase until the pole frequencies are reached. At this point, the phase drops off sharply. Because the accelerometer's crossover is well below the pole frequencies of the Δ-Σ modulator, the negative phase shift associated with the elliptic modulator is less than that of the Butterworth implementation in the region of system crossover.

While the robustness of the close loop accelerometer may be increased using the elliptic pole placement for the modulator, the stability of the modulator itself is reduced. A modulator designed with Butterworth pole placements is much less sensitive to coeffi-

50. The poles of the modulator are placed near 45kHz. Recall the crossover frequency of the accelerometer is placed at 4.5kHz.

cient mismatches than a modulator designed with elliptic pole placements [25]. With a relatively close placement of its poles to the unit circle, a modulator designed with elliptic pole placements requires a much smaller coefficient error to cause instability. However, since the coefficients of the modulator are set by capacitor ratios with better than 8-bit matching, the stability of the modulator should not be an issue[51].

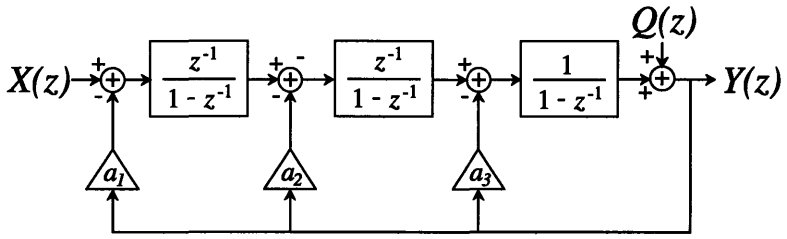


Figure 3.31 Simplified linear third order model

In order to facilitate design of the modulator, the system diagram of figure 3.29 is simplified such that all integrator coefficients, K_i, and the effective comparator gain, G_{comp}, are set to unity. The simplified system diagram is shown in figure 3.31 and is governed by the set of equations:

$$H_X(z) = \frac{z^{-3}}{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \alpha_3 z^{-3}} \quad [3.37]$$

$$H_Q(z) = \frac{(1 - z^{-1})^3}{1 + \alpha_1 z^{-1} + \alpha_2 z^{-2} + \alpha_3 z^{-3}} \quad [3.38]$$

where

$$\alpha_1 = a_3 - 3 \quad [3.39]$$

$$\alpha_2 = a_2 - 2a_3 + 3 \quad [3.40]$$

$$\alpha_3 = a_1 - a_2 + a_3 - 1 \quad [3.41]$$

51. Since the modulator is part of a larger loop, the third order modulator does not actually need to be stable for the closed loop accelerometer to be stable. However, to simplify design and testing, the use of an unstable modulator was not investigated in this research,.

These equations can be obtained directly from equations 3.32-3.36 by setting all the K_i terms to unity and assuming a comparator gain of 1.0.

MATLAB® was used to generate third order elliptic filter pole locations. Equations 3.37-3.41 were then used to evaluate the feedback coefficients necessary to implement the desired pole locations. CLASP was used to simulate functionality of modulator with each given set of coefficients. The design process was repeated iteratively until an optimal design was achieved. The pole placements for the final modulator design are given by:

$$\begin{aligned} p_1 &= 0.6924 + j0.4111 \\ p_2 &= 0.6924 - j0.4111 \\ p_3 &= 0.5752 \end{aligned} \qquad [3.42]$$

From this set of pole locations, values for α_1, α_2, and α_3 were calculated:

$$\begin{aligned} \alpha_1 &= -1.96 \\ \alpha_2 &= 1.445 \\ \alpha_3 &= -0.373 \end{aligned} \qquad [3.43]$$

Using equations 3.39-3.41, an initial set of values is calculated for the a_i coefficients:

$$\begin{aligned} a_1 &= 0.112 \\ a_2 &= 0.525 \\ a_3 &= 1.04 \end{aligned} \qquad [3.44]$$

At this stage in the design, the pole placements of the modulator were selected and the operation verified with simulation. The forward transfer characteristic of the modulator, $H_X(z)$, is given by

$$H_X(z) = \frac{z^{-3}}{1 - 1.96z^{-1} + 1.445z^{-2} - 0.373z^{-3}} \qquad [3.45]$$

The next step in the design of the modulator is scaling the integrator and feedback coefficients. The loop dynamics of the modulator are not changed with proper scaling of

the integrator and feedback coefficients, only the closed loop gain of the modulator is altered. Scaling is done as a means of reducing the required output swing from the integrators and adjusting the DC gain of the modulator.

The DC gain of the modulator is calculated from equation 3.37 to be:

$$H_X(z)\Big|_{z=1} = \frac{1}{a_1} = \frac{1}{0.112} = 8.93 \qquad [3.46]$$

Thus, the DC gain of the modulator is set by the a_1 (A_1) feedback coefficient alone. In a typical analog-to-digital conversion application, the modulator is usually designed to have unity gain. However, because this modulator is to be used in a closed loop application, it turns out to be advantageous to increase the low frequency gain as a means of raising the total loop gain. This, in turn, relaxes the gain requirements for other circuits within the accelerometer. Once the DC gain of the modulator has been selected, the value of feedback coefficient A_1 is constrained.

When the feedback coefficients of the modulator were initially selected and corresponding simulations were performed, no consideration was given to the output swing of the discrete-time integrators. To simplify the design process, it was assumed initially that the output range of the integrators was infinite. As a result, the required output swing from the modulator's integrators would be quite large for the unscaled modulator. The simulated output swing for the three integrators is shown in figure 3.32 for an 80mV DC input to the modulator. Due to the finite output swing capabilities of the amplifiers used to implement the modulator, clipping would occur in the discrete-time integrators. The loss of state information which occurs as a result of clipping can lead to instability [25]. For this reason, the integrator coefficients are scaled to reduce the required output swing from the amplifiers. The output swing of the integrators in the scaled modulator is shown in figure 3.33. Note the marked decrease in output voltage swing of the integrators.

When an integrator coefficient, K_i, is decreased or A_1 is adjusted, other coefficients within the modulator must be scaled accordingly to preserve the loop dynamics. One way of scaling coefficients is to make sure that the three loops of the modulator[52] maintain a constant gain. For example, if K_1 were decreased by a factor of two, K_2 should be

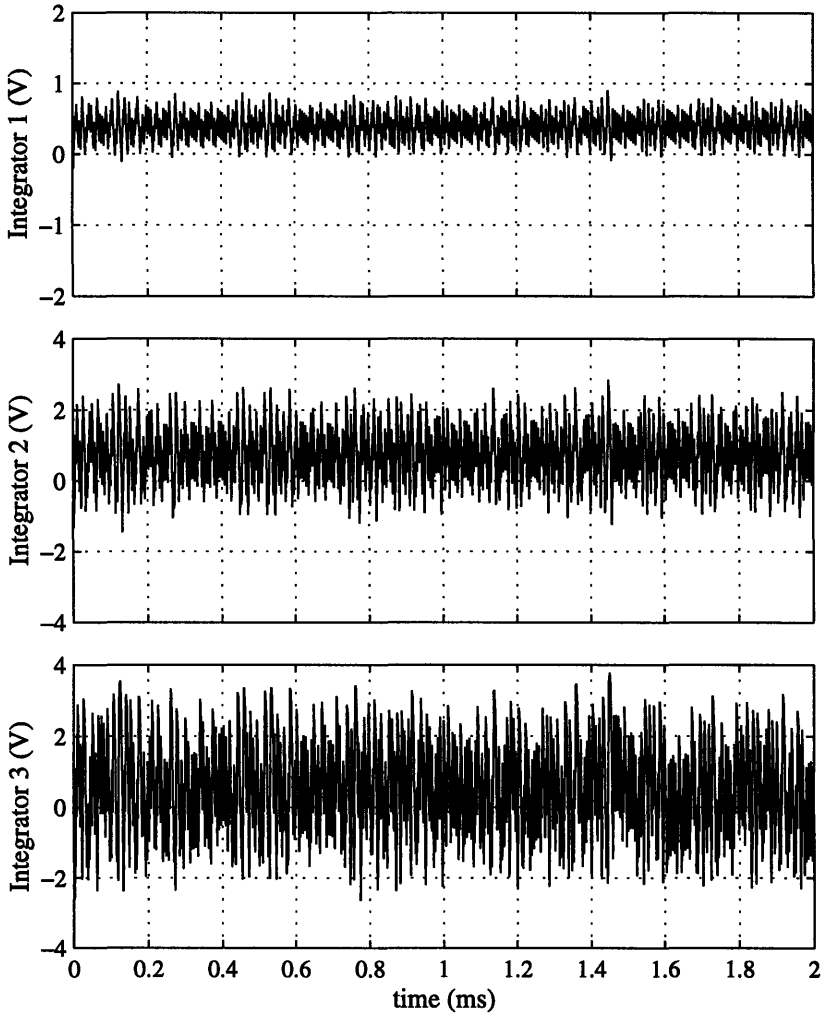


Figure 3.32 Integrator output swing for the unscaled modulator

increased by a factor of two to preserve the gain of the outer (3 integrator) loop. Because K_2 is also in the second (2 integrator) loop, A_2 should be decreased by a factor of two to maintain constant gain in the second loop. An alternate way to scale the coefficients is to match the denominators of equations 3.32 and 3.37:

52. The modulator has three loops, the first goes only around the third integrator, the second goes around the second and third integrators, and the last loop includes all three integrators. It is important to note that G_{comp} varies inversely with K_3. If K_3 is increased by a factor of two, G_{comp} will decline by 50%. Similarly, scaling A_3 and K_2 affect the value of G_{comp} in the same way. If both A_3 and K_2 are increased by a factor of two, its identical to increasing the value of K_3 from the standpoint of the comparator. For this reason, A_3 and K_2 should be scaled together.

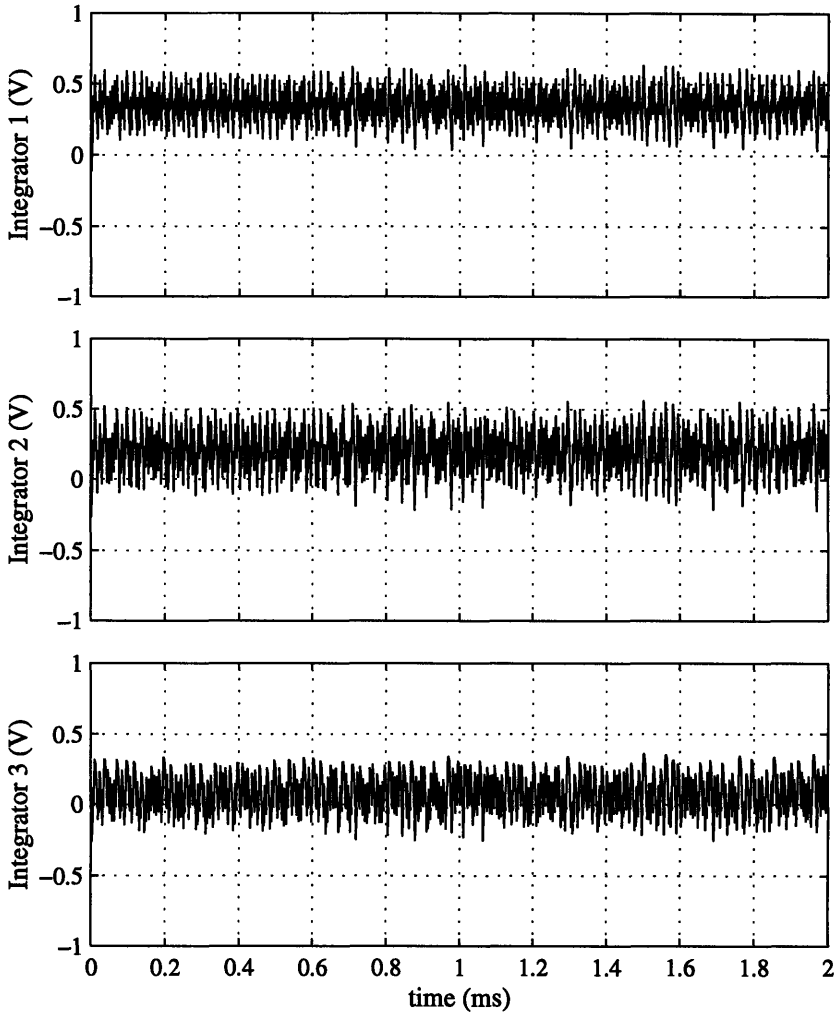


Figure 3.33 Integrator output swing in the scaled modulator

$$a_3 = A_3K_3G_{comp} \quad [3.47]$$

$$a_2 = A_2K_2K_3G_{comp} \quad [3.48]$$

$$a_1 = A_1K_1K_2K_3G_{comp} \quad [3.49]$$

where the lower case literals, a_i, represent the unscaled modulator coefficients. The two scaling methods produce identical results, however, the first method is more intuitive.

After scaling, the forward transfer characteristic of the modulator is given by:

$$H_x(z) = \frac{1.343z^{-3}}{1 - 1.96z^{-1} + 1.445z^{-2} - 0.373z^{-3}} \quad [3.50]$$

Note equations 3.50 and 3.45 only differ by a scale factor in the numerator. The final modulator design has a DC gain[53] of 12 which constrains the A_1 coefficient to a value of 0.08. The coefficient values of the modulator are given in table 3.3.

A sample output spectrum from the scaled modulator is shown in figure 3.34. The input to the modulator is a 0.03 V_{ref} sinusoid at 1kHz.

Feedback coefficients		**Integrator coefficients**	
A_1	0.0834	K_1	0.893
A_2	0.350	K_2	0.300
A_3	0.208	K_3	0.500

Table 3.3 Final coefficient values

3.4.2 The Fifth Order Model

The fifth order accelerometer is shown in figure 3.35[54]. Inspecting the electromechanical modulator, it is almost identical in topology to the 3rd order distributed feedback system shown in figure 3.28. The only differences are the added loop compensation and the lack of feedback to the output of the first mechanical integrator. Intuitively, this makes sense. Feedback is not possible to the output of the first mechanical integrator which makes compensation necessary to stabilize the loop. Because the accelerometer system can be accurately modelled as a fifth order Δ-Σ modulator, analysis of its nonlinear behavior can be greatly simplified by using well established Δ-Σ theory.

53. The stable input range to the modulator scales inversely with DC gain. If the modulator gain is increased by a factor of 5, the input range decreases by a factor of 5. Similarly, a larger stable input range can be attained by reducing the DC gain below unity.

54. This model is no different from the model shown in figure 1.3 except now all the feedback paths are drawn explicitly.

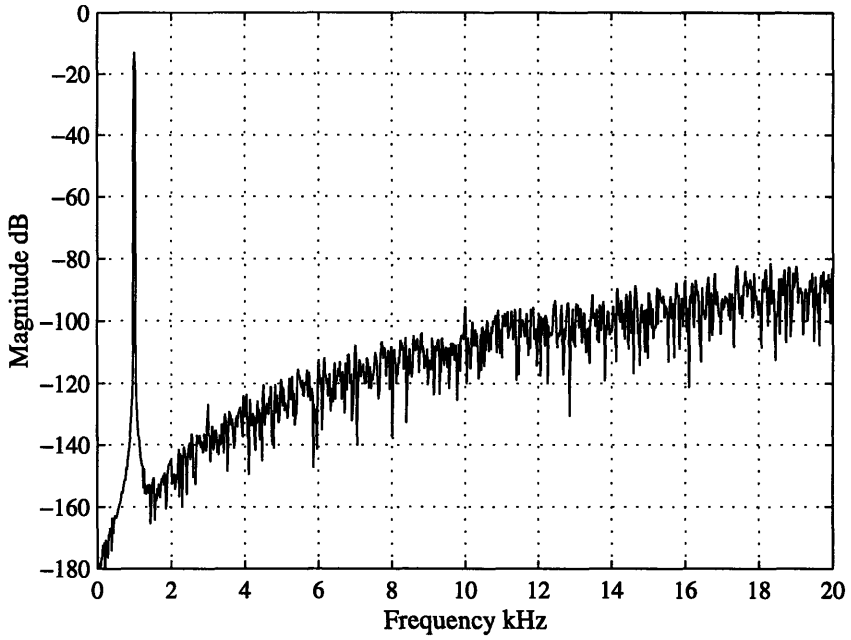


Figure 3.34 Modulator output spectrum for 0.03 V_{ref} sinusoidal input

3.4.3 Choosing the Feedback Force

The feedback force used for accelerometer was not chosen arbitrarily, but rather it was selected to provide the maximum resolution possible over the desired input range of the modulator. The stable input range of a Δ-Σ modulator usually ranges from 40% to 60% of the DAC output value. Because the quantization noise power of the modulator is proportional to the DAC feedback voltages (equation 3.27), the DAC outputs should be set to approximately twice the desired input range in order to attain the highest resolution possible without compromising the stable input range of the modulator.

Using the input range of the accelerometer, ±2g, the feedback force was selected to be ±4g. Because the feedback force is only applied when the C-V sense is inactive, a ±8g force is actually applied during feedback to generate the desired net restoring force. Using CLASP simulations, the stable input range of the modulator was verified to be exactly ±2g.

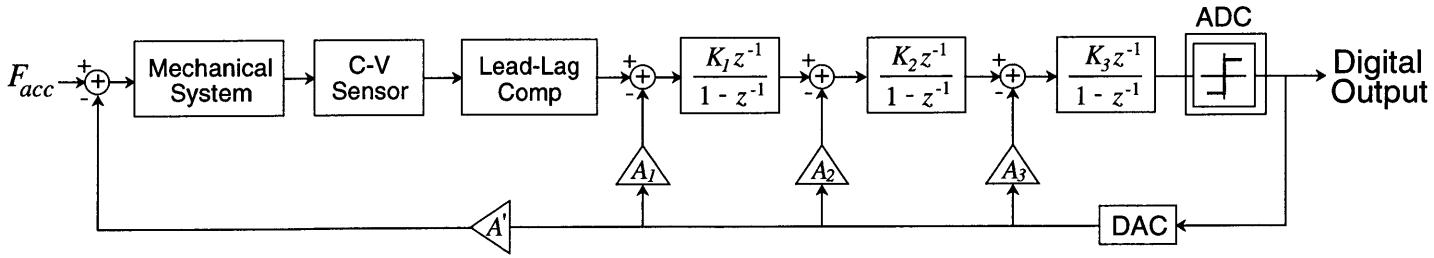


Figure 3.35 The Fifth Order Modulator

3.4.4 Spring and Damping Nonlinearity

Harmonic distortion can show up at the output of a Δ-Σ modulator as a result of nonlinear capacitors. If the input capacitance of the first stage has a voltage dependance, the output spectrum of the modulator will have distortion at multiples of the input frequency. Other nonlinear capacitors in the modulator result in errors as well, however their effects are reduced by the gain of the first modulator.

Similar to the nonlinear capacitors in the circuit implementation of a Δ-Σ modulator, nonlinearities can result in harmonic distortion at the output of the accelerometer. Since of the high linearity of the mechanical structure, the nonlinearity of the mechanical spring is below 10ppm over the closed-loop deflection range of the proof mass [2]. Because this nonlinearity is located within a closed loop, it is reduced by the open loop gain of the system. Simulations produced harmonic distortion more than 100dB below the input signal level with mechanical spring nonlinearities as high as 10% (10,000ppm!). Like the mechanical system, the nonlinear terms derived for the ΔC-to-Δx conversion which takes place in the C-V sensor (equation 3.7) can also result in harmonic distortion. Since the C-V sensor is also located within the loop, the effect of this nonlinearity is also decreased by the open loop gain of the system.

In addition to the nonlinearity of the mechanical spring, there is a nonlinearity associated with the electric spring, K_{EL}, which must also be taken into account. As discussed in section 3.3, the electric spring force, K_{EL}, is comprised of two components, one which is related to the applied feedback voltages and one component which results from the voltages applied during the capacitance sense. Previously, equation 3.19 gave the relation between the feedback and sense voltages and the electric spring constant, K_{EL}. Including two higher order terms, the electric spring constant is more accurately modelled by:

$$K_{EL} \approx \eta(\Phi_1)\frac{2\varepsilon_o A}{d^3}\left(V_{DC}^2 + V_{DIFF}^2 - 3\left(\frac{x}{d}\right)V_{DC}V_{DIFF} + 2(V_{DC}^2 + V_{DIFF}^2)\left(\frac{x}{d}\right)^2\right) \qquad [3.51]$$

$$+ \quad \frac{\varepsilon_o A}{d^3}[\eta(\Phi_2)V_{tune}^2 + \eta(\Phi_3)V_1^2 + \eta(\Phi_4)V_2^2]\left(1 + 2\left(\frac{x}{d}\right)^2\right)$$

The top part of equation 3.51 results from the feedback voltages and the bottom part of the equation results from the capacitance sense voltages. The two components of the electric spring constant have a very different effect at the output. The nonlinearity which results from the feedback voltages is identical to having an error in the feedback force. Thus, the feedback nonlinearity which is dominated by its first order term shows up as harmonic distortion directly at the output of the accelerometer. Since it is not within the loop, no rejection is provided by the loop gain. In contrast, the nonlinearity associated with the C-V sense is not part of the feedback loop, but rather it is grouped with the mechanical system in he forward gain part of the system. Thus, the portion of the electric spring nonlinearity which results from the sense voltages is reduced by the gain of the loop.

To illustrate the effect of the feedback nonlinearity, the output spectrum of the accelerometer is shown in figure 3.36 for a 2.0g sinusoidal input at 300Hz. Distortion can be seen at the third harmonic located 96dB down from the input signal. If the positional dependance of the feedback force is removed from the simulator, the third order harmonic becomes obscured by the quantization noise floor.

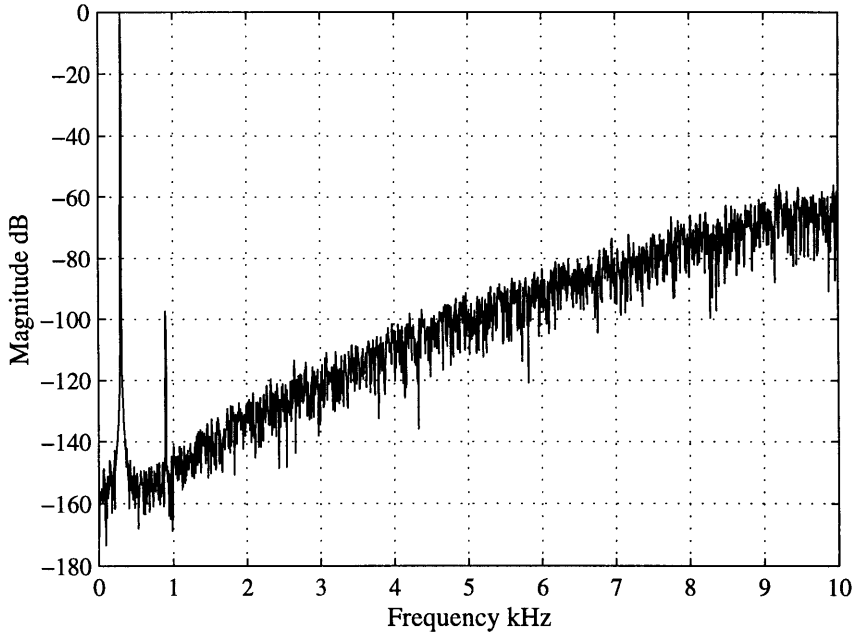


Figure 3.36 Output spectrum w/ odd harmonic distortion

Since the motion of the proof mass is restricted, the effect of the nonlinearity in damping force was found to be negligible. The nonlinearity in damping is largest when the proof mass is at its farthest point from equilibrium. However, at this same point the velocity is approaching zero and thus the damping force is at its lowest point. Simulations produced no noticeable harmonic distortion or error resulting from damping nonlinearity. Also note that there is a very low level of damping due to the vacuum packaging of the mechanical system.

3.4.5 The Startup Problem

Since the Δ-Σ modulator is a nonlinear system, the stability analysis which generated its design is only valid over a limited range of operation. This is the reason for the limited stable input range of the third order Δ-Σ modulator. When the input to the modulator grows to large, the incremental assumptions which were used to design the modulator no longer hold and the modulator becomes unstable. Similarly, instability can occur if the output values of the electrical or mechanical integrators of the accelerometer are outside of a limited range. This could be as a result of an out of range input excursion or initial startup conditions. For this reason, the electrical integrators of a Δ-Σ modulator are reset at startup and after any out of range excursions. Similarly the mechanical integrators of must be reset as well. Unfortunately, there is no simple way to reset the two integrators of the mechanical system. The next section presents the solution which was used to solve this problem.

3.5 The Reset Loop

Because the mechanical integrators cannot be reset by merely closing a switch (as with the electrical integrators), a more elaborate method must be used. The mechanical system, diagrammed in figure 3.37, shows the state variables associated with the two mechanical integrators. The output of the first integrator is the velocity of the proof mass, and the second integrator, its position. The velocity and position of the proof mass do not

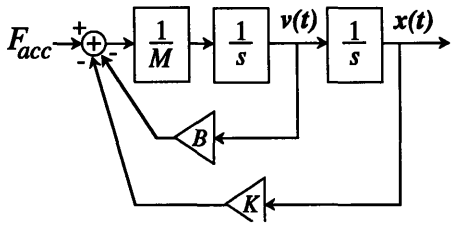


Figure 3.37 The mechanical integrators

need to be set exactly to zero to assume stable operation, however the proof mass must be within a few angstroms of its zero deflection point and the velocity should be no more than about 30μm/second.

Figure 3.38 shows the deflection of the proof mass with 0g input to the accelerometer, zero initial velocity, and 70 Å initial deflection. It is clear from the movement of the proof mass, the accelerometer never assumes stable operation.

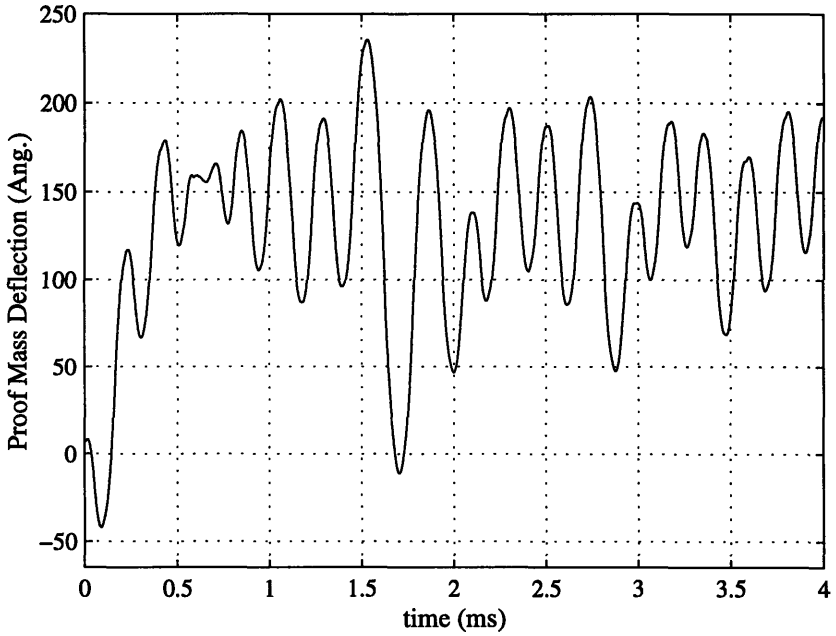


Figure 3.38 Proof mass deflection with 70Å initial deflection

In contrast, figure 3.39 shows proof mass deflection for a 0g input, zero initial velocity, and 50Å initial deflection. This time, the accelerometer readjusts and brings the proof mass to its equilibrium position. Through simulations, it was found that there is a

small range of initial deflections and initial velocities for which the fifth order system can reset the proof mass without going unstable. As with the noise immunity of the loop, a lower system bandwidth provides a greater tolerance for initial offsets in the position and velocity of the proof mass. This is another reason why a low system crossover is desired.

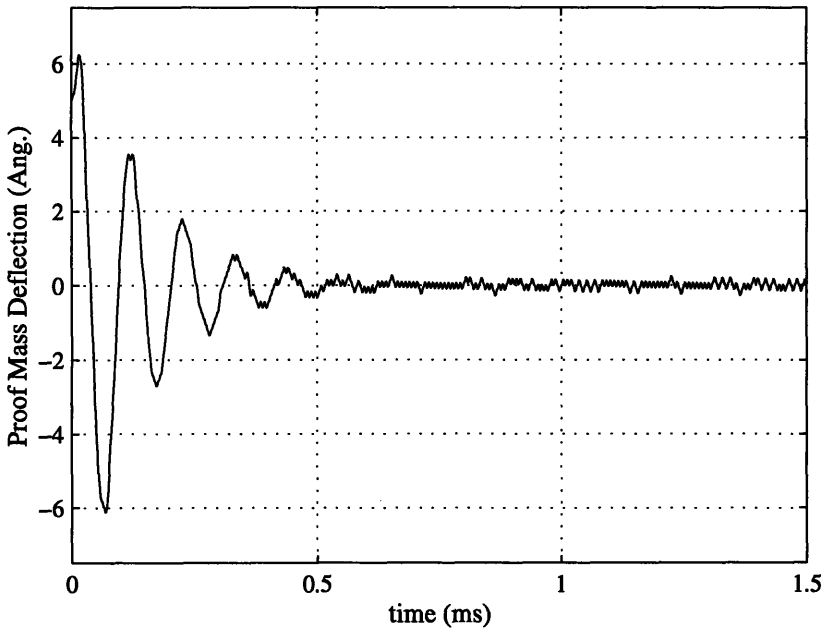


Figure 3.39 Proof mass deflection with 50 Å initial deflection

As a means of bringing the proof mass within the stable startup range of the accelerometer, a second order reset loop is used. The second order loop uses the same C-V sensor used in the fifth order (main) loop. The output of the C-V sensor is passed to a simple proportional-plus-derivative (P+D) compensation which is then input to the same comparator as used by the fifth order loop. This second order implementation is diagrammed in figure 3.40. Note the minimal extra circuitry necessary to add the second order loop to the accelerometer. The switching between the main loop and second order "reset" loop is performed simply by switching the input to the comparator between the output of the third integrator of the Δ-Σ modulator to the output of the P+D compensation.

The second order system has three modes of operation. The first mode of operation is that of a second order electromechanical Δ-Σ modulator. Mode II is a linear decay mode which slowly removes kinetic energy from the proof mass as it oscillates about its

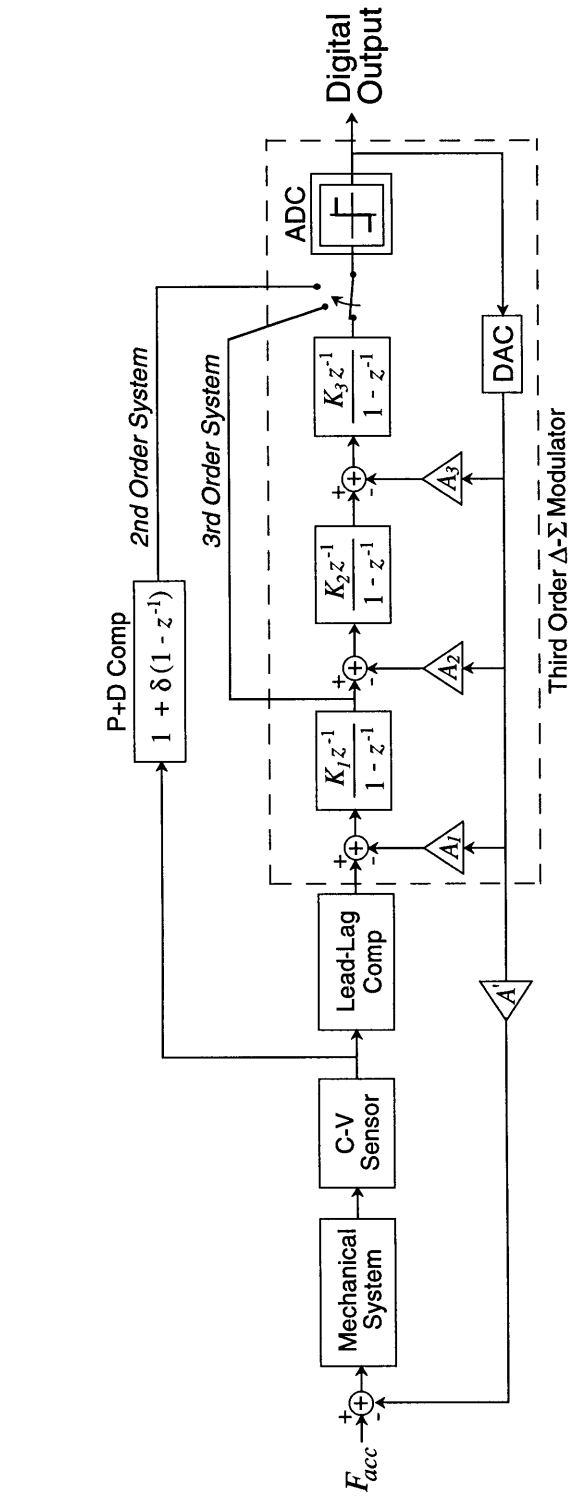


Figure 3.40 Integrating the Third Order System

zero deflection point. In the third mode of operation, the proof mass is placed too close to the fixed electrodes to "escape" the electrostatic force from the applied voltages and electrostatic "pull-in" occurs.

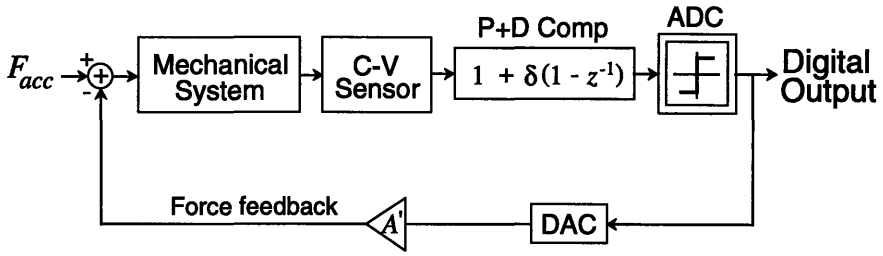


Figure 3.41 Second order electromechanical Δ-Σ modulator

Mode I operation, that of a second order electromechanical modulator (figure 3.41), is nearly identical to the second order Δ-Σ (electrical) modulator shown in figure 3.26. As with the fifth order system, feedback is not possible to the output of the first mechanical integrator (velocity feedback), thus an exact distributed feedback topology is not possible. The P+D compensation approximates velocity feedback by feeding back a derivative term to the input of the first integrator.

Note a stable second order system could also have been implemented by placing the P+D compensation in the feedback path instead of the forward path of the loop. This approach, however, has two drawbacks. First, separate feedback circuitry would be necessary to implement the feedback to the proof mass. By placing the P+D compensation in the forward path of the loop, the second order system utilizes the same feedback circuitry as the main (fifth order) system. The second drawback to using compensation in the feedback path is the complicated closed loop transfer characteristic of the system. Because of the derivative term in the feedback path, the relationship between the input and output of the system is no longer a simple scalar function. By implementing the compensation in the forward path of the system, the second order system has an identical low frequency transfer characteristic to the fifth order loop. Thus, the output of the accelerometer is still valid during operation of the reset loop, the only difference being the increased quantization noise present during second order operation. The incremental dynamics of the main

loop still hold for the reset loop, thus the input referred circuit noise for the second order loop is identical to that of the fifth order loop.

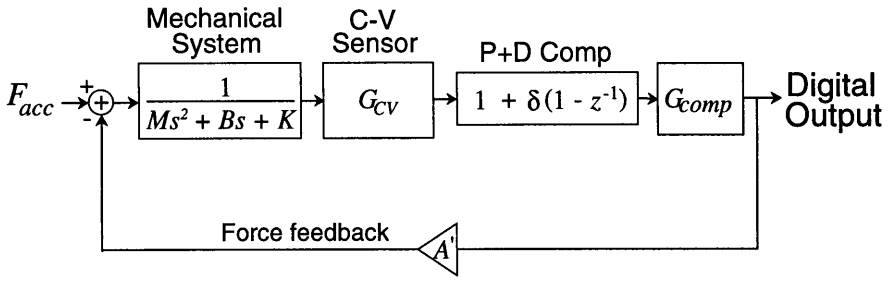


Figure 3.42 Linearized reset loop

The dynamics of the reset loop can be linearized in the same manner as the fifth order loop. The linearized model for the reset loop is shown in figure 3.42. The effective gain of the comparator, G_{comp}, was established through simulation. The loop gain and magnitude of the system is plotted in figure 3.43.

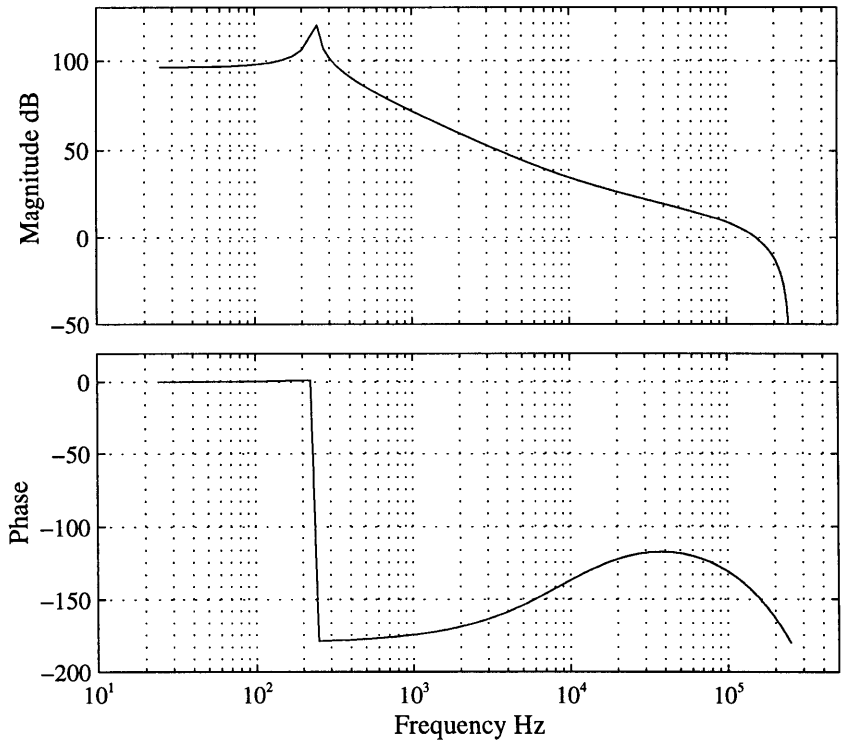


Figure 3.43 Second order loop dynamics

As with the main system loop, the second order modulator is stable only when the proof mass is within a certain vicinity of its equilibrium position. For the reset loop, this turns out to be within approximately ±20Å of zero deflection with zero velocity[55].

When the proof mass is outside of the stable operating range for the modulator but not so close to one of the fixed electrodes that electrostatic pull-in occurs, mode II operation is in effect. In mode II operation, the output of the modulator is no longer a rapidly fluctuating bit stream with an average value representing the input acceleration (as with mode I operation), but rather an output composed of long streams of consecutive 1s or 0s with relatively infrequent transitions. The proof mass oscillates at a fixed frequency about the zero deflection point, slowly decaying in magnitude until the system returns to mode I operation. Figure 3.44 diagrams mode II operation of the reset loop. The proof mass deflection is plotted below the output bit stream from the second order system. Note the decaying oscillations of the proof mass as the system slowly settles back into mode I operation. The transition from mode II to mode I operation can clearly be seen by inspecting the output of the modulator. The single bit output clearly changes from long streams of 1s and 0s to the rapidly changing bit stream associated with Δ-Σ modulation. It is using this clear transition that the mode of operation is determined.

When the accelerometer is operating in the fifth order mode, a string of consecutive 1s or 0s over a certain threshold length indicates instability. Once this occurs, the accelerometer is switched into the reset mode. Once in the reset mode, if over a certain specified period of time there is not a string of consecutive 1s or 0s over another specified threshold length, the proof mass is assumed to have settled to within a given range of the zero deflection point such that stable fifth order operation can resume. Upon startup, the accelerometer is placed in reset mode to initialize the proof mass to its zero deflection point.

Figure 3.45 illustrates how the second order loop brings the proof mass close enough to the equilibrium point to switch into fifth order operation. In contrast, figure

55. As the velocity of the proof mass increases, the proof mass must be closer to its zero deflection point to assume stable second order operation.

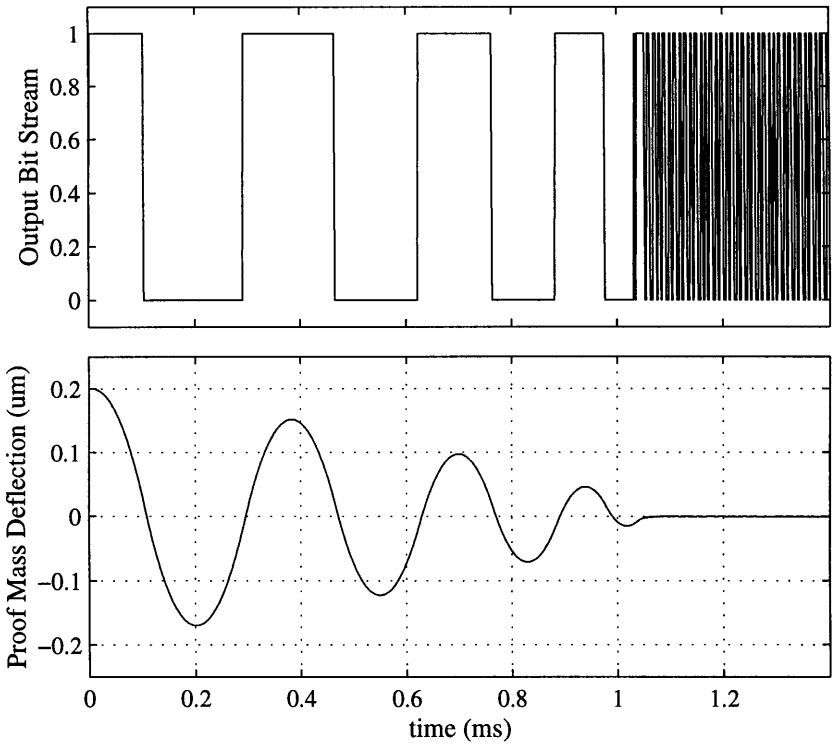


Figure 3.44 Mode I and II operation of the second order system

3.46 shows the operation of the same system with 12.8Å (thermal) circuit noise which prevents stable fifth order operation. Note the accelerometer tries continually to switch into fifth order mode.

3.6 Alternate Resonance Modes

In addition to the desired fundamental resonance mode of the mechanical structure, secondary resonance modes also exist. Figure 3.47 diagrams the main resonance mode (normal to the surface) followed by the next two resonances of the mechanical structure. In the main resonance mode, all four silicon tethers move simultaneously up and down in the direction normal to the surface of the wafer. The second and third resonant modes are rotational modes. In mode 2, two tethers move up and two move down creating an axis of rotation down the horizontal center of the proof mass. In the third

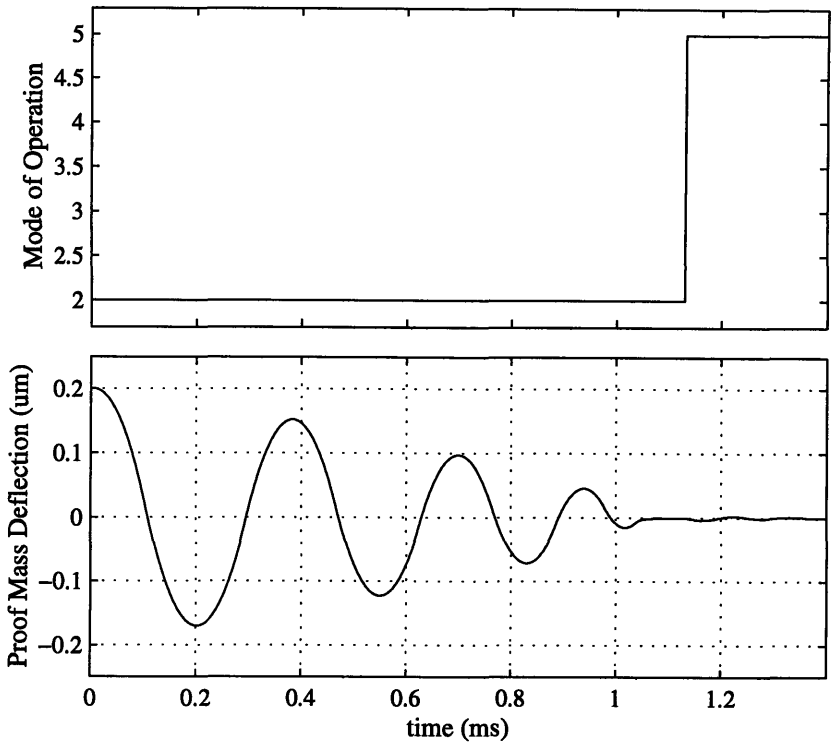


Figure 3.45 Mode control for the accelerometer

resonance mode, two of the tethers remain stationary and serve as the pivot point for rotation. Each of the two remaining tethers move in opposite directions setting up an axis of rotation along the diagonal of the proof mass. Other higher frequency resonances exist as well which are not mentioned here. The problem with these secondary resonances is that they can represent unstable modes of operation. Ideally, when a torque is applied to the proof mass, a small rotation occurs and decaying oscillations ensue until there is no further rotation. However, if the proof mass and feedback electrodes are slightly misaligned as shown in figure 3.48, there will be a small torque applied to the proof mass each time a voltage is applied to the fixed electrodes. Similarly, if the spring tethers do not all have the same bending constant, a torque will be applied every time the fixed electrodes are charged. Since the mechanical system is highly underdamped, if the gain of the loop around one of the secondary modes is greater than one above its mechanical resonant frequency, instability resulting in electrostatic pull-in will occur. With this in mind, extensive efforts were placed into separating the higher order resonance modes of the accelerometer

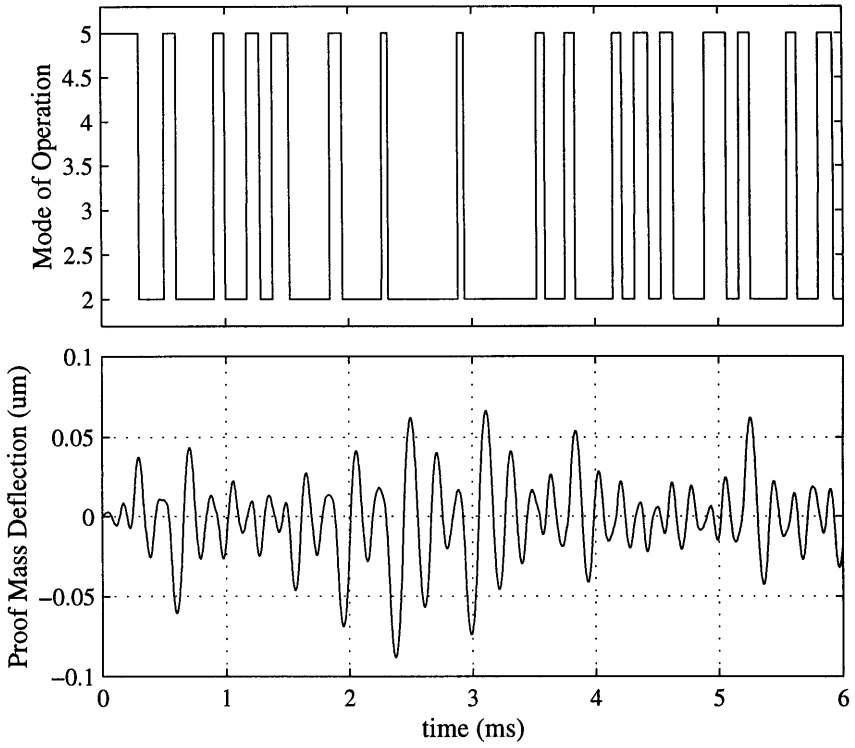
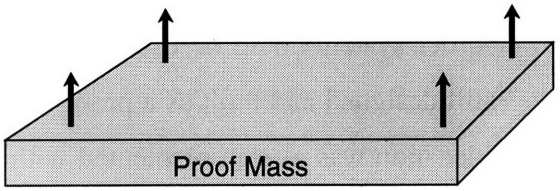


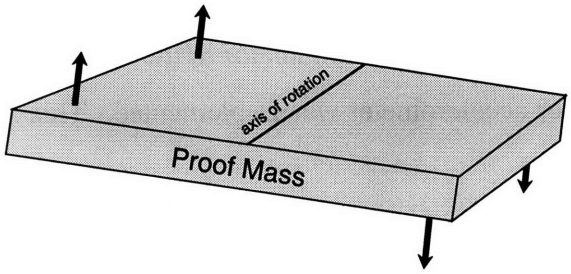
Figure 3.46 Unstable Fifth Order Operation

from a fabrication standpoint. Unfortunately, the secondary resonance mode was only separated from the fundamental resonance by a factor of 2.55 [18]. For this reason, it is possible that the proof mass will be drawn into the fixed electrodes due to an unstable higher order resonance. If this is the case, the accelerometer must be operated with partial viscous damping to stabilize the higher order resonance modes. Thus, the brownian noise floor will be raised.

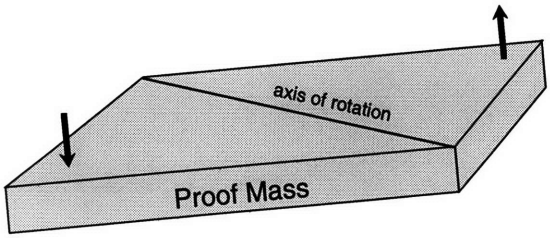
Section 6.2.1 diagrams two schemes to stabilize the proof mass in light of higher order resonance modes. One method taken from reference 22 uses multiple feedback loops to sense torque and acceleration while the other method uses electrical tuning with an alternate electrode placement to split the main resonance from the secondary resonance modes. The electrical resonance tuning described in section 3.3 lowers the resonant frequencies of the higher order modes as well as the fundamental.



a) Resonance Mode 1



b) Resonance Mode 2



c) Resonance Mode 3

Figure 3.47 Accelerometer Resonance Modes

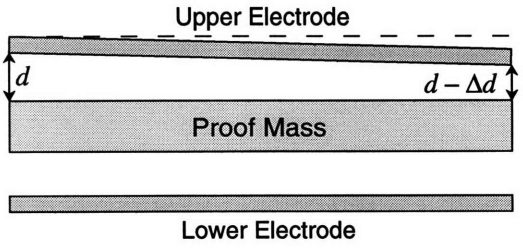


Figure 3.48 Mechanical Misalignment

3.7 The Third Order Accelerometer

By the time the full fifth order system had been designed, it became apparent that quantization noise and tones were not the limiting factor in determining the resolution of

the accelerometer. Since Brownian noise sets the noise floor of the accelerometer and not quantization noise, a lower order system could be used to achieve the same resolution. The fifth order system was still designed and built as a proof of concept. Along with the fifth order system, a third order loop was also implemented with only minimal extra circuitry. By feeding forward the output of the first integrator in the third order Δ-Σ modulator, a first order modulator can be implemented with identical gain to that of its third order counterpart. By placing this first order modulator in the loop instead of the third order Δ-Σ converter, a third order accelerometer was implemented. This is diagrammed in figure 3.49.

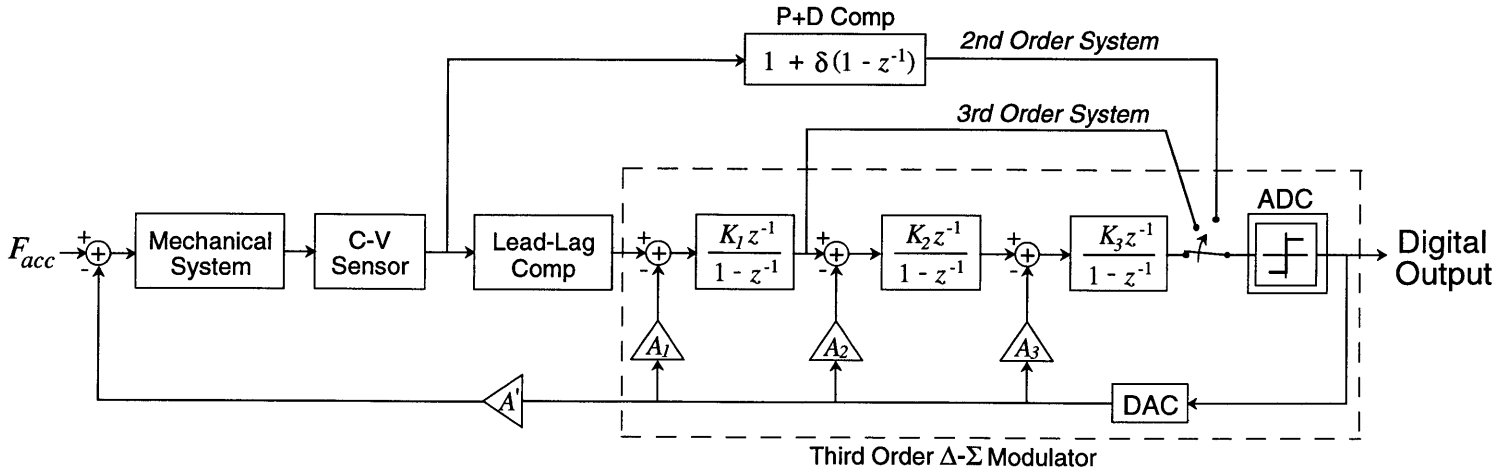


Figure 3.49 Integrating the Third Order System

CHAPTER 4

Circuit Implementation

Chapter three alluded to the circuit implementation to overall system performance showing how the dynamics of the mechanical system and the interaction of the C-V Sense method can be used to enhance the resolution of the accelerometer. This chapter details the switched capacitor implementations used for the C-V sensor, compensation networks, Δ-Σ modulator and feedback control. Noise reduction techniques are used which minimize the effects of thermal and low frequency noise as well as provide some immunity to the effects of capacitance mismatch. The electrical resonance tuning of the mechanical system is explored from the circuit domain.

4.1 Switched-Capacitor Design

Continuous time filters rely on absolute control of R and C values to set their dynamics. Because absolute tolerances for integrated resistors and capacitors range as high as 20%, precision control of a filter's dynamics is not possible. As an example, see the low pass filter in figure 4.1.

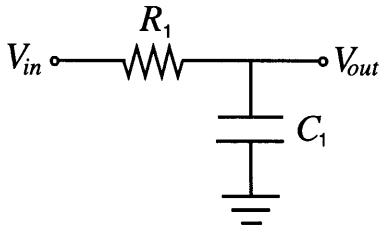


Figure 4.1 Continuous time low pass filter

The simple first order filter is composed of a single resistor and capacitor[56]. The RC time constant places the cutoff frequency of the filter. The transfer function given by:

$$H(s) = \frac{\omega_{co}}{s + \omega_{co}} \qquad [4.1]$$

where ω_{co} is the cutoff frequency:

$$\omega_{co} = \frac{1}{R_1 C_1} \qquad [4.2]$$

If the absolute values of R_1 and C_1 could be controlled to within 10% of their nominal values, the pole placement of the first order LPF would only be guaranteed within 20% of its desired location. For most filter applications, a 20% tolerance on cutoff frequency placement is unacceptable.

Switched-capacitor (S-C) circuits are used as a solution to the problem of controlling the dynamics of a continuous time integrated filters. By replacing resistors with "switched capacitors" the absolute tolerance for the placement of a time constant or cutoff frequency is controlled by the capacitance ratios instead of the absolute tolerance of resistors and capacitors. The basic circuit element for S-C filters is shown in figure 4.2.

A charge packet, ΔQ, is transferred between V_1 and V_2 each clock cycle given by:

$$\Delta Q = C_{SC}(V_1 - V_2) \qquad [4.3]$$

This transfer of charge generates an average current flow, I_{avg}, given by:

56. This example is taken from reference 33.

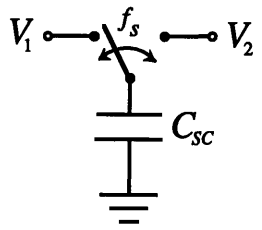


Figure 4.2 The "Switched-Capacitor"

$$I_{avg} = \frac{\Delta Q}{\Delta t} = \frac{C_{SC}(V_1 - V_2)}{T} \qquad [4.4]$$

where T is the period of the sampling frequency, f_s.

To approximate the operation of the switched capacitor as a resistor, divide the voltage across the effective resistance by the average current, I_{avg}:

$$R_{eff} = \frac{V}{I_{avg}} = \frac{(V_1 - V_2)}{\frac{C_{SC}(V_1 - V_2)}{T}} = \frac{1}{f_S C_{CS}} \qquad [4.5]$$

Thus, a capacitor and two switches can be used to "synthesize" a resistor. Returning to the first order lowpass filter example of figure 4.1, the resistor R_1 can now be replaced with a switched-capacitor "resistor" as shown in figure 4.3.

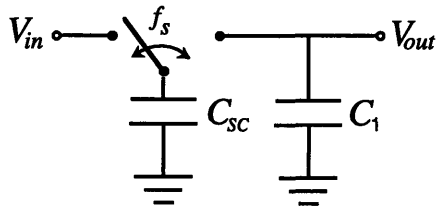


Figure 4.3 Switched Capacitor Filter

Using equations 4.5 and 4.2, the cutoff frequency for the SC filter is given by:

$$\omega_{co} = \frac{1}{RC} = \frac{1}{\left(\frac{1}{f_S C_{SC}}\right) C_1} = f_S \frac{C_{SC}}{C_1} \qquad [4.6]$$

Thus, the cutoff frequency of the filter is set by the ratio of two capacitors and the sampling frequency. Assuming precision control over the switching rate, f_s, the accuracy

of the cutoff frequency is set by the matching tolerance between capacitors, C_I and C_{SC}. This tolerance is typically in excess of 8-bits providing a better than 1% tolerance for the placement of ω_{co}.

4.1.1 The Switched-Capacitor Integrator

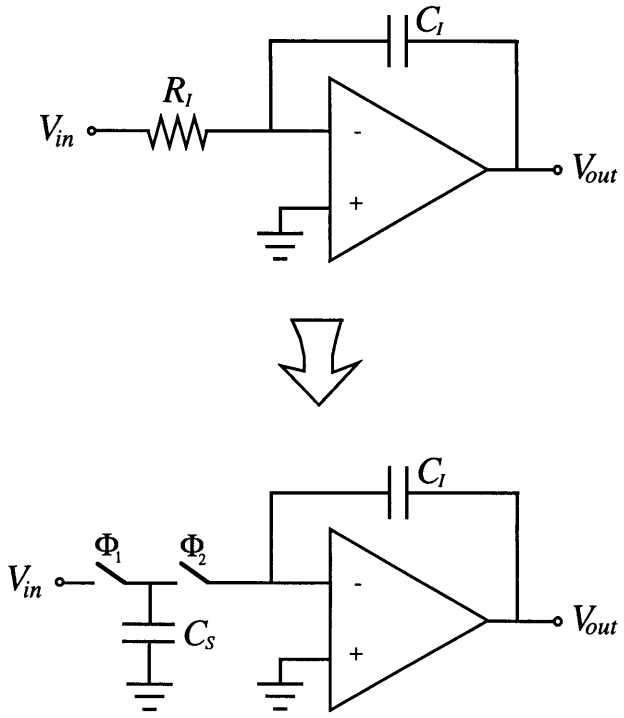


Figure 4.4 The Switched-Capacitor Integrator

The basic S-C building block is the S-C integrator. It is derived from its continuous time counterpart, shown on top in figure 4.4, by replacing R_I with the switched-capacitor C_S in the same fashion as C_{SC} replaced R_I in the prior example. The integrator operates with a two phase nonoverlapping clock. On clock phase ϕ_1, the first switch is closed dumping a total charge $C_S V_{in}$ onto capacitor C_S. On ϕ_2, the second switch is closed and all the charge from capacitor C_S is displaced onto C_I producing a change in voltage at the output given by:

$$\Delta V = -\frac{C_S}{C_I} V_{in} \qquad [4.7]$$

Note the negative sign for ΔV resulting from the integration. As with the continuous-time integrator, a positive current flow into the inverting terminal of the amplifier reduces the voltage across C_I. The operation of the integrator is given by [24]:

$$V(n) - V(n-1) = \Delta V = -\frac{C_S}{C_I} V_{in}(n-1) \qquad [4.8]$$

Solving equation 4.8, a z-domain transfer function can be established for the function of the discrete-time integrator[57]:

$$H(z) = -\frac{C_S}{C_I} \frac{z^{-1}}{1 - z^{-1}} \qquad [4.9]$$

Note the transfer function of the discrete time integrator is identical to within a sign of the transfer function for the integrators used for the Δ-Σ modulator (see figure 3.28).

4.1.2 Parasitic Insensitive Integration

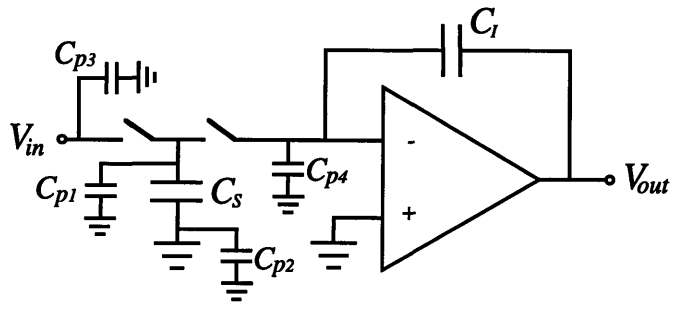


Figure 4.5 Integrator with parasitics modelled

While the S-C integrator shown in figure 4.4 performs the basic function of integration, it suffers from the drawback of being sensitive to parasitic capacitances. The basic S-C integrator is redrawn in figure 4.5 with stray parasitics now included. Parasitics arise in the circuit due to drain and source capacitances to substrate in the "switches" and

57. Here, it is assumed that the integrator output is sampled on phase Φ_1. If however, the output of the stage were clocked to the following stage on Φ_2, the integrator would be delayless and the transfer function would be given by

$$H(z) = -\frac{C_S}{C_I} \frac{1}{1 - z^{-1}}$$

All remaining examples will assume that the output of the integrator is sampled on Φ_1.

capacitances to bulk from the top and bottom plates of C_S and C_I. Since capacitor C_{pI} is located in parallel with capacitor C_S, it represents an error in its effective value. Charge placed on C_{pI} during phase one of the integration is discharged onto C_I during phase two which results in an error at the output. Because all other nodes of the circuit are connected to ground or driven voltages (V_{in},V_{out}), the operation of the integrator is insensitive to parasitics at other nodes in the circuit. Any charge which accumulates on any of the other parasitics is discharged through low impedance nodes and therefore does not affect the final charge on C_I[58].

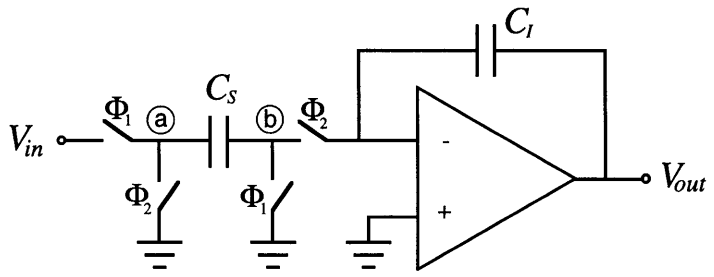


Figure 4.6 Stray Insensitive Integrator

Figure 4.6 shows an integrator which is insensitive to stray parasitic capacitance. Unlike before, any charge that accumulates on the stray capacitance at node "a" during the first clock phase is discharged to ground on phase two. None of the charge is displaced through C_S onto C_I. Similarly, because node "b" is held at ground or virtual ground on both clock phases, no parasitic charge is placed on C_I[59]. This integrator, as shown, has a noninverting transfer characteristic, identical in magnitude to equation 4.9. However, if node "a" is grounded during clock phase one then connected to V_{in} on phase two, inverting integration is performed. The alternate clocking scheme is shown in figure 4.7.

58. This holds for an ideal amplifier. Due to the finite gain and bandwidth of a real amplifier, parasitics are still an important design consideration. In the circuit layout, as a rule, the top plates of capacitors are connected to the inverting input of the amplifier to minimize the parasitics at the inverting node.

59. This in not true if the amplifier has an offset, V_{OS}. With an offset, V_{OS}, an integration error results given by:

$$\Delta V_{out} = + \frac{C_p}{C_S} V_{OS}$$

where C_p is the parasitic capacitance at node "b". Circuit techniques are used to mitigate the effects of this offset error. See section 4.2.

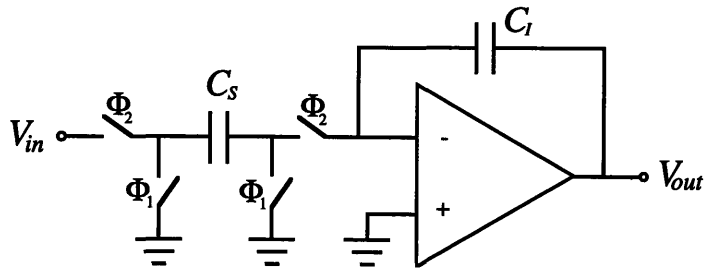


Figure 4.7 Inverting stray insensitive integrator

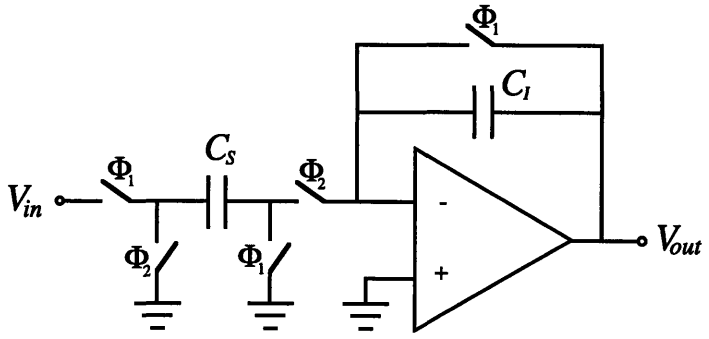


Figure 4.8 S-C gain stage

In addition to the discrete-time integrator, it is sometimes necessary to implement a pure gain stage in S-C circuitry. Figure 4.8 diagrams one such stage. On phase one, in addition to charging the sampling capacitor, C_S, the integrating capacitor, C_I, is discharged from its previous value. On clock phase two when C_S is discharged onto C_I, the output voltage will only be a function of the current input voltage. The transfer function for the amplifier is given by:

$$H(z) = \frac{C_S}{C_I} z^{-1/2} \qquad [4.10]$$

Like the S-C integrator of figure 4.7, an inverting gain stage can be implemented by switching the clock phases at the input.

4.1.3 S-C Noise Calculation

In a high resolution application such as this closed loop accelerometer, an accurate analysis of circuit noise is necessary to predict the overall resolution of the sensor. Examining figure 4.8, there are two dominate sources of noise in a switched capacitor gain stage, the input referred noise from the amplifier and the thermal noise of the switches. To calculate the total output noise from the stage, a transfer characteristic must be established between each noise source and the output.

The total noise power sampled onto a capacitor has been established as [24]:

$$\overline{v_n^2} = \frac{k_B T}{C} \qquad [4.11]$$

where k_B is boltzmann's constant and C is the total capacitance connected to each switch. Because the thermal noise from the switches is "white", the total noise power can be referred to the output of the stage by multiplying by the square of the transfer function between the noise source and the output. This results in an output noise power of [34]:

$$\overline{v_{out}^2} = \frac{k_B T}{C_S}\left(\frac{C_S}{C_I}\right)^2 = \frac{k_B T C_S}{C_I^2} \qquad [4.12]$$

for each pair of switches[60] which control the charging of C_S. The "reset" switch placed around C_I, has a unity transfer characteristic since it is directly connected to the output. The total output noise from the switch is thus, $k_B T/C_I$. The total output noise due to all the switches is given by:

$$\overline{v_{sw}^2} = \frac{k_B T C_S}{C_I^2}\left(2 + \frac{C_I}{C_S}\right) \qquad [4.13]$$

The input referred amplifier noise is comprised mainly of thermal noise and $1/f$ noise. The input referred thermal noise of the amplifiers is given by:

60. Note that equation 4.12 was derived for the total on resistance connected to a capacitor C during a clock phase and is fully independent of the number of switches through which the capacitor is charged. For this reason, equation 4.12 represents the effective output noise from each pair of switches connected to C_S.

$$\frac{\overline{v_{amp}^2}}{\Delta f} = 2\left(\frac{8k_BT}{3g_m}\right) \quad [4.14]$$

where g_m is the transconductance of the amplifier's first stage input devices. The noise described by equation 4.14 is referred to one input terminal of the amplifier. At low frequencies, the amplifier noise is related to the output by

$$H_n(s) = \frac{(C_S + C_I)}{C_I} \quad [4.15]$$

By integrating over the bandwidth of the amplifier, the total output noise power from the amplifier can be obtained [34]:

$$\overline{v_{out}^2} = \frac{4}{3}\frac{k_BT}{C_C}\frac{(C_S + C_I)^2}{C_I^2} \quad [4.16]$$

where C_c is the compensation capacitor of the amplifier[61]. Circuit techniques, described in section 4.2, are used to mitigate the effects of $1/f$ noise. An analysis of $1/f$ noise is therefore not pertinent in determining the resolution of the accelerometer and will be omitted here.

Note the prior noise analysis calculated the total output noise before decimation. Because thermal noise is "white", the noise from the amplifier and switches will be spread evenly over half the sampling frequency, f_S. Similar to the reduction of quantization noise in the Δ-Σ modulator, thermal noise from the amplifier and switches which is placed outside baseband will be eliminated by the decimation filter. Thus, the effective total noise power of the S-C gain stage is given by

$$\overline{v_{neff}^2} = \frac{\overline{v_{total}^2}}{\text{OSR}/2} = \frac{k_BT}{C_I^2}\left[\frac{4}{3}\frac{(C_S + C_I)^2}{C_C} + 2C_S + C_I\right]\frac{f_S}{2f_B} \quad [4.17]$$

where f_B and f_S are the baseband and sampling frequencies, respectively.

61. A single stage topology is used to implement the amplifiers for the S-C accelerometer circuitry. Thus, C_C is set by the load capacitance, C_L, and not set internally by a fixed capacitance as with a two stage topology. See section 4.6.

4.2 Noise Reduction Techniques

To maximize the resolution of the accelerometer, circuit techniques were employed which reduce the effects of low frequency noise, offsets, common mode noise, and even capacitance mismatch. Before detailing the actual application of each method in the accelerometer's critical circuits, the different procedures will be outlined in this section.

4.2.1 The Fully Differential Integrator

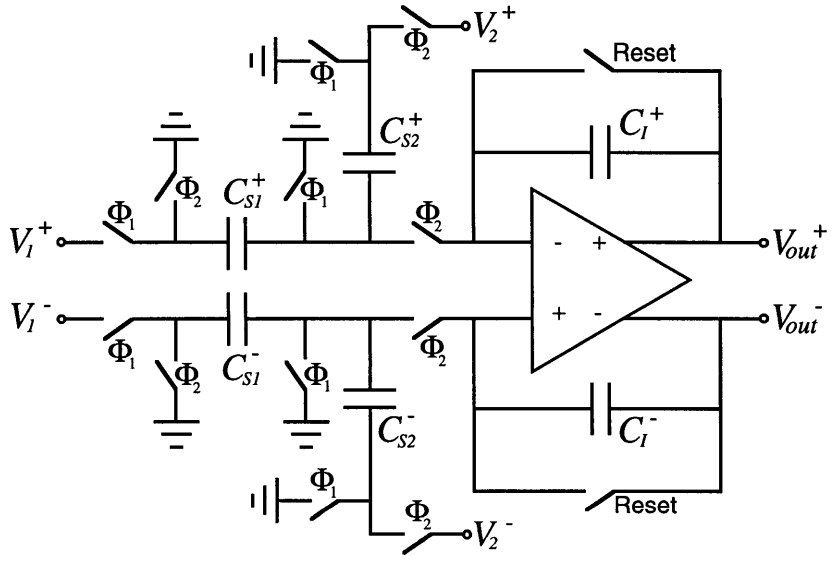


Figure 4.9 Fully Differential Integrator

Figure 4.9 shows the fully differential integrator that is used in the Δ-Σ modulator and Lead-Lag compensation network. Fully differential gain stages (not shown) are used in the C-V sensor and proportional-plus-derivative (P+D) compensation. Operation of the fully differential integrator is almost identical to its single ended counterpart described in section 4.1. Its transfer characteristic is given by

$$V_{out}(z) = \left(\frac{C_{S1}}{C_I}\right)\frac{z^{-1}}{1-z^{-1}}V_1(z) - \left(\frac{C_{S2}}{C_I}\right)\frac{z^{-1}}{1-z^{-1}}V_2(z) \qquad [4.18]$$

On clock phase one, the left side of capacitor C_{S1} is charged to V_1 while its right side is grounded. On clock phase two, the left side of C_{S1} is grounded and all the charge is dumped onto C_I. Concurrently on phase two, the voltage V_2 is coupled through C_{S2} onto C_I. Note the two phase integration of V_1 is noninverting while the single phase integration of V_2 is inverting. As with its single ended counterpart, each node of the differential integrator is kept at ground or virtual ground at all times yielding a stray insensitive design.

The fully differential integrator is designed to reduce or eliminate the effects of feedthrough from the power supply, substrate, or clock. Through the use of a highly symmetrical layout, many of these deterministic noise sources appear as common mode signals. By designing the fully differential amplifiers with high common mode rejection, the deterministic noise sources have little to no effect on the differential voltage seen at the output. Thus, these sources of error are effectively removed. In addition to reducing the effects of deterministic noise, the fully differential topology also facilitates chopping which is described next.

4.2.2 Chopping

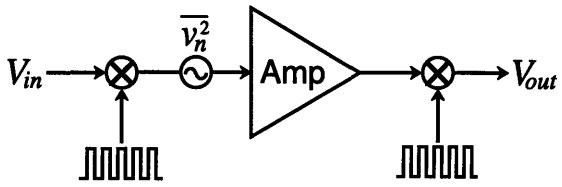
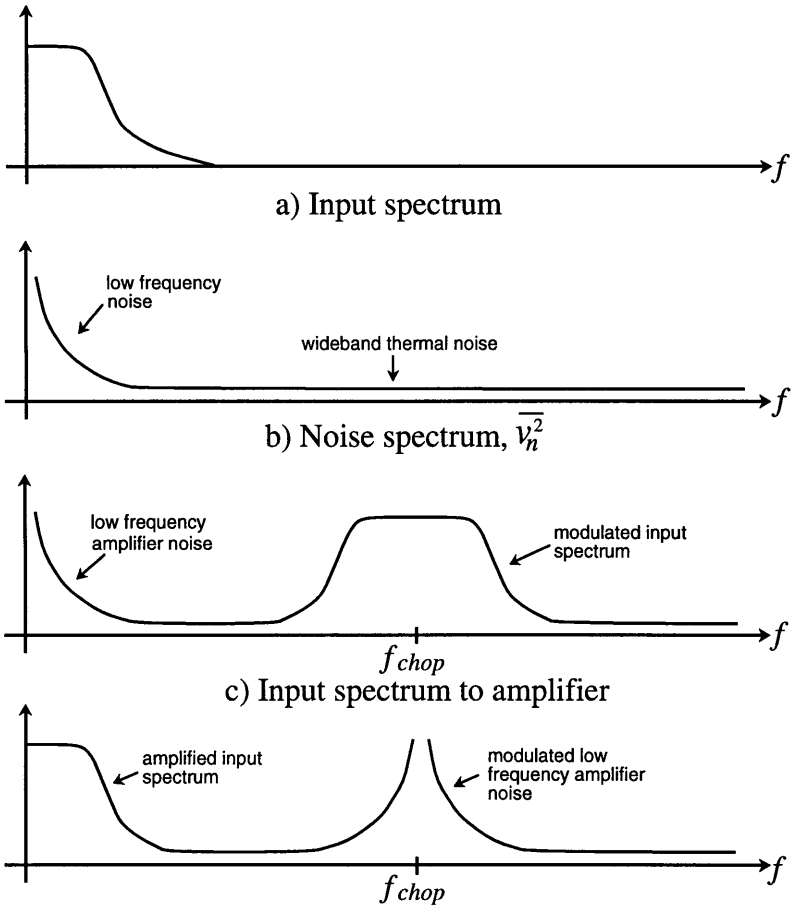


Figure 4.10 "Chopped" amplifier circuit

The low frequency noise reduction technique which is used most frequently in the accelerometer is chopping. The basic idea behind chopping is illustrated in figures 4.10 and 4.11[62]. Before a signal is passed through an amplifier it is multiplied by a square wave at a frequency f_{chop}. This modulates the signal spectrum to be centered about f_{chop}. The multiplied signal is then passed to the amplifier which combines the modulated signal with its own input noise spectrum. The amplifier noise spectrum is comprised of wide-

62. This explanation of chopping is based on a similar explanation from reference 24.



a) Input spectrum

b) Noise spectrum, $\overline{v_n^2}$

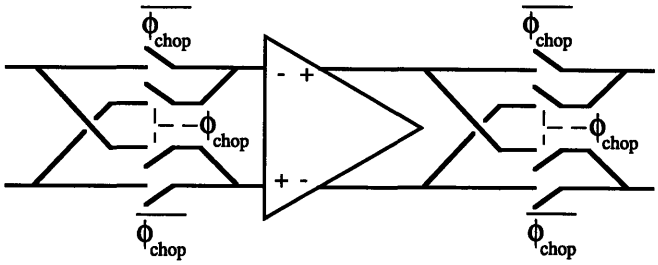
c) Input spectrum to amplifier

d) Output spectrum from second chopper

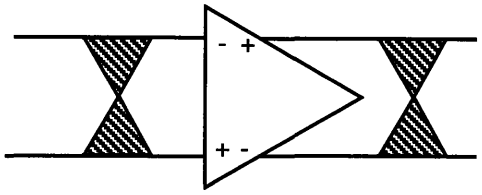
Figure 4.11 The "Chopped" Spectra

band thermal noise and low frequency flicker noise as shown in figure 4.11b. The output signal from the amplifier is multiplied by the same square wave as used before amplification which returns the signal to its original low frequency location. Likewise, the low frequency flicker noise from the amplifier is modulated to frequencies about f_c. Thus, the flicker noise from the amplifier is effectively removed from the baseband signal.

Because all low frequency noise peaks will be relocated to odd multiples of the chopping frequency, f_{chop}, the chopping frequency should be selected at half the sampling rate. This prevents aliasing of the shifted noise peaks back into the pass band during any subsequent sampling at the clock rate [24].



a) Chopper circuit realization



b) Circuit symbol for chopped amplifier

Figure 4.12 Chopper Circuit Implementation

Figure 4.12 shows the differential chopper circuit implementation. Since a differential signal is used, the signal coming into the amplifier can be inverted by simply exchanging the two inputs. In this manner, the four switches coming into the amplifier effectively modulate the input signal at the chopping frequency, Φ_{chop}. The same switching scheme is repeated at the output of the amplifier to return the signal information to the baseband frequencies. To simplify representation of the chopper-stabilized amplifier, the crosshatch symbol shown on the bottom of figure 4.12 is used to denote the four-switch chopping scheme.

4.2.3 Correlated Double Sampling

An alternate scheme for reducing the effects of low frequency noise and offsets is correlated double sampling (CDS). The idea behind correlated double sampling is fairly straightforward. Sample the noise from a circuit then a short time later, sample the noise plus signal. If the two samples are taken very close together, the low frequency noise will not appreciably change between samples. Thus, by subtracting the first sample from the

second, low frequency noise is removed. Note, as offsets do not change between samples, they are completely removed as well.

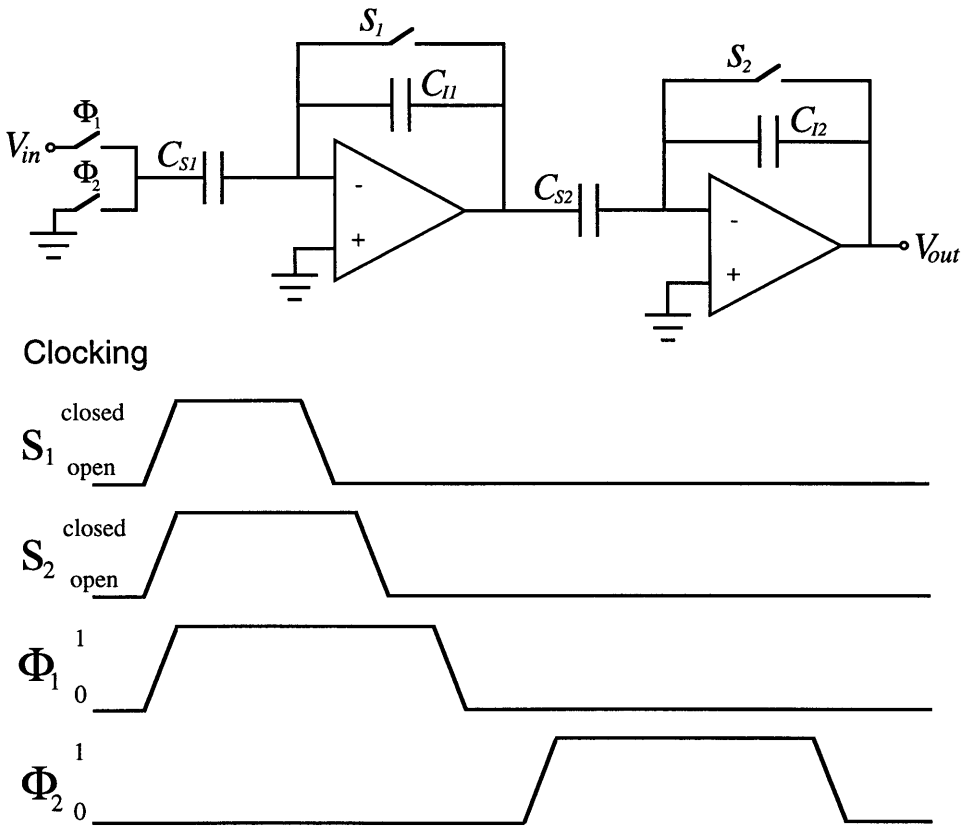


Figure 4.13 A circuit implementation for CDS

One possible circuit realization of correlated double sampling is shown in figure 4.13[63]. Initially, both switches S_1 and S_2 are closed while V_{in} is sampled onto C_{S1}. Next, switch S_1 is opened which injects a charge Q_{err} onto C_{I1}. It is at this time that the output noise from the first gain stage, $n(t_n\text{-}T/2)$, is sampled onto C_2. At some time later, S_2 is opened. Subsequently, the input capacitor C_1 is connected to ground which causes the output of the first stage to swing to its new value, $s(t_n) + n(t_n)$. Concurrently, the output of the second stage assumes its new value given by:

63. This circuit implementation performs correlated double sampling on the output of the first gain stage. Noise from the second stage amplifier which would show up at the output of the second gain stage is ignored here to facilitate explanation of CDS.

$$V_{out2}(t_n) = -\frac{C_{S2}}{C_{I2}}s(t_n) - \frac{C_{S2}}{C_{I2}}[n(t_n) - n(t_n - T/2)] \quad [4.19]$$

Since the low frequency output noise from the first gain stage will not appreciably change between time $(t_n\text{-}T/2)$ and time t_n, it is effectively removed by the correlated double sampling. Note, because switch S_1 is opened before S_2, the effect of Q_{err} is presampled onto C_2 as well and therefore removed from the final output.

While correlated double sampling removes low frequency ($1/f$) noise and DC offsets, it can actually make the effects of broadband noise worse. As an example, look at the total noise from a resistor, R, in the bandwidth, DC to $4\omega_1$. From equation 4.19, the z-transfer function for correlated double sampling is given by

$$H_{CDS}(z) = 1 - z^{-1/2} \quad [4.20]$$

and in the frequency domain,

$$H_{CDS}(e^{j\omega T}) = 1 - e^{-(j\omega T)/2} = e^{-(j\omega T)/4} 2j \sin\left(\frac{\omega T}{4}\right) \quad [4.21]$$

Thus, the total integrated noise power from the resistor is

$$\overline{n_{CDS}^2} = \int_0^{4\omega_1} 4\sin^2\left(\frac{\omega T}{4}\right)\frac{4k_B TR}{2\Pi} d\omega = \frac{16k_B TR}{\Pi}\omega_1 = 32k_B TRf_1 \quad [4.22]$$

For comparison, the total noise power from the resistor without CDS is given by

$$\overline{n_R^2} = 16k_B TRf_1 \quad [4.23]$$

Thus the use of CDS increased the total noise power of the resistor by a factor of two. While correlated double sampling acts to reduce the effects of low frequency noise, care should be taken when deciding whether to use this method if wideband noise is present.

4.3 The C-V Sensor

The C-V sensor is the most critical circuit in the accelerometer. Circuit noise from the C-V sensor and front end to the lead-lag network can be a major limitation on the over-

all resolution of the accelerometer. As discussed in chapter three, the positional sense of the proof mass which was originally thought to be noninvasive, actually alters the dynamics of the mechanical system. Not only must the C-V sensor measure the deflection of the proof mass with a high degree of accuracy, but the application of voltages to the fixed electrodes above and below the proof mass must be carefully adjusted to position the poles of the mechanical system. In addition, the capacitance sense must have the ability to completely shut off during the half cycle in which feedback is applied to the proof mass.

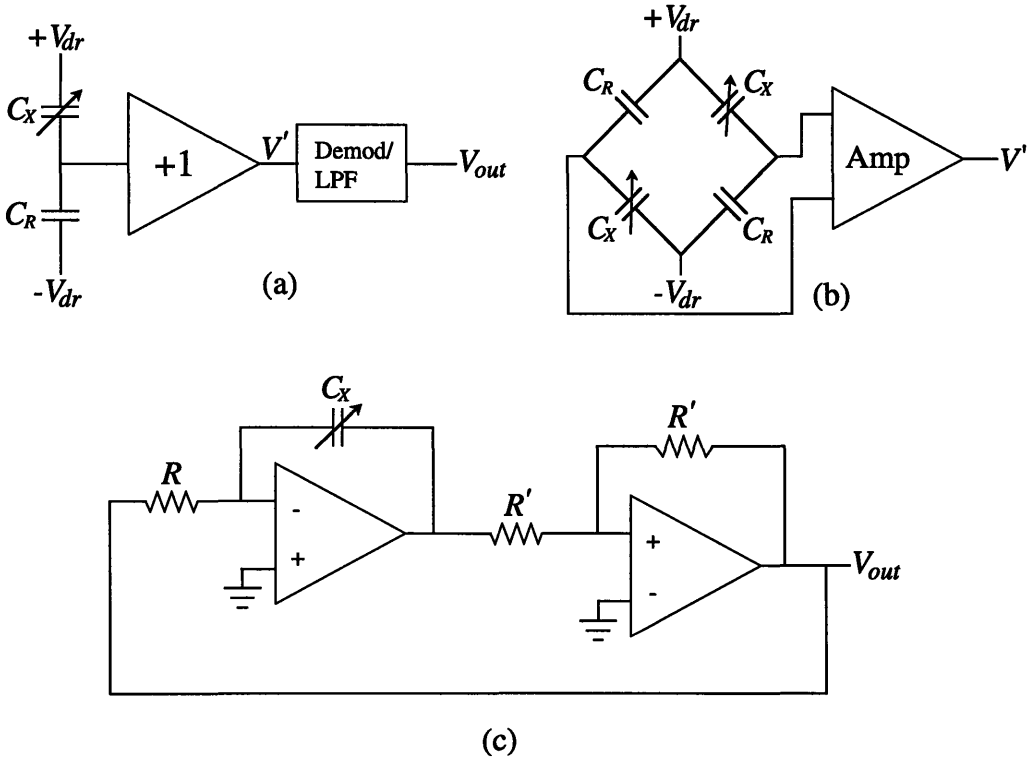


Figure 4.14 Possible C-V sense schemes

Extensive research has been devoted to developing different capacitive sense schemes [1,3,14-16,35-41]. Three of the many C-V sense implementations are shown in figure 4.14. Note, C_X represents the variable sense capacitor formed between the proof mass and a fixed sense electrode and C_R represents a fixed reference capacitor nominally equivalent to C_X with zero proof mass deflection. In the first sense scheme (figure 4.14a), C_X forms a half bridge with C_R which is driven by the differential voltage V_{dr}, which can

be either a DC [14-16] or time varying voltage [3]. If a time varying voltage is used, a demodulator and low pass filter are placed after the buffer. The obvious benefit of this implementation is its low circuit complexity while the main drawback is its high sensitivity to parasitic capacitances. The second C-V sense scheme (figure 4.14b) places the sensor into a full capacitor bridge [1]. The circuit operation is identical to that of figure 4.14a with a sinusoidal drive voltage used for V_{dr}. A demodulator and low pass filter (not shown) follow the amplifier. This circuit has the added benefit of insensitivity to common mode noise, however, it suffers from the same sensitivity to parasitics as in the prior circuit. In addition, the second sense scheme is highly sensitive to capacitance mismatch. Figure 4.14c shows a variable oscillator formed from an integrator and schmitt trigger [35-37]. As the proof mass moves causing a change in C_X, the integration "constant" changes which causes the output frequency to vary accordingly. The major disadvantage of this sense scheme is the additional circuitry required to convert the frequency output of the sensor into a voltage level necessary to implement the closed loop accelerometer. Other related capacitance sensors include capacitance-to-phase converters [38-40] and capacitance-to-frequency ratio converters [41], both of which require extra circuitry similar to that of figure 4.14c to obtain a simple voltage output. In addition to the aforementioned problems with each of these circuits, only the first sense scheme can be easily shut down for half a clock cycle as is required to apply a feedback force to the proof mass.

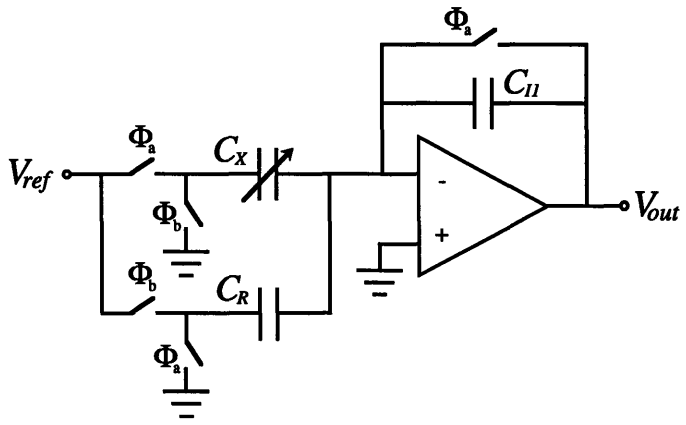


Figure 4.15 S-C capacitance sense

Figure 4.15 shows a switched capacitor implementation of a capacitance-to-voltage converter [42,43]. On clock phase a, the variable capacitance, C_X, is charged to V_{ref} and the integrating capacitor, C_I, is discharged. On phase b, the left side of C_X is grounded which discharges C_X onto C_I. Concurrently on phase b, V_{ref} is coupled through C_R onto C_I. The output voltage is given by

$$V_{out} = \frac{(C_X - C_R)}{C_I} V_{ref} = \frac{\Delta C}{C_I} V_{ref} \qquad [4.24]$$

Because the capacitance sense scheme must be disabled periodically while a feedback force is applied to the proof mass, a switched-capacitor implementation is a very practical choice for the sensor.

4.3.1 The Basic Switched-Capacitor Scheme

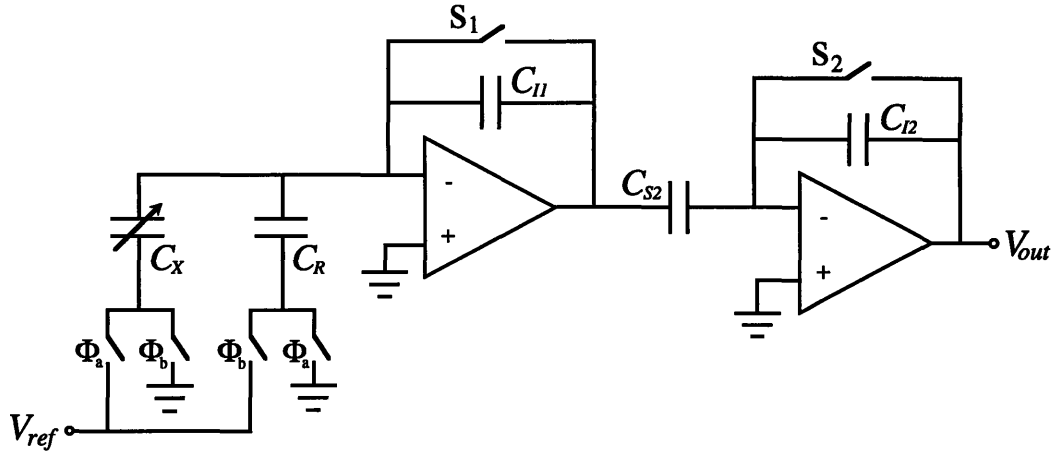


Figure 4.16 Basic C-V sensor

Figure 4.16 shows the basic capacitance sense scheme selected for the accelerometer[64]. Correlated double sampling is achieved in the same fashion as was described in section 4.2.3[65]. After C_X is charged to V_{ref} and S_1 has been opened, the output of the first gain

64. Φ_a and Φ_b are used to avoid confusion with Φ_1 and Φ_2, two of the actual clocks used in the accelerometer implementation.

stage is sampled onto C_{S2}. After S_2 is opened, C_X is grounded and C_R is connected to V_{ref}. The nominal output for the sensor is given by

$$V_{out} = -\frac{C_{S2}}{C_{I2}}\frac{(C_X - C_R)}{C_{I1}}V_{ref} = -\frac{C_{S2}}{C_{I2}}\frac{\Delta C}{C_{I1}}V_{ref} \quad [4.25]$$

Measurement and successive cancellation of the output noise from the first gain stage effectively removes the effects of offset in the first amplifier as well as charge injection and thermal noise from S_1 [42]. The effects of $1/f$ noise in the first stage amplifier are also greatly reduced.

4.3.2 The Full C-V Sensor Design

The full C-V sensor design is shown in figure 4.17 and the corresponding clocking diagram is shown in figure 4.18. The functionality of this circuit is identical to the basic sensor described in the prior section. The choppers, placed at the input to the single ended amplifiers and the output of the fully differential amplifier, are switched at half the sampling rate. The additional feedback circuitry (shaded in gray) controls the feedback during clock phase Φ_1. The output from the modulator (X) is used to select one of two voltages to be applied to each fixed electrode during feedback. The capacitance sense is performed solely during clock phase Φ_2. Note that Φ_3, Φ_4, and Φ_{S1} which control the capacitance sense are all subphases of Φ_2.

To analyze this circuit, first assume the switches in the choppers are controlled to pass voltages "straight" as drawn. Thus, the top electrodes of the proof mass and reference mass are connected to the $-V_1$ and $+V_2$ switches and the bottom electrodes are connected to the V_{tune} switches. By switching $-V_1$ and $+V_2$ across C_{X1} and C_{R1}, a differential voltage, v_X, is developed across the output of the two single ended amplifiers:

65. Unlike the previous scheme, the two samples which are taken to implement the CDS are much closer than one half of a cycle. Here, the transfer function of the correlated double sampling is given by

$$H_{CDS}(z) = 1 - z^{-0.2}$$

It turns out that because the samples are taken so close together, the total wideband (thermal) noise is decreased by the correlated double sampling.

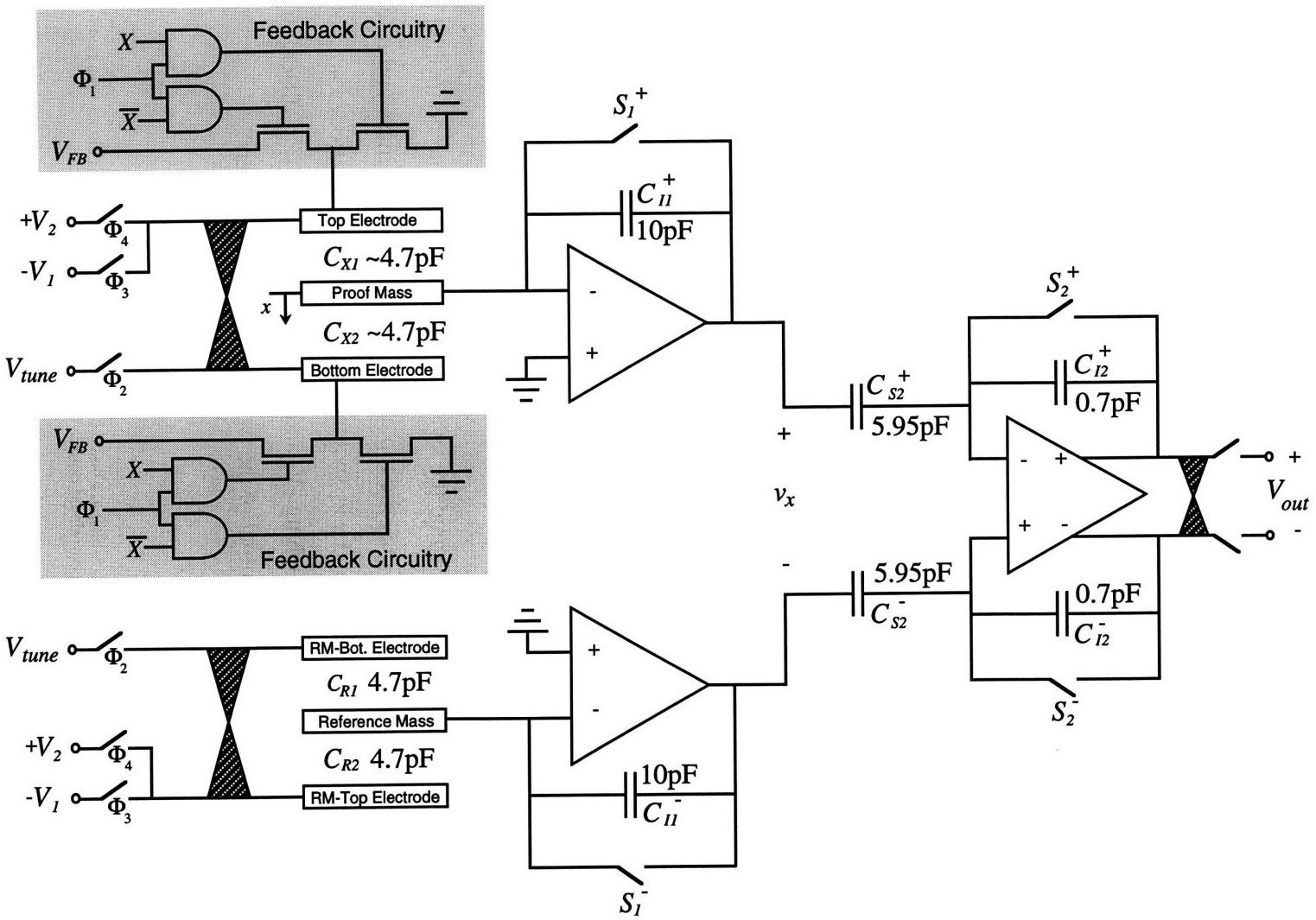


Figure 4.17 The C-V Sensor

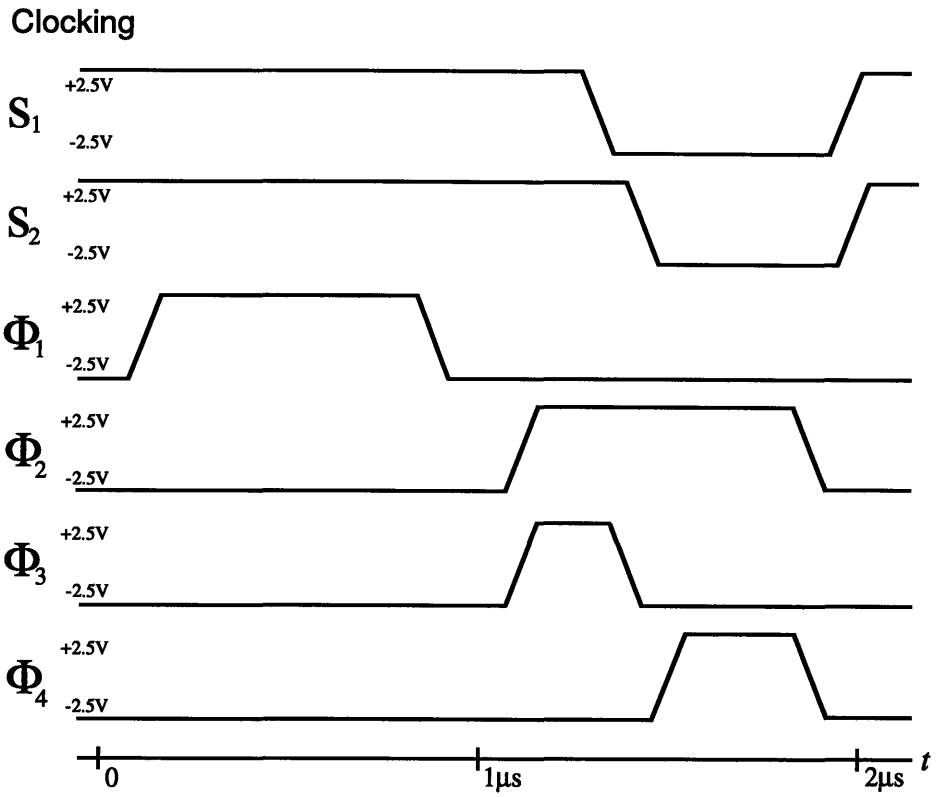


Figure 4.18 Clocking diagram

$$v_x = -\frac{(C_X - C_R)}{C_{I1}}(V_1 + V_2) = -\frac{\Delta C}{C_{I1}}(V_1 + V_2) \qquad [4.26]$$

The second stage implements the correlated double sampling in the manner as the second gain stage of figure 4.13.

Recalling the basic analysis of section 3.2.3, C_{XI} and C_{RI} are given by

$$C_X = \frac{\varepsilon_o A}{d+x} \qquad C_R = \frac{\varepsilon_o A}{d} \qquad [4.27]$$

and the differential capacitance, ΔC_I, is

$$\Delta C \approx -\frac{x}{d} C_R \qquad [4.28]$$

Substituting equation 4.28 into equation 4.26, a relation is established between deflection of the proof mass, x, and the differential voltage, v_X.

$$v_{X1} \approx \frac{C_R(V_1 + V_2)}{C_{I1}d}x \qquad [4.29]$$

A similar analysis for when the choppers are alternated to charge through capacitors C_{X2} and C_{R2} yields

$$v_{X2} \approx -\frac{C_R(V_1 + V_2)}{C_{I1}d}x \qquad [4.30]$$

Thus, the effective gain to the differential input of the second stage is alternating in sign each clock cycle. This is equivalent to chopping the signal at half the sampling rate. Chopping switches are placed at the output of the second gain stage to demodulate the signal. Thus, the second stage amplifier is effectively "chopped". Careful inspection of the circuit reveals that the entire C-V sense circuit benefits from the effects of chopping. By alternately charging the top and bottom electrodes of the sense and reference capacitors, the position of the proof mass is effectively modulated from the standpoint of the C-V circuit. Along with removing low frequency noise from the amplifiers, the chopping shifts the effects other nonidealities such as capacitor mismatch to half the sampling rate. Note, even though the first stage amplifiers are effectively chopped by the switches at the input of the sensor, correlated double sampling is still necessary to prevent the second gain stage from saturating due to any voltage offset in the first stage. The correlated double sampling also removes *kT/C* noise and charge injection from S_1.

Continuing the analysis, the output of the second stage is given by

$$V_{out} = -\frac{C_{S2}C_R(V_1 + V_2)}{C_{I2}C_{I1}d}x \qquad [4.31]$$

Note this equation is in the same form as used in the dynamics analysis of section 3.2.3.

The single ended amplifiers at the front end of the C-V sensor are necessary to place the proof mass at virtual ground. A fully differential amplifier scheme would place the proof mass at a signal dependant voltage level which would result in harmonic distortion at the output of the accelerometer. Note that even though the first stage amplifiers are single ended, any common mode noise present is effectively reduced by the common

mode rejection of the second stage fully differential amplifier. This includes noise coupled through parasitics in the proof mass and reference mass structures.

In addition to the differential output from the first stage amplifiers, there is a large common mode voltage present as well. The common mode voltage is approximated by

$$V_{CM} \approx -\frac{C_R}{C_{I1}}(V_1 + V_2) \qquad [4.32]$$

The second stage differential amplifier must have high common mode rejection to prevent the large common mode signal from showing up at its differential output. The integrating capacitor C_{I1} was selected to allow a first stage gain as large as possible without exceeding the common mode range of the fully differential amplifier.

To this point in the analysis of the C-V sensor, the voltage V_{tune} has been ignored. Since V_{tune} is constant for the duration of the position sense, it has no effect on the voltage which shows up at the output of the C-V sensor. However, because it places a positionally dependant (electrostatic) force on the proof mass, it does affect the incremental dynamics of the mechanical system. Assuming the proof mass is kept at 0V by the single ended amplifier[66], the force placed on the proof mass by the voltage V_{tune} is given by

$$F_{tune} = \frac{\varepsilon_o A}{2}\left(\frac{V_{tune}}{x+d}\right)^2 \qquad [4.33]$$

Since V_{tune} is first applied to the lower then the upper fixed electrodes, there is no average force applied when the proof mass is centered. Averaging the force placed on the proof mass over two cycles of operation gives

$$\begin{aligned} F_{avg} &= \frac{\eta(\Phi_2)}{2}\left[\frac{\varepsilon_o A}{2}\left(\frac{V_{tune}}{x+d}\right)^2 - \frac{\varepsilon_o A}{2}\left(\frac{V_{tune}}{x-d}\right)^2\right] \\ &= \eta(\Phi_2)\frac{\varepsilon_o A}{d^3}x\left[V_{tune}^2 + 2V_{tune}^2\left(\frac{x}{d}\right)^2 + \ldots\right] \end{aligned} \qquad [4.34]$$

where $\eta(\Phi_2)$ is the duty cycle for Φ_2. As expected, with zero deflection, there is no average force applied to the proof mass as a result of V_{tune}. There is, however, a positionally

66. Any force which is placed on the proof mass as a result of a first stage offset voltage is effectively removed by the chopping in the C-V sensor and is therefore not seen at the output from the accelerometer.

dependant term which contributes to the overall electrical spring constant, K_{EL}, and is given by

$$K_{tune} = \eta(\Phi_2)\frac{\varepsilon_o A}{d^3}V_{tune}^2 \qquad [4.35]$$

Using a similar analysis for the $-V_1$ and $+V_2$ voltages which are applied to the proof mass determines another component of the electric spring constant:

$$K_v = \frac{\varepsilon_o A}{d^3}[\eta(\Phi_3)V_1^2 + \eta(\Phi_4)V_2^2] \qquad [4.36]$$

where Φ_3 and Φ_4 are the duty cycles for the application of $-V_1$ and $+V_2$, respectively. Combining equations 4.35 and 4.36 with the K_{EL1} term derived in chapter 3 (equation 3.17) results in a total electric spring constant given by

$$K_{EL} = \frac{\varepsilon_o A}{d^3}[\eta(\Phi_1)2(V_{DC}^2 + V_{DIFF}^2) + \eta(\Phi_2)V_{tune}^2 + \eta(\Phi_3)V_1^2 + \eta(\Phi_4)V_2^2] \qquad [4.37]$$

Thus, by adjusting the voltage V_{tune}, the dynamics of the mechanical system can be altered without changing the effective gain of the C-V sensor.

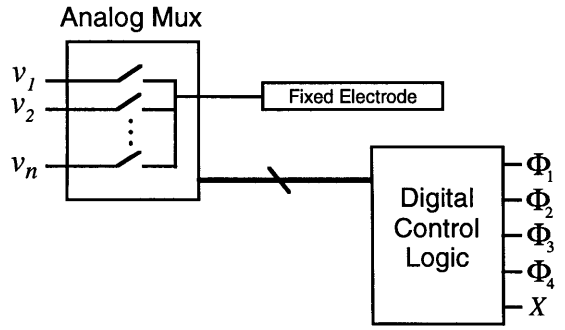


Figure 4.19 Basic circuit implementation for charging the fixed electrodes

As a practical circuit implementation, an analog multiplexer with some basic control logic is used to charge the fixed electrodes above and below the proof mass. Figure 4.19 shows the basic scheme for accomplishing this. By controlling the voltages placed on the fixed electrodes in this fashion, only one switch is placed between each electrode and a voltage. This topology minimizes parasitics and clock feedthrough. Another benefit

of this multiplexing scheme is the ability to implement additional sense schemes with very little extra circuitry. By adding minimal extra control logic to the multiplexers, a second differential capacitance sense scheme can be implemented as well. The additional sense scheme is explained in the next section.

4.3.3 The Fully Differential C-V Sense: Method II

Figure 4.20 shows the fully differential C-V sense method. Here, the C-V sensor measures the top and bottom capacitances of the proof mass and outputs a voltage proportional to the difference. The reference capacitors are grounded. Note, however, that any common mode noise from the two structures is still passed to the input of the second stage and reduced by the common mode rejection of the fully differential amplifier

Resonance tuning is achieved in a similar manner to before. With this scheme, however, there is no separate voltage to "tune" the mechanical resonance. Orthogonal control over the mechanical resonance is attained by varying the DC voltage placed across the fixed electrodes without changing the applied differential bias. As an example, suppose the fixed electrodes are charged with 0.1V then 1.1V during the C-V sense. By charging the electrodes with 0.4V and 1.4V instead, the electrical spring constant can be increased without changing the effective gain of the C-V sensor.

Comparing this sense scheme with the prior sense method, this sense scheme has several advantages. Since a differential sense is used, the output from the first stage single ended amplifiers is purely differential. The large common mode voltage necessary in the first sense scheme is no longer present. For this reason, the gain of the C-V sensor can be increased substantially without violating the common mode input range of the second stage amplifier. Also, because this scheme senses the upper and lower capacitances of the proof mass simultaneously, the effective signal is doubled as compared to the prior sense method.

The last advantage of this sense method is more subtle. The first sense scheme measures the sense capacitors of the proof mass and the reference mass. The output is a voltage proportional to the difference. Closing a loop around this sensor balances the proof mass to the same deflection as the reference mass. As an example, if the reference

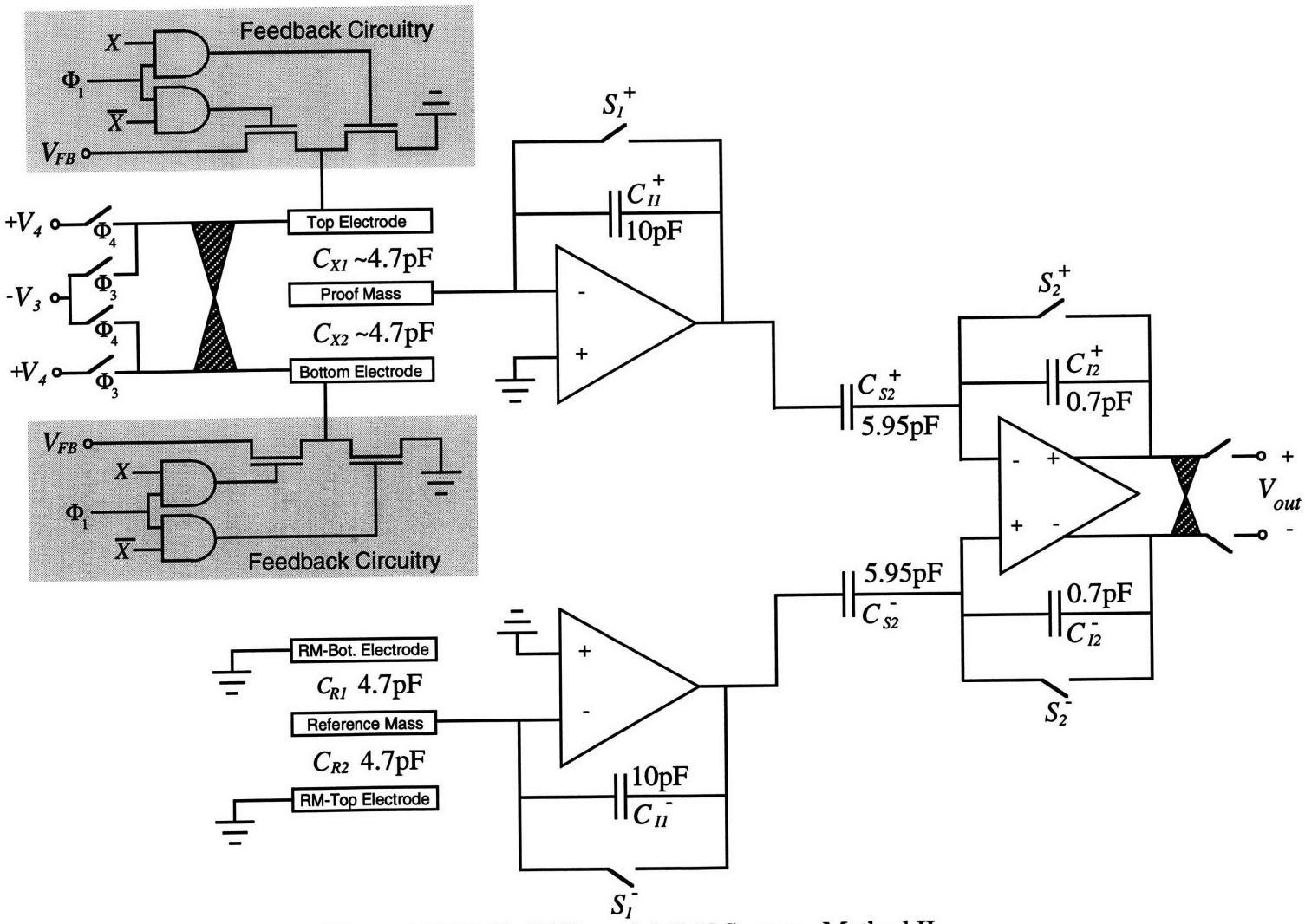


Figure 4.20 Fully Differential C-V Sensor - Method II

mass has a 10% offset in deflection, the proof mass will be "balanced" to a 10% deflection by the action of the closed loop. Thus, in steady state, the upper and lower capacitors of the proof mass will have different values. This can severely degrade the incremental dynamics of the mechanical sensor. Alternatively, the second sense scheme balances the proof mass such that the upper and lower sense capacitors are identical. Thus, the incremental dynamics of the sensor will not be compromised even with large mechanical tolerances. Unfortunately, the second sense method is also highly susceptible to instability caused by these same large mechanical tolerances.

The mechanical system and electrical system each have a "center". The mechanical "center" refers to the position of the proof mass where no force is applied by the mechanical spring. The electrical "center" refers to the proof mass position where there is zero output from the C-V sensor. Nominally, the electrical and mechanical center are identical, however due to fabrication variances, discrepancies usually exist between the two locations. When differences do exist, the loop balances the proof mass to the electrical center and any force exerted by the mechanical spring is seen at the accelerometer's output as a DC offset.

As discussed above, the first sense method balances the proof mass such that it has a nearly identical deflection to the reference mass. Because the reference and proof mass are guaranteed to match within 50Å, the worst case acceleration offset which can occur is ±0.21g. Alternatively, the bottom and top gap spacings of the proof mass can vary by as much as ±0.1μm. Thus, using the second sense method, an offset as high as ±4.2g can occur. Since the stable input range of the accelerometer is only ±2g, the accelerometer will never assume stable operation under worst case conditions. For this reason, the second C-V sense scheme is included only as an alternate sense scheme which may be viable for other structures with more exact fabrication tolerances.

4.4 Compensation

Like the C-V sensor, the compensation networks are implemented with switched-capacitor circuitry and exploit the benefits of a fully-differential design.

4.4.1 Lead-Lag Circuitry

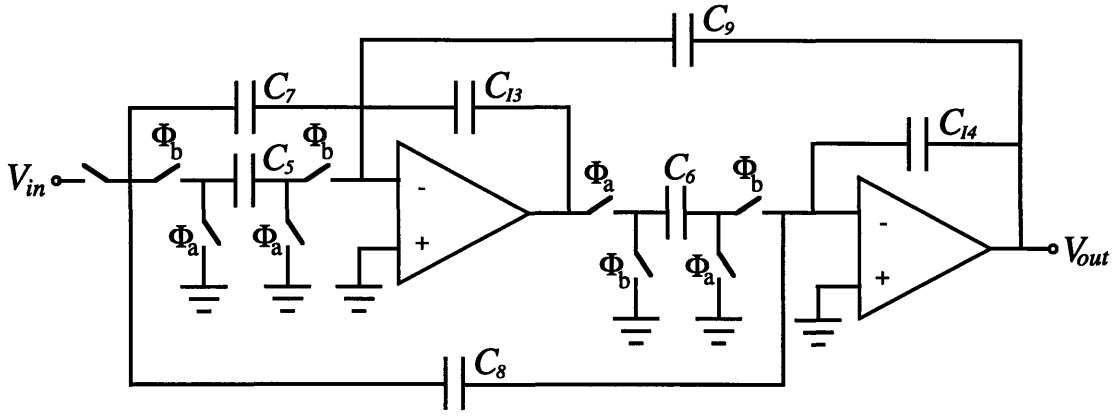


Figure 4.21 Basic lead lag circuit

The basic lead lag S-C circuit is shown in figure 4.21[67]. Once again, Φ_a and Φ_b are used to avoid confusion with the actual system clocks. The transfer function of the filter is given by

$$H_{LL}(z) = -\frac{C_8 + \left(\frac{C_5C_6}{C_3C_4} + \frac{C_6C_7}{C_3C_4} - 2C_8\right)z^{-1} + \left(C_8 - \frac{C_6C_7}{C_3C_4}\right)z^{-2}}{1 + \left(\frac{C_6C_9}{C_3C_4} - 2\right)z^{-1} + \left(1 - \frac{C_6C_9}{C_3C_4}\right)z^{-2}} \qquad [4.38]$$

Note the DC gain ($z = 1$) of the network is infinite. The infinite gain of the circuit results from a DC pole placement due to the C_9 feedback around the two integrators. The coefficients for equation 4.38 were selected by transforming the desired continuous time pole locations into the z-domain using the bilinear transform.

67. This circuit topology was developed directly from reference [24].

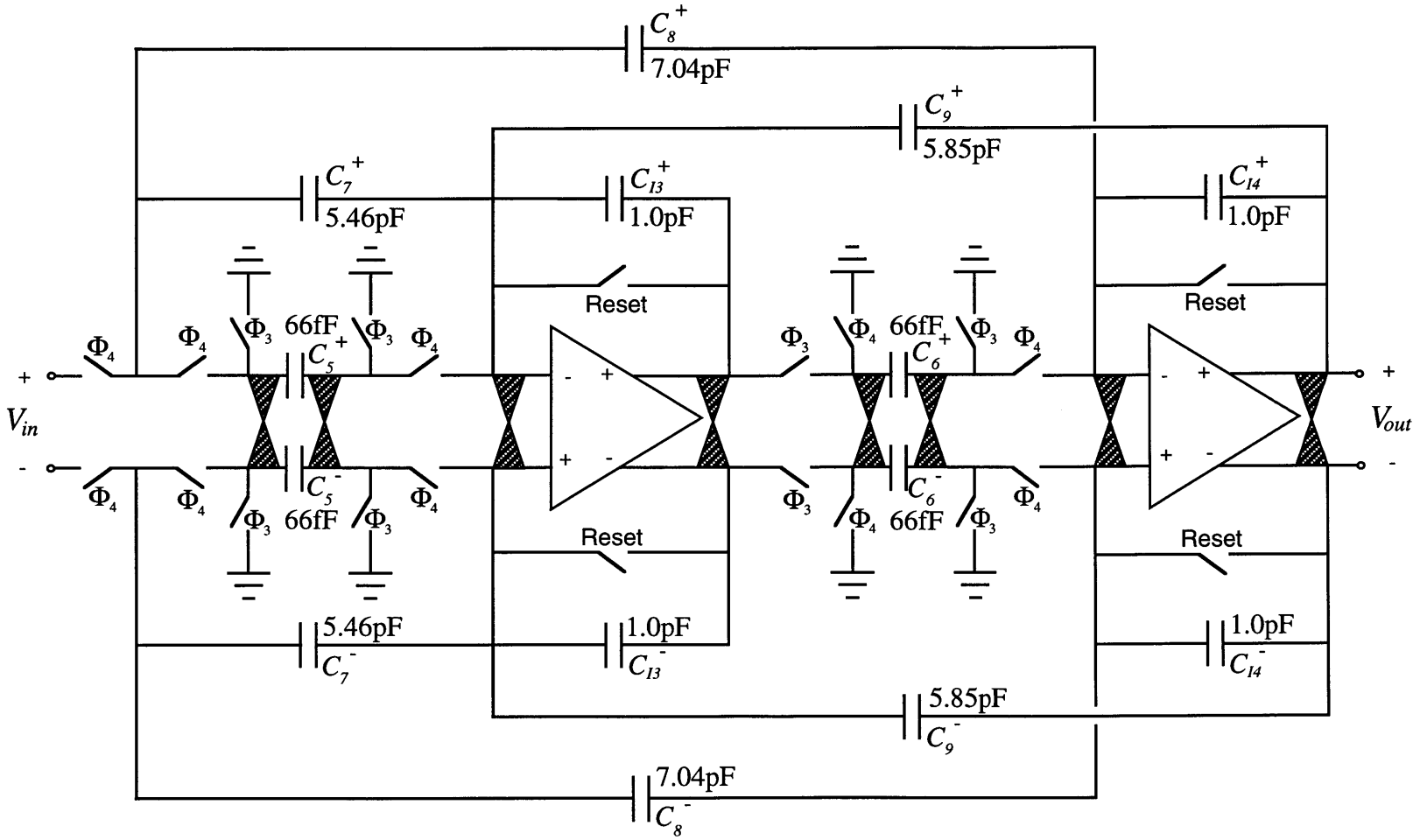


Figure 4.22 The Fully Differential Lead-Lag Circuit

The fully differential circuit implementation of the lead lag circuit is shown in figure 4.22. The differential amplifiers in the circuit are chopped to reduce the effects of low frequency noise and offsets. The corresponding transfer characteristic is given by

$$H_{LL}(z) = -\frac{7.039 - 13.7z^{-1} + 6.68z^{-2}}{1 - 1.614z^{-1} + 0.614z^{-2}} \qquad [4.39]$$

The gain of the circuit was selected by choosing the pole locations (denominator coefficients) of the filter and then determining the gain which would minimize the necessary capacitance ratios. Even using minimized capacitance ratios, 66fF capacitors were still necessary. To minimize the effects of mismatches in these capacitors, the 66fF capacitors are chopped along with the differential amplifiers.

4.4.2 P+D Circuitry

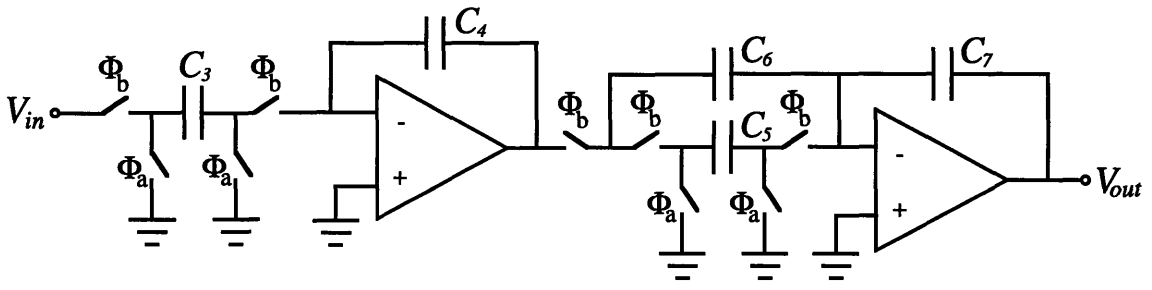


Figure 4.23 Basic P+D Circuit

The basic proportional plus derivative compensation circuit is shown in figure 4.23. The transfer function is given by

$$H_{P+D}(z) = \frac{C_3}{C_4 C_7}[C_5 + C_6(1 - z^{-1})] \qquad [4.40]$$

Note this transfer function could have been implemented with a single stage. However, due to the gain requirements of the circuit, a two stage implementation was used. Also note this transfer function is opposite in polarity to the prior lead lag compensation. To account for this, the connection from the differential output of the C-V sensor to the input of this stage was reversed in polarity to preserve negative feedback in the loop. The fully

differential circuit realization of the P+D compensation is shown in figure 4.24. The corresponding transfer function is given by

$$H_{P+D}(z) = 3(1 + 8(1 - z^{-1})) \quad [4.41]$$

4.5 The Delta-Sigma Modulator

The basic Δ-Σ modulator implementation used in the accelerometer is adapted from references 25 and 44. One of the variations used in this modulator is the multiplexing of different inputs to the comparator which include the output of the modulator's first integrator, the modulator's third integrator, and the output from the P+D compensation. In standard operation, the output from the third integrator is passed to the comparator to implement a third order Δ-Σ modulator. When a first order modulator is necessary (to implement the third order accelerometer), the output of the first integrator is input to the comparator. When the accelerometer is operating in its second order reset mode, the comparator receives its input from the P+D compensation, fully bypassing all of the modulator's integrators.

4.5.1 The Third Order Modulator

The basic architecture for the third order modulator is illustrated in figure 4.25. The discrete time integrators are implemented with switched capacitor integrators. The output value from the comparator is subtracted from each integrator to achieve binary feedback. Relating the circuit parameters in figure 4.25 to the transfer characteristic previously established for the Δ-Σ modulator (equations 3.16 - 3.36), the relation between capacitor values and the integrator and feedback coefficients is given by

$$K_1 = \frac{C_{S1}}{C_{I1}} \quad [4.42]$$

$$K_2 = \frac{C_{S2}}{C_{I2}} \quad [4.43]$$

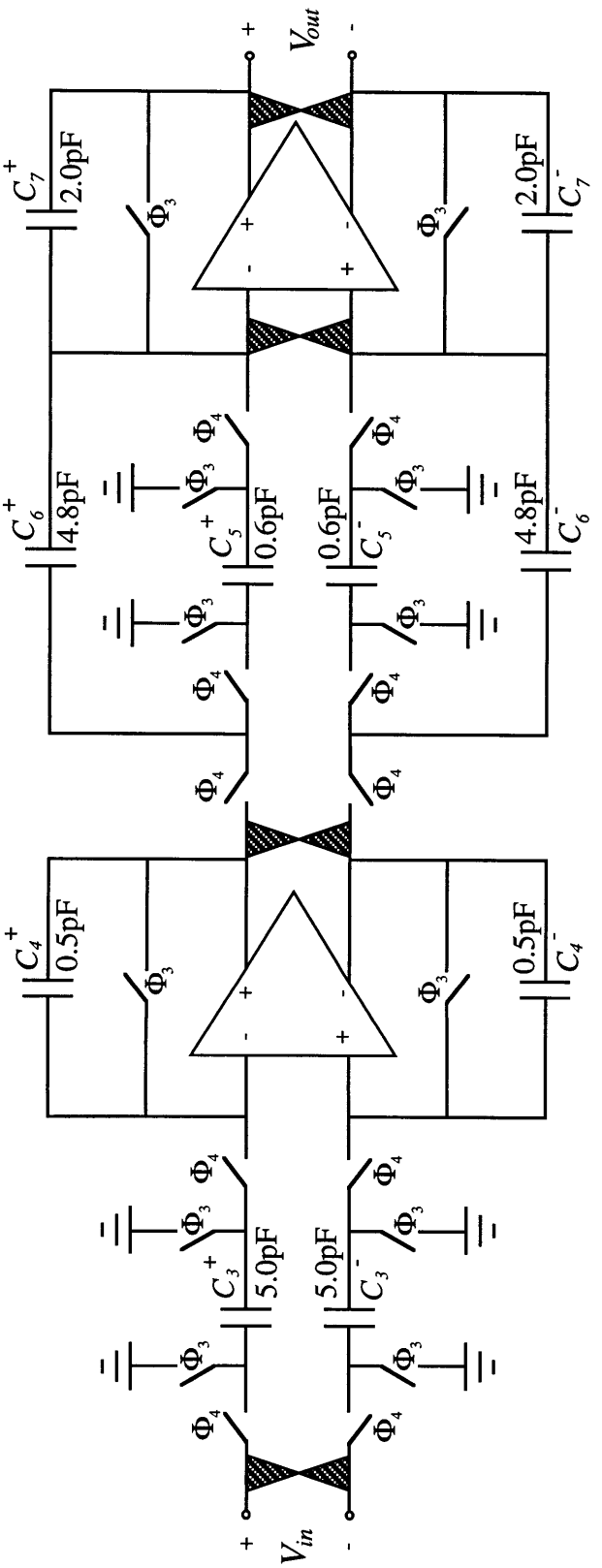


Figure 4.24 Fully Differential P+D Circuit

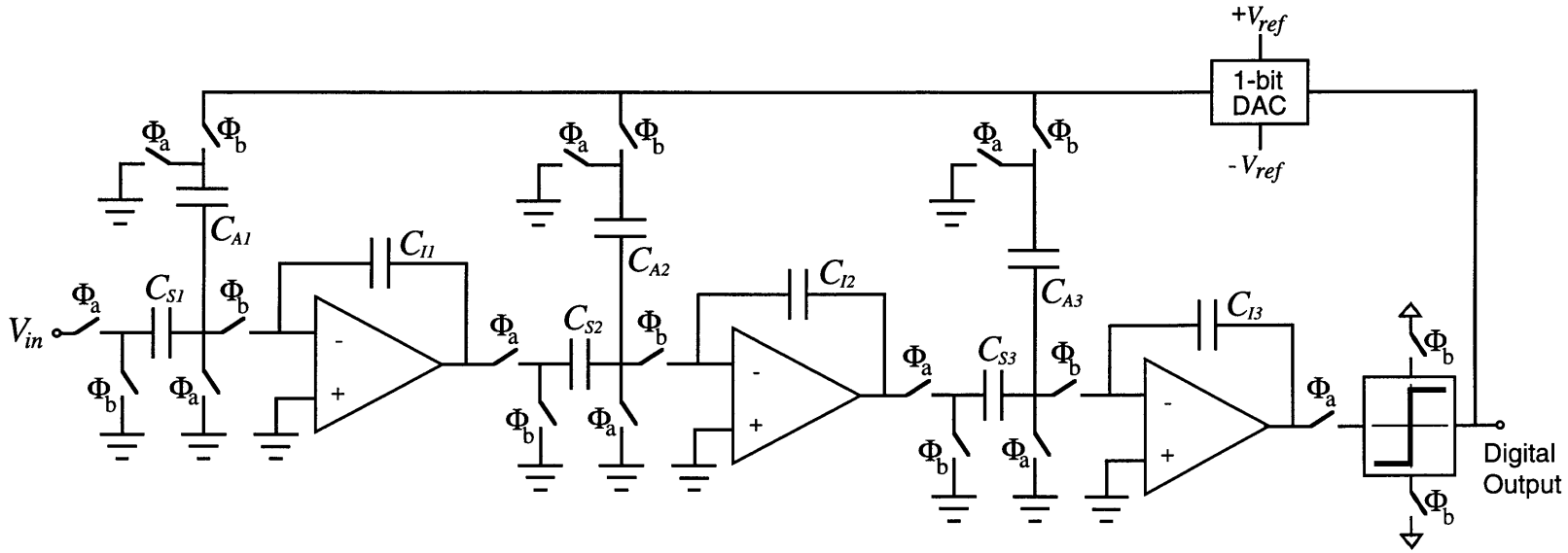


Figure 4.25 Third Order Δ-Σ Modulator

$$K_3 = \frac{C_{S3}}{C_{I3}} \quad [4.44]$$

$$A_1 = \frac{C_{A1}}{C_{S1}} \quad [4.45]$$

$$A_2 = \frac{C_{A2}}{C_{S2}} \quad [4.46]$$

$$A_3 = \frac{C_{A3}}{C_{S3}} \quad [4.47]$$

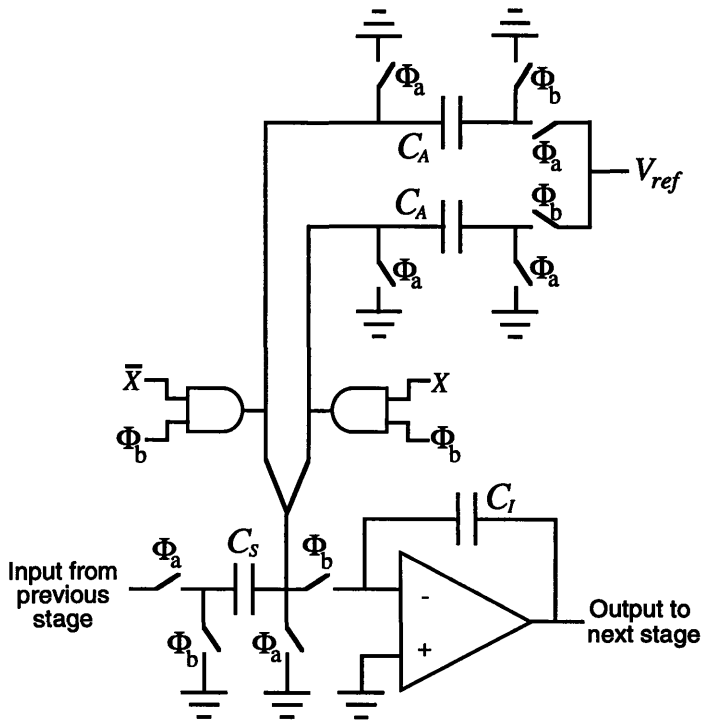


Figure 4.26 Bipolar Feedback using a single reference voltage

From a design standpoint, it is desirable to separate the precision DAC feedback voltages from the comparator output values. A technique for doing this is given in reference 44 and was adapted for use here. The basic idea is shown in figure 4.26. Using a single voltage reference, and separate clocking schemes, a positive or negative integration can be achieved as described in section 4.1.2. Recall, positive or negative integration can

be achieved by simply varying to clocking of an integrator. By applying these different schemes to a single voltage reference, bipolar feedback can be implemented. The output from the comparator is used as a control bit to select positive or negative integration. A separate "clean" voltage is used for V_{ref} to avoid noise corruption from the circuit.

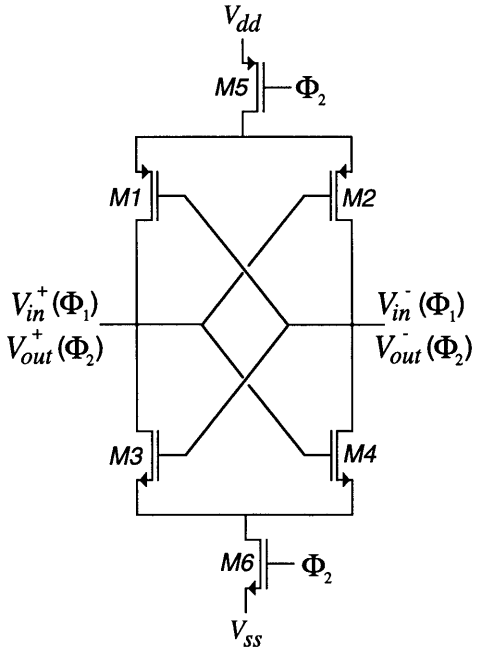


Figure 4.27 Differential comparator circuit

The differential comparator used in the modulator is shown in figure 4.27 [25]. On clock phase Φ_1, the differential input is sampled onto the drain capacitance of transistors *M1-M4*. On clock phase Φ_2, the latch is enabled by switching on transistors *M5* and *M6*. Positive feedback causes the output of the comparator to go to the voltage rails as determined by the sign of the input. The input/output nodes of the comparator are buffered with clocked NAND gates (not shown). Note, large gate lengths are used for the *M1-M4* input devices to reduce length and threshold mismatch. This, in turn, minimizes offset in the comparator.

The circuit realization of the third order modulator is shown in figure 4.28. Note how the single voltage reference scheme has been adapted for the fully differential topology. The fully differential architecture is used again here for its aforementioned benefits.

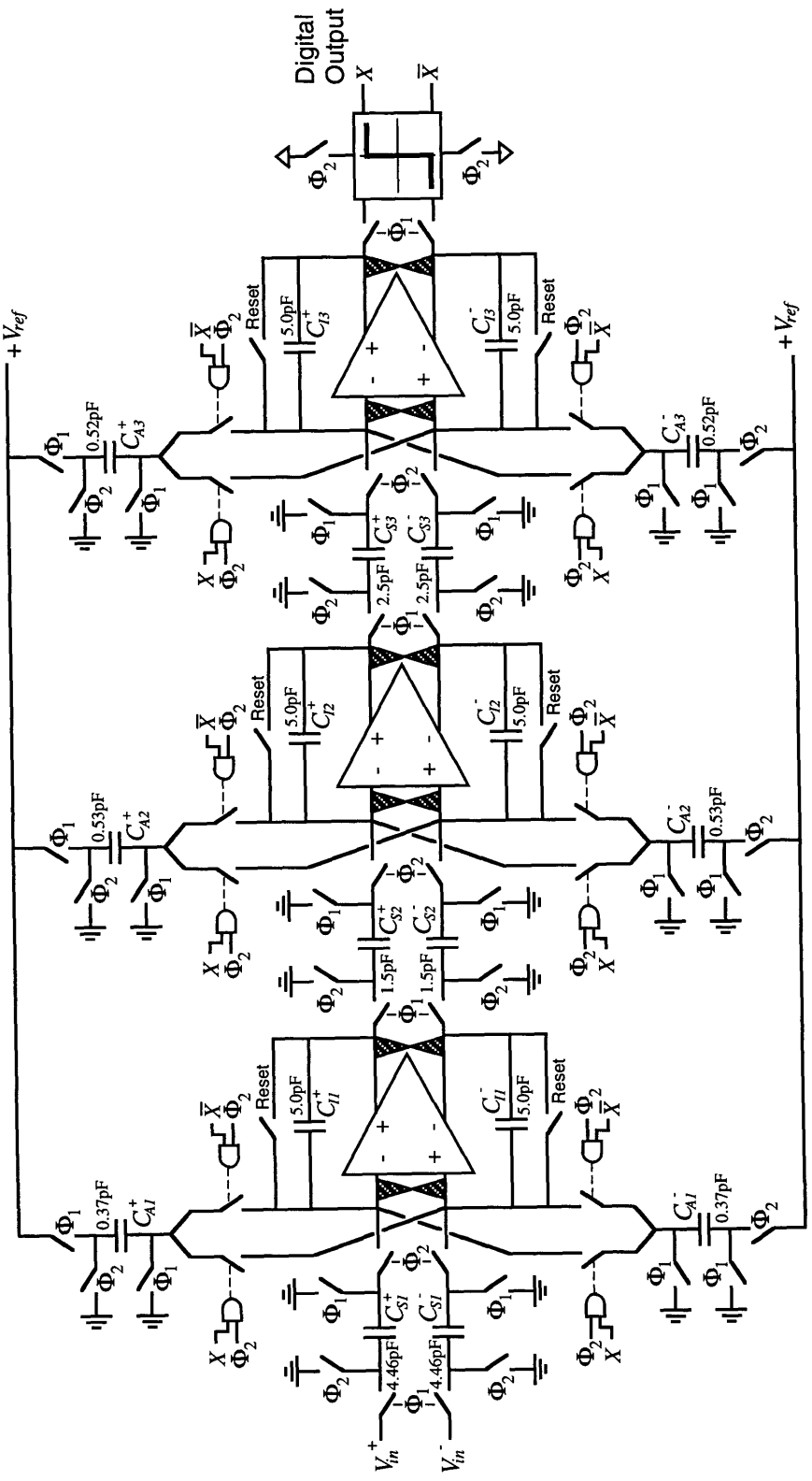


Figure 4.28 Fully Differential Third Order Modulator Implementation

Reset switches are located across the integrating capacitors to initialize their values at start-up or after period of unstable operation.

4.5.2 Incorporating the First Order Modulator and Second Order Reset Loop

With minimal extra circuit complexity, the first order modulator can be implemented from the existing third order architecture. Recall the first order Δ-Σ modulator is necessary to implement the third order accelerometer system. Similarly, the comparator necessary for the second order reset mode of the accelerometer is implemented with the same comparator used in the third order Δ-Σ modulator. This is illustrated in figure 4.29.

Note the extra comparator placed at the output of the modulator. In the third and fifth order accelerometer modes, this comparator acts as a digital latch for storing the output value from the first comparator. Because feedback within the modulator occurs during Φ_2 and the force feedback to the proof mass occurs during Φ_1, the output value from the modulator must be stored an extra half clock cycle. When the accelerometer is operating in its second order reset mode, the second comparator samples the output from the P+D compensation and determines its polarity. Unlike the output of the Δ-Σ modulator, the output from the P+D compensation is available on clock phase Φ_2 and therefore can be clocked directly into the second comparator. Clocking the P+D compensation directly into the second comparator avoids extra loop delay and therefore minimizes negative phase in the loop.

Note that the second comparator is chopped. By chopping the second comparator, any offset in the comparator is effectively removed. Without chopping, any offset in the comparator would place the steady state deflection of the proof mass (during reset mode) away from the true electrical center[68]. After stabilizing the proof mass, an offset greater than a few Å would inhibit stable operation in the fifth order mode. As an example, figure 4.30 shows the steady state deflection of the proof mass during reset mode when the sec-

68. Small offsets in the first comparator are insignificant. The output of the third integrator will assume the same DC offset as the comparator thus removing any offset error which would be present at the output. The offset only becomes a problem if it compromises the dynamic range of the differential amplifier used to implement the third integrator.

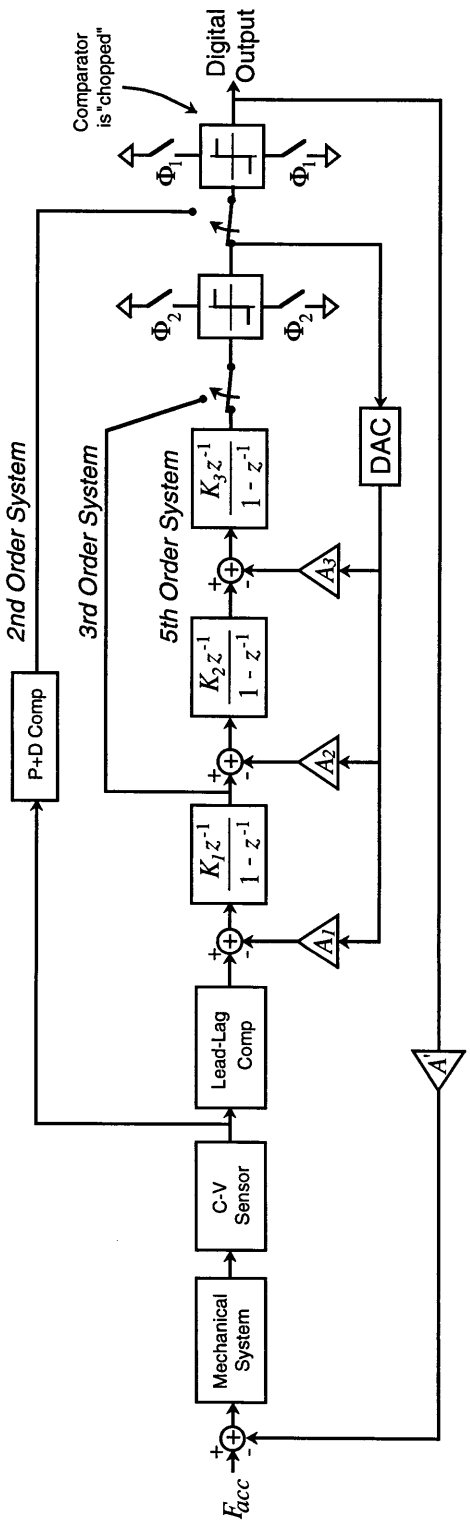


Figure 4.29 Circuit Realization for the Second, Third, and Fifth Order Accelerometer Modes

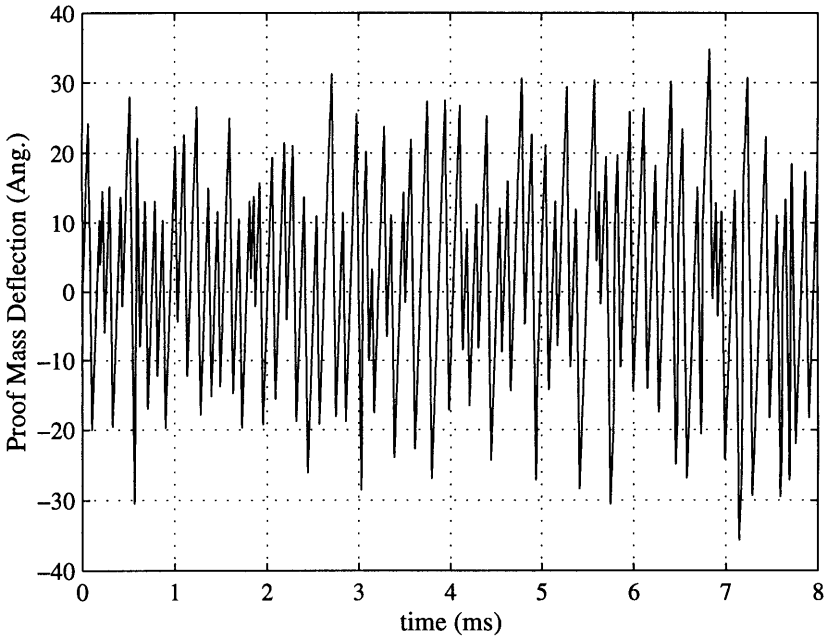


Figure 4.30 Proof mass deflection with a 100mV comparator offset - with chopping

ond comparator is given a 100mV offset and chopping is not used. Note the proof mass settles to a steady state deflection near 50Å, an offset which would barely allow stable operation in the fifth order mode. In contrast, figure 4.31 shows the accelerometer response with the same comparator offset, only now the second comparator is chopped. The steady state deflection now remains within ±30Å of the zero deflection point, close enough to resume stable operation in the fifth order mode.

4.6 Amplifier Design

The operation of the C-V sensor, compensation, and Δ-Σ modulator, set the performance requirements for the operational amplifiers used in each circuit. The C-V sensor in combination with the lead lag network settles four amplifiers in series. As a result, the speed requirement for the front end amplifiers is quite demanding. In addition to settling several amplifiers in series, the speed requirement is increased further by the clocking

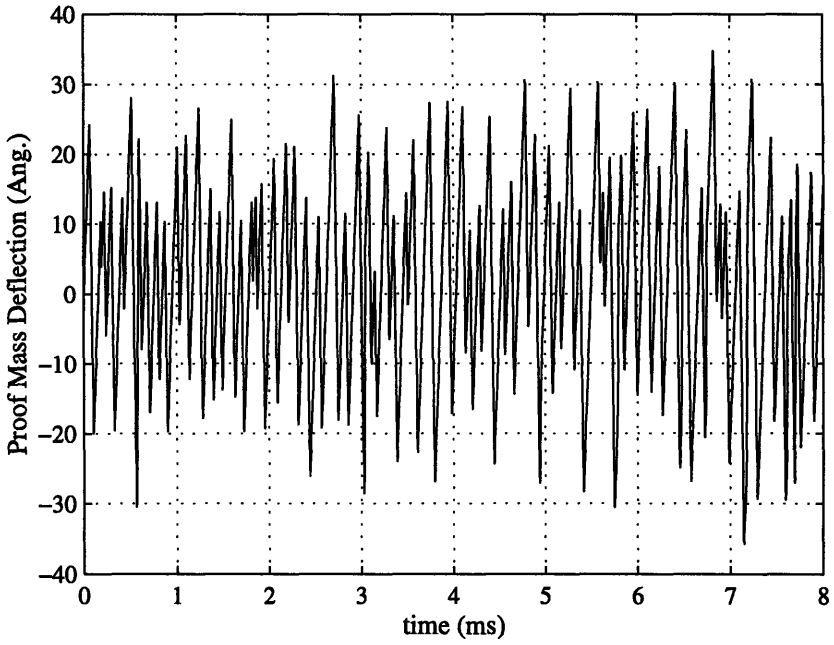


Figure 4.31 Proof mass deflection with a 100mV comparator offset - with chopping

scheme used for the first two stages. Recall the capacitive position sense occurs only during clock phase Φ_2. During this time, the amplifiers must settle twice.

The bandwidth requirement for the amplifiers was approximated as follows. The total settling time was assumed to be 400ns (half of Φ_2 plus a 20% margin of error). Because of the 20-bit target resolution for the accelerometer, 20-bit settling was desired from each amplifier for each sampling period. This results in a time constant, τ, of

$$13.86\tau = 400ns \quad ; \quad \tau = 28.8ns \qquad [4.48]$$

which would require a unity gain bandwidth of 5.5MHz. This first estimate ignores the effects of settling four amplifiers in series and assumes unity feedback in all cases. Approximating the total time constant of the four amplifiers as the sum of the individual time constants[69] increases the required bandwidth estimate to 22MHz. Now, accounting for a nonunity feedback around the opamps, an average feedback factor or 0.25 is assumed resulting in a total bandwidth estimate of 88MHz.

69. This is analogous to the use of open circuit time constants to evaluate a circuit's bandwidth.

The opamps used in the Δ-Σ modulator have considerably more time to settle than those of the first stage opamps. The amplifiers used in the Δ-Σ modulator are identical to those used in the C-V sensor and compensation networks however they are biased with less current which reduces both the power dissipation and bandwidth.

4.6.1 The Single Ended Amplifier

The single ended amplifier used in the C-V sensor is diagrammed in figure 4.32. This single stage (folded cascode) topology was selected for its (near) single pole settling characteristic. The bandwidth of the amplifier is determined by a single dominate pole set by the output impedance of the amplifier and the load capacitance. Because only the dominate pole affects the rolloff in magnitude of the amplifier at crossover, a very high phase margin can be achieved. The second pole from this topology results from the gate capacitances of devices *M19* and *M20* combined with the $1/g_m$ diode-connected impedance of *M20*. This second pole prevents the amplifier from having a full 90° of phase margin.

Note the auxiliary common source amplifiers located around each cascoded device in the amplifier. These act as gain enhancement amplifiers and boost the DC gain of the device by increasing the output impedance of the amplifier [45,46]. Figure 4.33 illustrates this basic idea.

Without the gain enhancement amplifier, the simple common source cascode has an output impedance of

$$R_{out} = r_{o1} + r_{o2}(1 + r_{o1}g_{m2}) \approx g_{m2}r_{o2}r_{o1} \qquad [4.49]$$

and a gain given by

$$G = g_{m1}(r_{o1} + r_{o2}(1 + r_{o1}g_{m2})) \approx -g_{m1}g_{m2}r_{o1}r_{o2} \qquad [4.50]$$

Repeating the analysis now including the auxiliary amplifier, the output impedance of the stage rises to

$$R'_{out} = r_{o1} + r_{o2}(1 + r_{o1}g_{m2}(A + 1)) \approx g_{m2}r_{o2}r_{o1}A \qquad [4.51]$$

and the gain increase to

$$G' = g_{m1}(r_{o1} + r_{o2}(1 + r_{o1}g_{m2}(A + 1))) \approx -g_{m1}g_{m2}r_{o1}r_{o2}A \qquad [4.52]$$

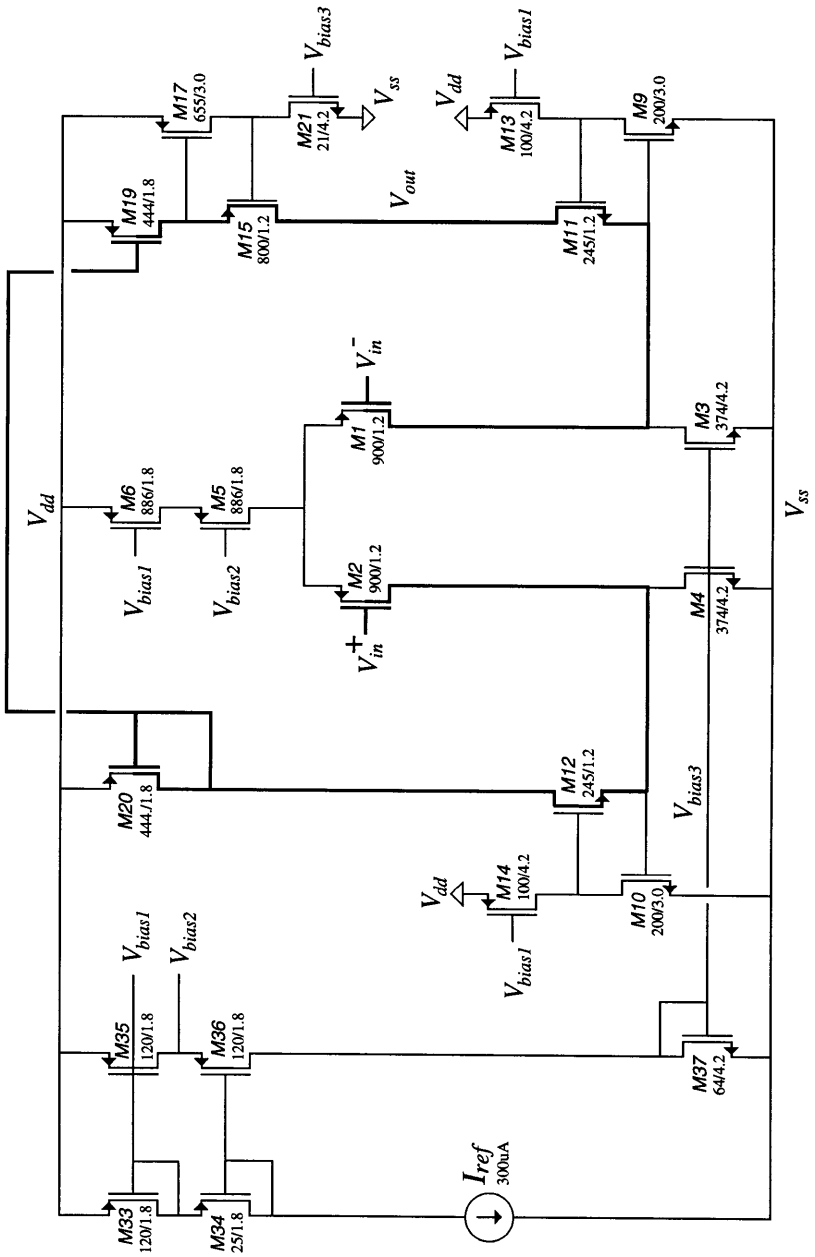


Figure 4.32 The Single Ended Amplifier

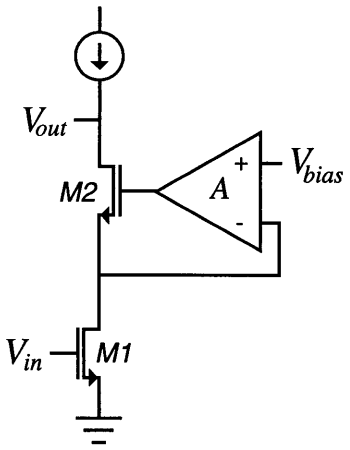


Figure 4.33 Gain enhancement amplifier

A similar analysis shows that the input impedance at the source of *M2* is decreased by the gain of the auxiliary amplifier. The identical effect greatly reduces the input impedance of devices *M11* and *M12* in the single ended amplifier. This almost entirely removes systematic offset from the amplifier. Table 4.1 summarizes the simulated performance of the amplifier.

Parameter	Value
DC Gain	100.4dB
Unity Gain Bandwidth (12pF Load)	83.4MHz
Phase Margin (12pF Load)	60.6°
CMRR (2.5% mismatch)	67.5dB
$PSRR^+$ (2.5% mismatch)	81.2dB
$PSRR^-$ (2.5% mismatch)	64.2dB
Output Swing	-1.5V to 1.3V
Power Dissipation	22.6mW
Input Referred Noise	$1.9nV/\sqrt{Hz}$

Table 4.1 Simulated Single Ended Opamp Performance

4.6.2 The Fully Differential Design

The fully differential amplifier circuit used for the accelerometer's circuits is shown in figure 4.34[70]. The basic function of the fully differential amplifier is identical to that of its single ended counterpart. A common mode feedback loop has been added to stabilize the common mode level at the output of the amplifier at 0V. Transistors *M27* and *M28* form a differential pair which amplifies the common mode voltage. The current from the differential pair is mirrored through *M29*, *M3*, and *M4* to the outputs of the amplifier. The common mode voltage is obtained using the switched capacitor circuit shown in figure 4.35. The common mode voltage, sampled across capacitors C_{1a} and C_{1b}, is periodically sampled onto capacitors C_{2a} and C_{2b} which are then discharged. The capacitors C_{2a} and C_{2b} form two switched- capacitor "resistors" which prevent charge from building up at the center (CM) node due to leakage current or initial conditions. The simulated performance of the fully differential amplifier is given in table 4.2.

4.7 System Noise Analysis

Now that the complete circuit diagrams have been given along with the operation of the amplifier, a full noise analysis can be performed. For the sake of brevity, the equations will not be given here, however, the results from each stage (i.e. C-V sensor, Lead-Lag, etc.) will be given in tabular form. The circuit noise analysis will only be continued to the input of the lead-lag network. Beyond this point, the input referred noise is insignificant due to the large gain of the Lag compensation. Table 4.3 summarizes the noise from the C-V sensor and table 4.4 summarizes the noise from the lead-lag network. In each table, the total noise is given followed by the portion of the noise which resides in baseband. Recall that only the noise present in baseband determines the final resolution of the sensor.

70. A 200μA bias is used for the amplifiers in the Δ-Σ modulator.

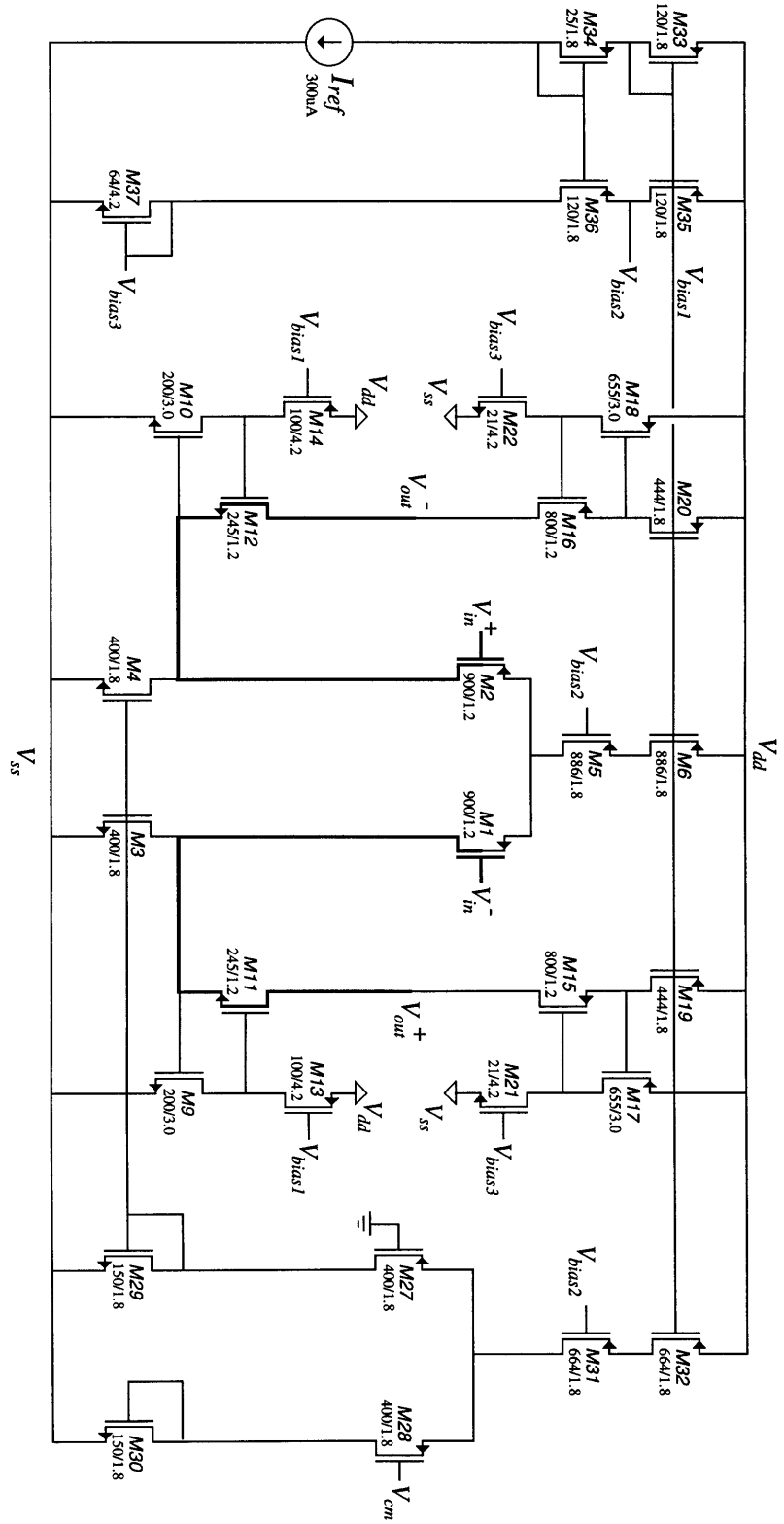


Figure 4.34 Fully Differential Amplifier

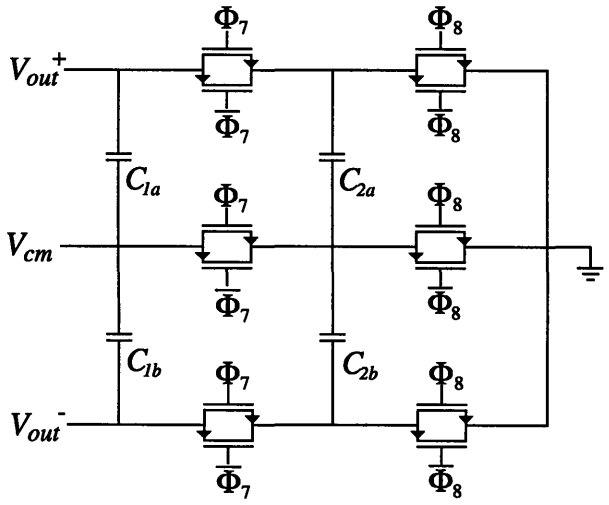


Figure 4.35 Switched capacitor common mode voltage circuit

Parameter	Value
DC Gain	97.9dB
Unity Gain Bandwidth (12pF load)	80.5MHz
Phase Margin (12pF load)	84°
CMRR (2.5% mismatch)	74.0dB
$PSRR^+$ (2.5% mismatch)	93.5dB
$PSRR^-$ (2.5% mismatch)	96.7dB
Output Swing	-1.15V to 1.2V
Power Dissipation	34.3mW
Input Referred Noise	1.9nV/$\sqrt{Hz}$
Common Mode Feedback	
Unity Gain Bandwidth (12pF load)	44MHz
Phase Margin (12pF load)	70.1°

Table 4.2 Simulated Differential Opamp Performance

Noise Source	Total Noise $\overline{x_{rms}}$	Baseband Noise $\overline{x_{rms}}$
Switch (thermal) noise from C_X connection to $-V_1$ and $+V_2$	0.2087Å	0.0132Å
Switch (thermal) noise from C_R connection to $-V_1$ and $+V_2$	0.2087Å	0.0132Å
Switch (thermal) noise from C_X connection to V_{tune}	0.1476Å	0.0093Å
Switch (thermal) noise from C_R connection to V_{tune}	0.1476Å	0.0093Å
Thermal noise from both single ended amplifiers	0.4317Å	0.0273Å
Thermal noise sampled onto C_{S2}	0.3941Å	0.0249Å
Switch (thermal) noise sampled onto C_{i2}	0.1352Å	0.0086Å
Thermal noise from the fully differential amplifier	0.2062Å	0.0130Å
TOTALS	0.7302Å	0.0462Å

Table 4.3 Noise from the C-V sensor

Note the circuit analysis assumes:

- Correlated doubling sampling removes the thermal noise injected across C_{i1}.
- Charge injection from all the switches is cancelled to first order.
- The $1/f$ noise from the amplifiers is removed by chopping and/or correlated double sampling.
- The voltage sources are ideal (noiseless).

Combining the results from tables 4.3 and 4.4, the total baseband noise which results from thermal noise in the circuits is 0.072Å. Note, this is comparable to sensing the differential capacitance to within an accuracy of 34aF. To refer this positional noise to the input of the accelerometer it is divided by the transfer function of the mechanical system and the Mass (of the proof mass) as shown in equation 3.12 which is repeated here:

Noise Source	Total Noise $\overline{x_{rms}}$	Baseband Noise $\overline{x_{rms}}$
Switch (thermal) noise sampled onto C_5	0.8294Å	0.0525Å
Switch (thermal) noise sampled onto C_7	0.0465Å	0.0041Å
Thermal noise from the fully differential amplifier	0.2568Å	0.0162Å
TOTALS	0.8706Å	0.0551Å

Table 4.4 Front end noise from the lead-lag circuit

$$\overline{a_n} = \frac{\overline{x_n}}{M\frac{X(s)}{F(s)}} \qquad [4.53]$$

Applying equation 4.53, the total input referred acceleration noise integrated over the 1kHz baseband (due to thermal noise) can be calculated[71]:

$$\overline{a_n} = \left[\tilde{x}_n \int_0^{1kHz} \frac{1}{M^2\left|H_{mech}(f)\right|^2} df\right]^{1/2} = 973.4\left(\frac{\mu m}{s^2}\right) = 99.3ng \qquad [4.54]$$

where

$$\tilde{x}_n = \int_0^{1kHz} \overline{x_n^2}\, df\ ,$$

$$H_{mech}(f) = \frac{X(f)}{F(f)}$$

Along with the acceleration noise from the positional measurement error, acceleration noise is also present as a result of electrostatic forces placed on the proof mass by noise present in the reference voltages[72], the input referred voltage noise from the single ended amplifier (which places the proof mass at virtual ground), and the thermal noise

71. Note, a 250Hz pole placement is used for the mechanical system in this calculation. If 3.23kHz were used for the mechanical resonance, the resultant noise would be 293μg using the same calculation.

72. Including the feedback voltages. The voltage references are output from an OP-227 low noise amplifier. The wideband noise of the amplifiers are given as $3.9nV/\sqrt{Hz}$. See chapter 5.

from the connection resistance to the proof mass. Note, all of these noise sources are effectively chopped by the C-V sensor implementation. Thus, as with the C-V sensor and lead-lag circuitry, only wideband noise is significant. The acceleration noise can be obtained by inserting the voltage noise into equation 1.4 and integrating over baseband. The results are given in table 4.5.

Noise Source	Baseband Noise $\overline{a_{rms}}$
Noise from the voltage references	2.58e-13g
thermal noise from the connection to the proof mass	2.10e-16g
Amplifier noise	1.95e-15g
TOTAL	2.58e-13g

Table 4.5 Noise from electrostatic forces placed on the proof mass

To estimate to the total quantization noise, the noise transfer function of the third order Δ-Σ modulator can be used to generate an approximation to the noise shaping characteristic of the entire modulator. This approximation is conservative because the two mechanical integrators provide increased low frequency gain to the loop, further lowering the quantization noise floor in baseband. Using equations 3.26-3.28 with σ set to 8g, the quantization noise is calculated as 0.34μg, well below the desired noise floor.

Combining the results from tables 4.3-4.5, the acceleration noise is 0.354μg, well below the target resolution for the accelerometer. However, recall the Brownian noise calculated in section 2.3.3 produced a noise floor of 2.21μg. Combining the Brownian noise with the other sources of error results in a total noise of 2.24μg[73]

73. This is not a conservative estimate. This analysis ignores mismatches and other process variations as well as deterministic noise, all of which could have a significant impact on the overall resolution.

4.8 Layout

The circuitry for the accelerometer was fabricated at the MOSIS™ foundry using the 1.2μm HP analog process. This process was selected in order to meet the speed requirements of the front end amplifiers of the C-V sensor and compensation networks. Unfortunately, the HP 1.2μm process does not support double-poly capacitors which would require significantly less die area than the metal-poly capacitors which were used. Linear poly-n^+ capacitors were available which had similar capacitance per unit area when compared to poly-poly capacitors, however, due to the large voltage coefficients of the linear capacitors (>1000ppm), the linear capacitors were only used for bypass and filter applications.

4.8.1 The Final Layout

A die photo of the circuit layout is shown in figure 4.36. The layout is 5.8mm×4.0mm. The total die area could have easily been reduced by a factor of two if poly-poly capacitors had been available. As shown, 34 pad connections to the chip are placed around the left, lower, and right sides of the die. Sixteen connections on the upper side of the die are used for bonding to the mechanical sensor. Every other connection to the mechanical sensor is grounded to minimize coupling between signal lines.

4.8.2 Layout Considerations

A few general precautions which were taken during the layout of the circuit include:

- A basic common centroid layout was used to achieve improved matching between capacitors.
- The top (metal) plates of capacitors were connected to critical nodes whenever possible to minimize parasitics.

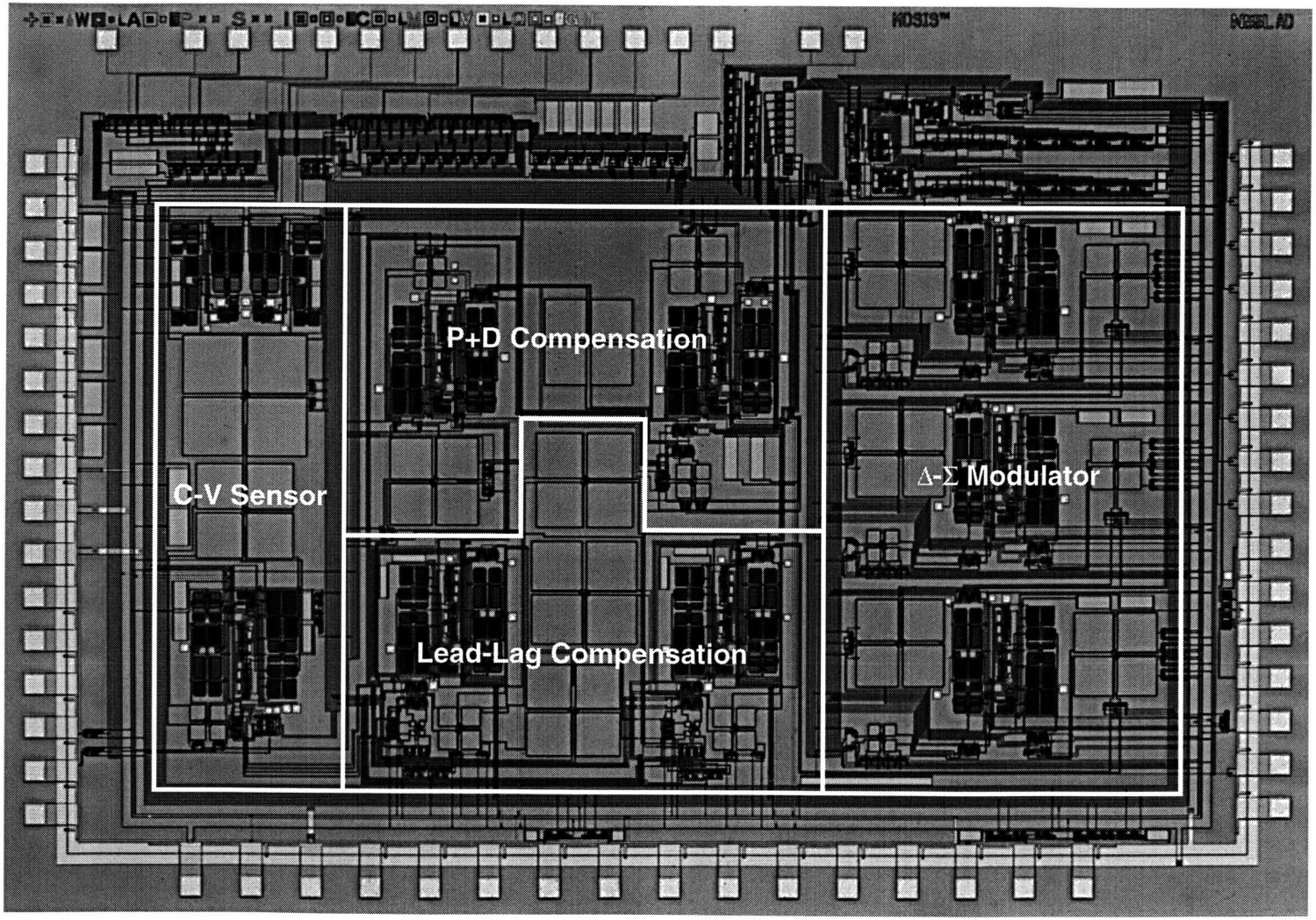


Figure 4.36 Die Photo

• The input connection from the proof mass to the virtual ground of the single ended amplifier is shielded from crossing lines by placing a grounded metal line between the critical node (Metal 2) and any crossing lines (Poly).

• Separate supplies were used for the output buffer from the chip to limit possible feed-back through the substrate.

4.9 System Summary

The important results from chapters three and four are summarized in table 4.6.

Parameter	Simulated Value
Resolution	2.24μg
Baseband	1kHz
Power Consumption	285.3mW
System Crossover	4.5kHz
Die Area	5.8mm×4.0mm

Table 4.6 Chapter 3 and 4 summary

CHAPTER 5

Testing and Results

After the design and fabrication of the accelerometer, the next step was to design a test system to verify its functionality. A full test system was designed which included the data acquisition circuitry, "glue" logic for the mode control, and biasing for the accelerometer circuitry. The test system is comprised of two boards. A larger test board contains most of the circuitry for the test system while a more compact secondary board houses the ZIF socket for the accelerometer and minimal biasing circuitry. The secondary board includes high precision references for charging the fixed electrodes of the proof mass and reference structures and biasing circuitry for the control chip. The minimal design of the secondary board is done to facilitate application of different acceleration inputs without stressing the entire test circuitry.

This chapter documents the design and functionality of the test system. The structure of the hybrid accelerometer is detailed followed by a discussion of any problems which arose during the bonding process. The functionality results from the integrated accelerometer control chip followed by the full hybrid system are then presented.

5.1 The Test System

As previously stated, the test system is formed from two circuit boards, the first board containing most of the functionality of the test setup while the second board houses only minimal biasing circuitry and the hybrid accelerometer. The basic layout for the main test board is shown in figure 5.1. Note the three ribbon cable connections to the main circuit board, two which connect to the secondary board and one to a PC. The PC interface is used to download data from the accelerometer for analysis. One of the connections to the secondary board is used to send and receive data. The last cable carries several ("clean") analog voltages which are used to generate precision references for the accelerometer and power the chip. The main test board will be detailed in the following section and is followed by a description of the secondary board (Board II).

5.1.1 The Clock Generators

Two programmable logic arrays (GAL22V10B) are used to generate the clocks necessary for operation (and control) of the accelerometer. The first PAL[74] subdivides a 20MHz clock to generate an 80-state FSM (finite state machine). The 80-state output of the first PAL is used by the second programmable logic array (PAL2) to generate the non-overlapping system clocks for the accelerometer. Other outputs from PAL1 are used to subdivide the main clocks. The slower clocks control the switched-capacitors used in the common mode feedback circuitry of the fully differential opamps. The main system clocks along with some of the control clocks are shown in figure 5.2. Recall from chapter 4, Φ_1 through Φ_{S1} are used to control the switched capacitor circuitry of the C-V sensor, compensation networks, and Delta-Sigma modulators. Φ_5 and Φ_6 which run at half the sampling frequency of the accelerometer (250kHz) are used to control the differential chopping circuitry. Φ_7 and Φ_8 (shown at the bottom of figure 5.2) are the slower clocks which control the switched-capacitor circuitry used for generating the common mode sig-

74. Figure 5.5 shows the connections for the clock generators, PAL1 and PAL2. They are omitted here to avoid redundancy later when the full schematic is given.

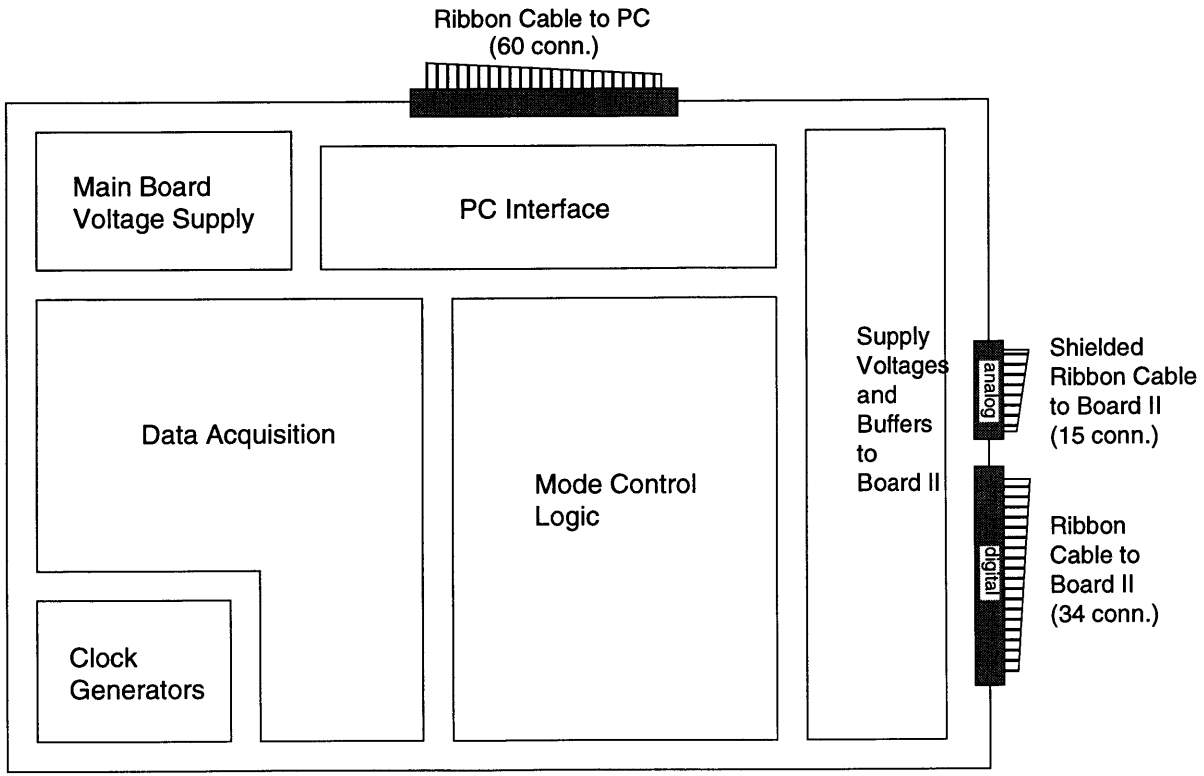


Figure 5.1 Layout for Main Test Board (Board I)

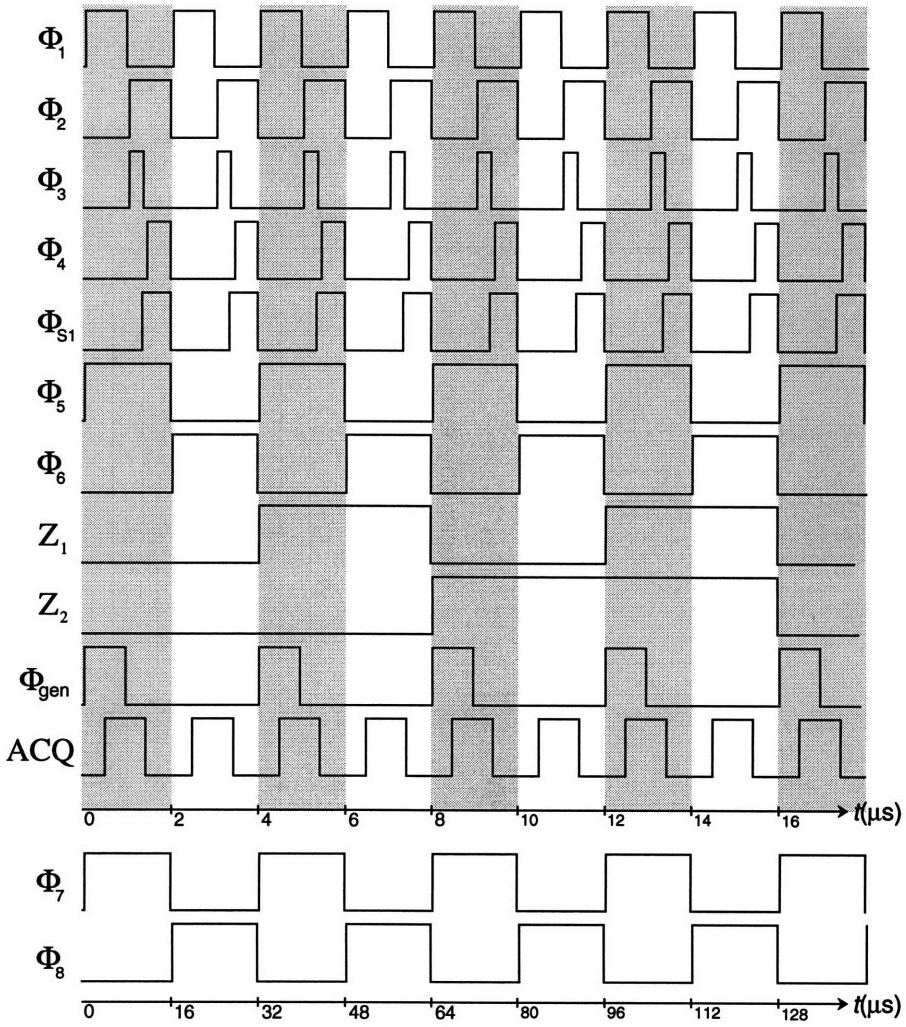


Figure 5.2 Clock Waveforms

nals in the fully differential amplifiers. The remaining waveforms are used for internal control on the main board.

5.1.2 Data Acquisition Circuit

The functionality of the data acquisition circuitry[75] is illustrated in figure 5.3. PAL3 is used to control the data acquisition circuitry. The data acquisition has two modes of operation, an "acquire" mode where data is stored in SRAM (KM681001) during oper-

75. The data acquisition circuitry was derived from similar work in reference [47].

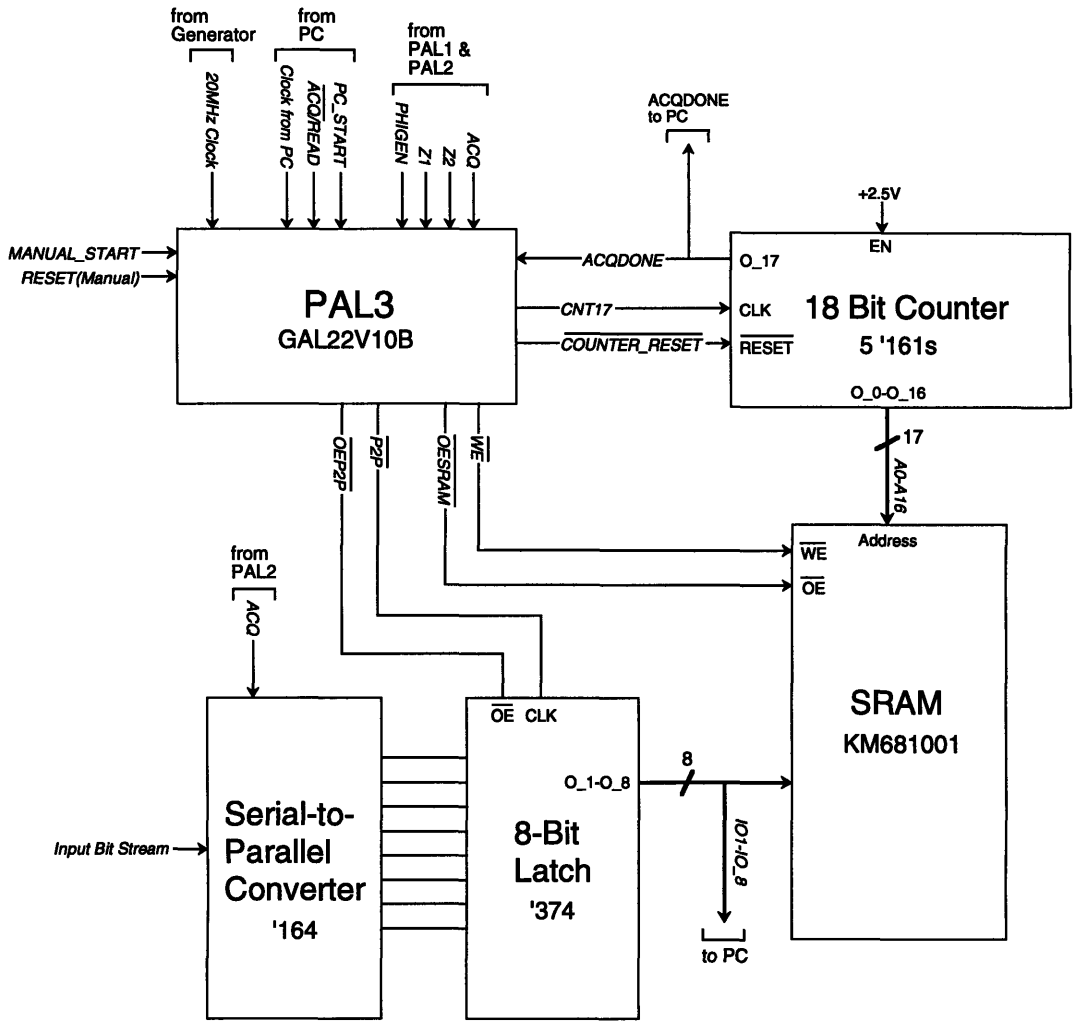


Figure 5.3 Data Acquisition Control

ation of the accelerometer and a "read" mode when the data is clocked into the PC. The mode of operation is selected via the $\overline{ACQ}/READ$ line from the PC. In the acquire mode, the 18-bit counter is reset when either the *MANUAL_START* or *PC_START* has a low-to-high transition. Just after the transition, data acquisition begins. Internal flags (not shown) in PAL3 are used to properly sequence the start of the data acquisition.

Two pieces of information are stored during a data acquisition, the output from the accelerometer and the mode bit. The mode bit sets the mode of operation of the accelerometer, a "0" (-2.5V) indicates reset mode and a "1" (+2.5V) indicates higher order operation. Third order or fifth order operation is selected for the "higher order operation" using

a separate manual control line implemented with a SPDT switch and debounce circuitry (not shown).

Before the data is stored in the SRAM, it is first clocked into 8-bit serial-to-parallel converters (74LS164s). Once the buffers are full, each byte of information is clocked into 8-bit latches (74LS374s) where it is stored until the information is loaded in SRAM. The SRAM holds 128 kBytes, thus the acquisition system is capable of storing just over one million samples of data. Each time a byte of information is loaded in the SRAM, the 18-bit counter is incremented to point to a new address within the SRAM. Note that only 17 bits are necessary to address 128k of SRAM. The MSB of the counter is used to indicate when an acquisition has been completed. When the counter reaches 2^{17} and the MSB of the counter changes from "0" to "1", PAL3 knows to stop clocking data and waits for the PC to begin read mode. Once the PC receives the *ACQDONE* signal from the counter, the $\overline{ACQ}$*/READ* line is toggled and the read mode begins. In the read mode, control of the counter is passed from on board clocking to the clock from the PC (*PC_CLOCK*). The PC then increments the counter and stores the bytes of data as they become available.

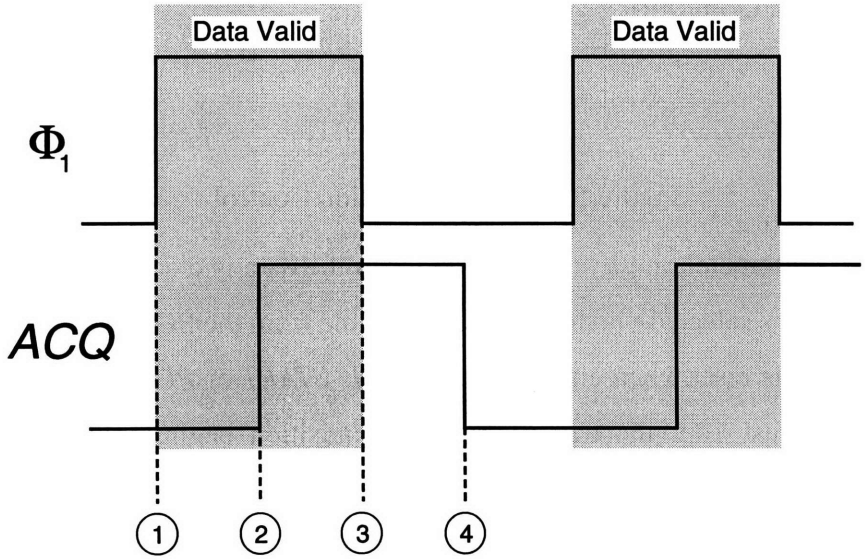


Figure 5.4 Acquisition Timing

The simplified clocking scheme for the data acquisition is shown in figure 5.4. Recall from chapter four that the output from the accelerometer is valid only during Φ_1. Thus the data must be sampled at this time. At time "1" in figure 5.4, the data becomes valid. The data should not be sampled right at this point to avoid possible race conditions. The address counter is incremented at this point every eight cycles (except on the first cycle so that the address "000...0" will not be skipped). At time "2", the *ACQ* signal goes high and the data is clocked into the serial-to-parallel converters. This is the optimal point to sample the data as this is the farthest point from a transition. At time "3" the 8-bit latch is loaded (every eight cycles). Finally, at time "4" the SRAM is loaded from the output of the 8-bit latch (again, every eight cycles).

Figures 5.5 and 5.6 document the schematics of the data acquisition circuitry.

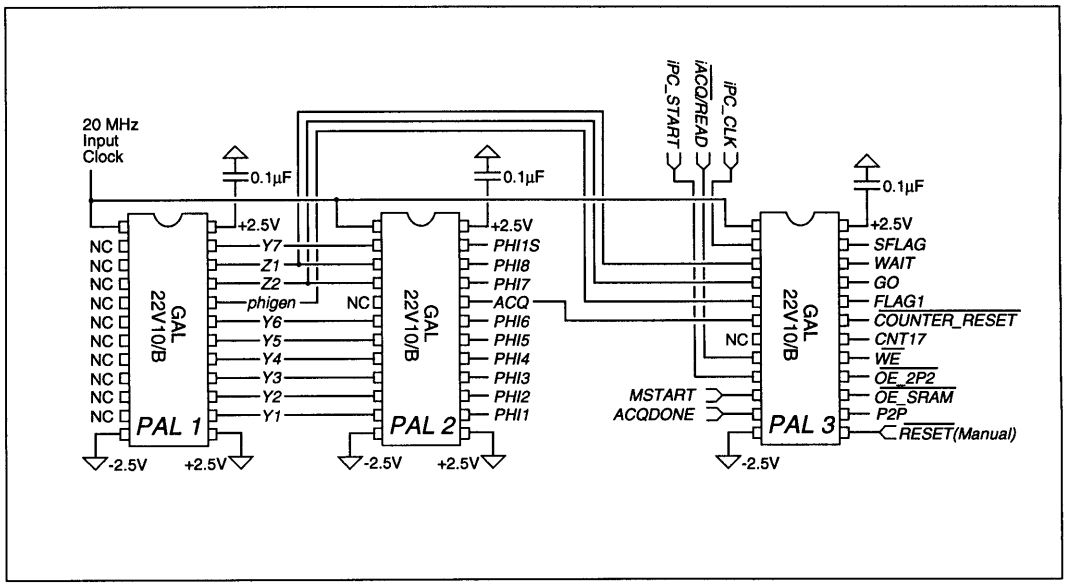


Figure 5.5 Data Acquisition Circuitry - Schematic 1

5.1.3 The Mode Control for the Accelerometer

Though the mode control circuitry of the test system requires about the same board space as the data acquisition circuitry and the same number of ICs, it is much simpler in concept. Recall from chapter three, unstable operation of the accelerometer is indicated by an abnormally long string of 1s or 0s. Thus by counting the number of consecutive 1s

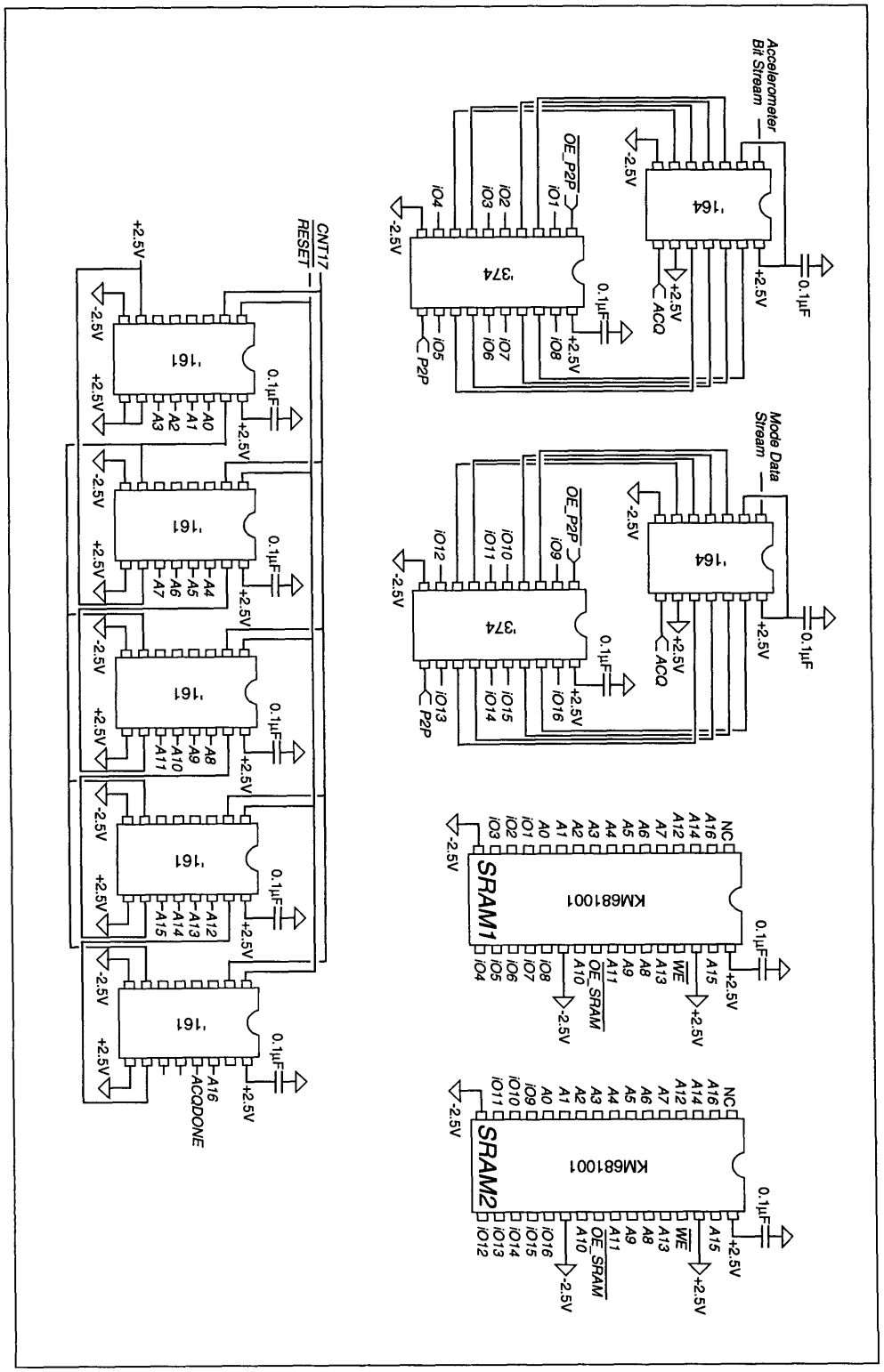


Figure 5.6 Data Acquisition Circuitry - Schematic 2

and 0s which are output from the accelerometer, the stability of the system can be assessed. If the accelerometer is operating in its fifth order mode and a string of 1s is output over a certain threshold length, then the mode control circuitry switches to reset mode to restore stable operation. Similarly, if the accelerometer is operating in its reset mode and over a long period of time there are no long strings of consecutive 1s or 0s then the mode control circuitry knows its time to switch back to higher mode operation (third order or fifth order, depending on which mode has been manually selected). This is the basic function of the mode control circuitry.

Figure 5.7 illustrates the basic operation of the mode control circuitry. PAL4 stores the last bit from the accelerometer in an internal flag (not shown). If the current output of the accelerometer is identical to the previous output, the 8-bit counter is incremented, otherwise, it is reset. The output from the 8-bit counter is input to two comparators. The other inputs to the comparators are connected to DIP (SPST) switches which are connected to pull-up resistors (not shown). The DIP switches are manually programmed to generate the value to which the output of the counter is compared. In the high order mode (third or fifth order), the output from comparator one controls the mode of operation. As long as the counter is continually reset before comparator one triggers, the mode will remain in higher order. If comparator one does generate a trigger ("A=B" or "A>B") then a bit stream of too many consecutive 1s or 0s has occurred and the accelerometer is switched into its reset mode.

Once the accelerometer is switched into its reset mode, the output of the first comparator is no longer used by the mode control circuitry. Instead, the outputs from comparators two and three are used.

When the output from comparator two indicates a long string of 1s or 0s, the 10-bit counter is reset and the accelerometer remains in its reset mode. If, however, no long strings of 0s or 1s are encountered over a long period of time, and thus, the 10-bit counter is not reset, comparator three will eventually trigger and the accelerometer will be switched (back) into its higher order mode. The schematic for the mode control circuitry is shown in figure 5.8.

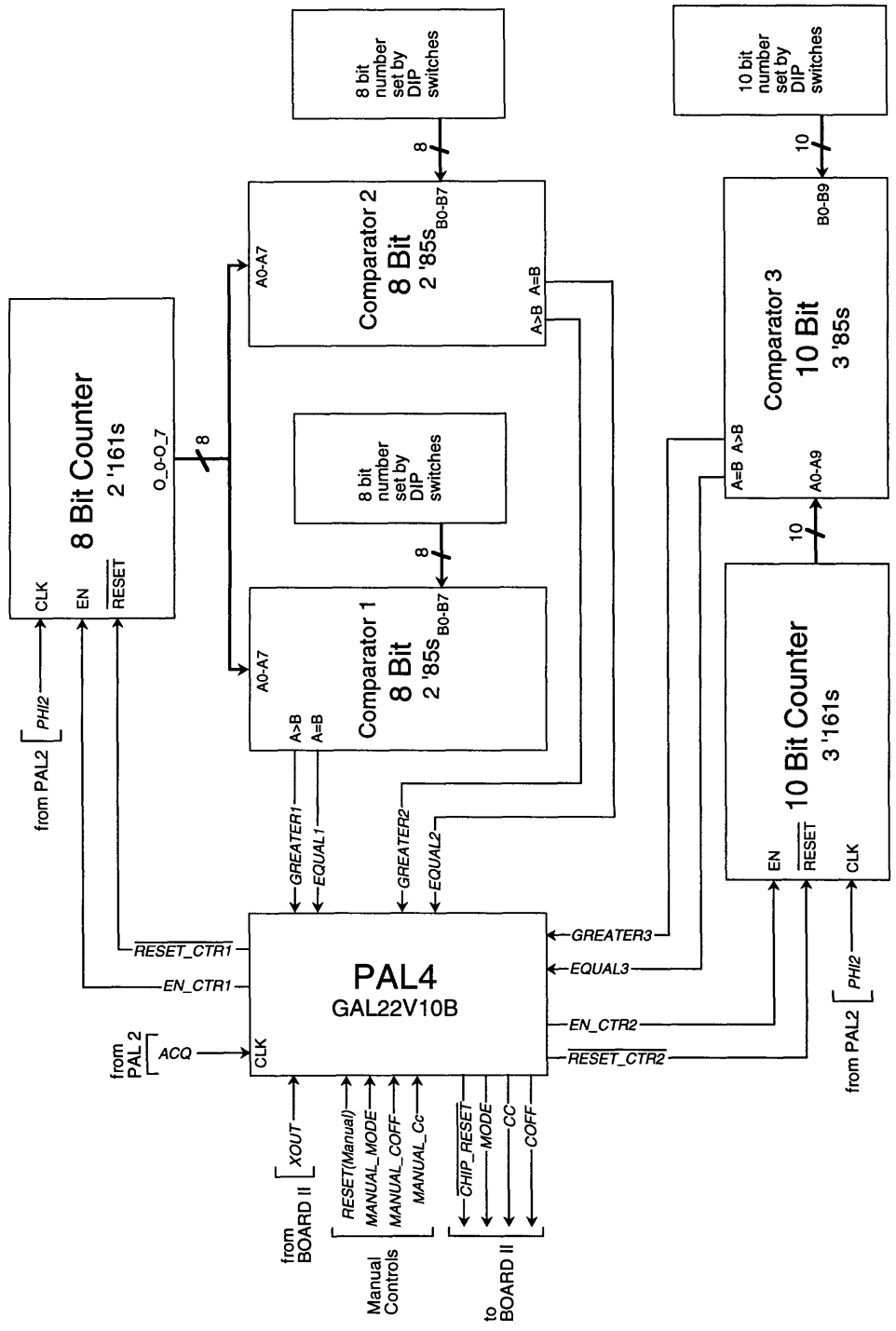


Figure 5.7 The Mode Control System

CLASP simulations were used to determine the optimal points for switching between higher order modes and the reset mode of the accelerometer. It was determined that after 22 consecutive 1s or 0s the accelerometer should be switched from its fifth order mode to its second order reset mode. Similarly, once in the reset mode, if the accelerometer goes 50 clock cycles without a consecutive string of 1s or 0s longer than 10 bits, the accelerometer should be switched back to fifth (or third) order mode. Typically, a string of 1s or 0s longer than 5 to 10 samples indicates instability in a high order Δ-Σ modulator [48]. The longer string of consecutive 1s and 0s which triggers instability in the fifth order accelerometer is probably due to the low bandwidth (crossover) of the system (4.5kHz). Note that only 10 consecutive bits are used to indicate instability for the reset loop which has a much higher bandwidth than the fifth order loop (~150kHz, see chapter 3).

5.1.4 Board I Voltage Supply

Separate voltage supplies are used for the main board to avoid corruption of the analog voltages which supply the secondary board. A separate ground plane is used for the supply voltages to the secondary board to further minimize the possibility of corruption from digital switching noise.

5.1.5 The PC Interface

The interface between the board and PC was accomplished using a Strawberry Tree™ data acquisition board. Using the data I/O board, information was passed between the test board and PC. NEWTON[76], a control program for the accelerometer test board, was written to handle the interface between the test board and PC. Because the Strawberry Tree I/O board has the capability to read two bytes at once, both the mode data and accelerometer output data are read simultaneously. This greatly simplified design of the data acquisition circuitry. Once the data is retrieved using the I/O board, a second program, CREATE, is used to strip the bit information from the stored bytes for processing using MATLAB®.

76. NEWTON was written courtesy of Michael Lee.

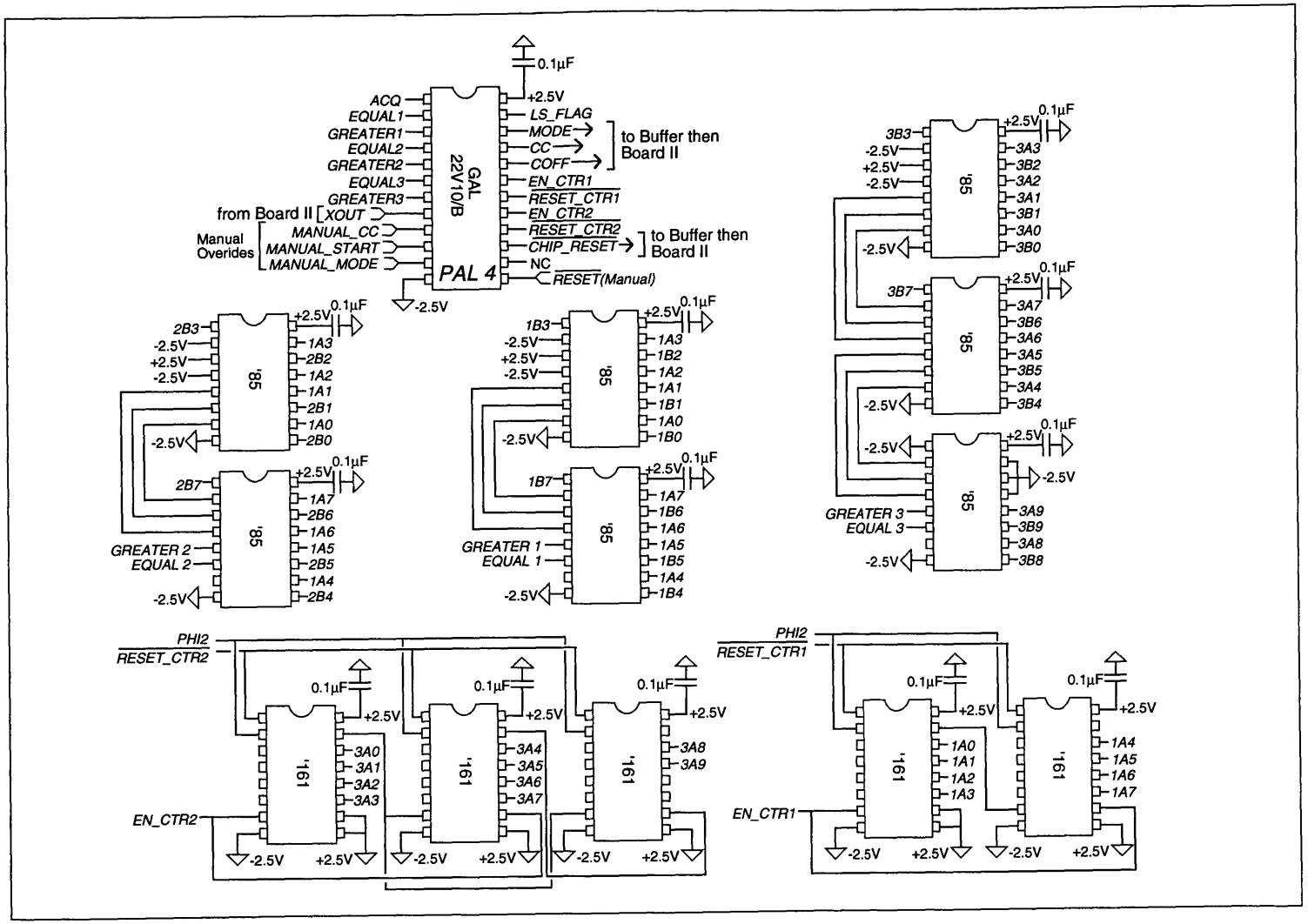


Figure 5.8 Mode Control Circuit Schematic

While the test board voltage levels are between -2.5V and +2.5V, the voltage levels from the PC are between 0 and 5V. To solve this interface problem, (HCPL 2631) optocouplers were used. Along with implementing a level shift, the optocouplers ensure that no problems will arise from ground loops between the PC and test board.

5.1.6 Supply Voltages and Buffers to Board II

To avoid the problem of having several bulky connectors attached to the secondary test board, the supply voltages for Board II are connected to the main test board. From there, the analog voltages are passed to the secondary board via a 15 connector shielded ribbon cable. The shielding is used to prevent corruption from the digital signals. The digital data which is passed to and from the secondary board is done through a separate 34 connector ribbon cable. Before the digital signals are passed to the secondary board they are buffered using 74HCT245s. These buffers convert the clock signals from TTL levels to a full -2.5 to +2.5V swing.

5.1.7 Board II

Board II is shown in figure 5.8. As previously mentioned, the circuitry for this secondary board was kept to a minimum to facilitate placing the sensor in different acceleration environments. The voltage references and supplies were placed on this board to avoid corruption which would occur over the ribbon cable. Other circuitry on this board includes buffers for the incoming clocks, current biasing for the amplifiers in the accelerometer, and a buffer to drive the output of the accelerometer onto the ribbon cable.

5.1.8 Clock and Signal Buffers

As with the signals which are passed from the main test board to the secondary test board, the output from the accelerometer which is returned to the main test board must also be buffered. A 74HCT245 is used to buffer the output from the accelerometer before it is input to the cable returning to Board I.

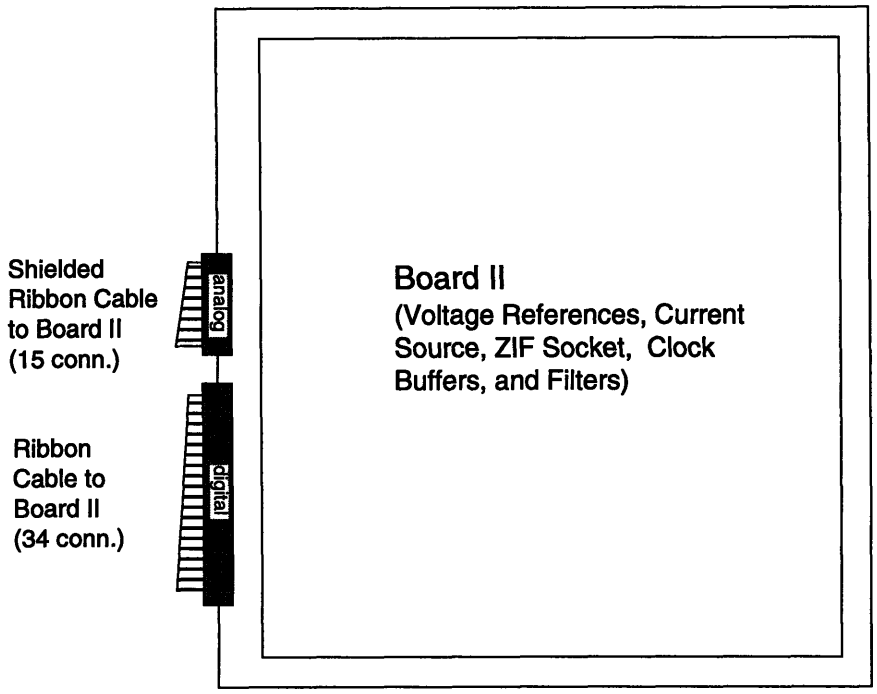


Figure 5.9 Board II

The clocks which arrive from Board I are buffered using 74F07s. This ensures that ringing and crosstalk is removed from the waveforms before they are passed to the accelerometer.

5.1.9 Voltage References

Figure 5.10 shows the circuit which generates the positive reference voltages necessary for the accelerometer (figure 4.17; $+V_2$, V_{tune}, V_{FB})[77]. A +2.5V reference is first generated from an AD780 reference. The desired reference voltage is selected using a potentiometer placed at the output of the voltage reference. The potentiometer in combination with a 4.7μF capacitor also serves as a low pass filter. The output from the low pass filter is buffered using an OP-227 which in turn supplies a low noise, low impedance voltage over a wide frequency range [49]. Note, all supplies and references are bypassed with

77. This circuit is adapted from reference [49].

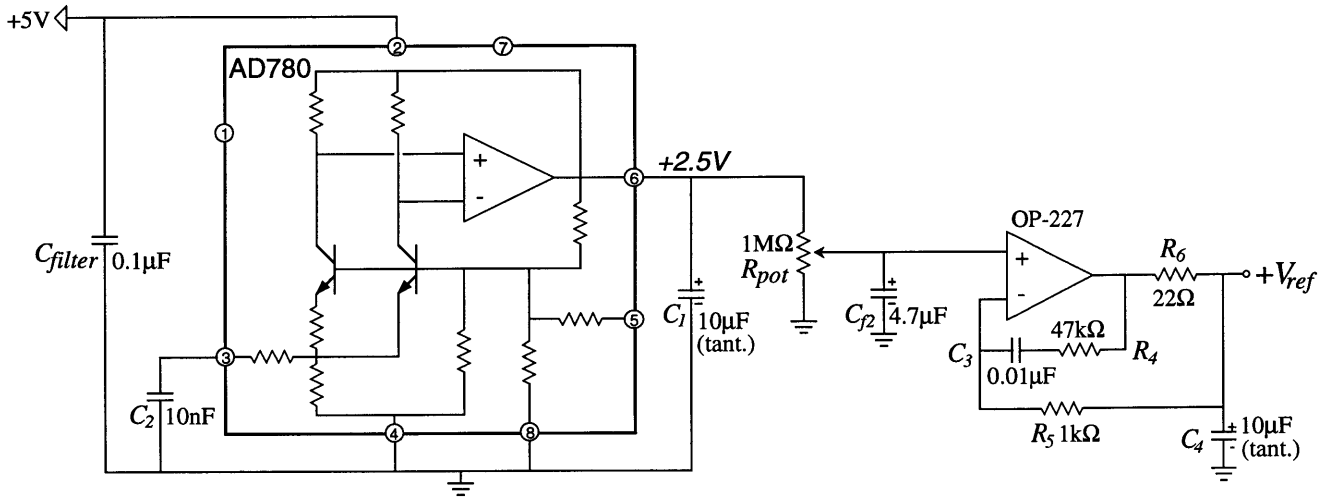


Figure 5.10 Positive Voltage Reference

large tantalum capacitors (82μF) and ceramic bypass capacitors in close proximity to the hybrid accelerometer.

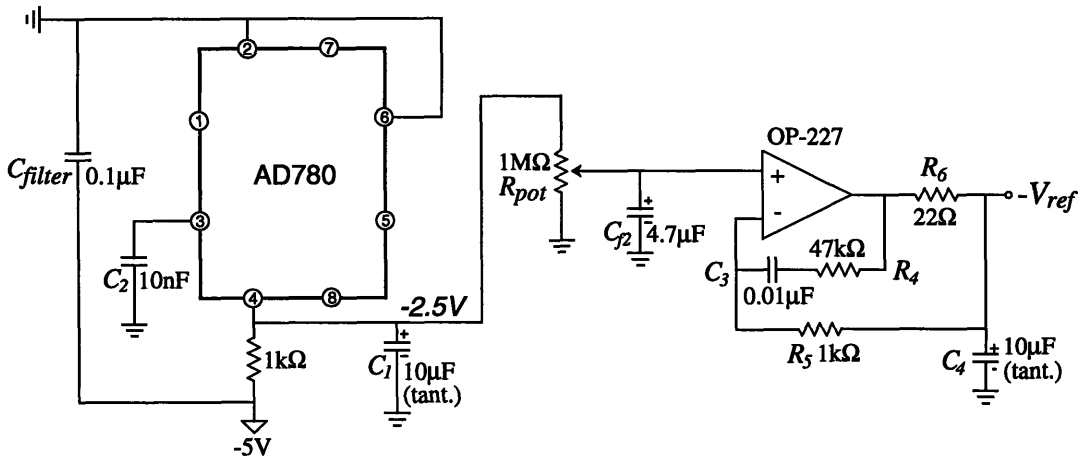


Figure 5.11 Negative Voltage Reference

The circuit shown in figure 5.11 was used to generate the negative reference ($-V_1$) needed by the C-V sensor. The AD780 is used in shunt mode to generate -2.5V which is then passed through a low pass filter and buffered as with the positive reference. Table 5.1 gives the voltages which are generated using the positive and negative reference of figures 5.10 and 5.11.

The absolute accuracy of the voltages given in table 5.1 is not nearly as important

Positive Reference Voltages	
$+V_2$	1.0V
V_{tune}	1.1V
V_{FB}	684.24mV
Negative Reference Voltage	
$-V_1$	-1.0V

Table 5.1 Reference Voltages

as the amount of thermal noise present. The wideband noise of the OP-227 is specified at $3.9nV/\sqrt{Hz}$. Integrating over the 1kHz baseband, the total baseband noise for each voltage

reference is 0.12μV. Note that low frequency noise in the voltage references is modulated to half the sampling rate by the choppers in the C-V sensor and therefore can be ignored in the baseband noise analysis.

5.1.10 Power Supplies

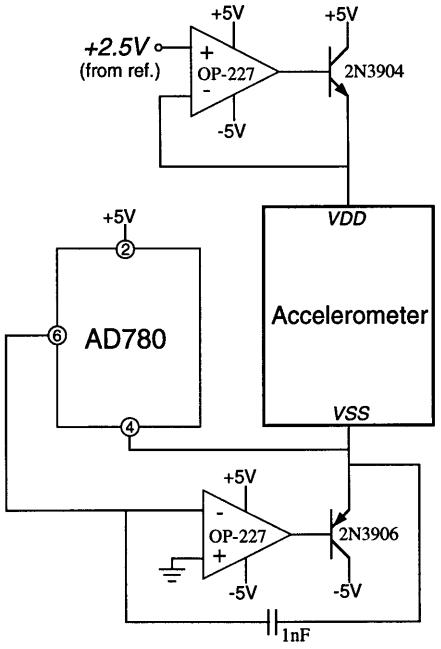


Figure 5.12 Power Supply Circuits

The power supply circuitry for the accelerometer is shown in figure 5.12. For the positive supply (V_{DD}), an OP-227 is used in a feedback loop with a 2N3904 npn transistor to generate the +2.5V supply. The +2.5V reference input to the OP-227 is generated from an additional AD780 (not shown). The negative power supply is generated from an AD780 driven in shunt mode with a feedback loop containing an OP-227 and a 2N3906 pnp transistor. The power supplies, like the voltage references, are bypassed in close proximity to the hybrid accelerometer circuit.

5.1.11 Bias Current

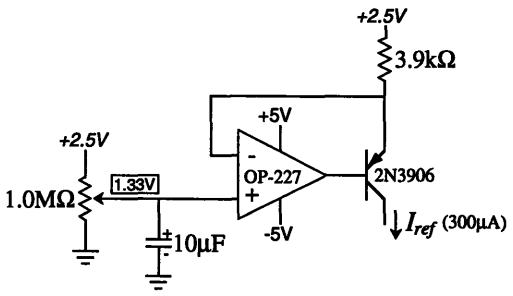


Figure 5.13 Bias Current Circuit

The 300μA bias current is generated using the bias circuit shown in figure 5.13. The feedback loop containing the OP-227 and 2N3906 sets the lower voltage on the 3.9kΩ resistor to 1.33V which sets the bias current at 300μA.

5.2 The Hybrid Sensor

This section details the incorporation of the accelerometer controller IC with the micromechanical structure on the same pin grid array (PGA) package. Some processing problems with the mechanical structure which had not been resolved at the time of testing will be discussed as well.

5.2.1 The Micromechanical Structure

A die photo of the unbonded micromechanical structure which was used for testing is shown in figure 5.14. Note the structure has been changed from the folded pinwheel design which was elaborated on in chapter 2, to a straight tether design. This was done to help separate the secondary resonance modes from the desired fundamental resonance mode. Simulations predicted just less than a factor of two separation of the fundamental resonant frequency from the secondary resonance mode using the folded pinwheel structure. The straight tether design yielded a 2.55× separation of fundamental and secondary

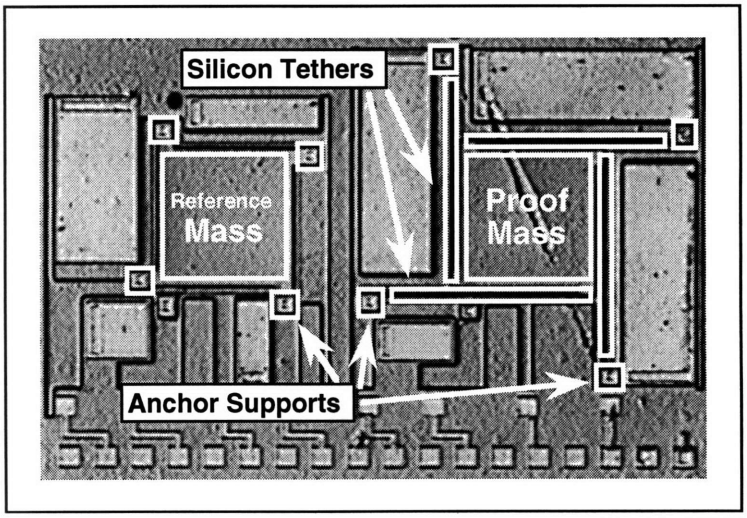


Figure 5.14 Die Photo of Micromechanical Structure

resonances during simulation [18]. Though not a large improvement, it could mean the difference between a high resolution accelerometer and a useless piece of silicon.

The analysis of the straight pinwheel structure is virtually identical to that of the folded pinwheel structure discussed in chapter two. Long silicon tethers are used to provide high linearity for the mechanical spring force[78]. The side-by-side fabrication of the proof mass and reference structure ensure good matching even with process variation. Note the short silicon beams which hold the reference mass rigidly in place. The bonding pads spread evenly along the lower bound of the die photo are used to stitch-bond the mechanical structure and accelerometer controller.

Problems

Some problems were encountered during the fabrication of the mechanical structure which severely degraded its yield and viability. The biggest problem was non-uniformity in the plasma etch which is used to release the proof mass and silicon tethers. A 25% non-uniformity was measured across the 4" wafer. Due to the gross non-uniformity of the etch, the yield was only about 10%.

In the future, a high density plasma etch will be used to free the mechanical structure. The high density plasma etcher will reduce non-uniformity to less than 3% across the wafer. Also, the etcher has more than a 100:1 selectivity of Si:Oxide. A passivation layer can thus be used to prevent the plasma etch from compromising the lower electrode.

5.2.2 Stitch-Bonding

A die photo of the stitch-bonded hybrid sensor is shown in figure 5.15. To minimize parasitics at the sensitive nodes, no ESD protection or guard rings were placed on the sixteen bondpads which connect to the mechanical structure. As a result, ESD problems were encountered several times during the hybridization of the sensor.

Due to time restrictions and the low yield of the mechanical sensor, only six hybrid sensors were bonded for testing. Of these, the first five hybrid sensors had problems with

78. Recall the linearity if the mechanical spring is reduced by the open loop gain of the system. Therefore no effort should be expended to obtain a highly linear spring force.

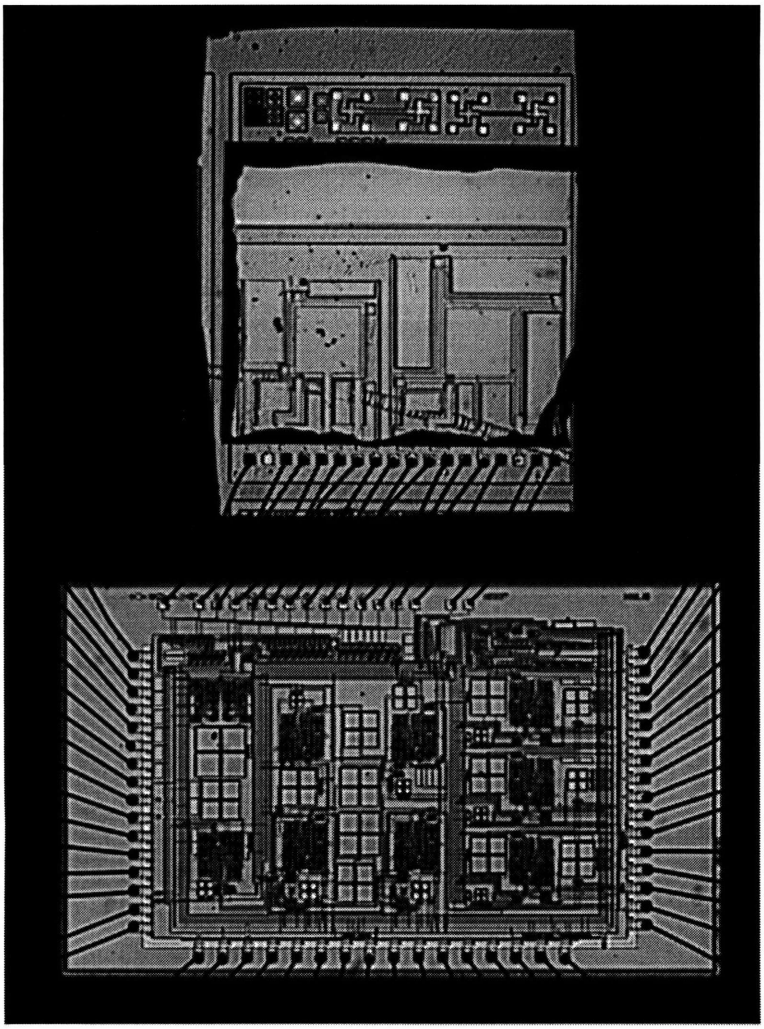


Figure 5.15 The Hybrid Accelerometer

electrostatic discharge blowing out gate dielectrics of MOS transistors. These devices multiplex voltages to the fixed electrodes above and below the proof mass and reference structures. It was not until the very last hybrid sensor was bonded that a viable accelerometer was available for testing.

5.3 Results

The operation of the accelerometer controller was first tested open loop (without the micromechanical structure), then together with the micromechanical structure as a hybrid closed loop system. 10 bonded test chips were packaged at the MOSIS foundry for open-loop testing. 65-pin PGA packages were used to house the test ICs. 82 unbonded die were received and available for stitch-bonding with the micromechanical structure. A 68-pin PGA package was used to hold the hybrid accelerometers. The results of the open loop testing of the accelerometer controller are given in the next section. The results from the closed loop testing are presented in the subsequent section.

5.3.1 Open Loop Testing

Since the accelerometer controller was designed for use in a closed loop system, only basic functionality could be tested with the chip operating open loop. The amplifier bias voltages for each of the amplifiers were first tested. Basic testing was then performed to assess the functionality of each system block.

The inputs to the first and third order Δ-Σ modulators were grounded to observe the quantization noise spectrum and offset in their output spectra. Because the Lead-Lag compensation has a pole placed at DC, open loop testing consisted of making sure the outputs "railed" when the chip operated in its higher order mode (when the Lead-Lag compensation is used). To assess the functionality of the P+D compensation, the output waveform from the P+D compensation was observed. Since the input to the P+D compensation is just the "chopped" offset from the C-V sensor, the output of the P+D compensation should alternately settle to plus and minus the amplified offset of the C-V sensor.

Open loop testing of the C-V sensor consisted of verifying that the proper voltages were applied to the fixed electrodes about the proof mass and reference structure including $-V_1$, $+V_2$, V_{tune}, and V_{FB}, as detailed in section 4.3.2. Because the feedback mechanism (V_{FB}) was examined at this point, the functionality of the force feedback was tested simultaneously. Due to a layout error, the outputs from the differential amplifier in the C-V sen-

sor were not connected to probe pads and thus, measurement of the output voltage from the C-V sensor was not possible.

Of the 10 chips which were tested, only one amplifier failed to bias correctly (Chip#9-the first amplifier in the P+D comp.). Every chip passed the basic functionality test for the C-V sensor and force feedback. The offsets of several of the single ended amplifiers were tested and in each case the offset was too small to measure using the oscilloscope (< 2mV). For all but the one defective chip, the P+D compensation and Lead-Lag compensation passed the basic functionality tests aforementioned. The output spectra from the first order Δ-Σ modulators were all very close to the simulated spectra using CLASP. Recall, the first order modulator is used when the accelerometer is selected to run in its third order mode.

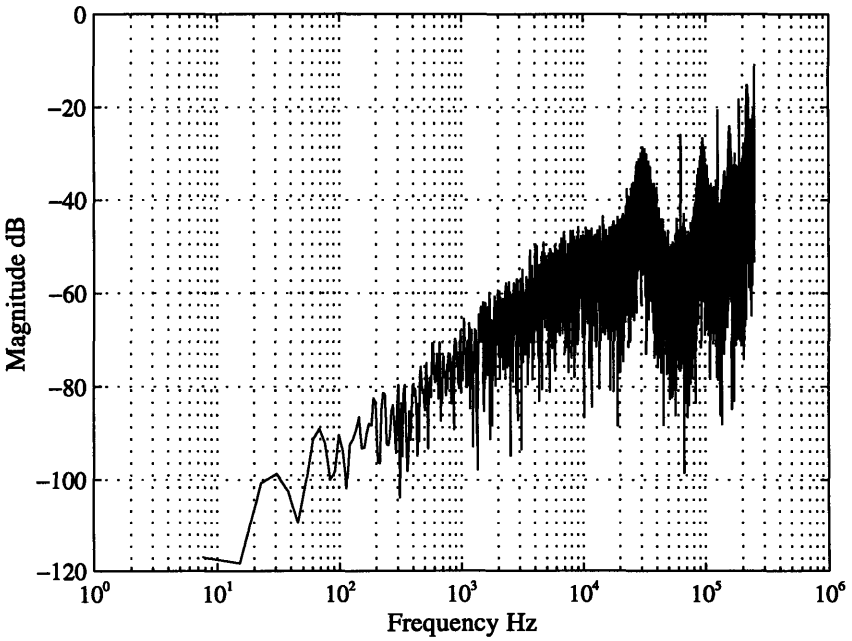


Figure 5.16 Output spectrum from first order modulator with inputs grounded

A sample output spectrum from one of the first order modulators (chip#6) is shown in figure 5.16. This modulator has a DC offset of only -135dB (not shown in figure 5.16). Several of the modulators had very low DC offsets as well. This is as a direct result of only using a single polarity reference voltage as described in section 4.5. Because a single

reference voltage is used to generate both the positive and negative feedback of the modulator, the DC offset is only a result of capacitance matching error. With 8-bit capacitance matching, the DC offset is guaranteed to be no worse than -48dB.

While excellent results were observed for the first order modulator, the third order

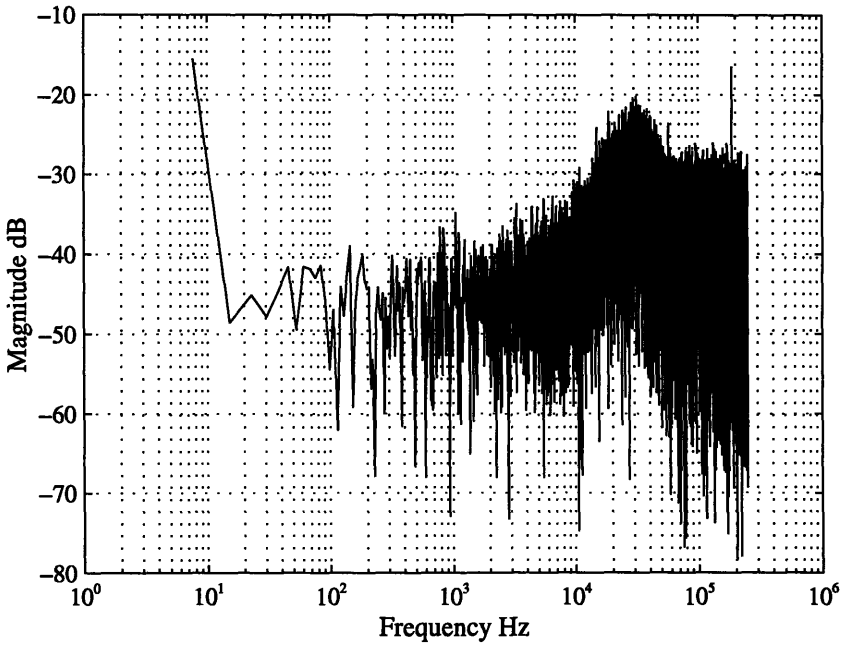
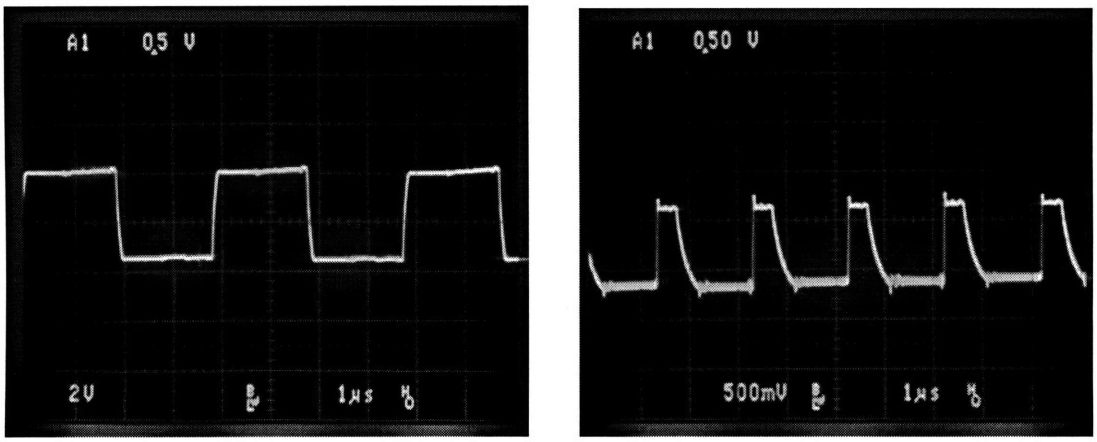


Figure 5.17 Third order modulator with inputs grounded

modulator spectrum was not quite as promising. Figure 5.17 shows a typical spectra taken from one of the third order modulators. Recall the third order modulator is used when the accelerometer is operating in its fifth order mode. The poor open loop performance of the third order Δ-Σ modulator is probably as a result of the placement of the complex pole pair of the modulator in close proximity to the unit circle. Recall from chapter three, the complex conjugate pole pair of the third order modulator was placed very close to the unit circle to reduce the low frequency negative phase shift in the forward transfer characteristic of the modulator. This was done in order that the main loop of the accelerometer would have maximum phase margin. Like the mechanical system, unstable open loop poles in the third order modulator does not indicate instability for the closed loop system.



a) Lead-Lag Output (before chop)

b) P+D Output (before chop)

Figure 5.18 Waveforms from the amplifiers in the lead-lag and P+C compensation stages

Figure 5.18 shows the output waveforms from the second amplifiers in the lead-lag compensation and P+D compensation circuits. Note these waveforms were measured coming out of the differential amplifiers but before the signal has been passed through the choppers placed at the output of the stage. Thus, the output from the lead-lag compensation is really "railed" and the output of the P+D compensation represents the chopped (and amplified) offset from the C-V stage.

Figure 5.19 shows the voltages applied to the upper electrode of the proof mass structure. Initially (going from left to right), Φ_2 is high and the electrode is differentially charged between $-V_1$ and $+V_2$ (see figure 4.17). Recall that during Φ_1, feedback is applied to the proof mass. During Φ_1 the first time, the electrode is grounded. The second time F1 goes high, the feedback voltage, V_{FB} (~634mV) is applied. V_{tune} is applied to the upper electrode the second time Φ_2 is active. During this time, the lower electrode is used for the differential sense.

5.3.2 Closed Loop Testing

As previously discussed, an ESD problem was encountered when the hybrid accelerometer circuit was stitch-bonded together which destroyed all but one of the hybrid sensors. More mechanical structures were not available for bonding due to the low yield (10%) of the micromechanical structure which was caused by the nonuniform etch problem.

The accelerometer was first tested in second order reset mode. The hybrid structure assumed stable operation in an open air environment with a 1.0g DC input acceleration (gravity). The output spectrum from the second order operation is shown in figure 5.20. Note the large amount of "white" noise which is present in the output spectrum. This is as a result of the Brownian noise from the heavily overdamped system. Also note the small signal "spike" at 120Hz. This is as a result of a microscope light which should have been powered off.

While the spectrum of figure 5.20 verifies the function of the second order reset loop, operation of the higher order modes was never tested. Unfortunately, while the data was being analyzed for the output spectrum shown in figure 5.20, the proof mass was

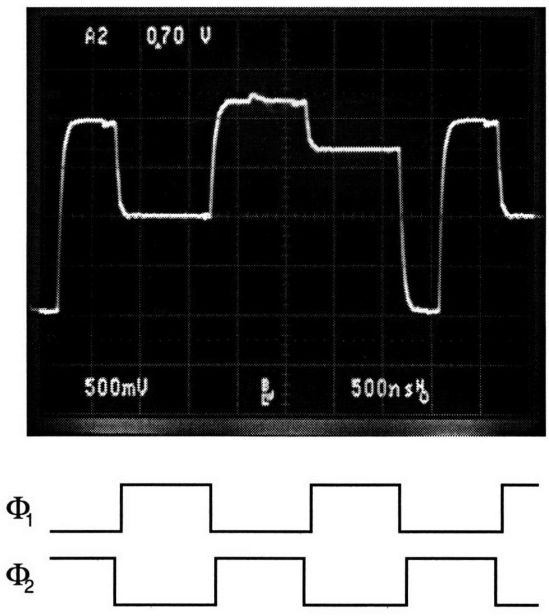


Figure 5.19 Voltage waveform applied to the fixed electrode above the proof mass

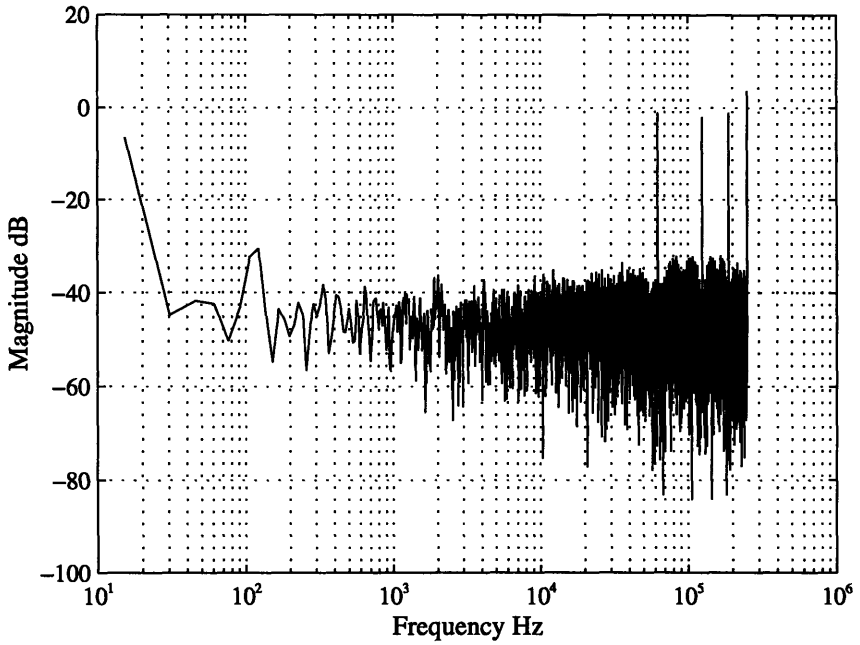


Figure 5.20 Output spectrum of second order accelerometer with 1.0g DC input

pulled-in to the upper fixed electrode where it fused. Because this was the only viable hybrid accelerometer, the testing of higher order operation as well as testing in a vacuum will have to be the focus of later research. Ongoing research is currently investigating the possibility of placing mechanical stops on the upper electrode to prevent fusion of the proof mass as occurred here.

CHAPTER 6

Conclusions

Throughout the course of any research, certain realizations come to light that can significantly affect the documented results. Ideally, all of this knowledge is obtained early enough in the chronology of the research such that the optimal theory may be developed and fully verified when the study has ended. More often than not, however, important ideas come to light continually and are built upon other ideas which have previously surfaced. There is no clear cutoff when these ideas should stop forming and only testing and documentation should take place. Thus, when a period of research has ended, some realizations are fully solidified while others are just beginning to form. Any or all of this information may be applicable to future research. It is for this reason that the thoughts and conclusions which are summarized from a piece of research form the most important part of its content.

In this chapter, the thoughts and conclusions which were taken from this research are presented. Ideas are presented for future research which were not investigated during the course of this research.

6.1 Conclusions

The conclusions are presented as they pertain to each component of the accelerometer including both the accelerometer controller IC and the micromechanical structure. Each significant noise source is re-examined and methods for reducing the associated errors are given.

6.1.1 Brownian Noise

Brownian noise was determined to be the source of error which set a fundamental limit on the resolution of the accelerometer. To increase the overall resolution of the accelerometer , the Brownian noise floor of the accelerometer must first be lowered. From equation 3.12, the input referred Brownian noise is inversely proportional to the size of the proof mass. Under the assumption that the total damping of the mechanical system cannot be reduced further once it has been placed in a vacuum[79], the size of the proof mass must be increased to lower the input referred Brownian noise and thereby increase the predicted resolution of the accelerometer.

6.1.2 Quantization Noise

After Brownian noise, quantization noise was estimated to be the next largest source of error in the accelerometer. In actuality, the quantization noise will be significantly lower than the value estimated in section 4.7 (0.34μg). Recall the gain of the two mechanical integrators was not incorporated into the quantization error calculation, only the noise rejection provided by the third order Δ-Σ modulator. Thus, the noise prediction is quite conservative.

If the additional quantization noise rejection provided by the mechanical system does not result in the desired quantization noise floor, then the quantization error can be

79. Recall the Brownian noise floor calculated in chapter 2 was only an estimate. The damping was calculated using a Q of 50,000 and the mechanical damping was estimated to have the same limiting effect on resolution as viscous damping. It is entirely possible that the Brownian noise estimate is off by an order of magnitude, either lower or higher than the predicted value (2.21μg). In either case, to reduce the noise floor further, the size of the proof mass must be increased.

reduced further by either increasing the order of the accelerometer (adding another electrical integrator) or increasing the sampling rate. Increasing the order of the modulator will make the closed loop system very difficult to stabilize and is therefore not a very attractive solution. However, using the current 1.2μm technology, the clock speed can be increased by a factor of two or three using an alternate clocking scheme[80]. After the clock rate has been maximized, the resolution of the accelerometer is technology limited.

6.1.3 The Capacitance Sensor

Two different capacitance sense schemes were presented. The first sense method employed fixed reference capacitors to generate a differential capacitance when compared with the variable capacitors above and below the proof mass. The second sense scheme used no reference capacitors at all, but instead implemented a fully differential capacitance sense between the upper and lower sense capacitors of the mechanical structure.

The second (fully differential) capacitive sense scheme is optimal for maximizing the resolution of the closed loop accelerometer. The capacitive sense scheme incorporating the reference capacitors was only used because of the large fabrication tolerances of the micromechanical structure. Under worst case conditions, these fabrication tolerances would cause instability if the fully differential capacitive sense scheme were used. Since the reference capacitor scheme balances the proof mass to the same (proportional) deflection as the reference structure, the upper and lower capacitors are not equal in value when mechanical offsets are present. Due to this, the incremental dynamics of the mechanical structure will be skewed which results in a much larger input referred thermal noise from the C-V sensor as well as increased harmonic distortion. Alternatively, if the second sense scheme could be used, the top and bottom capacitors would stabilize to the same value and thereby preserve the incremental dynamics of the mechanical system.

In order to use the second capacitance sense scheme with the current mechanical structure, one of two things must be done. Either the tolerances of the mechanical struc-

80. An improved clocking scheme for the accelerometer is presented in section 6.2.1 which would enable a faster clocking rate without increasing the speed requirements placed on the circuitry.

ture must be tightened or a calibration method must be developed which cancels the acceleration offset resulting from processing variations in the mechanical structure. To lower the effective offset acceleration resulting from errors in the mechanical structure, a larger proof mass should be used. This would, in effect, reduce the input referred offset acceleration. Developing an offset calibration method is a possible focus for future research.

6.1.4 The Mechanical Structure

The mechanical structure should be optimized to minimize offset in the proof mass deflection and separate the secondary resonances of the structure from its fundamental resonance. As previously stated, the offset in the position of the proof mass greatly limits the usability of the optimal capacitance sense scheme. A larger proof mass would be very effective in overcoming the fabrication tolerances of the mechanical structure. For this particular accelerometer, if the thickness of the proof mass were increased by a factor of 4, the overall resolution of the sensor would be increased to 0.55μg, the second capacitance sense method could be used, and the dynamic range of the accelerometer would be guaranteed to be at least ±0.95g under worst case conditions. Because of Brownian noise and the usability of the second capacitive sense scheme, there is a limitation on how small the proof mass can be sized and still attain a specified resolution.

Mechanical stops should be investigated for the proof mass to prevent electrical contact and fusion between the proof mass and the upper and lower fixed electrodes. Since the nonlinearity of the mechanical spring constant is reduced by the open loop gain of the complete system, the design focus of the mechanical structure should be moved away from using long silicon tethers for high linearity. The focus should concentrate on further separating the fundamental resonance mode from the secondary modes of the structure. A mechanical structure is presented in section 6.2.3 which could possibly be used to electrically separate the fundamental resonance frequency from secondary resonance modes.

6.1.5 System Topology

The basic closed loop architecture used for this accelerometer is optimal. As previously stated, the fully differential capacitance sense scheme should be used if at all possible. One possible improvement in the front end architecture would be to partially incorporate the C-V sensor directly into the lead-lag compensation[81].

When using this basic topology, the number of electrical integrators should be chosen by assessing the desired resolution of the accelerometer and the speed capabilities of the technology selected to implement the switched capacitor control circuitry. If the quantization noise is too large with only one electrical integrator and the sampling rate is as high as possible, another electrical integrator should be added to the loop. This increases the order of the system and thereby reduces the low frequency quantization noise. This should be repeated until the desired resolution is achieved.

6.1.6 Nonlinearities

Assessing the effect of different nonlinearities in the accelerometer, it is important to determine the location of the nonlinearities within the closed loop system. If a nonlinearity is present in the forward path of the loop, the effect of the nonlinearity at the output is decreased by the open loop gain of the system. If, however, the nonlinearity is located in the feedback path, its effect is seen directly at the output and there is no rejection from the loop gain.

The mechanical system has two associated nonlinearities, the nonlinearity of the mechanical spring and the nonlinearity in viscous damping. Since the mechanical system is part of the forward gain of the accelerometer, both the spring nonlinearity and damping nonlinearity are reduced by the loop gain.

A nonlinearity exists in the position-to-capacitance (Δx-to-ΔC) conversion which takes place in the C-V sensor. Like the nonlinearities of the mechanical system, the posi-

81. This would further reduce the input referred circuit (thermal) noise as well as the total power dissipation of the accelerometer. The C-V sensor should also be incorporated into the Proportional-plus-Derivative compensation to implement the second order reset loop.

tion sense nonlinearity is located within the forward path of the closed loop system and is therefore reduced by the large open loop gain.

The last two major nonlinearities are due to the positional dependence of the electrostatic forces placed on the proof mass. One such nonlinearity occurs due to the application of the electrostatic restoring force which rebalances the proof mass at its equilibrium position. The other results from the voltages applied during the capacitive position sense. Though the same mechanism causes both of these nonlinearities, their effect at the output of the accelerometer is entirely different. The nonlinearity in the applied feedback force is clearly in the feedback path of the accelerometer and thus shows up directly at the output of the system as harmonic distortion. In contrast, the nonlinearity caused by the capacitance sense is not part of the feedback path and can be grouped with the other nonlinearities of the mechanical system.

A quick and easy test to determine whether a nonlinearity is in the forward path of the loop is to remove the feedback path from the system. The nonlinearities which remain are part of the forward loop. In other words, if the nonlinearity is independent of the output from the accelerometer, then it is located in the forward path of the system. Using this approach, the nonlinearity which results from the capacitance sense is still present when the loop is "opened". In contrast, the nonlinearity from the applied feedback force has been removed by "opening" the loop.

6.2 Suggestions for Future Research

The obvious first goal for future research is the full monolithic integration of the micromechanical sensor and control circuitry for the accelerometer. Along with full integration, there are several other possible steps which could be taken which may improve the performance of the accelerometer. This section discusses the (not aforementioned) possible improvements.

6.2.1 Clocking

In the clocking scheme of the accelerometer[82], Φ_1 and Φ_2 are nonoverlapping clocks. On Φ_1, the electrostatic feedback force is applied via the fixed electrodes placed above and below the proof mass. During this time, there is no amplifier in the entire circuit which is settling[83]. In contrast, during Φ_2, not only must the amplifiers of the C-V sensor and compensation networks settle twice, but when the amplifiers settle the second time (during Φ_4), they must settle in series.

Currently, Φ_1 and Φ_2 split a full clock cycle evenly, each being high just under half the time. If on the other hand, the duty cycle of Φ_1 were shortened to a third or a quarter of the cycle time, then more time could be allocated for settling during Φ_2. Using this asymmetric clocking scheme[84], the sampling rate of the accelerometer could be easily increased by a factor of two in order to increase the oversampling rate of the system. Note that the feedback voltage would have to be increased to account for the shorter duty cycle of Φ_1.

6.2.2 Op Amp Design

A couple of steps can be taken which would greatly reduce the power dissipation of the accelerometer control circuitry. First, recall that the differential amplifiers of the Δ-Σ modulator are identical to the differential amplifiers used elsewhere in the circuit except the Δ-Σ amplifiers are biased with two-thirds the current. Thus, the unity gain bandwidth of the amplifiers in the modulator is approximately 20% less than the unity gain bandwidth of the amplifiers in the C-V sensor and compensation networks. Since the amplifiers in the Δ-Σ modulator have approximately twice the settling time as the other amplifiers and none of the amplifiers in the Δ-Σ modulator ever have to settle in series, the bandwidth requirements for the amplifiers in the Δ-Σ modulator is only about an eighth of that required by the remaining amplifiers. Thus, the amplifiers of the Δ-Σ modulator should

82. See figure 5.2.

83. The differential amplifiers in the Δ-Σ modulator are charging capacitors at their outputs however no settling is taking place.

84. Φ_2 was however split with an asymmetric clock to form Φ_3 and Φ_4. Φ_4 is high longer than Φ_3 to allow more time for the amplifiers to settle in series.

only require about 2% of the power required by the faster amplifiers. This alone would reduce the total power dissipation of the accelerometer controller chip by over 20%.

Because the resolution of the accelerometer is not limited by thermal noise from the C-V sensor, the noise floor from the amplifiers can be increased significantly without changing the overall resolution of the accelerometer. Recall the input referred noise floor from the C-V sensor and lead-lag circuitry was calculated to be only 99.3ng. The thermal noise from the first two stages can be increased by an order of magnitude without increasing the 2.2μg noise floor of the accelerometer by more than 20%. To maintain the same speed for the amplifiers while the power dissipation is reduced, the load capacitance of the amplifiers must be decreased. Thus, as the power dissipation is reduced to lower and lower values, a practical limit is reached due to capacitance matching issues. It is safe to assume that the total power dissipation of the controller chip could easily be decreased from just under 300mW to less than 75mW.

6.2.3 Second Order Resonances

The problem with second order resonances never came into play in the hybrid accelerometer that was built and tested because a vacuum test was not preformed. The mechanical structure was heavily overdamped which prevented excitation of the secondary resonance modes. If the structure had been placed in a vacuum however, problems due to underdamped secondary modes could have easily surfaced.

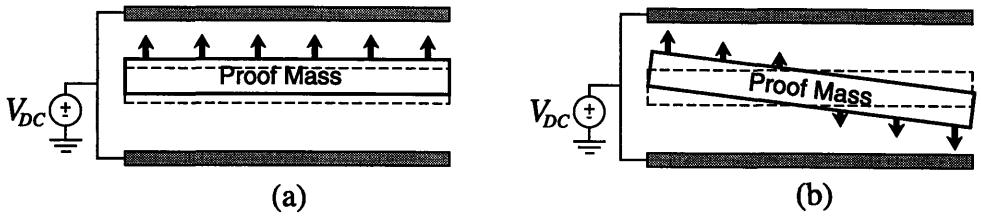


Figure 6.1 Electrical Resonance Tuning Revisited

The basic idea behind the electromechanical resonance tuning which was used to place the poles of the mechanical is revisited in figure 6.1a. If both the upper and lower electrodes are charged to the same voltage and the proof mass is perfectly centered, no net force is applied to the proof mass. However, once the proof mass moves away from its center position, a net force is applied in the direction of the deflection. It is this positionally dependent force which is modelled as a negative spring constant, to first order. Ideally, when this resonance tuning is used to bring the poles of the fundamental resonance mode to low frequencies, the poles of the secondary resonance mode would be unaffected and thus the resonant frequencies of the fundamental and secondary modes would be further separated by electrical resonance tuning. This, unfortunately, is not the case. Figure 6.1b illustrates how the same effect which lowers the fundamental resonance mode acts to lower the secondary resonance modes as well.

When there is no rotation of the proof mass, there is no net torque applied by the DC voltages. If, however, the proof mass is rotated slightly, one end of the proof mass is closer to the upper electrode and one is closer to the lower electrode. As a result, a net torque is applied. This rotationally dependent torque acts to lower the resonant frequency of the secondary resonant mode in the same fashion as the fundamental resonance was reduced. A possible solution to this problem is shown in figure 6.2.

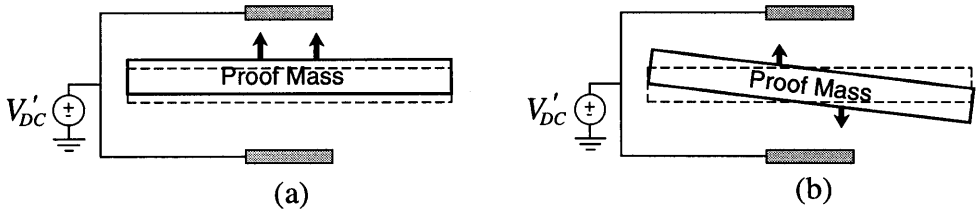


Figure 6.2 Separating the Fundamental and Secondary Resonances

If, instead of using the previous mechanical structure, much smaller fixed electrodes are centered above the proof mass, its possible that the fundamental frequency could be electrically separated from the secondary resonances. The fundamental fre-

quency is reduced in the same fashion as before (Figure 6.2a). Larger voltages are of course necessary to achieve the same applied electrostatic force. In contrast, the positionally dependent torque which is applied to the proof mass is greatly reduced with this structure because the effective "lever arm" has been greatly reduced. Thus, although the secondary resonance is still lowered by the electrical tuning, the secondary resonances should be less affected by this alternate mechanical structure. In effect, the fundamental and secondary resonance modes would be electrically split. Note this analysis ignores fringing effects in the electric field lines which would reduce the benefits of this structure. This would need to be taken into account in a detailed analysis before this method is used.

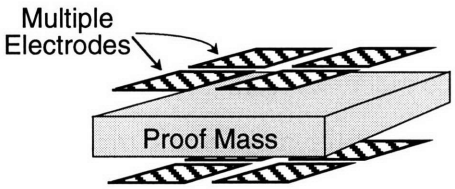


Figure 6.3 Four Quadrant Sensing

A method of avoiding the problem of secondary resonances was presented in reference 22. Four separate sense capacitors are formed by splitting the fixed electrodes placed above and below the proof mass as diagrammed in figure 6.3. Using the four sense capacitors, four separate Δ-Σ loops are implemented. This stabilizes the proof mass for both normal and angular acceleration modes.

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