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A SCENARIO OF PLANNING AND DEBUGGING
IN ELECTRONIC CIRCUIT DESIGN

by

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Abstract

The purpose of this short document is to exhibit how a HACKER-like top-down planning and debugging system can be applied to the problem of the design and debugging of simple analog electronic circuits. I believe, and I hope to establish, that this kind of processing goes on at all levels of the problem-solving process--from specific, concrete applications, like Electronic Design, through abstract piecing together and debugging of problem-solving strategies.

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Working Papers are informal papers intended for internal use.

A Scenario of Planning and Debugging in Electronic Circuit Design

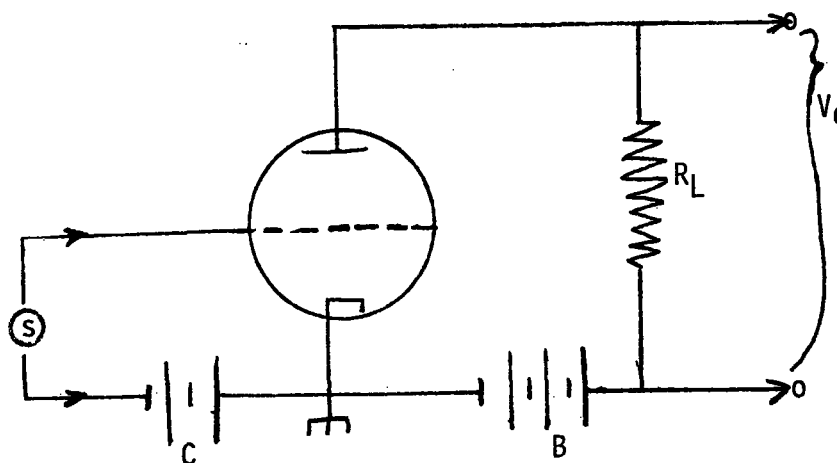
The purpose of this short document is to exhibit how a HACKER-like top-down planning and debugging system can be applied to the problem of the design and debugging of simple analog electronic circuits. I believe, and I hope to establish, that this kind of processing goes on at all levels of the problem-solving process--from specific, concrete applications, like Electronic Design, through abstract piecing together and debugging of problem-solving strategies.

The essence of the theory is that the problem-solver starts out with a set of basic modules which are solutions to various basic problems. Each module is indexed by some coarse description of the problem it is intended to solve. There may be several modules which are solutions to the same coarsely described problem. The choice of which to use in any case constitutes a design decision and must be based upon a finer description of the module, how it interacts with a finer description of the problem which it is to solve and other modules which it must interact with in solution of the problem of which it is a solution of a subproblem. When confronted by a problem, the problem-solver must first see if it has an immediate coarse solution to try out. If not, it must concoct one by breaking up the problem into subproblems and patching together the subsolutions. The proposed solution is then tried out and debugged. Debugging consists of isolating the cause of failure to one submodule or a particular sort of interaction between the submodules.

The affected region of the solution is then examined in finer detail and a subproblem is generated to patch the bug. The problem solver can be caused to acquire skill by saving the problem solutions it generates, coarsely indexing them by generalizations of the problems for which they were constructed.

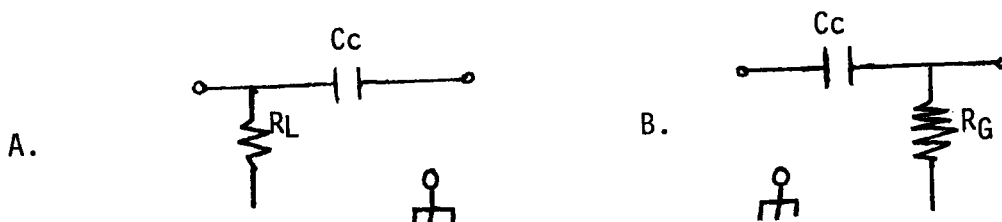
In this scenario the following modules are used:

I Class A amplifier: (tube type)



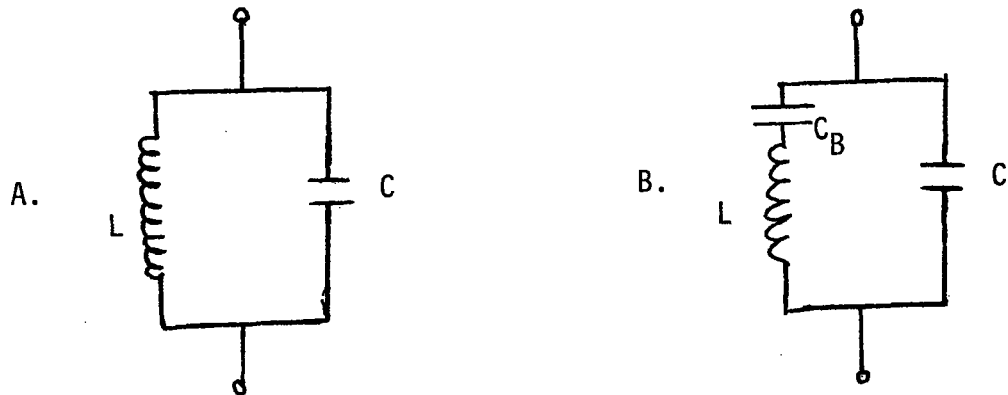
It is specified that the signal source, S , is pure A.C. and (to first order) sees an infinite impedance. The output voltage, V_o , has a D.C. bias caused by the battery, B .

II The "RC coupling" trick. To pass the AC component of a signal without coupling the DC bias circuits:

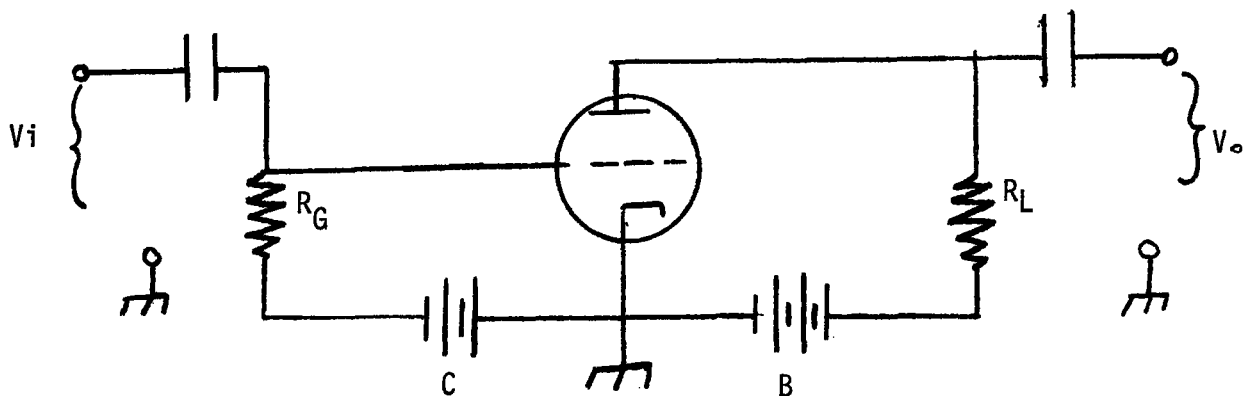


We want C_c to have a small impedance at the signal frequency and have a large impedance to DC; R_i , R_g to have large impedances at the signal frequency and small impedances to D.C. (R_g may be large.)

III The "Tank" circuit--Infinite impedance at one frequency, zero at all others.

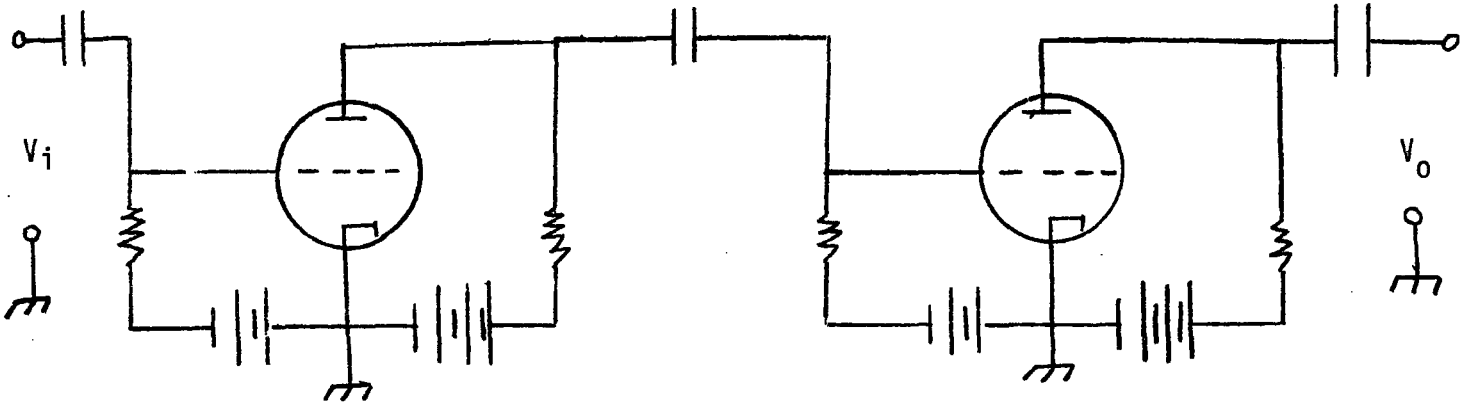


Circuit B has infinite impedance at DC as well as at resonance-- $C_b \gg C$. Certainly with modules I and II we could produce an untuned amplifier which amplifies the AC component of a signal, ignoring the DC component. This circuit works O.K.

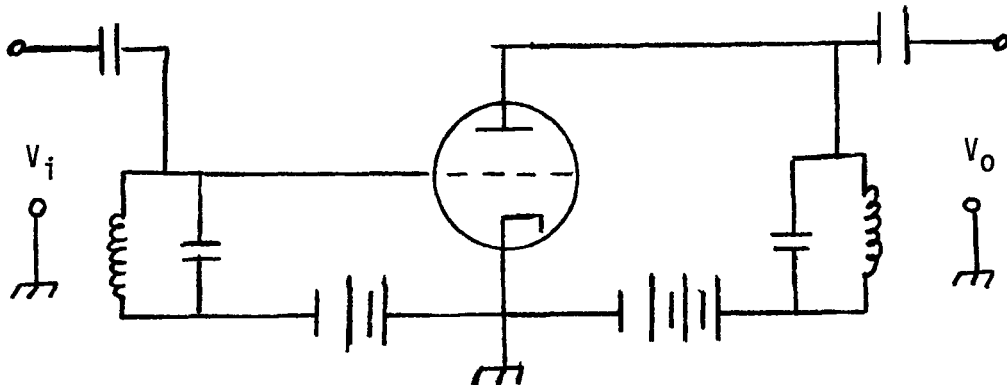


$V_o = \text{gain} \times V_i$ for AC voltages V_i , V_o (above some frequency determined by the component values. And within some maximum amplitude.)

The gain is also determined by the component values. If we need more gain than can be feasibly obtained with one stage we can surely "cascade" stages:

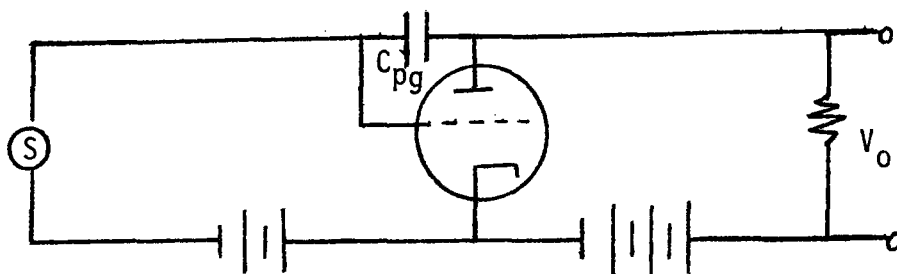


Suppose, however, we want to build a tuned amplifier-- one that amplifies at only one frequency. Surely we can replace our R_g , R_l with tank circuits which will short to ground all frequencies except the desired one. Type A provides a good DC path as well:



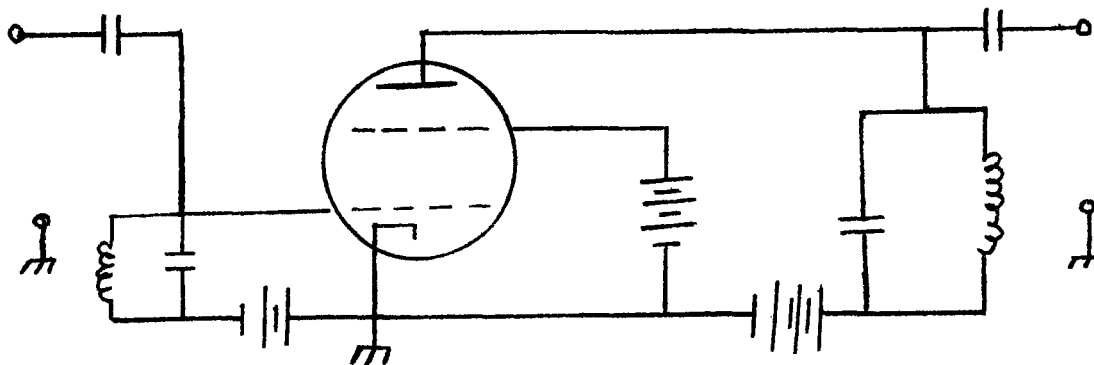
This works well enough up to some frequency like 1MHz. Above that frequency the circuit oscillates rather than amplifies. We have a "bug". Why does the circuit oscillate? In planning we used a coarse description of module I, the basic amplifier; we ignored such effects as inter

electrode capacitance. In more detail, the tube looks like:



C_{pg} is very small, say 1 - 10 pf, so it has little effect at low frequencies, but at high frequencies there is feedback through C_{pg} which causes the spurious oscillation.

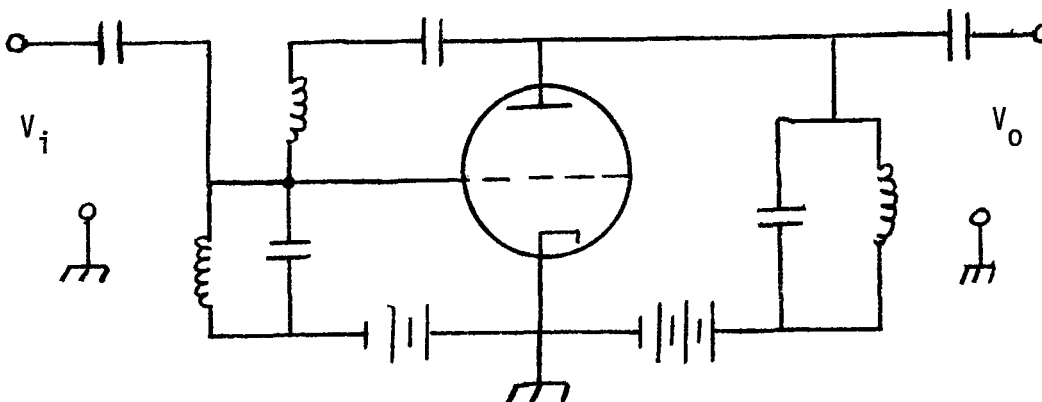
How can we correct the bug? We can try two possibilities--remove C_{pg} or cancel C_{pg} . We can remove C_{pg} by substituting a tetrode for a triode (not always the best choice because a tetrode has a higher noise figure and the bias circuitry becomes more complex). A tetrode is a tube which has a Faraday shield between the control grid and plate:



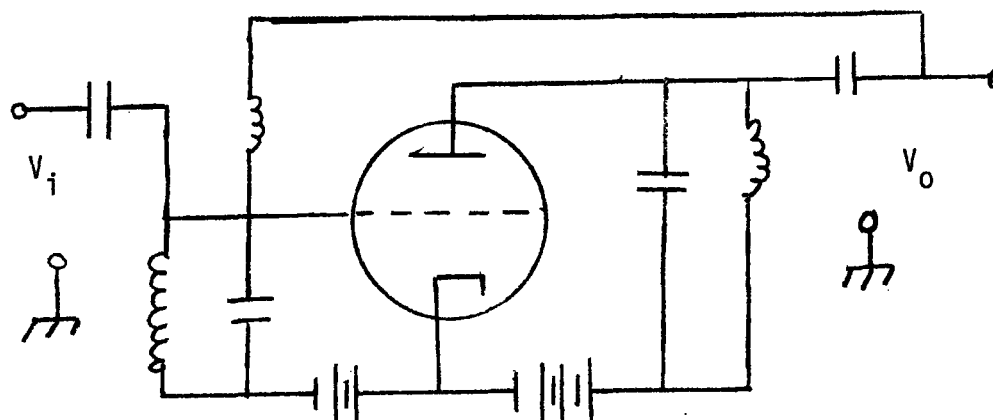
This is one possible answer which works. We haven't considered the problems of replacing all of the bias supplies by a bias network and one supply.

We can also try to cancel C_{pg} . We can always make the impedance across a capacitor infinite (open the capacitor) at one frequency by

bypassing it with an inductor at that frequency (using our tank circuit idea). Furthermore, we can prevent shorting out our power supply through the inductor by using a D.C. blocking capacitor as in circuit II B. This new circuit is called a "neutralized tuned amplifier":



If we want to be clever, we can even "bum out" the plate blocking capacitor on another pass:



This circuit is used extensively (with an appropriate D.C. bias network superimposed) as a linear RF amplifier.