Improving Mechanical Reliability of Integrated Circuits

by

LAN H. HOANG

B.S., Materials Science & Engineering, Massachusetts Institute of Technology,
Cambridge, MA (1995)

Submitted to the Department of
Materials Science and Engineering
in Partial Fulfillment of the Requirements for the
Degree of

Master of Science
in
Materials Science and Engineering
at the
Massachusetts Institute of Technology

February 1996

© 1996 Lan H. Hoang
All rights reserved

The author hereby grants to MIT permission to reproduce and to distribute publicly paper
and electronic copies of this thesis document in whole or in part.

Signature of Author_____
Department of Materials Science and Engineering
January 19, 1996

Certified by_____
Frederick J. McGarry
Professor of Polymer Engineering
Thesis Supervisor

Accepted by_____
Michael F. Rubner
TDK Professor of Materials Science and Engineering
Chair, Departmental Committee on Graduate Students

MASSACHUSETTS INSTITUTE
OF TECHNOLOGY

MAR 26 1996

Science

LIBRARIES

IMPROVING MECHANICAL RELIABILITY OF INTEGRATED CIRCUITS

by

LAN H. HOANG

Submitted to the Department of Materials Science and Engineering on January 19, 1996 in partial fulfillment of the requirements for the Degree of Master of Science in Materials Science and Engineering

Abstract

Two concepts were explored to improve the mechanical reliability of silicon integrated circuits in plastic packaging. A low stress liquid epoxy was placed on the top surface of test devices to reduce interlayer dielectric cracking. We found that a low cost, high stress molding compound in combination with the low stress glob top yields over 75% less failure over the standard process where no stress buffer was used. When the glob top was allowed to spread from the silicon to the supporting copper pad, large amounts of wire breaks were observed.

We used an electroless plating process to improve the interconnection reliability between the aluminum bond pads on silicon devices and gold wires to form an electrical path to the outside of the package. The second concept focused on improving the interconnection between the gold bond wires and the aluminum bond pads. An electroless plating process was used to form a barrier nickel layer on top of standard aluminum bond pads. On average, the shear strength of the gold wire / nickel cap interface was 15% higher than gold wire / aluminum bond pad interface after temperature storage between 175 to 300 °C at different time points. Micrographs showed no detectable intermetallics with the nickel cap at 200 °C for 168 hours. For the same condition, aluminum was consumed by the gold wire bond in standard interconnects. The nickel cap protects the aluminum bond pads against common chemical attacks, however, it is not resistant to steam at 121 °C in 2 atm pressure.

Thesis Supervisor: Professor F. J. McGarry

Title: Professor of Polymer Engineering

Table of Contents

Abstract 2

Table of Contents 3

List of Figures 5

List of Tables 10

Acknowledgments 11

Introduction 12

1.1. Background 12

1.2. Current Reliability Issues 14

1.2.1. Stress 14

1.2.1.1. Passivation and Interlayer Dielectric Cracking 16

1.2.1.2. Bond Wires Integrity 18

1.2.2. Intermetallics 19

1.2.3. Corrosion 20

1.2.4. Environmental Conditions 21

1.2.4.1. Moisture Absorption 21

1.2.4.2. Delamination 22

1.2.4.3. Popcorn Cracking 24

1.2.5. Current Solutions 25

1.2.5.1. Stress Buffers 25

1.2.5.2. Design Rules 26

1.2.5.3. Moisture Barrier Dry Packing 26

1.2.5.4. Hermetically Sealed Package 27

1.2.5.5. Molding Compound 27

1.3. Standard Reliability Testing 27

1.3.1. Preconditioning 28

1.3.2. Environmental Tests 29

1.4. Objective of Research 30

1.4.1 Glob Tops for Stress Reduction 30

1.4.2 Electroless Plated Caps for Improved Bond Pad Reliability 31

Glob Tops Results 33

2.1. Introduction 33

2.2. Experimental Proceedures 33

2.2.1. Test Vehicles 34

2.2.1.1. Test Chip A 36

2.2.1.2. Test Chip B 38

2.2.1.3. Test Chip C 39

2.2.2. Automated Dispenser 39

2.2.3. Environmental Testing 40

2.3. Results 41

2.3.1. Test Chip A 41

2.3.1.1. Wire breaks 41

2.3.1.2. Interlayer Dielectric Cracking 44

2.3.2. Test Chip B 49

2.3.3. Test Chip C 52

2.4. Discussions 53

2.4.1. Gross Wire Failures 54

2.4.2. Stress Concentrations 55

2.4.3. Glob positioning 56

2.4.4. Globbing materials 56

2.4.5. Cure Temperature 58

2.4.6. Molding Compound 59

2.4.7. High Temperature Storage 59

2.5. Summary 60

Electroless Capping Results *62*

3.1. Introduction 62

3.2. Background 62

3.2.1. Activation 63

3.2.2. Plating Baths 63

3.2.3. Plating Mechanisms 64

3.3. Experimental Procedures 65

3.3.1. Capping Structure and Metallurgy 66

3.3.2. Environmental Tests 67

3.3.3. Analytical Techniques 68

3.4. Results 69

3.4.1. Bond Pad Structure Evaluations 70

3.4.1.1. Standard Nickel Capped Bond Pad 70

3.4.1.2. Activation Issues 72

3.4.1.3. Corrosion 75

3.4.1.4. High Temperature Storage 78

3.4.2. Mechanical Testing 79

3.4.2.1. Wire Pull Test 80

3.4.2.2. Bond Shear 81

3.4.3. Electrical Testing 84

3.5. Discussions 86

3.5.1. Plating Uniformity 86

3.5.2. High Temperature Resistance 87

3.5.2.1. Diffusion Rates 88

3.5.2.2. Aluminum-Nickel Intermetallics 88

3.5.2.3. Time and Temperature Dependence 88

3.5.3. Corrosion 89

3.6. Summary 89

Conclusion and Recommendations *91*

4.1. Introduction 91

4.2. Glob Top 91

4.3. Electroless Cap 92

4.4. Summary 93

Appendix A: *Typical Assembly Process Flow* *94*

Appendix B: *Asymtek 402 Fluid Move Gantry System* *95*

Appendix C: *Preconditioning Sequence for Test Chips A, B, and C in the Glob Top Evaluations.* *96*

Bibliography *97*

Biographical Note *99*

List of Figures

Figure 1.1: Cross-section view of a typical electronic packaging showing the different components. Common industry jargon is shown in italics. 13

Figure 1.2: Four different types of interlayer dielectric cracking is captured. (A): Cross-sectional schematic. (B): Surface of the integrated circuit revealing cracks with dye staining methods.[17] 17

Figure 1.3: Shear stress distribution across surface of die as calculated with FEA techniques.[10] 18

Figure 1.4: Maximum principal stresses for (a) ball bond with plastic-to-die delamination and (b) no delamination. Stresses are reported in psi. (Source: Moore and McKenna) 19

Figure 1.5: Concept of moisture diffusion model. (a) cross-section of a typical plastic package. (b) From left to right, moisture diffusion curves for absorption, drying, and solder reflow simulation.[8] 23

Figure 1.6: Stresses calculated in IC package using FEA with 300 psi load between the DAP and the molding compound.[10] 24

Figure 1.7: Crack is shown extending from bottom corner of the die attach pad to the outside of the package. Most cracks are initiated at the corners where the stress concentration is greatest. 25

Figure 2.1: Cross-section of the typical interlayer dielectric above the surface of the silicon. The electrical test detects a crack in the D2 layer by measuring the resistance between M1 and M2 aluminum metal traces.[18] 35

Figure 2.2: Layout of Test Chip A reveals the aluminum metal grids located at the corner of the die. Our test used a 2x2 array to obtain a larger die size. Starting from the top left quadrant, moving in a clockwise direction, we see the 8, 4, 1, and 2 mils aluminum line width in the horizontal direction.[18] 37

Figure 2.3: A section layout of a Test Chip B corner shows the pad locations and a typical crack propagating at the corner denoted by the A marker. The top left bond pad connects to ground, while the other pads are surrounded by diodes.[18] 38

Figure 2.4: A typical schematic showing how a dome can be achieved by the dispensed liquid encapsulant impinging on the top surface of the die. The viscosity of the liquid greatly determines the size and shape of the dome.[5] 40

Figure 2.5: An X-ray photograph showing some of the effects of a typical glob top applied to the die only. A slight amount of wire shift can be observed due to the flow pattern of the molding compound. The top of the die reveals that most of the connections to the leadframe have been broken. 42

Figure 2.6: A photograph showing X-ray of a glob top applied to the die and DAP. Note that the wires are kept straight where they are encapsulated by the glob. Wire bending observed at the interface between the molding compound and glob top suggests that the wire damage occurred after the globbing process. 42

Figure 2.7: The X-ray illustrates a few rare cases of severe damage of the wire which is likely to be from the assembly mishandling of the parts. This is one of the control leg without glob top. 43

Figure 2.8: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after preconditioning. Only a few failures are detected. 45

Figure 2.9: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after 500 temperature cycles. This figure indicates a significant increase in failures of the 200 μm wide metal lines. 46

Figure 2.10: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after 1000 temperature cycles. The figure indicates significant failures in each metal trace widths. More failures are generally observed at the corners. 46

Figure 2.11: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob A is dispensed on die alone. Only a few failures are detected after 1000 temperature cycles in the 200 μm quadrant. 47

Figure 2.12: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob A is dispensed on the die and allowed to overflow on the DAP. Only a few failures are detected after 1000 temperature cycles in the 200 μm line width region. 47

Figure 2.13: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob B is dispensed on the die only. No failures are detected even after 1000 temperature cycles. 48

Figure 2.14: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob B is dispensed on the die and DAP. Significant failures are observed in the 200 μm metal width regime. 48

Figure 2.15: The percentage of open failures is indicated for different combinations of glob top materials and molding compounds under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 °C to 150 °C, Precon-85°C/85%RH @168 hrs, 245 °C reflow) 50

Figure 2.16: The percentage of electrical shorts is indicated for different combinations of glob top materials and molding compounds under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 °C to 150 °C, Precon-85°C/85%RH @168 hrs, 245 °C reflow) 50

Figure 2.17: The percentage of open failures is indicated for different combinations of glob top locations and curing temperatures under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 °C to 150 °C, Precon-85°C/85%RH @168 hrs, 245 °C reflow) 51

Figure 2.18: The percentage of electrical shorts is indicated for different combinations of glob top locations and curing temperatures under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 °C to 150 °C, Precon-85°C/85%RH @168 hrs, 245 °C reflow) 52

Figure 2.19: Open failure is observed with Test Chip C for different molding compounds and glob top positionings. (TMCL-temperature cycling from -65 °C to 150 °C, Precon-85°C/30%RH @48 hrs, 245 °C reflow) 53

Figure 3.1: Actual cross-section of a 10 μm nickel cap on aluminum bond pad. A gold wire bond is situated on top of the pad. 66

Figure 3.2: Schematic of a gold wire bond on aluminum bond pad with respect to the shearing tool. The different components of the gold wire are identified in the illustration. In the case of the wire pull, most of the breaks occur at the shoulder of the bonded ball. 69

Figure 3.3: Cross-section of a typical bond pad showing the electroless nickel and immersion gold serving as a cap to protect the aluminum underneath. 71

Figure 3.4: Topography of nickel/gold surface. The physical features of the nickel and gold follow that of the aluminum bond surface. The small bumps are contributed by the Cu nodules in the aluminum. 71

Figure 3.5: Top surface of an aluminum bond pad shows that the aluminum is almost completely etched out by the zincate. The residual zinc is left on top of silicon after the aluminum is etched. 73

Figure 3.6: Cross-section micrograph confirms that the aluminum not protected by the passivation is etched away in the zincating solution. 73

Figure 3.7: Non-uniformity of Al-2%Cu bond pads are indicated following the zincate process. Each pad connects to different metallurgy in the silicon. 74

Figure 3.8: Pads plated to approximately 6 μm do not show drastic variations from one bond pad to the next. 75

Figure 3.9: Aluminum bond pads subjected to 5 minutes of concentrated HCl dip and 1 month of air time. The underlying oxide structure is exposed where the aluminum is etched. 76

Figure 3.10: Nickel/Gold cap improves resistance to chemical attacks. Marker A indicates the corrosion at the corner. These devices were placed in concentreated HCl for 5 minutes and in air for 1 month. 76

Figure 3.11: When placed in 121 °C at 2atm pressure for 24 hours, the Au wire bond and Ni cap lift off from the aluminum bond pad. Failure occured between the aluminum and nickel interface. An epoxy based potting material was used to keep the wires in place for cross-sectioning. 77

Figure 3.12: The right side shows an unsheared 28 μm bump. The left side shows the Ni fracture surface left as a result of the bump shear. Note that the Ni to Al adhesion is stronger than the bulk fracture strength of the electroless nickel. 78

Figure 3.13: Al/Au intermetallics are present in the bond pad without a nickel barrier metal. All of the aluminum seems to be consumed where it is in contact with the gold wire bond. This sample was exposed to 200 °C for 350 hours. 79

Figure 3.14: Data published by G. Harman showing the degradation of ball shear force as a function of time in 200 °C atmosphere. Note the change of scale from shear force (left) to pull force (right). (Sourc: Harman et al) 80

Figure 3.15: Shear force measured at room temperature after 175 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). The shear strength of mid-phosphorous Ni cap is slightly higher than the others at the 1000 hour time point. _____ *82*

Figure 3.16: Shear force measured at room temperature after 225 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 225 °C shows a sharp increase in the mid phos Ni cap after almost 1000 hours of heat treatment. _____ *83*

Figure 3.17: Shear force measured at room temperature after 250 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 250 °C shows an increase in the Ni capped units while the standard Al bond pad exhibits a drop in shear strength after 48 hours. 83

Figure 3.18: Shear force measured at room temperature after 300 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 300 °C does not distinguish between the different variables. Shear strength increases sharply after 4 hours. _____ *84*

List of Tables

Table 1.1 Mechanical properties of materials used in microelectronic packaging[10]. _____ *15*

Table 2.1: Comparison of die, DAP, and package dimensions as measured in mm. _____ *36*

Table 2.2: The table below indicates the percent of devices with gross wire breaks detectable visually by X-rays. Two globs are applied to either the die alone or on the die and DAP. _____ *43*

*Table 2.3: Comparison of mechanical properties is made between Glob A and Glob B liquid encapsulant. *The stress index is calculated by using the relationship given in equation 1.1.* _____ *57*

Table 3.1: Some typical contents of electroless plating baths and its purposes.[19] _____ *64*

Table 3.2: Process used by an outside source to plate electroless nickel with flash of gold. Deposition rate is provided where applicable. _____ *67*

Table 3.3: Summary of parameters that correspond to different environmental tests used in evaluating reliability performance of Ni capped bond pads. _____ *68*

Table 3.4: Bond pull result shows the percentage of bonds that failed at the bonding interface instead of at the wire. The average strength is given, corresponding to the bond failures. An average force of 10.5 grams was required to break the gold wires. _____ *81*

Table 3.5: Electrical Testing data are summarized below. The degree of failure is simplified by a 0 to 4 code (0 = no failures, 4 = gross failures). Failure is indicated for the standard aluminum bond pads and the nickel capped bond pads at various conditions. _____ *85*

Acknowledgments

First and foremost, I would like to take this opportunity to thank God who gave His one and only Son, that whoever believes in him shall not perish but have eternal life (John 3:16). He is the source of my strength through these years at MIT. Apart from Him, I can do nothing.

I would like to thank my academic and professional mentors, Professor Frederick McGarry and Peter M. Weiler for the research opportunities through the years. They have helped me develop through constant support and encouragement. A special thanks goes out to the Packaging Technology Group at the National Semiconductor Corporation for the resources to make this research possible.

Last, but definitely not least, I thank my parents for their enduring love and support. I would also like to acknowledge Cindy, who continues to encourage me.

Chapter 1

Introduction

1.1. Background

Technology is becoming more advanced, increasing the need for moving and storing information effectively. The drive for processing information at a faster rate demands more processing devices on microchips that are rapidly decreasing in size. At the same time, the encapsulation to silicon substrate size aspect ratio must decrease to increase the mounting density on standard PC boards. However, the device protection is compromised when the encapsulation or package becomes too thin. As the dimensions of the silicon substrate approach that of the plastic package, several reliability issues are considered in the assembly and operating environment.

In addition, the industry is finding ways to lower the manufacturing cost. Although some high end products such as microprocessors are still packaged in hermetically sealed ceramic, most high volume products are in plastic packages. Further reliability issues such as stress and corrosion must be considered with the use of plastic packages.

In understanding the reliability issues surrounding plastic packaging, it helps to visualize the package construction. Figure 1.1 shows a cross-section of a typical plastic package, revealing the industry jargon for different components.

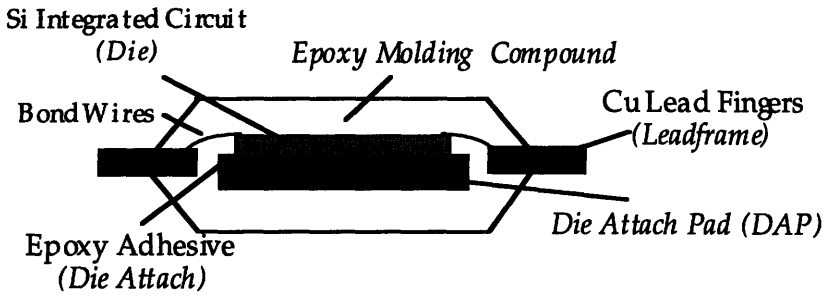


Figure 1.1: Cross-section view of a typical electronic packaging showing the different components. Common industry jargon is shown in italics.

Mounting these chips on top of a circuit board during assembly requires a furnace temperature of approximately 220 °C to reflow the tin-lead solder. The reflow process refers to the melting of solder paste on printed circuit boards to form solder joints with the lead fingers. Large changes in temperature induce residual stresses between the plastic package and the silicon device or die, resulting in electrical failures[1].

Vapor pressure can rupture the package allowing a direct path for the ambient moisture to enter, corroding the exposed aluminum interconnections inside the package. Furthermore, intermetallic compounds may form between the gold wire bond and aluminum bond pad. When the gold/aluminum intermetallic compounds are formed, voids are often left by the rapidly diffusing aluminum at high temperatures. Degradation of the bond pad/gold wire interconnections ultimately results in electrical opens.

Most of the failures may be discovered during the reliability qualification and screening before products are shipped to customers. However, a few may go undetected, resulting in electrical failures during service. Furthermore, electrical components may be placed in critical situations where they are expected to be reliable at 100%.

This dissertation will first present background information on reliability issues and testing procedures for product qualifications. Next, we will discuss two approaches of reducing stress on top of the die and protecting the aluminum bond pads.

1.2. Current Reliability Issues

The semiconductor industry faces the challenge of dealing with numerous reliability issues. The package technology group at the National Semiconductor Corporation (NSC) focuses much of its resources on improving reliability, reducing cost, and increasing yield. Addressing these factors often involve many trade-off. For example, using low cost epoxy as the encapsulation material increases the challenge of improving reliability and yield.

Reliability of integrated circuits is often measured by electrical opens and shorts in the final package assembly. These failures often occur as a result of stresses, intermetallics, and corrosion inside the package following environmental testing. This section will discuss the stress, intermetallic, and corrosion mechanisms that lead to electrical failure. Furthermore, we will examine some solutions that are being implemented in the today's semiconductor industry.

1.2.1. Stress

One major issue that must be dealt with in plastic packaging is the internal residual stresses at the different material interface. This is due to the thermal expansion and contraction mismatch between different materials. Table 1.1 lists some mechanical properties of typical elements used in plastic packages measured at 25 °C. Epoxy is cured at the zero stress temperature in contact with silicon and copper leadframe. The epoxy shrinks more than the rigid silicon, applying a residual stress at the interface. Therefore, the epoxy is

thus in tensile stress, while the silicon and lead frame is in compressive and shear stress.

Table 1.1 Mechanical properties of materials used in microelectronic packaging[10].

Si	19-29	2.3-3.5	16-25	0.278
Alloy 42	21	5	75	.31
Au eutectic	12.5	14.2	16	-
Cu	17.3	16.9	60	0.343
Epoxy mold Compound	1.8-3	7.5-28	10-20	.25
Polyimide attach	0.6	35-60	1-8	-

Using the data from Table 1.1, the stress at the interface between two materials can be estimated using the following simplified equation:

$$\sigma_0 = \frac{E\Delta\alpha\Delta T}{1-\upsilon} \qquad [1.1]$$

σ_0: Residual stress
E: Modulus of epoxy molding compound
$\Delta\alpha$: Difference in thermal expansion coefficient between two materials
ΔT: Difference between curing temperature and room temperature
υ: Poisson's ratio

The difference in the thermal expansion coefficient between two adhering materials and the modulus of the molding compound play a major role in defining the stress intensity at that interface. In addition, the temperature of the package is also critical. In standard testing methods, parts

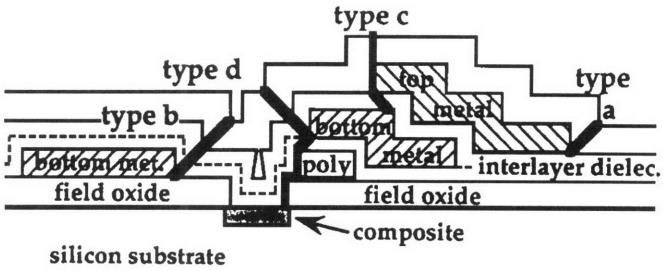
are often stressed by temperature cycling between -65 °C to 150 °C. The maximum residual stress is observed at -65 °C.

It is difficult to calculate directly the stress history of the plastic package. The physical properties of the package materials can also change with temperature. When heated, the CTE increases and the elastic modulus decreases in a nonlinear fashion. Furthermore, an abrupt change in the CTE and Young's modulus takes place at approximately 140 °C which is close to the T_g of the material[10].

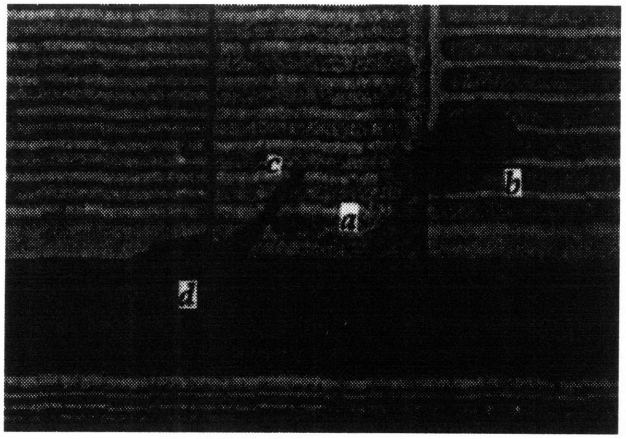
One useful tool to characterize stress inside a package is by finite element analysis (FEA). This is a computationally intensive tool executed on high-speed computers to calculate the value of stress fields within solid objects. Based on different geometrical designs and materials selection, one can observe the stress concentrations in the package, indicating the likely locus of failure.

1.2.1.1. Passivation and Interlayer Dielectric Cracking

During thermal cycle testing, residual stresses resulting from differences in expansion coefficient causes large relative displacements at the silicon and molding compound interface. The stress from epoxy molding compound transfers to the brittle passivation and interlayer dielectric film. An interlayer dielectric film separates two different metal metallizations at different layers, and the passivation film protects the top metallization from corrosion. Figure 1.2 shows four different types of cracks that can occur in the interlayer dielectric[2]. These cracks allow the different metal lines to short circuit one another, thus failing the device.



(A)



(B)

Figure 1.2: Four different types of interlayer dielectric cracking is captured. (A): Cross-sectional schematic. (B): Surface of the integrated circuit revealing cracks with dye staining methods.[17]

Moore and McKenna did FEA modeling showing the shear stress distribution across the die surface in Figure 1.3[10]. In some stress sensitive devices, electrical failures are more likely to result at the stress sensitive corners.

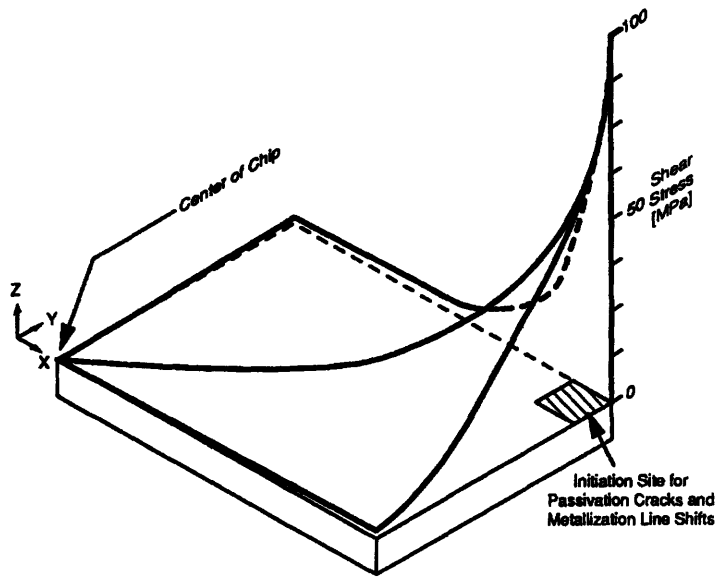


Figure 1.3: Shear stress distribution across surface of die as calculated with FEA techniques.[10]

1.2.1.2. Bond Wires Integrity

Stresses at the wire bonding site can become an issue in the presence of plastic-to-die delamination or when soft gel coatings are applied to the die surface[10]. Successful attempts have been made in applying a soft gel and conformal coatings on top of the die surface to reduce stress on the die. However, broken bond wires have been observed in temperature cycling tests.

Further two dimensional FEA data from Moore and McKenna show that the maximum shear stress on the wire bond increases from 135 MPa to 480 MPa in the case of delamination between the die and encapsulation[10]. Gold plastically deforms between 275 and 415 MPa, depending on its grain structure. Figure 1.4 shows the stress contours for the case of perfect adhesion and delamination on top of the die.

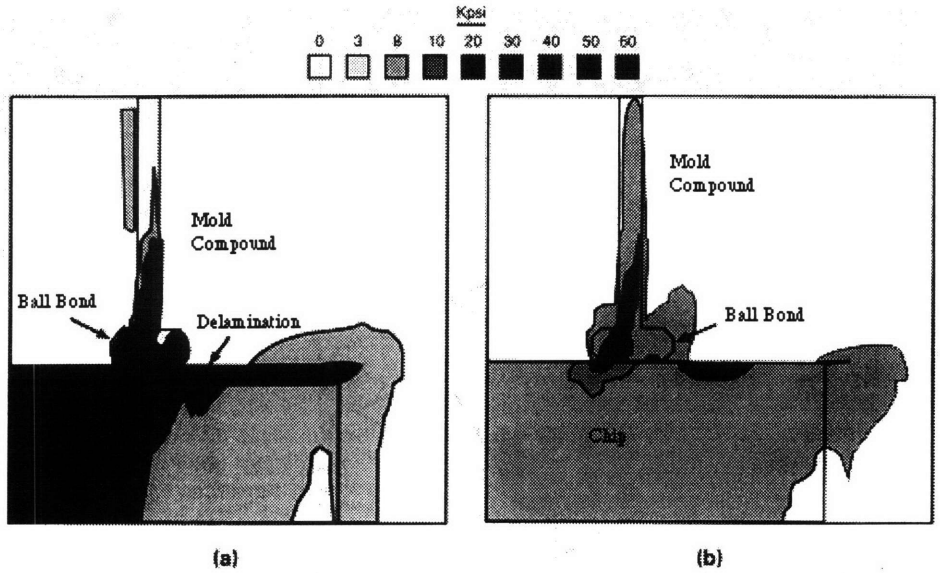


Figure 1.4: Maximum principal stresses for (a) ball bond with plastic-to-die delamination and (b) no delamination. Stresses are reported in psi. (Source: Moore and McKenna)

1.2.2. Intermetallics

The integrity of ball bonds can be further compromised by the presence of intermetallics at the contact between the gold wire and aluminum pad. The gold and aluminum intermetallics actually increases the adhesion strength between the two metal. However, the bond failures observed have resulted from formation of gold-aluminum intermetallic compound associated with Kirkendall void formation[3]. This occurs when the rapidly diffusing aluminum forms the intermetallic compound with gold, leaving large voids in the aluminum. In combination with the cyclical stresses from the molding compound, these large voids increases the chance of ball bond failures.

Although the classical formation of gold-aluminum intermetallics occurs only at high temperature, most present-day Au-Al related failures are driven by impurities. The typical intermetallics formation produces voids between gold wire bonded to aluminum metallization if the temperature-

time product is sufficiently large. These intermetallics may form during bonding, plastic encapsulation cure, surface mounting, and during the life of a device[3]. In automotive applications, it is crucial that these plastic packages can withstand a long, high temperature storage life. Intermetallics in conjunction with stresses inside the package can cause serious electrical opens and shorts failure.

1.2.3. Corrosion

Stresses in the package may cause it to fracture, allowing a path for moisture to corrode exposed aluminum bond pads. Corrosion is defined as materials deterioration caused by chemical or electrochemical attack, in the presence of electrically conductive solutions (electrolytes)[4]. These electrolytes may cause severe damage to exposed interconnections on the device surface. In most conventional packages, a gold wire is bonded directly to an aluminum pad, leaving a large area of the pad exposed. Without its protective oxide layer, aluminum reacts readily with pure water[5].

It is widely known that corrosion occurs by a combination of the following three reactions[5].

$$6HCL + 2Al \rightarrow 2AlCl_3 + 3H_2 \uparrow \qquad [1.2]$$

$$AlCl_3 + 3HOH \rightarrow Al(OH)_3 + 3HCl \qquad [1.3]$$

$$2Al(OH)_3 + Aging \rightarrow Al_2O_3 + 3H_2O \qquad [1.4]$$

Aluminum will stop being attacked when the reaction between HCl from the ionic contamination in the molding compound and Al proceeds to completion as in Equation 1.2. However, with the presence of water, the reaction will continue until the aluminum is completely dissolved.

When the moisture collects at the top surface of the silicon devices, it forms an electrolytic pool which is a source for galvanic corrosion. Most

devices are passivated with a film of SiO_2 or Si_3N_4 which protects the underlying aluminum traces from corrosion. However, a crack in the package allows a path for moisture to penetrate the encapsulation at an even faster rate. The following sections will describe the nature in which moisture penetrates the plastic package to corrode aluminum bond pads and traces, causing open electrical failure.

1.2.4. Environmental Conditions

We have recently discussed the internal stresses and potential problems inside a standard plastic package. This next section will address the hostile environment that often shortens a life of a device. The main disadvantage of plastic packaging is that, not being a fully hermetic package, it is greatly influenced by the environmental factors from the outside.

1.2.4.1. Moisture Absorption

One of the greatest threat to plastic packages is moisture in the atmosphere. Epoxy molding compounds have relatively porous structures, allowing the transport of water molecules and ions. In addition, the polar groups in epoxy provide an added mechanism for water absorption. The absorption of moisture is governed by Fick's Law of Diffusion. The equation is simplified and expressed as follows[6]:

$$\frac{Q_t}{Q_s} = \sqrt{\frac{Dt}{\pi L^2}} \qquad [1.5]$$

$$D = D_o * e^{\frac{-E_a}{KT}} \qquad [1.6]$$

Q_t: Sample moisture absorbed amount at time t (wt%)
Q_s: Moisture absorption amount at saturation
L: Sample thickness
t: time
D: Diffusion coefficient
E_a: Activation energy
K: Boltzmann Constant
T: Temperature

These equations show that the moisture content absorbed in the encapsulation is dependent on the moisture concentration, the temperature of the ambient environment, and the soak time in that atmosphere. To understand the realistic effects of environmental conditions on package reliability, we used special chambers to control relative humidity, temperature, and time. The relative humidity determines the amount of moisture that will saturate a package, while the temperature controls the rate at which moisture is absorbed with respect to time[7].

1.2.4.2. Delamination

Equations 1.5 and 1.6 indicate that moisture will diffuse into the plastic package at a rate dependent on the moisture gradient along the diffusive path. Figure 1.5 illustrates the concept of moisture diffusion in a plastic package[8].

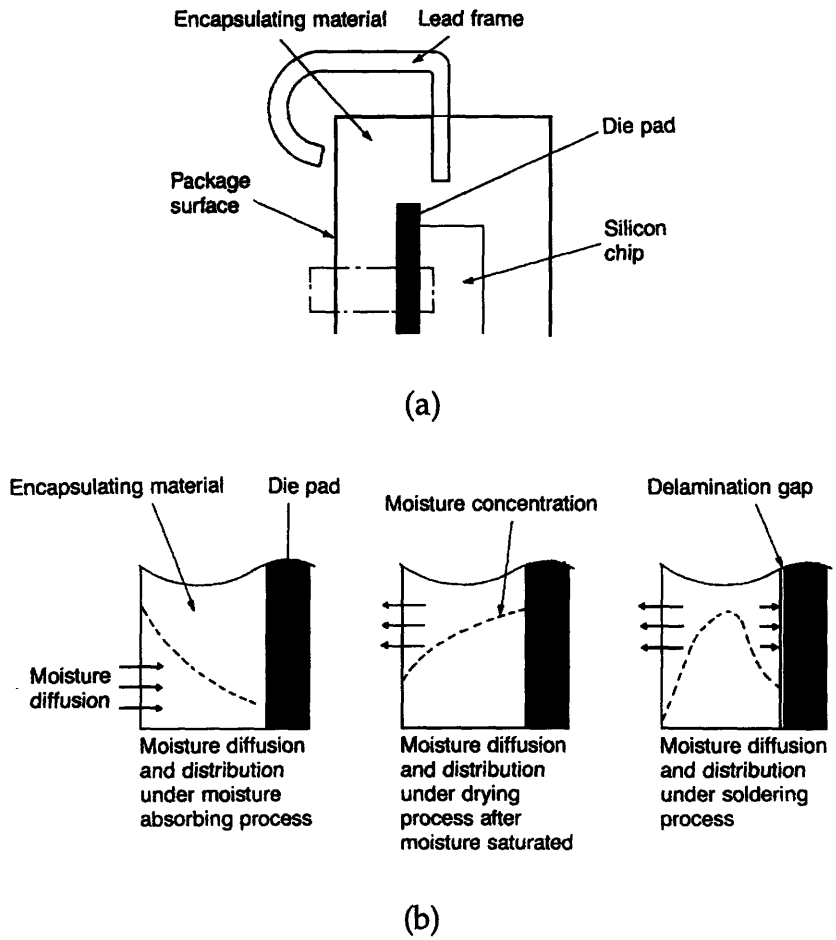


Figure 1.5: Concept of moisture diffusion model. (a) cross-section of a typical plastic package. (b) From left to right, moisture diffusion curves for absorption, drying, and solder reflow simulation.[8]

The models in Figure 1.5 show the moisture distribution under different conditions. The last model to the right indicates that delamination along the copper die attach pad and molding compound can be induced by the high solder reflow temperature. Delamination along an interface between two materials can serve as a reservoir for additional water to collect.

Another critical interface is along the die surface. Delamination on the surface of the silicon die allows moisture to form an electrolytic pool, inducing corrosion of the aluminum bond pads. In many cases,

delamination is used as an indicator of failure prone devices[9]. Scanning acoustical microscope is a common tool used to analyze delamination at different interfaces in a package, predicting failure prone devices.

1.2.4.3. Popcorn Cracking

When moisture inside the package is heated as in surface mount solder reflow, vapor pressure created by superheated steam may exceed the adhesive strength of the package causing delamination. Figure 1.6 shows a schematic of a package cross-section, highlighting the delamination that often occurs at the bottom of the die attach pad. Stress contours were taken from FEA work done by Moore and McKenna under a 300 psi pressure load along the delamination, simulating solder reflow at 220 °C[10]. High stress levels are concentrated at the corners of the die attach pad and at the top of the die surface.

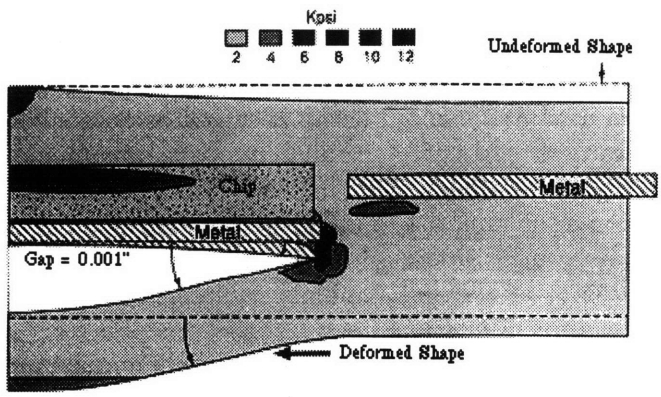


Figure 1.6: Stresses calculated in IC package using FEA with 300 psi load between the DAP and the molding compound.[10]

The vapor pressure causing the deformation is governed by the ideal gas law which states that the vapor pressure is proportional to the temperature[11] (PV=nRT). If the vapor pressure under the die attach paddle exceeds the strength of the molding compound, a crack may propagate from the bottom corner of the paddle to the bottom surface of the package as highlighted in Figure 1.7. This type I crack is the most commonly seen crack among various packages.

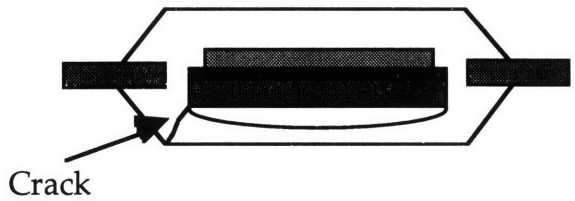


Figure 1.7: Crack is shown extending from bottom corner of the die attach pad to the outside of the package. Most cracks are initiated at the corners where the stress concentration is greatest.

In addition to the moisture absorption effects of the epoxy, geometric considerations in packaging design greatly affects the susceptibility of popcorn failure. As package size continues to shrink due to demands of higher board mounting density, there is less protection for the device. Thinner packages allow moisture to penetrate at a faster rate. In addition, as the die attach paddle increases in size, greater stress is concentrated at the corners. These factors make the package more prone to popcorn cracking, thus increasing the rate of failure due to corrosion.

1.2.5. Current Solutions

The electronic packaging industry offers a number of potential solutions to the current reliability issues. In the discussion earlier, we mentioned a few things that are being done to improve packaging reliability. We will discuss some solutions that have been widely implemented for plastic packaging to reduce stress and eliminate popcorn cracking that leads to corrosion.

1.2.5.1. Stress Buffers

Stress on the die may be reduced by an application of a compliant polyimide film. This adds another processing step in the fabrication process.

Different sets of equipment and chemicals are required since the polyimide is not compatible with the standard photoresist process flow. Although the polyimide does aid in reducing the stress on top of the die, it is not sufficient for some stress sensitive devices.

Thicker coats such as glob tops have been evaluated as a replacement for molding compound. This process involves the use of a liquid placed on top of the silicon die to protect it against environmental conditions. Glob tops are being used primarily in the chip on board assembly, where the silicon die is wirebonded directly to a PC board substrate. The glob replaces the packaging. This technology can be applied to low cost products that do not require high reliability standards.

1.2.5.2. Design Rules

Not all components and constructions are stress sensitive. Therefore, design rules have been developed to keep sensitive components away from stress sensitive regions at the corners of the die. However, this restricts the designer's use of already scarce substrate landscape due to the miniaturization trends. It is an added inconvenience for device designers to achieve the most electrically efficient construction with the small landscape area.

1.2.5.3. Moisture Barrier Dry Packing

One approach to control popcorn cracking is to not allow moisture to be absorbed in the package prior to subjecting it to high reflow temperatures of over 220 °C. Surface mount packages that are more susceptible to cracking are sealed up in desiccated, water impermeable packs after molding. This keeps the packages dry in the shipping and receiving docks. Once the bag is opened, the customer will have about two days to mount the products before they are required to bake out the moisture in a low temperature oven. This solution adds the cost of dry packs and trays to the product cost. In addition, the customer is limited to a time frame window for mounting.

1.2.5.4. Hermetically Sealed Package

Another approach to improving electronic packaging is to establish a hermetic seal in the package, eliminating any delamination that would form moisture pockets. The effects of moisture absorption can be reduced by eliminating delamination at the key interfaces in the package. Some approaches include creating dimples on the bottom of the die attach pad, cleaning the die surface with a plasma etch or ozone prior to molding, and resorting to different molding compounds. These solutions are often high cost and do not solve the total package reliability issues. A package without delamination will face other issues.

1.2.5.5. Molding Compound

One clear path for addressing many of these reliability issues is to improve on the properties of the molding compound. The ideal would be a low cost compound with low moisture absorption, low stress, and high fracture toughness. However, it is extremely difficult to optimize all of their properties. Any modifications to the molding compound would automatically lower the cost effectiveness of the plastic encapsulate.

The thermo-mechanical properties of molding compounds are strongly influenced by filler selection, filler loading, resin compounding, and catalyst blend[12]. With the increase use of fused silica filler contents, the modulus is increased based on the classic equation for composites. On the other hand, the increase in differential shrinkage-induced microcracks provide slippage planes that yield lower CTEs. In addition, short-chain coupling agents cause exceptionally high stresses at the filler-epoxy interface[12].

1.3. Standard Reliability Testing

Standard reliability testing methodology was developed to correlate processing parameters with device long-term reliability at an accelerated rate.

This section provides brief background information on some tests used in this experiment. Three typical stress tests used to predict reliability are high temperature/voltage bias, temperature/humidity/voltage bias, and temperature cycling[5]. In these tests, the parts are situated in different temperature and humidity chambers. The first two tests also require a voltage bias based on the device's operating conditions. The temperature cycling test subjects the parts to continuous changes in temperatures. These tests would generally take 5,000 hours to induce failures on good devices. Due to the lack of time and resources, we could not complete the full electrical characterizations required to qualify parts for customers.

In this experiment, we used the standard environmental tests to make comparisons between different test vehicles. We used different test chips to make simple resistance measurements to determine electrical leakage and opens. Since most failures are induced by the initial storage and mounting conditions, we simulated conditions that operating parts may be exposed to in its early life. To run the full electrical characterization would require months to be able to analyze the results. We simulated the initial preconditioning process and environmental stresses.

1.3.1. Preconditioning

After the molded units are fully cured, we exposed the plastic encapsulations to environmental stresses that simulate the package to board mounting process. We used the humidity chambers to simulate the moisture conditions that a real part may experience during storage at an assembly site before mounting. After the samples were sufficiently soaked with moisture (usually 85 °C/85% relative humidity at 168 hours), we subjected them to a solder reflow process. The convection IR furnace simulated the temperature profiles necessary to melt the solder that joins the chip to the circuit board during assembly. The furnace ramps up at a rate of

only 1 to 5 °C per second, taking a few minutes to reach the peak temperature between 220 °C and 240 °C.

1.3.2. Environmental Tests

Besides the standard preconditioning tests, further stresses can be applied to the test units to simulate and accelerate conditions that may be encountered during the operating life of the device. In choosing an accelerated test, we must be careful not to change the mechanisms that induce failure.

One common test that is performed is a temperature cycling. Most specifications are set for temperature changes from -65 °C to 150 °C in air ambient. A device can generally pass at 1000 temperature cycles. A few failures accelerated by temperature cycling are:

- Ball-bond lifts
- Wire breaks
- Chip and package cracks
- Passivation cracks
- Dielectric cracks

Another test which is often performed is an autoclave test. Parts are subjected to a 2 atm steam pressure chamber at 121 °C for an extended time period. The highly saturated environment induces corrosion as discussed in the previous section. Although devices may never be exposed to such extreme conditions, it will accelerate the moisture diffusion mechanisms much faster than the standard 85 °C/85% relative humidity conditions. These testing mechanisms aid us in quickly evaluating new package designs and solutions to solve these existing problems.

1.4. Objective of Research

The objective of our research was to focus on two concepts to address the current reliability issues. We will develop ways of making the silicon device more robust in relation to the plastic electronic package. We based our research on some of the work that was developed earlier from literature and also from the packaging technology group at the National Semiconductor Corporation. Since some devices may be sensitive to only one of these issues, it may not be necessary to integrate all of the "fixes" in one package. In addition, we will discuss other side benefits that could be achieved through these two programs.

We will discuss a glob top solution to solve the interlayer dielectric and passivation cracking issue on top of the die and the electroless cap solution to improve the bond pad reliability. This section describe briefly the solutions that have been developed. The remaining dissertation will provide more detailed description of the experimental procedures, and discussions of the analyzed results.

1.4.1 Glob Tops for Stress Reduction

Glob tops were made popular about 5 years ago, when they were used as a replacement for traditional molding compound. Some success has been observed in using the liquid encapsulant in lieu of molding compound in chip on board applications where a silicon chip is mounted directly onto the PC board substrate. This eliminates many molding problems associated with high pressure and cavity flow.

Instead of replacing the molding compound, we looked into using a low stress glob top material as a stress buffer between the molding compound and the device as revealed in Figure 2.4. There are certain devices in which the existing polyimide stress relieving/passivation layer is not sufficient to reduce the stress on the die. A few attempts have been made, using rubbery

or silicone gels as a stress buffer. However, many have resulted in broken wires[13].

We looked into using a low cost rigid liquid encapsulant with a low coefficient of thermal expansion. To leverage the cost of the stress buffer, we also tested the effects of using a higher stress, lower cost epoxy for overmolding the stress buffer. We ran tests to measure the wire breaks and passivation cracks by the electrical characteristics of the test chip.

1.4.2 Electroless Plated Caps for Improved Bond Pad Reliability

The trend for plastic packaging today is to achieve a better hermetic seal to protect the sensitive device inside. However, due to the limitations of the epoxy molding compound, moisture absorption is inevitable. We took a different approach by allowing moisture to freely enter the package as long as the critical surfaces were protected. We suggested an electroless nickel be used to passivate the most critical surface which is the exposed aluminum bond pads. The other areas on the die were passivated with a $Si0_2$ and Si_3N_4 and were well protected from moisture absorption. The leadframes can also be plated with nickel and palladium to passivate the bare copper. The palladium can eliminate the need for solder plating the outside lead fingers after the molding process, saving valuable processing time.

Electroless plating has been around for some time now, however, only recently has its use has been investigated in the microelectronic field. The dominant metal used in these plating processes has been nickel. The main advantage of the electroless plating process compared with the much faster plating rate in traditional electrolytic plating is that it is selective. Plating will only be done on active sites having a high electrochemical potential.

Work has been done in using a number of material such as Ni, Co, Pd, and Cu for contact filling, via filling, and for conductor patterns[14]. One of the most active area of work in microelectronics is selectively plating copper

patterns on printed circuit boards[15]. This is considered a low cost process because it does not rely on the use of masks to plate on patterned surfaces.

Most of the active research in this area resides in Japan and the European countries. Research was also done in plating on aluminum bond pads to form microbumps for an alternative bonding method[16]. We used these research data along with a few others as a basis to form the nickel cap on top of the aluminum bond pads[14-16,19-20]. The existing passivation serves as a mask for plating, eliminating the masking and etching of photoresist films. A typical plating line consists of temperature controlled plating baths with mechanical agitation, separated by water rinsing baths.

The nickel cap would serve as a moisture barrier to protect the corrosion-sensitive aluminum. The vents, which can be holes strategically placed at the bottom of the package will allow water to freely leave the package when heated to high temperatures. This will eliminate the steam pressure build-up at the bottom of the die attach pad which can lead to popcorn cracking and wire breaks. A Japanese company has experimented with these types of holes. Although it did stop popcorn cracking, they observed severe corrosion of the bond pads. Our methodology would take care of the bond pad corrosion and popcorn cracking.

Chapter 2

Glob Tops Results

2.1. Introduction

We will first discuss the use of glob tops as a stress buffer to prevent stresses on the top surface of the die. Glob tops are currently being used in lieu of a standard package in limited cases where cost is a major factor. It is used in applications that do not require protection from an extreme atmosphere. One of the most widely applied areas for glob top usage is in chips on board applications where the silicon device is bonded directly onto a PC board. A small glob is used to hold the wires in place for handling. However, in most cases, a liquid encapsulant material does not provide adequate protection against the corrosive effects of moisture.

In this dissertation, we used the glob top as a stress buffer to be placed between the silicon and the molding compound (Figure 2.4). In order to leverage the cost of the additional globbing operation, we looked into the effects of using the glob in conjunction with a lower cost molding compound. The low stress liquid encapsulant can cost approximately 10 times that of the molding compound because it is especially designed to have a low coefficient of thermal expansion in comparison to the molding compound. However, the volume of glob top material used is much smaller than the full package volume. This chapter will describe the experimental set-up of the glob top study, followed by a discussion of our results.

2.2. Experimental Proceedures

The experimental proceedures are described here to provide a better understanding of how the data were collected and interpreted. We will begin by first elaborating on the different test vehicles used for this study. The glob

dispensing technique will also be discussed. Finally, we will discuss the use of different environmental conditions for our evaluation matrix.

Appendix A lists a general process flow in packaging a silicon device. The globbing operation fits easily into the assembly process between the wirebonding and molding steps. We used an automated dispenser to achieve consistent globs on the selected test chips. The devices are then molded with different molding compounds. Resistance measurements are made from several test chips to determine the effects of the globbing with respect to interlayer dielectric cracking and bond wire breaking.

2.2.1. Test Vehicles

Although standard imaging techniques can reveal visible cracks as shown in chapter 1, they only account for 1 to 10% of the total existing cracks in the upper thin film layers. Different test chips were developed by S. A. Gee et al to simplify the task of finding packaging failures[17]. These test chips were used to detect cracks in the interlayer dielectric and electrical opens that may occur from broken bond wires. Different functionality such as diodes and resistors of varied sensitivity are placed on these chips to compare stress effects.

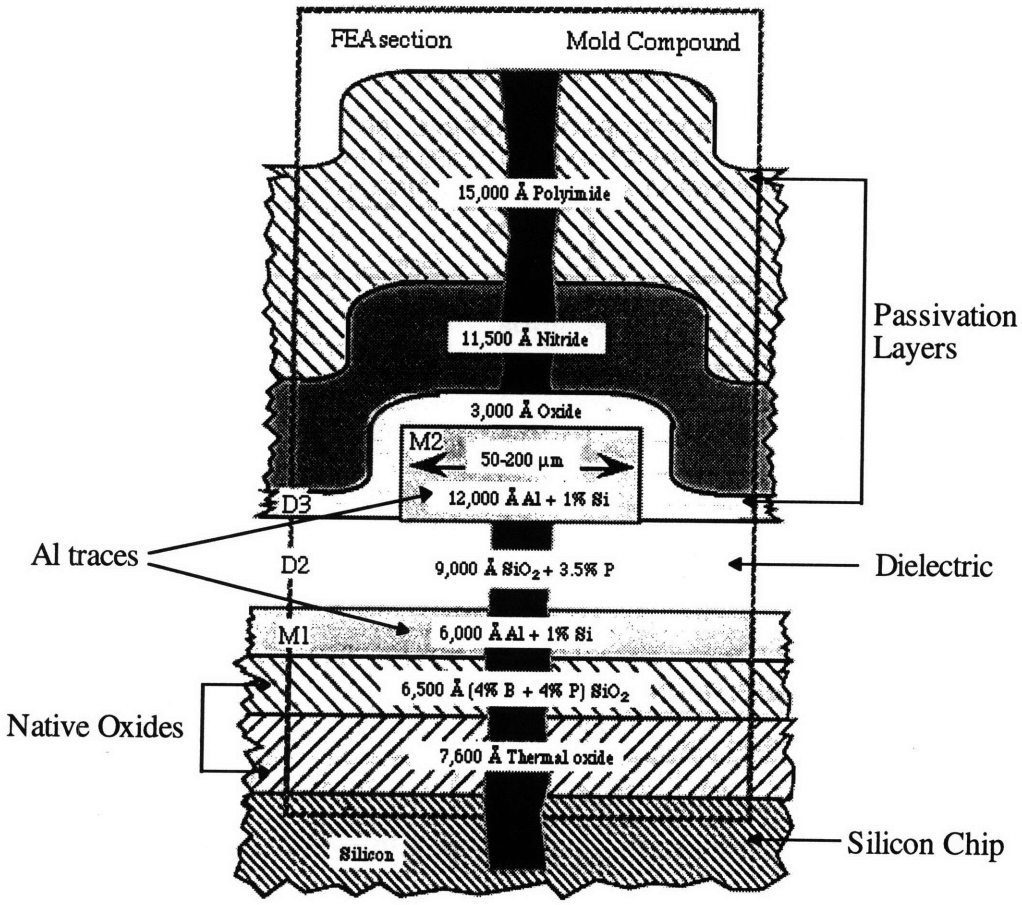


Figure 2.1: Cross-section of the typical interlayer dielectric above the surface of the silicon. The electrical test detects a crack in the D2 layer by measuring the resistance between M1 and M2 aluminum metal traces.[18]

Figure 2.1 shows the interlayers at the surface of the silicon with typical thickness. Cracking would usually occur in the D2 layer, yielding a short between the aluminum M1 and M2. These shorts were detected by resistance measurements made on a tester designed specifically for the device.

We will next describe the uniqueness of the different test vehicles used for this evaluation. They will be referred to as Test Chip A, Test Chip B, and Test Chip C. Due to the different size and configurations of these test chips, they are placed in different packages which will have varying stress characteristics. Table 2.1 shows the various dimensions of the test chips with

respect to the DAP and package body size. Higher stress is generally observed in a package with a large die and DAP with respect to the package dimensions.

Table 2.1: Comparison of die, DAP, and package dimensions as measured in mm.

Test Vehicles	Die (mm)	DAP (mm)	Package Dimensions (mm)
Test Chip A	5.3 x 11.0	11.3 x 11.3	29.2 x 29.2 x 3.2
Test Chip B	3.3 x 5.1	6.6 x 6.6	16.5 x 16.5 x 3.2
Test Chip C	5.4 x 5.4	8.9 x 8.9	28 x 28 x 3.4

2.2.1.1. Test Chip A

Test Chip A was designed to quantify the effects of molding stresses which result in passivation cracking and interlayer dielectric cracking. Its basic structure is composed of a 136μm x 205μm unit cell arrayed to form a 5 by 10 matrix of metal crossover points between the top and bottom metal lines. The metal matrices are positioned at the corner of the die as shown in Figure 2.2.

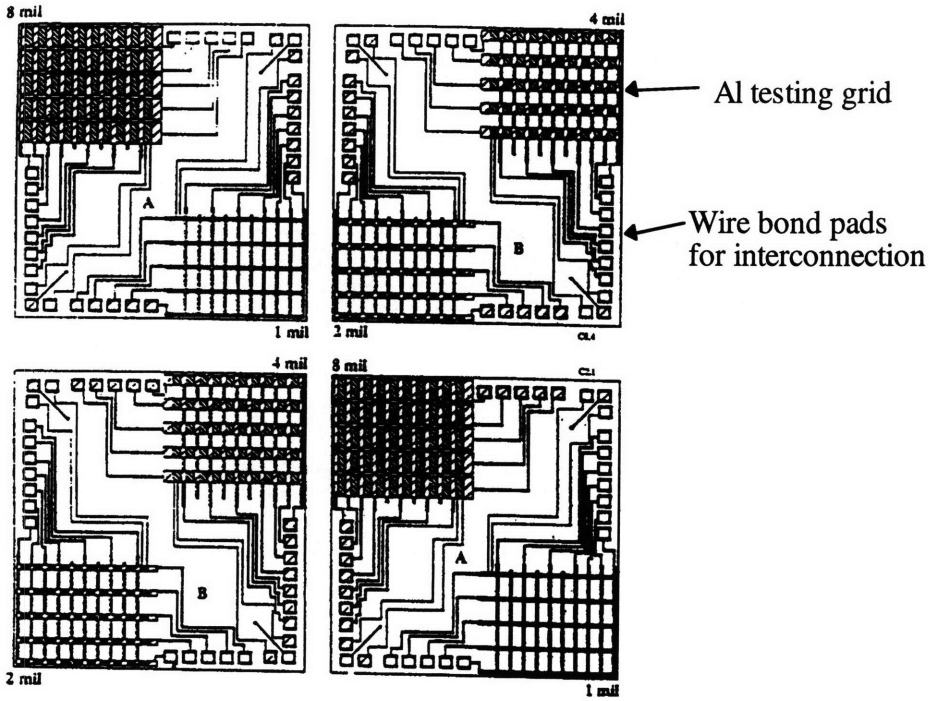


Figure 2.2: Layout of Test Chip A reveals the aluminum metal grids located at the corner of the die. Our test used a 2x2 array to obtain a larger die size. Starting from the top left quadrant, moving in a clockwise direction, we see the 8, 4, 1, and 2 mils aluminum line width in the horizontal direction.[18]

The width of the vertical bottom metal trace on the right is fixed at 75 μm while the top metal width varies depending on the location of the die corners. To evaluate the effects of metal line widths, each corner of the test chip has a fixed top metal trace of either 200 μm, 100 μm, 50 μm, or 25 μm^2.

One great advantage of this test structure is that it allows us to make numerous electrical measurements from each device. A high voltage is applied to the array in rows and columns to measure the current leakage from any of the 5 rows of top metal traces to any seven of the ten columns of bottom metal traces as in Figure 2.2. A computer is used to control the applied voltage as well as to record the resulting electrical resistance. As a result, we can collect up to 35 data points for each bottom metal trace, or 140 data points for each device.

2.2.1.2. Test Chip B

Test Chip A proves to be useful in collecting many data points with few devices built. However, one characteristic that cannot be measured by Test Chip A is the possibility of wire bond breakage resulting in an electrical open measurement. Hence, Test Chip B was designed to capture the electrical shorts and opens in a device by measuring the electrical characteristics of a diode between a ground pad and a few adjacent pads. Figure 2.3 illustrates the diodes positioned around the bottom four bond pads. The ground pad is located at the top left side of the figure.

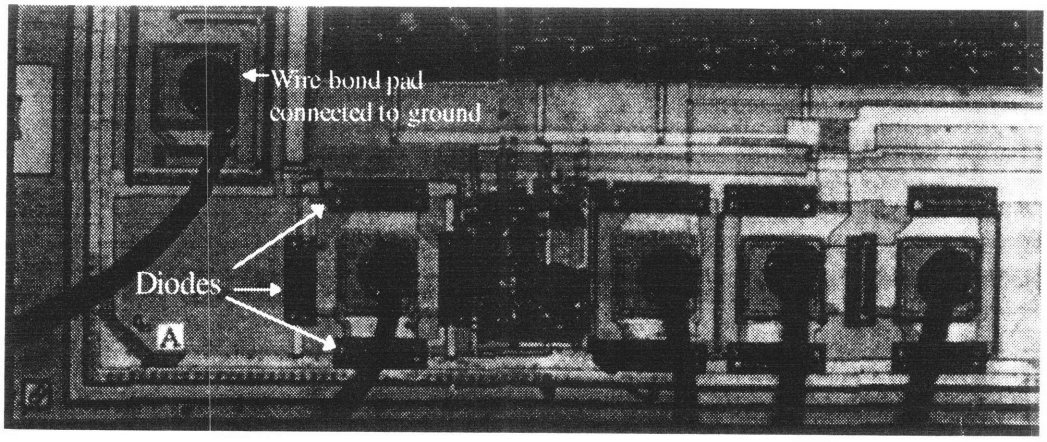


Figure 2.3: A section layout of a Test Chip B corner shows the pad locations and a typical crack propagating at the corner denoted by the A marker. The top left bond pad connects to ground, while the other pads are surrounded by diodes.[18]

As in Test Chip A, current measurements are made between two wires as a voltage is applied. In this case, we measured the current through the diode found between the two wires. A good device should exhibit a typical diode characteristic. In other words, as the applied voltage is increased, the current should also increase. A continuity problem between two wires is indicated by a low current value. Cracks in the interlayer dielectric would then propagate to damage the diode, yielding an electrical short. As a result, a high current will be observed even with a low applied voltage.

Although this test chip offers a more accurate picture of what is going on, there are still needs that would require the use of Test Chip A. For example, Test Chip B is not as stress sensitive as Test Chip A because it is smaller in size, and it is also protected with a polyimide stress relieving film. However, this test structure has been very useful in doing initial reliability testing for die surface stresses[18].

2.2.1.3. Test Chip C

Test Chip C was used primarily to complement Test Chip A. Test Chip C simply has all of the bond pads connected together in a daisy chain fashion. We used this to measure any electrical opens between the different bond pads due to poor wire bonding or wire breakage. Similar to the other test chips, we made electrical measurements using a computer to record the data. A high resistance indicates a continuity problem between two wires.

2.2.2. *Automated Dispenser*

We used an Asymtek Fluid Move 402 dispenser to apply the globs on top of the die. Appendix B contains a schematic of the automated dispenser used in our experiments. A pressure pulse of controlled magnitude and duration is then applied to dispense a calibrated volume of material through a needle heated to approximately 90 C to improve the flow rate. In addition, the die rests on a plate heated to 80 C to improve the radial flow of the material when it impinges on the die surface. Due to the nature of the liquid flow, the resulting glob will yield a dome shaped glob, as shown in Figure 2.4.

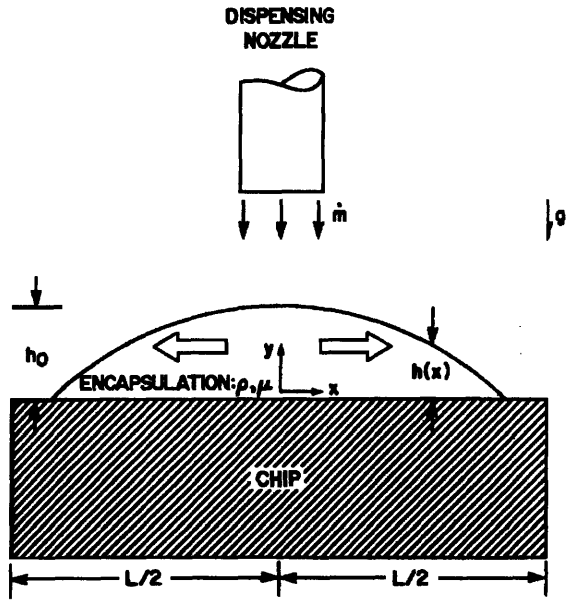


Figure 2.4: A typical schematic showing how a dome can be achieved by the dispensed liquid encapsulant impinging on the top surface of the die. The viscosity of the liquid greatly determines the size and shape of the dome.[5]

In addition to comparing two different globbing materials in our evaluation, we also looked into the effects of glob placement. We evaluated the use of the glob on the die alone versus on top of the die and DAP. In addition, we checked to see if the curing profile for the glob top affects the performance of the liquid encapsulant.

2.2.3. *Environmental Testing*

We subjected the test units to standard preconditioning and environmental testing following the molding process. Our testing specifications required slightly different preconditioning processes for different package sizes. Appendix C shows the specific conditions we used for each test chip-- consisting of a series of temperature cycling tests, each followed by electrical testing to determine the failure rates. At the end of the temperature cycling series, we added a high temperature storage test for Test Chip B where packages are stored in a 175 C chambers for up to 500 hours.

2.3. Results

We will first present the results that were acquired from the three different test chips used in our study. Using these three test chips, we could verify the results under similar environmental conditions. Furthermore, the effectiveness of each of the test chip vehicles can be evaluated.

2.3.1. Test Chip A

We used Test Chip A to evaluate the stress reducing performance of two different glob top materials. The glob top materials will be referred to as Glob Top A and B. We molded these parts with a standard low stress molding compound that we will refer to as MC1. Electrical measurements were made after the molding, preconditioning, and temperature cycling sequences. Approximately 35 units were tested for each leg of the experiment. Some legs had a few more or less units due to the assembly yield. Therefore, we normalized the results to percent failure based on the total number of units tested.

2.3.1.1. Wire breaks

In addition to electrical testing, we used the X-ray to determine if there was significant wire damage due to the assembly process. The X-ray photographs shown in Figure 2.5 to 2.7 represents the typical phenomena we observed in the entire set.

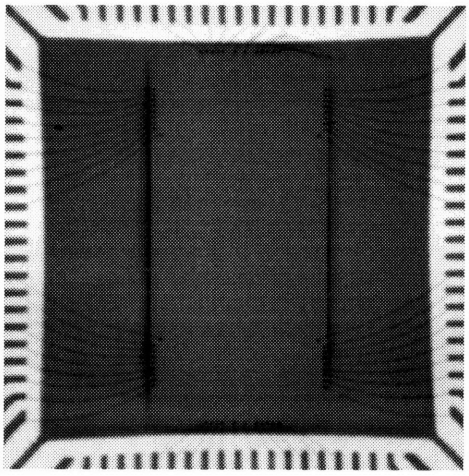


Figure 2.5: An X-ray photograph showing some of the effects of a typical glob top applied to the die only. A slight amount of wire shift can be observed due to the flow pattern of the molding compound. The top of the die reveals that most of the connections to the leadframe have been broken.

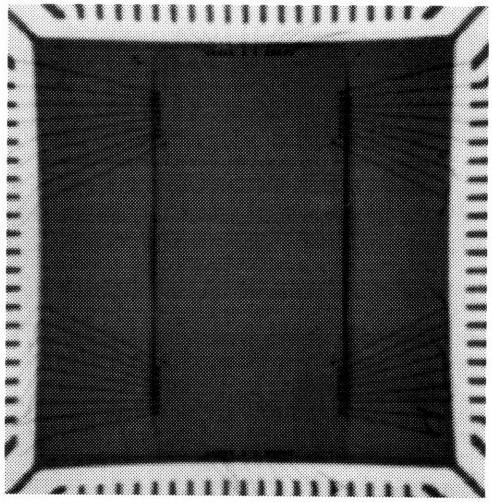


Figure 2.6: A photograph showing X-ray of a glob top applied to the die and DAP. Note that the wires are kept straight where they are encapsulated by the glob. Wire bending observed at the interface between the molding compound and glob top suggests that the wire damage occurred after the globbing process.

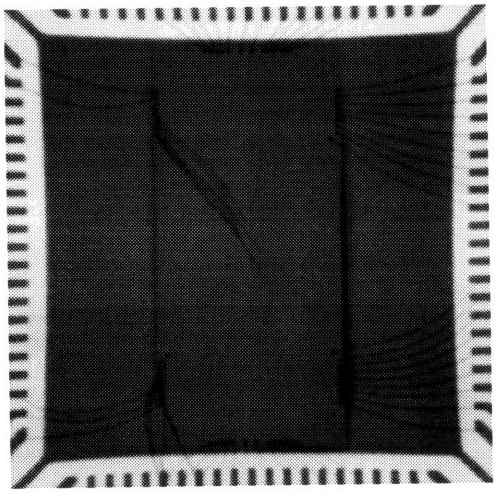


Figure 2.7: The X-ray illustrates a few rare cases of severe damage of the wire which is likely to be from the assembly mishandling of the parts. This is one of the control leg without glob top.

Table 2.2 summarizes the percent of breaks observed in the parts after molding. Recall that test chip A cannot be checked electrically for opens. The best method is to use X-rays to visually detect wire breaks. Although this will catch the gross wire breaks, it will not pick up on any fine breaks in the wire. Units with gross wire breaks were excluded from further testing.

Table 2.2: The table below indicates the percent of devices with gross wire breaks detectable visually by X-rays. Two globs are applied to either the die alone or on the die and DAP.

Experimental Legs	% of gross wire breaks
No globs	3
Glob A on Die	26
Glob A on Die and DAP	18
Glob B on Die	32
Glob B on Die and DAP	43

The data from Table 2.2 indicates that there are more gross wire breaks from the parts with globbing. From the two different globs used, there does not appear to be a consistent trend connecting the failure rate to the

positioning of the glob top. Glob B does seem to have a greater percentage of breakage than Glob A, however, based on the differences in failure percentage, a trend cannot be firmly established between the various globs and the positioning used in this experiment.

2.3.1.2. Interlayer Dielectric Cracking

The remaining units were tested electrically after each phase of the experiment. Any failures that were present after molding were not counted in the remaining phases. We plotted the data in terms of the percent failure found at each specific location where the top metal traces crosses the bottom metal traces. We only counted the data from the perimeter locations since failure in the outer lines can affect the data readings of the inside lines. A short on the outside lines can form a continuous electrical path which will cause the inside to effectively read a failure.

One hundred volts was applied across the top and bottom metal traces. The background current typically measured is in the order of 10×10^{-9} A. A failure is indicated when the current is measured at 22×10^{-6} A. Due to the nature of the electrical measurement set-up, there was room for some error in measurements based on the sensitivity of the wire connection. However, it is a sufficient tool to measure the gross effects of stress on top of the die.

Figures 2.8-2.14 summarize the results collected. Figures 2.8 to 2.10 show the progression of the failure after preconditioning, 500 temperature cycles, and 1000 temperature cycles. We performed 48 temperature cycles each day. Figures 2.10 to 2.14 in this series show results for the glob top units at 1000 temperature cycles. Very few failures were observed in these parts before the 1000 temperature cycle time point.

The electrical failure percentage at each perimeter location is plotted in Figures 2.8-2.14. There are four different top metal trace widths residing in four different quadrants. Moving clockwise from the bottom left quadrant of

the 3-D plots below, we respectively observe regions of 200 m, 100 m, 25 m, and 50 m line widths.

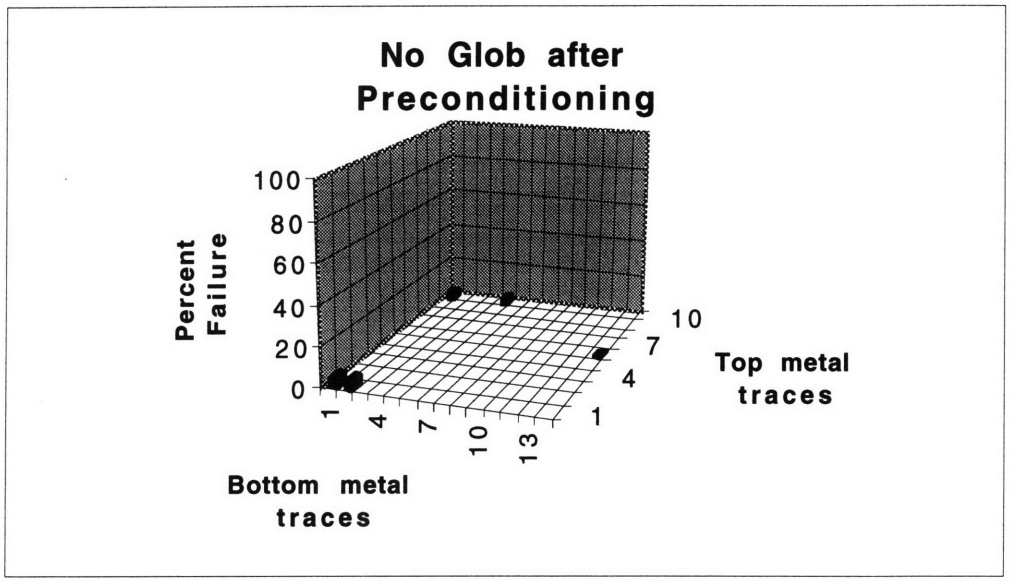


Figure 2.8: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after preconditioning. Only a few failures are detected.

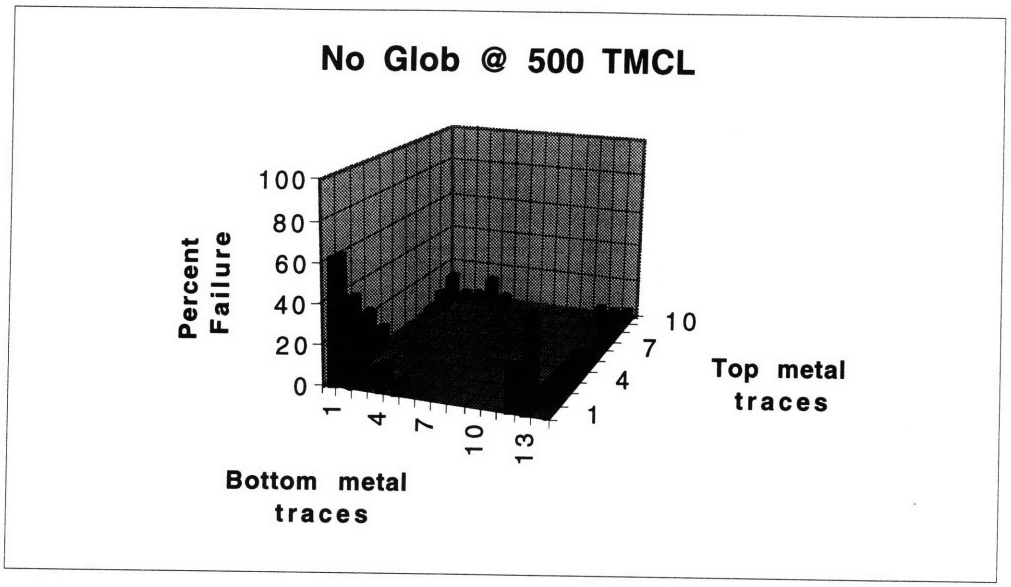


Figure 2.9: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after 500 temperature cycles. This figure indicates a significant increase in failures of the 200 m wide metal lines.

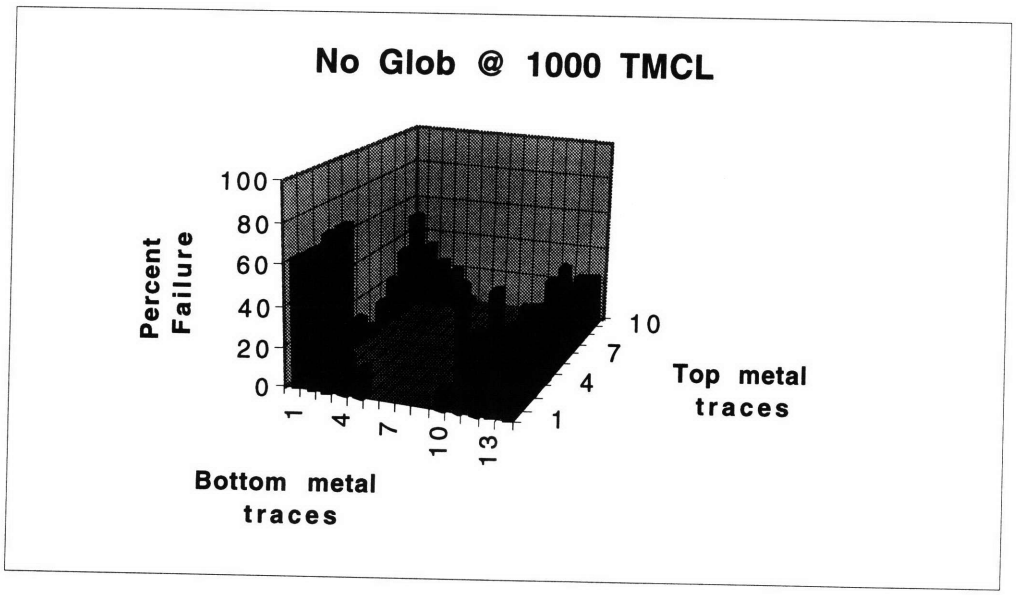


Figure 2.10: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Leg with no glob top is measured after 1000 temperature cycles. The figure indicates significant failures in each metal trace widths. More failures are generally observed at the corners.

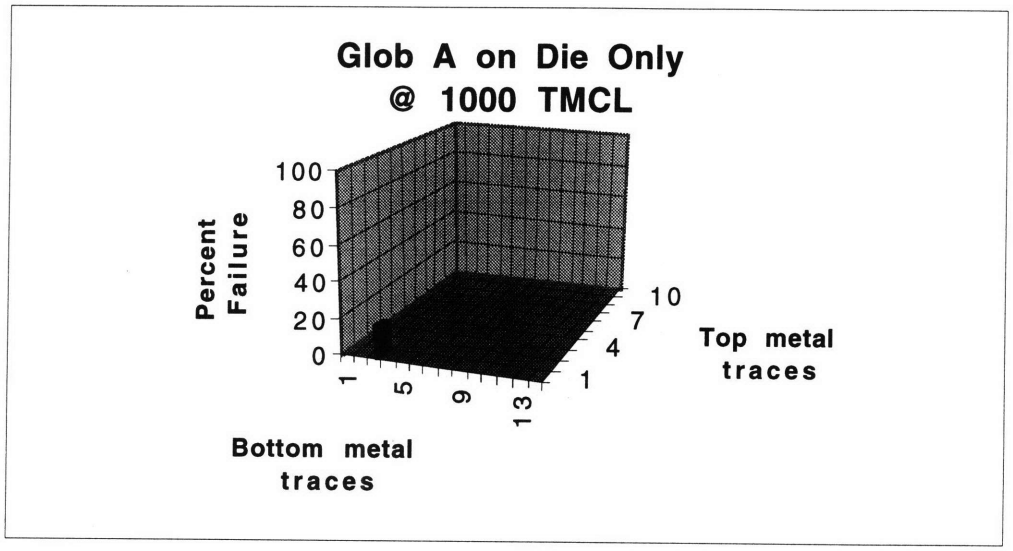


Figure 2.11: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob A is dispensed on die alone. Only a few failures are detected after 1000 temperature cycles in the 200 m quadrant.

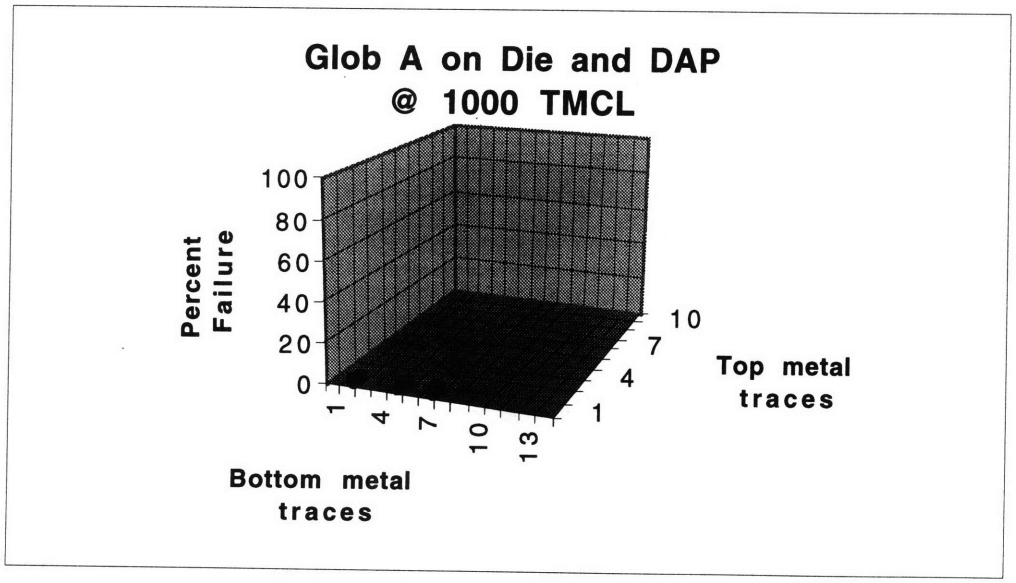


Figure 2.12: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob A is dispensed on the die and allowed to overflow on the DAP. Only a few failures are detected after 1000 temperature cycles in the 200 m line width region.

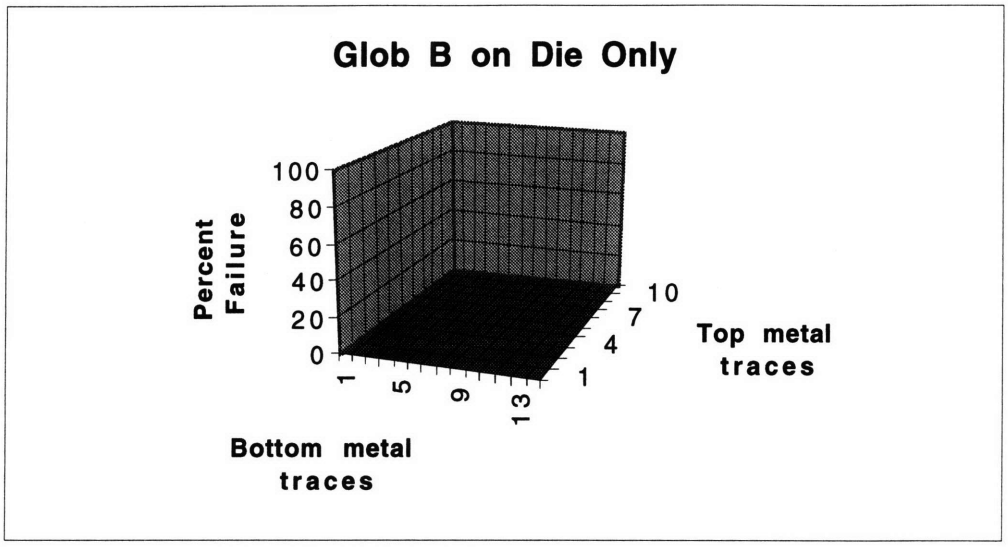


Figure 2.13: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob B is dispensed on the die only. No failures are detected even after 1000 temperature cycles.

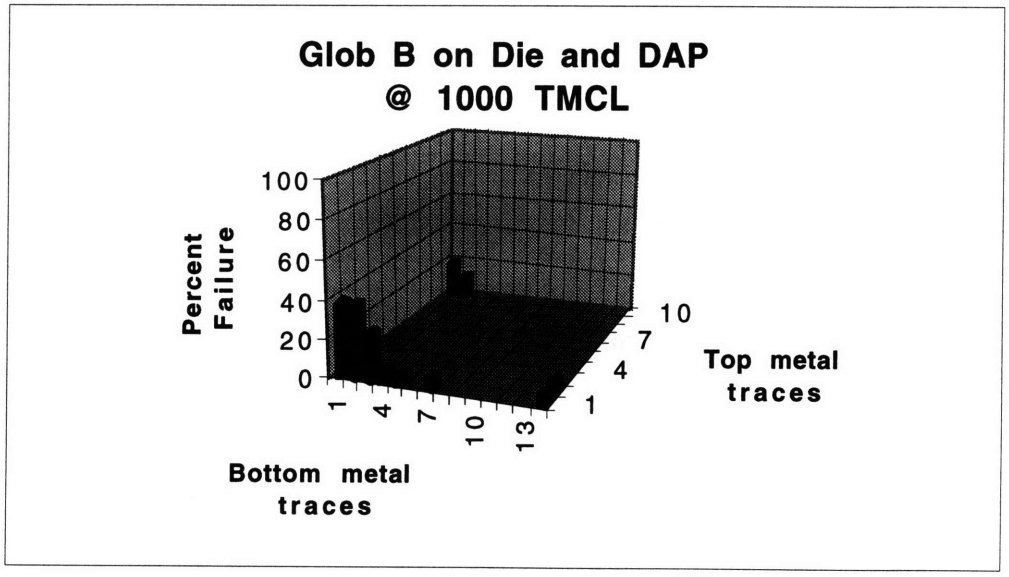


Figure 2.14: Test Chip A showing the percentage of failures at different metal trace locations on the perimeter of the test grid. Glob B is dispensed on the die and DAP. Significant failures are observed in the 200 m metal width regime.

Our results for Test Chip A show that the glob top does relieve the stress on top of the die even after 1000 temperature cycles. However, we observed that the number of wire breaks increases with the use of the glob top. The data also reflects that stress concentrates at the corner of the die.

2.3.2. *Test Chip B*

Test Chip B was used to confirm the results obtained in Test Chip A. Although the die for Test Chip B is smaller than Test Chip A as indicated in Table 2.1, it provided an added capability of detecting electrical opens as well as shorts. Two different experiments were executed using this test chip. In the first trial, we monitored the effects of different combinations of two molding compounds and two glob top materials (MC1, MC2, Glob A, Glob B). The molding compound MC2 has higher stress properties than MC1.

Figures 2.15 and 2.16 show the resulting open and short failures detected following different environmental conditioning. The general testing flow is similar to that of Test Chip A. We performed electrical testing following preconditioning, temperature cycle stressing, and high temperature storage at 175 C for 500 hours. Since this was one of the initial tests, only 16 units were available for testing each leg of the experiment. The high percentage of open failures indicate that many of the devices seemed to be damaged early in the experiment. Figure 2.16 indicates that the devices with the glob top did not experience any dielectric cracking after environmental stressing. As expected, MC2 molding compound did yield a significantly greater amount of shorting failures.

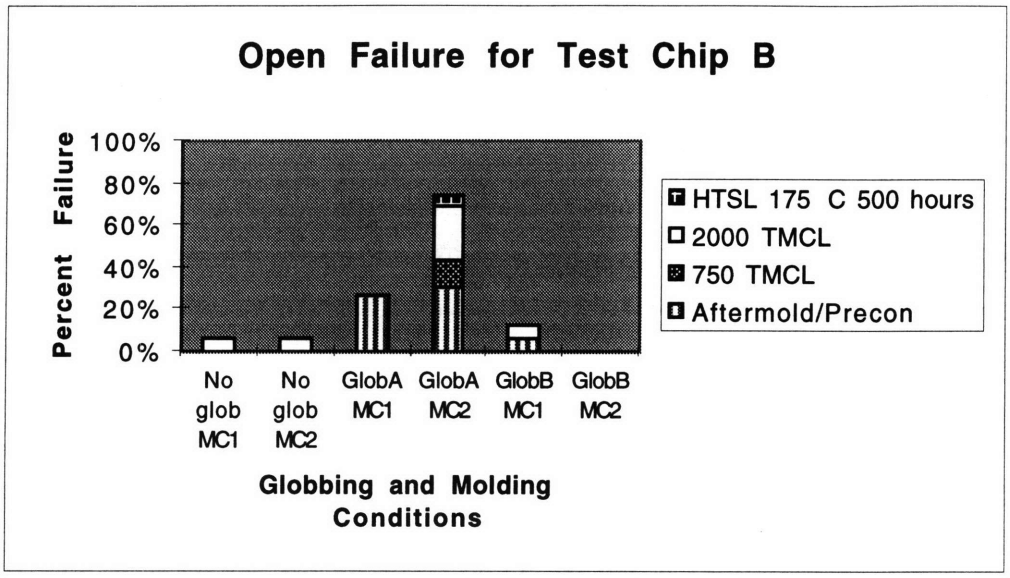


Figure 2.15: The percentage of open failures is indicated for different combinations of glob top materials and molding compounds under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 C to 150 C, Precon-85 C/85%RH @168 hrs, 245 C reflow)

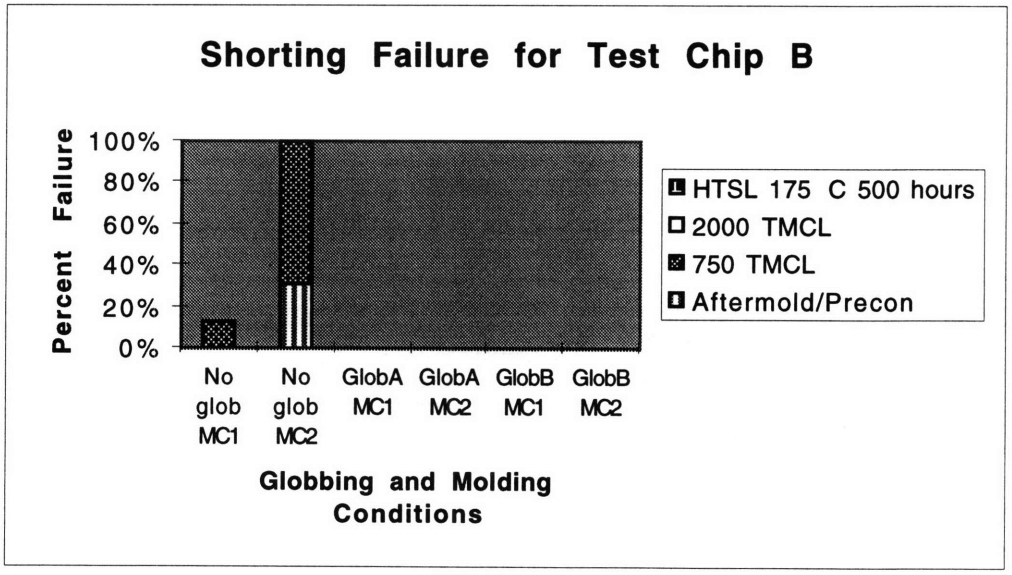


Figure 2.16: The percentage of electrical shorts is indicated for different combinations of glob top materials and molding compounds under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 C to 150 C, Precon-85 C/85%RH @168 hrs, 245 C reflow)

Since there were so many open failures obtained from the early part of the first experiment, we wanted to rerun the experiment with a greater sample size. There were approximately 40 units used for each leg of this experiment. In addition, we used the automated dispenser this time to achieve uniform globs with well controlled material flow. We wanted to revisit testing the effects of different globbing conditions. In addition, we wanted to see if there was a strong correlation between the electrical short failure and the curing temperature of the glob.

Figures 2.17 and 2.18 show that the amount of open failure was dramatically reduced in this experiment in which MC1 molding compound was used. In all of the conditions tested, the glob top did reduce the shorting failure compared with the non-globbed units. The 125 C recommended cure seemed to be slightly better than the modified 165 C cure. A clear trend could not be established about the positioning of the glob. However, if it offers equivalent results, it is much more cost effective to use the glob top on the die only.

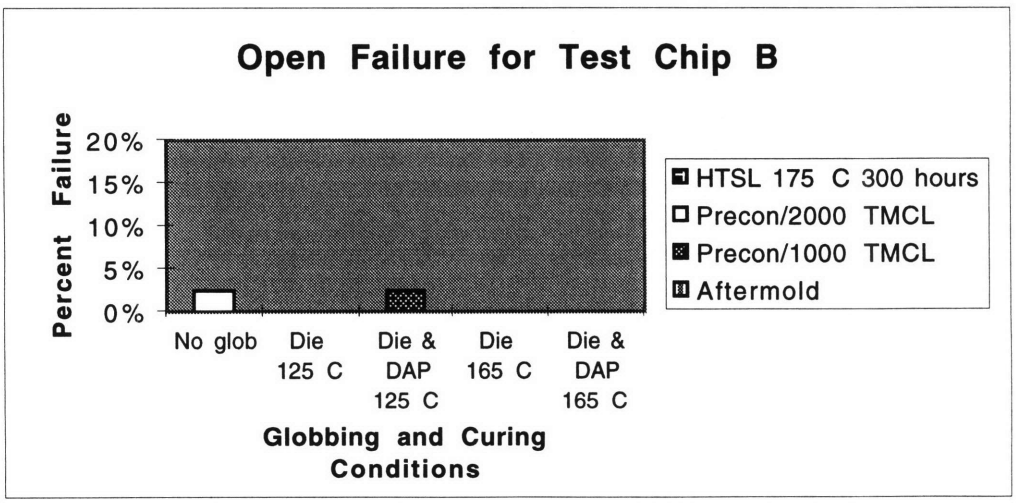


Figure 2.17: The percentage of open failures is indicated for different combinations of glob top locations and curing temperatures under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 C to 150 C, Precon-85 C/85%RH @168 hrs, 245 C reflow)

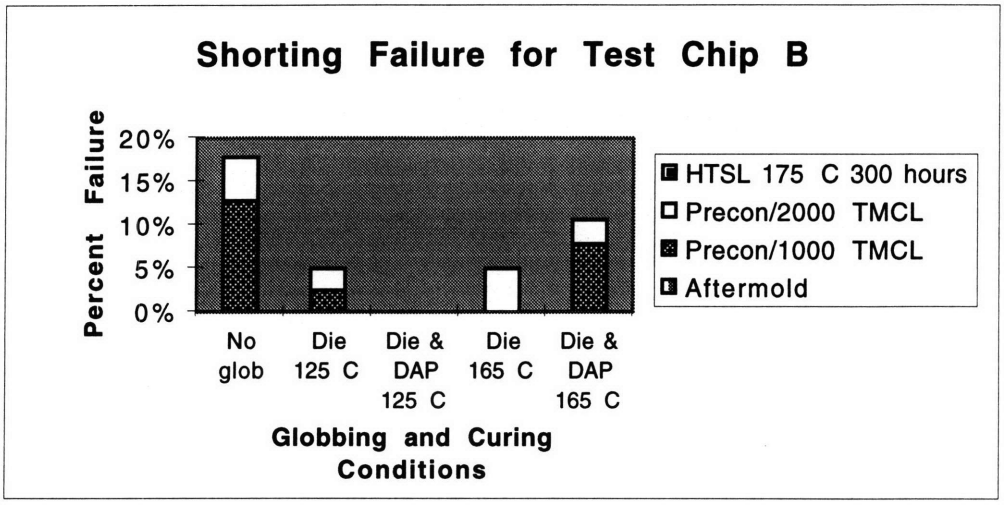


Figure 2.18: The percentage of electrical shorts is indicated for different combinations of glob top locations and curing temperatures under various environmental stresses. (HTSL- high temperature storage, TMCL-temperature cycling from -65 C to 150 C, Precon-85 C/85%RH @168 hrs, 245 C reflow)

2.3.3. *Test Chip C*

We used Test Chip C to verify the results of Test Chip A in regards to the gross wire breaks that were observed. The package size is roughly the same size as the one used for Test Chip A. From Figure 2.19, we observed that most of the open failures occurred only after post-mold cure. This supports the data we acquired from Test Chip A where the wire breaks occur at a stage up to and including the molding process. Most of the failures here are in units where the glob is applied to both the die and the DAP.

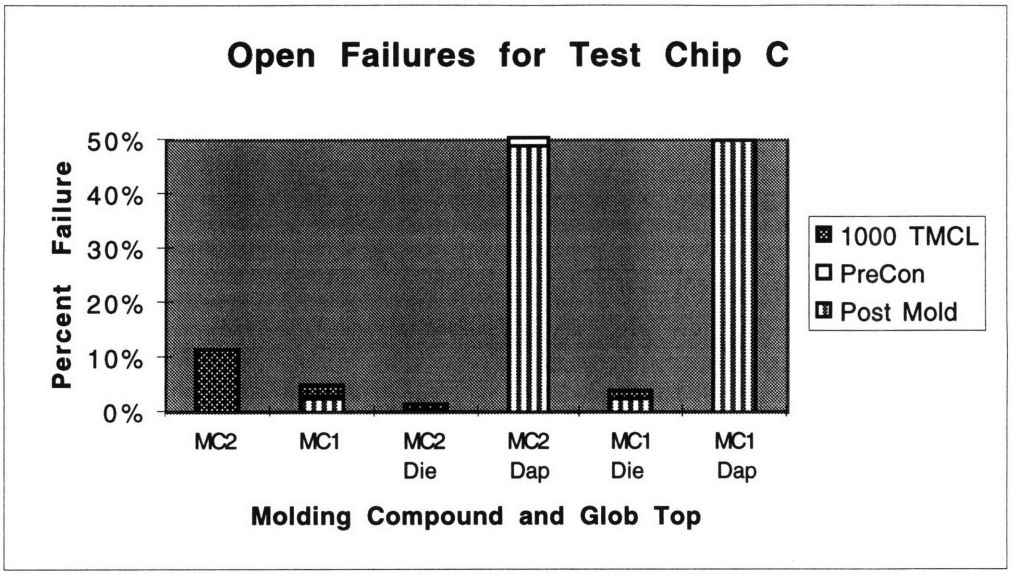


Figure 2.19: Open failure is observed with Test Chip C for different molding compounds and glob top positionings. (TMCL-temperature cycling from -65 C to 150 C, Precon-85 C/30%RH @48 hrs, 245 C reflow)

Without the use of glob tops, the MC2 molding compound yielded a greater percentage of wire breaks than MC1 after 1000 temperature cycles. However, with the glob top being used, electrical opens were no longer dependent on the molding compound. In this experiment, Glob A is used as the glob top material on the die alone as well as on the die and DAP.

2.4. Discussions

The three test chips gave us a good idea as to what is going on inside the package as a result of using the glob top. Overall, we discovered that when applied correctly, the glob top served as a good stress barrier, protecting the die against stress from the molding compound. When a high stress molding compound was used in conjunction with a glob top, it did not make a noticeable difference in the results. The following section will discuss these issues as well as other things that we learned from extrapolating the results.

2.4.1. Gross Wire Failures

There are a few things that may have contributed to the open failures detected in these parts. The wirebonds are extremely fragile before they are encapsulated. Proper handling of these unencapsulated parts may be an issue. This, in addition to the stresses from the flow of epoxy molding compound contributes to gross wire failures. Furthermore, since our parts are built in prototype environment with high demands on equipment use, many of the parameters may not be fully optimized for the process.

The results from Test Chip A indicate that many of the wire breaks originate from the assembly process prior to any environmental stressing of the devices. Table 2.2 does not reveal a significant correlation between the different variations of glob top material and dispensing location. However, only 3% of devices observed gross broken wires for the non-globbed parts compared to 30% average for the units with glob tops. The X-ray presented earlier indicates that these failures may be due to improper handling or from the molding compound flow pressure.

It is very likely that the data obtained were influenced by both the molding processes. The wire sweep in Figures 2.5 and 2.7 indicate that the wires were subjected to a very high pressure inside the molding cavity. Figure 2.6 shows that the glob top across the die and the DAP, fixed the wires in straight lines. However, the section of wire that was not covered by the glob top was subjected to very high stress.

The assemby process control may be another contributor to the massive wire breaks in Test Chip A. Figure 2.7 shows the dramatic breaks in the wires that is indicative of improper handling of the parts. Many of the failures may also be due to poor bonding conditions. Out of the four experiments we ran in our evaluation, this was the only test that yielded significant wire damage. Perhaps the glob top on Test Chip A made it more susceptible to wire damage, due to increased handling during processing and stress from molding.

2.4.2. *Stress Concentrations*

Due to the possibility of open failures caused by mis-handling of Test Chip A, reliable data could not be obtained from the glob top units. Open failures might have gone undetected by the X-ray, thus eliminating the possibility of measuring electrical shorts at those locations. Nevertheless, it is clear from Figures 2.11-2.14 that the glob top offers a large reduction in die surface stress.

The data from Test Chip A confirms that the stress does indeed occur at the corner of the die. Figures 2.8 to 2.10 show that, in a given quadrant, the corner is more susceptible to failure with an increase in thermal cycling. In addition, we confirmed results obtained by S. A. Gee et al that the wider metal line traces will fail first.

These results support modeling data discussed in the first chapter where stress was observed to be greatest at the corners. Further failure analysis by S. A. Gee et al revealed that the passivation cracks originated from the corner of the metal lines. The wider lines served as a larger internal crack, allowing it to be more susceptible to further crack propagation. This relates directly to Griffith s criterion which indicates that the critical stress for failure is inversely proportional to the square root of the crack length.

Although the trend for failures at the corners is not well supported by the data from the glob top devices, the metal line width trend is supported by these devices. The lack of support for corner failure trends may be due to the fact that the glob top was successful in eliminating most of the die stress. It may also be due to other wire breaks that were not detected by the X-ray. Recall that when there is an open in the electrical circuit, resistance measurements would effectively go to zero, not allowing the detection of electrical shorts between the two metal lines.

2.4.3. *Glob positioning*

We completed a total of three experiments with three different test chips to determine the effects of applying the glob top on top of the die alone, versus on top of the die and DAP. Test Chips A and B reveal that, in terms of stress reduction on top of the silicon, there is no significant difference in these two variables. Test Chips B and C, show that there are more open failures observed in parts where the die and DAP contain the glob top. Globbing on the die only is actually preferable since it requires less glob top material.

The effects of the glob top on top of the die and DAP is best demonstrated by Test Chip C in Figure 2.19, showing that 50% of parts failed the electrical continuity test compared to less than 5% failure rate found in parts with glob top on the die only. The units not using glob tops showed 5 to 10% failure rate corresponding to the low and high stress molding compound.

Figure 2.19 indicates that almost all of the failures from the die/DAP glob top are observed after the post-mold process, before any additional stressing. In fact, the amount of failure did not increase even after temperature cycling. Furthermore, with a small amount of glob top over the tip of the ball bond, the gold wire may move during molding, relieving the stress on the wire. Furthermore, the large glob on top of the die and DAP restricted the flow of the molding compound as it entered the molding cavity. This created an additional stress on the wire, which made these units more susceptible to failure.

2.4.4. *Globbing materials*

We considered using two different globbing materials for our study, Glob A and Glob B. These two materials were chosen because they are widely used in the industry, and because their mechanical properties seem to match our needs. In addition, cost was a major concern in selecting these materials.

Table 2.3 shows some of the significant data taken into consideration in comparing the stress level on top of the die.

*Table 2.3: Comparison of mechanical properties is made between Glob A and Glob B liquid encapsulant. *The stress index is calculated by using the relationship given in equation 1.1.*

Properties	Glob A	Glob B
α(ppm)	19	13
Tg (C)	157	145
Filler content (%)	73	83
Viscosity (CPS @25 C)	65,000	295,000
E (psi)	870,000	1,190,000
Stress Index* (Eq. 1.1)	4506	3323

These materials had the same basic chemistry since they were formulated by the same company. However, one difference was in the percentage of filler content in the liquid encapsulant. Glob B had a higher filler content, which justified the higher viscosity, higher modulus, and lower CTE.

In looking at the stress index calculated for the residual stress on top of the die, we would expect that Glob A would have more failure than parts that used Glob B. However, both Test Chip A and Test Chip B revealed no observable difference in terms of interlayer dielectric cracking. Although Test Chip B revealed that Glob A had a greater percentage of open failures (Figure 2.15), it is regarded as an anomaly since it was not confirmed by the second Test Chip B experiment (Figure 2.17).

2.4.5. *Cure Temperature*

We also looked at the effects of different cure temperatures for the glob tops. We believed that better adhesion between the molding compound and glob top could be obtained when the glob is not fully cured in the first cycle. We partially cured the glob top at 125 C for 30 minutes. In this manner, both the glob top and the molding compound could post-cure together at 175 C for 4 hours. With some units, we cured the parts completely at the recommended cure temperature of 165 C for 90 minutes following the 125 C cure cycle. In addition to this motivation for improved adhesion, we also recognized that the higher curing temperature would experience a higher stress state when the parts were cooled during temperature cycling.

Our results from the second experiment of Test Chip B showed that the units that were not fully cured at 125 C had fewer shorting failures than the completely cured units (Figure 2.18). Although the difference was only slight, it may have been contributed by the fact that there was a lower intrinsic stress in units cured at 125 C. Figure 2.18 shows that all of the failures were attributed to temperature cycling, where the maximum stress was experienced at -65 C.

The open failure data in Figure 2.17 suggest that the curing temperature did not affect the adhesion between molding compound and glob top. If there were an adhesion issue, we would expect gross wire breaks due to the movements at the interface when the units are stressed. In this case, only two units failed out of 200 units that were tested. It appears that even a fully cured glob top offers sufficient adhesion to the molding compound. Furthermore, the effects of the cure cycles can be diminished because the globbed units continue to cure as they wait to be molded.

2.4.6. *Molding Compound*

One of the objectives of our study was to use a lower-cost molding compound to leverage the cost of adding the additional glob top on the die. We investigated an alternative molding compound known to have higher stress properties. This molding compound is indicated as MC2 in this thesis, while MC1 is the standard low stress molding compound used in the majority of the products today.

In almost every case, MC2 had more open and short failures with respect to MC1. Improvements in shorting failures confirmed that MC1 does apply less stress on top of the die. Figure 2.16 clearly shows that without the glob top, 100% of the device with MC2 failed. Only 18% of MC1 units failed without glob top. However, with the use of glob tops, the change in different molding compounds were no longer significant, as presented in Figure 2.16. The fact that the glob top reduced stress on the die is confirmed by Test Chip A as well as both experiments with Test Chip B. As expected and demonstrated, there does not appear to be a correlation between open failures and the use of different molding compounds.

2.4.7. *High Temperature Storage*

We performed a high temperature storage experiment with Test Chip B to determine whether the glob top material degrades after a 500-hours bake in 175 C. Due to the lack of time, the second experiment of Test Chip B only reached 300 hours of storage. There did not appear to be a significant contribution to failure by the high temperature environment in terms of opens and shorts. Only one sample failed after 500 hours of testing in Figure 2.15. However, as discussed earlier, this may not have been a well assembled experimental leg. At the raised temperature, we would not expect to see any shorting failures since the stress is actually reduced from room temperature.

Degradation of the glob top could cause open failures which we have not seen in significant numbers.

2.5. Summary

We looked at several different variables in developing a process to reduce stress on top of the die. Our goal was to eliminate failures due to interlayer dielectric cracking. The three test chips were valuable in confirming some of our data. In addition, the use of different chip sizes and packages assured that we could cover a broad range of devices. It is clear from our results that the glob top was successful in reducing stress on top of the die surface. We will conclude this chapter by reviewing the significant results we obtained from this portion of the research.

We found that the glob tops can reduce stress on the die even when a high stress molding compound is used as an overmold. This is extremely significant because it allows us to leverage the cost of adding the glob top by using a less expensive molding compound. Since a large amount of molding compound is used in proportion to glob top material, we may possibly save money by using a glob top in addition to a low cost molding compound. This eliminates the need for very high cost, low stress molding compound.

One issue of concern which was observed in many of the tests, was the number of wire breaks in the units after molding. Most of these failures are likely contributed to the fact that the molding parameters were not optimized for each of these parts. The facilities where this research was performed was not optimized for productions. The control of the molding compound flow is extremely significant in getting high yields on reliable parts. Although processing parameters may not be optimized, it appears that the parts with glob tops spreading out to the DAP were more susceptible to wire breakage. This matter requires further investigation in a more controlled molding environment.

It is clear that glob tops offers improved reliability where stress on the die is a major issue. We recommend that further tests be done using glob top on the die only in combination with the higher stress molding compound. Test Chip B can be expanded to be used as a larger die by placing it in a larger package as a 2 x 2 or 2 x 1 matrix. This will allow us to use this test chip for different packages.

Chapter 3

Electroless Capping Results

3.1. Introduction

In addition to using glob tops to prevent dielectric cracking on the die, we examined protecting the exposed aluminum bond pads against corrosion and detrimental intermetallics. An electroless plating process was chosen as a barrier metal because it is a simple and inexpensive process. Electroless plating is a selective deposition process that does not require the a masking and an etching step. Since nickel tends to form an tenacious oxide, making it difficult for bonding, we used a flash of gold to protect it against oxidation.

Nickel and gold are widely used to protect aluminum and copper against corrosion in printed circuit boards. However, the use of plating on bond pads at the wafer level is currently being explored. We will address some issues that are specific to this application. This chapter will first present background information on the plating process. Next, we will give further details on the experimental set-up before presenting the results. We will then discuss the significant results and accomplishments achieved in this research.

3.2. Background

This section provides a slightly higher level of detail into the plating process. However, we can not disclose some details that are not made known by our plating chemical suppliers. We will also discuss some mechanisms that allow selective plating on top of aluminum wire bond pads. A device is first cleaned and activated before it is subjected to a series of plating baths.

3.2.1. *Activation*

Devices to be plated are first cleaned with a mild acid to remove fingerprints, grease, or dust that may be present during handling. Furthermore, aluminum requires special treatment prior to plating since the aluminum forms an impervious oxide film instantaneously[19]. The oxide layer inhibits the plating potential of the electroless metal.

A typical activating bath contains zinc oxide, sodium hydroxide, metal salt ($FeCl_3$), and a complexing agent (tartrate). The tartrate removes the oxide and slightly etches the aluminum substrate to forms a thin layer of zinc to prevent aluminum oxidation. Soak time and zincate concentration play a major role in optimizing the aluminum surface for subsequent electroless plating. The smooth, well adherent zincate will often yield a more adherent, fine grained nickel.

The behavior of the zincate will depend on the electrochemical potential and surface topography of the aluminum substrate. In the case of microelectronics devices, aluminum bond pads are connected to different layers in the silicon, often yielding bond pads of different electrochemical potential. In production, various process can yield aluminum with different copper and silicon doped into the sputtered surface. After zincating, the parts are thoroughly rinsed and prepared for plating.

3.2.2. *Plating Baths*

When placed in the first plating bath, nickel replaces the zinc then plates catalytically. After nickel is plated to the proper thickness, the sample is rinsed thoroughly in distilled water. We can proceed with the next plating bath. In this case, we plate with an immersion gold since it can provide adequate oxidation protection. Table 3.1 gives some typical elements and solutions found in these plating baths.[19]

Table 3.1: Some typical contents of electroless plating baths and its purposes.[19]

Zincate (Alkaline)	ZnO (0.1)	Stops further Al oxidization
	Sodium, Potassium Hydroxide (0.88)	Forms complex: $Zn(OH)_4^{-2}$
	Ferric chloride + potassium hydrogen tartrate	Etch Al Oxide and slightly etch Al
Electroless Metals	Nickel sulfate, or Cyanoaurate, or Thiosulfate-Au	Metal salt providing metal ions to be plated
	Sodium hypophosphite Sodium boride	Reducing agent for heterogeneous interface (boron and phosphorous based)
	Lactic acid	Complexing metal ions to prevent bulk decomposition
	Sodium hydroxide	Insure optimum pH for plating rate and deposit composition
	Thiourea	Stabilizer to insure greater homogeneity

3.2.3. *Plating Mechanisms*

Selective deposition in the case of electroless plating occurs when there is a significant difference in electrochemical potential between the depositing surface in equilibrium with the ionic solution. For example, when plating on aluminum bond pads, the deposition process is highly favorable at the chemically active aluminum against the chemically inert dielectric and passivation surfaces such as silicon dioxide, silicon nitride, and polyimide[14]. There are two basic mechanisms associated with electroless plating, displacement and autocatalytic reactions. The overall reaction of electroless metal deposition is given as[20]:

$$\text{Metal}^{Z+}{}_{\text{solution}} + \text{Red}_{\text{solution}} \xrightarrow[\text{Catalytic surface}]{} \text{M}_{\text{latice}} + \text{Ox}_{\text{solution}} \qquad [3.1]$$

One electroless plating mechanism is associated with the displacement of the existing metal to plate the new metal layer. In the case of selectively plating nickel on the zincated aluminum surface, nickel in solution dissolves the zinc on the surface of the aluminum. A small amount of aluminum is displaced as nickel initially plates on top of the aluminum. When the nickel layer is sufficiently thick, it can no longer displace the aluminum layer. Therefore, a reducing agent is needed in the nickel plating solution. In this experiment, we used sodium hypophosphate as the reducing agent. As a result a certain percentage of phosphorous is deposited along with the nickel.

When we have achieved a desired thickness to provide adequate environmental protection of the bond pad, we plate a thin layer of gold. This solution is self-limiting because it does not have a reducing agent to provide the electron for the reaction to continue. As a result, we can only achieve a flash of gold. However, it is sufficient in preventing oxidation that would inhibit wire bonding.

3.3. Experimental Procedures

The electroless plating process is relatively simple and has been for some time. We identified some typical baths used in the industry. This process would be implemented after the wafer fabrication process, and before the assembly process. The previous section discussed the general set-up and requirements in electroless plating. Since our facilities could not support the chemical processes, we used an outside source to provide the plating services for these initial evaluations. We would take the plated parts to assemble and to perform environmental tests. In this section, we will describe our capping structure and metallurgy, environmental testing conditions, and analytical techniques.

3.3.1. *Capping Structure and Metallurgy*

We selected electroless nickel as our choice of barrier metal to protect the bond pad because it is relatively inexpensive and is believed to resist corrosion and intermetallics formation. We set a target for 7 to 10 μm nickel barrier layer thickness to adequately seal off the aluminum bond pad to improve corrosion resistance. Figure 3.1 shows a typical cross-section of a gold wire bonded to a nickel capped aluminum pad.

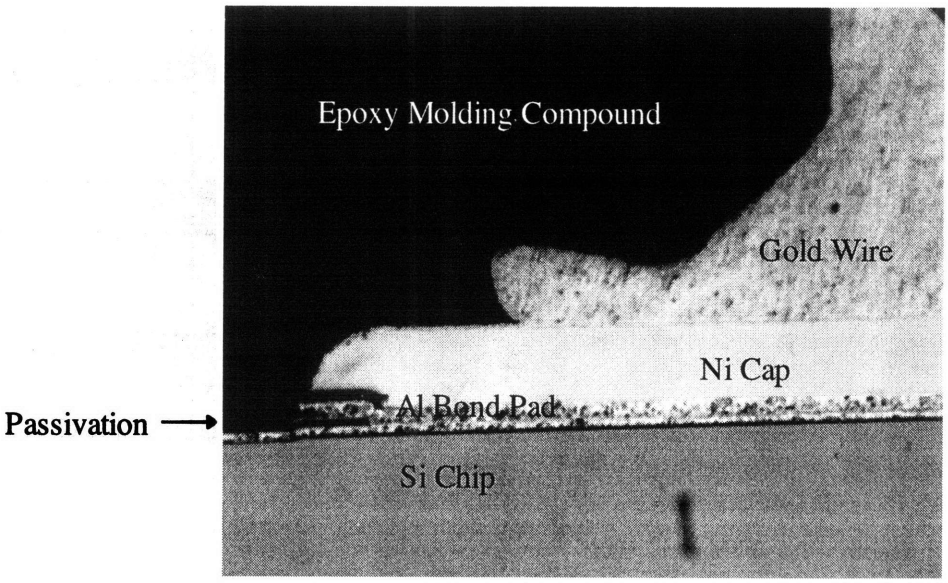


Figure 3.1: Actual cross-section of a 10 μm nickel cap on aluminum bond pad. A gold wire bond is situated on top of the pad.

The goal of our research was to present possible solutions to improve robustness of the silicon device. We did not have the adequate facilities to optimize the process to achieve better control. Table 3.2 summarizes the process flow and parameters used by a vendor in providing the plating services.

Table 3.2: Process used by an outside source to plate electroless nickel with flash of gold. Deposition rate is provided where applicable.

Process	Description	Temp. / Time	Deposition Rate (µm/min.)
Pre-clean treatments	Degrease, promotes wetting	25 °C / 1 min.	
DI H_20 Rinse			
Zincate	Strips aluminum oxide, prevents further oxidation	25 °C / 1 min.	
DI H_20 Rinse			
Ni Barrier	Electroless Ni with 4.8 pH	88 °C/ as needed	0.25
DI H_20 Rinse			
Au Flash	Immersion Au exchanges 2 mole of Au for 1 of Ni	88 °C/ as needed	.075-.125 in 15 minutes
DI H_20 Rinse			
Dry			

3.3.2. *Environmental Tests*

After plating, we proceeded to wire bond gold to the Ni/Au plated aluminum bond pad. We performed tests that would allow us to detect potential problems without losing too much time. On these initial tests, we did not run a full standard qualification because an operational device was unavailable. We used electrically failed devices and Test Chip C to evaluate the process. Recall from the previous chapter that Test Chip C consists of wire bond pads shorted to one another by a daisy chain. Two failure modes we looked for in this experiment were corrosion and intermetallic induced failures. To save even more time in this development stage, we did not fully assemble the device where electrical testing was not needed. These units where tested after the wire bond stage, where the die is still exposed to the

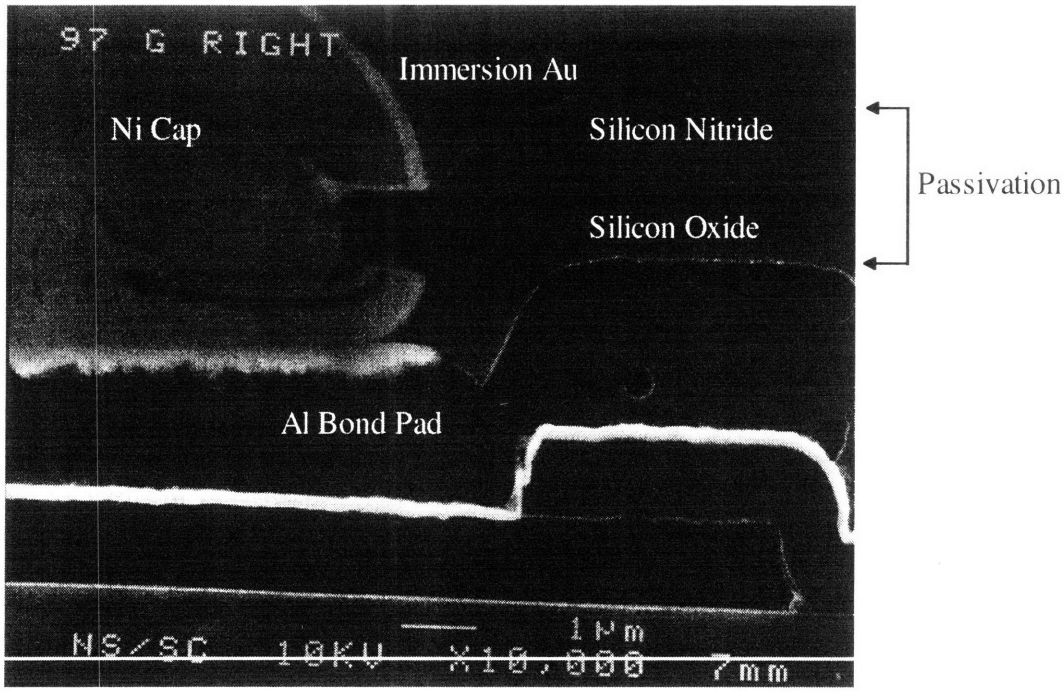


Figure 3.3: Cross-section of a typical bond pad showing the electroless nickel and immersion gold serving as a cap to protect the aluminum underneath.

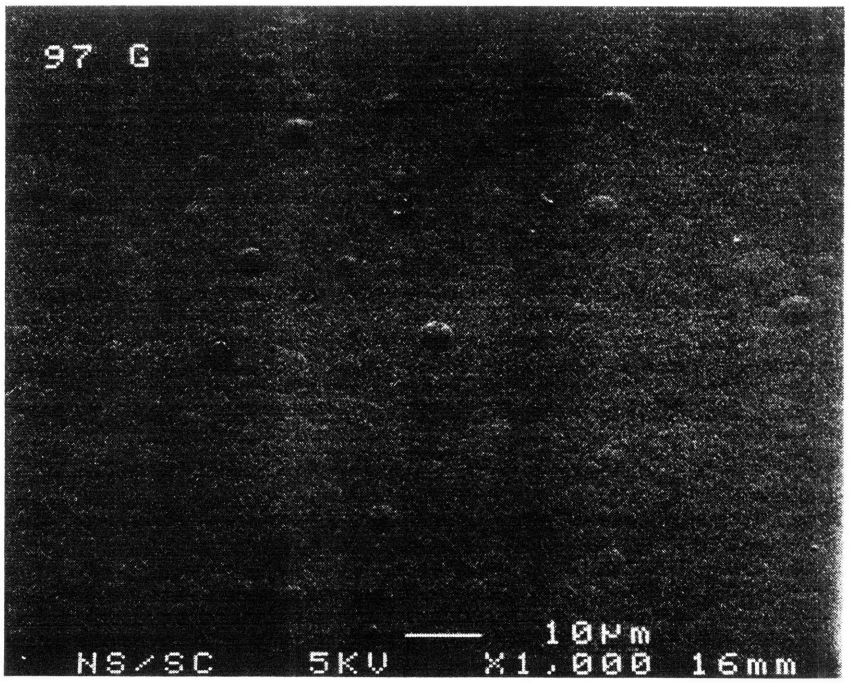


Figure 3.4: Topography of nickel/gold surface. The physical features of the nickel and gold follow that of the aluminum bond surface. The small bumps are contributed by the Cu nodules in the aluminum.

3.4.1. Bond Pad Structure Evaluations

We used SEM and high powered microscopy to check the bond pads for plating uniformity and to obtain initial reliability information. A few iterations were performed before achieving the pad structure desired to serve the capping needs. Several factors in the plating bath play a role in obtaining a uniform plating layer. However, since these initial evaluations were not done in our facilities, it was difficult to quantify the effects of plating. This section will first characterize the structure of a well plated bond pad. Next, we will look at the effects of a bond pad with problems in the activation process. Finally, we will observe some potential reliability problems.

3.4.1.1. Standard Nickel Capped Bond Pad

First we will show the structure of a typical bond pad that has been capped with nickel and a gold flash. Figure 3.3 and 3.4 show a cross-section and top view of a bond pad as seen under SEM. The Al appears to be sealed off from the outside environment by a relatively uniform plating. The small nodules result from the Cu nodules in the Al bond pad.

3.4.1. Bond Pad Structure Evaluations

We used SEM and high powered microscopy to check the bond pads for plating uniformity and to obtain initial reliability information. A few iterations were performed before achieving the pad structure desired to serve the capping needs. Several factors in the plating bath play a role in obtaining a uniform plating layer. However, since these initial evaluations were not done in our facilities, it was difficult to quantify the effects of plating. This section will first characterize the structure of a well plated bond pad. Next, we will look at the effects of a bond pad with problems in the activation process. Finally, we will observe some potential reliability problems.

3.4.1.1. Standard Nickel Capped Bond Pad

First we will show the structure of a typical bond pad that has been capped with nickel and a gold flash. Figure 3.3 and 3.4 show a cross-section and top view of a bond pad as seen under SEM. The Al appears to be sealed off from the outside environment by a relatively uniform plating. The small nodules result from the Cu nodules in the Al bond pad.

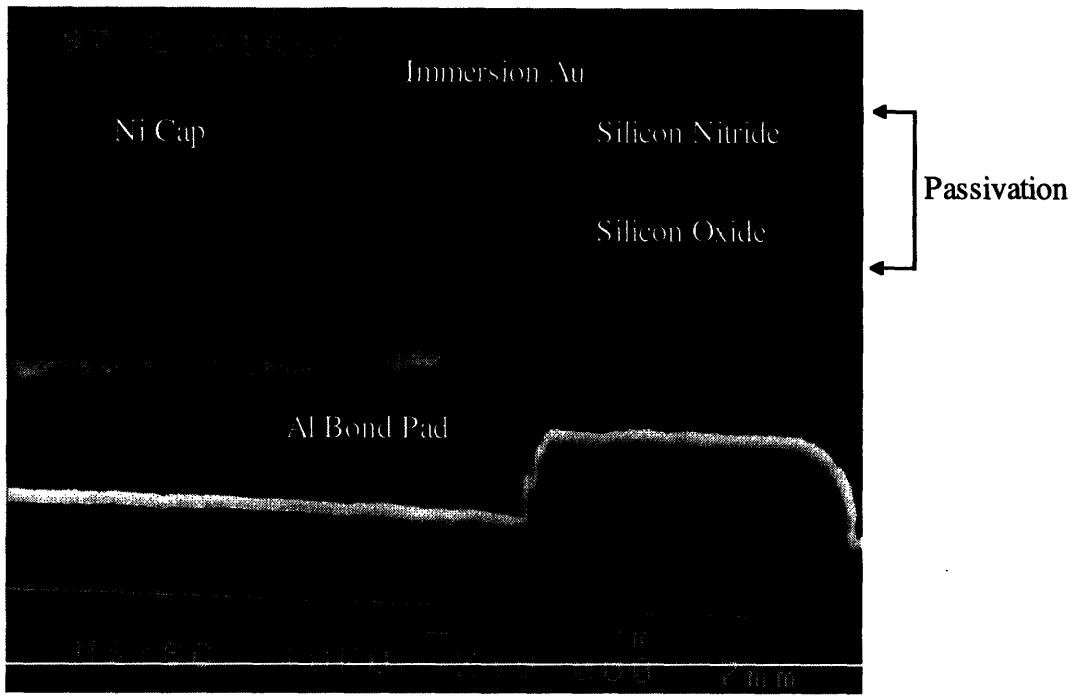


Figure 3.3: Cross-section of a typical bond pad showing the electroless nickel and immersion gold serving as a cap to protect the aluminum underneath.

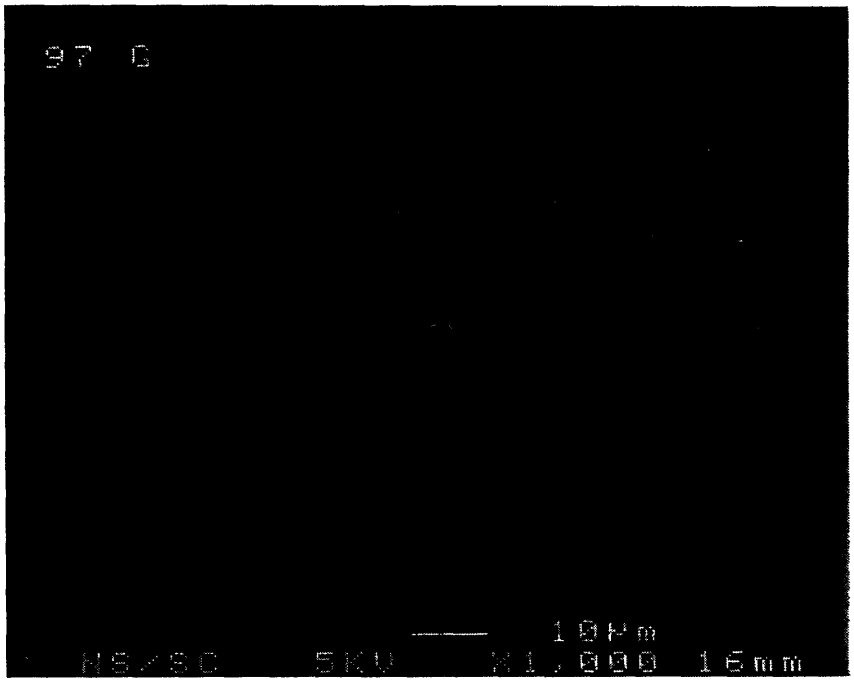


Figure 3.4: Topography of nickel/gold surface. The physical features of the nickel and gold follow that of the aluminum bond surface. The small bumps are contributed by the Cu nodules in the aluminum.

3.4.1.2. Activation Issues

The pretreatment steps were varied to obtain the best plating results for these wafers. Traditionally, an alkaline cleaner was used, followed by a 50% nitric acid dip to remove residual dirt or grease. However, in our specific application, these aggressive cleaners were not necessary since wafers were generally kept clean. Since the thickness of the aluminum is only 2 μm, an aggressive cleaner will completely remove the aluminum in a short amount of time. We substituted these cleaning steps with a 10% citric acid dip to aid in the wetting of the zincate. Comparable results were obtained with this modification.

After observing that the Al-0%Cu bond pads did not plate evenly, we looked closely at the bond pad structure to determine the cause. The SEM micrographs in Figure 3.5 and 3.6 show the top view and cross-section of the bond pad. The micrographs reveal that the zincate was too aggressive for the Al-0%Cu bond pads. The Al-0.5%Cu and Al-2%Cu bond pads, on the other hand, did not experience this problem.

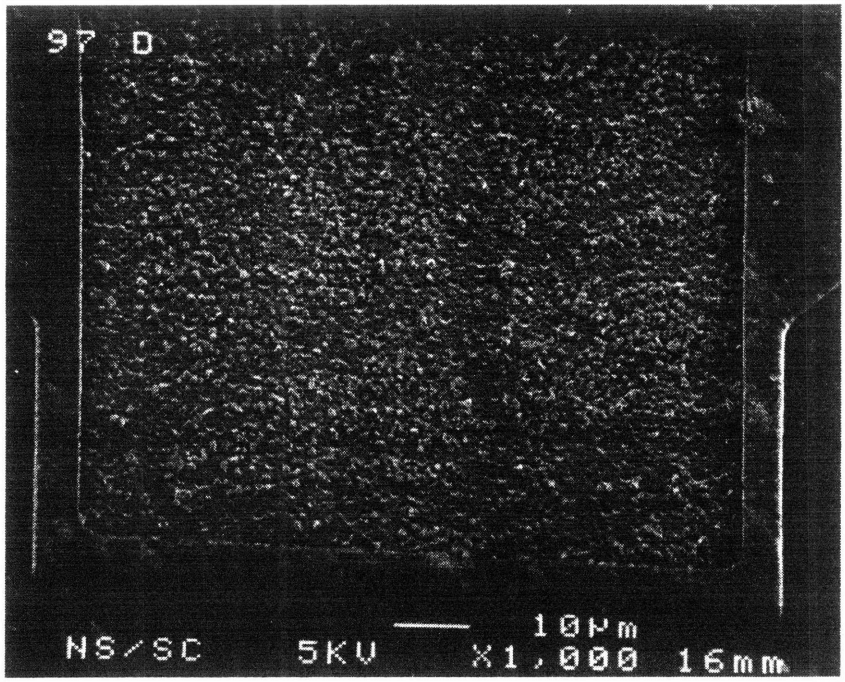


Figure 3.5: Top surface of an aluminum bond pad shows that the aluminum is almost completely etched out by the zincate. The residual zinc is left on top of silicon after the aluminum is etched.

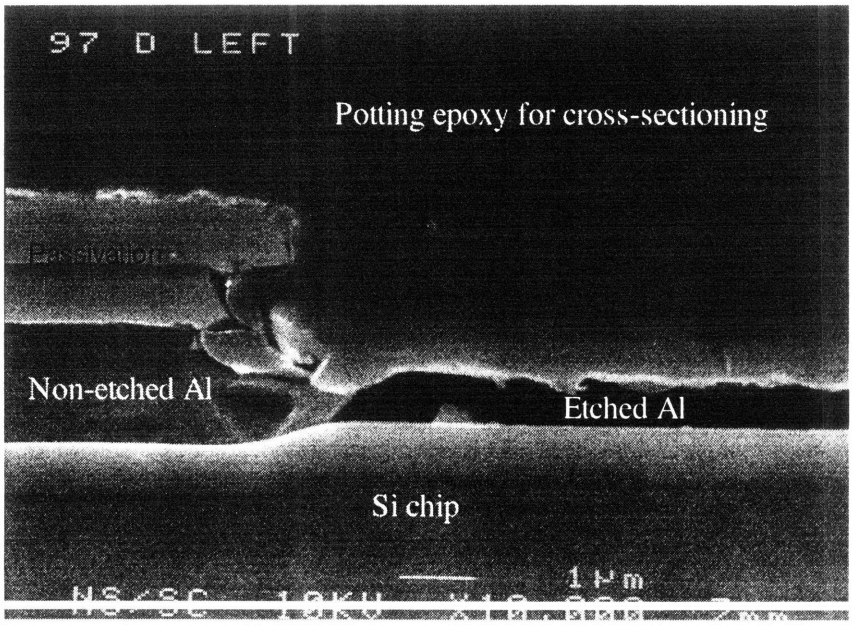


Figure 3.6: Cross-section micrograph confirms that the aluminum not protected by the passivation is etched away in the zincating solution.

Furthermore, we observed that the zincate aggressiveness is also dependent on the functions of the bond pads. Even on Al-2%Cu bond pad, we see non-uniformity in the different bond pads after zincating as shown in Figure 3.7. However, Figure 3.8 indicates that when the subsequent metal is deposited, this variation is not as apparent. These micrographs show that uniformity is greatly affected by the initial clean and activation process.

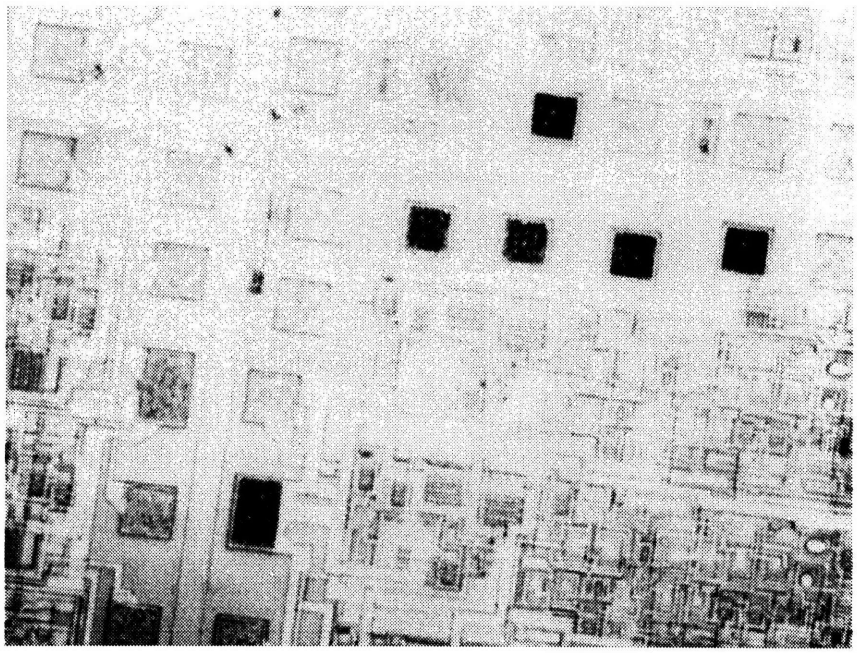


Figure 3.7: Non-uniformity of Al-2%Cu bond pads are indicated following the zincate process. Each pad connects to different metallurgy in the silicon.

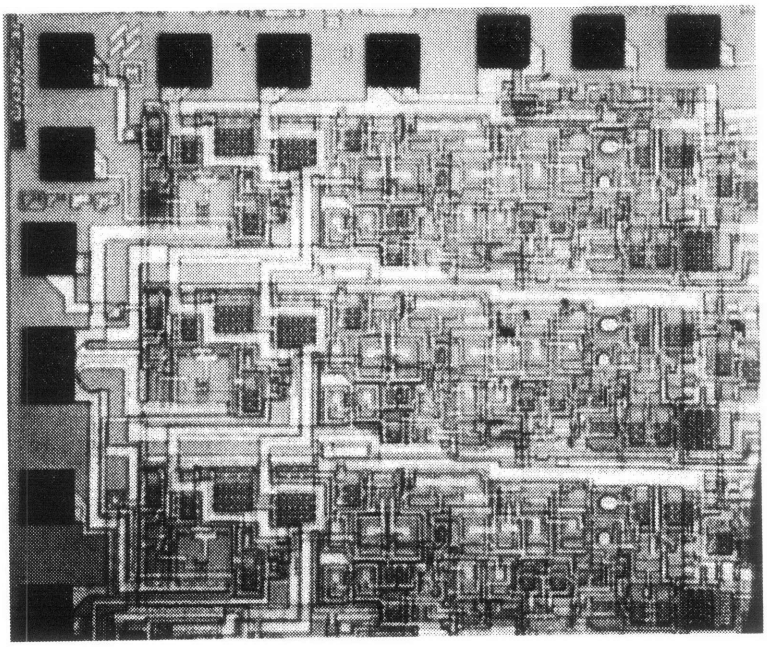


Figure 3.8: Pads plated to approximately 6 μm do not show drastic variations from one bond pad to the next.

3.4.1.3. Corrosion

We performed initial reliability experiments to determine the corrosion resistance of the nickel cap. Several tests were done to observe the bond pad caps. Although these tests are not standard, they provide a good general idea of how these parts will perform.

We first tested the chemical resistance of the nickel cap by dipping the bonded parts in concentrated HCl for five minutes, followed by a DI water rinse. Initially, it appeared that both the aluminum pad and nickel capped parts were not affected. However, after one month of air time, corrosion took place in the aluminum. Figure 3.9 reveals that the aluminum is almost completely etched away while Figure 3.10 indicates that corrosion is initiated only at the corners and edges.

Figure 3.9: Aluminum bond pads subjected to 5 minutes of concentrated HCl dip and 1 month of air time. The underlying oxide structure is exposed where the aluminum is etched.

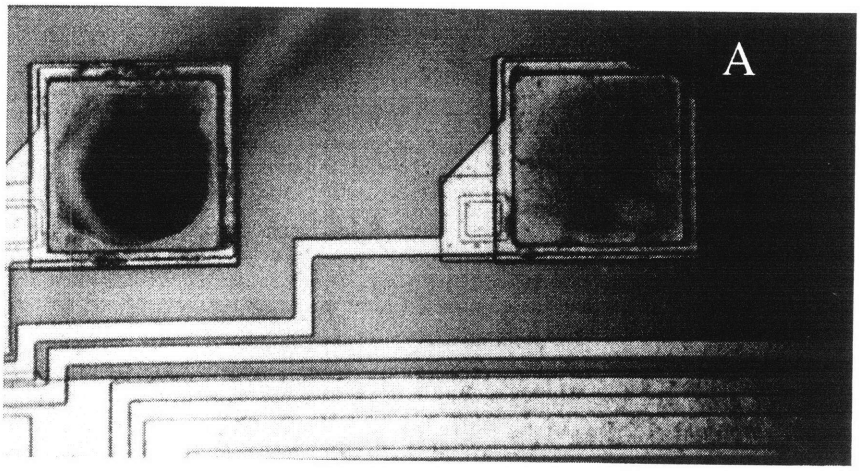


Figure 3.10: Nickel/Gold cap improves resistance to chemical attacks. Marker A indicates the corrosion at the corner. These devices were placed in concentreated HCl for 5 minutes and in air for 1 month.

In addition, we tested the steam resistance of the nickel caps. Unencapsulated units were placed in the moisture autoclave (ACLV)

chamber in 121°C at 2 atm. The nickel/gold caps came off of the aluminum substrate after the 24 hours in the ACLV, while the standard aluminum parts remained intact. Figure 3.11 shows the Ni cap delaminated from the Al pad. The nickel barrier does not seem to perform well against direct steam pressure.

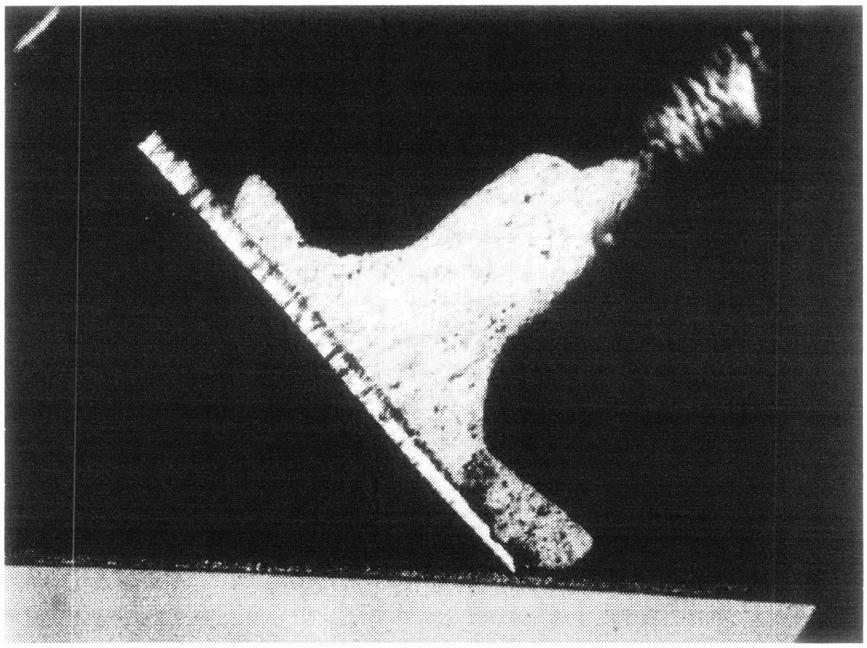


Figure 3.11: When placed in 121 °C at 2atm pressure for 24 hours, the Au wire bond and Ni cap lift off from the aluminum bond pad. Failure occured between the aluminum and nickel interface. An epoxy based potting material was used to keep the wires in place for cross-sectioning.

When we fabricated thick Ni/Au bumps of about 28μm, good adhesion was obtained even when the bare die was exposed to 66 hours in the ACLV chamber. The shear strength actually increased slightly after ACLV from 251 ± 9 gm force to 259 ± 8 gm force for a 110 μm square bumps. Figure 3.12 shows the sheared and non-sheared bump after ACLV. The photographs reveal some contamination on the surface of the die which may be from the residual plating chemicals.

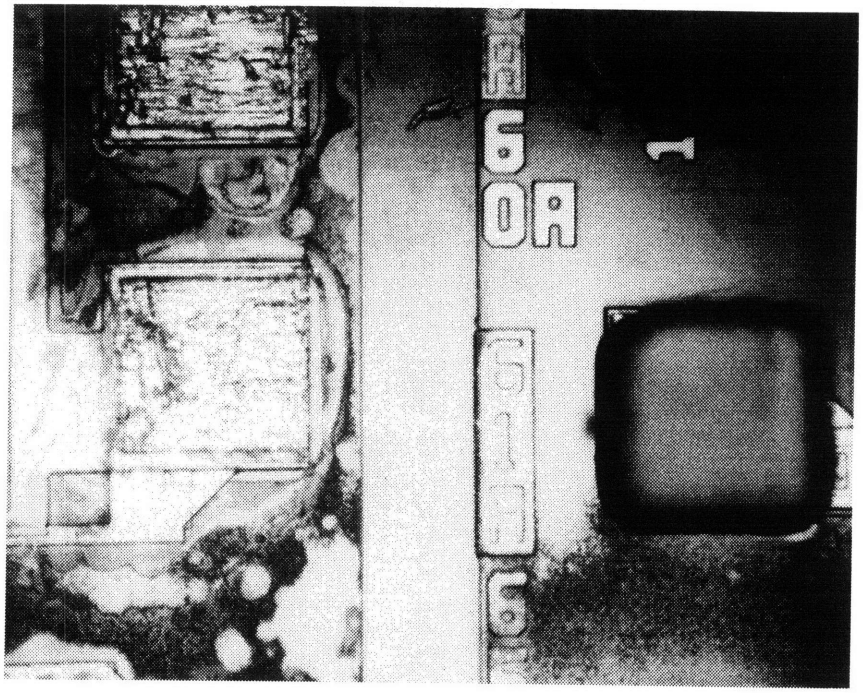


Figure 3.12: The right side shows an unsheared 28 μm bump. The left side shows the Ni fracture surface left as a result of the bump shear. Note that the Ni to Al adhesion is stronger than the bulk fracture strength of the electroless nickel.

The nickel cap seems to succeed in protecting the aluminum against corrosive chemicals that form due to impurities in the molding compound reacting with the surrounding moisture. However, the electroless nickel did not stand up well against direct steam pressure. We will later discuss the effects of the autoclave test in encapsulated test devices.

3.4.1.4. High Temperature Storage

We performed cross-sections of the aluminum pads bonded with gold wires at various high temperature storage temperatures. It should be clear that the intermetallics get progressively worse at higher temperature and longer time. Figure 3.13 shows the Al/Au intermetallics at 200 °C for 350 hours. Almost all of the aluminum is consumed by the gold in this case. When the nickel barrier is present, no change can be seen under the high temperature storage. We will look at the strength of these intermetallics in the next section to determine if it affects reliability performance.

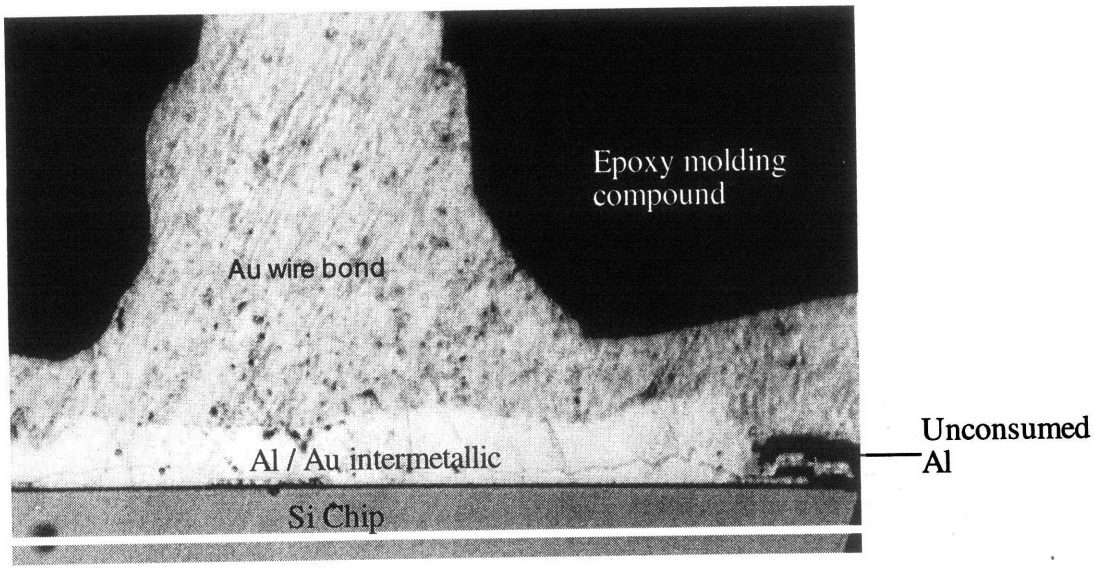


Figure 3.13: Al/Au intermetallics are present in the bond pad without a nickel barrier metal. All of the aluminum seems to be consumed where it is in contact with the gold wire bond. This sample was exposed to 200 °C for 350 hours.

3.4.2. *Mechanical Testing*

Mechanical data for evaluating the nickel cap were obtained by performing wire pull and ball shear tests on the samples before they are encapsulated with epoxy. After the baseline data was collected at 0 hour, we subjected the parts to various high temperature storage conditions to confirm its high temperature stability with respect to standard gold bond on aluminum bond pads. An example of ball bond shear and wire pull results are published by Harman in Figure 3.14[21].

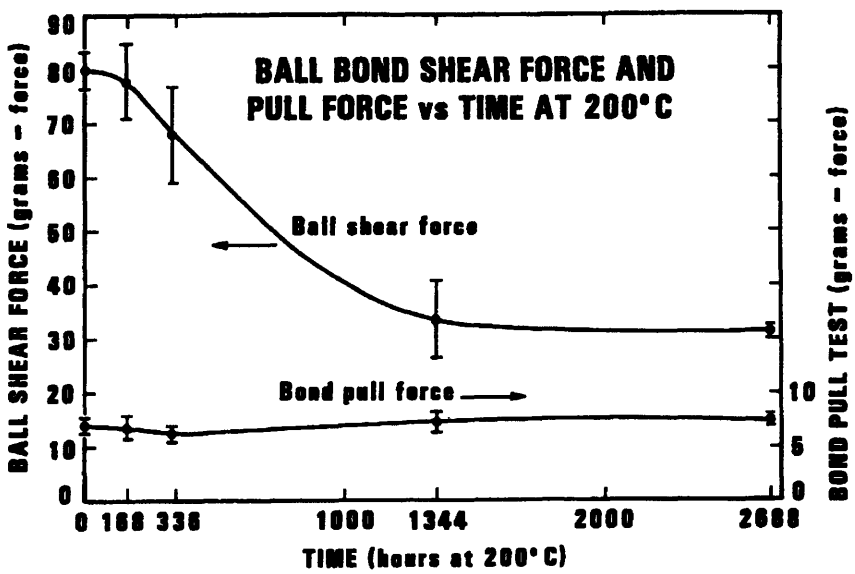


Figure 3.14: Data published by G. Harman showing the degradation of ball shear force as a function of time in 200 °C atmosphere. Note the change of scale from shear force (left) to pull force (right). (Sourc: Harman et al)

3.4.2.1. Wire Pull Test

We performed the wire pull tests on units after bonding to determine the amount of gold wire bond that did not bond to the Al pad. If there are no problems with the bonding, we would normally see the wire breaking at the shoulder immediately on top of the ball bond. The maximum pull force required to break the gold wire is typically in the 10 gm range. There is an indication of bonding failures when the wire pull data drops below the typical values. We investigated these failure locations by looking to see if the ball had lifted as a result of poor bonding.

In this experiment, we performed at least 40 wire pulls for the three conditions listed in Table 3.3 below. The standard aluminum bond pad is compared against two different electroless Ni plating solutions, the Ni low phosphorous and Ni mid phosphorous cap. The first bath yields 2-3% phosphorous, and the second bath yields 8-10% phosphorous. The failure percent is given as the percentage of wires that failed to make good bonds with the capped and non-capped wire bond pads.

Table 3.4: Bond pull result shows the percentage of bonds that failed at the bonding interface instead of at the wire. The average strength is given, corresponding to the bond failures. An average force of 10.5 grams was required to break the gold wires.

	Failure percent	*Pull force*	Failure percent	*Pull force*	Failure percent	*Pull force*
	1.3%	*9.0*	2.5%	*10.3*	2.5%	*9.5*
	0.0%		0.0%		0.0%	
	3.8%	*5.8*			10.0%	*2.5*

The data from Table 3.4 indicate that the Ni-8%P experienced no bonding failures through the different environmental conditions. The standard Al bond pad reveals a small amount of bonding failures. However, the pull force was relatively high, almost that of the maximum force measured by the non-failed parts. The Low Phos Ni Cap data shows some potential problems in bonding. It reported the highest percent of bond failure with the lowest measured pull force. This situation is amplified after the parts are soaked in 85 °C/85% relative humidity (RH) chambers. Due to the fact that the wire pull test can only measure up to the strength of the gold wire, we needed a method to mechanically measure the bonding site directly. Hence, we used the bond shear to make additional mechanical measurements.

3.4.2.2. Bond Shear

We performed numerous ball bond shears on parts under high temperature storage testing. To accelerate failures, we used temperatures greater than the normal operating temperatures. Four different temperatures where chosen between 175 °C to 300 °C. Shear strengths were measured at

different time points to observe the time to failure. We compared the performance of the standard aluminum bond pads against the low phosphorous (2%) Ni cap and mid phosphorous (8%) Ni cap.

Figures 3.15-3.18 shows the results after different temperatures soak temperatures. The shear data was obtained at room temperature, after the parts were cooled from the high temperature storage. These results indicates that not enough time has passed to induce failures in the Al-Au intermetallics. None of the units experienced a dramatic drop in shear strength. In fact, most of the mid phos Ni caps indicate an increase in shear strength with respect to time and temperature.

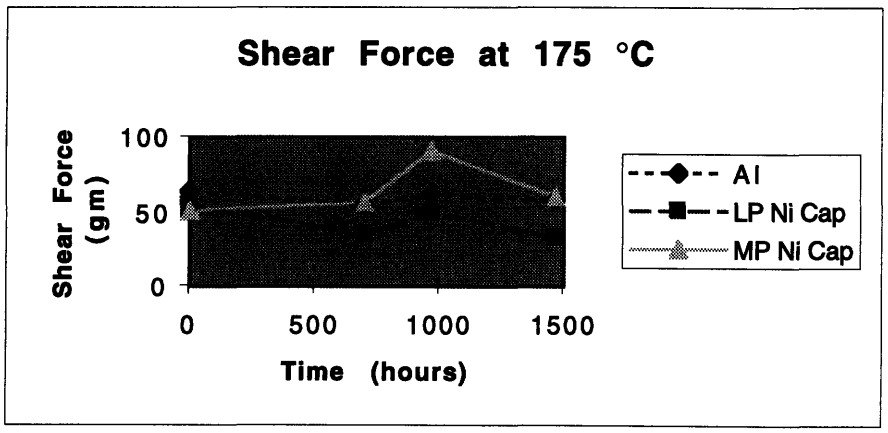


Figure 3.15: Shear force measured at room temperature after 175 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). The shear strength of mid-phosphorous Ni cap is slightly higher than the others at the 1000 hour time point.

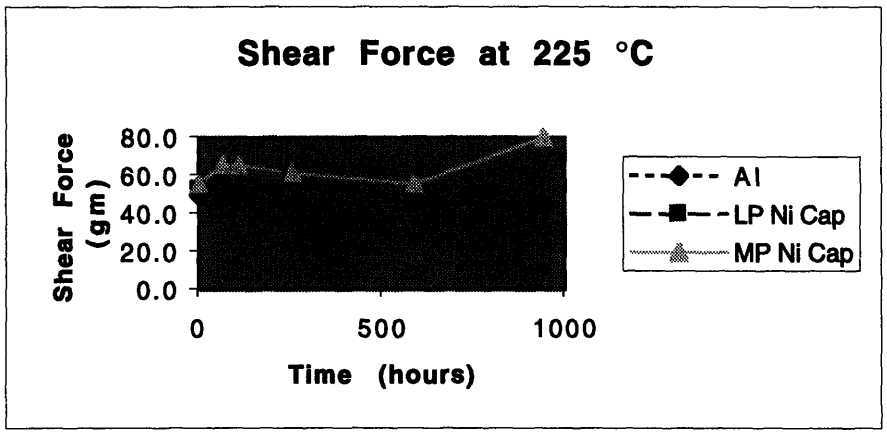


Figure 3.16: Shear force measured at room temperature after 225 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 225 °C shows a sharp increase in the mid phos Ni cap after almost 1000 hours of heat treatment.

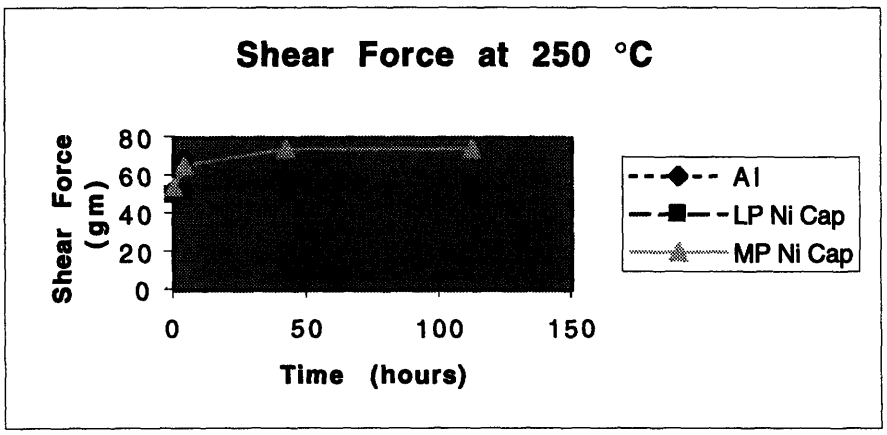


Figure 3.17: Shear force measured at room temperature after 250 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 250 °C shows an increase in the Ni capped units while the standard Al bond pad exhibits a drop in shear strength after 48 hours.

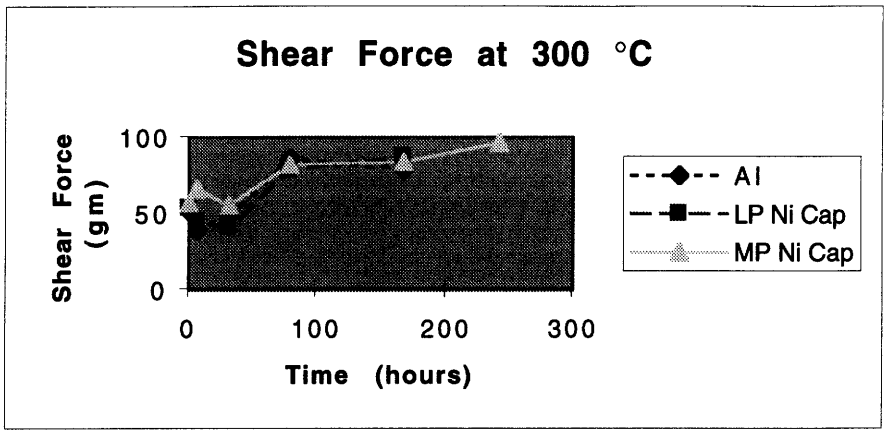


Figure 3.18: Shear force measured at room temperature after 300 °C soak for different time points. (Al: standard Al bond pads, LP: Ni-2-3%P, MP: Ni-8-10%P). Shear force at 300 °C does not distinguish between the different variables. Shear strength increases sharply after 4 hours.

The average standard deviation for shear testing these units are approximately 8 gm. Twenty to thirty shears were made at each time point. In a few cases shown in the figures above, the increase in shear strength is dramatic with respect to time. Other cases show that no distinctions can be made between the capped and uncapped units. The data set at 250 °C shows that the Mid Phos Ni cap increases in strength while the standard aluminum connections dropped in shear strength with increasing time.

3.4.3. Electrical Testing

Several experiments were run with unencapsulated silicon devices to obtain fast results at the beginning of our research program. As time progressed, we completely molded the test devices to evaluate them under standard preconditioning procedures and environmental stresses. Table 3.5 summarizes the results we obtained from the electrical testing. The shading in the cells help to identify the stage at which the packaging fails to protect the device.

Table 3.5: Electrical Testing data are summarized below. The degree of failure is simplified by a 0 to 4 code (0 = no failures, 4 = gross failures). Failure is indicated for the standard aluminum bond pads and the nickel capped bond pads at various conditions.

Environmental Conditions	Aluminum	Mid Phos Nickel Cap	Low Phos Nickel Cap
TMCL 500 cycles	0	0	0
TMCL 1000 cycles	0	0	0
HTSL 66 hours	0	0	0
HTSL 330 hours	0	0	0
HTSL 500 hours	0	0	0
TMCL 500 cycles	0	0	0
ACLV 500 hours	0	0	1
TMCL 336 cycles	0	0	1
TMCL 30, 85°C/30% RH, 220°C IR	0	0	0
ACLV 72 hours	3	3	3
TMCL 30, 85°C/30% RH for 168 hrs, 220°C IR	0	0	0
TMCL 500 cycles	0	0	0
ACLV 72 hrs			
TMCL 30, 85°C/85% RH for 168 hrs, 245°C IR	3	0	0
ACLV 96 hrs			
ACLV 96 hours	1	1	1
245 °C IR	1	1	0
TMCL 500 cycles	1	1	0
ACLV 72 hours			

TMCL: Temperature Cycling (-65 °C to 150 °C)
ACLV: Autoclave (121 °C at 2 atm)
HTSL: High Temperature Storage Life (175 °C bake)
IR: Reflow furnace to simulate surface mount assembly

Table 3.5 shows that the ACLV test causes the most failures when followed by preconditioning stressing. When the parts are placed in the ACLV immediately after molding, we do not observe failures even after 500 hours. However, when preceded by preconditioning, we see gross failures across the board. The data shows that there does not appear to be any discrimination between the aluminum bond pads or the Ni capped bond pads. The only condition when we see moderate failures only in the aluminum bond pads and not in the capped bond pads is in the most rigid preconditioning test (85 °C/85% RH, 245 °C IR). The electrical data do not seem to be affected by the high temperature storage test or the temperature cycling test.

3.5. Discussions

It is evident from the results obtained in this research that there is potential for the electroless caps in specific applications. However, further investigations are required to fully understand the nature of the existing failures. In this section, we will focus on a few key issues observed in our results.

3.5.1. Plating Uniformity

From a processing point of view, it is crucial that we can achieve a consistent cap height at a production level. Our experiments show that some factors play an important role in defining the plating rate and uniformity. In addition to standard plating processing controls such as temperature, chemical stability, and rate of agitation, we have observed that variations in the silicon device can affect the plating rate. Figure 3.7 indicates that the zincating rate depends on the function of the device. Variations in zincating

may affect the subsequent nickel plating. However, in this case, Figure 3.8 shows that the final thickness was not affected.

Reports confirm that this problem is seen in the ground pads where the aluminum traces connect directly to the silicon substrate. This affects the electrochemical potential of the specific pad. We have heard of a report from the Technical University of Berlin where this problem was solved by passivating the back side of the silicon to isolate it from contacting the ions in the plating solution[22].

In addition to plating variations due to different bond pad electrical configurations, we observed different plating capabilities dependent on the impurities and alloys in the aluminum bond pad. Copper in the aluminum reduces the electrochemical potential of zinc to aluminum. This allows the zincate to be mild enough so that it would not completely etch away the aluminum as seen in Figures 3.5 and 3.6. In fact, we were unable to properly activate the pure aluminum bond pads for evaluations. This is not a significant concern at this point since most of the devices are migrating towards copper doped aluminum bond pads for improved electrical characteristics.

3.5.2. High Temperature Resistance

Our results show that the nickel barrier was successful in preventing detrimental intermetallics between gold and aluminum. In all of the different temperature storage conditions, the mid phosphorous nickel (8-10%) consistently yields higher shear strength. The low phosphorous nickel (2-3%) yields results similar to the aluminum. Although we did not have enough time to obtain data at longer time points, we expect the shear strength for the standard aluminum bond pad to drop off as the intermetallic phases continue to develop. Comparing Figures 3.1 and 3.13, we see that there is a drastic change in the capped units compared to the non-capped unit. We will discuss how nickel could be use as an effective intermetallic barrier.

3.5.2.1. Diffusion Rates

The nickel-gold electroless cap offers a barrier against the rapidly diffusing gold in aluminum. The diffusion coefficient of gold in aluminum is about an orders of magnitude greater than the diffusion of nickel in aluminum calculated at 200 °C. The diffusion of nickel in gold is about seven order of magnitude slower.[23] Although nickel appears to be a good barrier for the rapidly diffusing gold, there appear to be a possibility of Al-Ni intermetallics formation.

3.5.2.2. Aluminum-Nickel Intermetallics

Numerous studies have been done on the aluminum-nickel system. Colgan has reviewed the thin-film investigations of nickel aluminide intermetallic formation. The Al_3Ni phase was identified as the initial phase formed between 250 and 275 °C. The formation is based on the kinetics of aluminum as the dominant moving species. He also reported that growth will be laterally uniform or it may proceed preferentially along grain boundaries.[24]

In the case of electroless nickel with phosphorous, Kwang-Lung Lin's study showed that no observable intermetallic interface was observed even after 900 hours of heat treatment. Ni and Al were not seen to coexist with each other.[25] Nickel has limited solubility in Al, at only .01 atomic per cent at 500 °C;[26] whereas, Al is much more soluble in Ni.[27] Although Ni_3Al could normally be formed under proper conditions, results in Kwang-Lung Lin's study indicated that no intermetallic compounds were formed.

3.5.2.3. Time and Temperature Dependence

In most cases, we observed that the shear strength increases with an increase in temperature and time. This may be due to the fact that while the intermetallic compounds may be more brittle, they improve stiffness and

increase adhesion between the two metals. We see that even when full intermetallic formation has taken place, the detrimental phases may only be found under specific conditions. We are currently looking into factors that may make some parts more susceptible to intermetallic failures.

3.5.3. Corrosion

Another one of our significant goal in using the electroless nickel cap to provide adequate corrosion protection for the bond pads. Our tests reveal that while the nickel barrier provides a good chemical barrier to ionics that may be present in the molding compound, it does not offer adequate protection at 121 °C in 2 atm pressure.

Our data revealed that the devices that failed the autoclave test was stressed to the point that delamination and cracks allowed the steam to come into direct contact with the nickel cap. Similar parts that was not stressed endured much longer time in the autoclave and yet experienced no electrical failure.

The autoclave test was used to accelerate the testing process. However, it is an unrealistic simulation of standard operating conditions. In addition, our preconditioning test for these particular packages was too aggressive. Our original thought was to push the packages as far as possible to determine if the nickel cap offers dramatic improvements over the standard aluminum bond pad. However, our plans were too aggressive, and we were unable to fully demonstrate the corrosion protection potential offered by the electroless Ni cap.

3.6. Summary

Our goal was to develop a concept of improving the reliability of the gold wire to aluminum bond pad interconnections. We demonstrated that, with a thin immersion gold layer for oxidation protection, the mid

phosphorous nickel cap is easily bondable. It offers protection against intermetallic formation between the aluminum and gold. This could be significant in automotive applications where the device is expected to function at high temperature for an extended period of time.

Although we did not have direct data to show corrosion improvements made by the electroless caps, we were successful in showing that this concept could be further developed. We would need to re-investigate our testing methodology to be more applicable to the product's operating conditions.

This program was also successful in bringing out factors to consider in plating, such as bond pad metallurgy and device functions. We accomplished the task of addressing some ground-breaking work. Further work would involve fine tuning the plating process and developing a new test plan that will allow for longer testing time to accomplish realistic results.

Chapter 4

Conclusion and Recommendations

4.1. Introduction

The chief goal of our research was to build a more robust silicon die in a plastic package. We first explored the current reliability issues that are inherent with plastic packages. We also revealed current solutions that are being implemented today to solve problems of specific packages. We proposed the glob top and electroless cap concepts to address the critical issues of stress and corrosion in the current plastic packages. In this chapter, we will review some of the major goals and objectives that were met, along with recommendations for future work.

4.2. Glob Top

This research has shown that adding a low stress liquid encapsulation can dramatically reduce the stress in the interlayer dielectric. We also determined that a lower cost molding compound can be used in conjunction with the glob top to leverage the cost of the additional processing step. This would be a good candidate for devices that are sensitive to stressing on top of the die.

In our study, we encountered problems with breaking of gold wire interconnection in some glob top parts. We discovered that when the glob top covers a significant amount of the wires, stress is placed on the exposed wires during the encapsulation process. When the glob top was placed on top of the die alone, covering a minimal part of the wire, we saw success in reducing stress on the die and the gold wire interconnection.

The multiple test chips allowed us to obtain a large number of data points to arrive at the above conclusions. However, we must be careful not to apply this process for all packages. We recommend selecting a live device test vehicle to verify these results on a standard reliability qualification schedule. For maximum benefits, the device should be sensitive to dielectric cracking. The dimensions of the different die and packages can result in differences in wire breaks results. Therefore, each package must be qualified on an individual basis.

4.3. Electroless Cap

The objective for developing the electroless capping concept is to protect the gold wire to aluminum bond pad interconnection against effects of stress and corrosion. We found that this is an inexpensive process which takes advantage of the selective plating capabilities of electroless nickel and immersion gold baths. We were successful in developing prototypes for evaluating potential reliability issues.

Although the nickel cap did not sufficiently protect the aluminum bond pads from corrosion at high steam atmosphere, it did provide an adequate barrier at moderate conditions. We need to further investigate the mechanisms that make the nickel more susceptible to corrosion due to high steam pressure.

We also discovered that nickel is an extremely good intermetallic barrier. At high temperatures, detrimental gold and aluminum intermetallic compounds can be prevented with the electroless nickel caps. Improving this interconnection interface allows for a more reliable package at higher stress levels. Our research time limitations did not allow us to obtain sufficient data for high temperature storage at longer time periods. We expect that, with enough time at a high temperature, the non-capped aluminum bond pads will fail compared to the nickel capped pads.

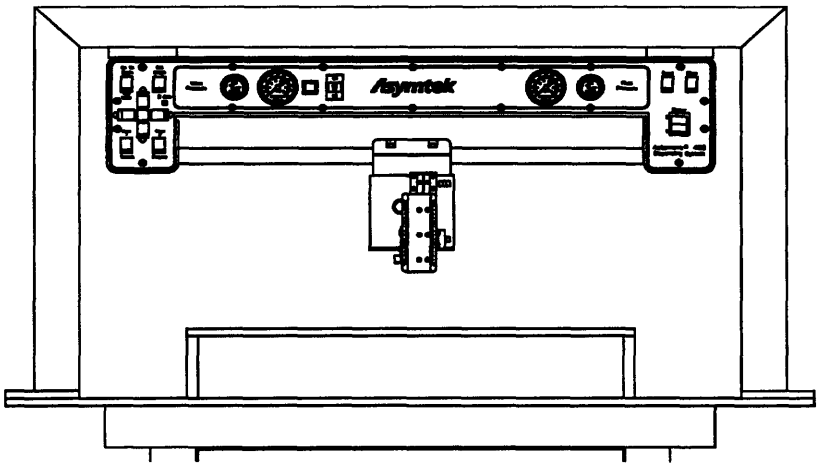
4.4. Summary

This dissertation demonstrates the feasibility of implementing these two concepts to improve the mechanical reliability of silicon circuits. More data would need to be obtained before progressing to bring these processes to production. In specific applications where the reliability is crucial, the added quality will outweigh the initial cost of introducing the new processes. We will continue our work in using these concepts to solve problems in product devices as the need arise. Once a product driver is defined, we can proceed with a complete reliability qualification without over accelerating the testing cycle time. Our objective in this dissertation is to provide tools which may be used to improve plastic packaging reliability by protecting the sensitive silicon die.

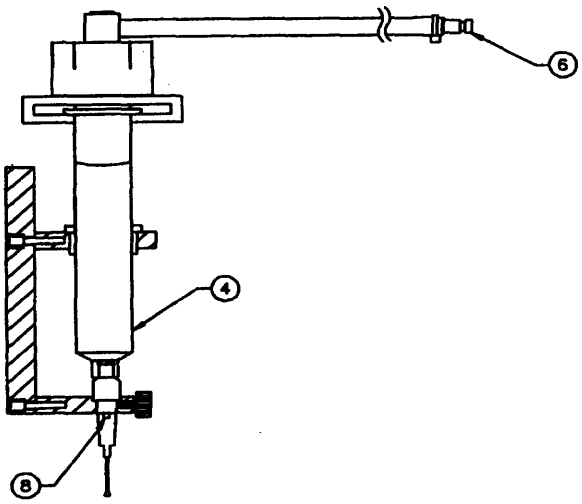
Appendix A: Typical Assembly Process Flow

#	Operation	Description
1	Wafer Saw	Wafer is diced into single die
2	Chip Bond	Silver filled epoxy die attach is used to secure the chip to the DAP
3	Wire Bond	Gold wire is bonded to aluminum bond pads by an ultrasonic scrubbing action at high temperature
4	Molding	A ram is used to force thermoset epoxy into the molding cavity where the leadframe resides
5	Post Mold Cure	Parts are placed in 175 °C oven for 4 hours to completely cure the epoxy
6	Deflash	Excess epoxy flash is removed from the parts by sand blasting
7	Lead Finish	Solder electroplating is done on the outside leads to enhance surface mount capabilities
8	Lead Trim and Form	Outside lead fingers are bent and curled to specified dimensions
9	Testing	Various electrical and optical inspections are performed

Appendix B: Asymtek 402 Fluid Move Gantry System



A simple linear valve is used to control the amount of fluid being dispensed.



4. **Cavity** serving as a reservoir for liquid encapsulant.

6. **Nozzle** connected to positive pressure to push out fluid.

8. **Needle base** which is often heated to control the viscosity of liquid to be dispensed.

Appendix C: Preconditioning Sequence for Test Chips A, B, and C in the Glob Top Evaluations.

Preconditioning Sequence	Conditions Testing Conditions		
	Test Chip A	Test Chip B	Test Chip C
Molding			
Electrical Testing			
TMCL	-65 °C to 150 °C, 30 cycles		
Bake	125 °C, 16 hours		
Soak	85 % RH / 30 °C, 168 hours	85 % RH / 85 °C, 168 hours	85 % RH / 30 °C, 48 hours
Reflow	245 °C maximum temperature measured on package.		
Flux Dip	15 seconds		
Electrical Testing			

Bibliography

[1] T.M. Moore, R. McKenna, S.J. Kelsall, 'Correlation of Surface Mount Plastic Package Reliability Testing to Nondestructive Inspection by Scanning Acoustic Microscope,' IEEE Proc. Int. Reliability Physics Symposium (1991): 106-6.

[2] S. A. Gee, M. R. Johnson, and K. L. Chen, 'A Test Chip Design for Detecting Thin Film Cracking in Integrated Circuit', IEEE 44th Electronic Components & Technology Conf. May 1-4, Washington, DC

[3] George G. Harman; Reliability and Yield Problems of Wire Bonding in Microelectronics, International Society for Hybrid Microelectronics, 1989, pp 49-50

[4] C. A. Harper, Electronic Packaging and Interconnection Handbook (McGraw-Hill, Inc., New York, 1991).

[5] R. R. Tummala and E. J. Rymaszewski, Microelectronics Packaging Handbook, (Van Nostrand Reinhold, New York, 1989).

[6] H. Suzuki, 'A Simulation Study of Moisture Absorption and Drying in IC Packages,' Hiroshi Suzuki, Electronic Device materials Lab, Sumitomo Bakelite Co., Ltd.

[7] Package Technology Group, Packaging Handbook, 1993

[8] T. Nishioka, S. Oizumi, S. Ito, 'Development of Encapsulating Materials for Surface Mounted Devices,' Nitto Denko Technical Reports, Jan. 1991, pp 82-92

[9] J. C. W. van Vroonhoven, 'Effects of Adhesion and Delamination on Stress Singularities in Plastic-Packaged Ingegrated Circuits,' Journal of Electronic Packaging, **115**, pp 28-32, March 1993

[10] T. M. Moore and R. G. McKenna, Characterization of Integrated Circuit Packaging Materials (Butterworth-Heinemann, Boston, 1993).

[11] R. L. Groover and J. H. Joroski, 'Impact of Moisture on PLCC/PJQFP Package Cracking'

[12] L. T. Nguyen and K. L. Chen, 'Molding Compound Trends in a Denser Packaging World: Part III - Property Optimizatin for Minimum Stress,' Electronic Packaging Reliability ASME, **6**, pp 101-114, 1993

[13] J. W. Balde, 'The Effectiveness of Silicone Gels for Corrosion Prevention of Silicon Circuits: The Final Report of the IEEE Computer Society Computer Packaging Committee Special Task Force,' IEEE Trans. on Components, Hybrids, and Manufacturing Technology, **14**, 2, pp 352-365, Juen 1991

[14] C. H. Ting, 'Electroless Metal Deposition for Integrated Circuit Fabrication,' Proceedings from the Symposium on Electroless Deposition of Metals and Alloys, **88**, 12, pp 223-243, 1988

[15] T. Inoue et al, 'Stable Non-Cyanide Electroless Gold Plating Which is Applicable to Manufacturing of Fine Pattern Printed Wiring Boards,' Hitachi, IEEE, 1995

[16] H. Honma, H. Watanabe, and T. Kobayashi, 'Direct Nickel Plating on Aluminum Substrate for Microbump Formation,' Journal of Electrochemical Society, Vol. 141, No. 7, 1994, pp 1791-1795

[17] S. A. Gee, K. L. Chen, and L. T. Nguyen, 'Test Chip and Finite Element Analysis of Passivation Cracking in Molded Integrated Circuits,' ASME Int. Mechanical Eng. Congress and Exposition, San Francisco, Nov. 12-17 (1995)

[18] S. A. Gee, L. T. Nguyen, R. E. Crippen, M. J. Strong, P. Hom, and C. J. Conklin, 'Structural Considerations for the Design of Integrated Circuits,' IEEE 4th International Symposium on Physical & Failure Analysis of Ics, Singapore, Nov. 1-5 (1993)

[19] D. C. Zipperian, S. Raghavan, and M. Pritzker, 'Physical and Chemical Characterization of Zincate Immersion Process for Aluminum,' Proceedings of the Symposium on Electroless Deposition of Metals and Alloys, 1988 vol. 88-12

[20] M. Paunovic, Plating, **55**, 1161 (1968)

[21] G. G. Harman, 'Reliability and Yield Problems of Wire Bonding in Microelectronics,' (International Society for Hybrid Microelectronics, Reston, Va, 1989)

[22] J. Wolf, et al, 'Solderbumping-A Comparison of Different Technologies,' 1st Flip Chip Technology & 6th TAB/Advanced Packaging 1994 Proceedings (San Jose, CA, 1994)

[23] CRC Materials Science an Engineering Handbook, 385-405, 1995

[24] E. G. Colgan, Material Science Rep. **5**, 1, 1990

[25] K. Lin and J. Chang, 'The Elemental Interaction in the Electrodeposited Pb-Sn/Electroless Ni-P Deposit/Al Multilayer upon Heat Treatment,' Scripta Metallurgica et Materialia, **30**, 559-564, 1993

[26] W. L. Fink and L. A. Willey, Trans. AIME, **111**, 293, 1994

[27] T. B. Massalski, J. L. Murray, L. H. Bennet and H. Baker eds., Binary Phase Diagram, ASM 1986

Biographical Note

There are so many things I want to say to sum up where God has taken me these past few years. I will take this opportunity to share more of my life so that I may give glory to God. His hands and providence was upon me even before I knew Him. When I was only eight years old, God took my family and I out of Vietnam by a small boat that held about twenty people. I was on a journey to meet my father who had to leave Vietnam when I was only 3 years old because of his involvement in the South Vietnamese military. God provided safe passage through the border patrol, the pirates, and the tumbling sea. We were at sea for three days until a Norweigian research vessel came to rescue us. They took us to Singapore where we waited a few months to complete the immigration paper work to come to the United States to be united with my father.

I grew up thinking that I needed to be successful to take advantage of the opportunity that was given to me in the United States. I wanted to live a life that was good and moral to me. There were no absolutes by which I was to be judged. I went to church every week, but my lifestyle did not reflect that. Due to this conflict, I was filled with guilt.

In my early undergraduate years at MIT, I knew I had to make a decision whether to give up going to church or to give up my carefree ways. In addition to academic pressures and frustrations, I felt no peace with what I am doing. Finally, as a result of the witness and prayers of other believers, I accepted Jesus into my heart, giving up my sinful nature. I was moved by the fact that apostle Paul had given up everything, turning 180° for Christ.

Things have not always been smooth sailing. Many times, I had to face the challenges from my past head on. Sometimes tasks appear to be impossible. Sometimes I did fail. He is always there. When the smoke clears, I can hear Him asking, "has no one judged you guilty?" I would nod my head in shame and guilt. He, however, lifts me up, saying, "I also don't judge you guilty. You may go now, but don't sin anymore."

4796 - 15