Vertical Profile Engineering and Reliability Study of Silicon-Germanium Heterojunction Bipolar Transistors

by

Kenneth S. Liao

B.S. Electrical Engineering, University of Pennsylvania (1988)

M.S. Physics, Harvard University (1990)

Submitted to the

Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the

degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

February 1996

Author_____

Department of Electrical Engineering and Computer Science
September 29, 1995

Certified by_____

L. Rafael Reif
Director, Microsystems Technology Laboratories
Thesis Supervisor

Accepted by_____

Frederick R. Morgenthaler
Chair, Departmental Committee on Graduate Students

Vertical Profile Engineering and Reliability Study of Silicon-Germanium Heterojunction Bipolar Transistors

by

Kenneth S. Liao

Submitted to the
Department of Electrical Engineering and Computer Science
on September 29, 1995,
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

Abstract

The research leading to this thesis focuses on vertical profile engineering and stress reliability aspects of the SiGe-base HBT development. Various topics on the device design, fabrication, characterization and modeling are examined. Detailed analysis and experiment are carried out to enhance our understanding of the subject.

We rely on a home-built, single-wafer, non-load-locked, quartz-halogen-lamp-heated, very-low-pressure chemical vapor deposition (VLPCVD) system to supply $Si_{1-x}Ge_x$ films for various material studies and device processing. Three process sequences — the "MESA", the "LOCOS", and the "POLY", are developed for the device fabrication. Functional devices with high current gain, excellent current ideality factors and good breakdown behaviors are obtained. High-frequency and 1/f noise measurements are performed. Matching of device current gains and turn-on voltages in the form of statistical measurement are investigated. Observation of a rapid current gain rolloff in devices with lightly doped emitters is reported. The rolloff can be attributed to the formation of a parasitic barrier at the base-emitter junction resulting from dopant outdiffusion. A model based on the inverse Early effect is proposed to explain the rolloff, confirming by MEDICI simulation. We have also initiated the reliability study to examine degradation behavior of the SiGe-base HBT device under high-forward current and reverse bias stresses. Important conclusions include: (1) SiGe devices do not suffer from early catastrophic failure under the condition applied; (2) inclusion of Ge in the base may potentially improve the base-emitter junction reliability; and, (3) existing homojunction theory — the hot-electron degradation model — can accurately model device degradation behavior under reverse current stress.

Thesis Supervisor: L. Rafael Reif
Title: Director, Microsystems Technology Laboratories

Acknowledgments

I thank all the people whose efforts have helped me cross the finish line ....

First and foremost, I wish to express my deepest gratitude and appreciation to my thesis supervisor, Professor Rafael Reif, for his constant guidance and encouragement. He also has my greatest admiration and respect as the most wonderful boss.

I am also grateful to my thesis readers, Prof. C. Sodini and Prof. J. E. Chung. I have benefited significantly from their valuable comments and suggestions that help shape this thesis. I am further indebted to Dr. T.I. Kamins, Dr. W.-J. Ho and Dr. D. Pelhke for providing assistance and technical comments.

Thanks go to all the former and present ICL and TRL staff members. Without their support, training and friendship, this thesis would not have gone far. Thanks also go to C. Zaccaria and C. Gordy for guiding me through the administrative jungle of MIT and SRC.

During the course of my graduate study many friends have assisted me and offered their support. Thanks go to Syun-Ming and Curtis for getting me started on this project in the first place. Thanks also go to my officemates, Zhen, Dr. Fan and Weize, for many many enlightening conversations and chess games. I am quite honored to be part of the "reifgroup", ... Nakano, Miyata, Julie, Kim, Andy, Alex, Rajan, Ben, Simon ... ; all of you will certainly be missed. I also owe much to my friends, Peng, Vei-Han, Paul, Charles, Fuzhong and Meng, for sharing the highs and lows throughout my graduate life.

Finally, I thank each and every member of my family for their love and unconditional support during these seemingly endless years. I thank Yaya for being so understanding and patient. I thank my grandparents for their sacrifices and life-long devotion to raise the family. My parents deserve the most credit and to whom this thesis is dedicated.

Contents

1 Introduction **11**

1.1 Trends of SiGe-base HBT Technology 11

1.2 Motivation 12

1.3 Properties of Strained $Si_{1-x}Ge_x$ Layers 14

1.4 Basic Operation of SiGe-base HBTs 19

1.5 Advantages of SiGe-base HBTs 23

1.6 Thesis Overview 23

2 Design Consideration for Analog Application **29**

2.1 Device Requirements 30

2.2 Figures of Merit 31

2.3 Vertical Profile Design 35

2.3.1 Base design issues 35

2.3.2 Emitter Design Issues 38

2.3.3 Collector Design Issues 40

2.4 Summary 43

3 Device Fabrication and Characterization **45**

3.1 HBT Fabrication Processes 46

3.1.1 The "MESA" Process 47

3.1.2 The "LOCOS" Process 51

3.1.3 The "POLY" Process 52
3.2 Fabrication Technology 55
3.2.1 $Si_{1-x}Ge_x$ Deposition by VLPCVD 55
3.2.2 Thermal Annealing 60
3.3 Device Characterization 61
3.4 Summary 70

4 Vertical Profile Engineering **73**
4.1 Base Region 73
4.1.1 Effect of Germanium 74
4.1.2 Graded Base 76
4.2 Device with Lightly Doped Emitters 80
4.3 Displacement of P-N Junctions 84
4.4 Summary 90

5 Reliability Study of SiGe-base HBTs **93**
5.1 Experiments 95
5.2 High-forward-current Stress 96
5.3 Reverse-voltage Stress 96
5.4 Reverse Current Stress 99
5.5 Summary 106

6 Conclusion and Suggestion for Future Research **107**
6.1 Technology Integration Issues 109
6.2 Applications 112
6.3 Future Materials and Devices 114

A Carrier Transport in Neutral Base Region **117**
A.1 Energy Band Structure 118
A.2 Modified Boltzmann Transport Equation 119

A.3 Solution to the Stationary Transport Equation 120
A.4 Generalized Drift and Diffusion 121

B "POLY" Process **123**
B.1 Process Description 123
B.2 Process Cross-section 130
B.3 Mask Layers 132

Bibliography **133**

List of Figures

1-1 Critical thickness of $Si_{1-x}Ge_x$ alloys as function of Ge content. 15

1-2 Energy bandgap of both strained and unstrained (bulk) $Si_{1-x}Ge_x$ alloys as function of Ge content [46]. 17

1-3 Advantages of using $Si_{1-x}Ge_x$ alloys. 22

1-4 Overview of the thesis organization. 24

3-1 Basic flow sequence of the "MESA" process. 49

3-2 Cross sectional schematic diagram of the "MESA" process for the SiGe-base HBT fabrication. 50

3-3 Typical parameters of $Si/Si_{1-x}Ge_x/Si$ heterostructure used for the device fabrication. 51

3-4 Cross sectional schematic diagram of the "POLY" process for the SiGe-base HBT fabrication. 53

3-5 Schematic diagram of the Very-Low-Pressure Chemical Vapor Deposition (VLPCVD) reactor used in this work [70]. 56

3-6 Cross-section and typical parameters of a device fabricated using the "MESA" process. 62

3-7 Device characteristics: the Gummel plot and the I_C vs. V_{CE} curve of a typical device. 63

3-8 Statistics of the collector and base currents at biases of V_{BE}=0.6, 0.66, and 0.72 volts. The considered devices are obtained from wafer A579 with emitter area of 4.5μm×4.5μm. 65

3-9 Statistics of I_C and I_B idealities as a function of emitter area. Devices are obtained from wafers A572, A575, and A579. 66

3-10 Reciprocal of measured transconductance (g'_m) versus reciprocal of collector current (I_C). $r_{e'}$ can be extracted from the plot. 67

3-11 The Getreu's setup and plot of I_B versus V_{CE}. The value of $r_{e'}$ can be determined from the slope of the dashed curve (corresponding to I_C=0). 68

4-1 Collector current enhancement and normalized current gain of SiGe-base HBTs (with 5% or 10% Ge in the base). The solid line shows the characteristics of a fabricated homojunction device with similar structure. 75

4-2 Ge profiles obtained by SIMS of a box (15% Ge), forward-graded (12–20% Ge), and retro-graded (20–12% Ge) devices. 77

4-3 Gummel plot and current gain vs. I_C of the devices from wafers A584 and A585. 78

4-4 I_C vs. V_{CE} plots obtained from the two devices in wafers A584 and A585. 79

4-5 SIMS Profile from the device wafer 82

4-6 Current gain plotted against the collector current density, showing the early rolloff of current gain. 82

4-7 Energy band diagram. 83

4-8 MEDICI simulation structure used to study the effect of B-E junction displacement. 86

4-9 Summary of the simulation results on the effect of B-E junction displacement. 87

4-10 Simulated energy band diagram for the three cases of base-emitter junction displacements. 87
4-11 Simulated Gummel plot and β vs. J_C curves for the cases of base-emitter junction displacements. 88
4-12 Summary of the simulation results on the effect of B-E junction displacement. 89

5-1 Schematic cross-section and typical parameters of the devices used in this work. 95
5-2 Device characteristics before and after current stressing at >1mA/μm^2 for 382 hours. 97
5-3 Device characteristics before and after reverse stressing at V_{BE}=-5V for 180 hours. 98
5-4 Emitter-base junction characteristics of a typical SiGe-base HBT . . . 99
5-5 Gummel plot and β vs. I_C curves of a device stressed with reverse current, I_R, of 5μA. 101
5-6 Degradation of I_B as function of stress time at different I_R. 102
5-7 Degradation of I_B as function of stress charge at different I_R. 103
5-8 Degradation of I_B as function of collector current at different reverse stress currents. 104
5-9 Effect of area/perimeter ratio on the degradation. 105
5-10 Effect of base doping level on the degradation under reverse bias. . . 105

List of Tables

1.1 Fundamental equations of semiconductor device analysis for the general case of materials with spatially varying composition [54]. 19

2.1 Summary of device requirements of various amplifier circuits [59]. . . 30

2.2 Key formulae for graded base structures. 38

3.1 Typical process recipe for depositing $Si_{1-x}Ge_x$ alloys in the APCVD [74]. 54

3.2 Summary of the standard operating procedure of the VLPCVD reactor. 59

3.3 Typical growth conditions of the VLPCVD for SiGe-base HBT structures. 60

3.4 Layer structures deposited in a commercial APCVD reactor to examine the effect of boron doping in the base. 64

3.5 Summary of device characterization results of device wafers A572, A575, and A579. 64

4.1 Layer structures deposited in the VLPCVD reactor to examine the effect of Ge in the base. The parameters are estimated from previous kinetic data. 74

4.2 Summary of the parameters of the layer structures in this experiment with both graded and retrograde Ge profiles. 77

6.1 Composition of group IV materials. 114

Chapter 1

Introduction

1.1 Trends of SiGe-base HBT Technology

In recent years, with maturity of epitaxial deposition techniques, silicon-germanium alloys have emerged as important silicon-technology-compatible materials that promise great potential of providing superior electronic and optoelectronic devices [1–3]. Novel structures and high performance devices, such as $Si_{1-x}Ge_x$/Si Quantum Well (QW), Modulation Doped Field Effect Transistor (MODFET), Heterojunction Bipolar Transistor (HBT), infrared detector, and modulator, are being realized and fabricated [4–7]. Most notable developments can be found in the area of HBT research using $Si_{1-x}Ge_x$ alloys [8–13].

$Si_{1-x}Ge_x$ offers an extra degree of freedom in meeting the conflicting design requirements of performance and reliability that impact conventional bipolar transistors. The use of $Si_{1-x}Ge_x$ alloys as narrow-bandgap base materials in the design of bipolar transistors has provided additional flexibility and leverage for device optimization. It is an attractive means for enhancing the emitter injection efficiency and base transport factor, thereby providing higher current gain. Moreover, the high current gain allows designers to either increase the base dopant concentration — thereby reducing the base resistance, or reduce the emitter doping levels — thereby lowering

the emitter-base junction field and, consequently, the junction leakage current.

Since the first report of SiGe-base HBT device appeared in 1987 [8], there has been a steadily increasing number of publications each year. A good summary of the development can be found in Ref. [12–14]. SiGe-base HBTs with f_T of 116 GHz, the record high in the Si-based technology, have been reported [15, 16]. Impressive figures of merit, e.g. f_{max} of over 100 GHz [17], noise figure of 0.9 dB at 10 GHz [18], current-gain-Early-voltage product of over 10,000 V [19], and ECL gate delay of less than 20 ps [20, 21], have also been attained. High performance BiCMOS process, with addition of SiGe-base HBTs to a standard CMOS process, has been successfully integrated [22]. Recent achievements also include the first demonstration of large-scale integration, a 1GHz/1W, 12-bit digital-to-analog converter (DAC) [23], as well as improved low temperature operation with SiGe-base HBTs [24–27].

Device results in the literature, so far, have demonstrated the potential of SiGe-base HBTs for digital applications. Recently, researchers have begun to explore the area for analog and mixed-signal applications. This area is gaining increasing attention because of the rapid growth and demand of the wireless and telecommunication products [28]. New systems in wireless digital communications require high performance, low cost RF components operating from few hundred MHz to several GHz. SiGe-base HBT with inherent merits such as high speed, low noise figure and high Early voltages — offering substantially greater leverages in analog circuitry, is an ideal candidate for the application.

1.2 Motivation

There are two main motivations why process and device engineers are actively pursuing the SiGe-base HBT technology: namely, introducing bandgap engineering into the Si-based technology; and overcoming limitations of Si bipolar transistors.

Concepts of Bandgap Engineering

With advanced growth techniques such as Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD), epitaxial $Si_{1-x}Ge_x$/Si has made feasible the realization of bandgap engineering concepts in the Si-based technology. Bandgap engineering greatly enhances the range of possible device configurations and opens the door to new physical phenomena such as heterojunction effects and alloy grading [29–32]. These widely practiced techniques in advanced III-V devices can now be introduced to improve the performance of Si-based devices. The detailed analysis of the added advantages will be elaborated in a later section.

Limitations of Si Bipolar Transistors

The major driving force behind the development of SiGe technology is to address the fundamental limitations of Si bipolar transistors.

Silicon bipolar transistors are widely used for various circuit applications, from small, high-speed to high density VLSI circuits [33,34]. New processes such as polysilicon emitter, various self-alignment schemes and deep trench isolation have led to significant improvements in intrinsic speed and reduction in parasitic RC elements in silicon bipolar devices [35]. However, the conventional advanced Si bipolar technology is reaching the device scaling limits and facing the physical doping limitations as well as many undesirable existing tradeoffs [36].

This leads to a tremendous amount of effort searching for alternative technology, e.g. AlGaAs/GaAs, InGaAs/InP, and SiGe/Si systems. Most importantly, SiGe is compatible with the existing Si-based processing technology, unlike other III-V materials which are not. Recent development in SiGe-base HBTs has proven that the use of $Si_{1-x}Ge_x$ as the narrow-bandgap base material provides additional flexibilities to overcome these basic limitations and improve device performance. In addition, $Si_{1-x}Ge_x$ alloys offer superior material parameters, such as higher minority carrier

mobility, and carrier velocity.

1.3 Properties of Strained $Si_{1-x}Ge_x$ Layers

There exists a vast amount of information on important properties of strained $Si_{1-x}Ge_x$ layers in the literature [37]. We will limit the discussion to properties that are relevant to the device operation only. The most important material parameters of $Si_{1-x}Ge_x$ pertaining to HBT operation, include the critical thickness, the bandgap, and the band alignment of $Si_{1-x}Ge_x$/Si heterostructure.

Critical Thickness

Silicon and germanium are completely miscible over the entire compositional range, giving rise to $Si_{1-x}Ge_x$ alloys with a diamond crystal structure. The lattice constant of $Si_{1-x}Ge_x$ at room temperature is given by the Vegard's rule [14],

$$a_{Si_{(1-x)}Ge_x} = a_{Si} + x(a_{Ge} - a_{Si}). \tag{1.1}$$

The equation is valid for low atomic concentrations (x) of Ge.

The major limitation on the growth of $Si_{1-x}Ge_x$/Si heterostructure is imposed by the lattice mismatch between the two materials. Because Ge has a larger lattice constant than Si by about 4.17%, commensurate or pseudomorphic growth of $Si_{1-x}Ge_x$ on Si requires one or both layers to be strained. The amount of strain depends on the difference in lattice constants between the two layers; the greater the difference of Ge concentrations, the larger the mismatch. During growth, because of the lattice mismatch, strain energy builds up through the layer and, in layers above certain thickness, strain energy will be relieved by dislocations. The maximum thickness for pseudomorphic growth of the alloy is defined to be the critical thickness.

Figure 1-1 plots both theoretical and experimental values of the critical thicknesses

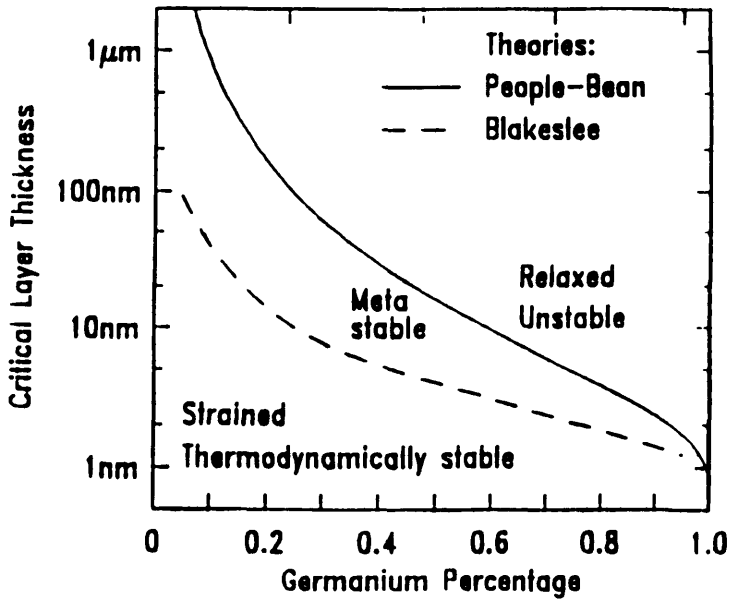


Figure 1-1: Critical thickness of $Si_{1-x}Ge_x$ alloys as function of Ge content.

as function of Ge content. The dotted curve shows the theoretical values derived, based on the kinetic and thermodynamic equilibrium theory of Matthews-Blakeslee [38]. Layers below this curve are found to be unconditionally stable. In general, layer growth above this theoretical curve is possible, shown by the experimentally fitted curve (the solid lines), provided that the layer is conditionally stable or meta-stable.

The critical thickness depends on the Ge concentration and the growth temperature. A major feature for successful commensurate growth of $Si_{1-x}Ge_x$ strained layers is to carry out the growth at as low a temperature as possible in maintaining high crystallinity and, at the same time, insuring two-dimensional growth. To date, both MBE and CVD are very successful for growth of $Si_{1-x}Ge_x$ layers with reported deposition temperatures in the range of from 500°C to 900°C [14, 39–41]. However, most $Si_{1-x}Ge_x$ layers found in these reports are metastable in nature. Therefore, it is essential to keep the post-deposition thermal treatment as low as possible in order to maintain integrity of the layers.

Energy Bandgap

The theory of band structure, i.e. the energy-momentum relation, of a crystalline solid is widely discussed in many textbooks [42–44]. It forms the basis for the modern theory of carrier transport and device physics. The bandgap of a semiconductor material, defined to be the separation between the energy of the lowest conduction band and that of the highest valence band, is probably the most important parameter and most useful concept within the theory.

The energy bandgap of $Si_{1-x}Ge_x$ alloy is determined by theoretical calculation and verified by optical absorption and photocurrent spectroscopy experiments [45–47]. Figure 1-2 shows the energy bandgap relationship of $Si_{1-x}Ge_x$ as function of Ge fraction for both strained and unstrained (bulk) alloys. For the unstrained $Si_{1-x}Ge_x$ alloys, the bandgap remains Si-like for Ge content of up to ~85%; then a sharp change of the bandgap occurs due to the transition from a Si-like conduction band, whose sixfold degenerate minima lie along <100>, to a Ge-like band, with eightfold degenerate minima directed along <111> [48].

In the case of strained $Si_{1-x}Ge_x$ alloys, the band structure is significantly modified by the strain. The bottom two curves shown in Figure 1-2 apply to commensurate growth of $Si_{1-x}Ge_x$ on a thick (100) Si substrate. The strain resulting from the lattice mismatch lifts the equivalence of the six <100> direction. The sixfold degeneracy is split into a twofold and a fourfold equivalence, raising the energy of the two minima whose wavevectors lies along the direction of growth, and lowering the energy of the four minima with wavevectors lying in the plane of growth. For SiGe-base HBT application, we will only concentrate on the deposition of $Si_{1-x}Ge_x$ on bulk (100) Si wafers. The splitting of valence band, giving rise to additional bandgap reduction, is advantageous for the device application. Because of the growth limitation, we are restricted to $Si_{1-x}Ge_x$ alloys with Ge fraction under 25 at.%. Note if the strain is reversed, i.e. if we are trying to grow strained Si on $Si_{1-x}Ge_x$ alloys, then the energy of the fourfold minima is raised and that of the twofold minima lowered. It is also

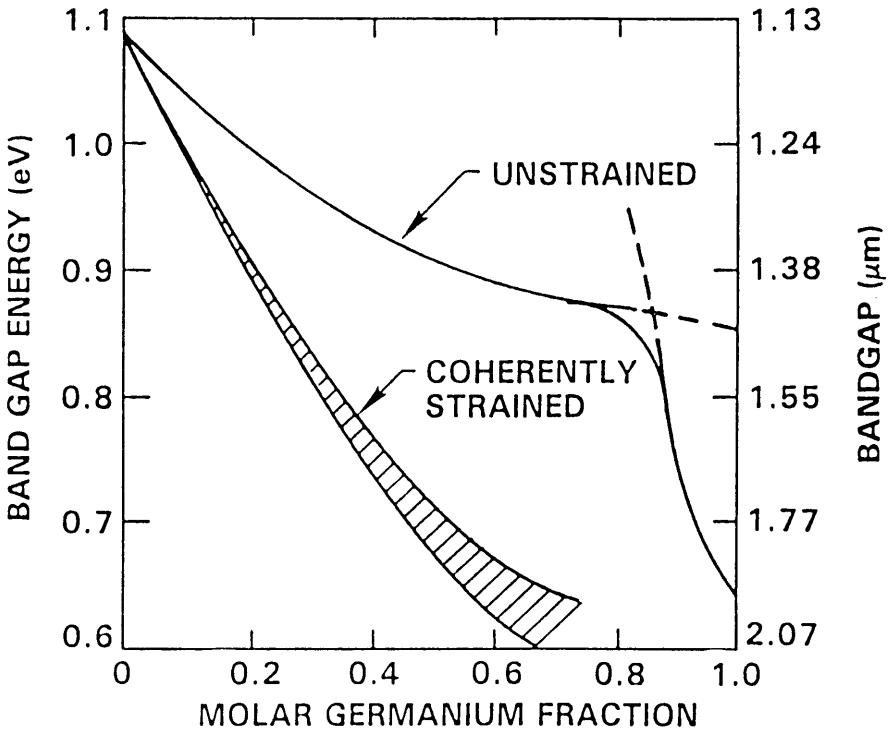


Figure 1-2: Energy bandgap of both strained and unstrained (bulk) $Si_{1-x}Ge_x$ alloys as function of Ge content [46].

interesting to note that if growth is on a (111) substrate, the splitting disappears altogether because the sixfold symmetry of the <100> direction is not destroyed [48].

Energy Band Alignment

Junctions between two dissimilar semiconductors, i.e. heterojunctions, have been studied extensively. When two dissimilar materials are brought in to proximity, thermal equilibrium requires the Fermi levels in the two materials to be coincident, giving rise to discontinuities or band offsets in both the conduction and valence bands [49,50]. Transport properties of carriers as well as other electrical parameters depend critically on the alignment and offsets of the band structures of the two materials.

In the case of $Si_{1-x}Ge_x$ on Si, the structure forms a type-I material with less than 20% of total bandgap difference appearing in the conduction band. This relatively small conduction band offset gives insignificant conduction band spike near the heterojunction, in contrast to most III-V materials where large spikes usually exist. Conduction band spikes can impede the transport of electrons across the junction and degrade the injection efficiency. In III-V materials, alloy grading is typically required to minimize the effect of the conduction band spike.

The large offset in the valence band of $Si_{1-x}Ge_x$/Si creates an ideal situation where the hole is facing a greater barrier than the electron by an amount ΔE_v, giving rise to an enhanced emitter injection efficiency. Therefore, $Si_{1-x}Ge_x$ is an ideal material for realizing n-p-n heterojunction bipolar transistors. The valence band discontinuity for $Si_{1-x}Ge_x/Si_{1-y}Ge_y$ is given by the expression:

$$\Delta E_v = (0.84 - 0.53y) \cdot x \qquad (eV) \tag{1.2}$$

For design of SiGe-base HBTs, a good rule of thumb in estimating the band offset at low Ge contents (x), is roughly equal to 75meV per 10% of Ge.

Time-dependent continuity equations:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} + (G_n - U_n) \tag{1.3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} - (G_p - U_p) \tag{1.4}$$

Drift-diffusion equations:

$$J_n = q\mu_n n\left(-\frac{d\Psi}{dx} + \frac{1}{q}\frac{d\Delta E_C}{dx}\right) + qD_n\left(\frac{\partial n}{\partial x} - \frac{n}{N_C}\frac{dN_C}{dx}\right) \tag{1.5}$$

$$J_p = q\mu_p p\left(\frac{d\Psi}{dx} + \frac{1}{q}\frac{d\Delta E_V}{dx}\right) + qD_p\left(\frac{\partial p}{\partial x} - \frac{p}{N_V}\frac{dN_V}{dx}\right) \tag{1.6}$$

Poisson equation (in 1-D):

$$\frac{\partial^2 \Psi}{\partial x^2} = -\frac{q}{\epsilon}(p - n + N_D^+ - N_A^-) \tag{1.7}$$

Einstein relation:

$$\frac{D}{\mu} = \frac{k_B T}{q} \tag{1.8}$$

Table 1.1: Fundamental equations of semiconductor device analysis for the general case of materials with spatially varying composition [54].

1.4 Basic Operation of SiGe-base HBTs

In this section, the basic operating principles of HBTs are presented to establish the foundation for later analysis. The operating principles of HBTs are in many ways identical to those of homojunction transistors; and the later are widely discussed in many standard textbooks [42, 51–53].

Listed in Table 1.1 are the fundamental governing equations of semiconductor devices: the continuity equations, current density equations (drift-diffusion equations), and the Poisson equation, plus the Einstein relation.

Note that these equations differ from the conventional ones in the expression for J_n and J_p. The new terms include drift-like contributions — in which the gradient of conduction band energy $d\Delta E_C/dx$ acts as a quasi-electric field affecting electrons only, and the gradient of valence band energy $d\Delta E_V/dx$ correspondingly affects holes; and diffusion-like terms — involving the gradients in the densities of states in the conduction and valence bands, N_C and N_V [54]. Approximate estimates of the behavior of HBTs can be obtained by solving these equations. In addition to the spatially varying band structures, materials may be under nonuniform temperature or strain, or devices may contain highly doped regions. The treatment of these cases is beyond the scope of this thesis and a brief overview is included in Appendix A.

Moll-Ross-Kroemer Formulation

It was first shown by Moll and Ross [55], and later extended by Kroemer to include heterojunction effect [56], that the minority-carrier current in the base region of a bipolar transistor in the forward active operation can be written independently of the boundary condition on the base side of the emitter junction .

Number of assumptions are made in order to arrive at the result: (1) 1-D geometry, (2) w_B large compared to carrier mean free path, (3) electron transport is by drift plus diffusion, (4) constant carrier mobility, (5) low level injection, i.e. net base doping $p(x) \approx N_A(x)$, and, (6) negligible recombination in the bulk region. The derivation is as follows:

First, consider the minority carrier drift-diffusion equations, expressed in term of quasi-Fermi levels E_n and E_p for electrons and holes:

$$\begin{aligned} J_n &= q\mu_n n \frac{d}{dx}\left(\frac{E_n}{q}\right) = \mu_n n \frac{d}{dx} E_n \\ J_p &= -q\mu_p p \frac{d}{dx}\left(\frac{E_p}{q}\right) = -\mu_p p \frac{d}{dx} E_p \end{aligned} \tag{1.9}$$

To simplify the analysis, we will assume the hole current density is small, i.e. $dE_p/dx \approx$

0. Thus, we can rewrite equation (1.9) in the form

$$J_n \approx \mu_n n \frac{d}{dx}(E_n - E_p) \tag{1.10}$$

Now, for nondegenerate densities,

$$np = n_i^2 \exp[(E_n - E_p)/k_B T] \tag{1.11}$$

From which,

$$\frac{d}{dx}(E_n - E_p) = k_B T \left(\frac{n_i^2}{np}\right) \cdot \frac{d}{dx}\left(\frac{np}{n_i^2}\right) \tag{1.12}$$

Substituting this into the current equation (1.10) and using Einstein relation, $qD_n = \mu_n k_B T$, we get:

$$\frac{d}{dx}\left(\frac{np}{n_i^2}\right) = \frac{J_n}{q} \cdot \frac{p(x)}{D_n n_i^2(x)} \tag{1.13}$$

Upon integration, yields

$$J_n = -q \cdot e^{qV_{BE}/k_B T} \left[\int_B \frac{p(x)}{D_n n_i^2(x)} dx\right]^{-1} \tag{1.14}$$

where we have applied the Shockley boundary condition that $np/n_i^2|_0 = \exp(qV_{BE}/k_B T)$.

The average transit time for electron can be written

$$\tau_B = \int_0^w \frac{dx}{v} \tag{1.15}$$

Use the fact that $J_n = -qnv$; after some algebra, we arrive at

$$\tau_B = \int_0^w \left[\frac{n_i^2}{p(x)} \int_x^w \frac{p(y)}{D_n(y) n_i^2(y)} dy\right] dx \tag{1.16}$$

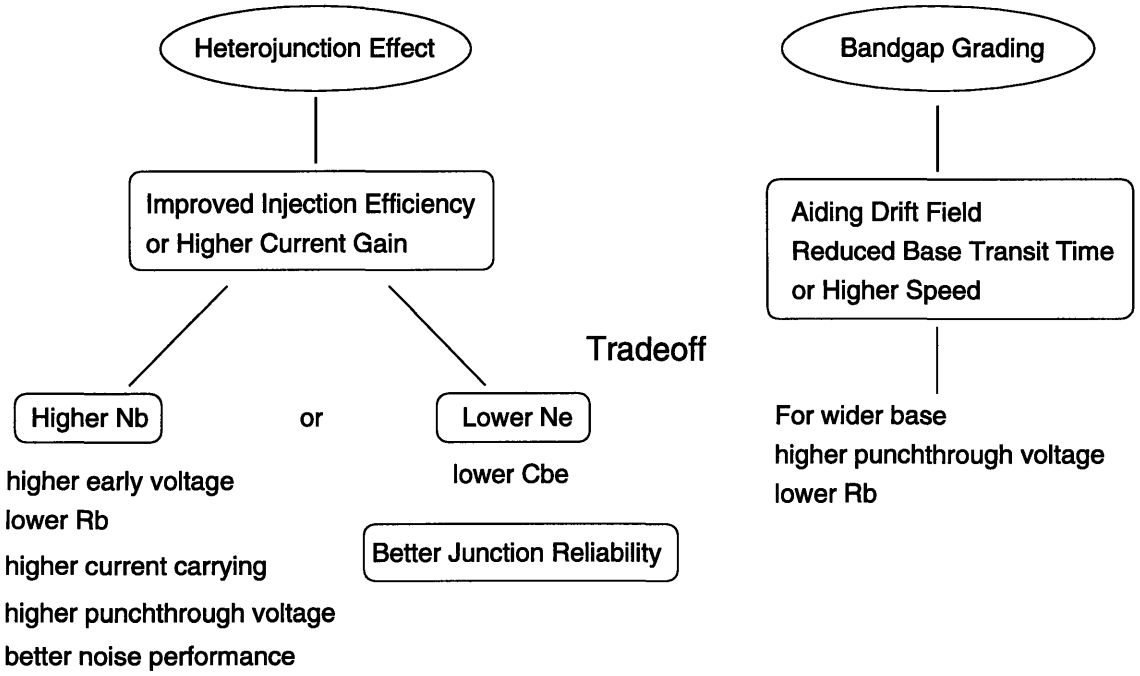


Figure 1-3: Advantages of using $Si_{1-x}Ge_x$ alloys.

1.5 Advantages of SiGe-base HBTs

SiGe-base HBTs offer additional design flexibilities for overcoming the limitations of homojunction devices, as well as, provide substantial leverages in analog applications. The bandgap offset of $Si_{1-x}Ge_x$ subtly alters some of the tradeoffs involved in optimizing transistor performance. There are two major approaches in realizing the advantages of $Si_{1-x}Ge_x$, as summarized in Figure 1-3, (1) exploiting heterojunction effect at the base-emitter junction which gives rise to an improved emitter injection efficiency or higher current gain; and, (2) employing a graded-germanium base profile which creates an aiding drift field to reduce total base transit time and increase device speed.

Various tradeoffs to improve device performance are possible. For example, high emitter injection efficiency (or high current gain) can be maintained while allowing a heavily doped base or a lightly doped emitter. The higher base doping concentration leads to a lower base resistance and lower noise figure as well as higher current drive capability. Furthermore, the high base doping results in small base width modulation, which gives rise to low output conductance (high Early voltage) and high device linearity capabilities. If the doping concentration in the emitter is lowered to a level below that of the base, a significant reduction of emitter/base junction capacitance occurs, and hence a corresponding increase in the cut-off frequency f_T. Decreasing the emitter doping level also improves the breakdown voltage of the base-emitter junction (BV_{EBO}), thus, provides better junction reliability.

1.6 Thesis Overview

Despite numerous reports on the device/circuit performance and processing technology, only until recently have researchers begun to explore the potential leverages of SiGe-base HBTs in analog and mixed-signal applications [13]. The most impor-

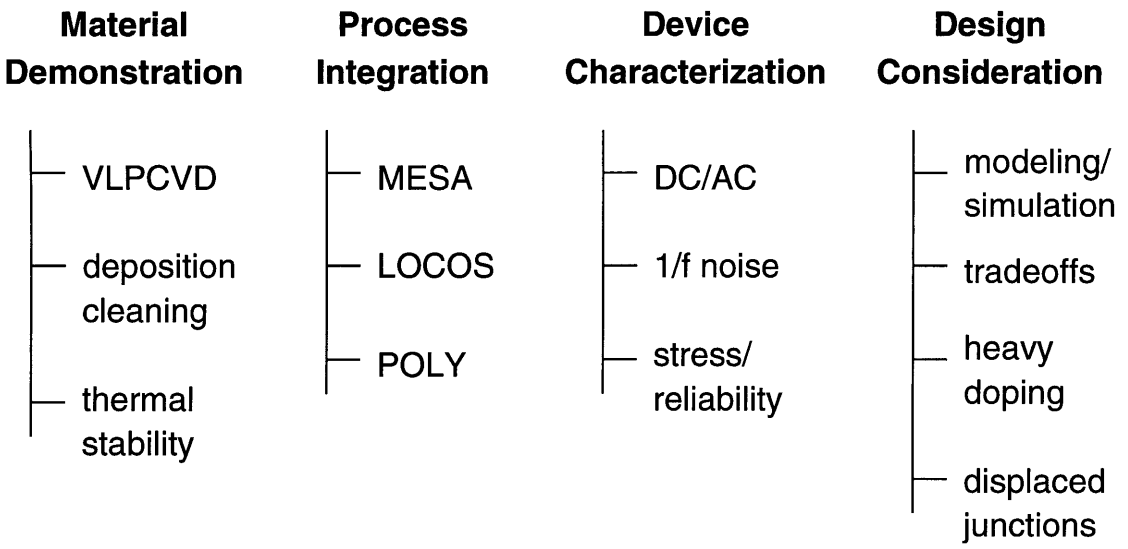


Figure 1-4: Overview of the thesis organization.

tant application of SiGe-base HBTs will likely be in the high-frequency, low-noise areas, taking advantages of their high f_T and f_{max}, high Early voltage, and low base resistance. The primary objective of this research is to evaluate various design considerations to improve the performance of SiGe-base HBTs. The research focuses on the engineering of vertical dopant and germanium profiles to optimize device performance, and on the characterization of devices to better understand tradeoffs and fundamental limitations. Issues concerning leverage in analog circuitry and factors influencing important figures of merit will be addressed. We also concentrate on the reliability study of SiGe-base HBT because relatively little information is available. What I intend to accomplish in this thesis is to complement what has been known in the literature and extend them to better understanding, at the same time, exploring new ground.

Figure 1-4 presents a quick overview of the scope of this thesis work. The task is divided into four closely interrelated phases, namely, the material demonstration, process integration, device characterization, and design consideration.

Material Demonstration

Being able to secure reliable material sources for the device fabrication is the first step of this research development. We primarily have relied on a home-built, single-wafer, non-load-locked, quartz-halogen-lamp-heated, very-low-pressure chemical vapor deposition (VLPCVD) system to supply $Si_{1-x}Ge_x$ films for various material studies and device processing. More recently we have gotten films deposited in commercial APCVD systems as well. The detailed operation of the VLPCVD reactor, including the ex-situ and in-situ cleaning procedure, and deposition conditions, will be presented in a later section.

Process Integration

After successful demonstration of deposition of $Si_{1-x}Ge_x$ materials on both blanket and patterned substrates, we then focus on development of process technology and device design. Three process, namely, the "MESA", "LOCOS" and "POLY", are developed for device fabrication. The objective of the fabrication is to yield working devices with excellent current idealities, high current gains and good breakdown characteristics for the experimental study that follows.

Key issues in the process design are compatibility and reduction of parasitics. We try to achieve both flexibility and integration in the design to allow the adaptation for many types of epitaxial deposition such as non-selective or selective, and later modifications, as well as merging into an existing CMOS process. Reducing parasitics usually involves formation of device isolations, contacting of thin base region, providing self-alignment scheme. Certain aspect of process integration will be considered and different isolation schemes need to be emphasized.

Device Characterization

The process technology used for the fabrication is compatible with the MIT/MTL baseline 1.25μm twin-well CMOS process [57]. The photolithography tools allow a minimum feature size of $\sim$1μm. The characterization phase follows successful completion of device fabrication. Extensive DC testings are carried out to extract necessary parameters for process modification and theoretical analysis. Statistical data are summarized to examine device mismatch and device yield. Preliminary reliability stress are performed to understand the degradation behavior of SiGe-base HBTs under forward, reverse operations. Finally, high-frequency measurement and 1/f noise characterization are measured.

Design Consideration

Fundamental behavior of SiGe-base HBT device is very similar to that of the Si homojunction transistors, making design translations from one to the other fairly straightforward. However, optimum circuit performance can only be obtained through a complete awareness of the unique characteristics of SiGe HBTs, and a knowledge of their impacts to circuit performance.

Due to the presence of $Si/Si_{1-x}Ge_x$ heterojunctions at both the emitter-base and collector-base junctions, there are some differences in the physics as well as the approach used in profile optimization. Effects such as Ge and boron profile, base bandgap grading, dopant outdiffusion and parasitics on important device parameters must be closely examined. We will focus on optimizing the vertical germanium and dopant profiles to achieve the desired specifications with the help of device and process simulation programs.

Thesis Organization

The organization of this thesis is as follows. In Chapter 2, device requirements and design considerations of SiGe-base HBTs for analog applications are presented, followed by a discussion on important figures of merit and performance limitations of bipolar transistors. Advantages of incorporating Ge into the structure is elaborated. Chapter 3 is devoted to the development of device fabrication processes. The details of fabrication sequences and key processing steps are described. Highlights from material and device characterization results are presented. Details of the experiments for engineering the vertical profiles are discussed in Chapter 4. Effects of Ge, boron doping, and graded-base profiles are examined in fabricated devices. Device modeling efforts, using a commercial 2-D simulation program (MEDICI), to investigate the issues of displaced p-n junctions with respect to the heterojunction are also included. In Chapter 5, experimental setup used to investigate device degradation under various biasing conditions is presented. Preliminary reliability stresses are carried out to understand the degradation behavior of SiGe-base HBTs. Finally, a conclusion and some suggestions for future research are stated in Chapter 6.

Chapter 2

Design Consideration for Analog Application

SiGe-base HBT has recently emerged as an important device technology for high-speed analog and mixed-signal applications, especially in the wireless and telecommunication areas [28, 58]. Because of its inherent merits, such as high f_T and f_{max}, low noise figure and high Early voltage, SiGe-base HBT is an ideal candidate for providing low cost RF components operating from few hundred MHz to several GHz in wireless communication systems.

Fundamental behavior of SiGe-base HBT device is very similar to that of the Si homojunction transistors, making design translations from one to the other fairly straightforward. However, optimum circuit performance can only be obtained through a complete awareness of the unique characteristics of SiGe HBTs, and a knowledge of their impact on circuit performance.

Due to the presence of $Si/Si_{1-x}Ge_x$ heterojunctions at both emitter-base and collector-base junctions, there are some differences in the physics as well as the approach used in profile optimization. In this chapter, we first examine the design requirements, key figures of merit, and limiting factors of the device, then highlight the design issues associated with base, emitter, and collector profiles for device opti-

Power Amplifier	Low Noise Amplifier	Linear Amplifier	Wideband Amplifier	Oscillators
Gain High voltage High current Low thermal resistance Power density Efficiency Linear Low 1/f noise	Gain Low NF Linear Low dc consumption	Gain Efficiency Low NF Moderate output Complementary	Gain Bandwidth Efficiency Low-Q impedance Output power	Gain Low 1/f noise Linear Low voltage Efficiency

Table 2.1: Summary of device requirements of various amplifier circuits [59].

mization.

2.1 Device Requirements

The device requirements and design procedures of heterojunction transistors are in many ways identical to those of homojunction transistors. Requirements of various amplifier circuits are summarized in Table 2.1 [59]. In general, desired device characteristics include the following: high current gain and Early voltage — large value of β and V_A, high-frequency AC operation — high f_T and f_{max}, fast switching speed — small τ_F, high device breakdown voltages — high BV_{CEO}, BV_{EBO}, and BV_{CBO}, minimum device size, and high reliability operation. This represents a very demanding yet conflicting set of performance requirements from the devices.

High current gain and Early voltage are desirable in order to minimize the circuit complexity required to achieve a given linearity specification. High Early voltage also allows for faithful amplification of AC signals. In achieving high-frequency AC performance, high f_T and f_{max} are essential for minimizing voltage settling time when driving large capacitive loads. To obtain high f_T and f_{max}, and fast τ_F, the para-

sitic resistances — R_E, R_B, and R_C, and the parasitic junction capacitances — C_{BE}, C_{BC}, C_{CS}, of the transistor must be minimized. Equally important are the DC accuracy parameters. In particular, good device-to-device parameter matching, especially of forward turn-on voltage $V_{BE(on)}$ and current gain β, is important for acceptable threshold uniformity or DC linearity [60]. Moderately high breakdown voltages are essential for accommodating large dynamic range signals. Finally, minimization of device sizes achieves high functional density, reduces device parasitics, and lowers power dissipation which is crucial in low-power application.

2.2 Figures of Merit

We have presented in the last section some of the device requirements desired for analog circuit applications. We will now focus the discussion on few important figures of merit.

Current Gain

The (common-emitter) current gain of a bipolar transistor is defined by the ratio of the collector current to the base current. From equation (1.14), a general expression of the current gain can be obtained:

$$\beta = \frac{\int_{\text{em}} \frac{n(x)}{n_{ie}^2(x) D_{pe}(x)} dx}{\int_{\text{base}} \frac{p(x)}{n_{ib}^2(x) D_{nb}(x)} dx} \tag{2.1}$$

If we assume uniform doping profiles and constant diffusion coefficients, equation (2.1) can be simplified to a more familiar form,

$$\beta = \frac{D_{nb} W_E N_{de}}{D_{pe} W_B N_{ab}} \exp\left(\frac{\Delta E_g}{k_B T}\right) \tag{2.2}$$

where ΔE_g is the bandgap difference between the emitter and base materials. The gain of a heterojunction bipolar transistor is therefore larger than that of a conventional one by the exponential factor $\exp(\Delta E_g/k_BT)$. In the $Si_{1-x}Ge_x$/Si system with (x=0.2) for example, ΔE_g has a value of ~0.15eV, giving a current gain improvement by a factor of nearly 400.

f_T and f_{max}

The frequency at which the transistor incremental current gain drops to unity is called the current-gain cutoff frequency (f_T). The cutoff frequency of the device is determined by the transit time of carriers from emitter to collector (τ_{EC}) [42], i.e.

$$\begin{aligned} \frac{1}{2\pi f_T} &= \tau_{EC} = \tau_E + \tau_B + \tau_C + \tau_{C'} \\ &\approx \frac{k_BT}{qI_C}(C_E + C_C + C_p) + \frac{W^2}{\eta D_B} + \frac{x_C - W}{2v_s} + R_CC_{BC} \end{aligned} \tag{2.3}$$

where τ_E, τ_B, τ_C and $\tau_{C'}$ are transit times through the emitter, base, collector and base-collector depletion region, respectively. In particular, the base transit time τ_B can be greatly reduced by introducing an aiding drift field by grading the base germanium fraction of a SiGe-base HBT.

Another important high-frequency figure of merit is the maximum oscillation frequency (f_{max}) or the unit power gain frequency, at which the power gain of a transistor reaches unity. f_{max} depends critically on the intrinsic device profile as well as parasitics; it is usually expressed as:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_BC_{BC}}} \tag{2.4}$$

SiGe-base HBT can have significantly higher f_{max} than a conventional Si homojunction bipolar transistor because of lower R_B achievable. The base-collector capacitance depends on the isolation technology; in state-of-the-art processes, trench isolation or

air-bridge technology have been employed to reduce C_{BC}.

The Early voltage

The Early voltage V_A is a measure of the so-called "base-width modulation" effect, in which the base width of bipolar transistors decreases as the collector-base junction voltage increases due to the widening of depletion region. As result, the collector current increases with V_{CB}, leading to a finite output resistance. A large value of V_A is desired because it yields high device linearity and large DC voltage gain, both are important in analog applications [61].

In the common-emitter configuration, V_A is given by [19]

$$V_A = J_C \frac{\partial V_{CE}}{\partial J_C} - V_{CE} \approx J_C \frac{\partial V_{CB}}{\partial J_C} \tag{2.5}$$

Substitute equation (1.14) for J_C, it can be shown that

$$V_A = \frac{q}{C_{BC}} n_i^2(W_B) D_n(W_B) \left[\int_0^{W_B} \frac{N_A(x)}{n_i^2(x) D_n(x)} dx \right] \tag{2.6}$$

Traditionally, in the design of HBT, the Early voltage is improved as result of heavy base doping; the improvement mainly comes from the integral term in equation (2.6). An additional important feature to note, from equation (2.6), is that the Early voltage has an explicit dependence on $n_i^2(W_B)$. Therefore, we may exploit the fact to increase the Early voltage by introducing a large Ge fraction near the base-collector edge.

Transconductance

The most important parameter that can be measured using low-frequency signal excitation is the transconductance g'_m. HBTs, like most bipolar transistors, can potentially have very high g'_m because of the inherent exponential output current-input

voltage relationship. The high g'_m permits small input voltage swings and facilitates low common-collector output impedance for fast charging of load capacitances.

At low frequencies, g'_m can be expressed as follows

$$\frac{1}{g'_m} = \frac{kT}{qI_c} + r_{e'} + \frac{r_{bb'}}{\beta} \tag{2.7}$$

Note, by extrapolation to zero $I_C{}^{-1}$, the emitter series resistance can be determined.

1/f Noise and Noise Figure

1/f noise can arise from resistance fluctuations due to fluctuations in the number of carriers or fluctuations in mobility. It can also be caused by generation-recombination due to distribution of trap levels at the Si-SiO_2 interface. 1/f noise imposes a fundamental lower-limit to low-frequency device noise. Bipolar transistors inherently has low 1/f noise, as a result of the fact that the intrinsic device is relatively well shielded from surfaces and bulk traps.

At medium and high frequencies the noise figure NF, i.e. the reduction factor of the signal to noise power ratio, can be approximate by [62]

$$NF = 1 + \frac{1}{R_s}\left[r_b + \frac{r_e}{2} + \frac{(r_b + R_s)^2}{2\beta r_e} + \frac{(r_b + R_s)^2}{2r_e}\left(\frac{f}{f_T}\right)^2\right] \tag{2.8}$$

where R_s is the source resistance, r_b is the base resistance, β is the current gain, r_e is k_BT/qI_C and f_T is the cutoff frequency. Thus, SiGe-base HBTs, featuring low base resistance R_B, high beta β and high f_T, can result in a substantial reduction of the noise figure.

2.3 Vertical Profile Design

A bipolar device can be divided into intrinsic and extrinsic regions. The intrinsic device accounts for the profile design associated with the emitter and the underlying base and collector regions and junctions. Extrinsic device concerns include parasitic resistances in series with the intrinsic regions, and capacitances associated with the base-collector and the collector-substrate junctions. Minimization of parasitic device capacitance is especially important for achieving wide bandwidth performance with reasonable power dissipation.

The principal benefit of using $Si_{1-x}Ge_x$ as base is the freedom to change doping levels in emitter and base without significant constraints by injection efficiency, and thereby to re-optimize the transistor at a higher performance level. In this section, the emitter, base and collector layers and their impacts on the device performance will be considered. In order to fully exploit the advantages of $Si_{1-x}Ge_x$, the layer parameters must be optimized according to the particular application of the transistor, e.g. low noise, high frequency, or high power applications. [63, 64]

2.3.1 Base design issues

Most key tradeoffs in the optimization of heterojunction bipolar transistors come from the base profile design. Important device parameters such as current gain β, Early voltage V_A, base resistance R_B, are all intimately related to the base profiles. High base doping is desired because it reduces the base resistance and gives higher Early voltage. However, increase of base charge will degrade the current gain and high frequency performance.

Current Gain versus Base Doping

Optimization of the base profile is driven by the base resistance R_B, current gain β and the base transit time τ_B considerations.

Base resistance is one of the most important electrical parameters of a bipolar transistor. It limits the rate at which the input capacitance can be charged or discharged. It also causes the undesirable emitter crowding effect. As the AC and DC currents flowing through the base layer, an I-R drop is produced that tend to reduce the forward bias V_{BE} of the base-emitter junction. As a result, the center of emitter regions ceases to conduct current during transistor operation at high current levels and high frequencies, reducing the device transconductance. High base doping is also needed to prevent early punchthrough of the device. As base regions are made thinner in an attempt to shorten transit time, a limit is established by the fact that at high collector-base biases the depletion region may extend all the way across the base and reach the emitter depletion region.

For the intrinsic transistor, most of the key tradeoffs come in the base profile design. The base Gummel number Q_B, which is defined as the integral of the base dopant between the two space charge layers of the junctions, sets the collector saturation current and the peak current gain. Since β, which is typically around 100, is inversely proportional to Q_B, the current gain sets a constraint on the maximum base doping allowed. This is traded off against the base resistance of the active base region; an increase in the base doping reduces R_B, which has a favorable impact on the switching speed of the device at higher current densities. An R_B of 300Ω or less is achievable in high performance devices.

The minimum doping level in the base is also constrained be the requirements of punchthrough and the Early voltage V_A, which is a measure of the sensitivity of the collector current to changes in the base width. Increasing reverse bias of the collector-base junction causes the spreading of the depletion region edge into the base, which reduces the neutral base width and increases the collector current. A similar effect occurs as a function of changes in the bias across the emitter-base junction. The emitter-base effect is usually only noticeable for very narrow bases. Doping level in the modern transistors are usually sufficient so that the Early voltage is not a critical

parameter in digital designs. A value of 15 to 20 volts is acceptable for digital circuits, while analog applications require an Early voltage of at least 30 volts.

Heavy Base Doping

With sufficient high peak doping in the base, the current density is on the order of $1\text{mA}/\mu\text{m}^2$ before the Webster effect becomes important. The cost of suppressing high-level injection and punchthrough is that the mobility in the base decreases and thus the base transit time suffers. The high doping in the base is beneficial in that the increase in intrinsic carrier concentration caused by bandgap narrowing favorably impacts the beta of the device, as well as decreases the sensitivity of the device to change in temperature.

The high base doping also allows design flexibility to avoid high level injection effects, such as Kirk and Webster effects, until current densities of 1×10^5 A/cm^2 or higher are reached, giving HBTs exceptionally high current density potential.

Graded Base

As described earlier, it is a common practice in the design of SiGe-base HBTs to incorporate graded germanium profiles in the base to provide an aiding drift field.

In homojunction devices, drift field created by doping gradient are on the order of

$$E_{\text{drift}} \approx \frac{k_B T}{q} W_B \ln\left(\frac{N_{Ao}}{N_{Af}}\right) \tag{2.9}$$

where N_{Ao} and N_{Af} are the acceptor concentrations at the beginning and the end of the quasineutral base. This field is typically of the order of $2k_BT/q$ across 500 to 1000-Å base regions, or $\sim$ 2kV/cm. With graded base HBTs, fields 2 to 5 times larger are easily implemented. The gradient of bandgap can provide an aiding drift field greater than 5kV/cm which reduces the base transit time (τ_B) significantly. Performance improvement, as much as of 50% increase in f_T, has been reported [15].

$$\frac{\beta_{\text{SiGe}}}{\beta_{\text{Si}}} = \frac{J_{\text{SiGe}}}{J_{\text{Si}}} = \frac{\frac{\delta E_g}{k_B T} exp(\frac{\Delta E_{go}}{k_B T})}{1 - exp(-\frac{\delta E_g}{k_B T})} \tag{2.10}$$

$$\frac{V_{\text{A,SiGe}}}{V_{\text{A,Si}}} = \frac{k_B T}{\delta E_g}\left[exp\left(\frac{\delta E_g}{k_B T}\right) - 1\right] \tag{2.11}$$

$$\frac{\tau_{SiGe}}{\tau_{Si}} = 2(\frac{k_B T}{\delta E_g})\left[1 - \frac{k_B T}{\delta E_g}\left(1 - exp(-\frac{\delta E_g}{k_B T})\right)\right] \tag{2.12}$$

$$\Delta E_g(x) = \Delta E_{go} + \frac{x}{W}\frac{\delta E_g}{k_B T} \tag{2.13}$$

Table 2.2: Key formulae for graded base structures.

For reference purpose, some useful formulae for calculation of graded-base structures are included in Table 2.2 [21].

2.3.2 Emitter Design Issues

In conventional bipolar transistor design, doping of the emitter is made on the order of 1×10^{20} cm^{-3} to improve emitter injection efficiency and increase current gain while keeping emitter resistance R_E low. The high emitter doping level suffers from bandgap narrowing and can cause problems such as low junction breakdown and undesirable tunneling. Reliability of the emitter-base junction under moderate reverse bias becomes an issue for many classes of circuits. An additional design concern for the emitter junction is the hot carriers generated under reverse bias conditions, due to the large electric fields along the periphery of the emitter-base junction. The generated carriers tend to increase the fixed oxide charge density, resulting in a degradation in current gain.

SiGe-base HBT offers a good solution to the above-mentioned problems. Lower emitter doping can be used to reduce base-emitter junction capacitance C_{BE} and to

improve the junction reliability. For small-signal microwave amplification, reduction in the emitter-base capacitance will significantly reduce the noise as well.

However, the emitter doping level can not be reduced without limit. The price of reducing emitter doping level is an increase of emitter resistance. Emitter resistance will become an even more limiting factor at smaller device dimensions, as a result of the increasing current density desirable for device scaling. In addition, the reliability of the emitter contact may become questionable with resistance increasing after prolonged stressing at high forward current densities.

In device with lightly-doped emitter structures, boron outdiffusion is likely to occurs, shifting the location of the p-n junction with respect to the heterojunction and causing additional degradation. The location of the Ge profile with respect to the metallurgical emitter-base junction plays a key role in the DC and AC characteristics of the HBT as will be discussed in a later section.

Emitter Resistance

Emitter resistance is shown to degrade the differential voltage gain at the switching point of a differential pair, reducing noise margin, speed, and voltage swing [65]. It is also an important factor in comparators because variation of the voltage $I_E \cdot R_E$ limits comparator accuracy. When R_E is large, a comparator must operate at low current to retain good ΔV_{BE} characteristics, and this further reduces achievable speed. The area of the emitter contact is roughly equal to the area of the intrinsic device. Values of intrinsic g_m achievable with bipolar transistors are very high (up to 40mS/μm^2 of emitter), but the extrinsic g_m may be limited if R_E is not maintained below 10 to 50 Ω-μm^2.

2.3.3 Collector Design Issues

The main tradeoff in the collector region comes from the contradicting requirements of high speed and high breakdown voltage. The issue is further compounded by the limitations of Kirk effect and collector resistances, as well as the base-collector junction capacitance. The choice of the collector profile is dictated by conflicting requirements to simultaneously optimize the breakdown voltage BV_{CEO}, the base-collector signal delay τ_{bc}, the "knee" current density J_k at which the f_T rolls off, and the intrinsic base-collector capacitance.

Tradeoff between f_T and Breakdown Voltage

Traditionally, analog circuits require larger power supply levels. The output power capability of an HBT is strongly influenced by the design of the collector layer [66, 67]. Thicker and lightly doped collector layers are always desired to sustain a large breakdown voltage at the base-collector junction. However, the requirement for a thick collector must be balanced by the need for a short transit time through the collector layer. A rule of thumb in the design of power HBTs is to select a collector thickness that produces about 50% of the emitter-collector transit time delay.

Analysis of the tradeoff between a short collector transit time across the collector space-charge region and the collector-base breakdown voltage has been carried out [68]. Assume for an one-sided abrupt junction, the breakdown voltage can be expressed as,

$$BV_{CBO} = E_{cr} \cdot w_C \tag{2.14}$$

where E_{cr} is the critical field and w_C is the depletion width. And, the collector transit time is

$$\tau_C = \frac{w_C}{2v_s} \tag{2.15}$$

where v_s is the saturation velocity. If we further assume that $f_T = 1/2\pi\tau_C$, the

so-called Johnson's limit can be obtained:

$$f_T \cdot BV_{CBO} = \frac{E_{cr} \cdot v_s}{2\pi} \tag{2.16}$$

Note that the product of $f_T \cdot BV_{CBO}$ only depends on material parameters of silicon. The theoretical value is found to be ~200 GHz·V.

Base Pushout or Kirk effect

An important limit on collector current density for bipolar transistors is the base pushout or the Kirk effect [69].

As the collector-current density J_C of an npn transistor increases, the density of electrons being transported across the C-B space charge region also increases. When the density of electrons injected into the C-B junction becomes comparable to the doping on the collector side of the space-charge region, i.e. a condition corresponding to high-level injection, the total charge in this region becomes significantly reduced from that under low-level injection conditions, leading to a lower electric field gradient in the C-B junction.

The onset of high-level injection occurs at the critical current density J_C given by

$$J_C = qv_s \left(N_D + \frac{2\epsilon_s(V_{CB} + V_{Bi})}{qW_C^2} \right) \tag{2.17}$$

; i.e. when the electron density ($n_C = J_C/qv_s$, where v_s is the saturation velocity) attains a critical value of

$$n_C = N_D + \frac{2\epsilon_s(V_{CB} + V_{Bi})}{qW_C^2} \tag{2.18}$$

where W_C is the collector layer width, V_{CB} is the base-collector bias, and V_{Bi} the base-collector built-in potential, then the electrostatic field at the edge of the base vanishes. Above this current density, holes penetrates into the collector and the space-

charge region edge in the base moves toward the collector, effectively increasing the base width. This phenomenon is known as the base pushout or the Kirk effect. Due to the increased effective base width and the increased hole storage, the switching speed and current gain are now degraded. In order to raise the onset of this effect, increasing values of collector doping are required as devices are scaled at constant current density.

Increasing the collector doping N_C level significantly above 1×10^{17} cm^{-3} improves the frequency performance in two ways: 1) it reduces τ_{bc}, and 2) it allows operation at higher collector current densities since the Kirk "knee" current J_k is proportional to the collector doping. Therefore, higher N_C results in higher f_T since the delay component associated with emitter and collector capacitances is reduced.

However, delay in the onset of the Kirk effect achieved with increased collector doping must be traded off against collector-base capacitance C_{BC} and breakdown (BV_{CBO} and BV_{CEO}) considerations. The breakdown voltage requirement will restrict the maximum doping allowed in the collector. The tradeoff between J_C and C_{BC} should be optimized according to the operating point of the transistor. For low current densities, which is often used for ECL circuits where power is an issue, the switching speed is limited by charging of the parasitic capacitances, and so C_{BC} should be minimized. For high current density applications, which includes bipolar transistors used in BiCMOS gates, the speed will be limited by the intrinsic device characteristics, and so the collector profile should be optimized to control base push out.

Collector Resistance

The use of epitaxially grown layer in bipolar transistors is common practice since performance can be considerably improved with respect to breakdown voltage and power handling capability. The problem associated with the epitaxial structure is high collector resistance which has a dominant effect on the propagation delay of a

BiCMOS gate under heavy capacitive loading. At high current levels or at a relatively low collector-emitter voltage, the voltage drop over the collector resistance can lead to forward biasing of the internal junction. This effect is called quasi-saturation and has been the subject of several publications. Quasi-saturation leads to current gain and cutoff frequency fall off at higher current levels. The onset of quasi-saturation also has a dominant influence on the distortion behavior of the bipolar transistor. For high performance bipolar transistors, a heavily-doped buried layer used underneath the epitaxial layer. This is necessary to minimize the collector resistance.

2.4 Summary

SiGe-base HBT is gaining increasing attention because of the rapid growth and demand of the wireless and telecommunication products [28]. The superior device characteristics of SiGe HBTs suggest that amplifiers and oscillators operating up to 20GHz and 40GHz respectively can be built from this technology. This open up the door for providing highly integrated, low power consumption, low voltage, surface mount transceiver integrated circuits.

We have discussed in this chapter the device requirements and design considerations of SiGe-base HBTs for high-speed, analog applications. Most of the tradeoffs occur in the design of the base and collector profiles. Transistor optimization for analog designs involves the same parameters as for the digital case, e.g. low base resistance, high f_T, low base collector capacitance and so on, but with addition of extra figures of merit such as $\beta \cdot V_A$, low noise figure, and high current driving capability. Careful design of the bandgap profile is crucial in optimizing the device performance. Traditionally, analog circuits require much higher power supply levels than digital. Thus, it important to examine issues such as the tradeoff between f_T and the breakdown voltage BV_{CEO}. Low collector doping levels and thick n- epitaxial layers are needed to achieve high values BV_{CEO} but at the cost of poor high frequency

performance.

Chapter 3

Device Fabrication and Characterization

The focus of this research is to evaluate the performance leverages of SiGe-base HBTs for analog application. The primary objective of the HBT process is to obtain transistors with near-ideal characteristics for the study.

In the first part of the chapter, process developments leading to successful fabrication of SiGe-base HBTs are presented. Three device fabrication sequences — the "MESA", the "LOCOS", and the "POLY" processes — are described, followed by a discussion on the key processes involved, which include the epitaxial deposition using the Very-Low-Pressure Chemical Vapor Deposition (VLPCVD), and thermal annealing for implant activation.

The second half of the chapter is devoted to the device characterization. After successful completion of device fabrication, DC testings are carried out extensively to extract necessary parameters for further process modification as well as theoretical analysis. Statistical data on the current ideality factors are generated to examine the device yield and the device matching. Measurements of breakdown voltages, 1/f noise characteristics, and parasitic elements are also performed. Detailed study to examine the effects of germanium, boron doping, and Ge gradient on device characteristics

is presented in the next chapter. High-current and high-voltage stress experiments leading to device reliability study are discussed in Chapter 5.

3.1 HBT Fabrication Processes

In this section, the three process sequences — "MESA", "LOCOS", and "POLY", developed for the device fabrication, are presented.

The "MESA" process is originally designed as a demonstration vehicle to prove viability of the VLPCVD-deposited $Si_{1-x}Ge_x$ materials for HBT fabrication [70]. The transistor structure features a junction-isolated base-emitter junction, a mesa-isolated base-collector junction, and a low thermal budget. Epitaxial layer of in-situ doped $Si/Si_{1-x}Ge_x/Si$ sandwich structure is first deposited on a blanket n+ substrate. The transistor active areas are patterned using plasma etch, forming mesa-like structures. Arsenic and boron/BF_2 are subsequently implanted through the epitaxial layers, making ohmic contacts to the emitter and base layers from the top surfaces. The heavily doped n+ substrate is used as the collector electrodes. The process is relatively simple and requires only few number of processing steps and masking layers. However, a major setback associated with the process is that fabricated devices are lacking natural isolations.

To address the device isolation issue, the "LOCOS" process is developed, in which a LOCOS oxidation step is incorporated into the "MESA" process prior to the $Si/Si_{1-x}Ge_x/Si$ deposition. The process also involves modifying reactor recipe to allow epitaxial deposition of $Si/Si_{1-x}Ge_x/Si$ sandwich structure on patterned substrates. Due to the limitation of the VLPCVD reactor, we are restricted to mixed-mode deposition, i.e. single crystalline (epitaxial) deposition occurs inside patterned window regions while polycrystalline material nucleates on the field oxide. Issues, such as in-situ cleaning, pattern sensitivity, and faceting problem, associated with deposition on patterned substrates have been examined elsewhere [71]. The remain-

ing processing steps, after the epi deposition, follow pretty much the same sequence as the "MESA" process.

Although devices fabricated from both "MESA" and "LOCOS" schemes exhibit reasonably good characteristics (to be shown later), the structures are nonetheless mesa-type in nature, and potentially have several disadvantages:

(1) ion implantations which are typically used to contact active regions, are shown to result in enhanced dopant outdiffusion;

(2) large parasitics associated with the mesa structure, in particular the extrinsic base resistance and base-collector capacitance, severely limit the device performance; and,

(3) devices are fabricated on n+ substrates, lacking electrical isolations.

In light of these limitations, the "POLY" process is proposed and developed to address these concerns. It is an attempt to scale the devices laterally to minimize parasitic resistances and capacitances. This double-poly process, combined with fine emitter dimensions, can potentially alleviate all the above-mentioned difficulties. The device structure uses the two levels of polysilicon as extensions to make contact with the base and emitter, and to allow pseudo-self-alignment between the emitter and extrinsic base regions. This process is also more compatible with the standard industrial practice and is capable of merging into an existing CMOS process. In developing the process, we try to achieve both flexibility and integration to allow adaptation of many types of epitaxial deposition — such as non-selective or selective, and later modifications.

3.1.1 The "MESA" Process

In this section, the detailed processing sequence of the "MESA" scheme is discussed. Most of the device characterization results presented in this thesis are performed on devices obtained from successful completion of this process.

The basic process flow is outlined in Figure 3-1 and a schematic diagram of the corresponding cross section is shown in Figure 3-2. The fabrication sequence is adapted from the MIT–BiCMOS process [72,73], and refined to accommodate epitaxial SiGe-base structures [70].

Starting wafer is a 4-in, (100), Sb-doped, 0.005–0.02 Ω-cm, silicon substrate. After treated with the standard ex-situ cleaning procedures (to be described in the next section), the wafer is transferred into the VLPCVD system for in-situ doped $Si/Si_{1-x}Ge_x/Si$ epitaxial deposition. Alternatively, $Si/Si_{1-x}Ge_x/Si$ layers deposited in a commercially available Atmospheric-Pressure (APCVD) system have been used in the device fabrication. Typical device profile is shown in Figure 3-3.

After the deposition of $Si/Si_{1-x}Ge_x/Si$ sandwich structure, 500Å of low temperature oxide (LTO) is first deposited to protect the wafer surface. In the first masking step, $Si/Si_{1-x}Ge_x/Si$ is etched by plasma, forming mesa-like structures, to define the device active areas and to lay down alignment marks for subsequent photolithographic steps. After the mesa etch, a Boron/BF_2 double implant is performed to allow contacting the thin SiGe-base region from the top surface, followed by a second mesa etch to open up regions for collector contacts. Then, a shallow arsenic implant is performed to contact the emitter and collector regions. 5000 Å of low-temperature oxide deposited at 400°C provides device passivation. After the passivation step, an 800°C, 20-minute furnace anneal in nitrogen ambient is used to activate implants. This thermal step represents the highest temperature step after the deposition of $Si/Si_{1-x}Ge_x/Si$ structure. It is important to keep the thermal treatment to the minimum because of the metastable nature of the films. During the annealing step, the LTO passivation is densified to improve the oxide and interface quality.

Finally, opening of contact cuts, depositing and patterning of metal, and sintering in forming gas, complete the backend of the fabrication sequence. The sixth mask is used to open contact windows over the emitter, base and collector, and this is followed by sputtering of a layer of metal (400Å Ti + 1μm Al/1%Si) over the entire wafer.

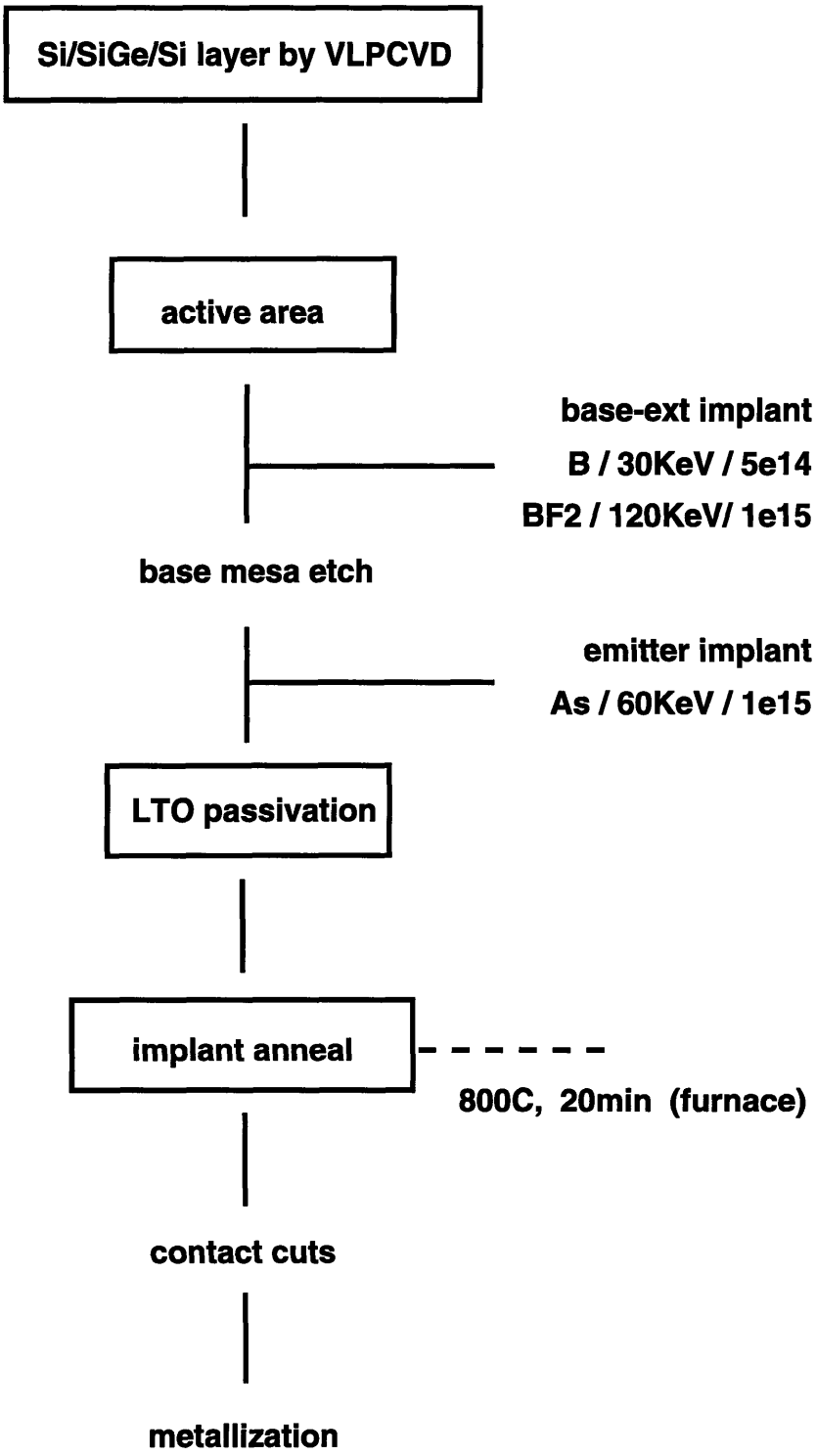


Figure 3-1: Basic flow sequence of the "MESA" process.

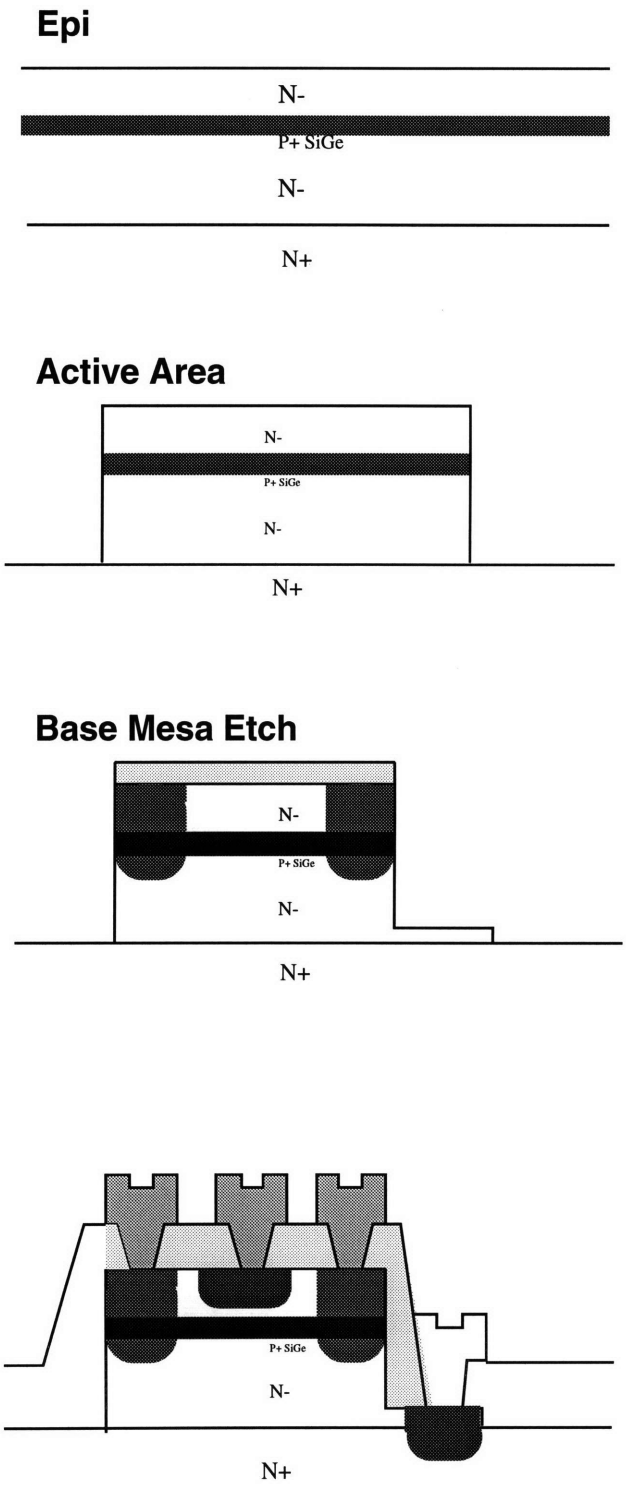


Figure 3-2: Cross sectional schematic diagram of the "MESA" process for the SiGe-base HBT fabrication.

Si	n-emitter	6×10^{17} cm^{-3}	1500 Å	625 – 675°C
$Si_{1-x}Ge_x$	p-base	7×10^{18} cm^{-3}	500 Å	625 – 675°C
Si	n-collector	6×10^{16} cm^{-3}	3400 Å	800°C
Si	n-buffer	6×10^{17} cm^{-3}	500 Å	800°C
$< 100 >$, N+, Silicon Substrate				

Figure 3-3: Typical parameters of $Si/Si_{1-x}Ge_x/Si$ heterostructure used for the device fabrication.

The last mask then defines the metal interconnects between the devices and probe pads. The final process step is a 400°C sintering in forming gas, which is needed to give low-resistance ohmic contacts. The presence of the hydrogen helps reduce the density of surface states at the oxide/silicon interface, especially at the mesa sidewall region. This step is crucial in obtaining good device characteristics because the surface states can give rise to generation/recombination centers in the emitter-base depletion region and degrade current ideality factors. The alloying process therefore serves the important function of improving the current gain of the transistor at low current densities.

3.1.2 The "LOCOS" Process

The "LOCOS" process is a modified version of the "MESA" process, developed to address the disadvantage of the "MESA" process. Instead of being deposited on blanket substrates, $Si_{1-x}Ge_x$ epitaxial layers are deposited on LOCOS-patterned wafers in the "LOCOS" process. Initially, buried collectors and LOCOS oxidation are set in place before the epitaxial deposition, forming low resistive contact paths and device isolations. Issues related to the deposition on patterned substrates have been well investigated by previous co-workers and will not be discussed in detail here [71]. The

remaining processing steps follow pretty much the same sequence as the "MESA" process. The device performances obtained with the "LOCOS" process are essentially the same as those with the "MESA" process, if not slightly worse due to the extra complication of deposition on patterned substrates. Thus, the main advantage of the "LOCOS" process is in achieving device integration and not in improving performance.

3.1.3 The "POLY" Process

A schematic cross-sectional diagram of the "POLY" process is illustrated in Figure 3-4. The detailed process description and mask identification are included in Appendix B. Modifications to the existing process flow are made to incorporate into the device structure a polysilicon-emitter layer which is more compatible with industrial practice.

A brief description of the process flow is as follows. The starting wafer is a 4-in, (100), Sb-doped, 0.005–0.02 Ω-cm, silicon substrate, with 1μm of lightly n-doped epitaxial collector layer on top. Initially, LOCOS oxidation is performed to define the device active area and to lay down alignment marks for subsequent photo-lithographic steps. After the LOCOS oxidation, ~1000Å of polysilicon is deposited and implanted with boron, followed by a plasma etch step to pattern the poly layer into base handles and, at the same time, open up in active regions the windows for the Si/SiGe/Si epitaxial deposition.

In-situ doped Si/SiGe/Si sandwich structure, with 15% Ge and base width of 500Å, is deposited at 625°C in a commercial ASM-Epsilon-One reactor, using a SiH_2Cl_2-based process. The deposition provides high-quality single crystalline growth in the device regions and polysilicon deposition over the poly and isolation regions. Typical process recipe of the reactor for depositing $Si_{1-x}Ge_x$ alloys is listed in Table 3.1 [74].

The next photo-lithography step removes the excess poly material nucleated on

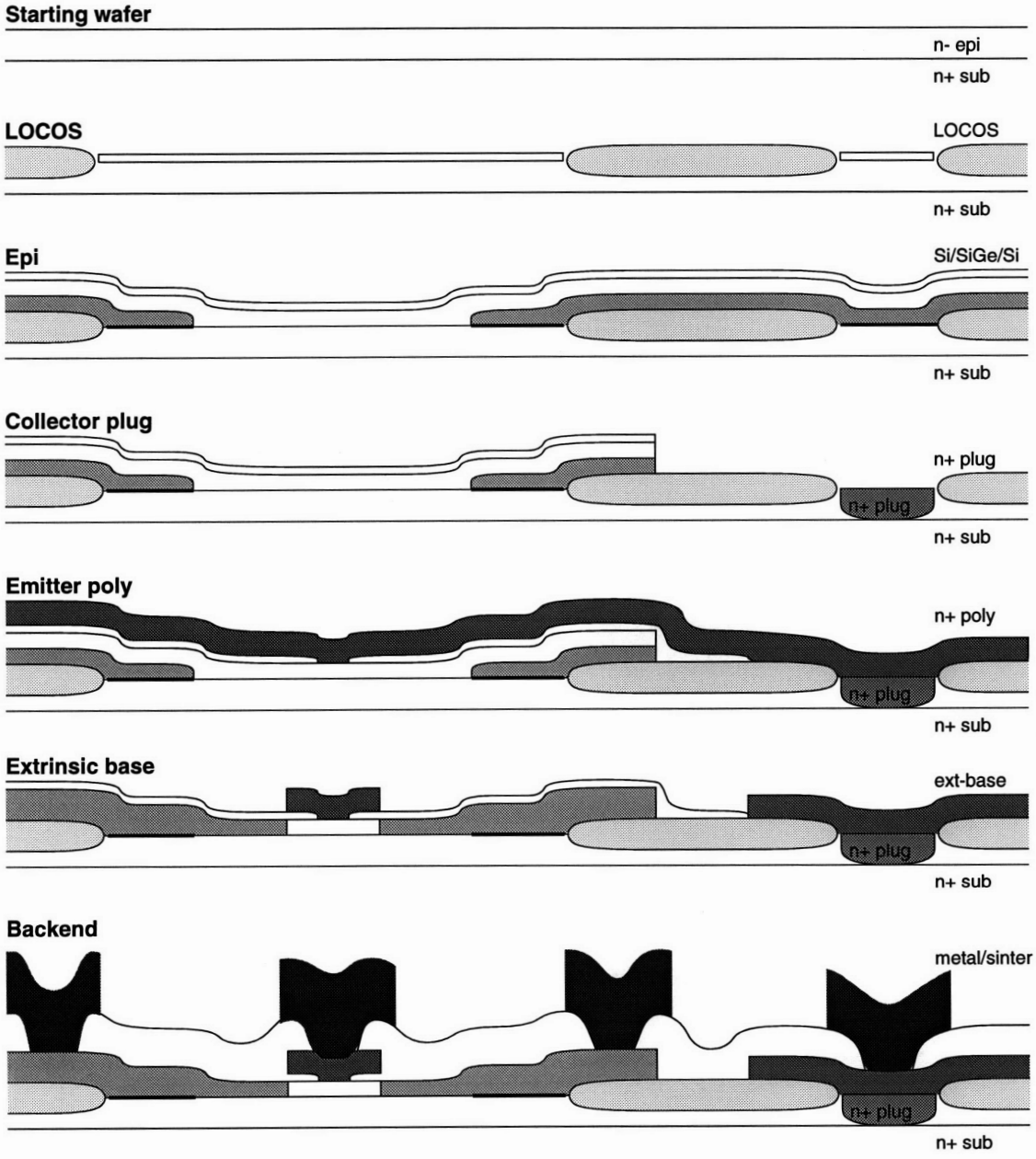


Figure 3-4: Cross sectional schematic diagram of the "POLY" process for the SiGe-base HBT fabrication.

Step	Temp (°C)	Time (sec)	H_2 Flow Rate (slm)	SiH_2Cl_2 Flow Rate (sccm)	10% GeH_4 Flow Rate (sccm)	HCl Flow Rate (sccm)
Load Wafer	900	15	20	0	0	0
Heat-up	1180	40	20	0	0	0
H_2 bake	1180	180	20	0	0	0
HCl etch	1180	30	40	0	0	600
Cool	1100	30	40	0	0	0
Deposit Si	1100	30	40	100	0	0
Cool	625*	180	40	0	0	0
Deposit SiGe	625*	600*	20	20*	2*	0
Unload wafer	625*	15	20	0	0	0
* Typical values only.						

Table 3.1: Typical process recipe for depositing $Si_{1-x}Ge_x$ alloys in the APCVD [74].

the field oxide during epi deposition, and, clears collector regions for n+ plug implant. After the collector plug implant, a 500Å of low temperature oxide is deposited and subsequently densified, serving as dielectrics that separates the polysilicon emitter and extrinsic base regions. The emitter openings are then opened through the LTO layer, followed by a deposition of ~3000Å emitter poly. The emitter polysilicon layer is subsequently doped by a phosphorus implant with 3×10^{15} cm^{-2} dose, at 60KeV of energy. After the phosphorus implant, the wafer receives a brief thermal treatment to partially activate the dopant. This step helps improve the etching uniformity of the poly layer during the patterning step that follows. After the patterning of N+ poly and before removing of the photoresist, a boron/BF2 self-aligned implant is performed to further reduce the extrinsic base resistance. Then, a 5000Å of low-temperature oxide is deposited at 400°C to provide device passivation. An 800°C, 20-minute furnace anneal in nitrogen ambient is performed to activate implants. Finally, opening of contact cuts, depositing and patterning of metal, and sintering in forming gas, complete the fabrication sequence.

3.2 Fabrication Technology

We have discussed the process sequences developed for the device fabrication in the last section. We will now focus attention on the fabrication technology. The process technology used for the fabrication is compatible with the MIT/MTL baseline 1.25μm twin-well CMOS process [57]. The photo-lithography tools allow a minimum feature size of $\sim$1μm. Several important key processing steps, including the epitaxial deposition of Si/$Si_{1-x}Ge_x$/Si films using the VLPCVD reactor and the annealing cycle for implant activation, will be discussed.

3.2.1 $Si_{1-x}Ge_x$ Deposition by VLPCVD

We primarily have relied on a home-built, single-wafer, non-load-locked, quartz-halogen-lamp-heated, very-low-pressure chemical vapor deposition (VLPCVD) system to supply $Si_{1-x}Ge_x$ films for various material studies and device processing. More recently we have gotten films deposited in commercially available APCVD systems as well.

The operating procedure, ex-situ and in-situ cleaning steps of the Very Low Pressure Chemical Vapor Deposition (VLPCVD) reactor are described in this section.

Description of VLPCVD

The details of the VLPCVD reactor have been described elsewhere [75, 76]. A schematic diagram of the VLPCVD reactor, taken from Ref. [70], is shown in Figure 3-5. The cylindrical growth chamber is constructed of quartz and is water cooled at both ends during operation to prevent excessive heating of the stainless steel seals (Kalrez). The growth chamber is evacuated by a turbopump capable of reaching a base pressure of 1×10^{-8} Torr at room temperature, and 1×10^{-7} Torr at the bakeout temperature of 800°C. Heating of the wafer is provided by a bank of six 6kW, high-intensity, tungsten-halogen lamps that situates outside the quartz chamber. Temper-

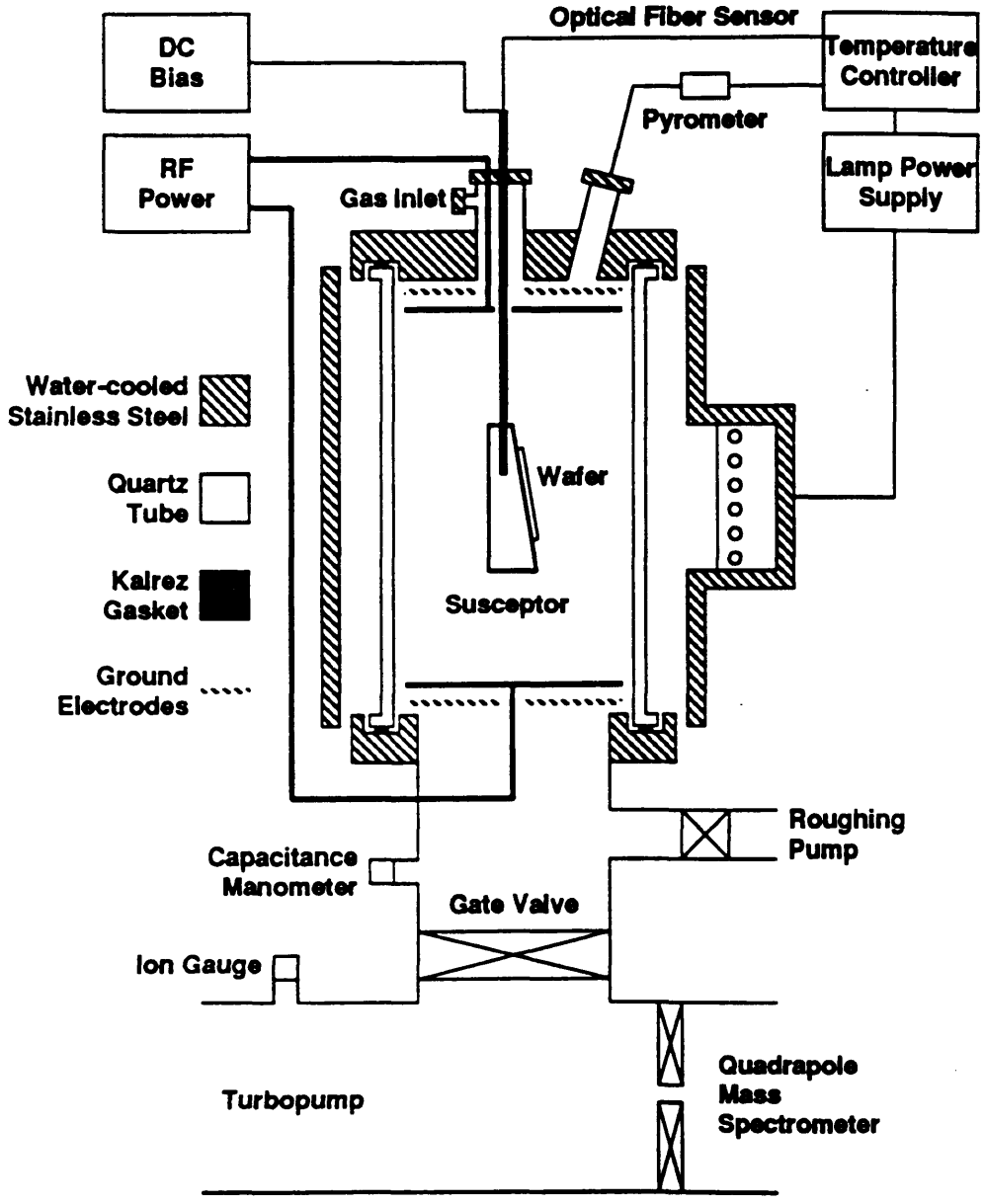


Figure 3-5: Schematic diagram of the Very-Low-Pressure Chemical Vapor Deposition (VLPCVD) reactor used in this work [70].

ature of the chamber is controlled by adjusting the lamp supply voltages; maximum temperature is limited to slightly over 850°C. Actual temperatures during a run are estimated from pyrometer and optical fiber readings. Calibration of the temperature with thermocouple is routinely carried out to ensure accuracy.

The wafer rests on a relatively high thermal mass, SiC-coated, graphite susceptor which helps reduce temperature variation across the wafer. The exposing surface of the susceptor is usually coated with an additional thin layer of silicon to reduce possible carbon contamination. Process gases of the system include pure silane (SiH_4) and germane (GeH_4) for deposition of Si and $Si_{1-x}Ge_x$ layers, and, diluted phosphine (PH_3, 100ppm), arsine (AsH_3, 1000ppm), and diborane (B_2H_6, 1000ppm) in silane, for n- and p-type in-situ doping capability. Gas switching is the primary technique used to initiate and terminate a growth process. To avoid transient and ensure repeatability, steady state gas flow conditions are first established at the system bypass before introduced into the chamber.

In addition, the reactor is equipped with an RF plasma source for both in-situ wafer cleaning purpose and plasma-enhanced mode of deposition. Typical deposition temperatures and pressures of the reactor range from 575°C to 800°C and 1 to 10 mTorr, respectively.

Ex-situ Cleaning Procedure

Starting wafers for the device fabrication are 4-in, (100), Sb-doped, 0.005–0.02 Ω-cm, silicon substrates. Initially, 1000 Å of thermal oxide is grown on the substrates to remove residual damages resulted from wafer polishing. Prior to the epitaxial deposition, a standard RCA clean is performed first. The wafer is then treated in a 50:1, H_2O:HF solution for several minutes to remove the 1000 Å oxide layer, and, rinsed in deionized water and spin-dried. The wafer is further cleaned by exposing to UV ozone for 5 minutes to reduce carbon contamination, at the same time, forming a ~10 Å of protective oxide on the wafer surface. This thin oxide serves as protective

layer to prevent re-contamination of the wafer surface during reactor bakeout. After this standard *ex-situ* cleaning procedure, the wafer is immediately loaded into the VLPCVD system and ready for $Si/Si_{1-x}Ge_x/Si$ epitaxial deposition.

In-situ Cleaning and $Si/Si_{1-x}Ge_x/Si$ Film Deposition

The detailed operation and maintenance of the reactor is well-documented in Ref. [76, 77]. A summary of the standard procedure is listed in Table 3.2.

The wafer is usually loaded into the system at the conclusion of previous deposition run. The chamber is then pumped down and continuously purged in Ar gas for at least 2 hours, typically overnight, before the actual epitaxial run. After a routine system check and start-up, the reactor bakeout is carried out at 800°C with a flow of 50 sccm Ar gas. When the temperature is stabilized and a chamber pressure of $\sim 2 \times 10^{7}$ Torr is reached, the protective oxide is removed by in-situ argon plasma and deposition of $Si/Si_{1-x}Ge_x/Si$ begins. In-situ doped $Si/Si_{1-x}Ge_x/Si$ sandwich structure is deposited without breaking vacuum. Typical deposition conditions, summarized in Table 3.3, are as follow. First, few hundreds angstroms of Si buffer layer and ~ 1 μm of collector are deposited at the bakeout temperature of 800°C. The collector doping is typically kept low to around mid-10^{16} cm^{-3} to maintain a good device breakdown characteristics. After the buffer and collector deposition, the substrate temperature is reduced to 625°C or 675°C, with about 30 minutes of growth interruption to allow temperature stabilization. Then, a 500 Å $Si_{1-x}Ge_x$ base layer and 1500 Å Si emitter cap are deposited. Typical layer growth rates in this temperature range are on the order of $\sim$100 Å/min. The deposition and material related study of epitaxial $Si_{1-x}Ge_x$ using the VLPCVD reactor were carried out by previous co-workers. The detailed deposition conditions, deposition kinetics, dopant incorporation and thermal stability issues, pertaining to the device fabrication, were discussed extensively in his thesis and will not be presented here [71].

Step	Description
System Check	check base pressure ($\sim 1\times10^{-8}$ Torr) open gate valve check cold pressure ($\sim 1\times10^{-7}$ Torr)
Bakeout	flow 50 sccm Ar ramp up lamp voltages ($\sim$ 240 V) stabilize temperature reach chamber pressure of $\sim 2\times10^{-7}$ Torr
Sputter Clean	Ar plasma 25 sccm Ar, 5 mA, 10 W, 4 Vac (peak-to-peak) -100 Vdc bias on susceptor
Deposition	(condition varies)
Shutdown	reduce lamp voltages gradually close gate valve back-fill with Ar open gasket seal
Idle State	load wafer for the next run close chamber open roughing valve reset system flow Ar gas (90 sccm + 80 sccm)

Table 3.2: Summary of the standard operating procedure of the VLPCVD reactor.

Layer Parameters			Gas Flow			
Layer	Temp (°C)	Time (min)	SiH_4 (sccm)	GeH_4 (sccm)	PH_3 100 ppm (sccm)	B_2H_6 1000 ppm (sccm)
Buffer	800	5	39.6	0	0.4	0
Collector	800	20	39.6	0	0.4	0
	ramp	30	— 50 sccm Ar —			
Base	625	5	18	0.6	0	2
Emitter	625	20	30	0	10	0
* Typical values only.						

Table 3.3: Typical growth conditions of the VLPCVD for SiGe-base HBT structures.

3.2.2 Thermal Annealing

Due to the meta-stable nature of $Si_{1-x}Ge_x$ layer, the most critical processing parameter concerning device fabrication is the total thermal budget — in particular, the post-deposition thermal annealing step for implant activation. When the metastable device layer is exposed to sufficiently high temperatures for long enough time periods, the strain in the $Si_{1-x}Ge_x$ layer will relax and misfit dislocations will form at the interface between the Si and $Si_{1-x}Ge_x$. Strain relaxation will lower the bandgap difference between Si and $Si_{1-x}Ge_x$ causing a degradation in injection efficiency and a reduction in current gain. Also, misfit dislocations that accompany strain relaxation can act as generation-recombination centers to increase leakage currents and cause current gain to be a function of collector current.

We have studied $Si_{1-x}Ge_x$ samples annealed under various thermal cycles. Thermal relaxation experiment are carried out on $Si_{1-x}Ge_x$ layers with 20% Ge and thicknesses of 0.08, 0.16, 0.40μm. The samples are annealed for 30 min at temperatures ranging from 800°C to 1100°C. Transmission electron microscopy (TEM), Raman scattering spectroscopy and double-crystal X-ray diffractometry (DCD) are used to characterize the films. TEM and DCD results confirm that strain relaxation by dislocation generation is the dominant relaxation mechanism at temperature below 950°C. From Raman spectroscopy, Ge diffusion is found to be significant at temperature

above 950°C, and can be used to explain observed rapid strain relaxation [78]. This result is also consistent with previous thermal stability study using DCD [79]. The diffusivity of Ge can be quantified using secondary ion mass spectrometry (SIMS); and, an activation energy of 4.61 eV and a prefactor of $2.54\times\ 10^2$ cm^2/sec are extracted from samples with Ge fraction of 0.15 – 0.20 [71].

We have also examined effect of annealing conditions on device characteristics. Excessive leakage currents at low V_{BE} bias resulted from insufficient annealing are measured in early devices; they are believed to be caused by residual implant damages and insufficient activation of dopants. Over annealing causing larger recombination current and degradation in current idealities are also observed; we speculate that defects and dislocations are being generated with the additional heat treatment. An optimal condition of 800°C, 20-min furnace annealing is obtained for our device fabrication.

3.3 Device Characterization

Results of device characterization from several process lots are presented in this section. Initially we have experienced difficulties in yielding functional devices. The main problem lies in the fact that $Si_{1-x}Ge_x$ layers in the device structures are metastable in nature and post-deposition thermal treatment partially relaxes the films and causes dislocations to generate. After carefully controlling the allowed thermal budget, we are able to produce functional devices with high current gain, excellent current idealities and good breakdown characteristics.

After successful completion of device fabrication, extensive device characterization are carried out to extract necessary parameters for further process modification as well as theoretical analysis. Statistical data on the current ideality factors and base and collector current variations, are generated to examine the device yield and the device matching. Measurements of breakdown voltages, 1/f noise characteristics, and

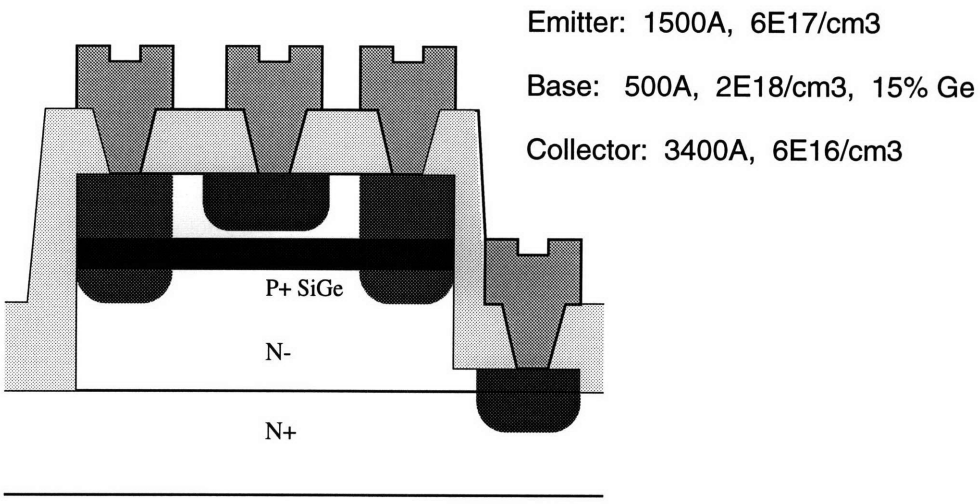


Figure 3-6: Cross-section and typical parameters of a device fabricated using the "MESA" process.

parasitic elements are also performed. Characterization results generally indicate that very good yield can be obtained.

DC Characterization

Most characterization results presented in this section are performed on devices obtained from successful completion of the "MESA" process. Figure 3-6 shows a schematic cross-sectional diagram of the fabricated SiGe-base HBT device.

Table 3.4 lists the layer structures deposited in a commercial APCVD reactor for the study. The three films have identical emitter and collector structures, as well as, a fixed 15% Ge in the base. These wafers differ only in their base boron dopant concentrations, with 2×10^{18} cm^{-3}, 5×10^{18} cm^{-3} and 7×10^{18} cm^{-3}, respectively. The parameters — germanium content, layer thicknesses, and dopant concentrations, are verified by SIMS results.

Plotted in Figure 3-7 are the Gummel plot and the I_C vs. V_{CE} curve of a typical device characteristics obtained. Gummel plot represents the most fundamental key to

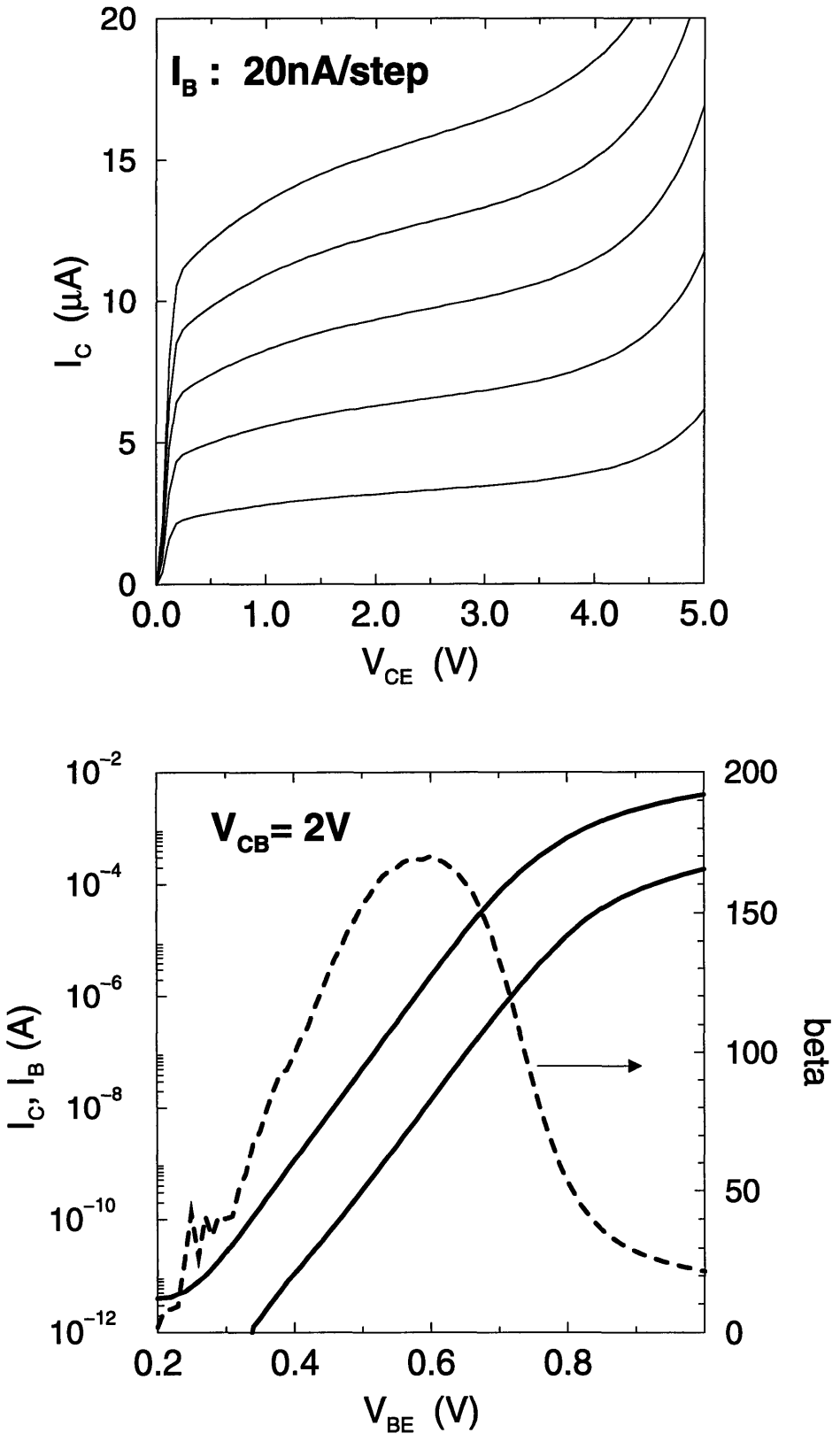


Figure 3-7: Device characteristics: the Gummel plot and the I_C vs. V_{CE} curve of a typical device.

Wafer #	Emitter		Base			Collector	
	N_{de} (cm^{-3})	W_e (Å)	N_{ab} (cm^{-3})	W_b (Å)	Ge (%)	N_{dc} (cm^{-3})	W_c (Å)
A572	6×10^{17}	1500	2×10^{18}	500	15	6×10^{16}	3400
A575	6×10^{17}	1500	5×10^{18}	500	15	6×10^{16}	3400
A579	6×10^{17}	1500	7×10^{18}	500	15	6×10^{16}	3400

Table 3.4: Layer structures deposited in a commercial APCVD reactor to examine the effect of boron doping in the base.

Parameter	Device Wafer		
	A572	A575	A579
N_{ab} (cm^{-3})	2×10^{18}	5×10^{18}	7×10^{18}
A_E (μm^2)	4.5 × 9.0	4.5 × 9.0	4.5 × 9.0
β_{max} (@ V_{CB} = 2V)	170	44.4	29.5
V_A (V) (@ I_B = 100nA)	9.5	14.0	30.2
$\beta \cdot V_A$ (V)	1520	620	890
BV_{CEO} (V)	6.1	7.4	7.6
BV_{CBO} (V)	17.5	17.4	16.9
BV_{EBO} (V)	7.3	7.4	6.8
R_E (Ω)	69	68	86
R_C (Ω)	90	85	85

Table 3.5: Summary of device characterization results of device wafers A572, A575, and A579.

the understanding of a bipolar transistor; it shows the dependence of I_C and I_B on the base-emitter voltages V_{BE}, when an appropriate collector-base voltage V_{BC} is applied such that the collector current becomes independent of V_{BC}. As we can see from the figure, functional devices exhibit excellent ideality factors ($\simeq$60 mV/decade) in both base and collector currents, high current gain ($\sim$170) and reasonable breakdown characteristics ($BV_{CEO} > 6V$).

Summarized in Table 3.5 are the characterization results obtained from the three device wafers. We can see that the current gain β and Early voltage V_A follow the expected trend with the base doping level. The emitter resistances are somewhat higher than expected; this is probably due to the low emitter dopings of the structures and insufficient annealing of the implant damages. We also examine the yield statistics

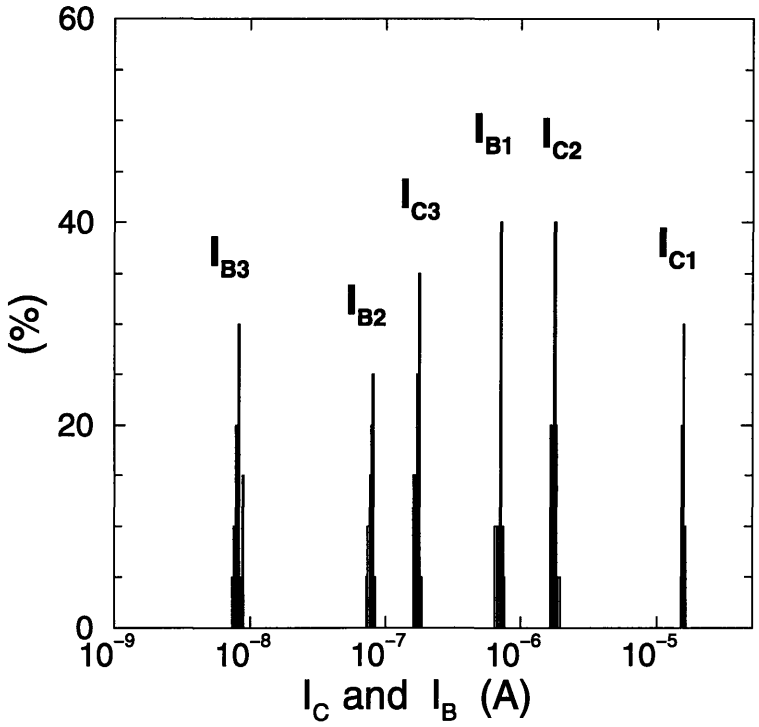


Figure 3-8: Statistics of the collector and base currents at biases of V_{BE}=0.6, 0.66, and 0.72 volts. The considered devices are obtained from wafer A579 with emitter area of 4.5μm×4.5μm.

of the device wafers and found that very high yield is obtained with this process.

Statistical Measurement

Statistical measurements of the collector and base currents over three decades are taken on transistors of emitter area of 4.5μm×4.5μm from device wafer A579. Both collector and base currents show vary little variation of less than 10% as a result of excellent control of the process. From the Figure 3-8, we observe a slight increase of variation in base current at low bias. This is due to nonuniform dopant distributions in the emitter and base contacting areas, resulting from insufficient annealing.

Yield studies, measured in terms of the base and collector current ideality factors of the fabricated devices, are carried out. The yield criteria is set to be ideality factor n less than 1.04. Figure 3-9 summarizes the results on over 100 devices obtained from

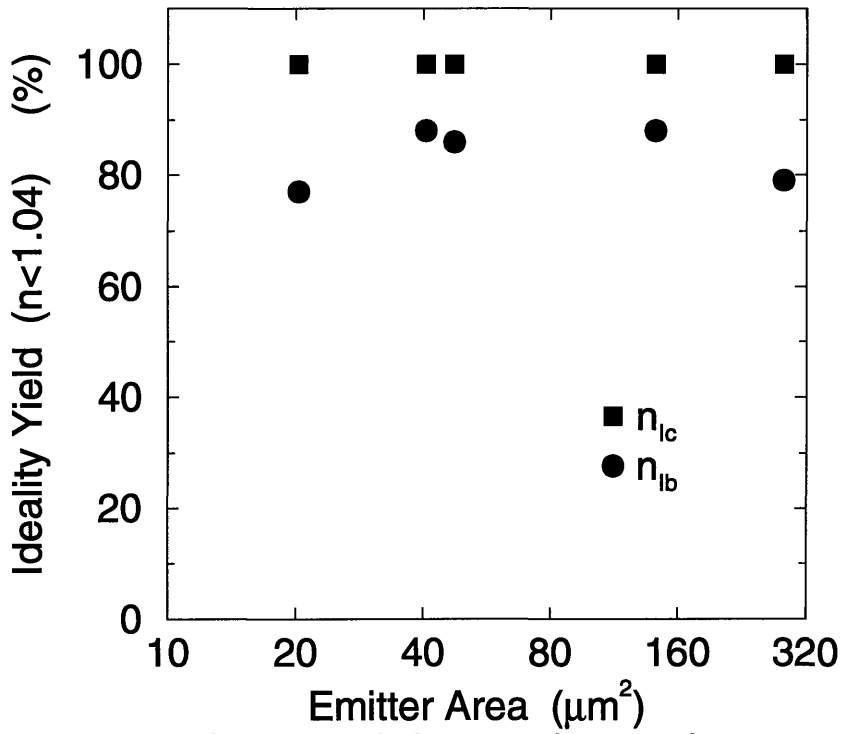


Figure 3-9: Statistics of I_C and I_B idealities as a function of emitter area. Devices are obtained from wafers A572, A575, and A579.

the three wafers (A572, A575, and A579). We have essentially achieved a 100% yield in the collector current ideality and a very high yield of 80% in the base. If we relax the yield criteria to be $n < 1.1$, we can achieve 100% yields in both base and collector current ideality factors. Transistor with larger emitter areas show a slight decrease in yield which is as expected.

Emitter and Collector Resistance

The series resistance of the emitter ($r_{e'}$) of a bipolar transistor can be determined by several methods. Two most commonly used techniques are (1) direct extrapolation from the $1/g'_m$ vs. $1/I_C$ plot of the device, and, (2) the Getreu's method by stimulating the base with current and measuring the voltage between the collector and emitter [80].

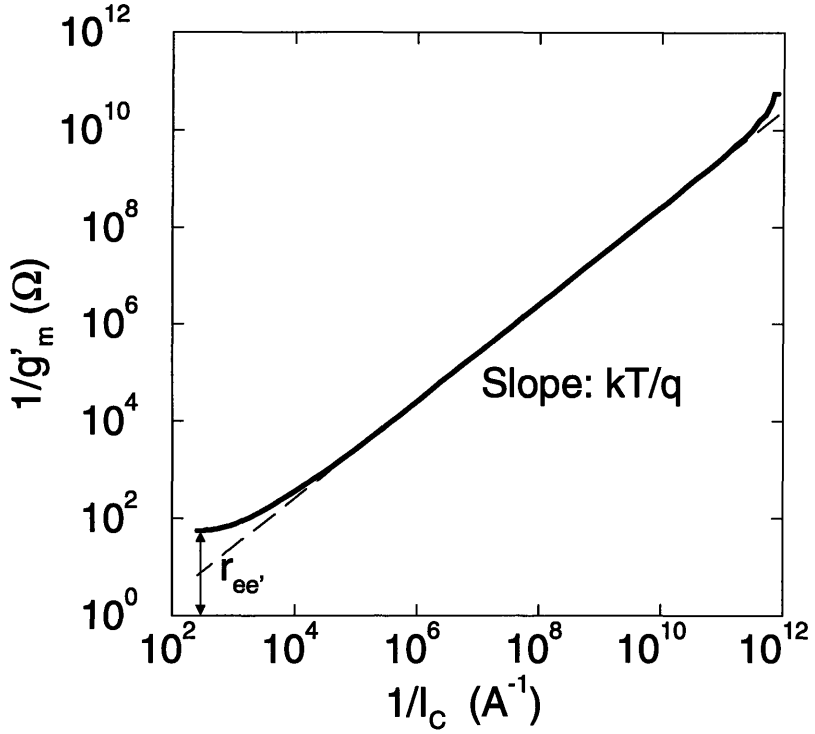


Figure 3-10: Reciprocal of measured transconductance (g'_m) versus reciprocal of collector current (I_C). $r_{e'}$ can be extracted from the plot.

At low frequencies, g'_m of a device can be expressed as follows:

$$\frac{1}{g'_m} = \frac{kT}{qI_c} + r_{e'} + \frac{r_{bb'}}{\beta} \tag{3.1}$$

By direct extrapolation to zero $I_C{}^{-1}$, the emitter series resistance can be determined (neglecting contribution from the $r_{bb'}/\beta$ term). Figure 3-10 plots the $1/g'_m$ vs. $1/I_C$ curve of the device shown in Figure 3-7. The emitter resistance is measured to be ~60 Ω in this case.

Alternatively, emitter resistance can be determined from the Getreu's method. The setup and the measurement result is shown in Figure 3-11. The value of $r_{e'}$, equal to the inverse of the slope of the dashed curve, is determined to be ~69 Ω. This is in good agreement with the extrapolation result just mentioned. The collector series resistance ($r_{c'}$) can be determined in a similar fashion once $r_{e'}$ has been obtained [80].

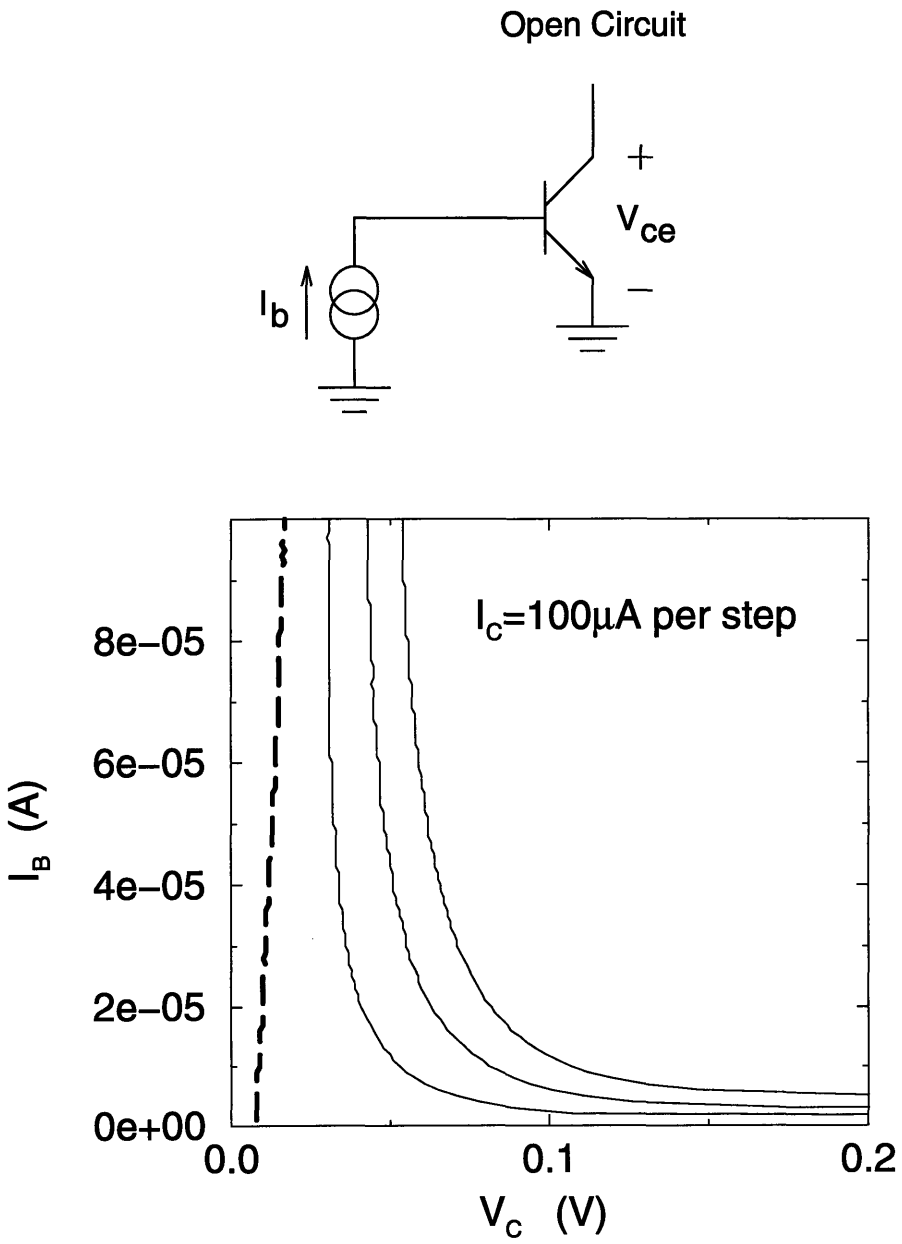


Figure 3-11: The Getreu's setup and plot of I_B versus V_{CE}. The value of $r_{e'}$ can be determined from the slope of the dashed curve (corresponding to I_C=0).

From Figure 3-11, the collector resistance is found to be ~90 Ω.

Base Resistance and Noise Characterization

The noise model for an HBT is the same as for the BJT. The main sources of noise are resistive noise in the base, and shot noise in the emitter and collector currents. The base resistance of the HBT can be made lower because of the higher base doping allowed. It is thus expected that HBTs should have better noise figure compared with BJTs.

The use of noise measurements to determine base resistance is one of the standard practices. It requires the use of very-high-gain amplifiers whose gain is stable in time, as well as extensive shielding to prevent excessive rf interference and 60Hz pick-up.

If the flicker noise is assumed to be negligible, the base resistance $r_{b'}$ can be estimated as [80]:

$$r_{b'} = \frac{\overline{(v_i^2)}}{4k_B T \Delta f} - \frac{1}{2g_m} \tag{3.2}$$

where Δf is the bandwidth of the measurement, $\overline{(v_i^2)}$ is the transistor's equivalent input mean-square noise voltage, and g_m is calculated from the known collector current.

We have performed noise measurement on a device with base dopant concentration of 2×10^{18} cm^{-3}. From our measurement, $\overline{(v_i^2)}/\Delta f = 5 \times 10^{-17}$ V^2/Hz is obtained and $r_{b'}$ is calculated to be ~3 kΩ using equation(3.2). This value is somewhat higher than what we would expect from a layer with ~4 kΩ/□ (base doping: 2×10^{18} cm^{-3}, thickness: 500Å). The high base resistance may be attributed to insufficient annealing of the contacting implants or contact resistance.

Device Parasitics

So far, we have demonstrated the good performances of fabricated devices. However, some anomalous behaviors are also observed: (1) the peaks of current gain seem to

occur at rather low collector current levels in some devices; and, (2) the current gains are found to be increasing with reducing emitter sizes in some cases.

Additional measurements and simulations are carried to better understand these behaviors. Results indicate that the early roll-off of current gain may be attributed to the formation of parasitic barriers at the base-emitter and base-collector junctions due to boron out-diffusion from the base regions during post-deposition processing. The out-diffusion of boron is greatly enhanced by the emitter contacting implants (using arsenic), similar to the emitter push effect commonly observed in homojunction bipolar transistors. The unexpected current gain dependency on emitter sizes and geometry is found to be related to the device parasitics.

3.4 Summary

In this chapter, device fabrication and characterization are discussed. We rely on a home-built, single-wafer, non-load-locked, quartz-halogen-lamp-heated, very-low-pressure chemical vapor deposition (VLPCVD) system to supply $Si_{1-x}Ge_x$ films for various material studies and device processing. The operating procedure, ex-situ and in-situ cleaning steps of the VLPCVD reactor, as well as other key processing steps are described. Detailed descriptions of the three processes, namely, the "MESA", the "LOCOS", and the "POLY", developed for SiGe-base HBT device fabrication are presented. The processes are consistent with the available tool set in the MTL-ICL and compatible with the MTL baseline 1.25μm twin-well CMOS technology. Upon completion of the fabrication, device and process parameters were extracted from both electrical and material characterization, for further process modification as well as theoretical analysis.

Functional devices with high current gain, excellent current ideality factors and good breakdown behaviors are obtained. Current gain exceeds 1000 has been measured in devices with 20% Ge in the base. Matching of device current gains and

turn-on voltages in the form of statistical measurement are investigated. Emitter and collector series resistances are measured using the Getreu's method. 1/f noise measurements are performed to extract the base series resistance. We also report an observation of a rapid current gain rolloff in devices with lightly doped emitters. The effect is probably due to the formation of a parasitic barrier at the base-emitter junction resulting from dopant outdiffusion. We will present a model based on the inverse Early effect to explain the observations and simulation results using MEDICI to confirm the model.

Chapter 4

Vertical Profile Engineering

We have previously described in Chapter 2 the design considerations of SiGe-base HBTs for analog applications. Various performance tradeoffs related to the engineering of vertical profiles are discussed. With successful completion of device fabrication and characterization, we are in position to systematically investigate some of the tradeoff issues. We will demonstrate some of the concepts with both experimental and theoretical approaches. Particularly, we will concentrate on device structures with various germanium and boron doping levels, forward- and retro-graded base germanium profiles, and lightly doped emitters. Modeling results on the displacement of p-n junctions with respect to the heterojunction will also be presented.

4.1 Base Region

Most key tradeoffs in the optimization of heterojunction bipolar transistors come from the base profile design. Important device parameters such as current gain β, Early voltage V_A, base resistance R_B, are all intimately related to the base profiles. We have fabricated devices with different levels of germanium and boron doping as well as forward- and retro-graded germanium profiles in the base to examine the effects of germanium, boron doping and germanium gradient.

Wafer #	Emitter		Base			Collector	
	N_{de} (cm^{-3})	W_e (Å)	N_{ab} (cm^{-3})	W_b (Å)	Ge (%)	N_{dc} (cm^{-3})	W_c (Å)
BJT	10^{18}	2000	10^{19}	1000	0	3×10^{16}	10000
HBT1	10^{18}	2000	10^{19}	1000	10	3×10^{16}	10000
HBT2	10^{18}	2000	10^{19}	800	10	3×10^{16}	10000
HBT3	10^{18}	2000	10^{19}	800	5	undoped	5000
HBT4	10^{18}	2000	10^{19}	800	5	10^{17}	5000

Table 4.1: Layer structures deposited in the VLPCVD reactor to examine the effect of Ge in the base. The parameters are estimated from previous kinetic data.

4.1.1 Effect of Germanium

We first examine the effect of inclusion of germanium in the base. Table 4.1 lists a set of wafers deposited in the VLPCVD reactor for the investigation. Layer structures of all films are essentially identical; the only real difference among the wafers is the amount of germanium, ranging from 0 to ~10%, present in the base regions. The germanium content, film thicknesses and doping levels of each wafer are estimated from previous kinetic data [71]. Although the actual values may differ somewhat, run-to-run variations of these parameters are proven to be quite small and qualitatively consistent results can still be obtained.

The devices are fabricated using the "LOCOS" process described in Section 3.1.2. Typical devices demonstrate reasonably good DC characteristics. The collector currents in all devices are ideal for over seven decades of current, although some nonlinearities are also observed in the base currents. The somewhat nonlinear base currents with excessive leakage at low bias (not shown) are due to poor device passivation and dislocation resulting from epi deposition on patterned substrates. Nonetheless, the non-ideal base currents do not affect the results here.

The effect of incorporating Ge into the base can be readily seen from the observed collector current enhancement and current gain improvement, shown in Figures 4-1. The ratio between the collector currents of the HBTs and the BJT depend expo-

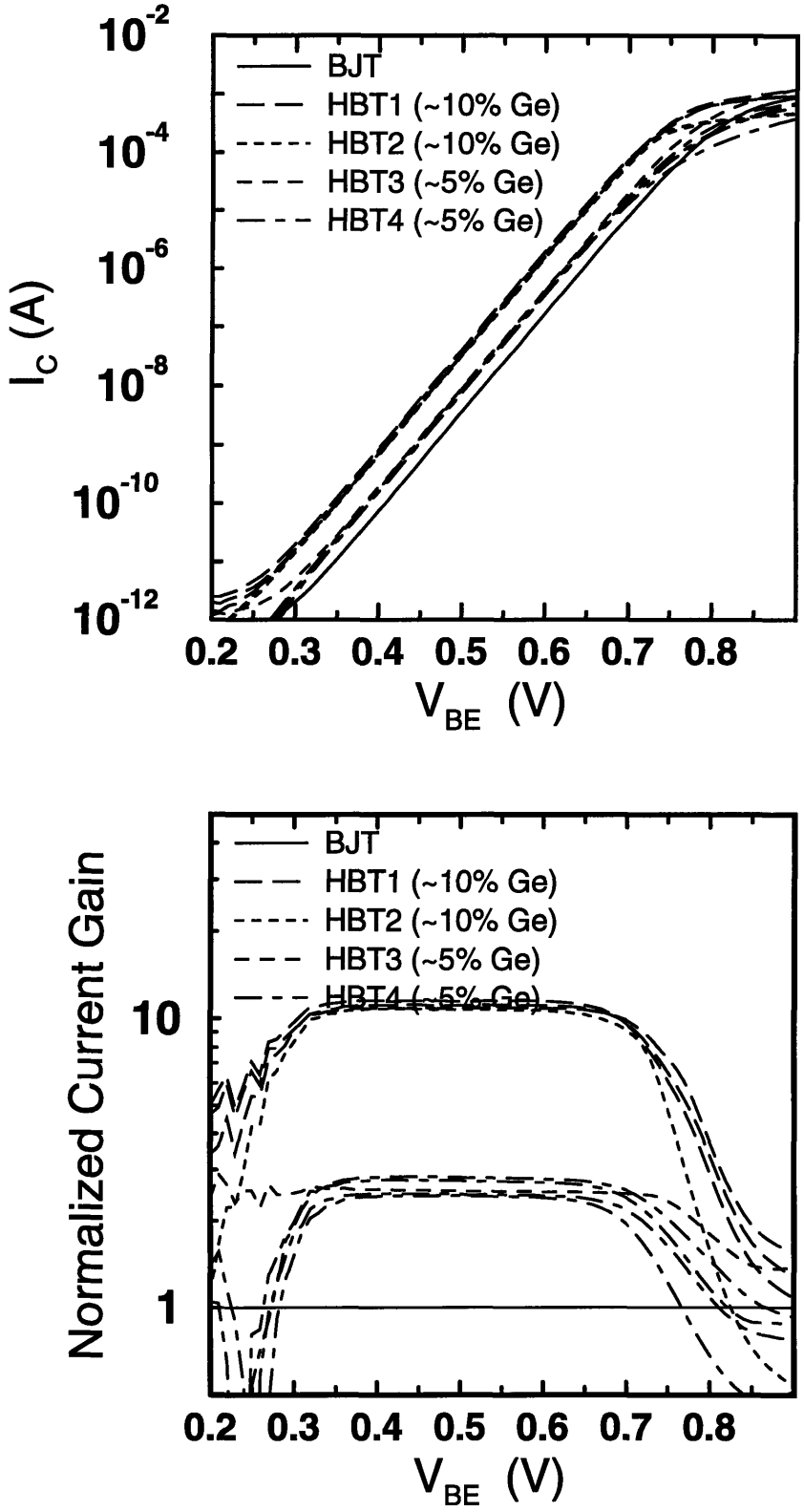


Figure 4-1: Collector current enhancement and normalized current gain of SiGe-base HBTs (with 5% or 10% Ge in the base). The solid line shows the characteristics of a fabricated homojunction device with similar structure.

nentially on the difference of the electron barriers ΔE_v. Neglecting the distinction between the effective density of states of Si and $Si_{1-x}Ge_x$, the ratio can be expressed as [81],

$$\frac{I_{C(\mathrm{HBT})}}{I_{C(\mathrm{BJT})}} \approx \frac{G_{B(\mathrm{BJT})}\nu_{B(\mathrm{HBT})}}{D_{B(\mathrm{BJT})}N_{B(\mathrm{HBT})}} \cdot \exp\left(\frac{\Delta E_v}{k_B T}\right) \tag{4.1}$$

where G_B is the base Gummel number and ν_B is the minority carrier velocity.

Comparison of the fabricated HBTs and BJT shows collector enhancement factors of 3 to 25 are obtained in devices with 5 to 12% Ge; this is consistent with published results in the literature [81].

Another feature to note from Figure 4-1 is that: the turn-on voltages $V_{BE(on)}$ of SiGe-base HBTs are smaller than that of a Si homojunction transistor, i.e. it requires less forward V_{BE} bias to achieve the same current level in HBTs, as result of smaller bandgaps of $Si_{1-x}Ge_x$ materials. The base-emitter turn-on voltage $V_{BE(on)}$ can be expressed as,

$$V_{\mathrm{BE(on)}} = \frac{E_g}{q} + \frac{k_B T}{q} ln\left(\frac{N_A W_B}{D_n N_C N_V} J_C\right) \tag{4.2}$$

As we can easily see, because of the contribution of the first term, the turn-on voltages $V_{BE(on)}$ of SiGe-base HBTs decrease with increasing Ge content in the base. The lower turn-on voltage can be beneficial, especially in low-power circuit application, because high switching speed and high current levels can be achieved at lower supply voltages.

4.1.2 Graded Base

We have successfully fabricated some devices with graded-germanium-base structures, both forward-graded and retro-graded ones. In this section, we will present some interesting device features pertaining to the graded-base devices.

The devices are fabricated using the "MESA" process discusses in Section 3.1.1. Table 4.2 summarizes the set of wafers used in the device fabrication for the investigation. The films are deposited in a commercial APCVD reactor and the parameters, e.g. germanium contents, layer thicknesses, and dopant concentrations, are verified

Wafer #	Emitter		Base			Collector	
	N_{de} (cm^{-3})	W_e (Å)	N_{ab} (cm^{-3})	W_b (Å)	Ge col → em	N_{dc} (cm^{-3})	W_c (Å)
A584	3×10^{17}	1500	5×10^{18}	500	20 → 12%	6×10^{16}	3400
A585	3×10^{17}	1500	5×10^{18}	500	12 → 20%	6×10^{16}	3400
A586	7×10^{17}	1500	2×10^{18}	500	20 → 12%	6×10^{16}	3400
A587	7×10^{17}	1500	2×10^{18}	500	12 → 20%	6×10^{16}	3400
A588	1×10^{18}	1500	1×10^{18}	500	20 → 12%	6×10^{16}	3400
A589	1×10^{18}	1500	1×10^{18}	500	12 → 20%	6×10^{16}	3400

Table 4.2: Summary of the parameters of the layer structures in this experiment with both graded and retrograde Ge profiles.

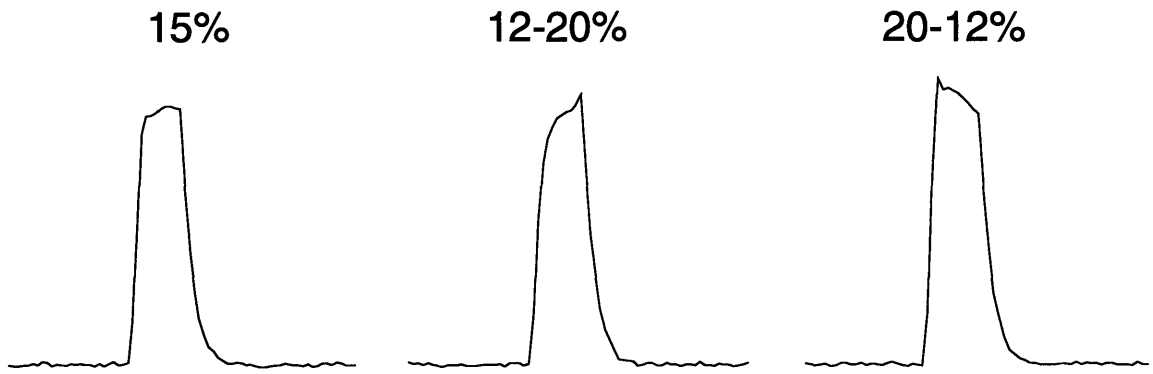


Figure 4-2: Ge profiles obtained by SIMS of a box (15% Ge), forward-graded (12–20% Ge), and retro-graded (20–12% Ge) devices.

by SIMS results. Shown in Figure 4-2 are the forward- and retro-graded germanium profiles obtained by SIMS; the box-like Ge profile is also included as a comparison.

Gummel plots and β vs. I_C curves, and I_C vs. V_{CE} plots of two devices from wafers A584 (forward-graded) and A585 (retro-graded) are shown in Figure 4-3 and Figure 4-4, respectively. Both devices exhibit excellent collector and base current ideality factors (~60 mV/decade), high current gains (>100) and good breakdown voltages (BV_{CEO}> 5V).

Comparing the two devices, i.e. making comparison between forward- and retro-graded cases, we have observed the following: (1) the current gain are comparable in the two cases, (2) the Early voltage is higher in the forward-graded case.

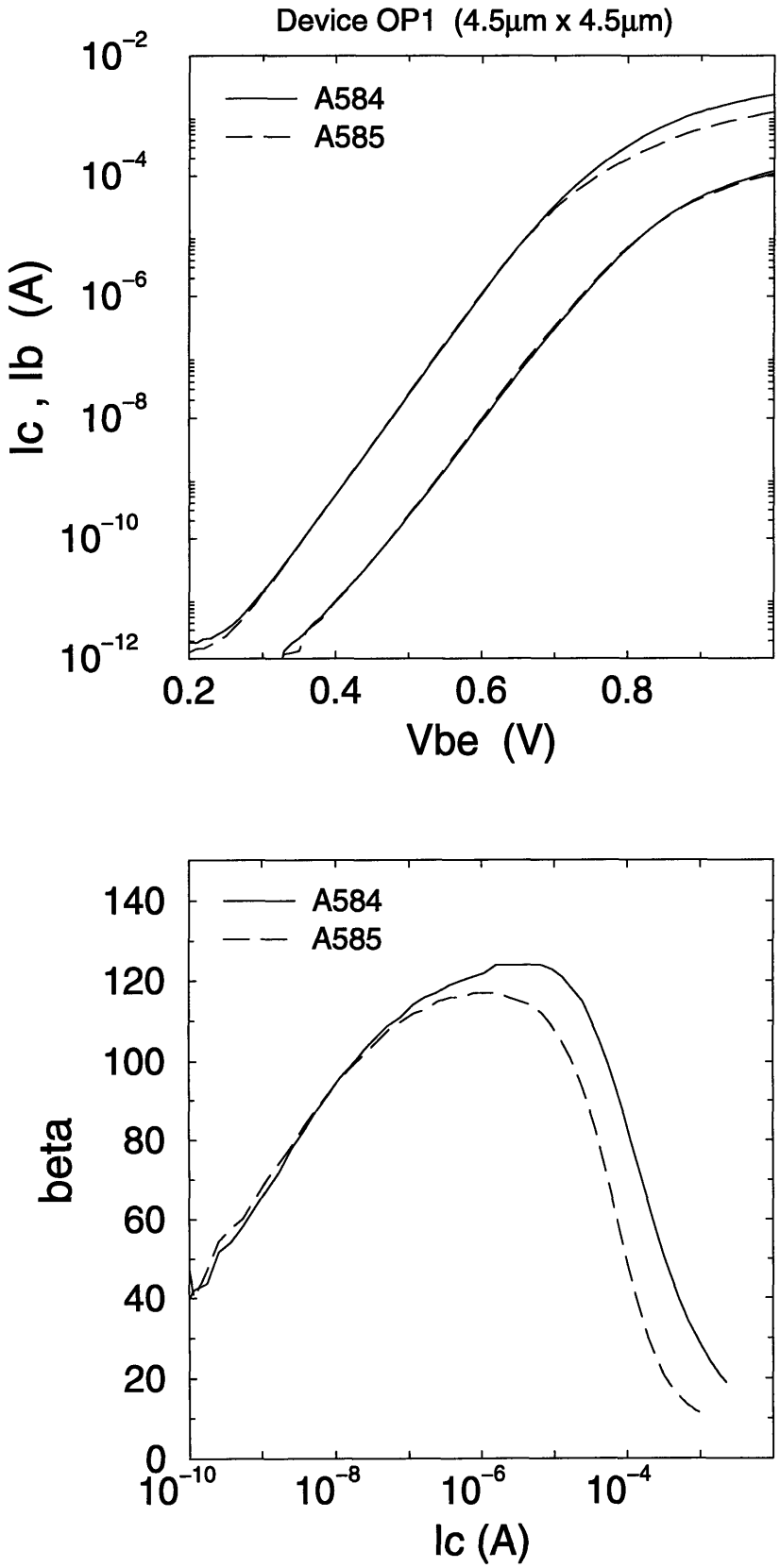


Figure 4-3: Gummel plot and current gain vs. I_C of the devices from wafers A584 and A585.

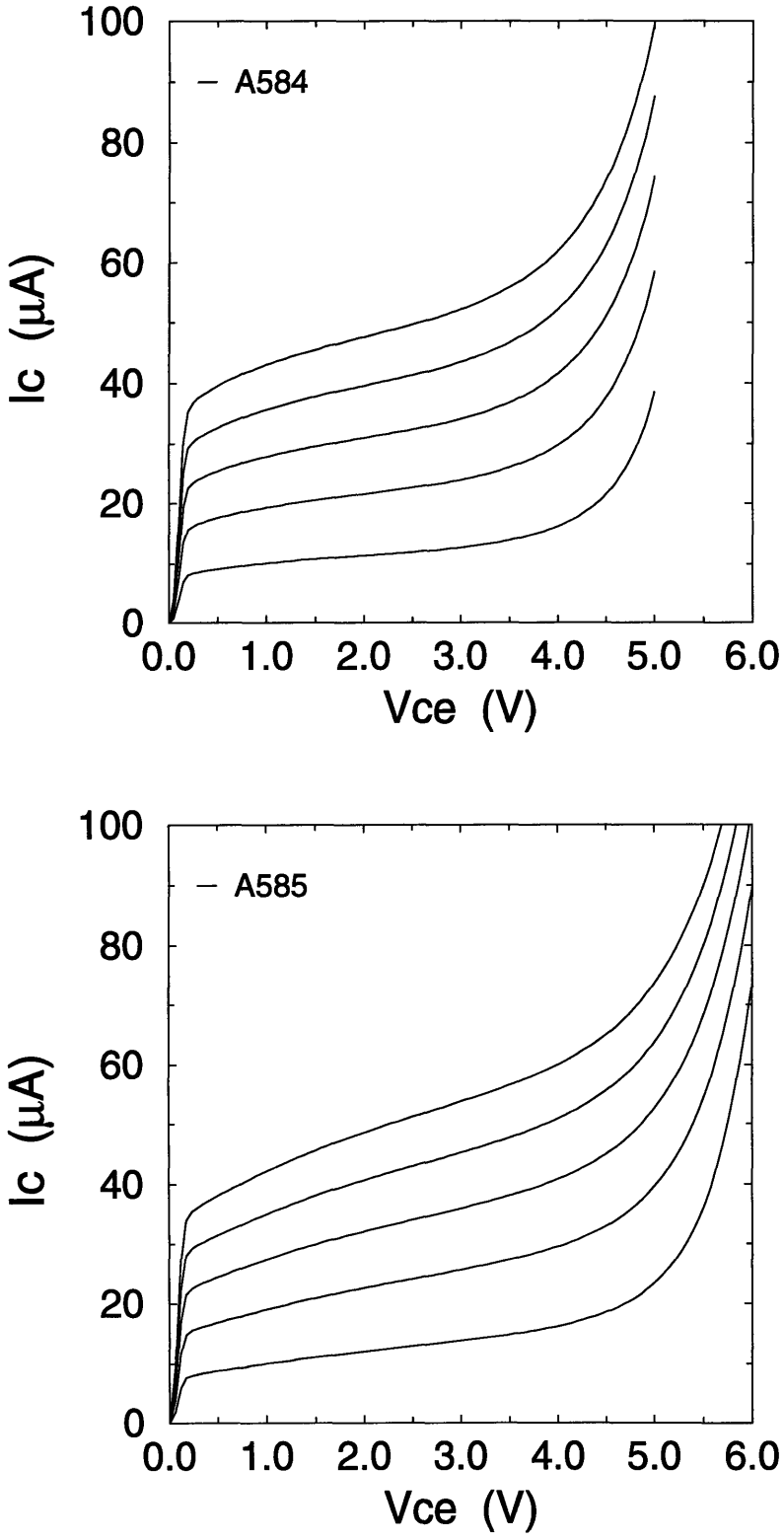


Figure 4-4: I_C vs. V_{CE} plots obtained from the two devices in wafers A584 and A585.

Observation (1) and (2) can be explained by the following equations:

$$\begin{aligned} \beta &= \frac{q}{J_{B,0}}\left[\int_0^{W_B}\frac{N_A(x)}{n_i^2(x)D_n(x)}dx\right]^{-1} \\ V_A &= \frac{q}{C_{BC}}n_i^2(W_B)D_n(W_B)\left[\int_0^{W_B}\frac{N_A(x)}{n_i^2(x)D_n(x)}dx\right] \\ \beta\cdot V_A &= \frac{q^2}{J_{B,0}C_{BC}}n_i^2(W_B)D_n(W_B) \end{aligned} \tag{4.3}$$

From the current gain expression, β is inversely proportional to the effective base Gummel number (the integral term). Since the integral is taken over the entire neutral base, the effect of base grading disappears; thus, as expected, the current gains are approximately equal in the two cases. From the second expression, we see that Early voltage has an explicit dependence on $n_i^2(W_B)$. In the case of forward-graded Ge, a larger Ge fraction exists near the base-collector edge, giving rise to a larger Early voltage.

4.2 Device with Lightly Doped Emitters

Advantages of using a lightly-doped emitter structure was discussed in Section 2.3.2. Lower emitter doping is typically used in heterojunction bipolar transistors to reduced the base-emitter junction capacitance C_{BE} and to improve the junction reliability. However, the price paid for reducing emitter doping level is an increase of emitter resistance. Although the emitter resistance R_E does not appear to be important with current technologies, it may soon become a limiting factor because it increases as lateral dimension decreases. In addition, in device with lightly-doped emitter structure, boron outdiffusion from the SiGe-base region is likely to shift the location of the p-n junction into the Si-emitter region, causing a misalignment with respect to the heterojunction and additional degradations.

Couple observations are noted from the Gummel plots and the I_C vs. V_{CE} curves

in some fabricated devices (see Figure 3-7). First, the device seems to have a rather poor Early voltage of around 10V; and secondly, the current gain seems to peak at a lower current density than expected and rolls off quite rapidly. Both observations can be attributed to the boron out-diffusion from the base into the adjacent collector or emitter regions, forming parasitic barriers near the electrical junctions. The outdiffusion of boron is found to be greatly enhanced by the emitter contacting implants (using arsenic), similar to the emitter push effect commonly observed in homojunction bipolar transistors. The enhanced outdiffusion of the as-grown box-like boron profile has been confirmed by the fact that boron profile remained box-like on those sites on the wafer that did not receive an emitter implant [82].

SIMS data obtained from an actual device wafer is shown in Figure 4-5. The amount of boron spread into the collector region is seen to be quite large, on the order of 1000Å; this explains why the Early voltage is lower than expected. From the SIMS plot, we also observe a slight boron outdiffusion into the emitter region, shifting the p-n junction away from the heterojunction. The effect of this junction displacement is the formation of a parasitic conduction band barrier near the heterointerface which causes degradation in the device current gain.

Plotted in Figure 4-6 is the current gain β versus collector current density J_C of the device shown earlier. From this plot we can see clearly that the current gain peaks at a current density roughly equal to $1\mu A/\mu m^2$ and rolls off quite rapidly. The reason for the early rolloff of current gain is explained by the boron outdiffusion from the base into the emitter region.

Figure 4-7 shows a simulated energy band diagram of an npn SiGe-base HBT. The solid line represents the case when the p-n junction and the heterojunction are perfectly aligned. And the dotted line shows the case when the p-n junction displaced toward the emitter (due to boron outdiffusion, for instance). As we can see, the effect of this displacement is the forming of a parasitic barrier in the conduction band because inside the p-doped region the valence band is "pinned" to the Fermi level.

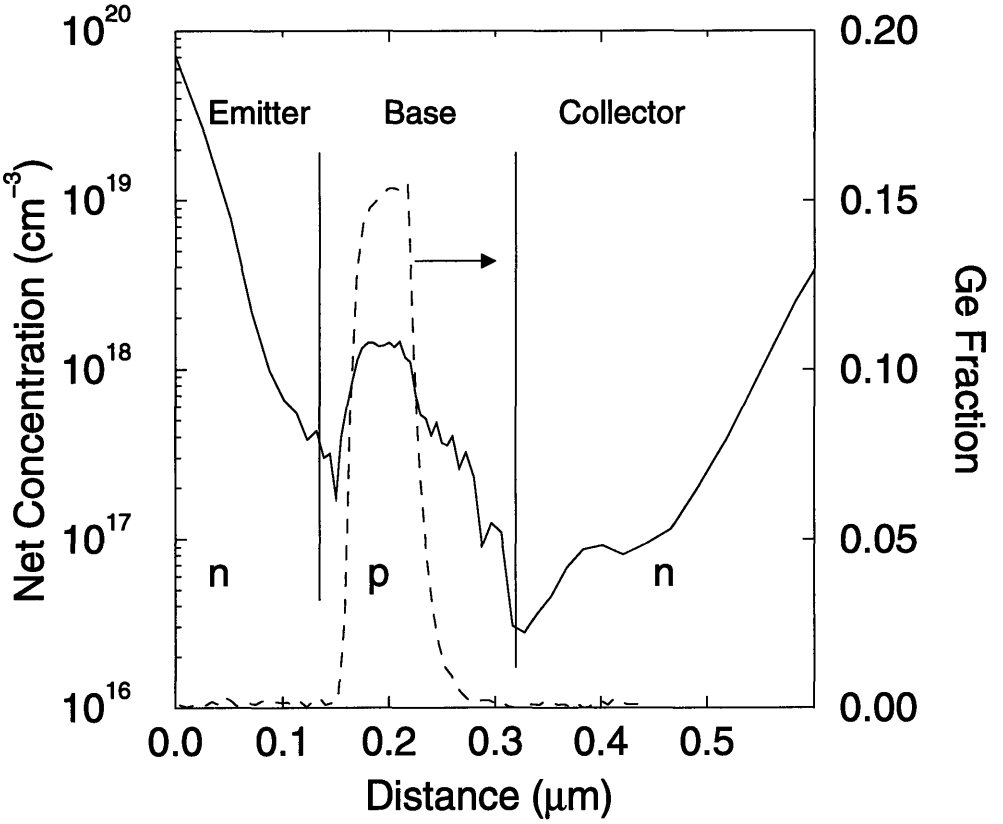


Figure 4-5: SIMS Profile from the device wafer

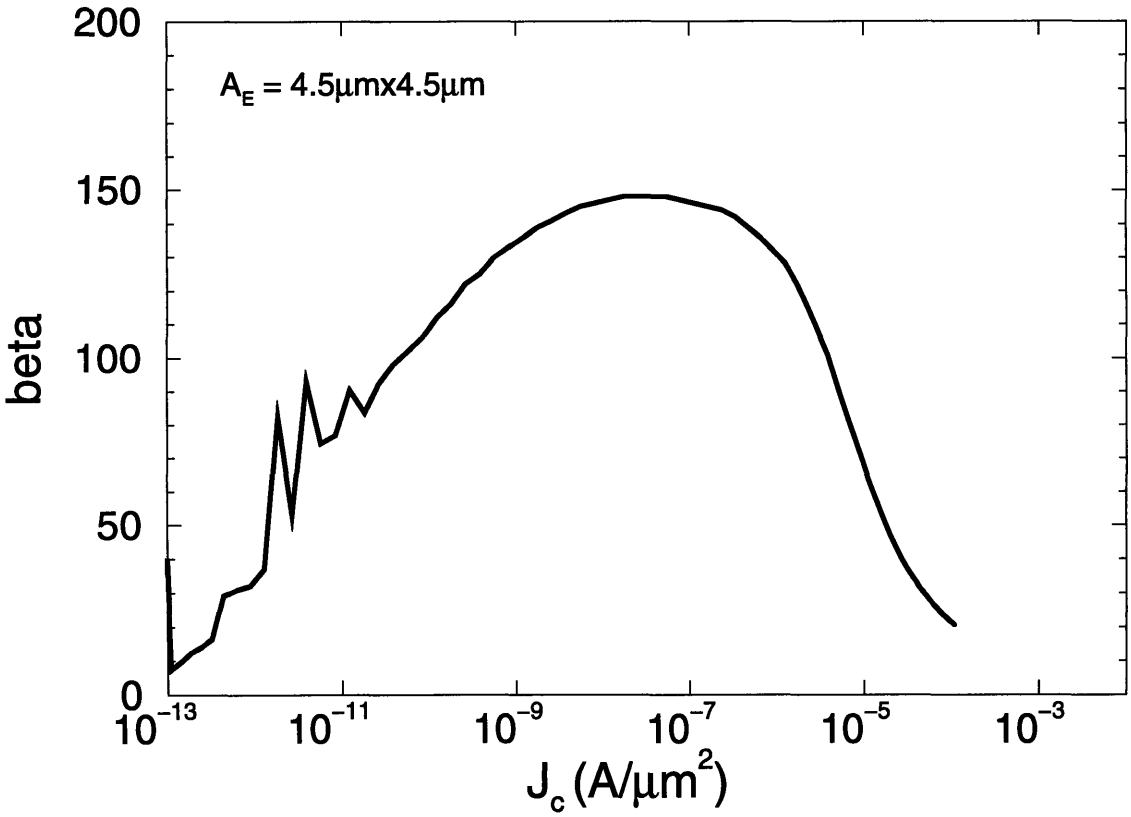


Figure 4-6: Current gain plotted against the collector current density, showing the early rolloff of current gain.

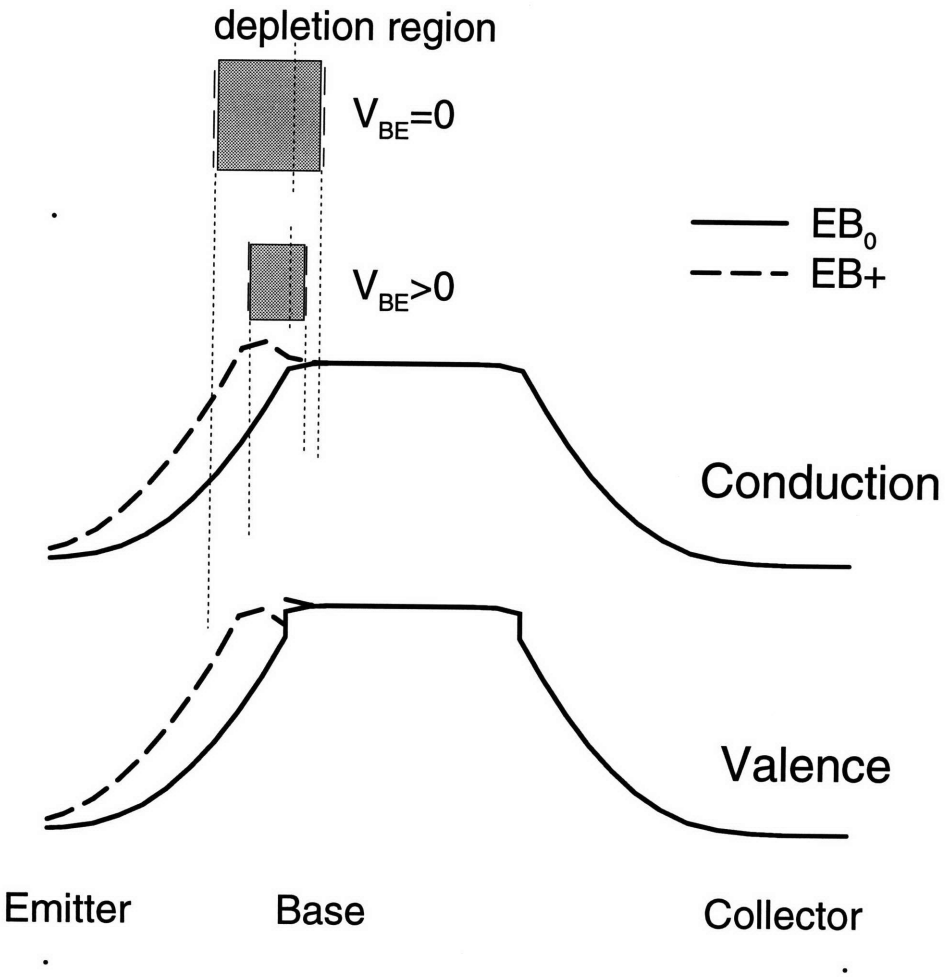


Figure 4-7: Energy band diagram.

The explanation for the rolloff of current at high current density is as follows. Initially, at relatively low bias, this barrier is completely depleted, i.e. contained inside the space-charge region; and, thus, the carriers do not experience the presence of the barrier. As the junction bias increases, due to inverse Early effect, the depletion width decreases and the barrier starts to appear; the barrier then decreases the collector current level and degrades the current gain. Thus, the inverse Early effect leads to a decrease of the current gain with increasing collector current. Although the current gain rolloff, to some extent, is also present in homojunction transistors, the effect is amplified by the exponential dependence of the collector on the barrier height at the

edge of space-charge region of the heterojunction devices. Simulation results will be presented in the next section to support this model.

4.3 Displacement of P-N Junctions

Control of dopant redistribution is an important engineering tasks. Often unintended, some degree of dopant outdiffusion into adjacent layers occurs during high-temperature growth and processing in device fabrication. Excessive dopant redistribution will lead to detrimental effects on the device performance. Therefore, allowable thermal budget must be carefully controlled in order to maintain the integrity of dopant profiles and achieve desired performance.

Dopant outdiffusion in heterojunction devices is of particular importance because the device characteristics, such as collector current density, current gain and Early voltage, are extremely sensitive to the location of the p-n junction with respect to the heterojunction. To obtain an accurate description of the device, the junction displacement issue must be taken into account. Note that junction displacement in heterostructure devices can also arise intentionally by incorporating an intrinsic spacers, for example.

Traditional analysis of HBTs has always assumed a perfect alignment between the p-n junction and the heterojunction. However, this is usually not the case. Because this is a difficult problem to solve analytically, researchers usually rely on simulation programs to provide some qualitative understandings. An excellent study of the p-n junction displacements in AlGaAs/GaAs HBTs, using 2-D simulation, has been reported recently [83]; we will follow the same systematic approach to examine the $Si/Si_{1-x}Ge_x$ structure.

Modeling results using the MEDICI simulation program are presented in this section. We will concentrate on the effects of displacement occurring at the base-emitter junction. Figure 4-8 shows the structure used for the simulations. For simplicity, a

1-dimensional structure, box-like dopant profile and constant germanium fraction in the base, are assumed. Simulation model parameters take into account the Shockley-Read-Hall and Auger recombination, bandgap narrowing, and concentration dependent carrier mobility and lifetime.

Figure 4-9 summarizes the simulation results on the effect of base-emitter junction displacement. We can see that the current gain degrades as the displacement increases, also that the degradation is more significant at higher bias. The simulation result has demonstrated, at least qualitatively, the essential feature of early current gain rolloff discussed earlier. To confirm the fact, we can perform measurements of device characteristics at various temperatures, since the barrier effects are usually quite sensitive to the operating temperatures. Note the barrier effect are more pronounced at low temperatures.

We further investigated the effect of the displacement of base-emitter junction by simulations. For comparison, displacements both into and out of the base region by 100Å are considered. Figure 4-10 shows the simulated energy band diagrams. The simulated Gummel plots and the corresponding β vs. J_C curves of the three cases are shown in Figure 4-11. There are several interesting features to be noted. First, the collector current degrades significantly in the case of junction shifting into the emitter (EB+), as result of parasitic barrier effect. Secondly, base currents differ in each case at high bias; this is probably due to the difference in the base width and base resistance in the three cases. Finally, we observe a significant rise in base current at low bias in the case when the junction shifts toward the base (EB−). This is due to existence of a conduction band minimum which causes excess charge storage and increasing recombination.

Finally, a matrix of different Ge contents and base-emitter displacements are simulated. The results are summarized in Figure 4-12. The figure shows the normalized peak current gain versus amount of base-emitter junction displacements for several germanium content. We can see that the degradation becomes quite severe when the

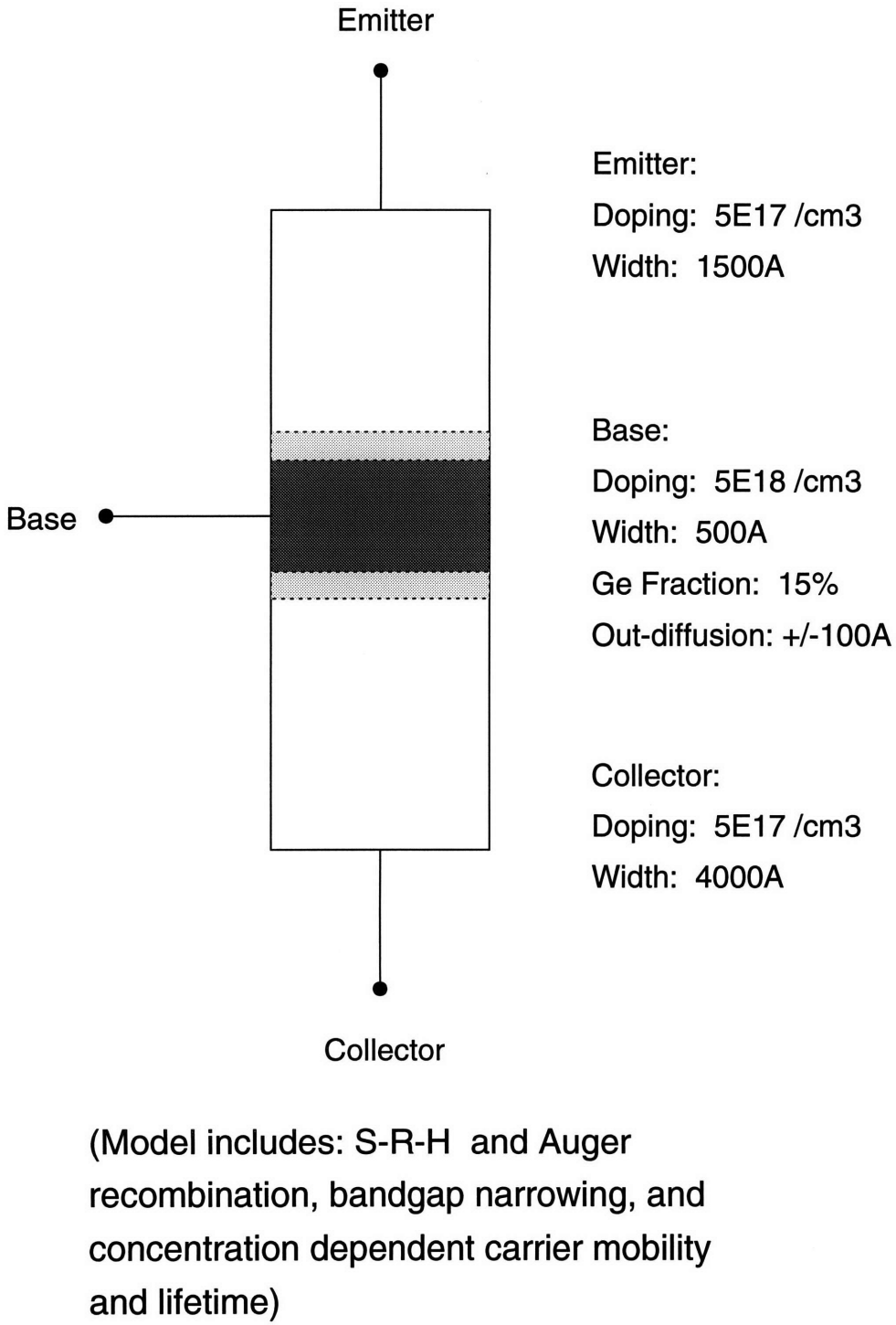


Figure 4-8: MEDICI simulation structure used to study the effect of B-E junction displacement.

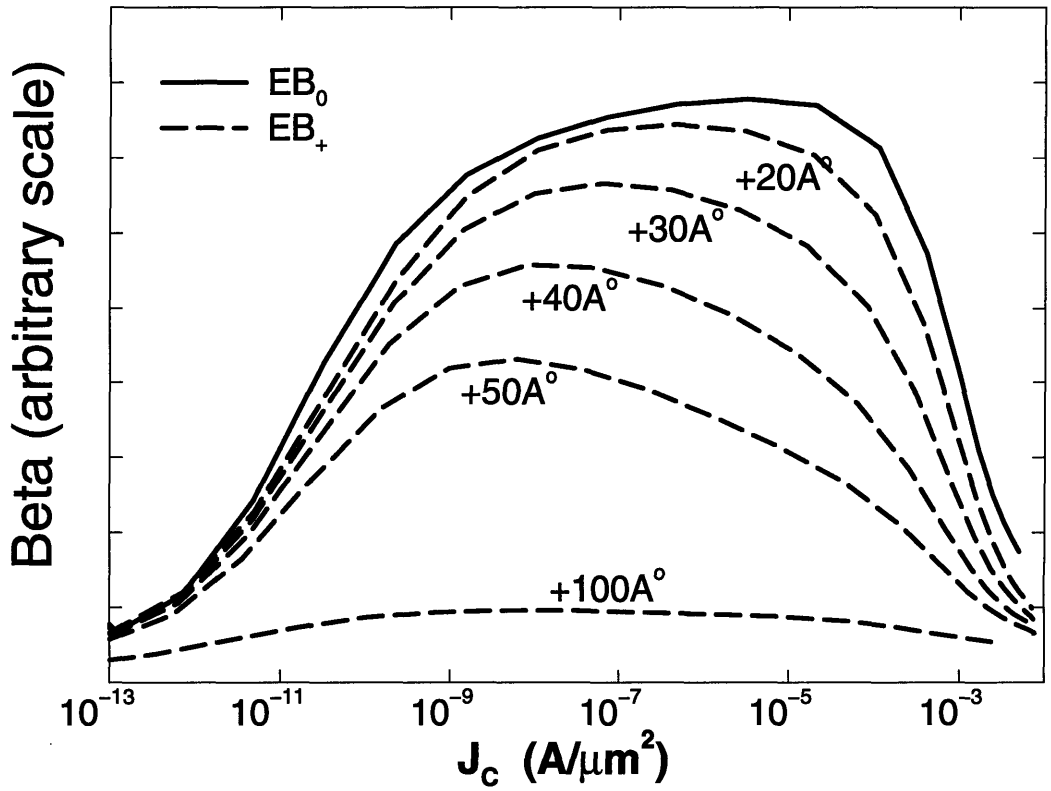


Figure 4-9: Summary of the simulation results on the effect of B-E junction displacement.

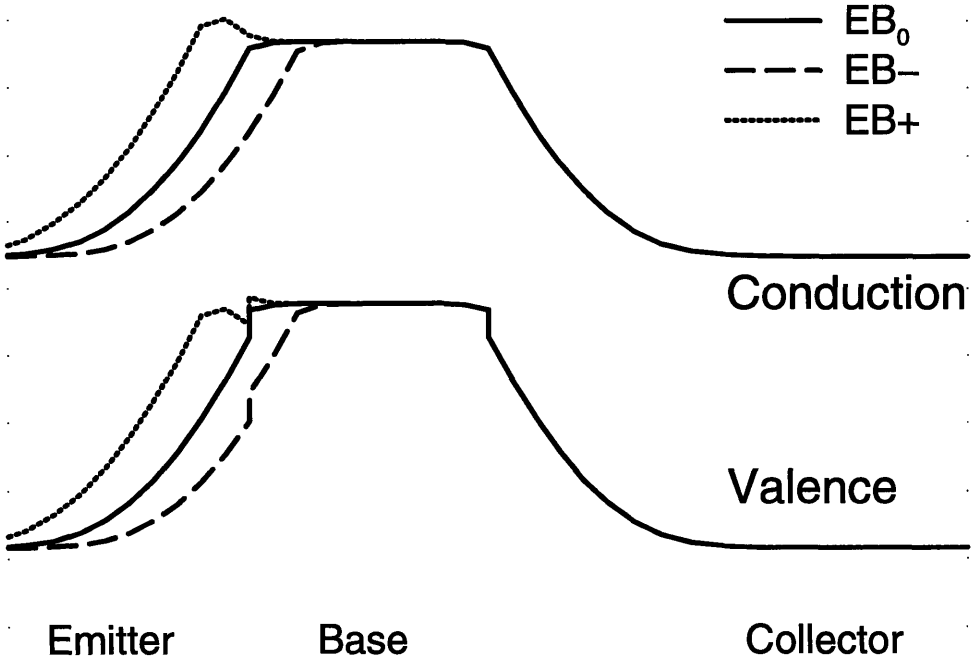


Figure 4-10: Simulated energy band diagram for the three cases of base-emitter junction displacements.

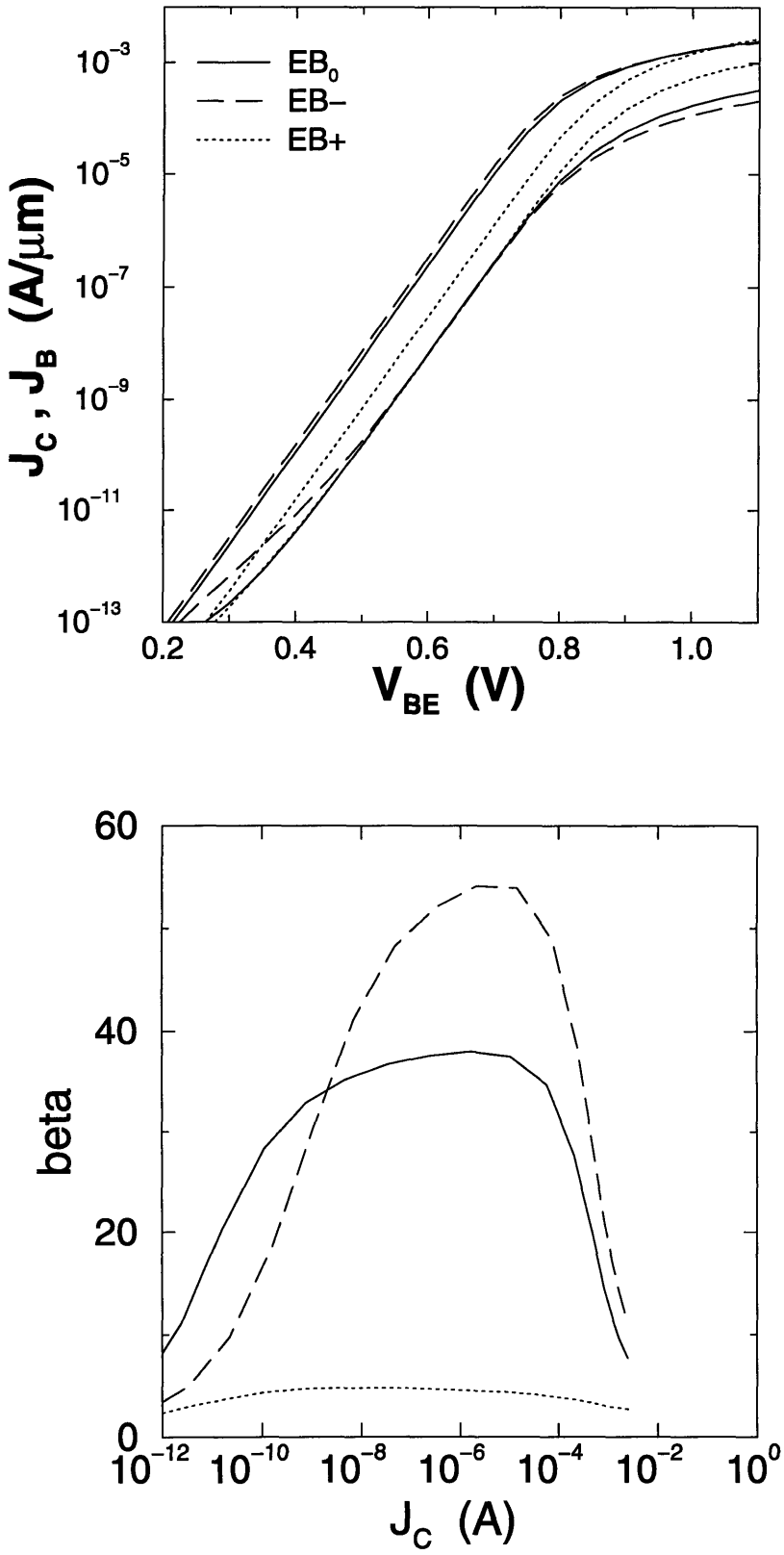


Figure 4-11: Simulated Gummel plot and β vs. J_C curves for the cases of base-emitter junction displacements.

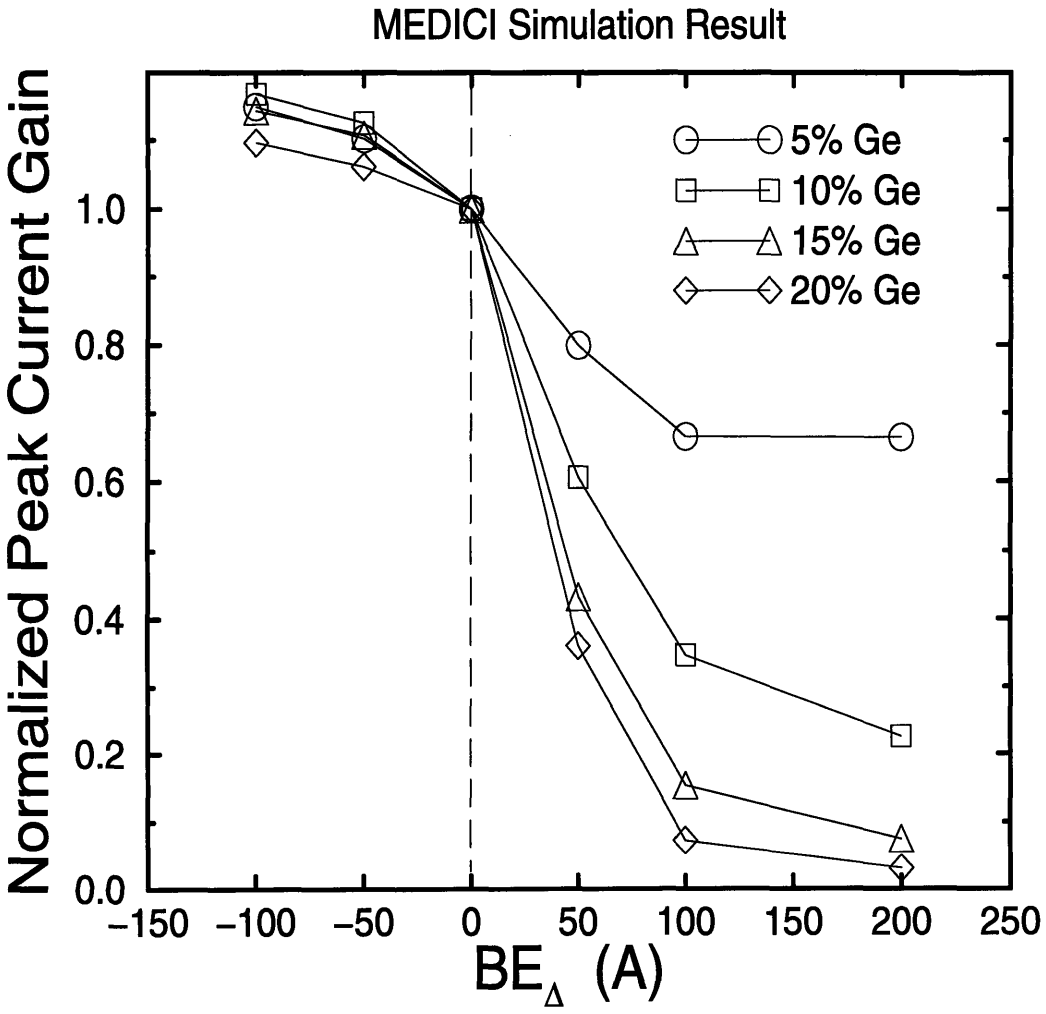


Figure 4-12: Summary of the simulation results on the effect of B-E junction displacement.

amount of displacement is greater than 50Å. Also, as expected, the degradation is more pronounced in the case of higher germanium in the base; this is because of a greater barrier resulting with the displacements.

4.4 Summary

In this chapter, we have examined several options in the vertical profile design of SiGe-base HBTs. Devices with various Ge contents, different base doping levels, and graded and retro-graded Ge profiles, as well as relatively lightly doped emitters (below 1×10^{18} cm^{-3}), are fabricated for the investigation. Collector current improvement and current gain enhancement, and tradeoff between β and V_A, are presented. We have also observed an early rolloff of current gain in some fabricated devices. The early rolloff of current gain is primarily due to formation of a parasitic barrier at the base-emitter junction as result of boron outdiffusion from the base into the emitter during post-deposition annealing. The outdiffusion of boron is found to be greatly enhanced by the emitter contacting implants (using arsenic), similar to the emitter push effect commonly observed in homojunction bipolar transistors.

Lower emitter doping is typically used in heterojunction bipolar transistors to reduced the base-emitter junction capacitance C_{BE} and to improve the junction reliability. To achieve high RF performance , HBT devices in general are made with thin base thicknesses on the order of 50nm and require high base dopings in the range of 1×10^{19} cm^{-3}. Therefore, outdiffusion of boron is likely to occur in these cases, causing the p-n junction to move into the higher bandgap Si region. Since the current gains of HBTs are particularly sensitive to the exact location of the p-n junction, the dopant outdiffusion will have significant effects on circuit applications and must be closely controled. Also, the base-emitter turn-on voltage depends on the bandgap of the material at the p-n junction, see equation (4.2), we can expect the turn-on voltage to increase if boron outdiffusion occurs.

A model based on the inverse Early effect is proposed to explain the observation of early rolloff of current gain. The effect is particularly interesting in devices with lightly doped emitter structures because the B-E junction shifts more toward the emitter side and the base width modulation effect is also more significant in the emitter side. Modeling results indicated that the electrical characteristics of devices could be significantly altered if the misalignments between the p-n and hetero- junctions were greater than 50Å. The early rolloff of current is also more pronounced in devices with higher Ge contents because of taller barrier heights can result from the junction displacement.

Chapter 5

Reliability Study of SiGe-base HBTs

Technology of SiGe-base HBTs has advanced rapidly in the past few years with numerous reports on the device and circuit performance. However, information on the reliability of the device is still very limited [84,85]. The assessment of device reliability is an important task because it ultimately affects the overall yield and long-term operating stability of the fabricated circuits. In this chapter, I will present some results of preliminary reliability study of SiGe-base HBTs, focusing on issues related to the degradation behavior of the device under both high-forward-current and reverse-bias stresses.

SiGe-base HBTs are facing with the same reliability constraints as many modern bipolar transistors. Namely, (1) typical bipolar devices are operating at an increasingly high current density level, commonly exceeding 1 mA/μm^2. Under such a high current density condition, the base-emitter junction is forward biased very near high-level injection condition and significant degradations of device characteristics can occur with time [86–88]. (2) Emitter-base junctions are frequently subjected to reverse bias during switching operation, especially in BiCMOS circuitry. It has been well established that, under reverse bias, the emitter-base junction degrades due to

hot carrier damages created at or near the boundary of the depletion layer with side-wall oxide. The resulted increase of interface state density causes the forward base recombination current to rise and degrades the device current gain [89–93]. And, (3) as devices are being scaled down to finer dimensions, a higher base doping is needed to prevent early punchthrough, at the same time, an increase of emitter doping is required to maintain a good injection efficiency. As a result, large emitter-base junction fields exist, increasing leakage current [89, 90].

The reliability concern of SiGe-base HBTs is further compounded by the presence of germanium in the device structure. On one hand, because of relatively small critical thickness of $Si_{1-x}Ge_x$/Si heterostructure, most reported devices contains $Si_{1-x}Ge_x$ layers that are above the equilibrium thickness, i.e. meta-stably strained. Due to the meta-stable nature of the $Si_{1-x}Ge_x$ film, there is concern that dislocations may be generated and propagating during normal operation, causing device failure. On the other hand, as alluded in Section 1.5, inclusion of Ge in the base may potentially improve the base-emitter junction reliability — the high injection efficiency of HBTs allows the emitter dopant concentration to be reduced, lowering the emitter-base junction field and, consequently, the leakage current [85]. Therefore, $Si_{1-x}Ge_x$ can provide an extra degree of freedom in meeting the conflicting design requirements of performance and reliability. Whether inclusion of germanium degrades or improves the reliability performance of SiGe-base HBT devices remains to be answered.

It is the purpose of this research to carry out a detailed study of HBT degradation to provide some preliminary answers to the question. Important issues to be addressed first are the degradation behavior of SiGe-base HBTs under both forward and reverse stresses.

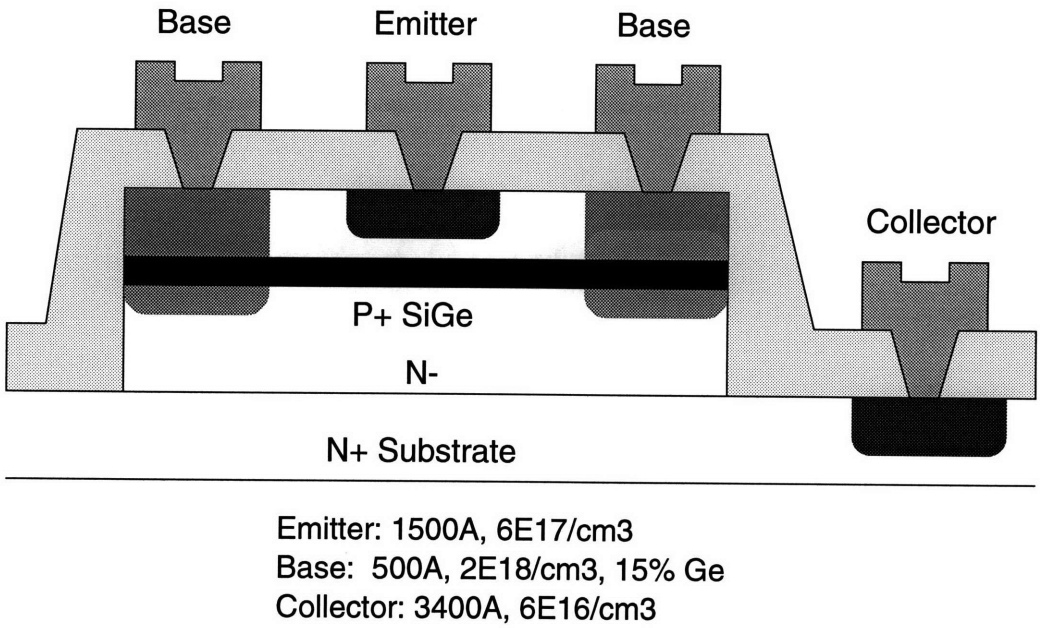


Figure 5-1: Schematic cross-section and typical parameters of the devices used in this work.

5.1 Experiments

SiGe-base HBT devices used in this work are of single-mesa type, fabricated with the "MESA" process described in Section 3.1.1. The epitaxial $Si/Si_{1-x}Ge_x/Si$ layers, with about 15% of Ge, are deposited in a commercially available APCVD system on heavily doped n+ substrates. Figure 5-1 shows a schematic cross-section and typical parameters of the devices. Fabricated devices with four different emitter dimensions — $4.5\mu m \times 4.5\mu m$, $2 \times 4.5\mu m \times 4.5\mu m$, $4.5\mu m \times 9\mu m$, and $3 \times 4.5\mu m \times 9\mu m$, and two different base doping levels — $2 \times 10^{18} cm^{-3}$ and $7 \times 10^{18} cm^{-3}$, are chosen for the stressing experiments. Note that the emitter dopant concentration is lower than that of the base. Devices are mounted on 28-pin sidebraze packages in order to fit the test fixture of HP4145B.

Experimental stress conditions are listed as follow:

(1) For the forward stress case, constant voltage sources are used to bias the devices

at current densities greater than 1mA/μm^2.

(2) For the inverse operation case, constant power supply is used to reverse bias the base-emitter junction at high voltage levels.

(3) For the reverse bias case, stress currents ranging from 10nA to 1mA, supplied by an HP4145B, are applied to the emitter-base junction with collector connection open.

The current stresses are interrupted periodically to measure the Gummel characteristics and junction leakage currents. The current gain β, change of base current ΔI_B, and junction leakage are used as parameters to monitor device degradations. All stresses and measurements are performed at room temperature.

5.2 High-forward-current Stress

In the forward stress case, the current density is greater than 1mA/μm^2. density level, base-emitter junction is typically biased at $\sim$2.5V. Gummel characteristics and junction leakages are monitored between periods of current stresses.

Figure 5-2 shows typical device characteristics before and after current stressing at >1mA/μm^2 for over 380 hours. Fluctuation of $\sim$10% in β and I_B are observed during the time period; this is probably due to competing mechanisms of generating and annealing of damages [87]. However, no significant degradation occurs in all devices stressed. This shows that SiGe HBTs do not suffer from early catastrophic degradation.

5.3 Reverse-voltage Stress

Figure 5-3 shows the device characteristics before and after a reverse stressing at V_{BE}=-5V for 180 hours; and, no degradation is observed. A homojunction device stressed under similar condition will show significant degradation. Figure 5-4 shows the emitter-base junction characteristics of the device. As we can see, the signature

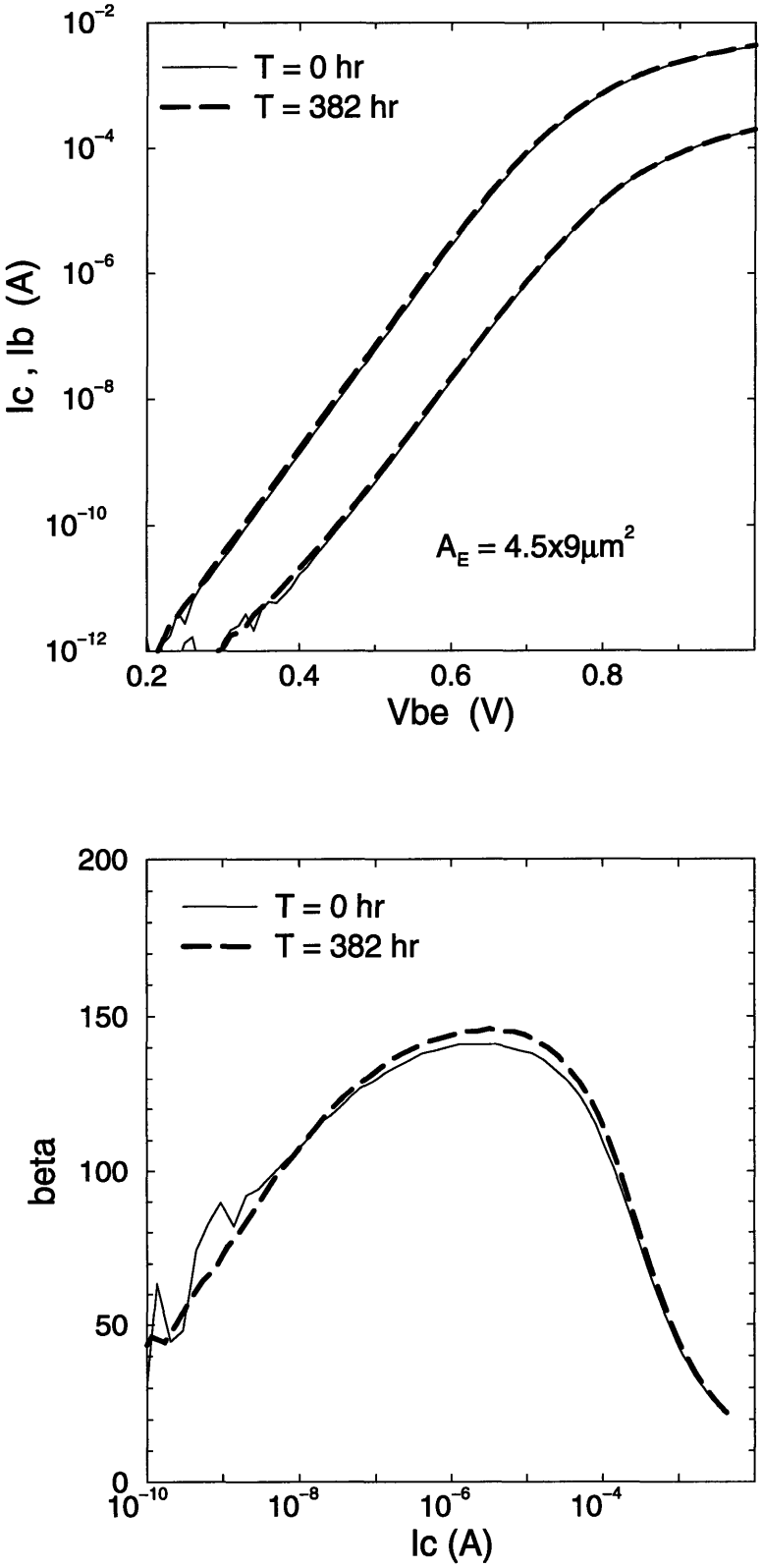
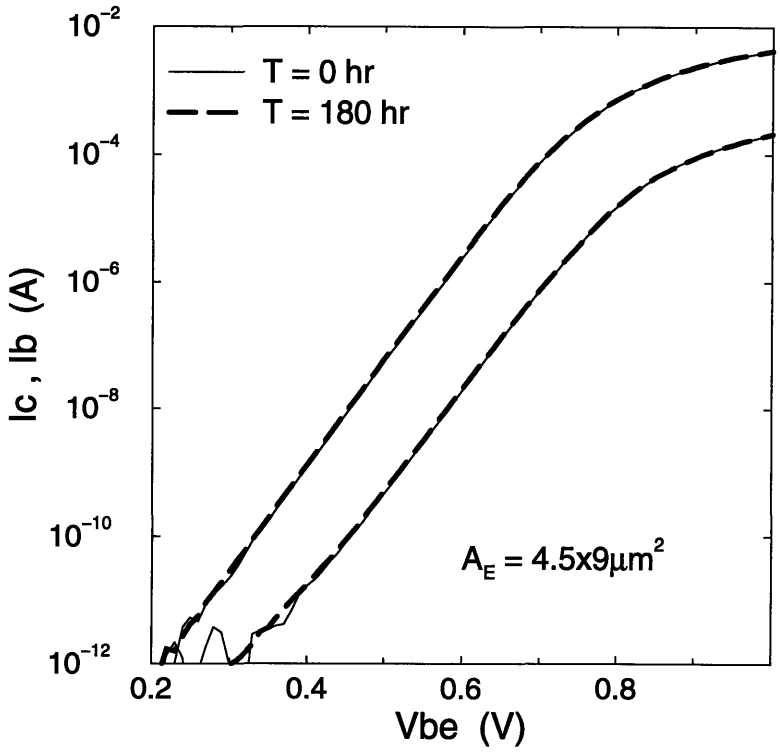


Figure 5-2: Device characteristics before and after current stressing at $>1\text{mA}/\mu\text{m}^2$ for 382 hours.



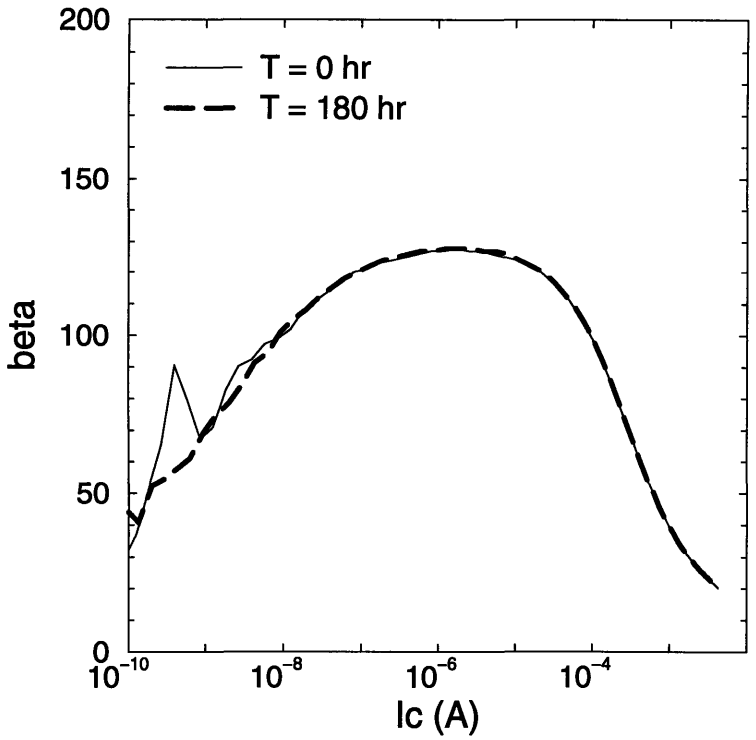


Figure 5-3: Device characteristics before and after reverse stressing at V_{BE}=-5V for 180 hours.

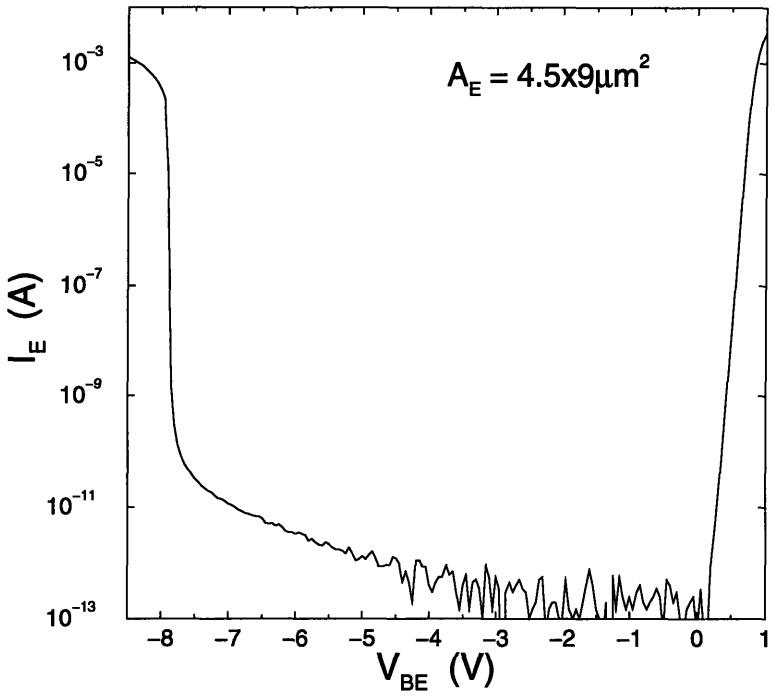


Figure 5-4: Emitter-base junction characteristics of a typical SiGe-base HBT

of the band-to-band tunneling, i.e. leakage current at moderate reverse biases, commonly observed in the modern homojunction devices is absent. This is because a lower emitter doping is used and the maximum electric field near the emitter-base junction is greatly reduced. The result, therefore, demonstrates that inclusion of Ge can potentially improve the reliability.

5.4 Reverse Current Stress

The effect of reverse biasing of emitter-base junction on the DC characteristics of bipolar transistors has been reported extensively [90–92]. It has been well established that the device current gain degrades due to hot carrier damages created at or near the boundary of the emitter-base depletion layer with sidewall oxide. Under reverse bias, the high electric field around the periphery generates hot carriers which result in an increase of interface state density and cause the forward base recombination

current to rise. Figure 5-5 is the Gummel plot of a typical device showing increases of I_B after repeated current stressing.

The conventional analysis of device degradation can be explained by the hot-electron degradation model In the model, change of the forward base current, ΔI_B, is used as an effective monitor. The excess forward base current, ΔI_B, can be accurately modeled by an empirical formula in [91]. ...

$$\Delta I_B = D J_C^{\eta} I_R^{m+n} t^n \tag{5.1}$$

The derivation of this result is straightforward. Hot-electron degradation model states that,

$$\frac{d\Delta}{dt} = C_1 G(\Delta) I_R e^{-\phi_t/kT_e} = C_1 G(\Delta) I_R e^{-B/E} \tag{5.2}$$

where

Δ : degradation monitor (ΔI_B in this case)

$G(\Delta)$: dependence of degradation rate on existing damages

ϕ_t : critical energy to create device damage

T_e : electron temperature, ($T_e = 8.5 \times 10^{-3} E$)

E : junction electric field.

If we further assume that $G(\Delta) \propto \Delta^{-h}$, i.e. assume a power law dependence of degradation rate on existing damages, the differential equation can be solved exactly. It can be straightforwardly shown that the close form solution to be:

$$\begin{aligned} \Delta &\propto \left[(I_R t) e^{-B/E}\right]^{1/(h+1)} = \left[Q e^{-B/E}\right]^{1/(h+1)} \\ &= A(I_R) Q^n = D J_C^{\eta} Q^n \end{aligned} \tag{5.3}$$

where we have let $1/(h+1) = n$, and defined $I_R t = Q$, the total accumulative stress charge.

ΔI_B plotted as a function of stress time is shown in Figure 5-6 for several different

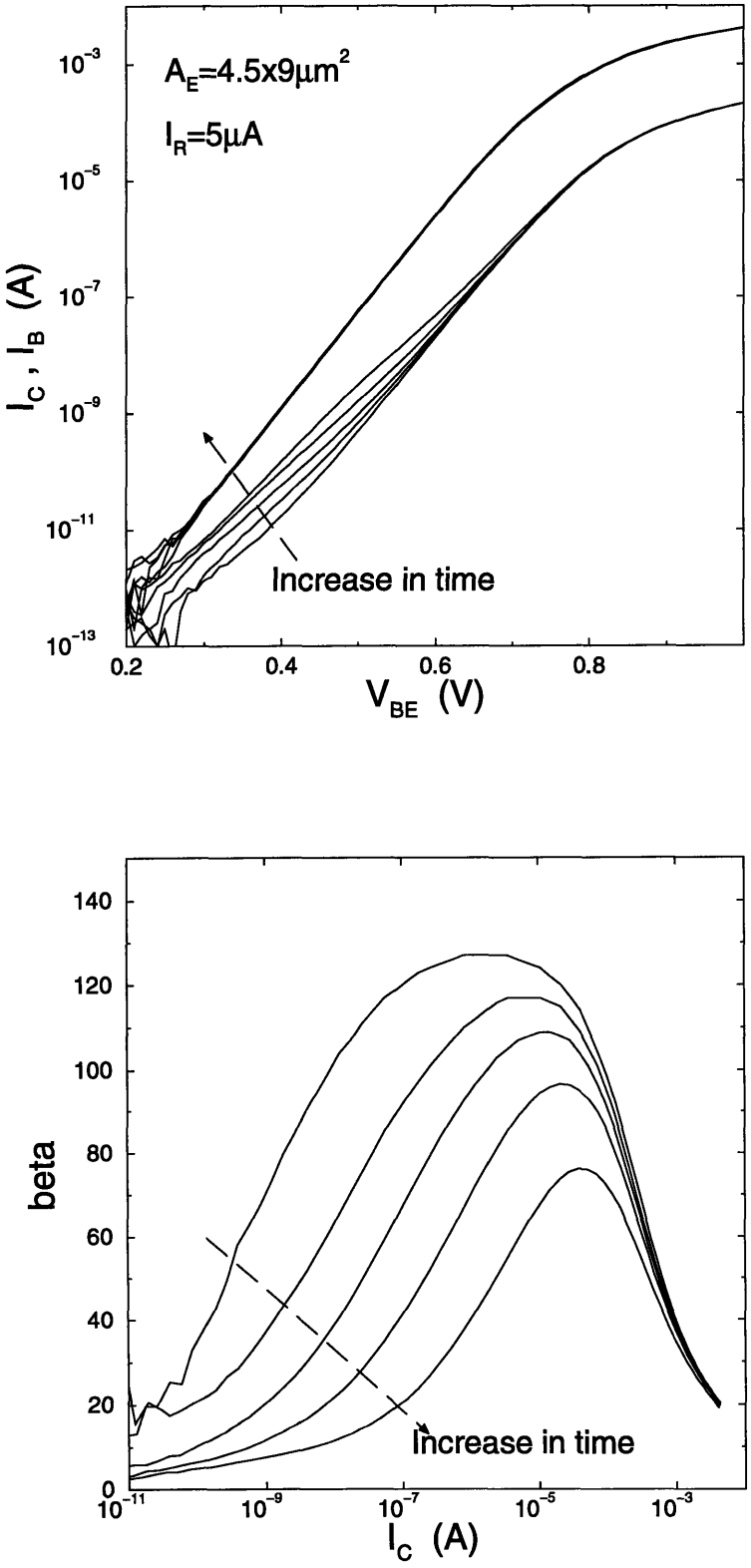


Figure 5-5: Gummel plot and β vs. I_C curves of a device stressed with reverse current, I_R, of 5μA.

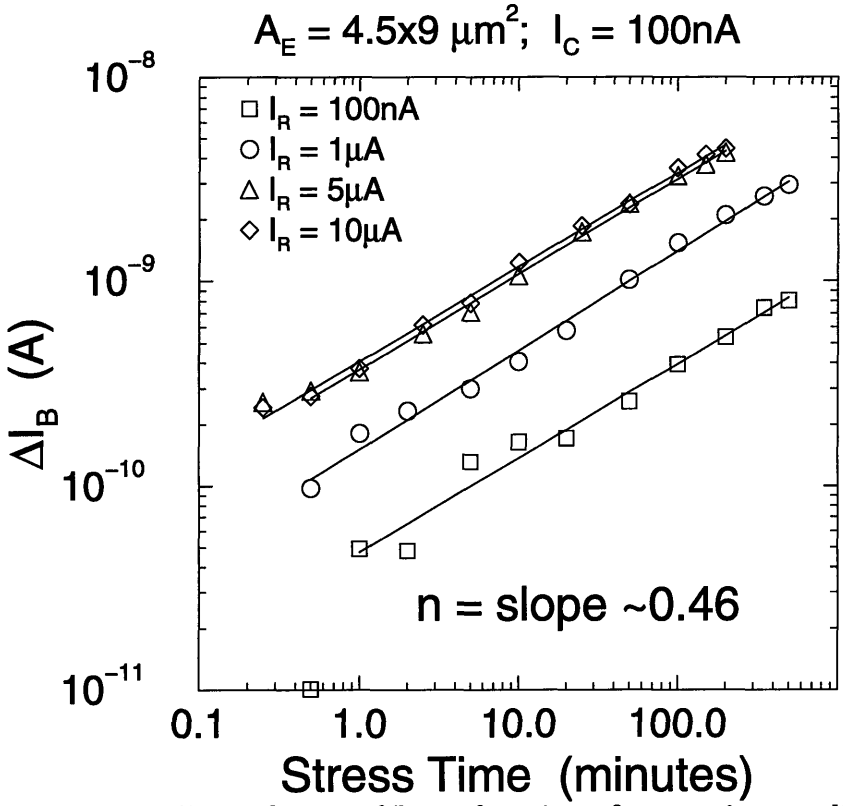


Figure 5-6: Degradation of I_B as function of stress time at different I_R.

reverse-bias stressing currents. All data fall on straight lines with slopes of ~0.46. This value is in good agreement with previously published Si BJT results of $0.3 < n < 0.7$. [91–93].

If we replot the figure with ΔI_B as function of total accumulative stress charge Q, we see that all data points merge onto a single straight line with the same slope of ~0.46, shown in Figure 5-7. The data indicates no dependence of degradation on stressing current I_R; this is because that all devices are operating under avalanche breakdown conditions, where junction electric fields are approximately the same [91]. Also observed is that there exists a threshold for creating device damages. Q_{crit} is found to be $\sim 2\times10^{-6}$C.

Figure 5-8 shows the power-law dependence of ΔI_B on I_C. The degradation has a weak dependent on I_R. The exponent η is found to be ~0.63 to 0.7. The significance of η is that it is approximately equal to the inverse of the base current ideality factor

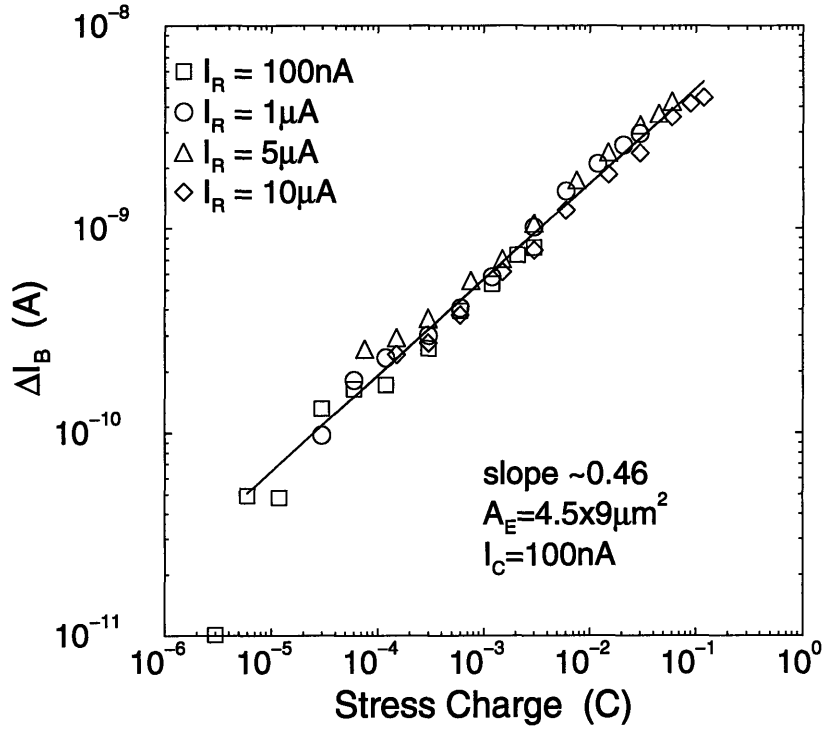


Figure 5-7: Degradation of I_B as function of stress charge at different I_R.

after device stressing.

Figure 5-9 examines the impact of device perimeter and area on ΔI_B. In agreement with an earlier report on homojunction devices, we also observe the degradation to be proportional to the perimeter/area ratio of the device [91]. Modern advanced BJTs are designed with high P/A ratio in order to improve current drive capability and to reduce emitter crowding effect.

Finally, dependence of degradation on base dopant concentration is investigated. It is interesting to note from Figure 5-10 that for the higher doping case, the degradation is greater but with a smaller slope. The observation of different slopes in the two cases may suggest different degradation mechanisms. The reason for the observation of different slopes is under further investigation.

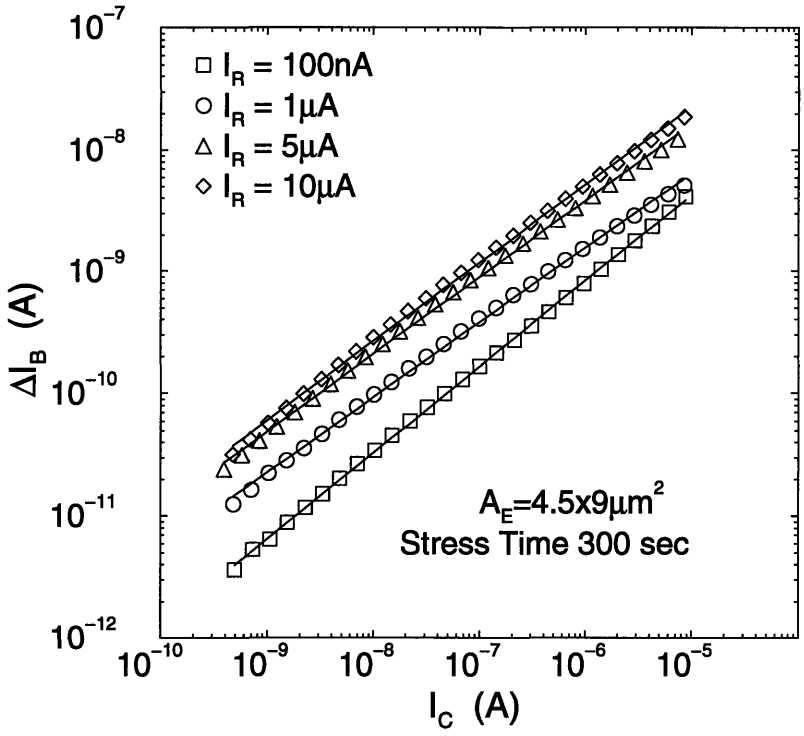


Figure 5-8: Degradation of I_B as function of collector current at different reverse stress currents.

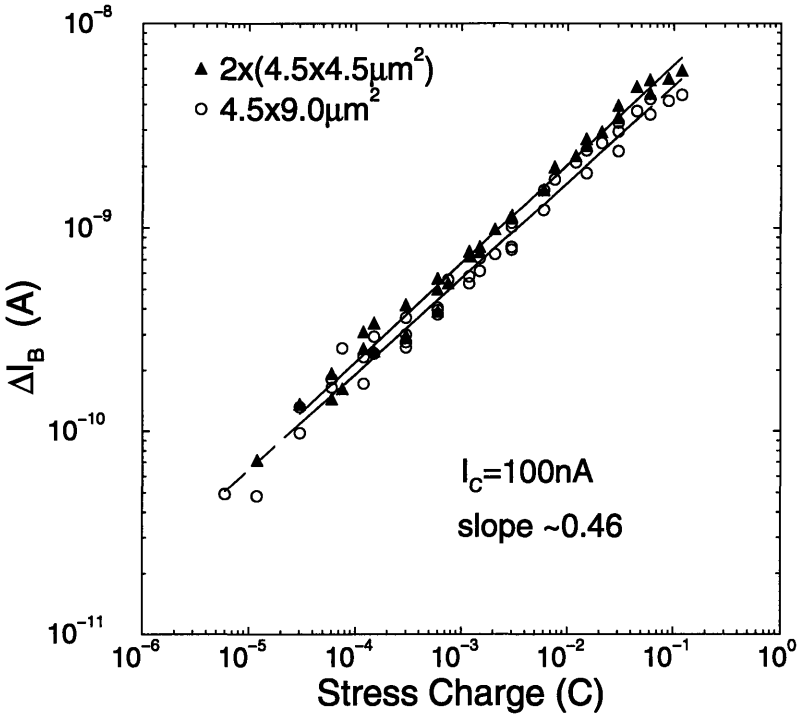


Figure 5-9: Effect of area/perimeter ratio on the degradation.

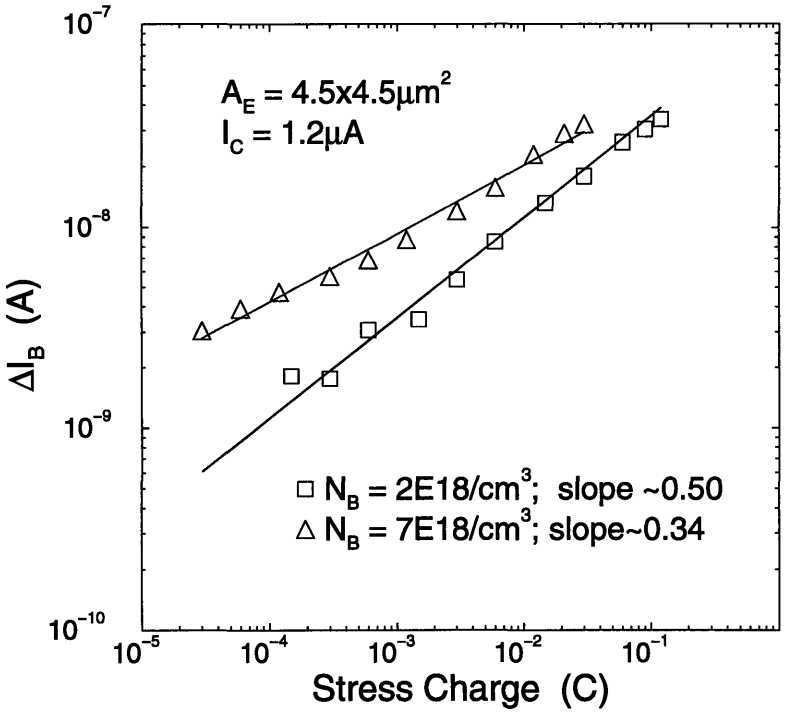


Figure 5-10: Effect of base doping level on the degradation under reverse bias.

5.5 Summary

We have conducted current and voltage stress experiments to examine the reliability of SiGe-base HBTs. Degradation of SiGe-base HBTs under high-forward-current and reverse-bias stresses are investigated. The study shows no significant degradation when devices were biased with high-forward currents. This indicates that SiGe HBTs do not suffer from early catastrophic degradation. In the reverse voltage stress, at V_{BE} = -5 V, no significant degradations were observed. Inclusion of Ge into the base may potentially improve the junction reliability of bipolar transistors. In the reverse current stress case, near avalanche condition, the observed degradation fits nicely with the empirical formula for Si homojunction devices. The observations are explained using existing homojunction theories. Dependences of degradation on the device perimeter/area and base dopant concentration were also reported.

Chapter 6

Conclusion and Suggestion for Future Research

The research leading to this thesis has focused on vertical profile engineering and stress reliability aspects of SiGe-base HBT development. Topics on the design, fabrication, characterization and modeling of SiGe-base HBTs were examined. Detailed analysis and experiments were carried out to achieve performance specifications suitable for high-speed analog applications. Major accomplishments and contributions include:

- Successful demonstration of epitaxial $Si/Si_{1-x}Ge_x/Si$ deposition on both patterned and unpatterned substrates using the Very-Low-Pressure Chemical Vapor Deposition (VLPCVD) reactor. Ex-situ and in-situ wafer cleaning procedures, deposition techniques as well as thermal stability of as-deposited films were investigated.

- Development of three process sequences, i.e. the "MESA", the "LOCOS" and the "POLY", for SiGe-base HBT device fabrication. The processes were consistent with the available tool set in the MTL-ICL and compatible with the MTL baseline 1.25μm twin-well CMOS technology. Upon completion of the fabrication, device and process parameters were extracted from both electrical and

material characterization, for further process modification as well as theoretical analysis.

- Functional devices with high current gain, excellent current ideality factors and good breakdown characteristics were obtained. Current gain exceeds 1000 has been measured in devices with 20% Ge in the base. High-frequency and 1/f noise measurements were performed. Matching of device current gains and turn-on voltages in the form of statistical measurement were investigated.

- Devices with several Ge contents, different base doping levels, forward- and retro-graded Ge profiles, and lightly-doped emitter structures were fabricated. Important observations included: collector current enhancement, tradeoff between β and V_A, and rapid rolloff of current gain.

- Observation of rapid rolloff of current gain in devices with lightly doped emitters. The effect was due to the formation of a parasitic barrier at the base-emitter junction resulting from dopant outdiffusion. A model based on the inverse Early effect was proposed to explain the observations and simulation using MEDICI were carried out to confirm the model. Modeling results indicated that the electrical characteristics of devices could be significantly altered if the misalignments between the p-n and hetero- junctions were greater than 50Å.

- Initiated the reliability study to examine degradation behavior of the SiGe-base HBT device under high-forward current and reverse bias stresses. Summary of the experimental results included: (1) Devices under high forward current stress with collector open showed no significant degradation for over 350 hours at current density >1 mA/μm^2. We concluded that the SiGe devices do not suffer from early catastrophic failure. (2) Devices stressed under high reverse field, with V_{BE}=-5 V, showed no degradation after 200 hours. (3) Devices

under reverse current stresses (biased near avalanche breakdown) showed significant degradation. Existing homojunction theory, the hot-electron degradation model, was used to explain the observation. For reverse current stress, the degradation was found to be proportional to the perimeter/area ratio of the device. Dependence of the degradation on base dopant concentration was observed.

In several areas, we have complemented what is already known in the literature and achieved better understanding of the basic device physics and device operation.

Finally, it is my hope to present some prospects of the SiGe technology for future generation of electronic devices at the end this thesis.

6.1 Technology Integration Issues

Since the first report of SiGe-base HBT device appeared in 1987, there has been a steadily increasing number of publication each year. Devices reported have achieved very impressive performance, setting records in the Si-based technology and challenging the position of III-V compound technology in the ultra-high speed applications. While SiGe technology has clearly demonstrated sufficient performance leverage to be commercially useful in many applications, there are still research and manufacturing issues to be addressed. In order to make this technology viable and to achieve desired level of integration, issues, such as thermal stability and device reliability, need to be closely examined. In addition, accurate device/process modeling.

Thermal Stability

The main problems facing this technology are the constraints that the metastable nature of the film places on Ge content, layer thickness, subsequent thermal cycling, and effective process integration. Strain relaxation in an HBT will lower th bandgap difference between the Si and $Si_{1-x}Ge_x$ causing a degradation in injection efficiency

and a reduction in current gain. Also, misfit dislocations that accompany strained relaxation can act as generation-recombination centers to increase leakage current.

One of the biggest concerns in the manufacturing issues of SiGe devices is the stability of the strained layers. $Si_{1-x}Ge_x$ films used in most device layers are meta-stable in nature, in order to realize to the utmost potential. However, it is inevitable that the $Si_{1-x}Ge_x$ films be subjected to thermal treatment after deposition. Maintaining the integrity of the films poses the biggest challenge. Therefore, prior knowledge of the maximum allowable thermal treatment is essential in defining the device process. There exists numerous works in the area of thermal stability of $Si_{1-x}Ge_x$ films; however, most reports are confined to the study of blanket (unpatterned) films and informations on patterned layers remain limited. It is believed that the patterned films with small island-like structures, will have somewhat higher tolerance of the heat treatment because of different boundary conditions. However, this remains to be seen and definitely requires concentrated effort.

The sensitivity of the pseudomorphic SiGe layers to high temperatures generally requires new fabrication technology, differing from the process presently employed. Several new fabrication schemes have been reported, but all of them so far either restrict the possible range of HBT layer composition (and therefore device performance), or the process prohibits device integration. Further development of fabrication technologies is required in order to fully exploit the advantages of SiGe HBTs.

Device Reliability

The assessment of device reliability is an important manufacturing issue because it ultimately affects the overall yield and long-term operating stability of the fabricated circuits. These valuable informations will enable engineers to find solutions to the imposed limitations, and to improve device and process designs.

So far, several reports on the device reliability have been reported. The promising result is that SiGe device seems to behave like a homojunction device regarding to the

reliability. No anomalies have been observed and existing homojunction theory can adequately explain the observations. However, research efforts needed to be carried one step further by investigating the effect of high temperature stress, in hope to identify possible device degradation and failure mechanism that are generic to the strained Si/SiGe systems.

Process/Device Modeling

Process and device simulation tools are widely used in the technology development nowadays. The objective of using these simulators has been to minimize the costly empirical approach. For example, the number of traditional wafer split-runs can be dramatically reduced by using process simulation to obtain target parameters. Simulation can significantly reduce the cost of developing a new IC technology or modifying an existing one. In addition, some important benefits can be gained by effectively using process simulation tools: (1) the development cycle of a new technology can be made much shorter; (2) simulation allows the analysis of effects that cannot be measured directly; and, (3) process sensitivity and tradeoffs in device design can be analyzed.

There exists several device and process simulation programs; however, most of them are suffering from lack of accurate model parameters. Many of the physical processes involved in SiGe process are still not completely understood. Detail informations on the band alignment, heavy doping effect, mobility, other transport properties, and strain effect are not readily available. Effects such as tunneling, alloy grading, and parasitic barrier are not completely taken into account. Design windows for effects such as: a) heterojunction barrier phenomena, b) the bias dependent current gain induced by Ge grading at the emitter-base junction, and c) the much stronger temperature dependence of device parameters compared to Si BJT's, must be quantified.

Some important device and circuit design issues centering on the SiGe/Si het-

erojunction exist. Accurate device and circuit models need to be developed, and the impact of these effects on the overall performance and reliability of large circuit functions must be assessed. SiGe transistors can be modeled using the same large-signal Gummel-Poon and small-signal hybrid-π models for homojunction Si devices. Eventually it will be quite beneficial to see an accurate parameter extraction program being developed. It will cut down the cost of implementation. Also, it can provide circuit designer better tool to work with.

6.2 Applications

The development of SiGe-base HBTs has matured technologically over the years with devices demonstrating very impressive figures of merit, setting records in the Si-based technology and challenging the position of III-V compound technology in the ultra-high speed applications. However, their full potential in the circuit implementation has yet to be fully realized. Two of the most promising applications for SiGe-base HBTs, in the area of wireless and low-temperature applications, are presented in this section.

Wireless applications

New systems in wireless digital communications require high performance, low cost RF components operating from few hundred MHz to several GHz. Because of its inherent merits, such as high f_T and f_{max}, low noise figure and high Early voltage, SiGe-base HBT is well-suited for various applications, such as low noise amplifiers, wideband amplifiers and oscillators.

SiGe-base HBT technology has moved from merely a laboratory curiosity into mainstream development in the past few years. A flourish of results, demonstrating its utmost potential, will be presented in the BCTM conference later this year: including a 23 GHz static frequency divider, 5 GHz comparator, 12 GHz bandwidth Gilbert

mixers, and a 18 GHz wideband amplifier.

In foreseeable future, the development of SiGe technology may provide highly integrated, low power consumption, low voltage, surface mount transceiver integrated circuits manufacturable at very low cost in large volume.

Low Temperature Electronics

Low temperature operation is an attractive method to realize high circuit performance. For CMOS transistors, low temperature operation provides higher carrier mobility and lower threshold voltage, and therefore high-speed operation at low supply voltage. The interconnect delay also decreases due to the reduction of wiring resistance at reduced temperature.

However, traditionally, bipolar transistors performs poorly at reduced temperature due to several inherent limitations. The first problem is a severe degradation of current gain. Advanced bipolar transistors have emitter dopant concentration of exceeding 1×10^{20} cm^{-3}; the effective bandgap of the emitter is reduced because of heavy doping effect. As a result of the narrower bandgap in the emitter than in the base, the current gain decreases exponentially with lowering of operating temperature. The second problem is an increase of base resistance. Typical base doping level of bipolar devices is limited to below 3×10^{18} cm^{-3}. With the lowering of operating temperature, base resistance can increase sharply due to carrier freeze-out effect in the base region [94]. The third problem is an increase in base-emitter turn-on voltage at low temperature due to the exponential decrease in carrier concentration [26]. Higher turn-on voltage of bipolar transistors at low temperature wastes the supply voltages and reduces the output level. As a result, the switching speed of circuits degrades significantly.

Heterojunction provides solutions to some of these existing dilemma. The degradations mentioned above can be improved by using $Si_{1-x}Ge_x$ alloy as the narrow bandgap material in the base region of a heterojunction bipolar transistor. SiGe-base

Crystalline Alloys of Group IV Semiconductors			
BINARY	$Si_{1-x}C_x$	$Ge_{1-x}C_x$	$Sn_{1-x}C_x$
	$Si_{1-x}Ge_x$	$Si_{1-x}Sn_x$	$Ge_{1-x}Sn_x$
TERNARY	$Si_{1-x-y}Ge_xC_y$		$Si_{1-x-y}Sn_xC_y$
	$Si_{1-x-y}Ge_xSn_y$		$Sn_{1-x-y}Ge_xC_y$
QUATERNARY	$Sn_{1-x-y-z}Ge_xSi_yC_z$		

Table 6.1: Composition of group IV materials.

HBTs, which have the reversed bandgap difference between the base and emitter, show higher current gain at low temperature and allow sufficiently high doping levels in the base to prevent carrier freeze-out [26,27]. In addition, SiGe-base HBTs, having lower turn-on voltages, can achieve high speed switching characteristics at low supply voltage.

6.3 Future Materials and Devices

Semiconductor heterostructures greatly enhance the range of possible device configurations and open the door to new physical phenomena such as tunneling, alloy grading, two-dimensional carrier gases, ballistic transport and so on [5]. Most of the heterojunction device concepts are first realized in III-V compound material systems, such as AlGaAs/GaAs, InGaAs/InP, and, more recently, in IV-IV $Si_{1-x}Ge_x$/Si system. In principle the same theoretical and experimental frameworks can be extended to other semiconductors.

Since silicon is the dominant semiconductor material for the electronics industry, there have been continuing interests and developments in other Si-compatible material systems. In particular, alloys of Si with the rest of group IV elements (C,Ge,Sn) are the most likely candidates because cross-doping can be avoided [5]. Table 6.1 lists all conceivable binary, ternary, and quaternary group IV alloys,

SiC is widely researched as a material for widegap emitter of SiC/Si HBTs. The

unique properties of SiC make it suitable for high-temperature, high-power microwave transistors [95]. SiGeC is another attracting material because it offers widely variable bandgap as well as exact lattice-matching with Si.

Other notable development of SiGe-based devices include the SiGe-channel MODFET and photodetectors . SiGe-channel MODFET is gaining increasing attention in recent years because of the high mobility that can be achieved [4, 96, 97]. In the MODFET, the epitaxial layer structure is designed so that free electrons in the channel are physically separated from the ionized donors, enhancing electron mobility by reducing ionized impurity scattering. Take advantage of modulation doping in SiGe or Si to achieve "collision-free" high mobility in the two-dimensional electron or hole gases within the n- or p-channel, respectively.

It has long been known that the fundamental (indirect) bandgap of bulk $Si_{1-x}Ge_x$ alloys spans the $1.3 - 1.55$ μm range where silica communications fibers have the lowest losses. This also makes $Si_{1-x}Ge_x$ extremely attractive for applications involving long wavelength integrated optoelectronics on Si.

Appendix A

Carrier Transport in Neutral Base Region

In this appendix, an overview of the transport equations describing electron (and hole) motion and density in materials with nonuniform band structure is presented. The treatment can be extended to include structures with graded composition and heterojunctions, materials under nonuniform temperature or strain, and devices with highly doped regions [98–102]. In particular, we will concentrate on the derivation of semiconductor device equations, similar to the Schokley formulation, for heterojunction bipolar transistors.

Following closely the approach employed by Marshak and van Vlet [103–105], we first derive, in a summarizing fashion, the generalized drift-diffusion equations for heterostructure materials as a special case. We then use the generalized drift-diffusion equations to arrive at the current and transit time equations for the heterojunction bipolar transistors.

A.1 Energy Band Structure

The theory of band structure, i.e. the energy-momentum relation, forms the basis for the modern theory of carrier transport in a crystalline solid. It is obtained by solving the Schrodinger equation of an approximate one-electron problem with the consideration of the periodicity of crystal structure . The topic has been well discussed in many elementary quantum mechanics and solid-state physics books and will not be presented here [43, 44, 106].

Consider a material under influence of external force, in general the energy eigenvalues, i.e. solutions of the Schrodinger equation, can be written as:

$$\mathcal{E}_\beta = \mathcal{E}_{\beta o} + \Delta\mathcal{E}_\beta \tag{A.1}$$

where $\mathcal{E}_{\beta o}$ is the unperturbed band structure, $\Delta\mathcal{E}_\beta$ is the deviation due to external force, and β is the band index. The total energy (for band β) of a carrier in the material is then equal to:

$$E_\beta = \mathcal{E}_\beta + \psi \tag{A.2}$$

where ψ is the potential that gives rise to the external force. In general, $\psi = \psi(r)$, therefore, the total energy will be a function of position and the material will have a position dependent band structure. Use the semiclassical approach, total energy in the 6-dimensional phase space is:

$$E_\beta(k, r) = \mathcal{E}_\beta(k, r) + \psi(r) \tag{A.3}$$

The usual $\vec{r}$-space band diagram is then defined as:

$$E_{\beta,contour}(r) = \mathcal{E}_\beta(k_m, r) + \psi(r) \tag{A.4}$$

where k_m corresponds to band extrema. Or equivalently, the conduction band energy

can be written as:

$$E_c(r) = \mathcal{E}(k_{min}, r) + \psi(r) = \mathcal{E}_c(r) + \psi(r) \tag{A.5}$$

and, the valence band energy as:

$$E_v(r) = \mathcal{E}(k_{max}, r) + \psi(r) = \mathcal{E}_v(r) + \psi(r) \tag{A.6}$$

where $\mathcal{E}_c(r)$ and $\mathcal{E}_v(r)$ are the unperturbed band edges.

* Rewrite

$$\begin{aligned} E(k,r) &= E_c(r) + [\mathcal{E}(k,r) - \mathcal{E}_c(r)] \\ &= E_v(r) + [\mathcal{E}_v(r) - \mathcal{E}(k,r)] \end{aligned} \tag{A.7}$$

* We can define the concept of "local kinetic energy":

$$\begin{aligned} W_e(k,r) &= \mathcal{E}(k,r) - \mathcal{E}_c(r) \\ W_h(k,r) &= \mathcal{E}_v(r) - \mathcal{E}(k,r) \end{aligned} \tag{A.8}$$

A.2 Modified Boltzmann Transport Equation

Correspondence Principle:

* The equivalent (quantum mechanical) Hamiltonian, $\hat{H}_\beta$,

$$\hat{H}_\beta = \mathcal{E}_\beta(-i\nabla, r) + \psi(r) \tag{A.9}$$

and, * The classical Hamiltonian, H_β,

$$H_\beta = \mathcal{E}_\beta(k,r) + \psi(r) = E_\beta(k,r) \tag{A.10}$$

Hamilton's Equations:

$$\frac{d\vec{r}}{dt} = v_{k\beta} = \frac{\partial H_\beta}{\partial p} = \frac{1}{\hbar}\nabla_k \mathcal{E}_\beta \qquad \text{(A.11)}$$
$$\hbar\frac{dk}{dt} = -\frac{\partial H_\beta}{\partial r} = -\nabla E_\beta$$

* Boltzmann equation in its general form:

$$\frac{df}{dt} = C[f] \qquad \text{(A.12)}$$

where $f(r,k,t)$ is the carrier distribution function and $C[f]$ is the collision integral. Or, more specifically,

$$\begin{aligned} \frac{df}{dt} &= \frac{\partial f}{\partial t} + \frac{\partial f}{\partial r}\cdot\frac{dr}{dt} + \frac{\partial f}{\partial k}\cdot\frac{dk}{dt} \\ C[f] &= \frac{-(f-f^o)}{\tau} \end{aligned} \qquad \text{(A.13)}$$

* For electron (conduction band):

$$\frac{\partial f}{\partial t} + v_k\cdot\nabla f - \frac{1}{\hbar}(\nabla E_c + \nabla W_e)\cdot\nabla_k f = \frac{-(f-f^o)}{\tau_e} \qquad \text{(A.14)}$$

Note: the extra term is resulting from position dependence of kinetic energy.

A.3 Solution to the Stationary Transport Equation

Perturbation approximation:

* Writing $f = f^o + f^1$,

$$f^1 = -\tau_e\left[v_k\cdot\nabla f^o - \frac{1}{\hbar}(\nabla E_c + \nabla W_e)\cdot\nabla_k f^o\right] \qquad \text{(A.15)}$$

* The electron current is defined as usual,

$$\begin{aligned} J_n &= -\frac{q}{4\pi^3}\int v_k f d^3k \\ J_n &= \frac{q}{4\pi^3}\int d^3k v_k \tau_e \left[v_k \cdot \nabla f^o - \frac{1}{\hbar}(\nabla E_c + \nabla W_e)\cdot \nabla_k f^o\right] \end{aligned} \tag{A.16}$$

* The local equilibrium distribution function is given by:

$$f^o = \frac{1}{1+\exp[(E(r,k)-E_{fn}(r))/k_BT]} \tag{A.17}$$

* After some algebra,

$$J_n = -\frac{q}{4\pi^3}\int d^3k \tau_e \frac{\partial f^o}{\partial E} v_k v_k \cdot \nabla E_{fn} = n\mu_n \cdot \nabla E_{fn} \tag{A.18}$$

Note: this result is identical to that of a material with fixed band structure; and the effects involving ∇W is hidden.

A.4 Generalized Drift and Diffusion

* We have derived

$$J_n = n\mu_n \cdot \nabla E_{fn} \tag{A.19}$$

* Consider the normalization integral:

$$n(r) = \frac{1}{4\pi^3}\int_{E_c}^{\infty} d^3k f^o(E, E_{fn}) \tag{A.20}$$

From this,

$$\begin{aligned} \nabla n &= \frac{1}{4\pi^3}\int d^3k \left[\frac{\partial f^o}{\partial E}(\nabla E_c + \nabla W_e) + \frac{\partial f^o}{\partial E_{fn}}\nabla E_{fn}\right] \\ &= \left(\frac{\partial n}{\partial E_{fn}}\right)(\nabla E_{fn} - \nabla E_c) + \frac{1}{4\pi^3}\int d^3k \frac{\partial f^o}{\partial E}\nabla W_e \end{aligned} \tag{A.21}$$

* We get

$$\nabla E_{fn} = \nabla E_c + \left(\frac{\partial E_{fn}}{\partial n}\right) \nabla n + \left(\frac{\partial E_{fn}}{\partial n}\right) \frac{1}{4\pi^3} \int d^3k \frac{\partial f^o}{\partial E} \nabla W_e \tag{A.22}$$

* Define ∇n^* by

$$\nabla n^* = \frac{1}{4\pi^3} \int d^3k \frac{\partial f^o}{\partial E} \nabla W_e \tag{A.23}$$

* Use the generalized Einstein relation:

$$qD_n = \mu_n \left(\frac{\partial E_{fn}}{\partial \log n}\right) \tag{A.24}$$

* We arrived at the generalized drift-diffusion equation:

$$J_n = n\mu_n \cdot \nabla E_c + qD_n \cdot \nabla n - qD_n \cdot \nabla n^* \tag{A.25}$$

Appendix B

"POLY" Process

B.1 Process Description

Step	Process Description
1	**Run Make-Up** Starting wafer: Si (100), n+ substrate, w/ 500nm of n- epi (or thicker) Scribe ID's on wafers [*opset*: begin.set]
2	**Stress Relief Oxide** (43nm) RCA clean 950°C, dry O_2, 100min 950°C, N_2, 30min [*opset*: dsro430.set; *recipe*: 210]
3	**LPCVD Silicon Nitride** (150nm) 800°C, SiH_2Cl_2 and NH_3 [*opset*: dnit1.5k.set; *recipe*: 410]
4	**Active Area Pattern** HMDS Positive Photoresist (1.0μm) Mask ID: ACT (SIGE2P)

[*opset*: phactive.set]

5 **Nitride Plasma Etch** (Lam Etcher)
SF_6 + He Plasma
[*opset*: plnit1.5k.set; *recipe*: 15]

6 **Resist Ash**
O_2 Plasma
[*opset*: ash.set]

7 **Field Oxide** (510nm)
RCA clean
950°C, dry O_2, 30min
950°C, wet O_2, 200min
950°C, dry O_2, 30min
950°C, N_2, 30min
[*opset*: dfield5.1k.set; *recipe*: 240]

8 **Nitride Wet Etch**
7:1 BOE dip
[*opset*: wox.set]
Transetch-N, 180°C
[*opset*: wnit1.5k.set]

9 **SRO Removal**
7:1 BOE dip
[*opset*: wsro430.set]

10 **Dummy Pad Oxidation** (100nm)
RCA clean
950°C, dry O_2, 180min
[*opset*: dox1k.set; *recipe*: 100]

11 **LPCVD Base Polysilicon** (100nm)
625°C, SiH_4
[*opset*: dpoly1k.set; *recipe*: 422]

12 **Base Polysilicon Implantation** (w/o resist)
Boron, Energy 30KeV, Dose $2 \times 10^{14}\text{cm}^{-2}$
(note: may leave this step out until later)
[*opset*: ip+poly.set]

13 **Base Polysilicon Pattern**
HMDS
Positive Photoresist (1.0μm)
Mask ID: PIR (SIGE2P)
[*opset*: phepi.set]

14 **Base Polysilicon Plasma Etch**
CCl_4 + He plasma
[*opset*: plbase.set; *recipe*: 10]

15 **Resist Ash**
O_2 plasma
[*opset*: ash.set]

16 **Pad Oxide Removal**
7:1 BOE dip
[*opset*: wox.set]

17 **Epitaxial Growth**
VLPCVD/APCVD Si/SiGe/Si deposition
[*opset*: dsige.set]

18 **Low Temperature Oxide (LTO) Deposition** (50nm)
RCA clean
400°C, SiH_4 and O_2
[*opset*: dlto500.set; *recipe*: 439]

19 **Collector Region Pattern**
HMDS
Positive Photoresist (1.0μm)
Mask ID: BAS (SIGE2P)
[*opset*: phbas.set]

20 **Oxide/Poly/Oxide Etch**
7:1 BOE dip
[*opset*: wox.set]
SF_6 + CCl_4 + He plasma
[*opset*: plpoly3k.set; *recipe*: 100]
7:1 BOE dip
[*opset*: wox.set]

21 **N+ Plug Implantation** (w/ resist)

Phosphorus, Energy 150KeV, Dose $2\times10^{15}cm^{-2}$
(note: may be skipped if n+ substrates are used)
[*opset*: in+plug.set]

22 **Resist Ash**
O_2 plasma
[*opset*: ash.set]

23 **LTO and Collector Pad Oxide Removal**
7:1 BOE dip
(note: may be done in step 20)
[*opset*: wox.set]

24 **Low Temperature Oxide Deposition** (50nm)
RCA clean
400°C, SiH_4 and O_2
[*opset*: dlto500-2.set; *recipe*: 439]

24a **LTO Densification Step**
furnace, 800°C, boat-in/boat-out
[*opset*: danneal.set]

25 **Emitter Area Pattern**
HMDS
Positive Photoresist (1.0μm)
Mask ID: NIR (SIGE2P)
[*opset*: phemitter.set]

26 **Emitter Oxide Opening**
50:1 HF dip
[*opset*: wlto500.set]

27 **Resist Strip**
piranha clean
[*opset*: wpiranha.set]

28 **LPCVD Emitter Polysilicon (270nm)**
RCA clean, HF dip
625°C, SiH_4
[*opset*: dpoly2.7k.set; *recipe*: 443]

29 **Emitter Polysilicon Implantation (w/o resist)**

Phosphorus, Energy 60KeV, Dose $3\times10^{15}cm^{-2}$
[*opset*: in+o.set]

29a **Emitter Implant Activation**
RTA (to ensure uniform poly etch)
[*opset*: drta.set]

30 **Emitter Polysilicon Pattern**
HMDS
Positive Photoresist (1.0μm)
Mask ID: CP (SIGE2P)
[*opset*: phn+poly.set]

31 **Emitter Polysilicon Plasma Etch**
CCl_4 + He plasma
[*opset*: plpoly3k.set; *recipe*: 100]

32 **Extrinsic Base Ion Implantation (w/ resist)**
Boron, 30KeV, Dose $2\times10^{14}cm^{-2}$
BF_2, 60KeV, Dose $1\times10^{15}cm^{-2}$
[*opset*: ip+exb.set]

33 **Resist Ash**
O_2 plasma
[*opset*: ash.set]

34 **Low Temperature Oxide Deposition** (500nm)
RCA clean
400°C, SiH_4 and O_2
[*opset*: dlto5k.set; *recipe*: 430]

35 **Implant Drive-in (furnace)**
800°C, N_2 + O_2, 30 min
[*opset*: danneal.set]

36 **Resist Coat (front)**
HMDS
Positive Photoresist (1.0μm)
[*opset*: phcoat.set]

37 **Backside Clean**
Oxide Wet Etch, 7:1 BOE dip

[*opset*: wox.set]
Poly Etch, SF_6 + O_2 plasma
[*opset*: plpoly5k.set; *recipe*: 10]
Oxide Wet Etch, 7:1 BOE dip
[*opset*: wox.set]

38 **Resist Clean**
O_2 plasma
[*opset*: ash.set]
Piranha strip; 3:1 H_2SO_4:H_2O_2
[*opset*: wpiranha.set]

39 **Contact Pattern**
HMDS
Positive Photoresist (1.0μm)
Mask ID: CC (SIGE2P)
[*opset*: phcont.set]

40 **Contact Plasma Etch**
CF_4 + CHF_3 + He plasma
[*opset*: pllto.set; *recipe*: 24]

41 **Contact Wet Clean**
Ash in O_2 plasma, 2 min
7:1 BOE dip
[*opset*: wclean.set]

42 **Resist Ash/ Piranha Clean/ HF Dip**
O_2 plasma
[*opset*: ash.set]
3:1 H_2SO_4:H_2O_2, 10 min
[*opset*: wpiranha.set]
50:1 H_2O:HF, 1 min

43 **Metal Deposition** (1.0μm)
Ti/Al-Si(1%) Alloy (front side)
Al-Si(1%) Alloy (back side)
[*opset*: mAl1u.set]

44 **Metal Pattern**
HMDS
Positive Photoresist (1.4μm)

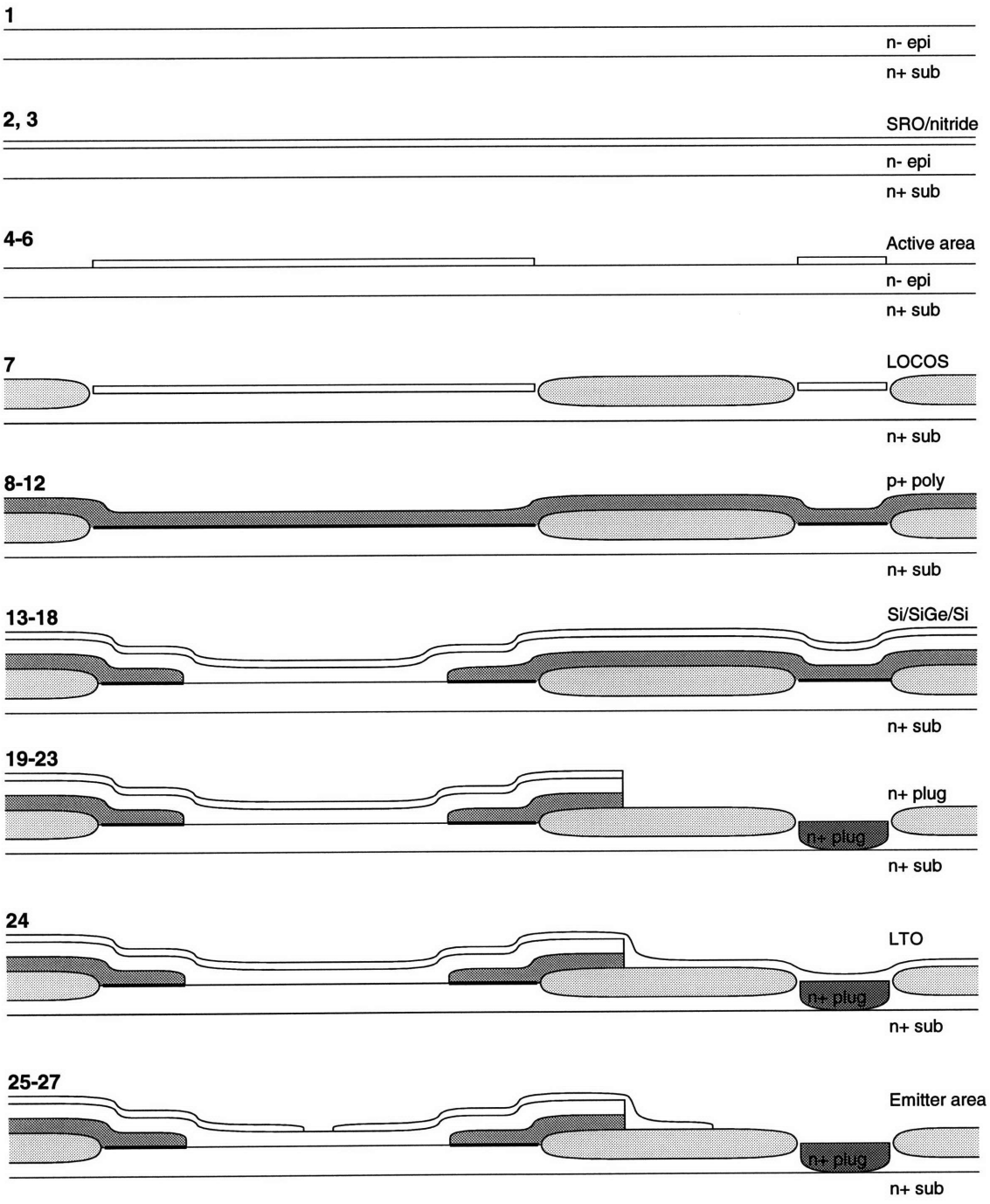
Mask ID: CM (SIGE2P)
[*opset*: phmetal.set]

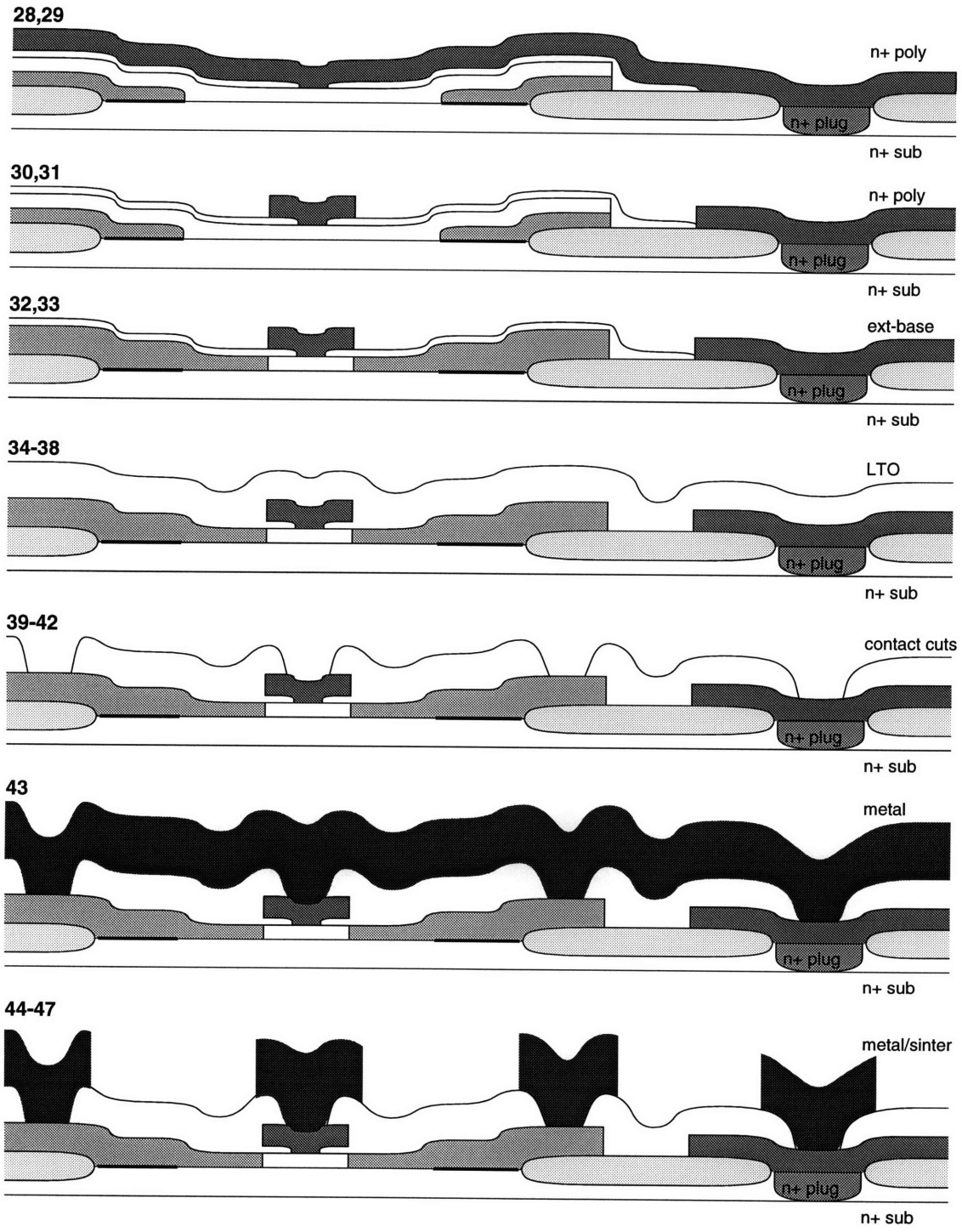
45 **Metal Plasma Etch**
$BCl_3 + CHCl_3 + Cl_2 + N_2$ plasma
[*opset*: plmetal.set; *recipe*: 32]

46 **Resist Ash**
O_2 plasma
[*opset*: ash.set]

47 **Sinter**
Dump rinse
400°C, Forming gas, 30min
[*opset*: dsinter.set; *recipe*: 710]

B.2 Process Cross-section




28,29
n+ poly
n+ plug
n+ sub
30,31
n+ poly
n+ plug
n+ sub
32,33
ext-base
n+ plug
n+ sub
34-38
LTO
n+ plug
n+ sub
39-42
contact cuts
n+ plug
n+ sub
43
metal
n+ plug
n+ sub
44-47
metal/sinter
n+ plug
n+ sub

B.3 Mask Layers

Mask#	Mask ID		Description
1	ACT	clear	active area definition
2	PIR	dark field	epi region
3	BAS	clear field	base-emitter region
4	NIR	dark field	emitter and collector opening
5	CP	clear field	N+ poly
6	CC	dark field	Contact cuts
7	CM	clear field	Metal patterning

Bibliography

[1] J. C. Bean, L. C. Feldman, A. T. Fiory, S. Nakahara, and I. K. Robinson, "Ge_xSi_{1-x}/Si strained-layer superlattice grown by molecular beam epitaxy," *J. Vac. Sci. Technol. A*, vol. 2, p. 436, 1984.

[2] B. S. Meyerson, "Low temperature silicon epitaxy by ultrahigh vacuum chemical vapor deposition," *Appl. Phys. Lett.*, vol. 48, p. 797, 1986.

[3] B. S. Meyerson, "UHV/CVD Growth of Si and Si:Ge Alloys: Chemistry, physics, and device applications," *Proc. IEEE*, vol. 80, no. 10, p. 1592, 1992.

[4] S. Verdonckt-Vanderbroek, E. F. Crabbe, B. S. Meyerson, D. L. Harame, P. J. Restle, J. M. C. Stork, A. C. Megdanis, C. L. Stanis, A. A. Bright, G. M. E. kroesen, and A. C. Warren, "High-mobility modulation-doped gradded SiGe-channel p-MOSFET's," *IEEE Electron Device Letter*, vol. 12, no. 8, p. 447, 1991.

[5] J. C. Bean, "Silicon-based semiconductor heterostructures: column IV bandgap engineering," *Proc. IEEE*, vol. 80, no. 4, p. 571, 1992.

[6] R. P. Karunasiri and K. L. Wang, "Infrared photodetectors with SiGe/Si multiple quantum wells," *Optical Engineering*, vol. 33, no. 5, p. 1468, 1994.

[7] R. A. Soref, "Silicon-based optoelectronics," *Proc. IEEE*, vol. 81, no. 12, p. 1687, 1993.

[8] S. S. Iyer, G. L. Patton, S. L. Delange, S. Tiwari, and J. M. C. Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," *IEEE IEDM Tech. Dig.*, p. 874, 1987.

[9] T. I. Kamins, K. Nauka, J. B. Gruger, J. L. Hoyt, C. A. King, D. Noble, C. Gronet, and J. F. Gibbons, "Small-geometry, high performance, Si-$Si_{1-x}Ge_x$ heterojunction bipolar transistors," *IEEE Electron Device Letter*, vol. 10, no. 11, p. 503, 1989.

[10] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, G. J. Scilla, E. de Fresart, J. M. Stork, J. Y.-C. Sun, D. L. Harame, and J. N. Burghartz, "75-GHz f_T SiGe-base heterojunction bipolar transistors," *IEEE Electron Device Letter*, vol. 11, no. 4, p. 171, 1990.

[11] A. Gruhle, H. Kibbel, U. Konig, U. Erben, and E. Kasper, "MBE-grown Si/SiGe HBT's with high β, f_T, and f_{max}," *IEEE Electron Device Letter*, vol. 13, no. 4, p. 206, 1992.

[12] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors, part I: materials, physics, and circuits," *IEEE Trans. Electron Devices*, vol. 42, no. 3, p. 455, 1995.

[13] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors, part II: Process integration, and analog applications," *IEEE Trans. Electron Devices*, vol. 42, no. 3, p. 469, 1995.

[14] S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, and D. L. Harame, "Heterojunction bipolar transistors using Si-Ge alloys," *IEEE Trans. Electron Devices*, vol. 36, no. 10, p. 2043, 1989.

[15] E. F. Crabbe, B. Meyerson, J. M. C. Stork, and D. L. Harame, "Vertical profile optimization of very high frequency epitaxial Si- and SiGe-base bipolar transistors," *IEEE IEDM Tech. Dig.*, p. 83, 1993.

[16] A. Schuppen, A. Gruhle, H. Kibbel, U. Erben, and U. Konig, "SiGe-HBTs with high f_T at moderate current densities," *Electronics Letter*, vol. 30, no. 14, p. 1187, 1994.

[17] A. Schuppen, A. Gruhle, U. Erben, H. Kibbel, and U. Konig, "Multi emitter finger SiGe-HBTs with f_{max} up to 120 GHz," *IEEE IEDM Tech. Dig.*, p. 377, 1994.

[18] H. Schumacher, U. Erben, and A. Gruhle, "Low-noise performance of SiGe heterojunction bipolar transistors," *IEEE MTT-Symp. Digest*, p. 1167, 1994.

[19] E. J. Prinz and J. C. Sturm, "Current gain - early voltage products in heterojunction bipolar transistors with nonuniform base bandgaps," *IEEE Electron Device Letter*, vol. 12, p. 661, 1991.

[20] F. Sato, T. Hashimoto, T. Tatsumi, H. Kitahata, and T. Tashiro, "Sub-20psec ECL circuits with 50GHz f_{max} self-aligned SiGe HBTs," *IEEE IEDM Tech. Dig.*, p. 397, 1992.

[21] D. L. Harame, J. M. C. Stork, B. S. Meyerson, K. Hsu, J. Cote, K. A. Jenkins, J. D. Cressler, P. Restle, E. F. Crabbe, S. Subbanna, T. Tice, B. W. Scharf, and J. A. Yasaitis, "Optimization of SiGe HBT technology for high speed analog and mixed-signal applications," *IEEE IEDM Tech. Dig.*, p. 71, 1993.

[22] D. L. Harame, K. Schonenberg, M. Gilbert, D. Nguyen-Ngoc, J. Malinowski, S.-J. Jeng, B. S.Meyerson, J. D. Cressler, R. Groves, G. Berg, K. Tallman, K. Stein, G. Hueckel, C. Kermarrec, T. Tice, G. Fitzgibbons, K. Walter, D. Colavito, T. Houghton, N. Greco, T. Kebede, B. Cunningham, S. Subbanna, J. H. Comfort, and E. F. Crabbe, "A 200mm SiGe-HBT technology for wireless and mixed-signal applications," *IEEE IEDM Tech. Dig.*, p. 437, 1994.

[23] J. D. Cressler, D. L. Harame, J. H. Comfort, J. M. C. Stork, B. S. Meyerson, and T. E. Tice, "Silicon-germanium heterojunction bipolar technology: the next leap in silicon?," *IEEE/ISSCC*, p. 24, 1994.

[24] K. Imai, T. Yamazaki, T. Tashiro, T. Tatsumi, N. Aizaki, and M. Nakamae, "A cryo-BiCMOS technology with Si/SiGe heterojunction bipolar transistors," *IEEE Bipolar Circuits and Technology Meeting*, p. 90, 1990.

[25] T. Yamazaki, K. Imai, T.Tashiro, T. Tatsumi, T. Niino, and M. Nakamae, "A Si/SiGe heterojunction bipolar transistors with undoped SiGe spacer for cryo-BiCMOS circuits," *IEEE IEDM Tech. Dig.*, p. 379, 1990.

[26] J. D. Cressler, J. H. Comfort, E. F. Crabbe, G. L. Patton, J. M. C. Stork, J. Y.-C. Sun, and B. S. Meyerson, "On the profile design and optimization of epitaxial Si- and SiGe-base bipolar technology for 77K applications — part I: transistor DC design considerations," *IEEE Trans. Electron Devices*, vol. 40, no. 3, p. 525, 1993.

[27] J. D. Cressler, E. F. Crabbe, J. H. Comfort, J. M. C. Stork, and J. Y.-C. Sun, "On the profile design and optimization of epitaxial Si- and SiGe-base bipolar technology for 77K applications — part II: circuit performance issues," *IEEE Trans. Electron Devices*, vol. 40, no. 3, p. 542, 1993.

[28] C. Kermerrec, G. Dawe, T. Tewksbury, B. S. Meyerson, D. L. Harame, and M. Gilbert, "SiGe HBTs reach the microwave and millimeter-wave frontier," *IEEE Bipolar Circuits and Technology Meeting*, p. 155, 1994.

[29] H. Kroemer, "Theory of a wide-gap emitter for transistors," *Proc. IRE*, vol. 45, p. 1535, 1957.

[30] H. Kroemer, "Quasi-electric and quasi-magnetic fields in nonuniform semiconductors," *RCA Review*, vol. 45, p. 1535, 1957.

[31] H. Kroemer, "Heterostructure bipolar transistors and integrated circuits," *Proc. IEEE*, vol. 70, p. 13, 1982.

[32] H. Kroemer, "Heterostructure bipolar transistors : what should we build?," *J. of Vac. Sci. Technology*, vol. B1, p. 126, 1983.

[33] H. D. Barber, "Bipolar device technology challenge and opportunity," *Canadian J. Physics*, vol. 63, p. 683, 1985.

[34] T. H. Ning and D. D. Tang, "Bipolar trends," *Proc. IEEE*, vol. 74, p. 1669, 1986.

[35] J. D. Warnock, "Silicon bipolar device structures for digital applications: technology trends and future directions," *IEEE Trans. Electron Devices*, vol. 42, no. 3, p. 377, 1995.

[36] S. P. Gaur, "Performance limitations of silicon bipolar transistors," *IEEE Trans. Electron Devices*, vol. 26, no. 4, p. 415, 1979.

[37] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained-layer heterostructures," *IEEE J. of Quantum Electronics*, vol. 22, no. 9, p. 1696, 1986.

[38] J. W. Matthews and A. Blakeslee, "Defects in epitaxial multilayers:I. misfit dislocations," *J. Crystal Growth*, vol. 27, p. 118, 1974.

[39] M. L. Green, B. E. Weir, D. Brasen, Y. F. Hsieh, G. Higashi, A. Feygenson, L. C. Feldman, and R. L. Headrick, "Mechanically and thermally stable Si-Ge heterojunction bipolar transistors grown by rapid thermal chemical vapor deposition at 900°C," *J. of Applied Physics*, vol. 69, no. 2, p. 745, 1991.

[40] S.-M. Jang, C. Tsai, and R. Reif, "Growth of epitaxial $Si_{1-x}Ge_x$ layers at 750°C by VLPCVD," *J. Electronic Materials*, vol. 20, no. 1, p. 91, 1991.

[41] J. C. Sturm, P. V. Schwartz, E. J. Prinz, and H. Manoharan, "Growth of $Si_{1-x}Ge_x$ by rapid thermal chemical vapor deposition and application to heterojunction bipolar transistors," *J. of Vac. Sci. Technology*, vol. B9, p. 2011, 1991.

[42] S. M. Sze, *Physics of Semiconductor Devices.* John Wiley & Sons, second ed., 1981.

[43] N. W. Ashcroft and N. D. Mermin, *Solid State Physics.* Holt, Reinhart and Winston, 1976.

[44] K. Hess, *Advanced Theory of Semiconductor Devices.* Prentice Hall, 1988.

[45] R. Braunstein, A. R. Moore, and F. Herman, "Intrinsic optical absorption in germanium-silicon alloys," *Phy. Rev.*, vol. 109, no. 3, p. 695, 1958.

[46] R. People, "Indirect bandgap of coherently strained Ge_xSi_{1-x} bulk alloys on (100) silicon substrate," *Phy. Rev. B.*, vol. 32, no. 2, p. 1405, 1985.

[47] D. Lang, R. People, J. C. Bean, and A. Sergent, "Measurement of the bandgap of Ge_xSi_{1-x}/Si strained-layer heterostructures," *Applied Physics Letter*, vol. 47, no. 12, p. 1333, 1985.

[48] C. Smith and A. D. Welbourn, "Prospects for a hetero-structure bipolar transistor using a silicon-germanium alloy," *IEEE Bipolar Circuits and Technology Meeting*, p. 57, 1987.

[49] R. L. Anderson, "Experiments on Ge-GaAs heterojunctions," *Solid-State Electronics*, vol. 5, p. 341, 1962.

[50] W. R. Frensley and H. Kroemer, "Theory of the energy-band lineup at an abrupt semiconductor heterojunction," *Phy. Rev. B.*, vol. 16, p. 2642, 1977.

[51] R. M. Warner Jr. and B. L. Grung, *Transistors: Fundamentals for the Integrated-Circuit engineer.* John Wiley & Sons, 1983.

[52] P. Ashburn, *Design and Realization of Bipolar Transistors.* John Wiley & Sons, 1988.

[53] D. J. Roulston, *Bipolar Semiconductor Devices.* McGraw-Hill Inc., 1990.

[54] P. M. Asbeck, "Heterojunction bipolar transistors : status and directions," *IEEE Bipolar Circuits and Technology Meeting*, p. 65, 1989.

[55] J. L. Moll and I. M. Ross, "The dependence of transistor parameters on the distribution of base layer resistivity," *Proc. IRE*, vol. 44, p. 72, 1956.

[56] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," *Solid-State Electronics*, vol. 28, no. 11, p. 1101, 1985.

[57] P. K. Tedrow and C. G. Sodini, *Twin Well CMOS Process*, 1.2 ed., 1989.

[58] C. Kermarrec, G. Dawe, T. Teewksbury, B. Meyerson, D. Harame, and M. Gilbert, "SiGe technology: application to wireless digital communications," *IEEE Microwave and Millimeter-wave Monolithic Cir. Symp.*, p. 1, 1994.

[59] B. Bayraktaroglu, "GaAs HBT's for microwave integrated circuits," *Proc. IEEE*, vol. 81, no. 12, p. 1762, 1993.

[60] B. K. Oyama and B. P. Wong, "GaAs HBT's for analog circuits," *Proc. IEEE*, vol. 81, no. 12, p. 1744, 1993.

[61] P. M. Asbeck, M. F. Chang, K. C. Wang, D. L. Miller, G. J. Sullivan, N. H. Sheng, E. Sovero, and J. A. Higgins, "Heterojunction bipolar transistors for microwave and millimeter-wave integrated circuits," *IEEE Trans. Electron Devices*, vol. 34, no. 12, p. 2571, 1987.

[62] A. Van der Ziel, *Noise in Solid State Devices and Circuits.* John Wiley, 1986.

[63] J. M. C. Stork, G. L. Patton, E. F. Crabbe, D. L. Harame, and B. S. Meyerson, "Design issues for SiGe heterojunction bipolar transistors," *IEEE Bipolar Circuits and Technology Meeting*, p. 57, 1989.

[64] S.-Y. Chiang, D. Pettengill, and P. V. Voorde, "Bipolar device design for circuit performance optimization," *IEEE Bipolar Circuits and Technology Meeting*, p. 172, 1990.

[65] E. F. Chor, A. Brunnschweiler, and P. Ashburn, "A propagation delay expression and its application to the optimization of polysilicon emitter ECL processes," *J. of Solid-State Circuits*, vol. 23, p. 251, 1988.

[66] K. Horio, Y. Iwatsu, A. Oguchi, and H. Yanai, "Study on collector design of AlGaAs/GaAs heterojunction bipolar transistors by two-dimensional simulation," *IEEE Bipolar Circuits and Technology Meeting*, p. 195, 1990.

[67] G. B. Gao, M. S. Unlu, J. Chen, B. Mazhari, K. Adomi, X. Liu, F. Fan, and H. Morkoc, "Double-layer collector for heterojunction bipolar transistors," *Solid-State Electronics*, vol. 35, no. 1, p. 57, 1992.

[68] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Review*, vol. 26, p. 163, 1965.

[69] C. T. Kirk Jr., "A theory of transistor cutoff frequency (f_T) falloff at high current densities," *IRE Tran. on Electron Devices*, vol. 9, p. 164, 1962.

[70] C. Tsai, *Deposition and characterization of very low pressure CVD silicon/silicon-germanium heteroepitaxial structures.* PhD thesis, Massachusetts Institute of Technology, 1992.

[71] S.-M. Jang, *Growth, characterization and thermal stability of undoped and in-situ doped silicon-germanium heteroepitaxial layers.* PhD thesis, Massachusetts Institute of Technology, 1993.

[72] K. K. O, *BiCMOS technologies for analog/digital applications utilizing selective silicon epitaxial growth.* PhD thesis, Massachusetts Institute of Technology, 1990.

[73] J. J. Lutsky, "Design fabrication and testing of a high slew rate BiCMOS Opmp," Master's thesis, Massachusetts Institute of Technology, 1992.

[74] D. J. Meyer and T. I. Kamins, "Atmospheric pressure CVD used for Si-Ge," *Semiconductor International*, p. 95, May 1992.

[75] J. H. Comfort, L. M. Gaverick, and R. Reif, "Silicon surface cleaning by low dose argon ion bombardment for low-temperature (750°C) epitaxial silicon deposition. I. process considerations," *J. of Applied Physics*, vol. 62, no. 8, p. 3388, 1987.

[76] J. H. Comfort, *Plasma enhanced chemical vapor deposition of in-situ doped epitaxial silicon from silane at low temperatures.* PhD thesis, Massachusetts Institute of Technology, 1988.

[77] T.-R. Yew, *Growth and characterization of low temperature silicon selective epitaxy.* PhD thesis, Massachusetts Institute of Technology, 1990.

[78] N. Nakano, L. Marville, S.-M. Jang, K. Liao, C. Tsai, J. A. Tsai, H.-W. Kim, and R. Reif, "Effect of thermal annealing on the Raman spectrum of $Si_{1-x}Ge_x$ grown on Si," *J. of Applied Physics*, vol. 73, p. 414, 1993.

[79] S.-M. Jang, H.-W. Kim, and R. Reif, "Thermal stability of $Si/Si_{1-x}Ge_x/Si$ heterostructures deposited by very low pressure chemical vapor deposition," *Applied Physics Letter*, vol. 61, p. 315, 1992.

[80] I. E. Getreu, *Modeling the Bipolar Transistor.* Elsevier Scientific Publishing, 1978.

[81] C. A. King, J. L. Hoyt, and J. F. Gibbons, "Bandgap and transport properties of $Si_{1-x}Ge_x$ by analysis of nearly ideal $si/Si_{1-x}Ge_x/si$ heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 10, p. 2093, 1989.

[82] A. Pruijmboom, J. W. Slotboom, D. J. Gravesteijn, W. Fredriksz, A. A. van Gorkum, R. A. L. van de Heuvel, J. M. van Rooij-Mulder, G. Streutker, and G. F. A. van de Walle, "Heterojunction bipolar transistors with SiGe base grown by molecular beam epitaxy," *IEEE Electron Device Letter*, vol. 12, no. 7, p. 357, 1991.

[83] Q. M. Zhang, G.-L. Tan, W. T. Moore, and J. M. Xu, "Effects of displaced p-n junction of heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 39, no. 11, p. 2430, 1992.

[84] H. U. Schreiber and J. N. Albers, "DC characteristics and stability behavior of high-speed Si/SiGe HBTs undoped SiGe spacer between base and collector," *Electronics Letters*, vol. 28, p. 1187, 1992.

[85] K. Liao, R. Reif, and T. I. Kamins, "Effect of current and voltage stress on the DC characteristics of SiGe-base heterojunction bipolar transistors," *IEEE Bipolar Circuits and Technology Meeting*, p. 209, 1994.

[86] T. C. Chen, C. Kaya, M. B. Ketchen, and T. H. Ning, "Reliability analysis of self-aligned bipolar transistor under forward active current stress," *IEEE IEDM Tech. Dig.*, p. 650, 1986.

[87] R. A. Wachnik, T. J. Bucelot, and G. P. Li, "Degradation of bipolar transistors under high current stress at 300K," *J. of Applied Physics*, vol. 63, no. 9, p. 4734, 1988.

[88] D. D. Tang, E. Hackbarth, and T.-C. Chen, "On the very-high-current degradation on Si n-p-n transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 7, p. 1698, 1990.

[89] S. P. Joshi, R. Lahri, and C. Lage, "Poly emitter bipolar hot carrier effects in an advanced BiCMOS technology," *IEEE IEDM Tech. Dig.*, p. 182, 1987.

[90] D. D. Tang and E. Hackbarth, "Junction degradation in bipolar transistors and the reliability imposed constraints to scaling and design," *IEEE Trans. Electron Devices*, vol. 35, no. 12, p. 2101, 1988.

[91] J. D. Burnett and C. Hu, "Modeling hot-carrier effects in polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 35, no. 12, p. 2238, 1988.

[92] D. Burnett and C. Hu, "Hot-carrier reliability of bipolar transistors," *IEEE/IRPS*, p. 164, 1990.

[93] Y. Niitsu, K. Yamamura, H. Momose, and K. Maeguchi, "Anomalous current gain degradation in bipolar transistors," *IEEE/IRPS*, p. 193, 1991.

[94] W. P. Dumke, "The effect of base doping on the performance of si bipolar transistors at low temperatures," *IEEE Trans. Electron Devices*, vol. 28, p. 494, 1981.

[95] M. M. Rahman and S. Furukawa, "Silicon carbide turns on its power," *IEEE Circuits and Devices*, vol. 8, p. 22, 1992.

[96] K. Ismail, B. S. Meyerson, S. Rishton, J. O. Chu, S. Nelson, and J. Nocera, "High-transconductance n-type Si/SiGe modulation-doped field-effect transistors," *IEEE Electron Device Letter*, vol. 13, no. 5, p. 229, 1992.

[97] K. Ismail, S. Rishton, J. O. Chu, , K. Chan, and B. S. Meyerson, "High-performance Si/SiGe n-type modulation-doped transistors," *IEEE Electron Device Letter*, vol. 14, no. 7, p. 348, 1993.

[98] M. S. Mock, "Transport equations in heavily doped silicon, and the current gain of a bipolar transistor," *Solid-State Electronics*, vol. 16, p. 1251, 1973.

[99] R. J. Van Overstraeten, H. J. DeMan, and R. P. Mertens, "Transport equations in heavily doped silicon," *IEEE Trans. Electron Devices*, vol. 20, no. 3, p. 290, 1973.

[100] R. P. Mertens, H. J. DeMan, and R. J. Van Overstraeten, "Calculation of the emitter efficiency of bipolar transistors," *IEEE Trans. Electron Devices*, vol. 20, no. 9, p. 772, 1973.

[101] A. H. Marshak, "Transport equations for highly doped devices and heterostructures," *Solid-State Electronics*, vol. 30, no. 11, p. 1089, 1987.

[102] A. H. Marshak, "Modeling semiconductor devices with position-dependent material parameters," *IEEE Trans. Electron Devices*, vol. 36, no. 9, p. 1764, 1989.

[103] A. H. Marshak and K. M. van Vliet, "Electrical current in solids with position-dependent band structure," *Solid-State Electronics*, vol. 21, p. 417, 1978.

[104] A. H. Marshak and K. M. van Vliet, "Carrier densities and emitter efficiency in degenerate materials with position-dependent band structure," *Solid-State Electronics*, vol. 21, p. 429, 1978.

[105] A. H. Marshak and C. M. van Vliet, "Electrical current and carrier density in degenerate materials with nonuniform band structure," *Proc. IEEE*, vol. 72, no. 2, p. 148, 1984.

[106] G. Burns, *Solid State Physics.* Academic Press, 1985.