Reliability and 1/f Noise Properties of MOSFETs With Nitrided Oxide Gate Dielectrics

by

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Abstract

This thesis is broadly concerned with the electrical properties of MOS devices with thin (12 nm) nitrided oxide and reoxidized nitrided oxide gate dielectrics and specifically with the reliability and 1/f noise properties of MOSFETs with such dielectrics. Nitrided oxides are formed by low pressure annealing of thermal silicon dioxide films in ammonia and reoxidized nitrided oxides are formed by low pressure annealing of nitrided oxides in oxygen. The annealing is accomplished at 950 °C in a custom-built low pressure furnace system operating at a pressure of 0.1 or 0.01 atmospheres for anneal times ranging from 15 minutes to 10 hours.

Previous researchers have shown that sufficiently heavy nitridations of silicon dioxide provide resistance to interface state generation under electrical stress, insensitivity to ionizing radiation, and a barrier to various dopants and contaminants. However, the nitridation process, which is typically performed at atmospheric pressure and at high temperatures ($\geq$ 1000 °C), is known to introduce a large number of electron traps and a high fixed charge density. The process of reoxidation has also been shown to be somewhat effective in reducing nitridation-induced electron traps. Thus, reoxidized nitrided oxides show promise as reliable dielectrics but suffer from high fixed charge which reduces the inversion layer mobility of devices.

In this thesis, we demonstrate that light, low pressure nitridations coupled with reoxidations can be used to reduce fixed charge and trap densities to levels approaching those of silicon dioxide, while maintaining better reliability under electrical stress as well as under ionizing radiation.

A capacitor study indicates that a reoxidized nitrided oxide process reduces interface state generation under high-field stress by more than a factor of 25 compared to silicon dioxide. While the process of nitridation and reoxidation degrades the pre-stress interfacial characteristics of oxide, we are able to achieve fixed charge densities as low as $\sim$ 2-3 $\times$ 10^{11} cm^{-2} and midgap interface state densities as low as $\sim$ 3 $\times$ 10^{10} cm^{-2} eV^{-1}, while maintaining the improvement in reliability.

A transistor study indicates that a low pressure reoxidized nitrided oxide process results in devices with a projected operating life that is one order of magnitude larger than for silicon dioxide devices. We achieve this with only a ~20% degradation in the electron and hole inversion layer mobilities.

Since nitridation introduces oxide traps near the band edges of Si, this thesis also investigates the use of 1/f noise measurements as means of characterizing these traps. Two extensions of the basic number fluctuation model, which attributes noise to tunneling of channel electrons to and from interfacial oxide traps, are considered. In the first case, the effect of a nonuniform oxide trap distribution in space and energy is analyzed. It is theoretically shown that a nonuniform distribution of oxide traps can give rise to a gate voltage dependence in the magnitude and exponent, γ, of the $1/f^{\gamma}$ spectrum.

In the second case, an extension of the 1/f noise theory based on the McWhorter tunneling number fluctuation model is considered which includes both number fluctuations and correlated mobility fluctuations. Both the number and mobility fluctuations arise from the same physical mechanism involving electronic tunneling transitions between interfacial oxide traps and the MOSFET channel. The trapped electrons result in coulombic scattering of channel carriers causing mobility fluctuations. The model includes the dependence of coulombic scattering on the distance of the trapped charge from the interface and considers the consequence of such a scattering dependence on the shape of the 1/f noise spectrum. It is shown that the correlated model also predicts a gate voltage dependence in the magnitude and exponent of $1/f^{\gamma}$ noise even for the case of uniform trap distributions.

Both the above noise models are then used to analyze 1/f noise data on oxide devices to extract the oxide trap density and distribution in space and energy.

The number fluctuation model is also applied to characterizing the effect of ammonia and oxygen annealing of the gate oxide on the 1/f noise properties of n- and p-channel MOSFETs. It is shown that nitridation increases the interfacial electron trap density in the oxide near the conduction band of silicon by a factor of 2-10 over control oxide devices. Reoxidation is shown to decrease the nitridation-induced interfacial electron trap density under certain conditions.

Analysis of p-channel results indicate that the nitridation process increases the hole trap density near the valence band of Si by a factor of 2-6 over control oxide devices. Hole traps due to nitridation have not been previously observed. Reoxidation is shown to reduce the nitridation-induced interfacial hole trap density to values approaching those found in oxide.

Thesis Supervisor: Professor Charles. G. Sodini

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Chapter 1

Introduction

1.1 Limitations of thermal silicon dioxide

Thermally grown silicon dioxide on silicon forms a nearly perfect insulator-semiconductor system with an atomically smooth and abrupt interface with few dangling bonds. Approximately 30 years of development have lead to low interface states densities($\leq 10^{10}$ cm^{-2} eV^{-1}), low fixed charge density ($\leq 5 \times 10^{10}$ cm^{-2}), and high dielectric breakdown strengths (10 - 12 MV/cm). The kinetics of the oxidation process are well-understood and modelled by the Deal and Grove theory making it possible to reproducibly grow oxides with uniform thickness. Silicon dioxide also has a large effective bandgap of approximately 9 eV that creates a 3.2 eV barrier to electrons and a 4.7 eV barrier to holes from the silicon conduction and valence bands, respectively. The large bandgap yields MOS devices with a large input resistance. These properties have facilitated the manufacture of high performance MOS transistors with high transconductance, good reproducibility and stability [1,2,3].

Silicon dioxide, however, is not without limitations. To achieve greater functionality and performance in integrated circuits, device channel lengths, oxide thickness, and junction depths have continued to be scaled down without a proportional decrease in power supply voltages. This has resulted in larger electric fields within

devices leading to a greater susceptibility to hot carriers, particularly in n-channel devices [4]. Hot electrons can lead to charge trapping and interface state generation in silicon dioxide and is one of the criteria that determines the overall operating life of an MOS device. Hot electron issues have received considerable attention in recent years [5,6]. One popular solution is the use of the lightly doped drain (LDD) region which reduces the maximum electric field in the device [7,8]. An alternative solution, addressed in this thesis, is the use of a gate dielectric with greater resistance to hot-electron effects.

Other concerns have been raised regarding the dopant barrier properties of thin silicon dioxide films. For example, 10nm SiO_2 films are known to be a poor barrier to the diffusion of dopants and contaminants [9,10]. Further concerns center around the increasing use of plasma processes in the manufacture of integrated circuits, which expose the wafer to ionizing radiation and the overall integrity of thin silicon dioxide films with respect to dielectric strength, defect density, and yield [11].

1.2 Nitrided silicon dioxide as an alternative

Nitrided silicon dioxide is formed by first thermally growing an SiO_2 film and subsequently annealing the film in an ammonia ambient. The process was first introduced by Ito and Naiman [12,13]. The resulting dielectric is referred to as nitrided oxide, nitroxide, nitrized oxide, or oxynitride. Here we will use the term nitrided oxide. The term oxynitride has typically referred to both deposited as well as thermally grown films. The nitridation process has been shown by several authors to result in the incorporation of nitrogen and hydrogen into the dielectric, radically changing its electrical properties. Under certain nitridation conditions, the process results in reduced interface state generation under high-field stress [14] and under ionizing radiation [15,16,17]. In addition, the process provides a diffusion barrier to various dopants and contaminants [9,10]. These advantageous properties

have spurred research in nitrided oxides as a thin reliable gate dielectric [18,19,20], as a radiation hard dielectric [15,16,17,21,22], as tunnel dielectric for non-volatile memories [14,23,24], as a local oxidation mask [25], as a dielectric waveguide [26], and as a dielectric system for the study of impurity diffusion in silicon [27,28,29].

The nitridation of silicon dioxide, however, has several side effects that has limited its usefulness in MOS devices. The nitridation process is known to greatly increase the density of electron traps [30,31,32], the fixed positive charge density [21,33,34,96], and the density of interface states [33,34]. The fixed charge and interface state density have been shown to increase with increasing nitridation, peak, and subsequently decrease [35,36]. Typical behavior is shown in figure 1.1. This turnaround behavior in fixed charge and interface state density motivated previous researchers to use high temperatures and/or lengthy nitridation cycles to achieve low fixed charge and interface state density. However, even in the post-turnaround regime, the electron trap density remains large.

The fixed positive charge, high electron trap density and large interface state density are detrimental to device stability and inversion layer mobilities [19,38]. The electron traps in nitrided oxides are also responsible for increased flicker noise measured in MOS transistors [39].

The reoxidation (oxygen anneal) of a nitrided oxide film results in a film referred to as reoxidized nitrided oxide with the terms ONO or ROXNOX being used as abbreviations. Previous authors have reported a dramatic reduction in electron trap density by the process of reoxidation [14,37,40]. However, fixed charge and interface state density do not appear to be significantly reduced by reoxidation. Thus the application of the nitridation/reoxidation process to scaled devices is limited by the lower inversion layer mobilities available in these devices.

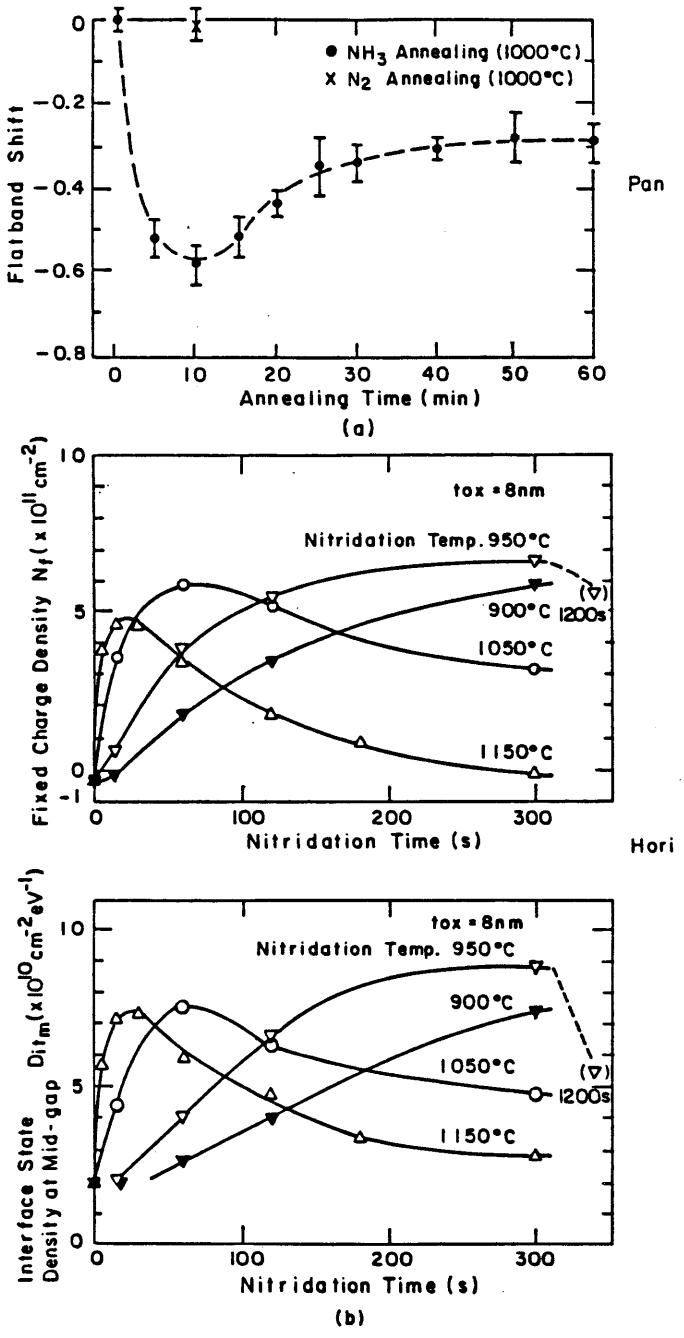

Figure 1.1: Typical fixed charge and interface state density behavior as a function of nitridation conditions as reported in the literature [35,36].

1.3 Why low pressure nitridation?

There is a need to develop a nitridation technique which results in greater reliability without compromising the low fixed charge and interface state density found in oxide. Of the various techniques explored - atmospheric pressure [13,21,33,35,41,42], dilute [17], low pressure [10], high pressure [43], rapid thermal [36,44,45,46,47], nitrogen implantation [48,49], and plasma nitridation [50,51] - we have favored the low pressure technique. The initial motivation to pursue the low pressure process was simply to reduce the fixed charge, interface state density, and electron trapping while attempting to preserve the property of improved resistance to hot carriers. In the course of our experimentation, the low pressure process was found to differ from the atmospheric nitridation technique in two important respects. First, the fixed charge and interface state density increased, peaked, and decreased with increasing nitridation similar to atmospheric nitridation but in a more gradual fashion. This suggested a sufficient process window in the early stages of the nitridation process (pre-turnaround regime) to optimize the dielectric's electrical properties. Second, low pressure nitrided oxides typically did not exhibit a suppression of interface state generation under electrical stress unless a lengthy nitridation was performed. However, when coupled with a reoxidation, short nitridations dramatically suppressed interface state generation. Moreover, reoxidation eliminated electron trapping as expected from previous work. These differences allowed the use of the pre-turnaround regime in order to optimize the electrical properties of the dielectric.

A further motivation for low pressure nitridation was better process control. The use of a low pressure furnace allowed the rapid and complete switching of gas ambients facilitating the control of the 3-step process needed to form reoxidized nitrided oxides. As shown in section 4.5, a dilute process with equivalent ammonia partial pressure yielded erratic results which we attributed to residual oxygen.

1.4 Summary of results

The objective of this work was to develop a thin gate dielectric for scaled MOS devices with improved reliability over silicon dioxide devices. Improved reliability is sought without compromising the performance available in oxide devices. A second objective was to develop a 1/f noise technique to study interfacial oxide traps near the conduction and valence bands of Si, regions inaccessible to conventional capacitance–voltage techniques [52].

The primary findings of this thesis can be broadly divided into two parts, relating to the reliability of nitrided oxide MOS devices and to the 1/f noise properties of nitrided oxide transistors.

(1) A low pressure nitridation/reoxidation process for the formation of thin (12 nm) and reliable gate dielectrics was developed. A capacitor study indicated that dielectrics with dramatically reduced interface state generation and electron trapping could be formed with fixed charge and interface state density approaching oxide values. When applied to scaled MOSFETs the process exhibited dramatically reduced transconductance degradation under channel hot-electron stressing compared to MOSFETs with thermal oxide as a gate dielectric. The projected operating life of reoxidized nitrided oxide transistors was at least a factor of 10 greater than oxide transistors. This achievement in reliability was partially offset by a 20% degradation in inversion layer mobility.

A related study of ionizing radiation effects in reoxidized nitrided oxides showed reduced interface state generation and reduced positive charge trapping compared to conventional silicon dioxide.

The low pressure process was compared to an Ar-diluted process under conditions of equivalent ammonia and oxygen partial pressure. The low pressure process showed better control due to the ability of the system to rapidly and completely switch between gas ambients. The dilute process suffered from residual oxygen in the system which lead to erratic electrical results.

(2) The use of 1/f noise measurements in extracting the interfacial oxide trap density and distribution was demonstrated. The method involved the application of the McWhorter number fluctuation model, with inclusion of the effects of nonuniform oxide trap distributions (in space and energy) and correlated mobility fluctuations on the 1/f noise spectrum. It was theoretically demonstrated that both nonuniform trap distributions and mobility fluctuations give rise to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ spectrum. Thus by analyzing the 1/f noise data, it was possible to infer the oxide trap density and distribution.

The above noise model was also used to study interfacial oxide traps near the conduction and valence bands of Si due to the effect of nitridation and reoxidation.

1.5 Organization of the thesis

The thesis begins with a discussion of the low pressure nitridation/oxidation system constructed for the formation of gate dielectrics. The gate dielectric processes and the procedures used in the fabrication of poly-gate capacitors and transistors are then described. The measurement techniques are outlined in chapter 3. A brief literature review of the material properties of nitrided oxides is given in the last section of chapter 3 and provides a context in which to understand the electrical properties discussed in subsequent chapters. Our approach to dielectric development was to first investigate a matrix of nitridation/reoxidation conditions in poly–gate MOS capacitors. Selected dielectrics were then incorporated into a transistor process to assess their suitability for scaled MOSFETs. The electrical properties of MOS capacitors are first reported in chapter 4 and the electrical properties of MOS transistors are reported in chapter 5. In chapter 6, a 1/f noise theory based on the McWhorter tunneling model is reviewed. The effect of nonuniform oxide distribution in space and energy is then considered. In addition, the effect of correlated carrier and mobility fluctuations are considered. The extented model is

then applied to extracting the interfacial oxide trap density and distribution near the conduction and valence bands of silicon in oxide, nitrided oxide, and reoxidized nitrided oxide transistors.

Chapter 2

Oxidation/Nitridation System and Processing Techniques

In this chapter, an overview of the low pressure oxidation/nitridation system and associated processing techniques are described. The low pressure oxidation/nitridation system was constructed for the formation of oxide, nitrided oxide, and reoxidized nitrided oxide gate dielectrics studied in this thesis. The details of gate dielectric formation and the integration of the gate dielectric process into a standard polysilicon gate capacitor process and a polysilicon gate NMOS/PMOS process is described.

2.1 Low pressure oxidation/nitridation system

The oxidation/nitridation system is a high temperature, low pressure furnace system located in a class 100 clean room environment dedicated to the thermal growth of thin (12 nm) silicon dioxide films, for *in-situ* nitridation (ammonia anneal) and *in-situ* reoxidation (oxygen anneal). The system was designed after the system of Wong [50]. An overall schematic and photograph of the system are shown in figure 2.1 and figure 2.2. The system resembles a typical low pressure chemical

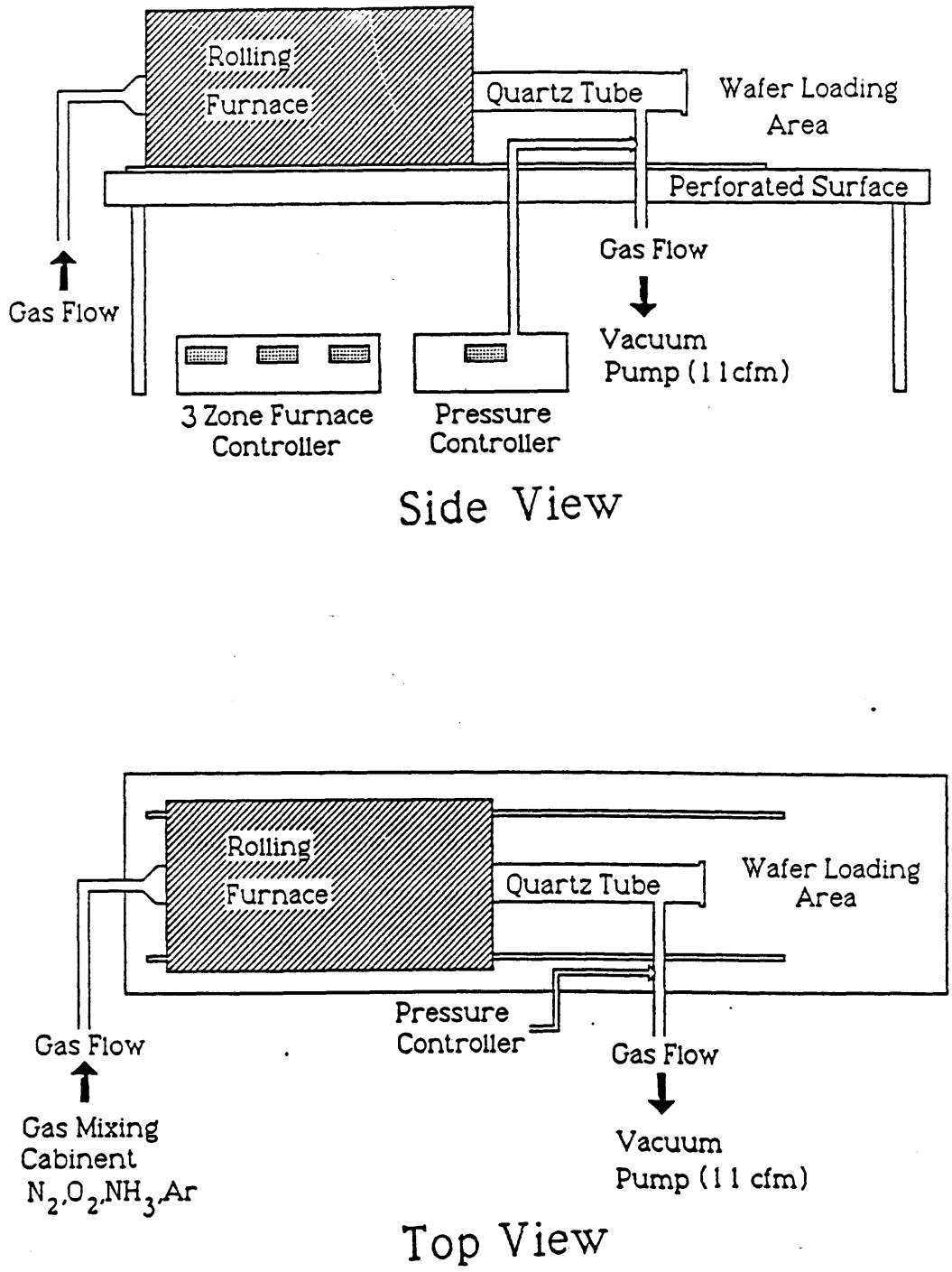

Figure 2.1: Schematic of low pressure oxidation/nitridation system.

Figure 2.2 Photograph of low pressure oxidation/nitridation system.

vapor deposition (LPCVD) system except for two differences. First, typical LPCVD systems are limited in temperature capability by the use of o-ring vacuum seals which cannot withstand temperatures greater than $\sim$ 200 °C. In the present system higher temperatures are made possible by placing the vacuum seals further away from the hot zone through the use of an extra long process tube. A second difference is the use of higher process pressures. LPCVD systems typically operate at less than 1 torr whereas in the oxidation/nitridation system the pressure can be controlled from 1.0 to 100 torr. The higher pressures are possible due to the use of a fine metering valve and an exhaust throttle valve which together control the conductance of the vacuum line and hence the process pressure.

The details of the implementation are discussed below. Conceptually, the system consists of four subsystems:

Gas Handling Subsystem

A schematic of the gas handling subsystem is shown in figure 2.3. The subsystem is based on the design of Brown [53]. The gas handling subsystem is equipped with four gases - dry nitrogen, dry oxygen, dry argon, and anhydrous ammonia. For all experiments, house nitrogen and argon sources were used. Oxygen was used either in bottled form or was obtained from the building source. There was no apparent difference in the quality of the oxides formed with either of these sources. Ammonia was always used in bottled form. The purity of all gases was rated at least 99.999 %. Flow rotameters were used to control the flowrate of gases at typically 1-4 liters/min. $\frac{1}{4}$-inch stainless steel lines and welded fittings with metal gasket seals were used extensively throughout the system.

Furnace Subsystem

The temperature within the quartz tube was maintained via a 3-zone resistively heated tube furnace. The temperature flat zone was typically 6 inches in length allowing a maximum load of 25 2-inch or 4-inch wafers. The temperature was maintained to within $\pm$ 2.5 °C. While the temperature for all experiments reported

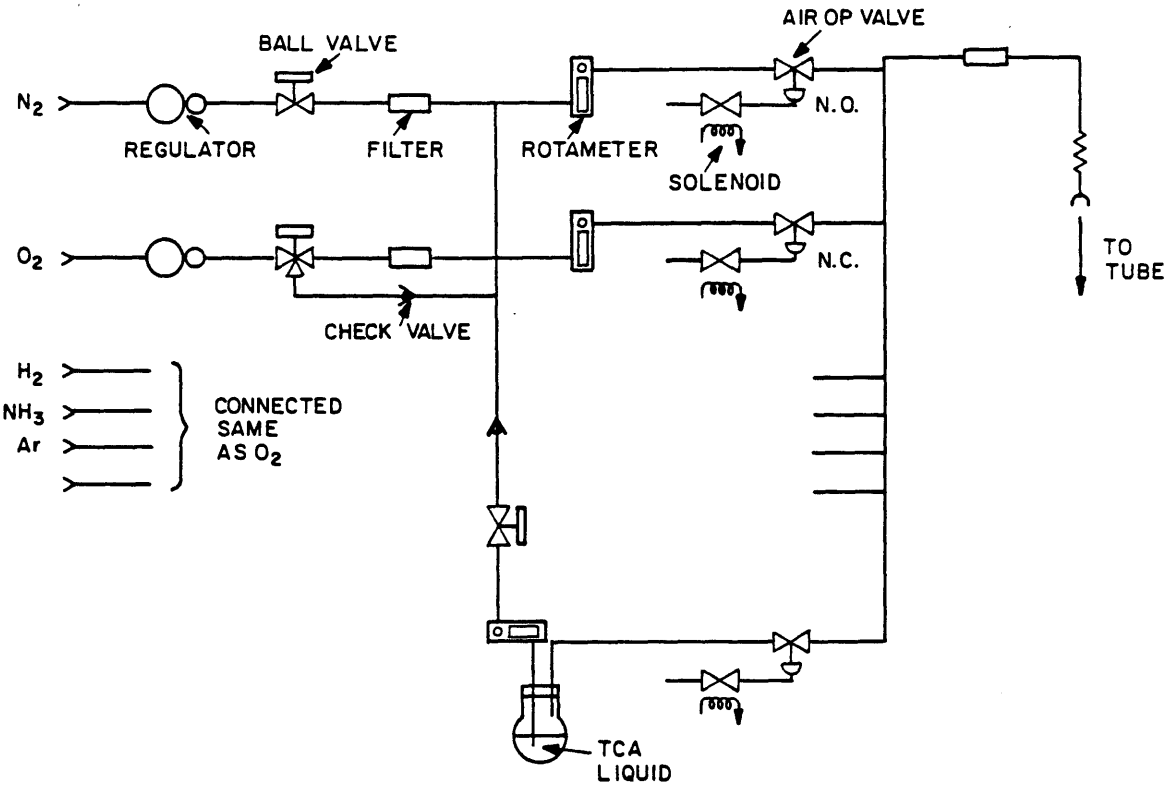

Figure 2.3: Schematic of gas handling subsystem.

here was 950 °C, the upper temperature limit of the furnace system is 1050 °C. The furnace was fitted with a wheel base allowing linear motion along tracks. This facilitated the loading of the wafers into the tube under cool conditions by rolling the furnace hot zone away from the wafers. Following pump down and the establishment of the process ambient, the furnace hot zone was positioned over the wafers under controlled (typically vacuum) conditions.

Vacuum Subsystem

A schematic of the vacuum subsystem is shown in figure 2.4. All seals to the furnace are made with silicone o-rings. The quartz tube is evacuated by a mechanical pump with a pumping speed of $\sim$ 200 l/min. A fine metering valve and an exhaust throttle valve together provide coarse and fine control of the process pressure. The range of controllable pressure is 1 torr to 100 torr. The pressure can be controlled to $\pm$ 0.1 torr. The vacuum subsystem may be disabled allowing the operation of the furnace at atmospheric pressure. During atmospheric operation, the door of the tube is attached to the exhaust stack with a $\frac{3}{8}$-inch teflon line.

Quartz Tube

The quartz tube has a $5\frac{1}{4}$-inch inside diameter and is 8 feet in length yielding a total volume of 34 liters. The tube is fitted with a quartz flange at the loading end allowing a seal to be made with a silicone o-ring which is sandwiched between the aluminum door and the flange. The tube is typically evacuated from atmospheric pressure in under one minute. For usual flow rates of 4 liters/min at atmospheric pressure, the gas residence time is $\sim$ 8 minutes. For typical flow rates of 1 liter/min at 0.1 atmospheres pressure, the gas residence time is 3.4 minutes. The gas inlet is located at the rear of the tube and vacuum lines are attached near loading end of the tube. We used a quartz pushrod to position the wafer boat in the furnace. The tube was cleaned at 6-9 month intervals when yield on the oxide control wafers began to drop. However, no HCl cleaning was performed. Mobile charge content was periodically monitored but in all cases the mobile charge content was $\leq 5 \times 10^{10}$

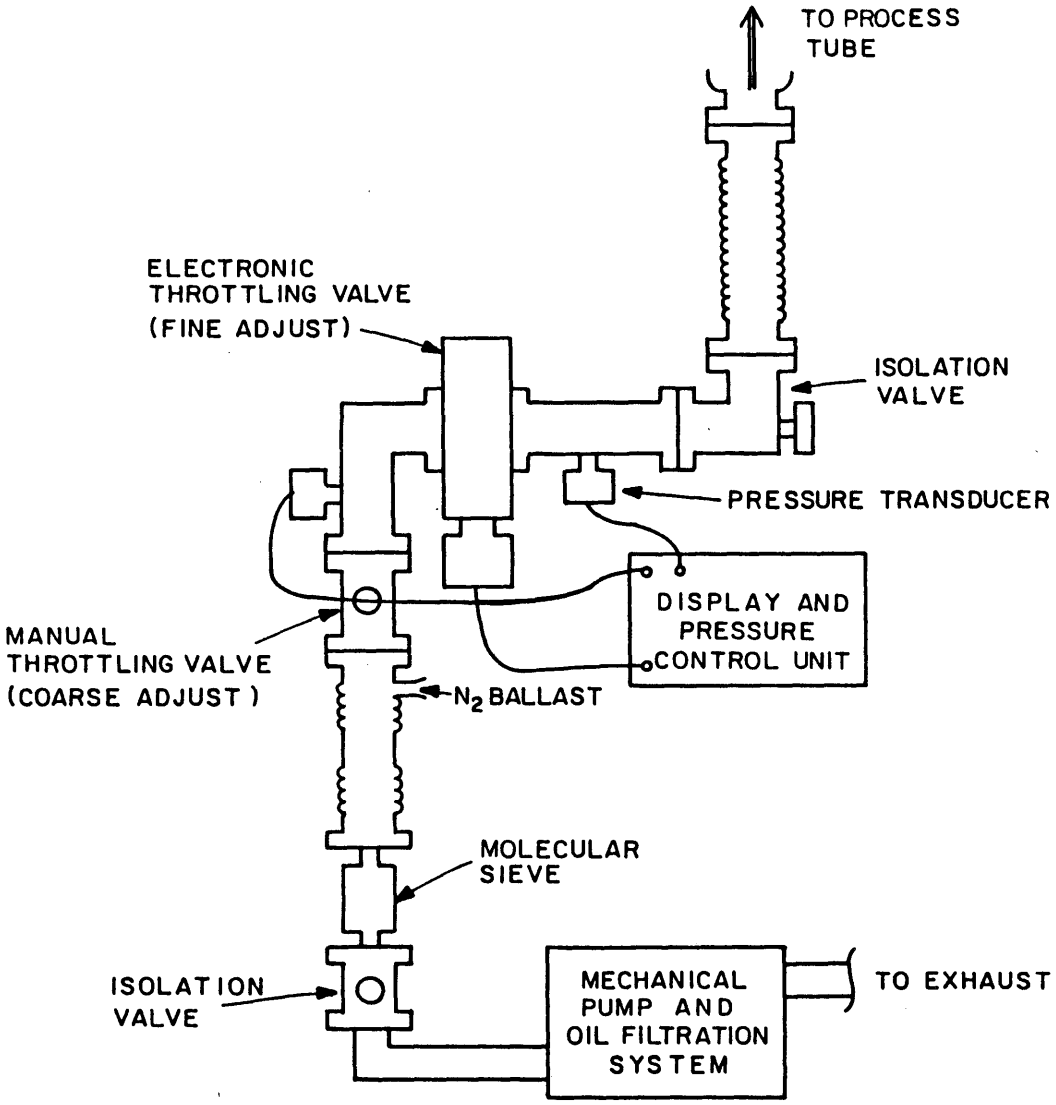

Figure 2.4: Schematic of the vacuum subsystem.

cm^{-2}. The furnace system was restricted to the growth of gate dielectrics on lightly doped substrates. During the idle state the furnace was always left at 0.5 torr nitrogen.

2.2 Low pressure dielectric growth process

A flow diagram of the fabrication process for various gate dielectrics in the low pressure oxidation/nitridation system is outlined in figure 2.5. The processing of various dielectrics begins with wafer cleaning in standard RCA solutions [115]. For the experimental data presented on low pressure dielectrics the wafers were cleaned in an existing 2" facility and then transported to the furnace for dielectric growth. Following the clean, the wafers are loaded into the cool zone ($\sim$ 850 °C) of the furnace and the tube immediately evacuated to 50 mTorr. This takes approximately 1 minute. Following the pump down cycle, the pressure is raised to 0.1 atm. in nitrogen and the furnace is rolled forward so that the wafers are now located in the hot zone (950 °C). Once the pressure is stabilized at 0.1 atm., the system is ready for the growth of gate dielectrics. Three types of gate dielectrics were investigated: control oxides, nitrided oxides, and reoxidized nitrided oxides.

Control oxides are formed by a 40 minute cycle in undiluted oxygen at 0.1 atm. The resulting oxide is $\sim$ 12 nm in thickness. The oxidation kinetics appears to be in the parabolic regime at 0.1 atm. Following the oxidation cycle, the tube is again evacuated to 50 mTorr. The oxide then undergoes a final anneal in 0.1 atm. nitrogen for 30 minutes. Following the anneal, the wafers are removed from the hot zone by rolling the furnace away. The tube is then brought to atmospheric pressure in nitrogen and wafers unloaded at $\sim$ 9 inches/min.

Nitrided oxides are formed by a two-step process. The first step begins with the growth of a 12 nm oxide identical to the way in which the control oxide is formed. Following the oxidation cycle and the pump down, however, the oxide undergoes

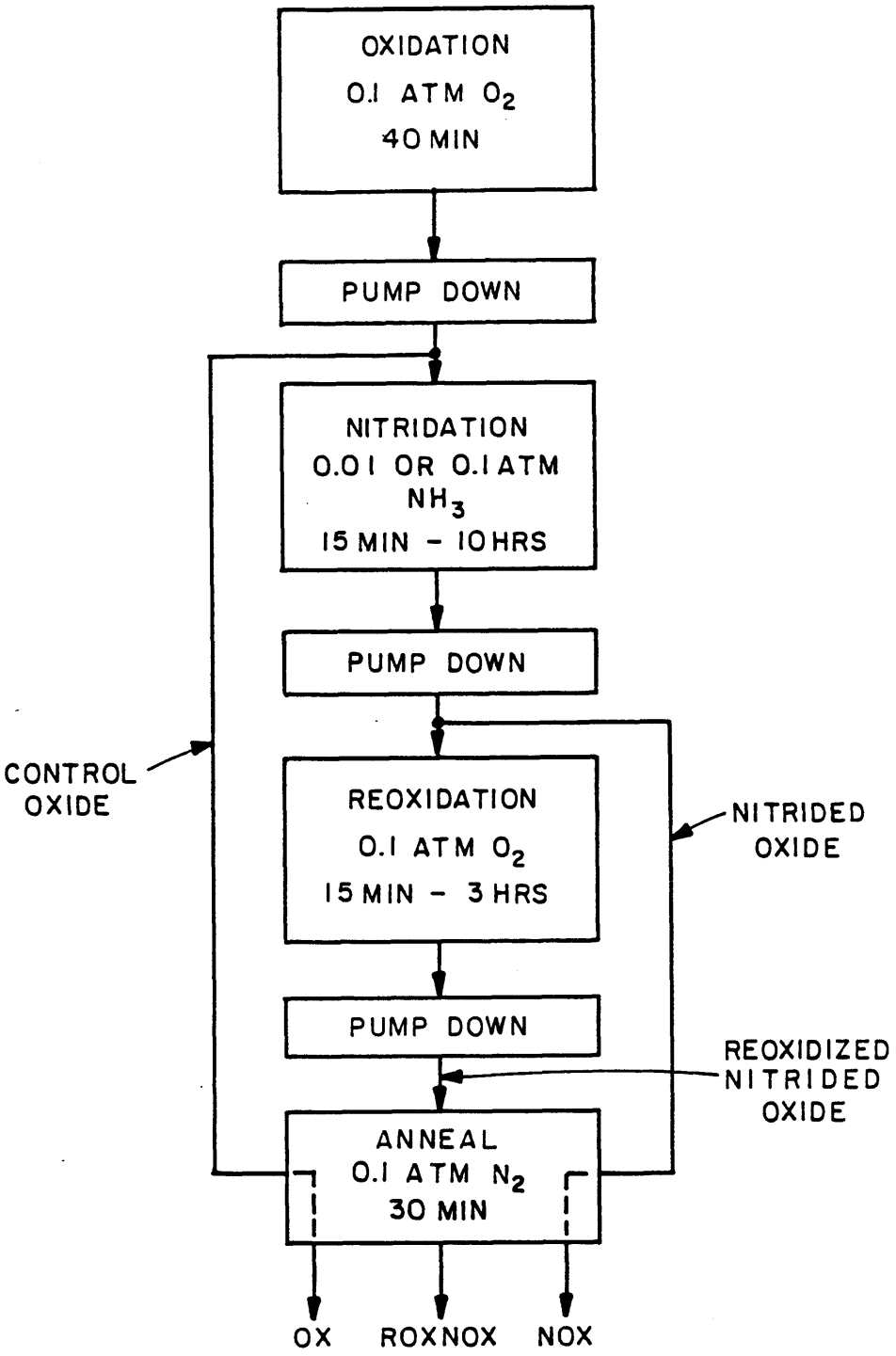

Figure 2.5: Flow diagram of the low pressure dielectric growth process.

ammonia anneal cycle at 0.1 or 0.01 atm. for anneal times ranging from 15 min. to 10 hours. Following the nitridation cycle, the tube is again evacuated and a final anneal in nitrogen is carried out.

Reoxidized nitrided oxides are formed by a three-step process. The first two steps are identical to the formation of nitrided oxides. Following the nitridation cycle and a pump down, the nitrided oxide undergoes an oxygen anneal cycle at 0.1 atm for times ranging from 15 min. to 3 hours. Following the reoxidation, the tube is again evacuated and an anneal in nitrogen is performed.

The entire process of evacuating the tube and the establishing of a new gas ambient typically takes 3 minutes. Thus the low pressure system is able to rapidly switch between gas ambients without cross-contamination of gases.

On a typical day of runs we grew control oxides first and then the test dielectric. Polysilicon was deposited immediately after dielectric growth on control and test wafers simultaneously. The control and test wafers were then processed together. Monitor wafers were included for Auger analysis and ellipsometry.

2.3 Dilute dielectric growth process

The purpose of examining a dilute dielectric growth process is twofold:

(1) To determine whether the low pressure process is intrinsically different in terms of nitridation and reoxidation mechanisms from an Ar-diluted nitridation/reoxidation process under conditions of equivalent ammonia and oxygen partial pressures.

(2) To develop a process that can be more easily incorporated into existing oxidation furnaces which typically do not have a low pressure capability.

A flow diagram of the dilute process in shown in figure 2.6. The primary differences between the low pressure process and the atmospheric process are : (1) the use of Ar-dilution to achieve a partial pressure of ammonia and oxygen equivalent

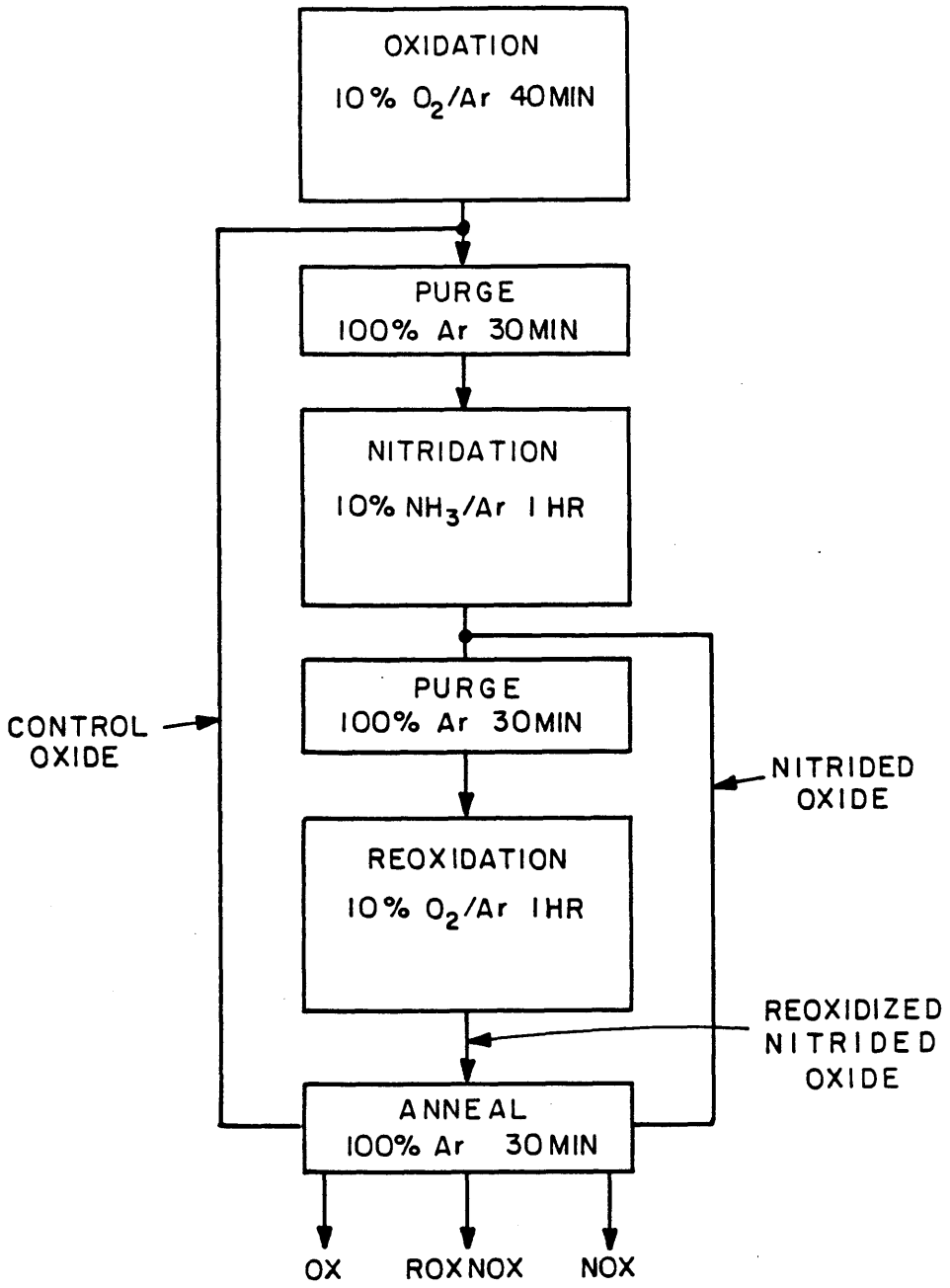

Figure 2.6: Flow diagram of the dilute nitridation/reoxidation gate dielectric growth process.

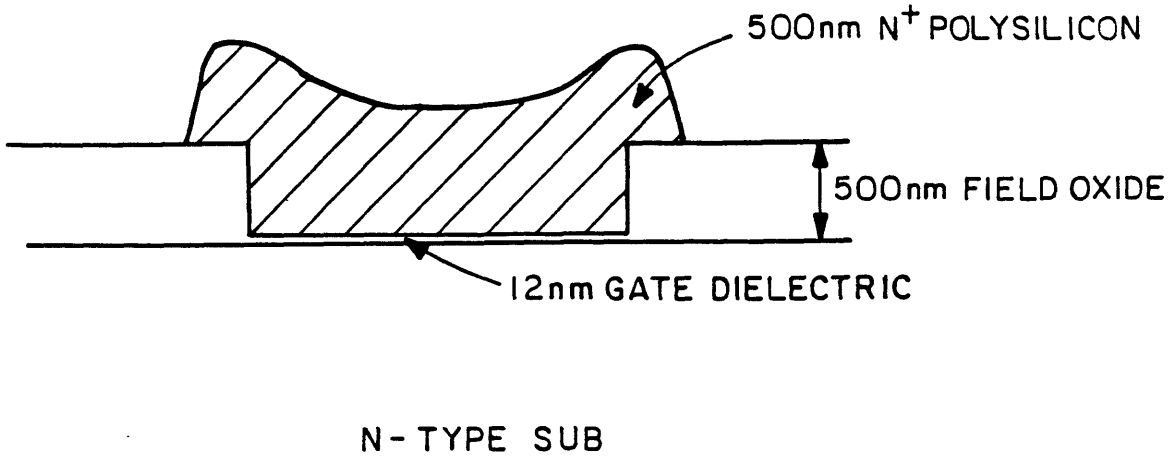

Figure 2.7: Cross-section of the etched field oxide isolated MOS capacitor test structure.

to that used in the low pressure process and (2) the use of tube and gas manifold purges between oxidation and nitridation cycles to prevent cross-contamination of gases. These inert purges took typically 30 minutes as compared to a $\sim$ 3 minute pump down used in the low pressure process to evacuate an ambient.

2.4 Polysilicon gate capacitor process

Since the various dielectrics are ultimately intended for a scaled CMOS process, a simplified polysilicon gate MOS capacitor test process was devised. Two processes were used. The process flows are outlined in Appendix A and B. For most of the low pressure results, an etched field oxide isolated MOS capacitor test structures were fabricated with an n^+ polysilicon gate on 10-20 ohm-cm, $< 100 >$, 2-inch, n–type silicon wafers. The n–type silicon substrate was used to prevent inversion under the field oxide caused by positive charge introduced by the nitridation process. The cross-section of the device structure is shown in figure 2.7. For most of the dilute results, 4-inch wafers were used to form a LOCOS-isolated MOS capacitor

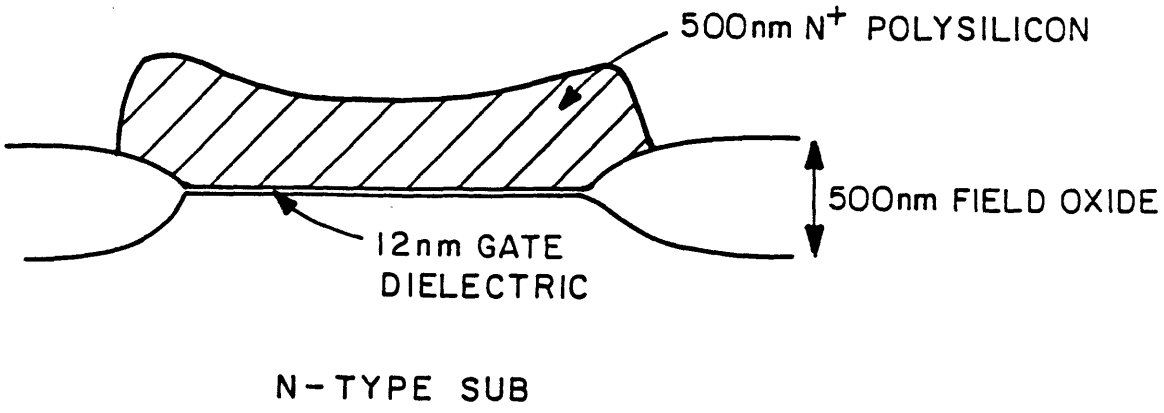

Figure 2.8: Cross-section of the LOCOS-isolated MOS capacitor test structure.

structure with n^+ polysilicon gate on an n-type substrate. A cross-section of the device structure is shown in figure 2.8. The devices received a final anneal in forming gas (20% H_2:N_2 ratio) for 30 min. While capacitors of area 100 × 100, 300 × 300, and 500 × 500 μm^2 were fabricated, the smallest capacitors were commonly used for high-field stress experiments.

2.5 NMOS and PMOS transistor process

NMOS and PMOS transistors with various gate dielectrics were fabricated using a standard, four mask, self-aligned polysilicon gate MOS process on n- and p-type (100) 2-inch diameter wafers of 10-20 ohm-cm and 10-40 ohm-cm, respectively. No channel implants were used in order to minimize the number of process variables. The devices received a final anneal in forming gas (20% H_2:N_2 ratio) for 30 min. Transistors with geometries ranging from W/L=200/200 to 20/0.5 and capacitors of various areas were fabricated. The process flow is outlined in appendix C.

Chapter 3

Measurement Techniques and Material Properties

3.1 Auger electron spectroscopy

The Auger Electron Spectroscopy (AES) profiles shown in this thesis were obtained through Charles Evans Associates (Redwood City ,CA). The profiles were taken on monitor wafers immediately after gate dielectric formation and did not experience further thermal processing. AES was used to identify the atomic concentrations of nitrogen, oxygen, and silicon in 12 nm and 24 nm dielectrics under various nitridation/reoxidation conditions. In the Auger electron spectroscopy method, an electron beam is used to ionize atoms near the surface of the sample ranging from 0.5 to 2.0 nm in depth. In a core level (n=1) ionized atom, if an electron from the second shell (n=2) drops into the core level vacancy, the resulting energy can be released as an X-ray or used to eject an energetic electron (Auger electron) from outer shell forming a doubly ionized atom. The energy of the Auger electron is characteristic of the nuclear charge and thus can be used to identify the amount of a given element near the surface of the sample. The Auger process requires three electrons: the initially ionized electron, the electron that relaxes to a

Primary Beam Voltage	10	KV
Primary Beam Current	0.6	mA
Primary Beam Spot Size	5-10	mm
Sputtering Rate	0.6	nm/min
Data Acquisition Rate	2	pts/min

Table 3.1: AES Analysis Parameters.

lower energy state, and the ejected (Auger) electron. The AES method, therefore, cannot be used to detect hydrogen which is also incorporated during nitridation.

The AES conditions used to analyze the films are shown in Table 3.1. The sample was sputter etched with argon while the AES was periodically measured to profile the atomic composition as a function of depth. In discussions with Greg Meeker of Charles Evans Associates, who performed the measurements, it was noted that the spacing between AES measurement points was about 0.3 nm. However, the actual depth resolution was limited by the ionization of surface atoms in a depth range of 0.5 nm to 2 nm during a scan. The effect is called AES broadening. The knock–on effect of sputtering was found to be negligible by comparing chemically and sputter etched samples. The sensitivity of the AES measurement to nitrogen, oxygen, and silicon was calibrated with SiO_2 and Si_3N_4 standards. The resolution of nitrogen, oxygen, and silicon was estimated to be approximately $\pm$ 2 atomic percent.

3.2 Electrical characterization system

A schematic of the measurement system for MOS capacitors and transistors is shown in figure 3.1. An HP4140 picoammeter and voltage source was used to measure the quasi-static capacitance-voltage characteristic at a ramped voltage of 100 mV/sec. The HP4140 was also used in the measurement of I–V characteristics

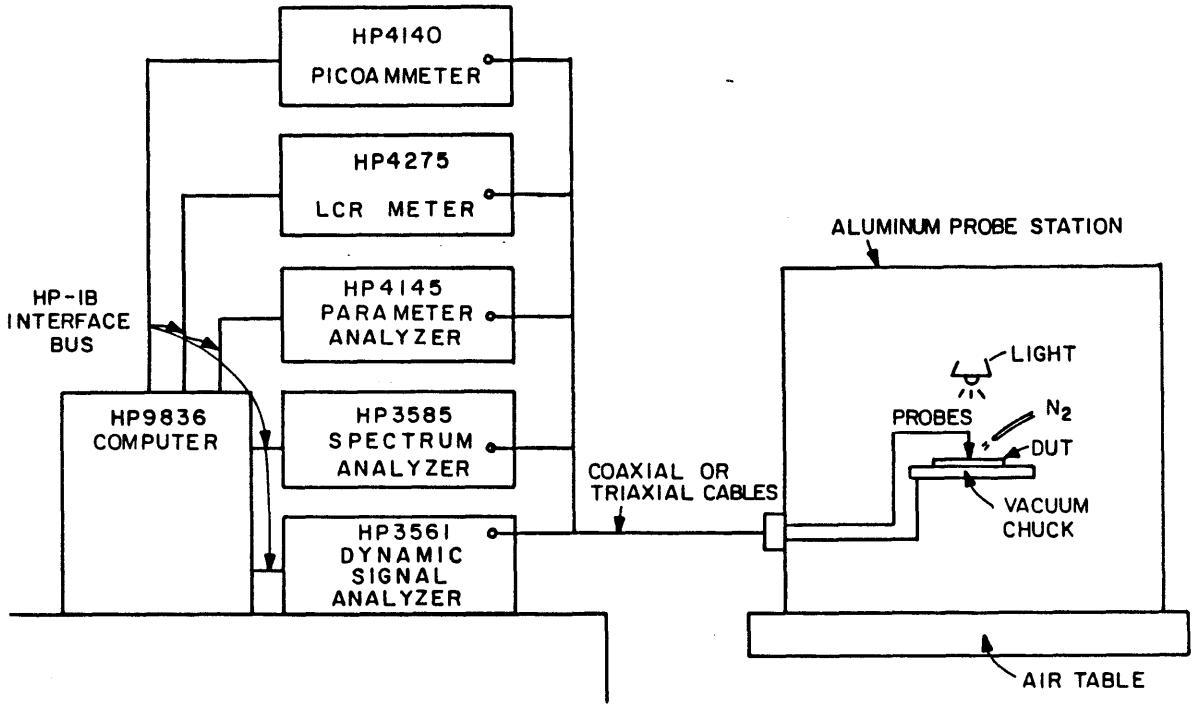

Figure 3.1: Schematic of the electrical characterization system used to analyze MOS capacitors and transistors.

of capacitors. An HP4275 LCR meter was used to measure the small signal, high frequency (30 mV, 100 kHz) capacitance at various bias voltages. The voltage step size for QS and HF capacitance-voltage was 10 mV and measurements were taken from strong inversion to accumulation. The bias for the HP4275 is provided by the HP4145 semiconductor parameter analyzer. The HP4145 also provided a constant current source and voltage meter for high-field stress measurements. The HP9836 computer with associated TECAP [54] software was used to control the above instruments, to acquire data, and to perform analysis.

In DC transistor measurements, the HP4145 semiconductor parameter analyzer together with HP9836 was used for I–V and channel hot-electron stress measurements. 1/f noise measurements used either the HP3585 spectrum analyzer or the HP3561 dynamic signal analyzer.

During measurements, capacitor samples were placed in a probe station. The probe station was located on an air table to minimize vibrations. A microscope light was used for the photogeneration of minority carriers in CV measurements. For some measurements, a stream of dry nitrogen was flowed over the sample to prevent surface conduction. With these precautions, ultimate leakage could be limited to $\leq$ 10 fA.

3.3 Capacitor measurements

A detailed discussion of the measurement techniques used in the evaluation of various gate dielectrics in MOS capacitors is contained in the Master's thesis of Woodward Yang [55]. A summary of the techniques is provided here.

Three types of electrical measurements were performed on capacitors. (1) Quasi-static (QS) and high frequency (HF) capacitance-voltage characteristics of MOS capacitors were used to extract midgap interface state density and the flatband voltage from which the dielectric charge was inferred. (2) Current-voltage measure-

ments were used to identify dominant conduction modes in various dielectrics and to determine the dielectric strength. (3) High-field constant current stress measurements were used to evaluate the reliability of dielectrics formed under various oxidation/nitridation conditions.

3.3.1 Capacitance–Voltage

Capacitance-voltage measurements were used to extract the equivalent oxide thickness, the substrate doping, the flatband voltage and the midgap interface state density.

Equivalent oxide thickness

The insulator thickness is reported as the equivalent oxide thickness inferred from the HF capacitance in accumulation by the relation

$$t_{ox} = \frac{\epsilon_{ox} A}{C_i} \tag{3.1}$$

where $\epsilon_{ox} = 3.9\epsilon_0$, A is the area of the capacitor, and C_i is the measured HF capacitance in accumulation. It should be noted that the measurement of the insulator thickness in this fashion may be in error for dielectrics undergoing a nitridation/reoxidation treatment due to slight changes in the dielectric constant. Therefore changes in the dielectric thickness as a result of the nitridation/reoxidation process were not detectable [56]. The above expression thus gives only the equivalent oxide thickness. The actual insulator thickness, t_i, is related to the equivalent oxide thickness, t_{ox}, by

$$t_{ox} = \frac{\epsilon_{ox}}{\epsilon_i} t_i \tag{3.2}$$

where ϵ_i is the actual insulator dielectric constant. In practice, we have observed that nitrided oxides and reoxidized nitrided oxides typically have an equivalent oxide thickness which is $\leq$ 5-15% smaller than the thickness of control oxides. This may be accounted for by a combination of a slight increase in the dielectric constant

and/or a slight decrease in the dielectric thickness due to densification during the nitridation process.

In the work of Naiman [57], 361 $\AA$ nitrided oxides formed by atmospheric pressure nitridation at 1000 °C, 1 hour, were characterized by ellipsometry. It was found that the nitrided oxide could be modeled as a three-layer structure consisting of surface (7.4 $\AA$), bulk (334 $\AA$), and interface (22 $\AA$) regions. The data indicates that nitridation dramatically increases the index of refraction of the surface (n_f = 2.0) and interface (n_f = 1.7) regions, while increasing the index in the bulk by $\sim$ 3 %. The change in the overall dielectric thickness is less than 1 %. The process of reoxidation is shown to reduce the index of the surface region until it becomes indistinguishable from the bulk, which itself continues to have a slightly larger index than oxide. The interface region does not appear to be affected by reoxidation. The overall dielectric thickness, however, appears to slightly increase with reoxidation (1-3 % depending on the length of the reoxidation). Further discussion of the composition of such films is deferred to section 3.5.

Substrate doping

Calculation of the substrate doping is used in the determination of the flatband voltage. The substrate doping is calculated from the measurement of the maximum high frequency capacitance in strong accumulation and the minimum high frequency capacitance in strong inversion. The method is often referred to as the max-min method [3]. The minimum high frequency capacitance in strong inversion is

$$C_{HF}(inv) = \frac{C_i C_s(inv)}{C_i + C_s(inv)} \tag{3.3}$$

where $C_i = C_{HF}(accum)$ and $C_s(inv)$ is the high frequency semiconductor capacitance in strong inversion given by

$$C_s(inv) = \frac{\epsilon_s A}{(2\epsilon_s(\phi_F + E_g/2q)/qN_D)^{1/2}} \tag{3.4}$$

where it is assumed that the electron quasi-Fermi level is pinned near the conduction

band of Si in strong inversion. In addition, the depletion approximation has been used and ϕ_F is the bulk potential given by $\phi_F = (kt/q)ln(N_D/n_i)$, ϵ_s is the dielectric constant of silicon, E_g is the silicon bandgap and N_D is the substrate doping. Using the above expressions the following expression for N_D is obtained:

$$N_D = (2\frac{kT}{q}ln\frac{N_D}{n_i} + \frac{E_g}{q})\frac{1}{q\epsilon_s A^2}(\frac{C_i C_{HF}(inv)}{C_i - C_{HF}(inv)})^2 \tag{3.5}$$

Thus using the maximum and minimum of the high frequency capacitance curve, the above equation can be iteratively solved for the substrate doping. For n-type substrates used in this thesis, the value of the substrate doping varied from 8×10^{14} to 1.5×10^{15} cm^{-3}.

Fixed charge

Flatband voltage measurements are used to calculate the positive charge introduced by nitridation and to measure the trapped electrons following a constant current stress. The flatband voltage is the voltage at which the measured high frequency capacitance is equal to the flatband capacitance.

$$C_{FB} = \frac{C_i C_s(\psi_s = 0)}{C_i + C_s(\psi_s = 0)} \tag{3.6}$$

where $C_s(\psi_s = 0)$ is semiconductor capacitance when the surface potential, ψ_s, is zero. $C_s(\psi_s = 0)$ is given by

$$C_s(\psi_s = 0) = \frac{\epsilon_s A}{(kT\epsilon_s/q^2 N_D)^{1/2}} \tag{3.7}$$

where N_D is obtained from the method of the previous section.

The fixed charge density, Q_f, is found from the high frequency C–V measurements by first measuring the flatband voltage, comparing it with the theoretical flatband voltage assuming zero fixed charge, and multiply the resultant flatband voltage shift by the measured insulator capacitance.

$$Q_f = \Delta V_{fb} C_i \tag{3.8}$$

where ΔV_{fb} is the difference between the measured flatband voltage and the flatband voltage for the case of zero fixed charge and C_i is simply the high frequency capacitance in strong accumulation. The flatband voltage for the case of zero fixed charge is simply the metal-semiconductor work function difference, ϕ_{ms}. Based on the work of Hickmott [58], a value of ϕ_{ms} of -0.20 V was used for the case of a phosphorus-doped polysilicon gate and a n-type substrate doped to 1.5×10^{15} cm^{-3}. The uncertainty in the value of ϕ_{ms}, however, is about $\pm$ 0.06 V given the range of values reported by Hickmott [58]. The flatband voltage of control oxide samples was consistently -0.23 $\pm$ 0.01 V for numerous runs, yielding an average fixed charge of 5×10^{10} cm^{-2} with a variation of approximately $\pm 2 \times 10^{10}$ cm^{-2} over various runs. However, due to the uncertainty in ϕ_{ms}, the precise value of the fixed charge cannot be specified to less than $\pm$ 10^{11} cm^{-2}.

The above approach refers the calculated fixed charge to the interface and assumes that the charge due to interface states at flatband is negligible. In reality, the fixed charge may be distributed throughout the bulk of the dielectric. To determine the actual charge centroid $(\overline{Q_f}, \overline{x})$ one can in principle look at the positive and negative gate I–V characteristics of the dielectric. These measurements, however, are difficult to interpret for the thin dielectrics (12 nm) used in this study [55].

The accuracy of the flatband voltage measurement is limited to $\pm$ 10 mV (due to the minimum step size of the voltage source) which corresponds to an uncertainty in the fixed charge of $\pm 2 \times 10^{10}$ cm^{-2}. The overall precision with which the fixed charge can be specified, however, is dominated by the uncertainty in the work-function difference limiting the absolute value of the fixed charge to approximately $\pm$ 10^{11} cm^{-2}.

Interface State Density

The interface state density between flatband ($\psi_s = 0$) and the onset of strong inversion ($\psi_s = 2\phi_F$) was obtained from the combined high-low frequency method [109]. In this method, the interface state capacitance, C_{it}, is determined from the

difference between the QS C–V and HF C–V measurements as a function of gate bias, V_g,

$$C_{it} = (\frac{1}{C_{QS}} - \frac{1}{C_i})^{-1} - (\frac{1}{C_{HF}} - \frac{1}{C_i})^{-1} \tag{3.9}$$

The density of interface states, D_{it} (states/cm^{2}eV), is obtained as a function of V_g as

$$D_{it}(V_g) = \frac{C_{it}(V_g)}{q}. \tag{3.10}$$

A relationship between the surface potential and the gate voltage can be obtained from the QS C–V by noting that an incremental change in V_g causes an incremental change in ψ_s through the capacitive voltage divider relation

$$d\psi_s = \frac{C_i}{C_i + C_s + C_{it}} dV_g \tag{3.11}$$

Rearranging equation 3.11 in terms of C_{QS} and integrating from the condition that $\psi_s = 0$ at $V = V_{fb}$ we obtain

$$\psi_s = \int_{V_{fb}}^{V_g} (1 - \frac{C_{QS}}{C_{ox}}) dV_g \tag{3.12}$$

The extraction of the interface density from the HFCV and QSCV by the high–low method is limited to the range $0 < \psi_s < 2\phi_f$. Near $\psi_s = 2\phi_f$, the method erroneously counts inversion charge (Q_{inv}) as interface states (D_{it}). Near $\psi_s = 0$, interface states with short time constants may respond to the high frequency signal. Thus the method is most valid near midgap where $\psi_s = \phi_f$.

The resolution of the interface state density is determined by the magnitude of the minimum displacement current. Typical maximum and minimum capacitances for a capacitor area of 100μm x 100μm area are $\sim$ 30pF and $\sim$ 1pF, respectively. For a ramp rate of 100 mV/sec, the minimum displacement current is $\sim$ 100 fA. The displacement current due to stray capacitances is usually 25 fA which can be compensated to $\pm$5 fA. Thus the resolution of capacitance measurement is $\pm$50 fF

corresponding to an uncertainty in the interface state density of about $\pm 5 \times 10^9$ states/cm^{2}eV.

3.3.2 Constant current stress

The constant current stress technique was used to study the time dependent generation of interface states, the trapping of charges (primarily electrons), and the charge-to-breakdown. The charge-to-breakdown is measured under constant current conditions and is defined as the amount of charge that can passed through the dielectric before destructive breakdown occurs. The technique provides a simple means to evaluate the relative reliability of various dielectrics. Typically, a constant current under high field conditions (6MV/cm - 10 MV/cm) is applied to the dielectric and the voltage necessary to maintain the current is monitored. To study the early degradation characteristics of the dielectric, a current density of 10 μA/cm^2 was used for stress times up to 10,000 seconds corresponding to a fluence of 0.1 C/cm^2. The constant current stress is periodically interrupted for C–V measurements from which the generated interface states and the trapped charge can be extracted as a function of stress time. Both positive and negative gate stresses were investigated. Under positive gate conditions, electrons tunnel from the substrate into the dielectric and under negative gate stress, electrons tunnel from the gate into the dielectric. The tunneling of holes was assumed to be negligible due to the larger barrier height for holes.

When the stress is performed under higher current densities, the technique can be used to measure the charge-to-breakdown, Q_{bd}. This technique has seen extensive use in recent years [59]. The charge-to-breakdown data reported here were obtained under a constant current stress condition of 10 mA/cm^2. The resulting charge-to-breakdown is normalized by the area of the device and is expressed in units of C/cm^2.

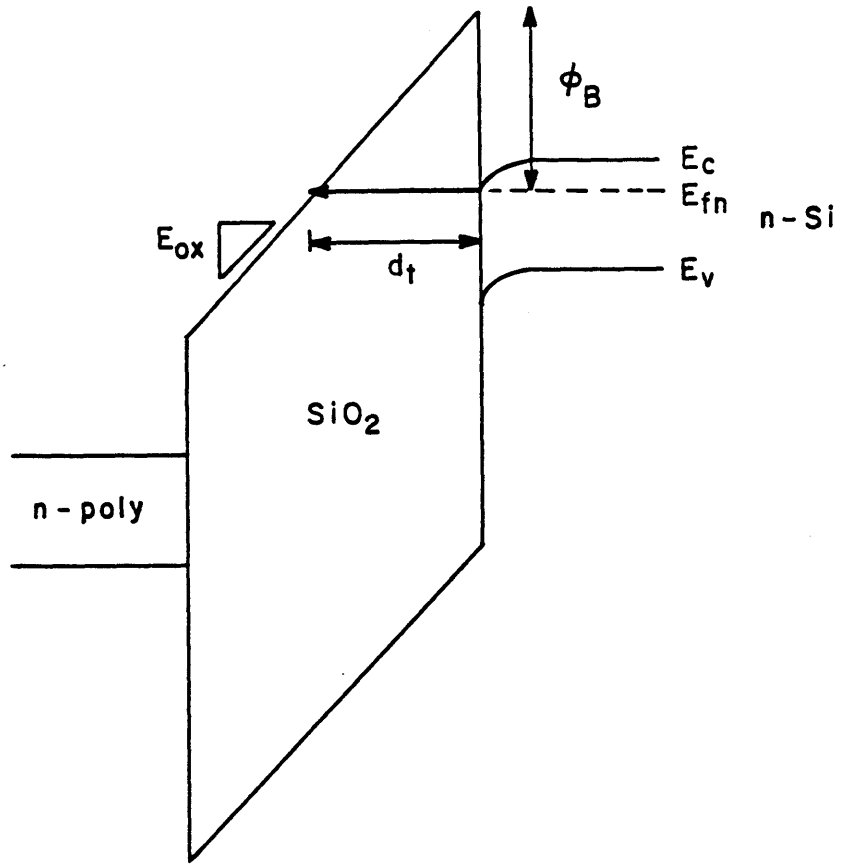

Figure 3.2: Fowler–Nordheim Conduction in MOS Structure.

3.3.3 Current–Voltage

The current–voltage (I–V) characteristic of the dielectric was measured to identify the dominant conduction mechanisms and to determine the breakdown field. In silicon dioxide MOS devices, Fowler–Nordheim (F–N) electron tunneling is the dominant conduction mechanism [60] under high electric fields (> 5 MV/cm). Electrons tunnel from the silicon conduction band into the oxide conduction band at a constant energy under high electric fields as shown in figure 3.2.

In the figure, d_t is the F–N tunneling distance, Φ_b is the electron barrier height at the interface, and E_{ox} is the electric field in the dielectric. In principle, holes

can tunnel from the gate into the valence band of the dielectric. However, the hole current is negligible since the barrier for holes is $\sim$ 1.5 eV larger than for electrons. The tunnel current is normally given by

$$I = ACE_{ox}^2 \exp -\frac{B}{E_{ox}} \tag{3.13}$$

where A is the area of the sample and the pre–exponential factor, C, is given by

$$C = \frac{q^3 m}{8\pi h m_{ox} \Phi_b} \tag{3.14}$$

and the exponential factor, B, is given by

$$B = \frac{8\pi}{3qh}(2m_{ox})^{\frac{1}{2}}\Phi_b^{\frac{3}{2}} \tag{3.15}$$

where h is Planck's constant, m is the free electron mass, and m_{ox} is the effective electron mass in oxide. Experimental data for silicon dioxide on silicon was found to be in excellent agreement with $C = 1.06 \times 10^{-6}$ (amp/V^2) and $B = 2.385 \times 10^8$ (V/cm) which corresponds to $m_{ox} = .5m$ and $\Phi_b = 2.9$ eV. The value of Φ_b is in agreement with that calculated by Weinberg [60]. It is calculated assuming that electrons in the emitting electrode are described by a Fermi gas. Weinberg [60] points out that, in fact, electrons in the Si are confined in a narrow potential well at the interface which leads to a quantization of their energy normal to the interface. Since the current is dominated by tunneling from the lowest subband, the calculated Φ_b represents the barrier from the bottom of the lowest subband ($E_0 - E_c \sim 0.2$ eV for (100) Si) and the conduction band of SiO_2. Correcting for the quantization of the electron energy, Φ_b, as defined in figure 3.2, becomes 3.1 eV.

The resolution of the current measurements were limited by leakage at 10 fA. The I–V characteristics were obtained by stepping the bias voltage at 250 mV increments, waiting for 100 msec, and measuring the current as an average over 256 samples.

3.3.4 High-field edge effects

For constant current stress measurements, it is important to uniformly stress the dielectrics. In order to investigate possible edge effects at high fields due to the gate edge geometry, the current–voltage characteristics of capacitors with various areas were compared. The geometries used were 100 × 100, 300 × 300, and 500 × 500 μm^2, which yielded devices with different perimeter-to-edge ratios. Figure 3.3a shows the current–voltage characteristics of capacitors using the etched field oxide isolation scheme (figure 2.7). Since the measured current density is the same for the various geometries, we conclude that edge effects are negligible for such capacitors. Figure 3.3b shows the current–voltage characteristics of capacitors using LOCOS isolation (figure 2.8). In this case, there is a variation in the current density for the various geometries, suggesting possible edge effects.

The data presented in this thesis on low pressure nitridations were taken on capacitors using the etched field oxide isolation scheme. However, data taken on dilute nitridation experiments were taken on capacitors using LOCOS isolation. Due to edge effects, the comparison of high-field stressing of low pressure and dilute nitridations must be qualitative, as discussed in section 4.5.

3.4 Transistor measurements

3.4.1 Effective channel length

The actual channel length of devices can differ substantially from the drawn channel length due to photolithography variations as well as the lateral diffusion of dopants. The determination of the actual length is important for device analysis. The method used here was proposed by Chern, et. al. [61] and is outlined below. Briefly, the method involves the measurement of the device resistance (V_{DS}/I_{DS})

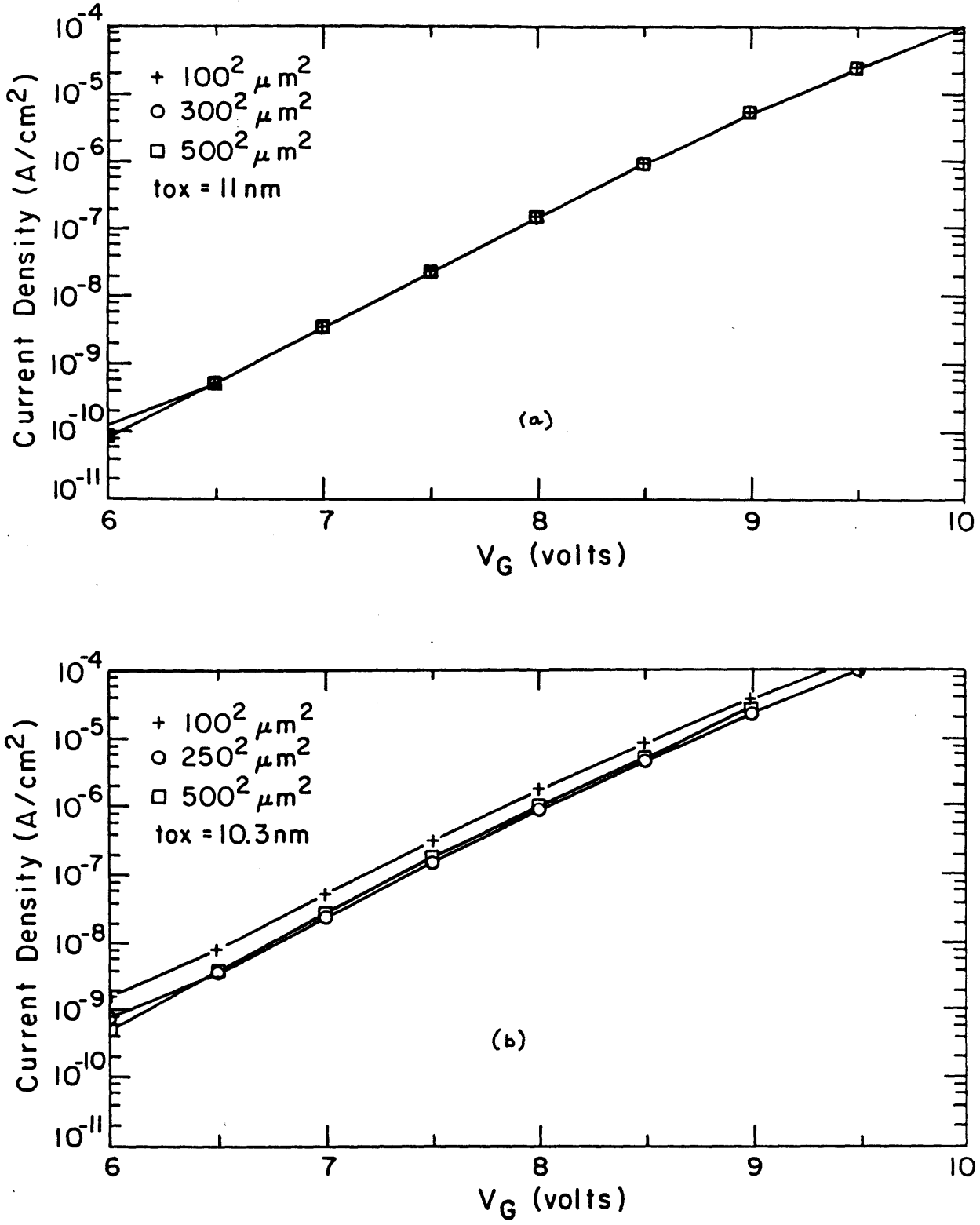

Figure 3.3: Positive gate current–voltage characteristics of capacitors with (a) etched field oxide isolation and (b) LOCOS isolation.

of a set of transistors with the same widths but with different channel lengths for a set of gate biases.

The current through a MOS transistor operating in the linear region is given by

$$I_{DS} = \frac{W_{eff}}{L_{eff}} \mu C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS} \tag{3.16}$$

and its intrinsic channel resistance is

$$R_{int} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\frac{W_{eff}}{L_{eff}} \mu C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}) V_{DS}} \tag{3.17}$$

where $W_{eff} = W_{drawn} - \Delta W$ and $L_{eff} = L_{drawn} - \Delta L$ The measured resistance however includes intrinsic and extrinsic resistances

$$R_m = R_{int} + R_{ext} = R_{ext} + A(L_{drawn} - \Delta L) \tag{3.18}$$

where

$$A = ((W_{eff} \mu C_{ox} (V_{GS} - V_T - \frac{1}{2} V_{DS}))^{-1} \tag{3.19}$$

Given at least two transistors with different L_{drawn} measured at the same V_{gs}, a plot of R_m versus L_{drawn} forms a straight line. When several lines with different gate biases are plotted the lines intersect at $(R_{ext}, \Delta L)$. An example is shown in figure 3.4.

3.4.2 Channel hot–electron stress

The channel hot electron stress technique has seen extensive use in recent years as a DC accelerated aging tool used to model and monitor hot-electron induced degradation in MOSFETs [6]. We have used the technique to evaluate the relative reliability of transistors formed with various gate dielectrics. The classical explanation of hot-electron effects is that in short n-channel MOSFETs, electrons are strongly accelerated (heated) by the lateral E-field particularly near the drain and

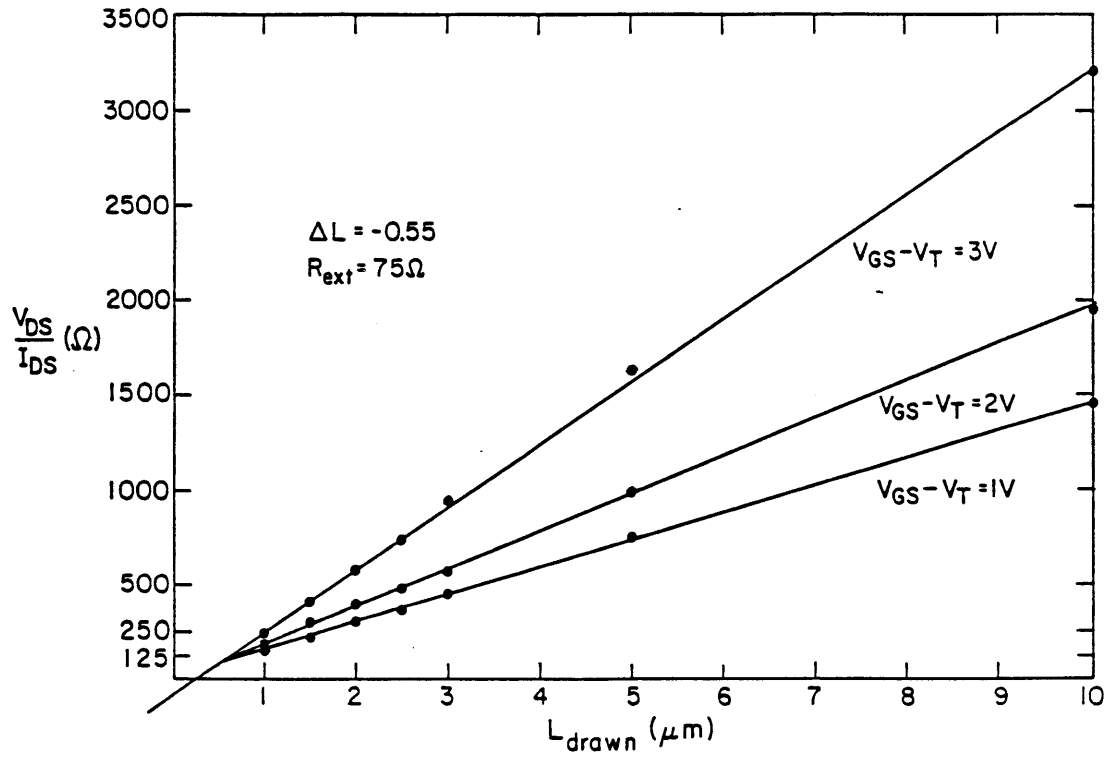

Figure 3.4: Measured resistance as a function of drawn channel length used to extract the effective channel length and extrinsic resistances.

some fraction are emitted into the gate oxide. This leads to electron trapping and/or interface state generation which accounts for experimentally observed threshold voltage shifts, transconductance degradation, and subthreshold slope degradation. The damaged region is believed to be localized near the drain [62]. A simultaneous effect associated with hot-electrons is the presence of a substantial substrate hole current which is produced by impact ionization near the drain. The substrate current is an excellent monitor for hot-electron effects. The substrate current characteristically forms a bell-shaped curve when I_{SUB} is plotted against V_{GS} for a given V_{DS}. The substrate current is modeled empirically by [63]

$$I_{SUB} \propto E_m I_{DS} \alpha e^{-\beta/E_m} \tag{3.20}$$

where E_m is the maximum channel electric field proportional to $(V_{DS} - V_{DSAT})$ and the term $\alpha e^{-\beta/E_m}$ is the impact ionization rate. As V_{GS} increases, I_{DS} increases causing the initial rise in I_{SUB}. However, as V_{GS} becomes larger, V_{DSAT} also becomes larger and thus the maximum channel electric field decreases, eventually causing I_{SUB} to decrease, giving rise to the characteristic bell-shaped curve. In the work of Chan [63], it was shown that a plot of $\ln(I_{SUB}/I_{DS})$ versus $1/(V_{DS} - V_{DSAT})$ yields a straight line for device channel lengths ranging from 0.95 μm to 2.7 μm for various gate voltages. This implies that the I_{SUB}/I_{DS} ratio can be used to estimate the maximum channel electric field. Chan [63] cautions, however, that the proportionality between I_{SUB}/I_{DS} and E_m can depend on such factors as t_{ox}, N_{SUB}, and x_j. In this thesis, we are interested in estimating the relative reliability of transistors with different types of gate dielectrics. Given that such factors as t_{ox}, N_{SUB}, and x_j are nominally the same in the various devices, the stressing of various devices under conditions of similar I_{SUB}/I_{DS} ratios should subject the various devices to similar stress conditions. As discussed in chapter 5, however, the level of degradation at a given I_{SUB}/I_{DS} was observed to have a slight channel length dependence.

It is customary to stress the device under a high V_{DS} and a V_{GS} corresponding

to the peak in the substrate current and to monitor hot-electron degradation by monitoring the peak linear transconductance degradation as a function of stress time. It is also common to define a quantity called lifetime, the stress time required to reach 10% transconductance degradation, and to plot lifetime as a function of I_{SUB}/I_{DS} or V_{DS}. The linear extrapolation of lifetime from conditions of high V_{DS} or I_{SUB}/I_{DS} to lower operating conditions is often used to determine the operating life of the device.

In measurements shown in this thesis, NMOS transistors with various dielectrics and nominally similar channel lengths were stressed at large V_{DS} and V_{GS} corresponding to the peak in the substrate current. However, since devices are not identical due to slight variations in channel length and mobility, the drain voltage during stress was set appropriately to obtain a range of I_{SUB}/I_{DS} ratios over which the various devices could be compared. In this way, the effect of the gate dielectric in the determining the reliability of a MOSFET was estimated.

3.4.3 Inversion layer mobility

Measurements were made on n- and p-channel devices with a W/L ratio of 100/100 μm. Values were extracted from the linear region of the I_{DS} vs. V_{GS} curve for $V_{DS} = 50$ mV. The effective mobility was defined as:

$$\mu_{eff} = \frac{I_{DS}}{\frac{W}{L} C_{ox}(V_{GS} - V_T)V_{DS}} \tag{3.21}$$

where the threshold voltage, V_T was found by linear extrapolation of the I_{DS} vs. V_{GS} curve to $I_{DS} = 0$. Since the process of nitridation and reoxidation produces slight changes dielectric capacitance, it is important to use the actual dielectric capacitance, C_{ox}, as determined from high frequency C–V measurements. The above method may be somewhat in error near the threshold voltage particularly in thin oxides because the assumed relation $Q_N = C_{ox}(V_{GS} - V_T)$ is not entirely accurate [64]. We therefore report the mobility at $V_{GS} - V_T \geq 0.5V$. For evaluating

the normal field dependence of the mobility, μ_{eff} is plotted against $V_{GS} - V_T$.

3.4.4 1/f noise

1/f noise, due its sensitivity to the density of oxide traps, has been used here as a measurement tool to study oxide traps near the band edges of silicon [52] where the process of nitridation/reoxidation is believed to introduce traps. As discussed in section 3.3.1, normal C–V techniques are not valid in this region of the bandgap. According to the McWhorter model [66], 1/f noise is attributed to carrier density fluctuations arising from the trapping and de-trapping of inversion layer carriers by oxide traps located within a tunneling distance of the interface. Thus 1/f noise measurements indicate the number of inversion layer carriers that are in communication with oxide traps and allow an estimate of the interfacial oxide trap density. As shown in section 6.1, 1/f noise expressed in terms of the drain voltage noise spectrum is given by

$$S_{VD} = \frac{\overline{V_{DS}^2}}{\Delta f} \propto \frac{N_T(E_{Fn})}{WLC_{ox}^2 f^{\gamma}} \quad (\frac{V^2}{Hz}) \tag{3.22}$$

where $N_T(E_{Fn})$ (cm^{-3}) is the oxide trap density at the electron quasi-fermi level, WL is the device area, C_{ox} is oxide capacitance, f is the frequency, and typically γ = 1. Since 1/f noise is sensitive to traps near the quasi-Fermi level, a low V_{DS} is desirable to maintain a nearly constant E_{Fn} from source to drain so as to determine the energy location of traps. In strong inversion ($V_{GS} - V_T \geq 0.2$V), the E_{Fn} is pinned near the conduction band but the oxide bands may move relative to the E_{Fn} as shown in figure 3.5. Thus in principle, one can plot 1/f noise as a function of gate bias to extract the oxide trap density as a function of energy and space.

To measure S_{VD}, the test apparatus of figure 3.6 was used to measure the open circuit drain voltage fluctuation. The entire device and test circuit are located within a shielded probe station. The probe station was generally effective in eliminating radio-frequency interference, but additional care was required in reducing

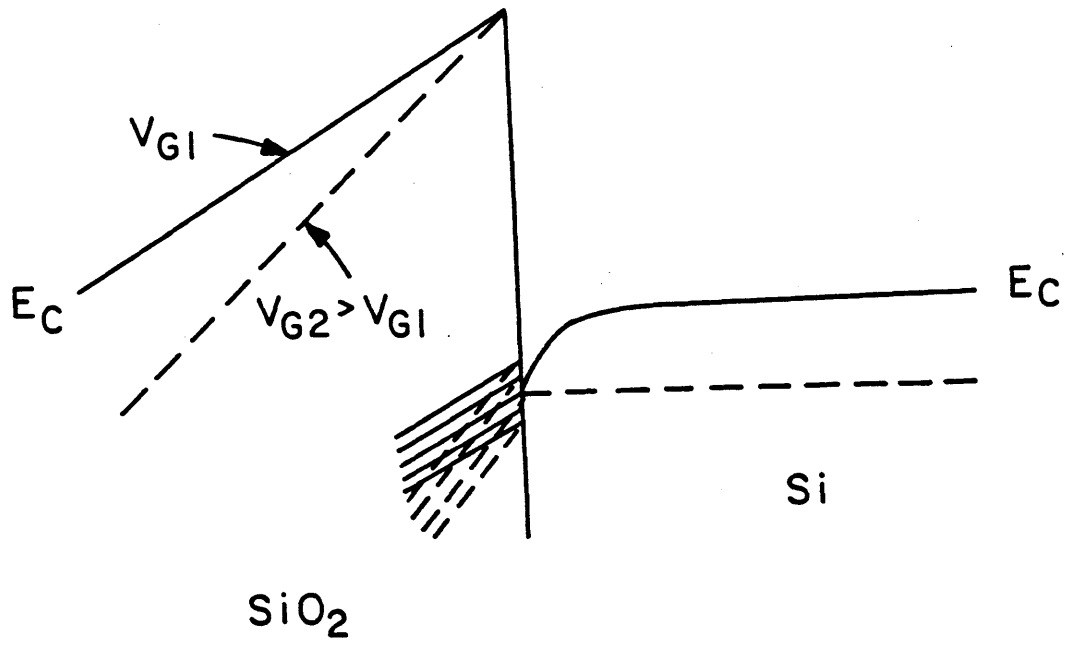

Figure 3.5: Oxide band bending illustrating the relative position of oxide traps and the electron quasi-Fermi level in Si.

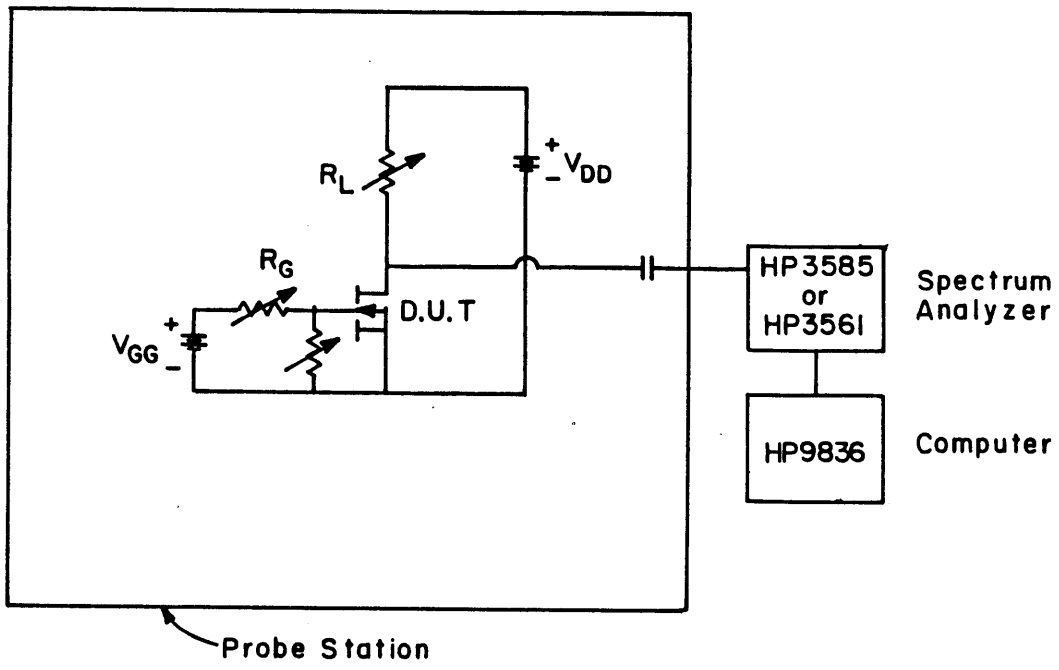

Figure 3.6: Test circuit used to measure 1/f noise in MOSFETs.

60 Hz noise interference. Two types of interference were observed: noise due to a magnetic field and capacitively coupled noise. The former can be reduced by (i) eliminating the sources of interference such as fluorescent lights, power supplies, and power strips or (ii) by shielding the measurement system by enclosing it in material with a high conductivity and high permeability. The skin depth of a material is given by [65]:

$$\delta = \frac{1}{\sqrt{f\pi\mu\sigma}} \tag{3.23}$$

In the case of aluminum, the skin depth at 60 Hz is on the order of 9 mm. The thickness of aluminum used in the construction of the probe station was 6 mm; thus, the probe station was not particularly effective in attentuating magnetic fields at 60 Hz. However, greater success was had in reducing capacitively coupled noise by reducing noise sources and eliminating stray capacitances. As final precaution, noise measurements were not made at frequencies corresponding to 60 Hz multiples. The device is biased with battery supplies instead of switch-mode power supplies to eliminate the noise due to the power supply. The noise due to the batteries was below the detection limit of the spectrum analyzers. The noise of the potentiometers was limited to thermal noise and was well modelled by the relation $\overline{V_{th}^2} = 4kTR\Delta f$. The drain voltage fluctuations are AC coupled to either of two spectrum analyzers, the HP3585 or the HP3561. The HP3585's ultimate resolution is limited to $\sim 8nV/\sqrt{Hz}$ for a measurement bandwidth, Δ f = 3 Hz. It is capable of noise measurements in the frequency range of 20 Hz - 50 kHz. The resolution of HP3561 is $\sim 35nV/\sqrt{Hz}$ at Δ f = 0.3 Hz. but is capable of lower frequency measurements. With AC coupling, the lower frequency limit of the HP3561 is $\sim$ 1 Hz. For even lower frequency measurements, DC coupling must be used and the measurement becomes extremely sensitive to bias drift, thermal fluctuations, and other low frequency fluctuations. Measurements with either the HP3561 or the HP3585 are in agreement within the variances found on a single device that is measured repeatedly.

The total noise spectrum measured at the drain is a combination of the device

noise of interest and the noise due to the measurement system. In the following first order analysis we determine the magnitude of the system noise which must be subtracted from the total noise to yield the device 1/f noise. The total noise spectral density, S_{V_T}, measured by the spectrum analyzer is given by

$$S_{V_T} = \frac{\overline{V_{TOT}^2}}{\Delta f} = \frac{\overline{V_D^2}}{\Delta f} + \frac{(r_o \parallel R_L)^2}{R_L^2} 4kTR_L + g_m^2 (r_o \parallel R_L)^2 4kTR_G \tag{3.24}$$

where $\frac{\overline{V_D^2}}{\Delta f}$ is the drain voltage noise spectral density of the DUT, $4\mathrm{kTR}_L$ is the thermal noise of the load resistor, $4\mathrm{kTR}_G$ is the thermal noise of the gate bias resistor, and $r_o = 1/g_o$ is output resistance of the device. The drain voltage noise of the DUT contains both 1/f and thermal noise components

$$\frac{\overline{V_D^2}}{\Delta f} \approx \frac{k_1}{WLC_{ox}^2 f} + \frac{4kT}{2/3 g_m} \left(\frac{g_m^2}{g_o^2}\right) \tag{3.25}$$

where the first term of the RHS represents the 1/f noise of interest and second term of RHS is the device thermal noise [67]. For measurements in the linear region, $V_{DS} < V_{GS} - V_T$, the drain current of the DUT is given by

$$I_D = \frac{W}{L} \mu C_{ox} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS} \tag{3.26}$$

and the device transconductance, neglecting the normal field dependence of the mobility is

$$g_m = \frac{W}{L} \mu C_{ox} V_{DS} \tag{3.27}$$

and the device output conductance is

$$g_o = \frac{W}{L} \mu C_{ox} (V_{gs} - V_T - V_{DS}) \tag{3.28}$$

The value of the load resistance is

$$R_L = \frac{V_{DD} - V_{DS}}{I_{DS}} \tag{3.29}$$

where $V_{DD} = 1.5V$. For typical measurement values of $V_{DS} = 0.2$ V and $V_{GS} - V_T = 0.5$, $\frac{r_o}{R_L} \sim 0.2$ so that the measured noise can be approximated by

$$S_{V_T} \sim \frac{\overline{V_D^2}}{\Delta f} + (r_o/R_L)^2 4kTR_L + (g_m r_o)^2 4kTR_G \tag{3.30}$$

where $g_m r_o \leq 1$ in the linear region. For typical numbers, $V_{GS} - V_T = 0.5$, $V_{DS} = 0.2$, W/L = 20/5, $R_L = 10$ kΩ the noise at the output due to the thermal noise of the MOSFET is $\sim 8nV/\sqrt{Hz}$, due to the load resistance is $\sim 8nV/\sqrt{Hz}$ and due to the gate resistance is $\sim 9.6nV/\sqrt{Hz}$. Thus the total system noise for HP3585, including the noise due to the spectrum analyzer is

$$system\ noise = ((9.6)^2 + (8)^2 + (8)^2 + (8)^2)^{1/2} \sim 17nV/\sqrt{Hz} \tag{3.31}$$

For the HP3561 the total system noise is

$$system\ noise = ((9.6)^2 + (8)^2 + (8)^2 + (35)^2))^{1/2} \sim 38nV/\sqrt{Hz} \tag{3.32}$$

In devices with low 1/f noise, the system noise floor is easily detected in the frequency range of the measurement. Usually, in comparing the noise in devices with various gate dielectrics, we averaged the noise over at least 5 devices per wafer to determine the variance in the noise. Typical relative variance across a wafer defined as the ratio,

$$relative\ variance = \frac{\sigma^2_{S_{V_D}}}{\overline{S_{V_D}}} \tag{3.33}$$

where $\sigma^2_{S_{V_D}}$ is the variance in the observed noise and $\overline{S_{V_D}}$ is the average observed noise, varied from 10 % to 50 %. These variances are indicated as error bars in our data.

Since the measured noise is also sensitive to the device area and the oxide capacitance the noise of devices from different wafers must be appropriately scaled for meaningful comparisons. Unless otherwise indicated, the data is not the raw data but has been scaled. Ideally, one would like to use large area devices to minimize geometry variations, but as indicated by equation 3.22, the 1/f noise magnitude falls off linearly with the area. This limits measurements to devices with areas $\leq$ 100 μm^2 for $t_{ox} = 12nm$ particularly in the case of p-channel oxide devices which consistently showed the lowest noise.

3.5 Effect of nitridation and reoxidation on composition

In this section, we will briefly review the material properties of nitrided oxides as discussed in the literature. Where appropriate we include our data in support of various observations on nitridation mechanisms.

It is generally accepted that the process of nitridation (or ammonia anneal) results in the incorporation of nitrogen and hydrogen into the silicon dioxide matrix [12,41]. The extent of the incorporation depends on various factors including nitridation temperature, pressure, time, and initial oxide thickness. Nitridation characteristically results in the relatively rapid incorporation of nitrogen (or nitrogen-containing species)into the surface and the interface region by primarily replacing oxygen (or oxygen-containing species). The reaction with the bulk of the silicon dioxide occurs more slowly by comparison. A typical AES depth profile is shown in figure 3.7. It has been postulated that nitridation involves the reaction of NH_3 (or its derivatives) with the surface of the silicon dioxide film as well as the diffusion of NH_3 (or its derivatives) through the silicon dioxide film to react with strained bonds at the Si/SiO_2 interface. The concept of a diffusion-limited reaction at the interface is supported by the dependence of the interface nitrogen concentration on the initial

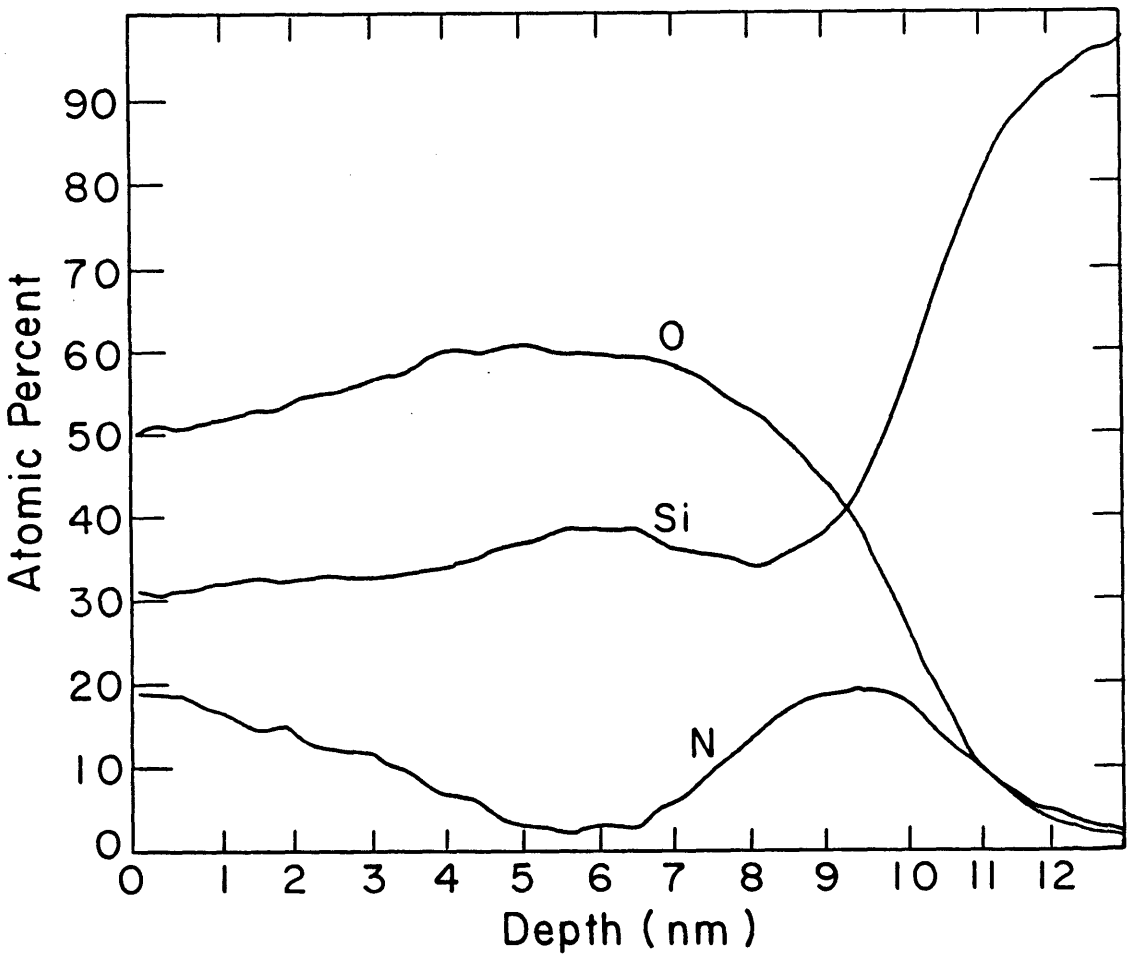

Figure 3.7: Typical Auger depth profile of a 12nm oxide nitrided in 0.1 atm ammonia at 950 °C for 1 hour.

oxide thickness as shown in figure 3.8 as well as the dependence on the ammonia partial pressure (figure 3.9). The following reactions have been postulated to take place [42]:

$$2Si0_2 + 2NH_3 \leftrightarrow Si_2N_2O + 3H_2O \tag{3.34}$$

or

$$3SiO_2 + 4NH_3 \leftrightarrow Si_3N_4 + 6H_2O \tag{3.35}$$

Both reactions result in the evolution of oxygen-containing species which may react elsewhere in the dielectric or out-diffuse from the dielectric. The role of oxygen-containing by-products will be discussed shortly. The change in the free energy for equation 3.34 is smaller than for equation 3.35 favoring the former as the dominant reaction [42]. In addition, the direct reaction of ammonia with the silicon substrate is also possible. However, heavy nitridations indicate that the nitrogen concentration is typically saturated at < 40 at. %, which would correspond to the conversion of SiO_2 to Si_2N_2O. This is supported with AES data shown in figures 3.9 and 3.10. Nevertheless, the data does not preclude the presence of both Si_2N_2O and Si_3N_4 phases on a molecular scale within the dielectric [57].

IR (infrared spectroscopy) studies by Naiman [69], indicate the presence of a new line at a wavenumber of approximately 1000 cm^{-1} which, due to its proximity to the trisilylamine peak, was attributed to nitrogen which is planar triply bonded to silicon. The nitridation conditions studied by Naiman, however, are relatively heavy compared to the conditions used in this thesis. Thus the trigonal bonding may represent a latter or final stage of the nitridation process.

An appealing view of the nitridation process has been proposed by Kuiper, et. al. Naiman, et. al. Vasquez, et. al. and Han, et. al. [72,57,73,45] Nitridation of SiO_2 is viewed as an equilibrium between nitridation by NH_x species and oxidation by OH_y fragments which are by-products of the nitridation reaction. Everywhere in

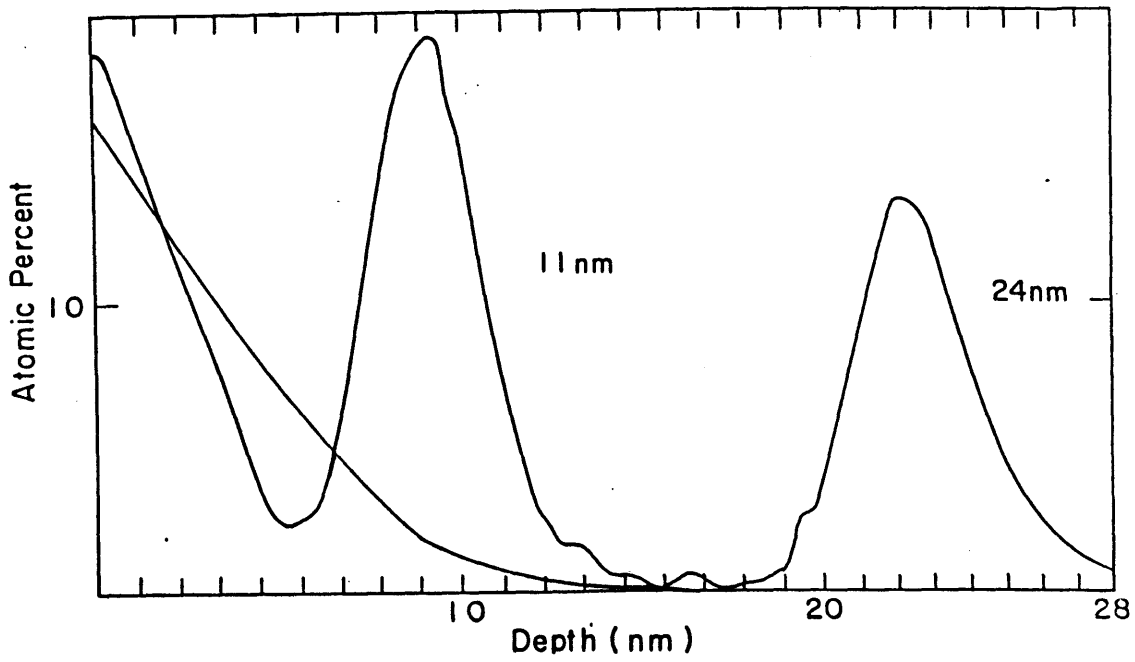

Figure 3.8: Effect of initial oxide thickness on the incorporation of nitrogen during nitridation at 0.1 atm, 950 °C, 1 hour.

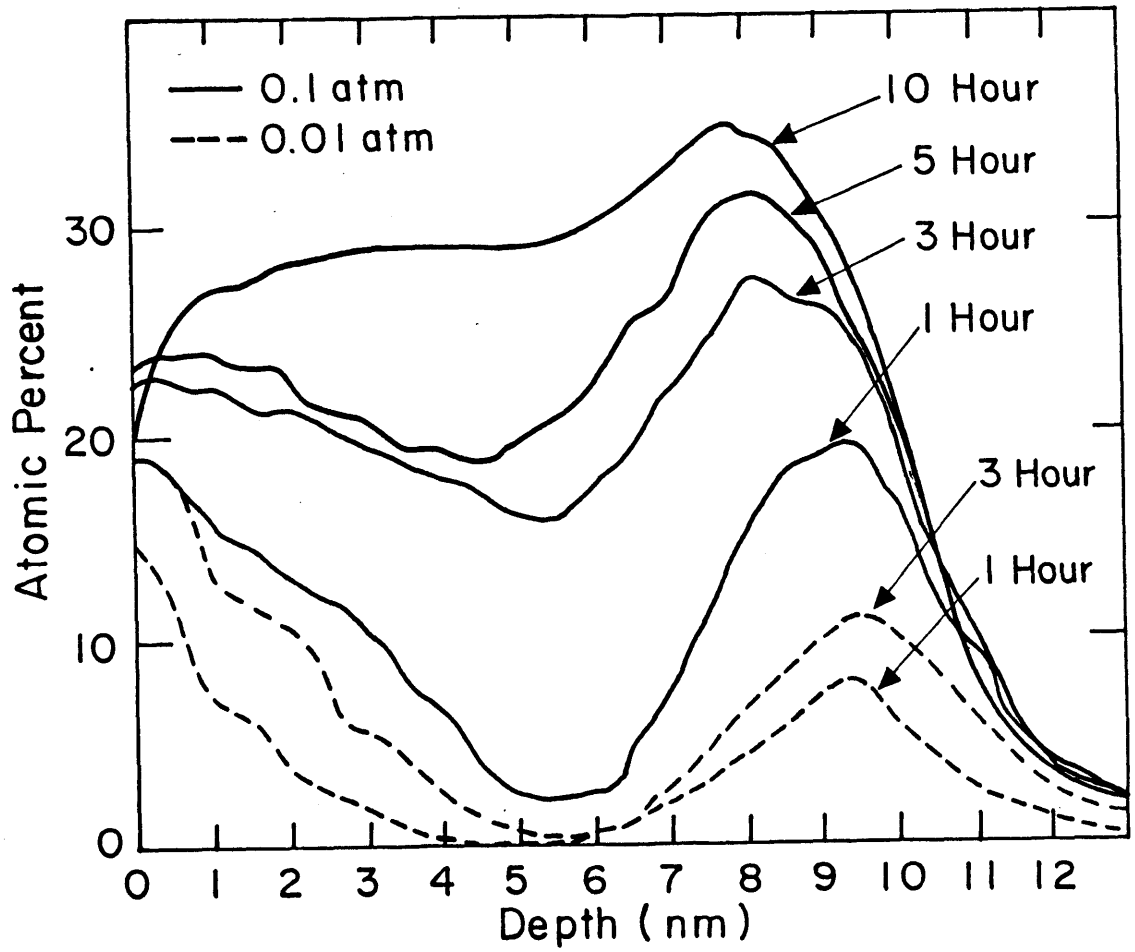

Figure 3.9: Effect of ammonia partial pressure and nitridation time on the incorporation of nitrogen during nitridation.

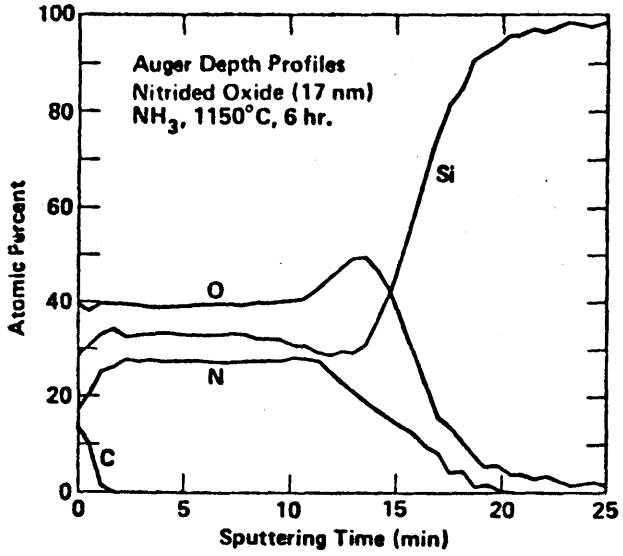

Figure 3.10: Data of Chang [31] showing the composition of a heavily nitrided oxide. The oxide was annealed in ammonia at 1150 °C for 6 h.

the oxide film, a competition exists between nitriding species and oxidizing species. While the nitridation of the surface occurs, the OH_y by-products can easily escape from the dielectric as long as the diffusion-limiting nitride-like layer is not completely formed. Simultaneously, the interface region is nitrided, with OH_y groups being consumed in the oxidation reaction of the underlying silicon. After a short time, the reactions at the surface and at the interface are slowed down as a result of the formation of diffusion barriers. At this time the nitridation of the bulk has not proceeded very far since the escape of OH_y species from the bulk is more difficult. Incorporation of nitrogen into the bulk of the dielectric is limited by the out-diffusion of oxygen-containing by-products. It is also possible that some NH_x species and by-products may also become trapped within the film. Increasing nitridation temperature enhances the out-diffusion of OH_y and results in greater nitrogen incorporation as well reduced hydrogen to nitrogen (H/N) ratios in the film bulk [72].

Evidence for oxidation of the underlying silicon by oxygen-containing by-products during nitridation can be seen in the data of Chang [31]. They present a 17 nm film nitrided at 1150 °C for 6 hours, a very heavy nitridation condition, as shown in figure 3.10. It is interesting to note that the profile clearly shows an oxygen peak at the interface. Further evidence of oxygen-rich interfacial region is given by Vasquez [70] in an XPS (X-ray photoelectron spectroscopy) study and by Han [45] in an AES study. Our AES data was not optimized to detect the oxygen-rich region though its presence may be suggested by electrical measurements.

The incorporation of hydrogen, while implicit in the above discussion, has not been as extensively studied as the incorporation of nitrogen. The primary reason is the difficulty in detecting hydrogen. However, in the work of Habraken and Kuiper [71,72] hydrogen was detected by means of nuclear reaction analysis (NRA). The NRA technique depends on a resonant nuclear reaction between protons (hydrogen) in the sample and an incident $^{15}N^{++}$ beam. As shown in figure 3.11, the incident

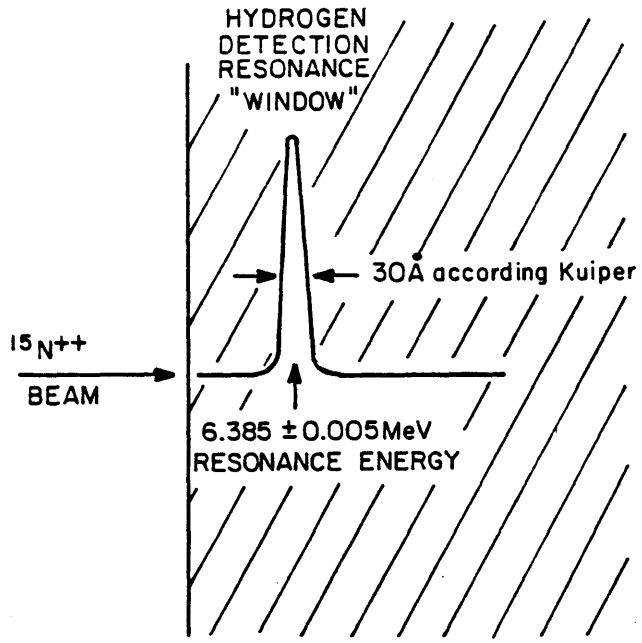

Figure 3.11: Nuclear reaction technique. The incident beam loses energy until it is at 6.385 MeV when a nuclear reaction occurs releasing a γ-ray which can calibrated to the amount of hydrogen. The width of the resonance window is estimated to be 30 $\AA$ [71].

beam enters the sample at an energy above 6.385 MeV. As it penetrates the material the beam loses energy until it is at 6.385 MeV. At this precise energy a nuclear reaction occurs yielding an α particle and a characteristic 4.43-MeV γ ray which can detected and calibrated to the amount of hydrogen in the sample [103]. Kuiper and Habraken studied the simultaneous incorporation of nitrogen and hydrogen in the temperature range of 800 - 1160 °C for ammonia pressures ranging from 1-10 atm. It was found that the distribution of hydrogen was nearly uniform throughout the dielectric unlike the non-uniform nitrogen distribution. However, the amount of hydrogen incorporated was related to the nitrogen content. The concentration of hydrogen varied from less 1 at. % to 10 at. % in the case of a 10 atm. nitridation.

The fact that nitrogen and hydrogen incorporation is somehow correlated favors a nitridation mechanism involving NH_x as the reactive species. They speculated that the hydrogen content of the more heavily nitrided interface and surface regions may be less as more nitrogen becomes trigonally bonded to silicon in these regions. Due to the resolution limit of the NRA technique to approximately 3nm, this could not be directly substantiated. However, etch-rate measurements (which should be sensitive to the hydrogen content of the film) suggested a reduced etch-rate for surface and interface regions [57,72]. It was also found that the number of hydrogen atoms incorporated per nitrogen atom incorporated (H/N ratio) decreased with increasing nitridation temperature and decreasing nitridation pressure. The reduced H/N ratio with lower nitridation pressure is explained by enhanced out-diffusion of OH_y by-products due to a more transparent diffusion barrier at the surface. The reduced H/N ratio with increasing temperature is believed to be due to enhanced out-diffusion of hydrogen-containing species at elevated temperatures.

Hydrogen is believed to be incorporated primarily as N-H into the dielectric. In the work of Pan [35], FTIR analysis indicated an increase in the concentration of N-H bonds. Si-OH bonds were not found to increase. The work of Ruggles, et. al. [74] generally supports this. Infrared spectroscopy was used to detect a large increase in the concentration of N-H groups. The concentration of O-H and Si-H groups were only slightly increased. This does not, however, rule out the presence of Si-H groups below the detection limit of the technique.

Wherever hydrogen is detected, the coordination of atoms is expected to deviate from that of a complete amorphous network characteristic of SiO_2 or Si_3N_4. As nitridation proceeds, however, the nitrogen atoms become more completely coordinated with silicon in the form of Si_3N_4 and/or Si_2N_2O [57] and the hydrogen content is reduced [72].

The reoxidation of a nitrided oxide film again effects the nitrogen and hydrogen content of the film. The most immediately apparent effect associated with reoxida-

tion is the observation that the interfacial nitrogen acts as a diffusion barrier which prevents oxidation of the substrate [25,42]. As reoxidation proceeds, nitrogen appears to be removed from the surface and then the bulk regions of the dielectric while leaving the interface nitrogen relatively intact [57] preventing the oxidation of the substrate. This is illustrated in the AES profile of figure 3.12. While reoxidation slowly removes the incorporated nitrogen in the surface and bulk of the dielectric leaving the interface intact, the electrical properties of the dielectric change dramatically and comparatively quickly as discussed in chapter 4. Sufficiently long reoxidations, however, eventually increase the film thickness [25,42].

The effect of reoxidation on the hydrogen content of nitrided oxides has received relatively scarce attention. In the work of Pan [101], it is shown by the NRA technique that the hydrogen content of nitrided oxide films is reduced upon reoxidation. However, the magnitude of the decrease and the time scale on which hydrogen is removed is not reported.

In contrast with previous work, we have concentrated on low pressure nitridations which are relatively light and subsequent reoxidations of these light nitridations. Typically, a 1 hour, 0.01 atm. nitridation at 950°C had $\leq$ 8 atomic % of interfacial nitrogen and a negligible amount of bulk nitrogen. While 0.1 atm. reoxidations up to 3 hours do not significantly change the interfacial nitrogen content or increase the dielectric thickness, reoxidation was found to significantly alter the electrical properties of nitrided oxides.

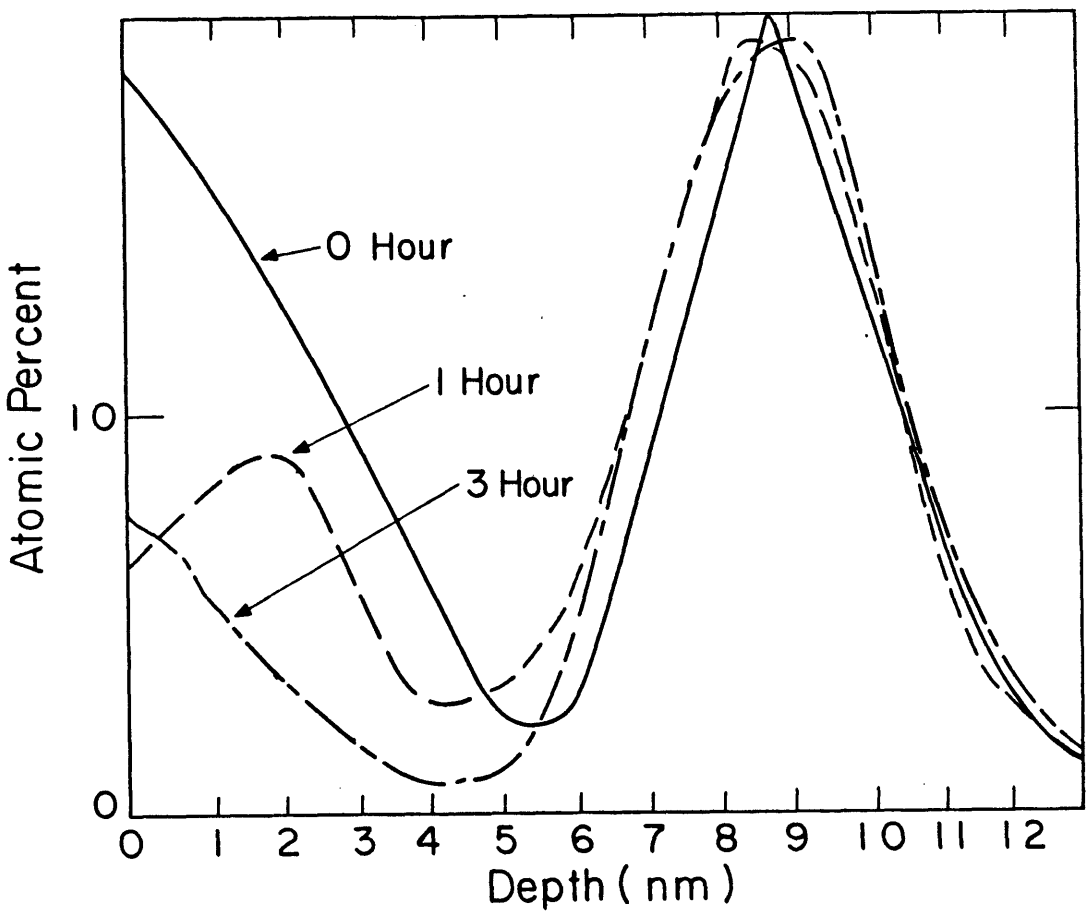

Figure 3.12: Effect of reoxidation on the nitrogen profile in the original nitrided oxide film.

Chapter 4

MOS Electrical Properties of the Nitridation/Reoxidation Process

4.1 Low pressure nitridation/reoxidation process

Various dielectrics were incorporated into field isolated, 100μm $\times$ 100μm, polysilicon gate MOS test capacitors for electrical characterization. The pre-stress fixed charge (Q_f) and midgap interface state density (D_{it}) were extracted from the high–frequency and quasi–static C–V measurements. Constant current stressing (CCS) was used for accelerated aging to study dielectric degradation under electrical stress. A constant current stress of 10 μA/cm^2 under positive gate bias and negative bias was used and the CCS was periodically interrupted to measure the generation of interface states at midgap (ΔD_{it}) and the trapped charge (ΔQ_f). In addition, the dielectric charge–to–breakdown (Q_{bd}) was measured at a constant current density of 10 mA/cm^2 under positive and negative gate bias. I–V measurements were used to determine the dielectric breakdown field (E_{bd}) and to study the dominant conduction mechanism at high electric fields. The measurement techniques are described in greater detail in section 3.3.

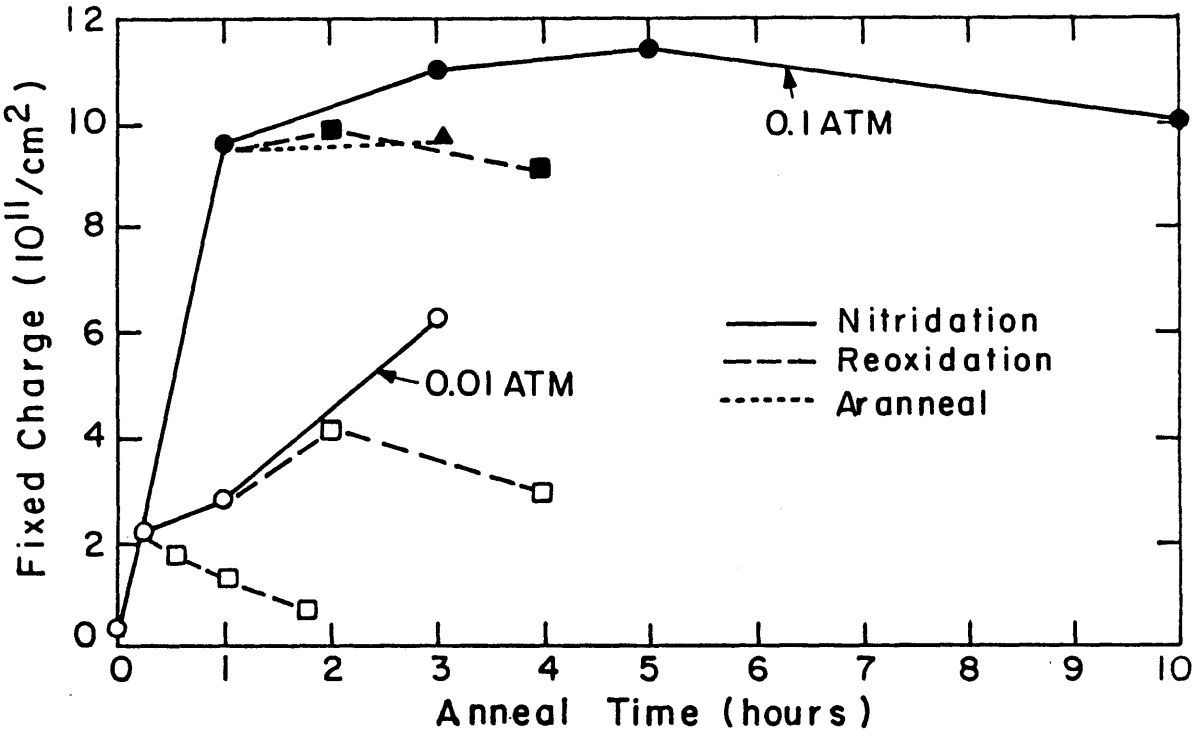

Figure 4.1: The fixed positive charge measured as a function of nitridation conditions. (●,○) data points represent nitrided oxides, (■,□) data points represent reoxidized nitrided oxides, and (▲) data points represent nitrided oxides that have undergone an inert anneal.

4.1.1 Fixed Charge

The fixed charge, Q_f, in the dielectric is reported as the effective charge at the substrate interface. As discussed in section 3.3.1, the accuracy of the flatband voltage measurement is ± 0.01 V, corresponding to an uncertainty of about $\pm 2 \times 10^{10}$ cm^{-2}. However, due to the uncertainty in the value of ϕ_{ms} of ± 0.06 V, the precise value of the fixed charge is uncertain to ± 10^{11} cm^{-2}.

Typically, our oxides had very little fixed charge, $\sim 5 \times 10^{10}$ cm^{-2}. Low pressure nitridation introduces fixed positive charge into the dielectric. In figure 4.1, the fixed positive charge is shown to increase with increasing nitridation time and pressure. With a sufficiently long nitridation (5 hour, 0.1 atm.), a maximum in the fixed

charge is reached at 1.1 $\times 10^{12}$ /cm^2. With heavier nitridations the fixed charge begins to decrease. This turnaround behavior in fixed positive charge has been reported extensively by other researchers [21,33,34,38,96]. The peak fixed charge reported in the literature ranges from 0.6 to 2.0 $\times 10^{12}$ /cm^2 depending on the initial oxide thickness, nitridation temperature, nitridation technique (i.e. atmospheric [21,34,38,37], rapid thermal [36,47], dilute [17], high pressure [42], and low pressure [88]), and post nitridation anneal [56]. In general, in the post-turnaround regime, lower fixed charge is associated with higher temperatures [21,96]. While low pressure nitridation at 0.1 atm., 950 °C requires approximately 5 hours before the fixed positive charge peaks and begins to decrease, atmospheric pressure nitridations of 10nm oxides turnaround more quickly and are reported to require only 10 and 30 minutes at 1000°C and 900°C, respectively [95,96]. A significant difference between our work and previous work is the attempt to optimize the electrical properties of the nitridation process in the pre-turnaround regime.

As shown in figure 4.1, an inert post-nitridation anneal at 0.1 atm Ar, 950°C did not alter the fixed charge significantly. Other workers [21,34] have observed a slight decrease ($\leq$ 10%) with sufficiently long inert anneals and have observed that continued nitridation appears to be more effective in reducing fixed charge than an inert thermal anneal in the post-turnaround regime.

The reoxidation of nitrided oxides was performed in 0.1 atm. oxygen at 950°C and did not significantly reduce the fixed positive charge (See Figure 4.1). Initially, reoxidation of heavily nitrided oxides marginally increases the fixed positive charge. Longer reoxidations or reoxidations of lightly nitrided oxides slightly reduce the fixed positive charge. We speculate that the continued increase in fixed charge during the initial stages of a reoxidation may due to a continued nitridation arising from trapped NH_x species in the dielectric [57] (See section 4.3).

We have concentrated on light nitridations to minimize the fixed positive charge in nitrided oxides and reoxidized nitrided oxides. In contrast, previous workers

have used heavy nitridations to exploit the turnaround in Q_f to minimize the fixed positive charge. In the post-turnaround regime, the minimum fixed charge appears to vary from 1.0-3.0$\times 10^{11}$ cm^{-2} depending on the nitridation condition [21,37,96].

4.1.2 Midgap Interface State Density

The midgap interface state density, D_{it}, is reported as an average over 50 meV around midgap. Typically our oxides had low interface state densities ($\sim 1 \times 10^{10}$ states/cm^{2}eV). Low pressure nitridation increases the midgap interface state density depending on the nitridation pressure and time until a maximum of 1.3 $\times 10^{11}$ states/cm^{2}eV is reached with a 5 hour, 0.1 atm. nitridation. Heavier nitridations eventually decrease the midgap interface state density. (See Figure 4.2). The turnaround behavior of D_{it} with nitridation closely tracks the behavior of Q_f. Similar results were reported by Hori, et. al. using rapid thermal nitridation [36]. Previous researchers have reported peaks in D_{it} ranging from 0.7 to 5.0 $\times 10^{11}$ cm^{-2} eV^{-1} depending on nitridation conditions with higher nitridation temperatures favoring a lower peak interface state density [34,36]. In the case of an atmospheric nitridation, a peak in the interface state density is reached at 30 minutes at 950 °C.

As shown in figure 4.2, an inert post-nitridation anneal at 0.1 atm Ar, 950 °C does not reduce the interface state density significantly. Other workers [34,56] have reported a slight decrease ($\leq 10\%$) for sufficiently long inert anneals.

The reoxidation of nitrided oxides did not reduce midgap interface state density significantly (See Figure 4.2). In fact, initial reoxidations of heavy nitrided oxides tend to increase D_{it} while longer reoxidations or reoxidations of lightly nitrided oxides slightly reduce the midgap interface state density. Note that the behavior of Q_f and D_{it} are closely correlated over the range of nitridation and reoxidation conditions studied.

Again, we have used the pre-turnaround regime to minimize interface state density. In the post-turnaround regime the minimum D_{it} values range from 1-3 $\times 10^{10}$

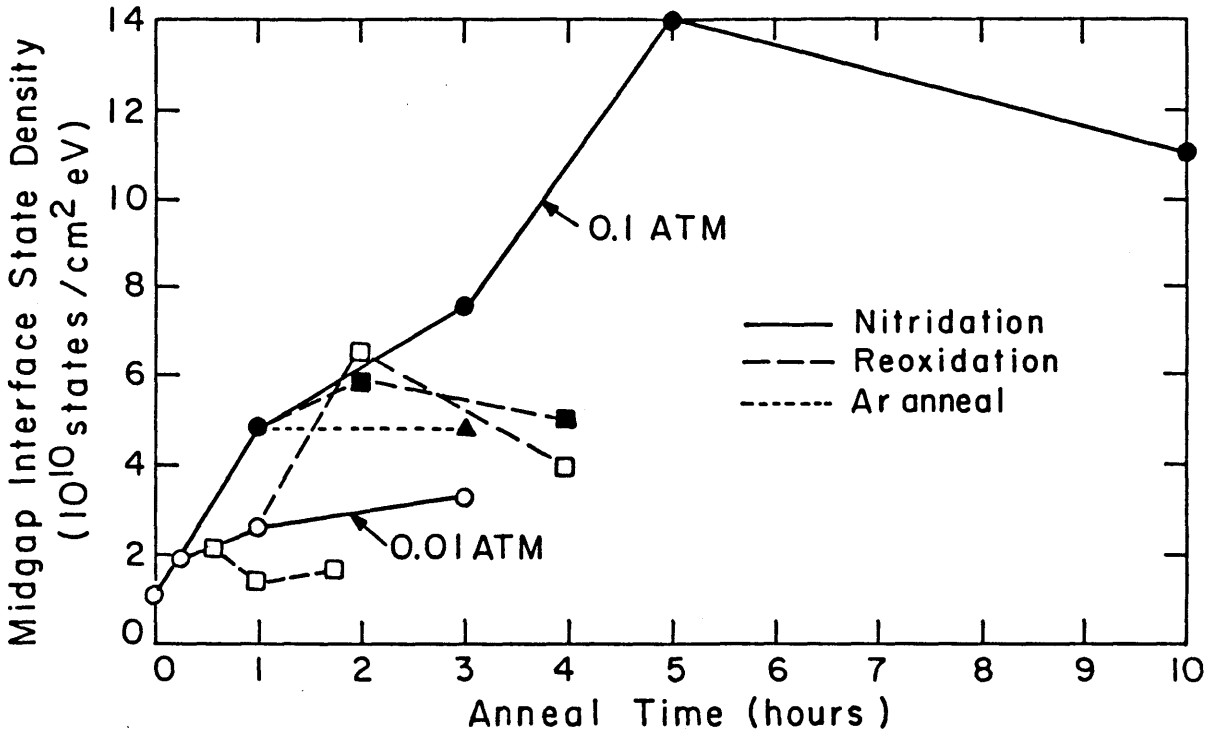

Figure 4.2: The midgap interface state density measured as a function of nitridation conditions. (●,○) data points represent nitrided oxides, (■,□) data points represent reoxidized nitrided oxides, and (▲) data points represent nitrided oxides that have undergone an inert anneal.

cm^{-2} eV^{-1} depending on the nitridation conditions with heavier nitridation generally leading to lower D_{it} [34,36,37].

4.1.3 Charge Trapping

MOS capacitors with various dielectrics were stressed at a constant current density of 10 $\mu A/cm^2$ under positive gate bias. The trapped charge, ΔQ_f, was measured as a flatband voltage shift for various fluence levels to $0.085 C/cm^2$ and is reported as the effective charge at the substrate interface. Oxide characteristically exhibited a very small negative flatband voltage shift corresponding to $\sim 4 \times 10^{10}$ $/cm^2$ positive charge trapping over the 8500 second CCS stress. In contrast, the flatband voltage shifts of nitrided oxides were positive indicating that electron trapping dominated. The amount of trapped charge versus fluence is shown for various nitrided oxides in Figure 4.3. Notice that lighter nitridations exhibit much less electron trapping compared with heavier nitridations. In figure 4.4, a maximum in the amount of electron trapping at a fluence level of $0.035 C/cm^2$ is found to be 2×10^{12} $/cm^2$ for a 3 hour, 0.1 atm. nitridation. Previously reported results on various nitrided oxides under various stress conditions [30,31,32,94] indicate that the electron trapping saturates between 2.0 to 6.0 $\times 10^{12}$ $/cm^2$. Notice that in figure 4.4, the ΔQ_f at a fluence of $0.035 C/cm^2$ increases, peaks with a 3 hour, 0.1 atm. nitridation, and decreases with heavier nitridations. A turnaround in electron trapping has not been previously reported. This may be due to the fact that in the post-turnaround regime, electron trapping remains very significant. Unlike fixed charge and interface state density, electron trapping does *not* return to oxide values in the limit of heavy nitridations [31].

As shown in figure 4.4, an inert post-nitridation anneal in 0.1 atm Ar does not significantly reduce electron trapping. Other researchers have reported that a high temperature atmospheric pressure inert anneal (at 1100 °C) is effective in reducing electron trapping by as much as 35 % [32].

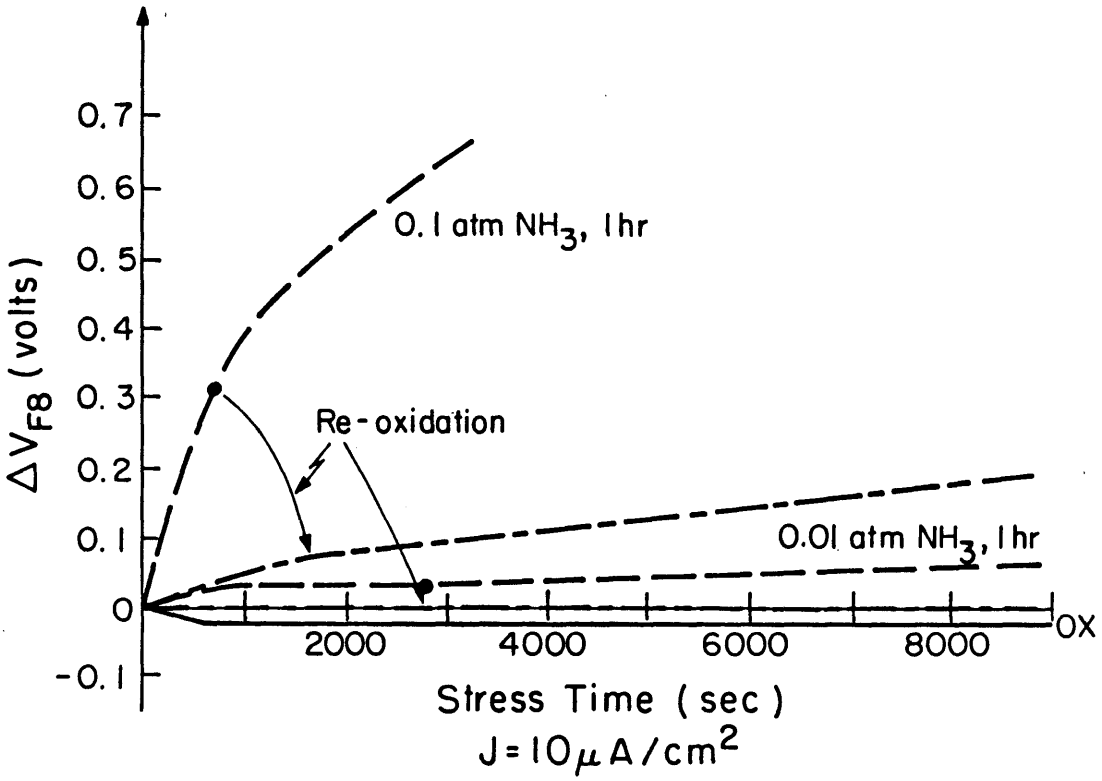

Figure 4.3: Charge trapping as evidenced by flatband voltage shifts during a constant current stress under positive gate conditions in nitrided oxides.

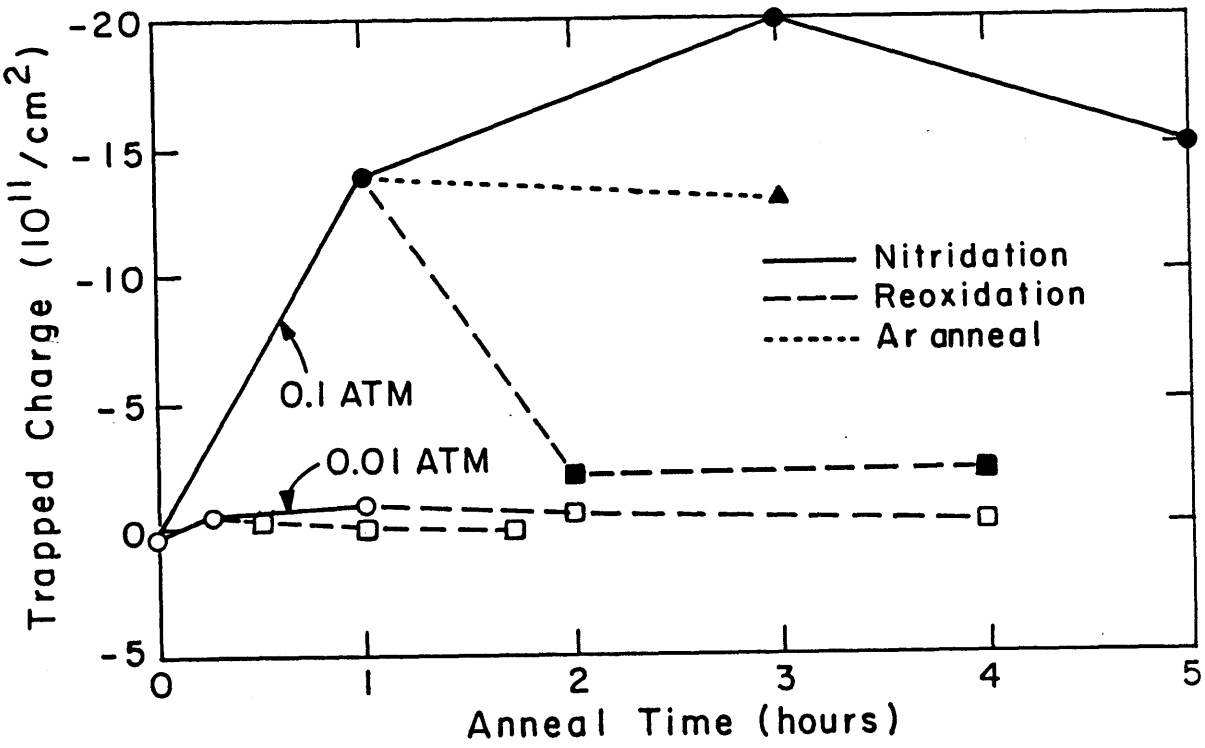

Figure 4.4: The amount of trapped charge at a fluence of 0.035C/cm^2 is plotted as a function of nitridation/reoxidation conditions. (●,○) data points represent nitrided oxides, (■,□) data points represent reoxidized nitrided oxides, and (▲) data points represent nitrided oxides that have undergone an inert anneal.

In agreement with previously reported results [14,37,40], reoxidation of nitrided oxide produces a dramatic reduction in electron trapping under electrical stress compared to the original nitrided oxide (See Figure 4.3 and 4.4). Charge trapping in the 0.01 atm. nitrided oxides can be essentially eliminated by reoxidation. Reoxidations of heavier nitridations appear to be less effective than reoxidations of lighter nitridations in reducing electron trapping. The similarity in the characteristics of the nitrided oxides after being reoxidized for a range of times indicates that the process window for achieving reduced electron trapping with reoxidation is quite large (See figure 4.4). However, excessive reoxidation of nitrided oxides increase the dielectric thickness and cause an increase in positive charge trapping under electrical stress which is characteristic of oxide.

For certain applications, constant current stressing under negative gate conditions is also important [48]. In this case, electrons are injected from the n^+ poly gate as opposed to the substrate. Due to the inferiority of the polysilicon-insulator interface relative to the single crystal-insulator interface, many capacitors, particularly those with nitrided oxide and oxide gate dielectrics, did not survive a negative gate stress. In figure 4.5, however, we see that reoxidized nitrided oxides are superior to oxides under negative gate stress.

4.1.4 Interface State Generation

The generated interface state density at midgap, ΔD_{it}, under positive gate constant current stress at 10 μA/cm^2 is shown for various dielectrics in figure 4.6. Our oxides have a interface state generation rate which is within 20% of that reported for oxide under similar CCS conditions by Liang, et. al. [90]. In contrast to previously reported results, we found that lightly nitrided oxides generate more interface states under electrical stress than oxide. However, heavily nitrided oxides eventually exhibit interface state generation below that of oxide in agreement with previous work using atmospheric, heavily nitrided oxides [14,23]. In figure 4.7, we

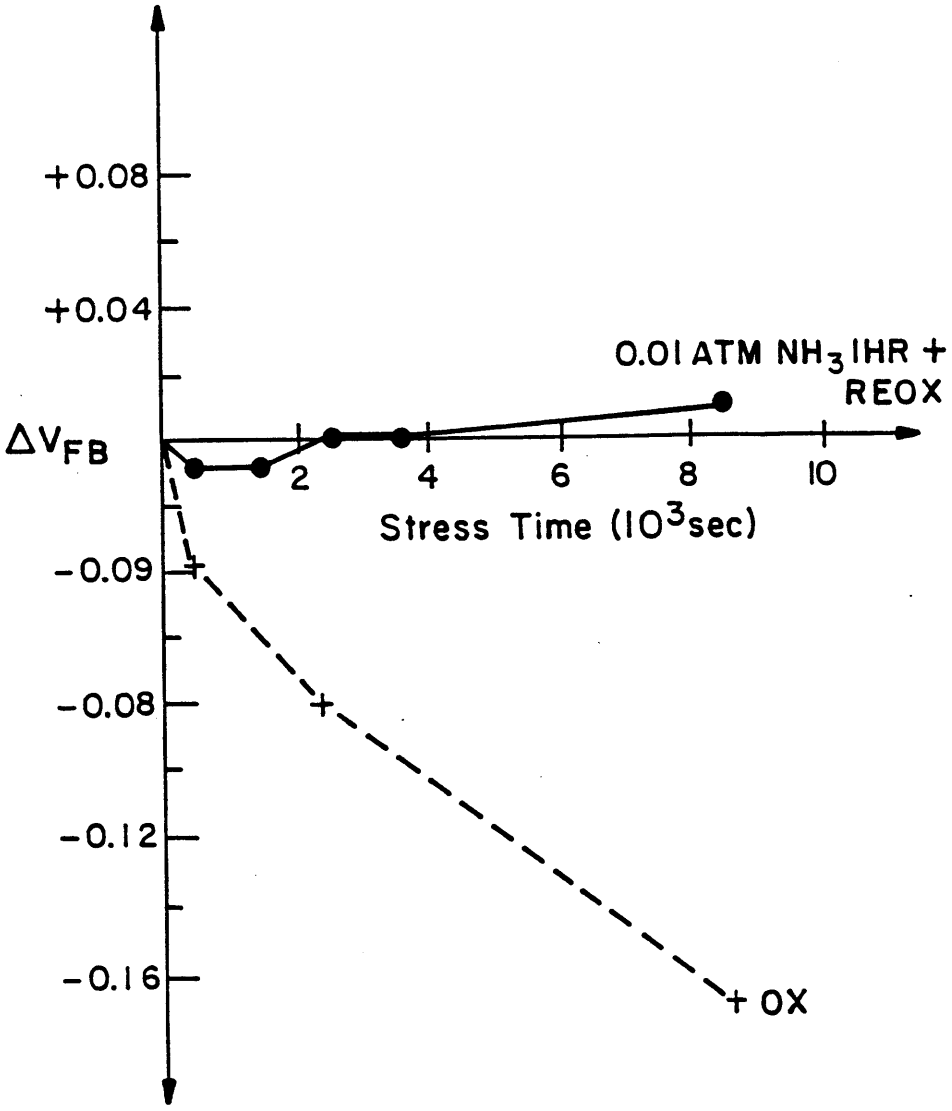

Figure 4.5: Comparison of the flatband voltage shifts in reoxidized nitrided oxide and control oxides under constant current stress for negative gate bias.

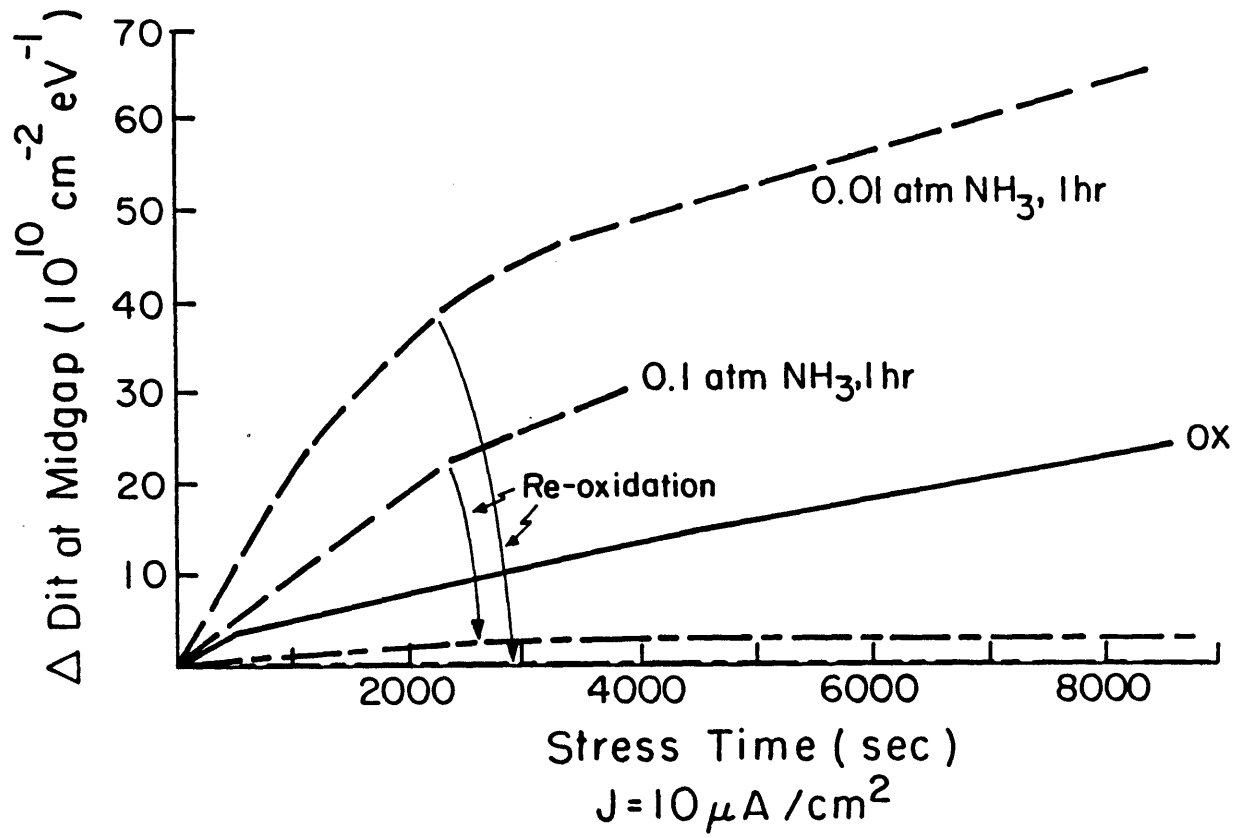

Figure 4.6: Interface state generation during a constant current stress under positive gate bias in nitrided oxides.

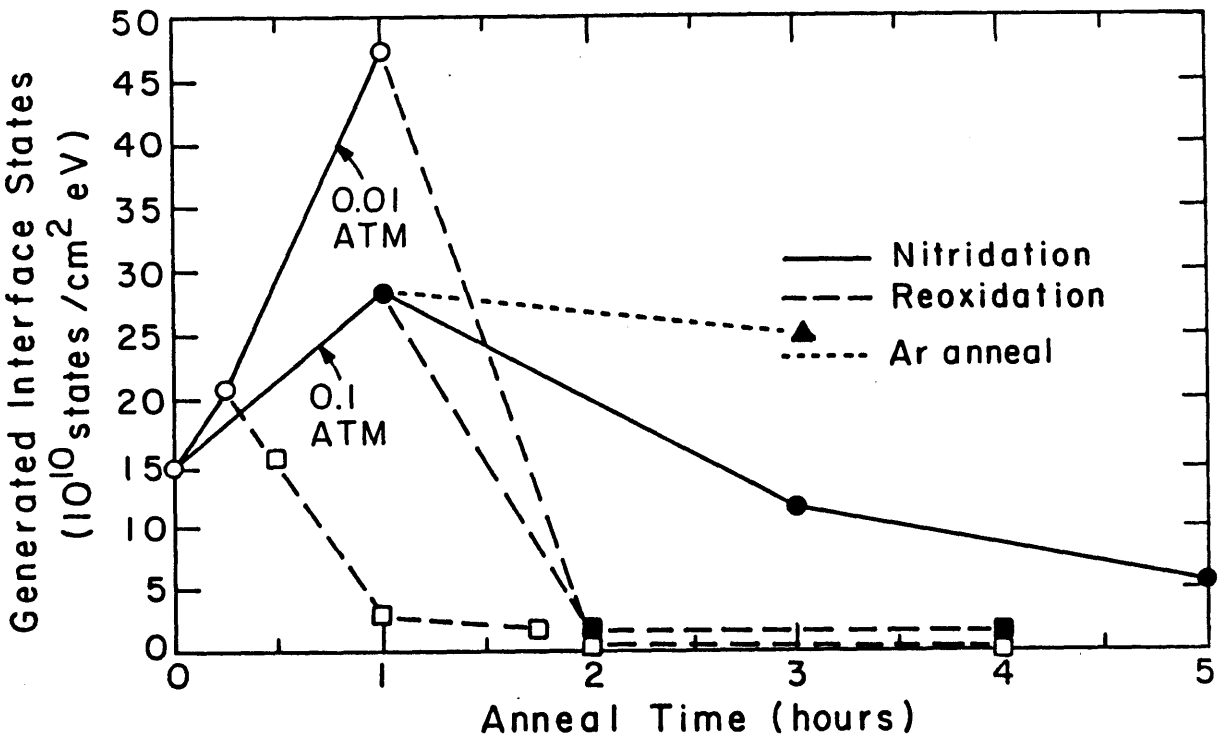

Figure 4.7: Interface state generation at a fluence of 0.035C/cm^2 is plotted as a function of nitridation/reoxidation conditions. (●,○) data points represent nitrided oxides, (■,□) data points represent reoxidized nitrided oxides, and (▲) data points represent nitrided oxides that have undergone an inert anneal.

observed that ΔD_{it} at fluence level of 0.035C/cm^2 exhibits a turnaround with nitridation with a peak at a 1 hour, 0.01 atm. nitridation and decreases for heavier nitridations (increasing nitridation time and pressure). A turnaround in ΔD_{it} has not been specifically reported though it can be seen in the data of [37,88]. In the data of Terry, a light nitridation at 800 °C exhibits greater ΔD_{it} than oxide. In the most recent data of Hori [102] 950 °C rapid thermal nitridations also exhibit a greater ΔD_{it} than oxide in agreement with our results.

As shown in figure 4.7, an inert post-nitridation anneal at 0.1 atm Ar does not significantly reduce ΔD_{it}. Thus continued nitridations are more effective in reducing ΔD_{it} than an inert thermal anneal.

The reoxidation of nitrided oxide dramatically reduces the generation of interface states under constant current stress particularly in lightly nitrided oxides. The improvement is by as much as two orders of magnitude (See Figure 4.6 and 4.7). Reoxidation is much more effective in reducing the interface state generation than increasing nitridation. Reoxidation of heavily nitrided oxides appear to have a diminishing effect on interface state generation. Notice that the reoxidations of the 1 hour, 0.01 atm. nitrided oxide exhibited the lowest generation of interface states under CCS. Similar to the reduced electron trapping effect, the process window for achieving the reduced interface state generation is quite large as can be seen by the similar characteristics of the nitrided oxides after various reoxidations. A reduction in ΔD_{it} due to reoxidation has not been specifically reported though it can be seen in the data of Wong [88]. Recently, Hori [102] has reproduced the above effect using rapid thermal nitridation and reoxidation.

Under negative gate constant current stressing, the generation of interface states in reoxidized nitrided oxides is much less than in oxides as shown in figure 4.8.

4.1.5 Current–Voltage

The positive gate bias I–V characteristics of a reoxidized nitrided oxide (3 hour, 0.1 atm. reoxidation of a 1 hour, 0.01 atm. nitrided oxide) and of an oxide are shown in Figure 4.9. Both the reoxidized nitrided oxide and oxide exhibit reproducible I–V characteristics with little charge trapping. In contrast, nitrided oxide I–V measurements irreversibly shift after each measurement due to significant electron trapping. A good fit to the experimental data was obtained with both oxide and reoxidized nitrided oxide by using the Fowler–Nordheim tunneling current model [60]. In addition, the critical breakdown field, E_{bd} of oxide was found to be $\sim$ 12 MV/cm while the E_{bd} of the reoxidized nitrided oxide was slightly higher at $\sim$ 14 MV/cm under positive gate conditions.

Under negative gate conditions, the critical breakdown field, E_{bd}, of oxide varied

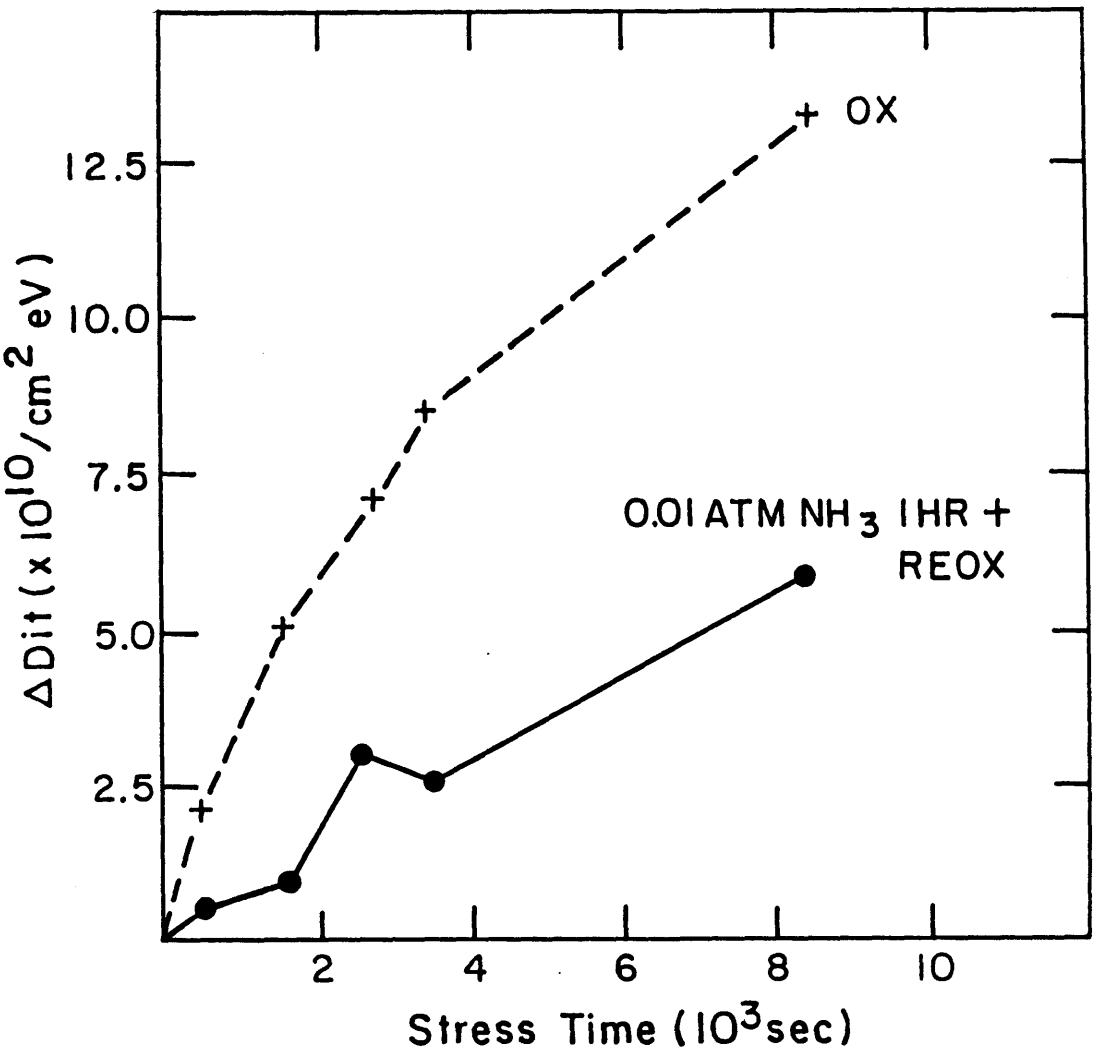

Figure 4.8: Comparison of interface state generation in reoxidized nitrided oxides and control oxides under negative gate constant current stress conditions.

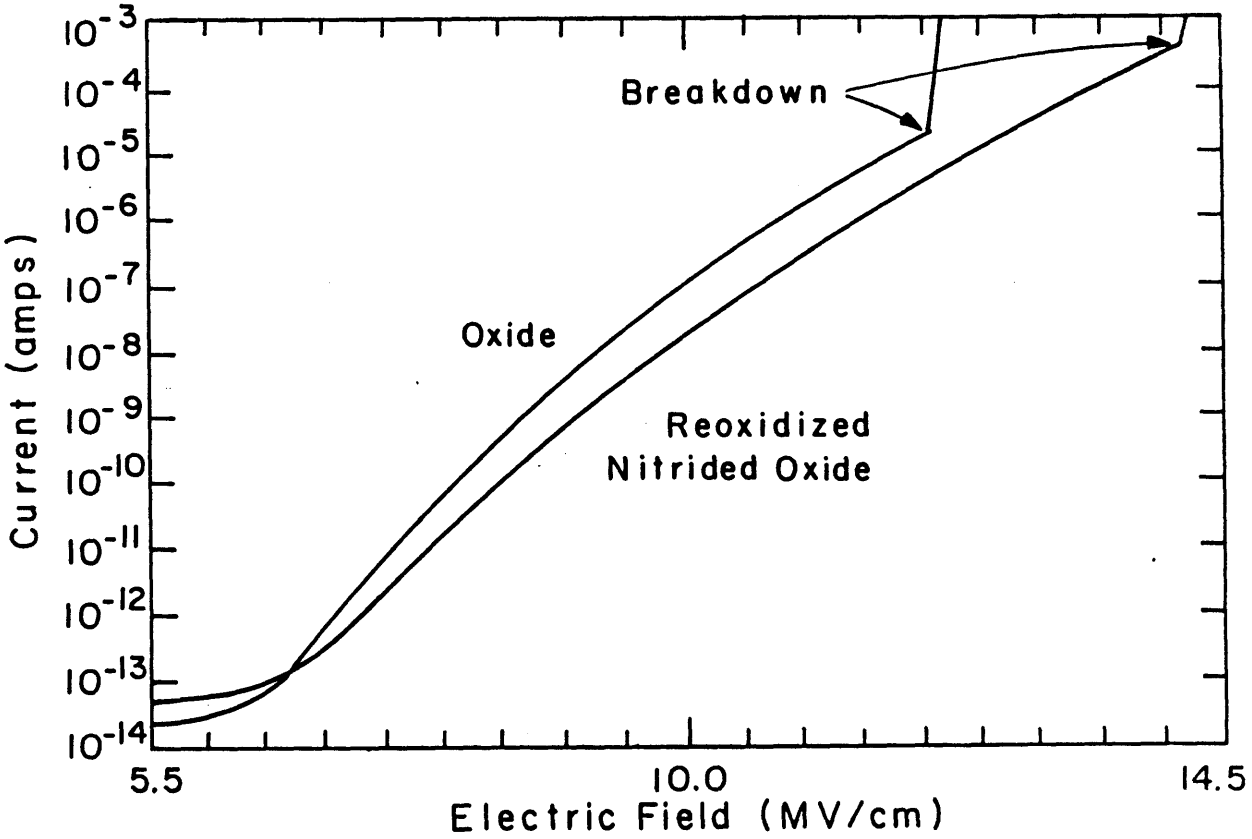

Figure 4.9: The positive gate bias I–V characteristics of a reoxidized nitrided oxide (3 hour, 0.1 atm. reoxidation of a 1 hour, 0.01 atm. nitrided oxide) and of an oxide.

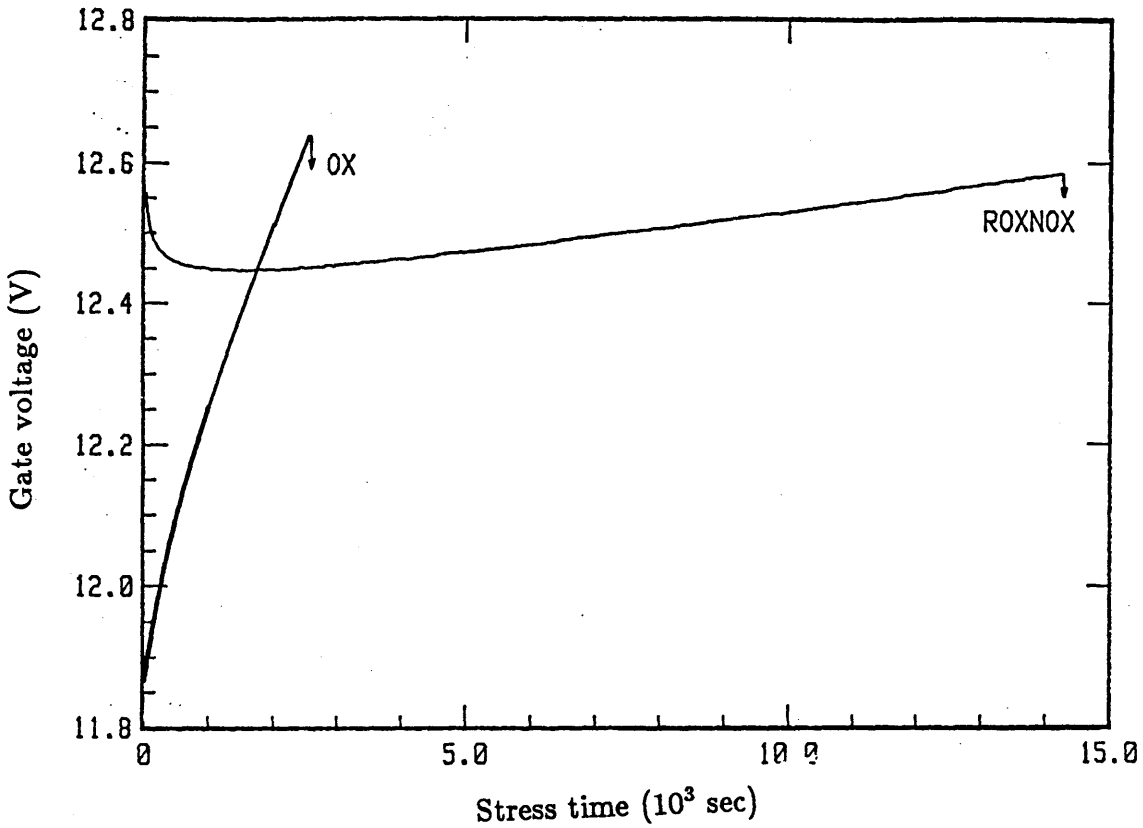

Figure 4.10: Comparison of charge-to-breakdown under constant current stress in reoxidized nitrided oxides and control oxides.

from 7-8 MV/cm while the E_{bd} of the reoxidized nitrided oxide varied from 8-10 MV/cm.

4.1.6 Charge–to–Breakdown

The charge–to–breakdown, Q_{bd}, of reoxidized nitrided oxides was measured by passing a constant current density of 10 mA/cm^2 (positive gate bias) through the dielectric until destructive dielectric breakdown. Our oxide was found to have a Q_{bd} comparable to the data presented by Chen, et. al. [59] Reoxidized nitrided oxides have a much larger charge–to–breakdown, Q_{bd}, compared to oxide. A typical Q_{bd} of 140 C/cm^2 was obtained with a 3 hour, 0.1 atm. reoxidation of a 1 hour, 0.01 atm. nitrided oxide. See figure 4.10.

In table 4.1, the Q_{bd} of various dielectrics is summarized for positive and negative

Nitridation of 12 nm Oxide	Reoxidation at 0.1 atm.	Positive Gate Q_{bd} (C/cm^2)	Negative Gate Q_{bd} (C/cm^2)
0.1 atm., 1 Hour	3 Hour	100	
0.01 atm., 1 Hour	3 Hour	140	18
0.01 atm., 15 Min	15 Min	40	
0.01 atm., 15 Min	45 Min	130	
0.01 atm., 15 Min	90 Min	60	
Oxide		20	1

Table 4.1: Charge–to–breakdown of reoxidized nitrided oxides at 10 mA/cm^2.

gate stresses. In general, Q_{bd} for reoxidized nitrided oxides are superior to that of oxides. Recently, Hori [102] has reported a Q_{bd} of 350 C/cm^2 for 8 nm dielectrics formed with rapid thermal nitridation and reoxidation.

4.2 Optimization of the nitridation/reoxidation process

In the previous section, the effect of nitridation/reoxidation conditions on a given electrical parameter was discussed independently of the behavior of other electrical parameters. In optimizing the process for use in scaled transistors we need to consider various parameters simultaneously. In general, optimization involves numerous electrical parameters including fixed charge, interface state density, charge trapping, interface state generation, charge-to-breakdown, breakdown

field, and low-field leakage. Additional considerations include defect density and yield, dopant masking properties, and thermal budget required to form the dielectric. In order to make the optimization problem tractable we limit the variables to just four electrical parameters: fixed charge (Q_f), interface state density (D_{it}), electron trapping under CCS (ΔQ_f), and interface state generation under CCS (ΔD_{it}). Note that fixed positive charge and interface states are parameters that relate primarily to device performance in that they affect inversion layer mobility, device transconductance, and noise. Interface state generation and electron trapping are parameters that relate primarily to device reliability since they represent a change in device characteristics.

Dielectric optimization involves identifying the nitridation/reoxidation conditions (time and pressure) which minimize the above process dependent electrical parameters. In general, this leads us to lighter nitridations (lower pressures and shorter times) which results in lower fixed positive charge, interface state density and electron trapping. In addition, nitridations coupled with reoxidations eliminate the remaining electron traps and result in improved suppression of interface state generation. The constraint to arbitrarily light nitridations in this process is the eventual loss of ΔD_{it} suppression. These ideas are illustrated in the series of Figures 4.11a-d which show the dependence of the various electrical parameters on the nitridation/reoxidation conditions.

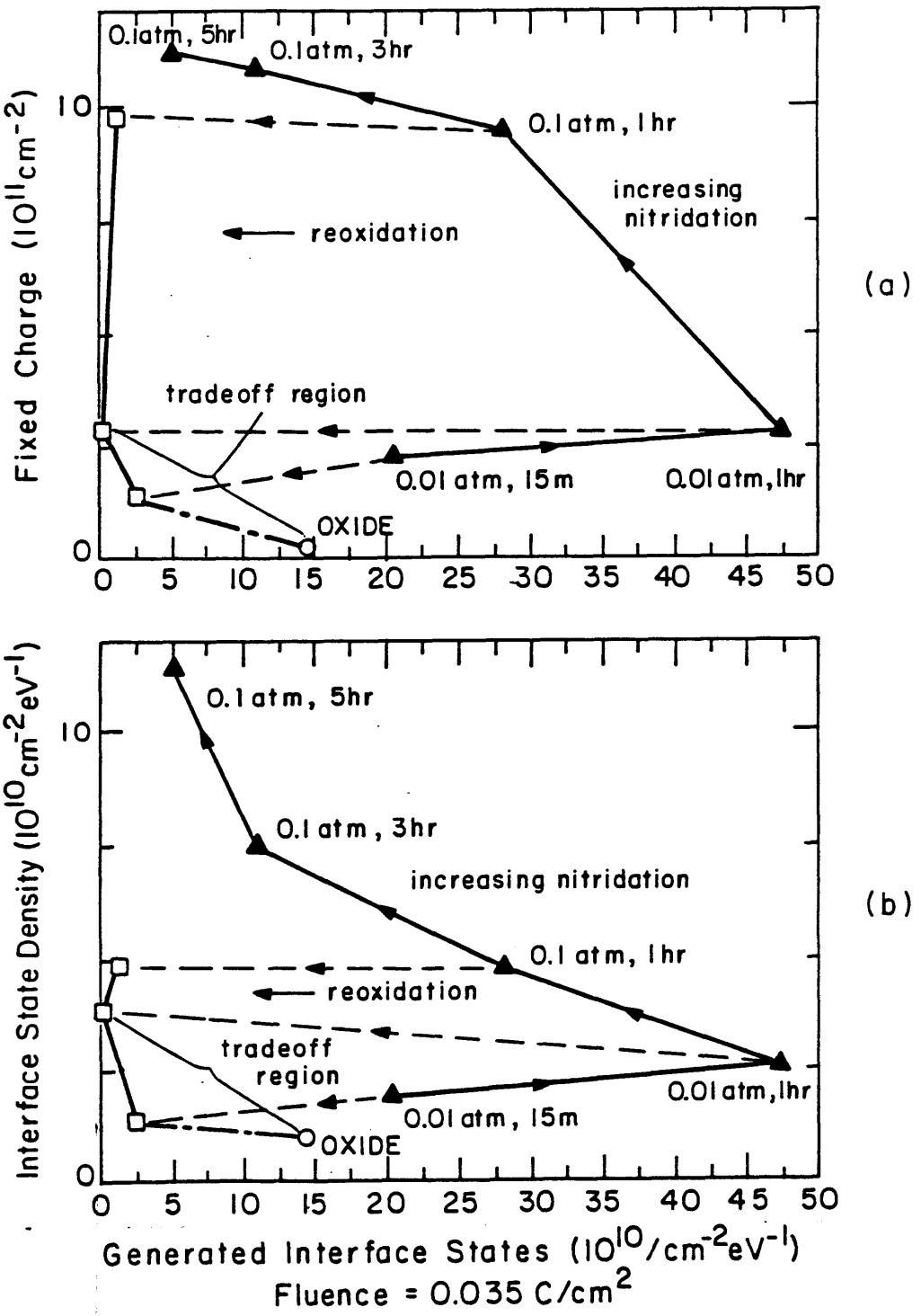

Figure 4.11: (a) Fixed charge plotted against observed interface state generation. (b) Interface state density plotted against observed interface state generation. Nitrided oxides are indicated by (▲), reoxidized nitrided oxides by (□), and oxides by (○).

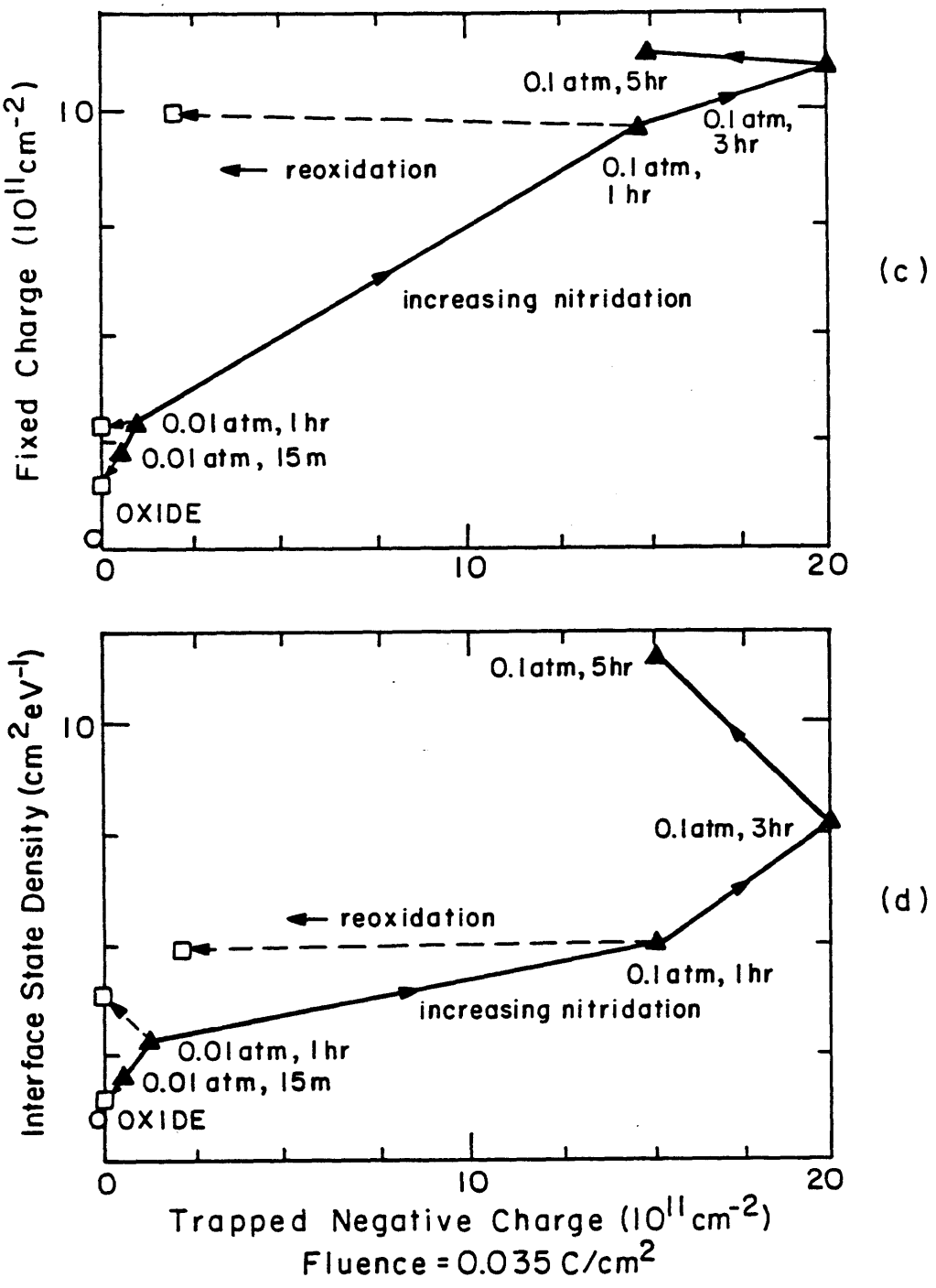

Figure 4.11: (c) Fixed charge plotted against observed charge trapping. (d) Interface state density plotted against observed charge trapping. Nitrided oxides are indicated by (▲), reoxidized nitrided oxides by (□), and oxides by (○).

In these figures, fixed positive charge and interface state density are each plotted against generated interface states,ΔD_{it}, and trapped electrons, ΔQ_f, for a given level of stress. Process conditions yielding points near the origin are optimal. In each plot, the effect of various nitridation conditions are represented by a curve which identifies the relationship between a given pair of performance-reliability parameters. The effect of reoxidation is the translation of the nitridation curve to a more favorable curve closer to the vertical axis. The primary advantage of reoxidation is improved reliability. In each plot the maximum reliability occurs at the following condition: 1 hour, 0.01 atm. nitridation combined with a reoxidation. Moving towards heavier nitridations is not desirable because of increased fixed positive charge, interface state density, electron trapping, and interface state generation. Moving towards lighter nitridations results in the virtual elimination of electron trapping and in a tradeoff between Q_f and ΔD_{it} and in a tradeoff between D_{it} and ΔD_{it}. The tradeoff region spans the region from the point of maximum reliability through points of successively lighter nitridations to the limit of zero nitridation corresponding to the case of silicon dioxide. Since the behavior of fixed positive charge and interface state density closely track under nitridation and reoxidation, the minimization of one parameter generally optimizes the other. The nitridation/reoxidation condition which produces the best reliability has the following characteristics: the interfacial nitrogen content of the dielectric is $\sim$ 8 at.%, the fixed charge is $\sim 2.5 \times 10^{11} cm^{-2}$, the interface state density is $\sim 3.0 \times 10^{10} cm^{-2} eV^{-1}$, charge trapping is virtually eliminated, and interface state generation is a factor of 25 less than in silicon dioxide. Lighter nitridations allow even lower fixed charge and interface state density but less improvement in reliability.

4.3 Discussion

A. Nitridation/reoxidation process

Nitridation degrades the pre-stress electrical properties of oxide by increasing the fixed positive charge and interface state density. Under electrical stress, lightly nitrided oxides also exhibit increased interface state generation and electron trapping compared to oxide. With heavier nitridation, the positive fixed charge (Q_f), midgap interface state density (D_{it}), electron trapping (ΔQ_f) under CCS, and interface state generation (ΔD_{it}) under CCS all increase, peak, and subsequently decrease (turnaround). Continued thermal nitridations seem to be more effective in achieving these turnarounds than an inert thermal anneal, particularly in the case of Q_f, D_{it}, and ΔD_{it} [56]. In the post-turnaround regime, fixed charge and interface state density approach oxide values in the limit of heavy nitridations. The generation of interface states is radically suppressed by at least an order of magnitude compared to silicon oxide. Electron trapping, however, remains significant and much worse than oxide in this regime. It should be noted that other researchers have reported that the amount of electron trapping increases monotonically with increasing nitridation and does not turnaround [30,102].

In our data, the interface state generation under CCS exhibits the earliest turnaround and peaks with a 1 hour, 0.01 atm. nitridation. The electron trapping under CCS exhibits the next turnaround and peaks with a 3 hour, 0.1 atm. nitrided oxide. The fixed positive charge and interface state density closely track in agreement with recently reported results [36] and exhibit respective peaks at a 5 hour, 0.1 atm. nitridation.

The observed turnarounds in $Q_f, D_{it}, \Delta Q_f$, and ΔD_{it} suggest a defect formation mechanism associated with the incorporation of nitrogen or hydrogen and an annealing process which reduces defects with continued nitridation. It is unlikely that a simple thermal anneal is responsible for defect reduction particularly in the case of Q_f, D_{it}, and ΔD_{it} since continued nitridation is more effective than an inert thermal anneal in reducing these defects. A possible defect annealing mechanism may be associated with the formation of a thin, interfacial oxygen rich layer

which is observed with continued nitridation and is attributed to the reaction of oxygen-containing byproducts of nitridation process at the substrate [45,93].

The reoxidation of nitrided oxides initially increases the fixed positive charge and interface state density. This may be attributed to a continued nitridation reaction arising from nitrogen-containing byproducts of the reoxidation process released from the surface and bulk regions that react at the interface and continue to form more fixed positive charge and interface states. A continued nitridation reaction might also be due to residual unreacted nitrogen-containing species which remain within the dielectric when the nitridation process is discontinued [57]. We have observed this effect only in nitrided oxides with surface and bulk nitrogen content greater than 8 at. %. The eventual decrease in Q_f and D_{it} with continued reoxidation may be the result of interface reoxidation analogous to the reoxidation that occurs for heavier nitridations. Reoxidation is more effective in reducing fixed charge and interface state density than an inert thermal anneal [56]. Excessive reoxidation of nitrided oxides results in an eventual increase in insulator thickness and electrical properties characteristic of oxide such as positive charge trapping under electrical stress and lower Q_{bd}.

B. Speculative models of reliability improvement

The most dramatic effects associated with reoxidation are reduced electron trapping relative to nitrided oxide and significantly decreased generation of interface states relative to thermal oxide. Consider electron trapping. It is unlikely that electron trapping is solely associated with the nitrogen content of the dielectric, since the nitrogen content of the dielectric is not significantly altered by reoxidation whereas electron trapping is dramatically reduced even for slight reoxidations. See figure 4.4. It has been suggested that electron traps may be associated with O-H bonds introduced by nitridation [30]. This speculation was motivated by research in silicon dioxide which showed a correlation between the presence of O-H bonds and electron traps [77,89]. The capture cross-section of such traps was estimated to

$10^{-17}cm^2$ in oxides in agreement with capture cross-sections found in nitrided oxide [30]. More recent work has shown that capture cross-sections in nitrided oxides may be closer to $10^{-14}cm^2$ [31] or $10^{-15}cm^2$ [32]. Moreover, FTIR measurements detect a greater number of N-H bonds in nitrided oxides than O-H bonds [35,74]. While this suggests that electron traps may not be water-related, they nevertheless may be related to the presence of hydrogen since nitridation is known to introduce hydrogen [35,72] whereas reoxidation is known to remove hydrogen [101]. Furthermore, high temperature (1100 °C) inert anneals have been shown to somewhat reduce electron traps [30,32] which may also remove hydrogen. Direct evidence for the removal of hydrogen due to an inert thermal anneal has not been provided yet.

The property of suppression of interface state generation is arguably the most advantageous property of nitrided oxides and reoxidized nitrided oxides. A plausible model of the suppression of interface state generation must explain the following observations:

(1) Thermal silicon dioxide readily generates interface states.

(2) Lightly nitrided oxides actually generate more interface states than oxide.

(3) Heavier nitridations eventually result in less interface state generation than oxides.

(4) The reoxidation of lightly nitrided oxide greatly reduces interface state generation compared to oxide. The reoxidation of heavier nitridations have a diminishing effect on the suppression of interface state generation.

There are two possible models which have been used to explain interface state generation in thermal silicon dioxide which might be applied to nitrided oxides.

In the first model, interface state generation in oxides is associated with interfacial stress in this Si-SiO_2 system. This model has been lent credence through the measurement of interface state generation under ionizing radiation as a function of intentionally introduced interfacial stress [91]. In the work of Ma, it is shown that interface state generation is suppressed when the underlying silicon surface

is placed under compression. In applying this model to nitrided oxides one might argue that the process of nitridation results in the densification of the insulator as the interface incorporates more nitrogen and as SiO_2 tends towards Si_3N_4. Since thermally grown oxide is compressive, as nitridation continues one might expect that the interfacial region of the oxide to grow less compressive and tend towards tensile stress characteristic of silicon nitride. This model, however, is difficult to reconcile with the observation that ΔD_{it} exhibits a turnaround whereas the model suggests a monotonic improvement in ΔD_{it} with nitridation. Moreover, it is inconsistent with the observation that a reoxidation of lightly nitrided oxides greatly suppresses ΔD_{it} despite the fact that the interfacial nitrogen content is not altered by reoxidation.

In the second model, interface state generation in oxides is associated with weak hydrogenated bonds at the interface which are broken by energetic electrons during electrical stress [6,78,92]. For example, one can write the following reaction

$$SiH + e^- \leftrightarrow Si^* + H_i \tag{4.1}$$

where S^* is a trivalent silicon atom (i.e., interface trap) and H_i is an interstitial hydrogen atom.

For short stress times, the model predicts that interface state generation is a reaction-rate limited process proportional to the concentration of hydrogenated bonds. We can then explain the turnaround behavior of ΔD_{it} by postulating a turnaround in the interface concentration of hydrogenated bonds as nitridation proceeds. Thus in the initial stages of the nitridation process, nitrogen and hydrogen is incorporated into the interface region resulting in a concentration of hydrogenated bonds which is much larger than in silicon dioxide. Thus interface state generation is enhanced for light nitridations. As nitridation proceeds the interfacial hydrogen concentration is reduced by two possible means: a) the incorporation of more nitrogen results in greater proportion of strong bonds as nitrogen becomes trigonally

bonded to silicon replacing weak hydrogenated bonds or b) interface reoxidation by oxygen-containing byproducts replaces weak hydrogenated bonds. In either case, the hydrogen concentration must be reduced below oxide levels to account for the suppression of interface state generation for heavy nitridations. Unfortunately, the measurement of the hydrogen content of the interface is limited by the depth resolution of the NRA technique [103]. To explain observation 4) above we recall that the interfacial nitrogen layer greatly hinders the diffusion of oxygen to the substrate suppressing further silicon oxidation to the extent that an interfacial oxide layer has not been observed. Nevertheless a small amount of oxygen may react with hydrogenated bonds thereby reducing the interface hydrogen concentration . Recall that reoxidation is known to remove hydrogen at least from the bulk of the nitrided oxide [101]. Moreover the amount of oxygen required for such a purpose is less than a monolayer since the number of generated interface states is $\sim 10^{12}$ cm^{-2} compared to a Si surface bond density of $\sim 10^{15}$ cm^{-2}.

4.4 Radiation effects

The results reported in this section were obtained in collaboration with Gregg Dunn of Lincoln Laboratories who performed radiation and C–V measurements on our samples. The results were submitted to Applied Physics Letters [79]. Appropriate sections are reproduced below.

The nitridation of silicon dioxide has been known to result in improved radiation resistance [16,17,21,22]. A general conclusion of the radiation studies has been that the heaviest nitridations (high temperatures, long times) produce the most radiation-resistant dielectrics [17,21,80]. A high temperature-time product is undesirable in device processing because this can result in unwanted dopant redistribution and wafer warpage. Sundaresan et. al. [22] have addressed this problem by employing rapid thermal nitridation. Here we show that light, low pressure

nitridations coupled with a reoxidation can be used to achieve radiation hardness.

For radiation experiments, a control oxide and two reoxidized nitrided oxide devices were investigated. Lot A refers to a 7.6 torr, 1 hour nitridation followed by a 76 torr, 3 hour reoxidation; lot B refers to a 7.6 torr, 15 minute nitridation followed by a 76 torr, 45 minute reoxidation. The processing procedure and structure of the capacitors were identical to those used in the above electrical measurements. The area of capacitors was 300 μm $\times$ 300 μm.

Capacitance-voltage measurements of the devices were performed before and after irradiation. Capacitors were irradiated in an Aracor X-ray test system at a dose rate of 312 krad(Si)/min to total doses 1, 2, and 5 Mrad(Si). +1.35 V bias was applied to the gate during irradiation. After irradiation the devices were left floating for 24 hours before testing. Measurements of selected samples immediately after irradiation demonstrated that less than 10% rebound [81] occurred under these conditions. Rebound refers to the annealing of radiation-induced fixed charge. This annealing is enhanced by temperature and applied positive bias, and should be an important consideration in any radiation experiment, as the time and conditions between irradiation and test can strongly affect results.

Radiation-induced interface state build-up in the capacitors is plotted in figure 4.12. It can be seen that interface state density in Lot A devices is constant to within experimental accuracy ($\sim 1 \times 10^{10}$ cm^{-2} eV^{-1}), even after 5 Mrad. A moderate build-up occurs in Lot B devices, about 2×10^{10} cm^{-2} eV^{-1}. Substantial build-up occurs in the oxide, about 1.5×10^{11} cm^{-2} eV^{-1}. The increase appears to follow a $D^{0.65}$ dependence on dose, as reported by Winokur [82].

In order to assess fixed charge generation during irradiation, the midgap voltage shifts were measured. The midgap voltage is the voltage at which the quasi-Fermi is at the middle of the Si bandgap. Measurement of the midgap voltage shifts has become preferred to flatband voltage due to reduced effect of interface states at midgap. Midgap voltage shifts for the capacitors are plotted in figure 4.13.

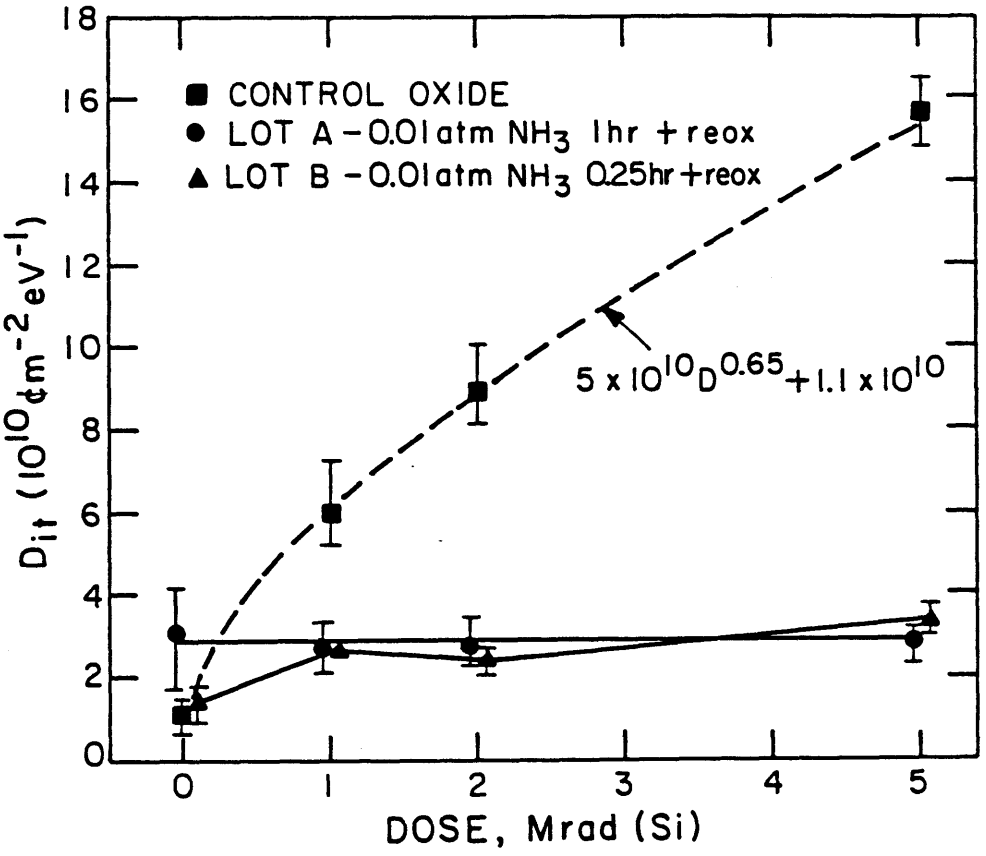

Figure 4.12: Radiation-induced interface state build-up in various dielectrics.

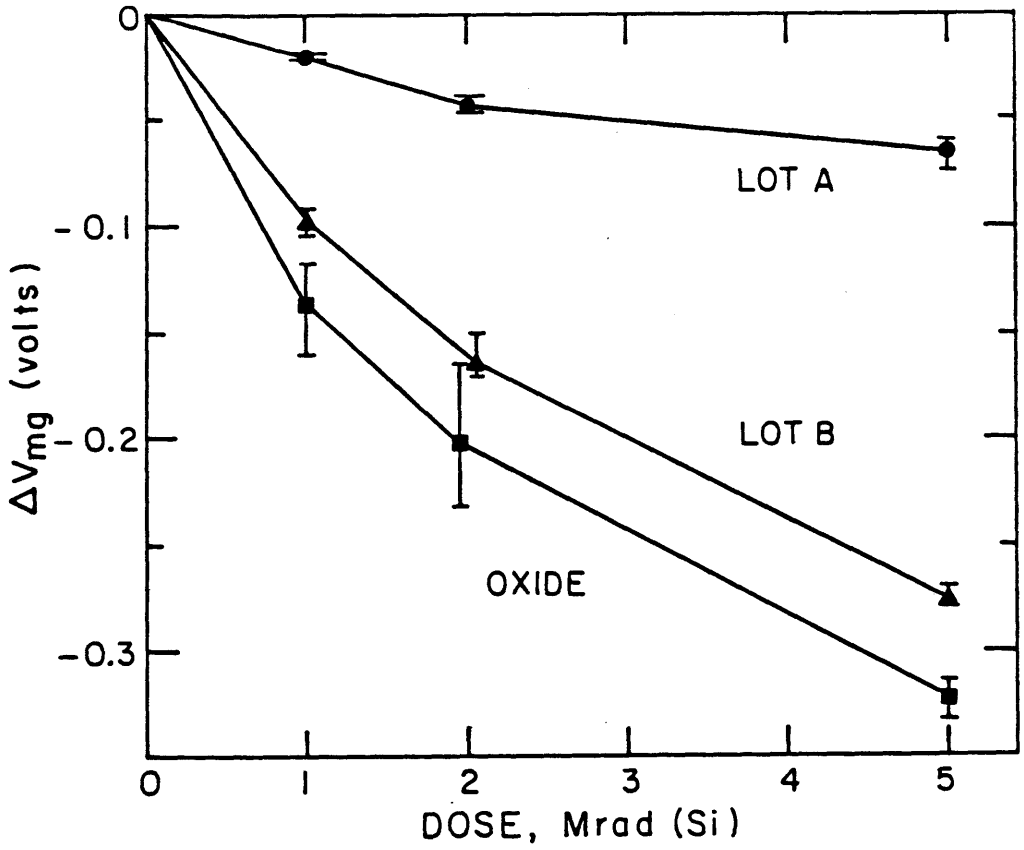

Figure 4.13: Radiation-induced midgap voltage shifts in various dielectrics. LOT A – 0.01 atm. ammonia 1 hr and reoxidation; LOT B – 0.01 atm ammonia 0.25 hr and reoxidation.

Because negligible interface state build up occurred in the reoxidized nitrided oxides, flatband and midgap voltage shifts agreed to within a few millivolts. Only 67 mV shift occurred in Lot A devices after 5 Mrad, indicating a fixed charge increase of approximately 1×10^{11} cm^{-2}. As with interface state build-up, the effect of radiation on Lot B devices was greater, producing a 280 mV shift, and greater still in the oxide, producing a 320 mV shift.

The reduced midgap voltage shifts measured in these reoxidized nitrided oxides are believed to be a true indication of reduced fixed charge build-up, and not an artifact due to electron trapping compensation, as discussed by Sundaresan et.al. It is well known that nitridation of gate oxide results in an increase in electron traps. Electrons released by the ionizing radiation may be trapped, resulting in a positive

voltage shift which counters the negative shift produced by trapped holes. However, constant current stress measurements have shown that these reoxidized nitrided oxides contain negligible amounts of electron traps (Section 4.1.3). Furthermore, a simple calculation shows that the compensating effect due to electron trapping must be very small, even in a nitrided oxide which contains considerable numbers of traps.

We know from simple trapping theory that

$$\frac{dn}{dF} = \sigma(N - n) \tag{4.2}$$

where n is the density of trapped electrons, N is the density of traps, σ is the capture cross-section of the traps, F is the fluence, and detrapping is neglected. For $n << N$ we can write

$$n = \sigma N F \tag{4.3}$$

If we consider that free electrons are generated uniformly throughout the oxide and subsequently move to the positively biased gate, we can define an effective fluence

$$F(x) = K(d - x) \tag{4.4}$$

where K is the total number of electron-hole pairs created per unit volume, d is the oxide thickness, x is measured from the collecting electrode, and recombination is neglected. K can be calculated from

$$K = \frac{\rho R}{E_{pair}} \tag{4.5}$$

where $\rho = 2.3$ g/cm^3 is the density of SiO_2, R is the radiation dose and $E_{pair} \sim 2E_g(SiO_2) = 18$ eV. Benedetto and Boesch [83] have derived an empirical expression from photocurrent measurements of X-irradiated thin MOS oxides which agrees closely with this theoretical equation.

The shift in midgap (or threshold) voltage due to electron trapping can then be calculated assuming that the effect of interface states is negligible by

$$\Delta V = \int_0^d \int_0^x \frac{qn(x')}{\epsilon_{ox}} dx' dx \tag{4.6}$$

Solving for the condition $n(x) = \sigma NK(d - x)$, we obtain

$$\Delta V = \frac{q\sigma NKd^3}{3\epsilon_{ox}} \tag{4.7}$$

For a dielectric thickness of 25 nm, as in Sundaresan's experiments, typical electron trap cross section $\sigma = 10^{-15}$ cm^2 and density $N = 10^{18}$ cm^{-3}, and a dose of 1 Mrad(Si) $\sim$ 0.55 Mrad(SiO_2), we obtain $\Delta V = 0.011$ V. Sundaresan reported voltage shifts due to fixed charge on the order of 0.5 V. It is clear that, even when detrapping and recombination are neglected, the compensating voltage shift due to trapped electrons must be a secondary effect.

A dramatic reduction in radiation induced interface state build-up in nitrided oxides was first reported by Terry [16] and has since been confirmed by several researchers [17,21,22]. This property makes nitrided oxides very appealing for low dose rate radiation environments such as space, in which the concurrent annealing of fixed charge reduces the importance of the latter's effect on device performance, and leaves the non-annealing interface state build-up as the primary concern. However, for high dose rate environments fixed charge build-up remains an important problem. The very low fixed charge build-up observed in Lot A devices shows particular promise for these reasons.

4.5 Dilute nitridation/reoxidation process

The data reported in this section were largely taken by B. Jeffery Gross of our group who is developing an atmospheric pressure nitridation/reoxidation process.

A set of experiments were performed to compare the low pressure nitridation

	Low Pressure Process	Dilute Process
Q_f	9.5 - 10.5 $\times 10^{11} cm^{-2}$	2.0 - 7.0 $\times 10^{11} cm^{-2}$
D_{it}	4.0 - 6.0 $\times 10^{10} cm^{-2} eV^{-1}$	2.0 - 5.0 $\times 10^{10} cm^{-2} eV^{-1}$
ΔD_{it}	3.0 $\times 10^{11} cm^{-2} eV^{-1}$	2.0 - 5.0 $\times 10^{10} cm^{-2} eV^{-1}$
ΔV_{fb}	+ 0.67 V	$\pm$ 0.02 V

Figure 4.14: Comparison of dilute and low pressure nitridation/reoxidation processes for 0.1 atm nitridation in 100 % NH_3 or nitridation in 10 % NH_3/Ar for 1 hour, 950 °C. ΔD_{it} and ΔV_{fb} data was obtained for fluence = 0.035 C/cm^2.

process with an Ar-diluted process under conditions of equivalent ammonia partial pressures. The results of the comparison are summarized in figure 4.14. The two processes differed in that the fixed charge and interface state density in the dilute process was generally lower than in the low pressure process and varied considerably from run to run. In addition, interface state generation in the dilute process was considerably less than in the low pressure process. Finally, charge trapping was virtually non-existent in the dilute process whereas it was prevalent in the low pressure process.

The reduced interface state generation and charge trapping in the dilute process is reminiscent of a nitrided oxide that has been partially reoxidized, and suggests that oxygen may have been present during the nitridation step. The lower fixed

charge and interface state density might also be explained by the presence of oxygen. As discussed in section 3.5, the nitridation process may be limited by the out-diffusion of oxygen-containing by-products of the nitridation reaction. The presence of oxygen in the nitridation ambient would tend to inhibit the nitridation reaction by retarding the out-diffusion of oxygen-containing by-products. Reduced nitridation could account for the smaller fixed charge and interface state density. The large variations in the electrical properties of the dilute process could then be accounted for by large variations in the levels of oxygen contamination during dilute nitridations. It should be noted that the presence of high-field edge effects in LOCOS isolated capacitors (see 3.4.4) might also partially account for the reduced interface state generation and electron trapping in dilute nitridations. However, edge effects cannot explain the lower fixed charge and interface state density values in dilute nitridations.

While further experimentation is required to substantiate the above speculation regarding the presence of oxygen, it is nevertheless clear that the low pressure process shows less variation in electrical properties than the dilute process.

4.6 Summary

In this chapter we presented a number of the basic electrical properties of dielectrics formed by the low pressure nitridation and reoxidation of silicon dioxide.

A major difference between our work and previous work was the use of the pre-turnaround regime of the nitridation process in order to optimize the electrical properties of the dielectric. We exploited the effect that a lightly nitrided oxide could be dramatically improved by reoxidation. Based on this effect, a dielectric process was developed which exhibited greatly improved reliability over conventional silicon dioxide. The amount of interface state generation under electrical stress was reduced by a factor of 25 compared to silicon dioxide and charge trapping was

virtually eliminated. In addition, the breakdown strength was somewhat improved compared to oxide and the charge-to-breakdown was about one order of magnitude better than oxide. On the other hand, parameters important to device performance were somewhat degraded. The fixed charge density increased to $\sim$ 2-3 $\times$ 10^{11} cm^{-2} and the interface state density to $\sim$ 3 $\times$ 10^{10} cm^{-2} eV^{-1}.

The procedure by which we optimized the dielectric processing was described and reliability-performance tradeoffs outlined. It was shown that lighter nitridation result in better performance but at the expense of reduced reliability improvement.

The low pressure nitridation/reoxidation process also showed better resistance to ionizing radiation both in terms of interface state and fixed charge generation.

Finally, the low pressure process was shown to have better control compared to a dilute process with equivalent partial pressure, even though the dilute process appeared to have less interface state generation and electron trapping, a result suggestive of the presence of oxygen contamination during the dilute nitridation.

Chapter 5

Application to Scaled Transistors

Selected nitrided oxide and reoxidized nitrided oxide dielectrics from the capacitor study were incorporated into the transistor process to demonstrate their applicability to scaled MOS devices. The selected dielectrics are listed in Table 5.1.

5.1 Inversion Layer Mobility

Inversion layer mobility measurements were made on n– and p–channel devices with a W/L ratio of 100 μm/ 100 μm. Values were extracted from the linear region of the I_{DS} vs. V_{GS} curve for V_{DS} = 50 mV. The effective mobility was defined as:

$$\mu_{eff} = \frac{I_{DS}}{\frac{W}{L} C_{ox}(V_{GS} - V_T)V_{DS}} \tag{5.1}$$

where the threshold voltage, V_T, was found by linear extrapolation of the I_{DS} vs. V_{GS} curve to I_{DS} = 0 and C_{ox} is the measured dielectric capacitance. The value of the mobility is reported at V_{GS} - V_T = 0.5 V. The mobility was averaged over 5 devices on a given wafer. The uncertainty in the mobility is approximately ± 10 $cm^2/V \cdot s$ for n–channel and ± 5 $cm^2/V \cdot s$ for p–channel devices.

The measurements, summarized in Table 5.2, show that nitridation reduces inversion layer mobilities in both n– and p–channel devices.

Dielectric	Process Conditions
OX	40 min, 0.1 atm. oxidation 12 nm control oxide
NOX-H	1 hour, 0.1 atm. nitridation of OX
NOX-L	1 hour, 0.01 atm. nitridation of OX
ROXNOX-H	1 hour, 0.1 atm. reoxidation of NOX-H
ROXNOX-L	3 hour, 0.1 atm. reoxidation of NOX-L

Table 5.1: Dielectric processing conditions for insulators selected for transistor study.

Dielectric	Effective Surface Mobility $cm^2/V \cdot s$	
	electron	hole
OX	620 ±10	182 ±5
NOX-H	340 ±10	133 ±5
NOX-L	480 ±10	150 ±5
ROXNOX-H	400 ±10	142 ±5
ROXNOX-L	505 ±10	153 ±5

Table 5.2: Effective inversion layer mobility measured at $V_{GS} - V_T = 0.5V$.

Observe that: (1) The percentage degradation, $\Delta\mu_{eff}/\mu_{eff}$, in n–channel devices is more severe than in p–channel devices (~50% versus ~25%). Upon reoxidation, the electron mobility readily recovers. The hole mobility, on the other hand, does not appear to recover as significantly within the resolution of the measurement.

(2) The gate voltage dependence of the electron mobility is also reduced with nitridation and recovers upon reoxidation. The gate voltage dependence of the hole mobility, on the other hand, is not affected as significantly by nitridation or reoxidation (figures 5.1 and 5.2).

These observations are in agreement with those made by Terry [37] and Schmidt, et. al. [38] on transistors with nitrided gate oxides formed by an atmospheric process.

In order to understand the role of the nitridation-induced fixed charge in mobility degradation in nitrided oxide MOSFETs we plot the normalized inversion layer mobility versus the observed effective fixed charge at the interface (figure 5.3). The fixed charge densities were obtained by C–V measurements on capacitors adjacent to the transistor. In the case of the electron mobility we plot the oxide device data of Sun and Plummer where the fixed charge was intentionally introduced by an oxygen anneal cycle [97]. In the case of the hole mobility we plot the oxide device data of Galloway,et. al. where the fixed charge was introduced by ionizing radiation [98]. We also plot the nitrided oxide data of Schmidt et. al. citeSchmidt:Mobility for comparison. Observe that:

(3) Our data lies above the data of Sun and Plummer in the case of electrons and above the data of Galloway in the case of holes. The degradation in mobility appears to be less than would be expected from the observed fixed charge. This can be explained by assuming that the centroid of the fixed charge is actually located within the insulator at some distance from the interface. Whereas the effective charge at the interface is reduced linearly with the distance at which the centroid is located from the interface, coulombic scattering is reduced as the square of the distance from the interface.

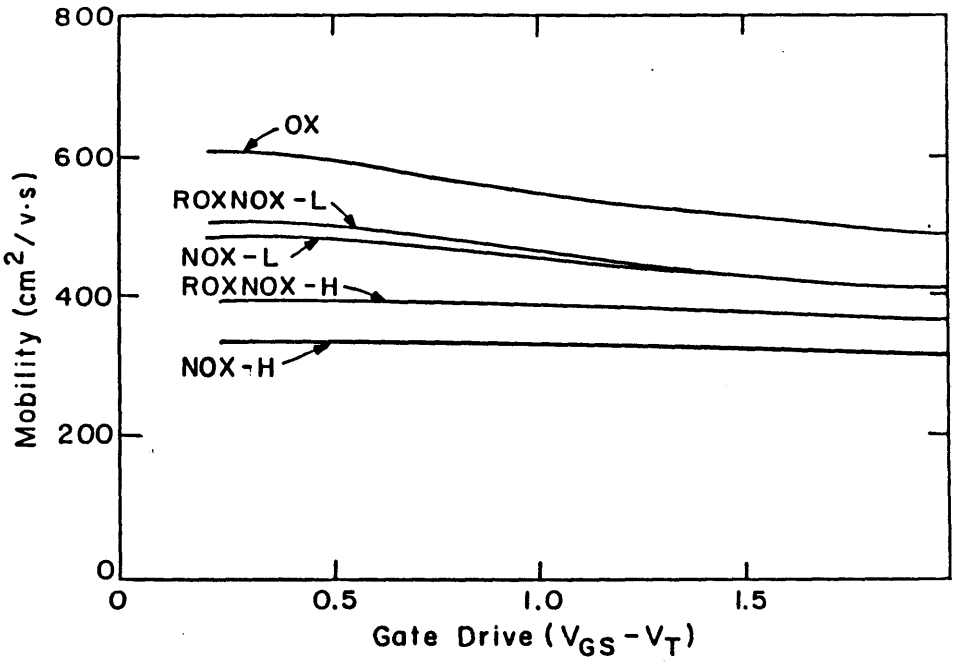

Figure 5.1: Gate voltage dependence of electron mobility.

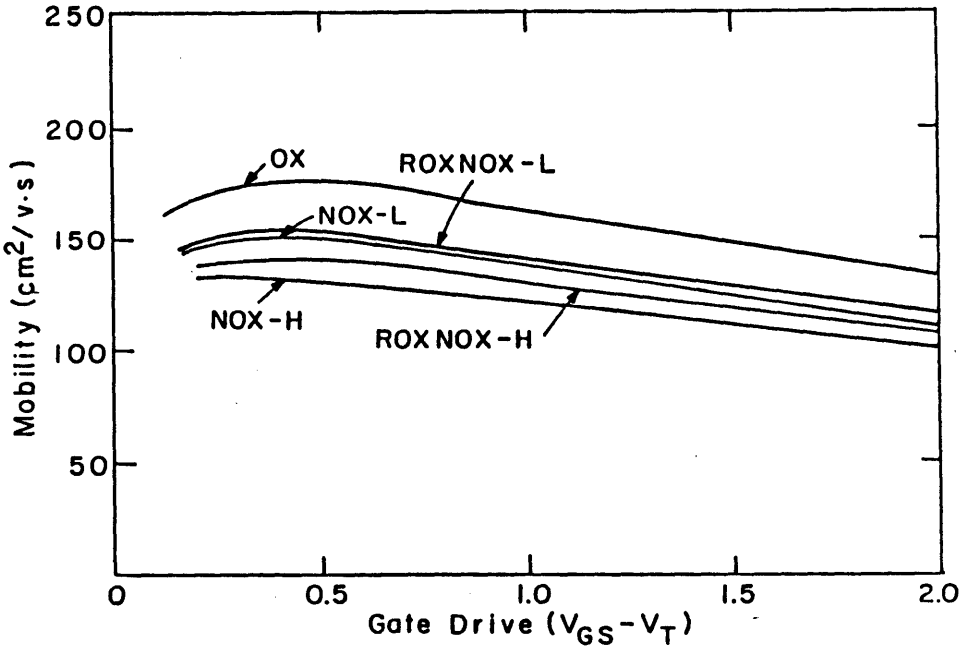

Figure 5.2: Gate voltage dependence of hole mobility.

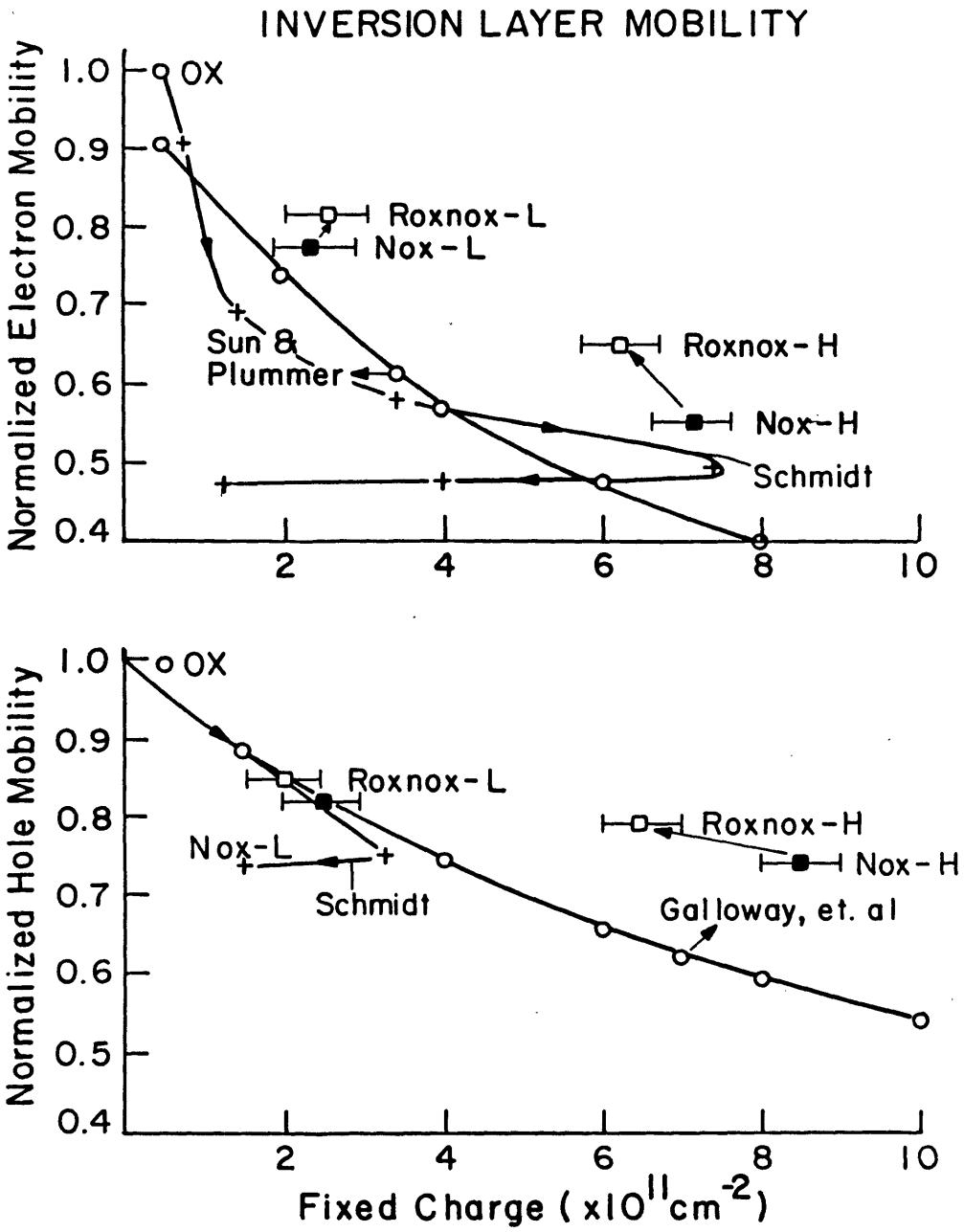

Figure 5.3: Normalized electron and hole mobility versus the observed effective charge at the interface. The data of Sun and Plummer [97] and Galloway [98] are also shown.

(4) The recovery of the electron mobility with reoxidation is more than can be accounted for by the slight changes in the fixed charge whereas the nominal change in the hole mobility with reoxidation can be explained by changes in the fixed charge.

Observations (1),(2), and (4) suggest an additional nitridation-induced scattering mechanism for electrons which is not present for holes and which is reduced with reoxidation.

The mobility data can be understood in the context of a recent model proposed by Schmidt, et. al. [38]. The model attributes the observed degradations in electron and hole mobilities to the combined effects of fixed charge and electron traps. Since nitridation introduces fixed positive charge, both electron and hole mobilities are degraded by coulombic scattering. In addition, nitridation introduces interfacial electron traps which are believed to be located near the conduction band of Si and charge neutral when empty (acceptor-like) [32]. These traps reduce the mobile charge in the channel due to trapping. In addition, the trapped charges further reduce the electron mobility due to coulombic scattering. The hole mobility is not affected by these electron traps since the traps are empty and hence neutral when the p–channel device is biased in inversion. The reoxidation of nitrided oxides, which removes nitridation–induced electron traps, improves electron mobilities while hole mobilities do not appear to be affected. The proposed model thus seems successful in explaining the observed mobility dependence on nitridation and reoxidation conditions despite differences in the nitridation techniques between the previous work and our work. The model further suggests that the difference in electron mobility that we have observed at a given level of fixed charge versus the electron mobility observed by Schmidt, et. al. may be due to differing electron trap densities in the two nitridation techniques.

In the case of a light nitridation combined with a reoxidation we are able to obtain mobilities within ~20% of the oxide devices. To obtain higher mobilities

even lighter nitridations must be used in combination with a reoxidation.

5.2 Channel Hot–Electron Stressing

Channel hot-electron stressing is a DC accelerated aging technique used to estimate the projected operating life of transistors. It is used here to verify that the decreased electron trapping and interface state generation observed in reoxidized nitrided oxide capacitors also results in improved transistor reliability.

Previous researchers have shown that channel hot-electron stressing of transistors with nitrided oxide as a gate dielectric results in increased threshold voltage shifts due to electron trapping but reduced transconductance degradation due to the suppression of interface state generation [19,20]. Here we report that reoxidized nitrided oxide devices show negligible V_T shifts as well as reduced transconductance degradation.

N–channel MOSFETs with effective channel length L_{eff} = 0.75 - 1.00 μm, width W = 20 μm, and gate dielectric thickness t_{ox} = 12 nm were used for channel hot–electron stressing experiments.

As discussed in section 3.4.2, channel hot-electron stressing is typically performed at a large drain-source voltage where impact ionization near the drain produces hole-electron pairs resulting in an appreciable substrate hole current. Device degradation has been shown to be primarily correlated with the substrate current used during stress [6]. To obtain worst-case degradation at a given V_{DS}, the gate-source voltage is biased at the peak of the I_{sub} vs. V_{GS} curve. The peak substrate current occurs roughly at $V_{GS} - V_T \sim V_{DS}/2$. The I_{DS} vs. V_{GS} characteristic at low V_{DS} = 0.1 V is taken before and after stress and the relative change in the maximum linear region transconductance $\Delta g_m/g_{m0}$ is taken as a measure of the degradation. The extrapolated threshold voltage shifts, ΔV_T, were < 40 mV in oxide devices and < 5 mV in ROXNOX devices for the range of stress conditions tested. These

apparent shifts in the extrapolated threshold voltage were due to a degradation in the slope of the I_{DS} vs. V_{GS} curve rather than an actual translation of I_{DS} vs. V_{GS} curve due to fixed charge generation or electron trapping.

In figure 5.4, typical transconductance degradation data is plotted as a function of stress time for transistors with various dielectrics stressed over a range of substrate-to-drain current ratios.

The curves are fit by the power law relation

$$\frac{\Delta g_m}{g_{m0}} = At^n \tag{5.2}$$

where the exponent n = 0.5-0.7 for our various devices. The value of n is in agreement with that reported in the literature [5,6] and does not appear to depend on the gate dielectric used. The magnitude of the degradation, A, is known to depend strongly on the stress conditions as follows [5]:

$$A \propto e^{-\frac{\alpha}{V_D}} \propto I_{SUB}/I_{DS} \tag{5.3}$$

In our case, the constant A also reflects the hot-electron resistance of the dielectric. Under conditions of similar I_{SUB}/I_{DS}, reoxidized nitrided oxide transistors show a factor of 10 improvement over oxide devices. In figure 5.5, this improvement is shown to hold over a range of substrate currents for a stress duration equal to 2 hrs.

Given figure 5.4, it is possible to estimate the projected operating life of devices. This is usually done by defining a quantity called lifetime, τ, as the stress time required to reach 10 % transconductance degradation and by plotting the lifetime versus the peak substrate-to-drain current ratio used during stress. This is shown in figure 5.6. The data points on this plot were obtained by interpolation and extrapolation of the data shown in figure 5.4 by assuming the power law relation. Note that there appears to be a channel length dependence to the level of degradation under conditions of similar I_{SUB}/I_{DS}, in that shorter channel length devices seem to ex-

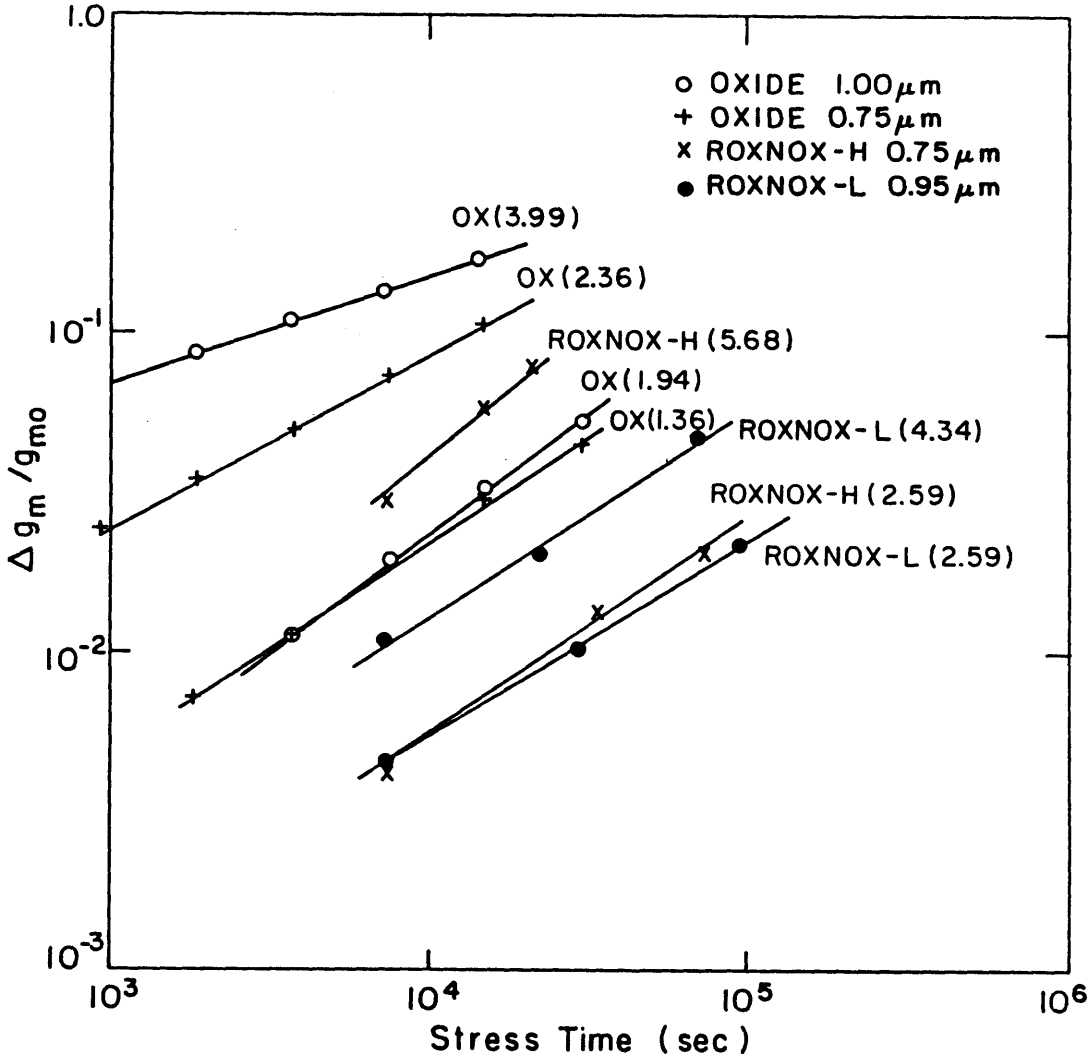

Figure 5.4: Transconductance degradation as a function of stress time for transistors with various dielectrics. The substrate-to-drain current ratio expressed as a percentage is shown in parentheses.

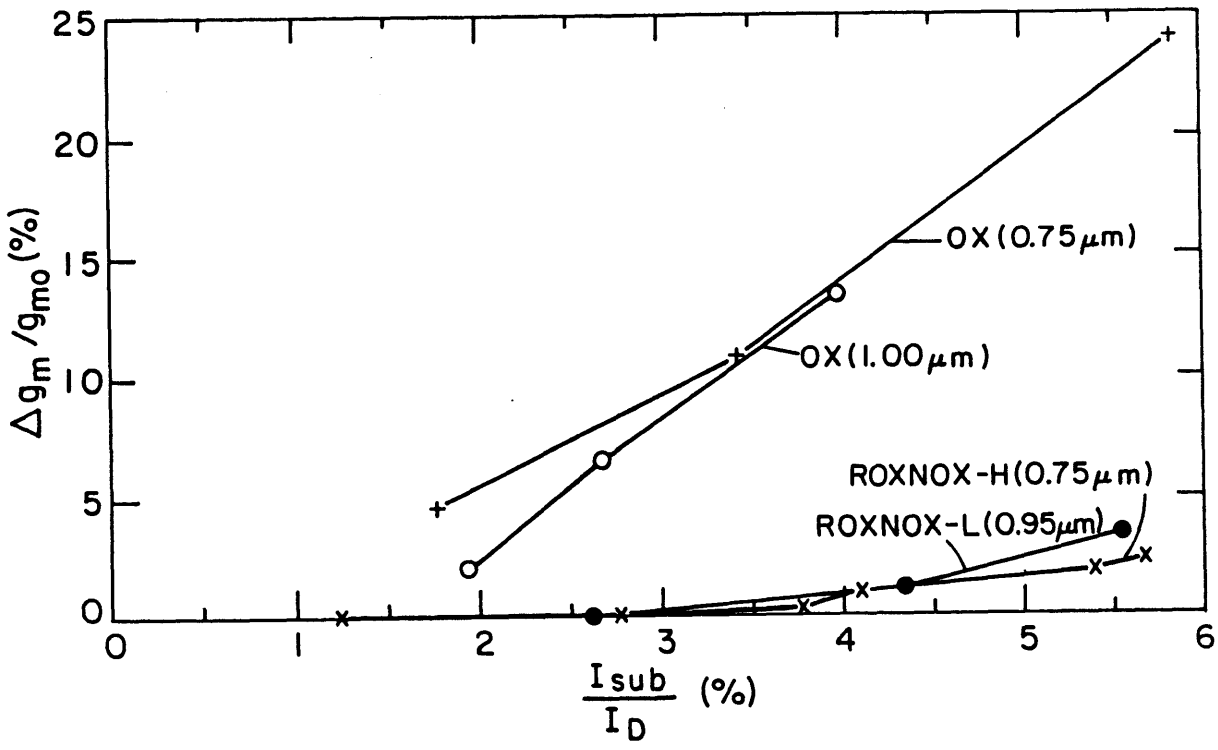

Figure 5.5: Amount of transconductance degradation versus substrate-to-drain current ratio for a stress duration of 2 hours.

perience greater degradation. However, by comparing 0.95 μm ROXNOX-L device with a 1.00 μm OX device, we can see that the reliability improvement due to the use of a reoxidized nitrided oxide gate dielectric is about one order of magnitude. Note that since the inversion layer mobility of ROXNOX devices is somewhat lower, the drain voltage corresponding to a given peak substrate current is higher. Thus it is more appropriate to plot lifetime vs. I_{SUB}/I_{DS} rather than to plot lifetime vs. V_{DS}. The former plot isolates the contribution of the gate dielectric in determining the overall life of the device whereas the latter reflects both the improved hardness of the ROXNOX dielectric as well as the lower mobility of reoxidized nitrided oxide devices.

5.3 Performance-Reliability Tradeoff

In the previous two sections we have demonstrated that ROXNOX devices exhibit a 20 % degradation in inversion layer mobility but at least an order of magnitude improvement in reliability under channel hot-electron stressing. From the standpoint of circuit performance, an important device parameter is the saturation-region transconductance [99]. While the inversion layer mobility of devices is lower by $\sim 20\%$ in ROXNOX devices, the saturated transconductance is only $\sim 10-15\%$ lower, depending on channel length. The apparent discrepancy is due to the somewhat increased ($\sim 5\%$) dielectric capacitance of ROXNOX insulators and due to the fact that in short-channel devices the carriers move near velocity saturation for a greater proportion of the channel [99]. Figure 5.7 shows that the saturated transconductance as function of inverse channel length for oxide and ROXNOX-L devices. The 10% reduction in transconductance in short-channel ROXNOX devices can be compensated for by using a thinner gate dielectric or a shorter channel length device. In assessing the advantages and disadvantages of the ROXNOX dielectric, therefore, the appropriate comparison is the measurement of the hot-electron resis-

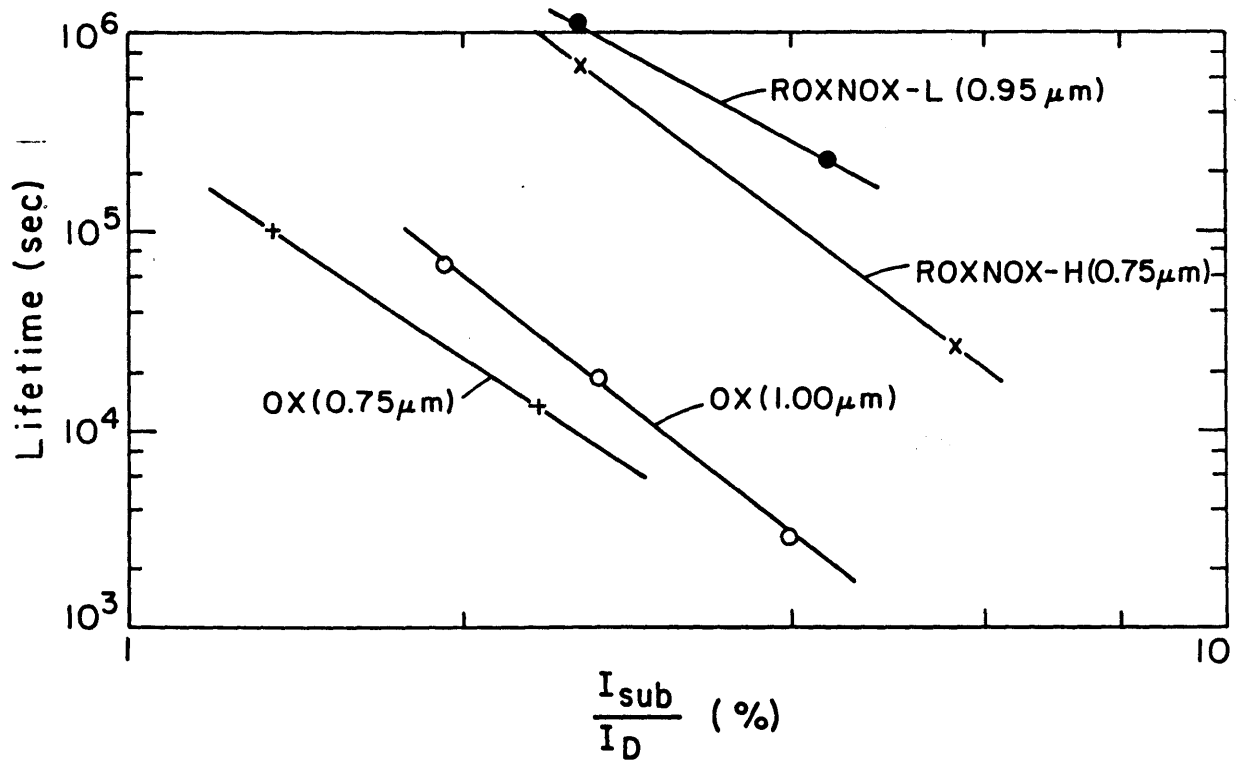

Figure 5.6: Projected operating life of short-channel transistors at various substrate-to-drain current ratio stress levels.

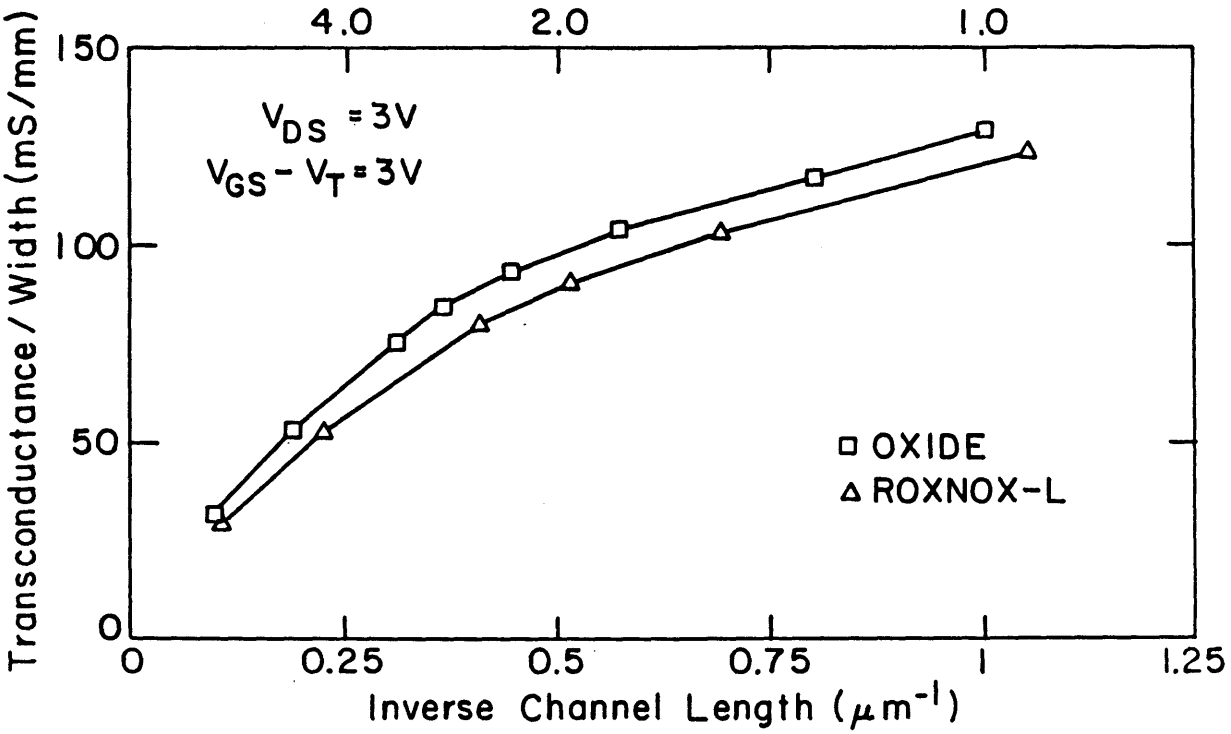

Figure 5.7: Saturated transconductance as a function of inverse channel length for oxide and ROXNOX-L devices.

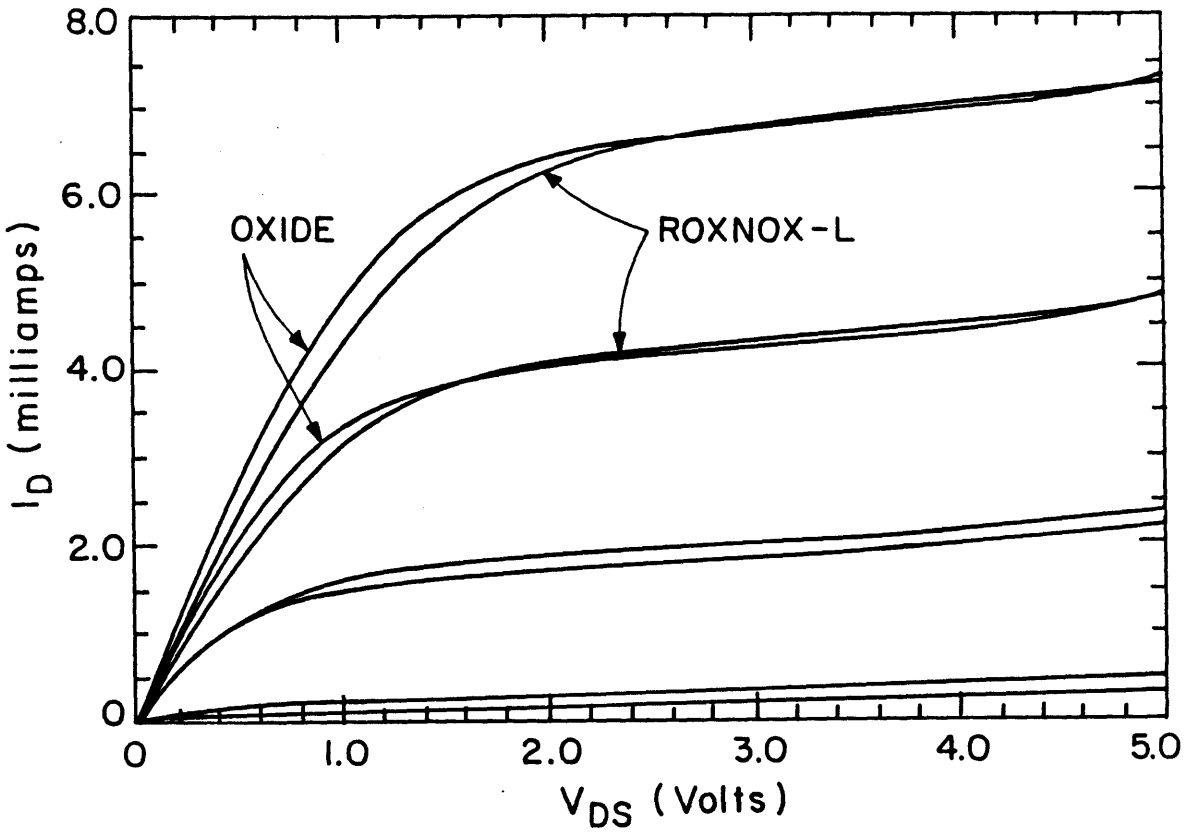

Figure 5.8: I–V characteristics of an oxide ($L_{eff} = 1.0\mu$m) and a ROXNOX-L device ($L_{eff} = 0.95\mu$m). The gate voltage is incremented at 1V/step.

tance of devices of identical performance. As shown in figure of 5.8, an oxide with $L_{eff} = 1.00$ μm has nearly the same I–V characteristics as a ROXNOX device with $L_{eff} = 0.95$ μm. The results of stressing these devices is shown previously in figure 5.5 indicates a factor of ten improvement in reliability.

5.4 Summary

In this chapter, we have discussed the incorporation of selected dielectrics into NMOS and PMOS devices. The inversion layer mobility of devices was analyzed. It was found that the degradation of electron and hole mobility due to nitridation is well-described by the Schmidt model [38]. In the case of a light nitridation combined with a reoxidation we obtained electron and hole mobilities within 20 % of oxide

values.

Channel hot-electron stressing measurements indicated an order of magnitude improvement in the projected operating life of ROXNOX transistors over oxide devices. It was also demonstrated that for devices of the same performance (same g_m), ROXNOX devices still had a factor of ten advantage over oxide devices.

Chapter 6

1/f Noise

6.1 Introduction

In this chapter, we investigate the use of 1/f noise measurements as a technique for extracting the oxide trap density near the conduction and valence bands of Si. The development of the technique, however, is complicated by the fact that 1/f noise in MOSFETs is not fully understood.

The theories that have been proposed to account for 1/f noise in MOS transistors can be broadly classified into three categories.

(1) The number fluctuation model, based on the original proposal of McWhorter [66], attributes 1/f noise to fluctuations arising from electronic tunneling transitions between interfacial oxide traps and the MOSFET channel. The model predicts an equivalent gate voltage noise power spectral density for uniform trap distributions which is independent of the gate voltage in strong inversion and proportional to C_{ox}^{-2}. The theory is supported by several experiments [116,118,119] and, in particular, by the widely observed proportionality between 1/f noise and the oxide trap density [120,121,122,123].

(2) The mobility fluctuation model, based on Hooge's relationship [124], is an empirical model able to fit noise data in homogeneous semiconductors and devices.

When the model is applied to MOSFETs with certain modifications [125], it can fit noise data which is proportional to $(V_{GS} - V_T)/C_{ox}$ [126,127]. Several suggestions have been made regarding the possible physical origin of mobility fluctuations [128,129] though none have been widely accepted.

(3) Some authors have combined both the number and mobility fluctuation models in order to explain a broader set of data [130,131,132]. However, previous models have combined number and mobility fluctuations in an *uncorrelated* manner.

In this chapter, we begin by reviewing the theory of 1/f noise based on the McWhorter tunneling model. The review is provided in two parts. In the first part, we develop the theory assuming that the oxide trap density and distribution is constant over space and energy. In the second part, we treat the effect of oxide band bending and nonuniform trap distributions. The nonuniformity is shown to give rise to a gate voltage dependence of the 1/f noise magnitude as well as a change in the exponent, γ, of the $1/f^{\gamma}$ noise spectrum.

In section 6.3, we consider an extension of the number fluctuation model of 1/f noise which includes carrier number fluctuations as well as *correlated* mobility fluctuations. We again begin by assuming a uniform trap distribution. As in the number fluctuation model, the fluctuations are physically caused by the tunneling of inversion layer carriers to and from interfacial oxide traps. Unlike the number fluctuation model, however, our model accounts for mobility fluctuations caused by scattering due to the trapped carrier. Initial evidence that such a mechanism may in fact prevail was given by Ralls, et.al. [133] in their study of single electron switching events in small area MOSFETs. In these experiments, it was shown that when an electron becomes trapped, the change in the channel resistance may be more or less than that expected from the effect of a missing charge. Such a switching behavior can be explained by considering traps that are either neutral or charged when filled and by accounting for the coulombic scattering due to these traps. Surya [131] developed a theory based on such a mechanism for large area MOSFETs. However,

Surya combined number and mobility fluctuations in an uncorrelated fashion despite the fact that both fluctuations arise from the same mechanism. Here, we consider a theory of 1/f noise which is based on *correlated* number and mobility fluctuations. We include the dependence of the scattering on the distance of the trapped charge from the interface and consider its effect on the frequency dependence of 1/f noise. Since the mobility fluctuations cause a drain current fluctuation proportional to the channel charge, noise due to mobility fluctuations is dependent on the gate voltage. Thus the combined effects of nonuniform trap densities and mobility fluctuations give rises to a gate voltage dependence of the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum.

In section 6.4, experimental results are presented and used to extract the oxide trap density in space and energy, $N_T(x, E)$, in terms of both noise models. Finally, the models are used to study the effect of nitridation (ammonia annealing of a gate oxide) and reoxidation (oxygen annealing of a nitrided gate oxide) on the trap density and distribution in the dielectric.

6.2 Number fluctuation model

6.2.1 Assumptions

The McWhorter tunneling model is also called the number fluctuation model because it involves calculating the noise power of the number of fluctuating channel carriers. In deriving the number fluctuation model we primarily follow the analysis of Christensson [116]. We begin by reviewing several assumptions and simplifications that are commonly made in formulating the number fluctuation model of 1/f noise. Initially, the case of uniform trap distributions in space and energy is treated.

(1) The trapping of an inversion layer carrier by an oxide trap is assumed to induce only a carrier density fluctuation in the channel. The scattering due to the trapped carrier produces a negligible mobility fluctuation. This assumption is

removed in section 6.3.

(2) The MOSFET is biased in strong inversion so that carriers in the conduction band tunnel directly into and out of oxide traps at the same energy level. Fluctuations due to electronic transitions between the conduction band and interface states located in the silicon bandgap are neglected under these conditions [123]. Inelastic tunneling (that is, tunneling between different energy levels) is regarded as unlikely [134].

(3) The device is biased in the linear region, ie. $V_{DS} \leq V_{GS} - V_T$, so that we can assume that the band bending is nearly constant along the channel from source to drain. In addition, we assume that the inversion charge, Q_N, the mobility, μ_N, and the electric field, $\mathcal{E}$, are all constant along the channel. Thus from simple MOSFET theory the drain current can be expressed as

$$I_D = \frac{W}{L}\mu_N Q_N V_{DS} \tag{6.1}$$

where $Q_N = C_{ox}(V_{GS} - V_T)$.

(4) The oxide tunnel barrier seen by an inversion layer carrier is a rectangular barrier of height ϕ_B, where ϕ_B is the height of the oxide conduction band from the Si conduction band. Since the wave function of an electron decays exponentially into such a barrier, the time constant associated with a trapping event is given by

$$\tau_T = \tau_0 e^{2\alpha x} \tag{6.2}$$

where x is the distance into the oxide from the Si-SiO_2 interface and

$$\alpha = \sqrt{\frac{2m_e^* \phi_B}{\hbar^2}} \tag{6.3}$$

where m_e^* is the effective mass of the electron in the oxide and $\hbar$ is Plank's constant divided by 2π. The value of α is typically taken to equal 10^8 cm^{-1} and τ_0 is typically taken to equal 10^{-10} sec [116]. The above form explicitly neglects band bending in

the oxide. If oxide band bending is included, then α becomes a function of x. Under the WKB approximation [117],

$$\tau_T = \tau_0 e^{2\alpha(x,\mathcal{E})} \tag{6.4}$$

where

$$\alpha(x,\mathcal{E}) = \frac{2}{3\mathcal{E}}\left(\frac{2m_e^*}{\hbar^2}((\phi_B - \mathcal{E}x)^{3/2} - \phi_B^{3/2}\right) \tag{6.5}$$

For an $\mathcal{E}$-field of 3 MV/cm (maximum used in this thesis), a noise measurement at a frequency of 20 Hz (corresponding to a $\tau_T \sim 0.05$ sec) corresponds to a trap depth of 10 $\AA$ assuming a rectangular barrier and a depth of 10.4 $\AA$ assuming a trapezoidal barrier. Given the small difference between the rectangular and trapezoidal barrier, we will assume a rectangular barrier for simplicity.

It is further assumed that the system is in steady-state and tunneling transitions involving a given trap are dominated by a single time constant.

(5) When one unit of charge is trapped at some distance, d_t, within the oxide it induces a charge fluctuation in the channel which is less than one unit of charge. That is,

$$\mid \delta Q_N \mid = \frac{t_{ox} - d_t}{t_{ox}} \mid \delta Q_T \mid \tag{6.6}$$

For t_{ox} much greater than d_t, however, we can assume that $\mid \delta Q_N \mid \sim \mid \delta Q_T \mid$.

6.2.2 Spectrum of carrier fluctuations in an element volume

In this section, the spectral density of fluctuations in the number of trapped carriers in an element volume, ΔV, and in an energy element, ΔE is calculated. Given the noise spectral density in a volume and energy element, we can sum (integrate) over all volume and energy elements of the device to calculate the total noise spectrum. The coordinate system in real and energy space is defined in figure 6.1. Consider first the effect of a single trap located at a distance, x, in the oxide,

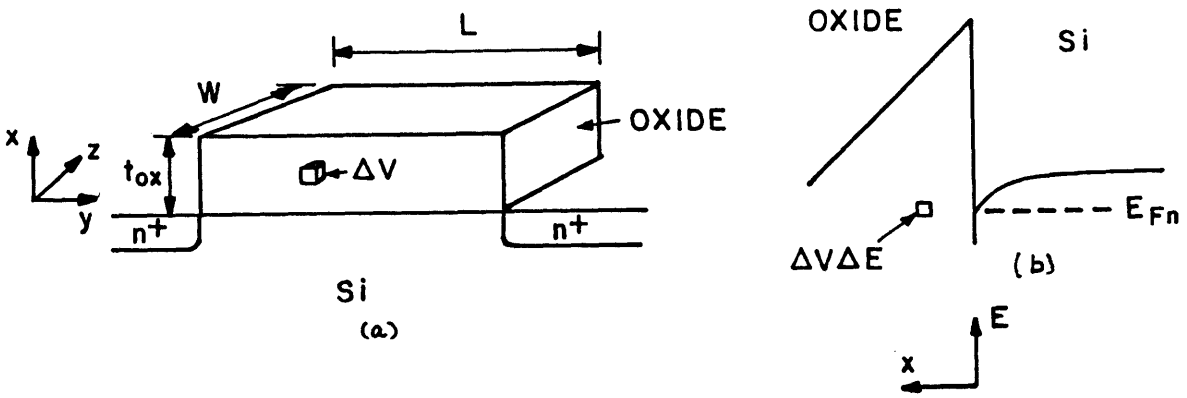

Figure 6.1: Definition of the coordinate system in (a) real and (b) energy space. $\Delta V = \Delta x \Delta y \Delta z$ is an element volume and ΔE is an energy element. $x = 0$ at the Si-SiO_2 interface and increases with distance into the oxide. $E = 0$ at the bottom of Si conduction band edge and increases with energy above E_c as measured under flatband conditions. Note that $\Delta V \Delta E$ shown in figure (b) is located at $(x > 0, E > 0)$.

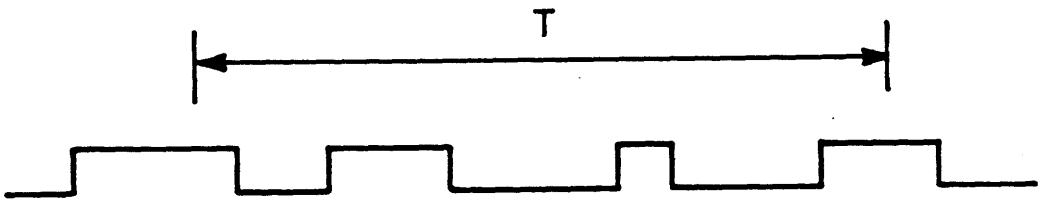

Figure 6.2: Random telegraph signal.

which interacts with the silicon inversion layer with a characteristic time constant, τ_T. The trapping and detrapping of carriers by a single trap will produce a current waveform at the device terminals which is normally referred to as a random telegraph signal [135] as shown in figure 6.2.

This type of signal has recently been observed in extremely small area MOSFETs where it has been possible to isolate the effect of a single trap [133]. For large area MOSFETs, we need to consider the behavior of an ensemble of traps.

The power spectral density of a random telegraph signal has a shot noise spectrum of the form:

$$S(\omega) \propto \frac{\tau_T}{1+\omega^2\tau_T^2} \tag{6.7}$$

This spectrum is often called a shot noise spectrum since it is white for frequencies less $1/\tau_T$. [135].

Now consider a collection of traps in an element volume, ΔV, that is sufficiently small so that all traps are characterized by a single time constant, τ_T. If these

traps are distributed in energy around the electron quasi-Fermi level, then traps a few kT below the quasi-Fermi level will be full and traps a few kT above the quasi-Fermi level will be empty. Thus only traps near the quasi-Fermi level will contribute to fluctuations. The power spectral density of the fluctuations in the *number* of trapped electrons in the volume element, ΔV, and in the energy element, ΔE, is thus [136,137]

$$S_{N_T \Delta V \Delta E} = \frac{\tau_T}{1 + \omega^2 \tau_T^2} N_t f_T (1 - f_T) \Delta V \Delta E \tag{6.8}$$

where N_t is the trap density in units of $cm^{-3}eV^{-1}$ and f_T is the probability that a trap is filled given by the Fermi factor

$$f_T = \frac{1}{1 + e^{\frac{E_T - E_{Fn}}{kT}}} \tag{6.9}$$

Note that the term $f_T(1 - f_T)$ is a peaked function about the electron quasi-Fermi level and reflects the fact that only traps near the electron quasi-Fermi level contribute to fluctuations or noise. Under strong inversion conditions with $t_{ox} \gg d_t$, the spectral density of the fluctuation in the trapped oxide charge is equal to the spectral density of the induced fluctuation in the channel charge [138]:

$$S_{Q_N \Delta V \Delta E} = q^2 S_{N_T \Delta V \Delta E} \tag{6.10}$$

6.2.3 Spectrum of voltage and current fluctuations.

Given the spectral density of fluctuations in the channel charge, we can relate these fluctuations to the noise that would be measured at the device terminals. Consider an induced fluctuation in the *number* of carriers in the channel element, $\Delta y \Delta z$, due to a fluctuation in trapped oxide charge in the element, $\Delta V \Delta E$. The drain current fluctuation, $\delta I_{D,\Delta V \Delta E}$, under conditions for which the drain is an AC short-circuit, is given by

$$\delta I_{D,\Delta V \Delta E} = \frac{W \mu_N V_{DS}}{L} \frac{(\delta Q_N \Delta y \Delta z)}{WL} \tag{6.11}$$

where $(\delta Q_N \Delta y \Delta z)$ is simply q times the total number of carriers in element $\Delta y \Delta z$. The drain current noise power spectrum is thus equal to

$$S_{I_{D,\Delta V \Delta E}} = \frac{I_D^2}{W^2 L^2 Q_N^2} \; S_{Q_N \Delta V \Delta E} \tag{6.12}$$

The short-circuit drain current noise spectrum is related to the open-circuit drain voltage noise spectrum by

$$S_{V_{D,\Delta V \Delta E}} = \frac{S_{I_{D,\Delta V \Delta E}}}{g_0^2} = \frac{V_{DS}^2}{W^2 L^2 Q_N^2} \; S_{Q_N \Delta V \Delta E} \tag{6.13}$$

where g_0 is output conductance of the device. The equivalent gate voltage noise spectrum can also be written as

$$S_{V_{G,\Delta V \Delta E}} = \frac{S_{I_{D,\Delta V \Delta E}}}{g_m^2} = \frac{S_{Q_N \Delta V \Delta E}}{W^2 L^2 C_{ox}^2} \tag{6.14}$$

The last equation has the particularly simple interpretation that a fluctuation in the channel charge produces a fluctuation in the gate voltage through the relation

$$\delta V_G = \frac{\delta Q_N}{WLC_{ox}} \tag{6.15}$$

which is simply an expression of $Q = CV$.

6.2.4 Total noise spectrum including geometrical factors

Given the noise spectral density in a volume and energy element, we can sum (integrate) over all volume and energy elements of the device to calculate the total noise spectrum. The assumption here is that the noise due to each element volume is uncorrelated. Integrating over x, y, z, and E and assuming that all variables are uniform over x, y, z and E we have for the equivalent gate voltage noise spectrum

$$S_{V_G} = \frac{q^2}{WLC_{ox}^2} \int_0^{d_m} dx \int_{E_V}^{E_C} dE \, \frac{N_t(x,E)\tau_T(x)}{1+\omega^2\tau_T^2(x)} \, f_T(E)(1-f_T(E)) \qquad (6.16)$$

Given that the trap distribution is uniform in space and energy, the above integral can be evaluated analytically. The integral over E of $N_t f_T(E)(1-f_T(E))$ is approximately $4kTN_t(E_{Fn}) \equiv N_T(E_{Fn})(cm^{-3})$ [116]. The integral over x is calculated as follows:

$$S_{V_G} = \frac{q^2 \; N_T(E_{Fn})}{WLC_{ox}^2} \int_o^{d_m} dx \frac{\tau_T(x)}{1+\omega^2\tau_T(x)^2} \qquad (6.17)$$

where d_m is chosen to be sufficiently large so as to account for all traps that contribute to noise in the frequency range of interest. For example, a d_m of 20 $\AA$ corresponds to a time constant of $\sim 2 \times 10^7$ sec, which is already sufficiently large for the frequency range of interest.

Changing variables to integrate over τ instead of x we have

$$\int_0^{d_m} \frac{\tau_T(x)}{1+\omega^2\tau_T^2(x)} \, dx \; = \int_{\tau_0}^{\tau(d_m)} \frac{\tau}{1+\omega^2\tau^2} \, \frac{d\tau}{2\alpha\tau} \qquad (6.18)$$

$$\int_{\tau_0}^{\tau(d_m)} \frac{1}{1+\omega^2\tau^2} \frac{d\tau}{2\alpha} = \frac{1}{2\alpha\omega}(tan^{-1}\omega\tau(d_m) - tan^{-1}\omega\tau_0) \qquad (6.19)$$

For $\omega\tau_0 \ll \omega\tau \ll \omega\tau(d_m)$, $tan^{-1}\omega\tau(d_m) \approx \pi/2$ and $tan^{-1}\omega\tau_0 \approx 0$, yielding

$$S_{V_G} = \frac{q^2}{8WLC_{ox}^2\alpha} \frac{N_T(E_{fn})}{f} \quad (\frac{V^2}{Hz}) \qquad (6.20)$$

where $N_T(E_{fn})$ is oxide trap density adjacent to the electron quasi-Fermi level in silicon.

6.2.5 Predictions of the number fluctuation model

Aside from explaining the frequency spectrum of the noise, the number fluctuation model predicts that:

(1) 1/f noise decreases with increasing device area.

(2) 1/f noise increases with the square of the oxide thickness.

(3) 1/f noise is independent of gate voltage since $N_T(E_{Fn})$ is independent of gate bias for uniform trap distributions.

6.2.6 Effect of nonuniform trap distributions and oxide band bending

In the above discussion, we have explicitly assumed that oxide trap density is uniform in space and energy. In this section, we show that nonuniform trap distributions can give rise to a gate voltage dependence in the magnitude and the exponent, γ, of the $1/f^{\gamma}$ spectrum.

We begin by identifying regions of the oxide (both in space and energy) that are accessed by 1/f noise measurements and consider the effect of nonuniformities within this region. Figure 6.3 illustrates the region or window of the (x, E) space accessed by a measurement of the 1/f noise magnitude versus frequency for a gate bias in strong inversion. The window is located within the oxide and is centered about the axis of the electron quasi-Fermi in the silicon. The energy width of the window is $\sim 4kT$ and the length of the window depends on the range of frequencies over which the noise measurement is performed. For example, a noise measurement over 4 decades of frequency corresponds to a length of $\sim 5\mathring{A}$. Note also that points of increasing depth and increasing energy are intersected along the length of the window due to oxide band bending.

In figure 6.4, it is shown that if the trap distribution is nonuniform along the length of the window then the noise spectrum deviates from strictly 1/f and might be approximated as $1/f^{\gamma}$ where $\gamma \neq 1$. For a trap distribution that is skewed towards the interface, there are a greater number of high frequency traps leading to $\gamma < 1$. Similarly for a trap distribution that is skewed away from the interface, there are a greater number of low frequency traps leading to $\gamma > 1$ [116,139]. Note that the

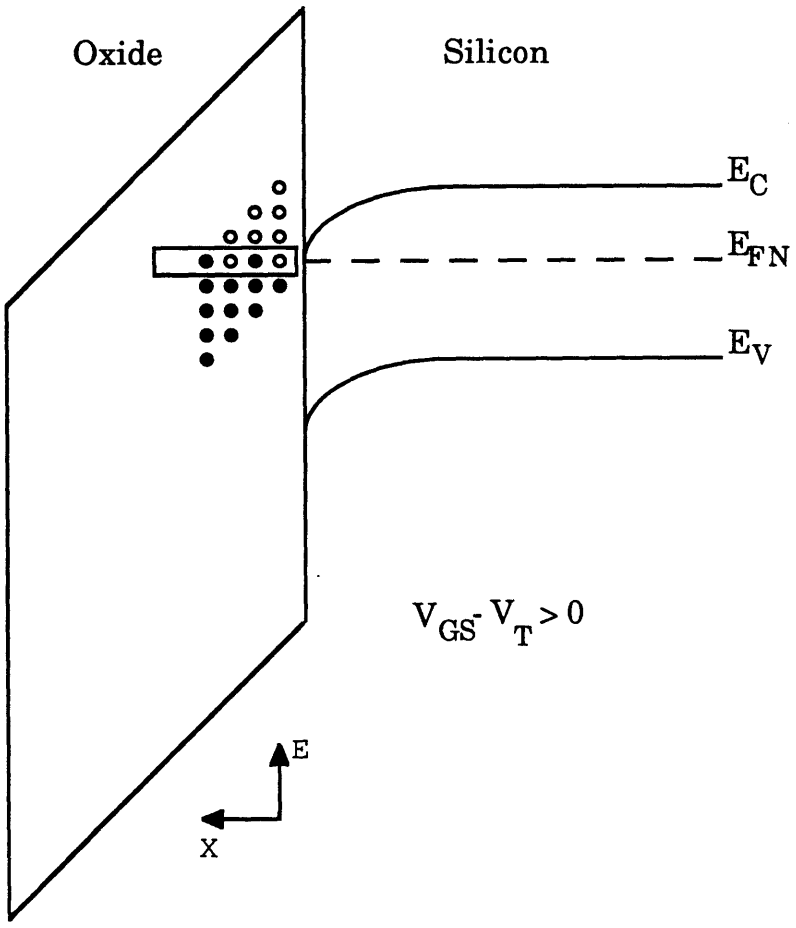

Figure 6.3: Window in (x, E) space accessed by a measurement of the 1/f noise magnitude versus frequency in strong inversion.

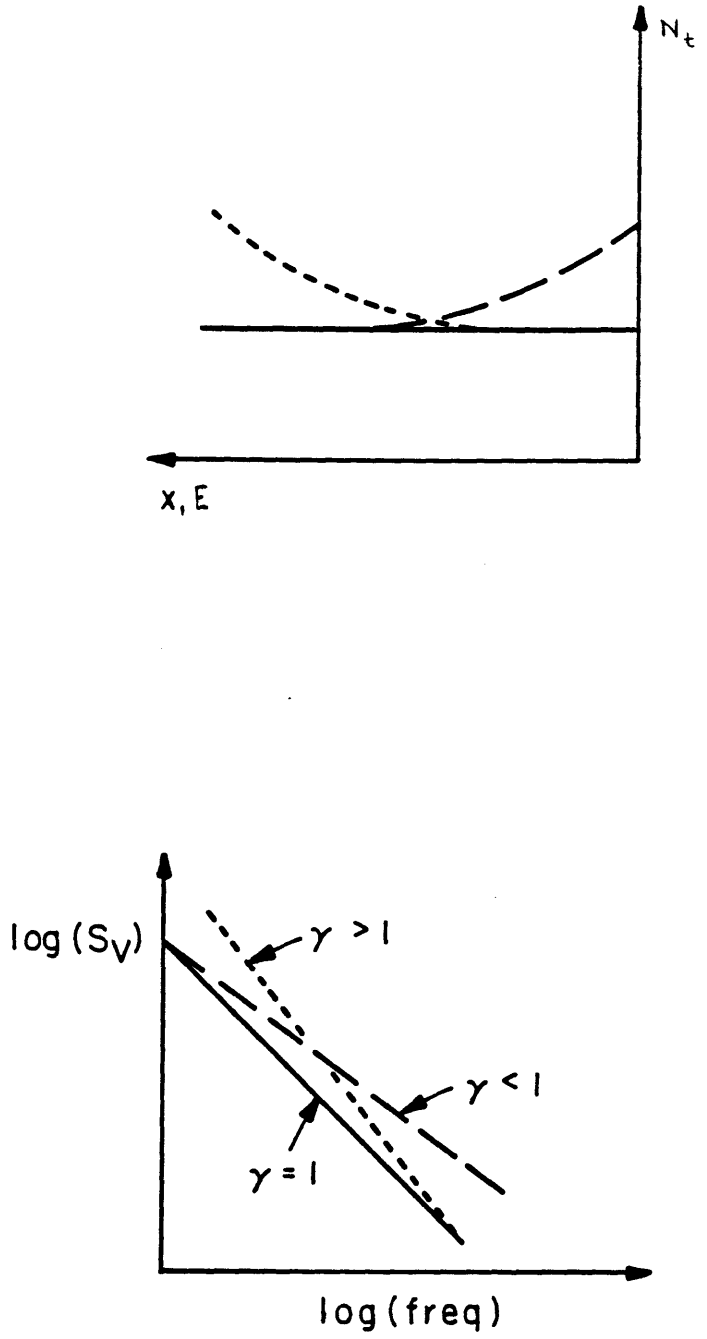

Figure 6.4: Effect of a nonuniform trap distribution on the exponent of the $1/f^{\gamma}$ noise spectrum.

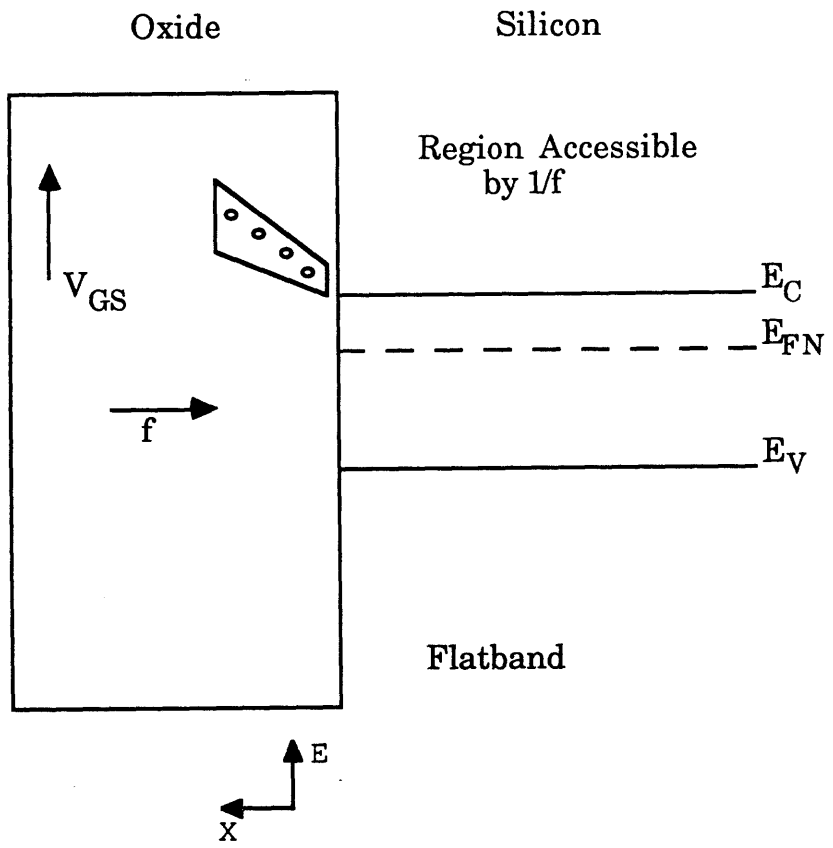

Figure 6.5: Entire region of the (x, E) space accessible by a series of 1/f noise magnitude versus frequency measurements over a range of gate biases.

nonuniformities along the length of the window can arise from nonuniformities in the trap distribution in space and/or energy.

By performing a series of 1/f noise magnitude versus frequency measurements over a range of gate biases, it is possible to examine a broader region of the oxide as illustrated in figure 6.5. The peculiar shape of this region arises from the effect of oxide band bending. As the gate bias is increased, traps which are above the Si conduction band edge under flatband conditions are brought down into the window accessible by 1/f noise measurements. Oxide traps that are further from the Si interface are affected to a greater extent by oxide band bending than traps that are nearer to the interface.

Given a set of noise data, the trap density and distribution used in the number fluctuation model can be adjusted so that the calculated noise equals the measured

noise. Using this procedure, it is possible to uniquely specify the oxide trap density at each point, $N_T(x, E)$, within the region.

Experimentally, a gate voltage dependence of 1/f noise has been widely observed [126,127,141,130]. Recently, a gate voltage dependence of the exponent, $\gamma(V_{GS})$, of the $1/f^{\gamma}$ has also been observed [139,140,131]. Both Surya [139] and Celik [140] assumed a trap distribution that was exponentially increasing in energy but uniform in space in order to fit both the magnitude and exponent, $\gamma(V_{GS})$, of the $1/f^{\gamma}$ spectrum. However, they found that it was not possible to simultaneously fit both the magnitude and exponent particularly at higher gate biases. This difficultly may be due to the peculiar functional form assumed for the oxide trap distribution. As discussed above, it should be possible to fit any noise data by appropriately adjusting the trap density at each point of the (x, E) space.

6.2.7 Limitations of the number fluctuation model

The primary limitation of the number fluctuation model is its neglect of possible mobility fluctuations which are correlated with number fluctuations. As discussed previously, evidence that mobility fluctuations might exist was provided by Ralls, et. al. [133] in their study of single electron switching events. In these experiments, it was shown that when an electron becomes trapped, the channel resistance may be more or less than that expected from the effect of a missing charge. Such switching behavior can be explained by considering traps that are either neutral or charged when filled and by accounting for the coulombic scattering due to these traps.

This limitation lead Surya [131] to consider a theory of 1/f noise which combined number and mobility fluctuations. However, mobility and number fluctuation were combined in an uncorrelated manner whereas in fact they arise from the same mechanism.

In the next section, we consider a 1/f noise model which combines number and mobility fluctuations in a correlated manner and consider the consequences of such

a theory on noise behavior. It is shown that the correlated fluctuation model also gives rise to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum even for uniform trap distributions.

6.3 Correlated number and mobility fluctuation theory

We begin by considering the case of uniform trap distributions and by making the usual assumptions of the number fluctuation model except for one critical difference. The trapping of inversion layer carriers by oxide traps is now assumed to induce a fluctuation in the number of channel carriers as well as a correlated fluctuation in the mobility of inversion layer carriers caused by coulombic scattering by the trapped charge. This changes the amplitude of the random telegraph signal of figure 6.2 but does not alter the time constant of interaction since both number fluctuations and mobility fluctuations arise from the same physical mechanism. A theory of 1/f noise considering such a mechanism of *correlated* number and mobility fluctuations is explored in this section.

Proceeding in a manner similar to section 6.2, the current fluctuation due to a fluctuation in the *number* of carriers in the channel element $\Delta y \Delta z$ and due to a correlated mobility fluctuation, $\delta\mu$, is

$$\delta I_{D,\Delta V \Delta E} = \frac{W}{L} V_{DS} (\mu_N \frac{\delta Q_N \Delta y \Delta z}{WL} + Q_N \delta\mu) \tag{6.21}$$

The form of this equation immediately suggests a noise component that is dependent on the gate bias through the relation $Q_N = C_{ox}(V_{GS} - V_T)$. Since the fluctuation in the mobility, $\delta\mu$, is *correlated* with the fluctuation in the channel charge, δQ_N, we can express $\delta\mu$ in terms of δQ_N.

Using Matthiessen's rule [142], we can write,

$$\frac{1}{\mu_n} = \frac{1}{\mu_N} + S(x)(\frac{\delta Q_N \Delta y \Delta z}{WL}) \tag{6.22}$$

where μ_n is the instantaneous mobility, μ_N is the time average mobility, and $S(x)$ is the scattering rate. The scattering rate, $S(x)$, will depend on the distance of the trapped charge from the interface. Based on the work of Brews [143], we assume the following approximate dependence of the scattering rate on the location of the scattering charge:

$$S(x) \approx S_0 \; ln \; (1 \; + \; (\frac{r_{max}}{x})^2) \tag{6.23}$$

where x is the distance into the oxide and S_0 can be estimated from published data [97] relating the inversion layer mobility to the oxide charge by the procedure described in 6.4.1. Brews [143] defines the distance r_{max} as the maximum distance from the scattering charge for which the effect of image charges can be neglected. For distance greater than r_{max}, the discreteness of a scattering charge is not apparent and image terms cause the coulombic scattering potential to fall off more rapidly than $1/r$. The distance r_{max} is given by,

$$r_{max} \approx \frac{(\epsilon_{ox} \; + \; \epsilon_{Si})}{(C_{ox} \; + \; C_s)} \tag{6.24}$$

For oxide thicknesses ranging from 12 nm to 40 nm, r_{max} ranges from $\sim$ 50 nm to $\sim$ 150 nm. Since tunneling occurs within $\sim$ 2 nm of the interface, $x \ll r_{max}$ in all cases and thus,

$$S(x) \approx 2S_0 \; ln \; (r_{max}/x) \tag{6.25}$$

For calculations used in this thesis, we use a value of r_{max} of 50 nm. Due to the logarithmic dependence, the scattering rate is relatively insensitive to the choice of r_{max}. A more accurate relationship between the scattering rate and the distance of the scattering charge from the interface has been theoretically treated by Sah, et.al. [145]. In their work, the effect of oxide charges is treated as producing perturbations in the surface potential and the scattering rate is determined using first order

perturbation theory treating mobile electrons as plane wave states. For simplicity, however, we use the above functional form which yields at least an approximate dependence. The above scattering rate dependence has the effect of increasing the contribution of mobility fluctuations for higher frequencies which correspond to scattering sites nearer to the interface. Over the frequency range of interest in this thesis ($\sim$ 20 Hz to 50 kHz), the scattering rate varies by a factor of $\sim$ 1.13 as calculated from equation 6.2 and 6.23. The effect of the scattering dependence on the exponent of the $1/f^{\gamma}$ noise spectrum is to make $\gamma < 1$ as discussed in section 6.3.1. The primary limitation of the above functional dependence is the presence of the non-physical singularity at $x = 0$. To avoid infinite scattering due to this singularity, we do not calculate the noise power due to traps at $x = 0$. The error due to the neglect of traps at $x = 0$ is negligible as discussed in section 6.4.1.

Rearranging the equation 6.22, the fluctuation in mobility, $\delta\mu$, is then

$$\delta\mu = \mu_n - \mu_N = \frac{\mu_N^2 S(x)\delta Q}{1 + \mu_N S\delta Q} \tag{6.26}$$

where $\delta Q = \frac{\delta Q_N \Delta y \Delta z}{WL}$. For small fluctuations,

$$\delta\mu \sim \mu_N^2 S(x)(\frac{\delta Q_N \Delta y \Delta z}{WL}) \tag{6.27}$$

Substituting the above equation into equation 6.21, the fluctuation in drain current can now be expressed in terms of charge fluctuations alone.

$$\delta I_{D,\Delta V \Delta E} = \frac{W}{L}\mu_N V_{DS}(1 + S(x)\mu_N Q_N)(\frac{\delta Q_N \Delta y \Delta z}{WL}) \tag{6.28}$$

Or expressing in terms of the equivalent gate voltage fluctuation,

$$\delta V_{G,\Delta V \Delta E} = \frac{1}{WLC_{ox}}(1 + \mu_N Q_N S(x))(\delta Q_N \Delta y \Delta z) \tag{6.29}$$

where we have approximated $Q_N = C_{ox}(V_{GS} - V_T)$. The power spectral density of the equivalent gate voltage is

$$S_{V_G,\Delta V \Delta E} = \frac{1}{W^2 L^2 C_{ox}^2}(1 + 2\mu_N Q_N S(x) + \mu_N^2 Q_N^2 S^2(x)) S_{Q_N,\Delta y \Delta z} \qquad (6.30)$$

where we have previously shown that the noise power spectral density of the term $\delta Q_N \Delta y \Delta z$ is

$$S_{Q_N \Delta y \Delta z} = \frac{q^2 \tau_T}{1 + \omega^2 \tau_T^2} N_T f_T (1 - f_T) \Delta V \Delta E \qquad (6.31)$$

Substituting 6.31 into 6.30, the power spectral density of the equivalent gate voltage noise is

$$S_{V_G,\Delta V \Delta E} = \frac{q^2}{W^2 L^2 C_{ox}^2}(1 + 2S(x)\mu_N Q_N + S^2(x)\mu_N^2 Q_N^2) \frac{\tau_T}{1 + \omega^2 \tau_T^2} N_t f_T (1 - f_T) \Delta V \Delta E \qquad (6.32)$$

The total noise spectrum is calculated by integrating over x, y, z, and E. The result is expressed as the sum of three terms.

$$S_{V_G} = S_{V_G 1} + S_{V_G 2} + S_{V_G 3} \qquad (6.33)$$

where

$$S_{V_G 1} = \frac{q^2}{8WLC_{ox}^2 \alpha} \frac{N_T(E_{fn})}{f} \qquad (6.34)$$

$$S_{V_G 2} = \frac{q^2}{WL} \int \frac{2S(x)\mu_N (V_{GS} - V_T)}{C_{ox}} \frac{\tau_T(x)}{1 + \omega^2 \tau_T^2(x)} N_T \, dx \qquad (6.35)$$

$$S_{V_G 3} = \frac{q^2}{WL} \int S^2(x)\mu_N^2 (V_{GS} - V_T)^2 \frac{\tau_T(x)}{1 + \omega^2 \tau_T^2(x)} N_T \, dx \qquad (6.36)$$

The first term yields the pure number fluctuation model derived in the previous section, the second term represents a cross product between number fluctuations and mobility fluctuations, and the final term represents pure mobility fluctuations.

The integral over x of the second and third terms must be carried out numerically as described in section 6.4.1.

The above model contains two parameters that might be considered adjustable: the scattering rate constant, S_0, and the oxide trap density, N_T. However, S_0 can be estimated from published data [97] relating the inversion layer mobility to oxide charge, leaving N_T as the single adjustable parameter.

6.3.1 Predictions of the model

For the case of uniform trap distributions, the model predicts that:

(1) 1/f noise decreases with increasing device area, WL.

(2) For gate voltages near the threshold voltage, 1/f noise is adequately modeled by the pure number fluctuation term which shows an increase in the noise with the square of the oxide thickness.

(3) For large gate oxide thicknesses, the cross-term dominates over the pure mobility fluctuation term yielding a gate voltage dependence of 1/f noise that is approximately linear with increasing gate drive with a slope proportional to $1/C_{ox}$ (figure 6.6).

(4) For thin oxides and large gate biases the pure mobility fluctuation term becomes large relative to the cross-term yielding a gate voltage dependence of 1/f noise that varies approximately as the square of the gate drive. This is illustrated in figure 6.7.

(5) In the regime where the mobility fluctuation term and/or the cross term is large, the noise varies as less than the square of the oxide thickness, in contrast to the prediction of the pure number fluctuation model. Experimentally, the dependence of the noise on oxide thickness has been observed to vary as $S_{V_G} \sim t_{ox}^n$ where n varies from one to two [126,144].

(6) The noise depends on the inversion layer mobility which appears in the cross-term and in the mobility fluctuation term. In addition, the normal field dependence

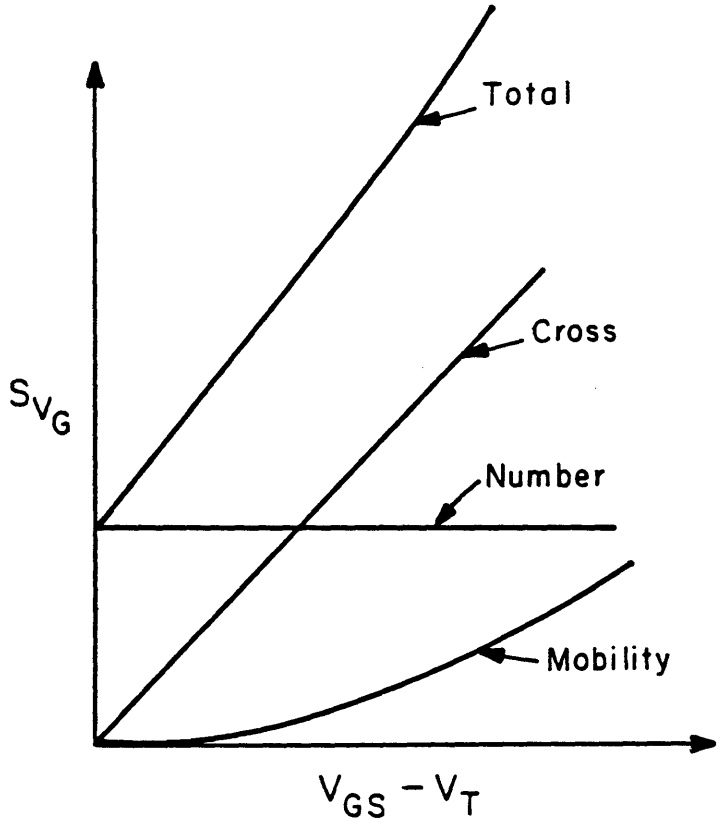

Figure 6.6: Gate voltage dependence of the gate voltage noise power at a given frequency in the regime where the cross term dominates.

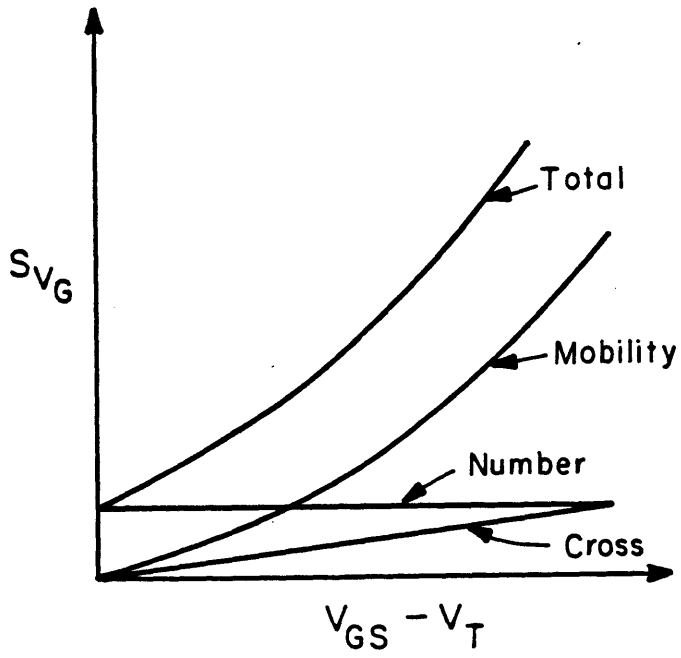

Figure 6.7: Gate voltage dependence of the gate voltage noise power at a given frequency in the regime where the mobility fluctuation term dominates.

of the mobility affects the dependence of the noise on gate drive.

(7) In the regime where the mobility fluctuation and cross terms are large relative to the pure number fluctuation term, the noise can deviate from a pure 1/f spectrum. In particular, the slope of the noise spectrum may be better approximated as $1/f^{\gamma}$ where $\gamma < 1$. The reason for this is that the magnitude of the mobility fluctuation depends on the location of the scattering charge from the Si interface, e.g., the scattering rate is larger for higher frequencies corresponding to charge scattering sites nearer to the interface. Since noise due to mobility fluctuations is larger for higher frequencies the slope of the noise spectrum is predicted to be slightly less than one ($\gamma < 1$) for a uniform trap distribution. The value of γ decreases as the gate bias increases since both cross and pure mobility terms increase with gate bias.

6.3.2 Effect of oxide band bending, mobility fluctuations and nonuniform trap distributions

In the previous sections, it was shown that within the context of the correlated fluctuation model, mobility fluctuations give rise to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum. With increasing gate bias, the magnitude of 1/f noise increases whereas the exponent of the 1/f noise spectrum decreases for the case of uniform trap distributions. It was also shown that within the context of the number fluctuation model, a nonuniform trap distribution gives rise to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum. With increasing gate bias, the 1/f noise magnitude tracks the trap distribution along a line of increasing energy above the conduction band of Si. In addition, with increasing gate bias, the exponent of the 1/f noise spectrum tracks the trap distribution along the length of the window accessed by 1/f noise measurements. Putting together the effects of nonuniform trap distributions, oxide band bending, and mobility fluctuations, the calculated noise can adjusted (by adjusting $N_T(x, E)$) to fit the measured noise.

6.4 Experimental results and extraction of $N_T(x, E)$

In this section, we present experimental results in two parts. In the first part, 1/f noise in n-channel MOSFETs with oxide thicknesses ranging from 14nm to 41nm are characterized. Measurements of the magnitude and exponent of the $1/f^{\gamma}$ spectrum as a function of gate bias are reported. The number fluctuation and the correlated fluctuation models are both used to extract $N_T(x, E)$. In the second part, we investigate 1/f noise in n- and p-channel MOSFETs with 12nm dielectrics which have undergone a nitridation/reoxidation treatment. Due to limitations in the measurement system, we restrict our investigation to low gate biases where mobility fluctuations can be neglected. We then use the model to extract $N_T(x, E)$ for various nitridation/reoxidation conditions.

6.4.1 Procedure for numerical evaluation of the correlated model

The correlated fluctuation model described by equation 6.33 requires the following parameters: S_0, μ_N, and $N_T(x, E)$. The scattering rate constant, S_0, is estimated from the data of Sun and Plummer [97] which relates the measured inversion layer mobility to the measured oxide charge. In order to estimate a value for S_0, we assume that the intentionally introduced oxide charge in the experiments of Sun and Plummer is uniformly distributed within 20 $\AA$ of the interface. It is also assumed that the scattering rate constant obtained from their experiments represent an appropriately weighted average of the various scattering rate terms corresponding to charges located at different distances from the interface. In other words, the average scattering rates are equated to solve for S_0.

$$S(x_1) + \frac{1}{x_2 - x_1} \int_{x_1}^{x_2} S(x)dx = S_{S,P} \tag{6.37}$$

where the limits of the integral are chosen as $x_1 = 0.5\mathring{A}$ and $x_2 = 20\mathring{A}$, the first term on the LHS is the scattering contribution from the region $x \leq 0.5\mathring{A}$, and $S_{S,P}$ is the average scattering rate obtained from the data of Sun and Plummer. Solving for S_0 yields a value of $2.56 \times 10^2\ V \cdot s/coul$. Due to the logarithmic dependence of the scattering rate on x, the estimated value of S_0 is relatively insensitive to the choice of x_1, x_2, and r_{max}.

The calculation of the noise also requires the value of the inversion layer mobility, μ_N. The value of the surface mobility used in the calculation is the measured value of μ_N at the operating point of interest. This avoids the need for a model of the gate voltage dependence of the surface mobility which would involve additional parameters. $N_T(x, E)$ thus represents the only fitting parameter used in adjusting the calculated noise to match the measured noise.

Note that the cross-term and pure mobility fluctuation terms involve an integral over x which must be performed numerically. The procedure involves calculating the noise magnitude for a given frequency by numerical integration using a step size of 0.5 $\mathring{A}$ and the evaluating the integral between 0.5 $\mathring{A}$ and 20 $\mathring{A}$. For a given frequency, f, the greatest contribution to the integral originates from a small region within the dielectric. This is best illustrated in figure 6.8 where the integrand

$$S(x)\frac{\tau_T(x)}{1 + \omega^2\tau_T^2(x)}$$

is plotted as a function of x, where we have assumed that the trap density is spatially uniform . Due to the exponential dependence of the time constant on x, the integrand is a sharply peaked function centered about a depth, x, corresponding to a time constant of 1/f. The lower limit of the integral is chosen to be 0.5 $\mathring{A}$ to avoid the non-physical singularity introduced by the functional form of the scattering rate. The choice of 0.5 $\mathring{A}$, in effect, places an upper bound on the scattering rate of $\sim 3.5 \times 10^3\ V \cdot s/coul$ for charges located at the Si-SiO_2 interface. The contribution of the integral from $x = 0$ to $x = 0.5\mathring{A}$ to the total integral (assuming a constant scattering rate equal to $3.5 \times 10^3\ V \cdot s/coul$ for $x \leq 0.5\mathring{A}$) is less than 0.1 %. Thus

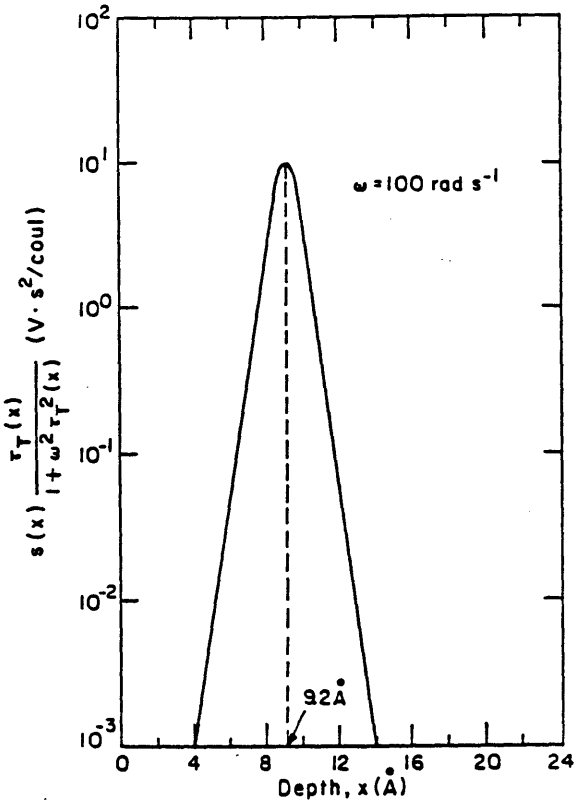

Figure 6.8: Plot of the integrand appearing in the cross term of the correlated fluctuation model. The peak of the function is centered on value of x corresponding to a time constant of 1/f. The greatest contribution to the integral of the function arises from a small region about x.

the use of lower limit of 0.5 $\AA$ is a reasonable approximation.

6.4.2 Experimental methods

The experimental apparatus and the measurement technique are described in section 3.4.4. Here, we discuss issues specific to extracting $N_T(x, E)$. The data required for such a purpose includes a series of 1/f noise sweeps over a range of gate biases where each sweep involves the measurement of the 1/f noise magnitude versus frequency. The data is summarized by plotting (i) the noise magnitude versus gate bias at a given frequency and by plotting (ii) the noise exponent versus gate bias where the noise exponent is found by a least squares fit of the noise spectrum. The

1/f noise measurement technique used in this thesis involves the measurement of the drain voltage noise power in the triode region of operation and its conversion to the equivalent gate voltage noise using the measured value of the small-signal voltage gain of the device. The technique is limited by the fall off of the device voltage gain at higher gate biases when the device is biased in the triode region. In order to obtain a sufficiently broad frequency spectrum, the measurement is performed from 20 Hz, the lower frequency limit of the HP3585 spectrum analyzer, to 50 kHz. The measurement requires additional care at 20 Hz since the spectrum analyzer itself begins to exhibit a small 1/f noise component for $f < 100$ Hz. This 1/f noise component is subtracted from the raw noise data.

6.4.3 1/f noise data and extraction of $N_T(x, E)$

In figure 6.9, the measured equivalent gate voltage noise power at a frequency of 20 Hz is plotted against the gate drive, $V_{GS} - V_T$ for devices with different oxide thicknesses. At a single frequency, the noise originates from a small region within the oxide, a specific distance from the interface. With increasing gate bias, the noise originates from points of increasing energy as previously shown in figure 6.5. Within the context of the number fluctuation model, this behavior is interpreted as an increasing trap density with increasing energy above the conduction band of silicon. Within the context of the correlated fluctuation model, the increasing noise with gate bias can be interpreted as being due to an increasing trap density or due to the increased effects of mobility fluctuations. The extracted trap density from the number fluctuation and correlated fluctuation models are shown in figure 6.10. Note that the extracted trap density from the correlated model increases more gradually with energy than the extracted density from the number fluctuation model. This is due to the effect of mobility fluctuations in the correlated model.

In figure 6.11, the extracted 1/f noise exponent is plotted against the gate drive for devices with various oxide thicknesses. The considerable scatter in the data

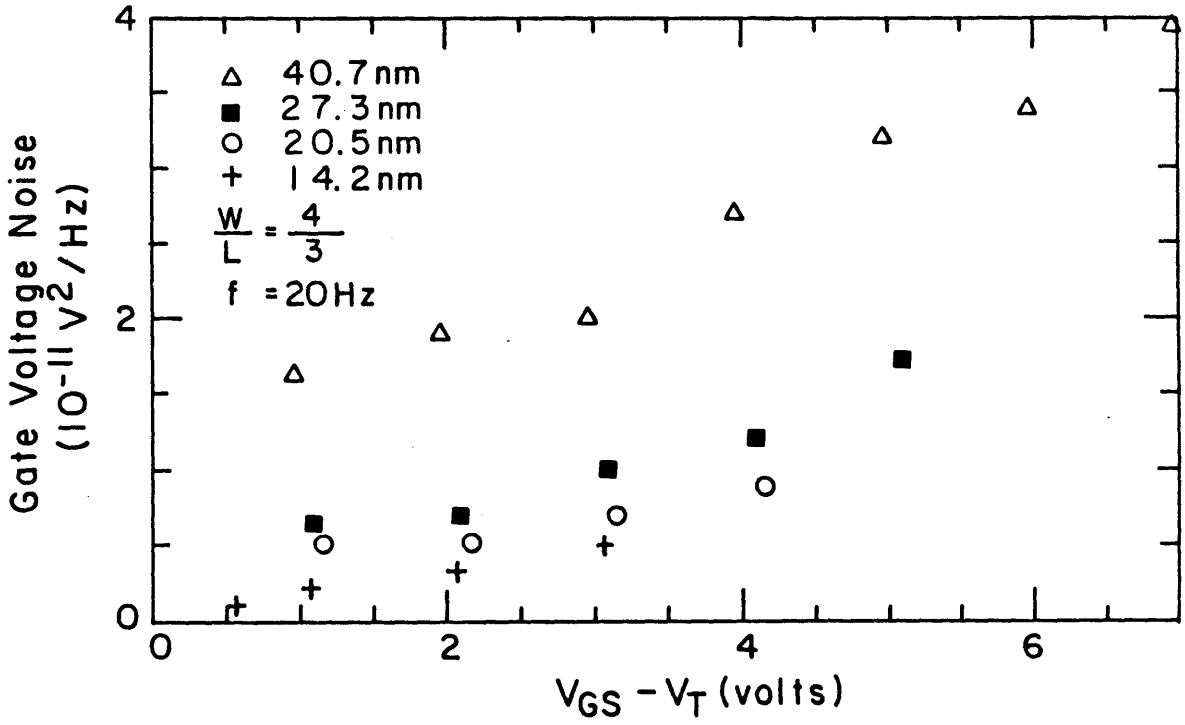

Figure 6.9: Measured gate voltage noise power versus gate voltage. f = 20 Hz.

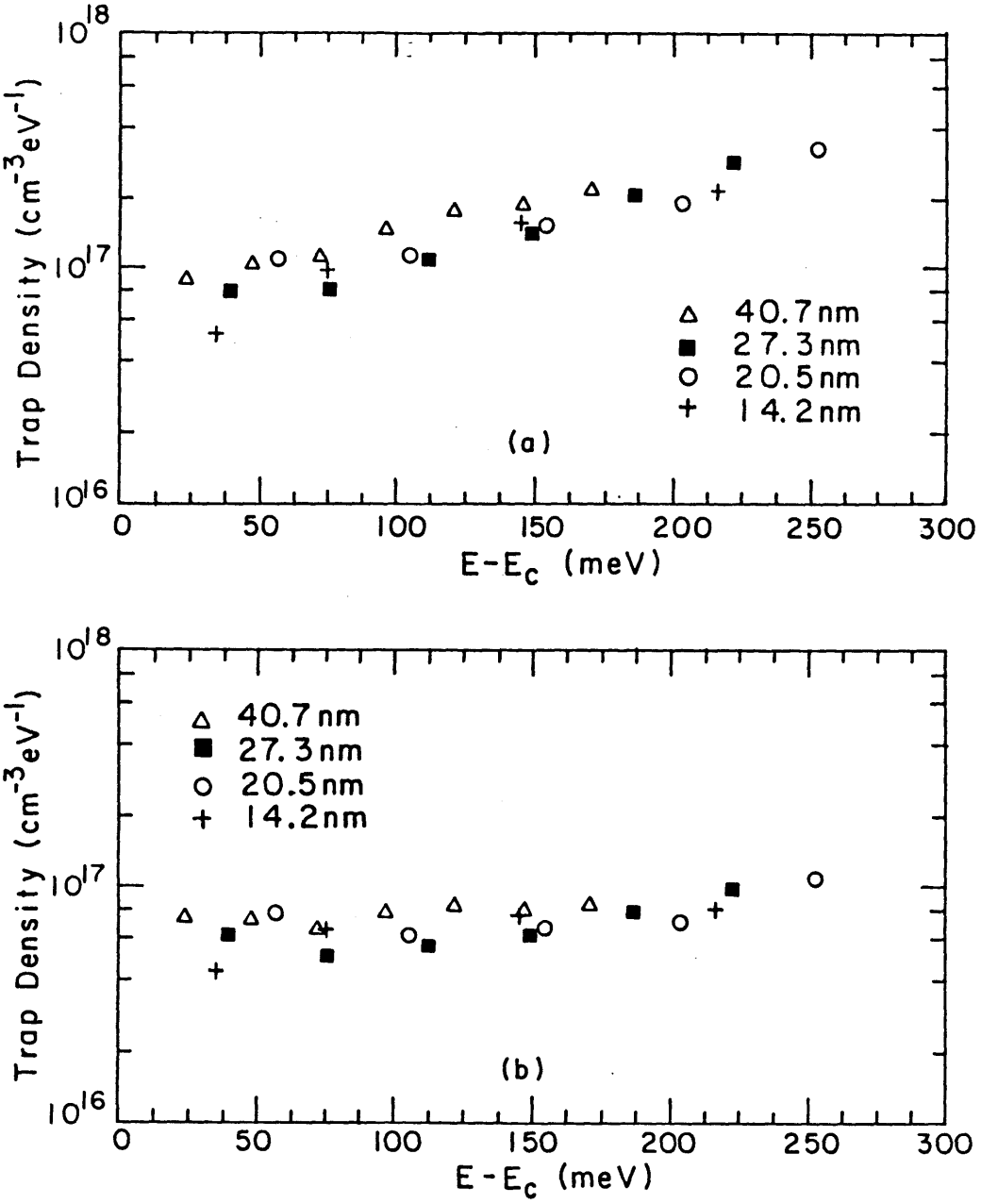

Figure 6.10: Extracted trap density using the data of figure 6.9 using the (a) number fluctuation and (b) correlated fluctuation models.

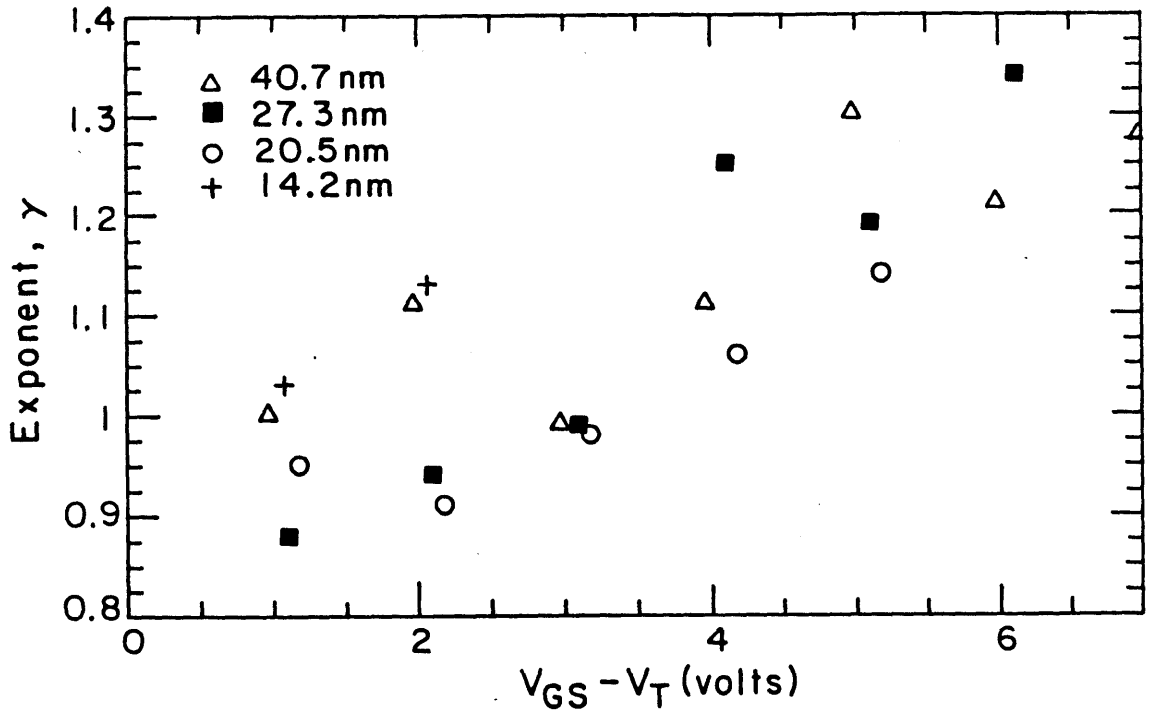

Figure 6.11: Exponent of the 1/f noise spectrum as a function of gate biases for devices with various oxide thickness.

makes it difficult to make conclusive remarks, but it can be seen that the exponent generally increases with gate drive. Both within the number fluctuation and correlated fluctuation models, the increasing value of the exponent is interpreted as a trap distribution that increases along the length of the window probed by 1/f noise measurements. Due to the considerable scatter in the data, we do not attempt to extract the value of the trap density over the entire set of (x, E) values.

The scatter in the exponent values is due to the limited frequency range over which the data can be fit. The frequency range becomes increasingly limited with increasing gate bias due to a decrease in the measured drain voltage noise with increasing gate bias. The problem is further accentuated in thin oxide devices which have lower noise. Possible solutions to this problem are discussed in section 6.5.

6.4.4 Effect of nitridation/reoxidation on 1/f noise.

In this section, we use the above noise models to understand the effect of nitridation and reoxidation of SiO_2 on 1/f noise. In order to avoid the above stated difficulties in measuring the exponent of the 1/f noise spectrum at higher gate biases and to minimize the effect of mobility fluctuation terms, we restrict our measurements to a gate bias near threshold. This allows us to isolate the effect of nitridation and reoxidation on the oxide trap density along a line of increasing (x, E) values near the conduction band of silicon as illustrated in figure 6.4. In these experiments, therefore, n–channel and p–channel transistors were biased in the linear region ($V_{DS} = \pm 0.2V$) under strong inversion conditions ($V_{GS} - V_T = \pm 0.5V$). The noise magnitude is measured in the frequency range of 100 Hz to 50 kHz and the data used to extract $N_T(x, E)$. The lower frequency limit of 100 Hz is used instead of the 20 Hz used in previous measurements to avoid correcting for the 1/f noise component of the spectrum analyzer at low frequencies. Since the small signal voltage gain is sufficient for gate biases near threshold, the use of 100 Hz instead of 20 Hz as the lower frequency limit does not pose a serious limitation in terms of the available frequency range that can be explored.

Figure 6.12 shows the data obtained on n-channel devices with various nitridation/reoxidation conditions. The data are fit with a least squares line to extract the exponent of the 1/f noise spectrum. The estimated error in the value of the exponent is ± 0.05. Given the 1/f noise magnitude and exponent information contained in figure 6.12, the number fluctuation model is used to calculate the trap density, $N_T(x, E)$, shown in figure 6.13. Since the effect of nitridation/reoxidation is compared at constant gate drive, the oxide band bending within each device is approximately the same. Thus, by examining the exponent of the noise spectrum for various devices, we can compare the relative trap distribution along the length of the window probed by 1/f noise.

Note that the 1/f noise in n–channel devices increases with nitridation. This is

interpreted as an increase in the interfacial electron trap density near the conduction band of silicon. Note also that the noise spectrum of the oxide and nitrided oxide devices have similar slopes. This implies that the trap distribution is not significantly altered by nitridation though the trap density increases by as much as one order of magnitude. In the case of the heavy nitridation, a reoxidation decreases the 1/f noise; that is, reoxidation appears to be effective in removing interfacial electron traps. This consistent with the observation of reduced electron trapping with reoxidation during constant current stressing in capacitor structures. Reoxidized nitrided oxide devices have a noise spectrum exponent that is less than for nitrided oxide devices. Thus the reoxidation process appears to preferentially remove traps that are located further from the interface and slightly higher in energy. In the case of the light nitridation, however, a reoxidation does not appear to reduce the 1/f noise, within the resolution of the measurement. This appears to be inconsistent with high-field constant current stressing results which indicate a reduction in electron trapping with reoxidation even for the case of a light nitridation. However, high-field stressing experiments probe traps that are deep in the bulk of the oxide whereas 1/f noise measurements probe near interfacial traps. Thus, the data may be consistent with a reoxidation model which predicts a preferential removal of traps located further from the interface.

Figure 6.14 shows the data obtained on p–channel devices. Again the information contained in figure 6.14 is used to extract the oxide trap density near the valence band of silicon assuming an hole effective mass of $0.5m_0$ and a barrier height of 4.7 eV (figure 6.15). Note that the 1/f noise in p-channel nitrided oxide devices is higher and suggests an increase in the interfacial oxide hole trap density near the valence band of Si as a result of nitridation. The process of reoxidation is effective in removing interfacial hole traps and in the case of the light nitridation combined within a reoxidation the noise is within 25% of the oxide device. Note that the slope of the noise spectrums for the various p-channel devices are similar and $\gamma > 1$

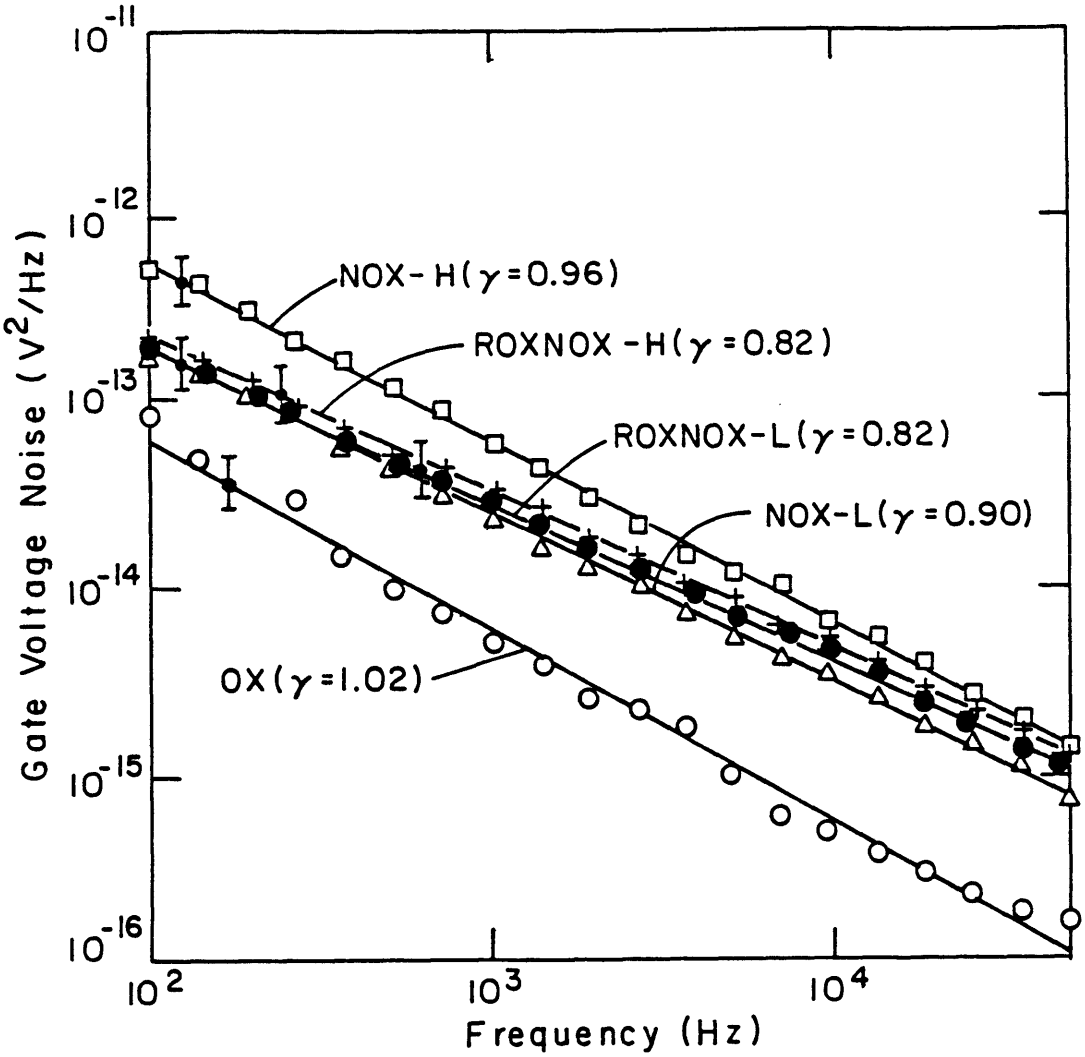

Figure 6.12: 1/f noise in n–channel devices as a function of nitridation and reoxidation conditions. W/L = 20/5; $V_{GS} - V_T$ =0.5V; V_{DS} = 0.2V. The error bar indicates the noise band within which most devices fall for a single wafer. The solid lines indicate a least squares fit to the data and is used to extract the 1/f noise exponent (shown in parenthesis). The error in the value of γ is estimated to be ± 0.05.

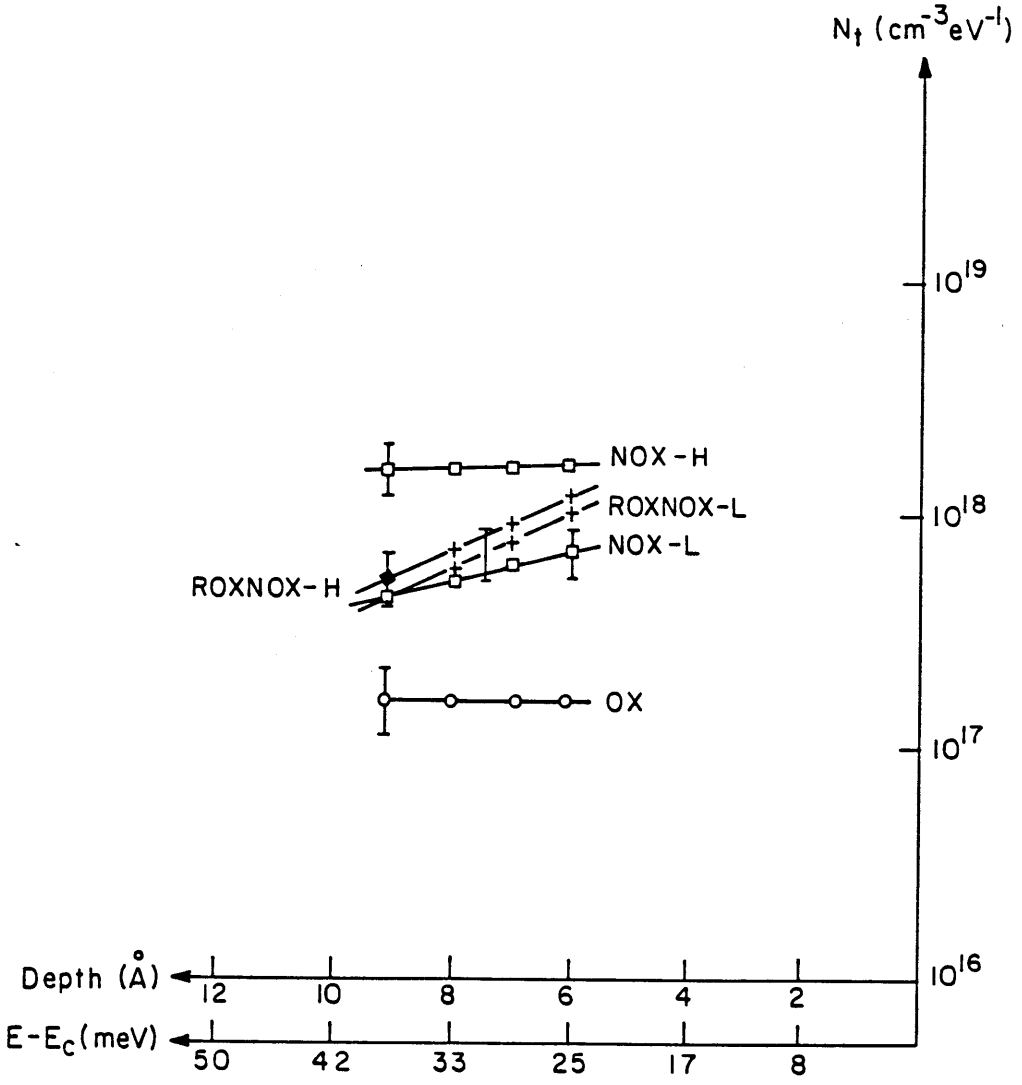

Figure 6.13: Extracted oxide electron trap density along a line of increasing distance from the interface and increasing energy above the conduction band of Si.

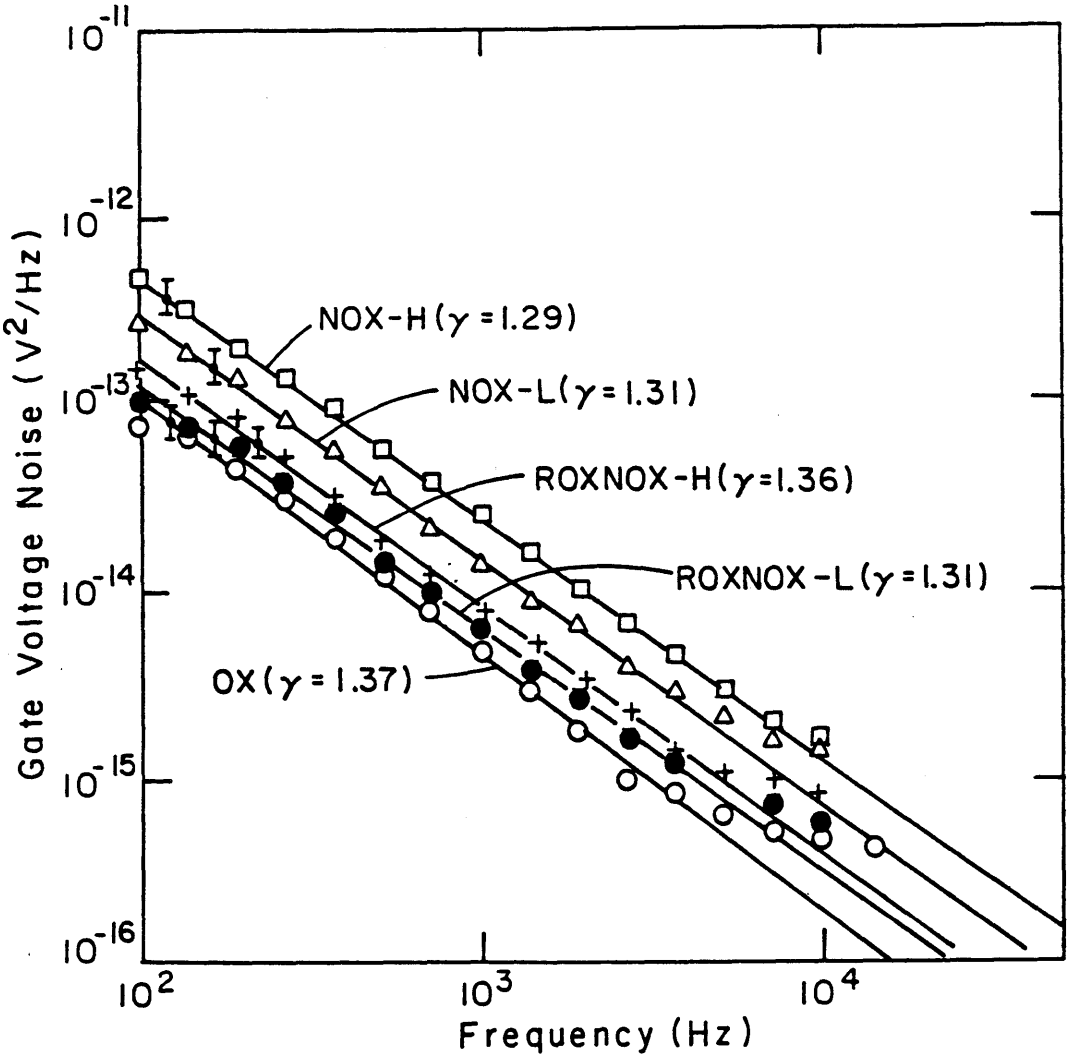

Figure 6.14: 1/f noise spectrum of p-channel devices with various gate dielectrics. W/L = 20/5; $V_{GS} - V_T$ = -0.5V; V_{DS} = -0.2V. The error bar indicates the noise band within which most devices fall for a single wafer. The solid lines indicate a least squares fit to the data and is used to extract the 1/f noise exponent (shown in parenthesis). The error in the value of γ is estimated to be ± 0.05.

giving rise to trap distribution that increases along the line of increasing (x, E). It should also be noted that an increase in hole traps near the valence band of Si due to nitridation has not been previously observed. Constant current stress measurements on capacitors would not detect these hole traps since the electron tunneling current always dominates the hole tunneling current and hence, electron trapping effects dominate hole trapping effects.

Comparing n-channel and p-channel devices, we find that nitridation increases both electron and hole trap densities near the conduction and valence bands of Si, respectively. Hole trap densities, however, are increased to a lesser extent by the nitridation process. Reoxidation appears to be effective in reducing both electron and hole trap densities near the conduction and valence bands, respectively. Electron trap distribution is changed by reoxidation whereas the hole trap distribution does not appear to be affected.

From the viewpoint of improving noise performance, lighter nitridations coupled with a reoxidation result in noise magnitudes approaching those of oxide devices particularly in the case of p-channel devices.

6.4.5 Relationship between 1/f noise and inversion layer mobility

Recall that in the discussion of the electron inversion layer mobility in section 5.1, the presence of acceptor-type electron traps located near the Si conduction band was essential in explaining the observed mobility behavior. From 1/f noise measurements, it is not possible to determine the donor or acceptor nature of traps. However, if we assume that the traps observed in the 1/f noise measurements are acceptor-type (negatively charged when filled) then the behavior of the n-channel 1/f noise is consistent with the mobility model of Schmidt, et. al. [38] which attributed electron mobility degradation in nitrided oxides to the combined effects of fixed charge and electron trap scattering.

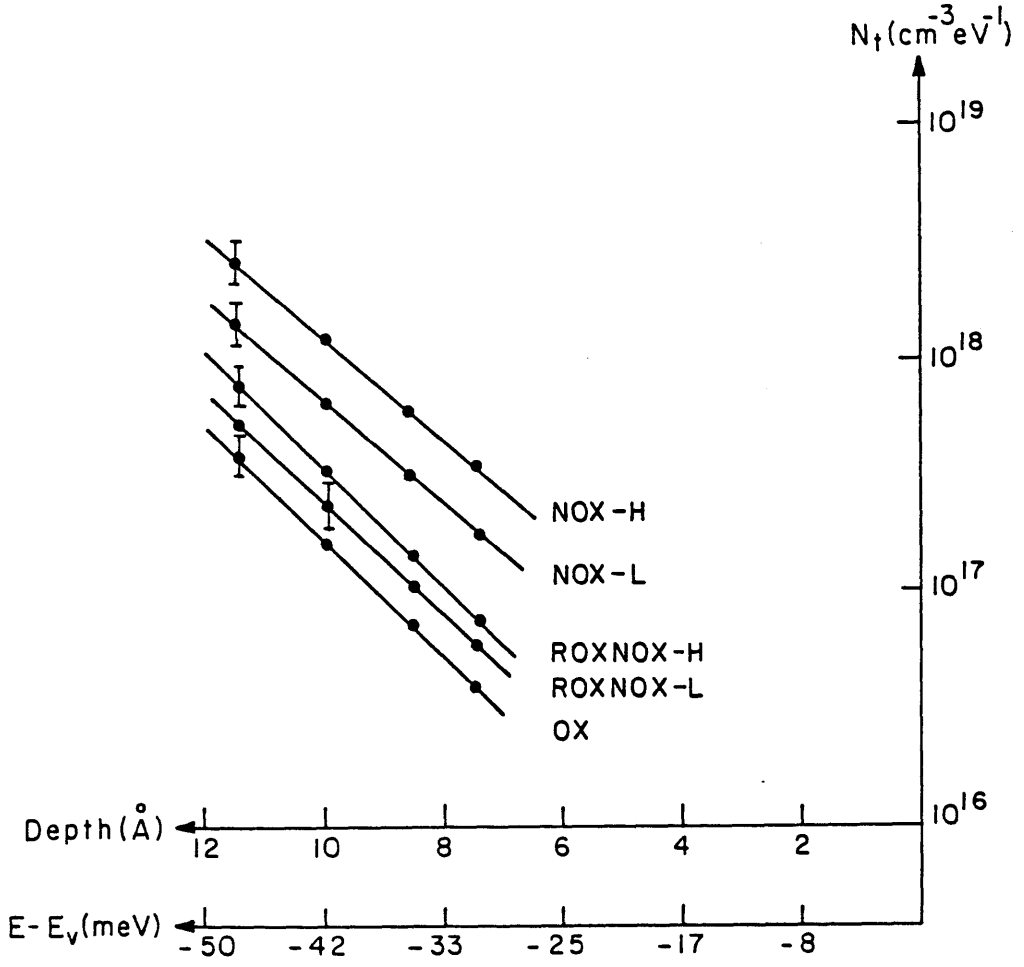

Figure 6.15: Extracted oxide trap density along a line of increasing distance from the interface and increasing energy below the valence band of Si.

The 1/f noise measurements of p-channel devices indicate the presence of the hole traps near the valence band of Si, whereas the mobility model of Schmidt, et. al. assumes that the hole trap density near the valence band is not affected by nitridation. The presence of hole traps near the valence band due to nitridation has not been previously reported. In order to reconcile the 1/f noise measurements with the hole mobility data, recall that the hole mobility appears to be explained by fixed charge effects alone. The hole mobility decreases with nitridation (consistent with increasing fixed charge) and is relatively insensitive to reoxidation (consistent with constant fixed charge), whereas the p-channel noise increases with nitridation and decreases with reoxidation. The discrepancy can be explained if we assume that hole traps observed in the noise measurements are neutral when filled (acceptor-type). Acceptor-type hole traps would not cause scattering of inversion layer holes but would cause 1/f noise. Further modeling and independent confirmation of the donor or acceptor nature of these traps is required to substantiate these speculations.

6.5 Problems and suggestions for future work

The primary problem encountered in the extraction of $N_T(x, E)$ arose from the considerable scatter in the value of the 1/f noise exponent at high gate biases. This was due to the measurement of the drain voltage noise spectrum which decreases with increasing gate bias, limiting the frequency range over which the data could be fit. A possible solution to this problem is to devise a measurement technique that directly measures the gate voltage noise spectrum which increases with gate bias.

The extent to which mobility fluctuations are important to 1/f noise depends on our estimate of the scattering rate constant, S_0. An additional weakness is the use of a relationship between the inversion layer mobility and the location of the oxide trapped charge which contains a singularity at $x = 0$. A more accurate relationship between the surface mobility and oxide trapped charge is needed. In addition, an in-

dependent means of confirming the importance of mobility fluctuations is required. A possible experiment to explore the importance of mobility fluctuations is to correlate the 1/f noise in MOSFETs with the charge transfer efficiency of similarly processed MOS charge-coupled devices (CCDs). Whereas 1/f noise in MOSFETs depends on both number and mobility fluctuation effects, the charge transfer efficiency of CDDs depends only on the number of carriers trapped by oxide traps. An additional experiment might include investigating the temperature dependence of 1/f noise. The variation of temperature would greatly affect the mobility without affecting oxide band bending and tunneling parameters.

6.6 Summary

In this chapter, we investigated the use of 1/f noise measurements as a tool in extracting the oxide trap density and distribution in space and energy near the conduction and valence bands of silicon. We began by reviewing the number fluctuation model of 1/f noise. It was shown that oxide band bending in devices with nonuniform oxide trap distributions led to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum. We then explored an extension of the 1/f noise theory based on the McWhorter tunneling model which included both number fluctuations and correlated mobility fluctuations. The predictions of the theory were discussed and compared to the predictions of the pure number fluctuation model. It was shown that the correlated fluctuation model also predicts a gate voltage dependence in the magnitude and exponent of the 1/f noise spectrum even for uniform trap distributions. Both the number and correlated fluctuation models were used to extract the oxide trap distribution in oxide devices with various oxide thickness. However, due to difficulties in reliably measuring the exponent of the 1/f noise spectrum, the method was limited in the (x, E) space that could be explored. The model was then used to interpret the effects of gate oxide nitridation and re-

oxidation on the 1/f noise properties of MOSFETs. It was found that nitridation increases the interfacial electron trap density in the oxide near the conduction band of silicon by a factor of 2-10. Reoxidation decreases the nitridation-induced interfacial electron trap density. Nitridation was also found to increase the interfacial hole trap density near the valence band of silicon by a factor of 2-6. Reoxidation reduces the nitridation-induced hole trap density to values within 25% of oxide values for light nitridations. In the final section, the limitations of the 1/f noise method and suggestions for future improvements in the technique were discussed.

Chapter 7

Conclusions

7.1 Summary

This thesis investigated the electrical properties of nitrided oxides and reoxidized nitrided oxides as MOS gate dielectrics. The focus of the discussion was on the reliability and 1/f noise properties of such devices.

The growth of the various dielectrics was accomplished in a special furnace system constructed for operation at low pressure (0.01 - 0.1 atm.). Anneals were performed at 950 °C in pure ammonia, oxygen, or inert (nitrogen or argon) ambients.

We used low pressure nitridation to explore the pre-turnaround regime of the nitridation process. Nitrided oxides formed under low pressure conditions differed from atmospheric pressure nitrided oxides in a number of respects. First, the fixed charge and interface state exhibited a turnaround behavior with increasing nitridation similar to atmospheric nitridation, but this turnaround occurred more gradually. This suggested a sufficient process window in the early stages of the nitridation process (pre-turnaround regime). Second, low pressure nitrided oxides typically did not exhibit a suppression of interface state generation under electrical stress unless a lengthy nitridation was performed. However, when coupled with a reoxidation, short nitridations dramatically suppressed interface state generation. Moreover,

reoxidation eliminated electron trapping, as expected from previous work. We exploited the above differences to develop a dielectric process which exhibited greatly improved reliability over conventional silicon dioxide devices. The amount of interface state generation under electrical stress was reduced by a factor of 25 compared to silicon dioxide devices and charge trapping was virtually eliminated. In addition, the breakdown strength was somewhat improved compared to oxide and the charge-to-breakdown was about one order of magnitude better than oxide. While the nitridation/reoxidation process generally degrades the initial interfacial characteristics of the oxide, we were able to achieve a fixed charge density as low as $\sim$ 2-3 $\times$ 10^{11} cm^{-2} and midgap interface state density as low as $\sim$ 3 $\times$ 10^{10} cm^{-2} eV^{-1}.

The procedure by which we optimized the dielectric processing was described and reliability-performance tradeoffs outlined. It was shown that lighter nitridation result in better performance (lower fixed charge and interface state density) but at the expense of reduced reliability improvement (less suppression of interface state generation and less reduction in charge trapping).

The low pressure nitridation/reoxidation process also showed greater resistance to ionizing radiation both in terms of interface state and fixed charge generation, suggesting that even light nitridations can be used to achieve improved radiation hardness.

Finally, the low pressure process was shown to have better control compared to a dilute process under equivalent partial pressures of ammonia and oxygen. However, the dilute process showed reduced fixed charge and interface state density. In addition, the dilute process exhibited reduced interface state generation and electron trapping under high-field stressing, a result suggestive of the presence of oxygen contamination during the nitridation process.

In order to demonstrate the viability of such gate dielectrics in scaled transistors, certain gate dielectrics were used in the fabrication of NMOS and PMOS transistors. It was found that reoxidized nitrided oxide gate dielectrics improve

the projected operating life of short-channel transistors by an order of magnitude over oxide devices, with only a 20 % degradation in the inversion layer mobility of devices.

We also investigated the use of 1/f noise measurements as a tool in extracting the oxide trap density and distribution in space and energy near the conduction and valence bands of silicon. We began by reviewing the McWhoeter number fluctuation model of 1/f noise. It was shown that oxide band bending in devices with nonuniform oxide trap distributions led to a gate voltage dependence in the magnitude and exponent of the $1/f^{\gamma}$ noise spectrum. We then explored an extension of the 1/f noise theory based on the McWhorter tunneling model which included both number fluctuations and correlated mobility fluctuations. The predictions of the theory were discussed and compared to the predictions of the pure number fluctuation model. It was shown that the correlated fluctuation model also predicts a gate voltage dependence in the magnitude and exponent of the 1/f noise spectrum even for uniform trap distributions. Both the number and correlated fluctuation models were used to extract the oxide trap distribution in oxide devices with various oxide thickness. However, due to difficulties in reliably measuring the exponent of the 1/f noise spectrum, the method was limited in the (x, E) space that could be explored. The model was then used to interpret the effects of gate oxide nitridation and reoxidation on the 1/f noise properties of MOSFETs. It was found that nitridation increases the interfacial electron trap density in the oxide near the conduction band of silicon by a factor of 2-10. Reoxidation decreases the nitridation-induced interfacial electron trap density. Nitridation was also found to increase the interfacial hole trap density near the valence band of silicon by a factor of 2-6. Reoxidation reduces the nitridation-induced hole trap density to values within 25% of oxide values for light nitridations. The limitations of the 1/f noise method and suggestions for future improvements in the technique were also discussed.

7.2 Future Work

The fact that light, low pressure nitridations coupled with reoxidations result in dramatic improvements in device reliability without significantly compromising performance, suggest that other techniques for achieving light nitridations and reoxidations may behave similarly. As such, lower temperature (850 °C) nitridation/reoxidation processes as well as rapid thermal nitridation/reoxidation processes may be worth investigating as alternatives to low pressure processing.

Our study of dilute nitridations showed that oxygen contamination results in nitrided oxides that appear partially reoxidized with desirable but variable characteristics. By controlling the level of oxygen contamination during the nitridation cycle, it may be possible to develop a one-step nitridation/reoxidation process.

Clues to further improvement in reliability might be obtained by developing better models for the mechanisms responsible for reliability improvement in reoxidized nitrided oxides. A possibly important component to such a model may be the role of hydrogen which has received relatively scarce attention. Particularly helpful would be to study correlations between the presence of hydrogen in the dielectric and the reliability of devices.

The correlated 1/f noise model considered in this thesis suggests a wide range of experiments that could be performed to verify its validity. Experiments over temperature and over a range of bias conditions including subthreshold might be used to separate the effects of number and mobility fluctuations. Other experiments might include comparing 1/f noise in MOSFETs with the charge transfer efficiency of charge coupled devices or comparing 1/f noise in MOSFETs with threshold voltage hysteresis in MOSFETs undergoing large voltage swings. While the correlated model appears successful in extracting $N_T(x, E)$ over a limited range, it remains to be seen whether it can extract oxide trap density and distribution from 1/f noise data taken over a wide range of gate biases and oxide thicknesses.

Reoxidized nitrided oxides may also be applied to other device structures such

as EEPROMs or polysilicon-emitter bipolar transistors.

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Appendix A

Process Flow For Etched Field Oxide Capacitors

0) Label Wafers (1-N) n-type <100>, 10-40 ohm-cm

Wafer Thickness :_____ (.32 mm)

Wafer Rs :_____ (500 ohms/square)

1) Field Oxidation

RCA Clean with HF dip

Oxidation (lower tube)

HCl clean oxidation furnace

Field Oxidation dry O2 @950C for 30 min

wet O2 @950C for 200 min

dry O2 @950C for 30 min

N2 @950C for 30 min

Field Oxide :_____ (5000 A)

3) Define Gate Region

PRAP, Contact Aligner, Small Mask (Oxide - Dark Field)

Standard Resolution Aligner - channel 1 12 sec

Inspect Resist

Etch Gate Dielectric Areas

Etch in Buffered HF 7:1 NH4F/HF (1500A/min)

Inspect for etch completion

Resist strip A20 solution @80C for 5 min

DIH20 rinse and N2 blow dry

Field Isolation Complete

5) Gate Oxidation/Nitridation

RCA clean with HF dip (short ~20sec 10:1 DIH20/HF)

See Oxidation/Nitridation Process Sheet

6) LPCVD Polysilicon Deposition

Immediately Deposit 5000A polysilicon (undoped)

7) Remove Backside Poly and Oxide

Protective Layer for Frontside of Wafer

Dehydrate @200C for 30 min

Spin KTI1370 30 sec 5000 rpm

Softbake @90C for 20 min

Plasma etch backside polysilicon

Day etcher SF6 @200W for 2-3min

loading =_____ (211)

tuning =_____ (245)

Etch backside oxide in BOE

7:1 NH4F/HF (1500A/min)

Strip frontside resist

acetone>methonal>DIH20 rinse

8) Dope Polysilicon

Organic clean (only)

6:1:1 DIH20/H202/NH40H @80C for 20min

DIH20 rinse and N2 blow dry

Phosphorous Predeposition (top tube)

N2, 925 C, 60min (40 rotameter scale)

02, 925 C, 10min (6.3 rotameter scale)

N2, 925 C, 15min (40 rotameter scale)

P-glass strip

Dip 10:1 DOH20/HF

DIH20 rinse and N2 blow dry

9) Polysilicon Gate

PRAP, Contact Aligner, Poly Mask (large - clear field)

Standard Resolution Aligner channel 1 12 sec

Inspect Resist

Plasma etch frontside polysilicon

Day etcher SF6 @200W for 2-3min

loading =_____ (211)

tuning =_____ (245)

Inspect for etch completion

Resist strip A20 solution @80C for 5 min

DIH20 rinse and N2 blow dry

10)Sinter

Forming Gas (20% H2 80% N2), 450 C, 50 min

Appendix B

Process Flow For LOCOS-Isolated Capacitors

STARTING MATERIAL: n-type 100

STEP #	STEP DESCRIPTION[1]
1	Stress Relief Oxide
2	LPCVD Silicon Nitride
3	Active Area Pattern
4	Nitride Plasma Etch
5	Resist Ash
6	Field Oxide
7	Nitride Wet Etch
8	Stress Relief Oxide Wet Etch
9	Gate Oxide (Oxidation, Nitridation, and Reoxidation)
10	LPCVD Polysilicon
11	Resist Coat

[1]Detailed description of the these standard steps can be obtained from the MIT Integrated Circuit Laboratory.

12	Backside Oxide Wet Etch
13	Backside Poly Plasma Etc
14	Backside Oxide Wet Etch
15	Resist Ash
16	Phosphorus Deposition
17	Phosphorus Glass Wet Etch
18	Poly Pattern
19	Poly Plasma Etch
20	Resist Ash
21	Sinter Metal

Appendix C

Process Flow For NMOS and PMOS Runs

Wafer labels: (nm) nmos field implant
(pm) pmos field implant
20 product wafers

1. **Label Wafers (20 product : 9 nmos, 11 pmos.)**

   p-type, < 100 >, 10–40 Ω-cm
   wafer thickness : (0.32mm)
   wafer sheet resistivity : (500Ω/□)

2. **Stress–Relief Oxidation (all)**

   RCA clean
   oxidation (lower tube)
   Dry O_2, 950°C, 100 min
   N_2, 950°C, 30 min

stress–relief oxide (nm,pm) : (40nm)

3. Deposit LPCVD Nitride (all + nitride monitor)

RCA clean (No HF)

LPCVD nitride, 45 min

nitride thickness (monitor) : (150nm)

4. Pattern Nitride (all - nm,pm)

diffusion mask

HMDS, 1370 photoresist, prebake

GCA mask: SLG84ND

job: RAJ1ND

postbake

plasma etch nitride (all)

10:1 HF, 30 sec

LAM etch: 150sccm SF_6, 150sccm He

300mTorr, 250W, 1.5cm gap

~200 nm/min, endpoint detection

stress–relief oxide : (35nm)

5. Field Implant (all)

nmos implant : B^+, 70KeV, 2×10^{13} cm^{-2}

pmos implant : P, 60KeV, 1×10^{13} cm^{-2}

strip resist

Day etch: O_2, 100mTorr, 200W, 5 min

all wafers at same time

Loading 13.8, Tuning 25.3

6. Field Oxidation (all)

RCA clean (No HF)

oxidation (lower tube)

Dry O_2, 950°C, 30 min

Wet O_2, 950°C, 200 min

Dry O_2, 950°C, 30 min

N_2, 950°C, 30 min

field oxide : (500nm)

7. Nitride Strip (all)

10:1 HF, 30 sec

Transetch, 180°C, 15 min, keep boiling

field oxide : (490nm)

resistivity(nm) : ($\Omega/\square$)

resistivity(pm) : ($\Omega/\square$)

8. Gate Oxidation and Poly Deposition (all + 4 oxide monitors)

RCA clean

etch SR oxide: 10:1 HF, 90–150 sec, check sheeting

oxidation/nitridation

Control oxide :950°C, O_2, 76torr, 35 min

Nitrided-oxide :

control oxide(tox3) : (10nm)

nitrided-oxide(tno3) : (10nm)

field oxide : (440nm)

deposit poly: 5000Å

poly thickness (monitor) : (500nm)

9. Dope Polysilicon (all)

RCA clean

phosphorus deposition (upper tube)

N_2, 925°C, 60 min

O_2, 925°C, 15 min

N_2, 925°C, 10 min

strip phosphorus glass

10:1 HF, 30 sec, check sheeting

10. Pattern Poly (all - nm, pm)

poly mask

1370 photoresist, prebake

GCA mask SLG84NP

job RAJ1ND

postbake

plasma etch poly (all)

Day etch O_2, 100mTorr, 100W, 60 sec (descum)

LAM etch: 130 sccm CCl_4, 20 sccm O_2, 130 sccm He

200 mTorr, 300W, 1.5 cm gap

~350 nm/min, endpoint detection

strip resist (*Leave resist on pmos wafers)*

Day etch: O_2, 100mTorr, 200W, 5 min

all wafers at same time

Loading 13.8, Tuning 25.3

source/drain oxide : (20nm)

field oxide : (430nm)

11. Source/Drain Implant (all)

nmos implant : As, 90KeV, 7×10^{15} cm^{-2}

pmos implant : BF2, 30KeV, 7×10^{15} cm^{-2}

em strip resist pmos wafers only

12. Backside Strip (all - nm, pm)

Coat front with KTI 732 resist and softbake

strip poly

30 sec in BOE

LAM etch: 130 sccm CCl_4, 20 sccm O_2, 130 sccm He

200 mTorr, 300W, 1.5 cm gap

~350 nm/min, endpoint detection

strip oxide

7:1 NH_4/HF, 30 sec, check sheeting

strip resist

acetone, methonol, DI rinse

13. **CVD Oxide (all)**

RCA clean (No HF)

oxidation (lower tube)

Dry O_2, 900°C, 30 min

N_2, 900°C, 30 min

deposit CVD oxide

preheat at 400°C, 30 min

deposit at 400°C, 6 min

source/drain oxide : (620nm)

field oxide : (1030nm)

14. **Densify CVD Oxide (all)**

RCA clean (No HF)

oxidation (lower tube)

Dry O_2, 950°C, 30 min

N_2, 950°C, 15 min

source/drain oxide : (570nm)

field oxide : (980nm)

15. **Contacts (all - nm, pm)**

contact mask

HMDS, 1370 photoresist, prebake

GCA mask SLG84NC

job RAJ1ND

postbake

two–step etch contacts

Descum: O_2, 100mtorr, 200W, 30sec.

5 min. in BOE

strip resist

A–20, 90°C, 5 min

source/drain R_s : ($30\Omega/\square$)

16. Contact Plugs (*nmos only*)

RCA clean

phosphorus deposition (upper tube)

N_2, 925°C, 60 min

O_2, 925°C, 15 min

N_2, 925°C, 10 min

strip phosphorus glass

7:1 NH_4/HF, 5 sec, check sheeting

contact R_s (1) : ($20\Omega/\square$)

field oxide (2) : (970nm)

17. Al–Si–Cu Deposition (all)

organic clean pmos

rinse in methanol, and blow dry

sputter Al–Si–Cu

1.8 kV, 5mTorr, 3×10^{-6} Torr base pressure

clean target: 15 min at 600W

deposit: ~60 min at 200W

Al–Si–Cu R_s : ($32m\Omega$)

18. **Pattern Al–Si–Cu (all - nm, pm)**

metal mask

1370 photoresist, prebake

GCA mask SLG84NM

job RAJ1NP

postbake

etch Al–Si–Cu

PAN etch, 5 min

Day etch: SF_6, 70mTorr, 50W, 2 min

four wafers at a time

loading 21.2, tuning 41.9

strip resist

A–20, 90°C, 5 min

field oxide (2) : (970nm)

19. **Contact Sinter (all - nm, pm)**

rinse well in DH_2O

sinter: 80% N_2: 20% H_2, 450°C, 30 min

Photoresist Application Procedure

Dehydration bake: 200°C, 30 min

Spin off particulates

Flood wafer with HMDS: 5000RPM, 30 sec

Coat wafer with KTI1370: 5000RPM, 30 sec

Softbake: 10 min, room temperature

25 min, 90°C

Expose: 0.3 sec for oxide, nitride

0.25 sec for poly, metal

Develop: 60 sec in MF312:DH_2O, 1:1

Hardbake: 25 min, 120°C