Improving the Control Strategy for a Four-Switch Buck-Boost Converter

by

Michael Peter Whitaker

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Abstract

The four-switch buck-boost converter, such as implemented with the Linear Technology LTC3440 integrated circuit, is useful in many applications. While this topology can be highly efficient, new strategies for controlling it could decrease power losses even more. The strategy proposed for this thesis involves the use of level shifted triangle waves and high speed comparators to achieve a narrower buck-boost region than achieved in previous control IC's such as the LTC3440. Reducing the amount of operation in this regime is desirable because it is the most inefficient mode of operation of the converter. This potentially simpler solution will allow for resources to be used to improve the performance of other elements of the circuit, allowing for potential increases in efficiency.

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Title: Associate Professor

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Chapter 1

Introduction

In many modern portable electronics devices the need arises for efficient DC to DC converters. These devices often use batteries which do not provide a constant voltage over time. Thus it is necessary to regulate an output voltage which can be above, below, or equal to the battery voltage such that it meets a device's required specification. This can be done with a buck-boost DC to DC converter in which low loss conversion of a DC battery voltage can be achieved. It is the aim of this thesis to examine an existing voltage mode buck-boost converter and to explore a new method of controlling the converter. This new method will involve a simpler control architecture compared to those currently in use and should save on resources such as die area and quiescent current. This extra area and current could be used to improve other parts of the converter. In addition the new control scheme may reduce power loss in the converter. This thesis studies the feasibility of the new control method and determines whether it could be used instead of the present architecture.

Despite tremendous advances in power conversion, the demands of many applications make it important to achieve even small improvements in efficiency by reducing loss as much as possible. As designs become increasingly complex, studying simpler solutions may yield designs with less potential problems and better results. This project has context in previous research conducted by Linear Technology Corporation, as this thesis is being supported by Linear Technology Corporation through the VI-A program.

1.1 Previous Work

Linear Technology has done extensive research on this topic and has a product, the LTC3440, which is a buck-boost regulator [9]. The LTC3440 uses four switches that allow energy to be transferred from the supply voltage to an output with an inductor. This topology is shown in Figure 1-1. Different switching sequences provide different converter modes that regulate the output voltage.

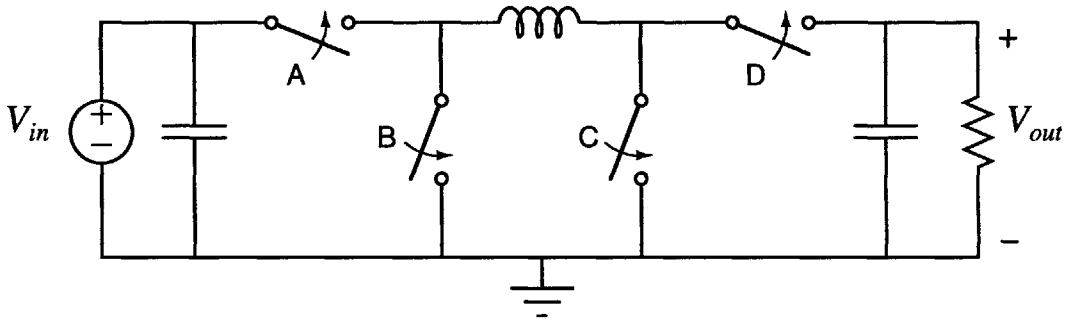

Figure 1-1: Buck-boost converter with switches A, B, C, and D

The four switches can be configured such that the converter operates in buck mode, boost mode, or buck-boost mode. With switch D on and switch C off all of the time, switches A and B can be pulse width modulated to form a buck converter, which steps the input voltage down. With switch A on and switch B off all of the time, switches C and D can be pulse width modulated to form a boost converter, which steps the input voltage up. Finally, the converter can operate such that all switches turn on and off in a given cycle to form a buck-boost mode in which the input voltage can be stepped up, stepped down, or replicated at the output. These three modes allow the converter to regulate a constant output voltage for a wide range of inputs. This is desirable because the input voltage is typically a battery whose voltage can change as it is used.

The conversion ratio, V_{out}/V_{in}, can be determined as a function of the switching times. The switches are operated such that at any given time switches A and C, A and D, B and C, or B and D are on. This will cause the voltage across the inductor to be V_{in}, $V_{in} - V_{out}$, 0, and $-V_{out}$ respectively. Note that the combinations AB and CD are not allowed as this connects the input or output directly to ground through the switches causing shoot-through current, a damaging effect. The average inductor voltage can be expressed as follows [2, p.

18]:

$$\overline{V_{ind}} = \frac{V_{AC}t_{AC} + V_{AD}t_{AD} + V_{BC}t_{BC} + V_{BD}t_{BD}}{T}$$

Since in periodic steady state the average voltage across the inductor is zero, a conversion ratio based on the switching times can be derived after substituting the appropriate inductor voltages [2, p. 18].

$$\frac{V_{out}}{V_{in}} = \frac{t_{AC} + t_{AD}}{t_{AD} + t_{BD}} = \frac{t_A}{t_D}$$

Thus, to achieve buck mode switch D can be left on for the whole cycle and switch A can be on for a length $D_A T$ of the cycle while B is on for $(1 - D_A)T$. Since the duty cycle of switch A is D_A, the conversion ratio will be D_A which is normal for a buck converter. If switch A is on constantly and D is on for only part of the cycle, D_D, then the conversion ratio will be $1/D_D$ and a boost condition will occur. When switch A is off for part of the cycle and switch D is off for part of the cycle the converter operates in the buck-boost region where the output voltage can be lower than ($t_A < t_D$), higher than ($t_A > t_D$), or the same ($t_A = t_D$) as the input voltage. This mode is the most important mode to look at since all four of the switches will be on at different points during the cycle. When more switches operate there is more loss. Thus it is desirable to minimize the time a converter spends in the buck-boost region. Other converters of this type may operate in a four switch region all of the time, never moving into a strictly buck or boost region, and exhibit more loss.

Given this four switch converter with its three modes of operation there remains the problem of how to choose between modes when regulating the output voltage. Addressing this problem is the heart of this thesis project. The existing LTC3440 buck-boost converter is controlled by synchronous sawtooth waveforms that are out of phase with each other; the present scheme is based on a variation of this approach. These two signals are fed into comparators that control logic circuitry which ultimately turns the switches on and off. By using one waveform to choose whether switch A or B is on and another to determine whether switch C or D is on, each of the three modes can be selected. A control voltage, V_c, is created from the output with an error amplifier and creates a negative feedback loop. As the output deviates from the desired voltage this control voltage will vary to cause the converter to change its conversion ratio in a given mode or to switch modes entirely in order to achieve the desired output voltage. A block diagram of this process is shown in Figure

1-2. The output voltage and a reference voltage are inputs to an error amplifier whose output is V_c. $V_{Saw_{AB}}$ and $V_{Saw_{CD}}$ are sawtooth waveforms and are inputs to comparators that drive logic circuitry which produces the drive signals for the switches.

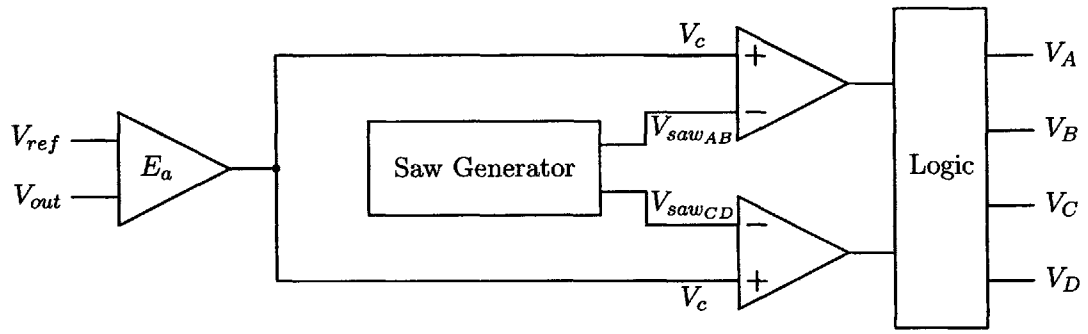

Figure 1-2: Block diagram of control scheme for a buck-boost converter.

In the purest implementation the comparators can look at the sawtooth waveforms and compare the voltage of each sawtooth to the error signal and generate a clean PWM output. However a comparator exhibits nonlinear propagation delays at high and low output duty cycles. Near these ends of operation the propagation delays can vary substantially from those for the middle of the range due to the absence of sufficient overdrive. This will cause the duty cycle of the PWM waveform to be nonlinear at the ends of operation as shown in Figure 1-3.

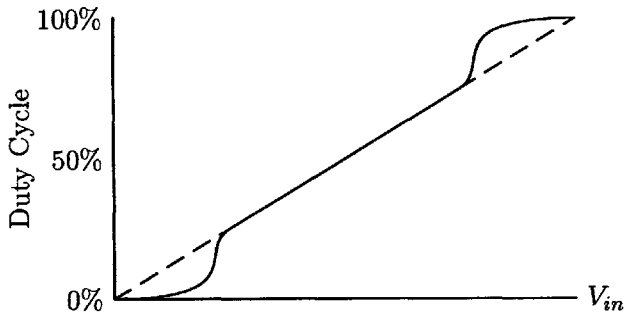

Figure 1-3: Duty ratio vs. input voltage for a comparator [3, p. 3]

To avoid this problem a multiplexer can be used to select when to use a sawtooth waveform for duty cycle control. By not choosing to use the ends of the sawtooth waveform the multiplexer can be used to effectively chop away the regions where the comparator propagation delays are nonlinear. This is best illustrated with the following two figures.

In Figure 1-4 two sawtooth waveforms are shown that are 180 degrees out of phase.

Pieces of these waveforms are selected to create a new pair of overlapping sawtooth waveforms as illustrated in Figure 1-5. In particular, on the vertical axis there are four voltage levels shown, V_{min}, V_{buck}, V_{boost}, and V_{max}. One of the sawtooths of Figure 1-4 is utilized in the range between V_{min} and V_{boost} and the other is utilized between V_{buck} and V_{max} via the multiplexing scheme.

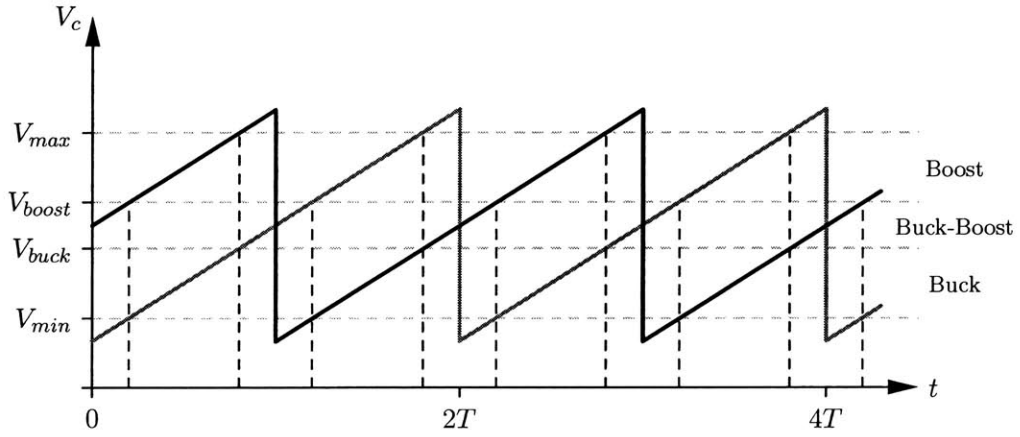

Figure 1-4: Sawtooth waveforms for converter control used in the LTC3440 [2, p. 15]

This results in the effective waveforms shown in Figure 1-5 which would have an overlap between levels V_{buck} and V_{boost}. Though these effective waveforms can be used to better understand what is going on, they are not actually generated in the system. Instead the sawtooths are fed into comparators whose outputs are multiplexed to result in the same effect on the control of the switches. An overview of this circuitry is omitted here for brevity.

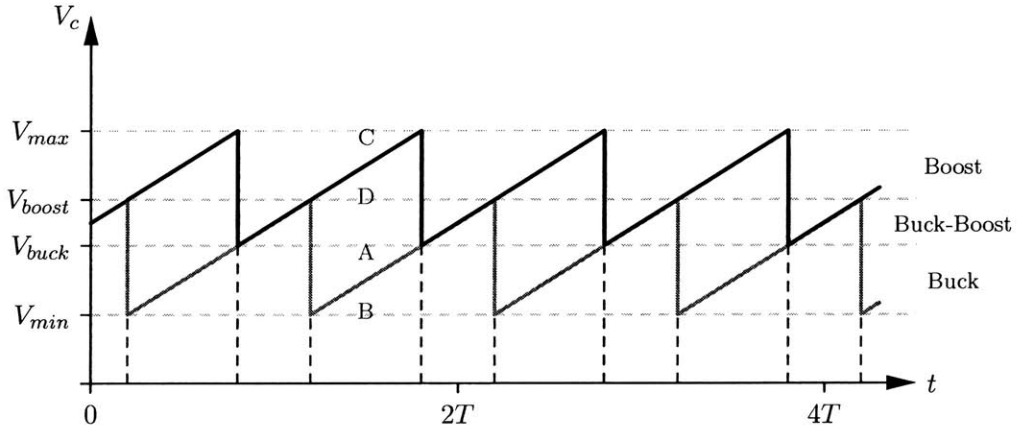

Figure 1-5: Effective sawtooth waveforms [3, p. 4]

In Figure 1-5 the top sawtooth waveform is used to control switches C and D and the

bottom sawtooth is used to control switches A and B. The control voltage obtained from the error amplifier is compared to these waveforms and when the control voltage is greater than either sawtooth the switches A or C will be on respectively. This convention is used throughout this paper. If the control voltage is greater than V_{min} but less than V_{buck} then the switches A and B will be pulse width modulated and the switch D will always be on causing a buck mode. If the control voltage is greater than V_{boost} and less than V_{max} then switches C and D will be pulse width modulated and switch A will always be on causing a boost mode, though a maximum boost duty ratio is imposed for practicality. If the control voltage is between V_{buck} and V_{boost} then all four switches will operate. In this case they operate in the following sequence: AD, AC, BD, AD. Figure 1-6 shows the inductor current ripple for this mode when $V_{in} = V_{out}$

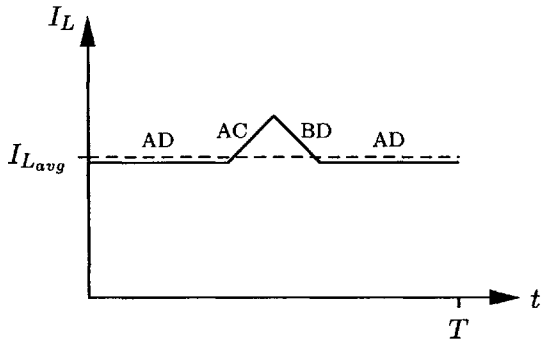

Figure 1-6: Current ripple for buck-boost mode

1.2 Proposed Work

This thesis suggests a new way of controlling the converter that results in a different inductor ripple waveform and will explore whether this new mode can be more efficient. This new method of control involves using level shifted triangle waves to control the switching instead of sawtooths. As shown in Figure 1-7 these waveforms will be in phase but their DC average will be different, though the lower extremity of the top waveform will overlap with the upper extremity of the bottom waveform. The top triangle wave will control switches C and D and the bottom triangle wave will control switches A and B as indicated. When the control voltage V_c is less than V_{buck} then switch D is on all the time and switches A and B switch to form a PWM waveform and the converter is in buck mode. When the control voltage is

greater than V_{boost} switch A is always on and switches C and D will switch to form a PWM waveform for boost mode operation.

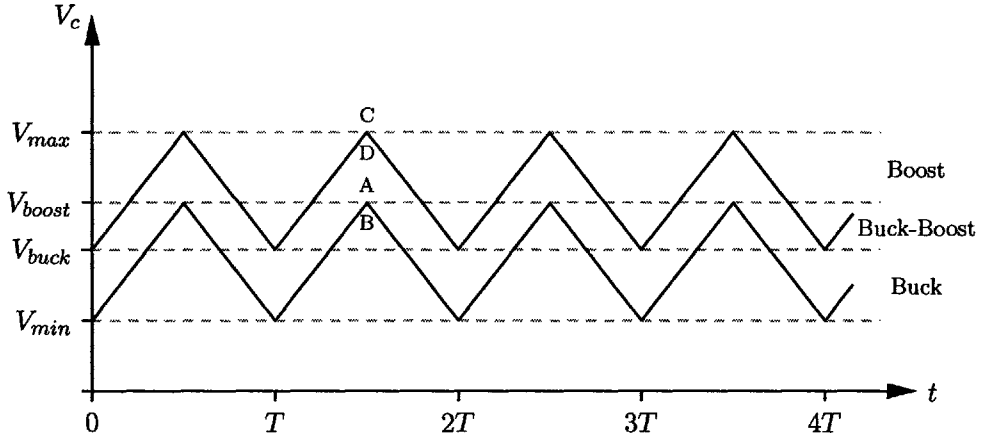

Figure 1-7: Triangle waveforms for converter control

The buck-boost region of the triangle wave converter is of the most interest. All four switches switch which yields the desired up/down conversion. However, the switching sequence is different than that of the sawtooth generator. Switches A and D are turned on followed by the normal A and C, but then A and D go back on. Finally B and D are turned on followed by A and D. Each switch is on for the same amount of time as it would have been had the sawtooths been used, but the current ripple looks significantly different as shown in Figure 1-8. One question of this project is whether controlling the switches this way is a better strategy.

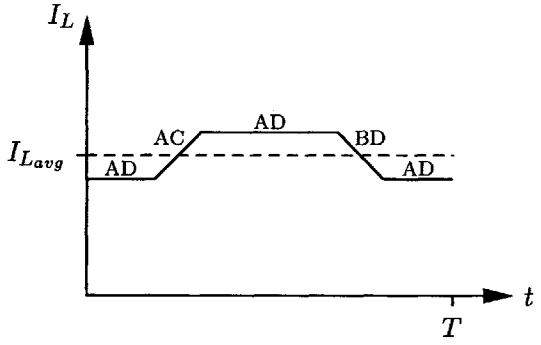

Figure 1-8: Current ripple in triangle wave controlled converter

The overlap of the triangle waves determines the width of the buck-boost region. Reducing this overlap will reduce the width of the buck boost region. This method of switching

may allow the buck boost region to be made smaller. If it can be made smaller than the sawtooth converter, then it should be more efficient than the sawtooth converter since the four switch mode is used over a narrower region. Also, this switching method should introduce less noise as no more than two switches are toggling at a time whereas in the sawtooth converter all four switches toggled in the AC to BD transition. This design is also a lot simpler than the sawtooth method because it requires less circuitry to generate the waveforms. In particular, the waveform generator will only need to use one capacitor to create the triangle wave. The sawtooth generation required two capacitors, one for each sawtooth. Unavoidable mismatch due to normal process variation in these capacitors causes a sub-harmonic component in the output spectrum at half the switching frequency. The triangle waveform generator will avoid this component. Because of the simpler topology of the control circuitry there will be more circuit area and quiescent current to devote to improvement of other parts of the circuit. For example, the triangle wave converter would be able to utilize higher speed comparators that would have smaller regions of nonlinear propagation delay but would require more current. This would help to keep linear duty cycles over a wider range of input voltages for the triangle wave converter. Finally, the area of the switches may be able to be increased, lowering their on resistances.

The rest of this paper explores the triangle wave method in several stages. First a comprehensive mathematical picture of the converter is presented which explains how the new method works, showing some of its merits. A treatment of the stability of the converter feedback loop is then given complete with derivations of the converter transfer functions in each region of operation. Next, considerations for a transistor level design and a lab design of the triangle wave converter are seen. This will unveil the triangle wave converter's validity and usefulness.

Chapter 2

Converter Fundamentals

The subtleties of the buck-boost converter's operation are deeply rooted in its underlying mathematical framework. An analysis for the ideal case with perfect PWM waveforms is presented in this chapter as a basis for what might happen when the non-idealities of individual circuit blocks are considered. A firm understanding of how the converter works when controlled by both sawtooth waveforms and triangle waveforms will help to determine what will be important in an actual design.

2.1 Overlap

The voltage overlap of either sawtooth waves or triangle waves will determine the width of the buck, buck-boost, and boost regions with respect to V_c. Changing the overlap will change which conversion ratios V_c can select in each region and thus determine what region will regulate an output for a given input. The overlap of the converter system can be expressed in terms of voltage or time.

2.1.1 Overlap in Voltage

As shown previously in Figures 1-5 and 1-7, in both the sawtooth and triangle wave system there are two waveforms present and their amplitudes will be denoted as V_{amp} for the following derivations. One of the two waveforms ranges from V_{min} to V_{boost} and the other ranges from V_{buck} to V_{max} such that $V_{buck} \leq V_{boost}$. Since the amplitude of either waveform is V_{amp}, $V_{boost} = V_{amp}$ and $V_{max} = V_{buck} + V_{amp}$ if $V_{min} = 0$v. The buck region is then bounded by 0v and V_{buck}, the buck-boost region is bounded by V_{buck} and V_{boost}, and the

boost region is bounded by V_{boost} and V_{max}. V_c sweeps through this whole range which generates the appropriate PWM waveforms in each region.

The buck-boost region is the region where the triangle waves or the sawtooth waves are overlapping such that a horizontal V_c line slices through both the top and bottom waveforms. The overlap then equates to the amount of each waveform that is in the buck-boost region with respect to its amplitude. For example, 0% overlap corresponds to a case where $V_{buck} = V_{boost}$, $V_{max} = 2V_{amp}$, and there is no buck-boost region, just a buck region and a boost region. 100% overlap corresponds to the case where $V_{buck} = 0$, $V_{boost} = V_{max}$, and there is only a buck-boost region. A 50% case would occur when $V_{buck} = V_{amp}/2$, $V_{boost} = V_{amp}$, $V_{max} = 1.5V_{amp}$, and all three regions are present. Overlap can be created by fixing V_{max} and changing the amplitudes of the triangle wave such that V_{buck} and V_{boost} change. It can also be created by keeping the amplitudes fixed and letting V_{max} vary.

Several equations can be derived to determine where the regions are. Referring to the width of the buck-boost region as V_{bb}, which is simply $V_{boost} - V_{buck}$, the percentage of overlap can be derived as $P_{ov} = V_{bb}/V_{amp}$. The value of V_{max} will be $2V_{amp} - V_{bb}$. Substituting into the equation for P_{ov}, V_{boost}, which equals V_{amp}, can be solved for:

$$V_{boost} = \frac{V_{max}}{2 - P_{ov}}$$

V_{buck} can be found in a similar manner by noting that $V_{buck} = V_{amp} - V_{bb}$ and then substituting for V_{amp} and V_{bb}:

$$V_{buck} = V_{max}\frac{1 - P_{ov}}{2 - P_{ov}}$$

Using these equations and knowing two of the four parameters, V_{max}, V_{amp}, V_{bb}, and P_{ov}, the arrangement of the waveforms can be completely determined and the boundaries of the regions can be found. Typically, V_{max} is selected first based on the input common-mode range of the PWM comparators and then P_{ov} is selected for optimal efficiency and transient performance. These equations will be useful tools when determining the efficiency of the converter over a range of parameters.

2.1.2 Overlap in Time

Sometimes the overlap is defined in terms of the period of the waveforms. As shown in Figure 1-5 the effective sawtooths overlap for a certain amount of time because they are out of phase with each other. The saws meet and are equal for a finite part the cycle. The percentage of the cycle for which this occurs is exactly equal to the percentage of the voltage overlap of the sawtooth waveforms. Examining closely, this is also the combined percentage of the time of the AC and BD phases when in the buck-boost region. In other words if the converter enters the buck-boost region, t_{AD} and $(t_{AC} + t_{BD})$ are fixed for any V_c in that region. Thus even though in the triangle wave system there is no visible time overlap between the waveforms because the waveforms are in phase, the overlap in time could be defined by the time the AC and BD phases operate per cycle and is also equal to the overlap in voltage.

2.2 Conversion Ratio

As the control voltage, V_c, sweeps through either sawtooth waves or triangle waves it traverses the buck, buck-boost, and boost regions of operation. Though conversion ratio is typically defined by the duty cycles of the switches, the conversion ratio that occurs for a given V_c is of interest — each V_c creates different duty cycles in the switches. Developing equations for conversion ratio as a function of V_c allows for a method to determine which region the converter operates in for a given input and output voltage. The buck, buck-boost, and boost regions each have their own equation for conversion ratio as a function of V_c and at the boundaries of the regions these equations produce the same value, yielding a continuous conversion ratio function.

2.2.1 Sawtooth Waveforms

In buck mode switch D is always on and the conversion ratio, D_{buck}, is the duty cycle of A, the main buck switch. The duty cycle of switch A is simply

$$D_{buck} = V_c/V_{amp}$$

In boost mode switch A is always on and the main boost switch, C, has a duty cycle of $(V_c - V_{buck})/V_{amp}$. The conversion ratio is found with the classic relation $1/(1 - D_C)$:

$$D_{boost} = \frac{1}{\left(1 - \frac{V_c - V_{buck}}{V_{amp}}\right)}$$

The conversion ratio in boost is also the inverse of the time that switch D is on during the cycle divided by the period.

In buck-boost mode all switches are on for part of the cycle, but the equations for D_A and D_D are the same. Since the conversion ratio is always t_A/t_D, multiplying the result for the buck region with the result for the boost region yields the conversion ratio for buck-boost:

$$D_{bb} = \frac{t_A}{t_D} = \frac{D_A}{D_D} = \frac{V_c}{V_{amp}} \frac{1}{\left(1 - \frac{V_c - V_{buck}}{V_{amp}}\right)} = \frac{V_c}{V_{amp} - V_c + V_{buck}}$$

.

2.2.2 Triangle Waveforms

Consider now a set of overlapping triangle waves ranging from 0V to V_{max} whose three regions of operation are also defined by V_{buck} and V_{boost}. Because of the symmetry of the triangle wave, the conversion ratio can be calculated by taking into account half of the cycle. One half of the cycle looks like a sawtooth and so the equations for D_A and D_D remain the same. Thus the conversion ratios yielded using the triangle waves are exactly the same as those yielded while using sawtooth waves in each region. This is true since the conversion ratio equals D_A/D_D no matter which region the converter operates in.

2.2.3 Conversion Ratio Properties

The equation for the buck region and the equation for the buck-boost region are equivalent at $V_c = V_{buck}$. Similarly the equation for the boost region will equal the equation for the buck-boost region when $V_c = V_{boost}$, yielding a piecewise continuous conversion ratio

function, D_{conv}:

$$D_{conv} = \begin{cases} D_{buck} & 0 \leq V_c < V_{buck} \\ D_{bb} & V_{buck} \leq V_c \leq V_{boost} \\ D_{boost} & V_{boost} \leq V_c < V_{max} \end{cases}$$

However, it should be noted that the first derivative of this function, $\frac{d}{dV_c} D_{conv}$, will not be continuous as there are corners at the transitions between regions. Interestingly, at $V_c = V_{buck}$ the conversion ratio reduces to $D_{conv} = V_{buck}/V_{boost}$ and at $V_c = V_{boost}$ the conversion ratio becomes $D_{conv} = V_{boost}/V_{buck}$. Thus as the buck region, and hence V_{buck}, increase the conversion ratios that occur in that region increase. As the boost region increases, lowering V_{boost}, lower conversion ratios are possible. This confirms that shrinking the buck-boost region by reducing the overlap directly reduces the possible conversion ratios in the buck-boost region. This means that less input/output combinations will fall in the buck-boost region, which is the goal of reducing overlap.

2.2.4 Finding the Conversion Ratio Graphically

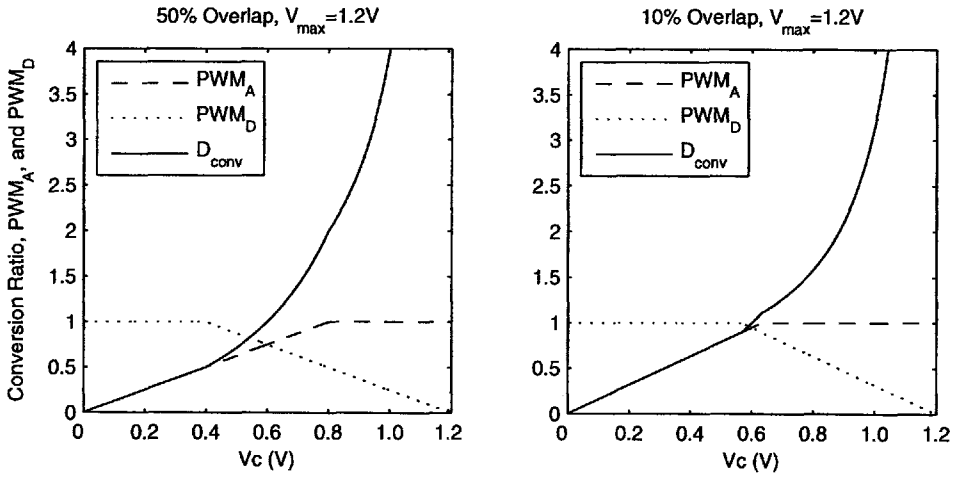

Figure 2-1: Graphical calculation of conversion ratio for two overlaps. Source code: Section D.1.

Whether sawtooths or triangles are used, a given overlap and V_{max} produce the same boundaries for the regions and the same conversion ratios inside those regions. This similarity for both systems lends insight into a way of determining the conversion ratios graphically. Since $t_A/t_D = D_A/D_D$ the duty cycles of the switches can be used to determine the conversion ratio given a particular V_c. Graphing the duty cycles of these switches versus V_c

and then dividing the curve for switch A by the curve for switch D can yield the conversion ratio. This is a rather straightforward method and is illustrated by Figure 2-1 which shows an ideal case where all duty cycles can be achieved by switch A and switch D. Of course the sawtooths and triangles produce the same duty cycles for a given V_c.

As seen in Figure 2-1, when V_c is less than V_{buck} the conversion ratio is the same as PWM_A. This occurs at $V_c \leq 400m\text{V}$ and $V_c \leq 568m\text{V}$ for the 50% and 10% overlap cases respectively. At the transition to the buck-boost region there is a corner after which the function has a monotonically increasing concave shape with a monotonically increasing first derivative. At the start of the boost region (at $V_c \geq 800m\text{V}$ and $V_c \geq 632m\text{V}$, respectively) there is another corner and the function has a similar characteristic as in the buck-boost region. For the 10% overlap case the buck-boost region is narrow as a result of the small overlap and the graph shows that the available range of conversion ratios in that region is smaller than that available in the 50% overlap case.

In reality the PWM curves will not be straight at the ends and so graphing the functions and then dividing them becomes the easiest way to obtain the conversion ratio for the whole range of V_c as a non-ideal PWM characteristic is difficult to characterize with an equation. It is crucial to see how non-idealities affect the conversion ratio, especially in the buck-boost region where they tend to increase the rate of change of conversion ratio with respect to V_c. This in effect increases the gain in this region which is an important consideration when stabilizing the converter feedback loop.

2.3 Inductor Current Ripple

A subtle difference between the two systems lies with the inductor current ripple waveform generated by each. Recall that the sawtooth system's switch pattern is AD–AC–BD whereas the switch pattern for the triangle wave system is AD–AC–AD–BD. For equal input and output voltages the inductor current waveform has a triangular peak, whereas for the triangle wave converter there is a trapezoidal peak. This trapezoid ends up being wider and smaller in peak value than the triangular peak. Figure 2-2 shows the buck-boost inductor ripple in both the sawtooth and triangle systems at $V_{in} = V_{out}$ overlaid for the same amount of overlap. At certain points the sawtooth ripple waveform has a greater absolute value and at other times the triangle ripple waveform is higher. In addition the average values of these

waveforms are different, $\overline{I_{L_{saw}}}$ being slightly higher than $\overline{I_{L_{tri}}}$.

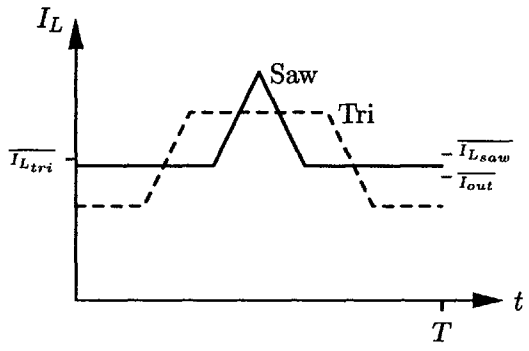

Figure 2-2: Overlay of inductor ripple produced by the sawtooth and triangle wave systems for $V_{in} = V_{out}$.

The inductor current directly determines conduction loss in the converter which is the dominant loss mechanism at high load currents. Gate charge loss, which dominates loss at low load currents is discussed in Section 2.3.4. During each switch phase the inductor current is always flowing through two of the switches and so the instantaneous conduction loss is equal to $2I_L^2 R_{sw}$, assuming that all of the switch on resistances are the same. In general the switch resitances will be different but for simplicity in this analysis they are made equal. Because of the geometry and the I_L^2 term and the difference in $\overline{I_L}$, the average power loss will be different. It appears that the triangle wave would be marginally lower because the absolute value of the current is lower than the sawtooth one for most of the cycle, and the sawtooth achieves the highest value overall. However, this is only true if there is an appreciable average inductor current. If the average inductor current were zero as in a forced continuous situation the inductor current generated by the sawtooth would be nearer zero than the inductor current generated in the triangle system, making the sawtooth system more efficient. The low load situation is important as many portable electronic devices have a low power mode when they do not have to supply much current (a cell phone in standby is a good example) and techniques exist to handle those situations efficiently. The burst mode feature of the LTC3440 handles such a situation, though this is not treated here.

2.3.1 Inductor Ripple in Buck Mode

The inductor current ripple in buck mode is determined by the buck duty cycle and the slopes of the current ripple in the AD phase and the BD phase. In the AD phase the current ramps up with a slope of $m_{AD} = (V_{in} - V_{out})/L$ and during the BD phase the inductor current ramps down with a slope of $m_{BD} = -V_{out}/L$. It is convenient to look at the inductor ripple in buck mode by drawing the AD phase followed by the BD phase. For the sawtooth waves this means the start of the period can be referenced to the time at which the lower saw is at its minimum. For the triangle wave scheme the start of the cycle shifts with V_c such that it begins where V_c intersects the down slope of the lower triangle.

In the buck converter the inductor is always connected to the output. Thus the inductor current has an average value equal to the output load current with ripple on top of it. The minimum value of the inductor current is then $I_{out} - 0.5M_{AD}D_A$ and the maximum value is $I_{out} + 0.5m_{AD}D_A$. The value of the ripple amplitude in terms of the constant V_{out} and D_A is $(V_{out} - D_A V_{out})T/L$ so at zero duty cycle the value is $V_{out}T/L$ and it decreases linearly with duty cycle to zero, when $D_A = 1$.

To calculate the average power loss component in the converter due to switch resistances the inductor current waveform has to be squared, multiplied by $2R_{sw}$, and integrated over the cycle. Figure 2-3 shows the power loss and efficiency versus duty cycle for a fixed 3.3V output voltage, a load current of $500m$A, a 5μH inductor, and $100m\Omega$ switches. As the duty cycle decreases the amplitude of the inductor current ripple waveform approaches its maximum value. For these extremely low duty cycles the overall shape of the inductor ripple changes very little since most of the cycle is the BD phase ramping down from almost the same value. Thus the loss approaches a final value – it will not increase without bound. At high duty cycles the ripple amplitude is very small and the average loss approaches $2I_{out}^2 R_{sw}$. The efficiency is calculated as the output power, $I_{out}V_{out}$, divided by the sum of the output power and the loss. As the duty cycle increases the efficiency is greatest. When plotted against input voltage it is seen that at high V_{in} the efficiency is almost constant with increase in V_{in} corresponding to the ripple waveform changing very little.

This view of how a simple buck converter works will be helpful in explaining the efficiency curve obtained for the full buck-boost converter. This buck behavior is the same for both the triangle wave and the sawtooth wave implementations. Whenever the buck-boost converter

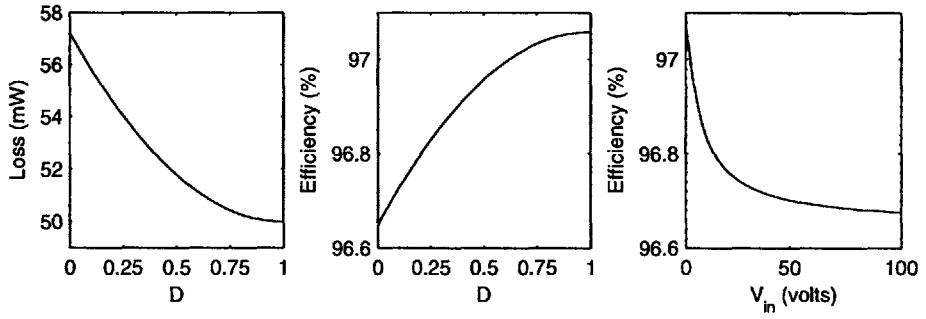

Figure 2-3: Buck loss and efficiency over D and V_{in} for $V_{out} = 3.3\text{V}$, $I_{out} = 500m\text{A}$, $R_{sw} = 100m\Omega$, and $L = 5\mu\text{H}$. Source code: Section D.2.

is in buck mode the efficiency will be similar to these graphs at the same conversion ratios.

2.3.2 Inductor Ripple in Boost Mode

In boost mode the inductor ripple waveform consists of an AC phase that charges up with slope $m_{AC} = V_{in}/L$ and an AD phase that discharges with a slope $m_{AD} = (V_{in} - V_{out})/L$ because in boost mode V_{out} is greater than V_{in}. Referencing the cycle to the AD phase is again useful in boost mode. This means that for both the sawtooths and the triangles the period begins at the point where V_c slices through the rising part of the wave. Using the fact that the amplitude of the inductor current ripple is $I_{amp} = m_{AC}(1 - D_D)T$ and that $V_{out}/V_{in} = 1/D_D$, the amplitude of the ripple is found to be a parabolic function of D_D, $(D_D - D_D^2)V_{out}T/L$. It has a maximum value of $0.25V_{out}T/L$ when $D_D = 0.5$. More important than the amplitude of the inductor current ripple is its DC value. The boost converter's input current is equal to the inductor current and has to be greater than the output current by at least a factor of $1/D_D$ because current is only delivered to the load during the AD phase of the cycle. Thus, as switch D's duty cycle decreases the inductor current rises dramatically, a reason for imposing a limit on the minimum switch D duty cycle.

Figure 2-4 shows the loss in the boost converter over a range of duty cycles. At low switch D duty cycles the inductor current is very high and the loss is high. This kills the efficiency for low switch D duty cycles and correspondingly low input voltages. However, as the duty cycle increases the converter becomes very efficient. At $D_D = 1$ the loss is just $2I_{out}^2 R_{sw}$, a result also obtained for the buck converter at full switch A duty cycle.

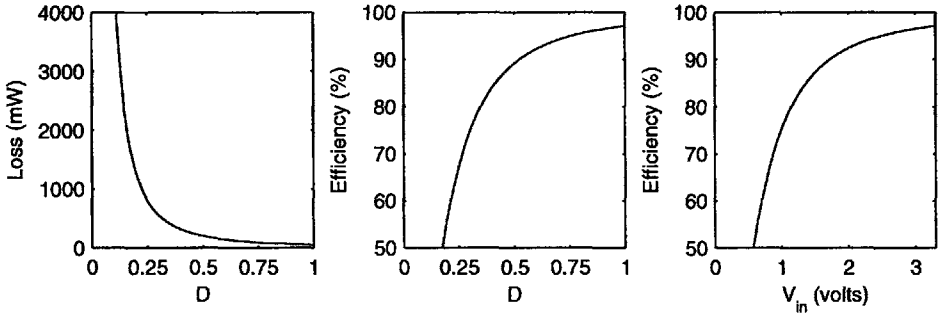

Figure 2-4: Boost loss and efficiency over D and V_{in} for $V_{out} = 3.3v$, $I_{out} = 500mA$, $R_{sw} = 100m\Omega$, and $L = 5\mu H$. Source code: Section D.3.

2.3.3 Inductor Ripple in Buck-Boost Mode

The previous analyses were carried out if as if there were one buck or one boost. In buck-boost mode it doesn't make sense to analyze a buck-boost converter that achieved all possible conversion ratios because that analysis would occur only in the 100% overlap where there is no AD phase, the phase which distinguishes the triangle wave based converter from the sawtooth wave based converter. Instead, it should be analyzed for a given overlap.

Sawtooth Buck-Boost

It is again convenient to reference the start of the cycle to the AD phase. For the sawtooth converter this begins at the fall of the lower sawtooth. The AD phase consists of a slope of $m_{AD} = (V_{in} - V_{out})/L$ but its slope may be positive or negative. As the converter comes out of boost mode and goes into buck-boost mode AD will have a negative slope. For equal input and output voltages m_{AD} will be zero and its slope will increase as the converter approaches buck mode where it will keep increasing as V_{in} becomes higher and higher. At the transition between regions the slope of AD is continuous as a result of the continuous conversion ratio function and thus continuous change in V_{in} at the transition. The AC phase will always have a positive slope and the BD phase will always have a negative slope. Figure 2-5 shows this progression of the inductor current ripple throughout the buck-boost region with the beginning of the cycle starting at DC values of I_{os1}, I_{os2}, and I_{os3} particular to their conversion ratios.

While in buck-boost mode the current that is delivered to the output is the same as the inductor current during the AD and BD phases of the cycle. The average inductor

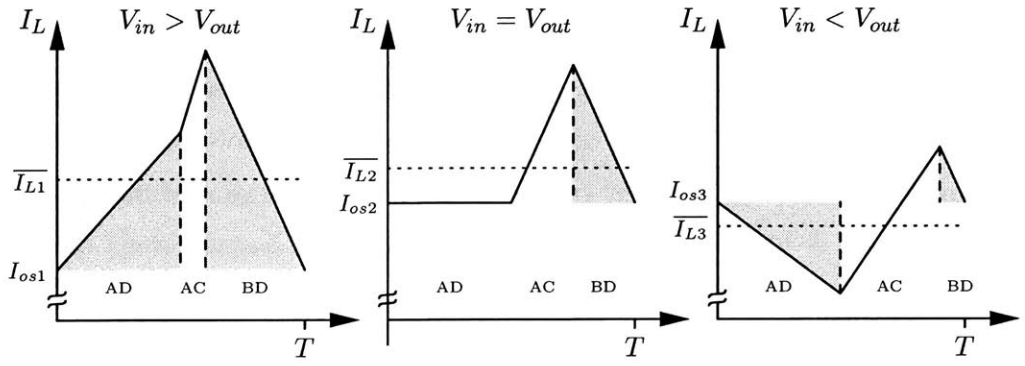

Figure 2-5: Inductor ripple waveform progression in sawtooth buck-boost for $P_{ov} = 50\%$. The shaded area denotes the area integrated in Equations 2.1, 2.2, and 2.3 as if I_{os1}, I_{os2}, and I_{os3} were at zero.

current during these phases must then be enough to average I_{out}. By imagining that the cycle starts at zero current and progresses through AD, AC, and BD the average inductor current delivered to the load can be found by integrating the AD and BD phases. The shaded area in Figure 2-5 is the area of integration; imagine the time axis is placed right at I_{os1}, I_{os2}, or I_{os3} for integration purposes. This area is averaged over the cycle to obtain the average current the ripple waveform delivers to the output. Then this amount is subtracted from the value of I_{out} and the result is divided by the percentage of the cycle that the AD and BD phases operate. This first step is shown in Equation 2.1:

$$I_{os} = \frac{T}{T - t_{ac}} \left(I_{out} - \frac{1}{T} \left(\int_0^{t_{AD}} m_{AD} t \, dt + \int_{t_{AD}+t_{AC}}^{T} (m_{AD} t_{AD} + m_{AC} t_{AC} + m_{BD} t) \, dt \right) \right) \tag{2.1}$$

Note that the AC phase has to be taken into account as it determines at what current value the BD phase starts at. This equation can be made simpler by noting that if the cycle starts at zero, it will also end at 0. Thus the limits of integration of the integral for the BD phase can be changed from 0 to t_{BD} as in Equation 2.2. The minus sign is added because integration now occurs backwards along the time axis. Equation 2.3 shows the final expression for the offset current at the beginning of the cycle.

$$I_{os} = \frac{T}{T - t_{ac}} \left(I_{out} - \frac{1}{T} \left(\int_0^{t_{AD}} m_{AD} t \, dt + \int_0^{t_{BD}} -m_{BD} t \, dt \right) \right) \tag{2.2}$$

$$I_{os} = \frac{T}{T - t_{ac}} \left(I_{out} - \frac{1}{2T} \left(m_{AD} t_{AD}^2 - m_{BD} t_{BD}^2 \right) \right) \tag{2.3}$$

Now the full inductor current waveform can be constructed by starting at this value and using the slopes and lengths of the phases to construct the waveform over the cycle in a piecewise manner. It should be stressed that these equations do not solve for the average inductor current. The average inductor current is the complete integral of the inductor current over the cycle divided by the period and is higher than the output current because no current is delivered to the output during the AC phase.

Triangle Buck-Boost

The triangle wave converter is a little bit simpler to analyze in buck boost mode because of its inherent symmetry. If the cycle is referenced to the midpoint of the AC phase (or the midpoint of the BD phase by symmetry) the average inductor ripple over the cycle will be zero. At the start of the cycle the AC phase charges for $t_{AC}/2$ and then AD charges or discharges depending on m_{AD} for $t_{AD}/2$. Then BD discharges for t_{BD} and after $t_{BD}/2$ the current value is back where it started. The last half of the cycle is a reflection of the first half as though it were an odd function. Therefore the total average inductor current is simply $I_{out}T/(T - t_{AC})$ and is less than the average inductor current in the sawtooth system. No complicated integration scheme is necessary to construct the full inductor ripple waveform in the triangle system. Figure 2-6 shows the ripple waveform progression where $\overline{I_L}$ is dependent on the conversion ratio for each plot. It shows that the average value of the waveform and the inherent symmetry about that average value.

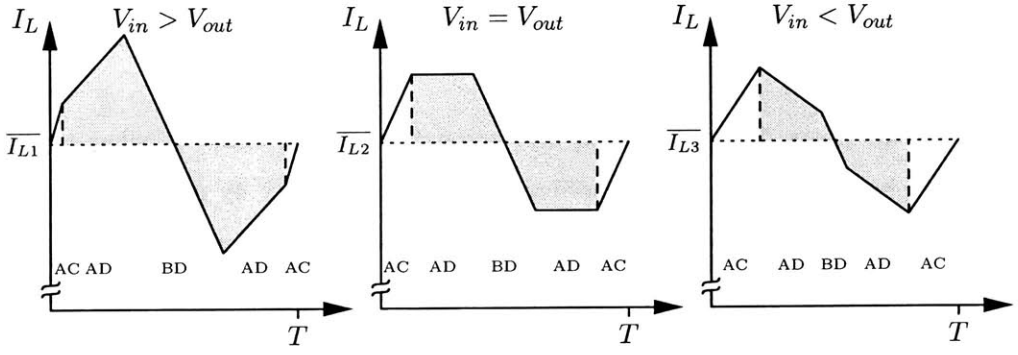

Figure 2-6: Inductor ripple waveform progression in sawtooth buck-boost for $P_{ov} = 50\%$.

It turns out that for a majority of overlap values the average inductor current for the triangle wave buck-boost is less than in the sawtooth. At $V_{in} = V_{out}$ the inductor current in the sawtooth is greater than the triangle inductor current for much of the cycle and achieves

the higher absolute current as in Figure 2-2. Though the triangle current waveform is also higher for part of the cycle, one might intuit that because the sawtooth inductor current reaches the highest peak value over the course of the cycle it will exhibit a higher average inductor current. Thus the difference in the average inductor currents, $I_{Lsaw} - I_{Ltri}$, will be positive. Moving away from this midpoint of the buck-boost region one would expect the average inductor current for the sawtooth converter to continue to be greater than in the triangle wave converter. In the buck and boost regions the average inductor current will be the same in both converters and the difference in average inductor current between the two converters will be zero. Then, given that the difference in conduction loss is nonzero at $V_{in} = V_{out}$ one would expect a monotonically varying difference in average inductor current from this point to the respective edges of the buck-boost region. This intuition is confirmed by numerical simulation, the results of which are shown in Figure 2-7. Since conduction power loss is directly linked to the average inductor current this shows that the conduction loss in the sawtooth converter will be greater than that in the triangle converter. Though this average inductor current relation is mathematically rigorous to prove over the whole buck-boost region, Appendix A goes through a proof of this property for $V_{in} = V_{out}$.

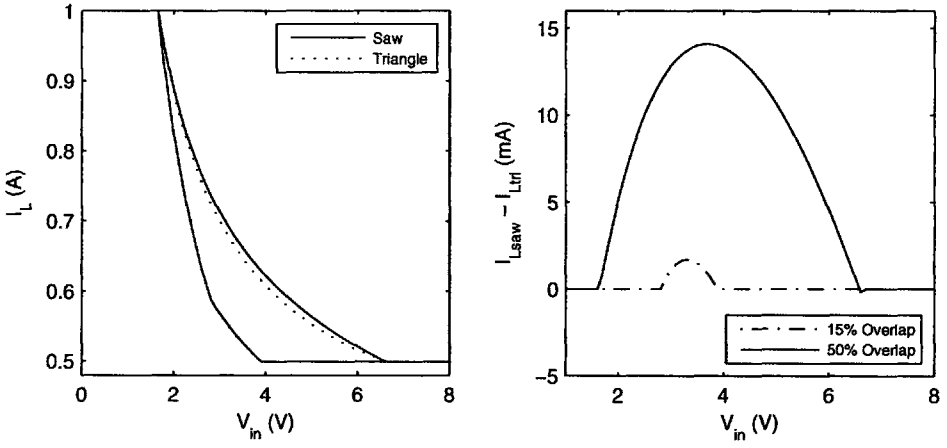

Figure 2-7: Average inductor current comparison over V_{in} with $V_{out} = 3.3\text{V}$, $I_{out} = 500m\text{A}$. The left plot shows the absolute average inductor current for a 15% and 50% overlap case while the plot on the right shows the difference in average inductor current for the same overlaps. Source code: Section D.4.

2.3.4 Full Operation

Conduction Loss

The full operation of the buck-boost converter has now been fully described and the equations involved are adequate to produce plots of converter efficiency over all three regions of operation. The efficiency of the converter is analyzed for a fixed output voltage of 3.3V. The converter is a regulator and it is assumed that the output voltage will be fixed in most applications. A Matlab program utilizes the derived equations to generate the inductor ripple waveforms for a given overlap and input voltage. The region of operation, conversion ratio, and lengths of the phases are determined by these operating parameters. The inductor current waveforms are constructed as described previously and are squared, multiplied by $2R_{sw}$, and averaged over the cycle to obtain the average conduction power loss. The efficiency is then calculated as the output power divided by the sum of the output power and the average power loss.

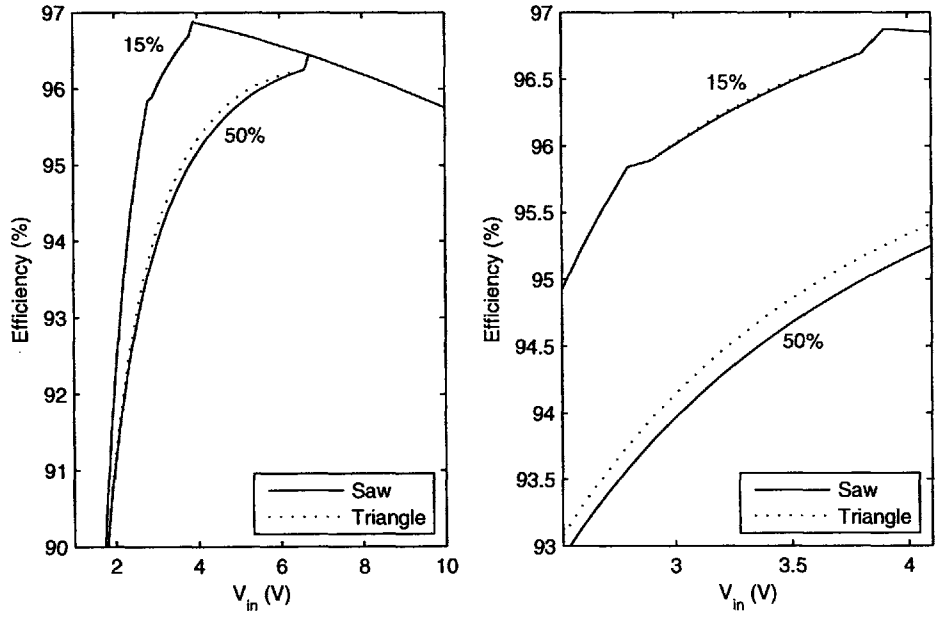

Figure 2-8: Buck-boost efficiency vs. V_{in} for $V_{out} = 3.3$V, $I_{out} = 500mA$, $R_{sw} = 100m\Omega$, and $L = 5\mu$H for overlaps of 15% and 50%. Source code: Section D.4.

Figure 2-8 shows two plots of efficiency for the full buck-boost converter. The left plot shows two sets of curves. The set that has higher efficiency is for a 15% overlap case and the set that has lower efficiency is for a 50% overlap case. The range of the buck-boost region

is 2.81V$\leq V_{in} \leq$ 3.88V and 1.65V$\leq V_{in} \leq$ 6.6V for each overlap respectively. Each set of curves has a solid line representing the efficiency versus V_{in} for a sawtooth waveform at that value of overlap. The dotted line in each set is the triangle wave efficiency. In the plot on the left the dotted line is barely visible for the 50% overlap case and really indistinguishable in the 15% case. The plot on the right is the same as the left but with a zoomed in view that clearly shows the higher triangle efficiency in both overlap cases. This is valid strictly for the buck-boost region – in the buck and boost regions the converter efficiency is exactly the same for both cases because the inductor ripple waveforms are exactly the same. Overall the converter is less efficient for large overlaps because as the overlap increases the relative length of the AC phase increases. This causes the average inductor current to be larger as current is only delivered to the load during the AD and BD phases. CV^2f losses as well as the effect of increasing R_{sw} as V_{in} decreases was not considered in order to simplify analysis.

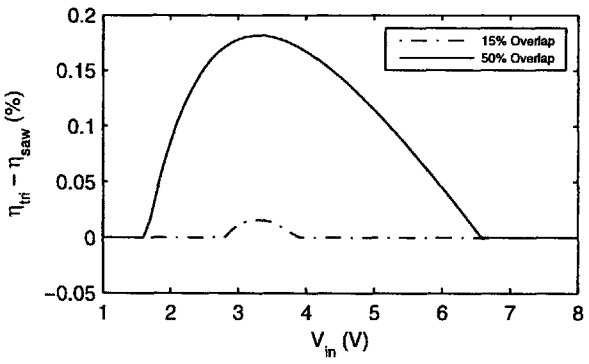

Figure 2-9: Difference in buck-boost efficiency over V_{in} for P_{ov} = 50% and P_{ov} = 15%. Source code: Section D.4.

The triangle wave based converter is more efficient than the sawtooth wave based converter in the buck-boost region for any overlap value and throughout the entire buck-boost region. This is due to $\overline{I_L}$ being less in the triangle wave system and the geometry of the inductor wave ripple. Figure 2-9 shows the difference between efficiency, $\eta_{tri} - \eta_{saw}$, for the 15% and 50% overlap cases. For the entirety of the buck-boost region the difference in efficiency is positive, indicating that the triangle wave is more efficient. However, the difference is not all that large. For the 50% overlap case a maximum increase of 0.18% in efficiency is observed while for the 15% overlap case a 0.015% increase is observed. These maxima occur for $V_{in} = V_{out}$ when the triangle waveform converter completely exploits the favorable geometry of the inductor ripple waveform. For other values of V_{in} at either end of

the buck-boost region the gain in efficiency falls off as the buck-boost inductor waveforms approach either a pure boost mode inductor current waveform or a pure buck inductor current waveform.

Addition of Gate Charge Loss

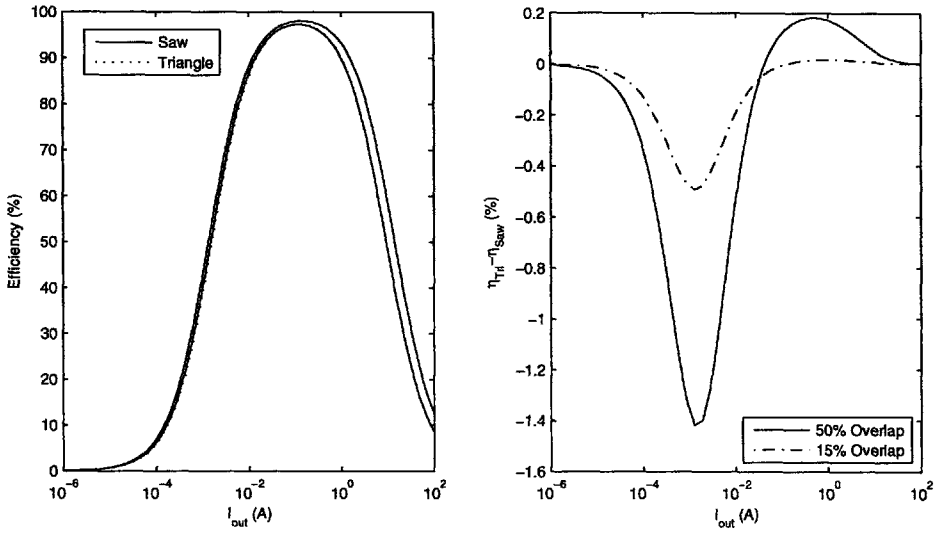

Figure 2-10: Buck-boost efficiency over I_{out} with gate charge loss for $V_{in} = V_{out} = 3.3v$, $R_{sw} = 100m\Omega$, and $L = 5\mu$H. Source code: Section D.5.

Gate charge or switching loss must also be considered in the buck-boost converter. The switch loss for a switch is equivalent to $C_g V^2 f$ where C_g is the gate capacitance of the switch, V is the gate swing voltage, and f is the switching frequency. Additionally, since pMOS devices are used for switches A and D, and nMOS devices are used for switches B and C, the gate capacitance is referred to as C_{gp} and C_{gn}. In buck mode switch A and B switch once per cycle and the V_{in} rail is used to charge the gates, so the gate charge loss is $(C_{gp} + C_{gn})V_{in}^2 f$. In boost mode switches C and D switch once per cycle, but switch D is charged by the V_{out} rail whereas switch C is charged by V_{in}. So the gate charge loss for boost mode is $(C_{gp}V_{out}^2 + C_{gn}V_{in}^2)f$. In buck-boost mode for the sawtooth all of the switches switch once per cycle and the gate charge loss is $(C_{gp}V_{in}^2 + C_{gp}V_{out}^2 + 2C_{gn}V_{in}^2)f$. Figure 2-10 shows the buck-boost efficiency curves plotted against output current where $C_{gp} = 150p$F and $C_{gn} = 50p$F. At low currents the gate charge loss dominates while at high currents the conduction loss dominates. The triangle wave converter is more efficient at appreciable

load currents on the order of $100mA$, but as the load current decreases the gate charge loss in the triangular converter is greater than in the sawtooth converter and the triangle wave converter is less efficient. However, the entire range of deviation in efficiency is minimal for both the sawtooth and triangle wave based converters.

Chapter 3

Frequency Compensation

In order to regulate a constant reliable output voltage with this architecture feedback must be used. If one had precise control of the PWM generators one could in theory produce a constant output voltage open loop. However, non-idealities in the system can cause small perturbations that can affect the output voltage. The only way to correct for these is to use feedback. In order for the feedback loop to be effective it has to be stable in all three regions of operation. In this topology a single feedback network has been chosen for the circuit to work in all three modes. Alternatively, one could build separate feedback networks and switch them in for each region of operation, but this would be cumbersome and possibly worse at the transition points from one region to the next.

3.1 Transfer Functions of the Converter in Each Region

In order to analyze the effectiveness of a feedback loop one must look at its stability. The level of stability of a system will determine the behavior of its closed loop response. In this case a reasonable phase margin is desired and in order to find the phase margin the transfer functions of the converter itself have to be derived. When combined with the transfer function of the compensation network to obtain the transmission of the entire loop, the phase margin can be found.

The transfer functions are obtained by circuit averaging and linearization for each mode. The state equations are written for the inductor and the output capacitor. These equations are averaged and then each variable that can experience a perturbation is replaced by its large signal value and small signal component ($x = X + \tilde{x}$) [7, p. 277].

For compensating the converter the primary interest is in the transfer function from $\tilde{d}$ to $\tilde{v}_o$. This transfer function is a major component of the loop that needs stabilization.

3.1.1 Buck Transfer Function

In buck mode the switch D is always on while the switches A and B are modulated by switching functions $q_A(t)$ and $1 - q_A(t)$. Writing the state equations given this switching function the following is obtained:

$$L\frac{di_L}{dt} = (v_{IN} - v_{OUT})q_A(t) + v_{OUT}(1 - q_A(t))$$

$$C\frac{dv_{OUT}}{dt} = i_L - \frac{v_{OUT}}{R}$$

The switching function is averaged such that $q_A(t) = d$ and $1 - q_A(t) = (1 - d)$. All other variables of interest are also averaged [7, p. 266-273].

$$L\frac{d\overline{i_L}}{dt} = (\overline{v_{IN}} - \overline{v_{OUT}})d + \overline{v_{OUT}}(1 - d)$$

$$C\frac{d\overline{v_{OUT}}}{dt} = \overline{i_L} - \frac{\overline{v_{OUT}}}{R}$$

Finally the variables i_L, v_{IN}, v_{OUT}, and d are replaced by using a Taylor expansion to linearize the averaged model (e.g. $i_L = I_L + \tilde{i}_l$). The Laplace transform of the result is taken and simplified. Terms that contain more than one small signal component are considered second order and are discarded. The large signal terms cancel and only the small signal terms remain. Since the ratio $\tilde{v}_{out}/\tilde{d}$ is desired the term $\tilde{v}_{in}$ is set to zero.

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{V_{IN}}{LCs^2 + \frac{L}{R}s + 1}$$

The buck transfer function is a two pole system. Closed loop stability is easily achieved but may require compensation for phase margin [11].

3.1.2 Boost Transfer Function

In boost mode switch A is always on and switches C and D are modulated by switching functions $q_C(t)$ and $1 - q_C(t)$. Following the method for deriving the buck transfer function the averaged state equations can be obtained yielding:

$$L\frac{d\overline{i_L}}{dt} = \frac{\overline{v_{IN}}}{L}d + \frac{\overline{v_{IN}} - \overline{v_{OUT}}}{L}(1-d)$$

$$C\frac{d\overline{v_{OUT}}}{dt} = \frac{-1}{RC}d + \left[\frac{\overline{i_L}}{C} - \frac{\overline{v_{OUT}}}{RC}\right](1-d)$$

After linearizing and taking the Laplace transform a two pole system with a right half plane zero is obtained for the boost mode. This right half plane zero will pull the complex poles toward the right half plane in a unity gain negative feedback loop causing poor phase margin and possibly instability. This needs to be addressed with a compensation scheme [12].

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{D_C^{'}V_{OUT} - sLI_L}{LCs^2 + \frac{L}{R}s + D_C^{'2}}$$

By substituting relations involving V_{out}, V_{in}, and I_L it can be shown that the right half plane zero location is

$$s = \frac{V_{IN}^2}{LI_{OUT}V_{OUT}}.$$

3.1.3 Buck-Boost Transfer Function

In the four switch region or buck-boost mode all four switches operate during each cycle. Switches A and B are modulated by switching functions $q_A(t)$ and $1 - q_A(t)$ while switches C and D are modulated by switching functions $q_C(t)$ and $1 - q_C(t)$. Each of these switching functions can be averaged as D_A, $1 - D_A$, D_C, and $1 - D_C$. Here it is important to note the voltage at the A-B switch node on the left side of the inductor, v_X can be represented as an average voltage by averaging the input voltage and switches A and B and linearizing:

$$\overline{v_X} = d_A v_{IN} \Rightarrow V_X + \tilde{v}_x = (D_A + \tilde{d}_a)(V_{IN} + \tilde{v}_{in})$$

Taking the small signal terms and dropping the DC and second order terms yields:

$$\tilde{v}_x = D_A\tilde{v}_{in} + \tilde{d}_A V_{IN}$$

Now the circuit can be treated as a boost with input voltage v_X. The same linearized state equations derived in boost mode are used. The DC terms cancel in the same manner

as in boost and $\tilde{v}_{in}$ in boost is replaced by $\tilde{v}_x$ and the desired transfer function is obtained. In this case any contribution by $\tilde{v}_{in}$, the buck-boost input voltage, is set to zero because it is assumed there are no perturbations in the input voltage. It is also assumed that $\tilde{d}_A = \tilde{d}_C$ because V_c controls both duty cycle and a perturbation in V_c will cause the same perturbation in $\tilde{d}_A$ and $\tilde{d}_C$. The transfer function for the four switch region is then:

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{D_C'(V_{IN} + V_{OUT}) - sLI_L}{LCs^2 + \frac{L}{R}s + D_C'^2}$$

It can be shown that the right half plane zero lies at

$$s = \frac{V_{IN}^2(D_A D_C' + D_A^2)}{LI_O V_O}$$

which, for the overlap this converter will run at, will always be higher than the value in boost mode. Thus as we move from buck-boost mode to boost mode the zero comes closer to the origin in the s-plane. The zero being closer to the other poles in the system will decrease the phase margin of the system. If the compensation scheme can handle buck and boost mode, it should be able to handle buck-boost mode. Figure 3-1 shows how the zero moves away as the input voltage is raised.

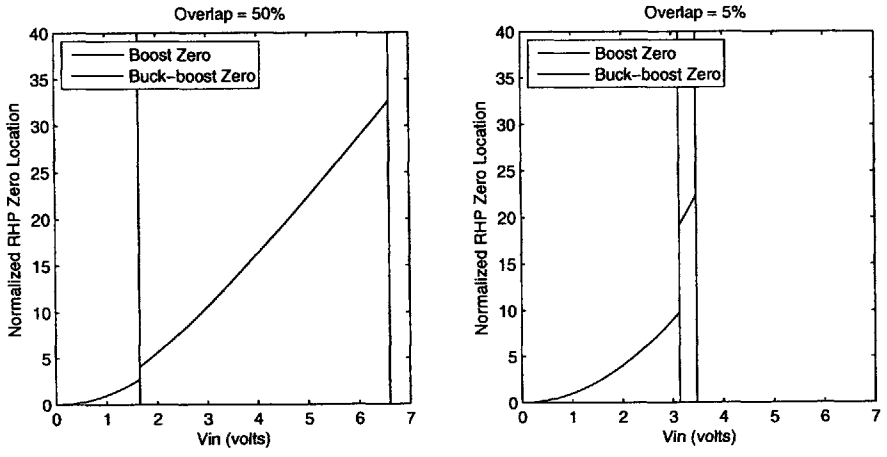

Figure 3-1: Location of right half plane zero as a function of V_{IN} for a fixed 3.3V output. Zero location is normalized to LP_o. Source code: Section D.6.

3.1.4 ESR Zero

There exists a zero due to the ESR of the output filter capacitor. This is a left half plane zero and its presence needs to be considered while designing the compensation scheme. The capacitors used in this application typically have on the order of $10m\Omega$ of ESR. The time constant $R_{ESR}C$ creates this zero. The presence of the zero also shifts the locations of the two poles slightly but has no affect on the location of the right half plane zero in boost and buck-boost modes. The ESR zero was solved for by the same method as above and the transfer functions obtained are shown here.

Buck:

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{V_{IN}(1 + sR_{ESR}C)}{LC(1 + \frac{R_{ESR}}{R})s^2 + (\frac{L}{R} + R_{ESR}C)s + 1}$$

Boost:

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{(D_C^{'}V_{OUT} - sLI_L)(1 + sR_{ESR}C)}{LC(1 + D_C^{'}\frac{R_{ESR}}{R})s^2 + (\frac{LD_C}{R_{ESR}+R} + \frac{D_C^{'}L}{R} + D_C^{'2}R_{ESR}C)s + D_C^{'2}}$$

Buck-Boost

$$\frac{\tilde{v}_{out}}{\tilde{d}} = \frac{(D_C^{'}(V_{IN} + V_{OUT}) - sLI_L)(1 + sR_{ESR}C)}{LC(1 + D_C^{'}\frac{R_{ESR}}{R})s^2 + (\frac{LD_C}{R_{ESR}+R} + \frac{D_C^{'}L}{R} + D_C^{'2}R_{ESR}C)s + D_C^{'2}}$$

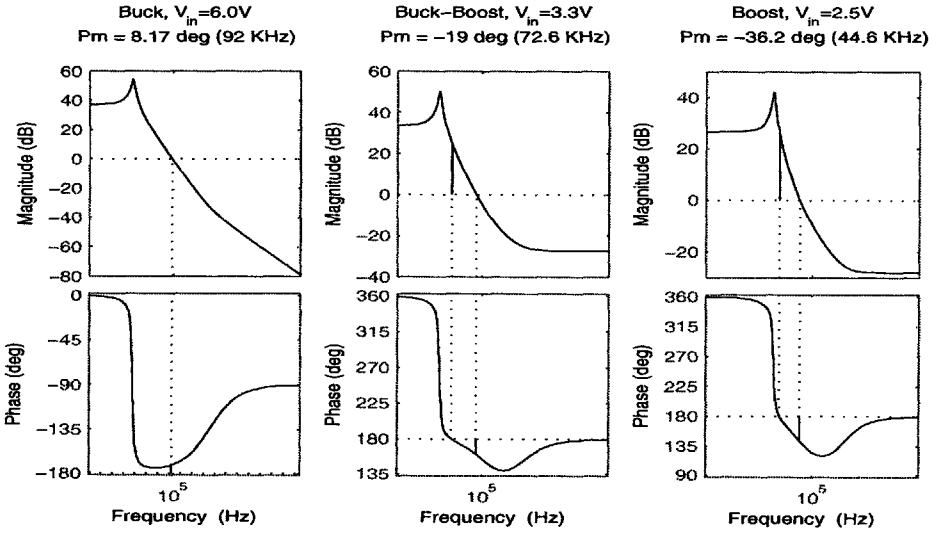

Figure 3-2: Converter transfer functions in the buck, buck-boost, and boost regions at a typical load of $600mA$. Source code: Section D.7.

When R_{ESR} is set to zero, these transfer functions reduce to what was obtained earlier. Figure 3-2 plots the converter transfer function in each region for a typical set of variables and shows that the converter function is either at the edge of stability or unstable in all three regions.

3.2 System Block Diagram

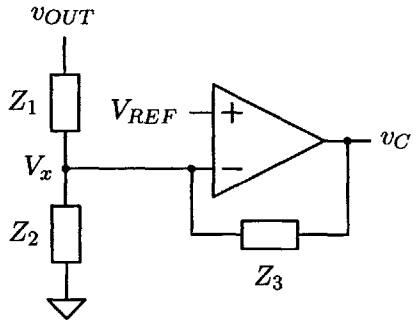

Figure 3-3: Error Amplifier

The error amplifier in the loop provides the means for DC error correction in the DC output voltage and also allows for small signal compensation of the loop. The error amp has a bandgap reference voltage at its positive terminal. The output voltage of the converter is impedance divided to the inverting terminal of the op amp. The error amplifier section of the converter is shown in Figure 3-3 where the compensation impedances have been lumped into Z_1, Z_2, and Z_3. Writing KCL at V_x, the following equation for V_x is found:

$$\frac{V_c - V_x}{Z_3} = \frac{V_x}{Z_2} + \frac{V_x - V_{out}}{Z_1}$$

$$V_x = \left(\frac{V_c}{Z_3} + \frac{V_{out}}{Z_1}\right) Z_1 \,\|Z_2\|\, Z_3$$

This voltage V_x is the inverting input to the error amplifier whose transfer function is defined as $E_A(s)$. A SPICE simulation of the error amplifier used in the LTC3440 shows that the amplifier transfer function is approximated by a single pole system with a gain of 90dB and a unity gain frequency of 1MHz. The error amplifier subtracts V_x from V_{ref} to produce V_c. V_c serves as an input to the converter and is also fed back to the input of the error amplifier as defined in the V_x equation. The output of the converter is also fed back to the same point. Thus, the block diagram in Figure 3-4 below can be derived.

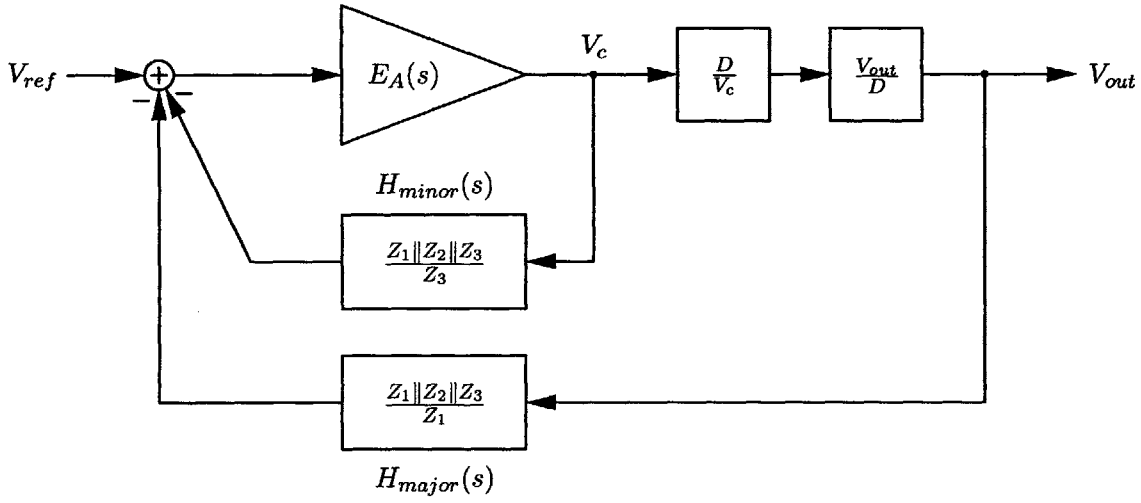

Figure 3-4: Converter Block Diagram.

In the properly compensated system Z_3 is comprised of at least one series capacitor which acts as an open circuit at DC and makes the impedance of Z_3 infinite. In this case the minor loop is broken and only the major loop acts on the circuit. The high gain of the error amplifier causes the closed loop transfer function at DC to be

$$\frac{V_o}{V_{ref}} = \frac{Z_1}{Z_1 \| Z_2 \| Z_3} = \frac{R_1 + R_2}{R_2}$$

where the impedances Z_1 and Z_2 are replaced by the resistors R_1 and R_2 because all capacitors are open at DC. Thus the loop regulates the output voltage by the voltage divider from the converter output to the error amplifier. The bandgap voltage V_{ref} reliably holds a constant value, thus ensuring an accurate output voltage.

Now the loop must be analyzed for stability. At AC frequencies the capacitors exhibit non-infinite impedance. Assuming that the impedance presented by Z_3 is low enough compared to the gain of the error amplifier that the minor loop can be approximated as $(Z_1 \| Z_2 \| Z_3)/Z_3$, the loop transmission of the entire system can be found. Looking at the block diagram this is simply $BB(s)H_{major}/H_{minor} = BB(s)Z_3/Z_1$ where BB(s) is the converter transfer function. Z_3/Z_1 will be denoted by H_c.

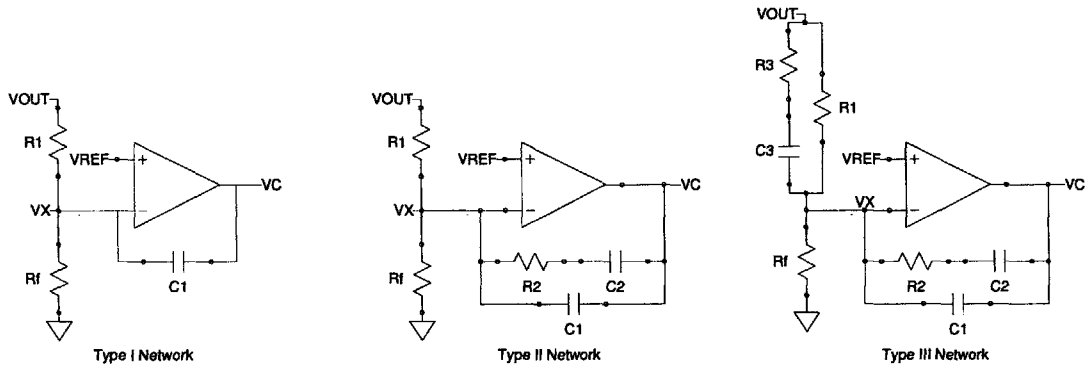

Figure 3-5: Compensation Networks

3.3 Compensation Networks

The converter can be compensated with any of the compensation networks shown in Figure 3-5. Compensation is performed for a 15% overlap system, however the principles behind the compensation schemes can be applied to systems with different amounts of overlap. Changing the overlap has an effect on which duty cycles, input voltages, and output voltages are present in each region and since the converter transfer functions can depend on these parameters the compensation network may need to be adjusted with overlap. There are three compensation schemes: Type I, Type II, and Type III. Each scheme yields progressively better results. This nomenclature is found in the LTC3440 data sheet [9] and in Intersil Technical Brief 417 [11] and is preserved here. The stability of the system is analyzed at high frequency where $H_c = Z_3/Z_1$ with the recognition that the low frequency behavior of the loop transmission will not factor into the stability analysis. As long as the loop crossover is less than the bandwidth of the error amplifier and the compensated system is always less in magnitude than the error amplifier transfer function, even near crossover, the analysis will be valid. The error amplifier can be approximated as a single pole system with a low frequency gain of 90 dB and a 1MHz bandwidth.

3.3.1 Type I

Type I compensation consists of no more than a dominant pole. R_1 and C_1 form an integrator producing the compensator H_{c_I} shown in Equation 3.1

$$H_{c_I} = \frac{1}{sR_1C_1} \tag{3.1}$$

As a baseline the recommended values for R_1 and C_1 provided by the LTC3440 data sheet were used and adjusted. 340KΩ is chosen for R_1 and must remain constant as it forms a resistor divider with the 200KΩ R_f to regulate the output to 3.3V. To achieve reasonable phase margin of 89.8° in buck mode a $3nF$ capacitor is used for C_1. This provides an adequate gain margin of 8.6 dB. At high V_{in} in the boost region the gain and phase margins are about the same. As V_{in} decreases the gain margin degrades until the converter goes unstable. To prevent this a higher value for C_1 can be used. In the buck-boost region the phase margin is also about 89° but the gain margin is consistently about 3 dB. Again, a large capacitor will add more gain margin. In all cases the loop crossover occurs at low frequencies on the order of 1KHz. Dominant pole compensation provides stability but lacks speed. An optimal system would provide between 45 and 60 degrees of phase margin at a higher bandwidth.

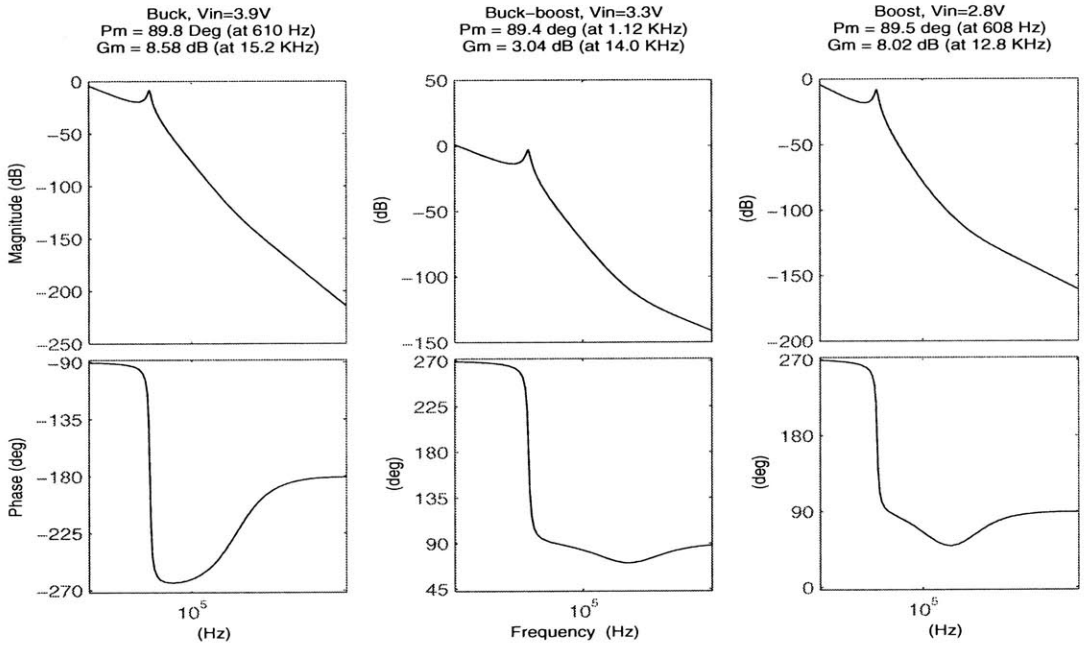

Figure 3-6: Type I compensated system in all regions for a typical load of $600mA$. Source code: Section D.7.

3.3.2 Type II

A type II network with transfer function H_{cII} as shown in Equation 3.2 adds a pole and zero in the fashion of a lag compensator. However, this compensation does not add enough phase near crossover to provide adequate phase margin. Though the converter can be compensated

with a Type II network, the result takes more advantage of the dominant pole behavior of the compensator as it pushes the transfer function down so that the resonance caused by the peaking in the converter transfer function does not factor in. It would make more sense to just use a Type I network as it provides the same result but with less components [11].

$$H_{c_{II}} = \frac{1}{R_1} \frac{1 + sR_2C_2}{s\left(C_1 + C_2 + sR_2C_1C_2\right)} \tag{3.2}$$

3.3.3 Type III

Type III compensation improves over Type II by adding another zero and pole to provide more phase near crossover resulting in the compensator transfer function $H_{c_{III}}$ shown in Equation 3.3. This also allows for increased bandwidth in the compensated loop. A Type III compensator can seem daunting, but if it is broken down it is rather straightforward. Several observations about the pole-zero pairs can be made to make compensation easier. The first concerns the pole and zero created by R_2 and C_2. Referring to locations of the pole and zero as ω_{z_2} and ω_{p_2} and assuming ω_{z_2} is the lowest frequency zero it is seen that the frequency of ω_{z_2} is simply $1/(R_2C_2)$ and that ω_{p_2} is a factor of $(C_1 + C_2)/C_1$ above ω_{z_2}. Additionally at ω_{z_2} the compensator transfer function takes on a flat slope and the magnitude here is $\frac{R_2}{R_1}\frac{C_2}{C_1+C_2}$. Since ω_{p_2} is usually placed at least a decade above ω_{z_2}, $C_2 >> C_1$, the second factor for the magnitude equation is close to one, and the magnitude is largely dependent on R_2/R_1. This magnitude is used to push the converter transfer function down to force it to crossover below the bandwidth of the error amplifier and to make sure that its magnitude peaking falls below the error amplifier transfer function, much the way a dominant pole would push the transfer function down [11].

$$H_{c_{III}} = \frac{1}{R_1} \frac{\left(1 + sR_2C_2\right)\left(1 + s\left(R_1 + R_3\right)C_3\right)}{s\left(C_1 + C_2 + sR_2C_1C_2\right)\left(sR_3C_3 + 1\right)} \tag{3.3}$$

The second pole-zero pair can be referred to as ω_{z_3} and ω_{p_3} where $\omega_{p_3} = 1/(R_3C_3)$ and ω_{z_3} is a factor of $1/(\frac{R_1}{R_3} + 1)$ below ω_{p_3}. In the full Type III system ω_{z_3} could be placed after ω_{z_2}, and then ω_{p_2} and ω_{p_3} would follow in order. After ω_{z_3} the transfer function would increase with a slope of 20dB/decade until ω_{p_2} at which point the slope would be zero and the magnitude would be a factor of $\omega_{p_2}/\omega_{z_3}$ above $\frac{R_2}{R_1}\frac{C_2}{C_1+C_2}$. This magnitude will push the converter transfer function up a little, pushing out the crossover frequency. With Type III,

the benefit of the dominant pole is realized as it pushes the transfer function down so it is close to being stable, but then the second pole-zero pair pushes the portion of the converter function near crossover up which extends the bandwidth. Since the second pole pair also provides additional phase this extension of the crossover point is acceptable.

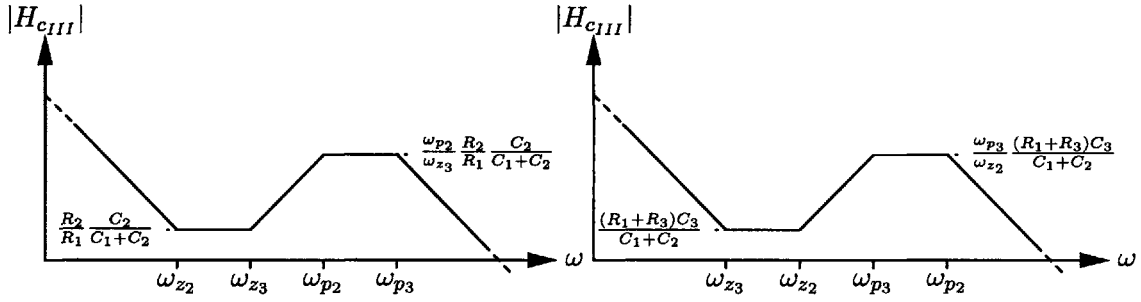

Figure 3-7: Type III bode plots for $\omega_{z_2} < \omega_{z_3}$ and $\omega_{z_3} < w_{z_2}$

Compensation in the above manner produces a set of values for the elements in the compensation network and adequate phase margin in all regions can be achieved. However, when compared to the values used in the 3440 datasheet [9] the component values for C_1 and C_2 are quite a bit higher. This is because ω_{z_2} was placed below ω_{z_3} making C_2 large. The LTC3440 compensation scheme placed ω_{z_3} below ω_{z_2} and also ω_{p_3} below ω_{p_2}. This allows C_2 to be made smaller which in turn allows C_1 to be made smaller. Compensating it in this way allows the use of physically smaller components which may be favorable. Figure 3-7 shows example Bode plots of these two methods of Type III compensation. When picking component values it is convenient to write a Matlab script that calculates component values based on user specified frequencies for ω_{z_2}, ω_{z_3}, ω_{p_2}, and ω_{p_3} and magnitude after the first zero. This removes complication of one component value affecting multiple parameters. Component values that were found to compensate the converter correctly with $V_{out} = 3.3$V and L=10μH over a range of input voltages and load currents are shown in Table 3.1.

Table 3.1: Component Values for Type III Compensation

	3440	$\omega_{z_2} < \omega_{z_3}$	$\omega_{z_3} < \omega_{z_2}$
C_1	10pF	200pF	15pF
R_2	15kΩ	10kΩ	6.8kΩ
C_2	330pF	20nF	1.5nF
R_3	2.2kΩ	3.3kΩ	680Ω
C_3	220pF	56pF	300pF

Though these values have been found to work for a particular converter with its speci-

fications and operating range, it is likely that the values found will not work for converters with different specifications such as input voltage range, overlap, load current, or required output voltage. Thus the methods and reasoning behind the compensation schemes should be learned so that they can be applied correctly. Also, when compensating a real converter on an actual board the capacitor values in particular can be far below the specified value. This gets worse as the capacitor's physical size gets smaller. For example, a 22μF 0603 size ceramic capacitor had a measured value of 7.5μF which is a significant difference.

Figure 3-8 shows the phase margin and crossover frequency as a function of V_{in} for the fully compensated converter at load currents of $200m$A, $600m$A, and 1A. As the load increases the phase margin is less in boost and buck-boost mode as the right half plane zero will be closer to the origin. In the input range from 2.5V to 6V where the converter is specified to operate the phase margin is adequate, though at low V_{in} and high load current the phase margin goes below 45 degrees. Since the input current limit on the LTC3440 is 1A at minimum input voltage the load current will be constrained to $758m$A which will be about 30 degrees of phase margin. Depending on what the load requirements are for a particular application the component values may have to be changed. This is merely an example of how a converter like this might be compensated. It is more useful to understand the compensation method than to memorize values.

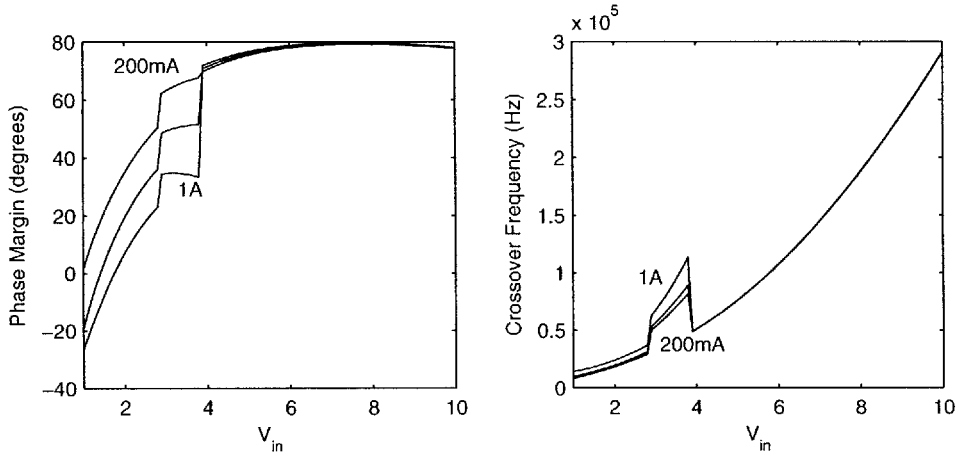

Figure 3-8: Type III phase margin at $200m$A, $600m$A, and 1A. Source code: Section D.8.

Chapter 4

PWM Comparators

To produce a PWM waveform the PWM comparators of the buck-boost converter each compare a triangle wave against the control voltage, V_c, provided by the error amplifier. The position at which the control voltage slices through the triangle wave will determine the duty cycle of the PWM waveform. Typically two triangle waves are offset in voltage and overlapped, creating a buck-boost region as previously explained. One triangle is fed to each comparator, and V_c is fed to both; the outputs of the two comparators are the AB and CD PWM waveforms. The triangle wave oscillator can produce a triangle wave with any voltage offset and any amplitude subject to the limitation that the triangle wave must fit within the common mode range of the PWM comparators determined by the lowest supply rail.

The offset triangle waves could be created by having two oscillators generating the same amplitude wave at different offsets. Alternatively, a single triangle wave oscillator could be used with two outputs from the error amplifier that are offset with respect to each other. As the two outputs sweep through a single triangle wave the effective PWM waveforms produced would resemble those of a system with one control voltage and two offset triangle waves. In the former case, matching the two triangle waves exactly while having the correct overlap would require DC level-shifting a high frequency AC waveform with minimal distortion. The latter case is preferable as it is easier to DC level shift a control voltage that is essentially DC when in closed-loop regulation. However, it is subject to the restricted headroom limitation.

4.1 Using PWM Comparators to Create Overlap

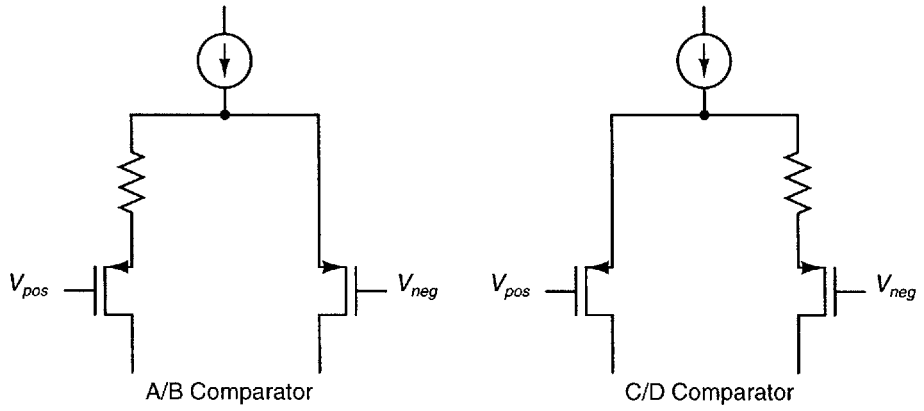

Figure 4-1: Input differential pairs of the A/B and C/D comparators with offset resistors.

An alternate solution to the overlap problem can be achieved with a novel implementation of the PWM comparators. A resistor is placed in series with one of the pMOS transistors of the comparator differential pair as shown in Figure 4-1. At balance, the tail current set up by the pMOS current mirror splits evenly between each leg of the differential pair. Thus a drop forms across the resistor equal to $I_{TAIL}R/2$. Now for a balance condition the voltage at the input side with the resistor must be lower by this offset voltage with respect to the other input instead of being equal as in the case of a regular comparator with a balanced input stage.

Two comparators can then be used with one triangle wave and the control voltage, V_c, to generate the PWM waveforms. The comparators are set up so that the A-B comparator has the resistor on the positive input leg and the C-D comparator has the resistor on the negative input leg. V_c is connected to each comparator's positive input while the triangle wave serves as the negative input. When the control voltage is at $V_{tri_{min}} - V_{os}$ the A-B comparator will start producing a PWM waveform with a small duty cycle, D_A. As the control voltage increases this duty cycle gets larger until $D_A = 1$ at which point $V_c = V_{tri_{max}} - V_{os}$. Meanwhile, the C-D comparator will start producing a duty cycle D_C when $V_c = V_{tri_{min}} + V_{os}$ increasing from zero to one when $V_c = V_{tri_{max}} + V_{os}$. Thus as V_c moves, the effective control voltage controlling the A-B comparator leads V_c in voltage by V_{os} while the effective control voltage for the C-D comparator lags V_c in voltage by V_{os}. D_C gets inverted in a later stage to produce D_D. Thus, as the control voltage sweeps up, D_A

increases while $D_D = 1$ corresponding to a buck region. Then, while D_A increases further D_D starts to decrease causing a four switch buck-boost region. Finally D_A increases to one and a boost condition occurs. In circuit limits are placed on the boost duty cycle so it does not become too high which can cause adverse effects.

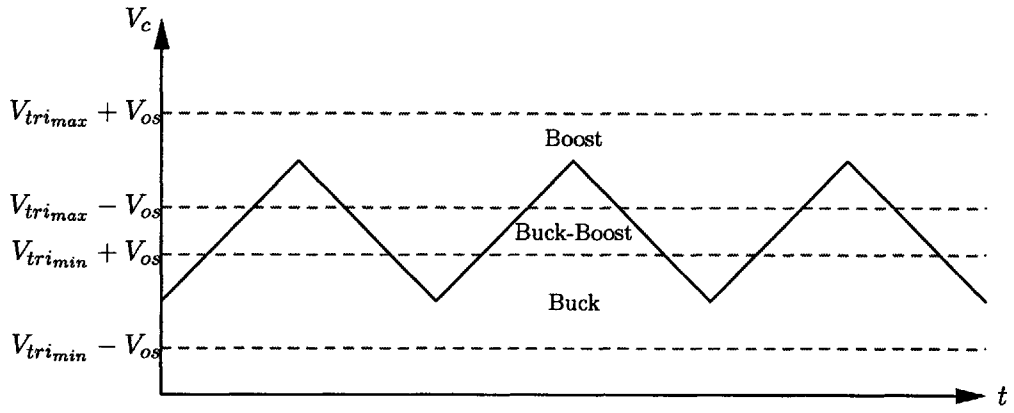

Figure 4-2: Region Boundaries

Figure 4-2 shows the real triangle wave along with the boundaries of each region. The buck region falls between $V_{tri_{min}} - V_{os}$ and $V_{tri_{min}} + V_{os}$; the buck-boost region falls between $V_{tri_{min}} + V_{os}$ and $V_{tri_{max}} - V_{os}$; and the boost region falls between $V_{tri_{max}} - V_{os}$ and $V_{tri_{max}} + V_{os}$. Thus the width of the buck-boost region and the value of the effective triangle overlap voltage is $V_{tri} - 2V_{os}$.

4.2 Implementation

The two inputs of a comparator must be a certain distance apart in voltage for a valid comparison to occur. In other words, the comparator requires a certain amount of overdrive for a valid comparison to be made. This stems from the characteristic equation for a MOSFET in saturation where the current varies with $(V_{gs} - V_T)^2$. The term $V_{gs} - V_T$ is referred to as the overdrive of the transistor. In a comparator the difference between the inputs is also called the overdrive, though it relates closely to the overdrive of the individual transistors as it will affect the V_{gs} of both devices. When a comparison is made in a comparator, the tail current of the differential pair moves from one leg to the other. Since the overdrive voltage directly determines the current through each MOSFET, the amount of overdrive will determine how the tail current flows.

Several parameters affect the propagation delay. When sufficient comparator overdrive is present, the MOSFETs can swiftly switch the current from one leg to the other. As the overdrive increases the comparator switches faster because one of the transistors gets turned on even harder, forcing the current to switch even more. Then the propagation delay depends on how fast the nodes of the comparator can slew in order to switch the voltage at the output. As the overdrive decreases the input transistors have less ability to switch the current swiftly. In this case less current will be available to slew the nodes of the comparator and it will take longer for the output to be realized. This nonlinearity in propagation delay as overdrive decreases can have a substantial effect on the PWM waveforms when these comparators are used in the converter.

In the case of the triangle wave, the tip of the triangle wave may come and go faster with respect to the control voltage than the comparator may be able to change its output, causing a pulse not to be generated. The tip does not rise above V_c enough to effect a change in the output. Making input devices with a high W/L ratio can help, as less overdrive is needed to switch the current, though this will increase input capacitance. As the tail current increases for the same devices, the output current increases which charges the output node faster, though since the transconductance is proportional to the square root of the current as tail current is increased delay may not decrease linearly. In other words, increasing the tail current does not cause a linear decrease in propagation delay, though it will cause a decrease.

4.2.1 Simple Comparator with Current Mirror Load

A comparator with a first stage consisting of a *p*MOS differential pair with a current mirror load and a tail current source as shown in Figure 4-3 is one option for the PWM comparator. However, its disadvantages become apparent upon careful inspection of its operation

When one input rises above the other the comparator wants to switch the tail current from one leg of the differential pair to the other. During the time of transition there exists an output current as the current in one leg decreases and the current on the other leg increases. The current mirror load of the comparator enables this difference current to appear as an output current. This output current charges or discharges the output node of the first stage and ultimately the second stage output as well. After the transition, the amplifier reaches a new steady state at a different operating point. At this operating point, any current

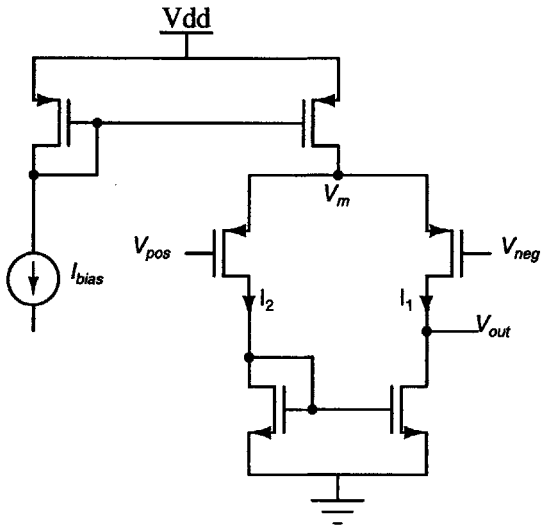

Figure 4-3: Differential pair with current mirror load used as a comparator.

that flows through legs of the differential pair is explained by what the transistor operating points are. For example, the operating point at which the output is at ground exists when the positive input is less than the negative input. In this case more than half up to all of the tail current will flow through the positive input transistor, and less current will flow through the other leg. The nMOS at the output has no current through it, causing its drain to source voltage to be zero, and thus causing V_{out} to be zero. When the positive input starts to increase, it pushes the voltage at the sources of the differential pair up with it as most of the tail current still flows through the positive input transistor. If the negative input is held constant the V_{sg} of the negative input transistor starts to increase, increasing the current in that leg. This starts a current exchange process during which the current mirror supplies the difference current to the output node, charging that node. This entire process is highly nonlinear as the gate source voltages are changing and all the DC bias parameters are changing, though it can be approximated by the small signal model. When the circuit settles to a new operating point, the tail current is found to be split between each leg, with the negative leg getting approximately two thirds of the current. Current still flows through the positive leg and sets up a V_{gs} for the diode connected nMOS of the current mirror. This V_{gs} along with the current through the output nMOS occurs at a point for which the V_{ds} of that output transistor is large. Thus the output node remains high. This process is reversed when the inputs switch again. A second stage common source amplifier with an active load and successive inverters can provide faster rise and fall times.

This topology has several disadvantages. First of all the propagation delay is dominated by the charging and discharging of the Miller capacitor at the common source stage. Increasing the tail current will speed this charging, but nothing has been done to avoid this slow node. Second, the two states of the comparator are intrinsically different because of the diode connected transistor in the active load. For large input voltage difference when the output of the first stage is high all the tail current will flow through the pMOS transistor of the differential pair connected to the output and none will flow in the other transistor of the pair. In the other case when the output of the first stage is low some tail current will still flow in the output pMOS although most of it will flow on the diode connected side. This leads to output currents that are different for each state, which means the Miller node is slewed at different rates. Since PWM waveforms are being generated from triangle waves the delay should be the same for both directions of output switching. Finally, the transconductance of the first stage may not be enough to enable small overdrive. A small overdrive can be likened to a small signal and thus the transconductance of the comparator is significant. More transconductance introduces more gain which could cause successive comparator stages to trip for smaller input overdrives to the first stage.

Since the overlap in the triangle wave system is made smallest when extreme duty cycles can be reached it is advantageous to design the PWM comparator to operate with the smallest delay and smallest overdrive possible. The current mirror load comparator just does not achieve that.

4.2.2 Improved Comparator with Decision Circuit

An improved topology shown in Figure 4-6 exists that exhibits less overall propagation delay and more balanced delays in each switching direction. It consists of a differential pair with a positive feedback decision circuit as a load. The decision circuit consists of two diode connected MOSFETs which form current mirrors with MOSFETs whose drains are connected in a cross coupled manner back to the drains of the differential pair, as shown in Figure 4-4. These diode connected MOSFETs form current mirrors whose outputs directly feed the single-ended output [1, p. 685-691]. At the comparator output are two diode connected MOSFETs, an nMOS and a pMOS, serving as clamps to restrict the swing at that node (Figure 4-6). This stage looks like a CMOS inverter with its input tied to its output and keeps the output node close to mid-rail, allowing a swing of about $60mV$ with

a 3.3V positive rail. This is desirable because the Miller capacitor at that node won't have to be charged or discharged much during a transition. The next stage is an inverter sized proportionally to the diode clamps, but much stronger. In this way a small variation is picked up, amplified, and fed to a final inverter.

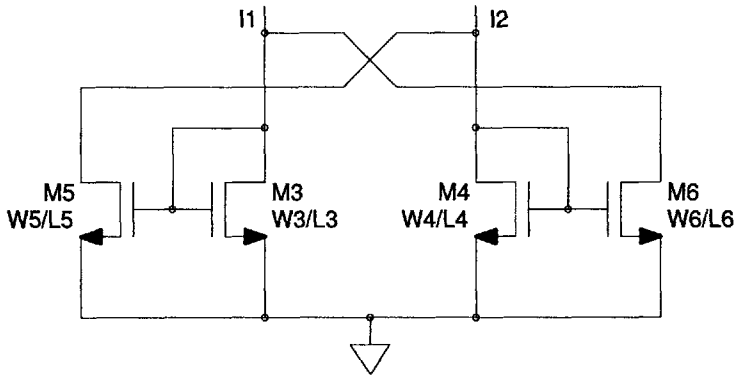

Figure 4-4: Comparator Decision Circuit

This comparator has the benefit of all the nodes in the first stage being low impedance, save the output node of the second stage. This means all of these nodes will be able to slew fast. The node of concern at the output of the second stage is taken care of by restricting its swing with the diode clamps. Thus this comparator can achieve small propagation delay.

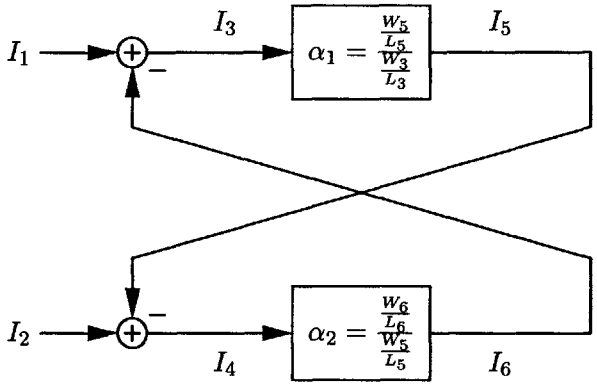

Figure 4-5: Block diagram of comparator decision circuit. Nominally $\alpha_1 = \alpha_2$.

The decision circuit is designed so that the mirror ratios between the M_3-M_5 pair and the M_4-M_6 pair are less than one. Figure 4-5 shows the feedback loop formed by this decision circuit. Considering the I_1 and I_2 loops separately, one input can be set to zero and then the other loop can be analyzed. As the loop is traversed two minus signs are encountered creating positive feedback. The loop transmission is α^2, where α is the current

mirror ratio in the decision circuit. Thus to ensure stability for each loop α^2 must be less than one. Then the transfer function from I_1 to I_3 and from I_2 to I_4 are both $1/(1-\alpha^2)$. Since the output currents are derived by mirroring I_3 and I_4 this positive feedback circuit gives a transconductance boost. More transconductance reduces required overdrive and propagation delay. Increasing α increases the transconductance boost, but also brings the loop transmission closer to one. Mismatch in the mirrors could raise the loop transmission above one and cause instability. As α increases the devices M_5 and M_6 become larger which increases capacitance and can cause delay. In simulation a ratio was found that optimized the tradeoffs and produced the smallest delay.

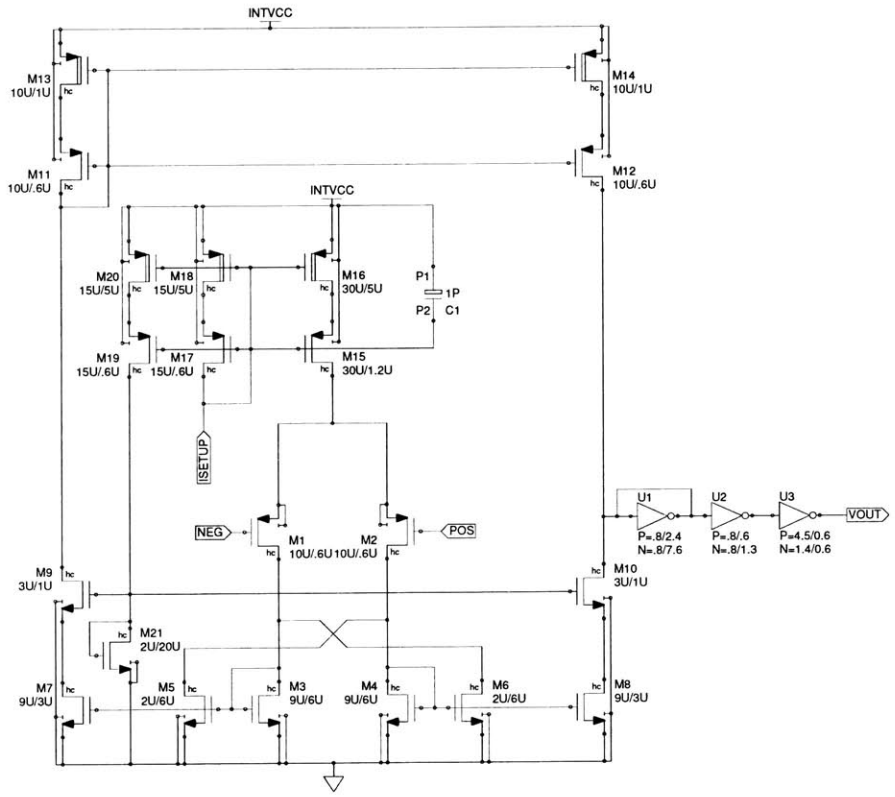

Figure 4-6: Complete comparator design shown without any offset resistor on the differential pair.

The comparator is dependent on current mirrors being accurate in order to produce the same propagation delay for both transitions. Thus, cascodes were used throughout the design shown in figure 4-6. The top pMOS mirror formed by M_{13} and M_{14} are native devices with a higher V_T than the regular pMOS cascode devices M_{11} and M_{12}. This allows for the

gates of both devices on the input side of the mirror to be connected while still keeping both transistors saturated, eliminating the need for a separate cascode bias voltage. It was difficult to form full cascode mirrors for the M_7 and M_8 mirrors since the drains of M_1 and M_2 were required to be as close to the rails as possible for input common mode range considerations. Thus the devices M_9 and M_{10} form cascodes at M_7 and M_8 and are provided with a fixed DC bias voltage at their gates. This provides adequate output resistance increase for those mirrors and improves current matching.

The final consideration for this improved comparator involves the technique for producing voltage overlap in the converter system as discussed previously. Resistors are placed in series with either the source of M_1 or M_2 to achieve the required overlap. Thus, the tail current source is cascoded to ensure that an accurate current flows through the offset resistor. This ensures a reliable and expected overlap. The input current source should be derived from a bandgap-voltage and a resistor that is matched to the offset resistor to create a bandgap referred offset voltage. The offset resistor as well as the tail cascode introduce input common mode range problems. These problems are mitigated by making the length of the cascode device M_{15} longer to reduce $V_{gs_{15}}$ and thus $V_{ds(sat)_{16}}$ while keeping M_{16} in saturation. The triangle wave is made $500mV$ in amplitude swinging from $400mV$ to $900mV$ (as discussed later in Chapter 5). The common mode range for the comparator with no resistor is about $100mV$ to 1.3V below the positive rail. By arranging the comparators as shown in Figure 4-7 the common mode problem becomes easier. The AB comparator has the offset resistor on the positive leg, reducing the upper boundary of the input common mode range at that input. The control voltage is present at this input and only has to provide reliable comparisons for the buck and buck-boost regions which, for no overlap, will be $150mV$ to $650mV$. The inverting input will be the triangle wave, $400mV$ to $900mV$. The CD comparator has the same inputs but its offset resistor appears in the negative leg. The inverting input has to handle the triangle wave, but even with the offset reduction in common mode range, this pin will handle it. V_c must range from $650mV$ to $1.15mV$ which it will be able to do at the minus pin. Thus input common mode range problems are avoided.

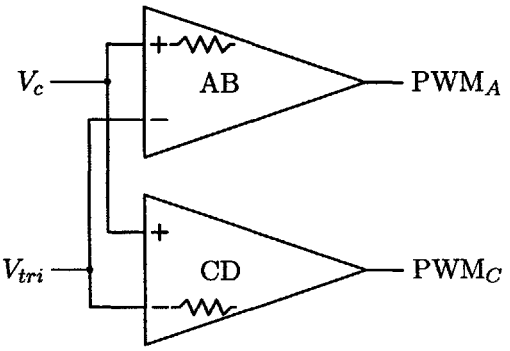

Figure 4-7: Dual Comparator Arrangement

4.3 Performance

The comparators for this design were chosen to use a substantial amount of tail current over the comparators used in the 3440. This extra current helps the comparator to switch faster, achieve lower duty cycles, and have balanced transitions, properties that were favorable and worth the power tradeoff. This comparator uses between 30μA and 50μA of current depending on the output voltage. When the output voltage goes high, current flows in both outer legs of the first stage, causing increased current consumption. The shoot-through current in the diode clamp and the second stage inverter also contributes to current consumption. A tail current of 10μA was chosen as it provided an optimized tradeoff between propagation delay and input common mode range as the tail current will affect the V_{gs} of the cascode and thus the $V_{ds(sat)}$ of the mirror device. This is illustrated in Figure 4-8 for which the propagation delay and common mode range are graphed against tail current. Here common mode range is defined as the input voltage for which the tail current deviates from its nominal value by 1%.

Since the propagation delay was reduced to $15ns$ the duty cycle of the PWM signal that could be generated ranged from 2% to 98%. Figure 4-9 shows the duty cycle generated by a dual comparator system as used in the converter with a triangle wave at the inverting input and the control voltage at the non-inverting input. These are generated with comparators for which an offset resistor corresponding to a 15% overlap was chosen. Note these duty cycles are the inputs to the output driver block which drives the switches, a stage which has its own effect on the PWM waveforms. While making the comparator propagation delay smaller is an important aspect of the triangle wave buck-boost design, it is not the end-all

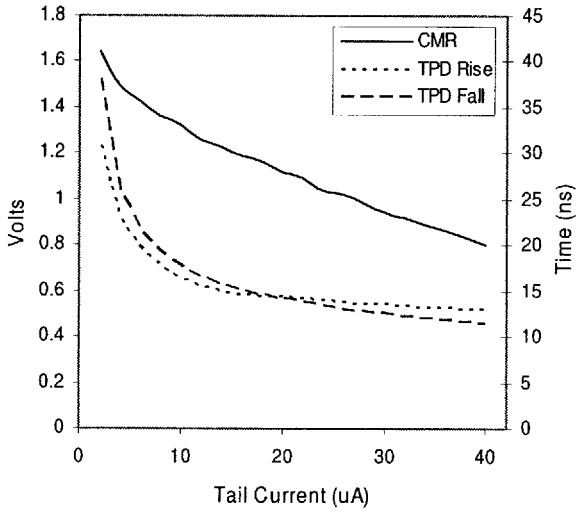

Figure 4-8: Common mode range and propagation delay vs. tail current.

as the output block adds a significant amount of delay, and can dominate the nonlinear propagation effects.

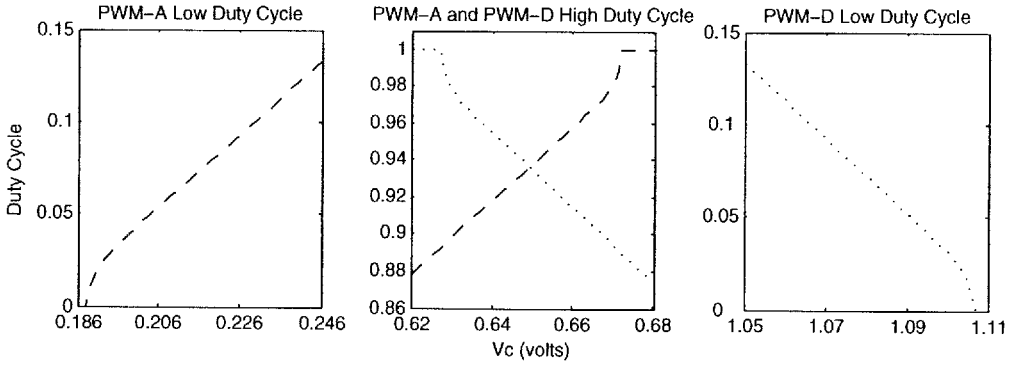

Figure 4-9: Duty Cycles for Switch A and Switch D

Chapter 5

Full Converter

The full triangle wave converter system relies on several building blocks, the most important of which are the PWM comparators and the triangle wave oscillator, which is discussed here. In addition there are many intricacies associated with designing an integrated circuit and the buck-boost converter in particular. Though important to the eventual viability of a product, some of these considerations are not central to the concept of the triangle wave converter and go beyond the scope of this paper, but the primary ones are mentioned in this chapter.

5.1 Triangle Wave Oscillator

The triangle wave oscillator is one of the core elements of the buck-boost converter as it supplies the waveform from which a PWM signal can be generated. A fully functional transistor level design of a triangle wave oscillator was designed to help strengthen the case for the triangle wave buck-boost converter. By comparing the area and quiescent current of the PWM generation blocks in each converter it can be seen that the triangle wave based converter uses substantially less area and quiescent current. The design of the oscillator is presented here and a schematic appears at the end of the section in Figure 5-1.

5.1.1 Design and Operation

The heart of the triangle wave oscillator is a capacitor, C_{tri}, which is charged and discharged with a current of the same magnitude to achieve a linear voltage ramp in both directions, creating a triangle wave. The target specification for this oscillator was 50% duty cycle

operation at 1MHz. A comparator looks at the voltage on C_{tri} and a reference voltage that has two states depending on whether C_{tri} is charging or discharging. When the comparator trips it causes the reference voltage and the direction of the capacitor current to change. In this way the triangle wave oscillation can be controlled.

A value of $4p$F was chosen for C_{tri} to provide reasonable accuracy with process variation. In order to achieve enough headroom with a minimum supply voltage of 2.7v and overlap requirements related to the PWM comparators and error amplifier, a target amplitude of 0.5 volts was chosen. Furthermore, the triangle wave had to swing from 0.4V to 0.9V. Charging a $4p$F capacitor to 0.5 volts in 500ns corresponds to a charging current of 4μA. This 4μA is available from a cascoded current mirror whose input setup current is 2.5μA. This current can charge the capacitor through pMOS M_{10} when $V_{sw} = 0V$. When a discharge condition is required V_{sw} goes high turning M_{10} off and M_9 on. Then the same 4μA charging current is mirrored through an nMOS cascoded current mirror whose output current discharges the capacitor though M_9 to ground. In this way the charging and discharging of the capacitor requires 4μA throughout the entire period. Other schemes use separate current sources and sinks for charging and discharging. Each source would constantly draw current even when not being used corresponding to a total current consumption of 8μA.

During design a problem arose with the biasing of the nMOS cascoded current mirror. The current mirror uses two nMOS native devices as cascode devices whose threshold voltage is lower than the regular nMOS mirror devices. The nMOS mirror devices have their bulk contact tied to ground as required by the design rules of the process. Because of the switching action the V_{gs} of the mirror varies during charging because the triangle wave pulls up the drain of M_{21} and the sources of M_{22} and M_{23} float. During switching there is nonlinearity in this V_{gs} and it doesn't hold the same value needed to make the current mirrored 4μA. This results in large spikes of current for a short amount of time. By KCL this current comes from C_{tri} causing the tip of the triangle wave to be distorted. To fix this, capacitor C_2 was used to hold this V_{gs} constant during switching. It allows the node V_2 to move common mode with V_1 and filters any large ripple in the difference of V_1 and V_2. This greatly reduced current spikes from the capacitor. However, this capacitor, if too large, needs a long time with respect to the frequency of oscillation to charge up from the current source provided by the M_{14} mirror. In this case the full discharging current is not mirrored to the capacitor current, causing distortion. This can be interpreted as an under damped

case while no capacitor can be interpreted as an over damped case with large overshoot. It turns out that a nominal value of $100fF$ is the right value to provide a critical damping case V_{gs} is held constant enough to prevent a current spike and the capacitor is small enough to prevent a long tail charging transient.

A capacitor was also added across the V_{gs} of all the pMOS mirror devices to provide bias stability and constant charging currents. "Free cascodes" were achieved by using native devices and used for the capacitor charging current mirrors and the reference resistor source.

The comparator is three stages, the first of which is a differential pair with a current source tail bias and an active current mirror load. This differential pair first stage is followed by two common source stages with active loads. The differential pair transistors had to be kept at a reasonable size so that the current required to charge the gate of M_1 was not so large as to cause noticeable distortion in the triangle wave.

The output of the comparator, V_{c_3} is used to change the reference voltage, V_{ref}, and to change the direction of the capacitor current. V_{c_3} drives two inverters which drive M_7 which is connected across the reference resistor R_1. A second resistor, R_2 is connected from R_1 to ground. When M_7 is off the current through R_1 and R_2, which is set my the current mirror M_{18}, sets V_{ref}. When M_7 turns on it shorts R_1 and V_{ref} becomes the value of the drop across R_2. Thus the reference voltage switches between IR_2 and $I(R_2 + R_1)$. The bias current and resistors were set to achieve a $500mV$ triangle wave ranging from $400mV$ to $900mV$ but because of comparator delay the amplitude ended up being larger. So the resistor values were reduced at simulation time to achieve the required amplitude. On chip these resistors would be split up into sections and trimmed with fuses to obtain the correct amplitude.

V_{c_3} also causes the change of current direction in C_{tri}. V_{c_3} is fed through a Schmitt trigger and an inverter. The Schmitt trigger causes the switching of V_{sw} to always occur after the change of reference voltage. This ensures that there is no race condition, that there will be no chatter on the tip of the triangle wave, and that the comparison is validated before the current changes.

5.1.2 Performance

The triangle wave oscillator was tested over a range of operating conditions to verify its ability to accurately produce an acceptable triangle wave. The frequency and amplitude of

oscillation as well as the DC offset are important parameters that are crucial to the operation of the converter. The frequency must stay constant so that the feedback loop can be designed based on one switching frequency and the filter components can be sized appropriately. The amplitude of oscillation depends on the overlap used in the system. Designing for a worst case of no overlap, the amplitude of two stacked triangle waves would have to fit between the rails without taking any transistors in the oscillator out of saturation. The common mode range of the error amplifier further constrains this amplitude as it provides the voltage that slices through the triangle waves. If the effective overlapped triangle waves fall outside this common mode range a maximum boost duty cycle and a minimum buck duty cycle will be imposed. Given these restrictions it is important that the triangle wave oscillator accurately produces the correct amplitude at the specified frequency.

In simulation the oscillator operates with a V_{in} of 3.6V at 27°C with a measured frequency of 1.077 MHz. The oscillator was tested over a range of input voltages and temperatures. The frequency varied by ±.5% over an input voltage range of 2.7V to 5.5V. Over a temperature range of -45°C to 125°C the frequency varied by ±4% from nominal. In steady state under nominal conditions the oscillator runs with 48.6μA of quiescent current and this value increases with the supply voltage to 65μA at 5.5V, but varies little with temperature.

In simulation the triangle wave oscillator consumes about 70% less quiescent power than its sawtooth generator counterpart. This consumption rate remains constant with temperature and supply voltage variations. The triangle wave oscillator achieves these power savings from reduced complexity and the use of the same current to charge and discharge the capacitor. The triangle wave oscillator is one circuit block with one charging capacitor and one comparator. The sawtooth generator requires four charging capacitors, two comparators, more logic circuitry, and more current biasing legs. Thus it consumes much more current and operates at a higher quiescent power. Furthermore, the triangle wave oscillator requires less on-chip area and if properly laid out could potentially save two thirds of the area that the sawtooth generator takes up. Not only are there far less devices in the triangle wave oscillator, but far less area needs to be devoted to routing wires. Clearly this oscillator is a core component in the savings and advantages associated with the triangle wave converter.

Table 5.1: Triangle and Sawtooth Oscillator Power Comparison at 27°C

V_{in}(V)	$I_{saw}(\mu A)$	$P_{saw}(\mu W)$	$I_{tri}(\mu A)$	$P_{tri}(\mu W)$	Tri Power Savings
2.7	149.1	402.5	45.5	122.7	30.5%
3.6	161.8	582.5	48.6	174.9	30.0%
4.2	172.5	724.6	52.4	220.0	30.4%
5.5	206.9	1137	64.2	353.3	31.1%

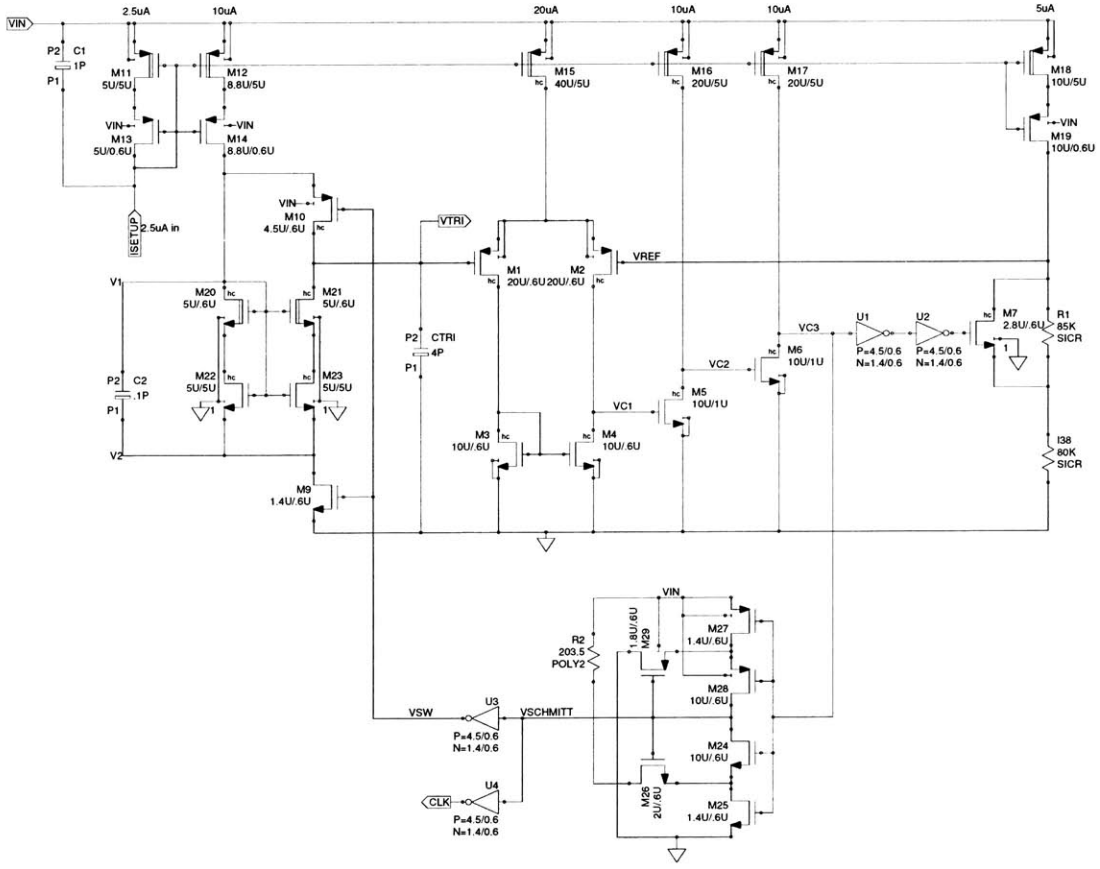

Figure 5-1: Integrated Triangle Wave Oscillator

5.2 Output Block

The main switches, A, B, C, and D, require proper drive circuitry that prevents shoot through current. The output block uses successive stages of tapered CMOS inverters to build up to the switches which minimize propagation delay. To avoid shoot through current, a latch-like structure ensures that for each switch pair the pMOS completely shuts off before the nMOS turns on and vice versa.

A requirement exists in the output block that greatly affects the propagation delay in the system and ultimately the minimum overlap of the triangle waves in the system. There exists a capacitor that is Miller multiplied at the output of the inverter driving the main switches. This capacitor restricts the slew rate of the output of the switches, which are connected to the inductor. This slew rate limit comes from an EMI requirement. The large current that the main switch handles cannot ramp up too quickly or EMI interference may be generated. This EMI may not necessarily affect the converter operation, but may affect other devices in the application or may be above required EMI limits.

This slew rate limiting adds significant delay to the output block stage. This delay in effect determines what duty cycles are available for a given V_c and makes low and high duty cycles harder to achieve. This means that there must be more overlap in the triangle waves. If the overlap was too small and a particular duty cycle was not realized, the converter may exhibit oscillatory behavior in this region. In the buck-boost region the converter is operating with high switch A and switch D duty cycles. Because the triangle waves are overlapped, the upper tip of the AB triangle wave that produces the highest switch A duty cycle is at a V_c for which a small switch C duty cycle occurs. Conversely at the lower tip of the CD triangle wave the highest switch D duty cycle is produced and a lower switch B duty cycle is produced. When the triangles are overlapped enough it is ensured that if a high duty cycle required in buck-boost mode is unattainable the converter will be able to operate in either the buck or the boost region because the other switch has wide enough duty cycle. If overlap is reduced too much there could exist a V_c in the buck-boost region for which both a switch A and a switch D duty cycle can not be achieved. In this case switch A and D will default to being on all of the time. The range of V_c for which this happens is a dead zone where the conversion ratio is always one. Because of this V_c will not be able to regulate the output because for a change in V_c no change in V_{out} will occur

and the error amplifier will try to slam V_c even further, leading to oscillations and potential instability.

One of the major reasons for using the sawtooth converter and having a method for obtaining effective sawtooth waveforms was to reduce the nonlinear propagation delay and thus decrease overlap. But if the output block limits this because of its own delay then spending complexity on the sawtooth system may not be worth it. It seems that either type of converter will be restricted to a safe 15% overlap and any large improvements in the comparator delay will not reduce this overlap much.

New output block designs were pursued but proved beyond the scope of the project. The body diodes in the output switches greatly affect the PWM waveforms as they can either increase or decrease duty cycle depending on how the transistor driven and in what direction current flows through the body diode.

5.3 Error Amplifier and Max Boost Conversion Ratio

The error amplifier shown in Figure 5-2 is designed to have a low-frequency gain of 90 dB and a unity gain bandwidth of 1 MHz. It is a fairly straightforward design and consists of a differential pair as a first stage and a common source second stage with a Miller capacitor for split pole compensation of the amplifier. The output stage is designed to swing from $V_{ds} + V_{gs}$ to a clamp voltage. This clamp voltage is set by the V_{gs} of a pMOS whose gate is held at a voltage set up by a current through a resistor. The output of the error amp is then level shifted with a pMOS diode so that the final output, V_c, ranges from ground to about one volt. This means that the highest V_c available from the error amplifier will not be able to produce high boost duty cycles as high V_c will be required for those duty cycles. This enforces a maximum boost conversion ratio which will ensure that the converter does not operate at boost duty cycles that will make the converter unstable. As the conversion ratio is increased in boost mode the converter becomes unstable. The resistor used to set the clamp voltage can be matched to the resistors in the triangle wave oscillator so that the clamp voltage will track with the placement of the triangle waves.

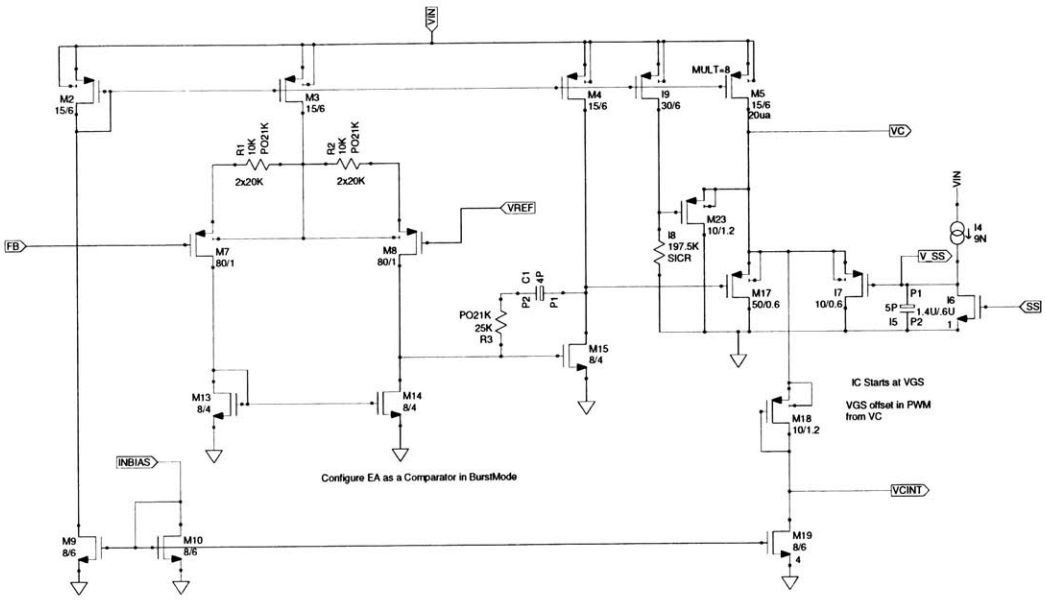

Figure 5-2: Schematic of error amplifier.

5.4 Current Limit and Other Considerations

A current limit scheme was employed primarily for the purposes of simulation, but it is definitely required in a finished product. The current limiting scheme limits the output current by using a sense pMOS that is in parallel with the main pMOS switch and is driven with the same gate voltage as the main switch. The current derived from this switch can be used to set up a voltage that is used to override the PWM waveforms and not allow additional power to be taken from the input when the current limit threshold has been reached.

One must be concerned with shutting the part down when not in use. Extra devices can be added all over the chip to turn off functional blocks when the converter is not in use and goes into a shutdown mode. In shutdown quiescent current should be as low as possible so as not to drain the battery in application. Care must go into designing shutdown circuits so that they are reliable.

The part must also be able to withstand variations in operating temperature and the functional blocks have been designed to be resistant or at least predictable with changes in temperature. If the part becomes too hot a thermal shutdown mode should be incurred where the part stops operating and cools down. This prevents damage to the part.

The concept of the triangle wave buck-boost has been proven in simulation and as discussed later with a lab setup. However, due to time constraints, no layout of the integrated circuit has occurred but will be crucial in making the converter work as all kinds of parasitic affects can be present. As mentioned, the triangle wave based converter should take up significantly less area than its sawtooth wave based counterpart. It is estimated that the triangle wave based converter would take up approximately two thirds the area for the sawtooth based converter. This takes into account all functional blocks besides the large switches (which may occupy up to half the chip or more). This savings is in part due to the oscillator design and the fact that only one oscillator capacitor is needed. Also, the simplicity of the triangle system eliminates some blocks present in the sawtooth converter and saves on area.

5.5 Simulation Results

The triangle wave converter was evaluated in simulation over a range of input voltages and load currents in order to determine efficiency. Overall the converter performed very well, both in steady state and during transients. Figure 5-3 shows an example of such a simulation where the input voltage is 3.3V and the load current is stepped in $100mA$ steps from $100mA$ to $700mA$. At startup the converter is slowly brought into regulation with the aforementioned current limiting scheme. The maximum allowable current rises linearly at startup and prevents large initial inductor currents. After starting up to a load of $700mA$, the load is stepped down to $100mA$ and then stepped back up in $100mA$ increments. At the transitions there is little overshoot or ringing in the regulated output voltage as the compensation network is providing adequate phase margin and bandwidth. Figure 5-4 shows the converter efficiency for a 15% overlap at several load currents. An ideal current was mirrored to simulate a real current load for the converter. These efficiency plots are in line with what Matlab predicted in Chapter 2. SPICE source code used to generate these plots is included in Appendix C

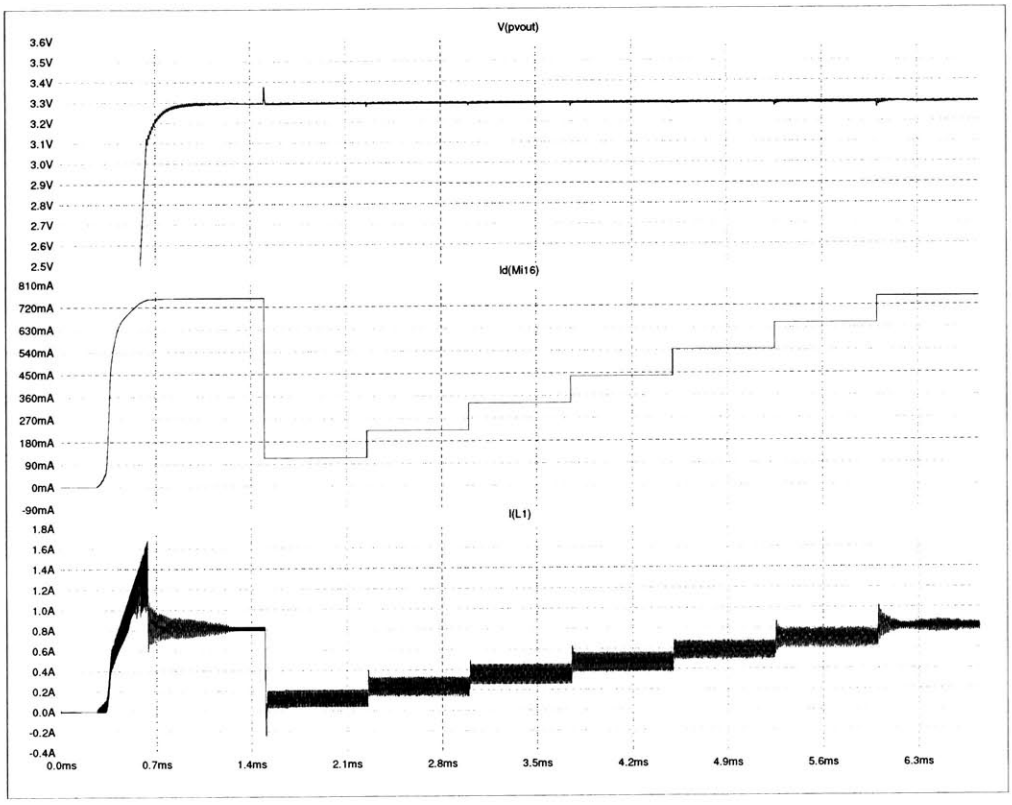

Figure 5-3: Spice simulation results for triangle wave based buck-boost converter at V_{in}=3.3V and $P_{ov} = 15\%$.

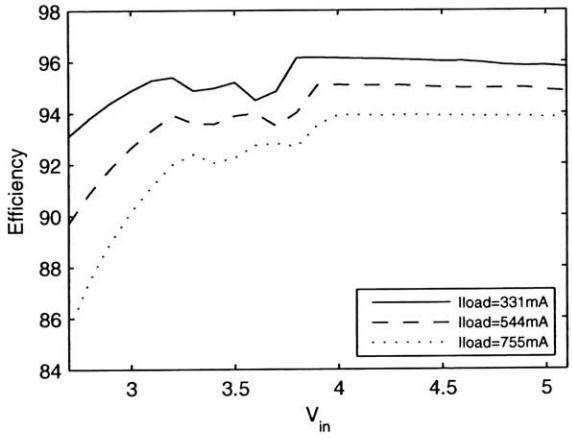

Figure 5-4: Spice simulation results for triangle wave based buck-boost converter at V_{in}=3.3V and $P_{ov} = 15\%$.

Chapter 6

Lab Design

To confirm that an actual triangle wave buck-boost converter could work and provide accurate regulation a demonstration board was constructed. This board used discrete components to generate PWM waveforms that drove four MOSFET switches. The PWM waveforms were generated by comparators whose inputs were a control voltage generated by a feedback loop and a triangle wave provided by a function generator. The setup allowed for operation in the buck, boost, and buck-boost regions, and allowed for a qualitative look at the triangle wave converter's transient behavior.

6.1 Basic Design

The lab design tried to faithfully simulate the integrated version of the buck-boost converter with discrete components in order to get an accurate representation of what could occur in an actual integrated circuit. Switches were chosen with on resistances similar to those of the switches in the LTC3440, even though switches with lower on resistances were available. Comparators were chosen to have similar overdrive capabilities as those in the LTC3440. Special attention was paid to the layout of the board so that it could function as well as an integrated circuit version. This layout took into account the power section and the signal level section of the converter and kept these parts isolated. Kelvin connections were used to accurately sense the output voltage so it could be regulated with precision.

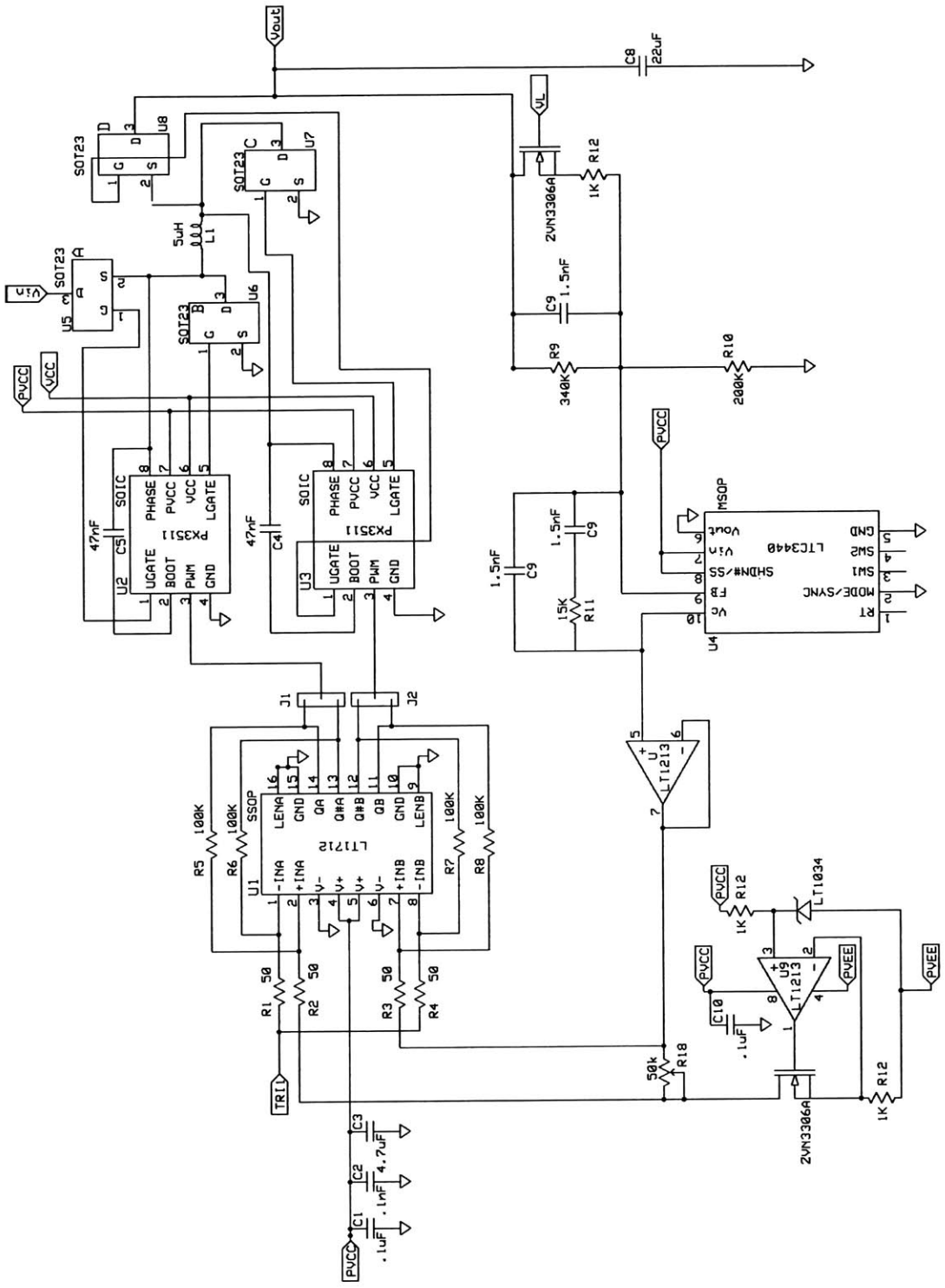

Figure 6-1: Triangle Wave Converter Demonstration Board Schematic

Fairchild FDN337N n-channel MOSFETs were used for the four switches [4]. They had a $50m\Omega$ typical on resistance and a gate charge of $3n$C. To drive the switches, Primarion PX3511B driver chips were used [13]. These devices are able to drive two nMOS switches in a totem pole configuration with the use of a bootstrap capacitor that provides enough gate charge to turn on the top switch. These Primarion drivers accept 5V PWM waveforms and require a supply rail of 12V. An additional supply rail was needed for the drive voltage for the gates of the switches. This voltage had to be below the maximum allowable gate voltage and 5V was chosen. The bootstrap capacitor allowed the gate of the upper switch to be driven with a V_{gs} of this value. Because the PX3511B can only drive two nMOS transistors, two were needed for all four switches. The switches were laid out close together with considerations for how the large converter currents would flow. The switch traces where kept on one side of the copper board which allowed a continuous ground plane to reside underneath the switches. Large traces were used to connect between switches and large pads were left to help dissipate heat as shown in a close up view of the switch layout in Figure 6-2. A 5μH Sumida inductor (CDRH6D28-5RD) was connected between the midpoints of the switch pairs and placed close to the switches. These layout techniques helped make a robust and reliable design.

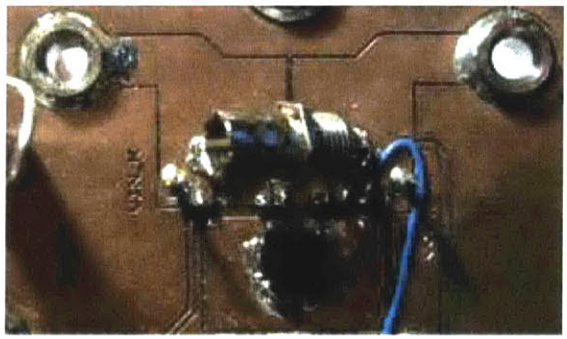

Figure 6-2: Close up of switch layout.

To replicate the feedback loop the error amplifier was used from a real LTC3440. The LTC3440 provides a feedback pin and a V_c pin for external compensation purposes. These pins were utilized to access the error amplifier and its internal bandgap reference for use in the discrete design. This also allowed for use of a Type III compensation network. When powered up, the LTC3440 tries to perform its main function as a DC to DC converter and as such it will attempt to make its onboard switches switch by driving their gates with

PWM waveforms. For the purposes of this board the switching is not desired because it could introduce noise and other disturbances to the circuit. To prevent this, the V_{out} pin was connected to ground along with the SW2 pin, which is the midpoint of the C and D switches where the inductor can be connected to the chip. This prevents switching of switches C and D from moving the SW2 pin voltage because the source of the switch D pMOS is connected internally to the V_{out} pin. However, this could not be done for the A and B switches as V_{in} could not be tied to ground because it provides the rail for the error amplifier. Noise that was observed at the output of the converter seemed to couple in with a frequency of about 0.25 Hz and the switching of switches A and B was attributed to this noise. Even though no programming resistor was used to program the switch frequency, small leakage currents caused the switching frequency to be extremely low as the switch frequency is proportional to the amount of current leaving the PROG pin.

An LT1712 dual comparator [10] was used to generate the PWM waveforms from the control voltage, V_c, and a triangle wave from a function generator. The LT1712 is rated for $4.5ns$ of propagation delay at $20m$V of overdrive and is fast enough for the application. The triangle wave is a fixed input at 1MHz, and in order to create overlap there must be a DC offset in V_c. This offset was created by using a current source and resistor. An LT1213 op amp [8] was used to control an nMOS transistor and feedback around this op amp was used to provide a constant current source as shown in Figure 6-3. A negative supply rail was used to extend the common mode range of V_c for which the current remains constant. To create different overlaps the offset can either be kept at a constant value and the amplitude of the triangle wave can be changed or the potentiometer can be used to adjust the offset while keeping the triangle wave amplitude the same.

The lab design was the product of a layout that was built, tested, and optimized. The final version incorporated a tight layout that minimized parasitic effects as much as possible. This final version is pictured in Figure 6-4.

6.2 Performance

This board was built in order to qualitatively examine the transient behavior of the triangle wave buck-boost converter and to obtain an estimate of the converters efficiency. The converter performed well over a range of operating parameters and accurately regulated the

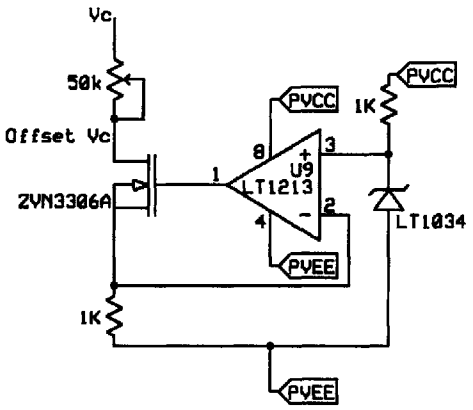

Figure 6-3: Demonstration Board Offset Generator

output voltage to a desired 3.3V with a typical ripple of $10mV$pp. The converter responded as expected to changes in overlap values as the width of the buck-boost region changed. The points at which transitions between regions occurred were consistent with the equations derived in Chapter 2. In addition, the conversion ratios and duty cycles of the switches for a given V_c were consistent with prediction. Efficiency measurements were taken at a load current of $500mA$ and Figure 6-5 shows the result as a plot of the efficiency over a range of supply voltages for several overlap values. To calculate η the buck-boost input and output voltages and currents were measured, V_{in}, V_{out}, I_{in}, and I_{out}. Additionally, the current supplied by the PVCC rail, I_{PVCC}, as well as its voltage, V_{PVCC}, was measured because the PVCC rail on the Primarion driver is the rail used to supply the gate drive to the switches. The input power was then the sum of this gate charge power and the buck-boost input power. Not included in the efficiency calculation was the quiescent power consumed by the rest of the circuits on the board or the small amount of power supplied by the function generator.

Agreeing with the predictions in Chapter 2, Figure 6-5 shows that for a given input voltage the efficiency in the four switch region increases as overlap decreases. This observation is seen best for the 11% and 5.5% overlap cases. For the 33% and 66% overlap cases the converter operates in the buck-boost region for the entire range of input voltages shown on the plot. Furthermore, at low input voltage for the 11% and 5.5% overlap cases where the converter operates in boost mode there is a sharp fall in converter efficiency as the input is reduced further because I^2R losses increase faster than CV^2f losses decrease. Similarly in the buck region the efficiency decreases with rising input voltage, but does so

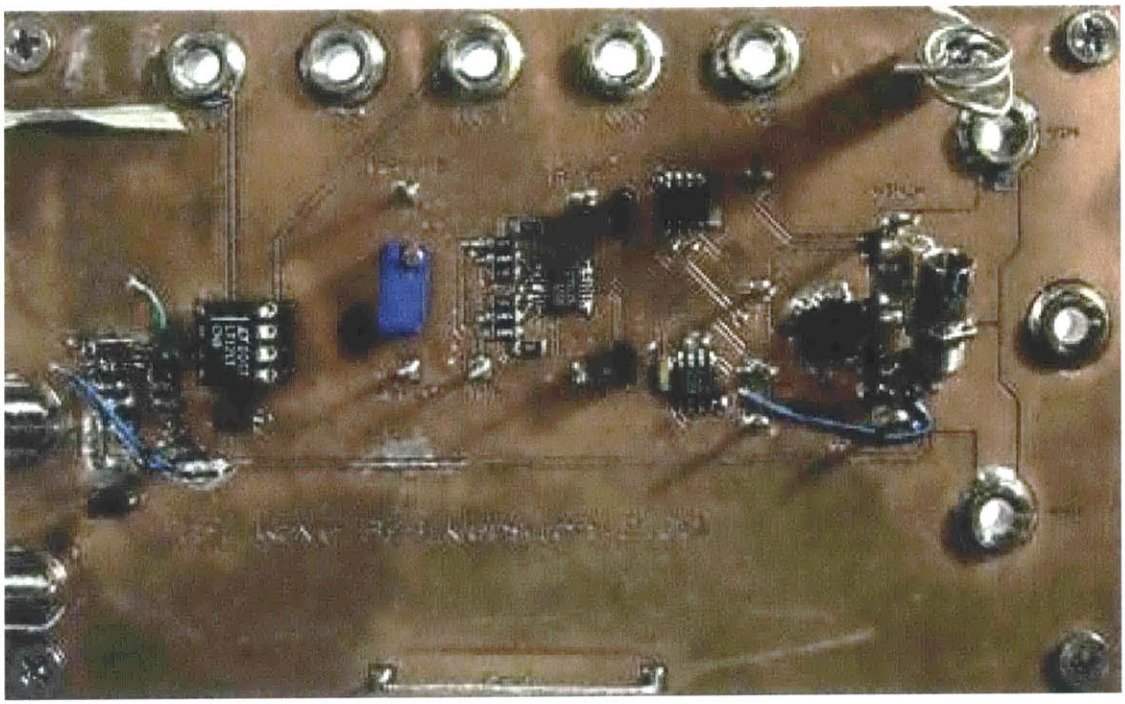

Figure 6-4: Triangle Wave Converter Demonstration Board

much more slowly than in boost becasue here the CV^2f are increasing as the I^2R losses decrease. In the buck-boost region the efficiency is lower because all four switches switch during the cycle. Outside the buck-boost region the efficiency should have been the same for all overlap cases, though the graph shows that they are slightly different. Overall, this demonstration board showed how the triangle wave converter could work in the real world and serves as a confirmation that a triangle wave converter is a viable option.

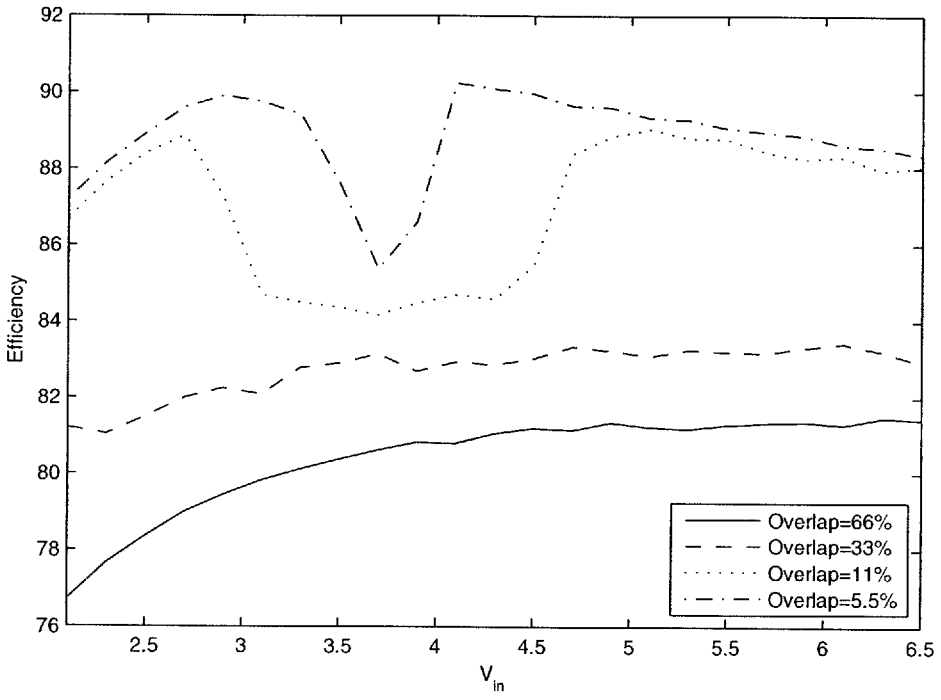

Figure 6-5: Efficiency vs. V_{in} for the Lab Design

Chapter 7

Conclusion

The triangle wave buck-boost converter has several advantages over the sawtooth buck-boost converter and these advantages may merit the use of the triangle wave converter. It has been shown that the triangle wave converter is similar to the sawtooth converter in many ways. Most of the mathematics are the same for both converters. The conversion ratios are the same for a given overlap and a given V_c. The converter transfer functions are the same and thus frequency compensation is the same for each. These similarities are favorable because if a triangle wave converter is substituted for a sawtooth design, its implementation does not necessitate a major redesign of the whole converter.

The differences between the two converters show why the triangle wave converter might be better. Though the triangle wave converter is mathematically more efficient, it is not so much more efficient to merit using it over the sawtooth converter. Rather, the advantage of the triangle wave converter is in its simplicity. The reduced complexity helps build reliability and increase understanding of converter operation which could yield insight on future improvements. The triangle wave converter also uses less die area for control circuitry because only one capacitor is required for the oscillator instead of four. Also a lot of the circuitry involved with the oscillator and timing signals in the sawtooth generator are no longer required and this also reduces area. In fact it is estimated that such a triangle wave converter will use two thirds of the area used by the sawtooth converter, neglecting the area used by the power switches.

If the triangle wave converter does use less area, then why were the sawtooths used in the first place? The reasoning behind the sawtooth system was to avoid the effect of

nonlinear propagation delay in the comparators. Indeed, the multiplexing scheme used in the sawtooth converter restricts the comparator to operating in the middle of the real sawtooth waveforms so that the propagation delay becomes linear. In this case then there is always enough overdrive to realize the high duty cycles of A and D in the buck-boost region. This is the most important place to have accurate duty cycle production because if high duty cycles cannot be achieved, the overlap will have to be increased. However, the output block has a large effect: it adds a larger delay than the comparators for most duty cycles, though its effect is seen most at high and low duty cycles. The effect of this puts a big restriction on the overlap in the system. The comparator delay in both the sawtooth and triangle wave systems is smaller than the delay in the output block, and the output block will dominate and determine the minimum overlap.

This trait of the output block could exist in many types of output blocks designed for EMI requirements on the switch slew rates and may be an acceptable tradeoff. Both the sawtooth-based converter and the triangle-wave-based converter suffer this tradeoff. Simulation results and calculations showed that a safe amount of overlap in the triangle wave is 15%, which is exactly the amount that the LTC3440 uses for its sawtooth waves. The only thing that the delay in the comparator stage might change is the gain from V_c to $\tilde{d}$ which will just change compensation parameters. The feedback loop will work to servo out any nonlinearity. In actuality the PWM waves are analog signals and the duty cycles that can be produced as V_c changes change continuously but not always linearly. This means that the feedback loop will be able to servo to the correct duty cycles and conversion ratio. The conversion ratio function will still be continuous.

More power was devoted to the PWM comparators in the triangle wave based converter to improve them over the ones used in the LTC3440 in order to allow for more duty cycles to be produced at reduced overdrive. This comparator, aided by a decision circuit, achieved delays on the order of $15ns$ and the delay was the same in each direction of switching to match the symmetry of the triangle waveform. Power that was saved on the oscillator blocks was used to make these comparators run faster. This further reduced the effect of the comparators on the amount of overlap.

In the laboratory a demonstration board was constructed to verify that a triangle wave converter could work. Qualitative results on the converter's ability to start up and faithfully regulate an output voltage were positive and the triangle wave converter seemed capable of

doing its job. Efficiency measurements matched the expected behavior in all three regions of operation.

The triangle wave converter could be a viable buck-boost converter. This paper provides a foundation for such a converter with insight on mathematical framework, frequency compensation, and circuit level design. In particular, the full transistor level design of the triangle wave oscillator, which is the heart of the triangle wave converter, shows that the triangle wave converter can indeed use less area than the sawtooth system. The primary difference in the two lies with the oscillators, the related circuitry, and the fact that the sawtooth converter requires more circuitry – four capacitors and all of the extra digital circuitry. Additionally the triangle wave system saves on quiescent current for these blocks as it uses the same current source to charge and discharge the oscillator capacitor, though some of this savings is spent on making faster PWM comparators.

Considerations certainly have to be made for an integrated circuit version of the triangle wave converter. The circuit would have to be constructed fully complete with special shutoff circuits, startup circuitry, and all other requisite circuits for the converter to be viable as an integrated circuit. The LTC3440 makes use of a Burst Mode which periodically delivers power to a load at very low output power. This functionality would have to be explored in relation to the triangle wave converter, although it could be identical to the LTC3440 implementation. A full layout of the triangle wave converter would also be necessary. Though this paper does not treat these matters it is assumed that these are reasonable tasks and that the ideas presented already may lead to a successful integrated buck-boost converter. Though this converter will have about the same efficiency as a sawtooth converter, its simplicity and area savings could be a benefit. As buck-boost converters are pushed to higher switching frequencies a simpler architecture may be more scalable. Area savings may allow for multiple buck-boost converters on a single chip which may be favorable in applications that require two different regulated voltages. The triangle wave converter exhibits many favorable properties and can be considered for regular use.

Appendix A

Average Inductor Current for $V_{in} = V_{out}$

This Appendix shows that the average inductor current in the sawtooth system is greater than in the triangle system for $V_{in} = V_{out}$. Because of the inherent symmetry of the triangle system inductor ripple, its average inductor current is simply $I_{out}T/(T - t_{AC})$. To find the average inductor current for the sawtooth system the ripple waveform is integrated, divided by the period, and added to the offset current (Equation A.3) that the cycle begins at found in Chapter 2.

$$\begin{aligned}\overline{I_L} = I_{os} \quad &+ \quad \frac{1}{T}\int_0^{t_{AD}} m_{AD}t\,dt + \frac{1}{T}\int_{t_{AD}}^{t_{AD}+t_{AC}} (m_{AD}t_{AD} + m_{AC}t)\,dt \\ &+ \quad \frac{1}{T}\int_{t_{AD}+t_{AC}}^{T} (m_{AD}t_{AD} + m_{AC}t_{AC} + m_{BD}t)\,dt \end{aligned} \tag{A.1}$$

Evaluating the integrals the following equation for the average inductor current is found. This equation is true anywhere in the buck-boost region.

$$\overline{I_L} = I_{os} + \frac{1}{T}\left(\frac{m_{AD}t_{AD}^2}{2} + m_{AD}t_{AD}t_{AC} + \frac{m_{AC}t_{AC}^2}{2} - \frac{m_{BD}t_{BD}^2}{2}\right) \tag{A.2}$$

$$I_{os} = \frac{T}{T - t_{AC}}\left(I_{out} - \frac{1}{2T}\left(m_{AD}t_{AD}^2 - m_{BD}t_{BD}^2\right)\right) \tag{A.3}$$

At $V_{in} = V_{out}$ m_{AD} equals zero and combining Equations A.3 and A.2 with this fact

yields Equation A.4. This result is simplified in Equation A.5 by combining the $m_{BD}t_{BD}^2$ terms.

$$\overline{I_L} = \frac{T}{T - t_{AC}} \left(I_{out} + \frac{m_{BD}t_{BD}^2}{2T} \right) + \frac{1}{2T} \left(m_{AC}t_{AC}^2 - m_{BD}t_{BD}^2 \right) \tag{A.4}$$

$$\overline{I_L} = \frac{T}{T - t_{AC}} I_{out} + \frac{m_{AC}t_{AC}^2}{2T} + \frac{-t_{AC}}{T - t_{AC}} \frac{m_{BD}t_{BD}^2}{2T} \tag{A.5}$$

Since at $V_{in} = V_{out}$ the AC area and the BD areas are the same Equation A.5 can be further simplified to Equation A.6:

$$\overline{I_L} = \frac{T}{T - t_{AC}} I_{out} + \frac{T - 2t_{AC}}{T - t_{AC}} \frac{m_{AC}t_{AC}^2}{2T} \tag{A.6}$$

The second term in Equation A.6 must be greater than zero because the maximum value t_{AC} can be is $T/2$ which occurs at a 100% overlap. Therefore $\overline{I_L}$ must be greater than $I_{out}T/(T - t_{AC})$ making the average sawtooth inductor current greater than the average triangle wave inductor current. This result suggests that the average sawtooth inductor current might be greater at other input/output combinations and it is found numerically that this is true for most values of overlap that are of interest.

Appendix B

Extension of the Triangle Wave Benefit

The triangle wave inductor ripple waveform achieves lower loss in part because at its highest absolute value it is less than that of the sawtooth generated inductor ripple. The triangle wave converter split the AD phase in two and placed it at different parts of the cycle. This gain from splitting the AD phase can be exploited to increase efficiency even further. Consider for simplicity the case where $V_{in} = V_{out}$, the inductor ripple is completely symmetrical with an average value of $I_{out}/(T - t_{AC})$, the slope $m_{AD} = 0$, the slope m_{AC} is positive, the slope m_{BD} is negative, and $m_{AC} = -m_{BD}$. One of the two AD phases causes the inductor current to stay at its highest value whereas the other phase causes it to stay at its lowest value. The amplitude is of course determined by the height $m_{AC} \cdot t_{AC}$ which is the same as $m_{BD} \cdot t_{BD}$. Imagine the AD phase now split into four equal pieces, each for a time $t_{AD}/4$, as in Figure B-1. The cycle moves in the following progression: AD, AC, AD, AC, AD, BD, AD, BD. There are two AC phases and two BD phases but their lengths are also halved as are the AD phases with respect to the triangle wave converter. This new waveform has the same average value, $I_{out}/(T - t_{AC})$, but the time spent at higher absolute current values is less and the square law relationship between the power loss and the current means that the loss for this new waveform will be less.

It would be nice to spend as little time as possible at the highest AD phase and splitting the AD phases further achieves that. If there are $n = 2$ AD segments for the triangle waveform converter there are $n/2 = 1$ AC and BD phases. In the four AD phase type

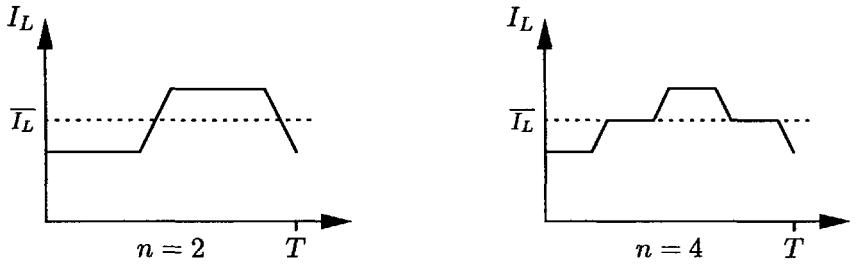

Figure B-1: Regular triangle wave ripple and 4 AD phase ripple at $V_{in} = V_{out}$. The flat segments are AD phases, the AC segment has a positive slope, and the BD segment has a negative slope.

above there are $n = 4$ AD segments and $n/2 = 2$ AC and BD segments. Correspondingly the lengths of each segment are t_{ad}/n, $2t_{ac}/n$, and $2t_{bd}/n$. If the number of AD segments is doubled, the time of those segments is halved, and there are double the AC and BC segments. This method is extendable for all $n = 2^i$ where $i = 1, 2, 3....$ As n increases the inductor ripple looks like two straight lines. This looks very similar to a buck-boost with no overlap so that there is no AD phase and just an AC and BD phase, a very inefficient type of buck-boost converter. However in such a converter current is not delivered to a load whereas in an n phase converter power is delivered for $T(1 - P_{ov}/2)$ where $TP_{ov}/2$ corresponds to the length of the AC phase. Figure B-2 shows the inductor ripple waveforms for n =8, 16, and 32. Notice the average value is always the same but the ripple looks more and more like two straight lines. Figure B-3 shows the average loss decreasing as n is increased.

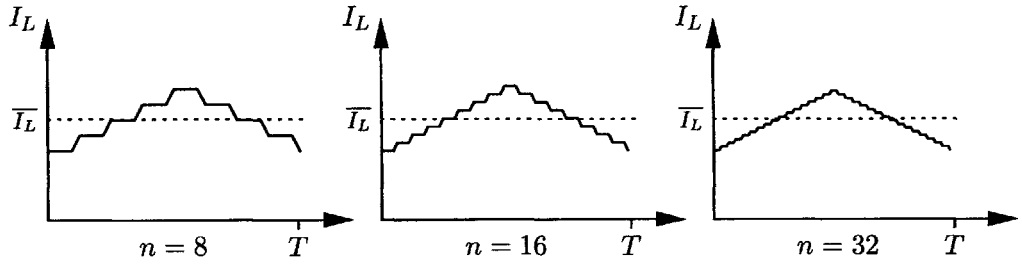

Figure B-2: Higher Iterations of the Multiple AD Phase Converter at $V_{in} = V_{out}$. The flat segments are again AD phases, the AC segment has a positive slope, and the BD segment has a negative slope.

Practically such an n-type converter would not be achievable with current technology because of switching loss in the MOSFETs. The amount of switching, or frequency of switching, for each cycle increases with n. The effective frequency of switching also goes

up and current technologies may not support this and if a technology could handle higher frequency, using the regular triangle converter would reduce the amplitude of the ripple anyway. As switch loss decreases with new technologies this n type topology may be more useful. However, the triangle wave converter only really showed marginal improvement over the sawtooth so would it really be worth it to move to an n-type system? The complexity of making such a converter may greatly outweigh the benefit in using it. How switches would be controlled may be extremely complex. The simplicity gained by going to the triangle is favorable and the marginal efficiency gain is a bonus. The small efficiency increase for an n converter would probably not be worth the cost in complexity, but it is instructive to show that method used in the triangle wave converter is part of a broader principle. This information shows that the triangle wave converter is a solid design choice – a good tradeoff between complexity and efficiency.

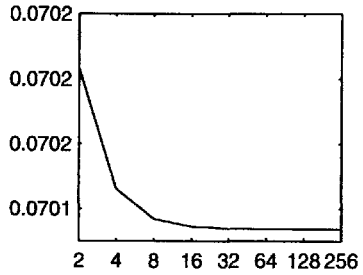

Figure B-3: Average Loss in an N-type Converter

Appendix C

Spice Simulation Source Code

This appendix contains the SPICE code used to simulate the full triangle wave buck-boost converter. The plots in Chapter 5 are made with the results of this simulation.

C.1 Spice .cir File

```
.include c:/projects/meng/a/schem/tri_toplevel4.spi
.include c:/projects/meng/a/lib/pspice/tt.par
.lib c:/projects/meng/a/lib/pspice/cmos060.lib
.model pch ako: mp
.model nch ako: mn
.model mpnl ako: mnn
.model pchnat ako: mpn
.model nchnat ako:mnn
.model mnnl ako:mnn
.model mnl ako:mn
.model po21k ako:rp2res
.model pact ako:rpactl
.model mnedsl ako:mn
.param Vdd=4.8
.step param {Vdd} 2.5 6.0 .1
Vpvin pvin 0 pwl (0 0 .01u {Vdd})
Vintvcc $g_intvcc pvin dc 0
```

```
Vkill4 kill4 0 pwl(0 {Vdd} 100u {Vdd} 100.1u 0 6m 0)
Vgnd gnd 0 dc 0
Vpgnd pgnd 0 dc 0
L1 sw1 sw2 5u
Iload 0 load 0 pwl(0 .7
+ 1.5000m .7
+ 1.5001m .1
+ 2.2500m .1
+ 2.2501m .2
+ 3.0000m .2
+ 3.0001m .3
+ 3.7500m .3
+ 3.7501m .4
+ 4.5000m .4
+ 4.5001m .5
+ 5.2500m .5
+ 5.2501m .6
+ 6.0000m .6
+ 6.0001m .7
+ 6.7500m .7)
.tran 0 6750u 1n
.aliases
.endalaises
```

C.2 Spice .spi File

This is a partial reproduction of the source .spi file used for the SPICE simulations. Since this circuit was built around existing circuit blocks of the LTC3440 not all circuit block netlists are included below. The below netlist includes circuits addressed in this paper including the triangle wave oscillator, the PWM comparators, the error amplifier, and circuitry that provides bias to these blocks. Not included below are parts of the current limiting scheme and the output drivers. Also not included for brevity are basic logic gates.

```
* LTC PSpice Netlist 6.71.0.6 - Laker AMS Version 6.10 50221
* tri_toplevel4.spi - 2006/12/22 6:03:04 PM
*
.SUBCKT ea_whit FB INBIAS SS VIN VREF V_SS VC VCINT
M7 N_9 FB N_7 N_16 PCH L=1U W=80U AS=128P AD=128P PS=163.2U PD=163.2U
+ NRS=0.008 NRD=0.008 M=1
M8 N_11 VREF N_6 N_16 PCH L=1U W=80U AS=128P AD=128P PS=163.2U PD=163.2U
+ NRS=0.008 NRD=0.008 M=1
M17 0 N_20 VC VC PCH L=0.6U W=50U AS=80P AD=80P PS=103.2U PD=103.2U NRS=0.012
+ NRD=0.012 M=1
M3 N_16 N_19 VIN VIN PCH L=6U W=15U AS=24P AD=24P PS=33.2U PD=33.2U NRS=0.04
+ NRD=0.04 M=1
M5 VC N_19 VIN VIN PCH L=6U W=15U AS=24P AD=24P PS=33.2U PD=33.2U NRS=0.04
+ NRD=0.04 M=8
M2 N_19 N_19 VIN VIN PCH L=6U W=15U AS=24P AD=24P PS=33.2U PD=33.2U NRS=0.04
+ NRD=0.04 M=1
M18 VCINT VCINT VC VC PCH L=1.2U W=10U AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
MI7 0 V_SS VC VC PCH L=0.6U W=10U AS=16P AD=16P PS=23.2U PD=23.2U NRS=0.06
+ NRD=0.06 M=1
M23 0 N_18 VC VC PCH L=1.2U W=10U AS=16P AD=16P PS=23.2U PD=23.2U NRS=0.06
+ NRD=0.06 M=1
M4 N_20 N_19 VIN VIN PCH L=6U W=15U AS=24P AD=24P PS=33.2U PD=33.2U NRS=0.04
+ NRD=0.04 M=1
MI9 N_18 N_19 VIN VIN PCH L=6U W=30U AS=48P AD=48P PS=63.2U PD=63.2U NRS=0.02
+ NRD=0.02 M=1
M15 N_20 N_11 0 0 NCH L=4U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U NRS=0.075
+ NRD=0.075 M=2
M10 INBIAS INBIAS 0 0 NCH L=6U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U
+ NRS=0.075 NRD=0.075 M=1
M19 VCINT INBIAS 0 0 NCH L=6U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U
+ NRS=0.075 NRD=0.075 M=4
```

```
M14 N_11 N_9 0 0 NCH L=4U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U NRS=0.075
+ NRD=0.075 M=1
M13 N_9 N_9 0 0 NCH L=4U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U NRS=0.075
+ NRD=0.075 M=1
M9 N_19 INBIAS 0 0 NCH L=6U W=8U AS=12.8P AD=12.8P PS=19.2U PD=19.2U NRS=0.075
+ NRD=0.075 M=1
MI6 V_SS SS 0 0 NCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U NRS=0.429
+ NRD=0.429 M=1
R2 N_16 N_6 PO21K 10K
R1 N_7 N_16 PO21K 10K
R3 N_11 N_17 PO21K 25K
C1 N_17 N_20 CP2P1 4P
CI5 0 V_SS CP2P1 5P
I4 VIN V_SS 9N
RI8 N_18 0 RSICR 197.5K
.ENDS ea_whit
***
.SUBCKT tri_abcomp ISETUP NEG POS VIN OUT
M8 ISETUP ISETUP N_10 VIN PCH L=0.6UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M28 OUT STAGE2 N_11 VIN PCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M29 0 OUT N_11 VIN PCH L=.6UU W=1.8UU AS=2.88P AD=2.88P PS=6.8U PD=6.8U
+ NRS=0.333 NRD=0.333 M=1
M27 N_11 STAGE2 VIN VIN PCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U
+ NRS=0.429 NRD=0.429 M=1
C1 VIN ISETUP CP2P1 1P
M2 DIFF2 NEG VM VM MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M1 DIFF1 POS VR VR MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M7 N_10 ISETUP VIN VIN PCHNAT L=5UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M4 DIFF2 DIFF1 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
```

```
M3 DIFF1 DIFF1 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M5 STAGE2 DIFF2 0 0 MNL L=1UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M9 VM ISETUP VIN VIN MPN L=5UU W=40UU AS=64P AD=32P PS=83.2U PD=41.6U
M10 STAGE2 ISETUP VIN VIN MPN L=5UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
RI35 VM VR RSICR 21.25K
M26 N_13 OUT N_12 0 NCH L=.6UU W=2UU AS=3.2P AD=3.2P PS=7.2U PD=7.2U NRS=0.3
+ NRD=0.3 M=1
M25 N_12 STAGE2 0 0 NCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U NRS=0.429
+ NRD=0.429 M=1
M24 OUT STAGE2 N_12 0 NCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
R2 VIN N_13 RPOLY2 203.5
.ENDS tri_abcomp
***
.SUBCKT tri_cdcomp ISETUP NEG POS VIN OUT
M8 ISETUP ISETUP N_10 VIN PCH L=0.6UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M28 OUT STAGE2 N_11 VIN PCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M29 0 OUT N_11 VIN PCH L=.6UU W=1.8UU AS=2.88P AD=2.88P PS=6.8U PD=6.8U
+ NRS=0.333 NRD=0.333 M=1
M27 N_11 STAGE2 VIN VIN PCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U
+ NRS=0.429 NRD=0.429 M=1
C1 VIN ISETUP CP2P1 1P
M2 DIFF2 NEG VR VR MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M1 DIFF1 POS VM VM MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M7 N_10 ISETUP VIN VIN PCHNAT L=5UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M4 DIFF2 DIFF1 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M3 DIFF1 DIFF1 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M5 STAGE2 DIFF2 0 0 MNL L=1UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M9 VM ISETUP VIN VIN MPN L=5UU W=40UU AS=64P AD=32P PS=83.2U PD=41.6U
```

```
M10 STAGE2 ISETUP VIN VIN MPN L=5UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
RI35 VM VR RSICR 21.25K
M26 N_13 OUT N_12 0 NCH L=.6UU W=2UU AS=3.2P AD=3.2P PS=7.2U PD=7.2U NRS=0.3
+ NRD=0.3 M=1
M25 N_12 STAGE2 0 0 NCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U NRS=0.429
+ NRD=0.429 M=1
M24 OUT STAGE2 N_12 0 NCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
R2 VIN N_13 RPOLY2 203.5
.ENDS tri_cdcomp
***
.SUBCKT triosc_500mv ISETUP VIN CLK VTRI
M9 V2 VSW 0 0 NCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U NRS=0.429
+ NRD=0.429 M=1
M26 N_11 VSCHMITT N_14 0 NCH L=.6UU W=2UU AS=3.2P AD=3.2P PS=7.2U PD=7.2U
+ NRS=0.3 NRD=0.3 M=1
M25 N_14 VC3 0 0 NCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U NRS=0.429
+ NRD=0.429 M=1
M24 VSCHMITT VC3 N_14 0 NCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M14 V1 ISETUP N_4 VIN PCH L=0.6UU W=8.8UU AS=14.08P AD=14.08P PS=20.8U
+ PD=20.8U NRS=0.068 NRD=0.068 M=1
M13 ISETUP ISETUP N_3 VIN PCH L=0.6UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M19 VREF ISETUP N_17 VIN PCH L=0.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M28 VSCHMITT VC3 N_18 VIN PCH L=.6UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M29 0 VSCHMITT N_18 VIN PCH L=.6UU W=1.8UU AS=2.88P AD=2.88P PS=6.8U PD=6.8U
+ NRS=0.333 NRD=0.333 M=1
M27 N_18 VC3 VIN VIN PCH L=.6UU W=1.4UU AS=2.24P AD=2.24P PS=6U PD=6U
+ NRS=0.429 NRD=0.429 M=1
```

```
R1 VREF N_19 RSICR 85K
RI38 N_19 0 RSICR 80K
CTRI VTRI 0 CP2P1 4P
C1 VIN ISETUP CP2P1 1P
C2 V1 V2 CP2P1 .1P
XU1 VC3 N_1 inv PARAMS:  WP=4.5 LP=0.6 WN=1.4 LN=0.6
XU2 N_1 N_2 inv PARAMS:  WP=4.5 LP=0.6 WN=1.4 LN=0.6
XU3 VSCHMITT VSW inv PARAMS:  WP=4.5 LP=0.6 WN=1.4 LN=0.6
XU4 VSCHMITT CLK inv PARAMS:  WP=4.5 LP=0.6 WN=1.4 LN=0.6
M20 V1 V1 N_5 0 MNNL L=.6UU W=5UU AS=8P AD=4P PS=13.2U PD=6.6U
M21 VTRI V1 N_6 0 MNNL L=.6UU W=5UU AS=8P AD=4P PS=13.2U PD=6.6U
M2 VC1 VREF N_8 N_8 MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M10 VTRI VSW V1 VIN MP L=.6UU W=4.5UU AS=7.2P AD=3.6P PS=12.2U PD=6.1U
M1 N_9 VTRI N_8 N_8 MP L=.6UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M18 N_17 ISETUP VIN VIN PCHNAT L=5UU W=10UU AS=16P AD=16P PS=23.2U PD=23.2U
+ NRS=0.06 NRD=0.06 M=1
M12 N_4 ISETUP VIN VIN PCHNAT L=5UU W=8.8UU AS=14.08P AD=14.08P PS=20.8U
+ PD=20.8U NRS=0.068 NRD=0.068 M=1
M11 N_3 ISETUP VIN VIN PCHNAT L=5UU W=5UU AS=8P AD=8P PS=13.2U PD=13.2U
+ NRS=0.12 NRD=0.12 M=1
M22 N_5 V1 V2 0 MNL L=5UU W=5UU AS=8P AD=4P PS=13.2U PD=6.6U M=1
M23 N_6 V1 V2 0 MNL L=5UU W=5UU AS=8P AD=4P PS=13.2U PD=6.6U M=1
M6 VC3 VC2 0 0 MNL L=1UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M5 VC2 VC1 0 0 MNL L=1UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M4 VC1 N_9 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M3 N_9 N_9 0 0 MNL L=.6UU W=10UU AS=16P AD=8P PS=23.2U PD=11.6U
M7 VREF N_2 N_19 0 MNL L=.6UU W=2.8UU AS=4.48P AD=2.24P PS=8.8U PD=4.4U M=1
M17 VC3 ISETUP VIN VIN MPN L=5UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M16 VC2 ISETUP VIN VIN MPN L=5UU W=20UU AS=32P AD=16P PS=43.2U PD=21.6U
M15 N_8 ISETUP VIN VIN MPN L=5UU W=40UU AS=64P AD=32P PS=83.2U PD=41.6U
R2 VIN N_11 RPOLY2 203.5
.ENDS triosc_500mv
```

```
***
.SUBCKT tri_bb2 IBB KILL4 PGND PVIN V_SS VC PVOUT SW1 SW2
MP2 IBB IBB $G_INTVCC $G_INTVCC PCH L=8UU W=20UU AS=32P AD=32P PS=43.2U
+ PD=43.2U NRS=0.03 NRD=0.03 M=1
MP6 N_11 IBB $G_INTVCC $G_INTVCC PCH L=8UU W=20UU AS=32P AD=32P PS=43.2U
+ PD=43.2U NRS=0.03 NRD=0.03 M=1
MI20 ILIMS IBB $G_INTVCC $G_INTVCC PCH L=8UU W=20UU AS=32P AD=32P PS=43.2U
+ PD=43.2U NRS=0.03 NRD=0.03 M=1
C1 IBB $G_INTVCC CP2P1 0.99856P
C3 N_11 0 CP2P1 0.98066P
MN2 N_11 N_11 0 0 NCH L=8UU W=20UU AS=32P AD=32P PS=43.2U PD=43.2U NRS=0.03
+ NRD=0.03 M=1
MN8 N_10 N_11 0 0 NCH L=8UU W=20UU AS=32P AD=32P PS=43.2U PD=43.2U NRS=0.03
+ NRD=0.03 M=1
MN6 N_9 N_11 0 0 NCH L=8UU W=20UU AS=32P AD=32P PS=43.2U PD=43.2U NRS=0.03
+ NRD=0.03 M=1
MN7 N_8 N_11 0 0 NCH L=8UU W=20UU AS=32P AD=32P PS=43.2U PD=43.2U NRS=0.03
+ NRD=0.03 M=1
XI10 AON_NEW CON_NEW KILL4 0 0 PGND PVIN PVOUT PVIN N_22 GATEA_B SW1 SW1REF
+ SW2 tri_output
XI13 N_8 VTRI VC $G_INTVCC AON_OLD tri_abcomp
XI12 N_9 VTRI VC $G_INTVCC CON_OLD tri_cdcomp
XI11 N_10 $G_INTVCC CLK VTRI triosc_500mv
XI19 N_22 0 GATEA_B ILIMS 0 0 SW1 SW1REF $G_INTVCC ILIM tri_ilim
XI18 AON_OLD CLK CON_OLD ILIM AON_NEW CON_NEW tri_ilimlogic
MI17 SW1REF V_SS N_20 0 NCHNAT L=.6UU W=7UU AS=11.2P AD=11.2P PS=17.2U
+ PD=17.2U NRS=0.086 NRD=0.086 M=1
MI16 N_20 N_19 N_21 0 NCHNAT L=3UU W=7UU AS=11.2P AD=11.2P PS=17.2U PD=17.2U
+ NRS=0.086 NRD=0.086 M=10
RLIM N_21 0 RSICR 80K
VI14 N_19 0 1.25
.ENDS tri_bb2
```

```
* Main network description
R2 FB 0 RP2RES 200K
R1 PVOUT FB RP2RES 340K
RI13 N_6 FB RP2RES 2.2K
R3 N_9 VC RP2RES 15K
VREF N_8 0 1.22
CFILTER1 $G_INTVCC 0 CP2P1 566.58P
C2 0 PVOUT CP2P1 22U
CI11 N_6 PVOUT CP2P1 220P
CI12 FB VC CP2P1 10P
C1 FB N_9 CP2P1 220P
RFILTER1 PVIN $G_INTVCC RPOLY2 37
IBIAS IBB IEA 2.5U
XI9 FB IEA KILL4 $G_INTVCC N_8 V_SS VC VCINT ea_whit
XI14 IBB KILL4 PGND PVIN V_SS VCINT PVOUT SW1 SW2 tri_bb2
MI16 PVOUT LOAD 0 0 NCH L=1UU W=375000UU AS=600000.009P AD=600000.009P
+ PS=750003.2U PD=750003.2U NRS=0 NRD=0 M=1
MI15 LOAD LOAD 0 0 NCH L=1UU W=375000UU AS=600000.009P AD=600000.009P
+ PS=750003.2U PD=750003.2U NRS=0 NRD=0 M=1
```

Appendix D

MATLAB .m Files

This appendix contains MATLAB .m files that were used to create plots contained in this thesis.

D.1 Figure 2-1 Source Code: pwm_graph.m

```
function D=pwm_graph(overlap, vmax)
%This program takes pwma, pwmd, overlap, and vmax to plot the conversion
%ratios.  The user inputs the overlap and vmax (say 1.2v) and the program
%grpahs the duty cycles over the correct range and does the division for
%the conversion ratio.
%This program only deals with the ideal case of perfect pwm waveforms.  To
%plot the conversion ratio for a set of data with Vc and duty cycle values
%simply plot PWMA, PWMD, and PWMA,PWMD, all versus Vc.  An explicit M-file
%is not required.
step=.0001;
pwma = [0:step:1]';
pwmd = [1:-step:0]';
offset=(1-overlap)*length(pwma);
vc=vmax/((length(pwma)+offset)*step)*[step:step:((length(pwma)+offset)*step)];
length(vc);
pwma_shift=[pwma;ones(offset,1)];
pwmd_shift=[ones(offset,1);pwmd];
```

```
D=pwma_shift./pwmd_shift;
for i=1:length(D)   %Limts range so y values don't go so high.
    if D(i)>4
        D(i)=4;
    end
end
plot(vc,pwma_shift,'k--')
hold on
plot(vc,pwmd_shift,'k:')
plot(vc,D,'k')
hold off
xlabel('Vc (V)')
title(overlap)
xlim([0 vmax])
legend('Location','NorthWest','PWM_A','PWM_D','D_c_o_n_v')
```

D.2 Figure 2-3 Source Code: rippleamp.m

```
function D=rippleamp(Dconv)
subplot(1,1,1)
hold off
for d=1:length(Dconv)
D=Dconv(d);
Vout=3.3;
Vin=Vout/D;
L=5e-6;
T=1e-6;
Iload = .5;
step=1e-9;
M_AD=(Vin-Vout)/L;
M_BD=-Vout/L;
t=[0:step:T];
```

```
tad = D*T;
tbd = T-tad;
Ioffset = Iload - 1/2*M_AD*tad;
for i=1:length(t)
     if t(i) < tad
          IL(i) = Ioffset + M_AD*t(i);
          Iout(i)=IL(i);
     else
          IL(i)=Ioffset + M_AD*tad + M_BD*(t(i)-tad);
          Iout(i)=IL(i);
     end
end
Vamp(d)= M_AD*tad;
Ploss(d) = mean(2*.1*IL.^2);
Pvout(d)=Iload*3.3;
VIN(d)=Vin;
end
subplot(1,3,3)
plot(Dconv,Vamp)
figure(2)
subplot(1,3,1)
plot(Dconv,Ploss*1000)
xlabel('D')
ylabel('Loss (mW)')
subplot(1,3,2)
plot(Dconv,Pvout./(Pvout+Ploss)*100)
xlabel('D')
ylabel('Efficiency (%)')
subplot(1,3,3)
plot(VIN,Pvout./(Pvout+Ploss)*100)
xlabel('V_i_n (volts)')
ylabel('Efficiency (%)')
```

D.3 Figure 2-4 Source Code: rippleampboost.m

```
function C=rippleampboost(Dconv)
figure(1)
subplot(1,1,1)
hold off
figure(2)
subplot(1,1,1)
hold off
for d=1:length(Dconv)
D=Dconv(d);
Vout=3.3;
Vin=Vout*D;
L=5e-6;
T=1e-6;
Iload = .5;
step=1e-9;
M_AD=(Vin-Vout)/L;
M_AC=Vin/L;
t=[0:step:T];
tad = D*T;
tac = T-tad;
Ioffset = Iload/D - 1/2*M_AD*tad;
for i=1:length(t)
    if t(i) < tad
        IL(i) = Ioffset + M_AD*t(i);
        Iout(i)=IL(i);
    else
        IL(i)=Ioffset + M_AD*tad + M_AC*(t(i)-tad);
        Iout(i)=0;
    end
end
```

```
figure(1)
subplot(1,3,1)
plot(t,IL)
hold on
subplot(1,3,2)
plot(t,2*.1*IL.^2,'r')
hold on
plot([0 1e-6],[mean(IL.^2) mean(IL.^2)])
Vamp(d)= M_AD*tad;
Ploss(d) = mean(2*.1*IL.^2);
Pvout(d)=Iload*3.3;
VIN(d)=Vin;
end
subplot(1,3,3)
plot(Dconv,-Vamp)
figure(2)
subplot(1,3,1)
plot(Dconv,Ploss*1000)
xlabel('D')
ylabel('Loss (mW)')
subplot(1,3,2)
plot(Dconv,Pvout./(Pvout+Ploss)*100)
xlabel('D')
ylabel('Efficiency (%)')
subplot(1,3,3)
plot(VIN,Pvout./(Pvout+Ploss)*100)
xlabel('V_i_n (volts)')
ylabel('Efficiency (%)')
C = [VIN; Ploss; Pvin; Pvout; Pvout./Pvin*100; Dconv];
```

D.4 Figures 2-7, 2-8, and 2-9 Source Code: I2R.m and inductorripple2.m

D.4.1 I2R.m

```
function [Pc_saw]=I2R(Vin, Vout, Rsw, L, Cgp, Cgn, overlap, Iload, plotdec);
%Calculates power loss and efficeincy given a sweep of input voltage
%Pc = Power loss through conduction (I^2R)
%Pg = Power loss from gate charge
%e = efficiency
%Rsw => on resistance of the FETS, all the same for now.
for j=1:length(overlap)
    for i=1:length(Vin)
        [IL_saw IL_tri Iout_saw Iout_tri t Pg(i,j)] =
        Inductorripple2(Vin(i), Vout, L, Cgp, Cgn, overlap(j), Iload);
        Pc_saw(i,j)=mean(IL_saw.^2*2*Rsw);
        e_saw(i,j) = 100*Vout*Iload/(Vout*Iload+Pc_saw(i,j)+Pg(i,j));
        Pc_tri(i,j)=mean(IL_tri.^2*2*Rsw);
        e_tri(i,j) = 100*Vout*Iload/(Vout*Iload+Pc_tri(i,j)+Pg(i,j));
        IL_tri_avg(i,j)=mean(IL_tri);
        IL_saw_avg(i,j)=mean(IL_saw);
    end
end
if plotdec == 1
    figure(1)
    subplot(2,2,1)
    plot(Vin, Pc_saw)
    title('Conduction loss')
    subplot(2,2,3)
    plot(Vin, Pc_tri)
    title('Conduction loss')
    subplot(2,2,2)
    plot(Vin, e_saw)
```

```
title('Efficiency')
subplot(2,2,4)
plot(Vin, e_tri)
title('Efficiency')
figure(2)
subplot(2,2,1)
plot(Vin, Pc_saw,'b')
hold on
plot(Vin, Pc_tri, 'r')
hold off
title('Conduction loss')
subplot(2,2,2)
plot(Vin, e_saw,'b')
hold on
plot(Vin, e_tri,'r')
hold off
title('Efficiency')
subplot(2,2,3)
plot(Vin,(e_tri-e_saw))
subplot(2,2,4)
ind=1:20:length(Vin);
%ind=29;
%Vin(ind)
plot(overlap,(e_tri(ind,:)-e_saw(ind,:)))
legend(num2str(Vin(ind)))
figure(3)
hold off
plot(Vin,(e_tri(:,1)-e_saw(:,1)),'k-.')
hold on
plot(Vin,(e_tri(:,2)-e_saw(:,2)),'k')
xlabel('V_i_n (V)')
ylabel('Efficiency_T_r_i-Efficiency_s_a_w (%)')
```

```
legend('15% Overlap','50% Overlap','location','NorthEast')
[Vin' e_tri-e_saw]
figure(4)
subplot(1,2,1)
plot(Vin, e_saw,'k')
hold on
H1=plot(Vin, e_saw,'k')
hold on
H2=plot(Vin, e_tri,'k:')
xlabel('V_i_n (V)')
ylabel('Efficiency (%)')
legend([H1(1,1) H2(1,1)],'Saw','Triangle','location','SouthEast')
hold off
subplot(1,2,2)
H1=plot(Vin, e_saw,'k')
hold on
H2=plot(Vin, e_tri,'k:')
xlabel('V_i_n (V)')
ylabel('Efficiency (%)')
legend([H1(1,1) H2(1,1)],'Saw','Triangle','location','SouthEast')
hold off
figure(5)
subplot(1,2,1)
hold off
H1=plot(Vin,IL_saw_avg,'k')
hold on
H2=plot(Vin,IL_tri_avg,'k:')
legend([H1(1,1) H2(1,1)],'Saw','Triangle','location','NorthEast')
xlabel('V_i_n (V)')
ylabel('I_L (A)')
xlim([0 8])
ylim([.48 1])
```

```
    subplot(1,2,2)
    hold off
    plot(Vin,1000*(IL_saw_avg(:,1)-IL_tri_avg(:,1)),'k-.')
    hold on
    plot(Vin,1000*(IL_saw_avg(:,2)-IL_tri_avg(:,2)),'k')
    legend('15% Overlap','50% Overlap','location','SouthEast')

    xlabel('V_i_n (V)')
    ylabel('I_L_s_a_w - I_L_t_r_i (mA)')
    xlim([1 8])
end
end
```

D.4.2 inductorripple2.m

```
function [IL_saw IL_tri Iout_saw Iout_tri t Pg] =
Inductorripple2(Vin, Vout, L, Cgp, Cgn, overlap, Iload);
%Inductor ripple for a sawtooth and triangle input
%New, cleaner version from Saw_Inductoripple.  Avoids getting conversion
%ratiowith other functions.
step=1e-9;
freq=1e6;
T=1e-6;
D=Vout/Vin;
Vmax=1.2;
Vbuck=Vmax*(1-overlap)/(2-overlap);
Vboost=Vmax/(2-overlap);
Tov = overlap*T;
M_AD=(Vin-Vout)/L;
M_AC=Vin/L;
M_BD=-Vout/L;
t=[0:step:T];
```

```
Dbuck=Vbuck/Vboost;
Dboost=Vboost/Vbuck;
if D < Dbuck
 tad=D*T;
 tbd=T-tad;
 Ioffset = Iload - 1/2*M_AD*tad;
 Pg = (Cgp + Cgn)*Vin^2*freq; %gate charge loss for swa and swb
 %which are charged by Vin
  for i=1:length(t)
   if t(i) < tad
    IL_saw(i) = Ioffset + M_AD*t(i);
    Iout_saw(i)=IL_saw(i);
    IL_tri=IL_saw;
    Iout_tri=Iout_saw;
     else
     IL_saw(i)=Ioffset + M_AD*tad + M_BD*(t(i)-tad);
     Iout_saw(i)=IL_saw(i);
     IL_tri=IL_saw;
     Iout_tri=Iout_saw;
     end
   end
else if D > Dboost
 tad=(1/D)*T;
 tac=T-tad;
 Ioffset=T/tad*Iload-(tad/2*M_AD);
 Pg = (Cgp*Vout^2 + Cgn*Vin^2)*freq;
 %gate charge loss for swc and swd which are
 %charged by Vin and Vout respectivly
 for i=1:length(t)
  if t(i)<tad
   IL_saw(i) = Ioffset + M_AD*t(i);
   Iout_saw(i)=IL_saw(i);
```

```
IL_tri=IL_saw;
Iout_tri=Iout_saw;
        else
            IL_saw(i)=Ioffset + M_AD*tad +M_AC*(t(i)-tad);
            Iout_saw(i)=0;
            IL_tri=IL_saw;
            Iout_tri=Iout_saw;
        end
    end
 else
    state=3;   %buck-boost mode
    Vc=D*(Vboost+Vbuck)/(1+D);
    tad=T-Tov;
    tac=(Vc-Vbuck)/Vboost*T;
    tbd=T-tad-tac;
    Ioffset=T/(T-tac)*(Iload - 1/(2*T)*(M_AD*tad^2 -M_BD*tbd^2));
    Pg = ((Cgp + 2*Cgn)*Vin^2 + Cgp*Vout^2)*freq;
    %gate charge loss for swa, swb, swc, and swd.  SWD is turned on
    %with Vout, the rest use Vin
    for i=1:length(t)
        if t(i)<tad
            IL_saw(i) = Ioffset + M_AD*t(i);
            Iout_saw(i)=IL_saw(i);
        else if t(i)<(tad+tac)
                IL_saw(i)=Ioffset + M_AD*tad + M_AC*(t(i)-tad);
                Iout_saw(i)=0;
            else
                IL_saw(i)=Ioffset + M_AD*tad + M_AC*tac +M_BD*(t(i)-tad-tac);
                Iout_saw(i)=IL_saw(i);
            end
        end
    end
```

```
        %tri buck boost mode
Ioffset = Iload/((tad +tbd)/T);
 Pg = ((Cgp + 2*Cgn)*Vin^2 + Cgp*Vout^2)*freq;
 %gate charge loss for swa, swb, swc, and swd.  SWD is turned on
 %with Vout, the rest use Vin
  for i=1:length(t)
   if t(i)<tac/2
    IL_tri(i) = Ioffset + M_AC*t(i);
    Iout_tri(i)=0;
     else if t(i)<(tac/2 + tad/2)
     IL_tri(i)=Ioffset + M_AC*tac/2 + M_AD*(t(i)-tac/2);
     Iout_tri(i)=IL_tri(i);
      else if t(i) < (tac/2 + tad/2 + tbd)
      IL_tri(i) = Ioffset + M_AC*tac/2
       + M_AD*tad/2 + M_BD*(t(i) - tac/2 - tad/2);
      Iout_tri(i) = IL_tri(i);
       else if t(i) < tac/2 +tad +tbd
       IL_tri(i) = Ioffset + M_BD*tbd/2
        + M_AD*(t(i)-tac/2 - tad/2 - tbd);
       Iout_tri(i) = IL_tri(i);
        else
        IL_tri(i) = Ioffset + M_BD*tbd/2
         + M_AD*tad/2 +M_AC*(t(i)-tac/2 - tad - tbd);
        Iout_tri(i) = 0;
        end
       end
      end
     end
    end
 end
```

D.5 Figure 2-10 Source Code: I2R_ivary.m

```
function [Pc Pg e]=I2R_Ivary2(Vin, Vout, Rsw, L, Cgp, Cgn, overlap, Iload);
%Calculates power loss and efficeincy given a sweep of input voltage
%Pc = Power loss through conduction (I^2R)
%Pg = Power loss from gate charge
%e = efficiency
%Rsw => on resistance of the FETS, all the same for now.
for j=1:length(overlap)
    for i=1:length(Iload)
        [IL_saw IL_tri Iout_saw Iout_tri t Pg(i,j)] =
        Inductorripple2(Vin, Vout, L, Cgp, Cgn, overlap(j), Iload(i));
        Pc_saw(i,j)=mean(IL_saw.^2*2*Rsw);
        e_saw(i,j) = 100*Vout*Iload(i)/(Vout*Iload(i)+Pc_saw(i,j)+Pg(i,j));
        Pc_tri(i,j)=mean(IL_tri.^2*2*Rsw);
        e_tri(i,j) = 100*Vout*Iload(i)/(Vout*Iload(i)+Pc_tri(i,j)+Pg(i,j));
        IL_tri_avg(i,j)=mean(IL_tri);
        IL_saw_avg(i,j)=mean(IL_saw);
    end
end
figure(1)
subplot(1,2,1)
hold off
H1=semilogx(Iload, e_saw,'k')
hold on
H2=semilogx(Iload, e_tri,'k:')
legend([H1(1,1) H2(1,1)],'Saw','Triangle','location','NorthWest')
ylabel('Efficiency (%)')
xlabel('I_o_u_t (A)')
xlim([1e-6 1e2])
subplot(1,2,2)
semilogx(Iload,(e_tri(:,2)-e_saw(:,2)),'k')
```

```
hold on
semilogx(Iload,(e_tri(:,1)-e_saw(:,1)),'k-.')
ylabel('\eta_T_r_i-\eta_S_a_w (%)')
xlabel('I_o_u_t (A)')
legend('Location','SouthEast', '50% Overlap','15% Overlap')
xlim([1e-6 1e2])
hold off
end
```

D.6 Figure 3-1 Source Code: RHPZ.m

```
function [Vinboost, D, D1, D2] = RHPZ(Vout,PercentOverlap);
%This program calculates the conversion ratio for a given Vc Voltage
%the conversion ratio is the same whether sawtooths or triangle waves are
%used.
Vc=[0:.0001:1.2];
Vmax=1.2;
Vbuck=Vmax*(1-PercentOverlap)/(2-PercentOverlap);
Vboost=Vmax/(2-PercentOverlap);
Vtri=Vboost;
VBB=Vboost-Vbuck;
Vbuckreal = Vout/(Vbuck/Vtri);
Vboostreal = Vout/(1/(1-(Vtri-Vbuck)/Vtri));
i=0;
k=0;
for j = 1:length(Vc)
    if Vc(j)<Vbuck
        D(j)=Vc(j)/Vtri;
        D1(j)=D(j);
        D2(j)=0;
    else if Vc(j)>Vboost
            i=i+1;
```

```
            D(j)=1/(1-(Vc(j)-Vbuck)/Vtri);
            D1(j)=1;
            D2(j)=(Vc(j)-Vbuck)/Vtri;
            Vinboost(i) = Vout/D(j);
        else
            k=k+1;
            D(j)=Vc(j)/(Vtri-Vc(j)+Vbuck);
            D1(j)=Vc(j)/Vtri;
            D2(j)=(Vc(j)-Vbuck)/Vtri;
            Vinbb(k) = Vout/D(j);
            D1bb(k)=D1(j);
            D2bb(k)=D2(j);
        end
    end
    Vin(j)=Vout/D(j);
end
D2p=ones(1,length(D2))-D2;
D2bbp=ones(1,length(D2bb))-D2bb;
plot(Vinboost, Vinboost.^2,'k')
hold on
plot(Vinbb, Vinbb.^2.*(D2bbp.*D1bb+D1bb.^2),'k')
plot([Vboostreal Vboostreal+.000001], [0 40],'k')
plot([Vbuckreal Vbuckreal+.000001], [0 40],'k')
legend('Location', 'Northwest', 'Boost Zero','Buck-boost Zero')
ylim([0 40])
xlabel('Vin (volts)')
ylabel('Normalized RHP Zero Location')
title(['Overlap = ' num2str(PercentOverlap*100) '%'])
hold off
end
```

D.7 Figures 3-2 and 3-6 Source Code: tri_comp_types.m

```
function [comp]=tri_comp_types(Vin,overlap,Iload,gain,wz,wp,wz3,wp3)
s=tf('s')
R1=340e3;
Vosc=.5;
R2=R1*gain;
C2=(wz*R2)^-1;
%C1=1/9*C2;
C1=C2*wz/wp/(1-wz/wp);
R3=R1/(wp3/wz3-1);
C3=1/(R3*wp3);
Vo=3.3;
L=10e-6;
C=22e-6;
R=Vo/Iload;
Resr=.01;
Vtri=.5;
D=Vo/Vin;
Vmax=1.2;
Vbuck=Vmax*(1-overlap)/(2-overlap);
Vboost=Vmax/(2-overlap);
Dbuck=Vbuck/Vboost;
Dboost=Vboost/Vbuck;
Vinbuck=Vo/Dbuck;
Vinboost=Vo/Dboost;
HI=1/(s*R1*C1);
HII=1/R1*(1+s*R2*C2)/(s*(C1+C2+s*R2*C1*C2));
HIII=1/R1*(1+s*R2*C2)*(1+s*C3*(R1+R3))/(s*(C1+C2+s*R2*C1*C2)*(1+s*C3*R3));
if D < Dbuck    %Buck
    Da=D;
    Hbuck=Vin/Vosc*Vin*(1+Resr*C*s)/
```

```
    (s^2*L*C*(1+Resr/R)+(L/R+Resr*C)*s+1);
    figure(7)
    subplot(1,3,1)
    margin(Hbuck)
    LIbuck=HI*Hbuck;
    LIIbuck=HII*Hbuck;
    LIIIbuck=HIII*Hbuck;
    figure(1)
    subplot(1,3,1)
    margin(LIbuck)
    figure(2)
    subplot(1,3,1)
    margin(LIIbuck)
    figure(3)
    subplot(1,3,1)
    margin(LIIIbuck)
else if D > Dboost      %Boost
        Dc=1-1/D;
        Dcp=1-Dc;
        IL=Iload/Dcp;
        Hboost=Vin/Vosc*(Dcp*Vo-s*L*IL)*(1+s*Resr*C)/
        (L*C*(1+Dcp*Resr/R)
        *s^2+(L*Dc/(Resr+R) +Dcp*L/R + Dcp^2*Resr*C)*s+Dcp^2);
        figure(7)
        subplot(1,3,3)
        margin(Hboost)
        LIboost=HI*Hboost;
        LIIboost=HII*Hboost;
        LIIIboost=HIII*Hboost;
        figure(1)
        subplot(1,3,3)
        margin(LIboost)
```

```
        figure(2)
        subplot(1,3,3)
        margin(LIIboost)
        figure(3)
        subplot(1,3,3)
        margin(LIIIboost)
    else      %Buck-Boost
        Vc=D*(Vboost+Vbuck)/(1+D);
        Da=Vc/Vboost;
        Dc=(Vc-Vbuck)/Vboost;
        Dcp=1-Dc;
        IL=Iload/Dcp;
        Hbb=Vin/Vosc*(Dcp*(Vin+Vo)-s*L*IL)*(1+s*Resr*C)/
        (L*C*(1+Dcp*Resr/R)*s^2
        +(L*Dc/(Resr+R) +Dcp*L/R + Dcp^2*Resr*C)*s+Dcp^2);
        figure(7)
        subplot(1,3,2)
        margin(Hbb)
        LIbb=HI*Hbb;
        LIIbb=HII*Hbb;
        LIIIbb=HIII*Hbb;
        figure(1)
        subplot(1,3,2)
        margin(LIbb)
        figure(2)
        subplot(1,3,2)
        margin(LIIbb)
        figure(3)
        subplot(1,3,2)
        margin(LIIIbb)
        end
end
```

```
figure(8)
margin(HII)
figure(9)
margin(HIII)
```

D.8 Figure 3-8 Source Code: tri_comp_types_pm_val.m

```
function [comp]=tri_comp_types_pm_val(Vin,Iload,overlap,C1,C2,R2,C3,R3)
s=tf('s')
R1=340e3;
Rf=200e3;
Vosc=.5;
HI=1/(s*R1*C1);
HII=1/R1*(1+s*R2*C2)/(s*(C1+C2+s*R2*C1*C2));
HIII=1/R1*(1+s*R2*C2)*(1+s*C3*(R1+R3))/(s*(C1+C2+s*R2*C1*C2)*(1+s*C3*R3));
for j=1:length(Iload)
    for i=1:length(Vin)
        Vo=3.3;
        L=10e-6;
        C=22e-6;
        R=Vo/Iload(j);
        Resr=.01;
        Vtri=.5;
        D=Vo/Vin(i);
        Vmax=1.2;
        Vbuck=Vmax*(1-overlap)/(2-overlap);
        Vboost=Vmax/(2-overlap);
        Dbuck=Vbuck/Vboost;
        Dboost=Vboost/Vbuck;
        Vinbuck=Vo/Dbuck;
        Vinboost=Vo/Dboost;
        Vinbuck;
```

```
Vinboost;
if D < Dbuck    %Buck
    Da=D;
    Hbuck=Vin(i)/Vosc*Vin(i)*(1+Resr*C*s)/(s^2*L*C*(1+Resr/R)+(L/R+Resr*C)*s+1);
    %figure(7)
    %subplot(1,3,1)
    %margin(Hbuck)
    LIbuck=HI*Hbuck;
    LIIbuck=HII*Hbuck;
    LIIIbuck=HIII*Hbuck;
    [gm(i,j), pm(i,j), wg(i,j), wcp(i,j)]=margin(LIIIbuck);
else if D > Dboost      %Boost
        Dc=1-1/D;
        Dcp=1-Dc;
        IL=Iload(j)/Dcp;
        Hboost=Vin(i)/Vosc*(Dcp*Vo-s*L*IL)*(1+s*Resr*C)/(L*C*(1+Dcp*Resr/R)
        *s^2+(L*Dc/(Resr+R) +Dcp*L/R + Dcp^2*Resr*C)*s+Dcp^2);
        %figure(7)
        %subplot(1,3,3)
        %margin(Hboost)
        LIboost=HI*Hboost;
        LIIboost=HII*Hboost;
        LIIIboost=HIII*Hboost;
        [gm(i,j), pm(i,j), wg(i,j), wcp(i,j)]=margin(LIIIboost);
        else      %Buck-Boost
        Vc=D*(Vboost+Vbuck)/(1+D);
        Da=Vc/Vboost;
        Dc=(Vc-Vbuck)/Vboost;
        Dcp=1-Dc;
        IL=Iload(j)/Dcp;
        Hbb=Vin(i)/Vosc*(Dcp*(Vin(i)+Vo)-s*L*IL)*(1+s*Resr*C)/(L*C*(1+Dcp*Resr/R)*s
        +(L*Dc/(Resr+R) +Dcp*L/R + Dcp^2*Resr*C)*s+Dcp^2);
```

```
                %figure(7)
                %subplot(1,3,2)
                %margin(Hbb)
                LIbb=HI*Hbb;
                LIIbb=HII*Hbb;
                LIIIbb=HIII*Hbb;
                [gm(i,j), pm(i,j), wg(i,j), wcp(i,j)]=margin(LIIIbb);
            end
        end
    end
end
figure(8)
margin(HII)
figure(9)
margin(HIII)
figure(10)
subplot(2,2,1)
plot(Vin,gm)
title('gm')
subplot(2,2,2)
plot(Vin,pm)
title('pm')
subplot(2,2,3)
plot(Vin,wg)
title('wg')
subplot(2,2,4)
plot(Vin,wcp)
title('wp')
figure(13)
subplot(1,2,1)
plot(Vin,pm,'k')
xlabel('V_i_n')
```

```
ylabel('Phase Margin (degrees)')
subplot(1,2,2)
plot(Vin,wcp/(2*pi),'k')
xlabel('V_i_n')
ylabel('Crossover Frequency (Hz)')
[Vin' pm]
[Vin' wcp]
```

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