

Commercialization of Germanium Based
Nanocrystal Memory

by

Kian Chiew Seow

B.Eng., (Electrical Engineering)
National University of Singapore, 2006

SUBMITTED TO THE DEPARTMENT OF MATERIALS SCIENCE AND
ENGINEERING
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF
MASTER OF ENGINEERING IN MATERIALS SCIENCE AND ENGINEERING

AT THE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

SEPTEMBER 2007

© 2007 Massachusetts Institute of Technology
All rights reserved

Signature of
Author:.....

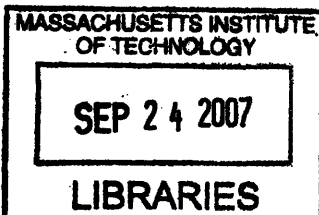
Department of Materials Science and Engineering
July 23, 2007

Certified
by:.....

Carl V. Thompson
Stavros Salapatas Professor of Materials Science and Engineering
Thesis Supervisor

Accepted
by:.....

Samuel M. Allen
POSCO Professor of Physical Metallurgy
Chair, Departmental Committee on Graduate Students



ARCHIVES

**Commercialization of Germanium Based
Nanocrystal Memory**

By

Kian Chiew Seow

**Submitted to the Department of Material Science and Engineering
On August 1, 2007 in Partial Fulfillment of the
Requirements of the Degree of Master of Engineering in
Material Science and Engineering**

ABSTRACT

This thesis explores the commercialization of germanium-based nanocrystal memories. Demand for smaller and faster electronics and embedded systems supports the development of high-density, low-power non-volatile electronic memory devices. Flash memory cells designed for ten years of data retention require the use of a thick tunneling oxide. This compromises writing and reading speed as well as endurance. A smaller device size can be achieved and speed can be improved by decreasing the oxide thickness. However, significant charge leakage will occur if the oxide is too thin, which will reduce the data retention time dramatically. This imposes a limit to the amount by which the oxide thickness can be decreased in conventional devices. Research has shown that by incorporating nanocrystals in the tunnel oxide, charge traps are created which reduce charge leakage and improve endurance through charge-storage redundancy. By replacing the conventional floating gate memory with one using Si or Ge nanocrystals, the nonvolatile memory exhibits high programming speed with low programming voltage and superior retention time, and yet is compatible with conventional silicon technology.

This thesis provides an analysis of competing technologies, an intellectual property analysis, costs modeling as well as ways to improve nanocrystal memories in order to compete with other forms of emerging technologies to replace conventional Flash memories.

Thesis Supervisor: Carl V. Thompson

Title: Stavros Salapatas Professor of Materials Science and Engineering

REPRODUCED

ACKNOWLEDGEMENTS

This thesis would not have materialized with the help, guidance and support of many people. First and foremost, I would like to thank Prof. Carl Thompson from the Massachusetts Institute of Technology (MIT) and Prof. Choi Wee Kiong from the National University of Singapore (NUS) for their guidance. I would also like to thank Prof Chim Wai Kim from NUS for lending me literature pertaining to nanocrystal memories.

I would also like to thank Dr. Vincent Ho and Mr Chin Khee Yeap from the semiconductor industry for providing me with estimated figures for the costs models.

The administrative officers from the Singapore-MIT alliance (SMA) office as well as the Department of Material Science and Engineering (DMSE) Office are also a great help. Special thanks to Ms Jocelyn Sales and Ms Juliana Chai for their assistance and help rendered throughout my entire course of studies.

In addition, I would also like to thank Roy, Zhengfei, Hongpeng and Zhihao from the Microelectronics Lab in the National University of Singapore for the time spent with me in discussing technical aspects pertaining to nanocrystal memories.

This thesis would also not be possible without the support of my fellow coursemates from the Singapore-MIT alliance program and the Massachusetts Institute of Technology, my housemates as well as my friends.

I would like to thank my family for having stood by me for all 26 years of my life. Last but not least, I would like to give my warmest thanks to professors in MIT and NUS who have taught me, and anyone who is not mentioned here but has helped me in one way or another.

Contents

1. Introduction	
1.1 History of Non-volatile Memory Structures	10
1.2 Working Principles of Conventional Flash Memory	13
1.3 Current and Future Non-volatile Memories	16
1.4 Nanocrystal Memory	22
Chapter 1 References	23
2. Nanocrystal Memory	
2.1 Nanocrystal Memory Device	27
2.2 Synthesis of Germanium Nanocrystals	30
2.3 Characterization of Nanocrystals	33
2.4 Charge Storage in Nanocrystal Memory Devices	34
2.5 Optimum Nanocrystal Size	43
2.6 Comparison of Different Nanocrystal Memory	48
2.7 Hetero-nanocrystal Memory	50
2.8 Comparison between NC Memory and other Flash Replacement Technologies	57
2.9 Multi-bit Schemes	62
Chapter 2 References	62

3. Market and Intellectual Property Analysis	
3.1 Market Overview	75
3.2 Market Growth	79
3.3 Competitors	83
3.4 Intellectual Property	84
3.5 Market and Intellectual Property Analysis Conclusion	86
Chapter 3 References	86
4. Cost Modeling	
4.1 Chip Industry Trends	90
4.2 Cost Model of Building a Fabrication Plant	94
4.3 Cost Modeling Conclusions	96
Chapter 4 References	97
5. Conclusions	
	99

List of Figures

Figure 1.1: Schematic of a Floating Gate Device	12
Figure 1.2: (Top) NOR Flash Memory and Wiring on Silicon. (Bottom) NAND Flash Memory and Wiring on Silicon.	15
Figure 1.3: (Left) Schematic Comparison between a Floating Gate Structure and a SONOS Structure (Right) A Transmission Electron Microscopy (TEM) Image of the SONOS Structure	18
Figure 1.4: Schematic of Phase Change Memory	20
Figure 1.5: A MRAM Cell During Read (Above) and Write (Below) Operations	22
Figure 2.1: Schematic of Silicon Nanocrystal Based Memory	28
Figure 2.2: Memory module size for both conventional floating gate NVM and nanocrystal based NVM showing approximate factor of two reduction for nanocrystal b Figure 2.3: Schematic illustration of the density of supercritical particles as a function of time after quenching based NVM	30
Figure 3.2: Schematic illustration of the density of supercritical particles as a function of time after quenching	31
Figure 2.4: C–V hysteresis loops for various annealed MOS capacitors. The inset is a schematic of the MOS memory structure based on silicon nanocrystals	35
Figure 2.5: Long-term charge retention characteristics in various annealed MOS capacitors, measured using the constant-capacitance method at the flat-band point	36
Figure 2.6: Energy band diagram of the MOS memory structure at flat-band condition for electron tunneling processes in the retention mode after injecting electrons	37
Figure 2.7: Drain current (I_{DS}) transient at a read voltage of 5V after a write operation at 15V for 20s.	40
Figure 2.8: Inverse of discharging time constant ($1/\tau_D$) divided by the square of the temperature plotted against the inverse of T.	41
Figure 2.9: Trap energy level required for 10 year charge retention performance vs nanocrystal diameter.	42

Figure 2.10: Retention characteristics at various tunnel oxide thicknesses and the Ge nanocrystal size on device performance	45
Figure 2.11: Plot of threshold voltage shifts ΔV_T and retention period τ_r as a function of tunnel oxide thickness	45
Figure 2.12: Nucleation curve of nanocrystal deposited by CVD on SiO ₂ showing the evolution of nanocrystal density and size with deposition time.	47
Figure 2.13: Ordered Array of Nanocrystals	48
Figure 2.14: (Left) The schematic cross sectional of Ge/Si heteronanocrystal memory half cell. (Right) The valence band diagram for (a) hole writing (b) retention and (c) erasing.	51
Fig 2.15: Fabrication of ordered nanocrystal array using porous alumina using a two step anodization process. The first anodization serves as a template for ordered hole formation in the second anodization.	52
Fig 2.16: Formation of heteronanocrystals using porous alumina.	53
Figure 2.17: High magnification view of Ge nanodot array fabricated using alumina membrane.	54
Figure 2.18: Ordered formation of silicon nanocrystals using diblock copolymers	55
Figure 2.19: Schematic for formation of vertical blocks of polystyrene.	55
Figure 2.20: Interfacial energies γ_{sf} and γ_{mf} as a function of f . $\gamma_{sf} = \gamma_{mf}$ at $f \sim 0.6$ (0.6 styrene and 0.4 PMMA).	56
Figure 2.21: Atomic force microscopic phase images. Images are from thin films of P(S-b-MMA) symmetric diblock copolymer with a random copolymer anchored either a) to the substrate only or b) to the substrate and air surface. Insets indicate the orientation of the lamellar morphology.	57
Figure 2.22: Cell Sizes of Different Memory Technology Nodes in the ITRS	58
Figure 2.23: Schematic of double gate nanocrystal memories with ultrathin body structure	62
Figure 2.24: Energy band diagram in retention just after a write pulse	62
Figure 2.25: Schematic on the use of discrete traps for charge storage to realise a dual bit memory cell	63
Figure 2.26: Difference of threshold voltage between the read with drain and with source after programming by channel hot electron with high drain bias	64
Figure 2.27: Two and three layer schematics of multilevel nanocrystal	65

memories.	
Figure 2.28: The dependence of the memory window on programming voltage. There are three apparent stages observed for the three layer samples, and two stages for the layer samples	65
Figure 3.1: Some Applications for NAND Flash	77
Figure 3.2: (Top) Breakdown of global sales of flash memory in 2004 (Bottom) Projected global sales in 2010.	78
Figure 3.3: Projection of unit shipments of mobile electronic products with flash memory.	79
Figure 3.4: Projection of price of a 1 GB thumbdrive	80
Figure 3.5: Price-weighted index comprised of the average retail price of 1GB Universal Serial Bus (USB) Flash Memory. The index is normalized to a base value of 100 as of October 1, 2005. The price index shows a 40% drop for a period of 1 year and a 65% drop for a period of 18 months	81 .
Figure 3.6: Price per megabyte of hard disk drives, dynamic random access memory, flash	82
Figure 4.1: Capital costs and normalized cost per unit output over the years	91
Figure 4.2: Exposure system costs trend	91
Figure 4.3: Wafer cost breakdown for a 300mm logic wafer. Much of the costs come from depreciation of building and equipment costs, followed by costs of raw materials and other consumables	92
Figure 4.4: Average cost curve of a typical Flash manufacturer.	93
Figure 4.5: Simulated cost curves for plant with annual production of 360,000.	95
Figure 4.6: Simulated Breakdown of costs for a plant with capacity and annual production of 360,000 wafer per annum	96

List of Tables

Table 2.1 Mask adders required to integrate nanocrystal based non volatile memory into a standard CMOS flow compared against conventional non volatile memory	29
Table 2.2: Different Types of Memory Technologies	59
Table 3.1: Major memory technologies and companies with research on	83
Table 3.2: Selected patents relevant to fabrication of nanocrystal based memory devices	84
Table 4.1: 2005 Rankings Top Suppliers of Flash Memories	94
Table 4.2: Parameters used in cost analysis	94

Chapter 1: Introduction

Demand for smaller and faster electronics and embedded systems supports the development of high-density, low-power non-volatile electronics. Flash memory cells designed for ten years of data retention require the use of a thick tunneling oxide. This compromises writing and reading speed as well as endurance.

A smaller device size can be achieved and speed can be improved by decreasing the oxide thickness. However, significant charge leakage will occur if the oxide is too thin and this reduces the data retention time dramatically. This imposes a limit to the amount by which the oxide thickness can be decreased in conventional devices.

Research has shown that by incorporating nanocrystals in the tunnel oxide, charge traps are created which reduce charge leakage. By replacing the conventional floating gate memory with one using Si or Ge nanocrystals, the nonvolatile memory exhibits high programming speed with low programming voltage, superior retention time and yet is compatible with conventional silicon technology.

In addition, nanocrystal based memories are also more resistant to defects in the tunnel oxide. In conventional Flash cells, when there is a defect in the tunnel oxide, charges stored in the floating gate will leak away, rendering the cell unusable. However,

for nanocrystal memories, a defect in the tunnel oxide will only affect the charges stored in neighboring nanocrystals. As a result, nanocrystal based memories would normally be able to function properly as long as the defect remains small and isolated.

1.1 History of Non-volatile Memory Structures

Memory can be classified as two main types: volatile and non-volatile. Volatile memory loses its data after the supply current is turned off. Examples of this type of memory include static random access memory (SRAM) and dynamic random access memory (DRAM). Non-volatile memory retains its data even when it is not powered. The main types of non-volatile memory include Electrically Erasable Programmable Read Only Memory (EEPROM,) Erasable Programmable Read Only Memory (EPROM) and Flash (also called Flash EEPROM).

Kahng and Sze proposed the first non-volatile floating gate memory in 1967. A conventional Metal Oxide Semiconductor Field Effect Transistor was modified to include an embedded metal floating gate as illustrated in Fig 1.1. The floating gate device looks like an n-channel Metal Oxide Semiconductor Field Effect Transistor (MOSFET) except that it has two gates: the floating gate and the control gate. The floating gate is able to store charges that were injected from the substrate through the thin tunneling oxide. The storage of charges changes the threshold voltage of the MOSFET and allows logic '0' and '1' to be represented.¹

A schematic of a floating gate device is as illustrated below:

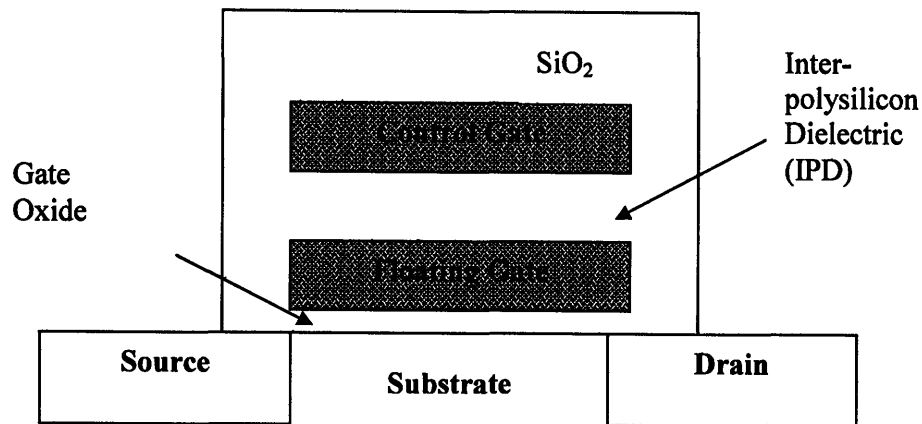


Figure 1.1. Schematic of a Floating Gate Device

In this type of memory, electrons are transferred from the substrate to the floating gate by tunneling through the thin layer of silicon dioxide. Storage of charges in the floating gate can be adjusted between high and low levels to represent '1' and '0'. The charges are retained even when the power is switched off.

In 1970, Frohman-Bentchkowsky demonstrated a floating polysilicon gate. The electrons were injected through a thick gate oxide to the floating silicon gate and removed using ultraviolet (UV) irradiation. This was also known as Electrically Programmable Read Only Memory (EPROM).

In 1980, an Electrical Erasable Programmable Read-Only Memory (EEPROM) utilizing tunneling write/erase was developed by Intel. The Floating Gate Tunneling Oxide (FLOTOX) technology proposed by Intel utilizes two transistors (a select transistor and a memory transistor) to achieve selective bit programming through Fowler-Nordheim (FN) tunneling. The select gate transistor is used to select or deselect floating gate transistors for programming or erasing. The die size was further increased to include error correction/redundancy circuitry, making them much larger than EPROMs.²

A single transistor EEPROM cell combining hot electron programming and FN tunneling erase was introduced in the 1980s. This new generation of EEPROMs does not have the select transistor and could only be erased by resetting the devices on the entire chip or a large portion of the chip. This generally sets all bits in the block to 1. Starting with a freshly erased block, any location within that block can be programmed. However, once a bit has been set to 0, only by erasing the entire block can it be changed back to 1. This chip is known as the Flash EEPROM. A smaller cell size can be achieved compared to the normal EEPROM. This can be further scaled down by using a thinner gate dielectric. However, if the gate oxide gets too thin, there will be current leakage problems, causing data retention issues. This limits the scalability of the minimum dimension of the memory cell.³⁻⁵

1.2 Working Principles of Conventional Flash Memory

Conventional state of the art Flash memory stores information in floating gates transistors similar to that illustrated in Figure 1. Traditionally, each transistor or cell holds one bit. However, newer Flash systems can hold multiple bits and are called multi level cell devices. As mentioned earlier, information is stored inside the floating gate by trapped electrons.

In a NOR flash cell, the floating gate is programmed by placing a large voltage at the control gate. Electrons are sucked up and deposited at the floating gate via a process called hot electron injection (HEI). In order to erase, a large negative voltage is supplied at the gate and the electrons tunnel out by Fowler-Nordheim (FN) Tunneling. The high voltage required is generated using an on chip charge pump. Most modern NOR flash memory components are divided into erase segments, usually called either blocks or sectors. All of the memory cells in a block must be erased at the same time. NOR programming, however, can generally be performed one byte or word at a time. On the other hand, NAND flash memory uses tunnel injection for writing and tunnel release for erasing.

In NOR cells, the source or drain of the transistors are connected to a single bitline in parallel. In NAND cells, the memory cells are connected from a single bitline in series. This is as illustrated in Figure 1.2. The wordline, connected to the control and floating gate, is stacked above the silicon substrate. Adjacent transistors share the same source/drain.

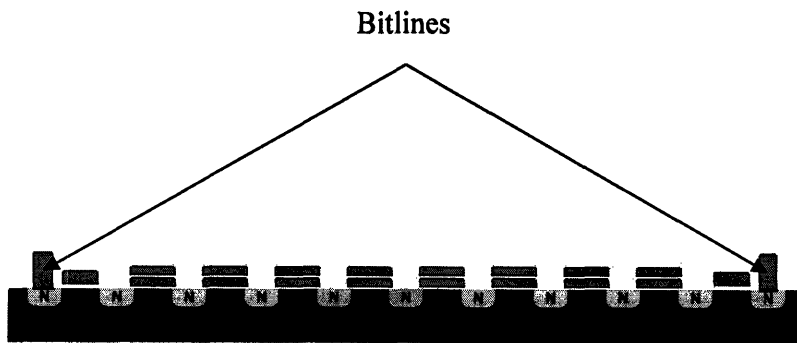
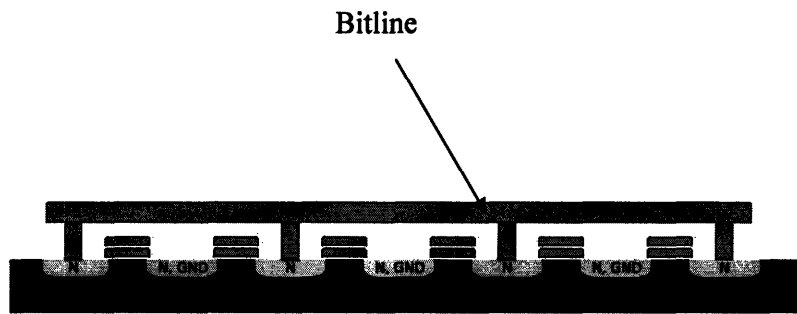


Figure 1.2: (Top) NOR Flash Memory and Wiring on Silicon. (Bottom) NAND Flash Memory and Wiring on Silicon.⁶

The parallel configuration of NOR Flash enables random access of data, enabling fast read speed. Hence, NOR flash is ideal for applications which are frequent read-only or perform-read operations such as code storage. NAND Flash enjoys higher cell density for a given technology node. This translates to smaller chip size, lower cost-per-bit and faster write/erase speed through programming blocks of data. Hence, NAND is ideal for applications such as data storage which requires low cost, small size and which rewrites data frequently.⁷⁻⁹

1.3 Current and Future Non-volatile Memories

Flash memory is the dominant form of non-volatile memory in the market. In recent years, there has been a drastic increase in demand for portable electronic devices such as cellular phones, digital cameras and thumb drives. In addition, new markets for flash memories are emerging. As prices fall, Flash memories are now able to compete with magnetic and optical storage media, especially in areas where users are willing to pay a premium for speed and performance¹⁰⁻¹⁵. Both developments contribute to skyrocketing demand for Flash Memory.

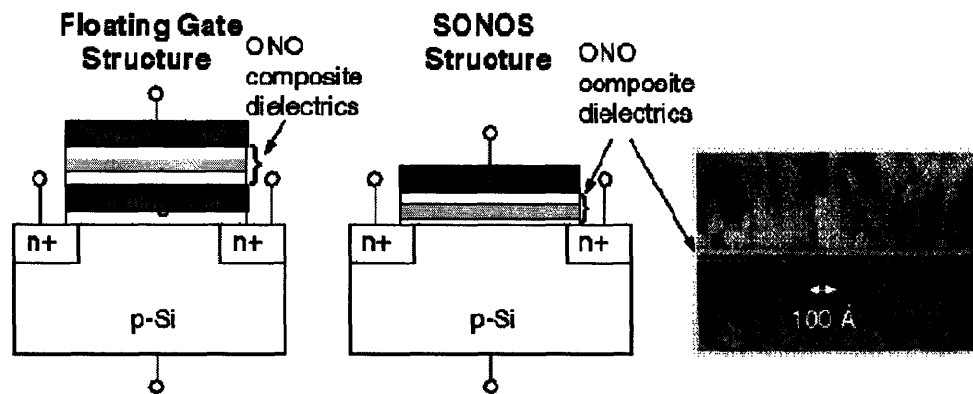
Great efforts have been carried out to make Flash memory cells smaller and more portable and at the same time faster and with lower power consumption. However, there is a limit to which cell size can be scaled down. Current flash memory technology is expected to be replaced or undergo some radical changes in the not-so-distant future¹⁶⁻¹⁸. There has been intense research interest into the various options available and various

new technologies have been mooted as potential successors to conventional Flash technology. The major forerunners include Silicon Oxide Nitride Oxide Semiconductor (SONOS), Ferro-electric Random Access Memory (FRAM), Magnetic Random Access Memory (MRAM) and phase change memory (PCRAM). Predictions of their attributes have been listed in the International Technology Roadmap for Semiconductors (ITRS)¹⁹. They are touted to be potential successors to conventional memory. A brief description of their working principles is given below while a more in depth comparison between them and nanocrystal based memories will be given in Chapter 2.

1.3.1 Silicon Oxide Nitride Oxide Semiconductor (SONOS)

Silicon Oxide Nitride Oxide Semiconductor (SONOS) "cells" consist of a standard n-channel MOS transistor with additional layers of insulators on the gate. These include the oxide layer (~2 nm), a silicon nitride layer (~5 nm), and a second oxide layer (5-10nm). SONOS is similar to Flash Memory. However, it relies on the charge trapping mechanism in which electrons are trapped in the nitride layer. SONOS offers a lower power usage, improved cycling endurance, reduction in process complexity and elimination of drain-induced turn-on. The SONOS memory device is more scalable than the floating gate flash memory since the equivalent oxide thickness (EOT) of the gate stack is thinner in the SONOS memory than in the floating gate memory.²¹ Moreover, current manufacturing processes are simpler compared to flash manufacturing process as they only require four additional non-critical masking steps over the basic logic processes (flash floating gate requires eleven additional processes).²² Also, the trapped nitrides do

not leak away easily and hence SONOS is more radiation hard than conventional Flash whose thin tunneling oxide is easily damaged by large ionizing doses, leading to charge leakage.²³



*Figure 1.3: (Left) Schematic Comparison between a Floating Gate Structure and a SONOS Structure (Right) A Transmission Electron Microscopy (TEM) Image of the SONOS Structure.*²⁰

1.3.2 Ferroelectric Random Access Memory (FeRAM)

A ferroelectric memory cell consists of a ferroelectric capacitor and a MOS transistor. It is similar to the storage cell of a DRAM. However, the material between the capacitor's electrodes has a high dielectric constant and can be polarized by an electric field. When an external electric field is applied across a dielectric, the dipoles tend to align themselves with the field direction, as a result of small shifts in the positions of atoms and shifts in the distributions of electronic charge in the crystal structure. This type of material is known as a ferroelectric material. Contrary to its name, this type of material does not necessarily have to contain iron. The polarization remains even when the electric

field is removed and remains until it gets reversed by an opposite electrical field. This makes the memory non-volatile. The polarity and quality of stored data is dependent on the direction and strength of the remnant polarization after the electric field is removed. Ferroelectric memories can be written much faster than EEPROMs and operating voltages are relatively small. FeRAM is also radiation hard.¹⁸ Today's FRAM uses lead zirconate titanate (PZT); other materials are being considered. The main developer of FRAM is Ramtron International. The main drawback of FRAM is incorporating ferroelectric materials into current silicon manufacturing processes.²⁴ The International Technology Roadmap for Semiconductors (ITRS) also highlighted that continued scaling of the stack capacitor would be challenging and FRAM production is sensitive to processing conditions and temperatures.¹⁹

1.3.2 Phase Change Random Access Memory (PCRAM)

Phase Change Memory (PCRAM) comprises of a transistor and a resistor made from chalcogenide material alloys (eg. $\text{Ge}_2\text{Sb}_2\text{Te}_5$) commonly used in rewritable compact disks. Electrical charges are used to convert the phase of the material from crystalline, which is conductive, to amorphous, which is resistive, vice versa. This is accomplished through Joule heating. In this way, the resistance state of the material can be used to represent logic '0' and '1'. Multi-state operations can also be achieved by programming the cell to intermediate values. The energy required for phase transformation also decreases with cell size, encouraging memory scaling. Erasable thermal phase change recording at a storage density of 3.3Tb inch^{-2} has been shown and Samsung has produced

a working prototype of PCRAM that is comparable to the size of NOR Flash²⁵⁻²⁶. Issues include reducing the reset current as cell size scales while maintaining writing capability and reducing thermal cross-talk at higher densities^{18,28}.

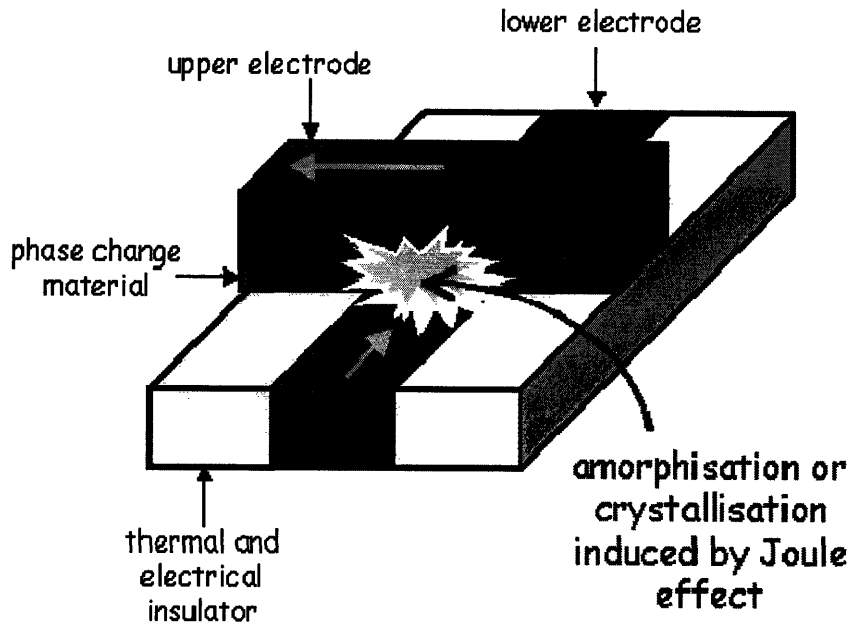


Figure 1.4. Schematic of Phase Change Memory⁵⁴

1.3.4 Magnetic Random Access Memory (MRAM)

In Magnetic Random Access Memory, the information is stored as the magnetization direction of ferromagnetic elements. In MRAM, the elements are formed from two ferromagnetic plates, each of which can hold a magnetic field, separated by a thin insulating layer. It utilizes the tunneling magnetoresistive (TMR) effect. The tunneling energy for electrons that are spin-aligned with both magnetic layers is less than that for electrons that are spin-aligned with only one layer. When the orientation of

both magnetic layers is the same, spin-aligned electrons have a higher probability of tunneling through the insulating layer. When the magnetic orientations of the layers are opposed, the tunneling probability of both spin-up and spin-down electrons is reduced. Due to the magnetic tunnel effect, the electrical resistance of the cell changes depending on the orientation of the fields in the two plates. Two plates having the same polarity indicate a logic state of "0", while two plates of opposite polarity indicates a logic state of "1" as resistance is higher. Another type of MRAM consists of two ferromagnetic plates separated by a magnetic, non metallic spacer layer. This utilizes the giant magnetoresistive (GMR) effect. Free electrons are generated 'spin-up' and 'spin-down' in equal proportions. When the orientation of both magnetic layers is parallel, only one type of electron is retarded. When the magnetic orientations of the layers are anti-parallel, both spin-up and spin-down electrons suffer retardation. In this way, resistance is varied to give logic "0" and "1". For both methods, one of the two plates is commonly fixed to one polarity and the other's field will change to match that of an external field²⁹⁻³¹. Issues with future development of MRAM includes disturbance from neighbouring cells, stability issues concerning the tunneling barrier and the free layer with increased scaling^{18, 31-33}.

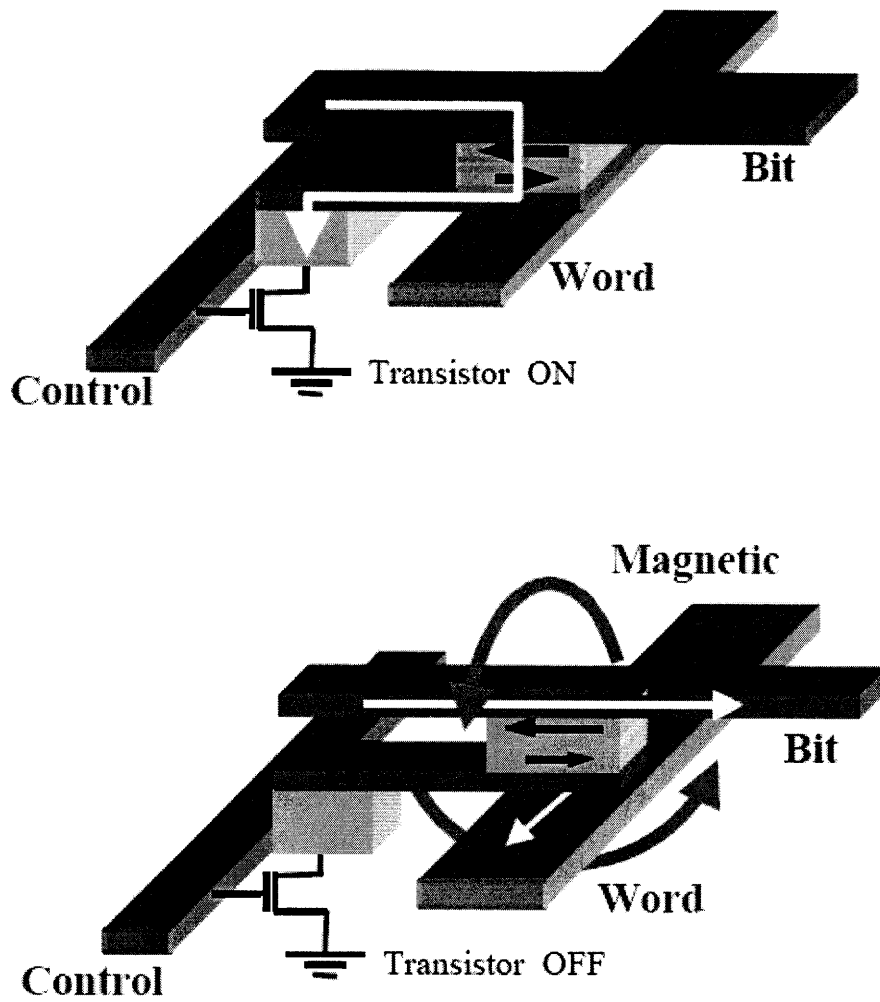


Figure 1.5. A MRAM Cell During Read (Above) and Write (Below) Operations³⁴

1.4 Nanocrystal Memory

Another area of active research is the use of nanocrystals to replace a single floating gate as storage sites. This is similar to the use of nitride traps in SONOS memory. It is

easy to integrate nanocrystal based memories into current CMOS processes. It also has several other advantages. This will be discussed further in the next chapter.

References

1. D. Kahng and S.M.Sze “A floating gate ad its application to memory devices,” Bell Syst. Tech. J., vol 46, p.1288, 1967
2. Jitu J. Makwana, Dieter K. Schroder “A non-volatile memory overview,” <http://aplawrence.com/Makwana/nonvolmem.html>
3. B.H. Koh *et al.* “Traps in germanium nanocrystal memory and effect on charge retention: modeling and experimental measurements,” J. of Appl Phys, vol 97, p.124305, 2005
4. Min She and Tsu-Jae King, “Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance,” IEEE Trans. On Electron Devices, vol 50, no 9, p. 1934, 2003
5. Ya-Chin King, Tsu-Jae King and Chenming Hu, “MOS Memory Using Germanium Nanocrystals Formed by Thermal Oxidation of $\text{Si}_{1-x}\text{Ge}_x$,” IEEE Electron Devices Meeting, p. 115, 1998
6. Wikipedia, “Flash Memory,” www.wikipedia.com.
7. Electronic Information Online, “Flash Memory Devices” <http://www.electronics-manufacturers.com/info/computers-and-laptops/flash-memory-devices.html>
8. Toshiba, “NAND vs NOR Flash Memory Technology Overview” <http://www.chips.toshiba.com>

9. Electronics Design, Strategy, News, "What is the difference between NAND and NOR Flash?" <http://www.edn.com/article-partner/CA6319916.html>
10. Michelle Kessler, "Demand for Flash Memory Skyrockets." http://www.usatoday.com/money/industries/technology/2005-09-18-flash-memory_x.htm
11. Michael Kanellos, "SanDisk drops prices with new flash drives." EETimes Encyclopedia http://news.com.com/SanDisk+drops+prices+with+new+flash+drive/2100-1041_3-6166983.html
12. Chris Preimesberger, "Hot Flash: 'Flashtops' Take On the Memory Market." eWeek.com <http://www.eweek.com/article2/0,1895,2008089,00.asp>
13. John Walko, "SanDisk targets gruvi music card at mobiles." EETimes Encyclopedia http://www.eetimes.com/showArticle.jhtml;jsessionid=ENNZMSCPVD3ZUQSN_DLOSKH0CJUNN2JVN?articleID=171201249
14. Dov Moran, "Progenitor of the USB Flash Drive," EETimes http://www.eetimes.com/showArticle.jhtml;jsessionid=ENNZMSCPVD3ZUQSN_DLOSKH0CJUNN2JVN?articleID=174401544
15. Theo Valich, "Flash will Kill BluRay ad HD DVD," <http://www.theinquirer.net/default.aspx?article=36930>
16. Michael Kenellos, "Is Flash Fried?" CNet News.com http://news.com.com/Flash+forward/2009-1040_3-994240.html

17. Aaron Theon and Jean Pierre Leburton, "Towards Single-Electronics," IEEE 2002
18. Betty Prince, "Trends in Scaled and Nanotechnology Memories," Memory Strategies International, IEEE, 2005
19. The International Technology Roadmap for Semiconductors 2006 Update, Process Integration, Devices and Structures
http://www.itrs.net/Links/2006Update/FinalToPost/04_PIDS2006Update.pdf
20. Jiankang Bu and Marvin H. White, "Design Considerations in Scaled SONOS Non-volatile Memory Devices"
http://klabs.org/richcontent/MemoryContent/nvmt_symp/nvmts_2000/presentations/bu_white_sonos_lehigh_univ.pdf#search=%22SONOS%20memory%22
21. Min She, "Semiconductor Flash Memory Scaling" pHD dissertation, 2003.
22. C.T. Swift et al, "An Embedded 90nm SONOS non-volatile memory utilizing hot electron programming and uniform tunnel erase," IEEE Electron Devices Meeting, p 927, 2002.
23. Dennis A. Adams, David Mavis, James R.Murray and Marvin H.White, "SONOS Non Volatile Memory Semiconductor Memories for Space and Military Applications."
http://klabs.org/richcontent/MemoryContent/nvmt_symp/nvmts_2000/papers/adams_d.pdf
24. Wikipedia, "Ferroelectric RAM,"
http://en.wikipedia.org/wiki/Ferroelectric_RAM

25. Samsung. "Samsung Introduces the Next Generation of Non-Volatile Memory – PRAM,"
http://samsung.com/PressCenter/PressRelease/PressRelease.asp?seq=20060911_000286481
26. Hendrik et al. "Ultra-high-density phase-change storage and memory," Nature Vol 5, 383, 2006.
27. PC-RAM Project Home Page <http://www.projects.ex.ac.uk/pcram/>
28. Yun Sheung Shin. "Non-volatile Memory Technologies for Beyond 2010," 2005 Symposium for VLSI Circuits Digest of Technical Papers, 2005
29. IBM, "IBM Research News",
http://www.research.ibm.com/resources/news/20001207_mramimages.shtml
30. Phillips Password Magazine, "MRAM- Magnetic Memory Goes Solid State",
<http://www.research.philips.com/password/archive/12/mram.html>
31. S. Tehrani et al, "Progress and Outlook for MRAM Technology", IEEE Transactions on Magnetics, Vol 35, No 5,p 2814, 1999
32. Johan Akerman, "Towards a Universal Memory", Science Vol 308, p508, 2005.
33. W.J. Gallagher et al. "Recent Advances in MRAM Technology, " IEEE VLSI Technology, p72-73 2005. (VLSI-TSA-Tech).
34. J.P. Nozieres, "Magnetic random access memories (MRAM): a truly universal memory?" Unpublished Paper

Chapter 2: Nanocrystal Memory

Nanocrystal memory has been an area under intense research since Tiwari et al. demonstrated a Si nanocrystal memory that uses direct tunneling into three dimensionally confined nanocrystals for bi-stability in the conduction of a transistor channel^{1,2}. Since then, memory effects of materials such as Germanium³⁻⁸ and transition metals such as Au, Ag, W, Pt and Sn⁹⁻¹³ have been investigated by various research groups worldwide.

2.1 Nanocrystal Memory Device

The memory devices demonstrated by Tiwari et al. are based on a Flash memory structure (consisting of a MOSFET as illustrated in Figure 1) with floating islands of silicon nanocrystals embedded in the gate oxide. This is illustrated in Figure 4. By using electrically isolated charge storage sites, charge leakage via localized oxide defects is reduced and a superior retention time can be achieved. As a result, a thinner tunneling oxide can be employed. This relaxation in the tunneling oxide constraint results in smaller operating voltages as well as lower power dissipation than current Flash EEPROM. It also brought about faster programming and at low operating voltage via direct tunneling mechanisms.^{1,2} Nanocrystal based memories are also more resistant to defects in the tunnel oxide. In addition, nanocrystal based memories are less complex to manufacture than conventional Flash memory. Conventional

memory requires 11 additional mask adds over the basic CMOS process while nanocrystal memory requires only 4. The reduction in complexity is due to the elimination of process steps to satisfy the high voltage requirements in conventional Flash memory. The removal of high voltage requirements in nanocrystal memory also enable nanocrystal memory to scale better than conventional Flash memory. This is evident from Figure 2.2. Germanium as well as metal-nanocrystal-based transistors work similarly to silicon nanocrystal memory.

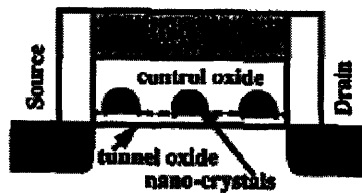


Figure 2.1: Schematic of Silicon Nanocrystal Based Memory

Process Step	Logic	Floating Gate	Nanocrystal
Isolation Formation	•	•	•
High Voltage Wells		2 masks	
NVM Array Well (1Mask)		1 mask	1mask
Tunnel Oxidation		•	
Floating Gate Deposition/Patterning		1 mask	
ONO/Nanocrystal Dep./Patterning		1 mask	1 mask
Low Voltage Wells	•	•	•
OGO Wells	•	•	•
High Voltage Oxidation/Patterning		1 mask	1 mask
OGO Oxidation Patterning	•	•	•
Low Voltage Oxide Growth	•	•	•
Gate Deposition	•	•	•
NVM Stack Patterning		1 mask	
NVM Source Hole Implant		1 mask	
NVM Drain Implant		1 mask	1 mask
Gate Patterning		•	•
High Voltage LDD Implants	•	2 masks	
OGO LDD Implants	•	•	•
S/D and Backend Processing	•	•	•
Masking Step Adder		+11	+4

Taken from:

R. Muralidhar et al, "A 6V Embedded 90nm Silicon Nanocrystal Non-volatile Memory",
IEEE Int Conf, 31, 2004

Table 2.1 Mask adders required to integrate nanocrystal based non volatile memory into a standard CMOS flow compared against conventional non volatile memory¹⁴

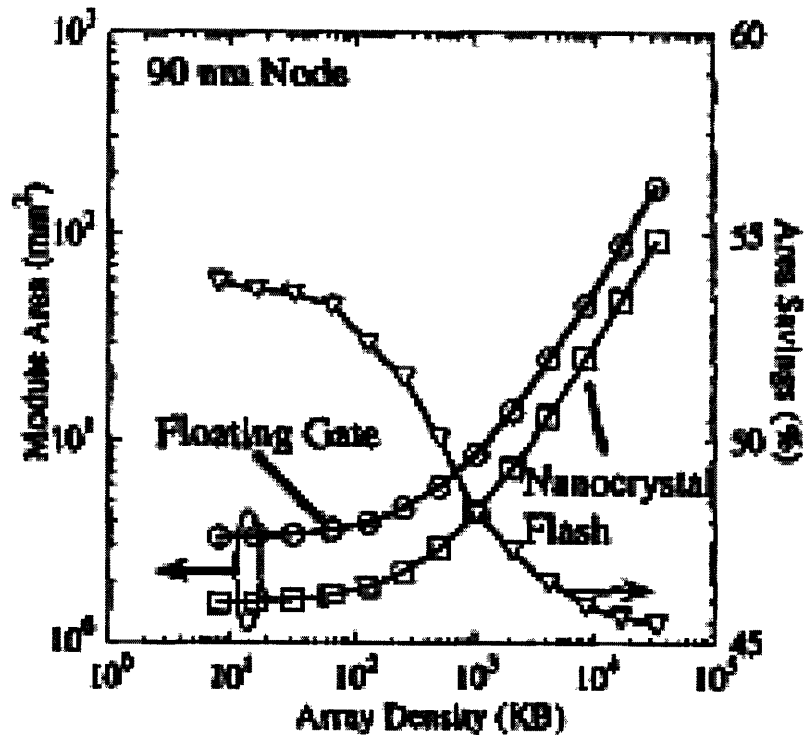


Figure 2.2: Memory module size for both conventional floating gate NVM and nanocrystal based NVM showing approximate factor of two reduction for nanocrystal based NVM¹⁴

2.2 Synthesis of Germanium Nanocrystals

There are numerous ways of synthesizing germanium nanocrystals. These include cosputtering⁵⁻⁷, chemical vapour deposition¹⁵⁻¹⁷, ion implantation^{3,4}, sol gel techniques¹⁸ oxidation and reduction of SiGe films¹⁹ and molecular beam epitaxy²⁰.

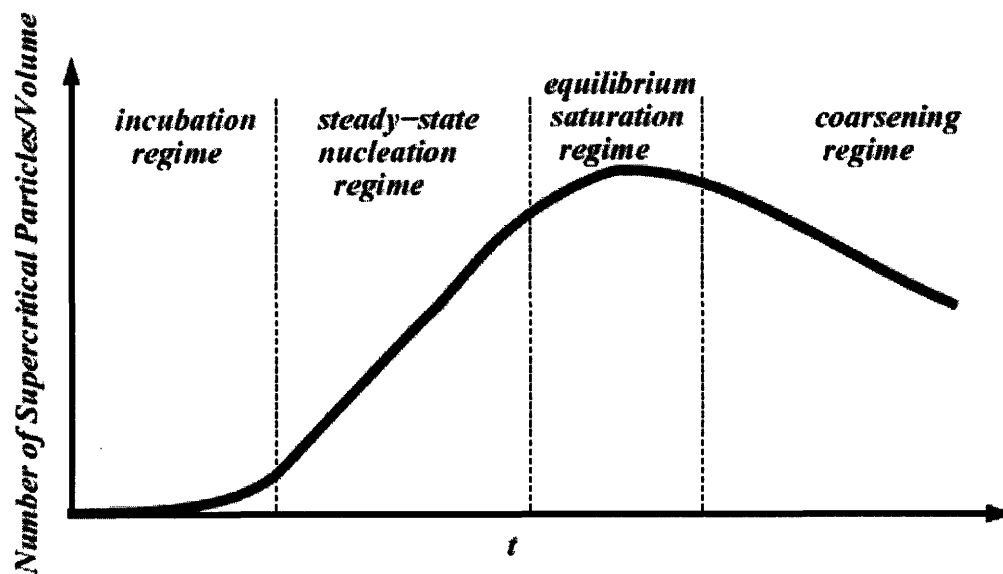


Figure 2.3: Schematic illustration of the density of supercritical particles as a function of time after quenching.²¹

Figure 2.3 shows a schematic illustration of the density of supercritical particles as a function of time after quenching. It can be observed that there are 4 stages of growth; namely, incubation, steady-state nucleation, equilibrium saturation and coarsening. In the incubation regime prior to the nucleation stage, the incubation time can be obtained by extrapolating the steady-state nucleation slope to zero density. In the nucleation stage, the steady-state nucleation rate can be predicted from the slope of the curve in this steady-state regime. Nanocrystals form by nucleation and growth.

The density of the particles peaks in the equilibrium saturation regime. Subsequently, coarsening or ripening of the particles occurs, where a decrease in the particle density is observed. In this stage, the supersaturation of the matrix with respect to the solute atoms is sufficiently small to make nucleation of new particles unlikely. Ostwald ripening (coarsening) of nanocrystals will then occur.

The nanocrystal size is usually controlled by time and annealing temperature. In the coarsening phase, the Lifshitz-Slyozov theory of coarsening in alloys is normally used to describe the time evolution of the sizes of the particles of a phase coarsening by mass transfer among particles in a matrix. The Lifshitz-Slyozov-Wagner (LSW) theory predicts the rate of coarsening in alloys. It states that at large times t , the critical dimension x_c tends asymptotically to depend on time as $t^{1/3}$. At the same time, the degree of supersaturation correspondingly falls as $t^{-1/3}$ and the number of grains as t^{-1} . Large particles grow while smaller ones shrink at the coarsening stage due to the Gibbs Thomson effect. The Gibbs-Thomson effect relates the curvatures of the spherical grains (represented by r_1 and r_2) to their corresponding activities (represented by a_1 and a_2) and hence solubilities in solution by the following equation:

$$RT \ln\left(\frac{a_2}{a_1}\right) = 2V_m \sigma \left[\frac{1}{r_2} - \frac{1}{r_1} \right]$$

R and T are the molar constant and the temperature, respectively. V_m represents the molar volume of a certain phase and σ represents the interfacial energy between two phases. The difference in the solute concentrations for different curvature particles

sets up a concentration gradient that drives diffusion of matter from the smaller to the larger particles^{21,22} .

The material in which Ge nanocrystals are embedded is usually SiO₂ although other types of materials such as Al₂O₃ are also investigated in research projects²³ .

2.3 Characterization of Nanocrystals

A variety of structural, optical and electrical techniques are commonly used to characterize Ge nanocrystals.

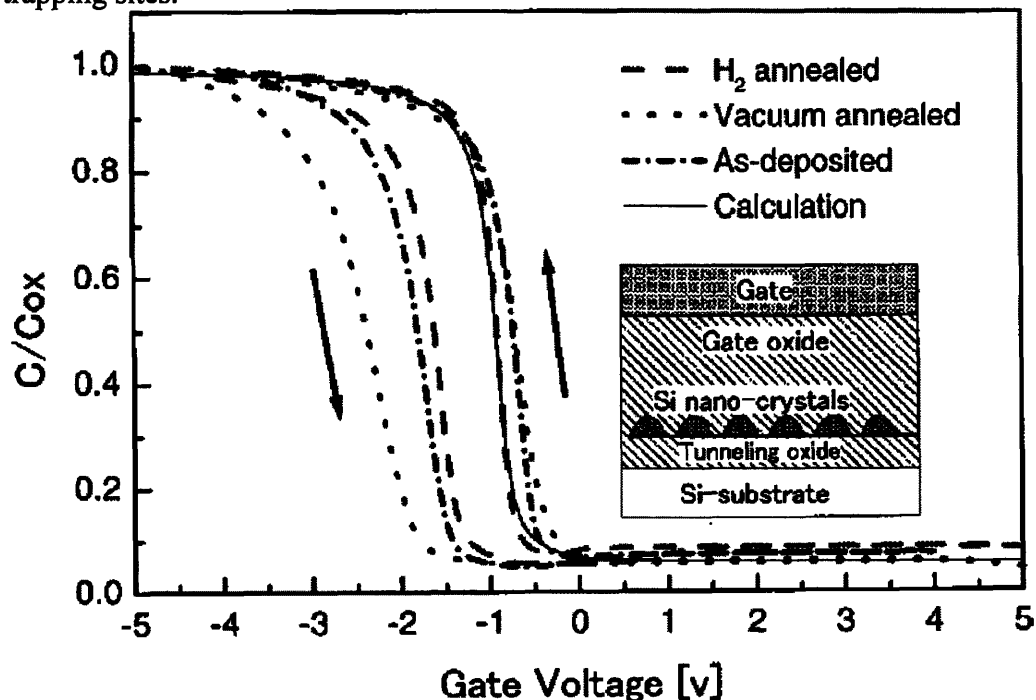
For structural characterization, transmission electron microscopy (TEM) is commonly used. It enables the size distribution, the spatial distribution, shape and defect structure of the nanocrystals to be studied. X-ray photoelectron spectroscopy is commonly used to investigate the chemical bonds that are present while Raman spectroscopy is used to determine the crystallinity and size of the nanocrystals. In addition, secondary ion spectroscopy (SIMS) allows a quantitative depth profiling of the elements in a sample.

The most commonly used characterization method is photoluminescence (PL) spectroscopy, especially in the study of quantum confinement effects. For electrical

methods, capacitance-voltage (C-V), capacitance-time (C-t) and current-voltage (I-V), measurements can be made to characterize the charge storing capability of nanocrystal-based transistor devices.

2.4 Charge Storage in Nanocrystal Memory Devices

There is an argument going on in the research community on the way in which nanocrystals store charge. It has been suggested that the charges are stored at the conduction band^{1,2,24} or at deep traps^{7,8,25}. Recent research indicates that charges are more likely linked to interfacial traps. Y. Shi et al. has highlighted that the band edge of a Si nanocrystal is higher than that of the substrate due to three dimensional quantum confinement effects. As a result, any electrons stored in the conduction band can easily tunnel back to the substrate. This cannot account for the observation of long retention times. He proposed that the injected electrons are stored at deep trapping sites.



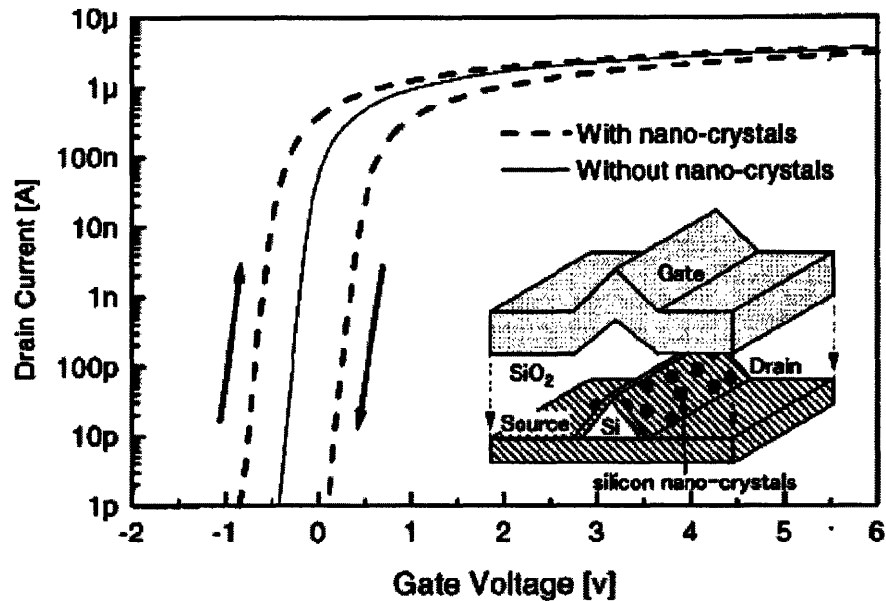


Figure 2.4: C - V hysteresis loops for various annealed MOS capacitors. The inset is a schematic of the MOS memory structure based on silicon nanocrystals²⁵.

In order to investigate the effect of traps on charge storage, Shi et al. annealed various MOS capacitors in an H_2 ambient at $430\text{ }^\circ\text{C}$ and in vacuum at $700\text{ }^\circ\text{C}$. The former process effectively decreased the number of interface traps by H-passivation, and the latter resulted in a high density of interface traps, especially P_b centers. Figure 2.4 shows the C - V characteristics for the treated samples as well as the as deposited ones. The device annealed in vacuum exhibited the largest V_{fb} shift as it has the highest trap density. The minimum V_{fb} shift is observed for the H_2 annealed device having the lowest trap density. This means that more charges are stored in the nanocrystals synthesized by annealing in vacuum rather than in H_2 .

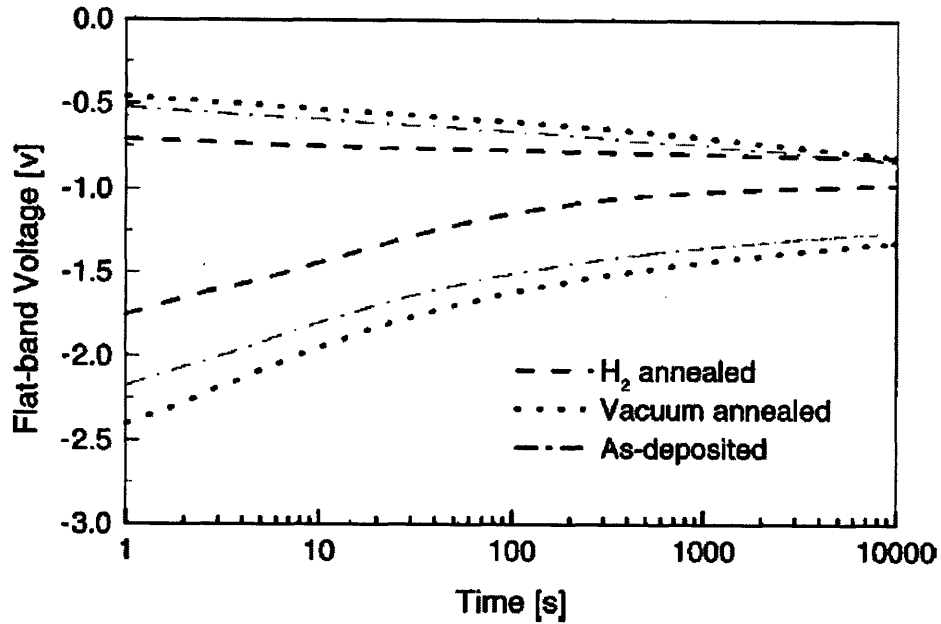


Figure 2.5: Long-term charge retention characteristics in various annealed MOS capacitors, measured using the constant-capacitance method at the flat-band point²⁵.

Figure 2.5 shows the long-term charge storage characteristics of various devices where the changes in the net charge stored in nanocrystals are proportional to the shifts of the V_{fb} obtained under constant-capacitance conditions. The fastest rate of electron loss is observed for the vacuum-annealed device while the H₂-annealed device has the slowest electron-loss rate. Therefore, a higher rate of charge loss is obtained for a device with a higher density of traps. Furthermore, the temperature dependence of the charge storage characteristics shows that the charge-loss rate decreases slightly when the temperature changes from 300 K to 80 K. This implies

that thermal activation is not dominant for the charge-loss processes in the tested samples.

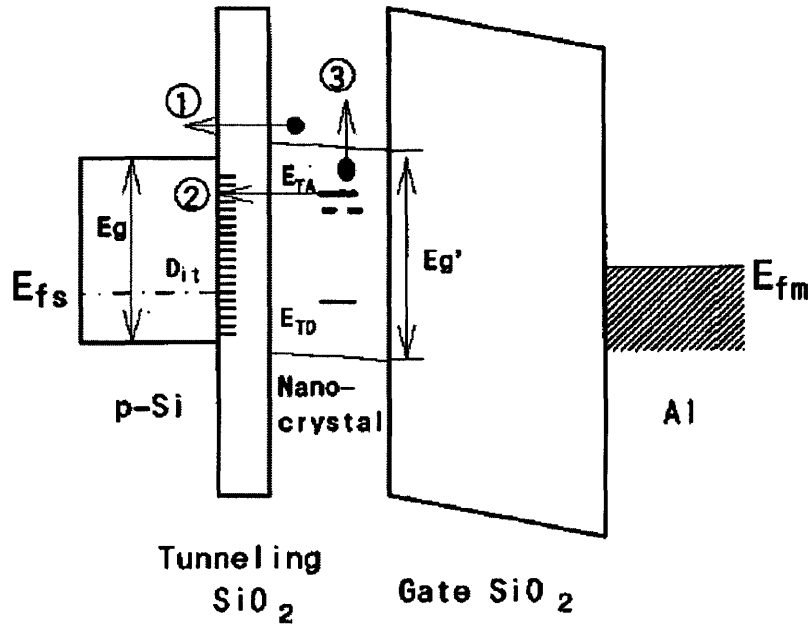


Figure 2.6: Energy band diagram of the MOS memory structure at flat-band condition for electron tunneling processes in the retention mode after injecting electrons²⁵.

Based on the above experimental results, Shi et al proposed a model whereby an injected electron will first fill up the empty states in deep trap levels prior to filling up shallower trap levels. There are two mechanisms in which electrons can be detrapped and lost to the silicon substrate. The first is direct tunneling from the traps to the interface states at the SiO_2/Si interface (process 2). Charge loss by this mechanism can be reduced by reducing number of interface states. The second is the indirect process involving the thermal detrapping of electrons to the conduction band (process 3) and then tunneling back to the substrate (process 1). A deeper trap level is

desirable for suppressing this kind of thermal activation. Shi et al. concluded from the experimental observation of charge loss rates on interface trap density and temperature that process 2 determines the long term charge retention in the samples. He further notes that the traps and defects at the internal/surface of nanocrystals and the interface states at the SiO₂/Si substrate play different roles in the charge-loss process. The traps and defects at the internal/surface of a nanocrystal determine the amount of charge that can be stored. On the other hand, a smaller number of the interface states in the Si/SiO₂ interface would effectively result in a lower tunneling rate and longer retention time²⁵.

Chen et al also concluded that at least some of the electrons are stored in traps after comparing experimental results with simulation data generated by another research group^{8,26}.

Unlike Shi et al²⁵, King²⁷ and Koh et al.²⁸ note a significant temperature dependence in their Ge nanocrystal memory samples. Like Shi, they demonstrated that the memory devices lose their memory effect after annealing in a hydrogen ambient, thus showing that charges are stored in the interfacial traps rather than in the conduction band. Koh et al²⁸ found good agreement of experimental data with simulations (Figure 2.6). The simulated data was based on the temperature dependent Shockley-Read-Hall (SRH) relationship developed by McWhorter et al.²⁹. The thermal equilibrium emission constant of electrons can be derived as

$$e_n = AT^2 \exp(-qE_t / kT),$$

where k is the Boltzmann constant, q is the electronic charge, T is the temperature, E_t is the trap energy level measured with respect to the conduction edge of the nanocrystal and A is the temperature independent constant which can be expressed as

$$4 \sqrt{\frac{6\sigma_e g k^2 m}{(\pi \hbar^2)^{3/2}}}$$

m is the effective mass of the electron, g is the degeneracy and

h is Planck's constant. Also, the drain current during the discharge phase is modeled as

$$I_{DS(transient)} = q \{ n_1 [1 - \exp(-\lambda_1 t)] + n_2 [1 - \exp(1 - \exp(-\lambda_2 t))] \},$$

where $n_1 + n_2 = n$ and n is the total number of nanocrystalline Ge charging sites. λ_1 and λ_2 represent the discharging rate constants for the two different discharging mechanisms.

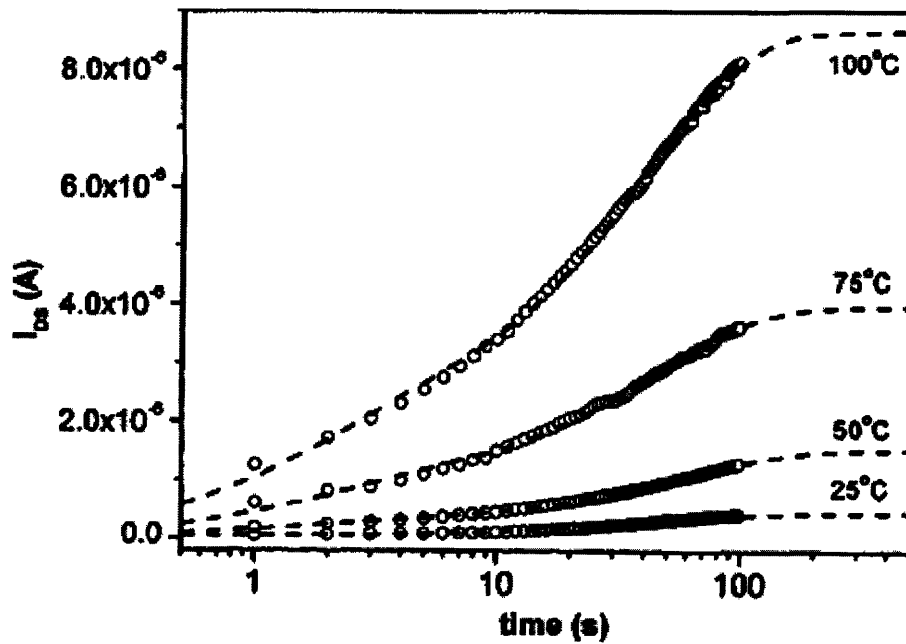


Figure 2.7: Drain current (I_{DS}) transient at a read voltage of 5V after a write operation at 15V for 20s. The symbols represent the measured data and the lines are fitted data from a simulation. The increase in I_{DS} for higher temperatures could be explained by the larger carrier mobility and the higher intrinsic carrier concentration of the substrate.²⁸

By performing transient drain current (I_{DS}) measurements, the trap energy levels (E_t) can be extracted. This is done by performing transient drain current measurements at different temperatures and calculating the discharging time constant (τ_D). τ_D is defined as the time corresponding to 90% of the I_{DS} at steady state, when the drain current gradually returns to steady state value. The electrons which are detrapped during the discharge phase increase the drain current over its steady state value. Figure 2.8 indicates that for the samples, below 307.7K, the discharging process is relatively temperature insensitive, which corresponds to Process 2 (direct tunneling from the traps to the interface states at SiO₂/Si interface) as described by Shi et al. Above 307.7K, Process 1 + 3 (indirect process involving the thermal detrapping of electrons to the conduction band and then tunneling back to the substrate) is more dominant and the discharging process shows a strong temperature dependence.²⁸

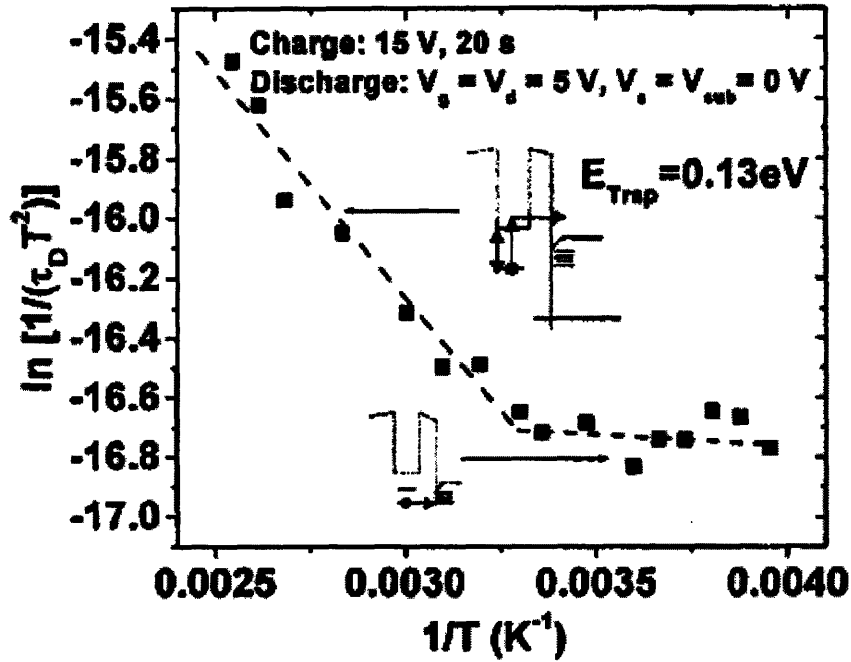


Figure 2.8: Inverse of discharging time constant ($1/\tau_D$) divided by the square of the temperature plotted against the inverse of T . The graph is plotted based on the calculations given by $R_D \propto e_n = AT^2 \exp(-qE_t / kT)$. R_D is the rate of discharge.²⁸

Based on the above research observations, the following conclusions can be made:

1. The discharge process is dominated by Process 1 + 3 at high temperatures and Process 2 at low temperatures.
2. At low temperatures, decreasing the interface state at SiO_2/Si substrate interface will improve retention time.²⁵

3. At high temperatures, controlling the deep level traps is crucial to increase the retention duration of the memory device. Engineering the trap energy level can be carried out by manipulating the material of the host matrix, doping with impurities or changing the material of the tunnel oxide. The last method is based on the assumption that the trap sites in the nanocrystals responsible for charge storage are close to the Si substrate and such trap sites are affected by the close proximity to the tunnel barrier. Koh et al were able to prove this by showing that that nc-Ge/Al₂O₃ has higher activation energies and hence deeper trap levels than nc-Ge/SiO₂.²⁸ Other than methods involving increasing trap levels, retention time can also be increased by increasing the tunnel barrier, such as using germanium/silicon (Ge/Si) heteronanocrystals, which will be discussed later.

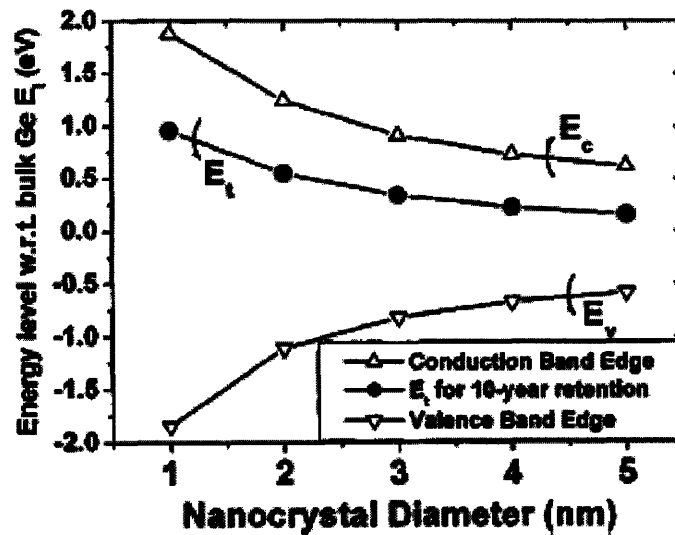


Figure 2.9: Trap energy level required for 10 year charge retention performance vs nanocrystal diameter. The Ge band-gap widening due to quantum confinement effect is also indicated. The conduction and valence bands edges at the boundaries of the

widened Ge band gap are given by E_c and E_v . $(E_c - E_i) = (E_i - E_v) = 0.33eV$ in bulk Ge, E_i is the midgap energy of Ge.²⁸

Figure 2.9 illustrates the trap energy required to meet the 10 year requirement taking into account quantum size effects²⁸. We can see from Figure 2.9 that as the size of nanocrystals decrease, $E_c - E_t$ increases, and deeper level traps are required. As the size of the nanocrystals decreases, the barrier height is lower and it is easier for the electrons to leak through the tunnel barrier. In order to compensate for this, deeper-level traps are required.

It is important to note that there is a tradeoff between read/write speeds and voltages with retention time. The thicker the tunnel oxide, the longer the retention time, the lower the operating speeds and the higher the voltages required. By improving retention time through other means, such as trap level engineering, read/write voltages can be decreased and operating speeds improved by decreasing the oxide barrier. Hence, other attributes such as operating speeds and voltages are inextricably linked to retention time.

2.5 Optimum Nanocrystal Size

There is also a tradeoff between the reliability/memory window with the retention time/programming speed. Generally, there is a need to fabricate nanocrystals as small

as possible in order to increase memory window and to reduce stress induced leakage during retention to improve reliability.

However, when the nanocrystals decrease, retention time is degraded as quantum confinement effects become significant. Confinement effects are strongly dependent on nanocrystal diameter and scales inversely with the square of nanocrystal diameter. In addition, coulomb blockage effects of small nanocrystals decrease tunneling probabilities and reduce programming speed. Coulomb charging effects are inversely proportional to the nanocrystal diameter. The two effects are evident from Figure 2.10. Retention time degrades as nanocrystal diameter decrease from 5nm to 2nm. Also, programming time is faster for 5nm diameter nanocrystals compared to 2nm diameter nanocrystals.

Neglecting effects of stress-induced leakage, we will attempt to estimate the largest nanocrystals that satisfy the minimum memory window requirements. The larger the size of the nanocrystals, the smaller the quantum confinement and coulomb blockage effects.³⁰⁻³²

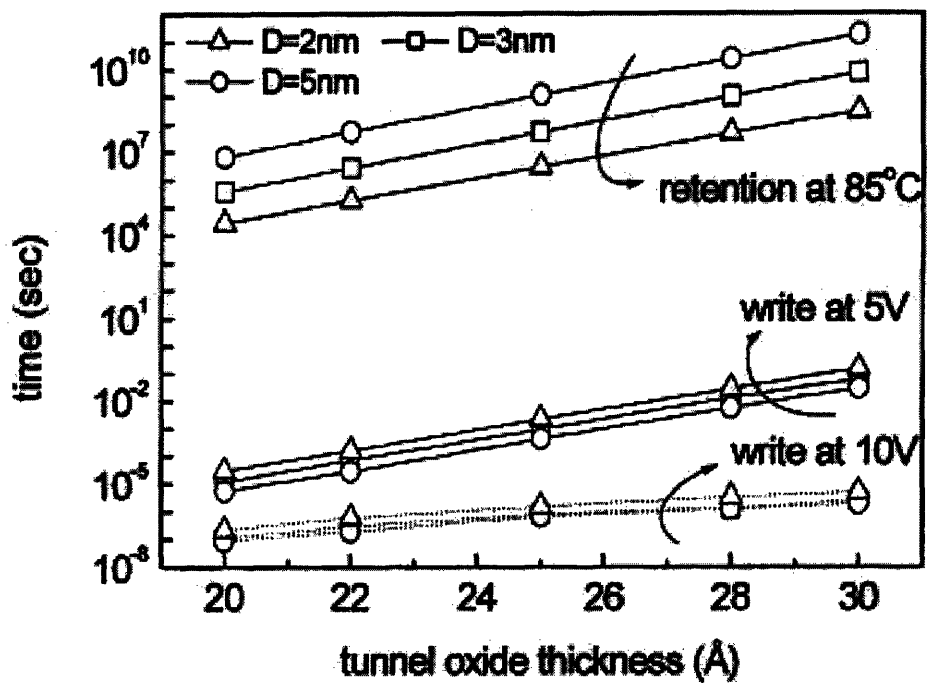


Figure 2.10: Retention characteristics at various tunnel oxide thicknesses and the Ge nanocrystal size on device performance³⁰

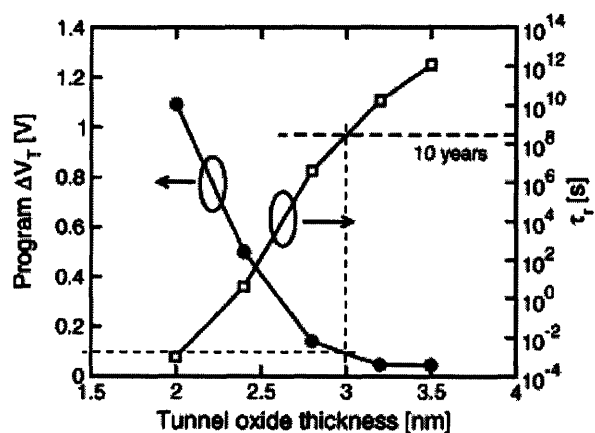


Figure 2.11: Plot of threshold voltage shifts ΔV_T and retention period τ_r as a function of tunnel oxide thickness.³¹

Referring to Figure 2.11, for a ten year retention period, a tunnel oxide thickness of 3nm is required. This corresponds to a ΔV_T of around 0.1V. This value can be used in the following equation

$$\Delta V_T = -R \frac{Q'}{C'}$$

where R is a factor correcting for the non uniform coverage of the area by discrete nanocrystals (assumed to be 0.4), Q' is the total charge density stored and C' is the nanocrystal-gate capacitance per unit area.³² Also,

$$C' = \frac{\epsilon}{t}$$

where ϵ is the dielectric constant of the interpoly silicon oxide dielectric and is given by $3.9 \times 8.854 \times 10^{-12} F/m$ and t is the interpoly silicon oxide thickness (assumed to be 6nm).³² Assuming that one nanocrystal on average stores one charge,

$$Q' = -Ne = -\frac{C' \times \Delta V_T}{R} = \frac{5.755 \times 10^{-3} \times 0.1}{0.4}$$

$$N = 9 \times 10^{15} / m^2 = 9 \times 10^{11} / cm^2$$

N is the nanocrystal density ($N = 9 \times 10^{15} / m^2 = 9 \times 10^{11} / cm^2$) and e is the electronic charge given by $1.6 \times 10^{-19} C$.³²

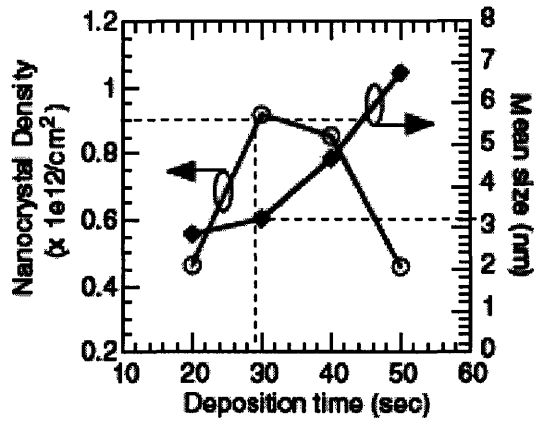


Figure 2.12: Nucleation curve for nanocrystal deposited by CVD on SiO_2 showing the evolution of nanocrystal density and size with deposition time.³³

Based on the above assumptions, the optimum nanocrystal size is 3nm. However, it must be noted that the optimum size is determined by factors such as the tunnel and interpoly oxide thickness as well as the method in which the nanocrystals are deposited (the nucleation curves for other methods of deposition, such as sputtering, may differ from that of CVD).

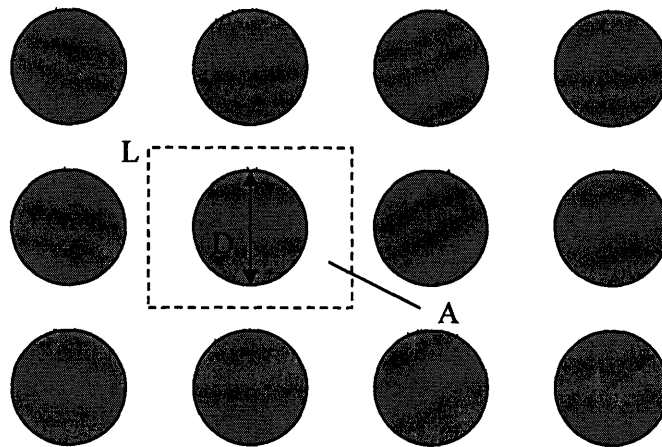


Figure 2.13: Ordered Array of Nanocrystals

If the nanocrystals are deposited in an ordered array as shown above, then

$$A = \frac{1}{N} = 1.11 \times 10^{-16} \text{ m}^2$$

$$L = \sqrt{A} = 1.05 \times 10^{-8} \text{ m}$$

Assuming that the spacing between the nanocrystal is equal to the nanocrystal diameter, then

$$D = \frac{L}{2} = 5.27 \times 10^{-9} \text{ m} = 5.27 \text{ nm}$$

2.6 Comparison of Different Nanocrystal Memories

The earliest work on quantum-dot Flash memories concentrated on nanocrystalline silicon (nc Si) as a replacement for the floating gate. Since then, numerous groups have proposed using nanocrystalline germanium (nc Ge) and metal dots such as Au, Ag, W, Pt, and Sn⁹⁻¹³. The main advantages of using metal nanodots include a higher density of states around the Fermi Level, making them more immune to Fermi Level fluctuations caused by contamination and ensuring tighter threshold voltage control, and the creation of an asymmetrical barrier by engineering the work function and thus inducing a smaller barrier for writing and a larger barrier for retention. The potential well of the metal nanocrystals can be carefully engineered to yield a small barrier for writing and a large barrier for retention. The use of different types of metal nanocrystals with different work functions opens the possibility of changing the barrier height by 2eV.⁹ However, the introduction of metal nanodots to current silicon processing technology is a great challenge. It is well known that the presence of contaminants vastly affects the performance of the transistor and an in-depth feasibility study needs to be undertaken before metal nanodots can be introduced to the baseline CMOS process.¹⁰ Also, most of the advantages of metal nanocrystals revolve around improving the retention time. This can be achieved through other means using semiconductor nanocrystal memories also as highlighted above.

There are no in-depth experimental studies comparing the performance of silicon and germanium nanocrystal memory devices. However, researchers have pointed out some theoretical advantages of Ge nanocrystals over Si. Ge has a smaller bandgap

compared to Si, which results in a higher confinement barrier for retention similar to metal nanocrystals.³⁴ Retention time could also be improved, especially if electrons detrapp by Process 1+3 as highlighted above.

2.7 Hetero-nanocrystal Memory

A novel MOSFET memory storage cell using Ge/Si hetero-nanocrystals has been proposed³⁵. Simulation results show that the hetero-nanocrystals have superior charge retention capability compared to Ge and Si nanocrystals alone. Ge has a smaller bandgap than Si and by introducing a Si interface around the nanocrystal, it would create an additional barrier height at the Ge/Si interface which makes it harder for electrons to leak out. A staircase potential well is created and charges will have to pass through both the potential barrier of Si nanocrystal and the tunnel barrier before it can leak out. During writing and erasing, the movement of charges is mainly affected by only the potential barrier of the tunnel oxide under the proper bias. Hence, the retention time could be prolonged remarkably while the writing and erasing time could be held to be approximately the same order of magnitude.³⁵

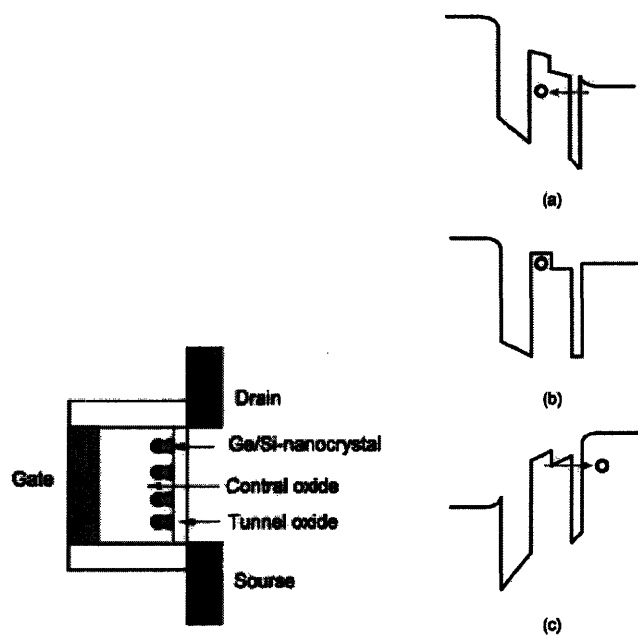
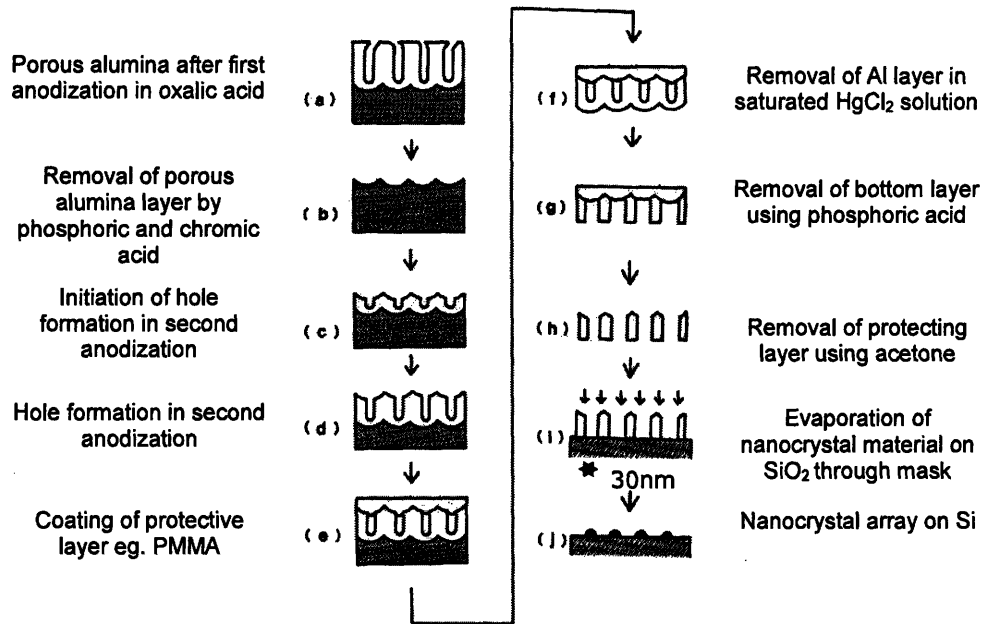


Figure 2.14: (Left) The schematic cross sectional of Ge/Si heteronanocrystal memory half cell. (Right) The valence band diagram for (a) hole writing (b) retention and (c) erasing. It is the effect of the compound barrier that prolongs the retention time of device evidently.³⁵

Two ways in which heteronanocrystal memories can be fabricated are: (1) using porous alumina and (2) using diblock copolymers.



*Fig 2.15: Fabrication of ordered nanocrystal array using porous alumina using a two step anodization process. The first anodization serves as a template for ordered hole formation in the second anodization.*³⁶

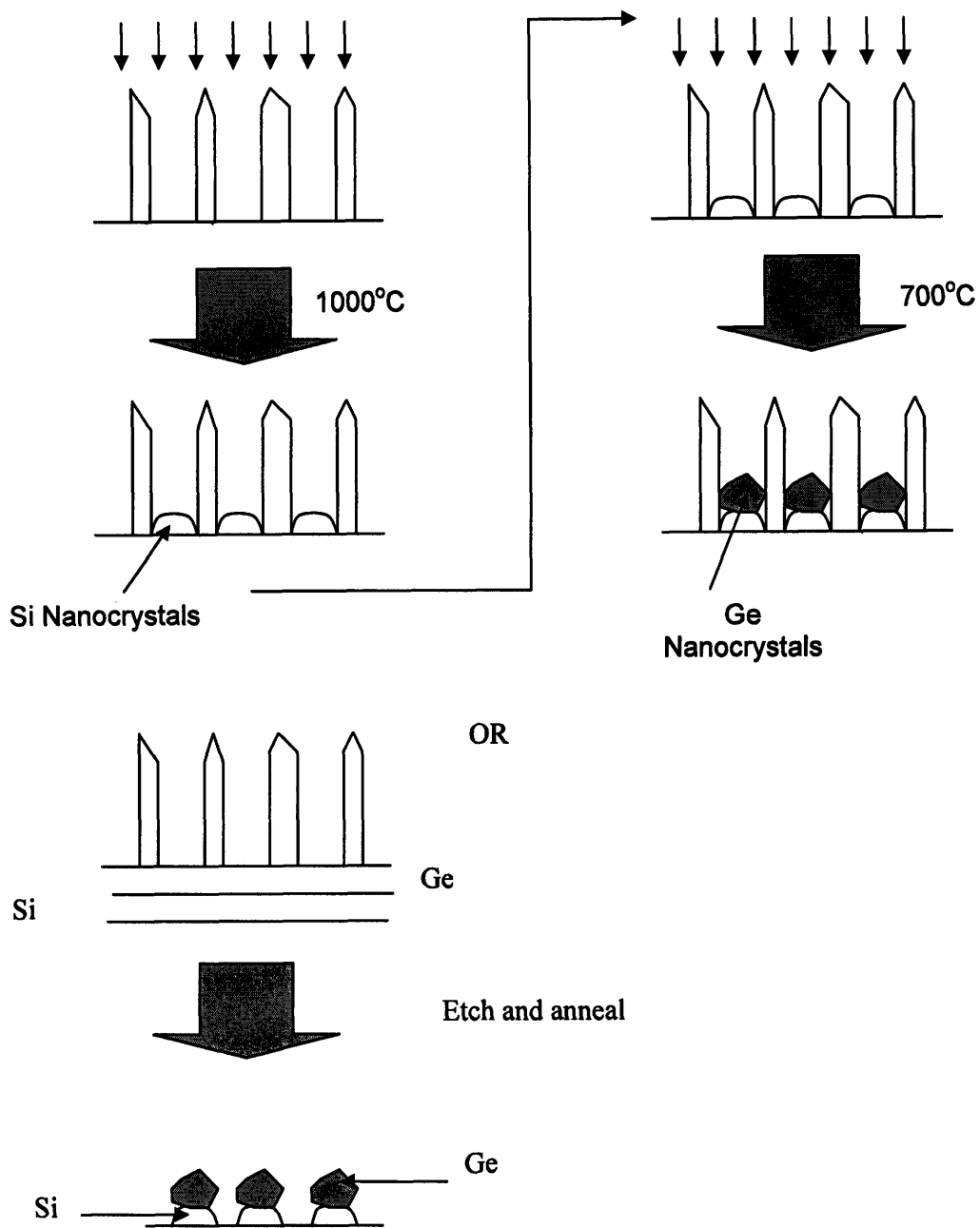


Fig 2.16: Formation of heteronanocrystals using porous alumina.

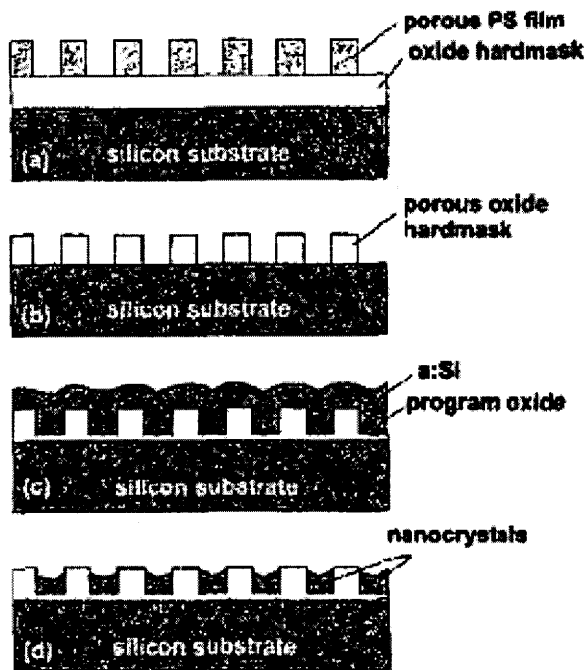
Fig. 2.15 illustrates one of the methods for fabricating porous alumina membranes. The fabricated alumina membrane can then be used for the ordered

deposition of heteronanocrystals or serve as masks for etching as shown in Figure 2.16. Experiments carried out using Ge nanodots show a highly ordered array.³⁷



*Figure 2.17: High magnification view of Ge nanodot array fabricated using alumina membrane.*³⁷

Diblock copolymers have been used for the ordered deposition of Si nanocrystals.³⁸ It is likely that these could be extended to heteronanocrystals.



Growing of oxide and spin coating + phase separation of polymer solution to promote phase separation

Etching of oxide

Growing of program oxide to form tunnel barrier + deposition of amorphous Si

RIE of amorphous Si + annealing for formation of Si nanocrystals

Figure 2.18: Ordered formation of silicon nanocrystals using diblock copolymers.³⁸

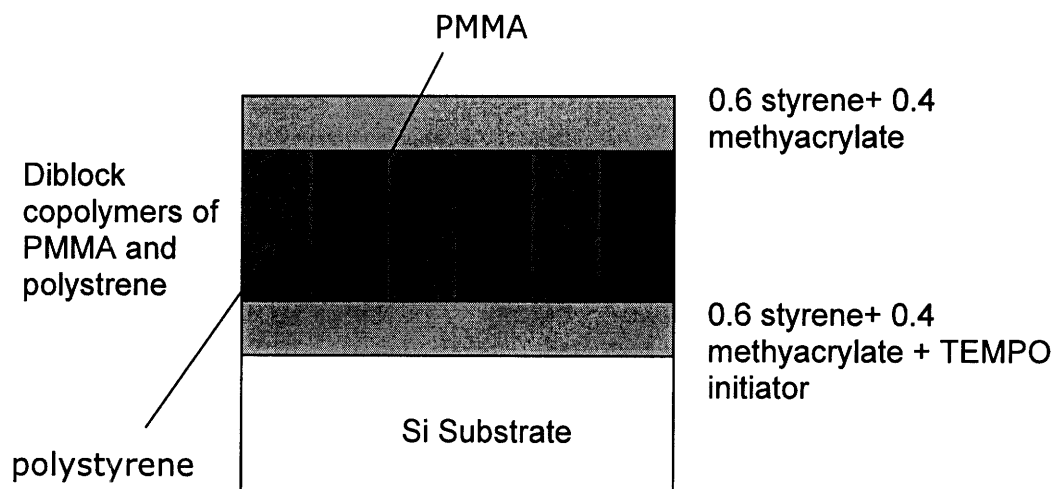


Figure 2.19: Schematic for formation of vertical blocks of polystyrene.³⁹

In order to form vertical blocks of polystyrene, a copolymer solution comprised of 0.6 styrene and 0.4 methylacrylate is first coated onto the silicon substrate and on top of the copolymers. At this proportion, the interfacial energy of styrene and the solution is equal to the interfacial energy of polymethylacrylate (PMMA) and the solution, resulting in vertical columns of styrene and methyacrylate being self assembled. If the copolymer solution is not applied, methylacrylate will preferentially wet the surface over styrene and horizontal blocks will result. If the top surface is not coated, an inverted 'U' shape, as shown in Fig 2.21, will develop.

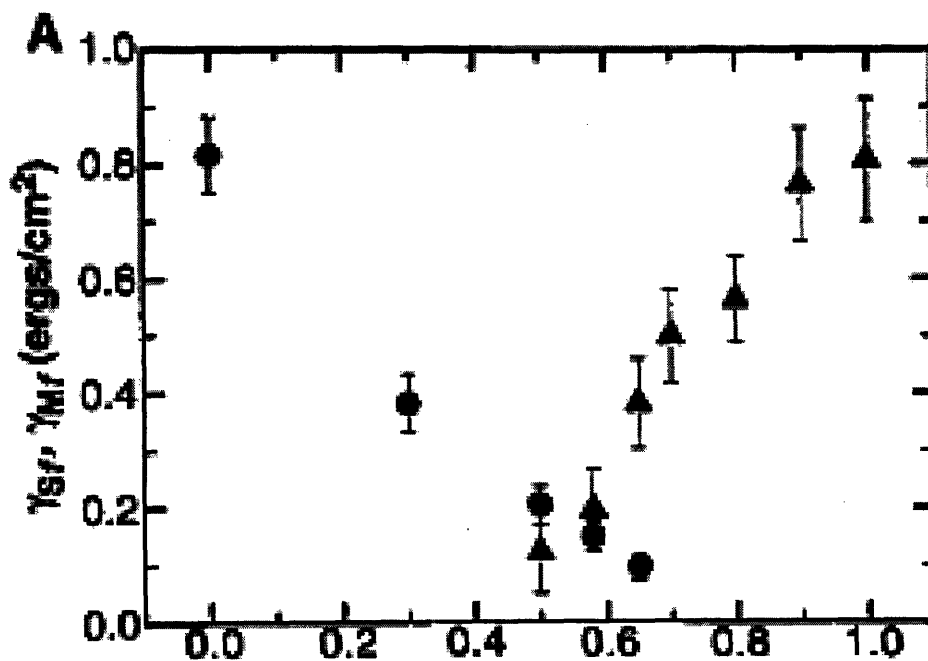


Figure 2.20: Interfacial energies γ_{Sf} and γ_{Mf} as a function of f . $\gamma_{Sf} = \gamma_{Mf}$ at $f \sim 0.6$ (0.6 styrene and 0.4 PMMA).⁴⁰

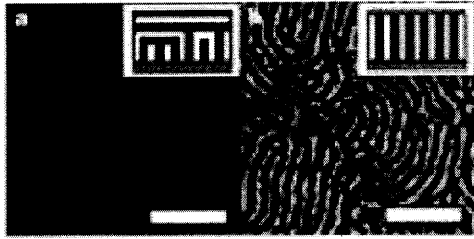


Figure 2.21: Atomic force microscopic phase images. Images are from thin films of P(S-b-MMA) symmetric diblock copolymer with a random copolymer anchored either a) to the substrate only or b) to the substrate and air surface. Insets indicate the orientation of the lamellar morphology.⁴¹

The TEMPO initiator shown in Fig. 2.19 binds the polymer solution to the silicon oxide through –OH functional groups on the TEMP initiator. The polystyrene film can then function as masks for deposition or etching as indicated in Figure 2.16.

2.8 Comparison between NC Memory and other Flash Replacement Technologies

In the International Technology Roadmap for Semiconductors (ITRS) 2006 Update, the predictions for cell sizes of the different memory technologies are as illustrated in figure 2.22. At the 80nm technology node, MRAM is ~16 times the cell size and FRAM is ~12 times the cell size of Flash Memory. In the near future, Flash and the closely related SONOS memories are still expected to have the highest chip densities. A flash memory /SONOS memory cell consists of only one transistor. An

FRAM cell consists of a transistor and a capacitor while a MRAM cell consists of a transistor and a magnetic tunnel junction. PCRAM consists of one chalcogenide and a transistor/diode. From the ITRS, it seems like it will take some time and effort for FRAM and MRAM technologies to catch up with flash/SONOS. On the other hand, nanocrystal-based memories are expected to face fewer difficulties in scaling as the architecture is similar to conventional Flash memories. Sizes comparable or less than (due to elimination of high voltage requirement structures) conventional Flash memories are expected.

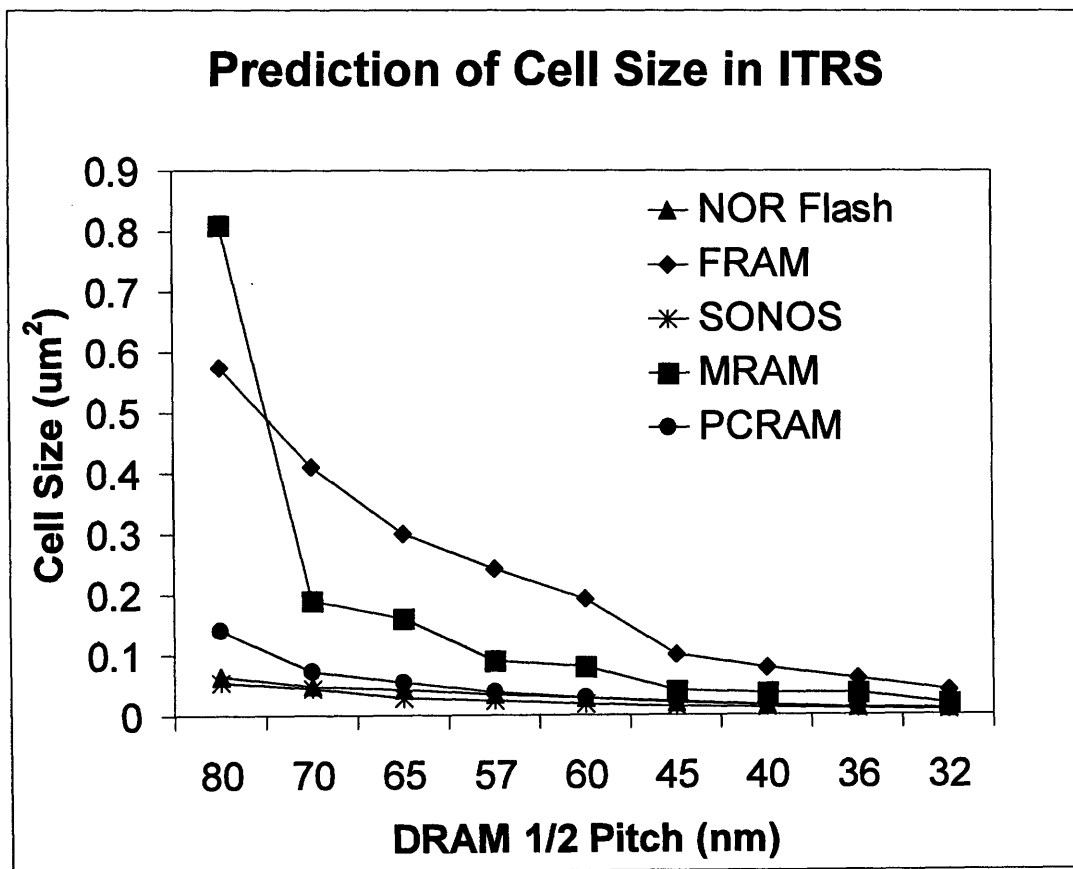


Figure 2.22: Cell Sizes of Different Memory Technology Nodes in the ITRS⁴²

Memory Type	Flash-NOR	Flash-NAND	FRAM	MRAM	PCRAM	SONOS	NC Memory
Endurance (Erase/Write Cycles)	1.00E+5	1.00E+5	1.00E+13	>3.00E+16	1.00E+12	1.00E+7	1.00E+7
Data Retention	20	20	10	>10	>10	20	20
Read/Program Voltage (V)	2/10	2/18	1.5/1.5	3.3/3.3	0.4/1	2/5.5	1/6
Read Time Per Bit	Fast ~10ns	Fast ~50ns	Fast/Medium 30-60ns	Fast 5-70ns	Medium 70ns	Fast	Fast
Write Time Per Bit	Low ~2 ms	Low ~0.4ms	Medium 30-60ns	Fast 5-70ns	Medium 100-500ns	Low-Medium 10µs	Medium <10µs
Erase Time Per Bit	Low ~900 ms	Medium ~2.0ms	Medium 30-60ns	Fast 5-70ns	Medium 100-500ns	Medium ~1ms	Low-Medium <100ms
Mask Adders to CMOS logic	11	11	2	3	5	4-7	4

<i>Process</i>							
<i>Technology</i>	<i>Charge</i> <i>Tunneling</i>	<i>Charge</i> <i>Tunneling</i>	<i>Ferroelectric</i>	<i>Magneti</i> <i>zation</i>	<i>Phase</i> <i>Transition</i>	<i>Charge</i> <i>Tunneling</i>	<i>Charge</i> <i>Tunneling</i>

Table 2.2: Different Types of Memory Technologies⁴³⁻⁵⁰

Table 2.2 compares some of the key attributes of nanocrystal memory with other forms of memories. Care must be taken when making comparisons as most of the emerging memories such as MRAM and nanocrystal memories are manufactured on older technology nodes compared to conventional Flash. Others such as PCRAM have not been mass manufactured at the time of writing and performances can only be compared based on research papers as well as press releases.

Some of the other key advantages of Ge nanocrystal memories, in addition to ease of scaling, include low read/write voltages and low manufacturing complexities. Si nanocrystal memory manufactured by Freescale Semiconductors has shown a read voltage of 1 V and a write voltage of 6V.⁴⁴⁻⁴⁵ Germanium based nanocrystal memory is expected to have similar read/write voltages. Also, nanocrystal memory requires 4 additional mask adders to the baseline CMOS manufacturing process. This is low compared to conventional Flash Memory's 11. In comparison to other emerging memories on Table 2.1, its manufacturing complexity is still low. The main weakness of nanocrystal based memories is expected to be the writing/erase speed. The thinner tunnel barrier is expected to improve the writing/erase speed over conventional Flash memories. However, its writing speed is slow compared to competitors such as MRAM. Although

the endurance of nanocrystal memories is lower than that of competitors such as PCRAM and MRAM, it is still higher than conventional flash memory cells. At present, endurance is still not a major issue for non-volatile memories. Nanocrystal memory is expected to face the strongest competition from phase change memory as Samsung has recently announced that it has produced a working prototype of PCRAM that is comparable to the size of NOR Flash.⁴⁵ At present, there seems to be no clear cut technical advantages of PCRAM over nanocrystal memories and vice versa based on Table 2.2. It is also difficult to predict whether continued research will allow any of the emerging forms of non-volatile memory to have a clear cut advantage over one another. In order for phase change memory to scale further down than conventional flash memory, other types of selectors other transistors should be used. Samsung is working on using vertical diodes to replace transistors. For nanocrystal memories, continued research into areas such as heteronanocrystals as well as trap engineering may help nanocrystal memory to improve attributes such as endurance and read/write speed. Schemes such double gate nanocrystal memories have also been proposed to improve retention. In double gate nanocrystal memories, the devices are fabricated on a silicon-on-insulator (SOI) substrate. The buried oxide below the SOI body is removed by dipping into hydrogen fluoric acid (HF). After the tunnel oxide is thermally grown, silicon nanocrystals, the control oxide, and a gate electrode of phosphorous-doped polysilicon are deposited around the undoped SOI body using low pressure chemical vapour deposition. In double-gate nanocrystal memories, the body potential is lifted up by electrons in the opposite additional nanocrystals, reducing the potential difference and discharge probability, improving retention time.⁵¹

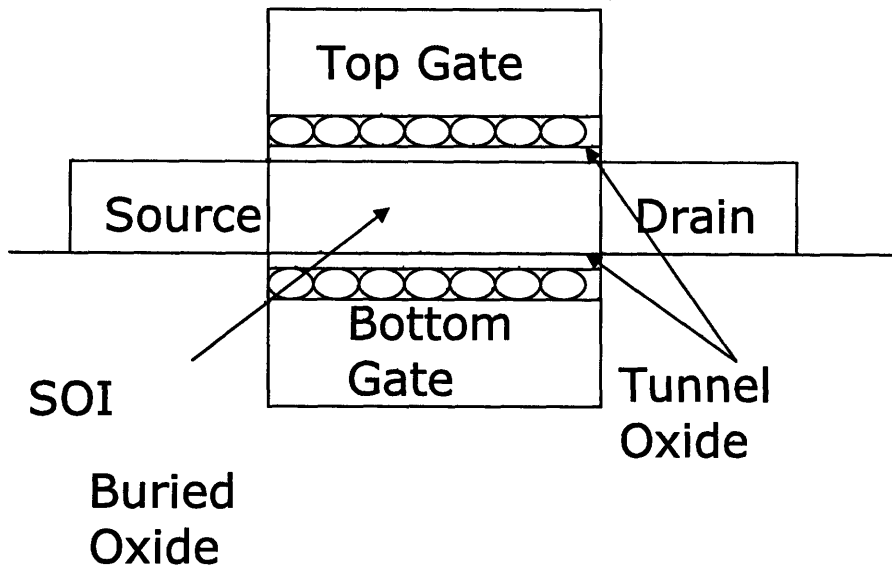


Figure 2.23: Schematic of double gate nanocrystal memories with ultrathin body structure

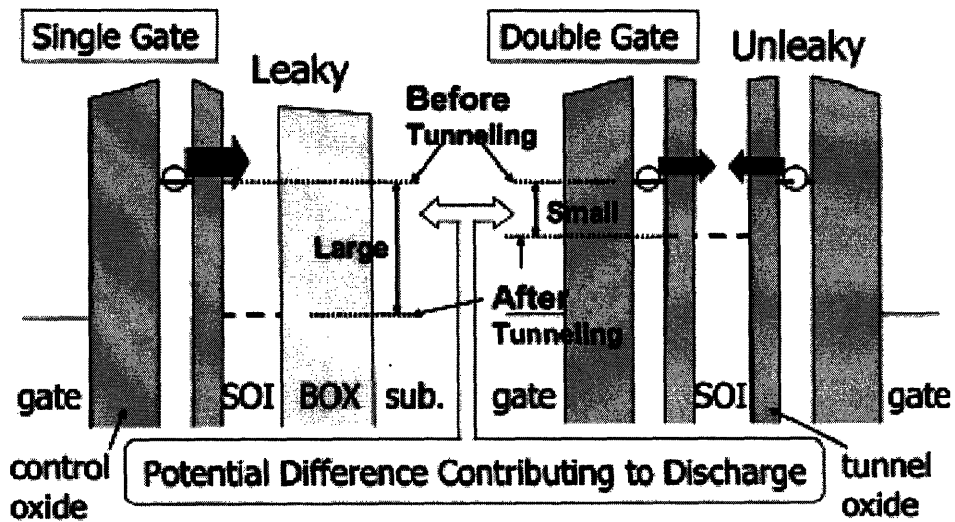


Figure 2.24: Energy band diagram in retention just after a write pulse⁵¹

2.9 Multi-bit Schemes

Various multi-bit schemes have been proposed in order for more bits to be stored per unit area.

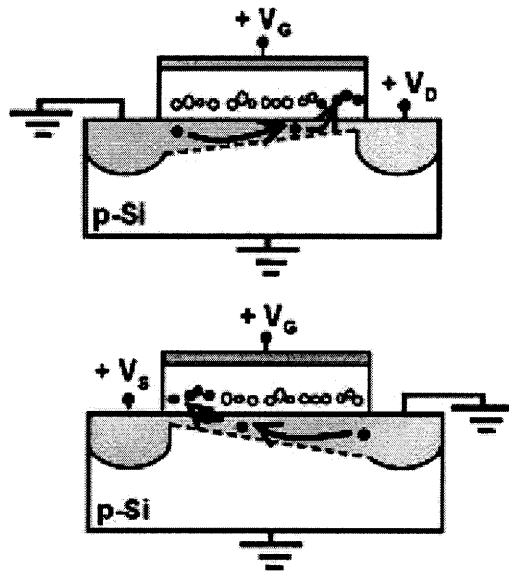


Figure 2.25: Schematic on the use of discrete traps for charge storage to realise a dual bit memory cell⁵²

Figure 2.25 shows one such scheme for multi bit storage. As the nanocrystals are well separated from one another with no or limited lateral diffusion. Charges stored can be localized near the source or drain. In order to store charges in the nanocrystal near the drain, a positive bias is applied to the drain during writing as shown in Figure 2.25. Similarly, charges can be stored in nanocrystals near the drain by applying a positive bias to the source.⁵²

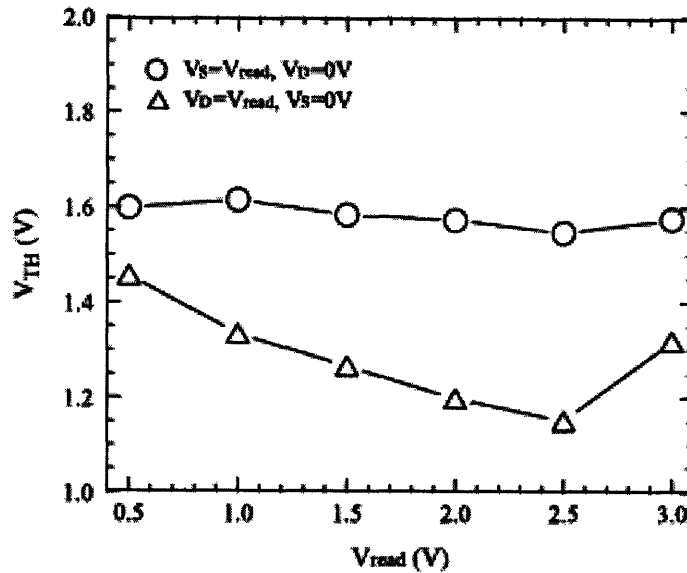
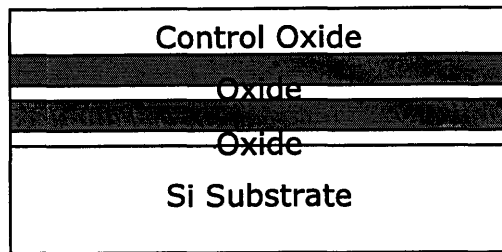


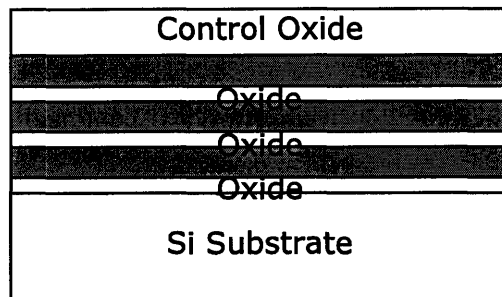
Figure 2.26: Difference of threshold voltage between the read with drain and with source after programming by channel hot electron with high drain bias⁵³

The programmed cell is read in the forward and reverse direction to determine whether the charges are stored near the source or drain. Due to the asymmetric distribution of charges, the threshold voltage for reverse reading is larger than the one for forward reading.⁵³

Multi-level nanocrystal memories have also been proposed for multi-bit storage. In multilevel nanocrystal memories, nanocrystal layers are deposited alternately with tunnel oxide as shown in Figure 2.27.



Two Layer Schematic



Three Layer Schematic

Figure 2.27: Two and three layer schematics of multilevel nanocrystal memories.⁵⁴

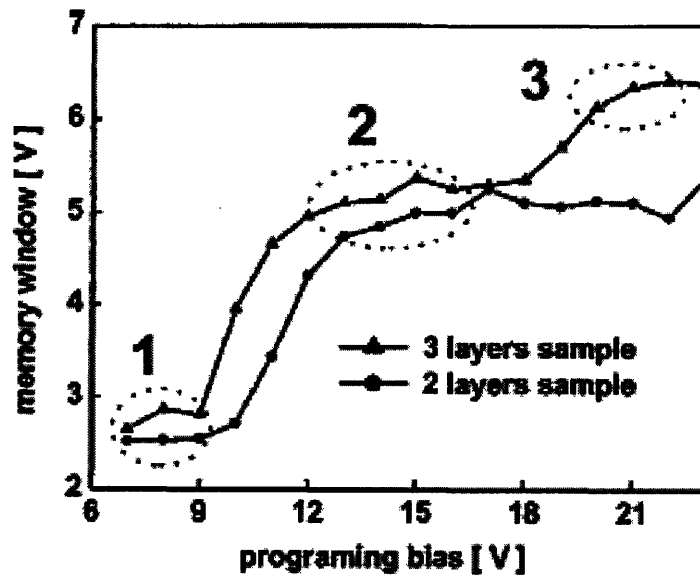


Figure 2.28: The dependence of the memory window on programming voltage. There are three apparent stages observed for the three layer samples, and two stages for the layer samples.⁵⁴

Distinct steps can be observed in the memory window and this can form the basis for a multi-bit storage scheme.⁵⁴ It is also possible to combine the above two multi-bit schemes to increase the number of bits per transistor. However, continual research work to increase the memory window and decrease fluctuations in the supplied voltage is required to make this a reality.

References

1. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe and K. Chan, "A Silicon Nanocrystals Based Memory", *Applied Physics Letters*, vol. 68, no. 10, pp. 1377-1379, 1996.
2. S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan and D. Buchanan, "Volatile and Non-volatile memories in Silicon with Nanocrystal Storage", *International Electron Device Meeting*, pp. 521-524, 1995.
3. Y. C. King, T. J. King and C. Hu, "MOS memory using germanium nanocrystals formed by thermal oxidation of $\text{Si}_{1-x}\text{Ge}_x$ ", *International Electron Device Meeting Technical Digest*, pp. 115-118, 1998.

4. Y.C. King, T. J. King and C. Hu, "Charge-trap memory device fabricated by oxidation of $\text{Si}_{1-x}\text{Ge}_x$ ", IEEE Transactions on Electron Devices, vol. 48, no. 4, pp. 696-700, 2001.
5. W.K. Choi, W.K. Chim, C.L. Heng, L.W. Teo, V. Ho, V. Ng, D.A. Antoniadis and E.A. Fitzgerald, "Observation of memory Effect in Ge Nanocrystals Embedded in Amorphous Silicon Oxide Matrix", Applied Physics Letters, Vol 80, No 11, pp. 2014-2016, 2002
6. L.W. Teo, W.K. Choi, W.K. Chim, V. Ho, C.H. Moey, M.S. Tay, C.L. Heng, Y. Lei, D.A. Antoniadis and E.A. Fitzgerald ;"Size control and charge storage mechanism of germanium nanocrystals in a metal-insulator-semiconductor structure", Appl. Phys. Lett., vol. 81, no. 19, pp. 3639-3641, 2002.
7. E.W.H. Kan, W.K. Choi, W.K. Chim, E.A. Fitzgerald and D.A. Antoniadis, "Origin of charge trapping in germanium nanocrystal embedded SiO_2 system: Role of interfacial traps?", J. Appl. Phys., vol. 95, no. 6, pp. 3148-3152, 2004.
8. J. H. Chen, Y.Q. Wang et al, "Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High K Tunneling and Control Oxides: Device Fabrication and Electrical Performance", IEEE Trans. On Electron Devices, Vol 51., No 11., pp 1840-1848
9. Z. Liu, C. Lee, V. Narayanan, G. Pei and E.C. Kan, "Metal Nanocrystal Memories – Part 1: Device Design and Fabrication," IEEE Trans. Electron Devices, vol 49, pp 1606-1613, 2002

10. Z. Liu, C. Lee, V. Narayanan, G. Pei and E.C. Kan, "Metal Nanocrystal Memories – Part 2: Electrical Characteristics," IEEE Trans. Electron Devices, vol 49, pp 1614-1622, 2002
11. Nakajima, T. Futatsugi, N. Horiguchi, H. Nakao and N. Yokoyama, "Single Electron Charging of Sn Nanocrystals in Thin SiO₂ Film Formed by Low Implantation," Int. Electron Device Meeting, p 159, 1997
12. Chungho Lee, Tup-hung Hou and Edwin C. Kan, "Metal Nanocrystal/nitride Heterogenous-stack Floating Gate Memory, " Device Research Conference - Conference Digest, DRC, v 2005, 63rd Device Research Conference Digest, DRC'05, 2005, p 97-98
13. C. Saragentis, K. Giannakop, A. Travolas, D. Tsamakis, "Fabrication and Characterization of a Metal Nanocrystal Memory Using Molecular Beam Epitaxy," Journal of Physics: Conference Series, v 10, n 1, 2005, p 53-6
14. R. Muralidlar, R.F. Steimle, R.F. Sadd et al, "An embedded silicon nanocrystal non-volatile memory for the 90nm technology node operating at 6 V," Integrated Circuit Design and Technology, ICICDT'04 International Conference on 2004, p 31-35, 2004.
15. Y.Q. Wang, J.H. Chen, W.J. Yoo, Y.C. Yeo, "Chemical Vapour Deposition of Germanium Nanocrystals on Hafnium Oxide for Non-volatile Memory Applications," Materials and Processes for Non-volatile Memories Symposium, Materials Research Society Symposium Proceedings, V830, p269-274, 2005.

16. M.Kanoun, T. Baron, E. Gautier and A. Soufi, "Charging Effects in Ge Nanocrystals Embedded in SiO₂ Matrix for Non Volatile Memory Applications", *Materials Science and Engineering C, Biomimetic and Supramolecular Systems*, V 26, n2-3, p360-3, 2006.
17. Medeiros-Ribeiro G, Bratkovski A.M., Kamins T.I, Ohlberg D.A.A., Williams, R.S., "Shape Transition of Germanium Nanocrystals on a Silicon (001) Surface from Pyramids to Domes", *Science*, V279, n5349, p 353-5, 1998.
18. M. Nogami and Y. Abe, "Sol-gel method for synthesizing visible photoluminescent nanosized Ge-crystal-doped silica glasses", *Applied Physics Letters*, vol. 65, pp. 2545-2547, 1994.
19. V. Craciun, A. H. Reader, D. E. W. Vandenhoudt, S. P. Best, R. S. Hutton, A. Andrei and I. W. Boyd, "Low temperature UV oxidation of SiGe for preparation of Ge Nanocrystals in SiO₂", *Thin Solid Films*, vol. 255, pp. 290-294, 1995.
20. A. Kanjilal, J. L. Hansen, P. Gaiduk and A. N. Larsen, "Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy", *Applied Physics Letters*, vol. 82, no. 8, pp. 1212-1214, 2003.

21. S.M. Allen, Massachusetts Institute of Technology, MIT 3.205 Thermodynamics and Kinetics of Materials Lecture Notes Chapter 7-11, 2006.
22. C.V. Thompson, Massachusetts Institute of Technology, MIT 3.44 Materials Processing for Micro and Nano Systems “Nanocrystal Growth and Assembly”, 2006
23. E.W.H. Kan, B.H. Koh, W.K. Choi, W.K. Chim, DA. Antoniadis and E.A. Fitzgerald, “Nanocrystalline Ge Flash Memories: Electrical Characterization and Trap Engineering”, The 5th Singapore-MIT Alliance Annual Symposium, 2005.
24. T. Kobayashi, T. Enoch, H. Fukuda, S. Nomura, A. Sakai and Y. Ueda, “Ge Nanocrystals in SiO₂ Films”, Appl. Phys Lett. 71, 1195, 1997.
25. Y. Shi, , K. Saito, H. Ishikuro and T. Hiramoto, “Effects of Traps on Charge Storage Characteristics in Metal-Oxide-Semiconductor Memory Structures Based on Silicon Nanocrystals”, Journal of Appl. Phys. 84, 2358, 1998.
26. C.M. Compagnoni, D. Ielmini, A.S. Spinelli, A.L. Lacaita, C. Gherardi, L. Perniola, B. De Salvo and S. Lombardo, “Program/erase dynamics and channel conduction in nanocrystal memories”, IEDM tech. Digest, V2003, pp549-552.
27. Y.C. King, Ph.D. Dissertation, University of California, Berkeley, CA, 1999.
28. B.H. Koh, E.W.H. Kan, W.K. Chim and W.K. Choi, D.A. Antoniadis and E.A. Fitzgerald, “Traps in Germanium Nanocrystal Memory and Effect on

Charge Retention: Modeling and Experimental Measurements”, J. of Appl. Phys. 97, 124305, 2003.

29. P.J. McWorter, S.L. Miller and T.A. Dellin, “Modelling the Memory Retention Characteristics of Silicon-nitride-oxide-silicon Non-volatile Transistors in a Varying Thermal Environment”, J. Appl. Phys, 68, 1902, 1990.
30. Min She and Tsu-Jae King, “Impact of Crystal Size and Tunnel Dielectric on Semiconductor Nanocrystal Memory Performance”, V50,N9, p1934, 2003.
31. Christian Monzio Compagnoni, Daniele Ielmini, Alessandro S. Spinelli and Andrea L. Lacita, “Optimization of Threshold Voltage Window Under Tunneling of Program/Erase in Nanocrystal Memories”, IEEE Transactions on Electron Devices, V52, N11, 2005.
32. Christian Monzio Compagnoni, Daniele Ielmini, Alessandro S. Spinelli and Andrea L. Lacita, “Modelling of Tunneling P/E for Nanocrystal Memories”, IEEE Transactions on Electron Devices, V52, N4, 2005.
33. R.A. Rao, H.P. Gasquet, R.F. Steimle et al, “Influence of Silicon Nanocrystal Size and Density on the Performance of Non-volatile Memory Arrays”, Solid State Electronics, 49, p1722-1727, 2005.
34. Teo Lee Wee, “ Germanium Nanocrystal Charge Storage Device in Silicon Oxide Matrix”, pHD dissertation, 2004.

35. H.G. Yang, Y. Shi, S.L. Gu, B. Shen, P. Han, R. Zhang and Y.D. Zhang, "Numerical Investigation of Characteristics of p-channel Ge/Si Heteronanocrystal Memory", *Microelectron. J.* 34, 71, 2003.
36. Hideki Masuda and Masahiro Satoh, "Fabrication of Au Nanodot Array Using Anodic Porous Alumina as an Evaporation Mask," V35, L126, 1996
37. Z. Chen et al., "Synthesis of Ge Nanodots on Si Using Anodic Alumina Membrane Mask," 268, p.560, 2004.
38. Guarini et al. ,"Low voltage, scalable nanocrystal FLASH memory fabricated by templated self assembly", *Technical Digest, IEDM*, 2003
39. Thomas Thurn-Albrecht et al. *Advance Mat. Communications*, 12, 11, 787.
40. P.Mansky, Y. Liu, E. Huang, T.P. Russell and C. Hawker, *Science*, V275, p1458, 1997.
41. E. Huang, L.Rockford, T.P. Russell and C.J. Hawker, *Nature*, 395, 757, 1998
42. The International Technology Roadmap for Semiconductors 2006 Update, Process Integration, Devices and Structures http://www.itrs.net/Links/2006Update/FinalToPost/04_PIDS2006Update.pdf
43. Betty Prince, "Trends in Scaled and Nanotechnology Memories", unpublished.
44. Kinam Kim and Gwan-Hyeob Koh, "Future Memory Technology including Emerging New Memories", *Proc 24th Int. Cof on Microelectronics*, Vol 1, 16-19, 2004.
45. Min She, "Semiconductor Flash Memory Scaling," *pHD dissertation*, 2003.

46. Toshiba, "NAND vs NOR Flash Memory Technology Overview,"
http://www.toshiba.com/taec/components/Generic/Memory_Resources/NANDvsNOR.pdf
47. Jiankang Bu and Marvin H. White, "Design Considerations in Scaled SONOS Nonvolatile Memory Device", Unpublished
48. R. Muralidhar, R.F. Steinle, M. Sadd, R. Rao et al., "A 6V 90nm Silicon Nanocrystal Non-volatile Memory," IEEE International Electron Devices Meeting, p. 601, 2003
49. Physorg.com, "Freescale manufactures world's first 24 Mbit silicon Memory," <http://www.physorg.com/news8524.html>
50. Samsung. "Samsung Introduces the Next Generation of Non-Volatile Memory – PRAM,"
http://samsung.com/PressCenter/PressRelease/PressRelease.asp?seq=20060911_0000286481
51. Kosuke Yanagidaira, Masumi Saitoh and Toshiro Hiramoto, "Enhancement of Charge Storage Performance in Double Gate Si NC Memories with Ultrathin Body Structure," IEEE, V26, N7, p473, 2005
52. S. Lombardo et al., "Multi-bit Storage through Si NCs Embedded in SiO₂", Microelectronic Engineering, 72, p411, 2004
53. D. Corso et al., "Programming Options for NC MOS Memories", Material Sci and Eng C 23, p687, 2003.

54. Lu, Alexe, Scholz, Taleaev and Zacharias, "Multilevel Charge Storage in Si Nanocrystal Multilayers", 87, 202110, 2005

Chapter 3: Market and Intellectual Property Analysis

As highlighted earlier, nanocrystal memory is considered as a potential replacement for conventional Flash Memory, which is expected to reach its scaling limits. Flash memory is currently the most dominant form of non-volatile semiconductor memory. It is used in diverse applications ranging from thumbdrives and Secure Digital Cards to Basic Input/Output System storage on computer mother boards. This chapter will give a brief overview of the current state of the Flash memory market and projections, existing and potential applications as well as a short description of competitor and intellectual property analyses.

3.1 Market Overview

The flash memory market was valued at \$10-16 billion in 2005. It is expected to reach \$18 to \$40 billion by 2010.¹⁻⁴ The traditional market for flash memory are diverse and different applications are implemented using NAND or NOR, depending on requirements of the particular application.

NAND Flash, which was designed with a very small cell size to enable a low cost-per-bit of stored data, has been used primarily as a high-density data storage medium

for consumer devices such as digital still cameras and USB solid-state disk drives. NOR Flash has typically been used for code storage and direct execution in portable electronic devices, such as cellular phones and PDAs. However, applications for NAND and NOR flash memories have become less distinct recently. For instance, new cell phone controllers support NAND Flash in addition to NOR. In addition, new phone models come with increased capabilities that incorporate video, pictures, music and games. These applications require low cost data storage as well as high speed write erase which makes NAND attractive for such purposes. Different types of memory are also stacked in Multi-Chip Packages (MCP) to create a component. For instance, NAND as the main memory can be stacked with dynamic random access memory (DRAM) which shadow runs the program code.⁶

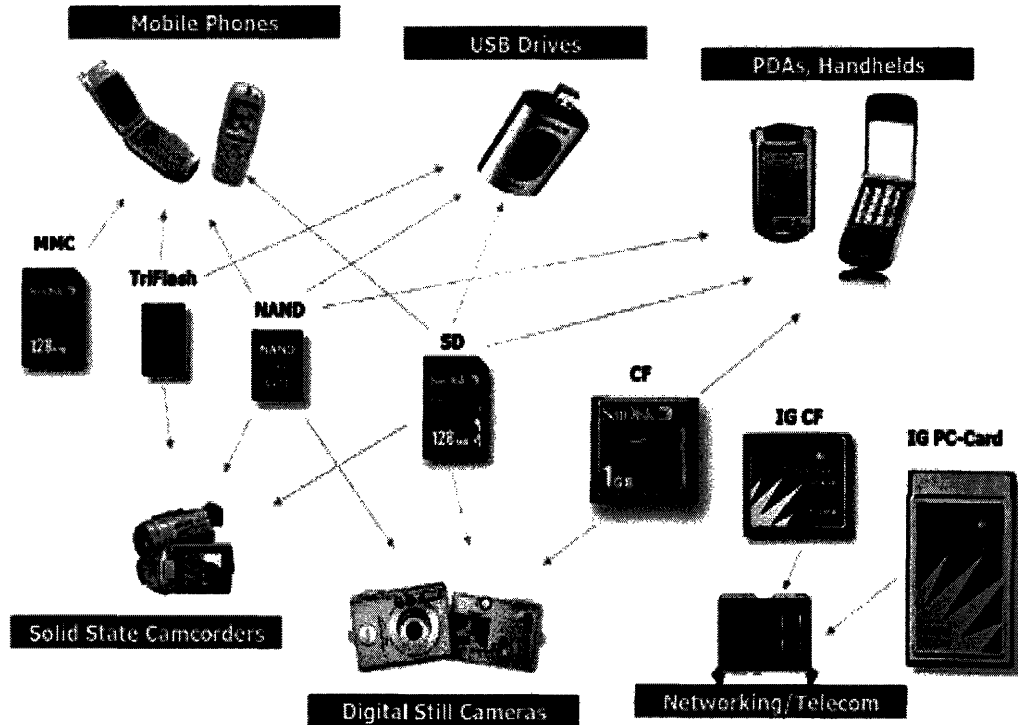


Figure 3.1: Some Applications for NAND Flash⁶

Figure 3.2 shows the breakdown of Flash sales in 2004 according to type as well as projections into 2010. Code flash refers to flash memory used to store executable code such as operating systems in communications or consumer electronics products such as Digital Video Disc players, computers. They usually have a fast read speed. Data flash are commonly used for high density storage such as digital camera cards and thumbdrives and have fast write speeds. Embedded flash combine flash with programmable logic. An example would be micro-controller embedded with memory. Serial flash memories such as those in VGA cards, wireless networking devices, usually have simpler interfaces, store only a few blocks of data and have a smaller form factor.⁷

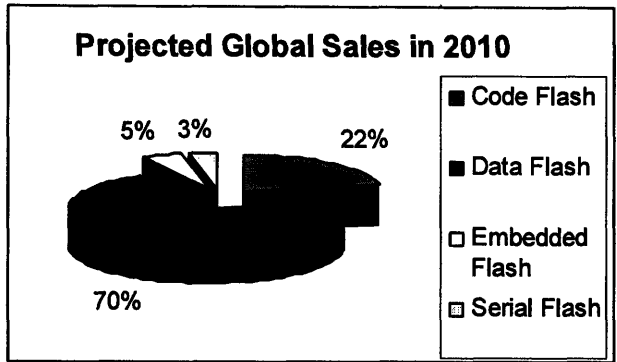
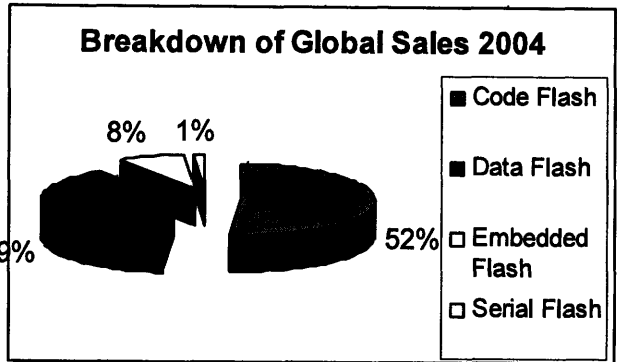


Figure 3.2: (Top) Breakdown of global sales of flash memory in 2004 (Bottom) Projected global sales in 2010. Embedded flash excludes revenue attributed to microcontroller, digital signal processor and/or programmable logic components of an embedded flash device⁷

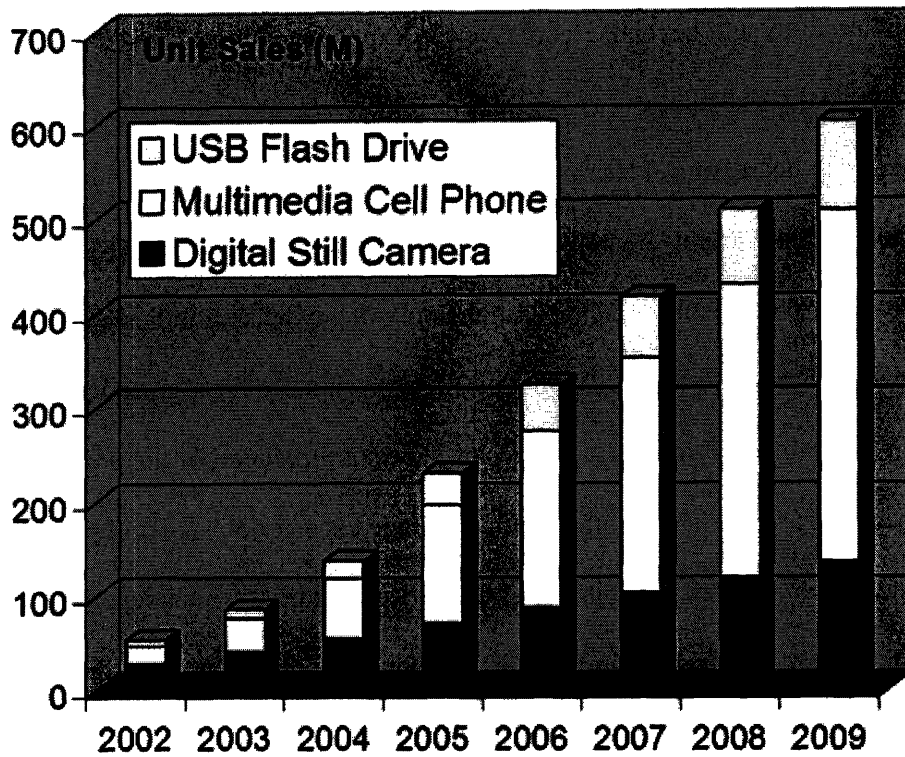


Figure 3.3: Projection of unit shipments of mobile electronic products with flash memory.⁶

3.2 Market Growth

Growth in the flash memory market is caused by two factors:

- 1) Strong demand in traditional flash memory applications, especially in data flash such as thumbdrives, camera cards and cell phone data storage. This is evident from Figure 3.2 and also from Figure 3.3. In Figure 3.2 the growth of data flash is so great than it dwarfs the growth of other segments of flash memory. From Figure 3.3, we can observe that the demand for such electronic products will

continue into 2009 and beyond. Hence, we can expect the demand for Flash will not dampen in the near future.

- 2) As prices keep decreasing, Flash memory has found applications in more areas. For instance, thumbdrives are replacing rewritable compact disks (CD-RW) in recent years. Projections from major flash memory manufacturers indicate that we may expect to see a street price decline of 30-40% annually for a given capacity and form factor of flash memory. Figure 3.4 shows a projection of the unit price of compact flash form factor storage with a storage capacity of 1 GB. Figure 3.5 shows the weighted retail price index of a 1 GB thumbdrive which supports the projection shown on Figure 3.4. There is an annual decline of 40% in the 1GB memory in the year 2006-2007 as illustrated in Figure 3.5.

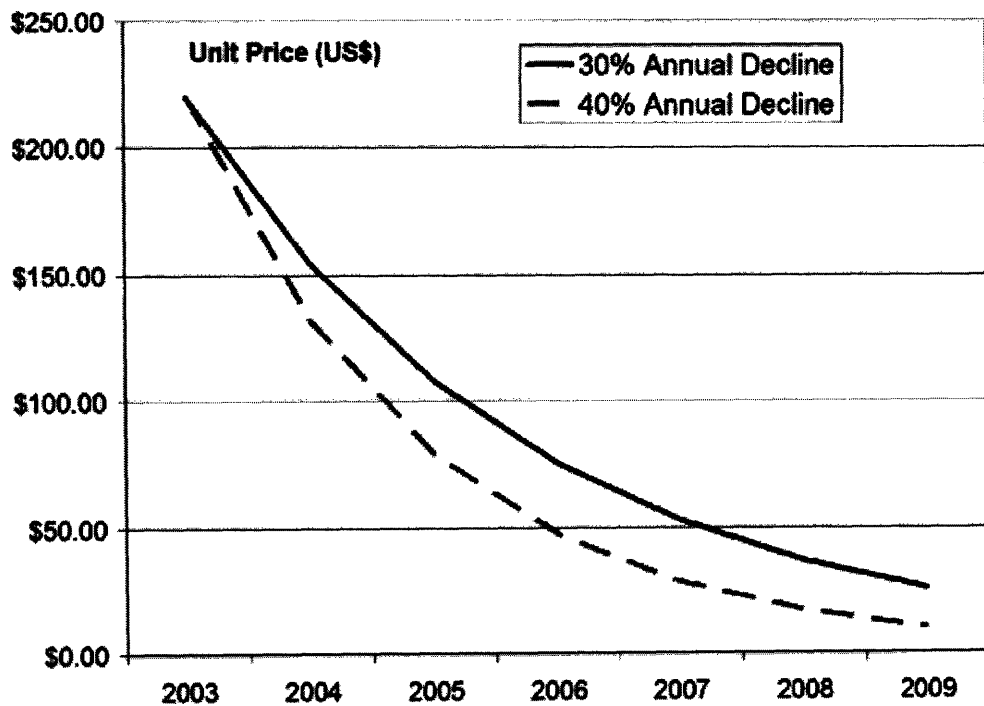


Figure 3.4: Projection of price of a 1 GB thumbdrive⁶

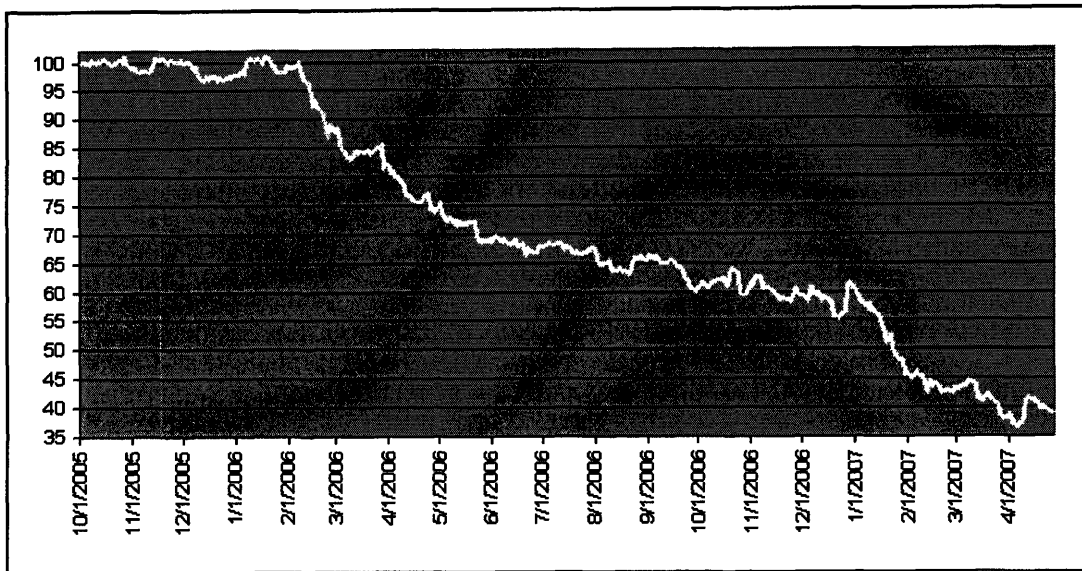


Figure 3.5: Price-weighted index comprised of the average retail price of 1GB Universal Serial Bus (USB) Flash Memory. The index is normalized to a base value of 100 as of October 1, 2005. The price index shows a 40% drop for a period of 1 year and a 65% drop for a period of 18 months⁸

Samsung has also recently announced the introduction of “flashtops”, laptops which use Flash memory for storage instead of the traditional hard disk.^{9,10} Traditionally, hard disks have much larger capacity and lower cost per megabyte compared to Flash memory. Figure 3.6 illustrates the cost per megabyte of storage for hard disk drives, dynamic random access memory, flash memory and paper/film. It is evident that hard disks offer the lowest cost for storage.¹¹ However, in recent years, the capacity of flash drives has increased tremendously. Even though the cost per megabyte of Flash is still higher than hard disks, consumers may be willing to pay a higher price for Flash memory based systems in exchange for superior performance. Flash based systems are able to read and write at much faster speeds and are more reliable due to the absence of mechanical

arms and spinning platters. They are also lightweight, have lower power consumption, and have lower heat dissipation.^{10,12} It is difficult to predict whether the cost per megabyte of flash-based systems will ultimately be lower than that of traditional hard disks or whether consumers will be willing to pay extra for the performance. There are advocates and detractors on both sides of the camp.⁹⁻¹⁵ However, there is one thing to be certain of- Flash memory is becoming a serious competitor to both optical and magnetic storage media.

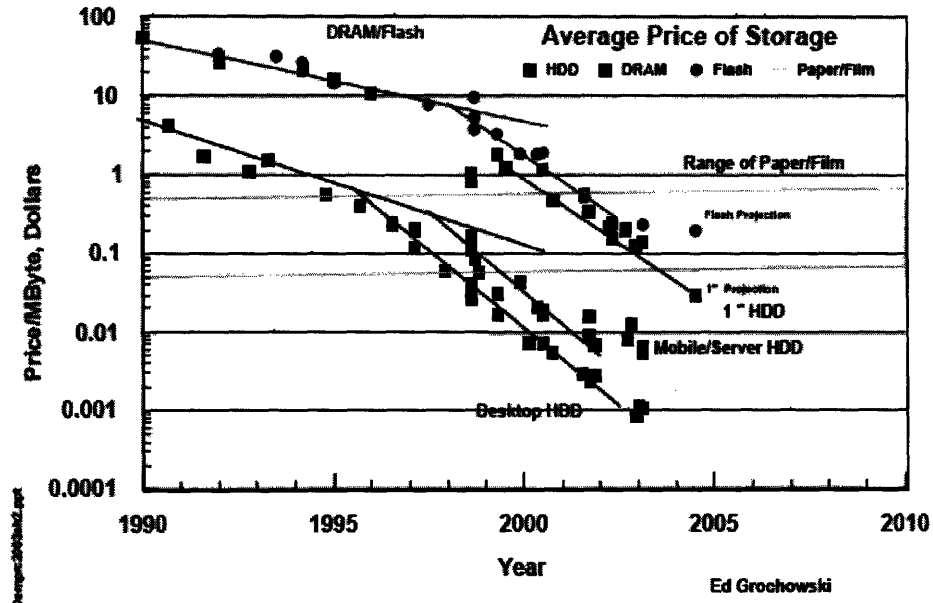


Figure 3.6: Price per megabyte of hard disk drives, dynamic random access memory, flash memory and paper/film¹¹

From the above, the market potential of Flash memory and its replacements seems bright. Growing demand for existing Flash applications as well as new applications for Flash as it matures will ensure that the whole Flash memory market will only grow bigger with time.

3.3 Competitors

With a pie that is worth about \$20 billion dollars currently and expected to get only larger in the future, it is not surprising that everyone wants a slice of it. As mentioned in Chapter 2 and 3, SONOS, MRAM, PCRAM, FeRAM and nanocrystal based memories are the major forerunners as successors to conventional Flash. There is also intense research being carried out on other technologies such as probe based memories, carbon nanotube based memories and molecular/organic switches, to name just some examples.¹⁶ Optical and magnetic storage manufacturers will also not be passive and will continue to improve their product attributes to compete with Flash-based systems.

Technology	Companies
MRAM	Freescale (Motorola), Cypress, Sony, IBM, Honeywell, Renesas, Micron, Infineon
PCRAM	Intel, Ovonyx, Samsung, ST Microelectronics, BAE Systems, Toshiba, Macronix, Renesas, Elphida, Sony, Matsushita, Mitsubishi, Infineon
SONOS	Freescale (Motorola), Phillips
Nanocrystal	Freescale (Motorola), IBM

FeRAM	Ramtron, Texas Instruments
-------	----------------------------

Table 3.1: Major memory technologies and companies with research on

3.4 Intellectual Property

Patent Number	Filing Date	Inventor	Claims
6962850	1 Oct 2003	Choi et al	Synthesis of germanium nc based Flash device by LPCVD/PECVD of silane, germane and ozone/nitrous oxide and RTA
6656792	1 Mar 2002	Choi et al	Synthesis of germanium nc based Flash device by cosputtering of insulator and germanium and RTA
5783498	28 May 1996	Achuyt Dotta	Synthesis of germanium nc films using APCVD of Si-based organic source, Ge-based organic source and ozone
7091130	25 June 2004	Rao et al.	Synthesis of memory device with poly-silicon nitride gate materials surrounding the nanocluster containing layer
6297095	16 June 2000	Muralidhar et al.	Synthesis of nanocluster containing memory device by nitriding the nanoclusters and tunnel oxide

6808986	30 August 2002	Muralidhar et al	Synthesis of nanocrystal for using silane and disilane (CVD)
6784103	21 May 2003	Muralidhar et al	Synthesis of nanocrystal on a semiconductor structure using silane and disilane (CVD)
6090666	30 September 1998	Ueda et al.	Formation of nanocrystal by heat treating amorphous thin films at pressures below atmospheric pressure
970500	29 January 1997	Forbes	Construction of floating gate meory using nanocrystalline silicon particles
5959896	27 February 1998	Forbes	Construction of multi state memory cell using semiconductor crystals
5714766	29 September 1995	Chen, Wei Smith, III, Teoren Perlee Tiwari, Sandip	Construction of memory device using semiconductor nanocrystals

Table 3.2: Selected patents relevant to fabrication of nanocrystal based memory devices

Table 3.2 shows a list of selected patents that are relevant to the fabrication of nanocrystal-based memory devices. Out of this list, patent 536510 describes the construction of a memory device using semiconductor nanocrystals without giving details of a fabrication process. The earliest patent that is filed pertaining to Ge nanocrystals

with a specific fabrication method is patent 5783498 using atmospheric pressure chemical vapour deposition (APCVD). Prof. Choi's patents describe the fabrication of Ge nanocrystals using low pressure chemical vapour deposition/ plasma enhanced chemical vapour deposition (LPCVD/PECVD) (patent 6962850) as well as co-sputtering (6656792). The patents utilized by Freescale Semiconductors in their fabrication of silicon nanocrystal memory device include 6297095, 6808986 and 6090666 by Muralidhar et al.

3.5 Market and Intellectual Property Analysis Conclusion

In Chapter 3, we have analyzed the Flash memory market as well as competition and intellectual property issues. Although the Flash memory market looks set to grow in the next few years, Ge-nanocrystal-based memories face stiff competition from other nanocrystal based memories, other technologies such as phase change memory and magnetic random access memory as well as optical and magnetic data storage. From the intellectual property analysis, we can see that no one has a monopoly and different patents with different fabrication methods are held by different people. It is thus difficult to erect a barrier to prevent others from manufacturing similar products. Any profit gained from successful commercialization will induce others to produce similar products. In addition, as there is no unique way, one-way-to-do-it path, it is extremely difficult to start a purely intellectual property (IP) company based on the existing patents.

References

1. Yun Seung Shin, "Non-volatile memory Technologies for Beyond 2010," 2005 Symposium on VLSI Circuits Digest of Technical Papers, 2005
2. Simon Burns, "Flash Memory Market Expected to Pass \$20 billion by 2010," <http://www.vnunet.com/vnunet/news/2153180/flash-memory-market-pass-20bn>
3. May Wong, "Storage Demands Flash Memory Industry," http://www.usatoday.com/tech/products/2006-06-04-storage-drive_x.htm
4. Ann Steffora Mustchler, "Intel to Help Grow Non-volatile Biz to \$40B by 2010," <http://www.edn.com/article/CA6422449.html>
5. Toshiba, "NAND vs NOR Flash Memory Technology Overview," http://www.toshiba.com/taec/components/Generic/Memory_Resources/NANDvsNOR.pdf
6. Thomas M. Coughlin, "Moving at the Speed of Flash," <http://www.mobiletrax.com/im/2004archives/20040202.html>
7. Seeking Alpha, "Overview of Flash Memory Technology and Market," <http://ce.seekingalpha.com/article/5346>
8. priceSCAN, http://www.pricescan.com/indices/1GB_USB_Flash_Memory_Index.asp
9. Robert Jaques, "Sumsung Moves NAND into Mobiles PCs," vnunet.com, http://www.vnunet.com/vnunet/news/2152446/samsung-moves-nand-flash?vnu_lt=vnu_art_related_articles
10. Chris Preimesberger, "Hot Flash: 'Flashtops' Take on the Memory Market," eWeek.com, <http://www.eweek.com/article2/0,1895,2008089,00.asp>

11. Hitachi, "Hard Disk Drives Overview Charts,"
<http://www.hitachigst.com/hdd/technolo/overview/chart03.html>
12. Wilson Wei Sheng Wang and Joanne De Peralta, "War of the Disks: Hard Disk Drives vs Flash Solid State Disks," <http://www.storagesearch.com/bitmicro-art3.html>
13. Zsolt Kerekes, "Squeak!- Why Are Most Analysts Wrong About Solid State Disks," <http://www.storagesearch.com/ssdmarketmodelupdate.html>
14. Michael Kanellos, "Bye-bye Hard Disks, Hello Flash," Cnet News.com
http://news.com.com/Bye-bye+hard+drive,+hello+flash/2100-1006_3-6005849.html
15. Newsmaker Q&A, "Hard Drives: No Flash in the Pan." Business Week,
http://www.businessweek.com/technology/content/sep2005/tc20050927_1608_tc057.htm
16. Betty Prince, "Trends in Scaled and Nanotechnology Memories," unpublished
17. Michael Kanellos, "Is Flash Fried?", Cnet News.com,
http://news.com.com/Flash+forward/2009-1040_3-994240.html
18. John G. Spooner, "Motorola To Outline New Flash Technology", Cnet News.com,
http://news.com.com/Motorola+to+outline+new+flash+technology/2100-1040_3-983685.html
19. IBM, "IBM Demos New Nanotechnology Method to Build Chip Components,"
http://domino.watson.ibm.com/comm/pr.nsf/pages/news.20031208_selfassembly.html

20. Wikipedia, <http://www.wikipedia.org/>

Chapter 4: Cost Modeling

In this Chapter, we will attempt to analyze some of the ways in which nanocrystal technology can be commercialized. First of all, we will look at some of industry trends in chip fabrication. Next we will do up a cost model to compare the average costs between nanocrystal memories to conventional flash as well as phase change memories.

4.1 Chip Industry Trends

The flash memory industry as well as the semiconductor industry in general is well known for prohibitive costs of setting up a plant as well as relatively low profit margins. The costs of setting up a wafer fabrication plant can come up to a few billion dollars.^{1,2} From Figure 4.1 it can be seen that the cost of a Fab has been increasing exponentially over the years. At the same time, capital costs per unit output has been decreasing, indicating productivity gains. Another measure of Fab affordability is to compare the cost of a Fab to the size of the overall semiconductor industry. In 1960 the average Fab cost represented 0.125% of the total industry revenue, by 2000 the latest 300mm Fabs have reached 1.28% of total industry revenue. As linewidths shrink, it also becomes more expensive to purchase the necessary equipment. Figure 4.3 shows the average cost of an exposure system over the years. Lithography systems used to cost around \$10,000. Now, a state-of-the-art Extreme Ultra Violet (EUV) system can cost up

to \$100,000,000.³ Variable costs, such as raw material costs, electricity costs and labour costs, take up a relatively small proportion of the total unit cost.

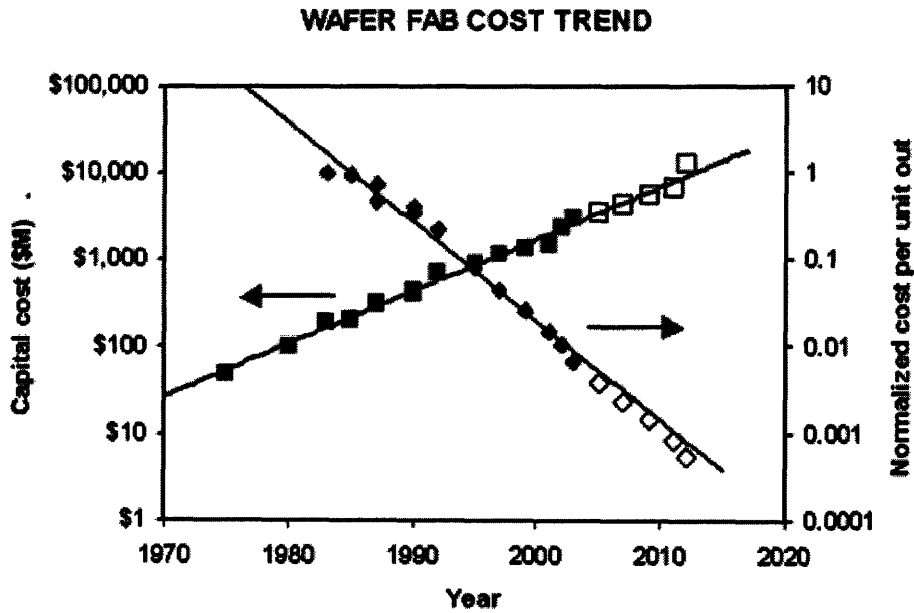


Figure 4.1: Capital costs and normalized cost per unit output over the years²

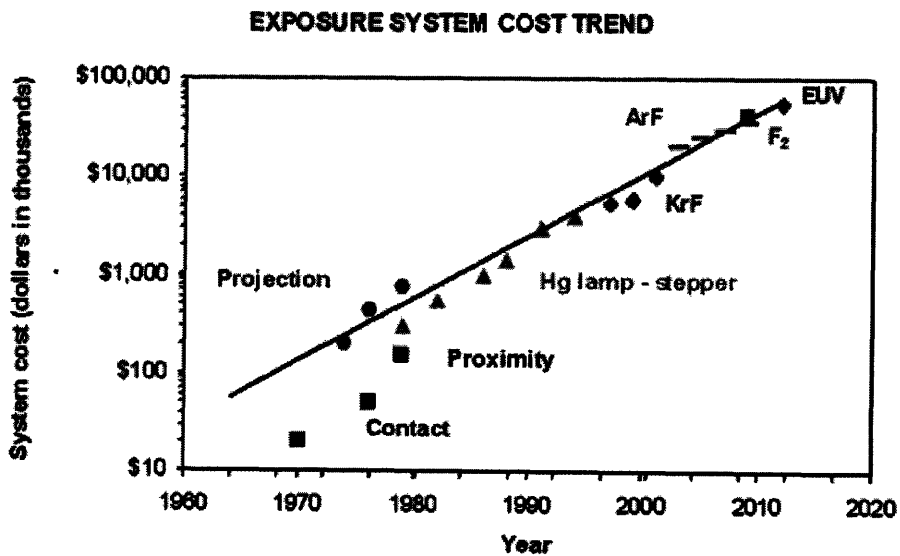


Figure 4.2: Exposure system cost trend³

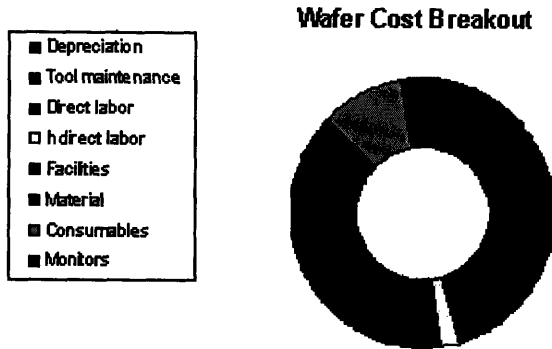


Figure 4.3: Wafer cost breakdown for a 300mm logic wafer. Much of the costs come from depreciation of building and equipment costs, followed by costs of raw materials and other consumables⁴

The high fixed costs and low variable costs tend to give rise to a monotonically decreasing average cost curve as shown in Figure 3.3. Total fixed costs are independent of actual production volume while total variable costs scales with production volume.

$$\text{Average Fixed Costs} = \frac{\text{Total Fixed Costs}}{\text{Production Volume}}$$

$$\text{Average Variable Costs} = \frac{\text{Total Variable Costs}}{\text{Production Volume}}$$

$$\text{Total Average Costs} = \text{Average Fixed Costs} + \text{Average Variable Costs}$$

At a low volume of production, the high fixed capital costs are shared between relatively few outputs, leading to decreasing average fixed costs. Average variable costs stay the same, independent of production volume. This gives rise to high average costs

per unit of production.

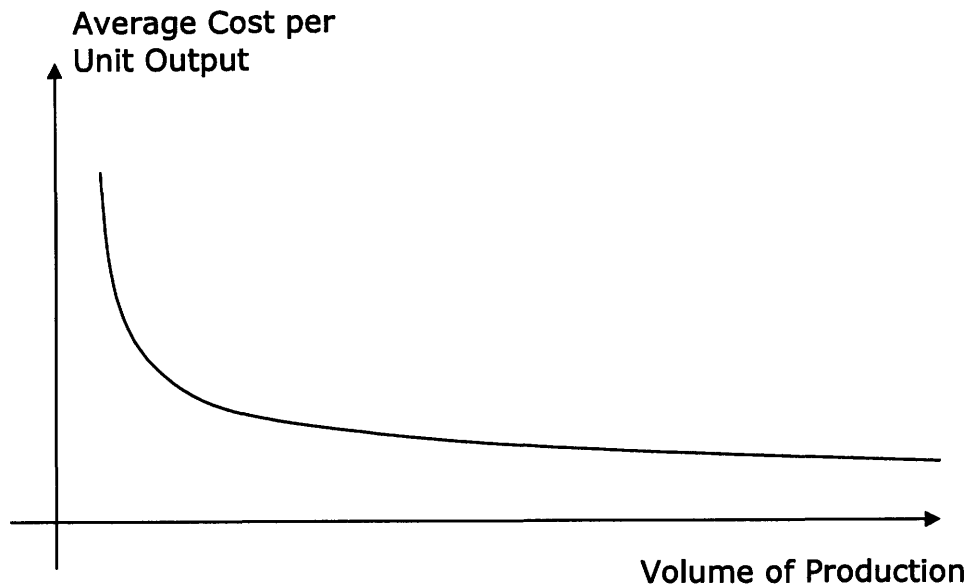


Figure 4.4: Average cost curve of a typical Flash manufacturer.

At high production outputs, the astronomical fixed costs are shared by large outputs. This leads to lower average costs. From the curve shown, we can expect manufacturers to produce as far to the right of the curve as possible to enjoy economies of scale reflected by lower prices. This leads to a natural monopoly in which new firms entering the industry will face high average costs as their volume of production is small and incumbent firms enjoy great economies of scale. Hence, it is not surprising to find the flash industry being dominated by a few major players. From Table 4.1, we can see that above 80% of the market is dominated by 5 companies. The flash memory industry is ruthless, especially to small companies. In order to lower per-unit cost while dealing with looming capital costs and aggressive competition, companies are forced to become more efficient and innovative in order to survive.

Company	Revenue (millions US \$)	% Market Share
Samsung	1376	33.3
Toshiba	614	14.8
Intel	528	12.8
Spansion	475	11.5
ST Microelectronics	295	7.1
Others	884	20.5
Total	4132	100

Table 4.1: 2005 Rankings Top Suppliers of Flash Memories⁷

4.2 Cost Model of Building a Fabrication Plant

<i>No of Masking Steps in Basic CMOS Process</i>	26
<i>No of Additional Mask Adders for Nanocrystal Memory</i>	4
<i>No of Additional Mask Adders for Conventional Flash Memory</i>	11
<i>No of Additional Mask Adders for Phase Change Memory</i>	5
<i>Capital Cost of Equipment per Masking Step</i>	\$10.5 million
<i>Process Cost per Layer per Wafer</i>	\$1.25
<i>Reticle Costs</i>	\$15,000

<i>Reticle Life</i>	<i>5000 wafers per reticle</i>
<i>Wafer Costs</i>	<i>\$150</i>
<i>Building and Land</i>	<i>\$2 billion</i>
<i>Accounting Life of Machine</i>	<i>10 yrs</i>
<i>Amortization Life of Building and Land</i>	<i>20 yrs</i>

Table 4.2: Parameters used in cost analysis⁸⁻¹¹

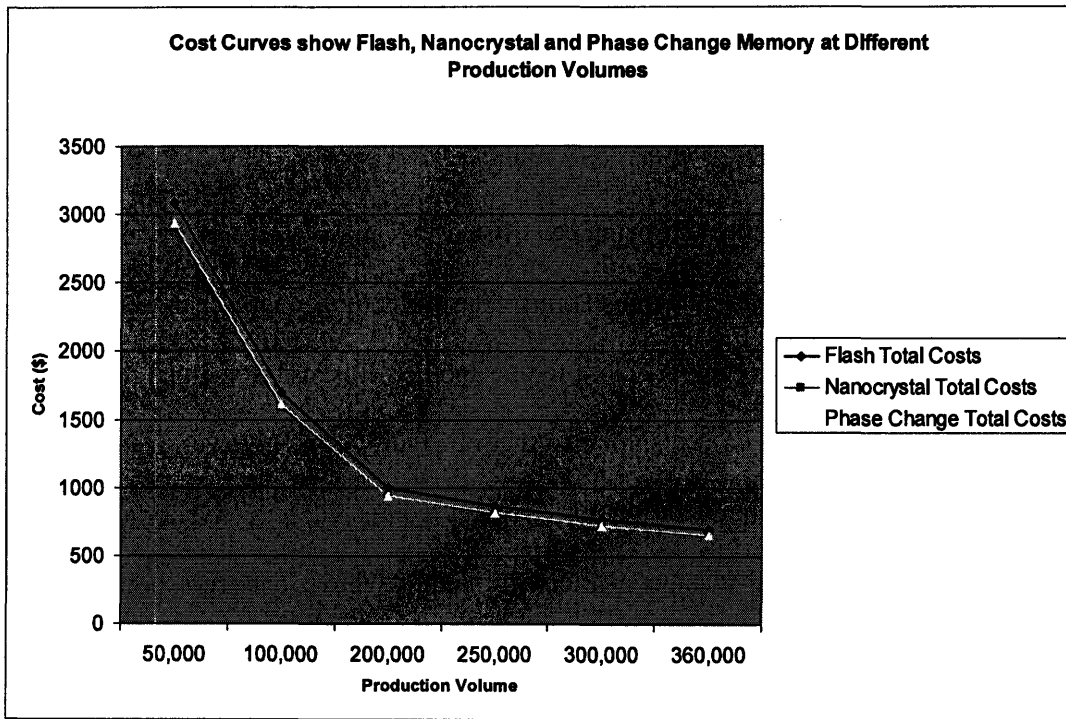


Figure 4.5: Simulated cost curves for plant with annual production of 360,000.

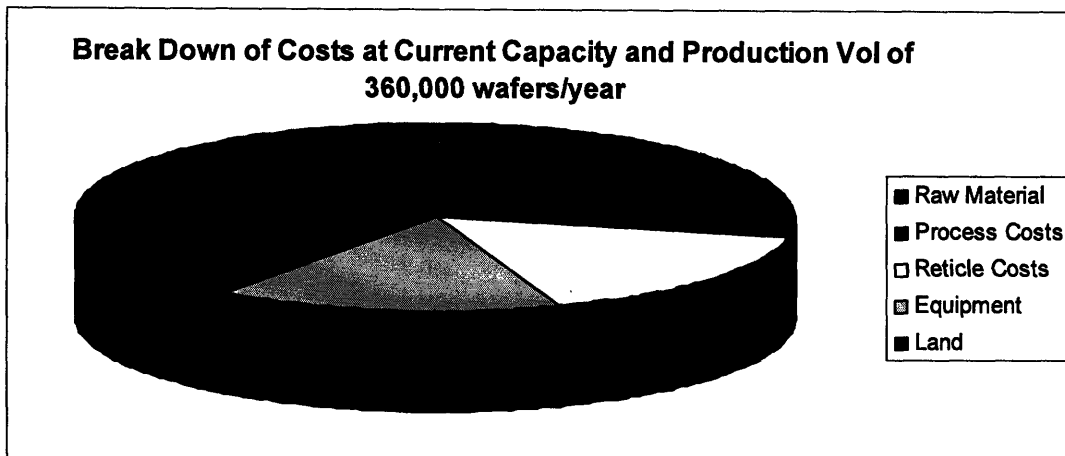


Figure 4.6: Simulated Breakdown of costs for a plant with capacity and annual production of 360,000 wafers per annum

A cost model was built with parameters listed in Table 4.2. It can be seen from Figure 4.5 that the cost curves for conventional Flash memory, phase change memory and nanocrystal memory are relatively close to one another. It is also noted that the shape of the cost curves in Figure 4.5 are similar to that of Figure 4.4. However, nanocrystal memories still enjoy some amount of cost savings compared to conventional flash memory. The cost of phase change memory is slightly above nanocrystal memory. Hence, nanocrystal memories enjoy some advantages in terms of costs in the aggressive memory industry.

4.3 Cost Modeling Conclusions

The flash memory industry has high barriers to entry. New entrants suffer prohibitive fixed costs. New entrants are also unable to compete with the dominant

players as their volume of production is lower. The flash memory industry is very competitive. Comparing nanocrystal memories with conventional flash and phase change memories, nanocrystal memories enjoy some cost savings due to fewer mask adders required.

References

1. David Manners, "The Price of 300mm- Wafer Fab- Industry Trend or Event,"
Electronics News,
http://findarticles.com/p/articles/mi_m0EKF/is_09_46/ai_59778714
2. IC Knowledge, "Can the Semiconductor Industry Afford the Cost of New Fabs,"
http://www.icknowledge.com/economics/fab_costs.html
3. Scotten W. Jones, "A Simulation Study of the Cost an Economics of 450mm
Wafers," Semiconductor International, <http://www.reed-electronics.com/semiconductor/article/CA632496>
4. IC Knowledge, http://www.icknowledge.com/economics/300mm_costs.html
5. MZ Zander, "Roadmap of Energy Consumption and Energy Saving Concepts in
the Semiconductor Industry" http://www.mw-zander.com/energy_consumption_and_energy_saving_concepts_in_the_semiconductor_industry_0.pdf
6. Sean Cusack, Eiji Takizawa and Joyce Tam, "Czochralski Growth of Silicon
Wafer," University of Pennsylvania.
7. iSuppli Corps, <http://i.cmpnet.com/siliconstrategies/2005/07/nanoflash.gif>

8. Dr Vincent Ho, Process Integration Engineer, Chartered Semiconductors, private communications.
9. Mr Chin Khee Yeap, Process Engineer, Tech Semiconductors, private communications.
10. Betty Prince, "Trends in Scaled and Nanotechnology Memories," Memory Strategies International, IEEE, 2005
11. Lyoyd C. Litt, "The Price of Success: The Cost of Lithography for the 13nm Node", http://www.future-fab.com/documents.asp?grID=213&d_ID=1156#
12. Samsung. "Samsung Introduces the Next Generation of Non-Volatile Memory – PRAM,"
http://samsung.com/PressCenter/PressRelease/PressRelease.asp?seq=20060911_000286481

Chapter 5: Conclusion

Germanium-based nanocrystal memory has been shown to have the potential to replace conventional Flash memory. However, it faces serious competition from other types of technologies. Phase change memory in particular poses a serious threat to nanocrystal memory as it is backed by major flash manufactures such as Samsung. Use of diodes instead of transistors will enable phase change memory to scale past the position of conventional flash memory. In order for nanocrystal memories to compete with phase change memory, continual research is essential. Retention time and other attributes such as programming speed and voltages can be improved by trap level engineering, removal of interfacial states at SiO_2/Si interface, use of heteronanocrystals and novel schemes such as double gate nanocrystal memory structures. A larger number of bits stored per transistor can also be realized by using the discrete traps and multi-level schemes.

The commercialization of this technology is also hampered by similar patents held by different companies/individuals. It is thus difficult to erect a barrier to prevent others from manufacturing similar products. Any profit gained from successful commercialization will induce others to produce similar products. For a company to specialize in producing nanocrystal memory, it is crucial for the company to build up a portfolio of patents, especially improvements on nanocrystal memories. With that, the company can compete with other companies advocating phase change memory. According to the cost models, the costs of manufacturing nanocrystal memories are

slightly lower than that of conventional flash or phase change memories. This might prove to be an advantage of nanocrystal memory.