Energy Efficient Ultra-Wideband Radio Transceiver Architectures and Receiver Circuits

by

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S.B., Massachusetts Institute of Technology (2002)
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Abstract

Energy efficient short-range radios have become an active research area with proliferation of portable electronics. A critical specification for radio efficiency is energy/bit. The FCC has allocated the 3.1–10.6 GHz band for radios using ultra-wideband (UWB) signals. In this research, I exploit UWB signaling to develop energy efficient hardware systems for high and low data rate radios.

In the high rate regime, a modular discrete prototype receiver is developed to observe pulsed UWB signals. Verification of system non-idealities upon bit-error-rate (BER) are easily observed with this system. The results are leveraged in designing a 3.1–10.6 GHz front-end in a 0.18 μm SiGe BiCMOS process, featuring an unmatched LNA and 802.11a switchable notch filter for interference mitigation. A 100 Mbps system demo is implemented to realize a wireless link.

In the low rate regime, energy/bit increases because fixed power costs are less effectively amortized over fewer bits/sec. However, by using UWB PPM signaling, the receiver is duty-cycled so that energy/bit is decoupled from data rate. Through careful signaling, system, and circuit co-design, a non-coherent, 0–16.7 Mbps receiver is implemented in a 90 nm CMOS process with a 0.5 V and 0.65 V power supply. This work achieves 2.5 nJ/bit of energy efficiency over three orders of magnitude in data rate. With adjustable bandpass filters and a new relative compare demodulator, the receiver achieves 10^{-3} BER with -99 dBm sensitivity at 100 kbps. A first-pass acquisition algorithm is developed on an FPGA platform and a transceiver system demo is assembled using this chip.

Thesis Supervisor: Anantha P. Chandrakasan
Title: Professor of Electrical Engineering and Computer Science

"The Word became flesh and made his dwelling among us.
We have seen his glory, the glory of the One and Only,
who came from the Father, full of grace and truth." - John 1:14

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And ultimately, I thank God for his undeniable hand upon my life. If I did not have your holistic guidance, life would not be as incredibly rich as it has been. I am humbled and thankful... and praising you through the "random gasps of joy attacks" when I remember that this thesis is finally done. =D Wooo Hoo!!

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Chapter 1

Introduction

An overview of wireless communications focusing on pulse-based communications development is discussed in this Chapter. The present day FCC-compliant ultra-wideband (UWB) signaling environment and known implementation challenges are described to introduce the key contribution of this thesis: utilizing UWB signaling to realize energy efficient communication systems at high and low data rates.

1.1 History of UWB Radio Development

In 1893, Heinrich Hertz used a carrier-less pulse generated by a spark discharge to verify the existence and propagation characteristics of electromagnetic waves as predicted by Maxwell's equations [6]. This historical experiment is classified as the first "radio" as we know of today. Expanding upon Hertz's work, Marconi demonstrated the first transatlantic wireless communications link in 1901 using a similar spark-gap pulse signal modulated-in-time by Morse-code to encode data [7]. Though wireless communications began with wideband pulsed signals, the lack of frequency control and non-existence of a MAC protocol for interference mitigation from other spark-gap transmitters caused these radio pioneers to turn towards more manageable narrow-band systems to achieve wireless communications. Quickly thereafter, new receiver architectures such as the regenerative receiver, the superheterodyne receiver, and superregenerative receiver were invented – all to the credit of radio pioneer Edwin

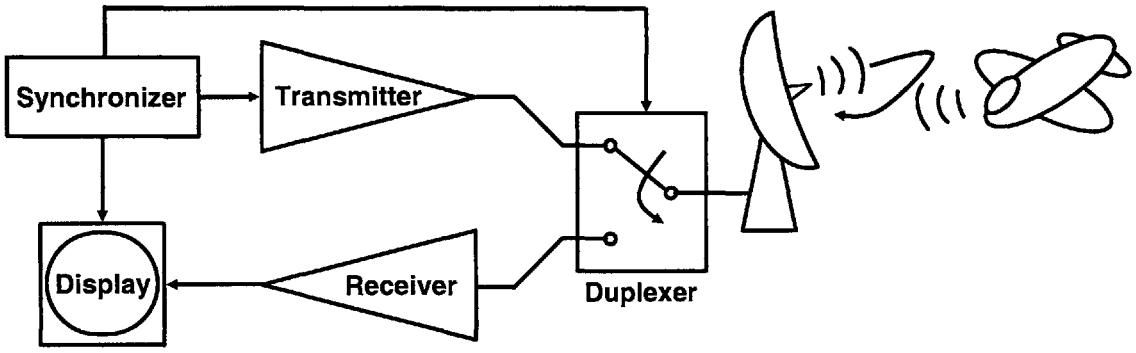


Figure 1-1: Radar system.

Armstrong [6].

Though radio communications development turned towards perfecting narrowband systems, the military continued to fund work developing radar technology based on wideband signals. Purdue University, Bell Labs, MIT, and University of Chicago were among the many institutions that made this technology available during World War II [8]. Figure 1-1 is a block diagram of a radar system. A high-energy pulse is sent from the transmitter, and a directional antenna guides the pulse. When the pulse strikes a reflective object, the pulse is dispersed and energy returns to the radar system at the same propagation velocity. The receiver demodulates the AM pulse signal using a diode rectifier and the baseband pulse is recovered. Since the propagation time of an electromagnetic signal in free space is $t = m/c$ (where t is in seconds, m is in meters, and c is the propagation velocity of electromagnetic waves – the speed of light), the radar system is able to calculate the distance spanned by the pulse. Also, basic information on the reflector material is embedded in the reflected pulse shape [8].

During operation, the radar system is completely synchronized since the transmitter and receiver use the same timing reference. Sensing begins when the transmitter sends a pulse through the antenna, and the receiver waits for $t_{min} = 2 \cdot m_{min}/c$ (the minimum round-trip scanning time) before switching the duplexer from the transmitter to the receiver. The synchronizer waits until $t_{max} = 2 \cdot m_{max}/c$ (the maximum round-trip scanning time), before initiating the sensing operation over again. The

pulse repetition frequency and transmit power set the maximum measurable distance. Immunity to noise and interference can be improved as additional pulses are integrated per scan angle; however, this reduces the scanning speed.

In the late 1960's, HP developed the sampling oscilloscope which enabled detailed evaluation and measurement of sub-ns pulse signals and transient responses of high speed circuits [9]. Due to the improved measurement equipment, pulse-based "impulse radio" communications and its associated hardware development became an active area of research once again. In 1973, Dr. Gerald F. Ross was awarded the first US patent for a UWB communications transceiver system [10]. Soon after, the US Department of Defense first coined the term "ultra-wideband radio," to describe impulse radio systems.

In 2001, interest for using UWB signals in communications came to a critical juncture which sparked the FCC to release 7.5 GHz of unlicensed spectrum in the 3.1–10.6 GHz band for the development of UWB radios [1]. Since this ruling, there has been a great effort by industry and research institutions alike to harness this new resource. System level advantages of UWB signaling over traditional narrowband radio signals include exploiting the increased timing resolution requirements of processing UWB signals for locationing and tagging applications [11, 12], biomedical imaging [13], and energy efficient data communications [14, 15, 16]. However, there are also challenges in implementing UWB wireless systems [17]. The following overview of the UWB signaling environment discusses these issues from a system perspective.

1.2 UWB Signaling Environment

UWB is meant to be an overlay technology to existing narrowband radios and appears "noise-like" to those systems. However, for extremely sensitive technologies such as GPS, a notch in the UWB spectral mask (Figure 1-2) suppresses interference upon those systems [18].

Although the FCC limits for UWB transmission have been carefully engineered to avoid interference upon existing narrowband receivers, there are no provisions to

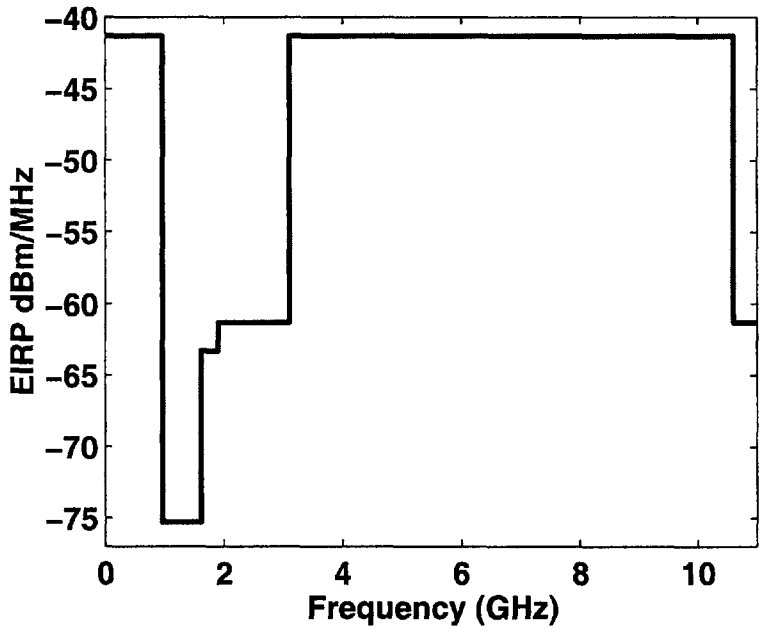


Figure 1-2: FCC issued UWB spectral mask [1].

guarantee that in-band narrowband transmitters do not saturate UWB receivers. Furthermore with such large bandwidths, the channel model diverges from a simple gain correction to a complex multi-path problem. The system must be designed with a sensible combination of signaling scheme, architecture, linearity & noise figure (NF) specifications, and solution to multi-path effects so that it can achieve a desired quality-of-service (QoS) for a given sensitivity, power constraint, and data rate. To begin, it is important to understand how narrowband signals, both in and out of band could potentially saturate or disturb the UWB receiver front-end, and models of typical UWB channels.

1.2.1 Narrowband Blockers

For narrowband radios below the UWB spectrum, it is possible for these systems to excite the non-linearities of the LNA and thereby create harmonics at integer multiples of the fundamental frequency within a block of frequency where the receiver expects a UWB signal. If there is insufficient filtering and band selection before the LNA, the amplifier itself could become saturated.

Within the 3.1–10.6 GHz band, 802.11a signals come in at two bands between 5–6 GHz. In the 5.725–5.825 GHz band, the 802.11a signal appears with a spectral density of 16 dBm/MHz. Also, the UWB receiver must also be robust to a "random frequency" in-band interferer that is transmitting at an assumed power level. The 802.15.3a effort, considered 0 dBm as the average power of such a signal [19].

1.2.2 Channel Models

Some key points of a channel model are in knowing the path loss, the average delay spread of the multi-path components over many different channel conditions, and the power decay profile. Within the IEEE 802.15.3a and 4a efforts, there are many mature models of what a typical UWB channel may look like.

The equation for the path loss of a UWB signal is as follows [20]:

$$PL(d) = PL_0 + 10 \cdot \gamma \cdot \log_{10}(d/d_0) + S \tag{1.1}$$

where

$$PL_0 = 10 \cdot \gamma \cdot \log_{10}\left(\frac{4 \cdot \pi \cdot d_0 \cdot \sqrt{f_{lo} \cdot f_{hi}}}{c}\right). \tag{1.2}$$

Usually the reference distance d_0 is chosen as 1 m. f_{lo} and f_{hi} represent the -3 dB bandwidth of the UWB signal. c is the speed of light in m/sec. S represents the shadowing factor of the channel, which is zero-mean Gaussian random variable, and represents the deviation of PL_0 from its nominal value. Finally, γ represents the severity of path loss. For line-of-sight, γ is measured to be 2, and can grow to be as large as 3.34 for non-line-of-sight measurements. For short distances, it is possible to utilize the entire UWB bandwidth for data transmission, but for larger distances, it is more difficult to achieve a high quality link across the entire band as the path loss becomes significant at higher frequencies. Figure 1-3 shows the path loss over different values of γ vs. frequency.

From the 802.15.3a task group, Figure 1-4 shows a set of 100 measured channel impulse responses [21][2]. These channel models are based on measurements taken

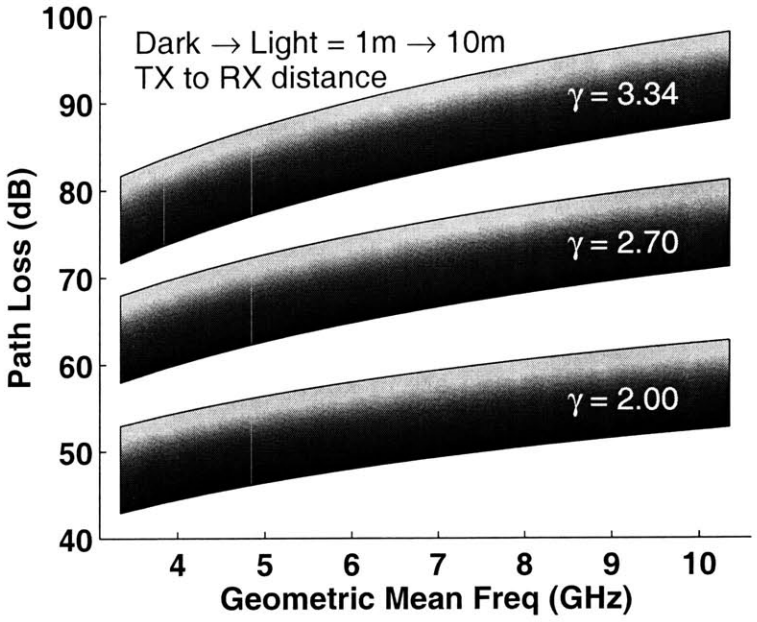


Figure 1-3: Signal loss from 1 m to 10 m paths at different values of γ.

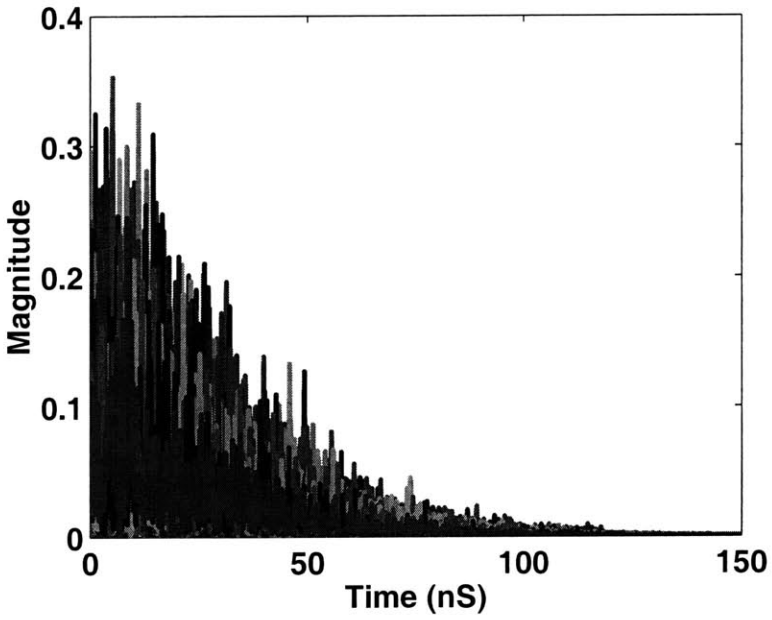


Figure 1-4: 802.11.4a channel responses of a typical office environment [2].

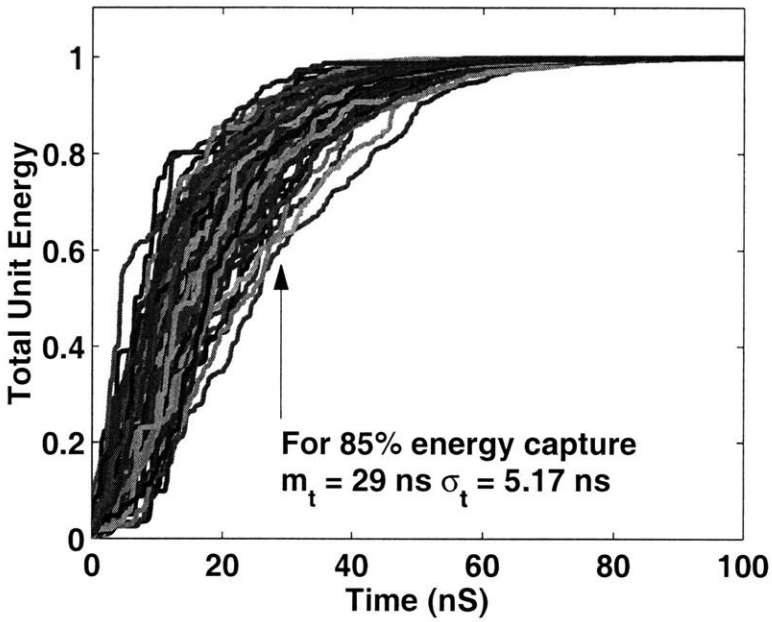


Figure 1-5: Sum of channel energy vs. time.

in a non-line-of-sight indoor office environment, with typical propagation distances of 4–10 m. The average RMS delay for this particular channel is 14.28 ns. The average time, m_t, for 85% channel power capture is shown in Figure 1-5. From the 3a and 4a efforts, the expected range of average RMS channel impulse response delay varies from 5.28 ns to 89 ns.

1.3 Receiver Architecture

Because of the wideband nature of UWB signals, direct-conversion architectures are more suitable for UWB receivers (Figure 1-6). This assertion is motivated through a simple analysis of the filtering needs of a non-direct conversion, heterodyne architecture (Figure 1-7). This exercise quickly reveals the impracticalities of utilizing an IF frequency and building the sharp roll-off anti-alias filter for such a system. Image-reject architectures may alleviate filtering needs, but they become more difficult to implement as bandwidth increases, as gain and phase errors across very large bandwidths become unwieldy to control.

However, large signal bandwidths have advantages in a direct-conversion architec-

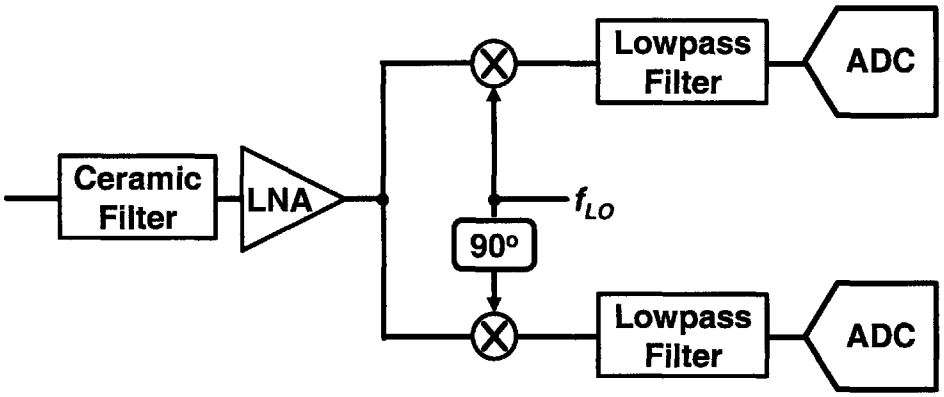


Figure 1-6: Direct-conversion receiver architecture.

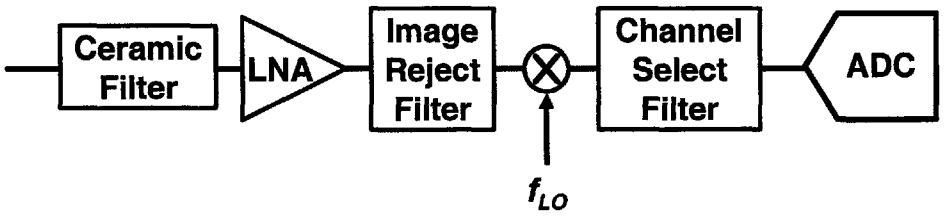


Figure 1-7: Heterodyne receiver architecture.

ture. The large bandwidth allows more flexibility in mitigating DC offsets, relaxed constraints for $1/f$ noise, and affords the lowest possible analog-to-digital converter (ADC) Nyquist rate. All of these contribute to reducing the overall UWB receiver power consumption, relative to a heterodyned architecture.

As for processing baseband UWB signals, a critical design choice is in how much back-end processing should be done in the analog or digital domain. Generally, as the ADC is moved towards the digital end, the sampling rate requirements tend to decrease, but as do flexibility and programmability. The reverse occurs when the ADC is moved towards the analog domain. When energy is the key metric, there are situations where flexibility must be sacrificed in order to reduce power consumption.

1.4 UWB Signal Choice

The FCC has specified that UWB signals must have a minimum continuous signal bandwidth of 500 MHz, a spectral mask of -41.3 dBm/MHz within the 3.1–10.6 GHz bandwidth, and a peak power limit that cannot be exceeded. As shown in Figure 1-2, the spectral mask is severely attenuated for signals outside the 3.1–10.6 GHz band. Two important design choices for UWB signals are bandwidth and modulation type.

1.4.1 Bandwidth

The impact of signal bandwidth upon the digital back-end receiver complexity is significant. With increasing signal bandwidth, the digital back-end requires a faster sampling rate ADC. Furthermore, the digital back-end also increases in power consumption, because increasing the signal bandwidth translates to increasing the digital activity. Specifically, the required switching energy in the digital back-end, clock/data routing, and I/O is likely to dominate that of the analog/RF energy consumption. For more complex signaling constellations, increased ADC resolution is required. Like increasing sampling rate, increasing the ADC resolution also affects all the blocks downstream from – and including – the ADC.

Practically, a larger signal bandwidth causes the analog/RF front-end to be more

susceptible to saturation because it would subject it to a larger set of possible in-band interferers. A solution to this would be to increase linearity, but to do so usually comes at the cost of higher power consumption in the LNA and front-end circuits.

A reasonable method to avoid over-design for a high data rate UWB system is to specify the minimum data rate and desired transmission distance required by the system, and choose the bandwidth at which the data rate is achievable. In this way, the receiver is operating at the minimum required bandwidth while meeting specification and being optimally configured for interference robustness and low power.

1.4.2 Modulation

This section discusses two mainstream UWB modulation schemes: orthogonal-frequency-division-multiplexing (OFDM) and pulse-based signaling.

OFDM

OFDM takes a band of frequency and divides it into orthogonal sub-carriers whose center frequencies are equally spaced. The sub-carriers are simultaneously and individually modulated by data, and the entire frequency band is transmitted at once. The main feature of OFDM signaling is the ease at which multi-path can be dealt with using a cyclic prefix, and the simplicity in which modulation and demodulation can be performed with an IFFT and FFT, respectively. In narrowband radio, OFDM has been adopted in the deployment of 802.11a/g, and is now being considered for WiMAX and UWB's WiMedia industrial group. However, some disadvantages of using OFDM are that it increases the complexity of the transmitter and of the receiver linearity requirements relative to a pulse-based UWB transceiver.

Pulse-based

A pulse-based receiver is more similar to the original intention of UWB as an "impulse radio." It consists of a baseband pulse generator and up-converter. Plots of a 3.1–3.6 GHz and a 3.1–10.6 GHz Gaussian pulse are shown in Figure 1-8. As can be seen,

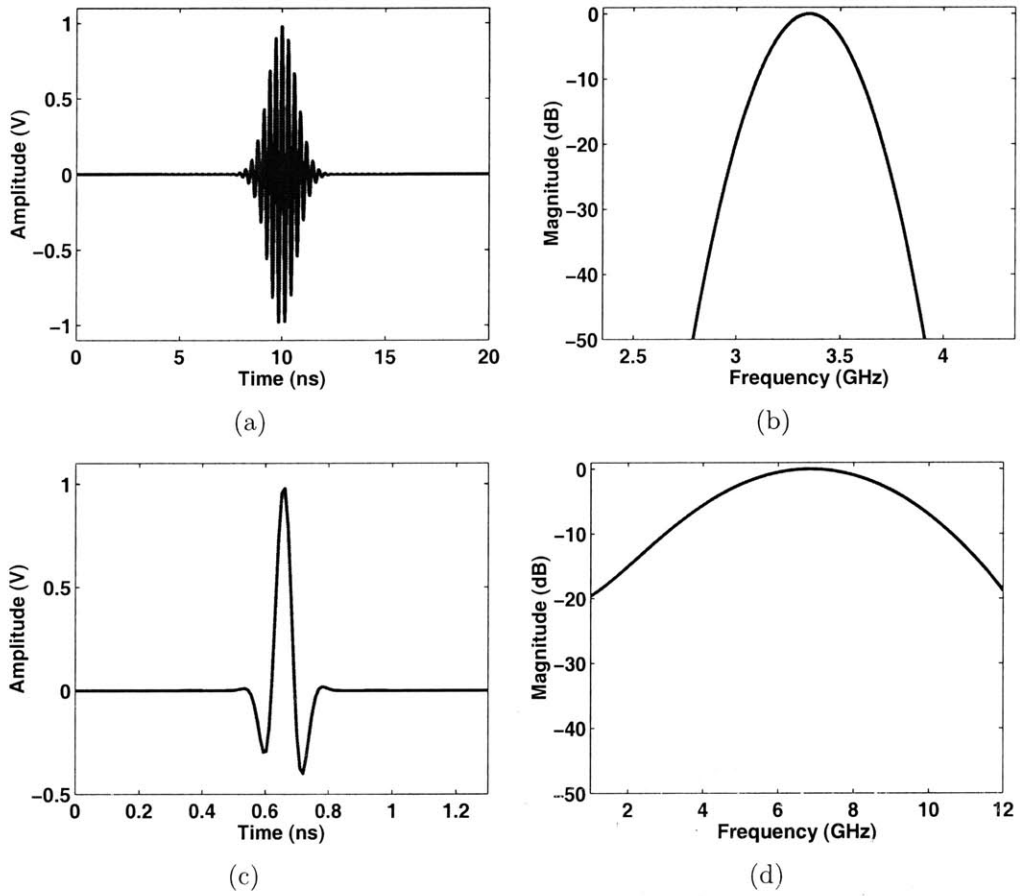


Figure 1-8: 500 MHz Gaussian pulse (a) time, (b) frequency domain. 7500 MHz Gaussian pulse (c) time, (d) frequency domain.

the Fourier transform of a time-domain Gaussian pulse is also a Gaussian in frequency. The -10dB bandwidths of the pulses in Figures 1-8(a) and 1-8(c) are 500 MHz and 7.5 GHz respectively. As can be seen, these signals are extremely short compared to narrowband radio signals.

1.5 Thesis Contributions

The contributions of this thesis are to explore and implement hardware using UWB signaling that realize energy efficient receivers for high and low data rates. The last portion seeks to decouple data rate dependency on energy/bit so that the radio can offer additional degrees of freedom to the system level of wireless sensor networks.

In the high data rate regime, a pulsed-based BPSK sub-banded discrete prototype

receiver is assembled to allow observation of the received UWB signal in a real-time wireless environment at any point in the receiver chain. It also allows for verification of design choices upon BER. Results from the discrete prototype are leveraged in integrating a 3.1–10.6 GHz UWB front-end receiver in a 0.18 μm SiGe BiCMOS process, featuring an unmatched LNA and 802.11a switchable notch filter for interference mitigation. Testing results reveal a noise figure of 3.3–5 dB over the entire band. Wireless verification of an un-matched LNA in the context of a full system receiver yield a BER of 10^{-3} at a sensitivity of -84 dBm, which matches theoretical calculations. The integrated -10 dB 802.11a notch filter improves the signal-to-noise-and-interferer ratio by at least 3 dB while the receiver is in the presence of a known narrowband interferer.

In the low data rate regime, energy/bit increases because fixed power costs are less effectively amortized over fewer bits/sec. However, by using UWB PPM signaling, the receiver can be duty-cycled so that energy/bit is decoupled from data rate. Through careful signaling, system, and circuit co-design, a non-coherent, 0–16.7 Mbps UWB receiver is implemented in a 90 nm CMOS process with a 0.5 V and 0.65 V power supply. This work achieves 2.5 nJ/bit of energy efficiency over three orders of magnitude in data rate. With adjustable bandpass filters and a new, low power relative compare baseband demodulator, the receiver achieves 10^{-3} BER with -99 dBm sensitivity at 100 kbps. A first-pass timing acquisition algorithm is developed on an FPGA platform and a transceiver system demo is assembled using this chip.

1.6 Thesis Structure

This thesis begins with an overview of UWB signals and systems, and proceeds to discuss this research in two sections: a high data rate 0.18 μm SiGe front-end and a low data rate 90 nm CMOS receiver. Both sections analyze the receiver circuits and systems in detail, and numerous measurements accompany the design choices to show the improvements and tradeoffs. Both sections conclude with a short discussion on the successful integration of the custom hardware systems that have been designed

here in achieving propagation of wireless video and/or images. The final chapter concludes and discusses exciting new research directions that expand this body of work.

Chapter 2

High Data Rate 100 Mbps, 3.1–10.6 GHz FCC Compliant Front-end

This chapter surveys previous work and shows how UWB signals have been utilized. It also describes the UWB RF front-end discrete prototype that is implemented for system testing, the UWB RF front-end RFIC chip that is implemented for the high data rate domain [22], and the system demo that is assembled [23].

2.1 Background and Previous Work

The initial response to a UWB LNA solution was driven by the need to achieve the broad bandwidth. A few papers had been published [24] [25] [26] for UWB based on the distributed amplifier principle [27]. Though this topology meets the specifications, it consumes a prohibitive amount of power for integration into battery-operated wireless devices.

More promising work was done using active matching LNAs [28] [29] [30], feedback LNAs [31] [32], and ladder matched LNAs [33] [34]. There was also theoretical work done by researchers at USC whose aim was to minimize the NF of a common source LNA without requiring input match [35].

Since the bandwidths of UWB signals are so large, is it possible to use simple AC coupling to handle $1/f$ noise and DC offset problems associated with direct-conversion receivers. To avoid higher order distortion, the mixer must have sufficient linearity to avoid these issues [36].

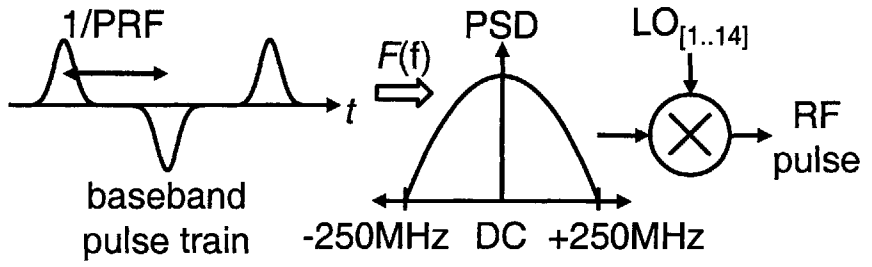
2.2 Signal Choice and Band Plan

Because BPSK pulse signals can be generated efficiently using analog techniques, demodulated with either analog and/or digital techniques, and have more relaxed linearity requirements on the receiver (as compared to OFDM signals), 500 MHz sub-banded Gaussian pulses are chosen for the signaling. For the Gaussian pulse, $\sigma \approx 1$ ns due to its desirable time and frequency response to occupy the sub-band bandwidth, leaving its -10 dB bandwidth to be 500 MHz. The pulse repetition frequency (PRF) is 100 MHz, which corresponds to a maximum data rate of 100 Mbps. Figure 2-1a shows the baseband pulse train signal, which is then up-converted to one of 14 channels in the UWB band. The frequency plan of this system is shown in Figure 2-1b, and f_{center} of each band is described by 2.1, where $n_{ch} = [1, 2, ..., 14]$.

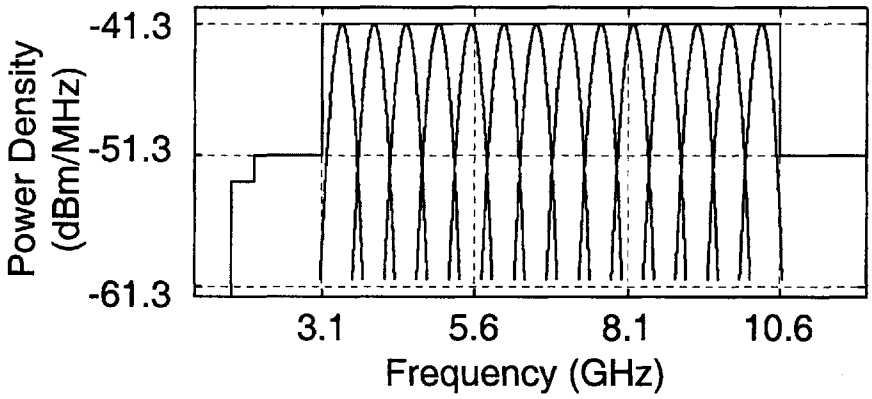
$$f_{center} = 2904 + 528 \cdot n_{ch}[MHz]. \tag{2.1}$$

2.3 Discrete Prototype

A UWB RF front-end shown in Figure 2-3, consisting of dual LNAs, phase splitters, mixers, I/Q gain stages, RF quadrature generator blocks, and RF PLLs is constructed in the context of a larger discrete UWB system prototype [37]. The center frequency of the discrete prototype is chosen to be in the 5 GHz band, since many of the RF blocks could be constructed by tweaking 802.11a building blocks. The system down-converts only one 500 MHz channel, and contains the necessary ADC and FPGA-implemented back-end algorithms to decode the UWB data packets. The wideband LNAs have a bandwidth up to 6 GHz and are built from discrete GaAs transistors



(a)



(b)

Figure 2-1: (a) Baseband Gaussian pulse signal and (b) Frequency plan.

from Agilent. The I/Q generator is built from delayed transmission lines to form the necessary phase shift. The wideband mixers and splitters are from Mini-Circuits. The baseband gain stages contain a custom phase splitter and cascade two 250 MHz, -6 dB to 30 dB adjustable-by-6 dB gain stages. The RF PLL contains a discrete VCO from Z-Communications and PLL from Analog Devices. The prototype allows the designer to analyze subtle and different effects of circuit non-idealities upon the entire system, allow real-time debugging of these problems and ultimately, assist in circuit and system design of the UWB transceiver. Results from the discrete prototype assisted in the circuit and system design, as well as providing a "swap-and-test" platform for verifying fabricated chips in a system context. In particular, the effects of I/Q phase/gain offset (Figure 2-2), ADC resolution, timing non-idealities between TX/RX LOs, and timing differences between the ADC clock and PRF clock can be observed using the system. LO feedthrough is a key phenomenon that was observed, and resulted in special care during circuit design to improve LO isolation in the

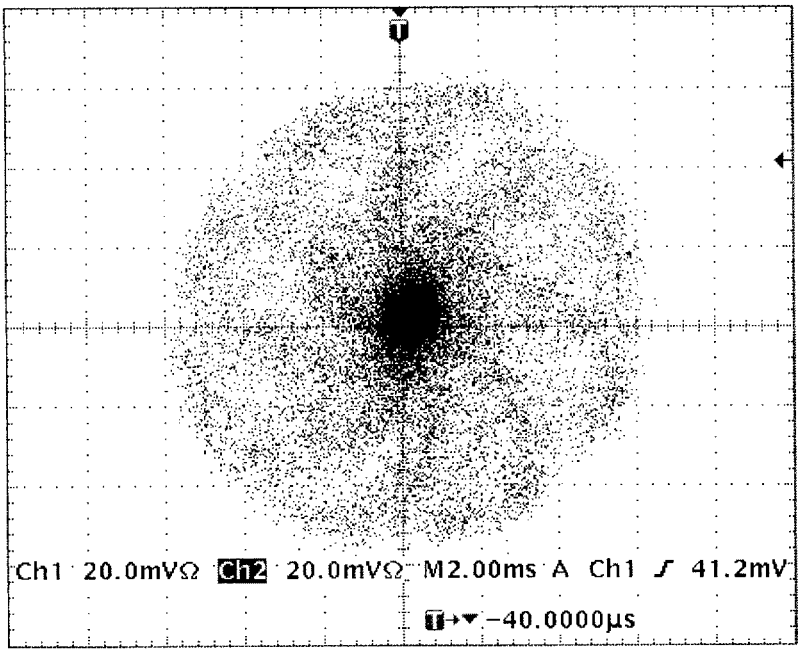


Figure 2-2: X/Y plot of baseband I vs. Q revealing I/Q gain and phase mismatch.

direct-conversion architecture.

2.4 Front-end Architecture

A diagram of the final receiver system is shown in Figure 2-4. The integrated RFIC front-end shaded in the figure is a product of this research. It consists of a single-ended LNA followed by an integrated 2^{nd}-order high-pass filter for improved out-of-band interference rejection at minimal cost to NF. The broadband LNA is chosen as opposed to a 500 MHz sub-banded LNA [38], due to the large number of required channels across the 7.5 GHz bandwidth. However, a more feasible trade-off to improve linearity and filtering while maintaining reasonable complexity would be to group multiple adjacent 500 MHz channels together into banks and to design an LNA that switches between these banks with a reduced number of switches and loads. The filter is followed by an RF single-to-differential converter with a switch-able notch filter to suppress unwanted 5 GHz ISM signals. The single-to-differential conversion done after the LNA helps to maintain low system NF and allows the RF notch filters to be

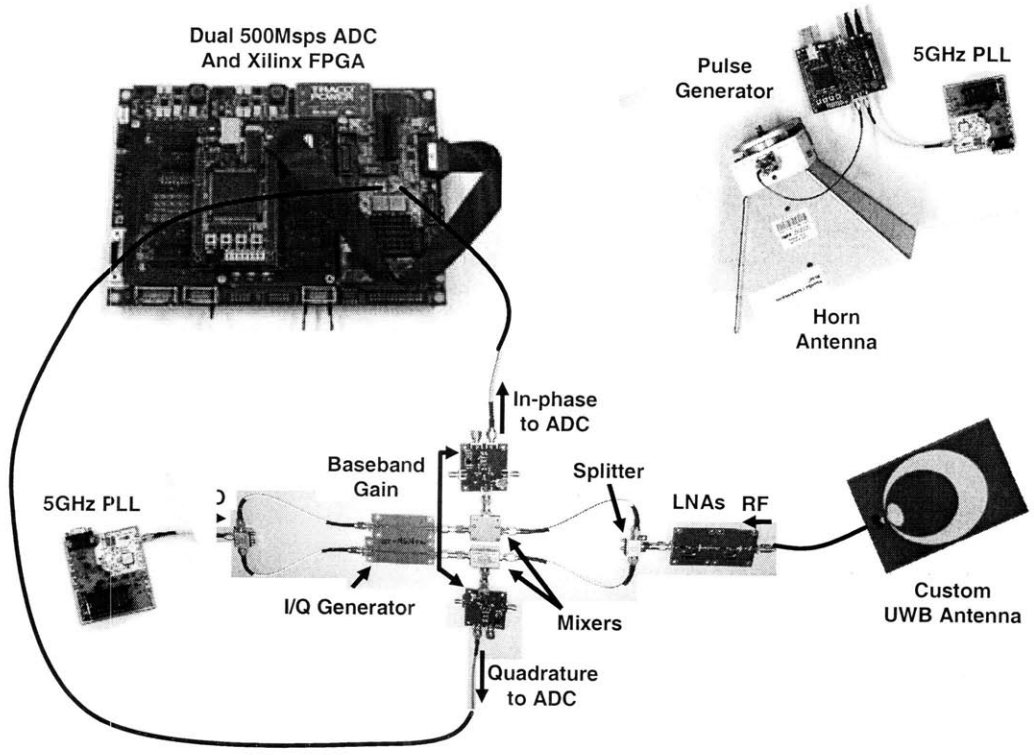


Figure 2-3: Transceiver discrete prototype.

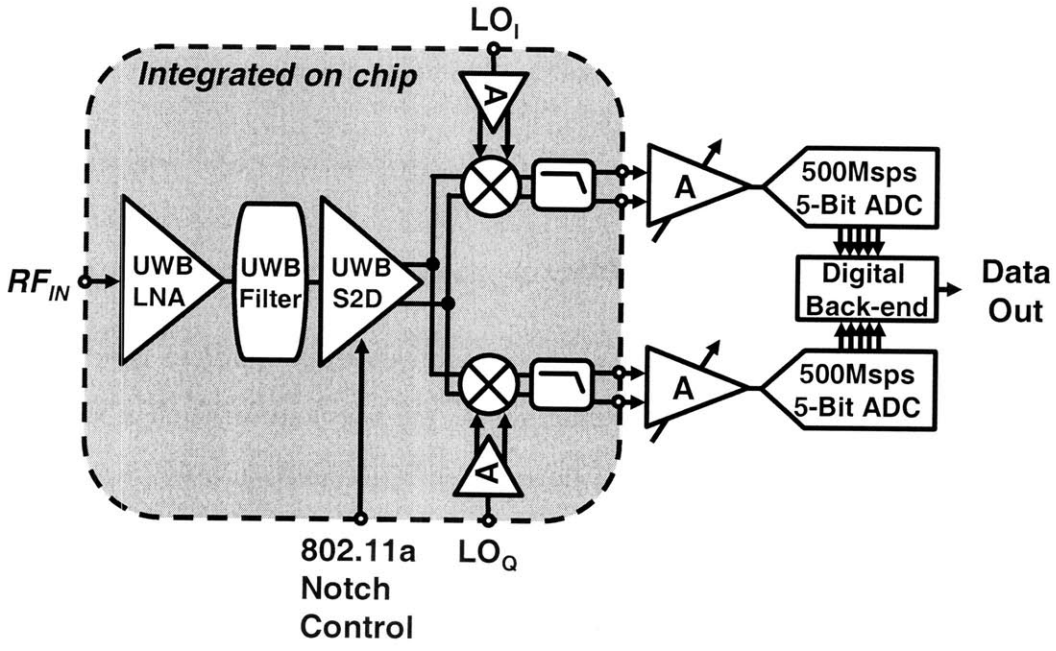


Figure 2-4: Receiver architecture.

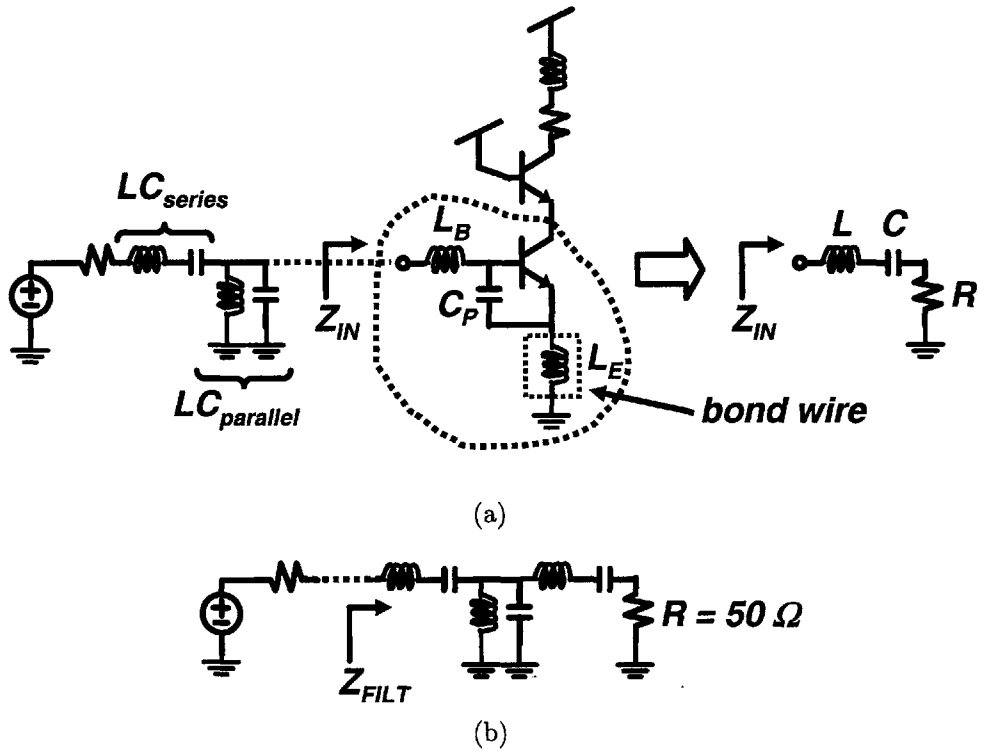


Figure 2-5: (a) Ladder matched LNA and (b) 3^{rd}-order Chebyshev filter.

easily implemented. The mixers are degenerated double-balanced Gilbert cell mixers. The local oscillator (LO) for the mixers is generated externally. The baseband output is filtered, buffered, and interfaced to the remaining receiver chain via AC-coupling to suppress $1/f$ noise and DC offsets.

2.4.1 Low Noise Amplifier

An LNA structure that achieves a broadband impedance match and good NF is the ladder matched LNA [33]. Figure 2-5a shows the topology of such a circuit, and R is given by (2.2), where L_E is the down bond inductance and C_P is an extrinsic capacitor placed in parallel with C_π.

$$R = 2\pi f_t \cdot L_E = \frac{g_m}{C_\pi + C_P} \cdot L_E. \tag{2.2}$$

The structure is based upon a narrowband inductively degenerated cascode LNA

that is extended to large bandwidths by adding $LC_{parallel}$ and LC_{series} to match the topology of a 3rd-order Chebyshev band-pass filter shown in Figure 2-5b [39]. S_{11} of Z_{FILT} is below -10 dB for filter values that have been extracted with a tolerable ripple of less than 1 dB [34]. The NF for such a topology in SiGe is given by (2.3), where r_b and Z_O are the base resistance of the input transistor and 50 Ω of the source impedance, respectively [33]. The main feature of this topology is the ability to match the NF close to NF_{min} while also achieving power match [34].

$$NF_{ladder} = 10 \cdot log_{10}\left(1 + \frac{r_b}{Z_O} + \frac{g_m}{2} Z_O \left(\frac{w}{w_t}\right)^2\right) \tag{2.3}$$

Though the ladder matched LNA provides a good input match and low NF for UWB LNAs, these specifications become difficult to maintain if the circuit is bonded to a PCB or a package. This is due to the input matching requirement depending on f_t and L_E of the circuit, as shown in (2.2). NF_{min} for a cascode LNA is given by 2.4, where β is the current gain of the transistor.

$$NF_{min} = 10 \cdot log_{10}\left(1 + \frac{1}{\beta} + \sqrt{2g_m r_b}\sqrt{\frac{1}{\beta} + \left(\frac{f}{f_t}\right)^2}\right). \tag{2.4}$$

Equation (2.4) shows that NF_{min} is proportional to f/f_t for $f/f_t \gg \sqrt{\frac{1}{\beta}}$. Thus, if f_t must be decreased because L_E is too large to achieve a 50 Ω match 2.2, then the achievable NF_{min} is increased. Common ways of decreasing f_t are by reducing the current density or by increasing C_P. In a packaged chip, L_E is usually constructed with a down bond whose inductance can be approximated by 1 nH/mm for 0.001" thick bond wires. The average length of the down bonds in this chip is 0.8 mm. Parallel down bonds can be used to reduce the inductance, but the reduction factor is limited by mutual coupling. Figure 2-6 shows simulated NF_{min} and $\Re\{Z_{IN}\}$ of three ladder matched LNAs each intrinsically biased at an f_t of 60 GHz, and then degraded by C_P accordingly to meet the input matching requirement. The L_E inductance ranges from 132 pH and 0.8 nH. C_π for these LNAs is 170 fF. The f_t is appropriately degraded by increasing C_P for the 0.4 nH and 0.8 nH cases to maintain the input

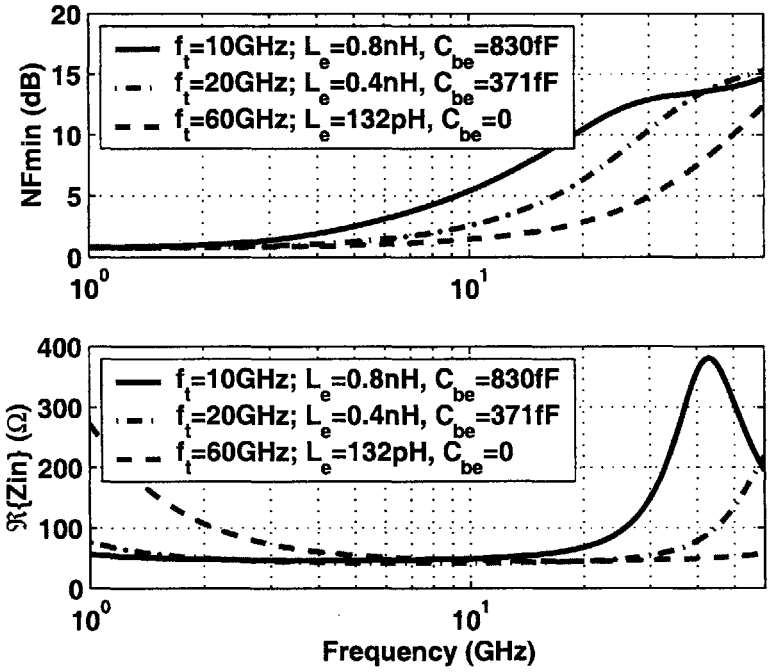


Figure 2-6: (a) NF and (b) $\Re\{Z_{IN}\}$ of three ladder matched LNAs.

match requirement. At 10 GHz, NF_{min} varies from 1.45 dB to 5.5 dB. In narrowband radio design, a solution to handle the coupled nature of NF_{min} and input match consists of using two- and three-element matching networks to allow the cascode LNA to operate at a high f_t while maintaining the input match requirement. However, narrowband impedance matching structures transform impedances only across limited bandwidths and are not suitable for UWB signals. Differential LNA structures that allow smaller on-chip degeneration inductors to be realized may be feasible with pre-LNA baluns, but the losses of the baluns which directly contribute to the NF of the system must be considered.

To leverage the high f_t of the SiGe transistors for reduced NF, the UWB LNA here does not attempt to achieve impedance match. Instead, the inductively-peaked cascode LNA shown in Figure 2-7 is viewed as a voltage amplifier and designed such that the NF to a 50 Ω source is minimized at 10 GHz, where propagation losses are greatest. Because an input match is not required, Q_1 can be biased at a high f_t for low-noise performance with minimum current. Furthermore, because the input match is not required, the lossy and noisy low-Q inductors in LC_{series} and $LC_{parallel}$ of the

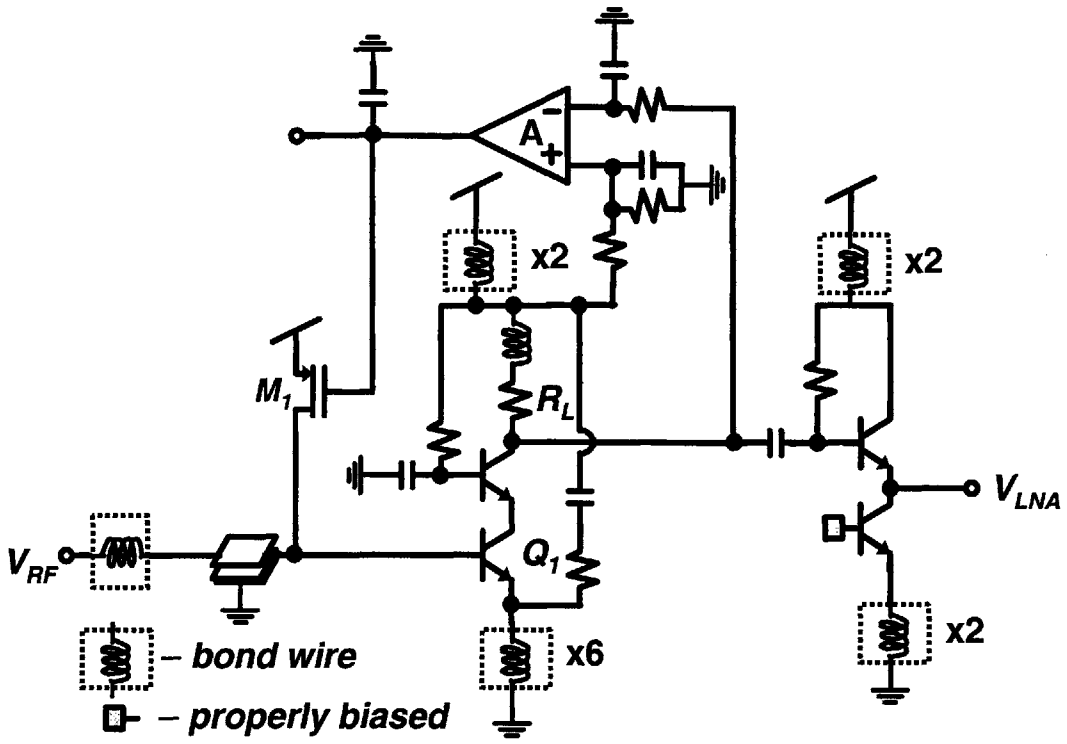


Figure 2-7: Low-noise amplifier and buffer.

ladder matched LNA are not needed. The drawback to this method is that wideband pre-select filters that improve out-of-band interference rejection can no longer be used, since they require a 50 Ω match at both ports. However, this problem can be partially mitigated with a post-LNA on-chip filter and/or an LNA with sufficient linearity. To improve immunity to bond wire, package, and PCB parasitics at the LNA load, a de-Qed capacitor shunts the RF current that would normally be sourced from the power supply to the low impedance ground established at the LNA emitter by parallel down bonds.

To suppress reflections due to an unmatched LNA, the antenna must be placed close to the LNA to reduce transmission line effects. The close proximity of the antenna to the IC is also desirable for minimizing cable losses that directly impact system NF. CST Microwave Studio is used to verify the antenna's transient response to an unmatched load in an electromagnetic simulator environment by replacing the receiver port with an equivalent input network of the LNA. To aid in circuit design,

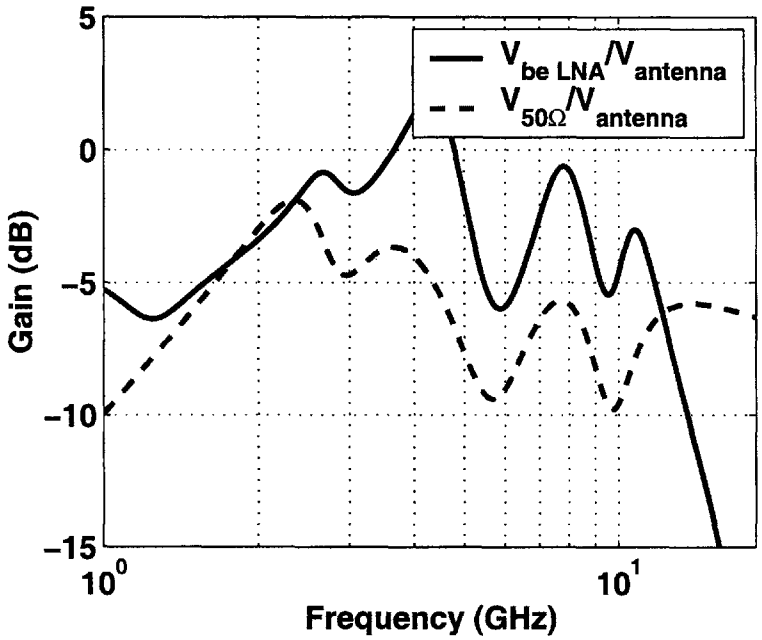


Figure 2-8: Transfer functions of the antenna to a 50 Ω load and to the un-matched LNA.

Spice models of the antenna are extracted from the electromagnetic simulator. Figure 2-8 shows the transfer function of the extracted model to a 50 Ω matched input and to the V_{be} of the LNA input transistor.

The UWB LNA in Figure 2-7 is biased with a high-impedance PMOS drain M_1 embedded in a μW feedback loop that monitors collector current through R_L and sets the g_m of Q_1. This circuit contributes minimal noise due to the large output impedance and small drain noise current of M_1. The buffer is optimized to interface the LNA to the high-pass filter and single-to-differential converter. The simulated NF of the LNA is 2-2.3 dB over the entire band, and provides a gain of 15 dB.

2.4.2 Channel-Select Filter and Single-to-Differential Converter

The channel select filter shown in Figure 2-9 is formed by a three element high-pass ladder network with two capacitors and shunt inductor. The low-pass portion of the channel select filter is formed by the cascaded amplifier roll-off.

The single-to-differential converter has a cross-coupled low-frequency PMOS loop

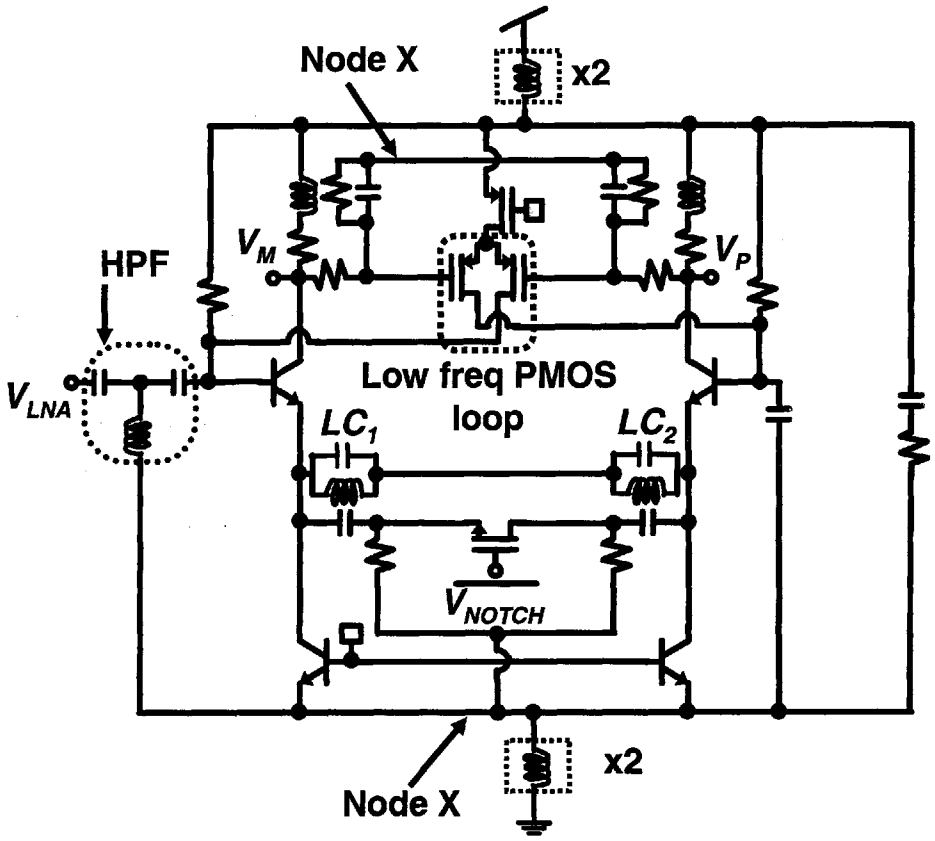


Figure 2-9: Channel-select filter and single-to-differential converter.

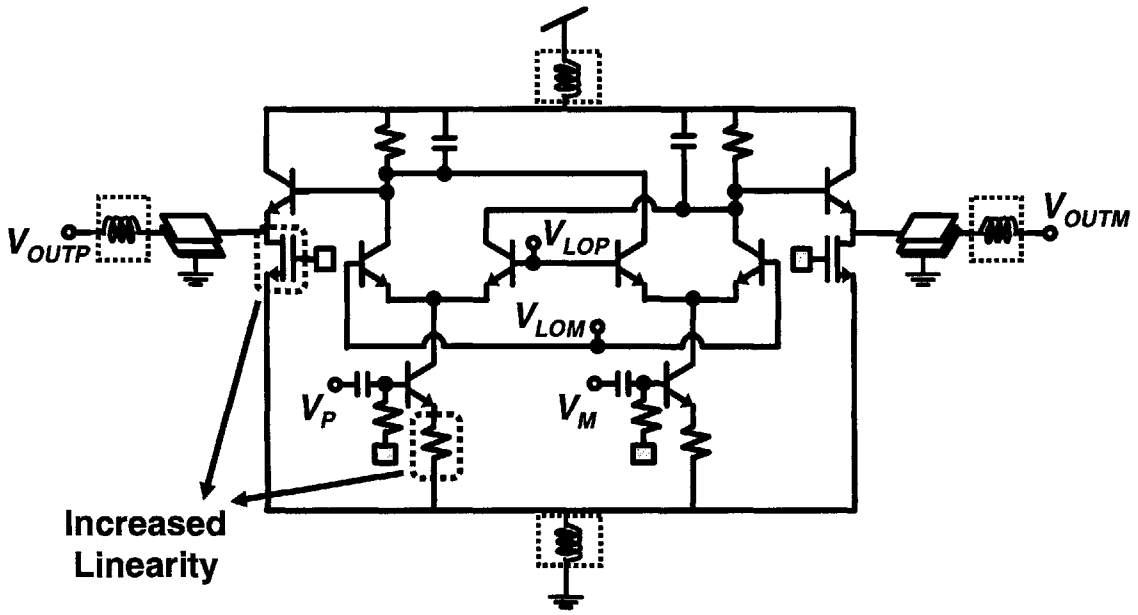


Figure 2-10: Double-balanced mixer.

that equalizes current differences between the differential pairs to ensure balanced operation.

The switch-able notch filter uses parallel LC_1 and LC_2 tanks that degenerate the emitters of the differential pair transistors with a high-impedance at their respective resonances. This reduces the gain at those frequencies. The notch frequencies are fixed at $1/\sqrt{LC}$. Any combination of LC is possible to create the filter. However, higher quality factors are obtainable with smaller inductors, thereby producing sharper notch filter characteristics. The notch frequency of each LC structure is designed at 5.25 GHz and 5.75 GHz respectively, where 5 GHz ISM signals may appear. The switch to bypass the notch filters is AC-coupled to the emitters of the differential amplifier transistor pair. This allows the switch to be reasonably sized while still having a low on-resistance because of the large overdrive. The notching and phase-splitting blocks are strategically placed after the LNA so that overall system NF is not significantly degraded.

2.4.3 Mixers and LO Amplifier Chain

The mixers are conventional double-balanced Gilbert mixers shown in Figure 2-10. The RF input is resistively degenerated to increase dynamic range (DR) and linearity while decreasing the load on the previous stage. Though resistive degeneration increases the NF of the mixer, the effective increase in system NF is marginal due to the two gain stages prior to the mixer. A 250 MHz 1^{st}-order low-pass filter is implemented at the output for attenuating high frequency mixing products and is assisted with a 3^{rd}-order off-chip filter for further channel selectivity in the system. The AC-coupling capacitors are also off-chip.

The single-ended quadrature LOs are generated off-chip through a frequency generator and a wideband I/Q phase shifter. The on-chip LO gain stages convert single-ended LO signals to differential and refine the signal through a cascade of two differential amplifiers with low common-mode gain. On-chip amplification of the LO reduces the external bond wire coupling of LO-RF and LO-LO signals.

2.5 Measured Results

RFIC front-end measurements are reported in Section 2.5.1. To verify the front-end in a wireless system environment, the system shown in Figure 2-4 is assembled and measurements are reported in the Section 2.5.2.

2.5.1 Wired RFIC Measurements

The receiver conversion gain and NF shown in Figure 2-11 are measured by sweeping the RF input from 3.1-10.6 GHz and offsetting the LO frequency by 50 MHz so that a baseband signal at 50 MHz is observed.

The average conversion gain is 32 dB and varies +/-5 dB across the bandwidth. The chip was originally designed for testing in a chip-on-board system but is packaged for robustness. The larger parasitic capacitances of the package (500 fF) and bond wire/pin inductances (2 nH) impact the RF pass-band. However, a system NF from

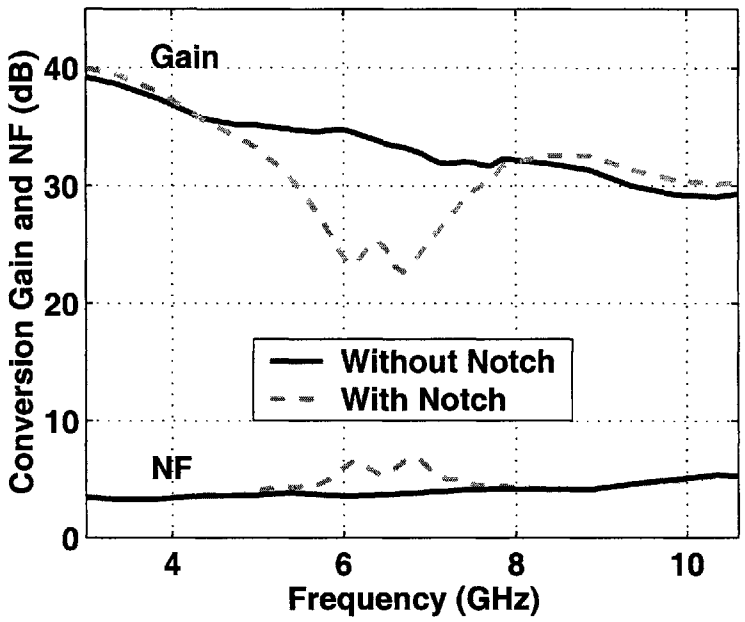


Figure 2-11: Measured conversion gain and NF.

3.3 dB to 5 dB is still achieved across the 3.1-10.6 GHz bandwidth. Therefore, a flat conversion gain curve can conceivably be recovered by baseband gain compensation without degrading NF significantly. The input P_{1dB} increases from -46 dBm at 3.1 GHz to -36 dBm at 10.6 GHz.

When the notch filter is activated, the attenuation is 10 dB. The frequency of the notch filter is higher than expected due to over-accounted parasitics, but functionality of an RF notch in a UWB receiver system can still be examined. This filter allows the receiver to tolerate an additional 10 dB of interferer power within the notch frequencies.

To verify the front-end functionality in a full receiver, the system in Figure 2-4 is implemented using the packaged RFIC front-end, external baseband gain and 3^{rd}-order channel-select filters, a dual 500 Msps 8-bit ADC acquisition card, and a back-end receiver built in Matlab [40]. BER measurements are made at $f_c = 3.432\ GHz$ and $f_c = 7.128\ GHz$. Figure 2-13 plots the two measured BER curves. Each non-interpolated BER point in the figure is generated by demodulating 20 packets. Each packet contains a preamble with a 31-pulse Gold code transmitted at 100 ns/pulse to achieve coarse acquisition and channel estimation, followed by 10^4 un-coded bits

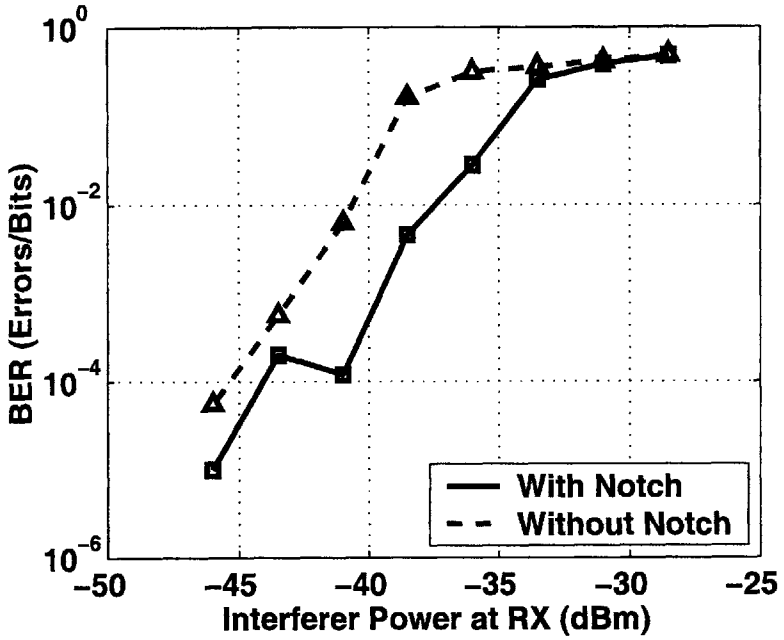


Figure 2-12: Measured notch filter improvement upon BER of a -70 dBm 500 MHz-wide pulse centered at 3.35 GHz in midst of a known interferer at 6.75 GHz.

of data in the payload transmitted at 100 Mbps. Also included in the plot is a simulated ideal BER curve for Gaussian-shaped UWB pulse signals that are limited only by Additive White Gaussian Noise (AWGN) and quantization noise of a 4-bit ADC. The input always spans the ADC's full scale input range and no timing offsets or pre-ADC distortion from nonlinearities that normally occur in a real front-end were included in this model [41].

For RX signals greater than -85 dBm, the maximum deviation from the ideal BER curve to the 3.432 GHz centered pulse is 3 dB. The difference in lateral translation between the BER measurements corresponds with the general increase in NF at 7.128 GHz from the NF at 3.432 GHz. For RX signals less than -85 dBm, the measured curves depart in shape from the ideal curve as they approach a BER of 0.5. This means that the signal to noise (and distortion) ratio of the system is decreasing by more than just the reduction in RX signal power.

To quantify the effectiveness of the notch filter for increasing the signal to interferer-plus-noise ratio (SINR) in the presence of a known interferer, BER measurements are

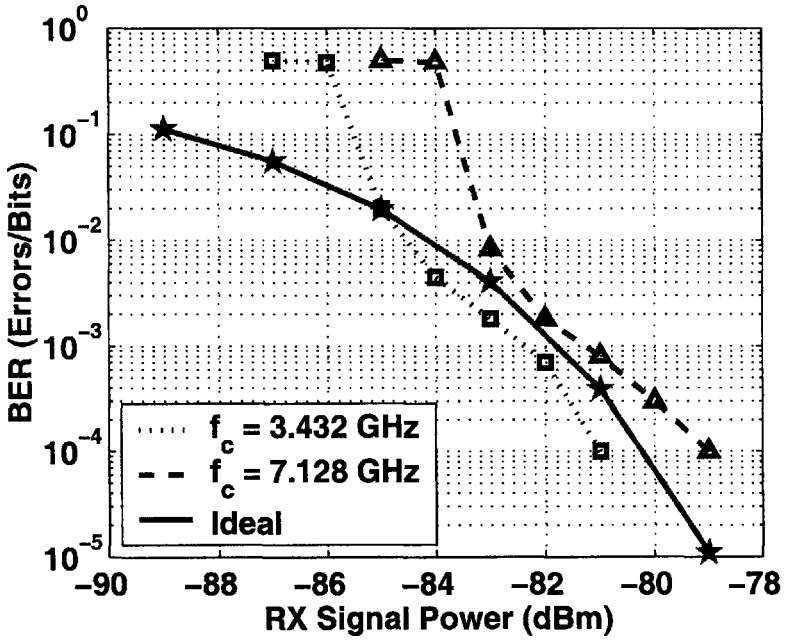


Figure 2-13: Measured and simulated BER curves.

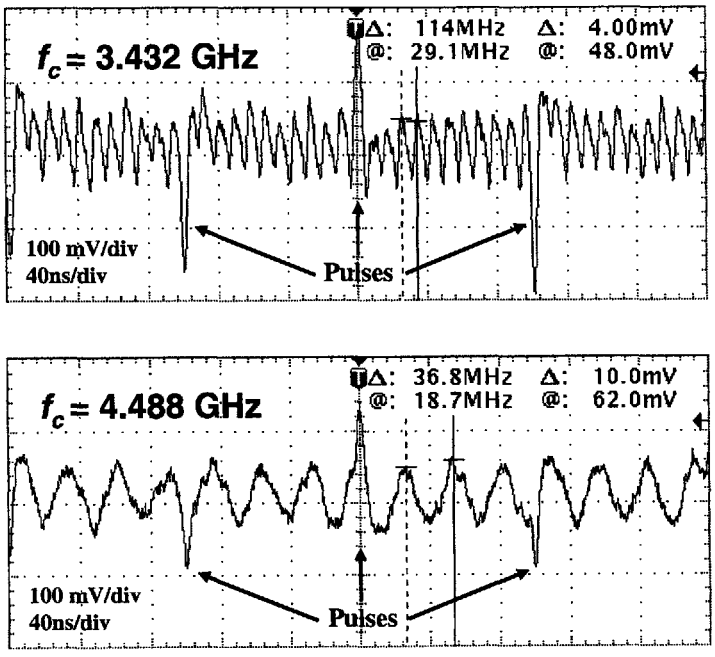


Figure 2-14: Oscilloscope plots of pulses amidst IM distortion.

made with two different 500 MHz-wide UWB pulses both with -63 dBm of signal power at the receiver; one centered at 3.432 GHz and another centered at 4.488 GHz. For both of these measurements, a known interferer in the notch filter band at 6.75 GHz is swept from -43 dBm to -23 dBm in 2.5 dB steps. The interferer reduces SINR by producing inter-modulation (IM) products that appear in the baseband frequency with the harmonics of the LO. Figure 2-14 shows the oscilloscope plots of the IM products that lie in-band. For the 3.432 GHz pulses, the 114 MHz baseband beat frequency is the IM_3 of $2 \cdot f_{LO}$ and $f_{interferer}$. For the 4.488 GHz pulses, the 36 MHz baseband beat frequency is the IM_5 of $3 \cdot f_{LO}$ and $2 \cdot f_{interferer}$. However, these unwanted IM products can be suppressed with the notch filter. Figures 2-15 and 2-16 plot BER versus increasing interferer power, with and without the notch filter. Though the 3.432 GHz pulses are further away from the 6.75 GHz interferer than the 4.488 GHz pulses, the effect of the notch filter is greater for pulses that suffer from higher order IM products. This can be understood by observing how the IM_3 amplitude coefficient is proportional to $P_{interferer}$, while the IM_5 amplitude coefficient for the 4.488 GHz pulses is proportional to $(P_{interferer})^2$. By comparing the SINR improvement of Figures 2-15 and 2-16, the one suffering from IM_3 produces a 3 dB shift between the with/without notch filter plots while the one that suffers from IM_5 produces a 6 dB shift. Correspondingly, the notch filter demonstrates one order-of-magnitude improvement in BER for the 3.432 GHz pulses and roughly four orders-of-magnitude improvement in BER for the 4.488 GHz pulses.

2.5.2 Wireless RFIC Measurements

To verify the unmatched RFIC in a wireless environment where reflections may exist, a horn antenna for wireless transmission and UWB antenna [42] for reception is added to the system configuration. Max/min gain excursions at the load due to reflections occurring in a transmission line with both ends unmatched are theoretically described by (2.5) and (2.6), where L is the loss through the transmission line and Γ is the reflection coefficient [43]. Figure 2.5.2 shows the photo and transceiver diagram of the setup.

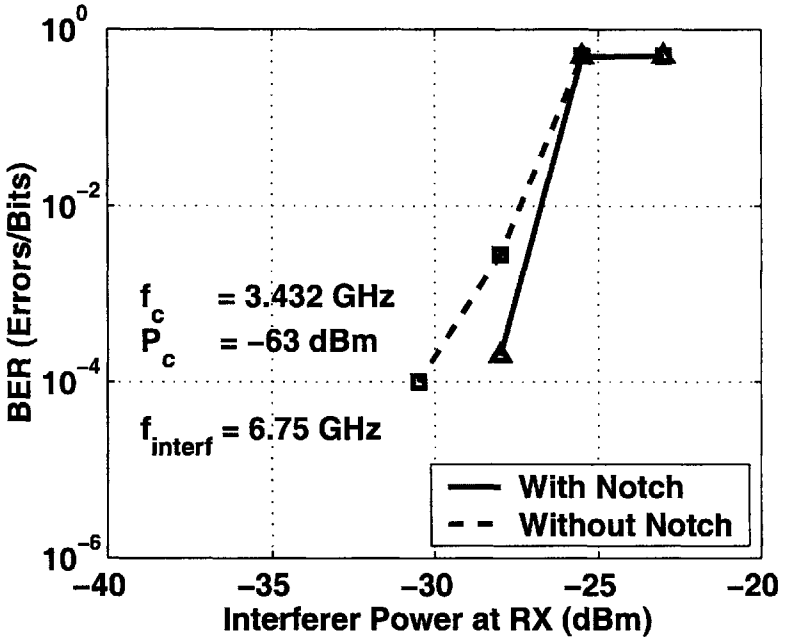


Figure 2-15: Measured BER gains for 3.432 GHz pulses with the notch filter.

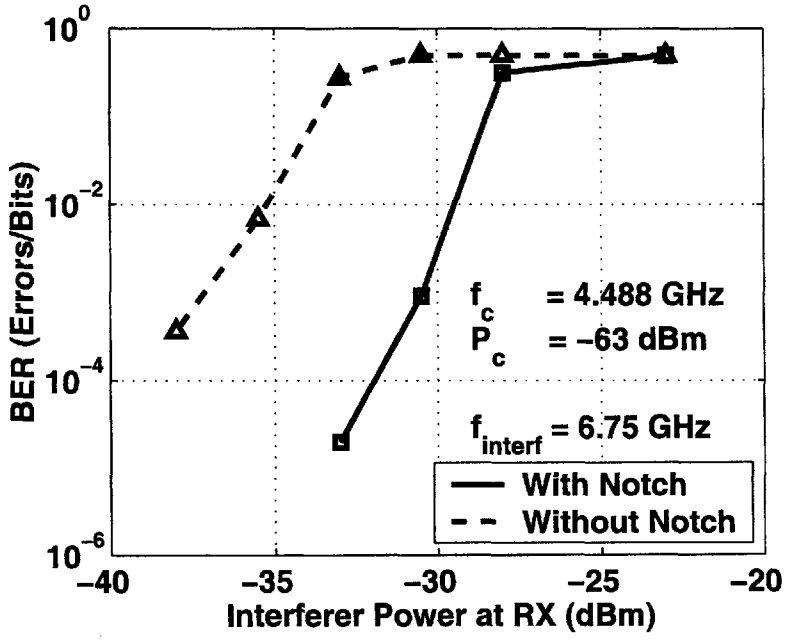
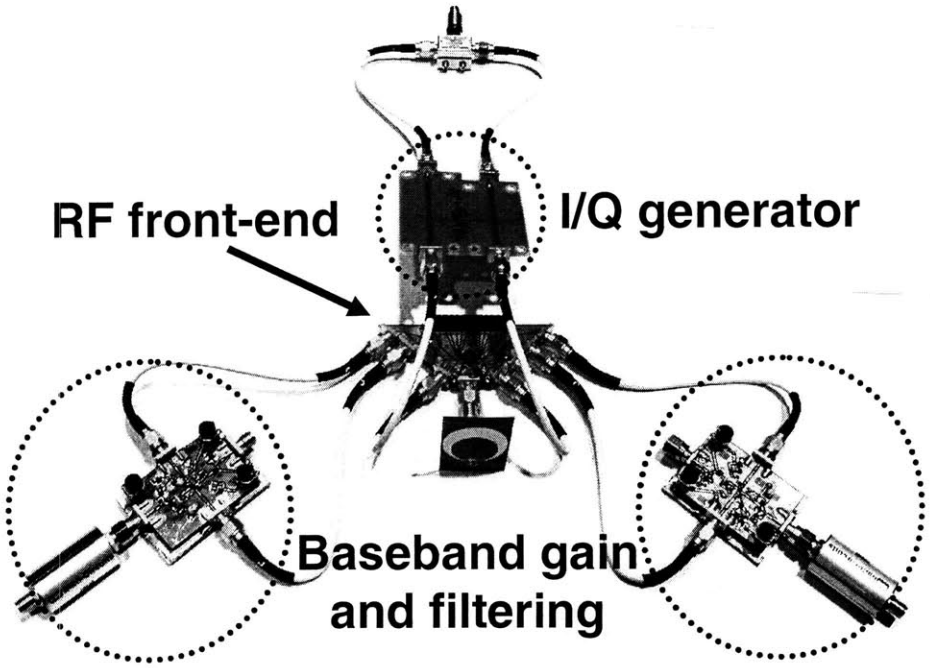
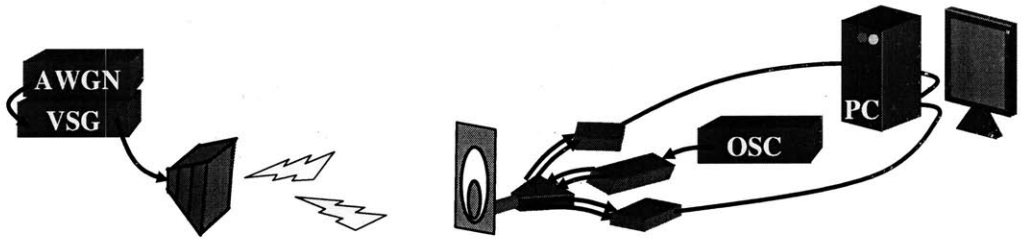


Figure 2-16: Measured BER gains for 4.488 GHz pulses with the notch filter.



(a)



(b)

Figure 2-17: (a) Setup photo and (b) transceiver diagram.

$$A_{max} = \frac{1}{1 - L^2 \cdot |\Gamma_{S11,LNA} \cdot \Gamma_{S11,Antenna}|} \tag{2.5}$$

$$A_{min} = \frac{1}{1 + L^2 \cdot |\Gamma_{S11,LNA} \cdot \Gamma_{S11,Antenna}|} \tag{2.6}$$

Figure 2-18a is a plot of conversion gains that are normalized to the minimum gain of the wireless measurement. The reference non-wireless plot is generated by piecing together the channel loss from the TX to RX antenna and the RFIC conversion gain. Both measurements are done in reflection-less environments by ensuring at least one end of the transmission line used in each measurement is properly terminated. The

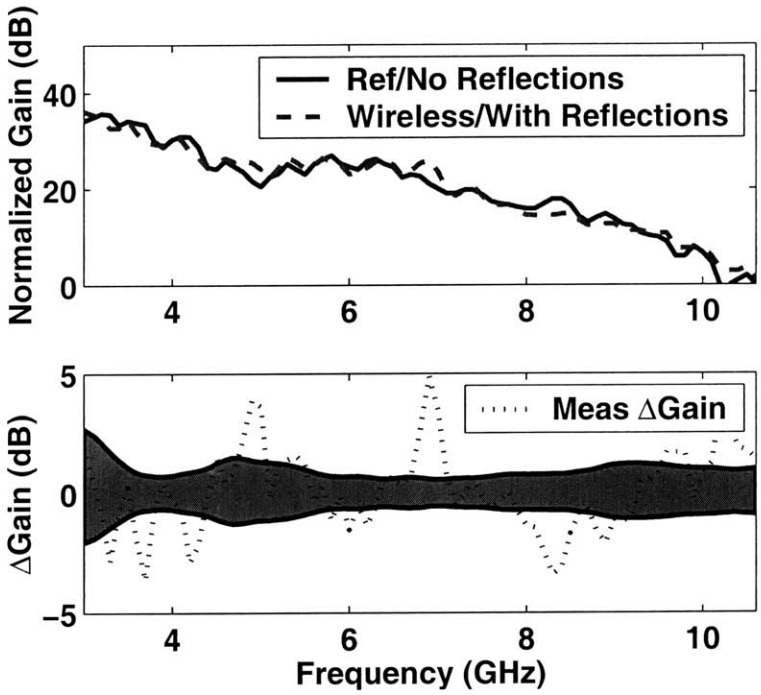


Figure 2-18: (a) Normalized transfer gains. (b) Theory and measured Δgain.

total transfer gain is obtained by directly measuring the conversion gain between the TX and RX antenna/RFIC baseband output, and is subject to reflections occurring in the short transmission line between the antenna and front-end.

The total channel losses seen in Figure 2-18a exceed what is expected from channel propagation losses [20] and measured RFIC conversion gain variations over bandwidth. The additional losses are accounted for in the reduction of the UWB antenna's azimuthal radiation pattern at higher frequencies [42].

Figure 2-18b uses measured values of $S_{11,Antenna}$ and $S_{11,LNA}$ that are shown in Figure 2-19 to plot a patch of theoretical max/min gain excursions of the system. Superimposed on this patch is a plot of the difference between the reference transfer gain without reflections and wireless transfer gain with reflections found in Figure 2-18a. The measured gain difference falls outside the boundaries within a few dB through the band while residing mostly within the boundaries otherwise. These excursions from the theoretical boundary may be due to the effective impedance of the antenna being sensitive to changing environmental factors and reflections. Though the transfer gain from antenna to LNA may fluctuate, the input signal-to-noise ratio

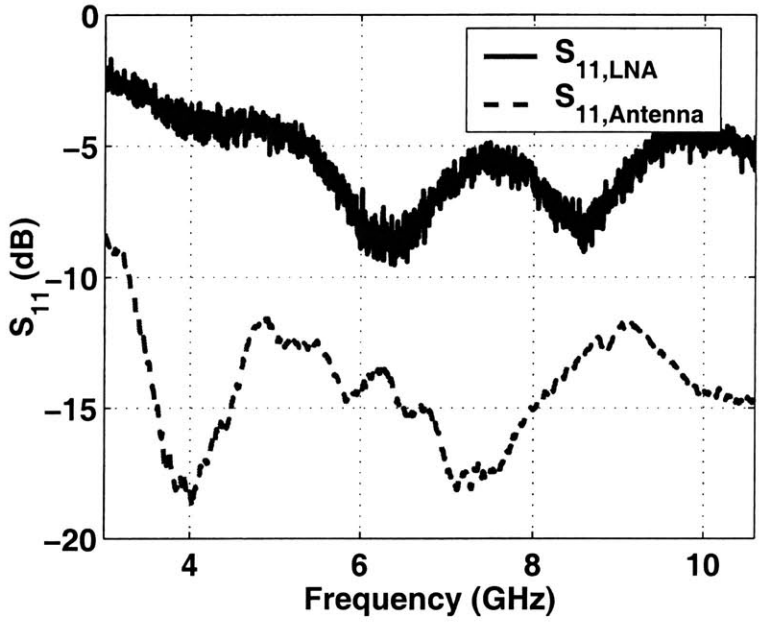


Figure 2-19: Measured $S_{11,LNA}$ and $S_{11,Antenna}$.

Block	**Power (mW)**
LNA	4.23
Buffer, S2D & notch	13.5
2 mixers and buffers	21.6
2 LO amplifiers	14.4
Total	**53.73**

Table 2.1: Power consumption at 1.8 V.

(SNR) does not, as the changes occur uniformly to both signal and noise.

To obtain wireless BER measurements, the system is fixed 1 m apart in a line-of-sight configuration, and the transmitter power is varied to achieve the desired RX antenna power. The RX antenna power is verified with a spectrum analyzer. For RX antenna powers greater than -76 dBm, no errors were observed through 20 packets. A BER of 10^{-3} is achieved at a receiver sensitivity of -84 dBm, which matches with the wired BER measurements. An oscilloscope plot of a wirelessly received and down-converted differential pulse during coarse acquisition is shown in Figure 2-20.

Table 2.1 shows the power breakdown of the front-end. A summary of chip performance is reported in Table 2.2, and Table 2.3 compares this UWB receiver to current work. The receiver in this work affords up to 10 GHz of sub-banded UWB

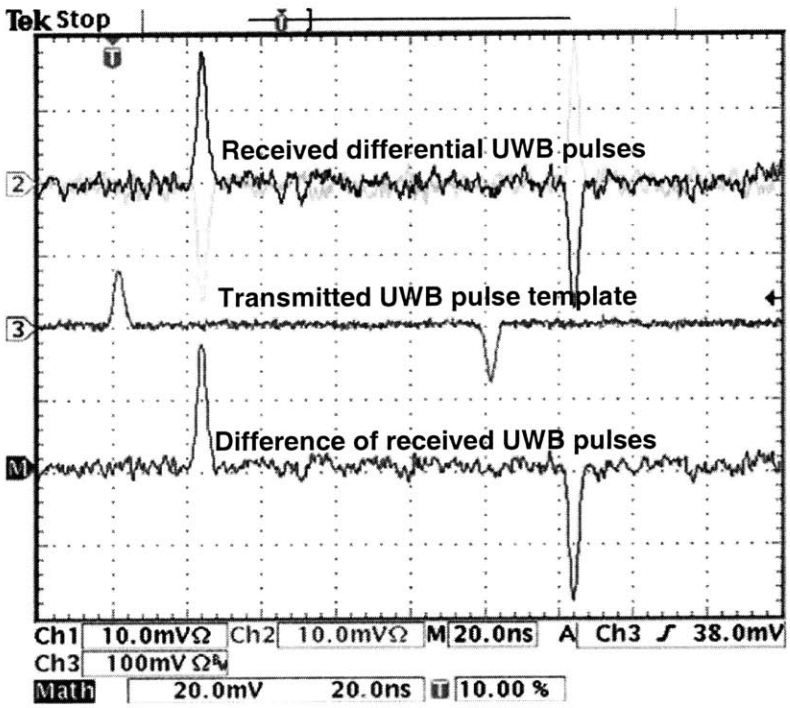


Figure 2-20: Oscilloscope plot of wirelessly received UWB pulses.

Specification	**Value from 3.1-10.6 GHz**
Conversion gain	39 to 29 dB
Noise figure	3.3 to 5 dB
Input P_{1dB}	-46 to -36 dBm
Notch filter attenuation	10 dB (6.25-6.75 GHz)
Sensitivity (BER=10^{-3})	-84 dBm (for 3.432 GHz pulses)
Process technology	0.18μm SiGe BiCMOS

Table 2.2: Chip performance summary.

Specs	**[4]**	**[13]**	**[14]**	**[15]**	**[16]**	**This work**
BW (GHz)	3 – 5	3 – 5	3 – 8	3 – 8	3 – 10	3 – 10
NF (dB)	5.5 – 8.4	4.5	5.2 – 7.7	3.3 – 4.1	4.1 – 6.2	3.3 – 5
Mean P_{1dB} (dBm)	-11	-6 (IIP3)	-10	-9.6	-23.5	-41
Power (mW)	105	195	18	238	84	54
PLL	yes	yes	no	yes	no	no
Packaged	yes	yes	no	no	yes	yes
Process	0.13 CMOS	0.25 BiCMOS	0.18 CMOS	0.25 BiCMOS	0.25 BiCMOS	0.18 BiCMOS

Table 2.3: Comparison table.

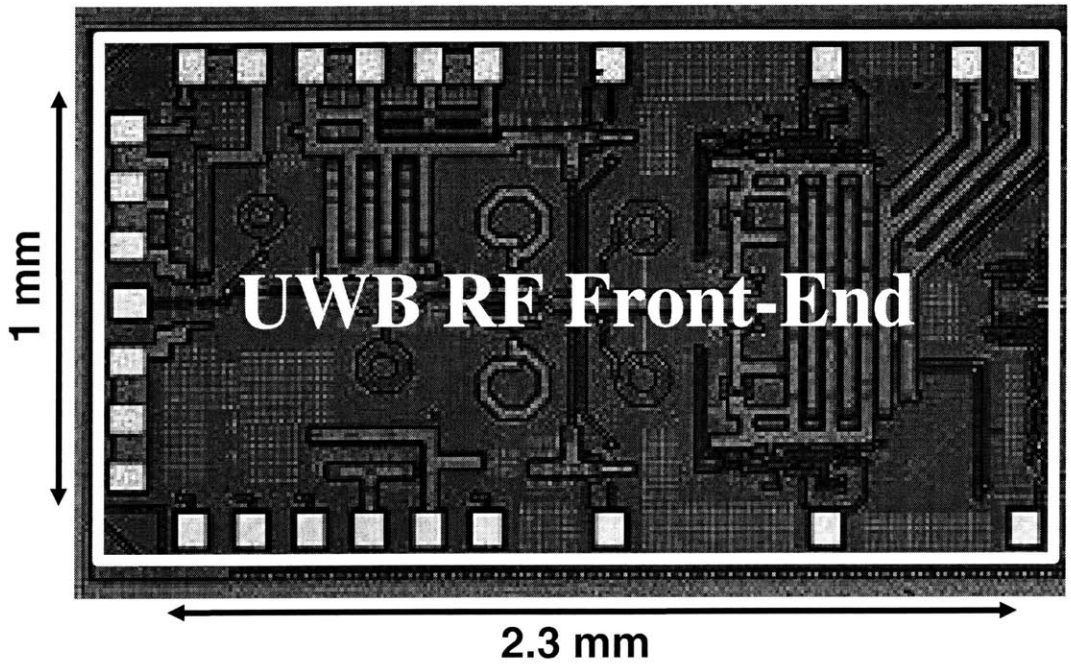


Figure 2-21: Die photo.

pulse reception in a QFN package with low NF through the band, but linearity could be improved with a coarse gain control setting in the RF gain path and improved linearity in the mixers. The die photo of the chip is shown in Figure 2-21. The active area is 1 mm x 2.3 mm.

2.6 Receiver System Demo

A block diagram of the complete system demo is shown in Figure 2-22, and is comprised of the work of five graduate students in designing four chips and a planar antenna. A JAVA interface for packet-ized wireless transmission and reception was developed by an undergraduate student [23]. Figure 2-23 shows a photo of the entire receiver.

The system is able to receive 500 MHz-wide sub-banded BPSK UWB pulses at 100 Mbps in each of the 14 channels across the 3.1-10.6 GHz band. Each packet (Figure 2-24) is comprised of a preamble and a payload, both of fixed length. The preamble contains pulses that are separated by 60 ns. It repeats a 31-pulse Gold

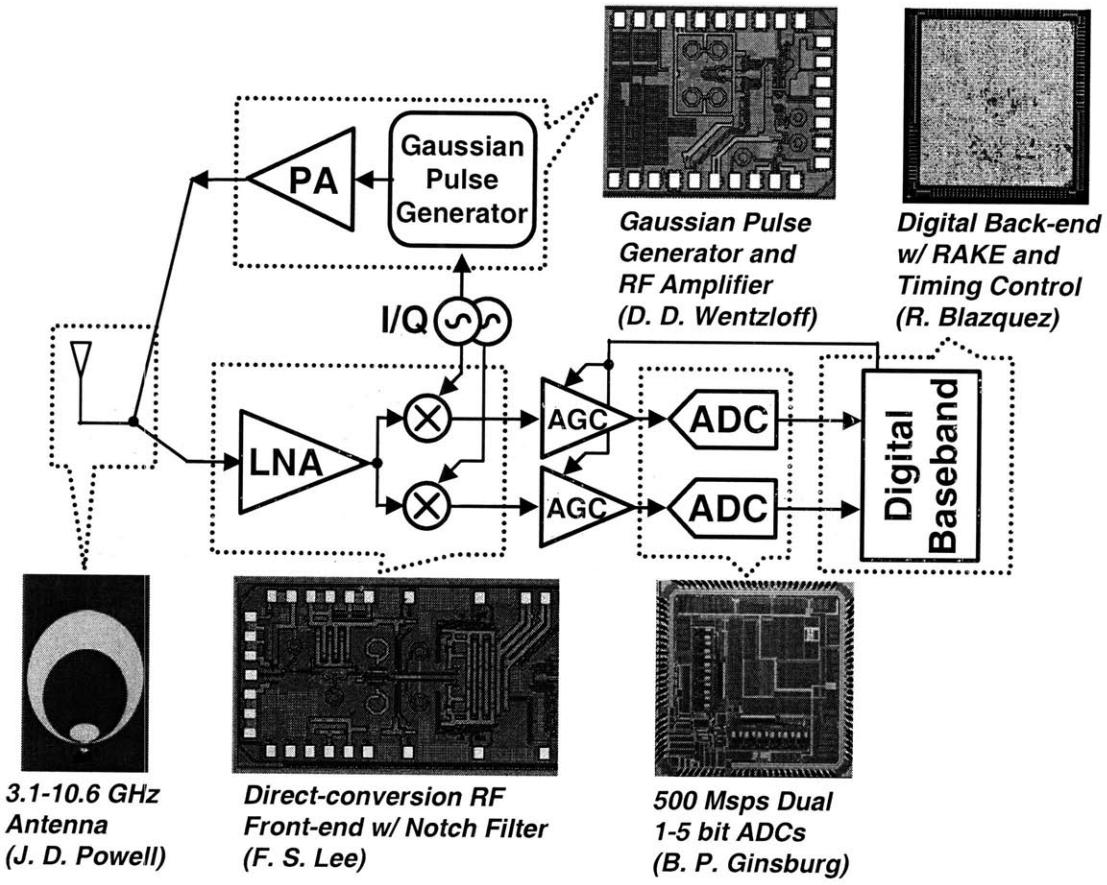


Figure 2-22: UWB system demo block diagram.

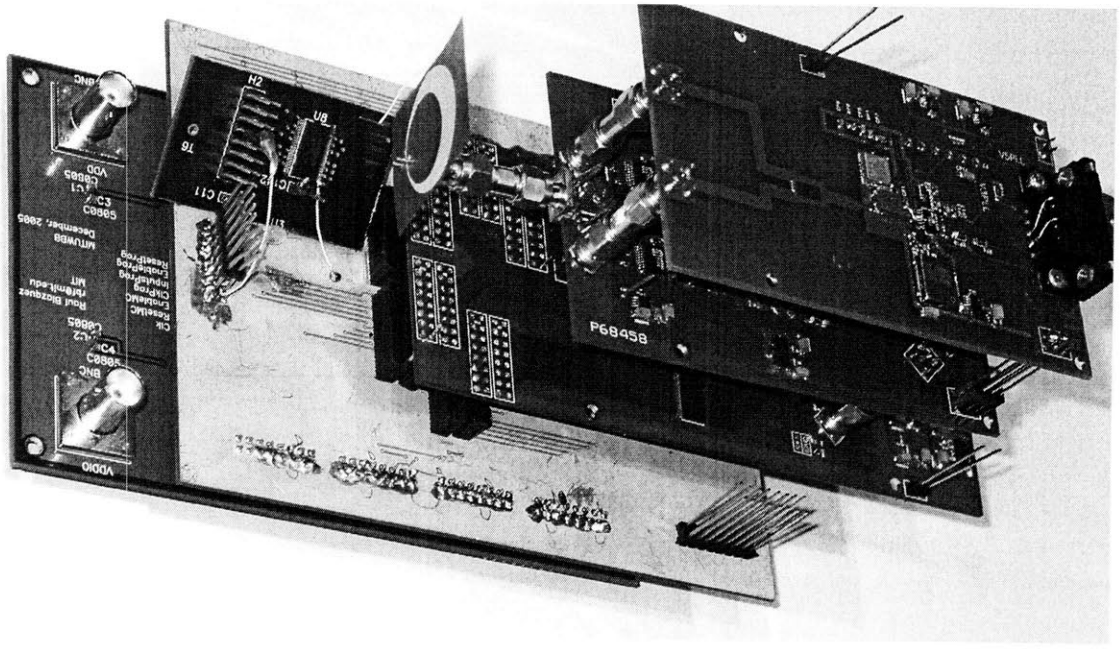


Figure 2-23: Photo of board stack.

code 19 times, which is used by the digital baseband to detect the presence of the packet and to achieve packet acquisition. The larger time interval between pulses in the preamble allows the receiver to estimate the channel impulse response without significant inter-symbol interference (ISI) for a worst-case multi-path channel environment. The payload is comprised of 4K pulses transmitted with a pulse repetition frequency of 100 MHz. Since each bit of information is represented by one pulse, this system transmits at a raw data rate of 100 Mbps. At the start of the payload, a known sequence of 32 bits is included to mark the beginning of the payload. Including a 10 μs guard time between packets, a complete packet transmission occurs in less than 100 μs.

Figure 2-25 shows the BER plots of acquired packets. A 6 dB difference in link margin is observed between the lowest and highest frequency channels. This is due to increased front-end NF at higher frequencies, as well as reduced front-end conversion gain which causes the baseband gain stages to contribute more noise at the higher frequency channels. Figure 2-26 shows the bit-scaling effects on BER. 4 dB of margin in the link budget can be recovered when the ADC resolution is scaled from 1 to 5

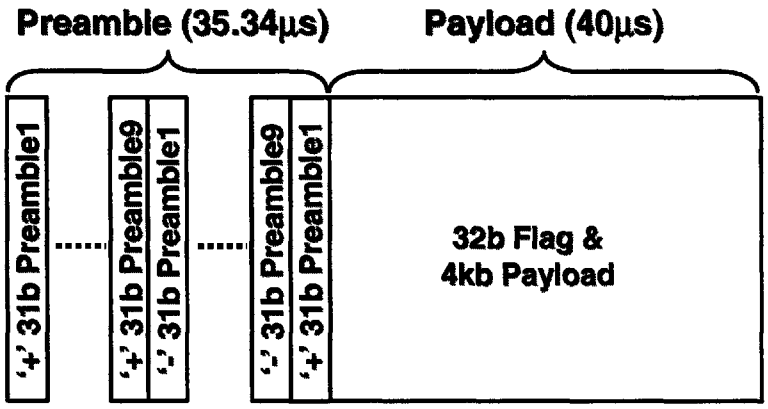


Figure 2-24: Packet structure.

bits. A power savings of 40% in the ADC can be observed when it operates in the 1-bit mode. For a 10,000 packet trial, 80% of the packets are acquired in a high SNR environment. The receiver operates at 3.2 nJ/bit and demonstrates a 6 m wireless link in a laboratory line-of-sight configuration.

2.7 Summary

An RF front-end discrete prototype is built in the context of a full system prototype to allow end-to-end system testing and "swap-and-test" design of a UWB transceiver. System design, circuit implementation, and hardware verification for a packaged 3.1–10.6 GHz UWB RF front-end is performed, and a wireless BER of 10^{-3} is achieved at a -84 dBm sensitivity that matches theoretical calculations. The tradeoffs of an un-matched LNA in the context of a wireless system is verified. The switchable notch filter demonstrates the ability to attenuate known in-band interferers. The filter improves SINR by 3 dB and BER performance by more than an order of magnitude. Finally, I led the assembly, debugging, and successful demonstration of a full system that received wireless packets for a video demo.

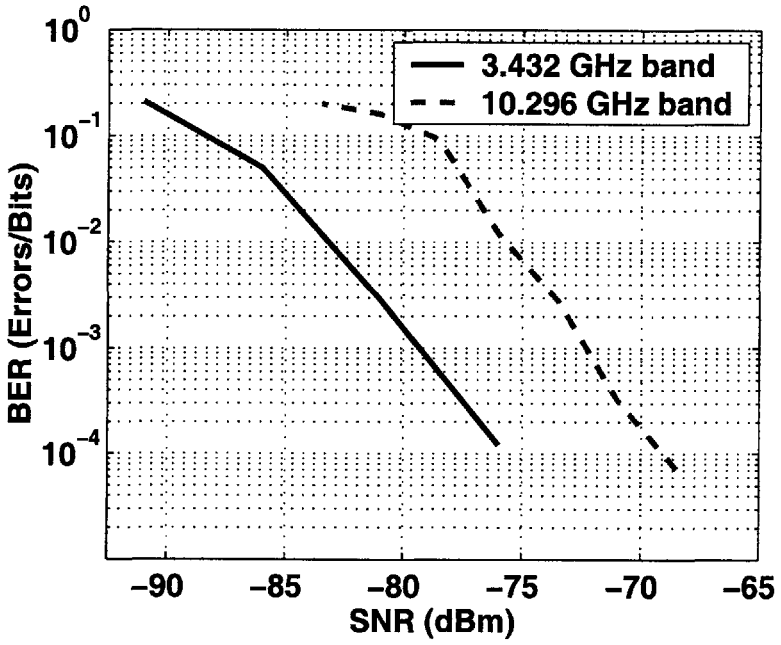


Figure 2-25: BER vs. SNR.

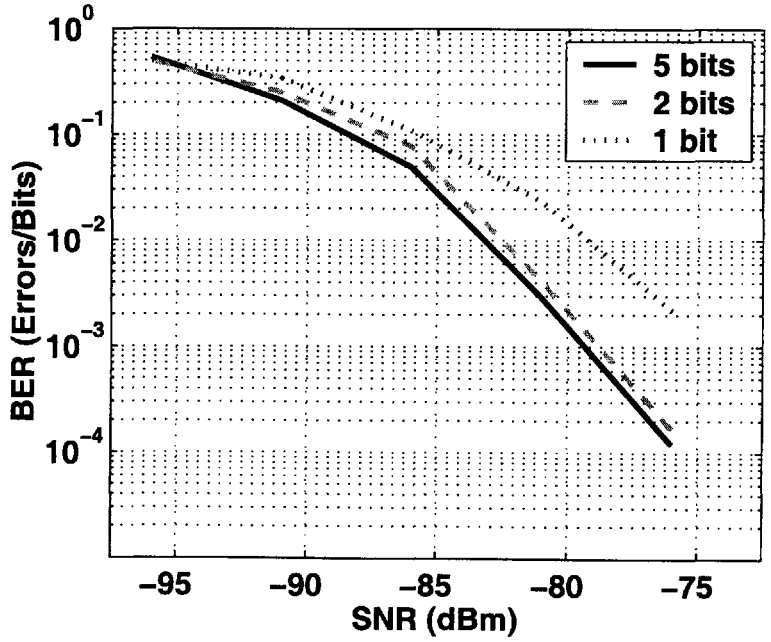


Figure 2-26: Bit-scaling effects on BER waterfall curves.

Chapter 3

Architectures for a Low Data Rate FCC Compliant UWB Receiver

With portable electronics and wireless sensor networks becoming increasingly pervasive, energy efficient radios have become an active area of research [44, 45, 46]. Though sub-nJ/bit data reception is achievable for data rates $\geq$100 Mbps using optimized coherent architectures [47], there is a need for simple, low-cost, low-power, and scalable radios as specified in the IEEE 802.15.4a task group [48]. This work explores the unique properties of FCC-compliant pulsed UWB signals and scaled CMOS devices to improve energy/bit of existing low data-rate GHz-range integrated radios.

3.1 Background and Previous Work

Wireless sensor networks are comprised of many sensor nodes distributed across a targeted landscape. Each node is equipped with sensors, algorithms, processors, and a radio that connects it to other nearby nodes for the purpose of deeply distributed environmental data harvesting. A top-level Multiple Access Control (MAC) layer coordinates the global energy minimization and data flow of the entire network [49]. Typical specifications for a wireless sensor node are outlined in Table 3.1.

Low power consumption has been a challenging design goal of wireless sensor nodes. To provide the necessary functionality, a typical node (Figure 3-1) contains

Specifications	Typical Values
Data Rate	kbps to Mbps
Spatial Density	0.1–10 nodes/m^2
Transmit Distance	10–100 m
Extended Lifetime	$\geq$ 5 Years
Small Size	1 "AA" Battery

Table 3.1: Specifications of a typical wireless sensor network.

four main blocks: sensor/ADC, DSP, radio, and power source. For the node to become energy autonomous and rely solely upon energy scavenging, energy efficiency becomes a key parameter. The efficiency of each block can be measured in terms of energy/conversion for the sensor/ADC (~200 fJ/conversion step), energy/operation for the DSP (~10 pJ/operation), energy/bit of the radio (~10 nJ/bit), and power conversion efficiency (~90%). It is apparent that the most power-hungry element is the analog/RF portion of the radio that customarily operates at steady-state operating points for amplifying and manipulating small signals. These operating points usually require a constant bias current. Many low power design techniques have been demonstrated to reduce the power consumption of such radios and analog circuits. Some examples are sub-threshold LNAs enabled by parallel resonant networks [50], low voltage ($\leq$1 V) LNAs enabled by series resonant networks [51], transformer feedback LNAs [52], stacked improved-Q on-chip inductors [53], circuits that use simple post-processing manufacturing techniques to increase the Q of inductors [54], circuits that employ advanced high-Q materials such as bulk acoustic wave (BAW) resonators and film bulk acoustic resonators (FBAR) [44] [55], and circuits that leverage improved process characteristics such as increased f_t and reduced parasitics to design low power RF circuits at center frequencies that have not changed much over the past 10 years [56] [57] [58], with the omission of recent efforts towards $\geq$60 GHz radio.

A high capacity 2,500 mA·h "AA" battery at 1.5 V contains 13,500 J of energy. For a node to operate five years on one "AA" battery, the average power consumption must be less than 85 μW. Figure 3-2 plots the energy/bit of recently published radio receivers and shows the dependency between achievable energy/bit and data rate.

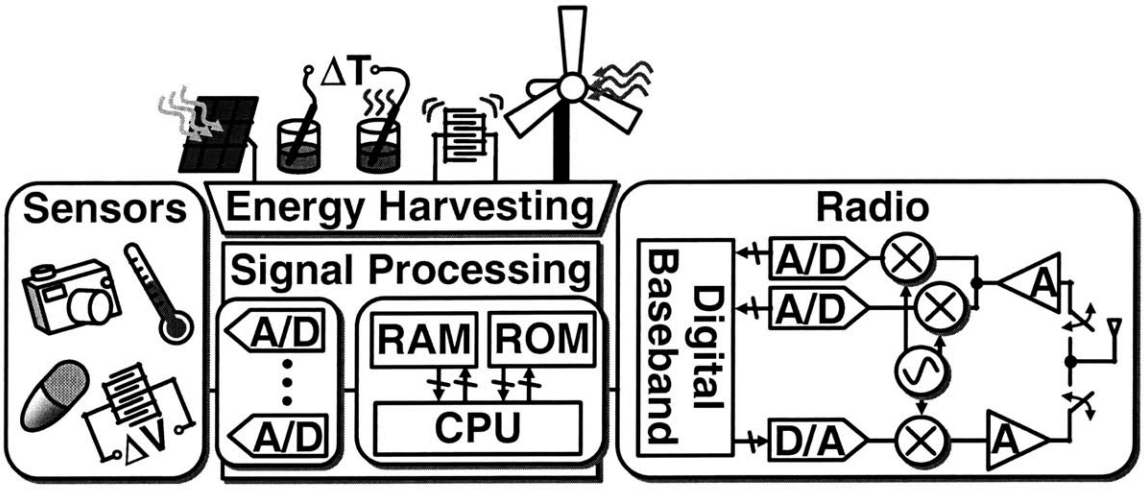


Figure 3-1: Wireless sensor node.

Table 3.2 shows the details of each receiver in Figure 3-2.

At the highest data rate of 480 Mbps shown in Figure 3-2, a WiMedia [68] compliant UWB receiver achieves an energy/bit of 0.68 nJ/bit [47]. At the lowest data rate of 5 kbps, a super-regenerative receiver [44] achieves 80 nJ/bit. This direct tradeoff between data rate and energy/bit is because the fixed cost of analog/RF bias currents in the receiver become amortized over more bits/sec as data rate increases. Furthermore, the trend line formed from the non-coherent architecture data points are lower than that formed by coherent architectures. This is primarily due to the costly nature of phase tracking necessary in coherent architectures for demodulation. By avoiding signaling schemes that encode data in the phase, high performance PLLs and backends are not required for complex phase and time tracking; henceforth, power consumption is reduced. Regarding signaling for non-coherent architectures, there are three prominent phase-independent methodologies: on-off-keying (OOK), frequency-shift-keying (FSK), and pulse-position modulation (PPM). Papers [64], [44], [69], and [70] are super-regenerative receivers that utilize OOK signaling. These receivers do not require a PLL, thereby saving power. The work outlined in [67] affords similar energy savings as the super-regenerative architecture by operating with a 20 dB NF system specification, thereby allowing the LNA to be realized in sub-threshold and

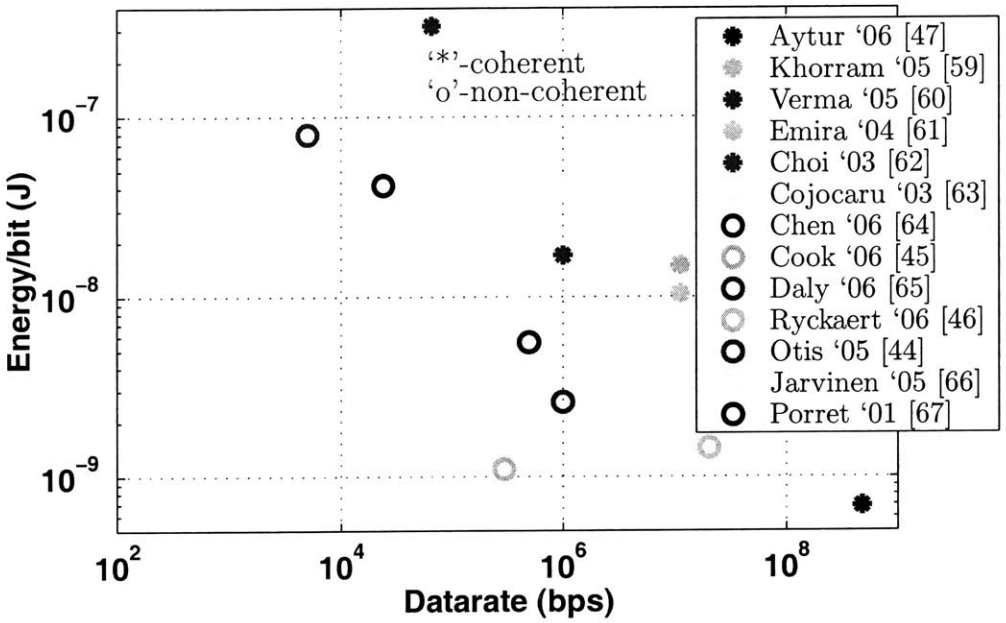


Figure 3-2: Energy per bit ratios for recent wireless receivers [3]

Paper	**Mod.**	**Sens.**	**Rate**	**Power**	**nJ/bit**
Aytur '06 [47]	MB-OFDM	-71 dBm	480 Mbps	330 mW	0.68
Khorram '05 [59]	802.11b	-88 dBm	11 Mbps	165 mW	15
Verma '05 [60]	DBPSK	-75 dBm	1 Mbps	17 mW	17
Emira '04 [61]	802.11b	-86 dBm	11 Mbps	114 mW	10.4
Choi '03 [62]	GMSK	-82 dBm	66 kbps	21 mW	318
Cojocaru '03 [63]	2-GFSK	-91 dBm	1 Mbps	39 mW	39
Chen '06 [64]	OOK, AM	-80 dBm	500 kbps	2.8 mW	5.6
Cook '06 [45]	2-FSK	-98 dBm	300 kbps	330 μW	1.1
Daly '06 [65]	OOK	-65 dBm	1 Mbps	2.6 mW	2.6
Ryckaert '06 [46]	PPM	N/A	20 Mbps	29 mW	1.44
Otis '05 [44]	OOK	-100 dBm	5 kbps	40 mW	80
Jarvinen '05 [66]	2-GFSK	N/A	333 kbps	3.4 mW	10.2
Porret '01 [67]	FSK	-95 dBm	24 kbps	1 mW	41.7

Table 3.2: Recently published receiver details.

Frequency (kHz)	ppm	Power (mW)	Type
32.768	$0.04/\Delta^oC$	0.001	Crystal
32.768	30	0.0264	Oscillator
70,000	50	0.1	Crystal
100,000	50	0.5	Crystal
19,440	1.5	4.5	TCXO

Table 3.3: Typical specifications of clock references [5].

the power requirements to be reduced. Paper [46] uses analog correlation and UWB PPM signaling to achieve low energy/bit, but only at a moderately high, fixed data rate. Paper [45], similar to [67], increases the modulation index of the FSK receiver to relax PLL and demodulation requirements. It also combines the aforementioned concept with an efficient method of achieving signal amplification through resonance, and thereby achieves an energy/bit measurement much lower than the non-coherent trend line.

Though Figure 3-2 reveals energy/bit as calculated by dividing the power by the data rate, it does not include two other important elements that contribute to receiver energy consumption, namely: the power required by the clock source reference for a given ppm frequency offset tolerance, and the energy consumed during receiver acquisition. In the architectural design, it is important to consider topologies that do not require a high speed crystal reference with stringent ppm requirements. Table 3.3 shows the average power consumption of crystals and their associated ppm. With shorter packets and a non-coherent architecture, it is possible to tolerate a larger ppm specification without significant impact on BER performance. For a low power architecture that could accommodate it, a 1 μW crystal at 32.768 kHz would consume less than 1.2 % of the total power budget. With shorter packets, the energy consumption during synchronization becomes more significant. Thus, it is of equal (if not more) importance to design the system, signaling, and circuits such that the time to achieve coarse acquisition is minimized.

The 802.15.4a task group focuses on creating a standard for low data rate, low energy wireless communications systems with precision ranging. Much of the prior

work in low data rate wireless sensor networks using UWB signaling can be found in this group, whose activity dates back to November 2002. There are numerous proposals for transceiver systems that have been submitted to the group; this section will review three of the more prominent architectures, ordered by increasing minimum E_b/N_o requirements for achieving a fixed channel link quality.

3.1.1 Direct Sequence Spread Spectrum UWB Receiver

The Direct Sequence Spread Spectrum (DSSS) is based upon a coherent direct conversion receiver architecture very similar to high data rate systems proposed in 802.15.3a [71]. The UWB signals are appended one after another, exhibiting a $\geq$100 Mbps chip rate. The receiver demodulates these signals with a RAKE that approximates the optimal match filter receiver. Out of the three architectures that are discussed, this one affords the lowest E_b/N_o at a fixed channel link quality. To achieve lower data rates as required by the 4a task group, a group of pulses are gathered in a code for significant processing gain that can be leveraged in areas such as power consumption or range. However, the savings in power from relaxed circuit specifications are marginal compared to the power consumption of a high sampling speed ADC (at least 500 MHz), GHz-range PLL, and digital back-end that is processing the extremely fast chip-rate.

3.1.2 Transmitted-Reference Receiver

Transmitted reference (TR) signals are based upon the signaling structure shown in Figure 3-3. The pulses in the figure are 1.5 GHz wide Gaussian-shaped UWB pulses centered at 3.9 GHz. The first pulse is the reference pulse, whose phase does not change. The second pulse is the data pulse, and arrives ΔT seconds (in this example, 10 ns) after the first. ΔT needs to be larger than the expected impulse response of the channel. For a BPSK TR scheme, the phase of the data pulse is modulated by 0^o or 180^o relative to the reference pulse to represent a one or zero, respectively. To receive such a signal, two receive paths are created; one that is a real-time stream,

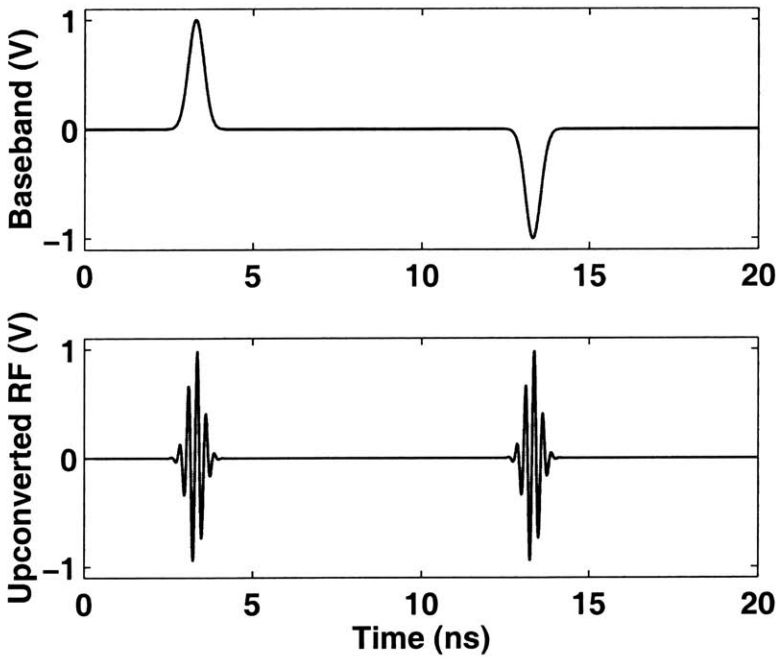


Figure 3-3: Transmitted-reference UWB signal. (a) Baseband Gaussian template. (b) Up-converted RF signal.

and the other that is delayed by ΔT. The two streams are then mixed together to correlate the data pulse with the reference pulse, and the output results in a 2:1 stream of demodulated pulses. Some drawbacks to TR signaling are that the system link budget is automatically reduced by 3 dB because a non-data reference pulse must be sent with a data pulse in a single data frame, and that TR receivers are also more susceptible to interferers relative to coherent UWB receivers. A major challenge in implementation is the ability to realize a multi-ns delay with ps accuracy in the receiver. Because the reference template is dirty/noisy, the E_b/N_o for TR receivers must be significantly larger relative to a coherent BPSK receiver for the same channel link quality; however, averaging in the TR receiver can reduce this difference at the cost of data rate [72].

Nonetheless, the advantages of this signaling scheme in its simplified transceiver architecture and ability to perform channel estimation in real-time analog may outweigh its challenges, if low power operation is desired [73]. There have been many variations and improvements on TR schemes, such as TR systems encoding data by

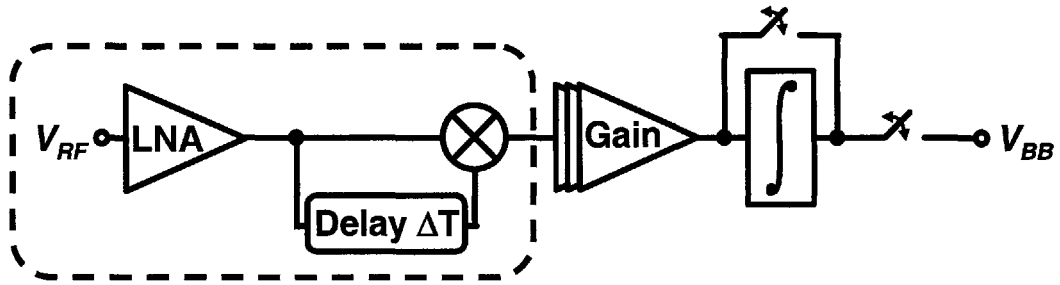


Figure 3-4: Transmitted Reference Architecture [4].

hopping the time delay between pulses [4], a signaling scheme that merges the data and reference bit into the same pulse [74], and methods to improve interference mitigation [75], but the basic concepts that afford a simple receiver architecture remain.

The next few paragraphs discuss the challenges of implementing the delay element in the receiver, and propose a new architecture that relax the design specifications of the delay while maintaining a low power solution.

Delay Generation in RF

Figure 3-4 shows the architecture for a basic TR receiver. The blocks within the dashed box are implemented in the RF domain. Implementing a ΔT delay on the order of tens of nanoseconds is very difficult at RF. A possible solution for implementing the delay is to cascade bandpass filters and build up sufficient group delay. However, further investigation shows that the group delay of a 3^{rd}-order 1.5 GHz Butterworth bandpass filter centered at f_{RF} is only hundreds of picoseconds – too small of a delay to practically implement a $\geq$ 10 ns delay. An all-pass filter with right-half plane zeros and corresponding left-half plane poles may seem like a good way to provide larger delays, but a first-pass implementation quickly reveals that process variation wreaks havoc on pole/zero placement. It seems that the only way to provide a reliable delay is through the use of transmission lines and possibly advanced materials with high dielectric constants.

Assuming that there is a method to achieve a ΔT delay, a more subtle issue is shown in Figure 3-5a. This figure shows the output of the integrator vs. the abso-

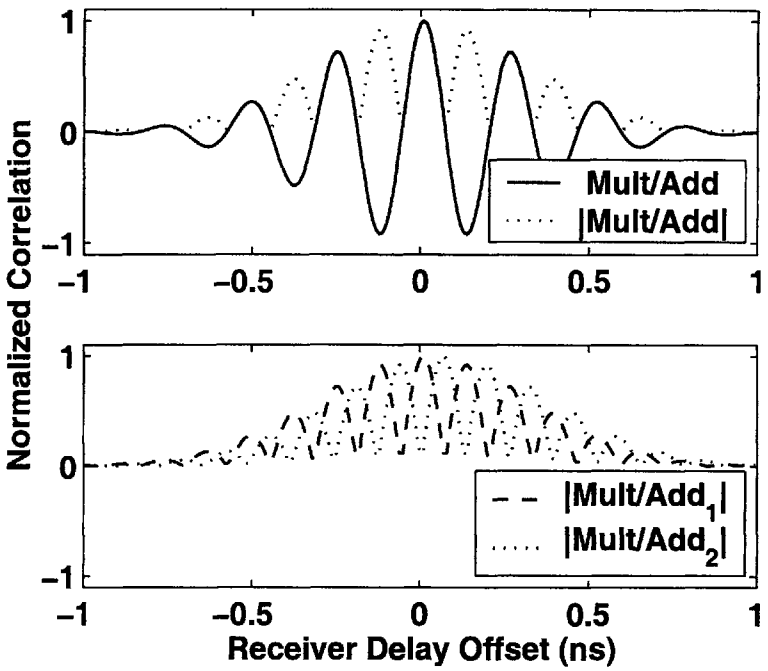


Figure 3-5: Transmitted-reference UWB signal. (a) Correlation output vs. ΔT_{TX}-ΔT_{RX}. (b) Energy envelopes for dual-RX path architecture.

lute difference in offset between ΔT_{TX} of the transmitter and $\Delta T_{RX}$of the receiver. Having swept this time difference from -1 ns to 1 ns, nulls in received pulse energy are observable. Taking the absolute value of the correlation reveals these nulls more clearly in a plot. A simple solution to the nulls would be to implement a parallel delay/mixer/integrator path after the LNA whose ΔT_{RX2} would be offset by $\frac{1}{4 \cdot f_{RF}}$ from the ΔT_{RX1} of the original path. Energy envelopes for the dual-RX path TR receiver are shown in Figure 3-5b. This dual-RX path architecture solution for addressing TR nulls in the receiver is reminiscent of how direct-conversion architectures must accommodate both I and Q down-conversion paths for full signal recovery.

A solution that would allow IC integration of the delay element in TR systems would be a mostly-digital, software-radio solution. In this architecture, a high-speed low-resolution sampler similar to the 14 Gsps 1-bit ADC in [76] would follow the LNA for direct-RF to digital conversion. The digitized signal thereafter would be easily manipulated in the digital domain. However, this architecture would also require an RF PLL clock driving the ADC at the sampling frequency. Though this is not

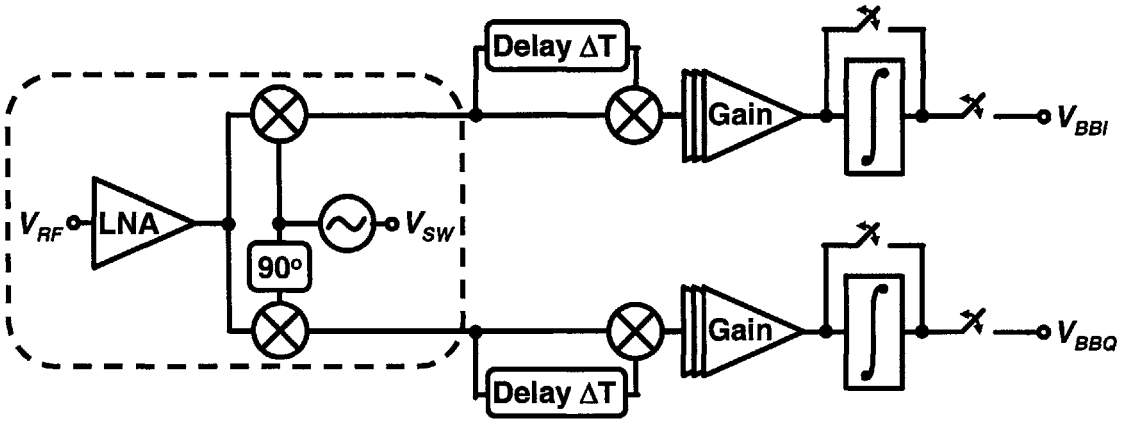


Figure 3-6: Improved Transmitted Reference – Baseband Delay Architecture.

a low-power solution compared to TR receivers that use analog delays built with passive transmission lines, the power consumption could be reduced if duty-cycled concepts were applied to such an ADC as in [77]. It is also important to note that the power consumption of a mostly digital receiver will scale more strongly with improved CMOS processes.

However, there is another solution presented in this work that would allow IC integration *and* low-power realization of the delay element in TR receivers: moving the delay operation to the baseband. The following section describes this architecture in further detail.

Delay Generation in Baseband

Figure 3-6 is the block diagram of the architecture that allows the ΔTdelay to be implemented in the baseband. This architectural improvement has not been found previously in the literature. The dashed box again denotes blocks that are implemented in the RF domain. The main enabling feature of this architecture is that of the duty-cyclable VCO. The VCO can be operated in open-loop, because the UWB signal spans a very large fraction of the ppm frequency offset. A simple simulation in Matlab shows that the tolerable clock offset can be in the 1000's of ppm for less than 1 dB energy loss when the signal is recovered using this architecture. The start-up time for the VCO is very quick, equivalent to X cycles of the RF center frequency,

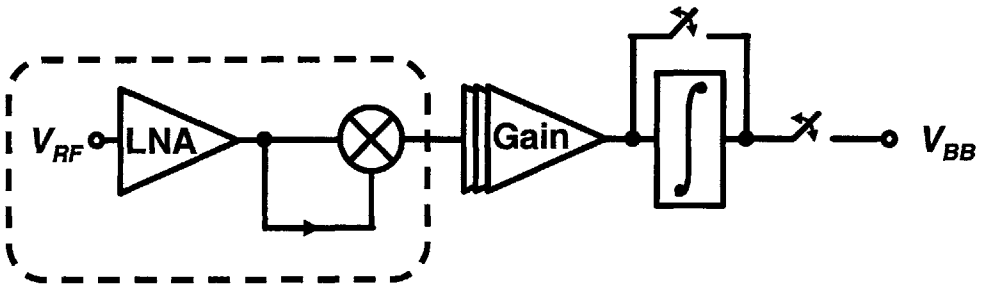


Figure 3-7: Self-Mixing Receiver Architecture.

where X is approximately the Q of the VCO tank.

The baseband delays can be realized in analog with very low power, since it is at low frequency. No inductors are required for the realization of these delay elements. A cascade of these stages can be embedded in a DLL-architecture to tune the ΔT delay to a high precision.

A trade-off can be analyzed and optimized between the baseband delay vs. the tolerable ppm oscillator offset. Larger signal bandwidths allow the receiver to tolerate larger ppm clock offsets. However, with larger signal bandwidths, the baseband delay would require more delay stages per required total ΔT, since filters with larger bandwidths and unchanged filter order achieve lower group delays.

Further system simulations to explore the mentioned trade-offs, effect of ΔT mismatch between both baseband delays, implementation of the baseband delay and tuning circuitry, and interference performance are necessary to determine the reliability of this architecture. Thus far, it seems to be a hopeful solution for complete IC integration of a low power TR receiver. However, there is one more architecture to consider.

3.1.3 Self-Mixing Receiver

The self-mixing receiver shown in Figure 3-7 is a simplification of the TR architecture [78]. By removing the delay altogether, we do not require the dual receive path and instead switch to PPM signaling. This results in a very simple, potentially low-power receiver that can be duty-cycled for extreme energy savings. In terms of

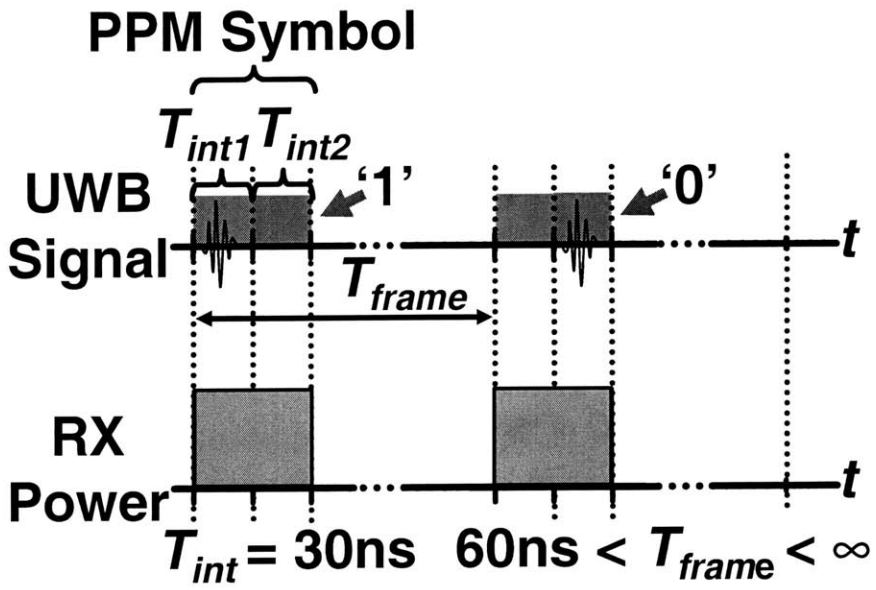


Figure 3-8: 2-PPM signal.

required E_b/N_o for a given QoS, the self-mixing non-coherent receiver operating on 2-PPM signals requires 10 dB extra margin to perform the same as a coherent BPSK receiver. This architecture is chosen for implementation as it shows the most promise for achieving low energy/bit.

3.2 Signal Choice and Band Plan

Stemming from the architectural choice of a self-mixing receiver, a non-coherent binary PPM scheme is chosen for its signaling. Figure 3-8 shows a binary PPM signal, its associated timing variables, and receiver power profile. In binary PPM, the 2 ns UWB pulse (corresponding to a 500 MHz signal bandwidth) can be placed in one of two time slots: T_{int1}, or T_{int2}. If the pulse arrives in T_{int1}, then a one is declared by the receiver. If the pulse arrives in T_{int2}, then a zero is declared. Though the UWB pulse is only 2 ns wide, T_{int} is set to 30 ns such that the worst-case multi-path channel and crystal frequency offsets can be tolerated. As can be seen, the data rate is scaled simply by changing the receiver off period between each PPM symbol. Because the

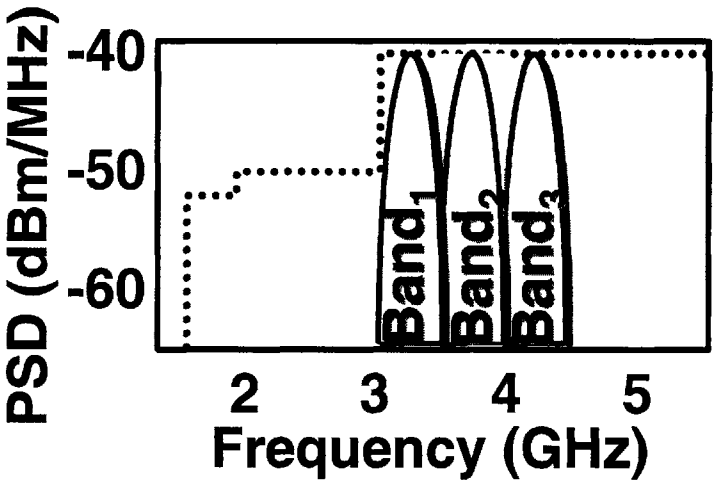


Figure 3-9: Band plan.

data rate is adjusted only by changing the duration of the off period, the receiver is designed so that it can be quickly shut on/off so that no power is consumed during the time between symbols, thereby exploiting the energy savings opportunities inherent in the signaling. To relate these effects of these savings on energy/bit, the amount of energy required to demodulate one bit does not change with data rate, thereby allowing us to realize a data rate independent energy efficiency for the radio. The maximum data rate of this architecture is 16.7 Mbps when $T_{frame} = 60$ ns and one bit is encoded in each frame.

In determining the band plan, the choices for signal bandwidth span between 500 MHz to 1.5 GHz. The advantages of using 1.5 GHz of bandwidth are that the pulse width is reduced by a factor of three, the receiver front-end is more simple to design, and the peak pulse amplitudes are maximized, thereby providing the greatest received SNR. However, the probability of experiencing an in-band interference is higher with a larger bandwidth, which can drastically degrade receiver operation. By choosing a subbanded architecture, the tradeoff becomes transmission distance vs. interference robustness. Figure 3-9 shows the band plan of this work. The following chapter details the circuit techniques and designs used for this receiver architecture.

Chapter 4

Circuits for a Low Data Rate 0–16.7 Mbps, 3.1–5.0 GHz FCC Compliant UWB Receiver

This chapter outlines the implementation details, circuit techniques, and measurements of the UWB low data rate self-mixing receiver system implemented in a 90 nm digital CMOS process that is extremely suitable for low power, low data rate wireless systems. Operation at 0.5 V and 0.65 V, rapid duty-cycling, and the low power relative-compare backend at 0.5 V are described in detail.

4.1 Receiver Architecture and Functionality

Figure 4-1 shows a simplified block diagram of the proposed non-coherent receiver architecture that is comprised of a 3–5 GHz subbanded RF front-end, a passive self-mixer, and a low power mixed-signal baseband [79]. The non-coherent architecture does not require a PLL, and the fastest clock frequency required by the receiver is 33 MHz for operation of the mixed-signal baseband. For out-of-band noise/interference robustness, the RF front-end performs channel selection in the 3.4, 3.9, and 4.4 GHz bands. More than 99% of the total power consumption in this receiver comes from the LNA gain stages. By switching on the receiver only during

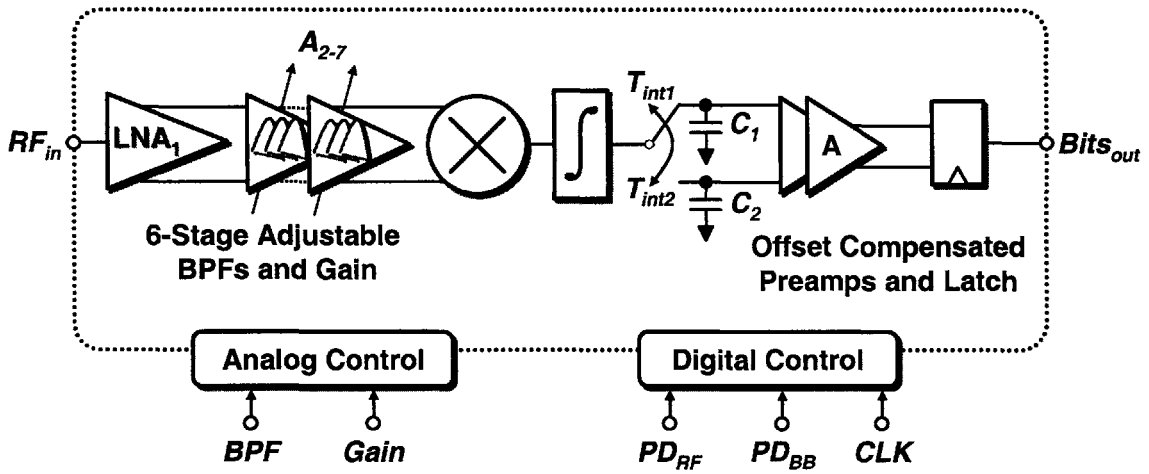


Figure 4-1: Self-Mixing Receiver Architecture.

the 60 ns PPM symbol, deep energy savings are possible by duty-cycling the receiver. The non-coherent receiver uses a mixed-signal relative-compare baseband to determine the bit. For bit-slicing, a low-power sample-and-hold (S/H) capacitor network stores analog integration results during T_{int1} and T_{int2} onto separate capacitors C_1 and C_2, respectively. Thereafter, two cascaded offset-compensated preamplifiers and a latch perform a relative-compare on the two capacitor voltages to evaluate the received bit. It can be seen that this scheme inherently performs dc-offset compensation and pre-integrator signal-path normalization due to the relative-compare. In this way, PPM signals are easily and reliably demodulated. For high-speed demodulation up to $1/2 \cdot T_{int}$ =16.7 Mbps, the integrated quad-capacitor baseband is described in Section 4.1.2. The entire receiver can operate at 0.5 V or 0.65 V, and is implemented in a 90 nm CMOS process.

4.1.1 RF Front-end

The RF front-end consists of an LNA, six RF gain stages, and passive self-mixer as shown in Figure 3-9. Each of the six amplifiers contain a 2^{nd} order bandpass filter for channel selection. The front-end also provides sufficient gain (40 dB) to overcome the $V_{out} = k \cdot V_{in}^2$ transfer characteristic of the self-mixer for small inputs. The single-to-

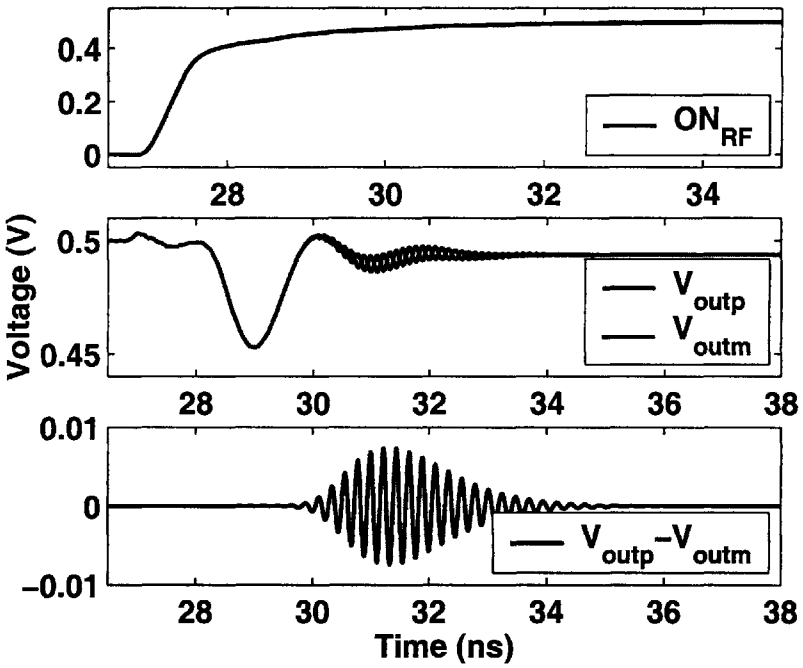


Figure 4-2: Simulated RF front-end switching transient characteristics.

differential conversion is done in the first stage so that the remaining LNAs with high CMRR equalize and condition the differential signal. The LNAs and passive mixer are DC coupled and chain-biased so that duty-cycling does not cause long-settling transients. Figure 4-2 shows the transient switching effects on the RF front-end. ON_{RF} switches the front-end on/off. The front-end outputs dip for 2 ns due to currents charging the inductors, and transient settling behavior is seen. When the differential output is taken, a negligible low amplitude (10 mV) transient is observed, which is 5x smaller than the amplified RF voltage of the minimum detectable signal.

4.1.2 High-speed Baseband

To achieve rapid coarse acquisition during the preamble search, adjacent integrations for continuous bit decisions are needed. Figure 4-3 shows the implemented baseband block diagram and the corresponding operation schedule. The four capacitors are rotated among three states *reset*, *integrate*, and *evaluate bit* to achieve integrations every T_{int}. Two offset-compensated relative-compare paths ($Decision_1$ and $Decision_2$) swap between *evaluate* and *reset* modes to provide a continuous stream

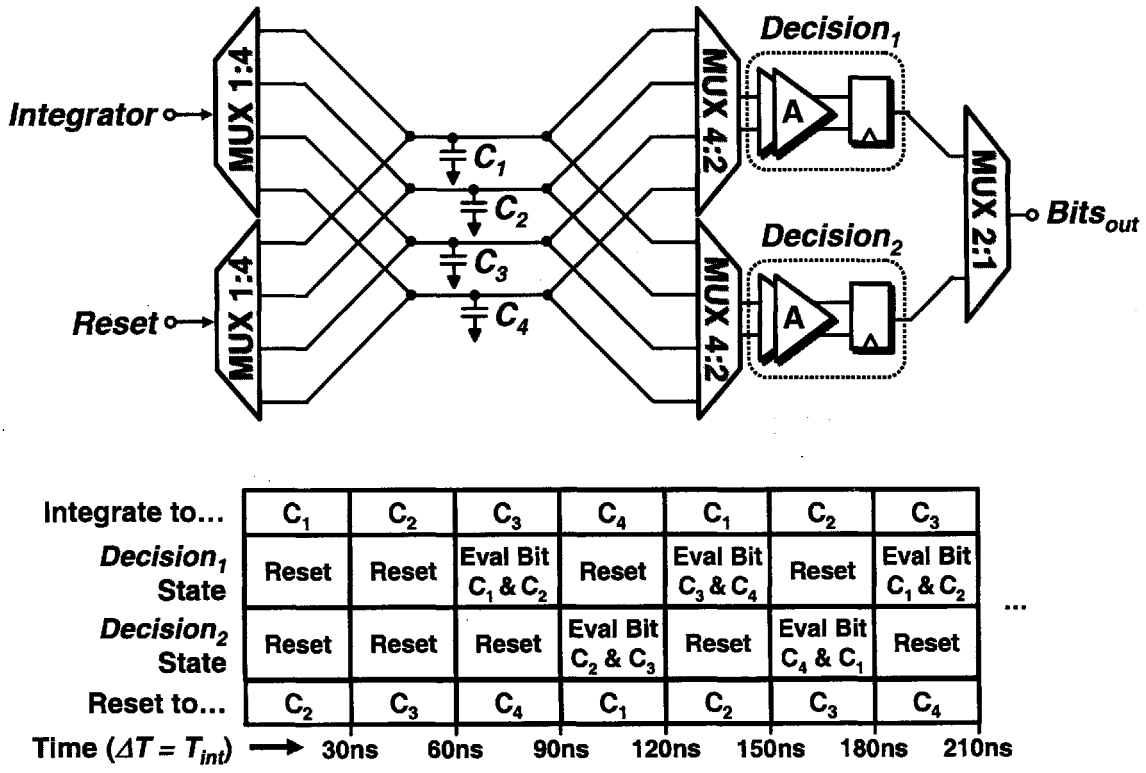


Figure 4-3: High-speed Baseband.

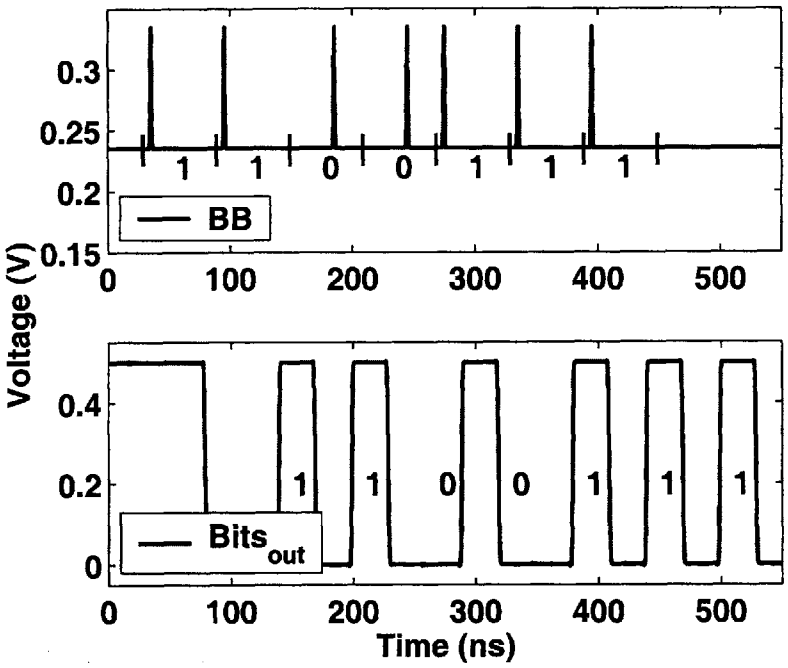


Figure 4-4: Simulated Baseband demodulator operation: $Bits_{out}$ with BB pulse input.

of bit decisions every $T_{int} = 30\ ns$. The pipeline delay for a bit decision to appear at the output from the end of a PPM symbol integration time is 45 ns. The fastest clock required to operate the entire receiver is $1/T_{int}$, or 33.3 MHz. Figure 4-4 plots the simulated operation of the implemented relative-compare baseband providing adjacent bit decisions every 30 ns.

4.2 Circuits

4.2.1 LNA and Gain Stages

The circuit schematic for the LNA is shown in Figure 4-3. Many essential functions are embedded in this amplifier. This block operates between 0.5 V and 0.65 V. The structure of this circuit is based upon a common-gate single-to-differential conversion architecture, with core transducers M_2 and M_3. Single-to-differential conversion is necessary to operate the self-mixer. Performing this operation in the first stage im-

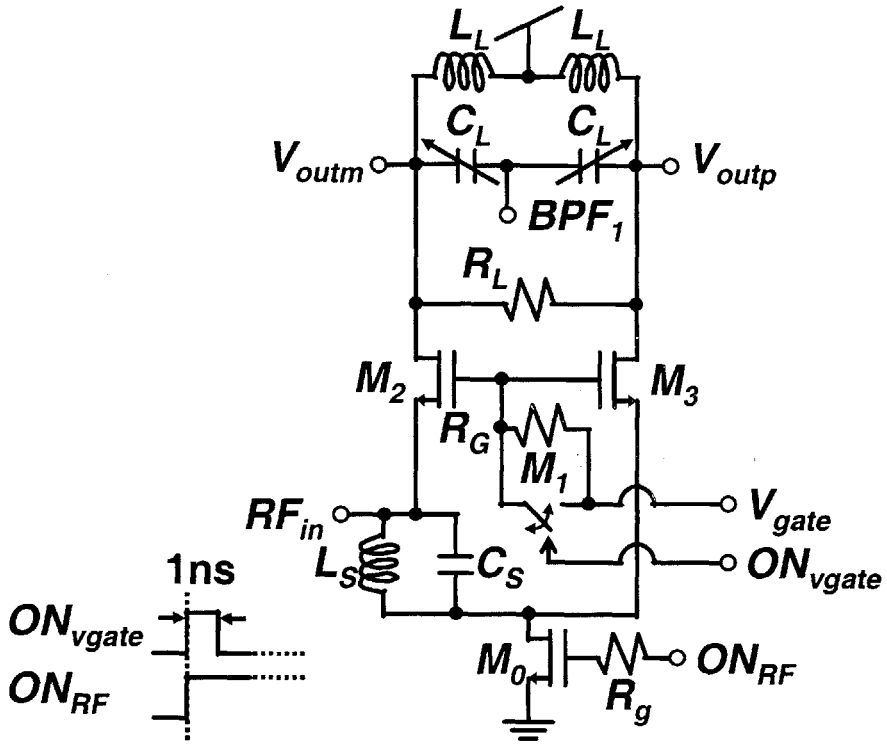


Figure 4-5: *LNA*.

pacts the NF significantly. However, if the conversion is done in the last stage, the signal no longer qualifies as "small-signal," and requires a highly linear, high dynamic range block, which is unrealistic for low-voltage circuits. Furthermore, power supply and substrate noise directly couple and appear inline with the signal for single-ended circuits. Therefore, for the sake of signal fidelity and reducing the number of nodes that are sensitive to power supply and substrate noise, the single-to-differential conversion is completed in the first stage and the effect on NF is accounted for in the link budget. Furthermore, because the conversion needs refinement, the following six LNA gain stages equalize the conversion by utilizing their associated high CMRR. A differential amplifier with one input grounded could suffice as a converter; but since this is the first stage, additional reactive elements for matching and diodes for ESD protection would need to be added, thereby undesirably increasing circuit complexity. Thus, a back-to-back common-gate architecture is used to meet the converter requirements by floating the common gate connection during small-signal amplification and allowing the series capacitive divider to invert the signal across C_{gs} of M_2 and M_3. The circuit also provides ESD protection from the inherent source-bulk diode contained in M_2.

The input match is easily met by $1/g_m$ of M_2, as the 0 V current source formed by the $L_S C_S$ parallel resonance forces most of the RF current into $1/g_m$ of M_2. A parallel resonance that forms the load also consumes zero volts of headroom, thereby allowing this LNA structure to operate with only a 0.65 V supply without saturating active transistors M_2 and M_3. Because $1/g_{ds}$ of M_2 is not large enough to be ignored, the gain of the amplifier also affects the input impedance as well. To address this issue, the LNA is designed to have a 1.5 GHz bandwidth by de-Qing the load with resistor R, so that the desired S_{11} is achieved all at once, without requiring channel-to-channel tuning to support the subbanded architecture. Subbanded channel selection is thereby delegated to the following six gain stages. To account for process variations, the DC bias for the transistors and load varactors are tunable through V_{gate} and BPF_1.

The energy savings during the data payload are realized with aggressive duty-cycling between pulses. Figure 4-6 shows how the LNA is dynamically biased and

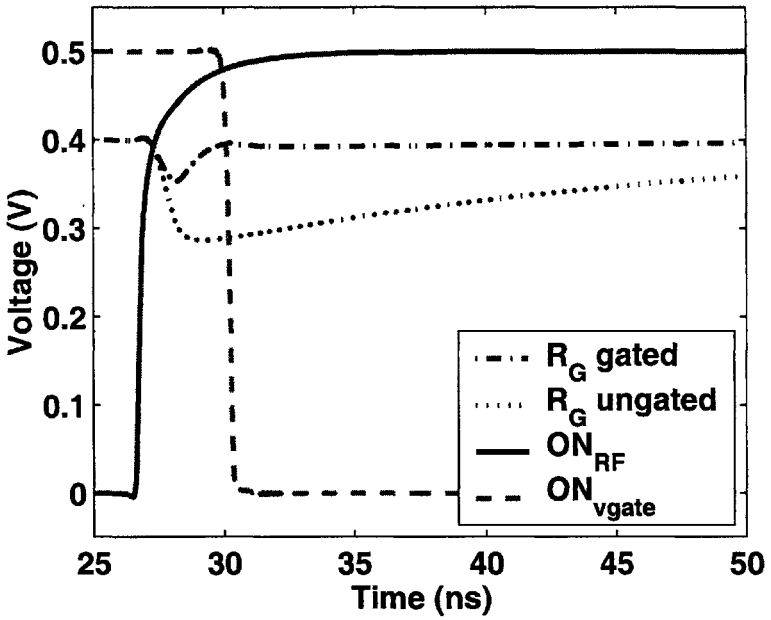


Figure 4-6: Simulated LNA transient characteristics.

switched on within 2 ns. To turn the amplifier on, ON_{vgate} is first flashed high to relay the gate voltage, V_{gate}, with low impedance. 5 ns after, ON_{RF} is switched high, and for 2 ns, ON_{vgate} and PD_{RF} are both high. Thereafter, ON_{vgate} is switched low, and the amplifier has reached its operating point and ready to amplify RF signals. R_g provides the necessary damping so that the signal driving ON_{RF} does not appear under-damped. Because the LNA is virtually symmetrical, switching M_0 does not cause significant differential mode excitation. For any differential perturbations, the settling time is dictated mostly by the effective time constant seen at the load. For a 1.5 GHz bandwidth, one time constant is approximately 100 ps. To minimize leakage currents when the amplifier is off, the length of M_0 for all the amplifiers is sized 2x minimum length.

Figure 4-7 shows the circuit schematics for A_{v1-6}. All of these amplifiers acquire their DC input voltage bias from the preceding amplifier's DC output voltage (a short to power through the load inductor). All of their loads are identical; thus, the control voltage to all the varactors, BPF_2, can be routed with one external analog voltage. Each stage provides an identical 6 dB of gain and can be tuned to any one of three subband channels at 3.4 GHz, 3.9 GHz, and 4.4 GHz. The tunable bandpass

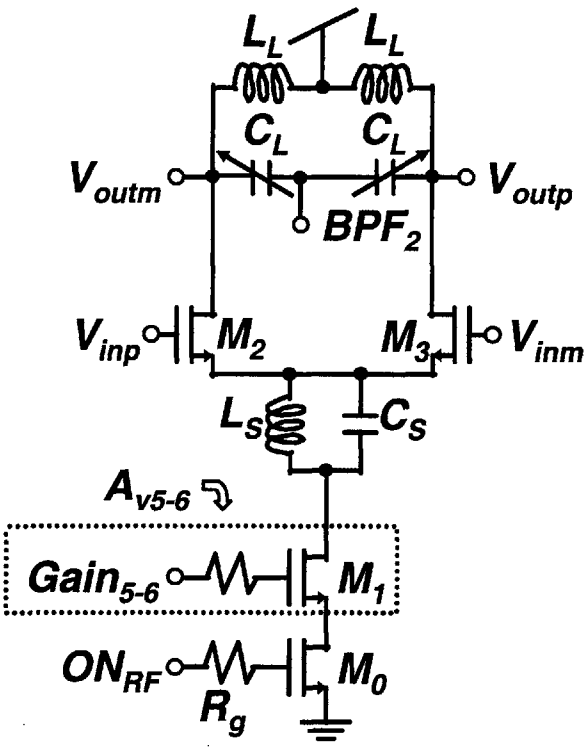


Figure 4-7: A_{v1-6}.

filter load is formed by a differential inductor L_L and varactor C_L, and has a tuning range of over 1 GHz. Gain stages A_{v5-6} have power scaleable, bandwidth independent gain control. Because the input gate voltages of each amplifier are DC biased to the power supply through the load inductors of the prior stage, large capacitances are not charged/discharged during power on/off – only the parasitic capacitances at the drain of M_0 are charged/discharged.

High CMRR is achieved in all of the amplifiers through the parallel $L_C L_S$ resonance. Figure 4-8 shows a drastic improvement in CMRR with the inclusion of $L_S C_S$ than without. PSRR is likewise improved. Monte Carlo simulations (to observe non-ideal cancellation of power supply noise due to mismatch) of the differential output gain from the power supply are shown in Figure 4-9. A 10 dB improvement is shown with the inclusion of $L_S C_S$. Like the LNA, these amplifiers can be switched on and settle at their operating points within a few nanoseconds. For A_{v5-6}, an additional transistor, M_1, is inserted in series with M_0. This serves as a method to

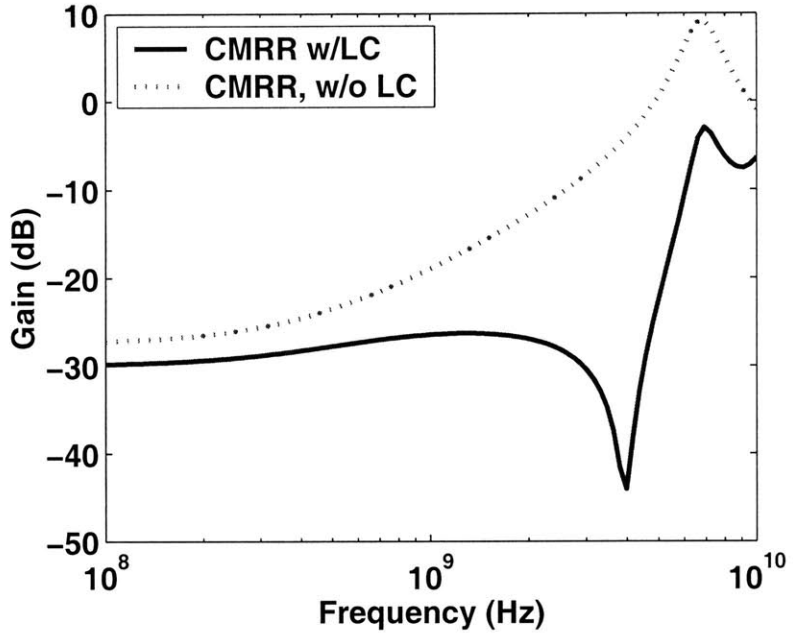


Figure 4-8: Plot of CMRR with and without $L_S C_S$.

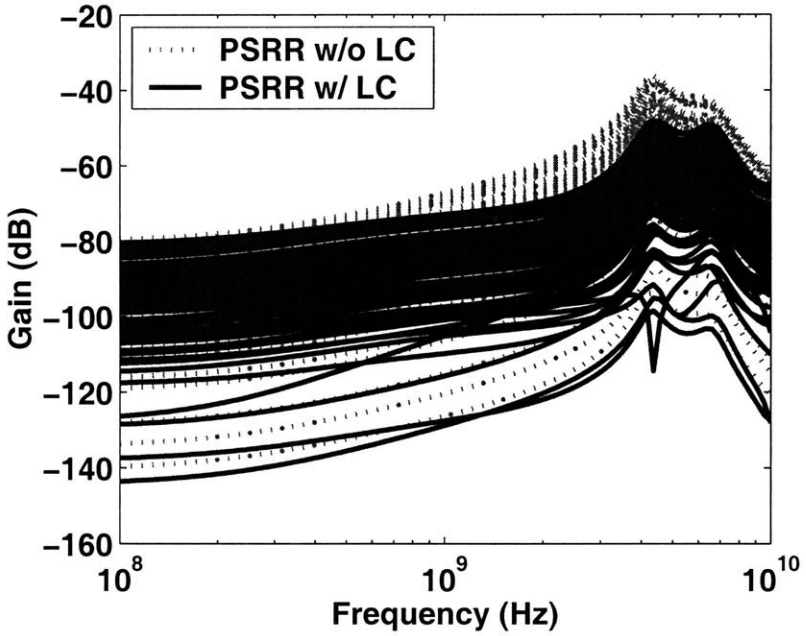


Figure 4-9: Monte Carlo plots of PSRR with and without $L_S C_S$.

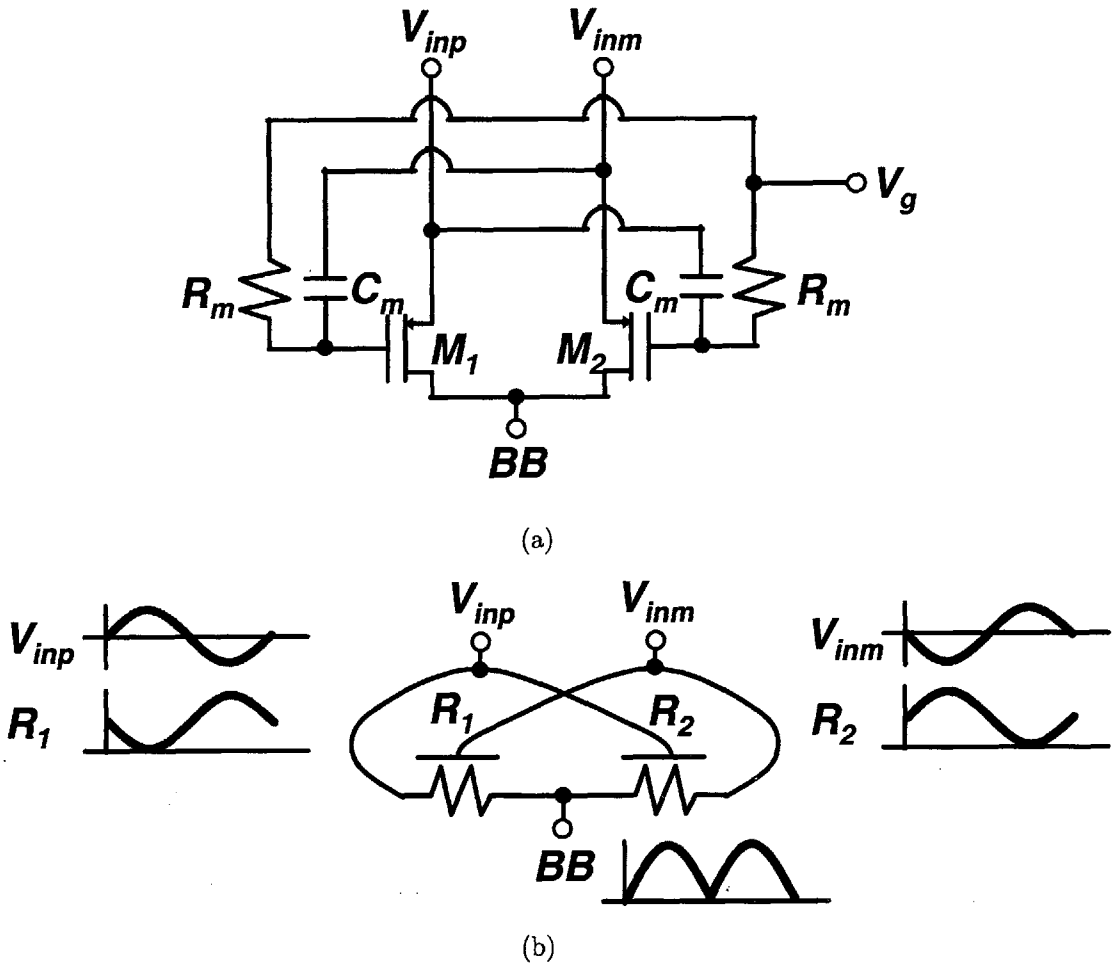


Figure 4-10: (a) Self-mixer and (b) equivalent model.

provide bandwidth-independent, power-coupled gain control. If less gain is required, the current through A_{v5-6} can be gradually choked using M_1, thereby saving power and providing the necessary functionality for gain control without affecting channel selection and bandwidth (which is embedded in $L_L C_L$).

4.2.2 Self-Mixer

In the passive self-mixer shown in Figure 4-10(a) M_1 and M_2 are used as voltage-dependent resistors (Figure 4-10(b)). The DC voltage for the source and drain of these transistors are derived from the DC output voltage of the previous amplifier stage (a short to power through the load inductor and through the transistors of the mixers themselves). Both PMOS and NMOS versions of this mixer are simulated, and

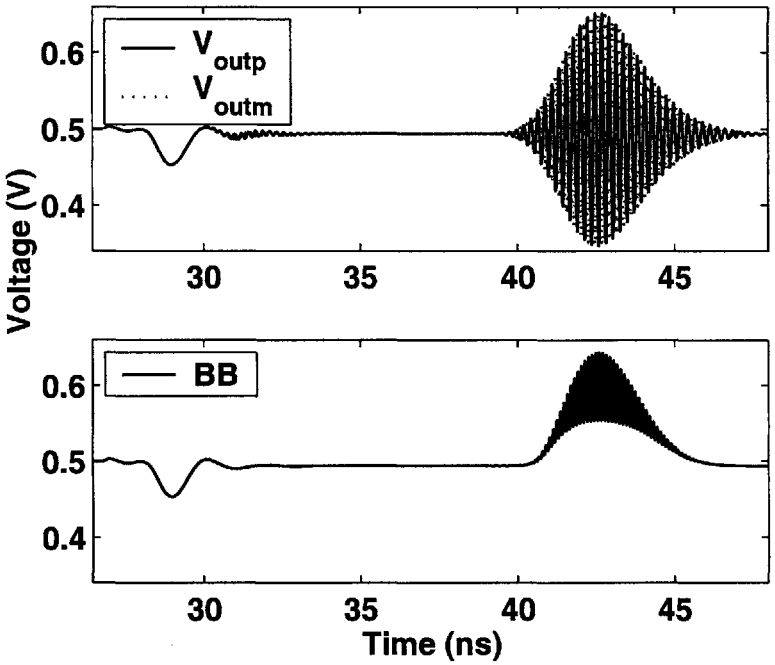


Figure 4-11: Simulated mixer transient characteristics.

superior noise performance is obtained with the PMOS version. The maximum gain through the mixer occurs when V_{GS} of the transistors are biased close to V_T of the transistor. This occurs, because it forces the input to traverse through the transistors' largest non-linearity (the transition from sub-threshold to above-threshold operation), and thereby traverse a larger difference of channel resistance between M_1 and M_2. The passive self-mixers produce the best performance regarding ultimate SNR ratio at the output of the mixer among all possible energy detectors that were considered, and also fits well with low-voltage RF design. The single-ended output of the mixer also lends itself to the baseband circuitry that follows. Figure 4-11 shows a simulated transient operation of the mixer.

4.2.3 Baseband Integrator

Because analog circuits become more difficult to design with decreasing voltage headroom, careful co-design of simple, distributed circuits to realize the desired system level behavior allows for low voltage, and low power operation. At baseband, the

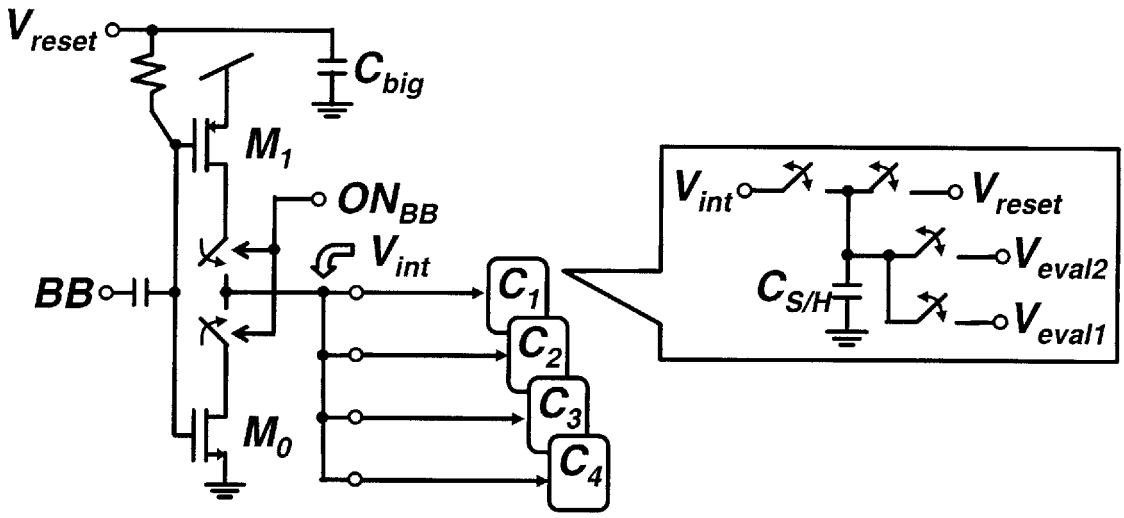


Figure 4-12: Integrator and S/H capacitors.

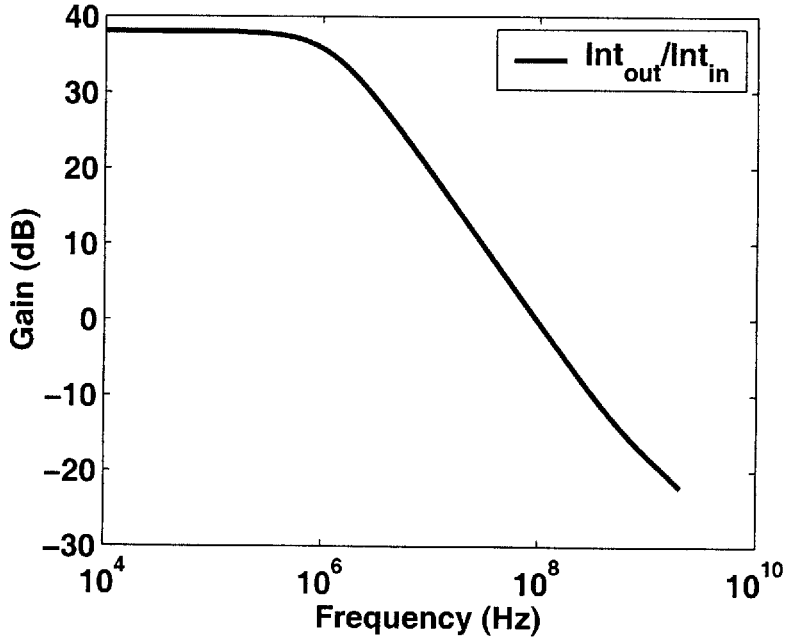


Figure 4-13: Simulated integrator AC response.

integrator, S/H capacitor bank (C_1, C_2, C_3, and C_4), offset-compensated preamplifier stages and latch are all designed for 0.5 V operation and work together to perform signal demodulation. The integrator, shown in Figure 4-12, is an inverter that is DC biased at the switching threshold for large simulated DC gain of 38 dB (Figure 4-13). DC gain must be maximized so that the integrator is able to hold the integrated voltage for the targeted time. Because a voltage shift is necessary from the mixer to the integrator, an AC coupling capacitor is used to interface the mixer to the integrator. However, because the integrator must also be duty-cycled along with the rest of the system, it is biased in two ways: resistively at the gate (because the gate voltage and output of mixer do not change when switching the system on/off), and dynamically at the output (the S/H capacitors are also pre-charged to V_{reset} before they are presented to the integrator to capture an integration). Thus, the integrator is always set to the switching threshold at the beginning of each integration and integrates in the same direction from the self-mixer rectified output. Figure 4-14 shows the integrator performing a new integration every 30 ns when a stream of pulses is present at the input. Figure 4-15 shows that these integrations are stored onto one of four capacitors that are rotated through at each integration time according to the operation schedule in Figure 4-3. It is seen that though the integrator integrates in increments of 30 ns, the capacitors hold this value for 60 ns so that adjacent bit decisions can be made. You can also see that for each capacitor, the 30 ns integration, two consecutive 30 ns hold times, and 30 ns reset time are staggered relative to each other. M_0 and M_1 are non-minimum length transistors to achieve the maximum DC gain, and their widths are sized such that a pole at 250 MHz is formed at the output of the mixer. The S/H capacitors are integrated using MIM capacitors for low loss to improve hold times and are sized such the inverter and capacitor combination approximates an integrator over the 250 MHz bandwidth (Figure 4-13). Two minimum length complimentary switches are used at the drain nodes for fast switching of the integrator, and allow for symmetric convergence (from the power supply and ground) to the operating point voltage. The length of the switching transistors are set such that R_{off}/R_{on} is sufficiently large for better isolation between input/outputs of the switches. V_{eval} and

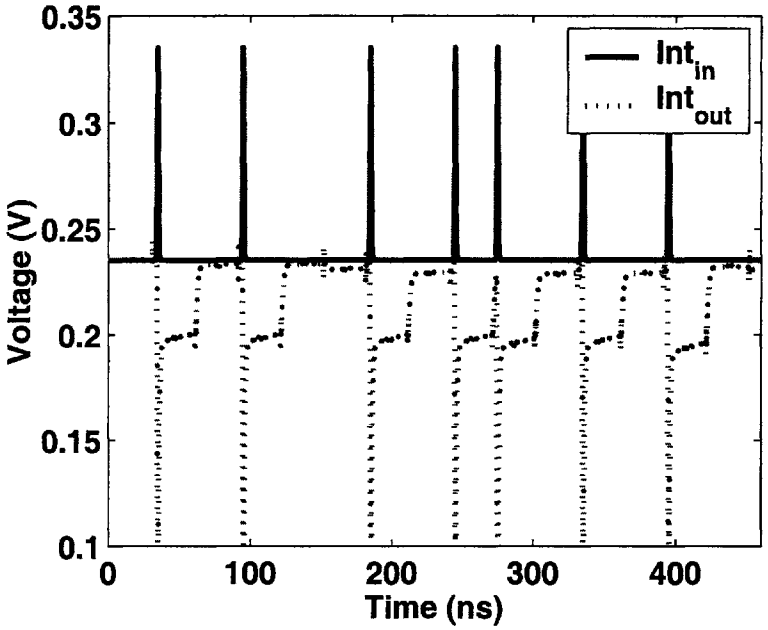


Figure 4-14: Simulated integrator transient response.

V_{eval2} connect the S/H capacitors to the appropriate offset-compensated preamplifiers for downstream bit evaluation.

4.2.4 Baseband Offset-compensated Preamplifiers and Latch

Offset compensated preamplifiers are necessary to reduce voltage offset in the latch. The offset voltage contributes significantly to bottom-line receiver sensitivity. If there is ideally zero offset, the latch will declare ones and zeros with equal probability in the presence of two noise integrations. However, for any non-zero offset, it is easy to see how the offset voltage will skew the declaration undesirably. One of the offset-compensated preamplifiers and its associated timing diagram is shown in Figure 4-16(a). In reset, all of the switches are closed to allow for fast turn-on time and S_4 presents a 0 V input to the amplifier. The switches are sequentially opened in a self-timed fashion to compensate for output offset. This occurs as follows. When S_1 is opened, the output offset of the amplifier is presented to C_C (Figure 4-16(b)). S_2 and S_3 successively open thereafter, and store the offset on to C_C (Figure 4-16(c)). Finally, S_4 releases the input from the 0 V input state, and another signal that is

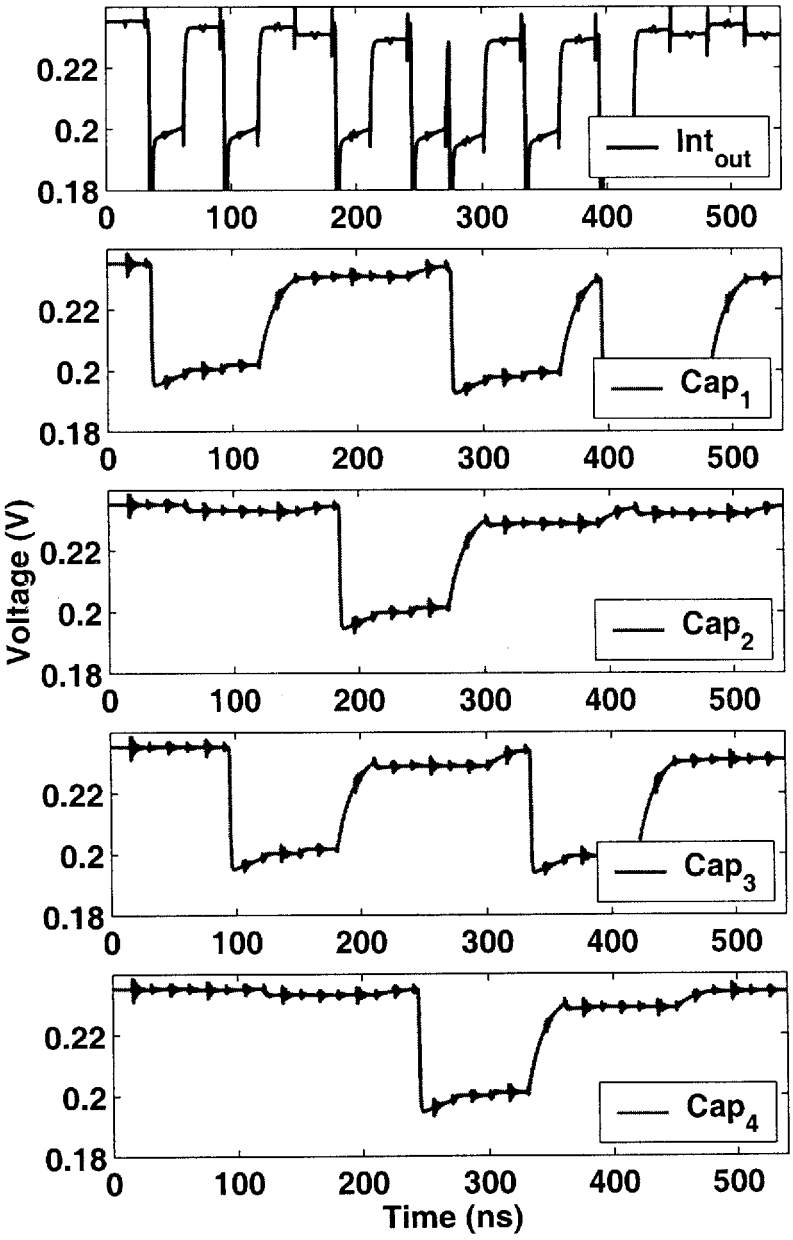


Figure 4-15: Simulated baseband capacitor bank transient response.

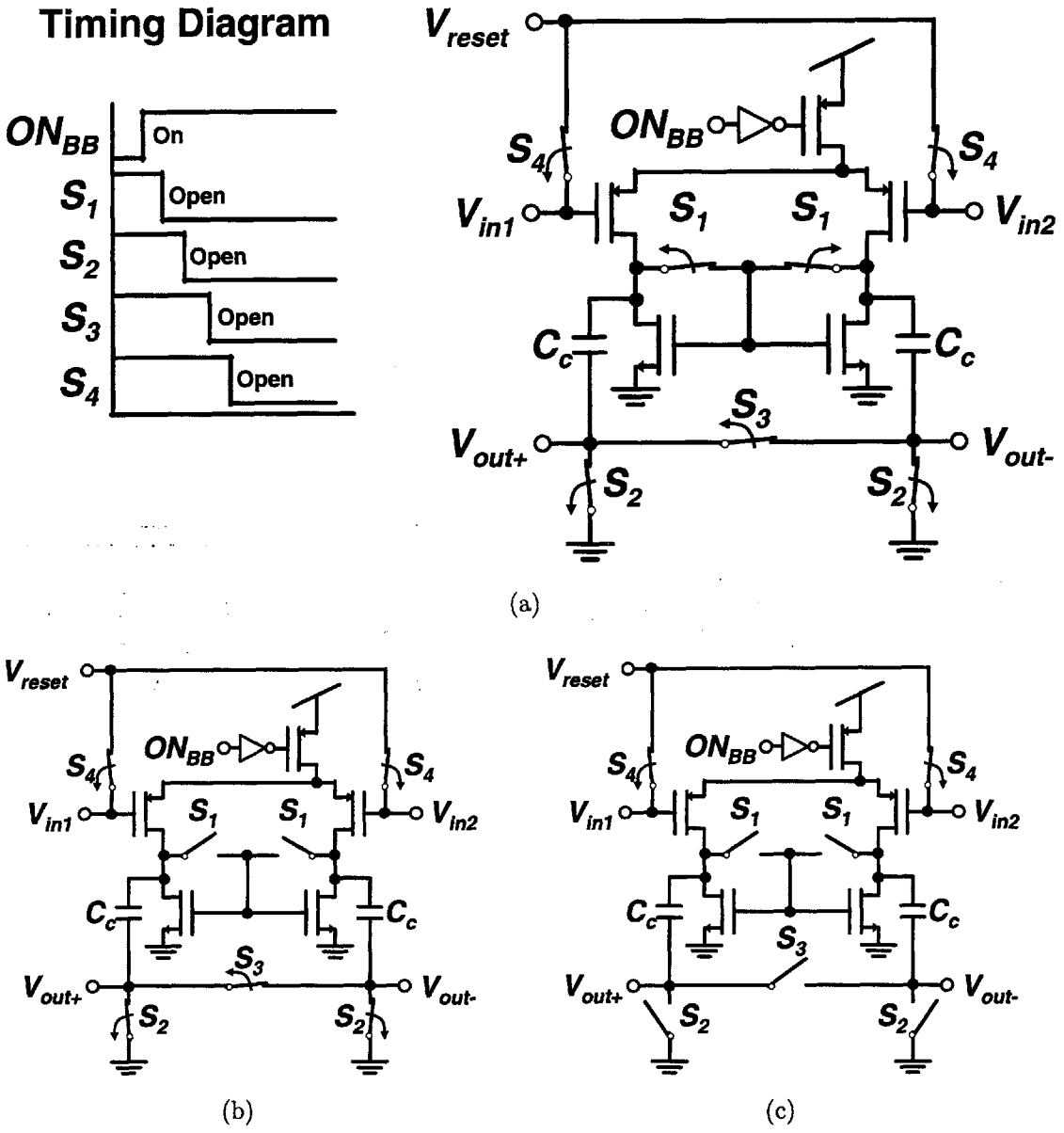


Figure 4-16: (a) Timing diagram and offset-compensated preamplifier in initial state. (b) Output offset presented onto C_C with zero input. (c) Output offset stored onto C_C, before switching from zero input to the desired input.

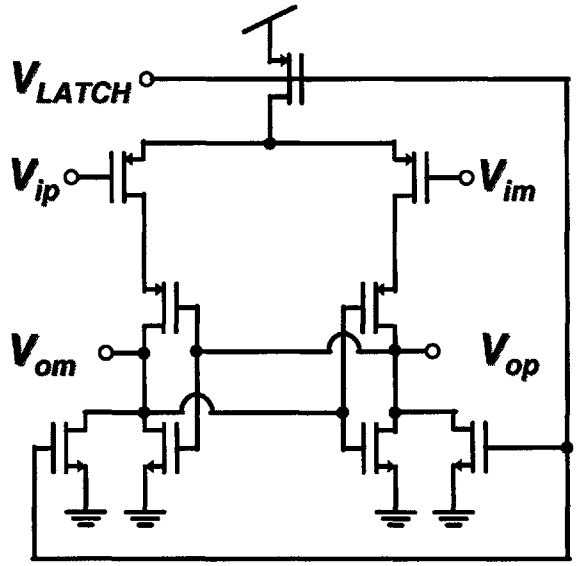


Figure 4-17: Latch.

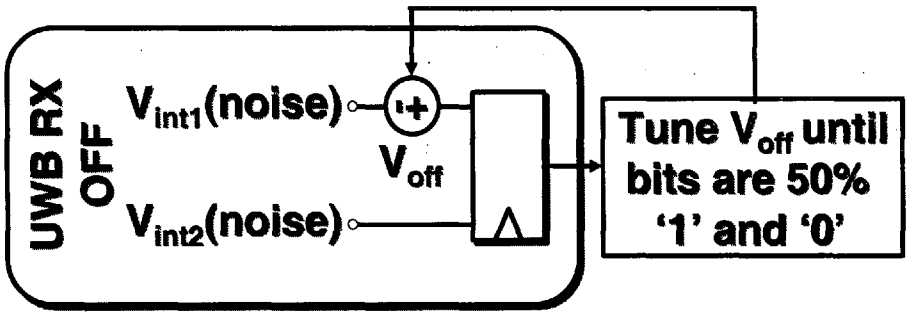


Figure 4-18: Simple, low power method for receiver sensitivity enhancement.

triggered from the falling edge of S_4 latches the appropriate V_{eval} voltages to the preamplifier for amplification. The total gain for the cascaded stages is 20 dB, which reduces the latch offset voltage by an order of magnitude.

The latch is based on the meta-stable StrongARM latch shown in Figure 4-17. When V_{LATCH} is high, the latch is in reset, and the outputs are zeroed. When V_{LATCH} is low, the latch is released into a meta-stable operating point that is disturbed by unequal inputs presented to it through V_{ip} and V_{im} through positive feedback, reaches one of two singular states for V_{op} and V_{om}. Monte Carlo simulations of the offset voltage shows that the maximum latch offset can be as much as ± 100 mV.

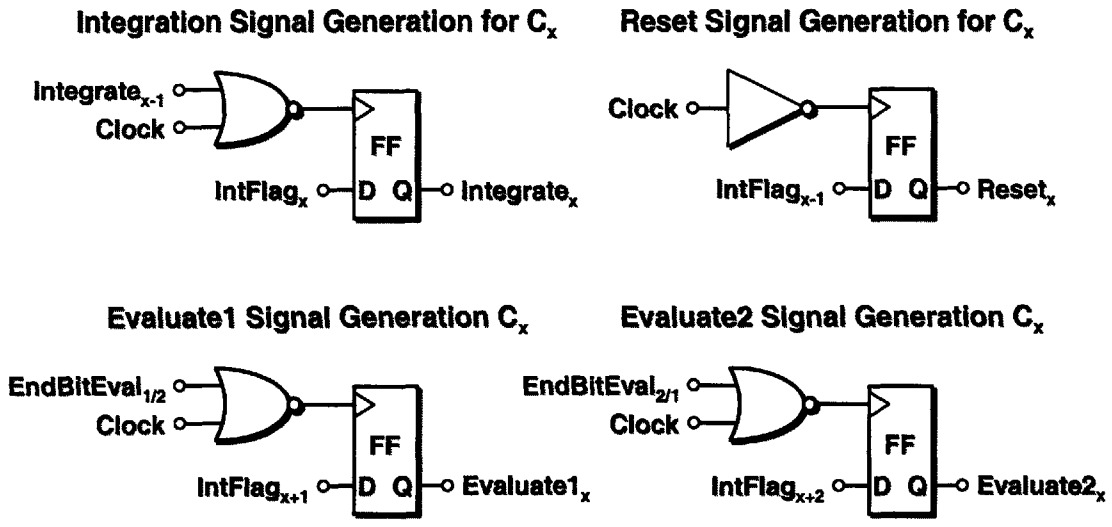


Figure 4-19: Digital edge-triggered combinational blocks for baseband control.

Another method to improve receiver sensitivity without using offset-compensated preamplifiers could be performed by adding an offset-voltage control to the latch, and wrapping the backend in a feedback loop. Figure 4-18 shows the conceptual block diagram of this method. A simple, low power calibration is done by disabling the front-end and running the baseband. The offset knob can be tuned until equal percentages of ones and zeros are observed at the bit decision output. Because the RF front-end – which consumes 99% of the total receiver power – is turned off, this method requires very little power overhead, while affording extreme improvements in receiver sensitivity and architectural simplicity.

4.2.5 Digital Timing Blocks

Because there is no RF oscillator required for this architecture, the fastest clock that is required to run the system is 33 MHz in the baseband circuitry to control the baseband. Four clocks are fed into the chip, and on-chip edge-triggered/combinational logic blocks scattered throughout the baseband help "shift-and-spread" the incoming clock signals such that no critical phases are overlapping. Figure 4-19 shows the circuits that perform this task, and Figure 4-20 shows the result upon the control

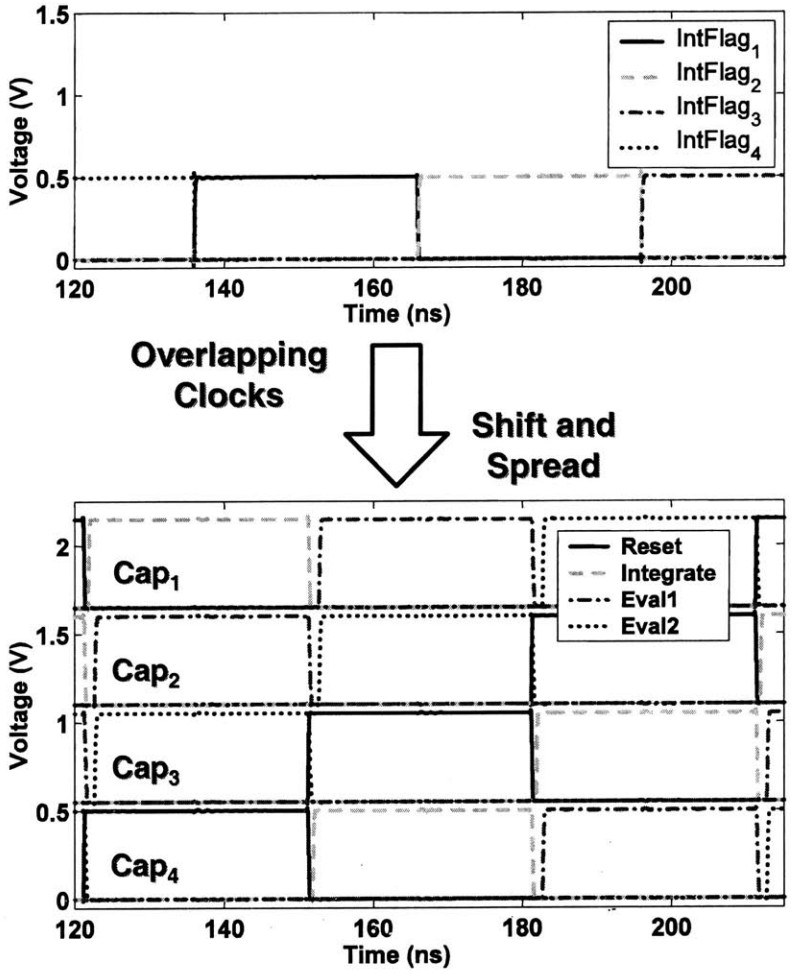


Figure 4-20: Shift-and-spread.

signals to the S/H capacitors. For proper synchronization, all of these blocks are referenced back to a monolithic 33 MHz master clock.

4.3 Measurements

Figure 4-21 shows the RFIC mounted on an FR4 PCB. The RFIC is packaged in a QFN 28 lead package with paddle. There is one RF input and two differential RF outputs. The two layer PCB has a continuous ground plane on the back, and the RF traces are built using 50 Ω coplanar microstrip lines that have ground vias for more reliable coplanar grounds. The analog tuning potentiometers are on the left edge of

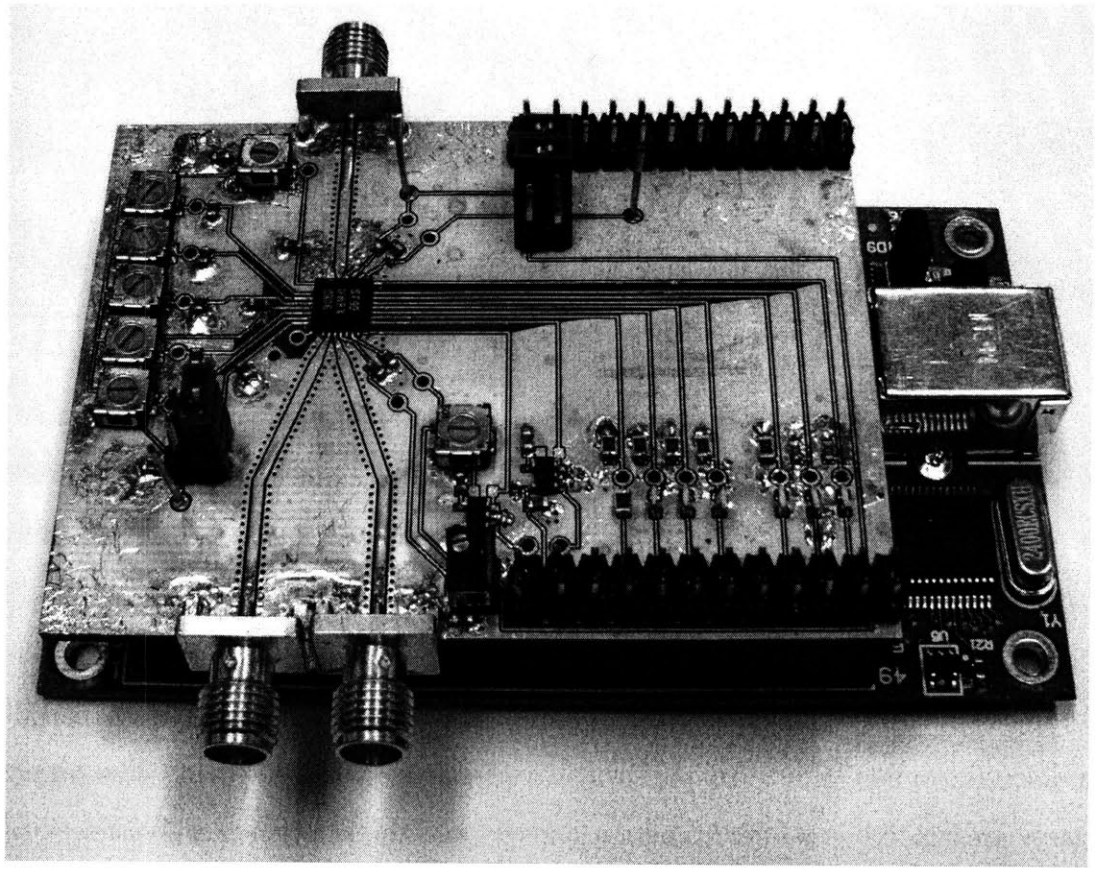


Figure 4-21: Test PCB.

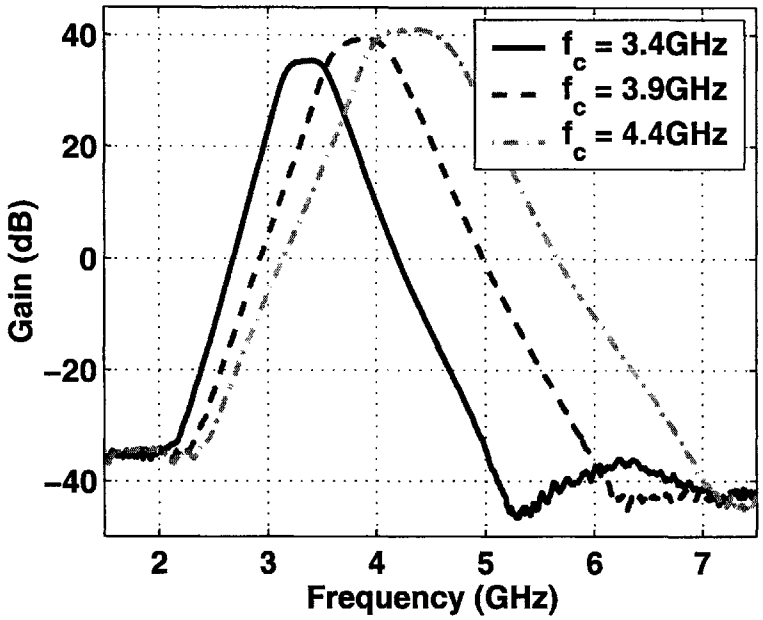


Figure 4-22: Gain in RF front-end.

the PCB, and the digital I/O with level shifting resistors and comparators are on the bottom right. The green board underneath is a commercial FPGA to USB2.0 board that provides the digital control to the chip, and is where the backend timing acquisition algorithm is implemented.

Figure 4-22 shows the measured RF gain response of the RF front-end in each of the three bands. The RF front-end provides up to 40 dB of gain. In the 3.4, 3.9, and 4.4 GHz bands, the 3 dB bandwidth varies from 430–715 MHz. The varactor voltages are tuned by an off-chip potentiometer, and the front-end can be successfully configured to be in one of the three bands. It is also seen that the filters roll-off rapidly, and offer channel selection and out-of-band suppression of noise and interference. Figure 4-23 shows the measured NF of the front-end. In the 4.4 GHz band, 8.6 dB of NF is achievable. Without external matching networks, the packaged chip exhibits -10 dB of matching across the entire 3-5 GHz channel, regardless of which subbanded channel the cascaded gain stages are configured (Figure 4-24). When the receiver is set in the highest gain state, the input P_{1dB} compression point is measured to be -39.2 dBm, -42.2 dBm, and -44.2 dBm in the 3.4 GHz, 3.9 GHz, and 4.4 GHz channels, respectively. The 40 dB of built-in gain control allows these to be scaled.

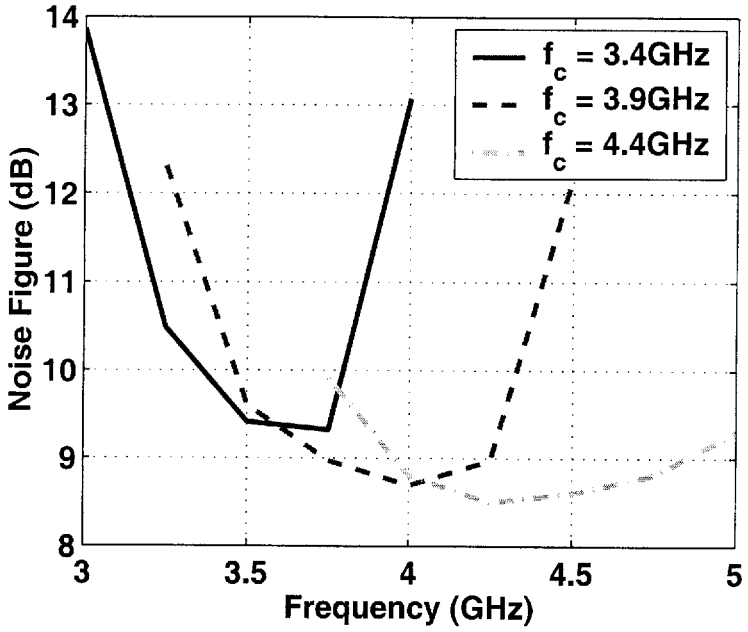


Figure 4-23: NF in RF front-end.

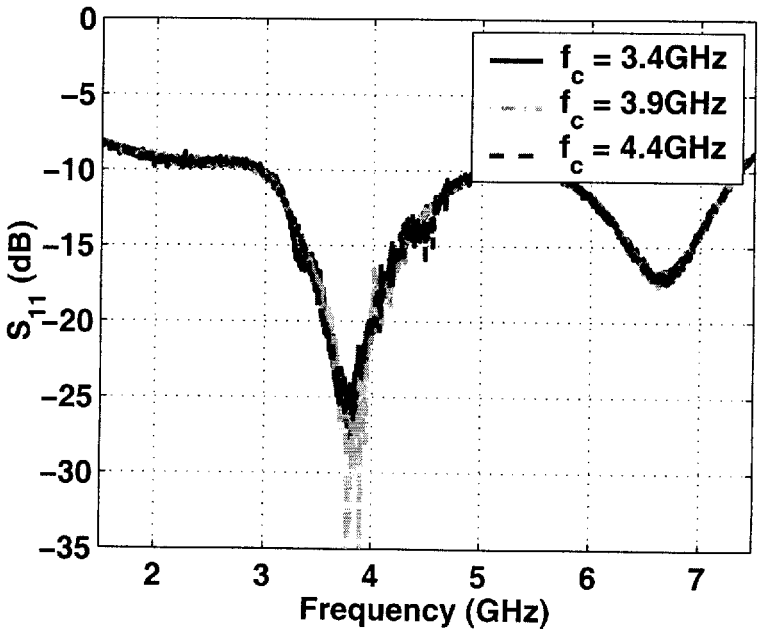


Figure 4-24: S_{11} of RF front-end.

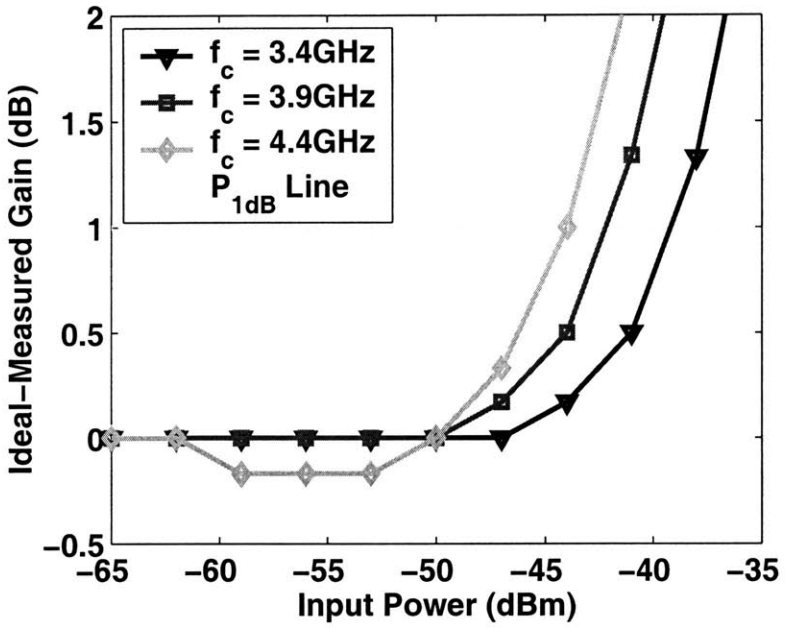


Figure 4-25: P_{1dB} of RF front-end.

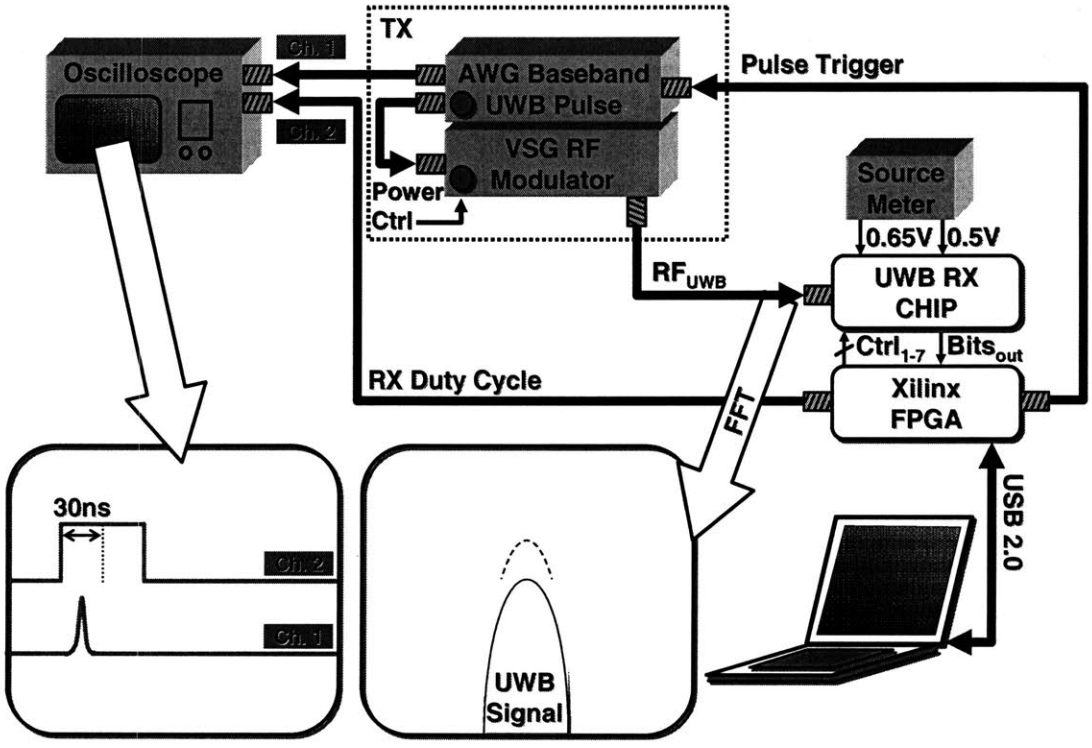


Figure 4-26: BER test setup.

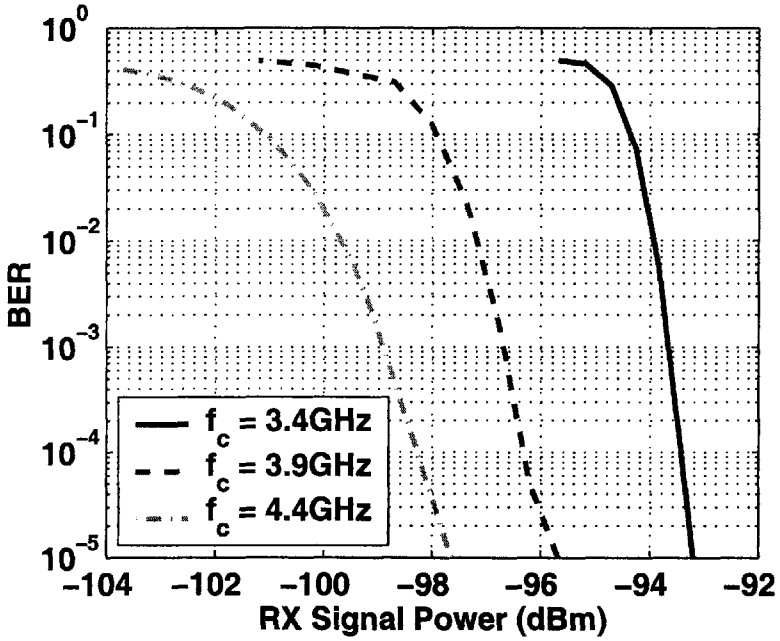


Figure 4-27: Sensitivity vs. BER at 100 kbps.

To measure BER, the test setup shown in Figure 4-26 is constructed. It is composed of an arbitrary waveform generator (AWG) that supplies the pulse waveform template constructed by Matlab to the vector signal generator (VSG). The VSG upconverts the baseband signal to RF, where the center frequency and power level can easily be adjusted by two knobs on the VSG. The FPGA board manually synchronizes the received pulse to the digital backend by sending a trigger signal to the AWG to command a pulse. Figure 4-27 shows -99 dBm of sensitivity is achievable for a BER of 10^{-3} at 100 kbps in the 4.4 GHz band. The sensitivity shifts to first order with respect to the gain differences achievable in each band. The BER waterfall curves are sharper for this PPM signal than for a raw BPSK signal, because the gain path contains a squared term, which links signal amplitude to achievable gain.

To measure the impact of interferers on BER, the test setup shown in Figure 4-28 is constructed. In addition to Figure 4-26, this setup contains an additional RF interference generator and power combiner. The impact of interference upon BER is tested as follows. The receiver is first configured such that the BER is at 10^{-5}. Then, the interference tone is activated and increases in amplitude while the BER

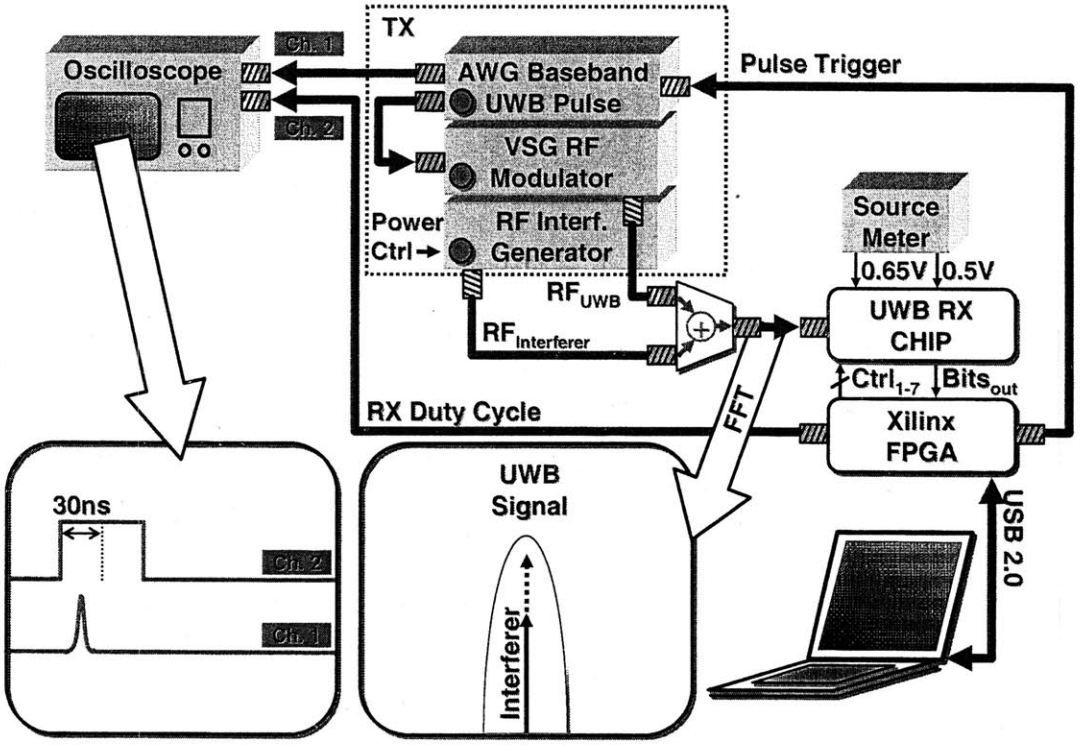


Figure 4-28: Interferer test setup.

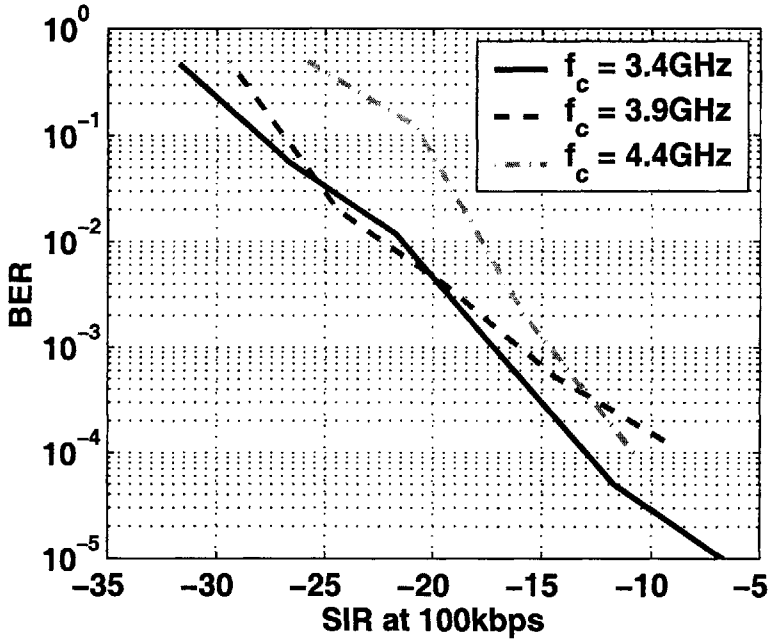
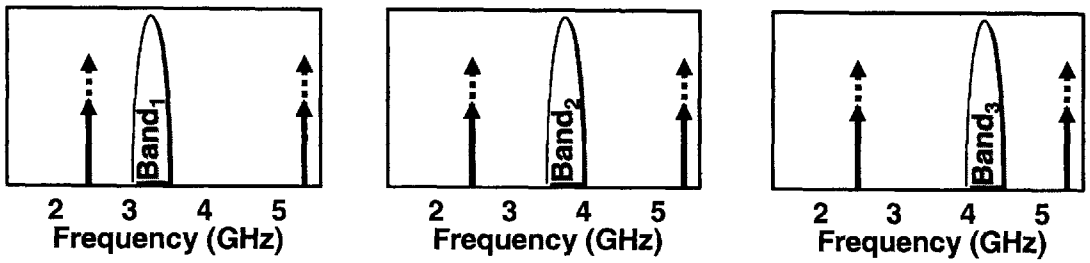


Figure 4-29: In-band interferer vs. BER at 100 kbps.

is recorded. Two types of interferers are tested here: in-band and out-of-band. The in-band test reveals how robust the demodulator is towards interference, and the out-of-band interference test reveals how effective the channel select filters are towards known out-of-band interferers.

Figure 4-29 shows how the UWB signal performs with an in-band interferer. To achieve a 10^{-5} BER, the sensitivity is set to -98 dBm in the 4.4 GHz band, which translates to a UWB pulse amplitude of 282 μV. for an SIR of -15dB, the -83 dBm interference power translates to a sinusoidal amplitude of 22.3 μV. An explanation for this low tolerance could be attributed to the integration window time. Since the integration window is 15 times larger than the pulse width, any noise/interference terms that are sustained through the window period are integrated as undesired energy.

Figure 4-30 graphically shows the tests performed for out-of-band interferers at the known 802.11 frequencies and the corresponding results. Again, the receiver is receiving -98 dBm UWB pulses at 100 kbps, which corresponds to a UWB pulse amplitude of 282 μV. -15 and -20 dBm of power correspond to 56 mV and 32 mV,



f_{interf}	P_{interf} for 10^{-3} BER
2.45 GHz	-20dBm
5.25 GHz	-15dBm

f_{interf}	P_{interf} for 10^{-3} BER
2.45 GHz	-20dBm
5.25 GHz	-15dBm

f_{interf}	P_{interf} for 10^{-3} BER
2.45 GHz	-20dBm
5.25 GHz	-47dBm

Figure 4-30: Out of band interference test.

respectively. In the 4.4 GHz band, when the interference is set at 5.25 GHz, the tolerable interference power is at -47 dBm, which corresponds to 1.4 mV amplitude. This is due to the slower bandpass filter roll-off in the 4.4 GHz band.

A summary of measurements are shown in Table 4.1. 2.5 nJ/bit is achieved for data rates greater than 10 kbps. Though the instantaneous power of this receiver is similar to that of an optimized 802.11 radio, it is important to note that the 802.11 radios cannot be duty cycled to achieve the same energy efficiency at the lower data rates. Further analysis of energy/bit performance on this receiver follows.

Figure 4-31 reveals the energy/bit performance of the entire receiver. For a 0.65 V supply, 2.5 nJ/bit is achieved for data rates above 10 kbps. For rates below 10 kbps, energy/bit increases as data rate decreases. This is due to leakage currents becoming more significant. Data is also taken at 0.5 V, which is what the circuits were originally designed for. The energy/bit becomes sub-nJ/bit; the tradeoff is that sensitivity degrades by 10 dB. The sensitivity degradation is also correlated to a gain reduction of 10 dB when the supply is reduced.

The chip area (Figure 4-32) is 1 mm x 2.2 mm. Three separate power/ground supply pairs are on the chip: one for the power-gating buffers for duty-cycling the front-end, another for the RF front-end, and another for the digital baseband. Isola-

UWBRX Chip Info	
Technology	90nm CMOS
Supply	0.65V
Die size	1mm x 2.2mm
Modulation	PPM
Data rate	0-16.7Mbps
Pulse BW	500MHz
f_c subbands	3.4GHz, 3.9GHz, and 4.4GHz
Measured Results	**f_c=4.4GHz, T_{int}=30ns, 100kbps**
Front-end gain	40dB
Front-end NF	8.6dB
Sensitivity (10^{-3} BER)	-99dBm
In-band SIR for 10^{-3} BER	-15dB
Instantaneous power	35.8mW
Leakage power	3.5μW
Turn-on time	2ns
Energy/bit	2.5nJ/bit
P_{interf} at 2.4GHz for 10^{-3} BER	-20dBm

Table 4.1: Summary of measured results for 90nm CMOS chip.

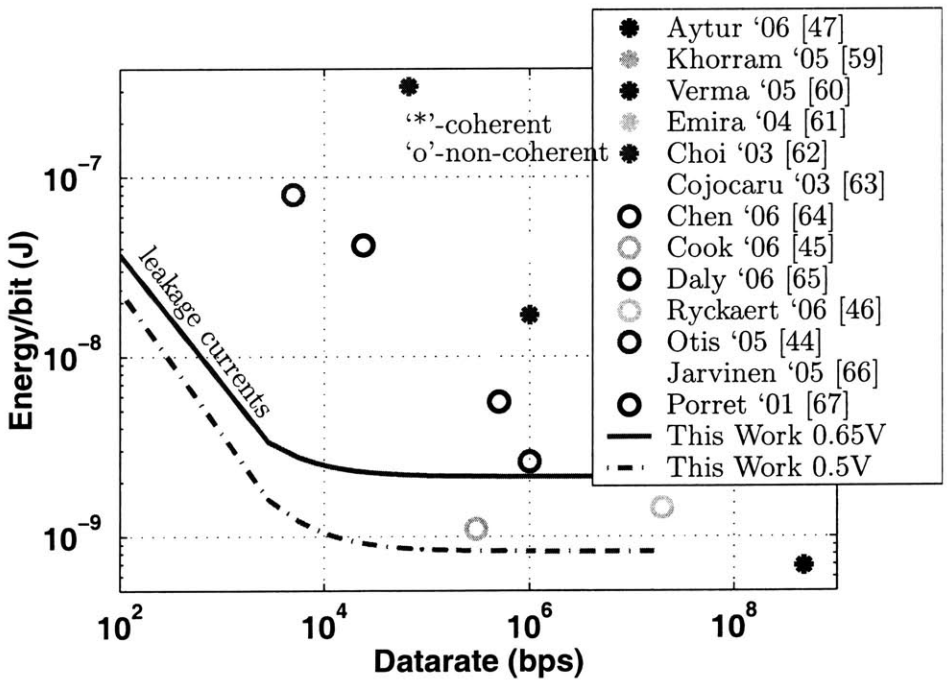


Figure 4-31: Energy/bit.

tion is accomplished through careful layout, usage of 40 μm thick p+ substrate guard rings, and separate downbonds for the substrate isolation.

4.4 Timing Acquisition and Energy Analysis

Figure 4-33 shows the effects of timing differences between the transmitter and receiver reference crystals. Assuming that the receiver clock is the frame of reference, all of the timing offsets can be lumped into the transmitter. When there is a small offset in clock center frequency, the data eventually shifts out of the desired integration window, and thereby causes incorrect bit-decisions to be made. For this architecture to be viable, a low power and efficient methodology for synchronizing and adjusting for a known and tolerable range of clock offsets must be considered at the packet level.

The chosen packet structure is shown in Figure 4-34. It consists of a 15-bit preamble code that is repeated twice, a 0.24 μS sequence for fine tracking, and a 60 μS payload. The code is found by using Matlab, and finding the code that has the largest auto-correlation singularity peak in the presence of noise. Once coarse acquisition is achieved, It is necessary to perform fine-track such that the pulse can be centered within the integration time window. Figure 4-35 shows this graphically. In $Frame_1$, the receiver has finished coarse acquisition and will advance state into the fine track mode. $Frame_2$ and $Frame_3$ are part of the receiver's fine track configuration. In coarse acquisition, it is known that the pulse frame begins somewhere in the 30 ns integration time, but the exact position is unknown. During fine track, the receiver is shifted by 10 ns steps, and through this, it is possible to deduce where the pulse is located, with a 10 ns resolution. If $Frame_2$ and $Frame_3$ yield zeros, then it is known that the pulse is in the first 10 ns of $Frame_1$. Thus, for the payload, the receiver is placed into a properly-delayed $Frame_3$ configuration.

For two clocks that have a relative $\pm$100 ppm frequency offset, it would take 100 μS to shift the edge by 10 ns. Thus, if a 100 ppm clock is assumed, the payload can demodulate data for at least 100 μS before another fine track sequence must be

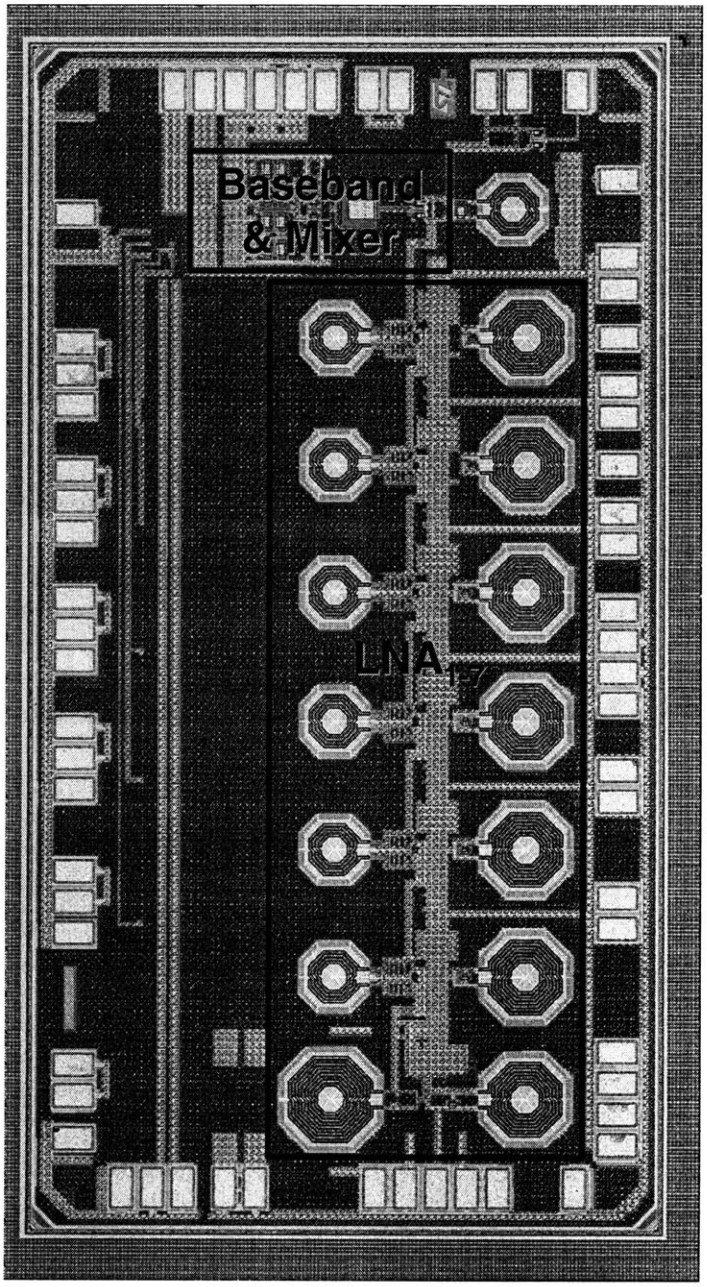


Figure 4-32: Die photo.

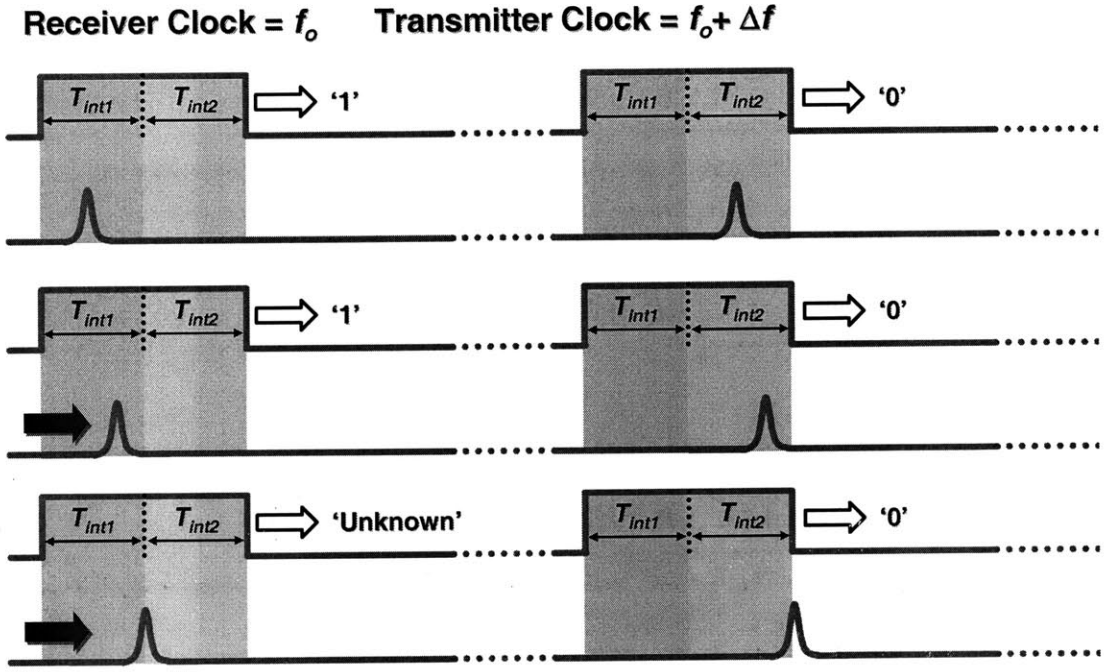


Figure 4-33: Illustration of clock offset effects.

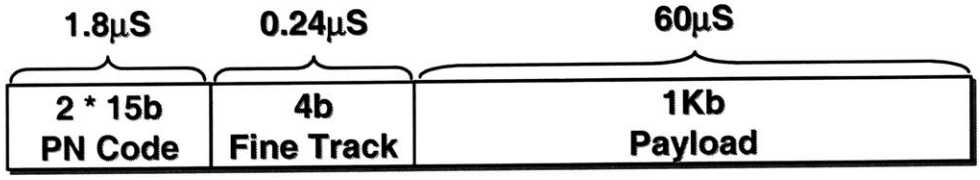


Figure 4-34: Packet structure.

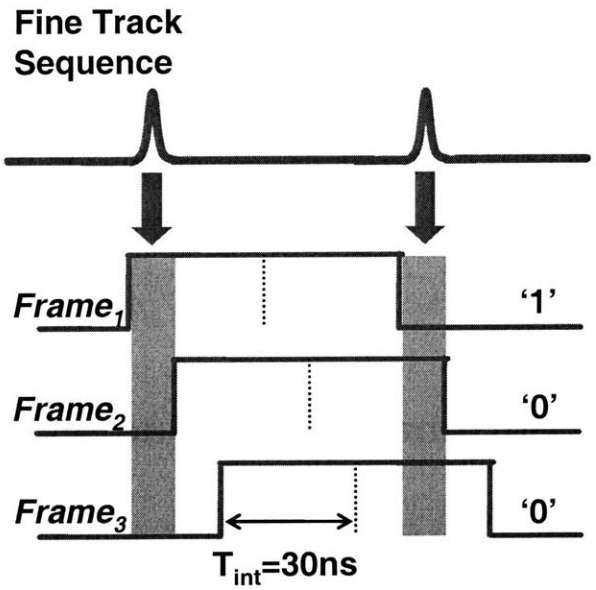


Figure 4-35: Unit fine track sequence.

initiated to recalibrate the receiver. In all, the overhead for coarse acquisition is very small compared to the payload.

Although the energy/bit plots in the Section 4.3 only include energy consumed during the payload, a more complete energy analysis is done with (4.1) and includes acquisition time into the calculation as well:

$$Energy/bit = \frac{T_{acq} \cdot P_{rx} + 2 \cdot T_{int} \cdot P_{rx} \cdot N_{bits}}{N_{bits}} + \frac{P_{leakage}}{\text{Data rate}}. \tag{4.1}$$

Without using the advanced energy saving techniques (preamble configuration and reducing T_{int} for less reflective environments), theoretical energy/bit calculations are performed for a receiver requiring 20 mW of instantaneous power. If a 1000 bit payload is assumed, a 30 ns integration time is allocated for T_{int}, and a 2.2 μS acquisition time is required, then the system is able to operate at 1.85 nJ/bit.

If the payload is reduced by two orders of magnitude to just 10 bits, then the energy/bit is dominated by the energy required for coarse acquisition and increases to 8.4 nJ/bit.

As stated before, energy can also be further reduced and performance increased in

channels with few reflections. This is done by reducing T_{int}, which allows the receiver to be powered on for less time, and for the integrator to reduce the amount of noise that is integrated, thereby improving SNR. To reduce the sensitivity of the receiver to crystal offsets, it is possible to add tuning capacitors in series with the crystal reference, and thereby reduce the ppm offset by more than an order of magnitude [80].

4.5 Post-measurement Link Budget Analysis

A post-measurement link budget calculation reliably quantifies how the receiver sensitivity compares to other systems. A key metric in comparing this is finding the required ratio of energy-stored-per-bit to the noise bandwidth (E_b/N_o) needed at the demodulator for a desired BER target. For 10^{-3} BER in a coherent BPSK system, E_b/N_o must be 7 dB. For the same BER in a non-coherent PPM system, E_b/N_o must be 17 dB [81]. Using (4.2) and (4.3), where R is data rate and BW is signal/noise bandwidth, the achieved E_b/N_o can be calculated and compared with the theoretical value. Through this, system inefficiencies can be revealed and quantified.

$$SNR(dB) = sensitivity - (10 \cdot log_{10}BW + NF - 174) \tag{4.2}$$

$$\frac{E_b}{N_o}(dB) = SNR + 10 \cdot log_{10}BW - 10 \cdot log_{10}R \tag{4.3}$$

With a measured NF of 9 dB, a measured sensitivity of -99 dBm at 10^{-3} BER, and a signal/noise bandwidth of 500 MHz, the SNR at the demodulator is calculated with (4.2), which is -21 dB. With a data rate of 100 kbps, the E_b/N_o of this measured system is 16 dB, which is very close to the theoretical value.

For a given sensitivity, channel model [20], and signal bandwidth, it is possible to find the theoretically achievable transmission distance using (4.4), where m is distance in meters, P_{tx} is power at the transmitter, PL_0 is the 1 m path loss (1.2), and P_{sens} is the desired sensitivity. For a line of sight (LOS) situation, γ for a 1 m path loss is

2. For non-line of sight environments (NLOS), γ can be as high as 3.44.

$$\gamma \cdot 10 \cdot log_{10}m = P_{tx} - PL_0 - P_{sens} \tag{4.4}$$

Assuming a LOS environment ($\gamma = 2$), a P_{tx} of $-41.3\ dBm/MHz + 10 \cdot log_{10}500 - 3\ dB = -17.3$, desired sensitivity of -99 dBm, and $PL_0 = 44\ dB$, the theoretical transmission distance is calculated to be 76.7 m. In a NLOS environment ($\gamma = 2.5$), $PL_0 = 55\ dB$, and the new distance is calculated to be 11.6 m. Thus, depending on channel environment, the achievable distances for un-coded signals vary widely. In the lab, 7 m of transmission distance was measured with omni-directional antennas in the transmitter [82] (whose maximum output power is 8 dB below the FCC limit) and receiver [79] at 16.7 Mbps.

4.6 Summary

A self-mixing, duty-cycled UWB receiver using UWB signaling enables data rate independent, energy efficient operation at 2.5 nJ/bit. This metric is an order of magnitude lower than the energy/bit metrics afforded by current state-of-the-art receivers in the lowest data rates. It is seen that as data rate reduces, leakage energy begins to dominate the receiver and degrades achievable energy/bit. A new, low power, relative compare demodulator is introduced and achieves -99 dBm of sensitivity for 10^{-3} BER at 100 kbps. The entire receiver operates from a 0.5 V or 0.65 V supply, and is implemented in a 90 nm CMOS process.

Chapter 5

Conclusions

5.1 Summary of Contributions

As wireless technology becomes more pervasive, un-tethered portability – and thereby low energy operation – becomes the paramount figure of merit to optimize in portable electronics, while still affording good performance. In this work, UWB signaling technology was explored for possibilities of achieving energy efficient radios at high and low data rates. At high data rates, which can be used for video and data communications, it is shown that systems with faster throughput benefit from the weakly-proportional relationship between increased power consumption vs. increased data rate, and thereby achieve lower energy/bit operation. However, because wireless systems also have linearity and interference concerns, extending bandwidth to afford higher data rates complicates receiver design. Currently, there is no reliable method to predict the existence of interference; there is only measured data on sampled wireless environments [83]. To enable truly wideband radios that can function in interference-rich environments, interference mitigation and frequency agility techniques (i.e.– cognitive radio, detect-and-avoid) must be created and employed in future, high speed radio links.

At low data rates where voice, sensing, and wireless sensor network applications dominate, the fixed costs of providing basic receiver functionality for a narrowband signal-based radio are not as easily amortized over fewer bits/sec as the data rate

decreases. This causes a direct increase in energy/bit as data rate is decreased. However, by making a fundamental shift from sensing data in frequency/phase (requiring "steady state," narrowband operation) to sensing data in time using pulsed UWB PPM signaling, energy/bit becomes uncorrelated to data rate. In this work, a data rate independent, low energy 2.5 nJ/bit radio receiver is realized in a 90 nm CMOS process. Future iterations of this benchmark work can be optimized for power savings to yield at least a 3x reduction in energy/bit. Because 99% of the receiver power is consumed in the front-end gain stages, the area that benefits the most from further optimization lies in finding ways to increase the gain/mW ratio. This can be done by using cascode amplifier structures, active down-conversion methods, and using supply voltages that are optimized for these RF analog blocks. For short-range, low data rate communications, it is without a question that ultra-wideband signaling is the best fit for such applications.

5.2 Future Work

For high data rate radio systems, concurrent full-band UWB solutions could bring about multi-GHz data communications for a limited range. Research in MIMO (added diversity for increased capacity) [84][85] and cognitive radio (detect and avoid, intelligent band re-use, as well as active cancellation of interferences in RF) [86] will aid in creating the technology necessary to realize such a system. For true multi-GHz data transfer at more generous distances, 60 GHz radio is the only legal frequency band that affords the bandwidth and higher FCC power limits (40 dBm EIRP) to realize those speeds. Many innovations across all domains – architecture, filtering, amplification, propagation, frequency control and demodulation – are necessary to process those signals elegantly and efficiently [87].

For low data rate systems, this work has used pulsed UWB PPM signaling to decouple energy efficiency from data rate. However, to achieve global energy efficiency, managing clock offset is costly. Techniques for either controlling or improving a receiver's immunity to clock offset to simplify the baseband is critical for achieving

lower power and deeper energy savings.

At the circuit level, managing the tradeoff between supply voltage, clock speed, and power consumption has been widely explored for digital circuits. However, analog designers are faced with a few challenges without answers as transistors continue to scale: creating new architectures to support low voltage operation and/or operating at the optimal supply voltage. Instead of blindly following voltage scaling for digital circuits, it is important to revisit and analyze tradeoffs made when important techniques and architectures such as cascoding and op-amps cannot be used [88]. Ultimately, to survive with voltage scaling, analog designers must think in "sub-systems" of simple circuits that functionally provide the same (or better!) performance as compared to well-known, monolithic analog circuits.

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