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A 8.45 GHz GaAs FET Amplifier

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A 8.45 GHZ GAAS FET AMPLIFIER

by

Alain Charles Louis Briancon

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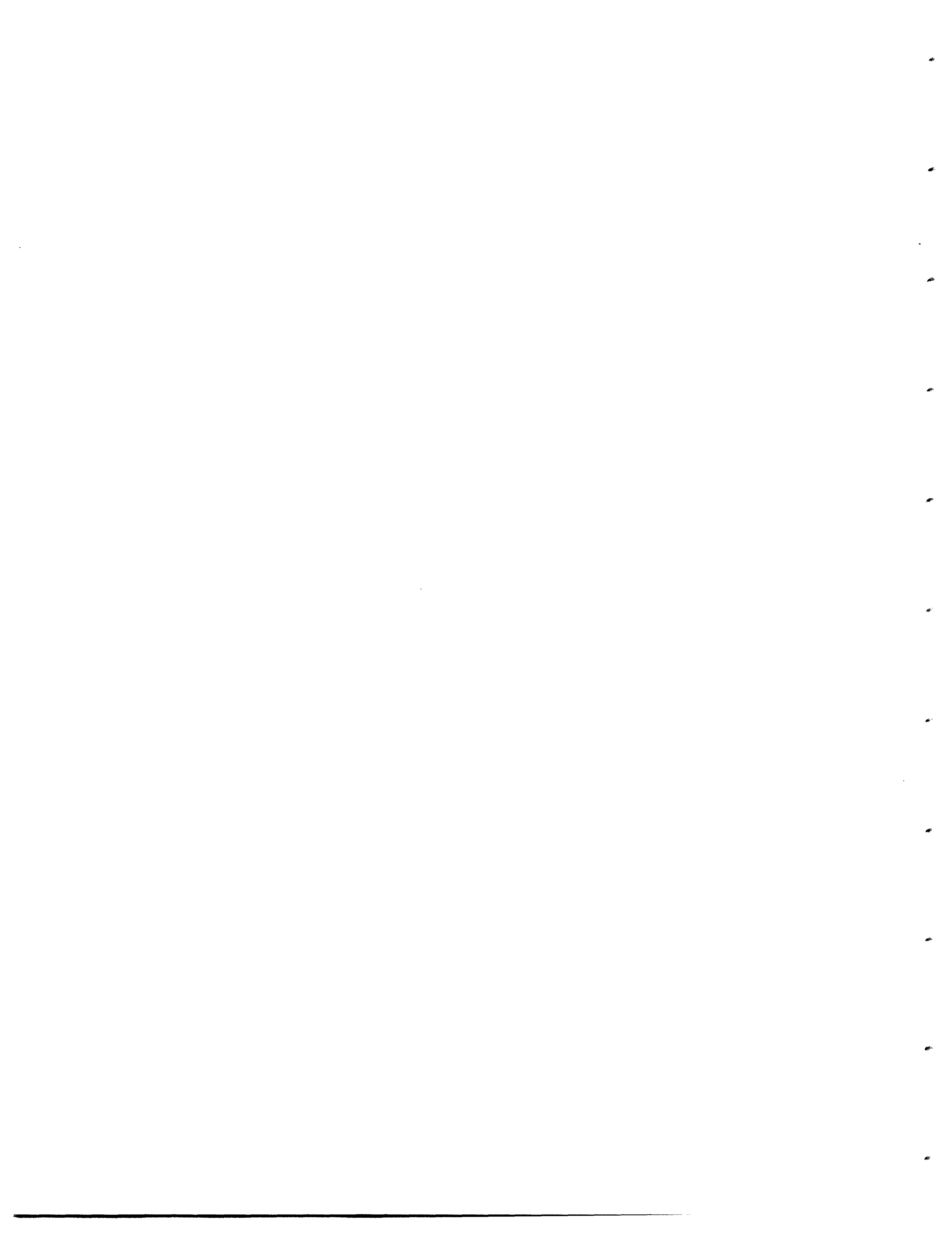
ABSTRACT

Procedures for measuring power scattering and noise parameters of Gallium-Arsenide field-effect transistors in the X-band are presented. The variations of the noise parameters and of various gains of a particular FET with frequency, the device's physical temperature and DC bias are reported. The physical parameters of the FET's channel are determined.

Details of the design, construction and evaluation of two single stage amplifiers operating at 8.45 *GHz* are presented. Both are tuned using microstrip boards. At 8.5 *GHz* and room temperature, the first prototype exhibits a 6.8 *dB* gain and a noise temperature of 160 *K* at 8.5 *GHz* and room temperature. Deformations of the microstrip boards, when cooled, prevent the operation of the amplifier at cryogenic temperatures. The second prototype, when cooled at 77 *K*, exhibits a 7.2 *dB* gain and a noisè temperature of 68 *K* (an improvement factor of 2.6 over the noise performance at 293 *K*). This study is part of the development of low noise, cryogenically cooled X-band FET amplifiers for VLBI observations in space.

Thesis Supervisor: Bernard F. Burke

Title: William A. M. Burden Professor of Astrophysics



A Eva et Maria

A quatre heures du matin, l'été,
Le sommeil d'amour dure encore.
Sous les bosquets l'aube évapore
L'odeur du soir fêté.

Mais là-bas dans l'immense chantier
Vers le soleil des Hespérides,
En bras de chemise, les charpentiers
Déjà s'agitent.

Dans leur désert de mousse, tranquilles,
Ils préparent les lambris précieux
Où la richesse de la ville
Rira sous de faux cieux.

Ah! pour ces Ouvriers charmants
Sujets d'un roi de Babylone,
Vénus! laisse un peu les amants,
Dont l'âme est en couronne.

O Reine des Bergers!
Porte aux travailleurs l'eau-de-vie,
Pour que leurs forces soient en paix
En attendant le bain dans la mer, à midi.

Arthur Rimbaud
Bonne pensée du matin.

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CHAPTER I: INTRODUCTION

1. Low noise receiver for Radio Astronomy

The purpose of a radio astronomy receiver is to detect and amplify signals received by the antenna from celestial radio sources. The power received is very low, varying from 10^{-20} Watt for a spectral line observation to 10^{-15} Watt [1] for a continuum observation. In most cases, the emissions consist of incoherent radiations as is the noise generated by the receiver itself. The requisites for a radio astronomy receiver are thus low noise and high stability. High stability is needed so that the input signal can be integrated and variations in the radiated power detected. Another requirement for an accurate reproduction of spectral observations is that the receiver be linear in output.

Most radio astronomy receivers operating under 15 GHz are superheterodyne. The input signal is amplified by a low noise amplifier, then converted to a lower frequency by mixing it with a local oscillator. The noise characteristics of this type of receiver are determined by the front end amplifier.

Although they are not as performant as cooled maser-upconverted systems, cooled Gallium-Arsenide Field Effect transistor amplifiers tend to be used with increasing frequency. These amplifiers present several advantages as compensation for their poorer performances. Input and output circuits are less critical to design than that for a negative resistance amplifier. The power is supplied through low DC voltages and not through power oscillators in the amplifier. Finally, tuning circuits are realized at the operating frequency.

2. Objectives

Projects of VLBI observations in space [2,3] require X band (8-12.4 *GHz*) low noise amplifiers. In this frequency range, the properties of low noise GaAs FET's have not been studied in detail, particularly at low temperatures. After several attempts, an FET (NEC 13783) was chosen for its performance at room temperature. The properties of the FET measured at both 77 *K* and 300 *K* and between 8 *GHz* and 10 *GHz* are reported. The power scattering and noise parameters of this transistor are calculated. A single stage amplifier is constructed. Using these data, attempts are made to answer the following questions:

Can the FET's performance at 77 *K* be inferred from its performance at 300 *K*?

How do the noise parameters of the FET vary with temperature and frequency?

How does the FET DC bias influence its noise and scattering parameters?

Is the circuit design for an amplifier operating at cryogenic temperature different from that of an amplifier operating at room temperature?

What problems and limitations are inherent to operation at cryogenic temperature?

3. The research

The work described herein was carried out at the MIT radio astronomy group laboratory.

Chapter II contains a brief summary of the properties of Gallium Arsenide and of GaAs Field Effect transistors. Microwave behavior of the FET and the currently admitted noise theory of the FET are presented. The classical noise representations of a twoport and how they relate to each other are also introduced.

Chapter III presents the measurement techniques and the measured scattering parameters. From the experimental data, stability and gain are computed. The noise parameters are determined and their variations with frequency, temperature and DC bias examined. The temperature dependence of the FET's DC characteristics and of several internal parameters is studied.

Chapter IV presents the design and performances of two single stage amplifiers at both room and cryogenic temperature. Conclusions are then drawn about microstrip tuning networks.

Chapter V summarizes the research and suggests further work in the field.

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3. R.A. Preston, B.F. Burke, R. Doxsey, J.F. Jordan, S.H. Morgan, D.H. Roberts, and I.I. Shapiro, "The Future of VLBI Observatories in Space," *MIT Radio Astronomy Contributions* 5 (1982).

CHAPTER II: THE FIELD-EFFECT TRANSISTOR

1. Field Effect Transistor Structure

Field-effect transistors offer many features for application in cryogenic microwave amplifiers. They have a higher input impedance than bipolar transistors that allows easier matching to microwave system. They are majority-carrier devices and consequently can be operated at higher frequencies and lower temperatures [1]. A typical structure of FET is shown in Figure II.1.

A thin epitaxial layer of thickness in the range $0.1-0.5\ \mu m$ is grown over a semi-insulating Gallium-Arsenide substrate. The substrate has a resistivity greater than $10^7\ \Omega cm$ and the layer of typically $10^{-2}\ \Omega cm$. Above the epitaxial layer are located three metal electrodes. This structure is approximately $300\ \mu m$ wide and is reasonably modeled as two dimensional.

Best noise results [2] of such FET's are achieved with a high doping level in the n layer, typically $10^{17}\ cm^{-3}$. This doping is usually realized with selenium impurities. One is also required to have the smallest possible gate and source metal resistances.

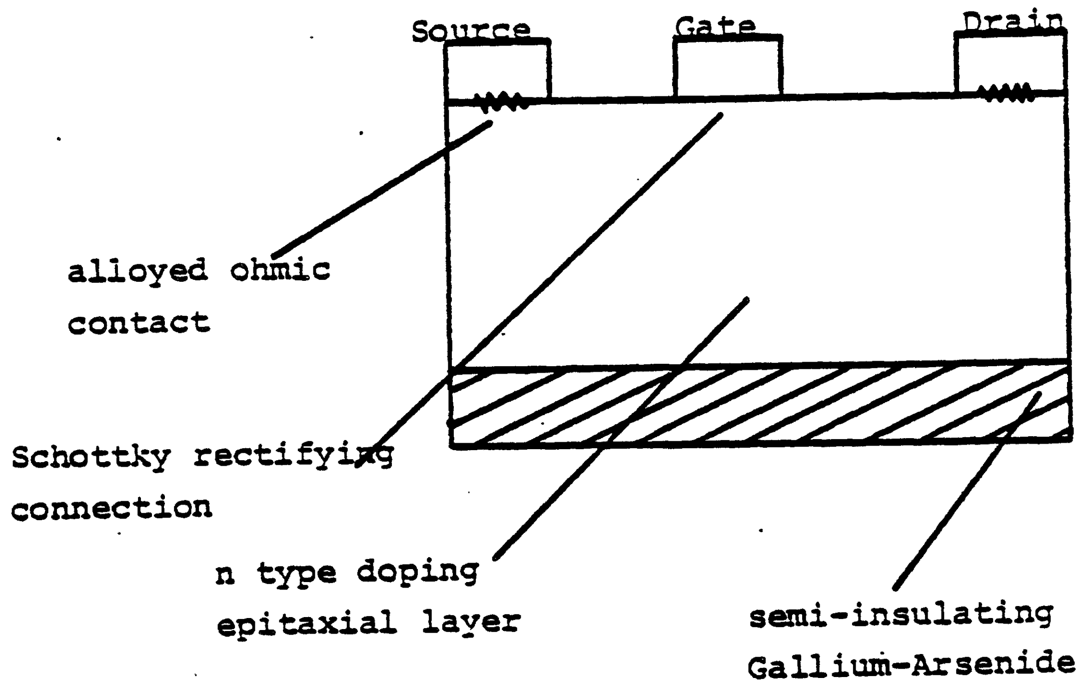

Figure II.1
FET Structure

This is realized by localized heavy doping (10^{19} cm^{-3}) under the electrodes. A short gate length is also needed; recent improvements in the fabrication allow a gate length of typically 0.5 μm.

An important characteristic of Gallium-Arsenide is its non-ohmic behavior for fields greater than 3 kV/cm. Let us consider a microwave FET of gate length 1 μm. A voltage drop of 1 V across this gate corresponds to an average field of 10 kV/cm. One must take the field dependence of the electrons' mobility into account in order to understand the operation of the FET.

2. Electron mobility in Gallium-Arsenide

The conduction band of the GaAs as presented in Figure II.2 has a central minimum at 1.43 eV and a satellite minimum at 1.79 eV; the two of them consist of

valleys with local minima of potential energy [1].

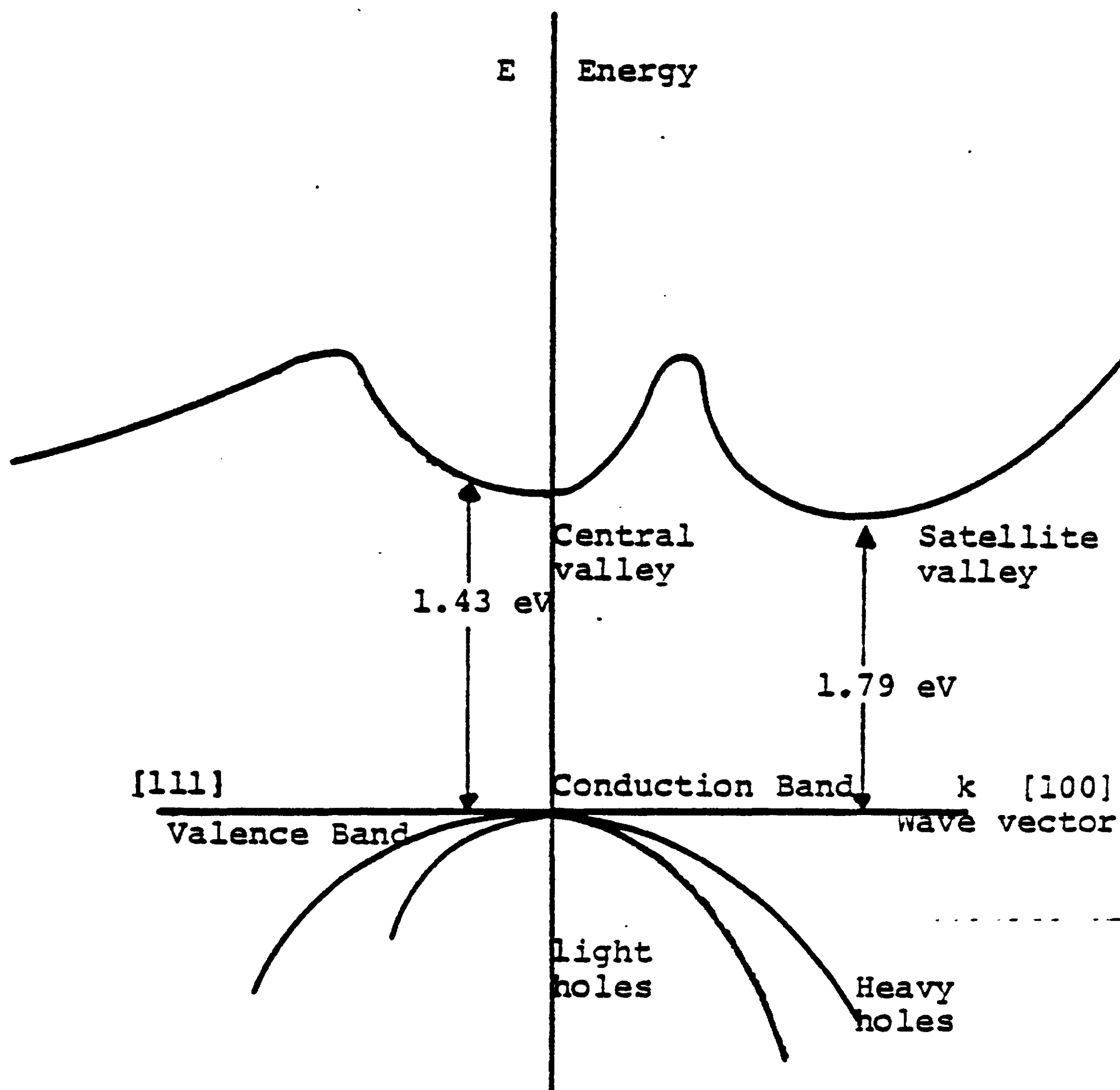

Figure II.2

Energy – Band Structure of Gallium – Arsenide

Rees [3] has calculated the electron velocity versus the applied electric field for the two valleys. These results are plotted in Figure II.3.

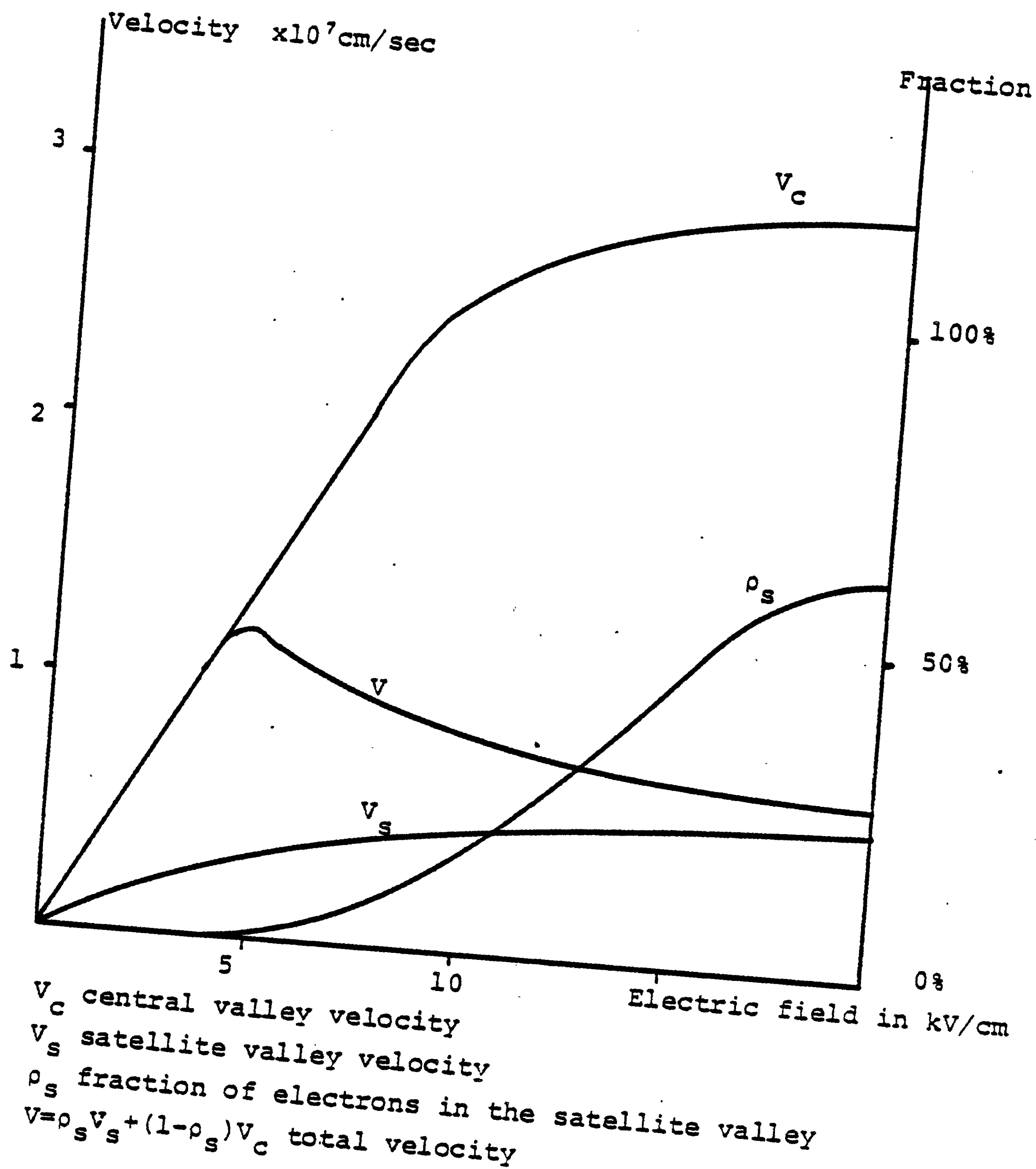

Figure II.3
Carrier Drift Velocity versus Electric Field for High Purity Gallium–Arsenide

For low fields, below 2 kV/cm, all the electrons are in the central valley ($\rho_s = 0$). As the field increases, conduction electrons tend to transfer to the satellite valley. The life time of the electrons in this valley is only 1.8 picoseconds and they tend to return to

the central valley. This travel of electrons back and forth between the two valleys will contribute to the noise of the FET. But, as the electric field increases, the time average fraction of electrons in the satellite valley also increases. For a field of 15 kV/cm, nearly 75 % of the conduction electrons are in the satellite valley. In the central valley, the mobility of an electron is about 8500 cm^2/Vs and its effective mass 0.068 m_0, where m_0 is the mass of the free electron. Higher effective mass in the satellite valley (1.2 m_0) reduces its mobility to about 100 cm^2/Vs. Electrons of the satellite valley essentially do not contribute to the conduction process. At low fields, the mobility is approximately constant, the velocity and therefore the current are almost linear. As the field increases, the current no longer obeys the linear relationship. At 3 kV/cm the transfer of electrons becomes significant. The current reaches a maximum for a field of 4 kV/cm. Higher fields up to 20 kV/cm cause the current to decrease and yield a negative differential mobility.

The saturation in velocity for carriers (electrons) in the central valley for fields greater than $E_p = 4\ kV/cm$ can be explained as follows. For fields greater than E_p, electrons have an energy comparable to the energy of an optical phonon; an increase in the electric field causes energy to transfer to the lattice and not to the carriers.

Rees also studied the way electrons respond to a transient field applied over the DC value when a sudden change in the field is applied. That is, carriers in the satellite valley reach equilibrium faster than the carriers in the central valley (0.1 picoseconds versus 5 picoseconds). This is more visible if the transient field applied is higher than 4 kV/cm [4]. As the electric field is applied, a time period of approximately 1 picoseconds passes before electrons are transferred from the central to the satellite val-

ley. During that period, they remain in a high mobility state and therefore acquire a high velocity. This total drift exceeds the steady state velocity they reach at equilibrium by more than a factor of 2. This effect is nevertheless only noticeable for FET's with a gate length less than 3 μm, which is the case for most recent FET's.

3. FET operation

During normal operation, the FET has a positive drain and a negative gate tension with respect to the source. Its principle of operation is explained in Figure II.4 [4]. A depletion region without carries is formed under the gate. This acts as an isolator and the electrons are constrained to flow through the channel so created. The height of the depletion region depends on both the applied gate to source and the drain to source voltages. The fluctuation of the tension V_{GS} that modulates the height of the channel also modulates its resistance and the drain current. This is the amplification mechanism of the FET.

Proceeding from the source to the drain, the depletion region becomes larger, the channel narrower. To compensate for this decrease in the channel cross section, the electric field and the velocity of the electrons increase. As the electric field increases, the electrons tend to transfer to the satellite valley. Himworth showed [5] that the velocity rises to a peak at x_1 then falls to a saturated value under the gate. The height of the conducting channel in this saturated region is approximately constant. This relatively slow movement of carriers under a high electric field, in order to maintain the drain current, requires a heavy electron accumulation. Between x_2 and x_3 (see Figure II.4) exactly the opposite phenomenon occurs. That is, the channel widens and the electrons move faster as they regain the central valley.

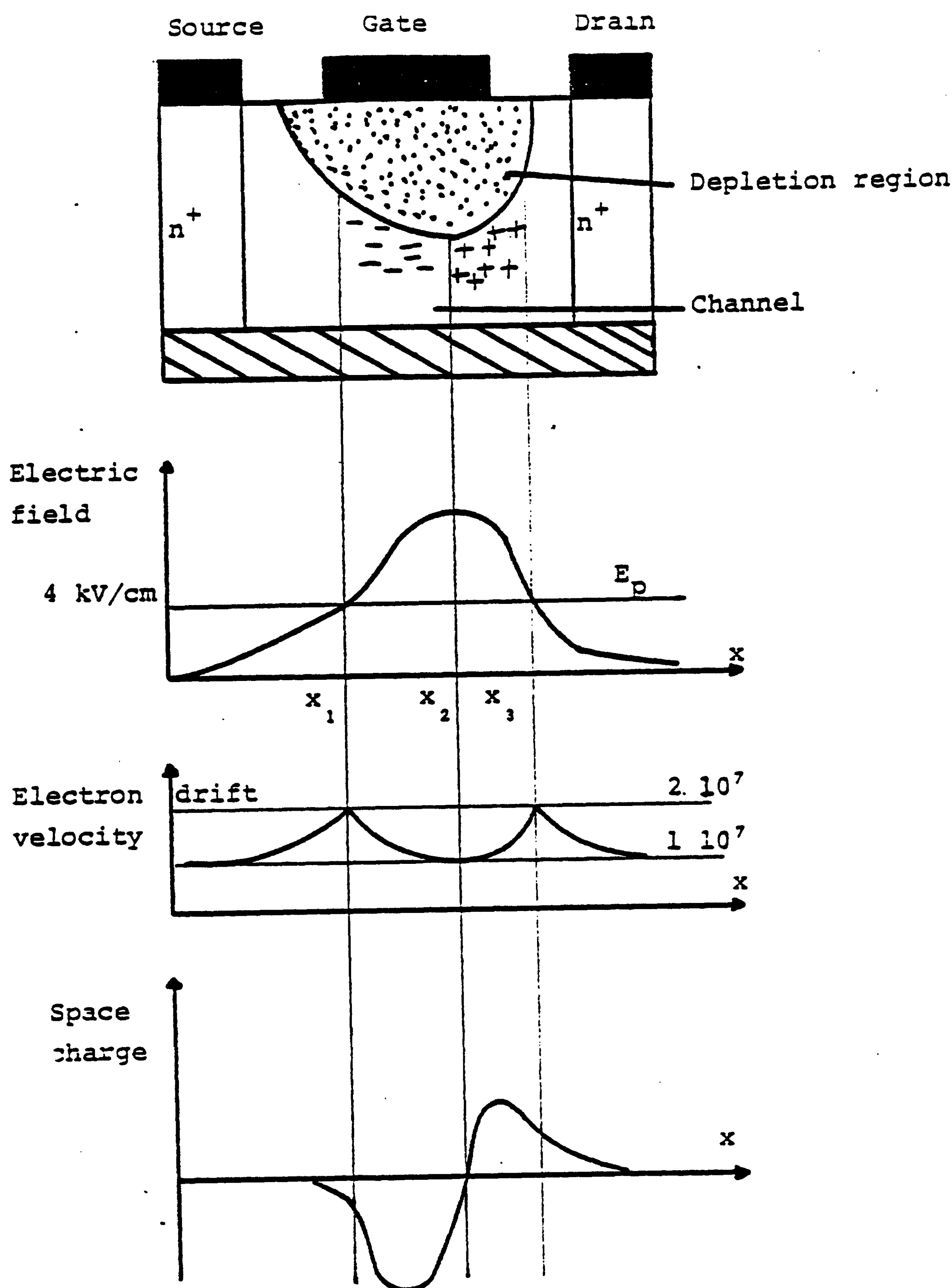

Figure II.4

Channel Cross-Section, Electric Field, Electron Drift Velocity and Space Charge Distribution of GaAs FET

This analysis does not take into account the non equilibrium phenomenon described by Rees that allows the electrons to exceed the peak equilibrium velocity, a phenomenon that occurs for gates less than 3 μm long. This effect increases the

velocity at point x_1 by a factor close to 2 and decreases the velocity at x_3 by a factor of 1.5. Globally, it shortens the transit time of the electron within the "saturated" region. This phenomenon is particularly visible for a gate length less than 1 μm.

Although it has been shown that this model gives an approximate behavior for small gate lengths, it does not permit an analytical treatment.

4. FET DC characteristics and small signal circuit

It is possible to describe the FET behavior using a lumped element network for frequencies up to 12 GHz. Several authors have examined this problem. Currently, the commonly accepted reference work is a paper by Pucel, Statz and Haus [6], which also develops the noise characteristics of the Gallium-Arsenide Field Effect Transistor.

The simplified model Pucel et al. used is illustrated in Figure II.5 and Figure II.6.

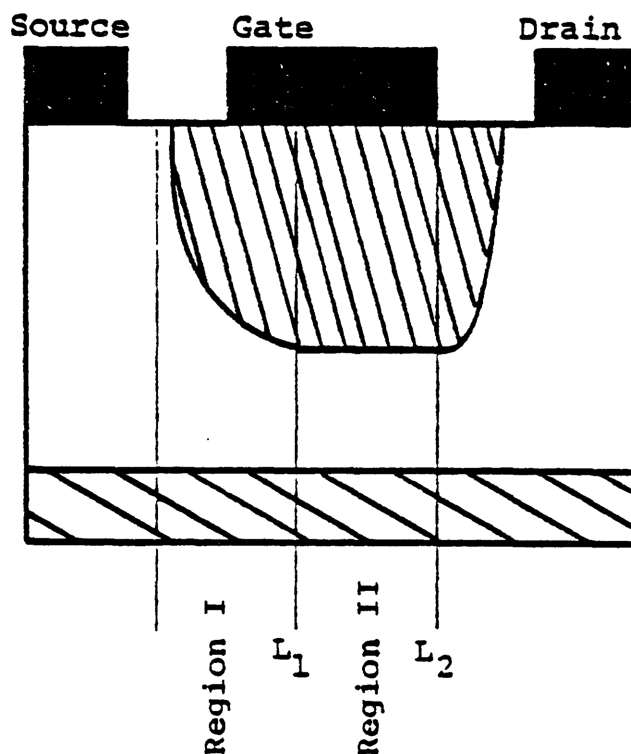

Figure II.5

Idealized Geometry of a Field Effect Transistor

The FET is broken into two parts. The region I close to the source is of ohmic

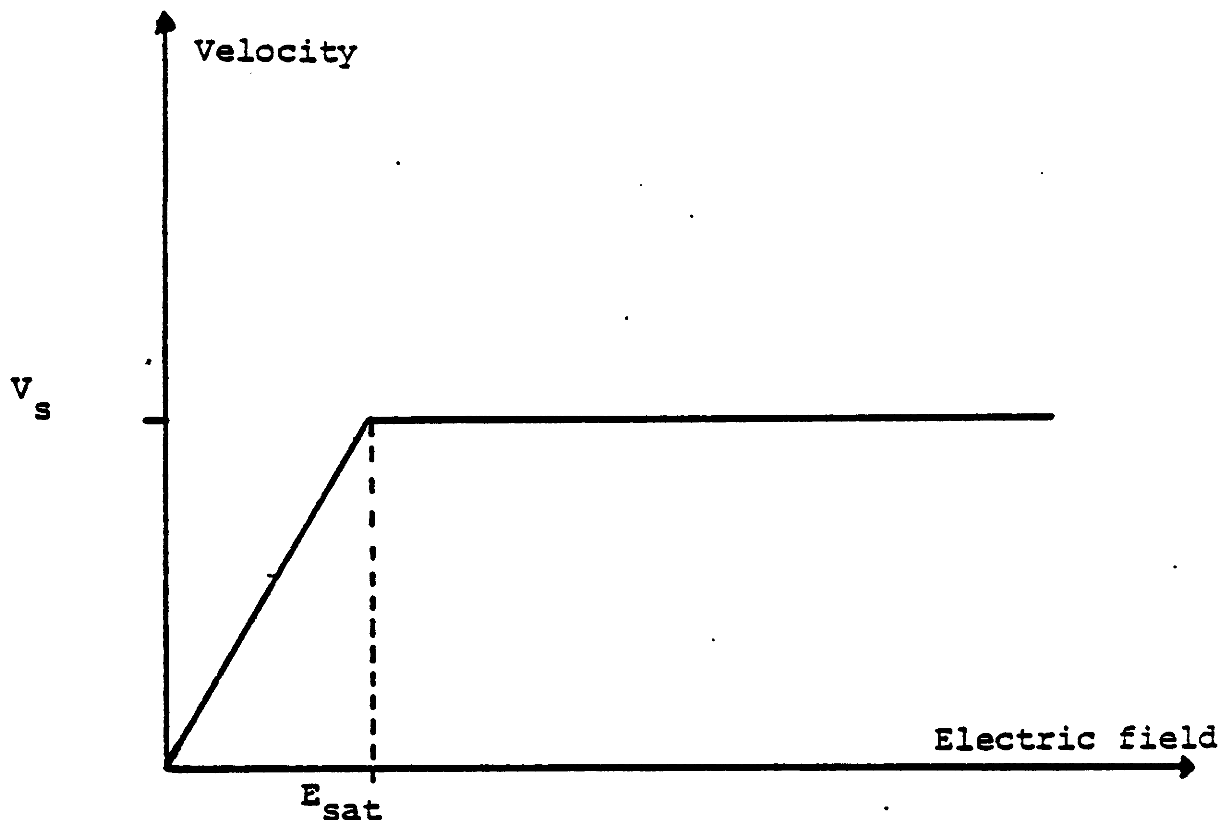

Figure II.6
Piece Linear Simplified Velocity
versus Electric Field Relationship

conductivity and the carriers have a linear velocity with respect to the electric field. For applied voltages exceeding the so called "pinch-off value", the longitudinal electric field will exceed the saturation field (taken to be 3 kV/cm) at point L_1. Beyond this pinch-off point, carriers drift at a constant velocity V_s, while the field due to the free charges on the drain electrode continues to increase, thus assuring that electrons remain within a saturated drift. The position of the pinch-off point and the height of the channel in the saturated region are functions of both gate to source and drain to source voltages.

Using this model Pucel et al. obtained a DC characteristic for a Field-Effect Transistor as presented in Figure II.7. The dotted line marks the limit between DC

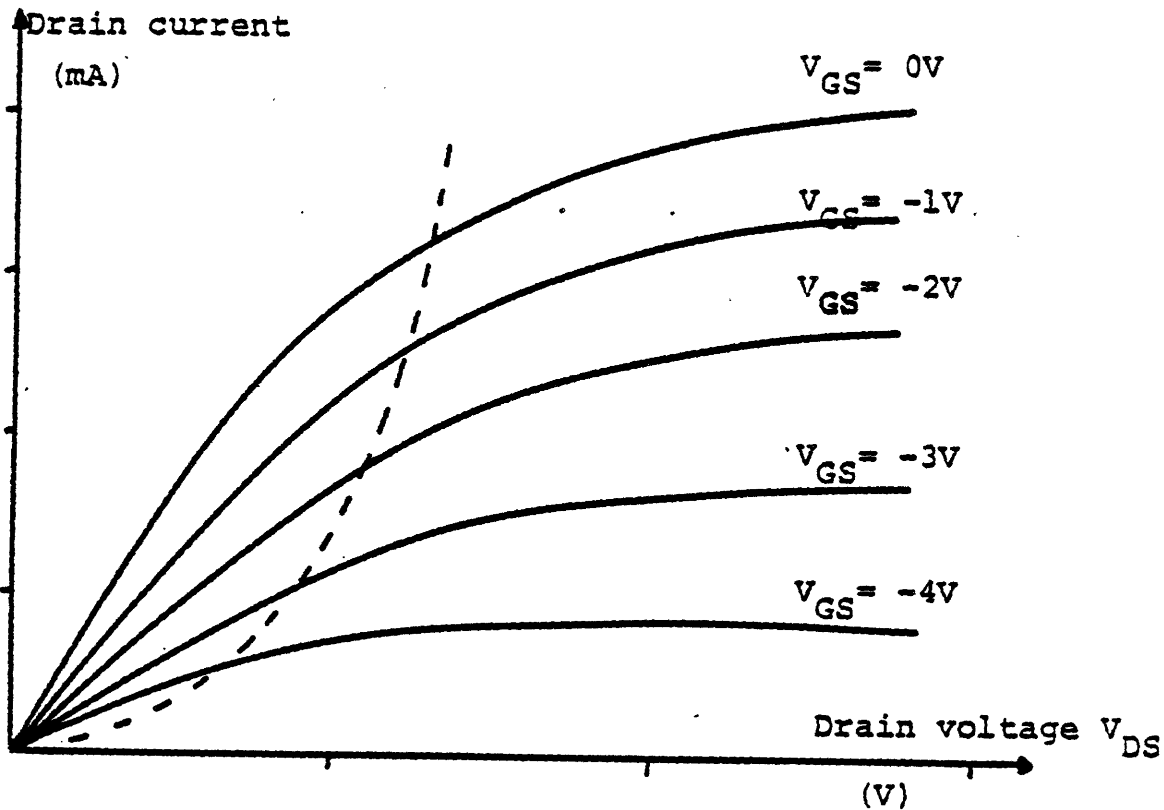

Figure II.7

FET DC Characteristic

bias where the FET works only in ohmic conductivity (at the left of the line) and DC bias where high fields create a velocity saturated region under the gate. The characteristics Pucel et al. derived from their model match well with DC characteristics of actual FET's [7,8], [section IV.3].

This model also provides an equivalent circuit for operation in the common source configuration. Figure II.8 presents the circuit while Figure II.9 shows the physical origin of the circuit elements. The intrinsic elements of the circuit are as follows:

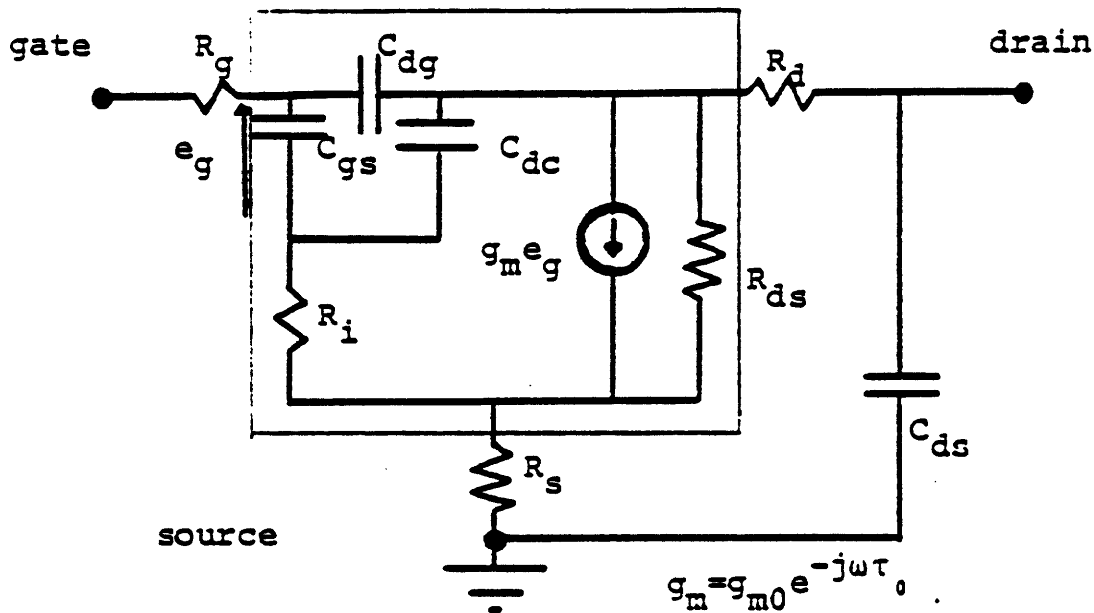

Figure II.8

Small Signal Equivalent Circuit of the GaAs FET

Gate to Channel Capacitance	C_{GS}
Drain to Gate Feedback Capacitance	C_{DG}
Drain to Channel Internal Feedback Capacitance	C_{DC}
Channel Resistance	R_i
Output resistance	R_{DS}
Voltage Controlled Current Source	i_{DS}
Transconductance	G_m
Phase Delay (Transit Time in Saturated Region)	τ_0

The extrinsic (parasitic) elements are as follows:

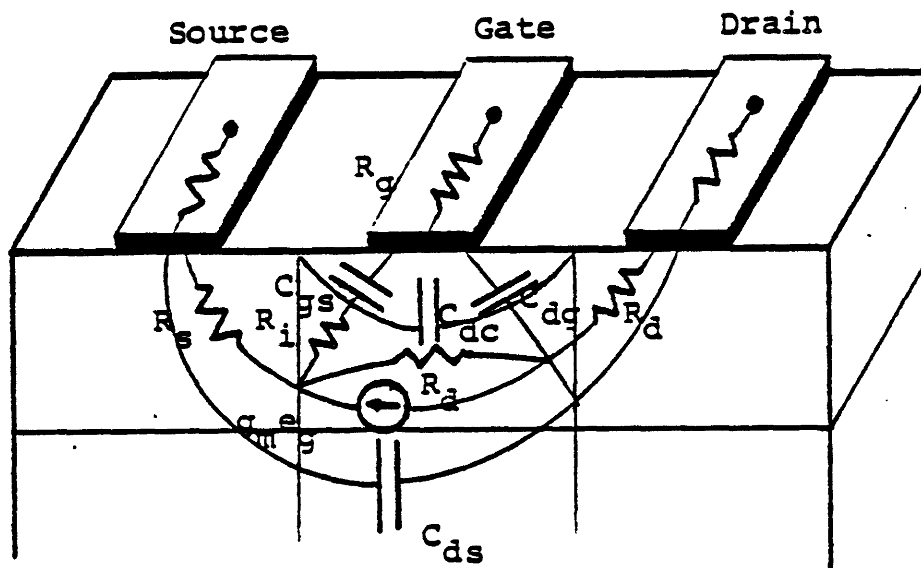

Figure II.9

Physical Origin of Circuit Elements

Substrate Capacitance	C_{DS}
Gate metal and Spreading Resistance	R_g
Drain to Source plus Contact Resistance	R_d
Source to Channel plus Contact Resistance	R_s

It is possible by using this model and the geometry of the FET to determine the frequency limitations of such a device. Let r be the input to output resistance ratio

$$r=\frac{R_g+R_i+R_s}{R_{ds}}$$

let τ be the feedback gate time constant

$$\tau=2\pi R_g C_{dg}$$

f_T the frequency at which the current gain is unity is given by

$$f_T \approx \frac{1}{2\pi} \cdot \frac{g_m}{C_{gs}}$$

The unity gain frequency (also referred as the maximum oscillation frequency) is

$$f_u = \frac{f_T}{2\sqrt{r + f_T . \tau}}$$

Decreasing L the length of the gate decreases the gate to channel capacitance and increases the transconductance. One can also express the current unity gain frequency as a function of the gate length, according to [9]

$$f_T = \frac{v_{eff}}{2\pi L}$$

where v_{eff} is the effective velocity during the crossing of the gate, i.e average of the drift velocity of the carrier over the gate length. For small gate length, v_{eff} is approximately independent of l and f_T varies as $1/L$. To have a high f_T and therefore a high frequency f_u, one needs a short gate and a high velocity carrier. In silicon and Gallium-Arsenide, electrons have a higher mobility than holes; in GaAs, electrons have a six time larger mobility and a two time larger peak drift velocity than in the silicon. This is why only n channel GaAs FET's are used for microwaves applications.

5. Noise theory of the FET

The complete description of the noise properties of the Gallium-Arsenide FET is an intricate problem mainly due to the involvement of noise production. In general, the phenomenon involved in the production of noise are both frequency and temperature dependent, dependences that are not always well understood.

As stated previously, an exhaustive but nonconclusive treatment of the noise production problem was written by Pucel et al. [6]. Pucel et al. predict the correct dependence of noise upon drain current but demonstrate poor agreement with the experimentation at low frequencies and at low temperatures. More recent works correct and improve the original approach [10,11].

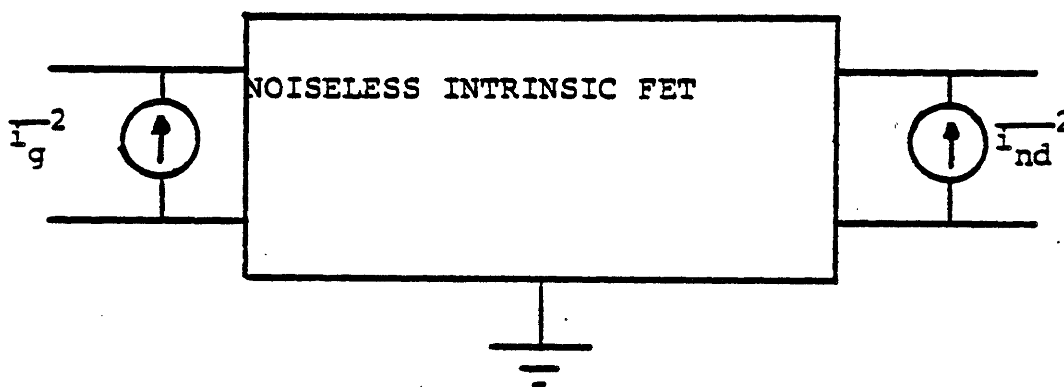

*Figure II.*10
Model of the Noisy FET

The first stage is to analyze the ideal transistor, postponing the computation of the noise contribution due to the parasitics elements. The equivalent circuit for the ideal FET is shown inside the dotted line box in Figure II.8. The noisy transistor can be represented by using two noise current sources, one at the input and one at the output as shown in Figure II.10.

Basically, the noise current of the input represents a Johnson type noise in the channel region which is emphasized by hot electrons in the channel. This noise voltage also causes noisy fluctuations in the depletion layer height. This results in the creation of electric dipoles drifting through the saturated region. The output noise source

represents these dipoles drifting to the drain contact.

The two noise currents i_{nd} and i_{ng} are caused by the same noise voltage in the channel and are therefore correlated. The correlation coefficient is defined as

$$jC = \frac{\overline{i_{ng}^{*} . i_{nd}}}{\sqrt{\overline{i_{nd}^{2}}} . \sqrt{\overline{i_{ng}^{2}}}}$$

where $j=\sqrt{-1}$. The correlation jC is purely imaginary because noise sources in the drain and in the gate circuits are capacitively coupled. The theory of Pucel et al. permits the calculation of $\overline{i_{ng}^{2}}$, $\overline{i_{nd}^{2}}$ and C.

One has to consider separately the two regions of the channel labeled I and II in Figure II.5. In a previous work Baetchold showed [12] that in the Gallium-Arsenide, the measured noise temperature electric field curve can be fitted by

$$T_n/T_0 = 1 + \delta \left(\frac{E}{E_{sat}} \right)^2$$

where T_0 is the physical temperature of the lattice, E_{sat} is the saturation field and δ is an empirical coefficient equal to 6. Using this relationship and the longitudinal dependence of the electric field, Pucel et al. computed for each point of the unsaturated region (region I) the Johnson noise contribution. Integrating over the whole region I, one can compute the induced gate noise current $\overline{i_{gn}^{2}}$.

In the saturated region, we cannot describe the noise as a Johnson noise. The noise current is interpreted as a distribution of spacialy uncorrelated impulses. Each of these impulses results in a displacement of a charge and produces a dipole. The dipole is created within a saturated velocity region and is thus unable to relax. The dipoles so created then drift unchanged to the drain contact where the drain noise current $\overline{i_{dn}^{2}}$ can

be calculated. Through capacitive coupling the noise production in region I will contribute to the noise current on the drain and vice-versa. These contributions are summarized in the overall correlation coefficient jC.

The mean square time average of $\overline{i_{nd}^2}$ and of $\overline{i_{ng}^2}$ can be expressed by [12]

$$\overline{i_{nd}^2} = 4kT_o \Delta f g_{mo} P$$

$$\overline{i_{ng}^2} = 4kT_o \Delta f \omega^2 C_{gs}^2 R / g_{mo}$$

where k is the Boltzmann constant, T_o the lattice temperature, Δf the bandwidth, ω the angular frequency, C_{gs} the gate to source capacitance, g_{mo} the magnitude of the low frequency transconductance, P and R both dimensionless factors dependent on the device geometry and on the DC bias.

The extrinsic resistances R_s and R_g generate thermal noise themselves and degrade the noise performance of the FET. The equivalent circuit model for the FET which includes the noisy parasitics is shown in Figure II.11.

One can express the minimum noise figure (see section II.6) of the intrinsic FET as a function of the parameters R, P and C. Under the assumption $f \ll f_T$ (This is usually the case; a typical value of f_T is 90 GHz), we have

$$F_{\min} \approx 1 + 2\sqrt{PR\left(1 - C^2\right)\frac{f}{f_T}}$$

We can have for short gate length a correlation coefficient close to one in magnitude and a substantial noise cancellation, corresponding to a destructive interference of the two noise currents.

The above expression predicts for low frequencies an almost linear dependence of

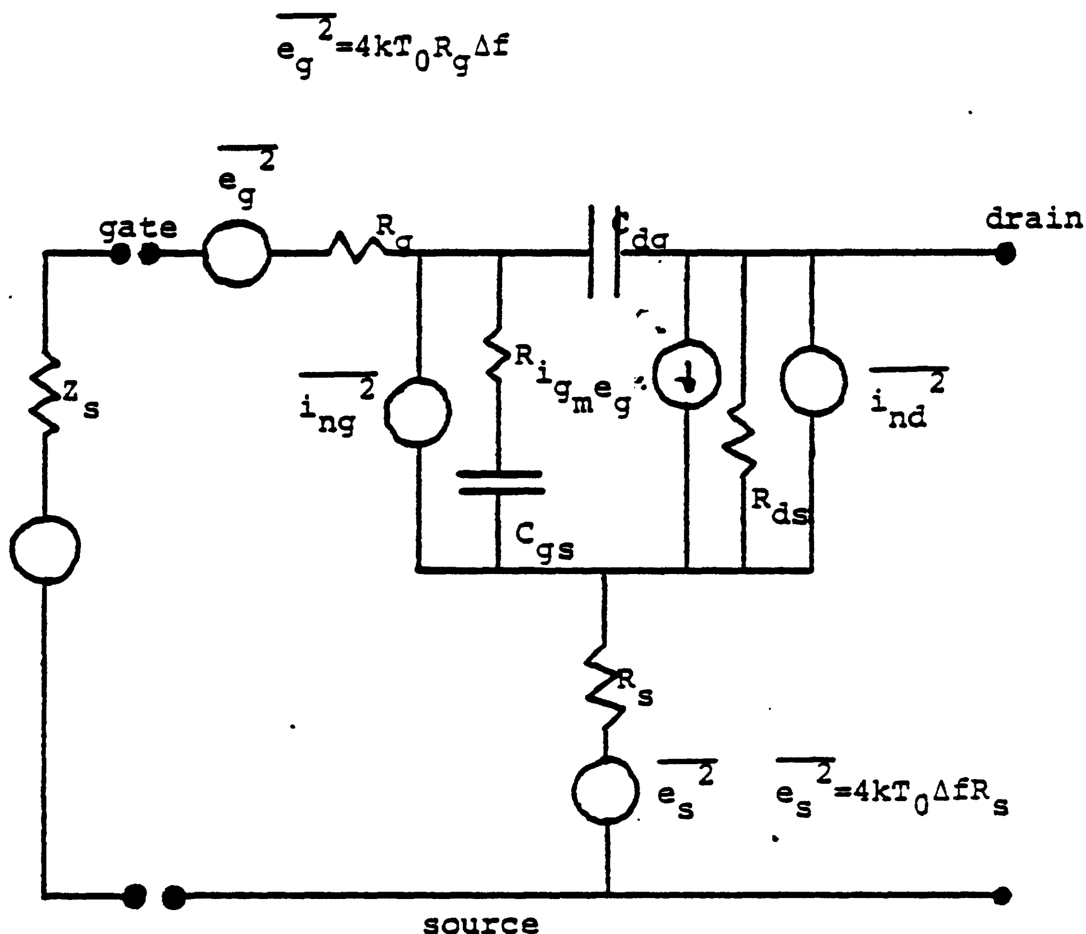

Figure II. 11

Equivalent Circuit for Noise Calculations

the minimum noise figure with frequency. Such a decline was not observed. Recent works at low temperatures [13,14] revealed a disagreement between Pucel et al.'s results and the experiment.

Several explanations were advanced to agree with experimental results. Pucel et al proposed a trap theory with traps at the epitaxial layer substrate interface. But the temperature dependence of the trap theory was found to differ from the experiment. Another explanation was that of the intervalley scattering noise [15]. The intervalley scattering noise is a weak function of the physical temperature of the lattice and thus

can be a significant contribution at low temperatures.

A different approach of the problem is proposed by Graffeuil [16] who considers the electron noise temperature to be both electric field and frequency dependent. Using this model, he succeeds to match theory and practice well. More recently, Brookes [11] reconsidered the Pucel et al.'s original approach applying it to a channel whose thickness is not constant but modeled as a gaussian random variable. Even when the variations of the channel height are small compared to its mean value, he matches low frequency noise figure data.

6. FET Noise Representations

The noise figure of a twoport device is defined as the ratio of the noise of the output of the two port driven by a noise source to the noise of the output of the same twoport idealized (noiseless) when driven by the same noise source.

The noise source used to compute the noise figure F is an impedance Z_s combined with its associated equivalent thermal noise source as described in Figure II.11. Using the expression for the noise generators of the FET it is possible to show [17] that the noise figure can be written as

$$F = 1 + \frac{1}{R_s}\left[r_n + gn\left|Z_c + Z_s\right|^2\right]$$

where $Z_s = R_s + jX_s$ is the source resistance and r_n, gn, Z_c three intermediate parameters whose theoretical values can be derived from the Pucel theory [6]. Z_c is known as the noise correlation impedance. F is a minimum when Z_s is at an optimum, ie

$$R_{opt} = \left[\mathrm{Re}\left(Z_c\right)^2 + \frac{r_n}{gn}\right]^{1/2}$$

$$X_{opt} = -Im\left(Z_c\right)$$

Expressed directly as a function of P, R, C and f_T the value of F at the minimum is

$$F_{min} = 1 + 2\sqrt{PR\left(1-C^2\right)\frac{f}{f_T} + 2g_m R_i P\left(1-\sqrt{P/R}\right)\frac{f^2}{f_T^2}}$$

Another representation of the noise behavior of the device is its equivalent noise temperature. This is related to the noise figure by the relation

$$T = T_0\left(F-1\right)$$

where T_0 is equal to 290 K

Any noisy two ports noise temperature can be represented by four parameters: the minimum noise temperature T_{min}, the optimum source impedance $Z_{opt} = R_{opt} + jX_{opt}$ and the noise conductance gn [17].

The noise temperature as a function of the source impedance $Z = R + jX$ is given by

$$T_n = T_{min} + T_0\frac{gn}{R}\left[\left(R - R_{opt}\right)^2 + \left(X - X_{opt}\right)^2\right]$$

The relation between the two representations is known as the Rothe-Dalke relations

$$R_n = gn\left|Z_{opt}\right|^2$$

$$R_c = \frac{T_{min}}{T_0}\cdot\frac{1}{2gn} - R_{opt}$$

$$X_c = -X_{opt}$$

$$r_n = gn\left(R_{opt}^2 - R_c^2\right)$$

The relations developed in this chapter form the basis for interpreting the experimental results.

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CHAPTER III: FET PARAMETERS

1. Scattering parameters

At microwave frequencies, the only quantities directly measurable are the amplitude and phase angle of propagating waves. If one considers an N port device [1] , at each of its ports, part of the input wave is reflected and part is transmitted (scattered) to other ports. If we denote with $\bar{a}$ the vector composed of the incident wave amplitudes and $\bar{b}$ the vector composed of the emanating wave amplitudes, the relation between $\bar{a}$ and $\bar{b}$ for a linear device is:

$$\bar{b} = \bar{\bar{S}}\bar{a}$$

where $\bar{\bar{S}}$ is the power scattering matrix. In the case of the FET, this S matrix is composed of only four parameters. These parameters are in general complex and thus require, for the phase term one or more reference planes for the phase term. Manufacturers usually provide the value of the various scattering parameters without indicating the plane they are referenced to. This causes a problem when using these specifications at high frequencies where small physical distances can create large phase shifts.

Measurement Techniques

Two different FET's from different manufacturers (NEC,ALPHA) were chosen to be studied and used in a cryogenically cooled amplifier; table III.1 presents the two manufacturers' claims [2,3].

FET	F_{min}	$G_{Associated}$
ALPHA 3003	1.5 dB	14 dB
NEC 13783	1.2 dB	11 dB

at 8 GHz

*Table III.*1

The ALPHA MESFET was found to oscillate around 3.5 GHz for a large variety of source impedances when biased with a drain current of 30 mA and was therefore disregarded for the use in the amplifier. Its scattering parameters were not even measured.

The scattering parameters of the NEC FET were measured using the test fixture described in Figure III.1. The test fixture does not allow the biasing of the transistor, thus avoiding the creation of parasitic elements due to DC bias networks. The task of biasing the FET was performed by two bias Tee networks (HP 11590A). They were found to be negligeably lossy over the frequency range of measurements. Two different kinds of connectors were used to connect the dielectric board to the network analyzer used for the measurements. The APC-7 standard was used at room temperature to obtain a better accuracy and an overall lower VSWR; heat links were avoided by using the OSM standard at cryogenic temperatures. The fixture's microstrip has a characteristic impedance of 50 Ω and lies on a teflon fiberglass board.

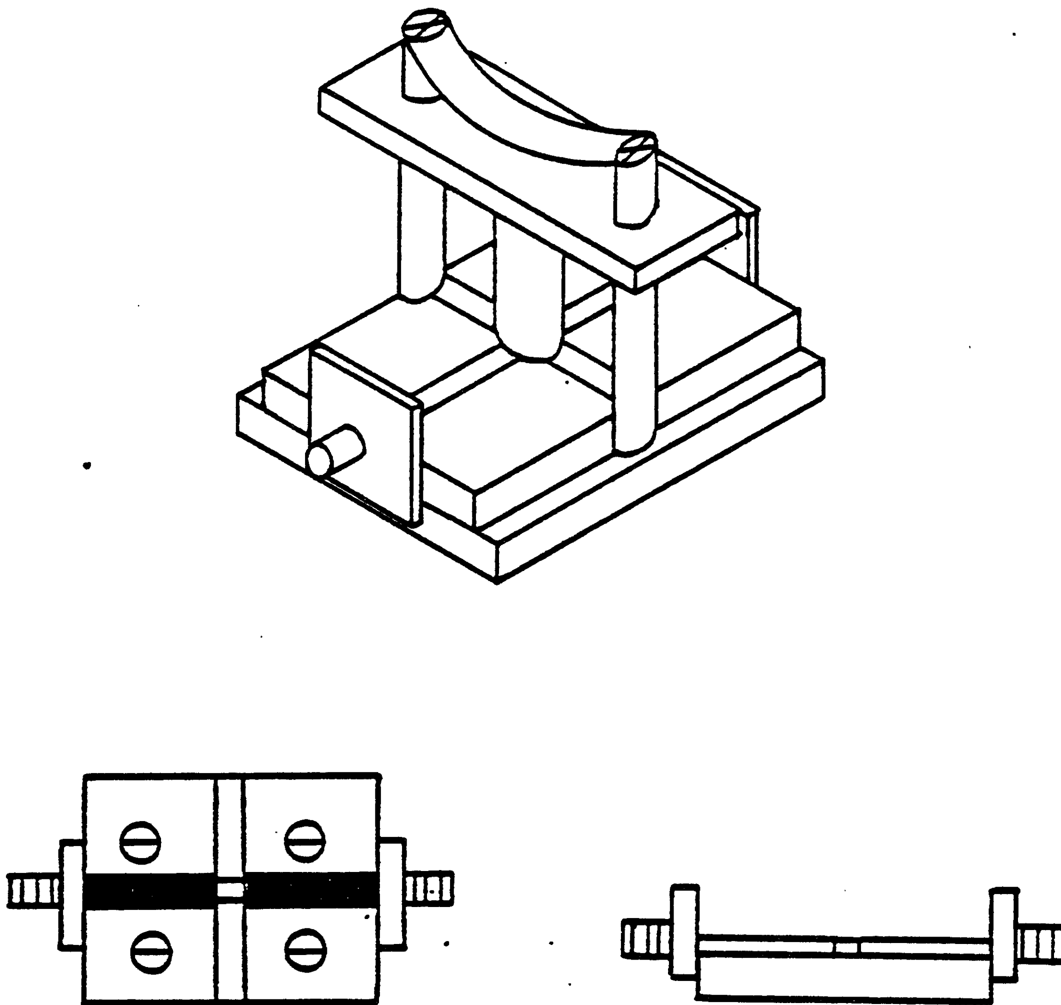


Figure III.1
Test Fixture Used for *Scattering*
Parameter measurements

A teflon cylinder was placed over the device and held firmly against the board with a spring like piece of copper (see Figure III.1). Between 8 and 10 *GHz*, the teflon cylinder created a phase shift of less than 2 degrees and an amplitude change less than .15 *dB* (<2 %). The gap between the input and the output boards was designed to exactly fit the FET package, so as to reduce phase errors due to positioning. These were limited to about 5 degrees at 8 *GHz* and 7 degrees at 10 *GHz*. The gap between the two source pads was equalized to that of the experimental amplifier. In order to

limit parasitic capacitance between gate and source, the ground plane under the transistor was milled down [4].

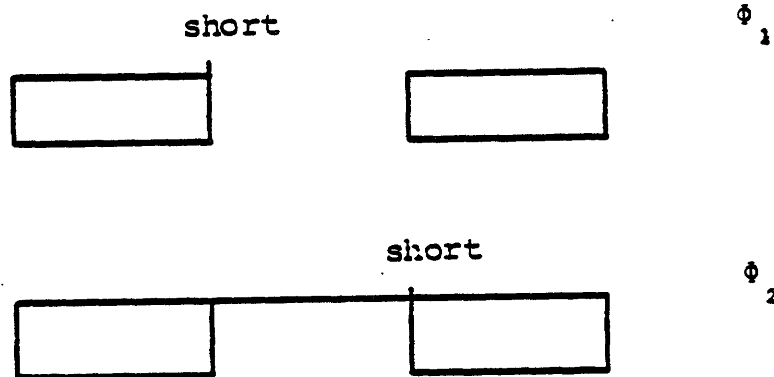
To set the reference in the measurement of the S_{ii} parameters, a 2 mils thick flexible piece of copper was positioned at the edge of the board and folded over the source pad. A small drop of solder provided the connection with the microstrip. This set the reference planes for the S_{ii} at the edges of the FET package. For the measurements of the S_{ij} parameters, a piece of copper with the width and thickness of the FET drain pin was held over the gap with the teflon cylinder. The S_{ij} parameters were therefore referenced to the center of the package.

To correct for the phase shift over the FET's package, a careful measurement of the electrical length of the copper pin was made. The phase of the reflexion for shorts placed on both sides of the gap were measured and the electric length was determined (see Figure III.2).

Results

All the parameters were measured using a Hewlett-Packard network analyzer. The different scattering parameters were measured for a V_{DS} of 3 V and a drain current of both 10 mA and 30 mA to compare with the manufacturer's specifications. Twenty one measurement points were taken over the frequency range of 8 to 10 GHz in order to use the available computer routines. The Figures $III.3\ a$ and $III.3\ b$ present a typical scattering parameter measurement at room temperature.

The reflexion coefficient magnitude agreed within 10% of the specifications of the constructor, the phase was off by 25 degrees for S_{11} and by a factor ranging from 30 to



$$\Phi_{pin} = \frac{\Phi_2 - \Phi_1}{2}$$

Figure III.2

Phase Measurements

40 degrees for S_{22}. A shift of 20 degrees corresponds (using an approximate theoretical description of the FET case) to the phase difference between the edge and the center of the FET package. Stresses introduced as the result of the cryogenic cooling displaced the microstrip off the board. This caused the dispersion in the phase shift of S_{22}. The remaining phase difference is most probably due to the measurement errors. One can conclude from these results that the manufacturer takes the center of the package as the reference plane for the scattering parameters.

Transmission coefficient magnitudes were found for different FET's varying between ±10% from the manufacturer specifications. This kind of dispersion was predictable for the transducer gain S_{21} but was not expected for S_{12}. The phase of S_{21} was found usually within 10 degrees of the claimed values. In addition S_{12} was found to be off by a factor of 90 degrees for one FET and by 10 to 30 degrees for the others.

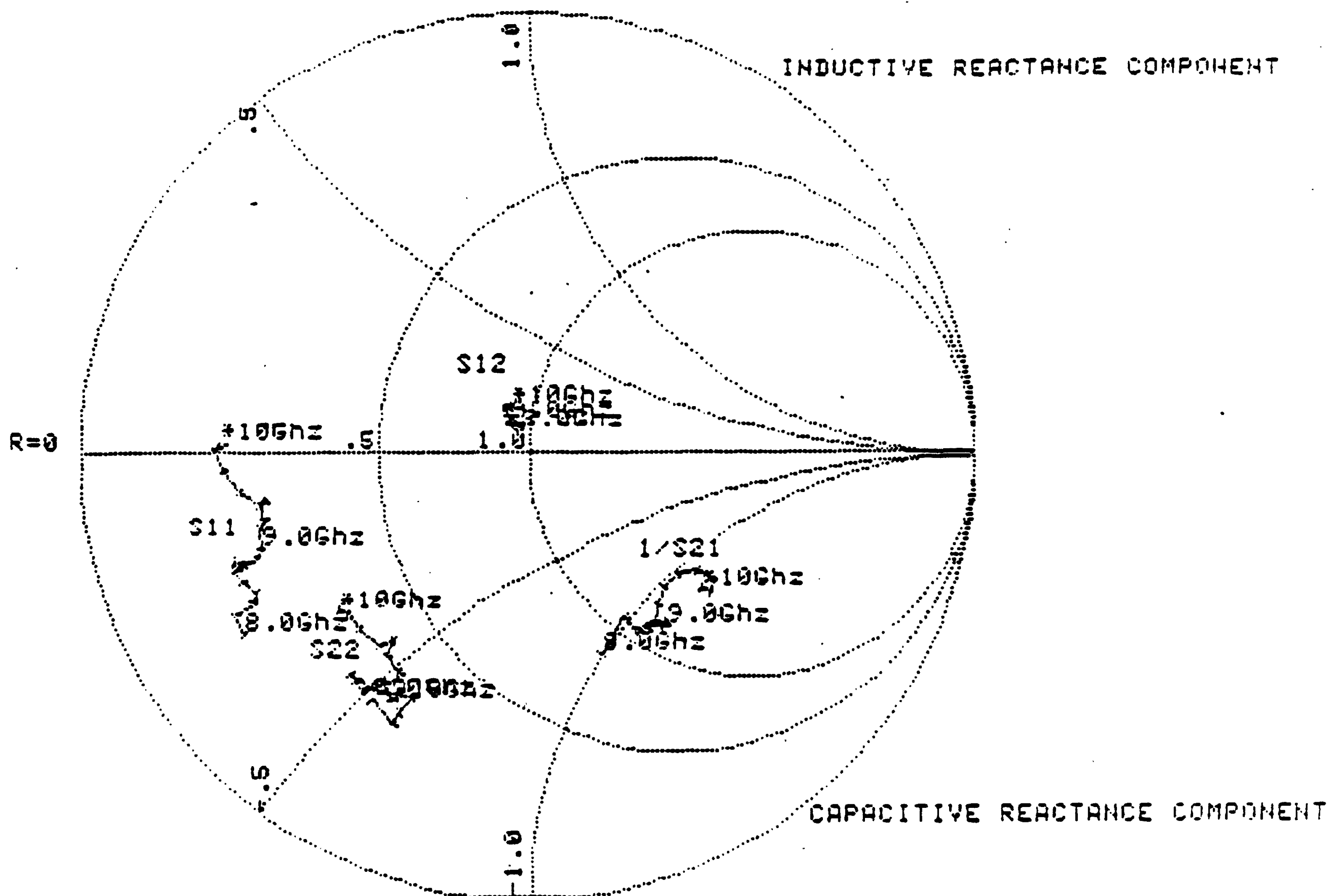


Figure III.3 a

Scattering Parameters at Room Temperature

$V_{DS}=3\ V \quad I_d=10\ mA$

Different measurements for the same FET provided results within 10 degrees. One possible explanation for this discrepancy is that the low level of the output signal does not allow the network analyzer to phaselock it.

2. Gain and Stability

From the measured power scattering parameters, one can determine the oscillation conditions and the different gains associated with the FET. The invariant stability factor k introduced first by Rollet [5] is the simplest way to uniquely describe the degree

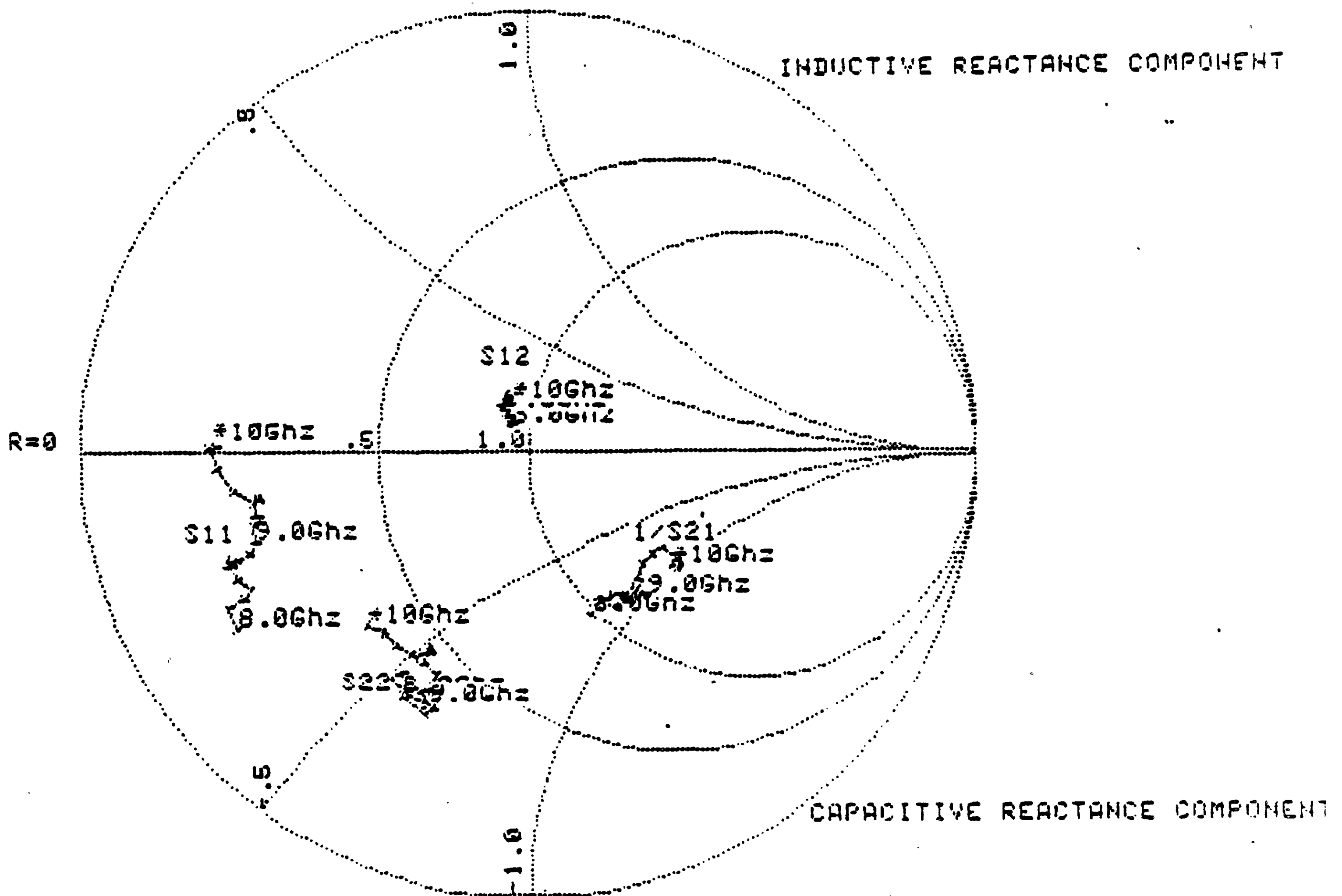


Figure III.3 b

Scattering parameters at Room Temperature

$V_{DS} = 3\ V \quad I_d = 30\ mA$

of stability of the transistor. Expressed as a function of the scattering parameters, k can be written as

$$k = \frac{\left(\left|S_{11}S_{22} - S_{12}S_{21}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2\right)}{2\left|S_{12}S_{12}\right|}$$

If k is greater than one, the FET will never oscillate for any value of passive source and load impedances. Therefore matching the FET for maximum gain or minimum noise can be done without restriction. The maximum available power gain

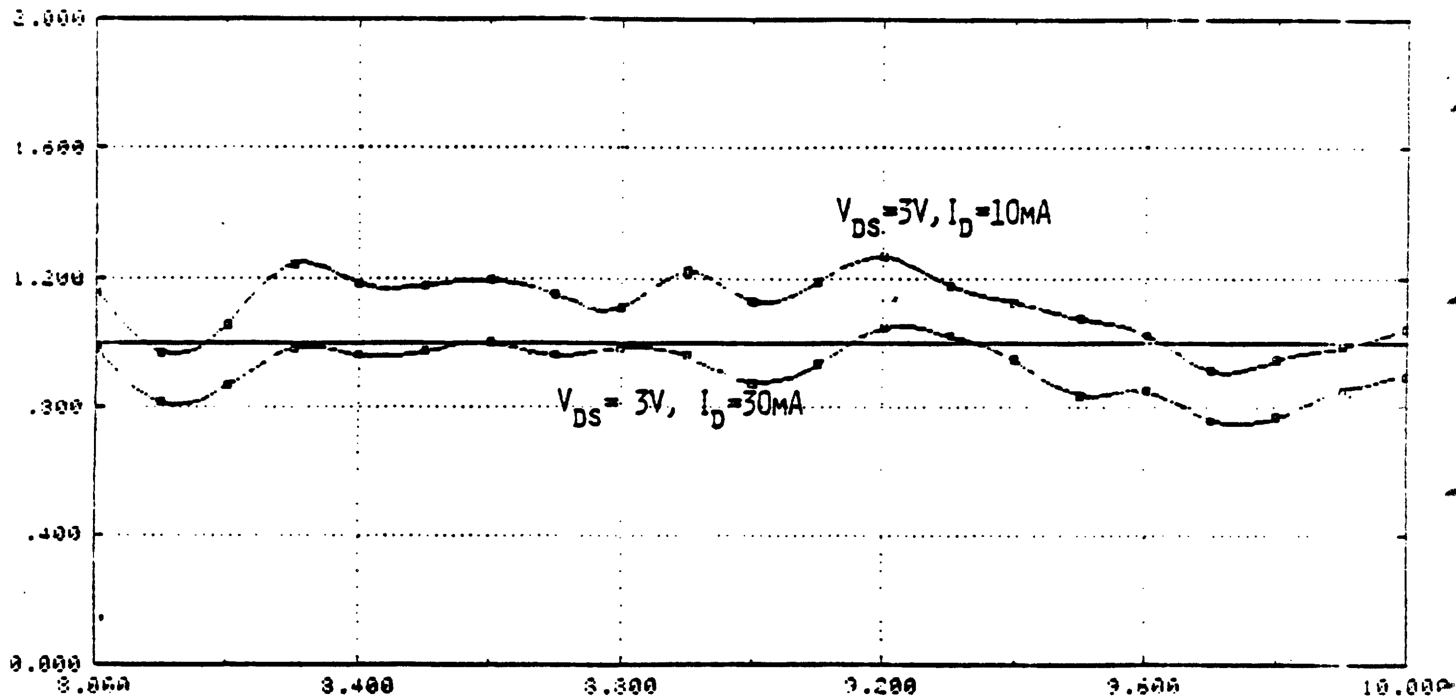


Figure III. 4

NEC 13783 *Stability Factor*

G_{ma} is obtained when the input and output are matched to their respective conjugates. In terms of the stability factor

$$G_{ma} = \left|\frac{S_{21}}{S_{12}}\right| \left(k \pm \sqrt{k^2 - 1}\right)$$

The greater k, the more stable the transistor.

If k is less than one, certain passive source or load impedances will create unstability and cause the transistor to oscillate. In the input and output planes, these unstable regions are inside circles [6] whose centers and radii are direct functions of the scattering parameters. The maximum stable power gain G_{ms} is obtained by padding the input and output of the FET with lossy elements so that the overall twoport is unconditionally stable [5]. In terms of the S parameters,

$$G_{ms} = \left| \frac{S_{21}}{S_{12}} \right| .$$

The measurement of the scattering parameters at cryogenic temperature requires the use of long semi-rigid cables to hold the test fixture in liquid nytrogen. These cables present an electrical length of several tens of a wavelength whose exact value depends on the shape of these cables. This electrical length problem prevents any accurate measurement of the phase of the scattering parameters.

Because the phase of the scattering parameters was not measured at cryogenic temperature, the computations of k, G_{ma} and/or G_{ms} were performed only at room temperature.

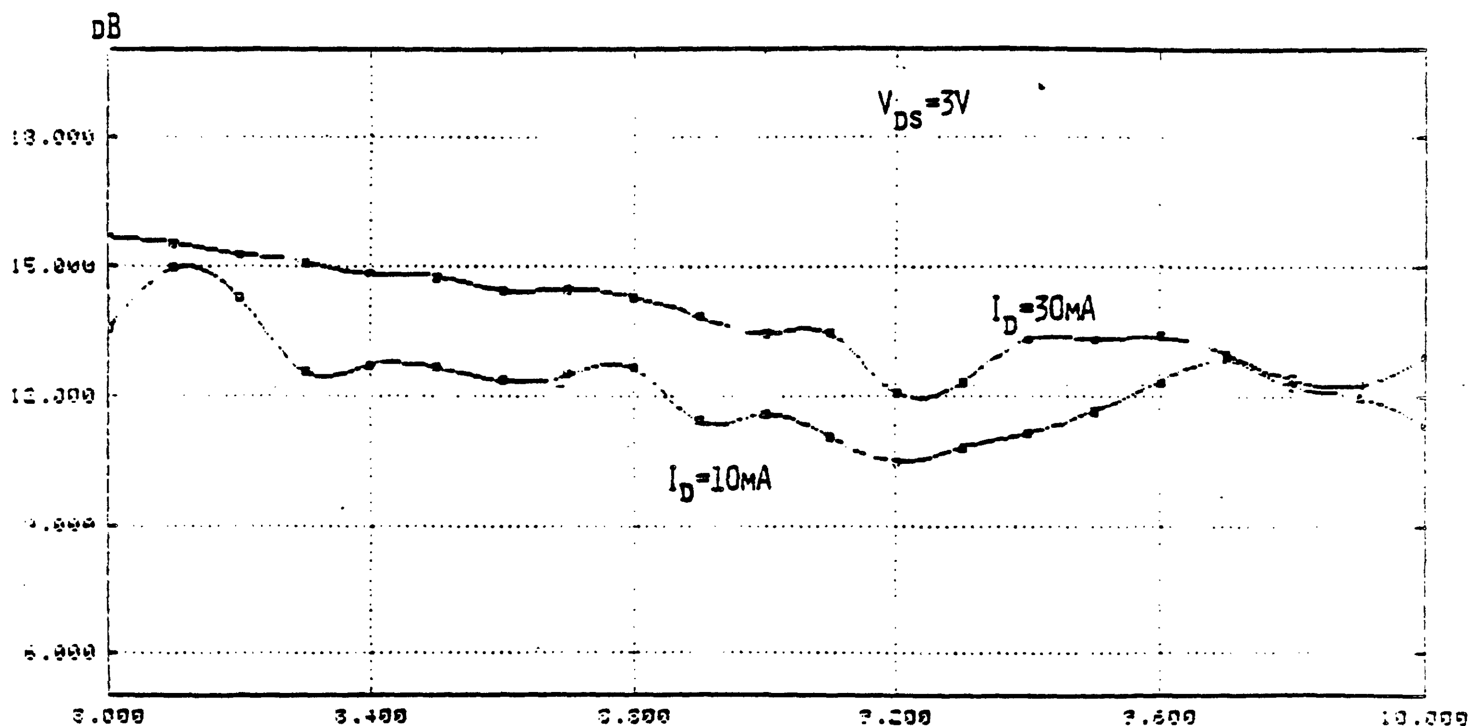


Figure III.5

NEC 13783 *Maximum Available Gain*

The Figure III.4 presents a typical plot of the variation of the stability factor k

with frequency for a drain current of both 10 *mA* and 30 *mA*. The stability factor is lower for a bias of 30 *mA*, principally because of the increase in the magnitude of S_{21}. Errors in the determination of the S parameters yield inaccuracies in the computation of the k factor. S_{21} and S_{12} are the two parameters most subject to measurement errors ($\pm 10\%$) and this results in an error bound of $\pm$ 15% for k. Between 8 and 10 *GHz*, the NEC 13783 has a stability factor close to one and this 15% error bound puts it at the threshold of being conditionally or unconditionally stable. Therefore, one has to be very careful before drawing any conclusion about the stability of this particular transistor in the 8 to 10 *GHz* band.

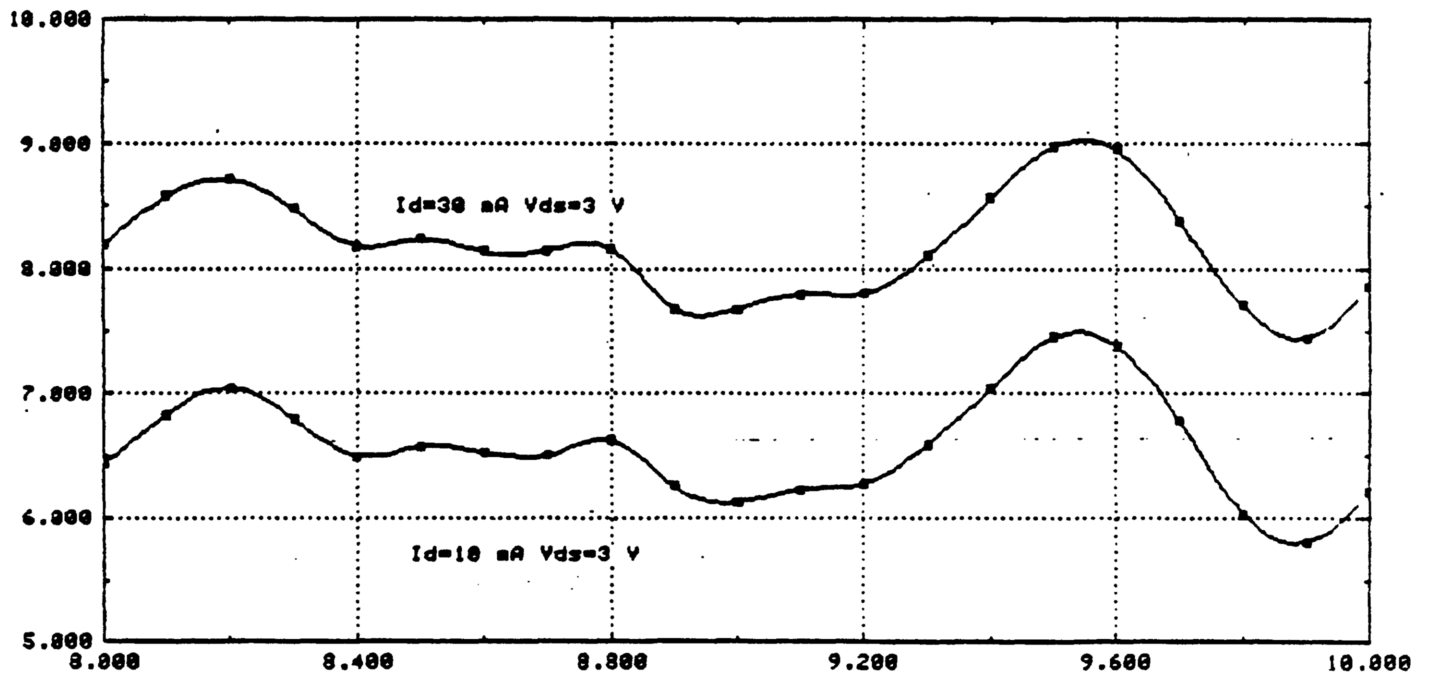


Figure III.6

NEC 13783 *Transducer gain*

Figure III.5 presents the computed maximum available gain (or maximum stable gain when k is less than one) as a function of frequency for the same bias currents as

before. As for the k factor, the same restrictions apply toward the accuracy of the computation of the gain of the FET.

The only directly measurable gain using the presented test fixture is the transducer power gain G_T of the FET when input and output are matched to 50 Ω. In such a case, G_T is equal to $|S_{21}|^2$. A typical plot of the variation of $|S_{21}|^2$ with frequency for both room and cryogenic temperature is presented in Figure III.6.

3. Noise Parameters

Theory of measurement

A way of obtaining the optimal source impedance and the minimum noise temperature of the FET is to look at the minimum while varying the source impedance. The problem encountered in using this method is that it is tedious and empirical. Since at the optimum configuration the partial derivatives of the noise temperature with respect to the source impedance are zero, it is inaccurate for the determination of R_{opt}, X_{opt} and T_{min}. A better way to measure the noise parameters of the device is to employ the analytical expression of noise temperature versus source impedance.

As seen in chapter II, the noise temperature as a function of the source impedance of the FET can be expressed as

$$T_n = T_{min} + \frac{T_0}{R}\left[\left(R - R_{opt}\right)^2 + \left(X - X_{opt}\right)^2\right]$$

If we maintain R constant and let X sweep through a range of reactance, T_n can be written

$$T_n = a + b\left(X - X_{opt}\right)^2$$

i.e a parabola whose minimum is located at $X = X_{opt}$. Likewise, if X is maintained constant, the T_n versus R curve will be asymmetric

$$T_n = a + b\frac{\left(R - R_{opt}\right)^2}{R}$$

whose minimum gives R_{opt}. Fitting the parabola gives the noise conductance gn. $T_{\min}$ is measured by setting $R = R_{opt}$ and $X = X_{opt}$. One can deduce that the parameters of a FET can be easily found if an amplifier that allows R and X to be varied independently of each other is built. This can be easily be done at frequencies up to 1-2 GHz with lumped elements such as inductances in series with adjustable quarter wave transformers, but cannot be realized in the X-band. One can ponder the usage of commercial tuners but the range of impedances they can provide is limited and they are lossy and thus noisy. If one develops the expression giving T_n [7] for the FET, one obtains

$$T_n = T_{\min} + \frac{T_0 gn}{R}\left(R^2 + R_{opt}^2 - 2RR_{opt} + X^2 + X_{opt}^2 - 2XX_{opt}\right)$$

$$T_n = T_{\min} + \frac{gnT_0}{R}\left(R^2 + X^2\right) - 2gnT_0R_{opt} - \frac{2XX_{opt}gnT_0}{R} + gn\left(\frac{X_{opt}^2 + R_{opt}^2}{R}\right)T_0$$

introducing the variables

$$\begin{aligned}
\Omega_1 &= T_{\min} - 2gnT_0R_{opt} \\
\Omega_2 &= gn \\
\Omega_3 &= gn\left(R_{opt}^2 + X_{opt}^2\right) \\
\Omega_4 &= gnX_{opt}
\end{aligned}$$

we can express T_n as

$$T_n = \Omega_1 + \frac{R^2 + X^2}{X}T_0\Omega_2 + \frac{T_0}{R}\Omega_3 - \frac{2X}{R}T_0\Omega_4$$

or

$$T_n = \begin{bmatrix} 1 & \frac{R^2+X^2}{R}T_0 & \frac{T_0}{R} & -\frac{2XT_0}{R} \end{bmatrix} \begin{bmatrix} \Omega_1 \\ \Omega_2 \\ \Omega_3 \\ \Omega_4 \end{bmatrix}$$

In principle, four (non-singular) measurements of the noise temperature will provide us with a linear system of four equations and four unknowns

$$\left[T_n\right] = \left[S\right] \left[\Omega\right]$$

such a system can be solved i.e

$$\left[\Omega\right] = \left[S\right]^{-1} \left[T_n\right]$$

A program in BASIC was written for the HP-85 desktop computer to perform the matrix inversion, to compute $[\Omega]$ and to derive the noise parameters of the FET. This program is listed in Appendix C1.

Theoretically, only four points of measurement are necessary. However, because of experimentals errors both in the measurement of the noise temperature of the FET and in the impedance at which it occurs, one has to compile data and average the results to realize a statistical smoothing of the measured parameters.

In order to find the intermediate parameters Ω_i, one has to determine both the noise temperature of the device for a given impedance and the source impedance. Because of the low gain of the experimental amplifier, one cannot measure directly its equivalent noise temperature without introducing a large error. A receiver (necessarily noisy itself) has to be incorporated in the measurement set-up as shown in Figure III.7. The overall noise temperature of the system is given by the Friis' formula

$$T_{system} = T_{FET} + \frac{T_{receiver}}{G_{FET}}$$

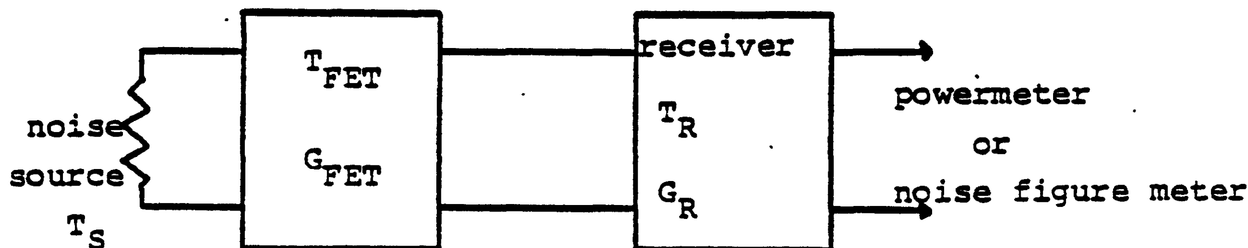


Figure III.7

Noise Figure Measurement Test Set

where G_{FET} is the available power gain of the amplifier. G_{FET} is relatively low and the second stage contribution cannot be ignored. The problem is to evaluate both parameters T_{FET} and G_{FET}. Two methods were used for complimentary reasons. The first one involves only noise temperatures.

Even if the calibration of the receiver noise temperature is provided, one cannot obtain T_{FET} directly without measuring the gain for a particular choice of input and output impedances. The operation is delicate and subject to errors since one has to disconnect the test board from the receiver. On the other hand, if two different receivers are available we have a set of two equations with two unknowns (T_{FET}, G_{FET}) that we are thus able to solve. A single reciever that simulated the operation of two different ones was built. This circumvented the problem of having to disconnect and reconnect the amplifier for an additoinal set of measurements. The Figure III.8 exam-

plifies the technique used.

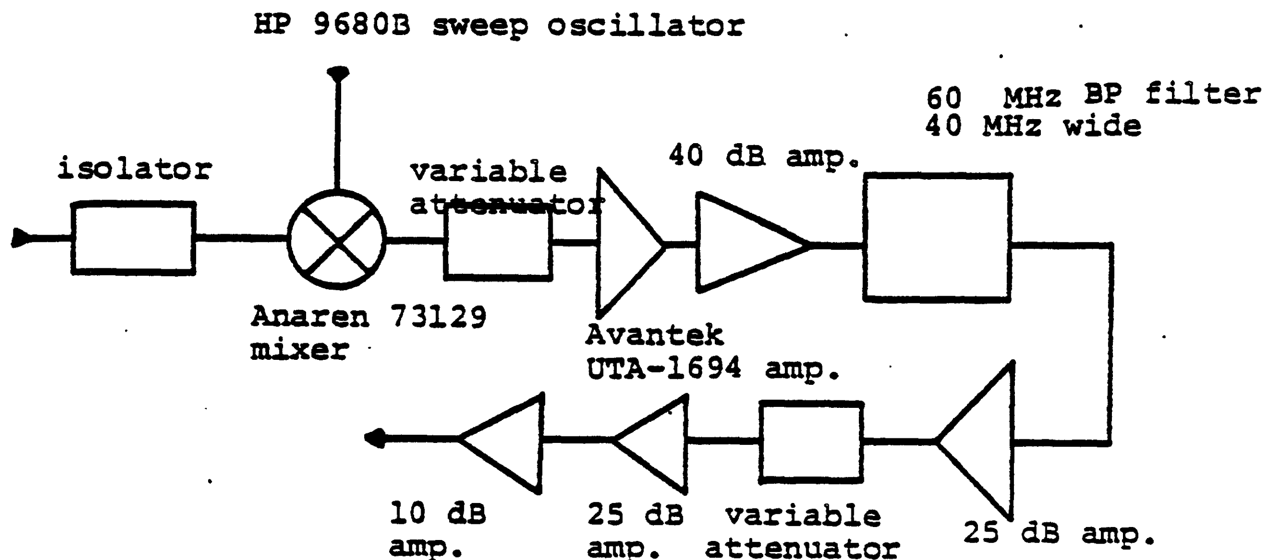


Figure III. 8
60 *MHz Receiver*

The variable attenuator changes the noise temperature of the receiver by adding a series resistance to the circuit, i.e a constant temperature increase. The attenuator was set to achieve 0 or 1 *dB* attenuation in order to minimize the noise temperature of the entire system. In this manner, the measurement errors are minimized especially at low gain levels of the FET. The noise temperature of the receiver was found to vary slightly with time, thus causing calibration problems. However, over a short period of time (2-3 hours) the correlation coefficient between the receiver in position 0 and in position 1 was found to be better than .995. The required measurements were performed with a noise figure meter. Details of the procedure and of the associated software are listed in Appendix C2.

The second method used the output power of the receiver for different noise sources. The noise level at the output power of the receiver is a function of four parameters: T_{FET}, G_{FET}, $T_{receiver}$ and $G_{receiver}$. By using a noise diode which provides two levels of noise and by calibrating the receiver, one obtains a system of four equations. The algebra and the software associated with this method are presented in Appendix C2.

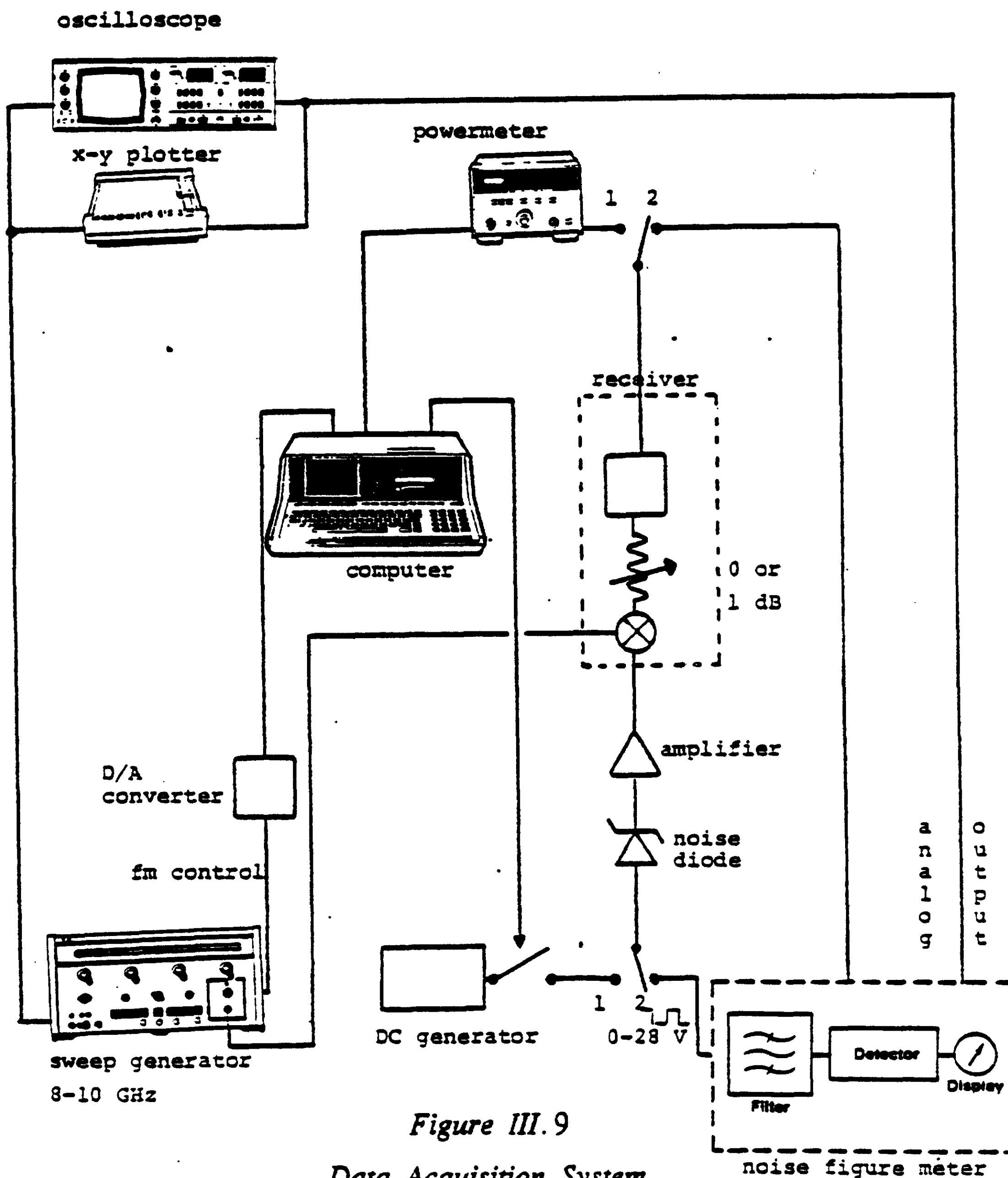


Figure III.9

Data Acquisition System

The two methods were used simultanously for verification purposes as shown in Figure III.9.

At first, it was hoped that the use of microstrip formulae would simulate the source impedance of a given configuration. However, such non quantifiable parameters as the amount of solder on the stub, the length of the pin of a feedthrough capacitance, or more drastically the choice of blocking capacitance were causing variations in the noise and the gain of the amplifier. The input half of the experimental amplifier was replicated in order to measure the source impedance of a given configuration (see Figure III.10).

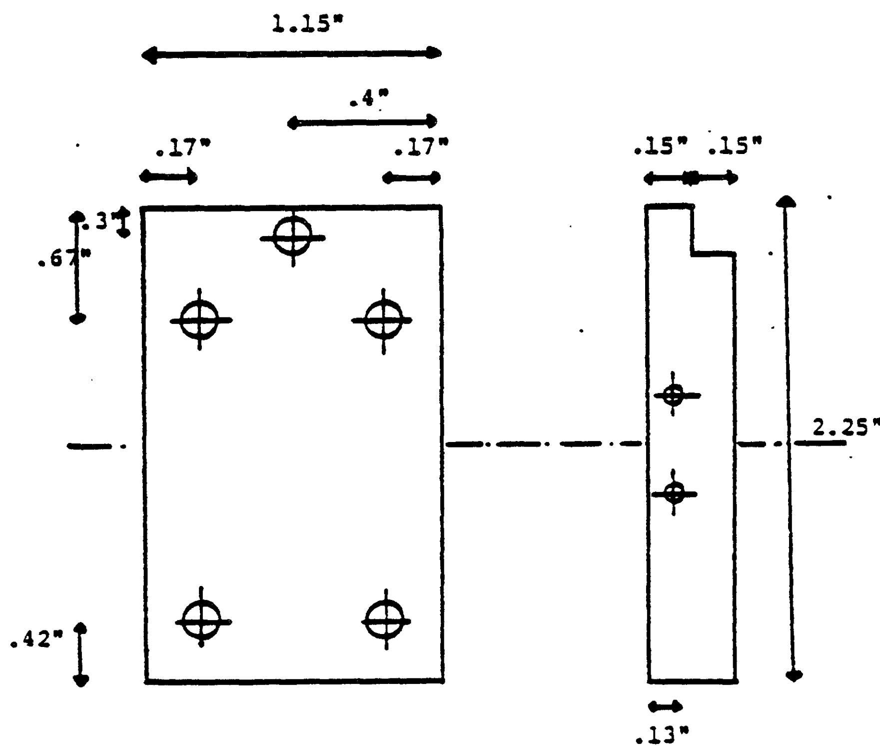


Figure III. 10

Case for the Measurement of Source Impedances

This board was also used to investigate losses due to the matching network, to calculate the noise induced by these losses and to compute the necessary corrections. The

complete derivation of these results is presented in Appendix C3.

Results

All the noise temperatures were measured using the data acquisition system described in Figure III.9. The amplifier used was the second prototype discussed in section IV.4.

To minimize the receiver's contribution to the noise temperature of the system and thus reduce the error* in the determination of the FET noise temperature, the gain of the amplifier (first stage in the Frii's formula) had to be maximized. At first, this was achieved by optimizing the output network of the amplifier. The load impedance presented to the FET was made close to S_{22} conjugate. The output network of the amplifier affects only the amplifier's gain and not its noise parameters.

Six different boards were used at room temperature, as input networks to provide the FET with a large variety of source impedances. Each of them could be easily adjusted depending on the particular frequency the noise parameters are measured at. The Figure III.11 presents some of the board's layouts. When cooled, the substrate boards are subjected to mechanical stresses that tend to bind them. To prevent this, the boards are held tightly against the amplifier case with screws and washers. Despite these precautions, two substrate boards could not be used at cryogenic temperatures.

The receiver's noise temperature is fairly high ($\approx 1000\ K$) and as a result, when the source impedance is mismatched, the system's noise temperature can be relatively important.

A complete study of the measurement errors is presented in Appendix C2.

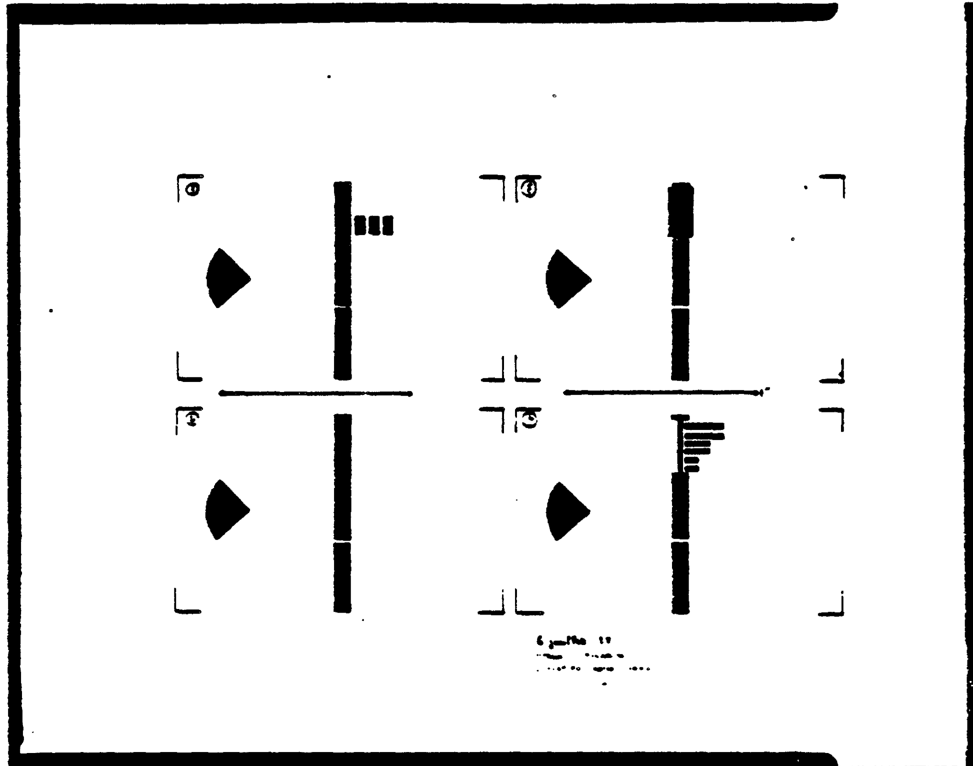


Figure III. 11

Input Boards Layouts

In the computation of the FET noise parameters, the contribution of a particular measurement point is weighted by a factor proportional to its measured noise temperature. Because erors are more important as the noise temperature of the FET increases, points with a FET noise temperature higher than 800 K were disregarded.

Measurements were performed for a drain source voltage of 3 V and a drain current of both 10 mA and 30 mA. The FET noise parameters of both room temperature (293 K) and cryogenic temperature (77 K) were calculated at 100 MHz intervals between 8.1 and 9.6 GHz. the input board yielding the best results at 8.45 GHz, was subjected to more measurements at other bias to study the latter's dependence on the minimum noise temperature. Tables III.2 a and III.2 b present the noise parameters at 8.45 GHz. (All the impedances are referenced to the source edge of the FET pack-

age)

Frequency 8.45 *GHz*			
NEC 13783	Bias 10 *mA* , 3 *V*		Errors
T (*K*)	293	77	±1
T_{min} (*K*)	126	42	±7
R_{opt} (Ω)	37.2	17.6	±2.5
X_{opt} (Ω)	5.0	-.2	±2.5
gn (*mmhos*)	15.7	7.8	±3.6

Table III.2 a

NEC 13783 *Noise Parameters* I_d=10 *mA*, V_{DS}=3 *V*

Frequency 8.45 *GHz*			
NEC 13783	Bias 30 *mA* , 3 *V*		Errors
T (*K*)	293	77	±1
T_{min} (*K*)	150	47	±7
R_{opt} (Ω)	45.9	22.3	±2.5
X_{opt} (Ω)	-3.3	-.7	±2.5
gn (*mmhos*)	21.0	10.7	±3.6

Table III.2 b

NEC 13783 *Noise Parameters* I_d=30 *mA*, V_{DS}=3 *V*

Figures III.12a and III.2b present the variations of the minimum noise temperature with respect to frequency and temperature. As seen, the cooling to 77 *K* dramatically improves the performance of the FET.

A power law fit for the noise temperature of the FET of the form

$$T_{NOISE} = \alpha T^{\beta} f^{\gamma}$$

produces the following results: For a bias of 10 *mA* β=.80, γ=1.58 and for a bias of 30 *mA* β=.86 and γ=1.66.

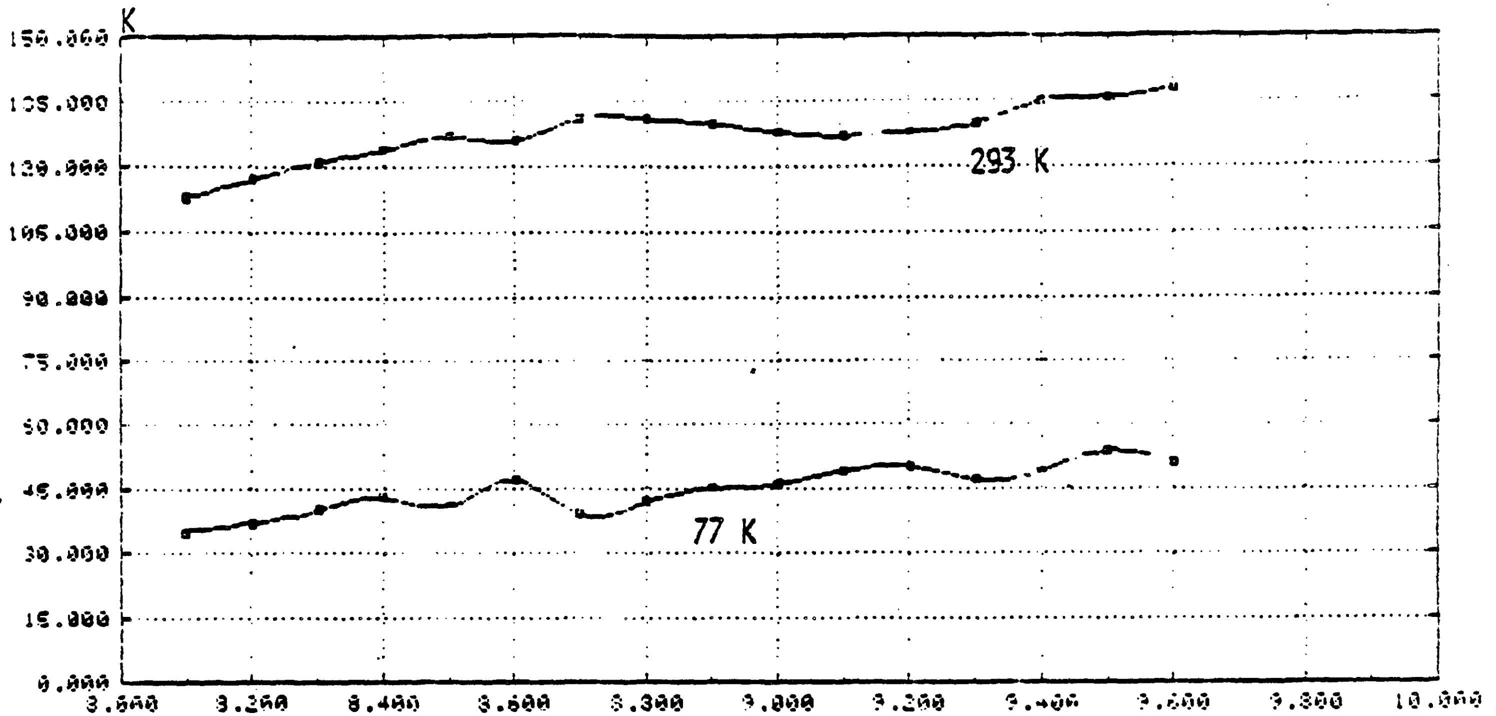


Figure III. 12 *a*

NEC 13783 *Minimum Noise Temperature* $I_d = 10\ mA$, $V_{DS} = 3\ V$

Although the value of the minimum noise temperature is dependent on the FET DC bias, its variations with frequency and temperature are found to be (given the imprecisions in the results) independent of the bias. The temperature dependence of $T_{\min}$ is comparable with published works performed at other frequencies and for other FET's [8,9,10]. The theoretical expression presented in the section II.6 expresses the minimum noise figure as

$$F = 1 + b\frac{f}{f_T} + c\left(\frac{f}{f_T}\right)^2$$

The minimum noise temperature then varies as

$$T_{\min} = \bar{b}\frac{f}{f_T} + \bar{c}\left(\frac{f}{f_T}\right)^2$$

As stated before f_T is very large and in the 8 to 10 GHz band one can approximate

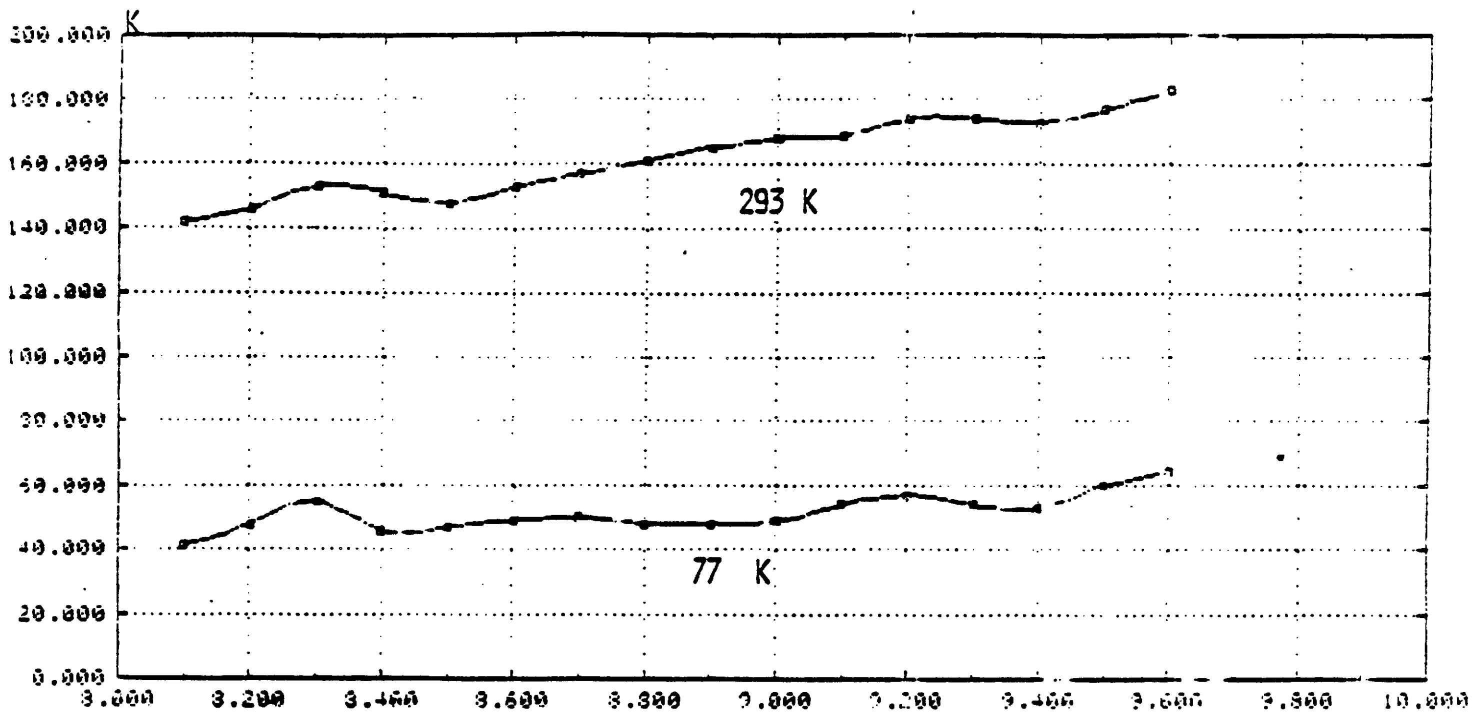


Figure III.12 b

NEC 13783 *Minimum Noise Temperature* $I_d = 30\ mA$, $V_{DS} = 3\ V$

T_{min} by $\bar{b}f/f_T$. This yields a theoretical factor γ equal to 1. The experimental value of γ predicts a higher noise temperature for high frequencies than that of Pucel's model. A fit disregarding measurements performed over 9.2 *GHz* provides a value γ equal to 1.17 for 10 *mA* (1.16 for 30 *mA*). That is, with the exception of frequencies greater than 9.3 *GHz* (because of measurement errors), the experiment confirms the variations of the minimum noise temperature (and therefore of the minimum noise figure) in accordance with Pucel's theory.

The value of the minimum noise temperature T_{min} was found to be larger that the value predicted by Sierra [11] for the NEC 13783*. From the 15 *GHz* chip noise

* Comparison of high frequency noise parameters has to be performed carefully. This is true since the mount and surrounding of the transistor affects the noise temperature of the device by reactive feedback.

parameters measurements, Sierra computed the noise parameters at various frequencies assuming the frequency variation of the Pucel et al. theory. At 8.45 GHz, he predicts a noise temperature $\bar{T}_{min}$ of about 110 K. The measurements provide T_{min} equal 126 K (14% higher). The other calculations performed by Sierra are for a physical temperature of 15 K. No measurements at this temperature were performed in this study.

The Figures III.13a and b present the variations of the optimum noise impedance at room temperature and at 77 K for bias of 10 mA and 30 mA. In both cases the real part of the optimal noise impedance decreases notably when the amplifier is cooled. From these plots one can conclude that if the input network of an amplifier realizes the optimum noise temperature impedance at room temperature, it will not achieve it once the amplifier is cooled. The tuning at cryogenic temperature will require a lowest real part for the source impedance, meaning the use of lower impedance transmission lines than at room temperature. The optimum noise impedance depends on the bias of the FET but its variations in the reflexion plane remain small as the drain current varies from 10 to 30 mA.

The variations of the noise conductance gn with frequency and temperature are shown in Figure III.14a for a DC bias of 10 mA and III.14b for a bias of 30 mA.

The measurements at room temperature are particularly noisy for the lowest drain current bias. As stated before, in order to reduce the number of high noise temperature measurement points, several input boards had to be used to cover the whole 8.1-9.6 GHz band. This results in discontinuities for the computed noise parameters. Among these, the noise conductance gn is the most sensible to measurement errors. At 8.45 GHz and room temperature, the measured gn is 16 ± 4 mmhos which agrees

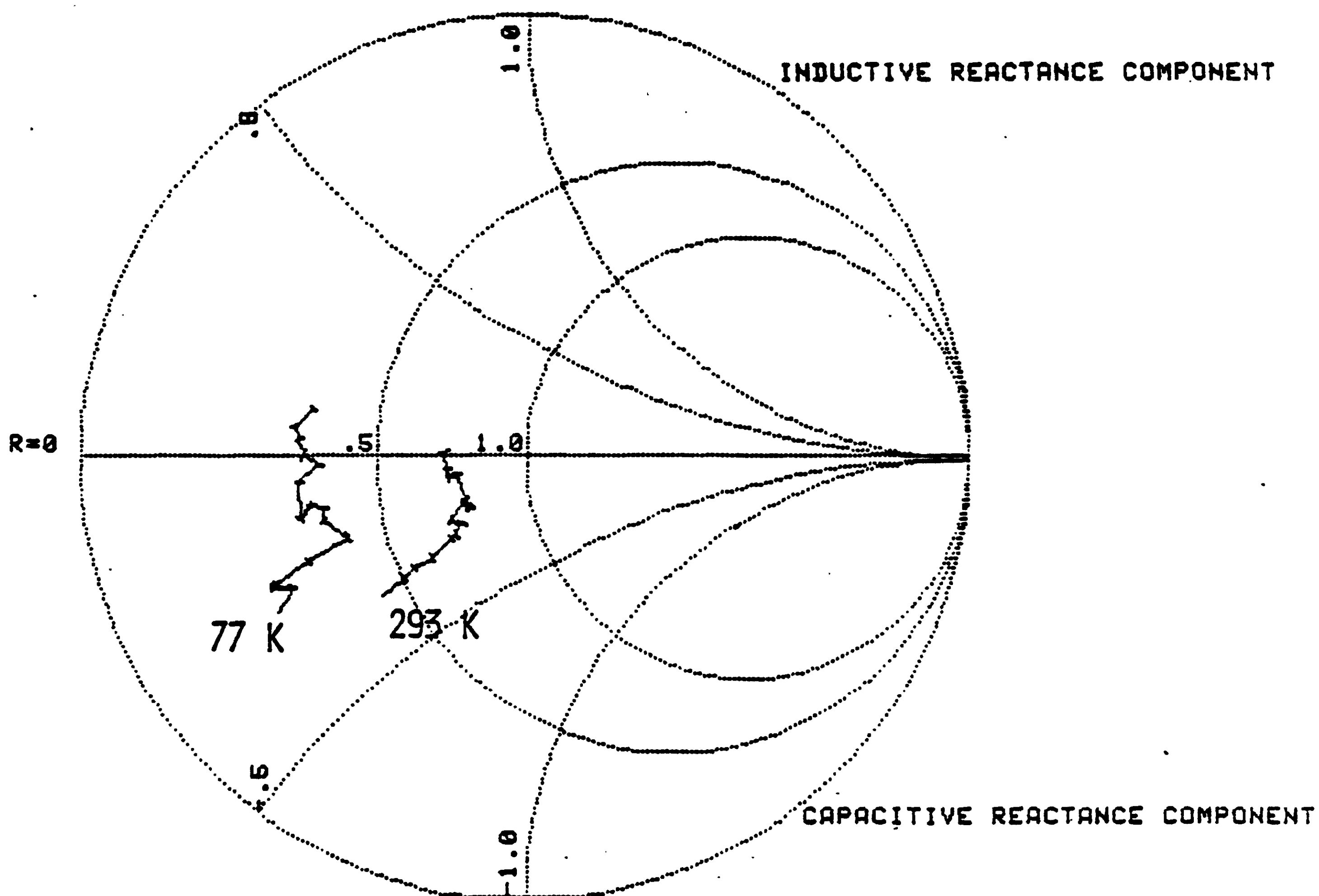


Figure III. 13 *a*

NEC 13783 *Optimum noise Impedance*, $V_{DS}=3\ V,\ I_d=10\ mA$

with the 12.5 mmhos value predicted by Sierra.

A power law fit of the form

$$gn=\alpha T^{\beta} f^{\gamma}$$

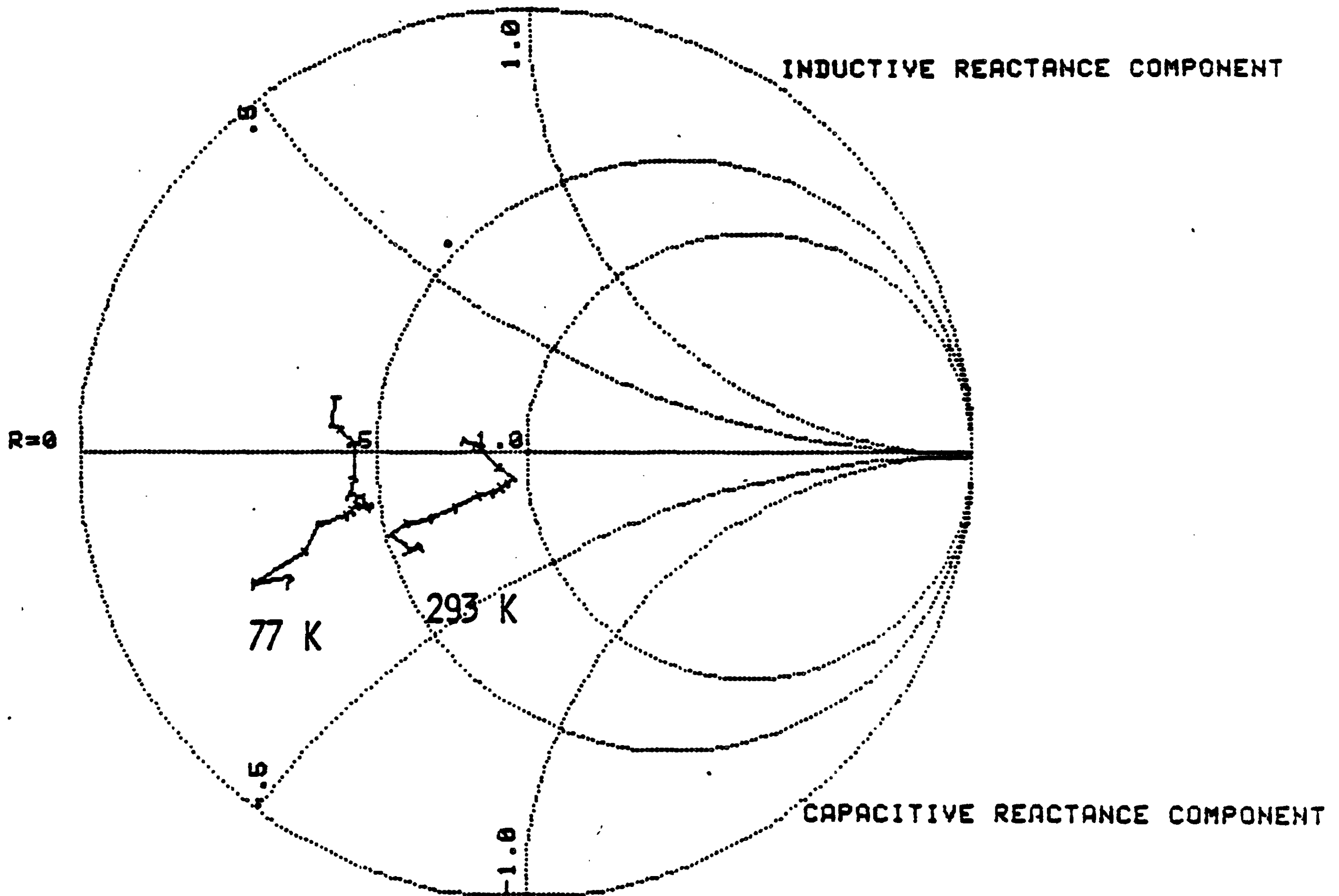


Figure III. 13 *b*

NEC 13783 *Optimum noise Impedance*, $V_{DS}=3\ V$, $I_d=30\ mA$

provides the following results: For a bias of 10 *mA* $\beta=.43$, $\gamma=2.17$ and for a bias of 30 *mA* $\beta=.44$ and $\gamma=2.26$. As for the minimum noise temperature, the variations of *gn* do not depend on the value of the DC bias of the FET. Theoretically, *gn* increases as

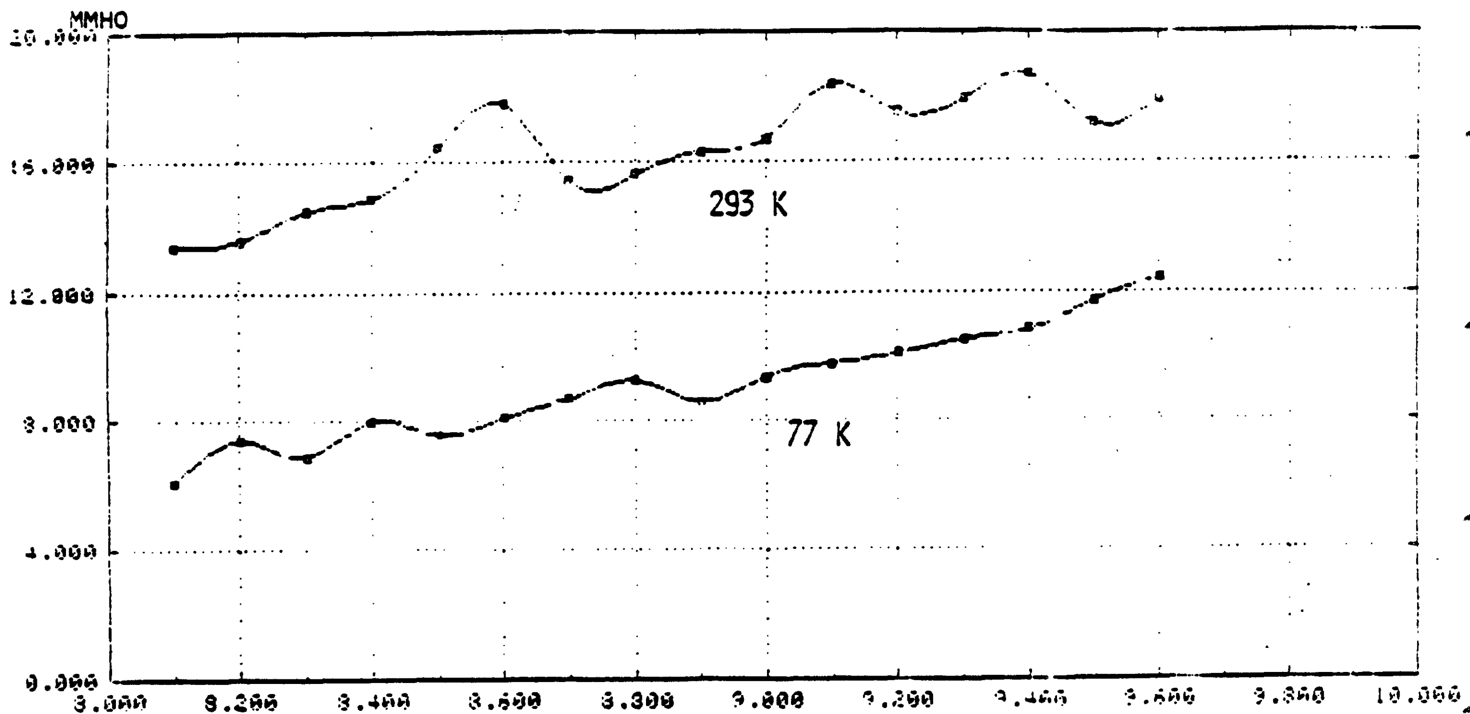


Figure III. 14 *a*

NEC 13783 *Noise Conductance*, $V_{DS}=3\ V,\ I_d=10\ mA$

the square of the operating frequency. Given the measurement imprecisions, the experiment confirms the theory of Pucel et al.s'. Between 77 and 293 K the experimental temperature dependence of gn is comparable to that found in previous work [10].

A more complete investigation of the dependence of T_{min} on the DC bias is presented in Figure III.15. The variations of the minimum noise temperature versus the drain current are plotted for both room and cryogenic temperature. In terms of minimizing T_{min}, there is an optimal current whose value depends on the physical temperature: 15 mA at 77 K, 17 mA at 300 K.

In conclusion, one can state that the measured noise parameters confirm all the features of the Pucel's theory. A more complete study of the temperature dependence

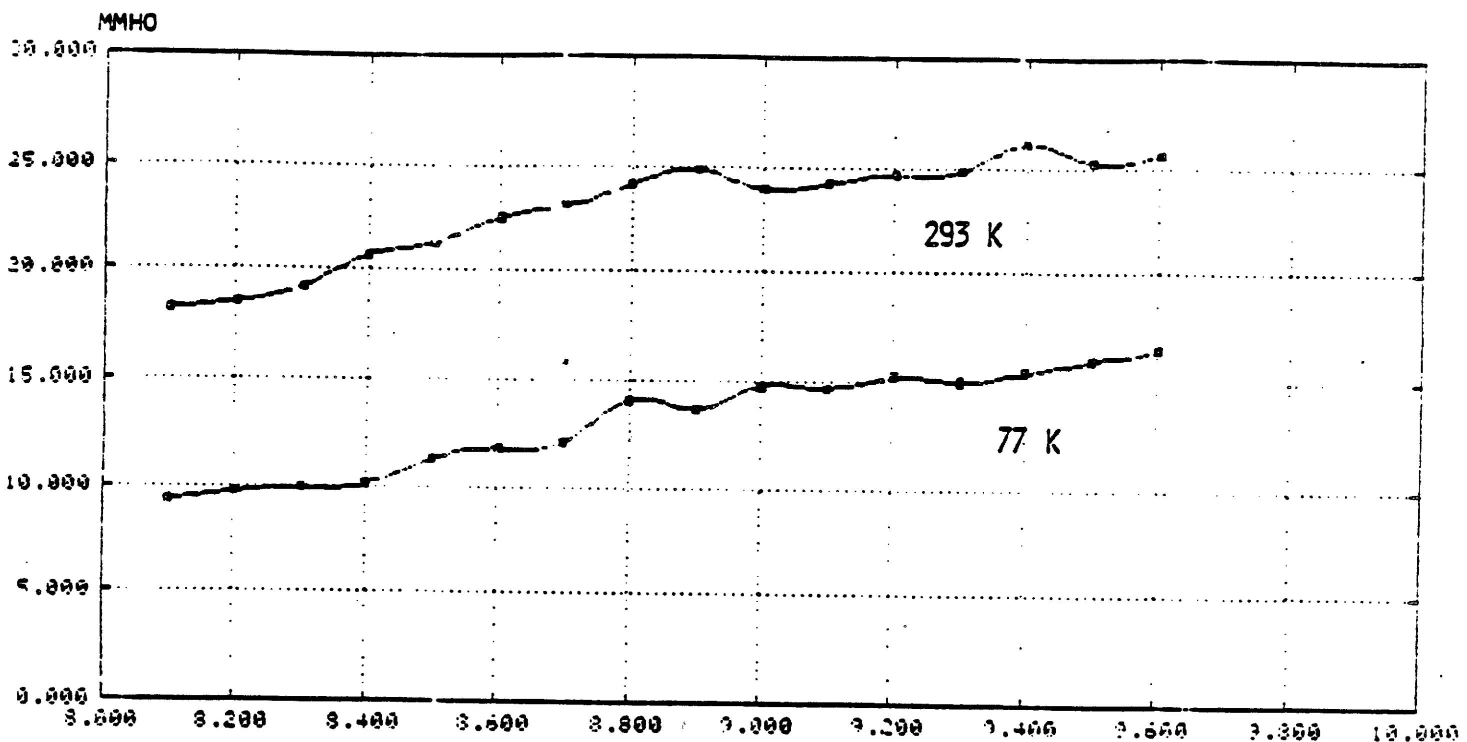


Figure III. 14 *b*

NEC 13783 *Noise Conductance*, $V_{DS}=3\ V$, $I_d=30\ mA$

of these three parameters should be undertaken (measurements at 4 and 20 K) to determine bounds on their variations with temperature.

4. DC characteristics and internal parameters

FET's DC characteristics can be analyzed to determine internal parameters of the FET such as transconductance, channel thickness, carrier doping density or saturation velocity. Combined with measurements at low frequencies and measurements of scattering parameters, it is possible to evaluate the values of the elements of the FET small signal model which enter directly in the noise equation.

Figures III.16 a and b present the classic FET characteristics at 293 K and 77 K. The variation of the drain current is plotted versus the drain source voltage, for .2 V

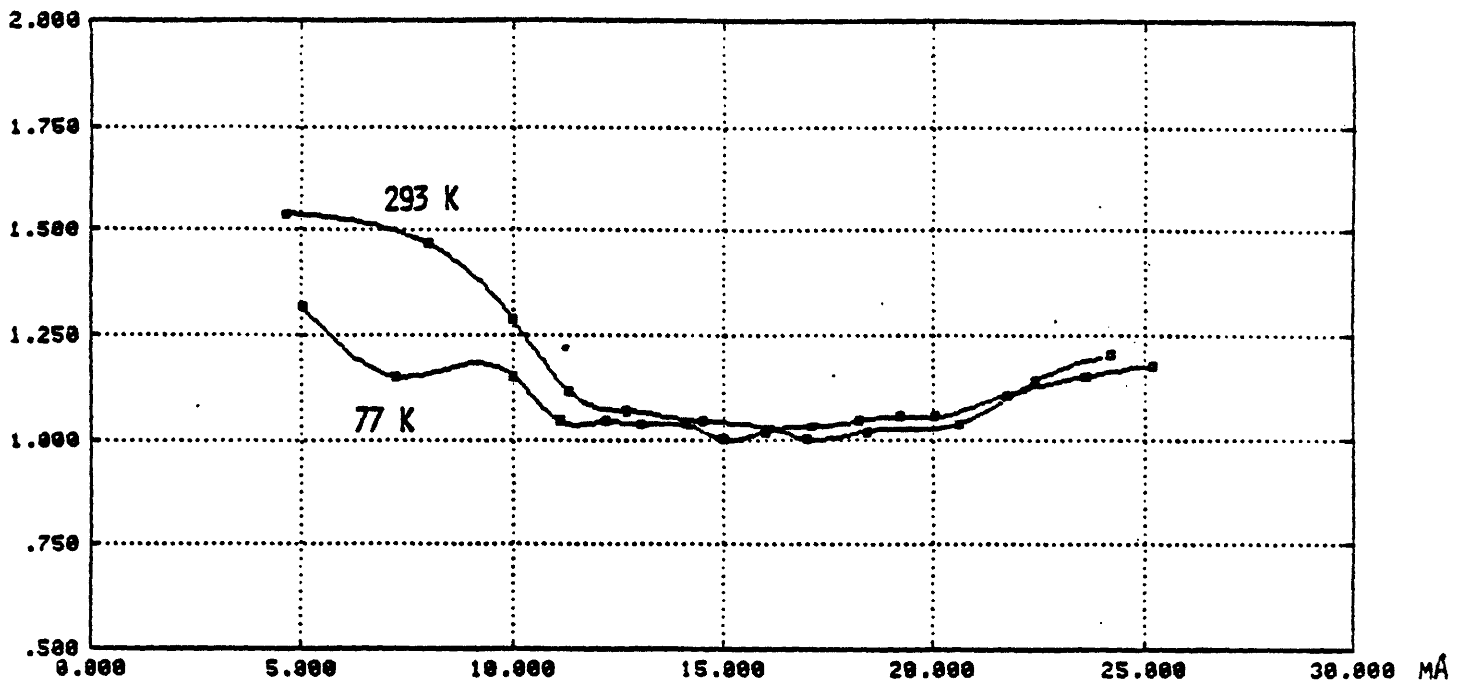


Figure III. 15

Noise Temperature versus Drain Current

steps of gate voltage. The top curve in each plot is at 0 V gate source voltage. Cooling severely affects the transconductance and the saturation current.

The gate current as a function of the forward gate voltage was measured to provide the Schottky barrier potential V_B. Using the methods developed by Fukui [12] the FET pinch-off voltage V_p (defined as the gate voltage for which the saturated region occupies the whole channel) was measured. The channel width Z and the gate length L were taken from the manufacturer's [3] published data (respectively 270 μm and .5 μm). The calculated* values of the carrier density N, channel thickness a and open channel saturation current I_s are tabulated in table III.3. The carrier density shows little variation with temperature. The measured change of thickness a is most

* All the formulae used for this derivation were taken from Fukui's paper [12].

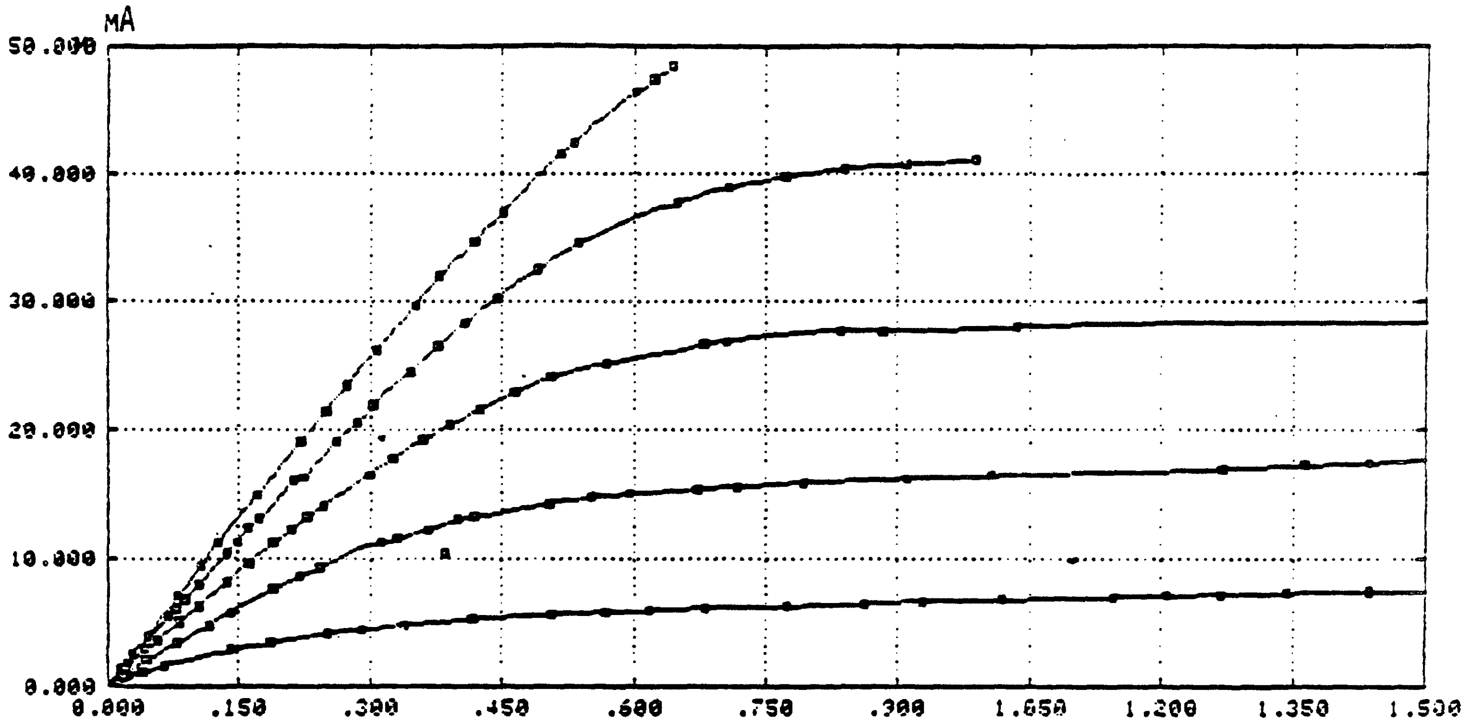


Figure III.16 a

NEC 13783 DC Characteristics at Room Temperature

probably due to measurement imprecisions on the Schottky barrier potential V_B and not to a physical shrinking of the channel. The increase of I_s confirms the already observed increase of the FET transconductance *gm* and of the FET RF gain at cryogenic temperatures.

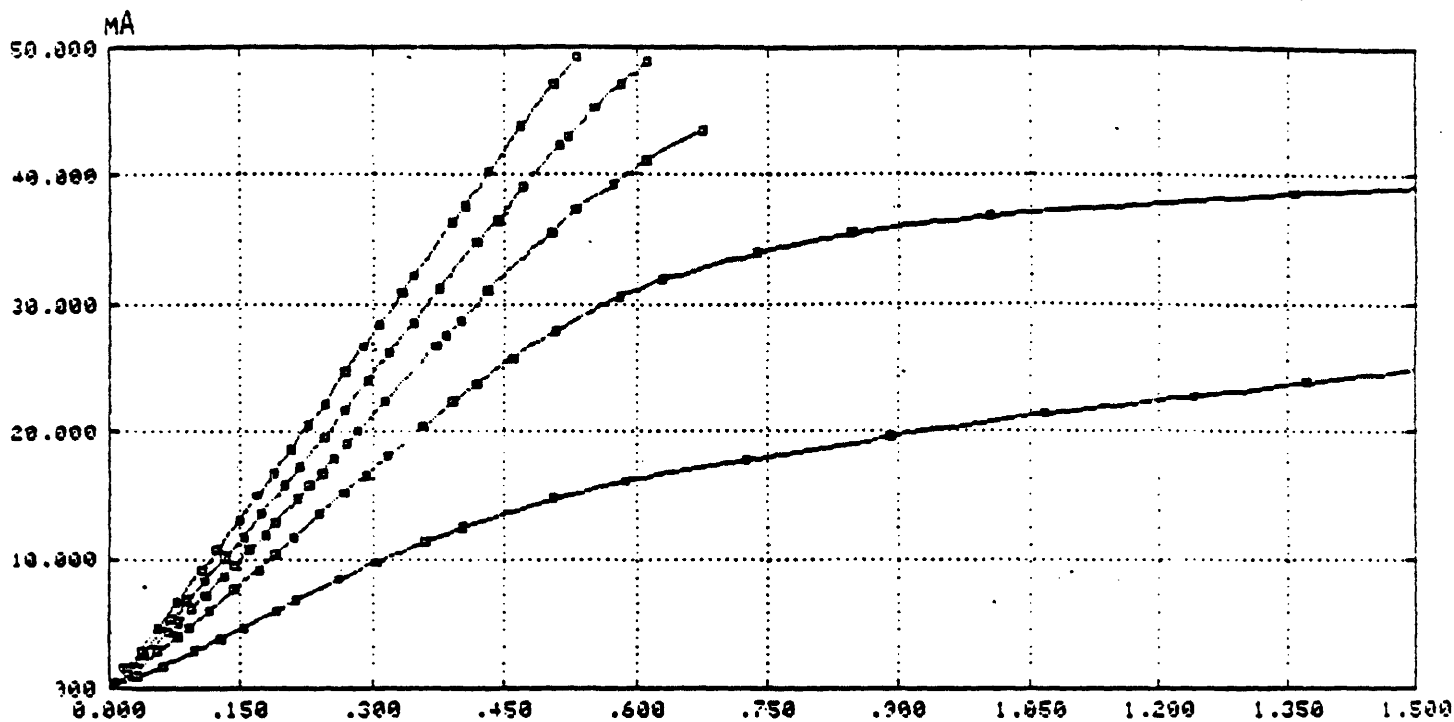


Figure III.16 b

NEC 13783 *DC Characteristics at Cryogenic Temperature*

NEC 13783 Internal Parameters		
T (K)	293	77
L (μm)	.5	.5
Z (mm)	.272	.272
N $(10^{16} cm^{-3})$	22.2	23.4
a (μm)	.11	.095
I_s (mA)	149	185
V_p (V)	1.15	1.272
V_B (V)	.793	.794

*Table III.*3

NEC 13783 *Internal Parameters*

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CHAPTER IV: FET SINGLE STAGE AMPLIFIER

1. Purpose

There are several goals in designing and constructing the FET single stage amplifier. First, the amplifier is purposely experimental in nature so that it can be easily modified. Also, since several FET's are to be used, the replacement of one FET by another should not disturb the overall characterizations of the prototype.

One objective of this research was to determine various parameters describing the microwave behavior of GaAs FET's. As explained in chapter III, this required the measurement of the characteristics of input and output networks. Thus, these networks had to be easily removable.

Finally, the amplifier had to be used at cryogenic temperatures, thus destructive stress that can develop at these temperatures was a concern. This is due to different contraction coefficients of the various components which constitute the amplifier.

2. Design

Minimizing the noise temperature of the amplifier or maximizing the gain requires the production of the optimum source and load impedances at the input and output of the FET. These values are, a priori, unknown and therefore matching networks have the capacity to produce a wide range of impedances.

At 8.45 GHz, the use of lumped elements is intricate because any piece of straight wire presents a very large reactive component. For instance, a wire with a diameter of 2 *mils* placed at 50 *mils* from a ground plane presents a reactance of 50 Ω/mm. This exemplifies the difficulties in using inductances.

The solution adopted used microstrip transmission lines. Microstrip line presents both advantages and disadvantages. On the positive side, it is relatively inexpensive and simple to use. Also, ultra-violet processing allows the design of any shape of circuit, any value of impedance. However, when cooled, boards usually shrink (1 % at 20 K), thus causing stress problems. In addition, for frequencies as high as 8 GHz, radiation losses can be fairly high. Use of a substrate board with a high dielectric constant (constraining electric and magnetic fields within the substrate) minimizes these losses. But, a high dielectric constant board slows down the EM wave, thereby reducing its wavelength. Thus, any obstacle present on the board (DC blocking capacitor, solder, FET) pertubes the propagation characteristics.

A compromise between the two defects is reached with a duroid teflon fiber glass board whose substrate has a dielectric constant of 2.2 [1]. This substrate has a thickness of 31 *mils* (.78 mm). The copper strip has a thickness of 1.34 *mils* (34 μm). Yet, another slight inconvenience in using a microstrip board is that it requires near

perfect grounding of the board to the case of the amplifier. This is done to avoid parasitic oscillations.

Extensive research has been undertaken on microstrip methods and various papers have been published on the subject [2,3]. To calculate the microstrip line width for the main 50 Ω line and other matching networks, quasi TEM approximation formulas developed by Wheeler [2] were used. These formulas provide characteristic impedance and phase velocity within 2 to 5 % of the measured value depending on the values of the characteristic impedance. A 5 % error gives a VSWR of 1.1, a value comparable to the VSWR of typical connectors.

Different tuning and matching techniques were tried for input and output networks. The use of a piece of dielectric moved across a microstrip discontinuity was immediately rejected because of its lack of repeatability. The use of a movable ground plane as suggested by Weinreb was eliminated since it did not allow easy measurements of the impedances associated with a particular circuit. The best solution employed stubs soldered to the main line as tuning elements. Once a particular structure is adopted, a careful mapping of the structure is made and a mask is generated for a later version.

The stubs are realized by cutting a 2 *mils* (50 μm) thick sheet of gold to the desired dimensions. Because the thickness of the gold sheet is not 1.34 *mils*, as the stub generated from the mask, and because the stub cannot be held perfectly against the substrate board, its dimensions have to be chosen cautiously. Using Wheeler's formulas, it is possible to study the amount of error produced by a slight gap between the substrate and the gold sheet stub. Figure IV.1 presents the plot of $\Delta Z/Z_c$, where Z_c is the characteristic impedance of the stub, ΔZ the difference in characteristic impedance

between the mask generated stub and the gold sheet stub as a function of Z_c the characteristic impedance of the stub.

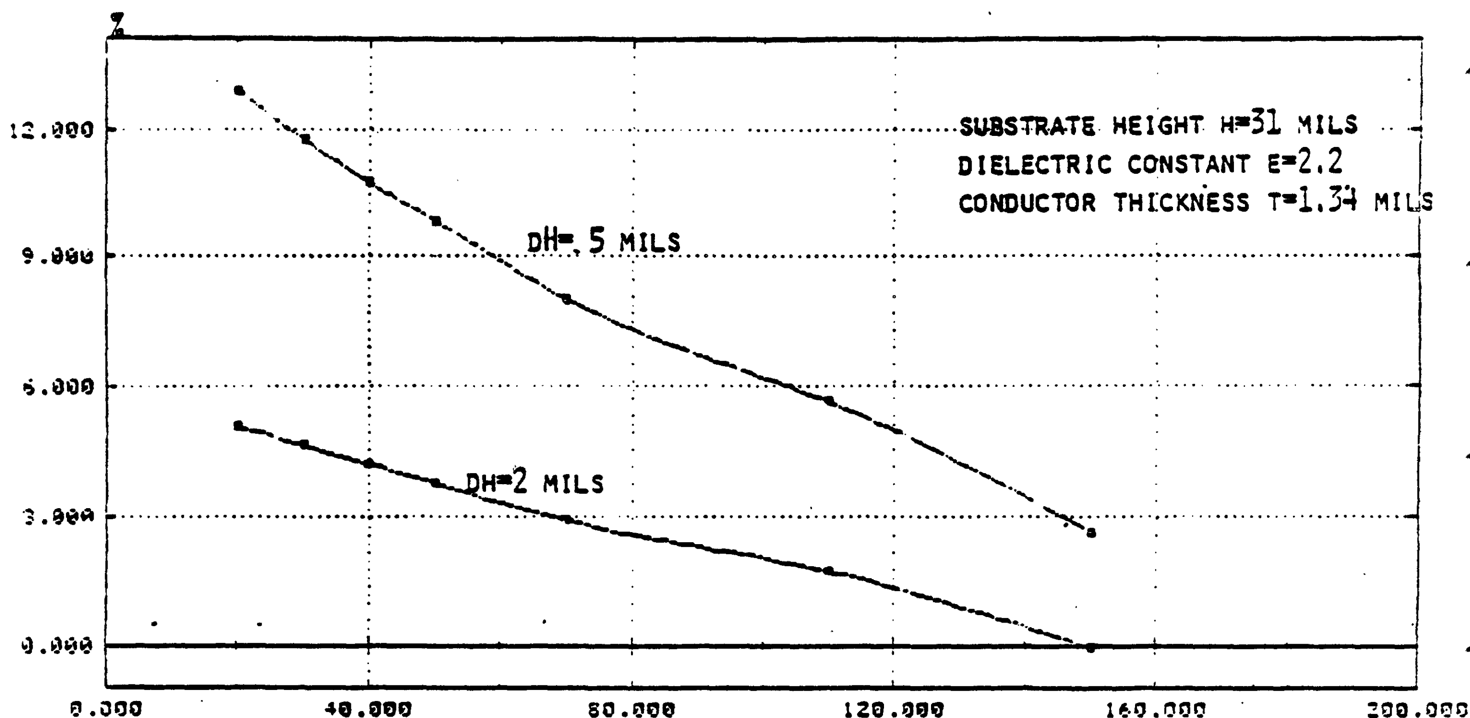


Figure IV.1

Effect of Gap between Stub and Substrate Board on the Characteristic Impedance of the Stub

It is obvious from these plots that high impedance stubs should be used. To hold the stubs firmly against the substrate, a thin tape of teflon (ϵ_r =2.2) is used. In order to study how this affects the impedance added in parallel to the main line, the transmission coefficients of a 50 Ω line, with and without a piece of teflon tape, were measured using a network analyzer. A piece of tape 4 *mm* wide changes the magnitude of the transmission coefficient by less than the network analyzer resolution ($<.05$ dB). It

produces a phase shift of 5 degrees at 8.5 *GHz*. As can be seen, the teflon tape only slightly affects the propagation of EM waves over the particular microstrip structure and therefore does not alter the ability to reproduce a given circuit.

SMA connectors were used for input and output. In order to remove thermal stress on the connector pin, when cooled at cryogenic temperatures, a flexible connection, constructed with a gold strip was placed between the microstrip and the connector's pin. To avoid creating a gap between this connection and the board stripline, and later parasitic oscillations, a teflon cylinder pressed the gold strip against the substrate metallization. Figure IV.2 illustrates how this was accomplished.

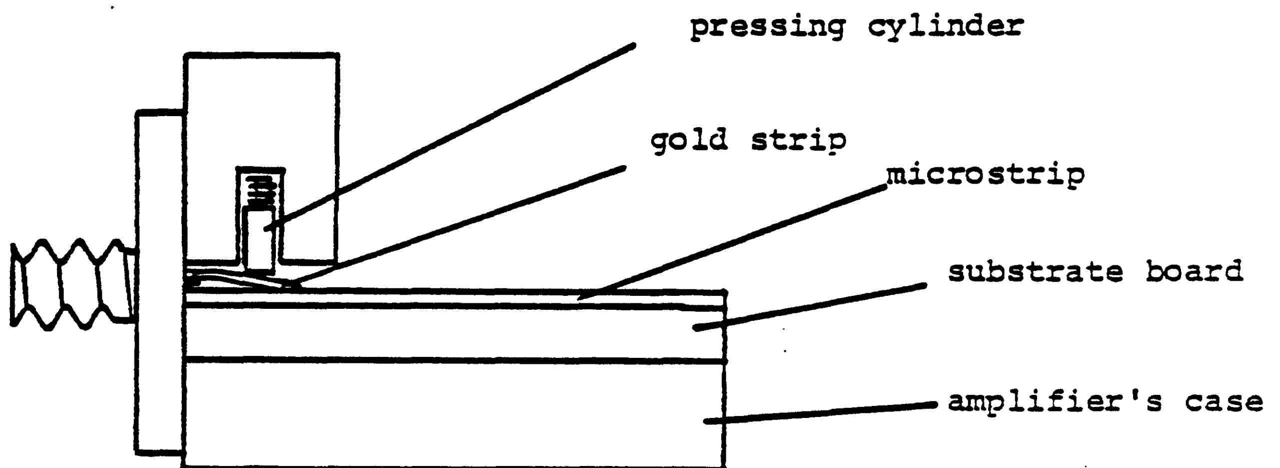


Figure IV.2
Mounting Details for Connectors

Two regular laboratory power supplies provided the FET bias. In order to protect the transistor against transients and overvoltage, a zener diode in parallel with a capaci-

tor were placed between the source and gate and between the source and drain. DC bias was applied to the FET with 100 pF feedthrough capacitors inserted through the case of the amplifier. 1 mil gold wires connected the feedthroughs to triangular resonators placed at $\lambda/4$ from the microstrip as shown in Figure IV.3 (all the wavelengths λ are referred to 8.45 GHz).

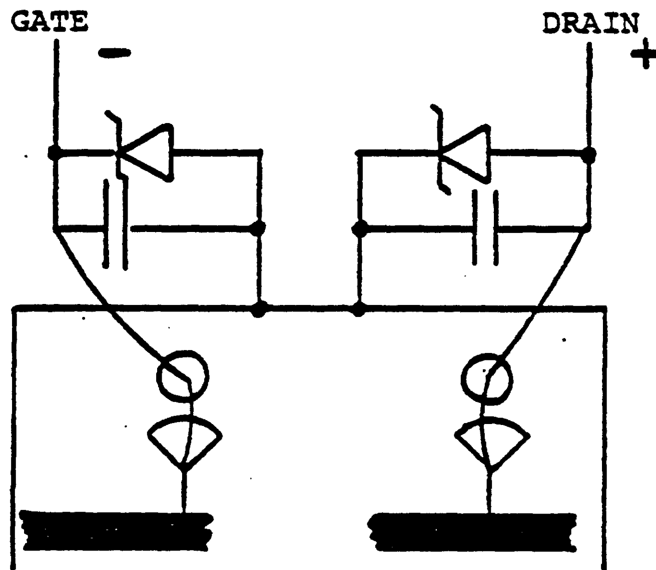


Figure IV.3
DC Bias Network

At 8.45 GHz the vertex of the triangle is a short circuit, and therefore $\lambda/4$ away the microstrip is an open circuit.

At other frequencies, the bias network perturbes the propagation along the microstrip. However, in the frequency range of interest (8-10 GHz) it does not cause any serious perturbations. It should be noted that resonance modes of the triangular shaped resonators [4] were not considered.

The FET's were used in a package form. The transistor package presents substantial parasitic reactances [5] and degrades gain and noise performances, however they are more practical to use. That is, they are less susceptible to mishandling and generally more stable than chips. The FET's were operated in a common source configuration. The two source pads of the FET had to be carefully grounded to the case of the amplifier to avoid creating any parasitic inductance which would degrade the gain of the amplifier and the overall noise temperature. For this reason, the FET source pads were soldered to two 31 *mils* high ridges as described in Figure IV.4.

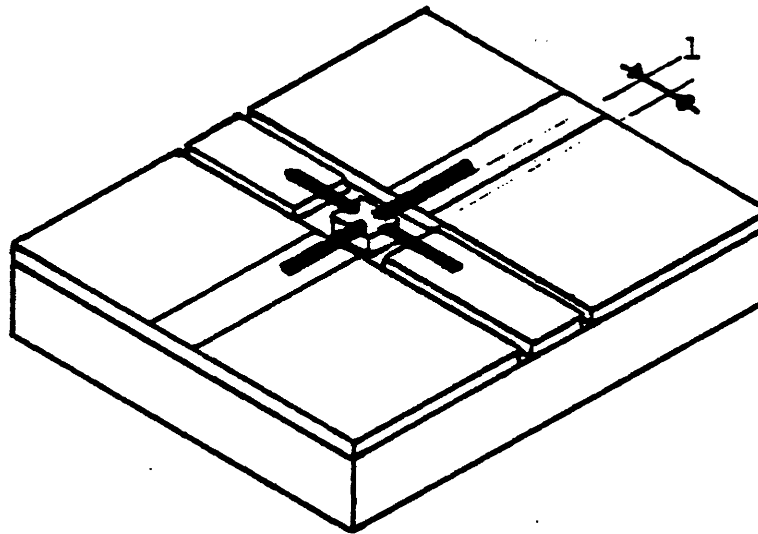


Figure IV. 4
Transistor Mounting Details

Consider a simplified model of the FET, neglecting the feedback capacitance C_{gd}, then an inductance L placed between source and ground will result in an effective conductance gm'

$$gm' = \frac{gm}{1 + jLgm2\pi f}$$

where gm is the FET conductance and f the frequency. Applying Wheeler's design formula to the source pad yields $L = 350\ nHm^{-1}$. Taking the low frequency conductance specified by the manufacturer (typically 50 $mmho$), gives a 8.45 GHz correction term of $1 + .929jl$ where l is the gap presented in Figure IV.4 expressed in mm. A gap of .5 mm causes a diminution of the effective conductance of approximately .45 dB. This corresponds to a gain diminution of .9 dB since S_{21} is proportional to gm. The actual effect of this created inductance is less than the calculated value, but nevertheless remains quite important.

The FET post can greatly perturbe the characteristics of the amplifier. For the same reasons as for the source pads, the drain and gate pins were made as short as possible.

3. First prototype

The first single stage prototype is shown in Figure IV.5. The amplifier case was constructed in brass. The substrate boards were soldered to the case using low temperature indium solder to assure good grounding. The FET was an ALPHA 3003 for which the manufacturer claims a minimum noise temperature of 120 K at 8 GHz. The two ridges necessary to ground the FET's source pads were constructed from copper, whose low thermal resistivity dissipates the heat generated by the FET at cryogenic temperatures. The two copper bars were soldered to the case with regular 60% lead 40% tin solder and to the source pads with indium. The difference between the melting points of the two solders made possible the removal of input and output boards as

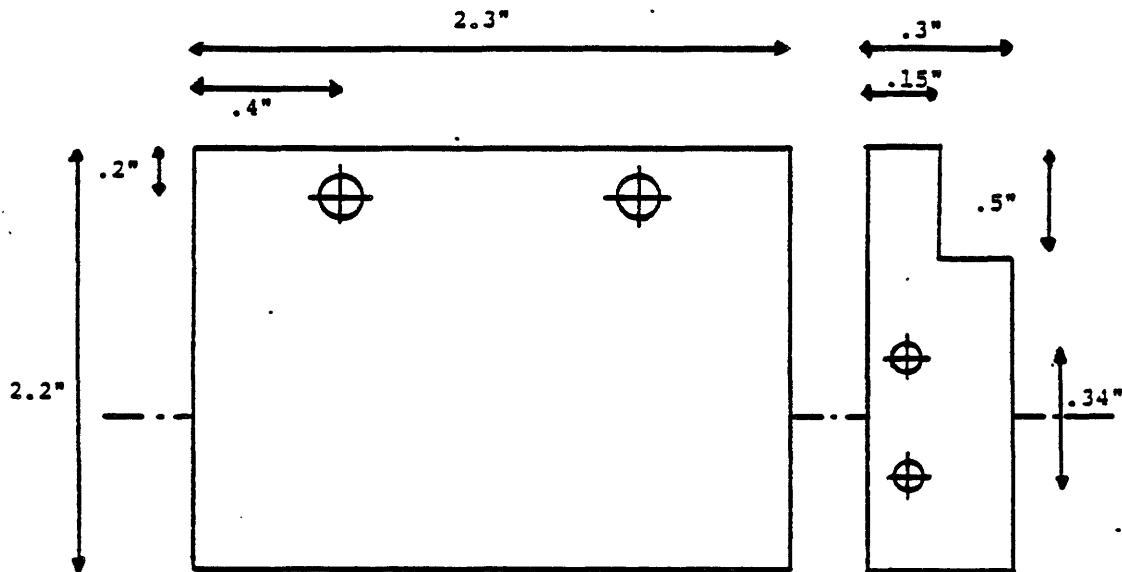


Figure IV.5

Single Stage First Prototype

well as the FET from the amplifier, all without removing the ridges.

The bypass blocking capacitors, necessary to avoid the shortening of the gate and drain when the amplifier is connected to the sweep oscillator, were 18 pF UTC microstrip chip capacitors. The capacitors were found to be lossy, typically .3 dB at 8.5 GHz. Neglecting the other losses induced by the input board, this corresponds to a 20 degree increase in the amplifier equivalent noise temperature at room temperature (8 degrees at 77 K). Higher nominals values of capacitors were found to be lossier and thus were rejected.

This amplifier was optimized at room temperature to provide the best noise temperature at 8.5 GHz. Figure IV.7 presents the gain of the optimized first prototype and Figure IV.8 presents the noise temperature.

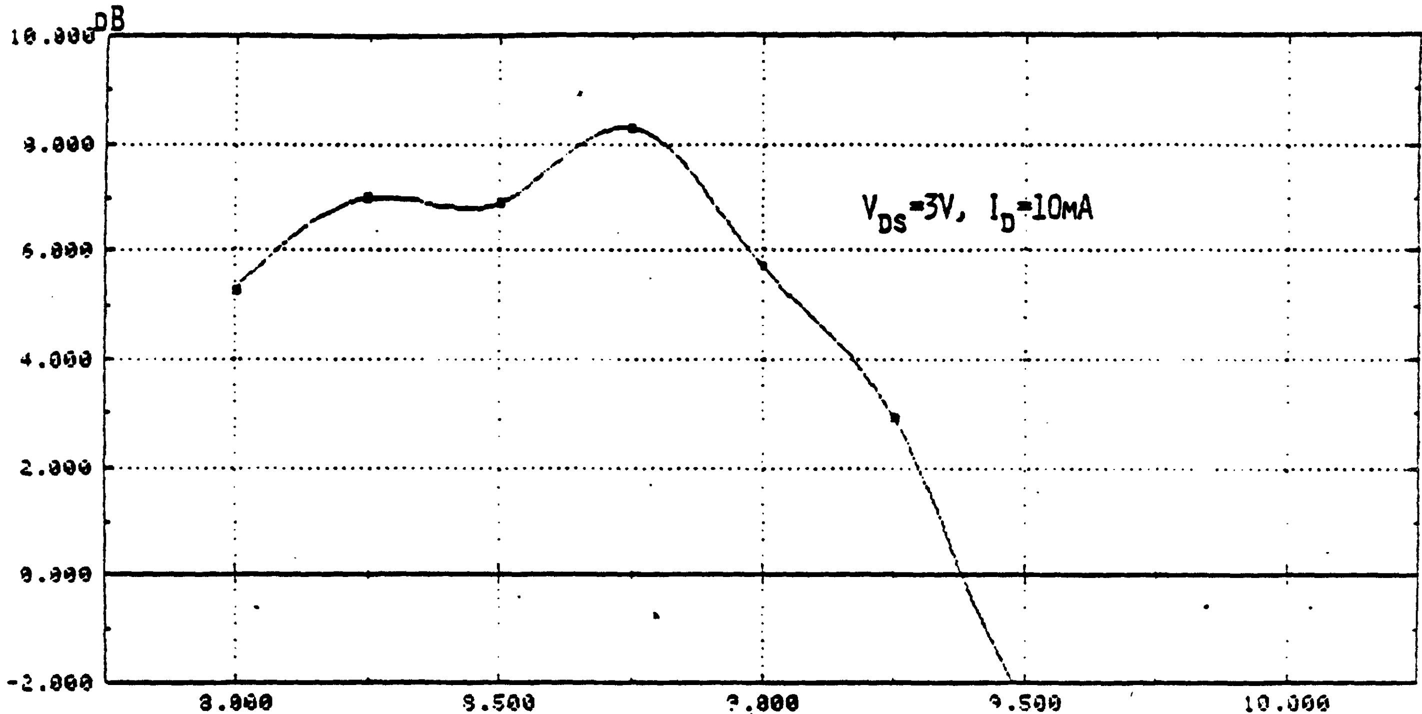


Figure IV.7

Single Stage Amplifier Gain

The amplifier exhibits a maximum gain of 8.35 dB at 8.75 GHz and a minimum noise temperature of 160 K at 8.5 GHz. The 3 dB gain bandwidth Δf_G is value at 8.75 GHz. The quality factor Q_G associated with it is 10.4, thus the Bandwidth to Central Frequency Ratio (BCFR) of 9.6 %. One can define the 1 dB noise bandwidth as the bandwidth where the noise figure is 1 dB higher than the minimum noise figure. In the case of the first prototype, the bandwidth Δf_N is 1.02 GHz wide which corresponds to a Q_N equal to 8.1 and a BCFR of 12 %.

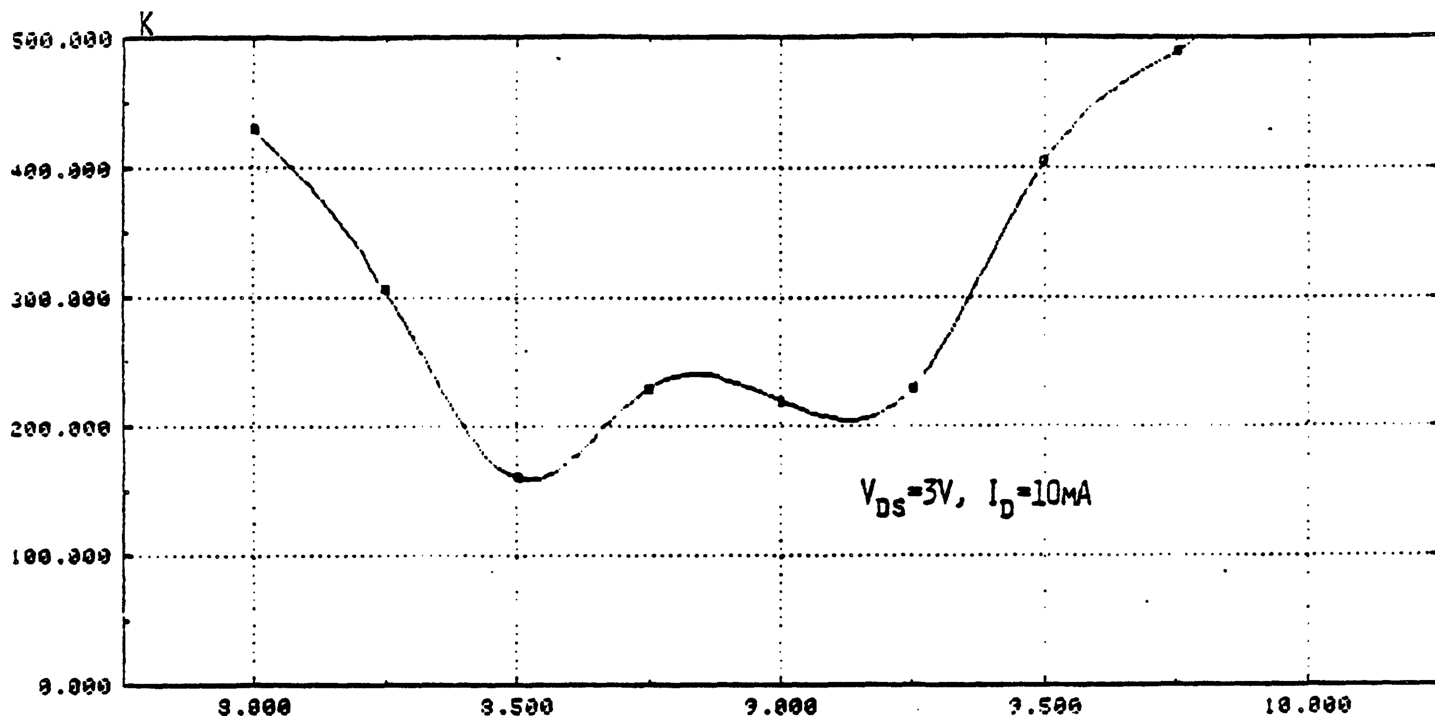


Figure IV.8

Single Stage Amplifier Noise Temperature

The cooling of the amplifier to 77 *K* was performed by bolting the case of the amplifier to a heavy copper bar, which was mounted inside a brass box. Then the box was imerged slowly in a bath of liquid nitrogen inside a Dewar vase. After 10 minutes the boiling rate of the liquid nitrogen slowed down as the temperature of the box, and therefore the amplifier's case, reached 77 *K*. Liquid nitrogen was added at steady intervals to maintain a constant level inside the Dewar vase.

The first time this amplifier was cooled down, the FET's gate pin broke, thereby prohibiting any further operation of the ALPHA FET. When brought back to room temperature, it appeared that the substrate board had curled and that its edges were no longer grounded to the amplifier's case. All attempts to solder the original boards back, failed. When operating with a new FET, the amplifier presented various reso-

nances within the frequency band of interest, and was finally abandoned for a completely new design.

4. Second prototype

The second and final single stage amplifier prototype is described in Figure IV.9.

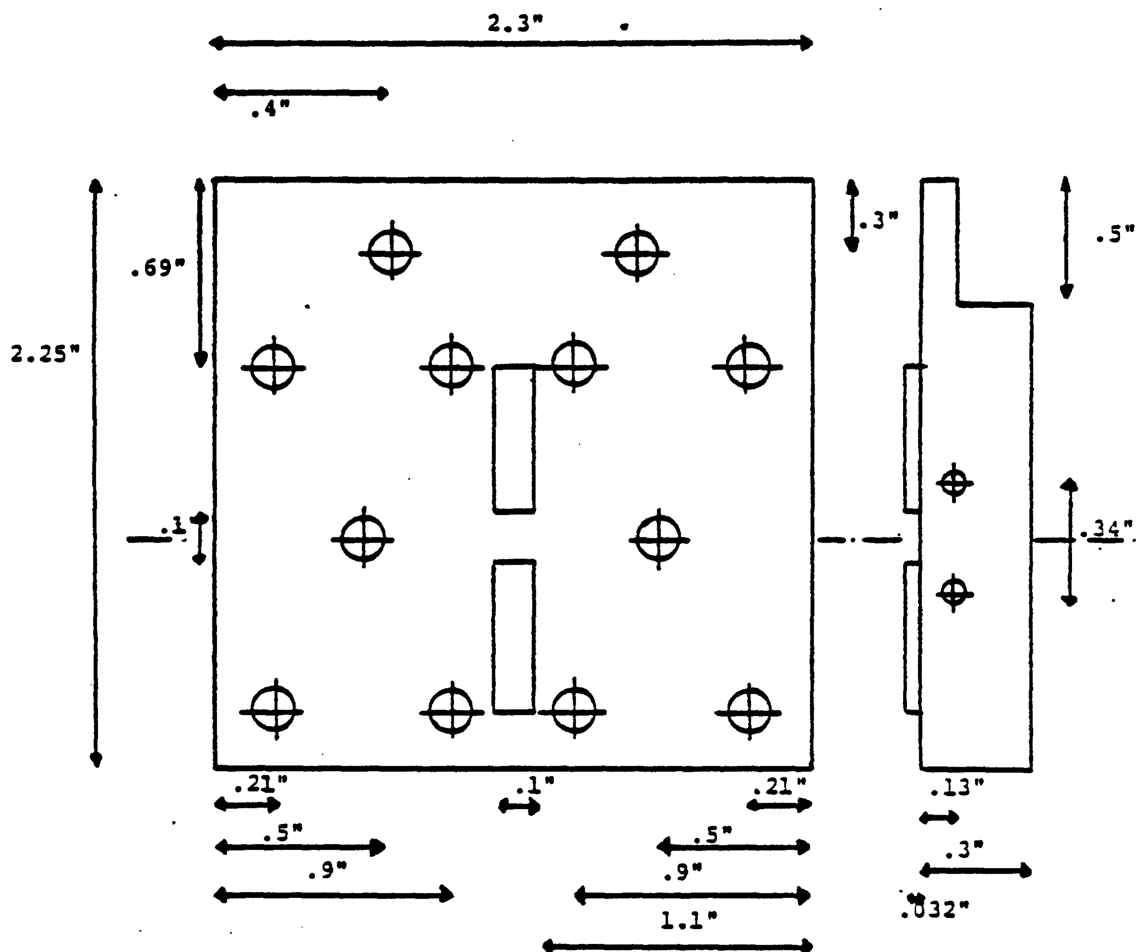


Figure IV.9

Second Prototype

This amplifier has a copper case. Although more difficult than brass to work with mechanically, copper presents the advantage of a better thermal conductivity. To avoid the board curling problem that affected the first prototype, input and output boards were bolted tightly against the amplifier's case. Nylon washers were used under each

screw to more evenly distribute the pressure on the substrate board and assure a better grounding. To achieve a better thermal contact between the FET and the amplifier's case, the source ridges were machined out of the copper case. The bias networks were similar to the first version.

Matching the FET to its optimal noise impedance over a large range of frequency is a difficult task. This because any physical impedance exhibits a reactive component whose variations are positive with frequency. That is

$$Z_\Phi(\omega) = R_\Phi(\omega) + jX_\Phi(\omega)$$

$$\frac{\partial X_\Phi(\omega)}{\partial \omega} \geq \left| \frac{X_\Phi(\omega)}{\omega} \right| \geq 0$$

Theoretical [6] and experimental [7], [section III.3] results show that the transistor's optimal noise impedance has a reactive component whose variations are negative with frequency. that is the opposite way,

$$Z_{opt}(\omega) = R_{opt}(\omega) + jX_{opt}(\omega)$$

$$\frac{\partial X_{opt}(\omega)}{\partial \omega} < 0$$

Nevertheless, the transistor can be fairly well matched to its optimal noise impedance over a finite range of frequency. this is provided that the variations of X_Φ and X_{opt} are small over the considered bandwidth.

In the case of the second prototype, the input was optimized for a match at 8.45 GHz. Figure IV.10a presents the single stage amplifier gain for a bias of $V_{ds} = 3\ V$ and $I_d = 10\ mA$ at both room and cryogenic temperatures. Figure IV.10b presents the

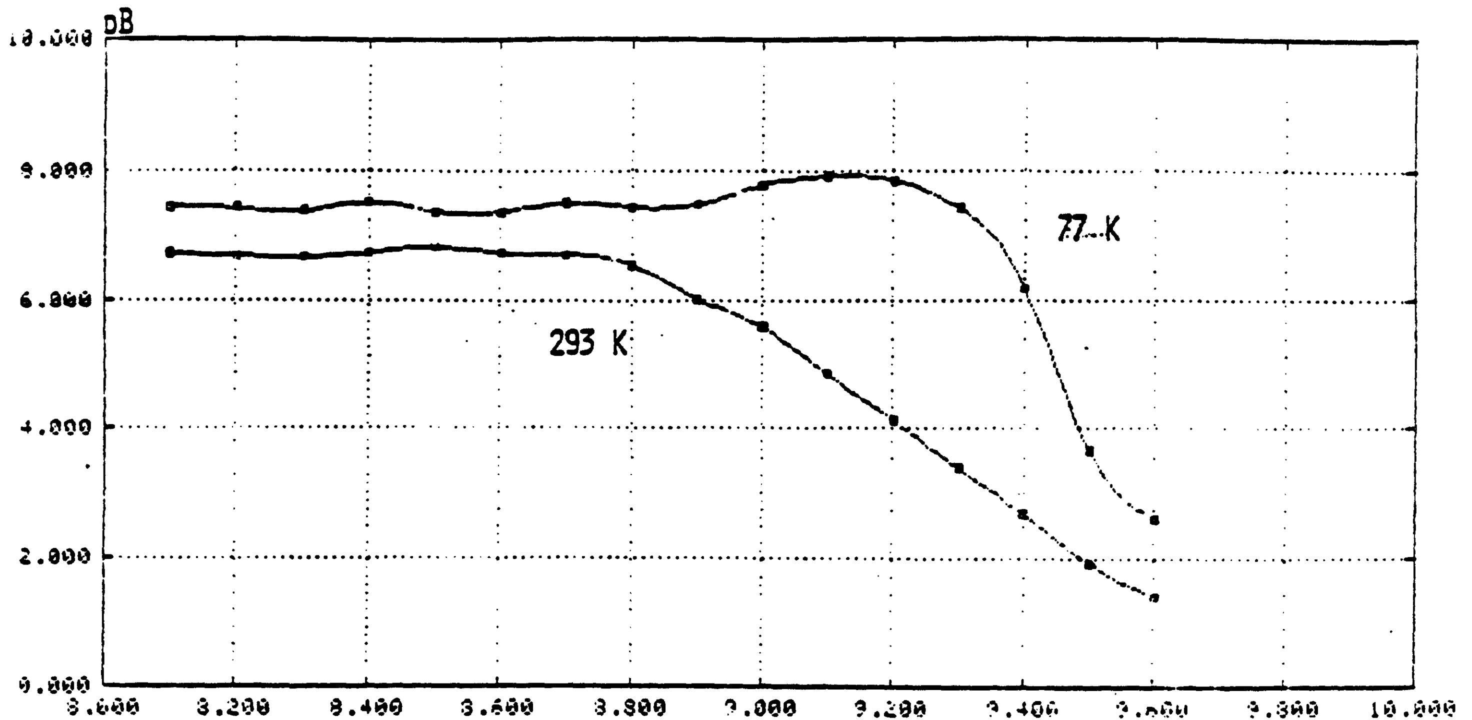


Figure IV.10 a

Second Prototype Gain Curve, $V_{ds} = 3\ V$, $I_d = 10\ mA$

equivalent noise temperature of the amplifier under the same conditions. Figures IV.11a and b display the same quantities for a FET bias of $V_{ds} = 3\ V$ and $I_d = 30\ mA$.

The cooling to $77\ K$ improves the performance of the amplifier in two ways. The gain increases an average of 1.85 dB for a bias of 10 mA (1.8 dB for 30 mA). This increase in gain results from the increase of the FET internal conductance gm as the physical temperature of the lattice decreases. In addition, especially for frequencies between 8.9 and 9.3 GHz, it seems that the input board better matches the FET's optimal gain impedance. Two explanations can be advanced to explain this effect: a drastic change in the scattering parameters of the FET (especially S_{11}), or a somewhat important deformation of the substrate board. The exact reason for this improvement was not further investigated.

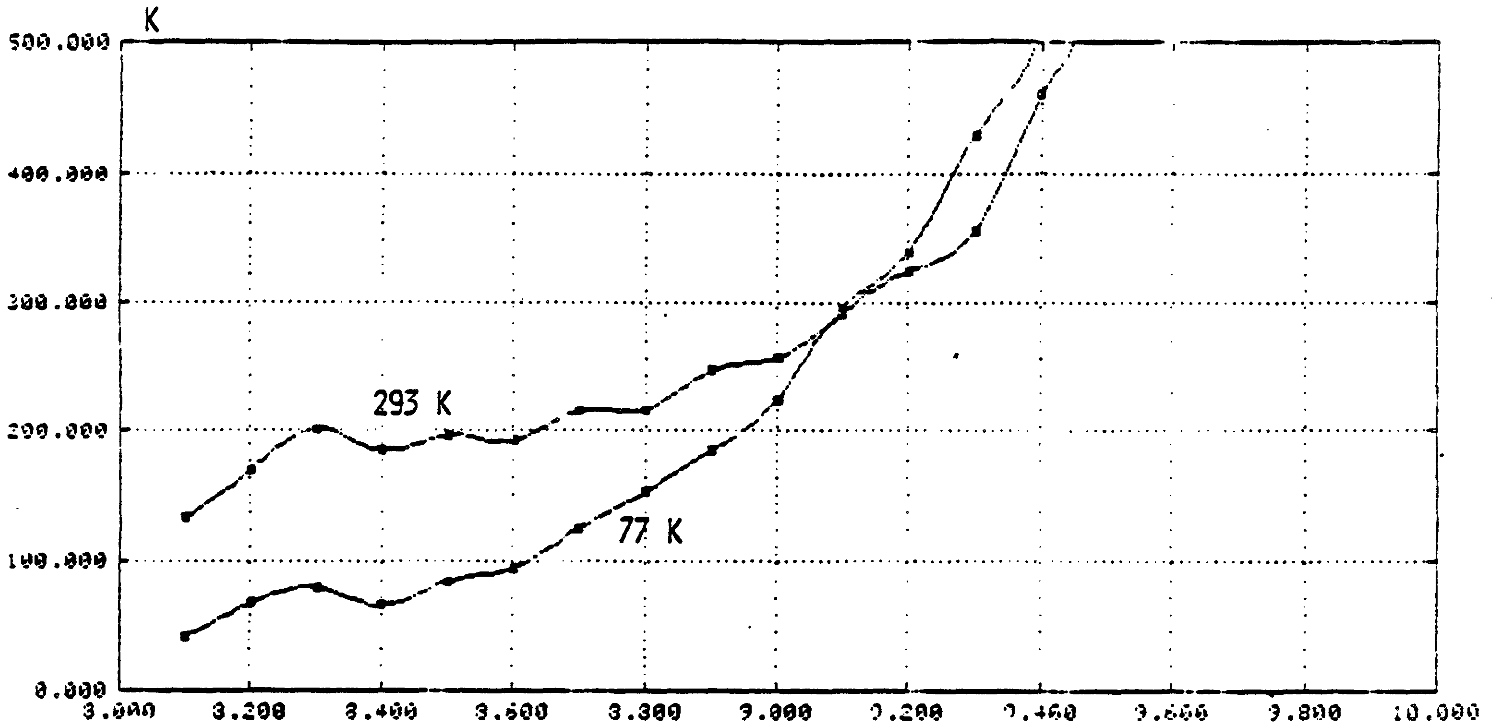


Figure IV. 10 *b*

Second Prototype Noise Temperature Curve, $V_{ds}=3\ V$, $I_d=10\ mA$

When imerged in liquid nitrogen, for frequencies lower than 9 *GHz*, the noise temperature of the amplifier decreases as expected. At 8.45 *GHz* the decrease is significant: 64% for a bias of 10 *mA*, 61% for 30 *mA*. For higher frequencies where the room temperature noise figure was much greater, the noise figure increased when the amplifier was cooled. This defect could be explained by parasitic oscillations developed under the substrate board when cooled. This possible explanation is consistant with the fact that although low, the noise temperature of the prototype remains much higher than the computed FET minimum noise temperature.

A better method of grounding is desirable. A proposed solution is to solder only the center of the substrate board to the case of the amplifier and hold its edges to the amplifier with screws.

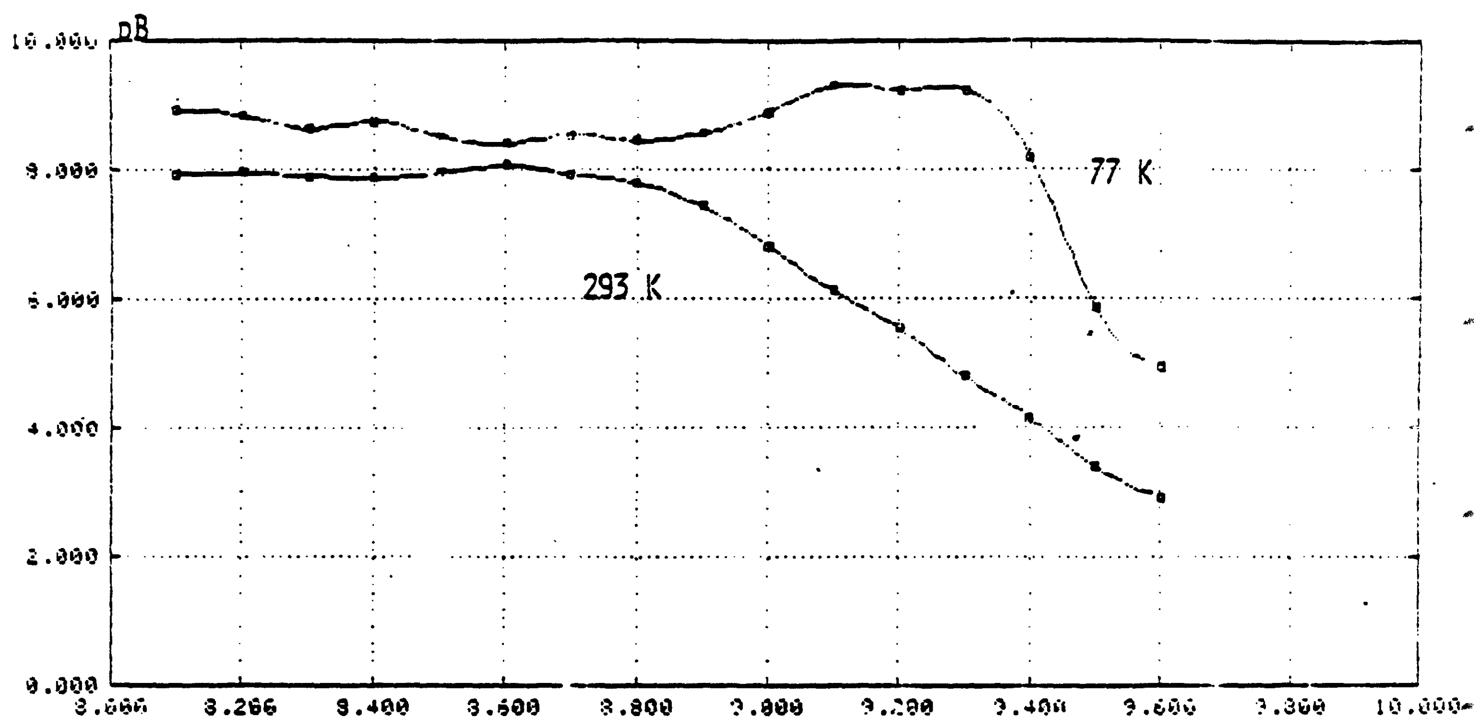


Figure IV. 11 *a*

Second Prototype Gain Curve, $V_{ds}=3\ V$, $I_d=30\ mA$

The gain bandwidth Δf_G of the second prototype is larger than that of the first one. For a bias of 10 mA at 77 K the bandwidth is, at least, 1.5 GHz* wide around 8.4 GHz. This corresponds to a quality factor Q_G of, at most, 5.6 and a BCFR of, at least, 18%. The 1 dB noise bandwidth Δf_N is greater than .9 GHz which correspond to a quality factor Q_N of, at most, 9.4 and a BCFR of, at least, 10.8%.

The variations of gain versus drain current was measured at 8.45 GHz and room temperature, after regrounding the input board The result is shown in Figure IV.12.

Using the computed noise parameters of the FET and the source impedance of the input board, the expected noise temperature of the prototype was calculated. At 8.45

* Measurements for frequencies lower than 8 GHz could not be performed because at the time of the measurement no sweeping oscillator was available in the 6-8 GHz band.

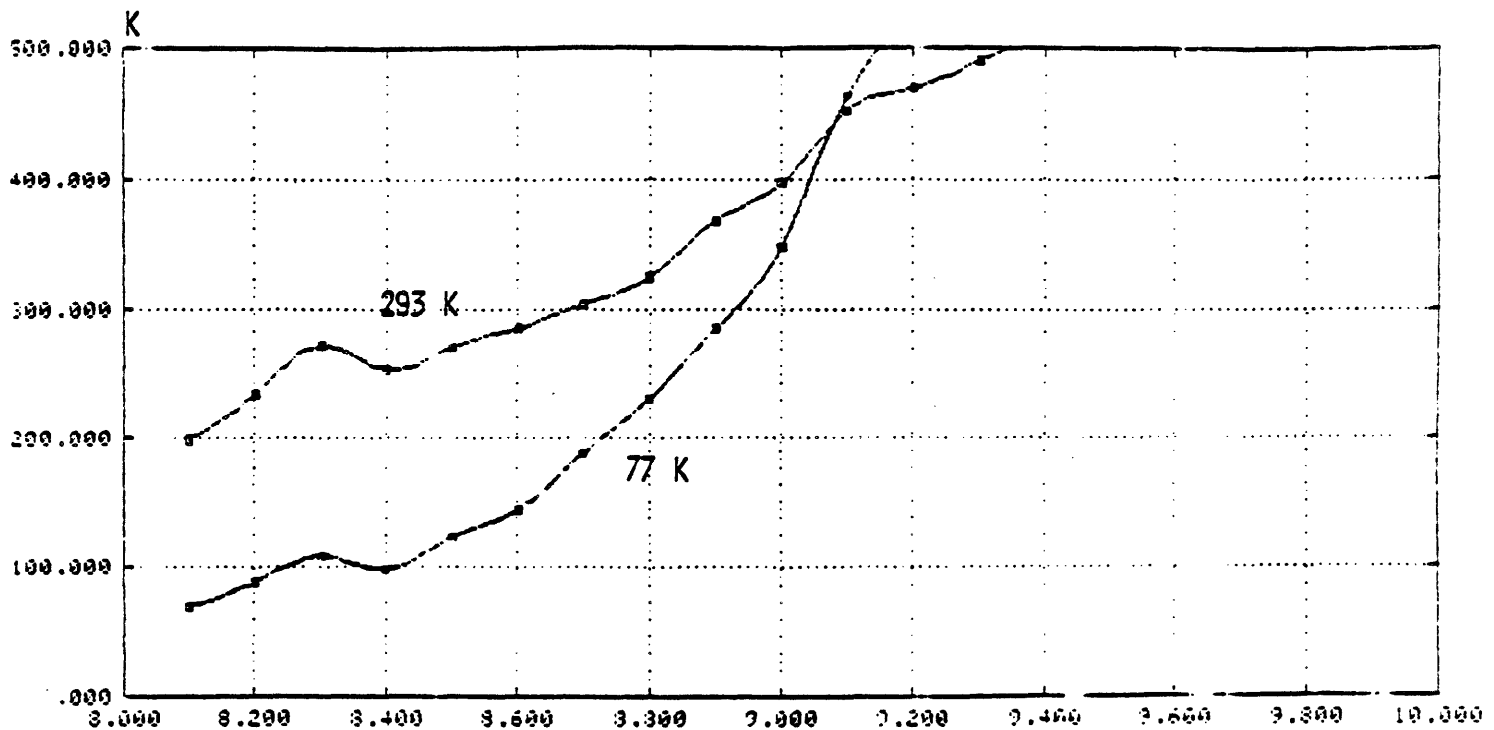
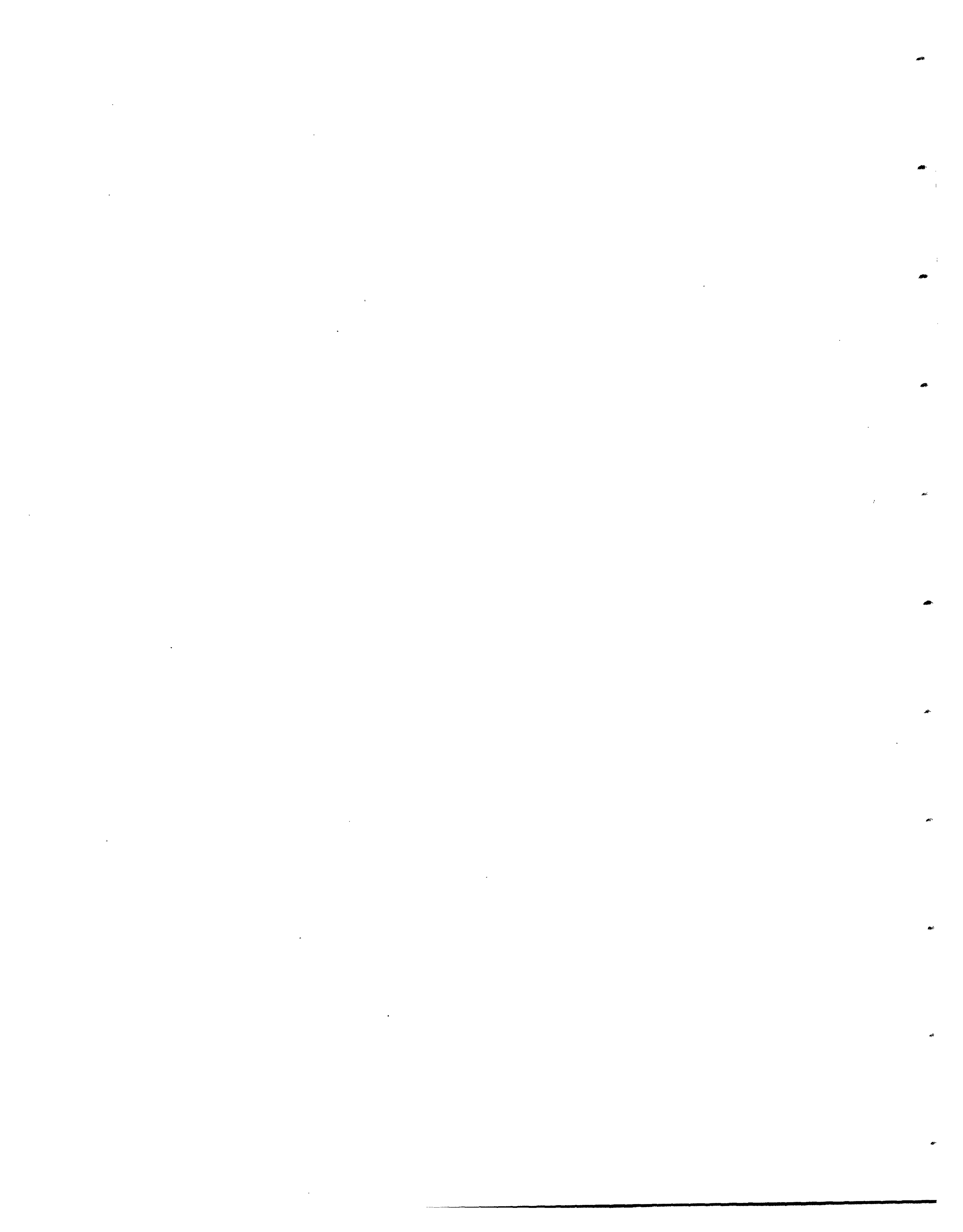


Figure IV.11 b

Second Prototype Noise temperature Curve, $V_{ds}=3\ V$, $I_d=30\ mA$

GHz, the calculations yield a noise temperature of 146 ±10 *K* at room temperature and 52±8 *K* at 77 *K*. In both cases, the noise performance of the single stage amplifier is worse (180 and 68 *K*) than the calculations indicate because of losses and mismatches in the input network. The attenuation formulae derived in Appendix C3 allow the calculation of these differences. At room temperature, the attenuation α is 1.2 *dB*, and at 77 *K* is 1.8 *dB*, out of which .3 *dB* is caused by the DC blocking capacitor. More work need to be done to reduce these attenuations and further improve the performance of the prototype.

It is possible to estimate the noise temperature and gain of a three stage amplifier with the first FET biased at 10 *mA* and the two last ones at 30 *mA*. Provided that each of the interstage networks create a .5 *dB* mismatch, a gain of 24 *dB* and a noise tem-



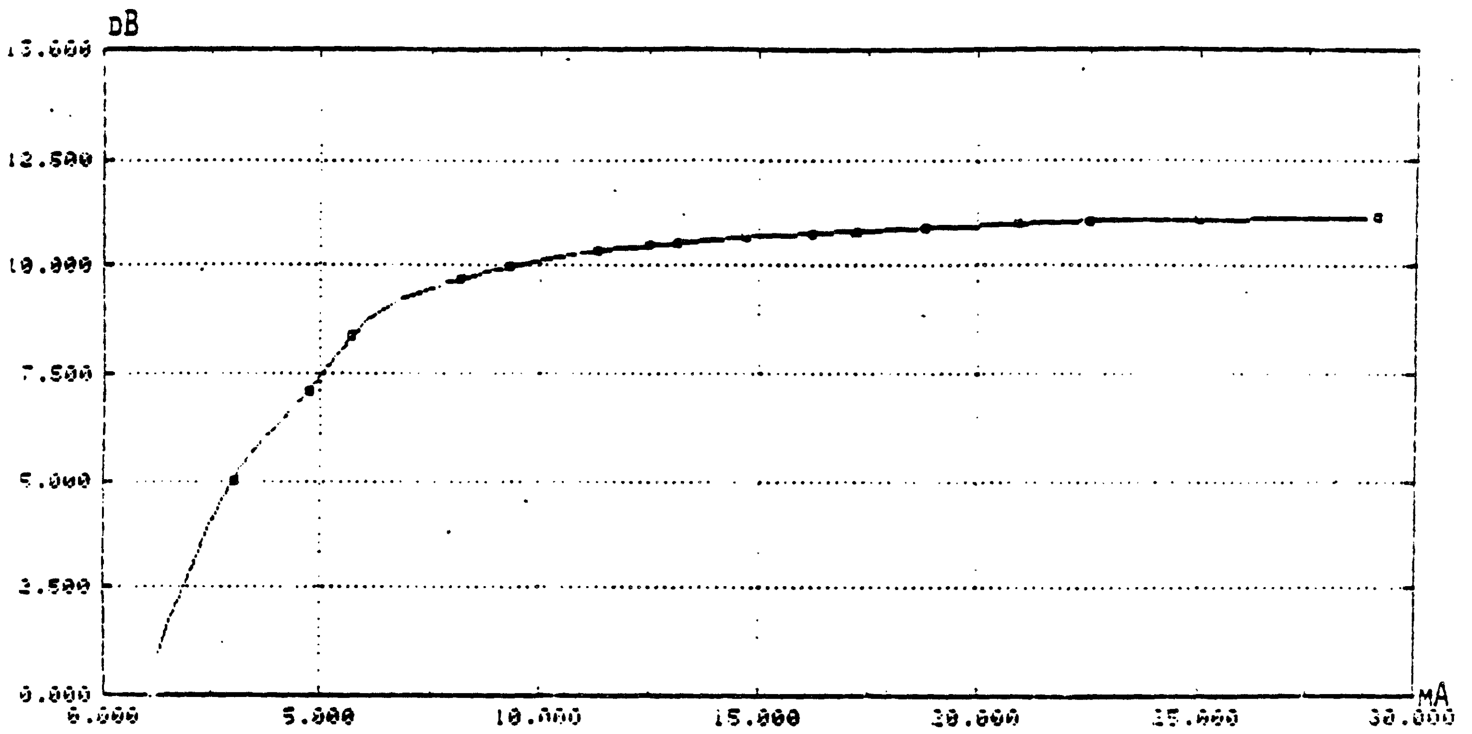


Figure IV.12

Gain versus Drain Current

perature of 90 K at 77 K can be expected.

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CHAPTER V: SUMMARY AND CONCLUSIONS

1. Results

In this thesis, a study was presented on the behavior of cryogenically cooled Gallium-Arsenide field-effect transistors. The research was carried out in two main directions.

The first part of the work was concerned with the measurement of several of the FET parameters in the X-band. The measurement of the power scattering parameters provided an estimate of the stability factor k and of the various gains associated with a particular FET and their variation with the DC bias of the FET. Because of insufficient accuracy in experimental measurements (especially those related to phase terms), one could draw limited conclusions concerning the operation of single or multiple stage FET amplifiers. The FET transconductance was found to increase when cooled, thus causing an increase in the RF gain.

The noise parameters of the FET and their variation with frequency, physical temperature and DC bias were extensively studied. Between 8 and 10 GHz, the frequency

dependence of the minimum noise temperature T_{min} was found to be almost linear and the dependence of the noise conductance gn quadratic. To this extent, these results confirm the theory of Pucel et al.

It has also been shown that the noise temperature improvement factor for cooling from 293 to 77 K varies from 2.1 to 2.8 depending on the frequency and DC bias of the FET. These physical temperature dependencies of the noise parameters and DC bias were found to be comparable to results pertaining other FET's and other frequencies.

Finally, FET channel physical parameters such as thickness, width and carrier density were determined. Changes in pinch-off voltage and Schottky barrier potential were found to be small in the 293-77 K range.

The second part of the work was concerned with the design and evaluation of a single stage cryogenically cooled FET amplifier.

When cooled at 77 K and operated at 8.45 GHz, the amplifier exhibited a noise temperature of 68 K and a gain of 7.2 dB. When biased with a larger FET drain current (30 mA), the gain of the amplifier improved to 8.5 dB, while the noise performance was degraded to a level of 100 K. Although, they did not greatly affect the gain bandwidth of the amplifier, grounding problems in the matching networks corrupted the noise temperature of the amplifier, especially at high frequencies. Overall, the reliability and feasibility of microstrip tuned X-band amplifiers was demonstrated. The single stage prototype has been subjected to over twenty 293-77 K cycles with no failure and little retuning.

2. Suggestions for further research

A more complete characterization of the FET is possible. It requires low-frequency measurement of the parasitic elements of the transistor and the matching of the small signal equivalent circuit with the measured scattering and noise parameters. Measurement of the noise parameters at lower temperatures are necessary to distinguish between thermal noise carried by parasitic resistances, and non thermal noise caused by high field diffusion noise and intervalley scattering. More accurate measurements of the scattering parameter are necessary to study the variations of the stability factor and available gains with temperature.

Although shown efficient, the use of microstrip tuning still presents questions that need resolving. One must master the problem of radiation loss and that of characterization of the impedance presented by blocking capacitors, connectors and other non perfect elements.

In order to test the measurements and results of the first stage amplifier and to investigate interstage matching networks, a three stage version has to be constructed.

APPENDIX C1: NOISE PARAMETERS DETERMINATION

The program VANDA listed below accepts as input data a set of four triplets T_{FET}, R_{source} and X_{source} and derives the parameters R_{opt}, X_{opt}, gn and T_0. It also provides with the R_n, $R_c/|Z_c|$, $X_c/|Z_c|$ of the Rothe-Dalke representation of noisy twoports.

The inversion of the matrix $[\Omega]$ uses the Gauss pivot method.

```
 10 DIM C(4,5),S(5),A(4),T(4,5),
    Y(4),R(4),Q(4),T1(4),X(4)
 20 INTEGER I(4),J(4),D(4)
 30 CLEAR @ BEEP 100,100
 40 ON KEY# 1,"MASTER" GOTO 1440
 50 ON KEY# 4,"PROG" GOTO 80
 60 KEY LABEL
 70 GOTO 70
 80 FOR K=1 TO 4
 90 CLEAR
100 DISP USING 110 ; K
110 IMAGE "resistance number: ",
    D
120 INPUT R(K)
130 DISP USING 140 ; K
140 IMAGE " reactance number: ",
    D
150 INPUT X(K)
160 DISP USING 170 ; K
170 IMAGE " input the value of T
     number: ",D
180 INPUT T1(K)
190 NEXT K
200 CLEAR
210 DISP "  n       T        R
      X"
220 DISP "+++++++++++++++++++++++
    ++++++++++"
230 FOR U=1 TO 4
240 DISP USING 250 ; U,T1(U),R(U
    ),X(U)
250 IMAGE "+  ",D," + ".DDDD." +
     ",MDDD.DD," + ",MDDD.DD,"+"
260 DISP "+++++++++++++++++++++++
    ++++++++++"
270 NEXT U
280 DISP "If it is ok hit [END L
    INE ]"
290 INPUT W$
300 IF W$<>"" THEN 80
310 COPY
320 CLEAR
330 DISP "that is it! It si work
    ing"
340 FOR L=1 TO 4
350 C(L,1)=1
360 C(L,2)=290/R(L)
370 C(L,3)=(R(L)^2+X(L)^2)*290/R
    (L)
380 C(L,4)=-(2*X(L)*290/R(L))
390 C(L,5)=T1(L)
400 NEXT L
410 N=4
420 FOR I=1 TO N
430 FOR J=1 TO N+1
440 T(I,J)=C(I,J)
450 NEXT J
460 NEXT I
470 M=N+1
480 D=1
```

```
490 FOR K=1 TO N
500 K1=K-1
510 P=0
520 FOR I=1 TO N
530 FOR J=1 TO N
540 IF K=1 THEN 610
550 FOR I2=1 TO K1
560 FOR J2=1 TO K1
570 IF I=I(I2) THEN 650
580 IF J=J(J2) THEN 650
590 NEXT J2
600 NEXT I2
610 IF ABS(T(I,J))<=ABS(P) THEN
    650
620 P=T(I,J)
630 I(K)=I
640 J(K)=J
650 NEXT J
660 NEXT I
670 I3=I(K)
680 J3=J(K)
690 D=D*P
700 FOR J=1 TO M
710 T(I3,J)=T(I3,J)/P
720 NEXT J
730 T(I3,J3)=1/P
740 FOR I=1 TO N
750 T=T(I,J3)
760 IF I=I3 THEN 810
770 T(I,J3)=-(T/P)
780 FOR J=1 TO M
790 IF J<>J3 THEN T(I J)=T(I,J)-
    T*T(I3,J)
800 NEXT J
810 NEXT I
820 NEXT K
830 FOR I=1 TO N
840 I4=I(I)
850 J4=J(I)
860 D(I4)=J4
870 S(J4)=T(I4,M)
880 NEXT I
890 T=0
900 N1=N-1
910 FOR I=1 TO N1
920 P1=I+1
930 FOR J=P1 TO N
940 IF D(J)>=D(I) THEN 990
950 T1=D(J)
960 D(J)=D(I)
970 D(I)=T1
980 T=T+1
990 NEXT J
1000 NEXT I
1010 IF INT(T/2)*2<>T THEN D=-D
1020 FOR J=1 TO N
1030 FOR I=1 TO N
1040 I4=I(I)
1050 J4=J(I)
1060 Y(J4)=T(I4,J)
1070 NEXT I
1080 FOR I=1 TO N
1090 T(I,J)=Y(I)
1100 NEXT I
1110 NEXT J
1120 FOR I=1 TO N
1130 FOR J=1 TO N
1140 I4=I(J)
1150 J4=J(J)
1160 Y(I4)=T(I,J4)
1170 NEXT J
1180 FOR J=1 TO N
1190 T(I,J)=Y(J)
1200 NEXT J
1210 NEXT I
1220 G=S(3)
1230 X=S(4)/G
1240 R=(S(2)/G-X^2)^.5
1250 T=S(1)+2*G*R*290
1260 PRINT "**************************
     *************"
1270 PRINT USING 1280 ; T,R
1280 IMAGE " T min= ",DDD.D," K"
     ,/," Ropt= ",MDDD.DD," Ω"
1290 PRINT USING 1300 : X,G
1300 IMAGE "  Xopt=",MDDD.DD," Ω
     ",/,"     Gn= ",DDD.DDE," Ω-
     1"
1310 R1=G*(R^2+X^2)
1320 P1=X/SQR(R^2+X^2)
1330 P2=T/(2*(R1*G)^.5*290)-(1-P
     1^2)^.5
1340 R2=P2*(R1/G)^.5
1350 X1=-(P1*(R1/G)^.5)
1360 R3=R1*(1-(P1^2+P2^2))
1370 PRINT USING 1380 ; R1,P2,P1
1380 IMAGE "      Rn=",MDDD.DD," Ω
     ",/,/,"              Γreal=",MD.
     DDD,/,"              Γimag=",MD.
     DDD
1390 PRINT USING 1400 ; R2,X1
1400 IMAGE "              Rcor=",MDDD
     .DD," Ω",/, "            Xcor=
     ",MDDD.DD," Ω"
1410 PRINT USING 1420 : R3
1420 IMAGE "              Rsuc=",MDDD
     .DD," Ω",/,"*****************
     ********************",5/
1430 END
1440 CHAIN "Autost"
```

APPENDIX C2: NOISE TEMPERATURE MEASUREMENTS

As explained earlier in section IV.2, two complementary methods were used to measure noise temperature and FET amplifier gain. In both cases the noise source was an H.P noise diode with an nominal excess noise of 15.2 *dB* in series with a 10 *dB* attenuation pad. An excess noise of approximately 5.2 *dB* permits the usage of the noise figure meter at its maximum sensitivity and also avoids any saturation of the amplifier. A three point fit was made over the calibration values provided by the constructor at 8, 9, 10 *GHz*. The attenuation was carefully measured using powermeter and network analyser.

The first method makes use of the a noise figure meter (HP 340B) and of its analog output to draw directly on an X-Y plotter or an oscilloscope the variations of the noise figure (therefore of the noise temperature) with frequency. First, the noise figure meter sends a square wave 0-28 *V* to the noise diode and reads the power at the output of the receiver when the diode is turned on and off. Then, it deals with the Y-factor of the system defined as

$$Y = \frac{power\ at\ the\ output\ when\ diode\ is\ hot\ (on)}{power\ at\ the\ output\ when\ diode\ is\ cold\ (off)}$$

and related to the different noise temperatures by

$$Y = \frac{T_{Sys} + T_{Hot}}{T_{Sys} + T_{Cold}}$$

where T_{Sys} is the system noise temperature, T_{Cold} the noise temperature of the cold diode, T_{Hot} the noise temperature of the hot diode (ie with the excess noise). One can calculate the noise temperature of the system from its Y-factor through

$$T_{Sys} = \frac{\Delta T}{Y-1} - T_{Cold}$$

where

$$\Delta T = T_{Hot} - T_{Cold}$$
$$\Delta T = 290.Excess\ Noise$$

The noise figure is related to T by

$$F = 1 + \frac{T}{290}$$

This operation is performed automatically by the noise figure meter assuming that the excess noise is 5.2 dB. The program EVA written for the purpose of the computation of T_{FET} takes into account the fact that the effective excess noise applied to the system is slightly different.

$$T_{Sys} = 290.10^{\frac{Exc-5.2}{10}} Fmeter - T_{Cold}$$

where Exc is the excess noise applied expressed in decibels and $Fmeter$ the reading of the noise figure meter. The calibration of the receiver provides us with T_{Reci}, noise temperature with the step attenuator in position i. We have

$$T_{Sys} = T_{FET} + \frac{T_{Reci}}{G_{FET}}$$
$$i = 0,1$$

The noise temperature of the FET is given by

$$T_{FET} = \frac{T_{Rec\,0} T_{Sys\,1} - T_{Rec\,1} T_{Sys\,0}}{T_{Sys\,0} - T_{Sys\,1}}$$

The gain of the FET amplifier is given by

$$G_{FET} = \frac{T_{Rec\,0} - T_{Rec\,1}}{T_{Sys\,1} - T_{Sys\,0}}$$

This computation is performed by the program listed below for 21 points equally spaced between 8 and 10 GHz.

```
10 !  USES THE HP X-Y PLOTTER
20 !
30 !
40 !
50 !
60 !   VERSION OF DEC 09.1982
70 !
80 !
90 DIM A(21),B(21),C(21),D(21),
   E(21),F(21),G(21),H(21),I(21
   ),J(21),K(21),L(21),M(21)
100 GCLEAR
110 CLEAR
120 DISP " what is the date alre
    ady?"
130 DIM B$[50]
140 INPUT B$
150 CLEAR
160 DISP "what is in degree cels
    ius the   temperature of the
     noise diode  please?"
170 INPUT B
180 B=B+273
190 IF B#290 THEN BEEP 300,10 @
    BEEP 900,20
200 IF B#290 THEN DISP "will nee
    d a correction for the  seco
    nd stage noise"
210 IF B#290 THEN WAIT 1000
220 CLEAR
230 DISP USING 240
240 IMAGE 7/,"                WORKI
    NG"
250 DISP USING 260
260 IMAGE 7/
270 FOR P=1 TO 21
280 A(P)=-(.00075*P^2+.018*P+15
    .20275
290 READ M(P)
300 DATA .82,.83,.83,.81,.8,.83,
    .81,.83,.83,.81,.8,.8,.81,.8
    ,.81,.8,.84,.85,.85,.81,.81
310 M(P)=M(P)+9
320 ! A(P) REPRESENTS THE EXCESS
    NOISE OF THE HP NOISE DIODE
    USING A 3 POINTS FITTING CUR
    VE OF
330 ! THE HP CALIBRATION REPORT
340 ! M(P) IS THE ATTENUATION OF
     THE 10 dB PAD COMPOSITE WIT
    H THE APC7 HP
350 A(P)=A(P)-M(P)
360 ! NOW A(P) IS THE REAL EXCES
    S NOISE APPLIED AT THE SYSTE
    M
370 NEXT P
380 DATA 9.84,9.78,9.81,9.84,9.8
    5,9.83,9.9,9.85,9.89,9.88,9.
    83,9.94,9.8,9.9,9.83,9.79,9.
    8,9.68
390 DATA 9.73,9.55,9.48
400 ! DATA M(P) MEASURED THE 7th
    OF OCTOBER 1982 FOR THE 10 d
    B NOMINAL OMNI SPECTRA PAD
410 ! THE INPUTS ARE THE ELONGAT
    IONS MEASURED IN CENTIMETER
    ON THE X-Y PLOTTER WITH THE
    RELATION
420 ! THAT 1.5 cm <--> 1 dB OF N
    OISE FACTOR
430 ! FIRST CHECK IF THE LAST CA
    LIBRATION WAS ALREADY READ
440 G=C(1)
450 IF G=0 THEN GOSUB 1730
460 ! C(P) IS THE ELONGATION EXP
    RESSED IN CENTIMETER OF THE
    PLOTON THE X-Y PLOTTER WHEN
    THE
470 ! RECEIVER IS IN POSITION 0
480 ! D(P) IS THE NOISE TEMPEART
    URE DERIVED FROM THE EXPRESS
    ION PRESENTED IN THE INTRODU
    CTION
490 ! E(P) IS THE ELONGATION EXP
    RESSED IN CENTIMETER OF THE
    PLOTON THE X-Y PLOTTER WHEN
    THE
500 ! RECEIVER IS IN POSITION 1
510 ! F(P) IS THE NOISE TEMPEART
    URE DERIVED FROM THE EXPRESS
    ION PRESENTED IN THE INTRODU
    CTION
520 !
530 CLEAR
540 !
550 DISP "  first serie of measu
    rement"
560 DISP "   Receiver in positio
    n 0"
570 WAIT 2500
580 CLEAR
590 FOR P=1 TO 21
600 F=7.9+P*.1
610 DISP USING 620 ; F
620 IMAGE "  for a frequency of"
       ,DD.D," GHz"
630 INPUT G(P)
640 H(P)=87.579*10^((1.5*A(P)+G(
    P))/15)-6
650 CLEAR
660 NEXT P
670 !
680 ! ENTRY OF THE ELONGATIONS G
    (P) FOR THE RECEIVER IN POSI
    TION 0
690 ! H(P) IS THE ARRAY OF NOISE
     TEMPERATURE
700 !
710 FOR P=1 TO 21
720 DISP USING 730 ; 7.9+P*.1,G(
    P)
```

```
730 IMAGE " [ F=",DD.DD,"GHz ][
    L=",DD.DD," cm ]"
740 NEXT P
750 DISP USING 760
760 IMAGE "if it is O K hit  [EN
    D LINE]"
770 INPUT A$
780 IF A$<>"" THEN 580
790 CLEAR
800 DISP "    second serie of mea
    surements"
810 DISP "     Receiver in positi
    on 1"
820 WAIT 2500
830 CLEAR
840 FOR P=1 TO 21
850 F=7.9+P*.1
860 DISP USING 620 ; F
870 INPUT I(P)
880 J(P)=87.579*10^((1.5*A(P)+I(
    P))/15)-B
890 CLEAR
900 NEXT P
910 !
920 ! I(P) ELONGATIONS IN CM FOR
    THE RECEIVER IN POSITION 1
930 ! J(P) IS THE ARRAY OF NOISE
    TEMPERATURE
940 !
950 FOR P=1 TO 21
960 DISP USING 730 ; 7.9+P*.1;I(
    P)
970 NEXT P
980 DISP USING 760
990 INPUT A$
1000 IF A$<>"" THEN 830
1010 M=0 @ T=10000
1020 FOR P=1 TO 21
1030 K(P)=(D(P)-F(P))/(H(P)-J(P)
     )
1040 L(P)=J(P)-F(P)/K(P)
1050 IF K(P)>M THEN M=K(P) @ N=P
1060 IF L(P)<T THEN T=L(P) @ O=P
1070 NEXT P
1080 CLEAR
1090 FOR P=1 TO 21
1100 DISP USING 1110 ; 7.9+.1*P,
     10*LGT(K(P)),L(P)
1110 IMAGE "F=",DD.DD," GHz G(dB
     )=",MDD.D,"  T=" ,DDDD
1120 NEXT P
1130 PRINT
1140 PRINT USING 1150 ; 10*LGT(M
     ),7.9+.1*N
1150 IMAGE "Gain max=",MDD.D," p
     our F=",DD.DD," GHz",//
1160 PRINT USING 1170 ; T,7.9+.1
     *O
1170 IMAGE "    T min=",DDDD,"  p
     our F=",DD.DD," GHz",6/
1180 INPUT A$
1190 GCLEAR
1200 SCALE 7.85,10.1,-100,1050
1210 XAXIS 0,.2,8,10.1
1220 YAXIS 8,100,0,1050
1230 FOR X=8 TO 10 STEP .4
1240 LDIR 0
1250 MOVE X-.035,-100
1260 LABEL VAL$(X)
1270 NEXT X
1280 FOR Y=0 TO 1000 STEP 100
1290 LDIR 0
1300 MOVE 7.85,Y-20
1310 LABEL VAL$(Y/100)
1320 NEXT Y
1330 FOR P=1 TO 21
1340 MOVE 7.9+P*.1,1000*LGT(K(P)
     )
1350 GOSUB 1660
1360 MOVE 7.9+P*.1,L(P)
1370 GOSUB 1700
1380 NEXT P
1390 PENUP
1400 PLOT 8,1000*LGT(K(1))
1410 FOR P=2 TO 21
1420 DRAW 7.9+.1*P,1000*LGT(K(P)
     )
1430 NEXT P
1440 LDIR 0
1450 LABEL "G"
1460 PENUP
1470 PLOT 8,L(1)
1480 FOR P=2 TO 21
1490 DRAW 7.9+.1*P,L(P)
1500 NEXT P
1510 LABEL "T"
1520 MOVE 10.05,-100
1530 INPUT A$
1540 IF A$<>"" THEN 10
1550 COPY
1560 FOR P=1 TO 21
1570 PRINT USING 1580 ; 7.9+.1*P
     ,10*LGT(K(P)),L(P)
1580 IMAGE "F=",DD.DD," GHz G=",
     MDD.D,"dB T=",DDDD," K"
1590 NEXT P
1600 PRINT
1610 PRINT " measures of the "&B
     $
1620 PRINT
1630 PRINT
1640 GOTO 10
1650 END
1660 IMOVE -.0075,5
1670 IDRAW .015,0 @ IDRAW 0,-10
1680 IDRAW -.015,0 @ IDRAW 0,10
1690 RETURN
1700 IMOVE 0,7.5 @ IDRAW 0,-15
1710 IMOVE .012,7.5 @ IDRAW -.02
     3,0
```

```
1720 RETURN
1730 ! THE COMPUTER DOES NOT KNO
     W C(1) THUS WE NEED OR TO E
     NTER ORTO READ A CALIBRATIO
     N
1740 CLEAR
1750 DISP "do you want to enter
     a new calibration (N) or us
     e the old one(O)"
1760 INPUT A$
1770 CLEAR
1780 IF (A$#"O")*(A$#"N")=1 THEN
      1750
1790 ASSIGN# 1 TO "CALIB"
1800 FOR P=1 TO 21
1810 IF A$="O" THEN READ# 1 ; C(
     P),E(P)
1820 IF A$="O" THEN DISP USING 1
     830 ; 7.9+.1*P,C(P),E(P)
1830 IMAGE "F=",DD.D,"Ghz POS0",
     DD.DD," POS1",DD.DD
1840 IF A$="O" THEN 1910
1850 F=7.9+.1*P
1860 CLEAR
1870 DISP USING 620 , F
1880 DISP " elongations in POS0,
     POS1"
1890 INPUT C(P),E(P)
1900 PRINT# 1 ; C(P),E(P)
1910 D(P)=87.579*10^((1.5*A(P)+C
     (P))/15)-B
1920 F(P)=87.579*10^((1.5*A(P)+E
     (P))/15)-B
1930 NEXT P
1940 ASSIGN# 1 TO *
1950 RETURN
```

The second method uses the power at the output of the receiver when the diode is off and on. Because the variations of the power at the output of the receiver are rapid with frequency (although the variations of the Y-factor are smoother), one needs to carefully set the frequency of the local oscillator. For this purpose, the oscillator was controlled using an HP-85 desk computer and a D/A converter.

Calling B the bandwidth of the receiver, G_R its gain and T_R its noise temperature, one can express the output power when the diode is applied to the receiver alone

$$P_{cold} = kG_R B \left(T_R + T_{cold}\right)$$
$$P_{hot} = kG_R B \left(T_R + T_{hot}\right)$$

where k is the Boltzman constant equal to $1.38\,10^{-23}\ J/K$. Solving the system of equations yields

$$T_R = \frac{T_{hot} - T_{cold}}{\frac{P_{hot}}{P_{cold}} - 1} - T_{cold}$$
$$kBG_R = \frac{P_{cold}}{T_R}$$

If we now place the amplifier in front of the receiver we obtain at the output

$$P_{cold} = kG_R BG_{FET} \left(T_{FET} + T_{cold}\right) + kG_R BT_R$$
$$P_{hot} = kG_R BG_{FET} \left(T_{FET} + T_{hot}\right) + kG_R BT_R$$

We can easily calculate G_{FET} and T_{FET}

$$G_{FET} = \frac{P_{hot} - P_{cold}}{\left(T_{hot} - T_{cold}\right) kG_R B}$$
$$T_{FET} = \frac{T_{hot} - T_{cold}}{\frac{P_{hot}}{P_{cold}} - 1} - T_{cold} - \frac{T_R}{G_{FET}}$$

Because of the rapid variations with frequency (and as stated for the first method slightly with time) of the output of the receiver, recalibration had to be undertaken regularly. The two programs listed below respectively completed the calibration of the receiver and the measurement of the FET gain and noise temperature. A typical output plot of results is also presented.

```
 10 ENABLE KBD 32
 20 ON KEY# 8,"" GOTO 1110
 30 ! ROOREC
 40 ! A(P) FREQUENCY TO APPLY
 50 ! B(P) VOLTAGE TO APPLY
 60 ! C(P) EXCESS NOISE DIODE
 70 ! D(P) ATTENUATION 10 DB PAD
 80 DIM Z(3)
 90 DIM A(21),B(21),C(21),D(21),
    E(21),F(21),G(21),H(21),I(21
    ),J(21),K(21),L(21),M(21),N(
    21)
100 ! T T COLD
110 T=293
120 CLEAR @ DISP "INITIALIZATION
    "
130 ASSIGN# 1 TO "RECEIR"
140 FOR P=1 TO 16
150 A(P)=8+.1*P
160 B(P)=-.40322+.80645*P
170 C(P)=15.22+.0165*P-.00075*P*
    P
180 READ D(P)
190 C(P)=C(P)-D(P)
200 ! NOW C(P) EXCESS NOISE APPL
    IED IN DB
210 ! E(P)= T HOT -T COLD
220 E(P)=290*10^(.1*C(P))
230 IMAGE "F=",DD.D, "Ghz POC="
    ,MDD DD," POH=" .MDD.DD
240 NEXT P
250 ! **************************
260 DATA 10.38,10.25,10,10.13,10
    .06,10.23,10 18,10 29,10 3,1
    0 35,10.31,10 37,10.36,10.36
    ,10.38
270 DATA 10.13
280 DISP "INITIALIZATION DONE"
290 BEEP 100,100 @ BEEP 500,20 @
     BEEP 100,100
300 DISP "SETTING THE GPIO INTER
    FACE"
310 CONTROL 4,0 ; 0
320 ! TURN OFF THE PARITY CHECKS
    241 ! ***********************
    ***
330 CONTROL 4,1 ; 0
340 ! NO INTERRUPT COMING FROM P
    ERIPHERAL
350 CONTROL 4,2 ; 64
360 ! INVERSES THE LOGIC ON THE
    FLAG LINE.THIS ONE IS CONNEC
    TED TO THE GROUND
370 CONTROL 4,4 ; 192
380 ! TURN OFF HANDSHAKE PROCEDU
    RE.
390 CONTROL 4,5 ; 0+4
400 ! NO TRIGGER PORT C IS OUTP
    UT
410 CONTROL 4,6 ; 0
```

```
420 ! STROBE PULSATION=0
430 CONTROL 4,9 ; 0
440 ! DO NOT OUTPUT INHIBIT
450 BEEP 10,500
460 DISP "MEASUREMENTS"
470 FOR P=1 TO 16
480 CLEAR
490 ! SWITHCHES DIODE OFF
500 ASSERT 4;0
510 V=B(P)
520 V=(V+12.5/512)/12.5
530 I=INT(V*255)
540 C$=DTB$(I)
550 DISP USING 580 ; A(P)
560 DISP USING 590 ; V*12.5
570 DISP USING 600 ; C$[9]
580 IMAGE "Operating Frequency="
    ,DD.D," Ghz"
590 IMAGE " Control Voltage=",DD
    .DD," V"
600 IMAGE "Transmission Pattern=
    ",K
610 OUTPUT 404 USING "#,B" ; I
620 ! SWEEPER AT THE RIGHT FREQU
    ENCY
630 WAIT 100
640 GOSUB 1000
650 ! READ POWER COLD
660 ! J(P) POWER COLD IN DB
670 J(P)=Z(1)
680 ! SWITCH DIODE ON
690 ASSERT 4;2
700 WAIT 100
710 GOSUB 1000
720 ! READ POWER HOT
730 ! K(P) POWER HOT IN DB
740 K(P)=Z(1)
750 ! SWITCH DIODE OFF
760 ASSERT 4;0
770 PRINT USING 230 ; A(P),J(P),
    K(P)
780 PRINT# 1 ; J(P),K(P)
790 ! POWERS IN WATTS
800 NEXT P
810 PRINT
820 PRINT
830 ASSIGN# 1 TO *
840 FOR P=1 TO 16
850 ! POWERS IN WATTS
860 J(P)=10^(.1*J(P))
870 K(P)=10^(.1*K(P))
880 H(P)=E(P)/(K(P)/J(P)-1)-T
890 I(P)=J(P)/(T+H(P))
900 PRINT USING 910 ; A(P),H(P),
    I(P)*100000
910 IMAGE "F=",DD.D ," T=",DDDD,
    "K  Gr=",DDD.DD
920 NEXT P
930 ! SWEEP BACK TO CW
940 OUTPUT 404 USING "#,B" ; 0
950 ASSIGN# 3 TO "PARAME"
960 READ# 3 ; A$,B$,T1,T2,T4
970 ASSIGN# 3 TO *
980 IF A$="AUTO" THEN CHAIN "RUN
    -PR"
990 END
1000 X$="9D+R"
1010 FOR I=1 TO 3
1020 OUTPUT 713 ;X$
1030 ENTER 713 ; V$
1040 Z(I)=VAL(V$[4])
1050 IF I<3 THEN WAIT 1000
1060 NEXT I
1070 IF (ABS(Z(1)-Z(2))<.02)*(AB
     S(Z(1)-Z(3))<.02)=0 THEN 10
     00
1080 Z(1)=(Z(1)+Z(2)+Z(3))/3
1090 RETURN
1100 END
1110 ENABLE KBD 255
1120 ! SWITCHES DIODE OFF
1130 ASSERT 4;0
1140 ! SWEEPER AT CW
1150 OUTPUT 404 USING "#,B" ; 0
1160 DISP "    AUTHORIZED INTERRU
     PT"
1170 STOP
1180 END
```

```
10 ENABLE KBD 32
20 ON KEY# 8,"" GOTO 1810
30 ! ROOFET
40 ! A(P) FREQUENCY TO APPLY
50 ! B(P) VOLTAGE TO APPLY
60 ! C(P) EXCESS NOISE DIODE
70 ! D(P) ATTENUATION 10 DB PAD
80 DIM Z(3)
90 DIM A(20),B(20),C(20),D(20),
   E(20),F(20),G(20),H(20),I(20
   ),J(20),K(20),L(20),M(20),N(
   20)
100 ! T T COLD
110 T=293
120 ASSIGN# 1 TO "RECEIR"
130 ! RECEI POW C AND POWH OF TH
    E RECEIVER
140 CLEAR @ DISP "INITIALIZATION
    "
150 FOR P=1 TO 16
160 A(P)=8+.1*P
170 B(P)=-.40322+.00645*P
180 C(P)=15.22+.0165*P-.00075*P*
    P
190 READ D(P)
200 C(P)=C(P)-D(P)
210 ! NOW C(P) EXCESS NOISE APPL
    IED IN DB
220 ! E(P)= T HOT -T COLD
230 E(P)=290*10^(.1*C(P))
240 ! F(P) POWER C IN DB
250 ! G(P) POWER H IN DB
260 READ# 1 ; F(P),G(P)
270 DISP USING 280 ; A(P),F(P),G
    (P)
280 IMAGE "F=",DD.D," Ghz POC=",
    MDD.DD," POH=",MDD.DD
290 F(P)=10^(.1*F(P))
300 G(P)=10^(.1*G(P))
310 ! POWER IN WATTS
320 ! H(P) NOISE TEMPERATURE OFF
     THE RECEIVER
330 H(P)=E(P)/(G(P)/F(P)-1)-T
340 ! I(P) IS THE PRODUCT k.B.Gr
350 I(P)=F(P)/(T+H(P))
360 NEXT P
370 ! ************************
380 DATA 10.38,10.25,10.10.13,10
    .06,10.23,10.19,10.29,10.3,1
    0.35,10.31,10.37,10.36,10.36
    ,10.38
390 DATA 10.13
400 ASSIGN# 1 TO *
410 DISP "INITIALIZATION DONE"
420 BEEP 100,100 @ BEEP 500,20 @
     BEEP 100,100
430 DISP "SETTING THE GPIO INTER
    FACE"
440 CONTROL 4,0 ; 0
450 ! TURN OFF THE PARITY CHECKS
460 CONTROL 4,1 ; 0
470 ! NO INTERRUPT COMING FROM P
    ERIPHERAL
480 CONTROL 4,2 ; 64
490 ! INVERSES THE LOGIC ON THE
    FLAG LINE THIS ONE IS CONNEC
    TED TO THE GROUND
500 CONTROL 4,4 ; 192
510 ! TURN OFF HANDSHAKE PROCEDU
    RE.
520 CONTROL 4,5 ; 0+4
530 ! NO TRIGGER. PORT C IS OUTP
    UT
540 CONTROL 4,6 ; 0
550 ! STROBE PULSATION=0
560 CONTROL 4,9 ; 0
570 ! DO NOT OUTPUT INHIBIT
580 BEEP 10,500
590 DISP "MEASUREMENTS"
600 FOR P=1 TO 16
610 CLEAR
620 ! SWITHCHES DIODE OFF
630 ASSERT 4;0
640 V=B(P)
650 V=(V+12.5/512)/12.5
660 I=INT(V*255)
670 C$=DTB$(I)
680 DISP USING 710 ; A(P)
690 DISP USING 720 ; V*12.5
700 DISP USING 730 ; C$[9]
710 IMAGE "Operating Frequency="
    ,DD.D," Ghz"
720 IMAGE " Control voltage=",DD
    .DD," V"
730 IMAGE "Transmission Pattern=
    ",K
740 OUTPUT 404 USING "#,B" ; I
750 ! SWEEPER AT THE RIGHT FREQU
    ENCY
760 WAIT 100
770 GOSUB 1710
780 ! READ POWER COLD
790 ! J(P) POWER COLD IN DB
800 J(P)=Z(1)
810 ! SWITCH DIODE ON
820 ASSERT 4;2
830 WAIT 100
840 GOSUB 1710
850 ! READ POWER HOT
860 ! K(P) POWER HOT IN DB
870 K(P)=Z(1)
880 ! SWITCH DIODE OFF
890 ASSERT 4;0
900 PRINT USING 280 ; A(P),J(P),
    K(P)
910 ! POWERS IN WATTS
920 J(P)=10^(.1*J(P))
930 K(P)=10^(.1*K(P))
940 ! L(P) T FET
950 ! M(P) G FET
```

```
960 ! N(P) G FET IN DB
970 M(P)=(K(P)-J(P))/(E(P)*I(P))
980 L(P)=E(P)/(K(P)/J(P)-1)-T-M(
    P)/M(P)
990 N(P)=10*LGT(ABS(M(P)))
1000 NEXT P
1010 OUTPUT 404 USING "#,B" ; 0
1020 ! SWEEPER AT CW FREQUENCY
1030 BEEP 1000,10
1040 CLEAR @ DISP "DATA REDUCTIO
     N"
1050 PRINT
1060 N1=-INF
1070 L1=INF
1080 ! SEARCH FOR GMAX TMIN
1090 FOR P=1 TO 16
1100 PRINT USING 1110 : A(P),N(P
     ),L(P)
1110 IMAGE "F=",DD.DD," Ghz G(dB
     )=",MDD.D,"  T=",DDDD
1120 IF N(P)>N1 THEN N1=N(P) @ N
     2=P
1130 IF L(P)<L1 THEN L1=L(P) @ L
     2=P.
1140 NEXT P
1150 PRINT
1160 PRINT
1170 PRINT USING 1190 ; N(N2),A(
     N2)
1180 PRINT USING 1200 ; L(L2),A(
     L2)
1190 IMAGE "Gain max=",MDD.D," f
     or F=",DD.DD," Ghz"
1200 IMAGE "    T min= ",DDDD," f
     or F=",DD.DD," Ghz"
1210 PRINT
1220 ! PLOT
1230 PEN 1
1240 GCLEAR
1250 SCALE 7.85,10.1,-100,1050
1260 XAXIS 0,.2,8,10
1270 YAXIS 8,100,0,1050
1280 FOR X=8 TO 10 STEP .4
1290 LDIR 0
1300 MOVE X-.035,-100
1310 LABEL VAL$(X)
1320 NEXT X
1330 FOR Y=0 TO 1000 STEP 100
1340 LDIR 0
1350 MOVE 7.85,Y-20
1360 LABEL VAL$(Y/100)
1370 NEXT Y
1380 FOR P=1 TO 16
1390 MOVE A(P),N(P)*100
1400 GOSUB 1640
1410 MOVE A(P),L(P)
1420 GOSUB 1680
1430 NEXT P
1440 PENUP
1450 PLOT A(1),100*N(1)
1460 FOR P=2 TO 16
1470 DRAW A(P),100*N(P)
1480 NEXT P
1490 LDIR 0
1500 LABEL " Gain"
1510 PENUP
1520 PLOT A(1),L(1)
1530 FOR P=2 TO 16
1540 DRAW A(P),L(P)
1550 NEXT P
1560 LABEL " Temp"
1570 COPY
1580 ASSIGN# 1 TO "PARAME"
1590 READ# 1 ; A$,B$,T1,T2,T4
1600 ASSIGN# 1 TO *
1610 IF A$="AUTO" THEN CHAIN "RU
     N-PR"
1620 BEEP
1630 END
1640 IMOVE -.0075,5
1650 IDRAW .015,0 @ IDRAW 0,-10
1660 IDRAW -.015,0 @ IDRAW 0,10
1670 RETURN
1680 IMOVE 0,7.5 @ IDRAW 0,-15
1690 IMOVE .012,7.5 @ IDRAW -.02
     3,0
1700 RETURN
1710 X$="9D+R"
1720 FOR I=1 TO 3
1730 OUTPUT 713 ;X$
1740 ENTER 713 ; V$
1750 Z(I)=VAL(V$[4])
1760 IF I<3 THEN WAIT 1000
1770 NEXT I
1780 IF (ABS(Z(1)-Z(2))<.02)*(AB
     S(Z(1)-Z(3))<.02)=0 THEN 17
     00
1790 Z(1)=(Z(1)+Z(2)+Z(3))/3
1800 RETURN
1810 ENABLE KBD 255
1820 ! SWITCHES DIODE OFF
1830 ASSERT 4;0
1840 ! SWEEPER AT CW
1850 OUTPUT 404 USING "#,B" ; 0
1860 DISP "   AUTHORIZED INTERRU
     PT"
1870 STOP
1880 END
```

F=	POC=	POH=
F= 3 1Ghz	POC= -.03	POH= 2 23
F= 8.2Ghz	POC= - 13	POH= 2.12
F= 3.3Ghz	POC= - 41	POH= 1 88
F= 8 4Ghz	POC= -.52	POH= 1.82
F= 3 5Ghz	POC= -.66	POH= 1 79
F= 8.6Ghz	POC= -.75	POH= 1 79
F= 3 7Ghz	POC= -.82	POH= 1 79
F= 8.8Ghz	POC= - 68	POH= 1.89
F= 8.9Ghz	POC= -.73	POH= 1.87
F= 9 0Ghz	POC= -.81	POH= 1 84
F= 9.1Ghz	POC= -.86	POH= 1 97
F= 9.2Ghz	POC= -.72	POH= 1 94
F= 9.3Ghz	POC= - 78	POH= 1 83
F= 9.4Ghz	POC= -.72	POH= 1 85
F= 9 5Ghz	POC= -.70	POH= 1.79
F= 9.6Ghz	POC= -.64	POH= 1.76

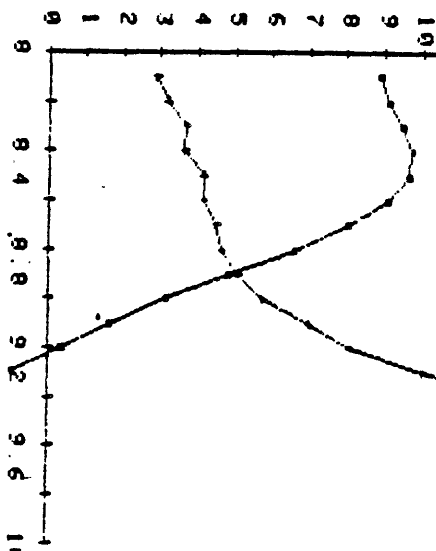
F=	T=	Gr=
F= 8.1	T=1009K	Gr= 76 28
F= 8 2	T=1061k	Gr= 71 76
F= 8 3	T=1110K	Gr= 64 85
F= 9.4	T=1035K	Gr= 66 37
F= 8.5	T= 981K	Gr= 67 43
F= 8.6	T= 880K	Gr= 71 81
F= 8.7	T= 853K	Gr= 72 31
F= 8 8	T= 849K	Gr= 74 89
F= 8 9	T= 826K	Gr= 75 55
F= 9.0	T= 788K	Gr= 76 79
F= 9.1	T= 757K	Gr= 79 13
F= 9.2	T= 777K	Gr= 79 15
F= 9.3	T= 805K	Gr= 76 11
F= 9 4	T= 831K	Gr= 75 47
F= 9.5	T= 868K	Gr= 73 34
F= 9 6	T= 997K	Gr= 66 94

TIME IS NOW 16-30-00

F=	POC=	POH=
F= 8.1Ghz	POC= 6.18	POH= 9 69
F= 8.2Ghz	POC= 6.37	POH= 9.86
F= 8.3Ghz	POC= 6.52	POH= 10.03
F= 8 4Ghz	POC= 6.84	POH= 10.32
F= 8 5Ghz	POC= 7 04	POH= 10 43
F= 8.6Ghz	POC= 6.77	POH= 10 96
F= 8.7Ghz	POC= 6.01	POH= 9 17
F= 8 8Ghz	POC= 5.09	POH= 8 05
F= 8.9Ghz	POC= 3 92	POH= 6 61
F= 9.0Ghz	POC= 2.96	POH= 5 34
F= 9 1Ghz	POC= 2.34	POH= 4.40
F= 9.2Ghz	POC= 1.95	POH= 3.70
F= 9.3Ghz	POC= 1.44	POH= 2.88
F= 9 4Ghz	POC= 1 15	POH= 2 29
F= 9 5Ghz	POC= .87	POH= 1 78
F= 9 6Ghz	POC= .73	POH= 1.46

F=	G(dB)=	T=
F= 8.10 Ghz	G(dB)= 8.9	T= 287
F= 8 20 Ghz	G(dB)= 9.1	T= 319
F= 8.30 Ghz	G(dB)= 9.[illegible]	T= 368
F= 8.40 Ghz	G(dB)= 9.7	T= 366
F= 8 50 Ghz	G(dB)= 9.7	T= 416
F= 8.60 Ghz	G(dB)= 9 1	T= 419
F= 8.70 Ghz	G(dB)= 8.0	T= 450
F= 8.80 Ghz	G(dB)= 6.6	T= 467
F= 8.90 Ghz	G(dB)= 4.9	T= 511
F= 9 00 Ghz	G(dB)= 3.2	T= 573
F= 9.10 Ghz	G(dB)= 1.7	T= 700
F= 9.20 Ghz	G(dB)= .4	T= 813
F= 9 30 Ghz	G(dB)= -1.0	T=1011
F= 9.40 Ghz	G(dB)= -2.4	T=1291
F= 9 50 Ghz	G(dB)= -3.6	T=1559
F= 9.60 Ghz	G(dB)= -4.7	T=2061

Gain max= 9.7 for F= 8 40 Ghz
T min= 287 for F= 8.10 Ghz



There are three main sources of error in this measurement system: error due to the system sensitivity, error in the measurement of power at the output of the receiver and error in the excess noise applied by the diode either to the receiver or to the amplifier.

The system sensitivity is determined by its standard deviation ΔT_{rms}

$$\Delta T_{rms} = T_{sys} / \sqrt{B\tau}$$

where τ is the time over which the powermeter averages the output signal. This error is very small (because of the large bandwidth of the receiver) of the order of 10^{-1}-$10^{-2}\,K$.

Error in the measurement of the power occurs because the power level at the detector (power sensor) is not a constant and is thus distorted by the non linearities of the detector. The manufacturer claims that the output power is measured within $\pm .02\,dB$ of its true value. This corresponds to an error of $\pm 4.6\,\mu W$.

The most important error in the system is the determination of the applied excess noise ratio. The effective cold temperature T_{cold} is the temperature of the room and is known within $\pm 1\,K$. The hot temperature T_{hot} is computed as

$$T_{hot} = T_{cold} + 290.10^{\frac{Exc. - Att.}{10}}$$

where Exc. is the calibrated excess noise of the diode and Att. the attenuation of the 10 dB placed in series with both expressed in decibels.

The manufacturer guaranties its calibration within $\pm .1\,dB$ of the true ENR. This yields a noise uncertainty of about $\pm 9.5\,K$. The variations of the diode source impedance when switched on and off, produce an error $e \approx 1 - (\Gamma_{on} + \Gamma_{off})^2$ equal to

$\pm .012\ dB$ (or $\pm\ 2.7\ K$). Finally, the calibration of the attenuator is performed with a finite precision of $\pm .02\ dB$ $(4.5\ K)$. Overall the hot temperature is known within $\pm 11\ K$.

At each frequency, three independent power measurements are performed to reduce random errors. This reduces the errors on T_R and kG_RB to $\Delta T_R = \pm 15\ K$ and $\Delta kG_RB = \pm 4.5.10^{-6}\ WK^{-1}$.

The error in the determination of G_{FET} and T_{FET} depends on the method used, on the noise temperature of the FET, and for a great part on its gain.

Method 1

	gain>3 dB	gain>7 dB
ΔT_{FET}	20 K	14 K
ΔG_{FET}	.07 dB	.07 dB

Method 2

	gain>3 dB	gain>7 dB
ΔT_{FET}	14 K	11 K
ΔG_{FET}	.07 dB	.06 dB

APPENDIX C3: LOSSES IN MATCHING NETWORK

Both input and output matching networks present losses which must be taken into account determinating the FET noise parameters.

The transducer gain of the FET (S_{21}^2) is large enough at the operating frequencies so that we disregard the effect of the second stage (ie, in that case of the output matching network) in determinating the FET noise temperature. Of course, there is no correction to be done to compute the noise temperature of the amplifier.

Let us consider the gain α of the input matching network. α is less than one since this network is purely passive. Expressed as a function of its scattering parameters and of the generator reflexion coefficient Γ_g in the 50 Ω system (see figure C3.1), one has

$$\alpha = \frac{|S_{21}|^2 \left(1 - |\Gamma_g|^2\right)}{\left(1 - |\Gamma_2|^2\right) \cdot |1 - S_{11} \cdot \Gamma_g|^2}$$

The case of the perfectly matched generator yields

$$\alpha = \frac{|S_{21}|^2}{1 - |S_{22}|^2} \qquad \Gamma_g = 0$$

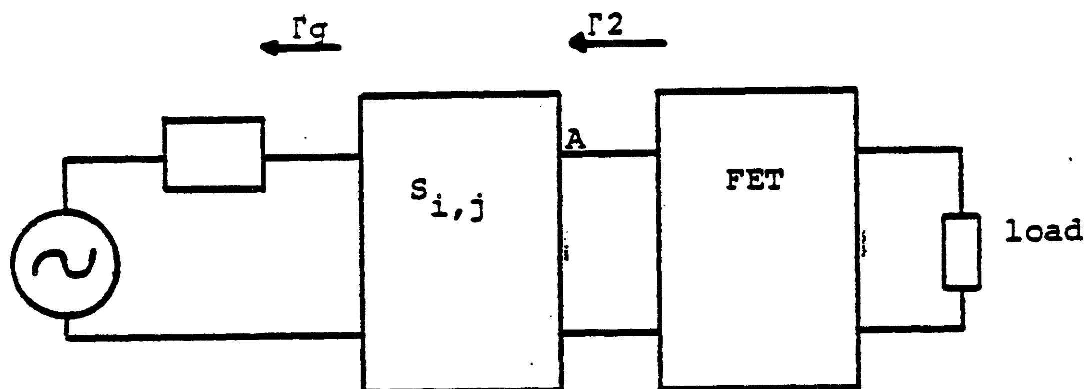


*Figure C*3.1

Geometry

Although it is impossible to have a rigorous Γ_g equal to 0, the inclusion of the amplifier's input connector in the matching network results in the application of the above formula without the introduction of a significant error.

Let us now consider the noise power at the output of the input network (point A in the figure C3.1). The noise power available at the output of the input network is the sum of two terms: The noise power of the generator impedance (or of the noise diode when one measures the Y-factor) multiplied by the gain of the network and the noise generated by the network itself. Let us call T_Φ the network physical temperature, T_S the noise temperature of the generator impedance and $\bar{T}$ the resulting input noise temperature. The noise generator by the the network itself is proportional to T_Φ. Let us find the proportionality constant. We have

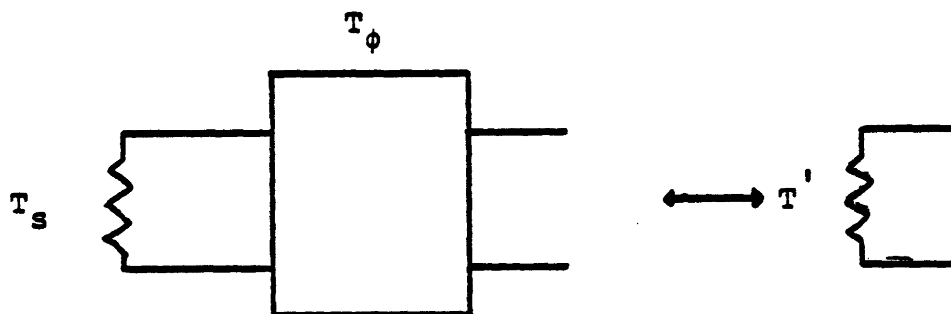


Figure C3.2

Equivalent Noise temperature

$$\bar{T}=\alpha\left(\Gamma_g\right)T_S+\beta T_\Phi$$

If both source and network are at the same physical temperature, we are in equilibrium. In such a case, we have $\bar{T}=\left(\alpha+\beta\right)T_\Phi$. Since we are at equilibrium, the available noise power is of the form $kT_\Phi B$ and is therefore independent of the variation of α with the value of the generator impedance. This gives us the value of β

$$\beta=1-\alpha$$

thus

$$\bar{T}=\alpha T_S+\left(1-\alpha\right)T_\Phi$$

If we note with a bar the effective noise temperature we drive the FET with, we have

$$\bar{T}_{Cold}=\alpha T_{Cold}+\left(1-\alpha\right)T_\Phi$$
$$\bar{T}_{Hot}=\alpha T_{Hot}+\left(1-\alpha\right)T_\Phi$$

The Y-factor we measure is in fact

$$Y = \frac{\bar{T}_{Hot} + \bar{T}_{FET}}{\bar{T}_{Cold} + \bar{T}_{FET}}$$

and

$$\bar{T}_{FET} = \alpha T_{FET} + \left(1 - \alpha\right) T_{\Phi} \qquad \alpha \leq 1$$

The measurements of S_{21} and S_{22} necessary for this correction were performed using the experimental board described in section IV 2.1.