Fabrication and Simulation of CMOS-compatible Photodiodes

by

Nicole Ann DiLello

B.S.E. Electrical Engineering, Princeton University, 2005

Submitted to the Department of Electrical Engineering and Computer Science
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Abstract

CMOS-compatible photodiodes are becoming increasinging important devices to study because of their application in combined electronic-photonic systems. They are already used as inexpensive optical transceivers in fiber optic telecommunications systems and they have the potential to be integrated in a number of applications.

This thesis focuses on germanium photodiodes to be used in an integrated electronic-photonic analog-to-digital converter. It specifically studies the dark current, responsivity, and frequency response of Ge-on-Si LPCVD-grown diodes that will be used in such a system. It outlines a process that can be used to add metal contacts to pre-existing diodes and discusses characterization procedure.

It was found that previously fabricated 50 μm square diodes had leakage current of 0.25 μA at -1 V, but responsivity of $\sim$5 mA/W. Diodes with higher leakage current, 1.1 μA at -1 V, had a higher responsivity of $\sim$0.5 A/W. Spreading resistance profiles (SRP) indicate that better control of the n-type contact is needed to systematically reproduce these results. Furthermore, spreading resistance analysis demonstrated that elimination of the p-type seed during growth will result in a more abrupt junction, for which simulations predict an improved frequency response.

Simulations indicate that removal of the p-type seed and associated autodoping should increase the frequency response from $\sim$1.6 GHz to $\sim$14 GHz. Better control of the n-type profile can further increase the frequency response from $\sim$14 GHz to $\sim$27 GHz.

Thesis Supervisor: Judy L. Hoyt
Title: Professor

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This thesis would not have been possible without the help and support of many people, most of whom I'll thank here, some of whom I'll inevitably forget.

First and foremost, I must thank my advisor, Professor Judy Hoyt. Her enthusiasm and support for this project is neverending. Her demand of excellence inspires her students to produce the best work possible.

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wedding planning over the last few months has been a great source of support.

I must especially thank Tim for his advice, support, and editing expertise. He is responsible for this thesis looking professional and sounding coherent.

This thesis would not have been possible without the frequent intake of coffee. In that vain, I'd like to thank Dunkin' Donuts, Starbucks, and the residents of 345 Broadway for providing me with many cups of that wonderful elixir.

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Chapter 1

Introduction to Photodiodes and Goals of This Work

1.1 Introduction

Photodiodes, or diodes that produce current when illuminated, are becoming increasingly important for a variety of applications, most notably as photodetectors in telecommunications systems. Photodiodes are also a possible candidate for use in integrated photonic-electronic integrated circuits.

Telecommunications systems currently use photonic networks to transmit data in the near infrared range over significant distances. With the explosion of high speed internet as well as the installation of fiber connections to individual buildings, there is a growing need for inexpensive optical transceivers [1]. Germanium is emerging as an attractive material for these transceivers because of its strong absorption at the wavelengths of interest (1.2 - 1.55 μm) and also because of its relative ease of integration in existing silicon technology.

The development of low-leakage, high-bandwidth, high-responsivity germanium photodetectors has opened the door for a whole new range of applications. There is significant interest in fabricating electronic-photonic integrated circuits to exploit the advantages of optics and electronics on a single chip. This thesis discusses the fabrication and characterization of germanium photodiodes for use in an analog-to-

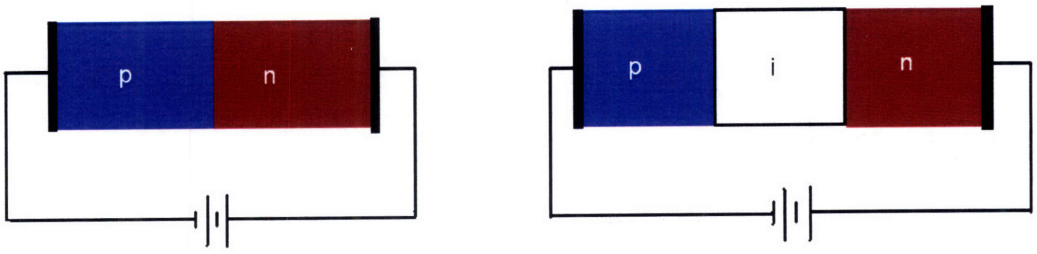

Figure 1-1: **Schematic diagrams of (a) a *pn*-junction and (b) a *pin*-junction.**

digital converter (ADC) that uses a mode-locked laser as its sampling source.

1.2 Physics of Photodiodes

Semiconductor photodiodes are generally fabricated from standard *pn*-junctions or *pin*-junctions (figure 1-1). Upon illumination with an energy greater than or equal to the bandgap of the material, electron-hole pairs are generated resulting in current flow.

In the *pn*-junction diode case, the total current in the device can be expressed as [2]:

$$I = I_0(e^{qV/kT} - 1) - qAG_0(L_p + L_n) \tag{1.1}$$

where the first term is the diode dark current and the second term is the current due to the light. In the above equation, q is the charge of an electron, A is the cross-sectional area, G_0 is the optical carrier generation rate in steady state, L_p is the diffusion length for holes, and L_n is the diffusion length for electrons.

The expression demonstrates that only those carriers generated within a diffusion length of the depletion region contribute to the current. These carriers reach the depletion region, are swept across by the high field, and reach the other side. Carriers generated beyond a diffusion length from the depletion region recombine before they reach the high field region.

The responsivity of a photodiode is defined as

$$R = \frac{I_{photo}}{P_{optical}} \tag{1.2}$$

As indicated by the above expressions, the responsivity of a *pn*-junction diode is limited by the relatively short diffusion lengths of the carriers. Inserting an intrinsic layer to create a *pin*-junction diode is a common method used to increase responsivity.

In a properly designed *pin* diode, the entire intrinsic region is depleted. Any carriers generated in the intrinsic (depleted) region or within a diffusion length on either side will be swept across the junction and collected on the opposite side, assuming negligible recombination of photogenerated carriers in the space charge region. The intrinsic layer in *pin*-photodiodes is usually $\sim$1 μm wide, thus providing ample space in which to generate carriers.

1.3 Germanium Photodiodes

1.3.1 Advantages of Germanium

Germanium is an attractive candidate for photodiodes for several reasons. First, germanium is easily integrated with silicon processing. Photodiodes are commonly used as interconnects between photonic and electronic systems. These could be large-scale systems, like the telecommunications system, or micro-scale existing on the same chip. Silicon is the primary material used in these systems, making integration with silicon a key factor.

Secondly, current telecommunications photonic systems operate on wavelengths in the range of 1.2 - 1.55 μm. While silicon is transparent over this range, germanium has strong absorption (figure 1-2). Thus, silicon is often used to fabricate waveguides for transmitting data in these systems while another material, such as germanium, is necessary to fabricate photodetectors.

There are various III-V devices currently being used as efficient photodetectors with good responsivity and high bandwidth. However, it is very difficult to integrate

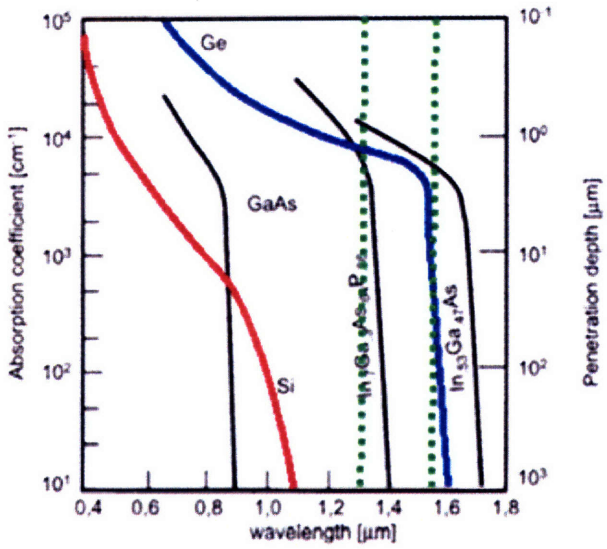

Figure 1-2: **Plot of absorption vs. wavelength for several semiconductors** From [3]

these materials on silicon substrates. Compared to III-V materials, germanium and SiGe alloys are relatively easy to grow on silicon as is discussed in the following sections. Coupled with its good absorption at the wavelengths of interest, Ge based detectors are encouraging materials to use in these photonic-electronic systems.

1.3.2 Disadvantages of Germanium

Despite the advantages discussed above, Ge-on-Si integrated devices remain difficult to fabricate. First, there is a 4% lattice mismatch between pure Ge and pure Si, creating significant stress in the Ge films. This stress is usually relaxed by misfit dislocations near the Ge/Si interface, with associated threading arms that penetrate up into the Ge film. Various techniques are used to reduce the threading dislocation density. However, these defects have adverse effects on the performance photodiode. Specifically, they typically lead to increased dark current. One way to reduce the density of dislocations in the active region of the diode is to use relaxed buffer layers where the percentage of Ge is increased slowly over a few microns of SiGe [4].

Another challenge when working with germanium is its lack of a good native oxide (similar to SiO_2 on Si). GeO_2 is water soluble. This makes GeO_2 difficult to

process and lends itself to poor performance [5]. Research into germanium-compatible dielectrics is currently underway; however, in this work, SiO_2 or SiON is used as the insulating material.

One final disadvantage of germanium is that it requires lower processing temperatures than silicon does. The melting point of germanium is 937°C [6] compared to 1410°C for silicon [7]. This means that after germanium deposition, processing temperatures must be kept low to avoid interdiffusion of silicon and germanium, and reduce impurity diffusion within the crystal.

1.4 Previous Work

The growth of high quality germanium on silicon is relatively simple compared to growth of III-V materials on silicon; however, it is far from trivial. Germanium films are grown by ultra-high vacuum chemical vapor deposition (UHVCVD) [8, 9, 10, 1], molecular beam epitaxy (MBE) [11, 12], or low pressure chemical vapor deposition (LPCVD) [13, 14, 15]. A wide range of growth conditions may be utilized. In the following paragraph, a brief description is given of processes typically used in CVD-deposition of Ge-on-Si.

For convenience in fabricating vertical *pin* diodes, the starting substrate is usually a $p+$ Si wafer. A silicon buffer layer may be grown on top of that. If not implementing a relaxed SiGe buffer layer, a low temperature (~350°C) germanium layer is then grown. The purpose of this low temperature layer is to produce a flat surface morphology (i.e. to suppress islanding) while relaxing the stress due to the lattice mismatch between Ge and Si. This low temperature layer allows the necessary strain relaxation without compromising the crystal quality of the subsequent layers. The next layer is a thick (~1 μm) layer of intrinsic germanium grown at a higher temperature, usually around 600°C. A cyclic anneal is typically performed to minimize the dislocations in the crystal. An $n+$ layer of Ge is realized by implanting with an n-type dopant, usually phosphorus. PiN mesa diodes are formed using standard wet etching and photolithography (figure 1-3).

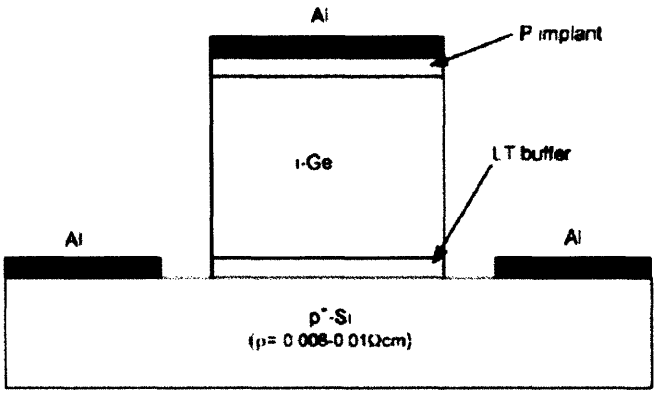

Figure 1-3: **Schematic diagram of *pin* mesa diode.** Sketch is from [4] and illustrates a diode grown using UHVCVD.

1.4.1 Electrical and Optical Characteristics

The characterization of Ge on Si photodetectors typically involves studying three figures of merit. First, the diodes must exhibit low leakage current in the off state, or dark current, in order to limit power consumption and increase the signal-to-noise ratio. The diodes must also have high responsivity when illuminated. Finally, since the detectors are often used in high-speed applications, they must have a high 3-dB frequency, typically ~10 GHz or higher.

Previous work has mainly focused on only one of these parameters to the detriment of the other two. Oehme *et al.* demonstrated photodiodes fabricated using molecular beam epitaxy showing excellent 3-dB frequencies. At a reverse bias of 2 V and an incident wavelength of 1550 nm, the cutoff frequency was measured to be 39 GHz [12], among the highest 3-dB frequencies reported. However, the dark current for these devices at a bias of -1 V was 100 mA/cm^2, which is significantly higher than photodiodes fabricated using other growth systems.

Colace, *et al.* used a UHVCVD system to fabricate diodes. Samples that were thermally annealed yielded dark current densities of ~20 mA/cm^2. At 1550 nm, these diodes had a responsivity of 0.2 A/W and could operate at 10 Gbit/s [9]. Colace *et al.* had previously reported fabricating germanium photodetectors with cutoff frequencies of 2.5 GHz and responsivities ~0.75 A/W, which is among the

highest reported. These detectors also had a dark current of ~20 mA/cm^2 [8].

Samavedam, *et al.* grew a relaxed graded buffer layer before growing germanium films in a UHVCVD system. The relaxed graded buffer layer served to greatly reduce the threading dislocations in the germanium film, which dramatically reduced the dark current of these devices. These diodes had an off state leakage current of 0.15 mA/cm^2 at a reverse bias of 1 V. The reported responsivity at 1.3 μm was 0.133 A/W. This relatively low value was attributed to the thin depletion layer width (0.2 μm) utilized in those devices [10].

More recently, Loh *et al.* used an ultrathin (30 - 50 nm) buffer layer before growing a thick (~1 μm) Ge cap layer. This buffer layer greatly reduced the threading dislocations and yielded diodes that had dark current densities of 1.5 - 2 mA/cm^2. These diodes had a 3-dB frequency of >15 GHz. Similar to the relaxed buffer layers, though, these photodetectors had a poor responsivity of 0.037 A/W [16].

In conclusion, it appears that germanium films grown using MBE can produce diodes with high 3-dB frequencies (~39 GHz), but high leakage current (~100 mA/cm^2) as well. Films grown using UHVCVD can yield diodes with much lower leakage current, especially if the films are annealed or grown on top of a buffer layer. The lowest leakage current reported using a UHVCVD system was 0.15 mA/cm^2. The highest responsivity reported so far has been 0.75 A/W, grown using a UHVCVD system. However, these diodes had only a moderate 3-dB frequency and leakage current.

This thesis discusses diodes fabricated using a low-pressure CVD (LPCVD) system to grow germanium films. LPCVD systems are more common in industrial settings and, thus, more easily integrated in a CMOS process. However, it is still necessary to produce diodes with leakage current of ~1 mA/cm^2, a responsivity of ~0.5 A/W, and a 3-dB frequency of ~10 GHz.

1.5 Analog-to-digital Converter

This work focuses on the fabrication of an integrated electronic-photonic analog-to-digital converter. Replacing the electronic sampling pulses in a standard ADC with

optical sampling pulses from a mode-locked laser can greatly increase the sampling frequency of the ADC. Current ADCs which employ an electronic sampling pulse have a jitter that is limited to the 250 fs range while mode-locked lasers demonstrate timing jitters below 10 fs [13]. Thus, a move to an optical sampling source could give the system an order of magnitude improvement in speed. The incorporation of a mode-locked laser in an ADC requires that electronic-optical modulators, optical filters, and photodetectors are developed that can all be integrated on a single chip, preferably in a CMOS compatible process. This thesis is concerned with the design and fabrication of photodetectors that can be used in such an integrated electronic-photonic system.

A diagram of the proposed integrated electronic-photonic ADC can be seen in figure 1-4. The mode-locked laser emits very narrow pulses which are sent through a dispersive medium to fully cover the period. Then the input signal is modulated on top of the pulse in the electronic-optical modulator. The optical filters can then select individual wavelengths and the accompanying data. These parallel channels are then fed into photodetectors where the optical signal is converted back into an electronic signal. After the detectors, it is proposed that the system will use commercial ADCs to do standard electronic processing.

1.6 Goals of this Work

This work will first outline a new process that was developed at MIT to add metal contacts to pre-existing germanium diodes. The aim of this process is to metallize diodes that are on small pieces of a 6" wafer. The metal contacts will allow better characterization of the diodes, yielding more accurate measurements of leakage current and photoresponse. It will also allow high-speed measurements to be performed.

Next, the work will discuss the electrical and optical characterization of germanium diodes. It will analyze leakage current mechanisms mainly via I vs. V measurements and scanning electron microscopy.

Chapter 4 of this thesis will discuss some basic modelling of these diodes, using the

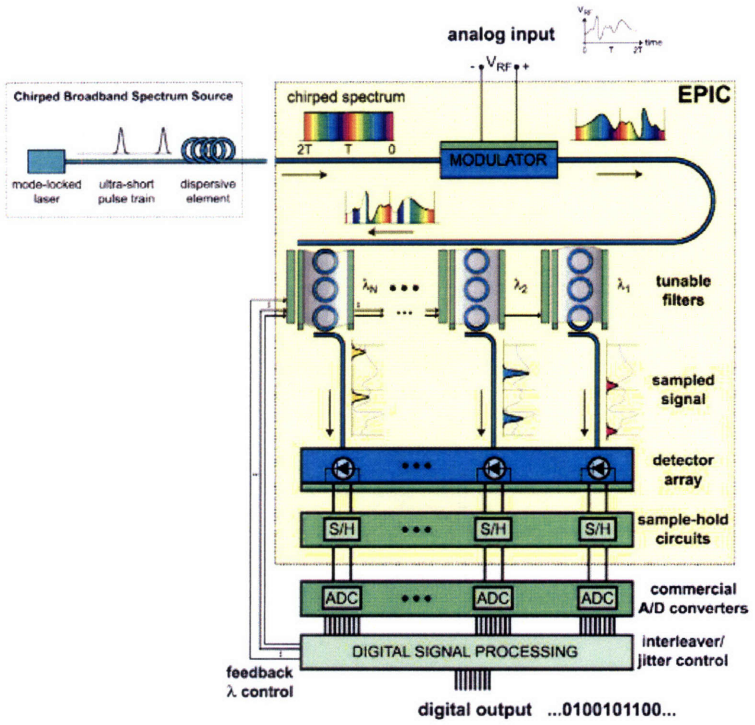

Figure 1-4: **Schematic overview of the integrated electronic-photonic ADC.** From [17].

Taurus Device platform. The aim of these simulations is to lend insight to improving the Ge diodes in future runs. These simulations investigate doping profiles and Ge film thickness in an attempt to make more effective diodes.

1.7 Chapter Summary

This chapter provides a brief introduction to the uses of photodiodes in current systems. The physics of generic photodiodes and the advantages and disadvantages of using germanium for these diodes was described. This chapter then described the previous work that has been done on the subject, first describing the growth process in MBE and UHVCVD systems. The electrical and optical properties of published germanium diodes were then summarized. Finally, the chapter described a potential application for such diodes, in an integrated electronic-photonic ADC.

Chapter 2

Fabrication of Germanium Photodetectors, Including New Metallization Process

This chapter discusses the fabrication of germanium photodetectors at MIT's Microsystems Technology Lab. These detectors were made as part of DARPA's Electronic Photonic Integrated Circuits (EPIC) program with the goal of creating an electronic-photonic analog-to-digital converter. The chapter will discuss the fabrication process and the problems that were faced in making the photodetectors.

2.1 Previous Work

2.1.1 Growth of Ge-on-Si Films

The growth of blanket Ge-on-Si films has been studied extensively in [13]. The effects of many factors on the growth and quality of the films are well documented there, but this section will summarize the important findings from that work.

Blanket germanium films were grown in a low-pressure chemical vapor deposition (LPCVD) epitaxial growth system. The starting substrates were six inch p-type CZ Si wafers with resistivities in the range of 0.005 - 0.02 Ω-cm. The effects of chamber

temperature, pressure, and hydrogen flow on the quality of the films were studied. It was found that a two-step growth procedure yielded the best results. The first step involved growing a low temperature $p+$ Ge seed layer. The optimum parameters for this layer were found to be 335°C at a pressure of 30 Torr with a hydrogen flow of 30 slpm. The layer must be at least 45 nm thick to yield a smooth surface morphology.

After seed layer growth, a thick ($\sim$2 μm) Ge cap layer was grown at a higher temperature. The temperature window for this step was determined to be 600°C - 700°C. At 650°C, chamber pressures between 30 Torr and 90 Torr yield smooth films. The hydrogen flow was kept at 30 slpm.

The films were cyclically annealed between 450°C and 830°C for 90 seconds and 150 seconds respectively. The samples went through 4 cycles of this anneal, all at a pressure of 30 T. For 320 μm square trenches, the dislocation density, determined by etching and optical microscopy, was $\sim$1 x 10^7 cm^2 and for 30 μm square trenches, the dislocation density was $\sim$4 x 10^6 cm^2.

2.1.2 Previous Fabrication of Germanium Photodiodes

Germanium photodiodes were created by Olumuyiwa Olubuyide from blanket Ge-on-Si films in MIT's Microsystems Technology Lab using standard CMOS processes and materials. After $\sim$1.7 μm of epitaxial Ge was grown on a $p+$ wafer, a 3000 $\AA$ layer of SiON was deposited using plasma enhanced chemical vapor deposition (PE-CVD). From there, the wafer was patterned and etched to open windows to the Ge film. A blanket layer of 2000 $\AA$ of poly-silicon was deposited on top of the wafer and then implanted with phosphorus. A subsequent anneal of the wafer diffused the phosphorus into the underlying Ge to create an $n+$ layer and complete the *pin* structure. The poly-Si was then patterned and etched to form contact pads. Contact to the $p+$ Ge was made through the substrate. The fabrication process is illustrated in figure 2-1. A more detailed discussion can be found in [13].

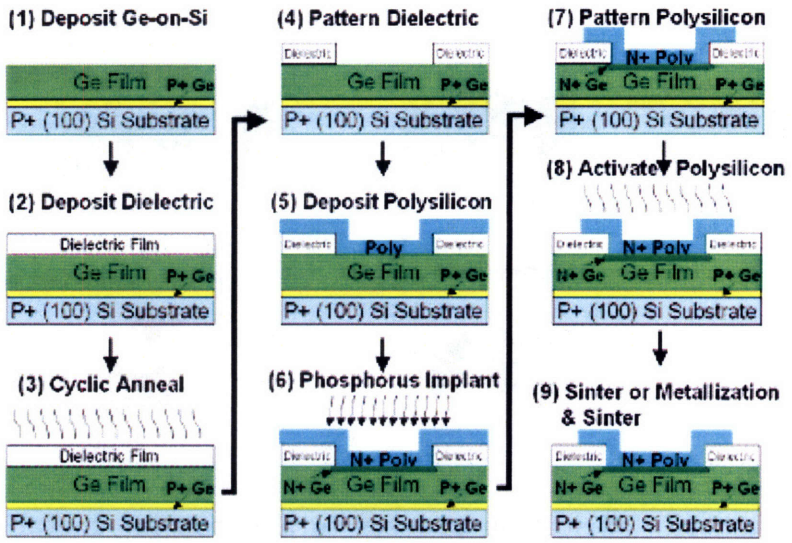

Figure 2-1: **Generic fabrication process for blanket Ge-on-Si *pin* photodiodes fabricated in [13].** Note that most diodes stopped before metal was deposited.

2.2 Metallization Process

As discussed previously, the high-speed applications envisioned for these diodes require them to have high bandwidths. Thus, an important figure of merit for these Ge photodiodes is their 3-dB frequency. In order to measure this, the devices need to have a contact to the $p+$ Ge on the topside of the wafer. This work discusses a new process developed to fabricate metal contacts to both the $p+$ and $n+$ portions of the diodes on the topside of the wafer. Some of the wafers fabricated in [13] were metallized, but many of them were cleaved before metal was deposited. Thus, it was necessary to develop a process that was compatible with smaller pieces of the wafer using a different tool set than the one used in [13].

This new fabrication process is detailed in figure 2-2. First, the substrate contact holes were patterned and etched. After that, oxide was deposited using PE-CVD. The oxide was then patterned and etched to create vias to the $p+$ substrate and the $n+$ poly-Si pad. Finally, titanium and aluminum were deposited and etched to create contact pads.

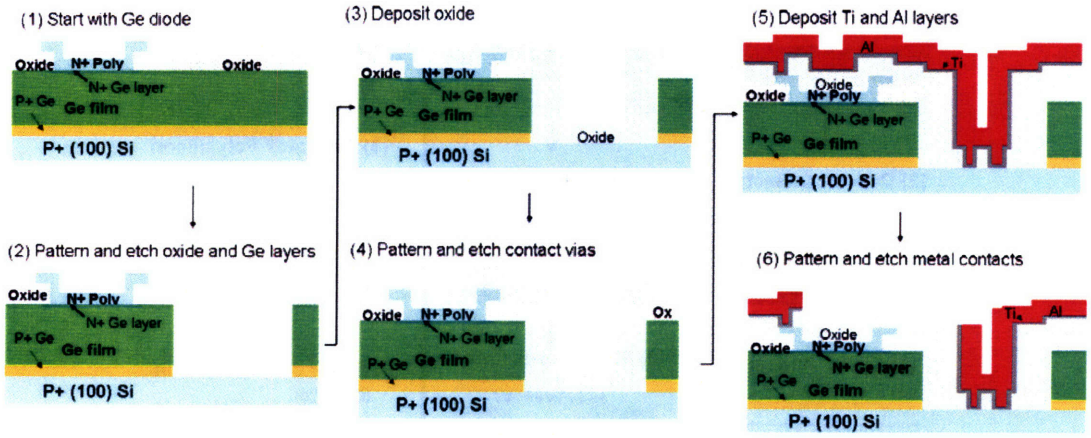

Figure 2-2: **Generic fabrication process to add topside metal contacts to both the n+ poly-Si and p+ Ge layer.** This process is different from that in [13] because of the different tool set available for processing small pieces of Si wafers.

2.2.1 Substrate Contact Etch

Initially, it was expected that a plasma etch would be suited to open holes through the SiON and Ge down to the $p+$ substrate. The SiON was etched using 40 sccm of CF_4 and 4 sccm of O_2 at a pressure of 10 mTorr and a power of 400 W. The Ge was etched using 40 sccm of Cl_2 and 20 sccm of Ar at a pressure of 10 mTorr and a power of 300 W. When implemented in the Plasmaquest in TRL, the etch yielded smooth, straight sidewalls. However, in order to etch through the germanium layer, the vacuum chuck was heated to 80°C. This increase in temperature caused part of the 1 μm layer of photoresist to become burned to the surface of the wafer. This thin layer of burned resist was impossible to remove with a standard O_2 plasma ash or a germanium RCA clean (see Appendix A for more details). The presence of this resist layer made further processing on those samples impossible and required a new etch to be used.

To replace the plasma etch, a series of wet etches was used. First a 7:1 buffered oxide etch (BOE) was performed to open windows through the SiON layer. Then the Ge was etched in a mixture of H2O:H_2O_2:HCl 4:3:1. This wet etch of the Ge layer caused a SiON overhang in the substrate contact holes, as shown in figure 2-3 This overhang caused a problem in subsequent processing because the oxide layer

Figure 2-3: **Cross-sectional Scanning Electron Microscopy (SEM) micrograph of the sample before the 2^{nd} BOE.** Underneath the resist there is a visible overhang of SiON that is approximately 4 μm long.

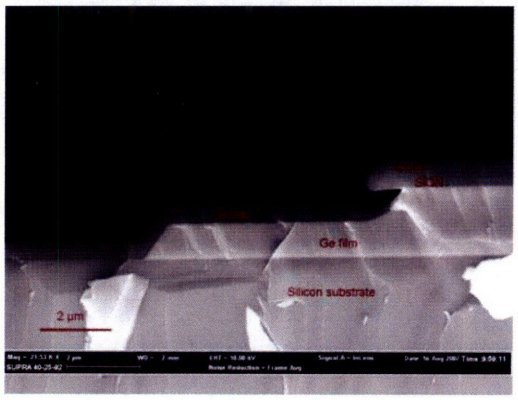

Figure 2-4: **Cross-sectional SEM of the sample after the 2^{nd} BOE with ultrasonic bath.** This sample also had ~500 nm of oxide deposited after the BOE. On the far right, there is a faint but clear distinction between the oxide and the SiON overhang.

could not cover the overhang without breaking. Thus, a second BOE was performed to eliminate this overhang and produce a smooth step. However, due to the small volume that the BOE had to enter, the samples were resistant to etching. To alleviate this problem, the samples were placed in an ultrasonic bath during part of the second BOE. A cross-section of the sample after the ultrasonic bath is shown in figure 2-4.

As figure 2-4 clearly shows, the BOE attacked the Ge layer significantly during the etch. Furthermore, while the etch seems to have eliminated the original overhang, it created a new overhang of SiON. This overhang created a problem when oxide was

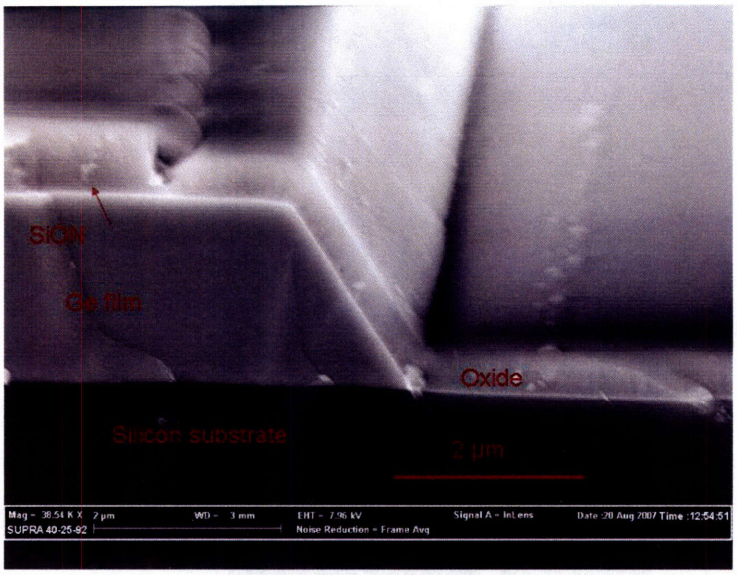

Figure 2-5: **Cross-sectional SEM of sample with successful wet etch.** Etch was 5 minutes in BOE, 15 minutes in 4:3:1 H_2O:H_2O_2:HCl, 5 minutes in BOE, 3 minutes in BOE with ultrasonic bath.

deposited on the sample, as it did not fully cover the Ge step.

In an attempt to eliminate the etching of Ge by the BOE, the length of the etch was dramatically shortened. The sample shown in figure 2-4 was etched for 14 minutes in BOE and then another 3 minutes in an ultrasonic bath. In the next experiment, the same series of etches was repeated, but the second BOE was 5 minutes without the aid of an ultrasonic bath, followed by 3 minutes in the bath. This etch successfully eliminated the SiON overhang and did not create a new one (figure 2-5).

As illustrated in figure 2-5, the overhang was eliminated and the deposited oxide layer successfully covered the SiON and Ge steps. With this etch procedure, the germanium film was electrically isolated by the oxide layer and was suitable for further processing.

2.2.2 Oxide and Metal Deposition

The next step in the processing was depositing PE-CVD oxide in the STS-CVD. It was expected that between 300 and 500 nm of oxide would cover the Ge step created by the etch. This oxide was then patterned and etched to create 4 μm square vias

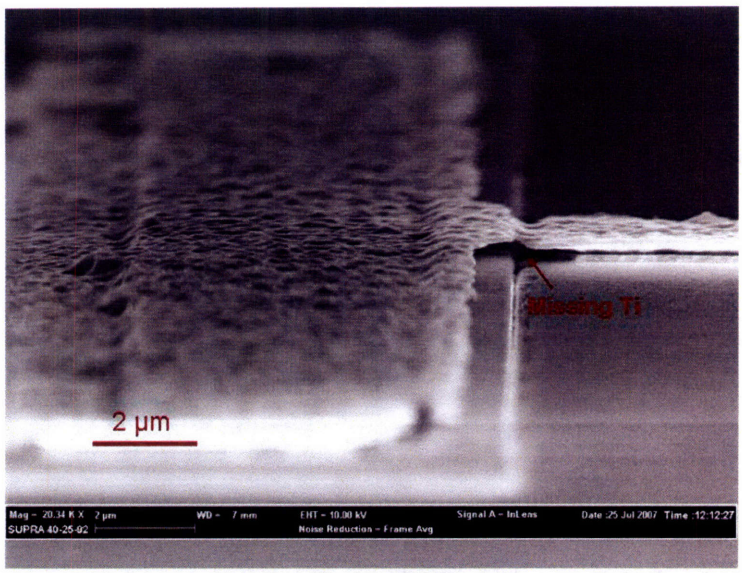

Figure 2-6: **Cross-sectional SEM of metal contact to the poly-Si layer.** The HF used to etch the Ti attacked the oxide around the poly-Si and helped create a void. The titanium layer is missing at the poly-Si step.

to the $p+$ substrate and the $n+$ poly-Si. The via etch was completed using a plasma etcher with the same parameters as the earlier SiON etch. The plasma etch created smooth sidewalls, making the subsequent processing significantly easier.

The final step in processing was the deposition and patterning of the metal stack. The stack consisted of 100 nm of titanium followed by 800 nm of aluminum. These metals were originally etched with a wet chemistry, but the HF used to etch the Ti did not stop on the underlying oxide layer. In fact, the oxide underneath the Ti etched quickly in HF, causing the formation of voids in the metal stack, especially over steps, as illustrated in figure 2-6.

To solve this problem, the Al was still etched with a wet chemistry, but the Ti was etched using a dry etch. Cl_2 plasma, which did not attack the STS-CVD oxide, was used to etch through the 100 nm of Ti. The use of a dry Ti etch kept the structural integrity of the metal stack over the steps, resulting in more structurally robust diodes.

Figures 2-7 and 2-8 illustrate the successful metallization process. Figure 2-7 shows a cross-section of the device through the substrate contact hole. This picture clearly

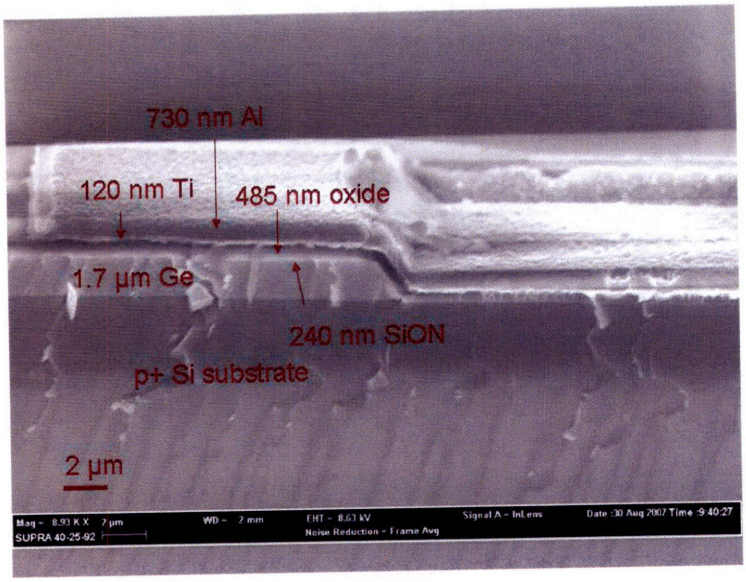

Figure 2-7: **Cross-sectional SEM of substrate contact hole.** Picture shows good step coverage of oxide and metal layers. Contact vias are not visible in this image.

illustrates the successful step coverage of the STS-CVD oxide and the successful deposition and etch of the metal layers. Figure 2-8 is an SEM of the metal contact to the poly-Si layer. This photo clearly shows the good step coverage of the metal layers over the poly-Si and dielectric steps.

2.3 Chapter Summary

This chapter first discussed the process that was used to fabricate germanium diodes. The process flow used by Olubuyide to fabricate Ge diodes was briefly discussed and then a process that would produce metal contacts on existing diode structures was outlined. The hurdles faced at each step were discussed and solutions were detailed. A process was developed that included a dry etch of the SiON film and a wet etch of the Ge cap layer to reach the Si substrate. Furthermore, a dry etch was used to etch the contact vias. 100 nm of Ti and 800 nm of Al comprise the metal contacts to both the poly-Si and the substrate.

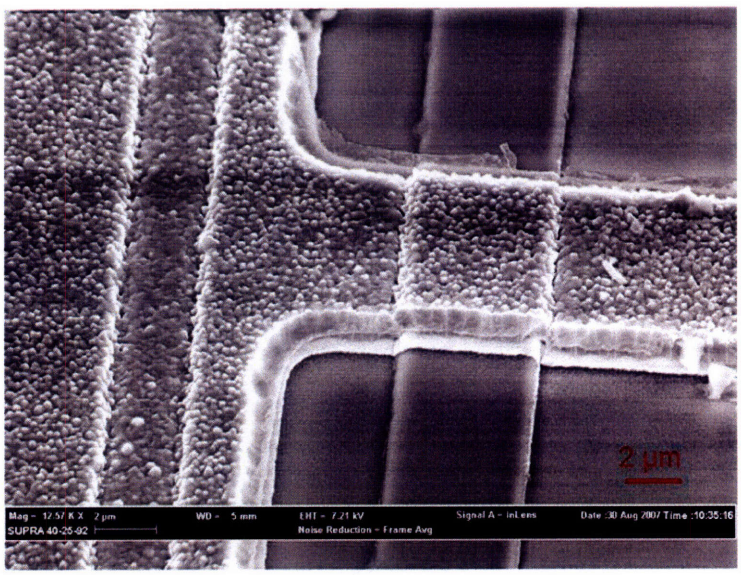

Figure 2-8: **SEM of successful metal contact to the poly-Si layer.** The metal shows good coverage over all steps.

Chapter 3

Electrical Characteristics of Germanium Photodetectors

This chapter discusses electrical characteristics of the germanium photodetectors that were fabricated in MIT's Microsystems Technology Lab. First, the leakage current of some diodes that were fabricated previously is discussed. The area and perimeter dependencies of these diodes are analyzed. Analysis of non-rectifying diodes is also performed to better understand the failure mechanisms.

3.1 Electrical Characteristics of Good Diodes

One of the most important figures of merit for these germanium detectors is dark current. To reduce power consumption and improve the signal-to-noise ratio, it is imperative that these diodes have a low-leakage current in reverse bias, typically measured at -1 V. The previous fabrication of these diodes resulted in the creation of two lots that showed low leakage current. As part of this thesis, a large number of diodes were measured on both samples, and the results are described in this section. Representative I-V curves of these two lots are shown in figure 3-1.

We can see from figure 3-1 that one of the lots had I-V curves that scale with the area of the device while the other lot had I-V curves that scaled with the perimeter

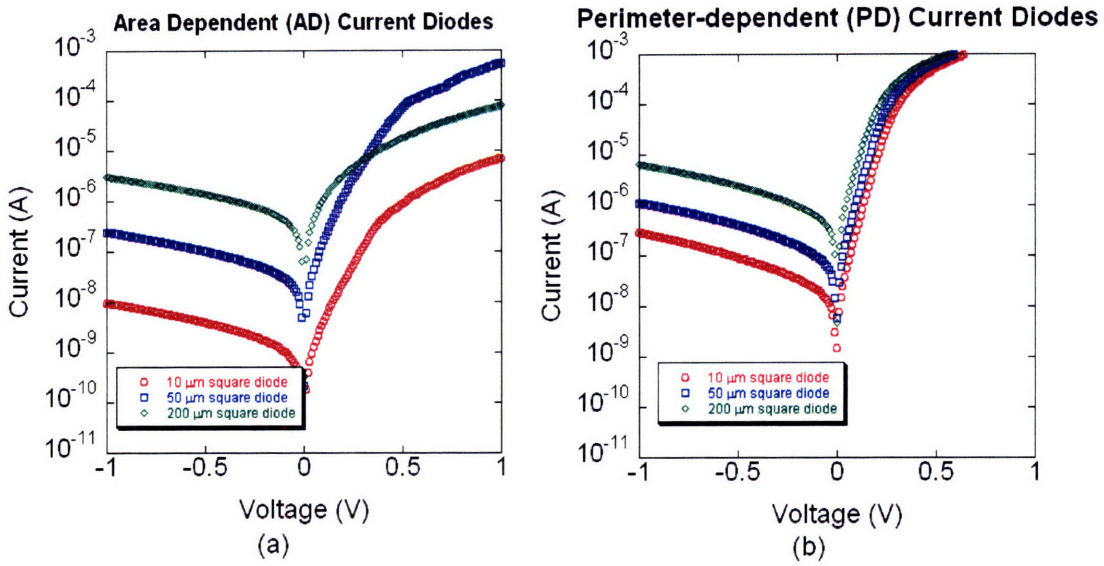

Figure 3-1: **I-V curves for diodes of various sizes.** Area dependent curves are shown in (a) while perimeter dependent curves are shown in (b).

of the device. We call these two lots area dependent (AD) and perimeter dependent (PD) respectively. For further analysis in this section, it is important to note that the AD diodes were unmetallized while the PD diodes had metal contacts. For the purposes of this thesis, the AD diodes came from lot 20, wafer 12, while the PD diodes were from lot 11, wafer 8.

At -1 V, the 50 μm square AD diodes had a leakage current of $\sim$10 mA/cm^2 while the 50 μm square PD diodes had a leakage current of $\sim$45 mA/cm^2. To further investigate the area and perimeter dependencies, the dark currents were plotted in another fashion. By plotting the dark current density at a specific voltage against a ratio of the diode perimeter over the diode area, such as in figure 3-2, the data can be fit to a simple model which incorporates the area and perimeter dependencies of the leakage current.

We can express the diode current with the following equation:

$$I_D = J_P(V) * Perimeter + J_A(V) * Area \tag{3.1}$$

If we divide each term by the area of the diode, the equation can be rearranged

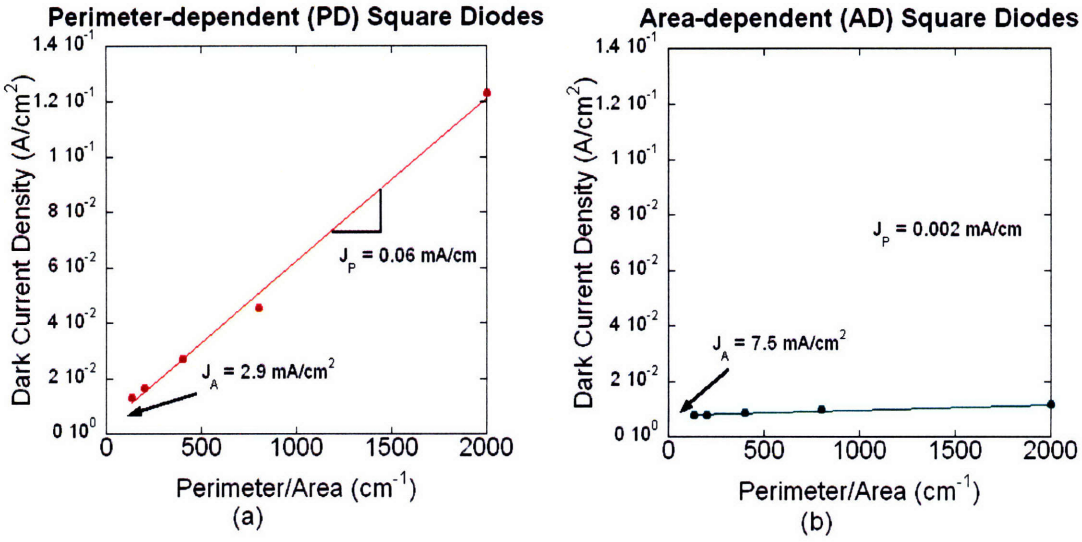

Figure 3-2: **Current density vs. perimeter/area ratio.** Perimeter dependent data is shown in (a) while area dependent data is shown in (b).

to be

$$J_D(V) = J_P(V) * \frac{Perimeter}{Area} + J_A(V) \tag{3.2}$$

where I_D is the total dark current, J_D is the dark current density, J_P is the coefficient of the perimeter current, and J_A is the coefficient of the area current. Thus, when J_D vs. $(Perimeter/Area)$ is plotted, J_P is the slope of the line and J_A is the y-intercept.

From the plots in figure 3-2, we can see that the PD diodes have a J_P value of 0.06 mA/cm and a J_A value of 2.9 mA/cm^2. Likewise, the AD diodes have a J_P value of 0.002 mA/cm and a J_A value of 7.5 mA/cm^2. Comparing the two lots, we see that the AD diodes have a J_A value that is $\sim$2.5 times larger than that of the PD diodes. More importantly, the PD diodes have a J_P value that is 30 times larger than that of the AD diodes. From this analysis, it is clear that the AD and PD diodes have comparable area dependence. Thus, it is evident that the main difference in leakage current is that the PD diodes have significant leakage current around the perimeter of the devices.

In an effort to reconcile the 2.5x difference in J_A values, the same analysis was

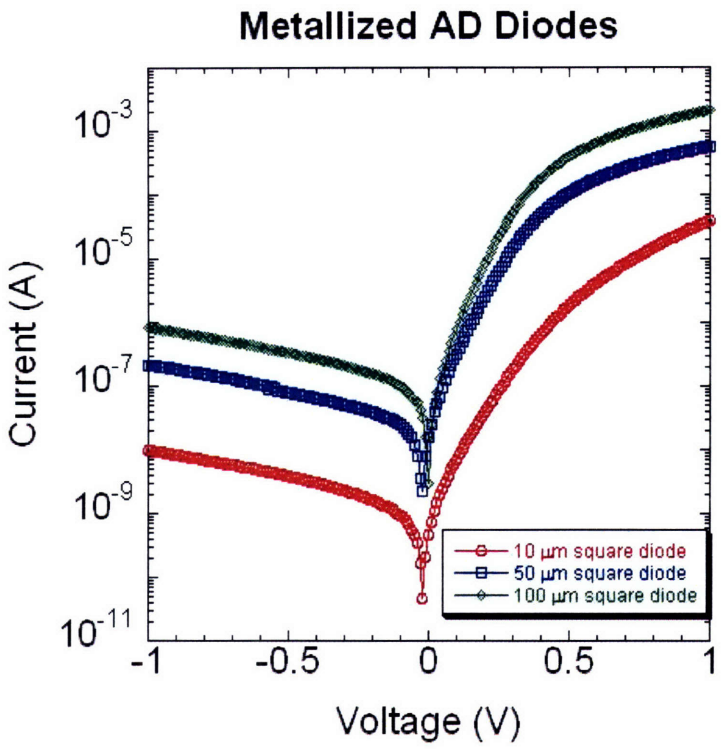

Figure 3-3: **I vs. V curves for metallized area dependent diodes.**

performed without the 20 μm square diodes (note that the 10 μm diodes are already excluded from the original analysis). It is hypothesized that these diodes are dominated by their perimeter-dependent leakage and their dark current values were skewing the analysis. Without the 20 μm diodes, the PD devices have a J_A of 6.7 mA/cm^2 while the J_P value remains fairly constant at 0.05 mA/cm. This new J_A value is within $\sim$10% of the J_A value for the AD diodes. Thus it is clear that the center portion of both types of diodes behave very similarly.

3.1.1 Results of Metallizaton Process

The metallization process that was described in chapter 2 was successful in making contact to the $n+$ poly-Si pads and the p-type substrate. Dark current measurements were performed on these devices to better characterize the AD photodiodes. Representative I vs. V curves for these metallized diodes can be seen in figure 3-3.

By comparing the plots in figure 3-3 with those in figure 3-1a, it is clear that the dark current is the same for both the metallized and unmetallized samples. It is difficult to get an accurate measurment of the series resistance of these diodes because the saturation current varies with reverse bias. However, if we assume that at V = 1 V, the current is dominated by series resistance, we can calculate that the series resistance of the 100 μm squares has decreased a great deal, from 11 kΩ to 143 Ω.

Photoresponse and frequency response measurements on these AD diodes can be seen in appendix B.

3.2 Electrical Characteristics of Non-Rectifying Diodes

Many diodes were fabricated that did not show well-behaved I-V characteristics such as the ones in figure 3-1. In fact, most of the diodes displayed I-V curves that resembled the plot in figure 3-4. Most commonly, these diodes do not show rectifying behavior.

In [13], it was hypothesized that the cause of the perimeter dependence in some diodes was a Si-Ge interaction that was more prominent along the perimeter of the diode. This Si-Ge interaction could have led to traps or some other mechanism that would increase leakage current. This interaction could have been induced during the fabrication of the diodes. This hypothesis is supported by cross-sectional SEMs that clearly indicate small nodules along the Ge-Si border. In the perimeter dependent diodes, these nodules extend underneath the adjacent dielectric whereas in the area dependent diodes, these nodules are just in the active area of the diode.

In this thesis, cross-sectional SEMs were taken of the non-rectifying diodes in an attempt to understand why they failed. Figure 3-5 is an image of the active area of the diode, where the poly-Si meets the Ge.

It is clear from figure 3-5 that there are Si-Ge nodules that extend far under the field dielectric. Furthermore, the interface between the dielectric and the germanium is quite poor, displaying some dark region in between the two materials. An early

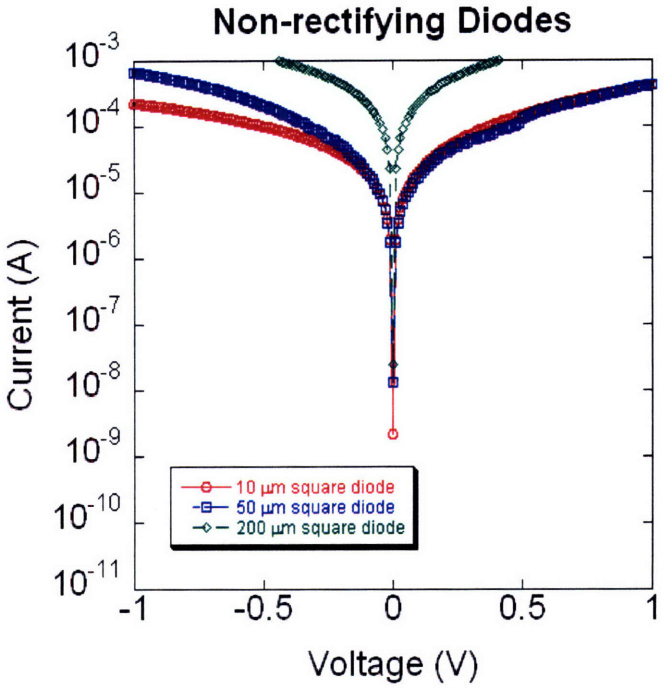

Figure 3-4: **I vs. V characteristics for typical non-rectifying diodes.** The I-V curves more closely resemble that of a typical resistor rather than a diode.

hypothesis is that the dark substance is a leftover residue from the dielectric etch. Windows were opened in the SiON dielectric using an initial dry etch and then a BOE at the very end. The BOE does not etch SiON particularly well and it may have left a nitride residue behind. A way to test this hypothesis is to change the SiON etch chemistry. Another possibility is that the BOE used to open the windows to the Ge attacked the Ge on some samples and etched laterally under the field dielectric. This exposed Ge surface intersects the *pn* junction and could be associated with shorting behavior. A possible solution is to etch the SiON in a mixture of 50:1 H_2O:HF. HF should not attack the underlyinng Ge film.

3.2.1 Spreading Resistance Profiling

Spreading resistance profiles (SRP) were taken on both the non-rectifying diodes and the low-leakage AD diode. The SRP analysis was done at Solecon Laboratories. The results were used to further interpret the I vs. V curves. Figure 3-6 shows the SRP

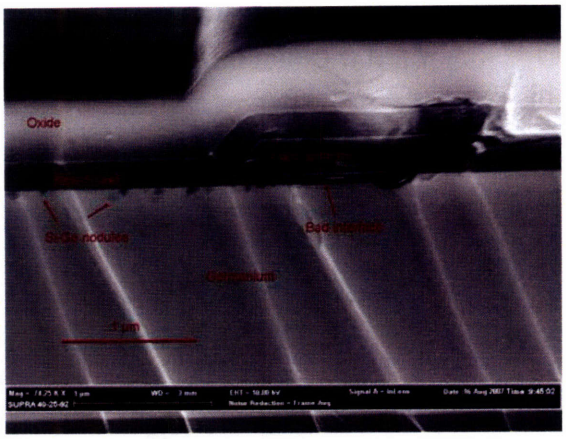

Figure 3-5: **Cross-sectional SEM of non-rectifying diode.** Diode is from lot 20, wafer 8.

results for the non-rectifying diodes while figure 3-7 shows the SRP results for the AD diodes.

The black lines in each figure indicate the poly-Si/Ge junction. The thickness of the poly-Si layers was confirmed by cross-sectional SEM. It is clear that in the non-rectifying diodes, the *pn* junction is not in the germanium film, but actually in the poly-Si layer or very close to the poly-Si/Ge interface. This might be expected to cause the diode to have very high leakage current, as the carrier lifetime in poly-Si is very short.

In contrast to the non-rectifying diodes, the *pn* junction in the PD diodes is fully in the Ge layer, as indicated by figure 3-7b. Figure 3-7a seems to indicate that the *pn* junction is in the poly-Si layer. If this were true, the leakage current of these diodes is expected to be much higher. Since the leakage current is quite low in the AD diodes, this discrepancy is perhaps due to SRP limitations. The SRP tools may not have been well calibrated for poly-Si or the Ge films.

More importantly, it is evident that the depth of the *pn* junction varies significantly from wafer to wafer. This junction is controlled by the out-diffusion parameters of phosphorus after poly-Si implant. The diffusion was performed in a rapid thermal processing (RTP) tool which can be difficult to control. The variation in temperature in this RTP tool can cause the depth of the junction to vary quite a bit.

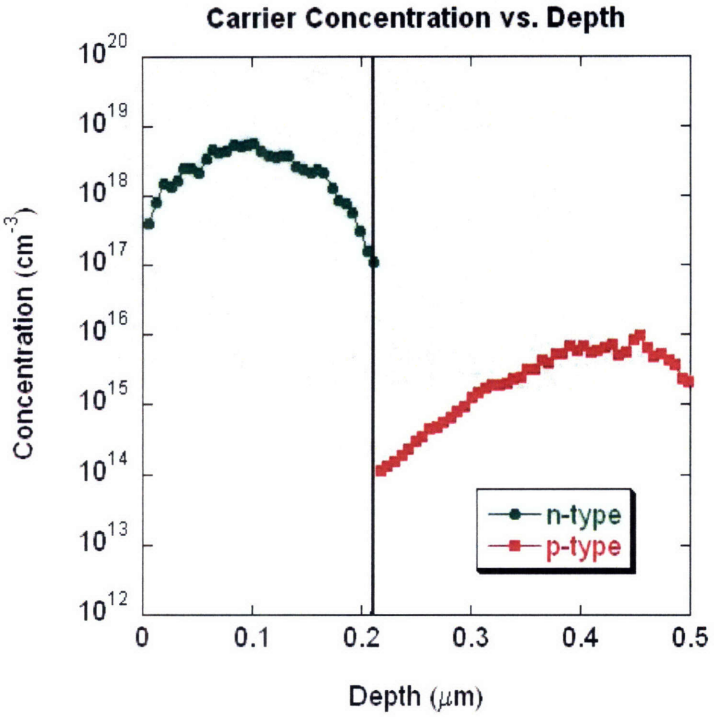

Figure 3-6: **SRP analysis of non-rectifying diode.** This plot shows the carrier concentration vs. depth for the initial 500 nm of the device. This diode was from lot 20, wafer 8. It is the same wafer that is imaged in figure 3-5. This sample was unmetallized.

To be able to repeatably make diodes with low leakague current, the *pn* junction must always be in the Ge film. Since the diffusion of carriers into the Ge is difficult to control in an RTP system, a better approach is to in-situ dope an *n*-type layer during growth. This would accurately control the junction depth from wafer to wafer. Another approach is to use a furnace anneal to out-diffuse the phosphorus from the polysilicon into the Ge. This will involve a certain thermal budget penalty, however, associated with furnace processing.

3.3 Chapter Summary

This chapter first discussed the perimeter and area dependencies of some low-leakage diodes. It was demonsrated that the differences in leakage mechanisms could be due to differences in Ge passivation layers. Then some possible reasons for the high-leakage

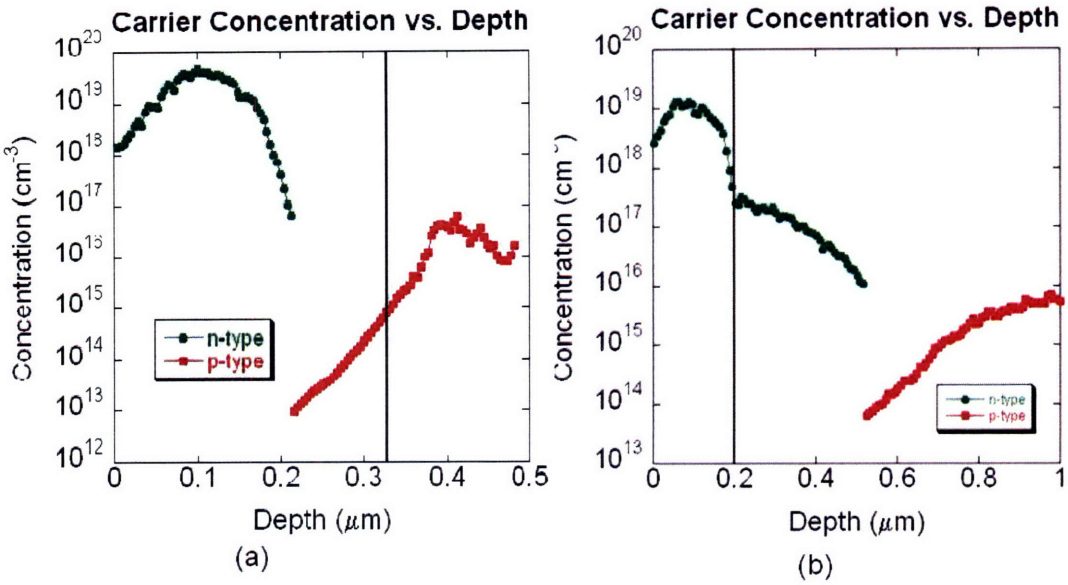

Figure 3-7: **SRP analysis of rectifying diodes.** This plot shows the carrier concentration vs. depth for the top ~500 nm - ~1 μm of the device. (a) is the profile of an AD diode while (b) is the profile of a PD diode as shown in [13]. The AD diode was unmetallized while the PD diode had metal contacts.

current observed in many diodes were discussed. SEM analysis demonstrated that this leakage current could be due to a poor poly-Si/Ge interface which is perhaps the result of the SiON etch chemistry. SRP analysis showed that the high leakage current could also be due to poor control of the *pn* junction. It indicates that the *n*-type carriers were not out-diffused well, forming a junction in the poly-Si layer.

Chapter 4

Simulation of Germanium Photodiodes

This chapter discusses simulations that were performed to gain a better physical understanding of the germanium photodiodes. The Taurus Device platform was used to simulate both DC and AC characteristics. This chapter will discuss the theoretical leakage current for these Ge diodes as well as the predicted responsivity at -1 V. Finally, it will discuss the 3-dB frequency for these diodes and postulate ways to improve their performance.

4.1 The Structure

The structure was designed in Taurus Device to emulate as best as possible the physical structure of the diodes fabricated by Olubuyide [13], within the constraints of a 2D simulation platform. The structures ranged in length (L) from 1 μm to 100 μm, and generally devices with L = 2 μm are studied in this chapter to save on computation time. The structure that was used in the simulations is shown in figure 4-1

The simulated structures start with a $p+$ Si wafer, doped at 2 x 10^{19} cm^{-3}. On top of this layer is a 60 nm thick $p+$ Ge seed layer doped at 2 x 10^{20} cm^{-3}. Then

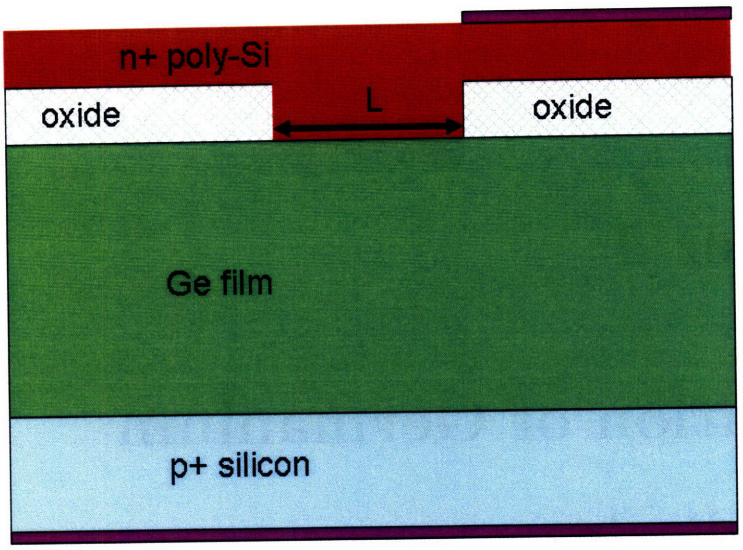

Figure 4-1: **Schematic diagram of structure used in simulations.** Ge-on-Si structure with poly-Si contacting the Ge region. The purple sections are ohmic contacts to both the p+ and n+ layers. Figure not to scale.

there is a 1.7 μm Ge cap layer that is doped to match the SRP analysis found in [13]. There is a 300 nm thick SiO_2 layer with a window that opens to the Ge cap. On top of the oxide is a 200 nm poly-Si layer that is doped n-type at 10^{19} cm^{-3}. The portion of the Ge cap that is exposed to the poly-Si has an n-type gaussian doping distribution that peaks at 2.5 x 10^{17} cm^{-3}. At a depth of 250 nm from the poly-Si interface, the doping concentration is 2 x 10^{16} cm^{-3}. The doping is also illustrated in figure 4-2. Finally, there are ohmic contacts placed on both the $p+$ Si layer and the $n+$ poly-Si layer.

When light is shined on the device, carriers are generated in the Ge layer. To best emulate the actual distribution of carriers, the light was blocked by a metal layer on the far left of the structure. This ensured that carriers were only generated in the active region - i.e. where the poly-Si meets the Ge. The optical generation rate under DC conditions is shown in figure 4-3.

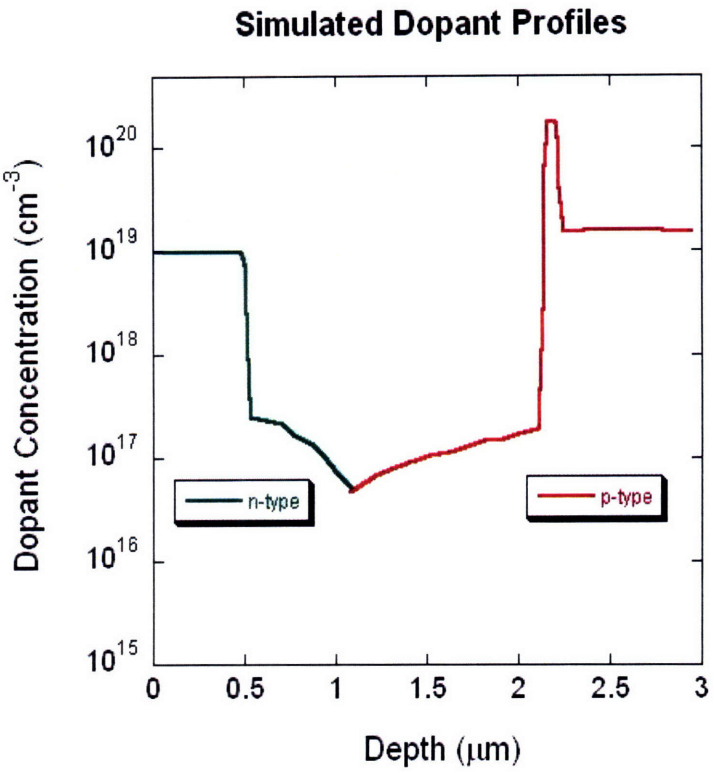

Figure 4-2: **Dopant concentration vs. depth for simulated structures.** Note the Gaussian distribution of n-type dopants and the presence of p-type dopants in the thick Ge cap.

4.1.1 Physical Models

To most accurately model the structure, various physical models were implemented in Taurus Device. The Chynoweth model was used for impact ionization. This model is better detailed in [18] and models effects like avalanche-induced breakdown of a junction. The Shockley-Read-Hall model for recombination is used with the default carrier lifetimes of germanium. The low field mobility model was concentration dependent and the high field mobility model took into account velocity saturation. Furthermore, Kane's model of band-to-band tunneling was included in the models. The generation rate of carriers can be given by [19]:

$$G = A\frac{E^2}{E_G^{1/2}}(e^{-B\frac{E_G^{3/2}}{E}}) \tag{4.1}$$

In this equation, A and B are constants, E_G is the bandgap and E is the magnitude

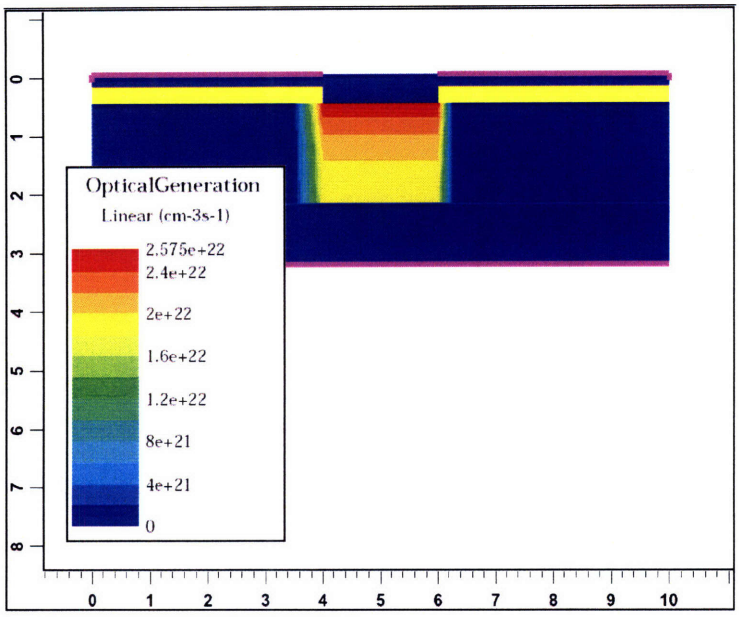

Figure 4-3: **2D plot of optical generation rate for simulated devices.** Carriers are only generated in the region under the poly-Si/Ge interface.

of the electric field. In the particular version used, E was the average field along the tunneling path.

4.2 Leakage Current

Initial simulations were run to investigate the dark current of these diodes. Figure 4-4 shows the I vs. V characteristic for a device that has L = 2 μm. At a reverse bias of 1 V, this device has a dark current of 230 pA or $\sim$1.2 mA/cm^2.

The simulated dark current density is on the same order of magnitude as the J_A values for both the PD and AD diodes discussed in chapter 3. The simulations indicate that a lower dark current density is possible for these diodes, but the previously fabricated diodes may be approaching the theoretical limit.

It is important to note that the shape of the curve in reverse bias differs greatly for the simulated and measured cases. In reverse bias, the simulated curve is very flat, as is expected in an ideal diode case. The measured diode (for example figure 3-3), however, shows leakage current which increases with reverse bias. It is hypothesized

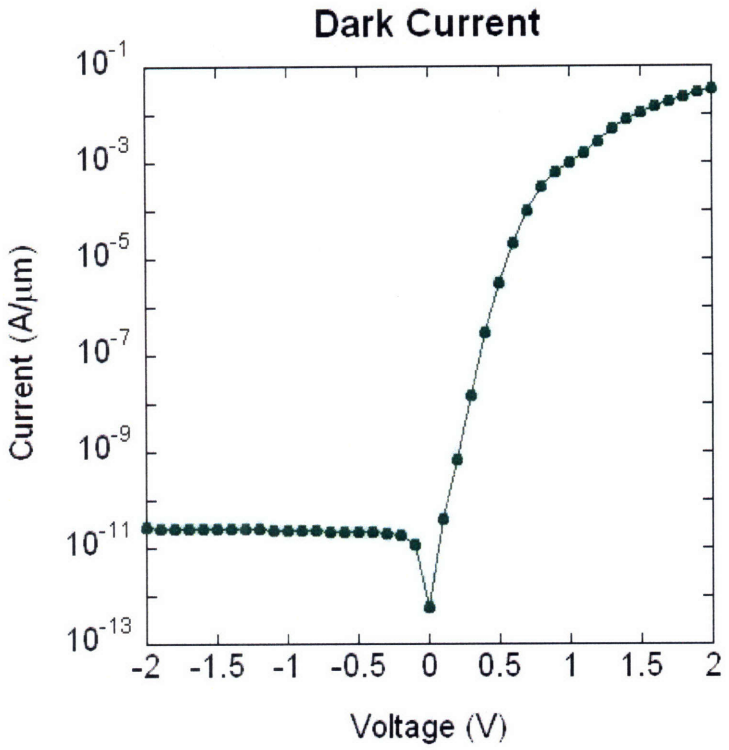

Figure 4-4: **Simulated dark current characteristic.** Device has L = 2 μm and a dark current density of $\sim$1.2 mA/cm^2 at -1 V.

that this leakage current is due to trap-assisted tunneling, which is not included in this model.

4.3 Responsivity

Next, simulations were run that investigated the photoresponse of these diodes. Taurus Device does not have accurate data for germanium's absorption constant at 1550 nm. According to [13] and [20] the absorption value of CVD-deposited Ge-on-Si is 5,000 cm^{-1}. This is slightly higher than that of bulk Ge ([21]) and is attributed to the residual strain in the Ge film.

Figure 4-5 shows the I vs. V characteristic for the same L = 2 μm device while illuminated with a wavelength of 1200 nm and an absorption constant of 5,000 cm^{-1}. (Note that since that absorption constant is set by the user, the wavelength of the light is irrelevant in the context of these Taurus simulations.)

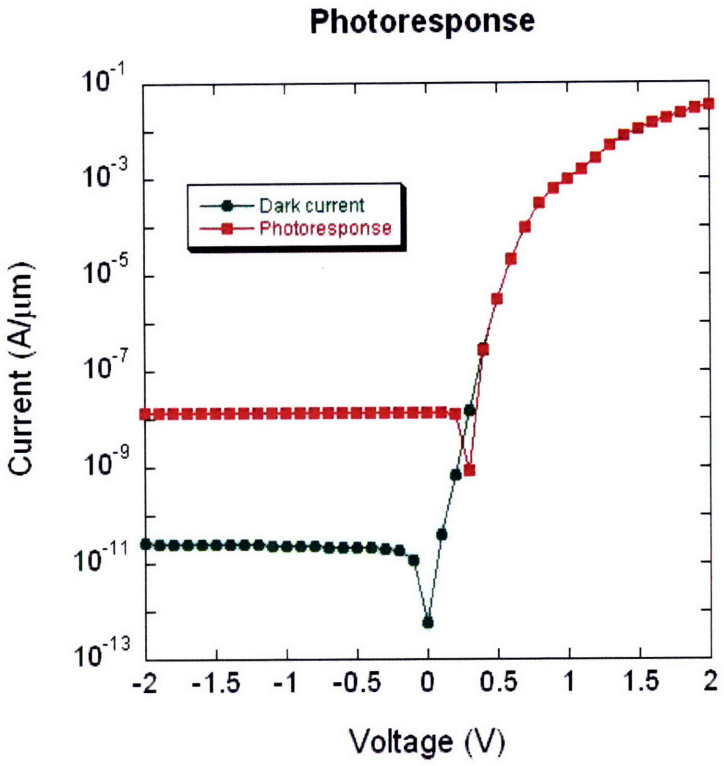

Figure 4-5: **Simulated photocurrent characteristic.** Device has L = 2 μm and a responsivity of ~0.68 A/W.

From these simulations, it is clear that the responsivity of these devices is 0.68 A/W. This responsivity is a bit higher than the responsivity value of 0.5 A/W measured by Olubuyide [13].

4.4 Frequency Response

An important figure of merit in these germanium diodes is a high cutoff frequency. Ideally, the EPIC project calls for a 3-dB frequency of 10 GHz. The perimeter dependent diodes were measured in [13] to calculate their cutoff frequency. A 20 x 100 μm diode was found to have a cutoff frequency of ~1.2 GHz at a bias of -5 V. It was postulated in [13] that idealities, such as traps, in the structure were causing such a low cutoff frequency. Simulations were performed in the present work to calculate the 3-dB frequency of an ideal diode - i.e., one without any traps.

The input parameters of these simulations were chosen to match the experimental

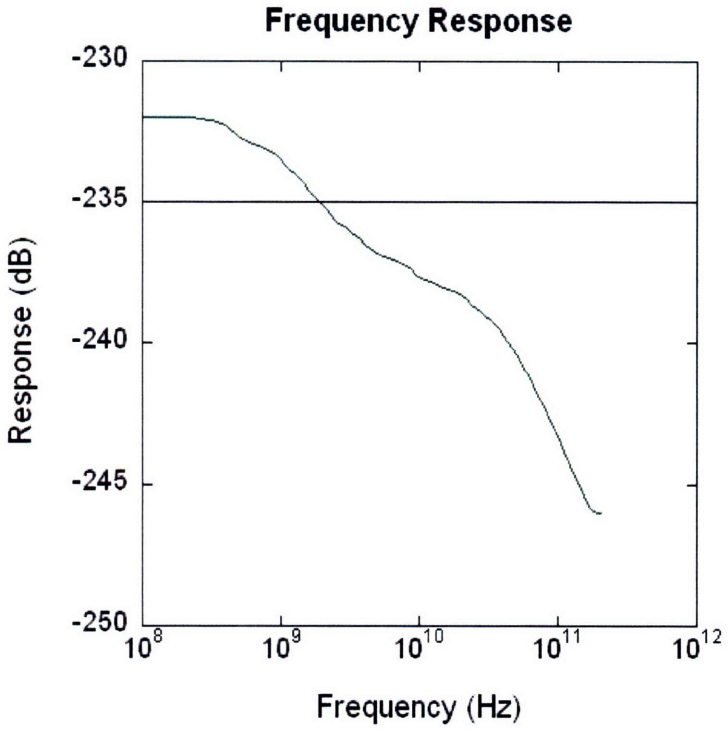

Figure 4-6: **Simulated frequency response.** Device has L = 2 μm and a 3-dB frequency of $\sim$1.6 GHz.

conditions that will be present in the final EPIC device. A 1 ps pulse of light at 1.55 μm was shined on the diode uniformly. Again, the absorption constant was set manually at 5,000 cm^{-1}. Taurus Device solved for the transient response of the diode and then calculated the Fast Fourier Transform (FFT) of the response. From there, the 3-dB frequencies were extracted. The frequency response of an L = 2 μm devices is shown in figure 4-6.

At -5 V, the simulated 3-dB frequency of this device is 1.6 GHz, as indicated by the dark horizontal line in the figure. While this number is close to what was measured on previously fabricated devices, it is nowhere near the 10 GHz that the EPIC project requires. Simulations were run on various structures to try to improve the response of these diodes.

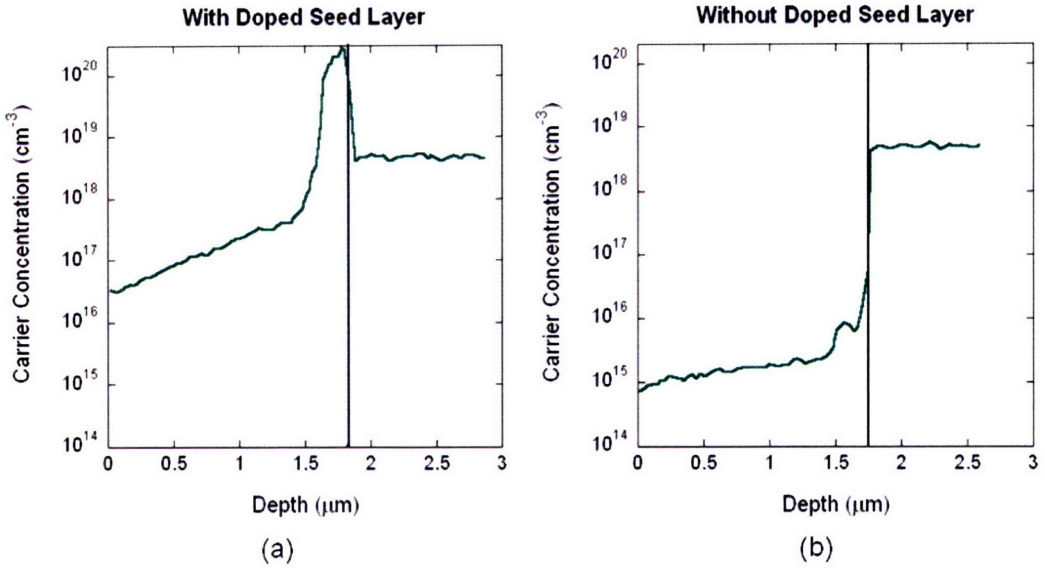

Figure 4-7: **Spreading resistance profiles of Ge-on-Si films grown (a) with $p+$ doping in the seed and (b) without $p+$ doping in the seed.** The source of the p-type doping appears to come from the presence of B_2H_6 during the seed growth. The black line in each figure indicates the Ge/Si interface.

4.5 Possible Improvements

While these Taurus Device simulations neglect the effect of traps, they can still help guide the future fabrication of these germanium diodes. SRP analysis of the actual diode samples show that the Ge cap layer is actually doped p-type when it was intended to be intrinsic. This will limit the frequency response of the device because it will take longer to sweep out the carriers, resulting in a lower cutoff frequency.

SRP analysis was run on blanket Ge-on-Si films to try to understand the origin of this p-type doping. It is clear from the SRP profiles in figure 4-7 that the Ge films are more intrinsic when the boron doping in the 60 nm-thick Ge seed is eliminated.

It is currently hypothesized that this $p+$ Ge seed is responsible for autodoping the subsequent Ge layer. Thus, even though the B_2H_6 gas is off during the Ge cap growth, the boron from the seed layer will move up as the germanium layer is deposited.

Simulations were run with the carrier profile from figure 4-7b and the 3-dB frequency was extracted. Figure 4-8 shows the frequency response of a 2 μm diode with

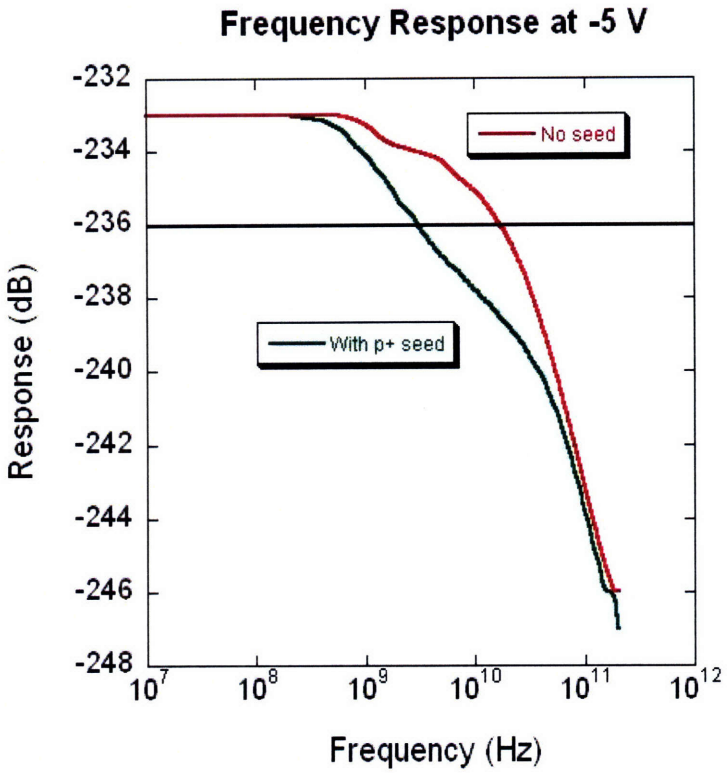

Figure 4-8: **Simulated frequency response of diodes with the spreading resistance profiles in 4-7.** The green line represents the structure with the $p+$ Ge seed and the red line represents the structure without a $p+$ seed. The black line marks the 3-dB point, indicating cutoff frequencies of 1.6 GHz (with $p+$ seed) and 14.1 GHz (without $p+$ seed).

both SRP profiles.

In figure 4-8, the curves were normalized to have the same frequency at 10 MHz for comparison purposes. The black line marks where the curves have fallen by 3 dB. As before, the structure with the $p+$ seed has a cutoff frequency of 1.6 GHz. Eliminating the seed layer results in a cutoff frequency of 14.1 GHz. This significant increase in cutoff frequency is attributed to a higher internal field in the device caused by the more abrupt doping profiles.

A further improvement is to better control the n-type doping profile. As discussed previously, the n-Ge contact is currently formed by diffusing out carriers from the poly-Si layer in a rapid thermal processing tool. This process is difficult to control and leads to unknown junction depths and broad n-type profiles. A better solution is

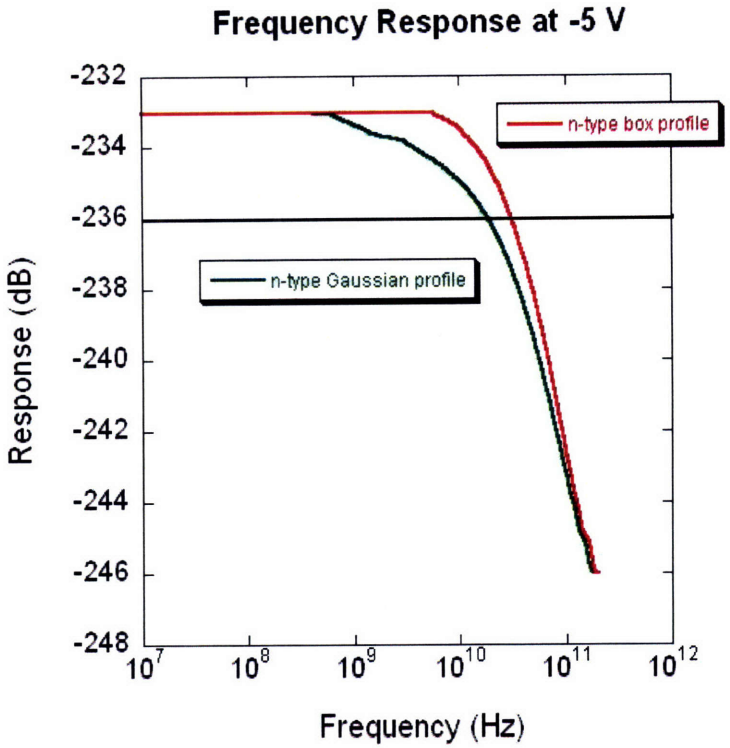

Figure 4-9: **Simulated frequency response of diodes a Gaussian *n*-type profile and a box *n*-type profile.** The black line marks the 3-dB point, indicating cutoff frequencies of 14.1 GHz (Gaussian profile) and 27.2 GHz (box profile).

to in-situ dope the n-type layer. This will allow better conrol over an abrupt junction.

Simulations were run to investigate the effects of a more abrupt n-type doping profile. The structure was kept the same except the top-most 100 nm of Ge was doped at various levels. Figure 4-9 shows the results of the frequency response for both the Gaussian profile and a box profile doped at a level of 10^{18} cm^{-3}.

The cutoff frequency for a device with a box profile is found to be 27.2 GHz when biased at -5 V. This is almost a 2x improvement over a device with a Gaussian profile. The reason for this increase is most likely an increase in the built-in electric field in these devices. The fields are shown in figure 4-10. The field near the n-Ge contact is an order of magnitude higher for the box profile than it is for the Gaussian profile. This high field sweeps the photogenerated carriers out more quickly, resulting in a higher cutoff frequency.

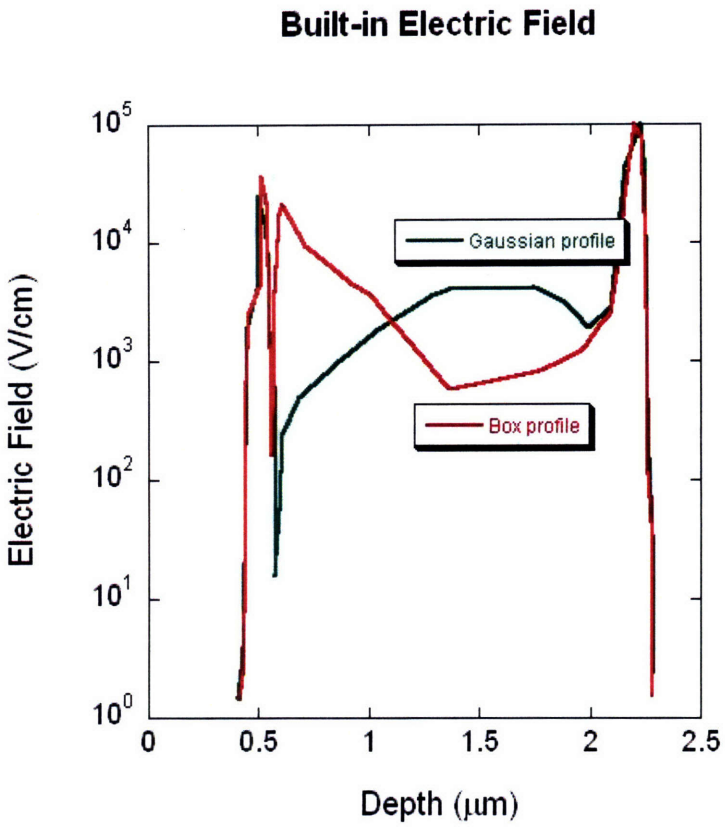

Figure 4-10: **Built-in electric fields vs. depth for Gaussian and box profiles.** The electric field is much higher at the n-type contact for the box profile. There is no p-type doping in the seed layer for either of these structures.

It was hypothesized that increasing the doping concentration in the n-type layer would increase the built-in field and, thus, increase the cutoff frequency. The effect of increasing the doping, however, is small up to concentrations of 10^{19} cm^{-3}. It is more important to have an abrupt profile, i.e. as box-like as possible. Since achieving an abrupt box-like profile is virtually impossible in reality, it is important to quantify the effect of the slope of the profile on the cutoff frequency. This quantification will shed insight on the implant and annealing restrictions during the fabrication of future devices.

In addition to removing the $p+$ Ge seed and better controlling the n-type doping, further improvement can be seen if the Ge film is thinned. In the devices that were fabricated, the Ge film was $\sim$1.7 μm thick. Simulations thus far have focused on devices with this same thickness. The structure was changed such that there was 0.8

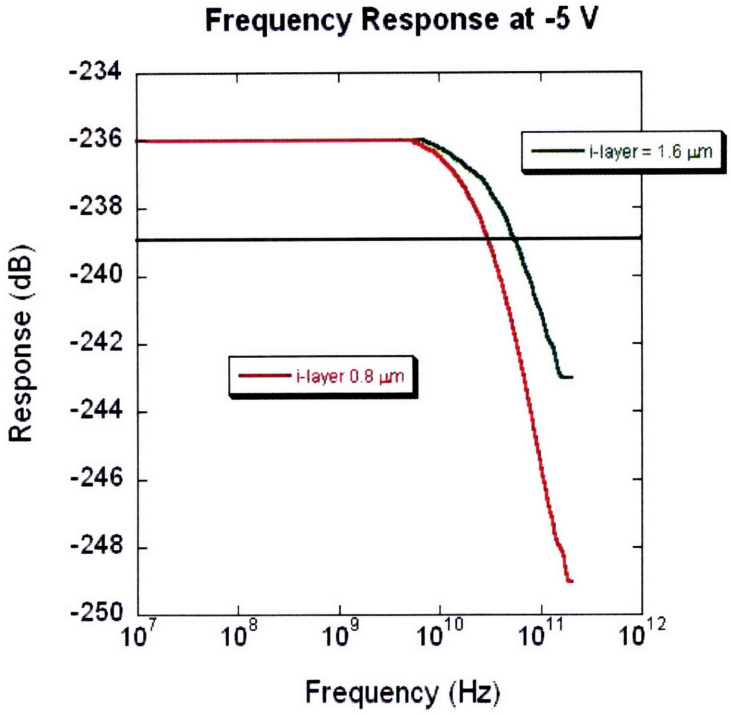

Figure 4-11: **Simulated frequency response of a thinned device.** Both structures have a 100 nm box n-type profile and the same background doping. The black line marks the 3-dB point, indicating cutoff frequencies of 27.2 GHz (1.6 μm i-layer) and 48.7 GHz (0.8 μm i-layer).

μm of i-Ge (with a background doping of 2 x 10^{15} cm^{-3} to match the SRP data) with an additional 0.1 μm of n-Ge on top. The doping level of the n-layer was kept at 10^{18} cm^{-3}. The frequency response of this thinned structure is plotted in figure 4-11 along with the thicker structure.

The cutoff frequency of the thinned device is 48.7 GHz. The fact that the 3-dB frequency is affected by the thickness of the device indicates that these diodes are transit time limited. A trade-off with this device is that the photoresponse is decreased due to the thinner Ge layer. The photoresponse for this structure is 0.24 A/W.

Thus, these simulations indicate that to improve the frequency response of these diodes, it is important to eliminate the autodoping in the Ge film. This can be done by eliminating the doping in the Ge seed layer. Furthermore, the n-type layer should be made as abrupt as possible, preferably by in-situ doping. Finally, thinning the Ge

i-layer will reduce the transit time of the carriers, improving the 3-dB frequency.

4.6 Chapter Summary

This chapter first discussed the simulated DC characteristics of Ge-on-Si photodiodes. It estimated that the leakage current density of these devices can be as low as ~1.2 mA/cm^2 and the responsivity can be as high as ~0.68 A/W, based on the parameters used in the simulations. Both of these values are lower than measured characteristics; however, they indicate that the previously fabricated diodes are performing quite well under constant stimulation. This chapter then discussed the simulated frequency response of various diode structures. It was shown that there is nothing fundamentally limiting these diodes from reaching a cutoff frequency of >40 GHz. To achieve this goal, the Ge cap layer can be thinned, the n-Ge should be fabricated to be as abrupt as possible, and the $p+$ doping in the Ge seed should be avoided to eliminate the autodoping.

Chapter 5

Summary and Future Work

5.1 Summary

In this thesis, I have demonstrated a metallization process that uses the tools available in MIT's Microsystems Technology Lab. This process is aimed at processing on wafer pieces. The process was used to successfully make metal contacts to a wafer piece that had been fabricated in [13].

In chapter 3, I discussed the DC characteristics of previously metallized diodes (PD) and the unmetallized diodes (AD). Chapter 3 showed that these two wafers had very similar area dependencies, but that the PD diodes had some defects around the perimeter of the device which probably accounted for the dark current.

Chapter 3 also discussed the effect of the metallization on the DC characteristics of the AD diodes. The series resistance was decreased. Furthermore, chapter 3 discussed some possibilities that caused many diodes to fail. Processing issues were discussed and they will be addressed in an upcoming study.

In chapter 4, I discussed the results from simulations using the Taurus Device platform. These results showed the fundamental limits of the dark current and responsivity for the current structure. Chapter 4 also discussed the factors that limit the frequency response of these devices and indicated structural changes that could increase the frequency response up to at least 40 GHz.

5.2 Future Work

There are clear steps that can be taken to fabricate better performing Ge-on-Si photodiodes. Some of them will be discussed in this section.

As discussed in chapter 3, the poly-Si/Ge interface is not as clean as it could be. The interaction of Ge and Si atoms may be responsible for traps that contribute to the leakage current. Furthermore, the diffusion of n-type dopants from the poly-Si to the underlying Ge layer is not well controlled. This lends itself to a poor *pin* structure. A possible solution is to eliminate the poly-Si layer and in-situ dope the Ge film. Metal contact would be made directly to the Ge film. These diodes would probably be mesa-isolated.

Another area of future work is to study the Ge passivation. As discussed in chapter 3, it appears that the Ge/dielectric interface is quite poor for most of the diodes fabricated. It was hyposthesized that this poor interface generated traps around the perimater of the devices which contributed to high leakage current. The AD diodes had the best interface and these were the samples that saw a rapid thermal anneal before oxide deposition. The RTA left a thin layer of GeON, which is one of the best ways to passivate a Ge film [22]. Further study can be done to optimize this GeON film. Moreover, better passivation of the Ge film can be accomplished with the incorporation of high-κ materials, such as HfO_2 [23]. MIT's MTL recently installed an atomic layer deposition tool which has the capability of depositing high-κ materials.

Furthermore, SRP results indicated that the intrinsic layer of germanium was actually p-type, with a doping level of $\sim 5 \times 10^{16}$. These p-type carriers are due to autodoping of the Ge film that occurs during growth. Blanket Ge films have been grown without the $p+$-Ge seed layer. SRP analysis showed that these films have a much lower auto-doping effect, indicating that future Ge films should be grown without this $p+$ seed layer. By making the Ge film more intrinsic, the diodes will have a greater 3-dB frequency.

Finally, simulations indicate that these diodes are transit time limited. According to results in chapter 4, the Ge cap layer can be thinned to approximately half of what

it is now. This will reduce the distance that the carriers must travel and increase the frequency response. Furthermore, by making the n-type doping profile as box-like as possible, the internal electric field will increase, thus increasing the frequency response. Future work will include quantifying this effect and building diodes with such a profile.

Appendix A

Germanium RCA Clean

1. NH_4OH:H_2O 1:4 for 5 minutes to etch native oxide
2. Rinse
3. H_2O_2:H_2O 1:6 for 15 seconds to grow about 20 $\AA$ of GeO_2
4. Rinse
5. HF:H_2O 1:50 for 30 seconds
6. Rinse
7. HCl:H_2O 1:4 for 30 seconds
8. Rinse
9. Dry

Appendix B

Photoresponse and Frequency Response of AD diodes

After the metallization process outline in chapter 2, the AD diodes were measured under a series of conditions. Chapter 3 discussed the DC I vs. V characteristics of these diodes and the series resistance. The addition of topside metal contacts also made it possible to perform photoresponse and frequency response measurements on these diodes, the results of which are detailed here.

B.1 Photoresponse

The photoresponse of these diodes was measured on a 100 μm square diode, with 0.9 mW of incident light at a wavelength of 1550 nm. The I vs. V curves for both dark current and photoresponse are shown in figure B-2.

It is clear from figure B-2 that the response at -1 V is $\sim$5 mA/W. This is much lower than the value of 0.5 A/W reported in [13]. This data is unexpected because the leakage current on these diodes was so low, but it is possible that the *pn*-junction is actually in the poly-Si layer. The SRP analysis left the junction depth unclear. It is also possible that traps are causing the photogenerated carriers to recombine before they reach the metal contacts. These traps could be due to the passivation of the Ge

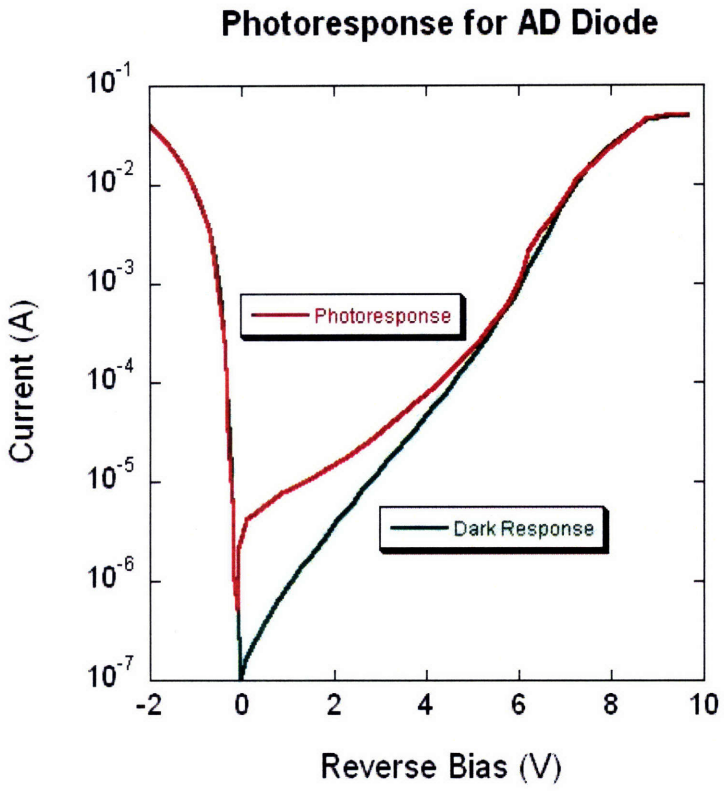

Figure B-1: **Photoresponse of metallized AD diode.** This plot indicates that the responsivity at a bias of -1 V is ~5 mA/W. Measurements are courtesy of Jason Orcutt.

film or from the poly-Si/Ge interaction at the interface.

In [13] a responsivity of 0.39 A/W is quoted for AD diodes. This value, however, was not measured on the same wafer that was processed in this study. This value was measured on a diode from lot 20, wafer 11 which had a very high leakage current. When this thesis refers to AD diodes, it is referring only to those diodes found on lot 20, wafer 12.

B.2 Frequency Response

The frequency response of a 100 μm square diode was also measured. The frequency response is shown in figure 4-6. At 0 bias, the diode has a cutoff frequency of ~1 GHz while at a -5 V bias, the response has already started to fall off at <0.1 GHz.

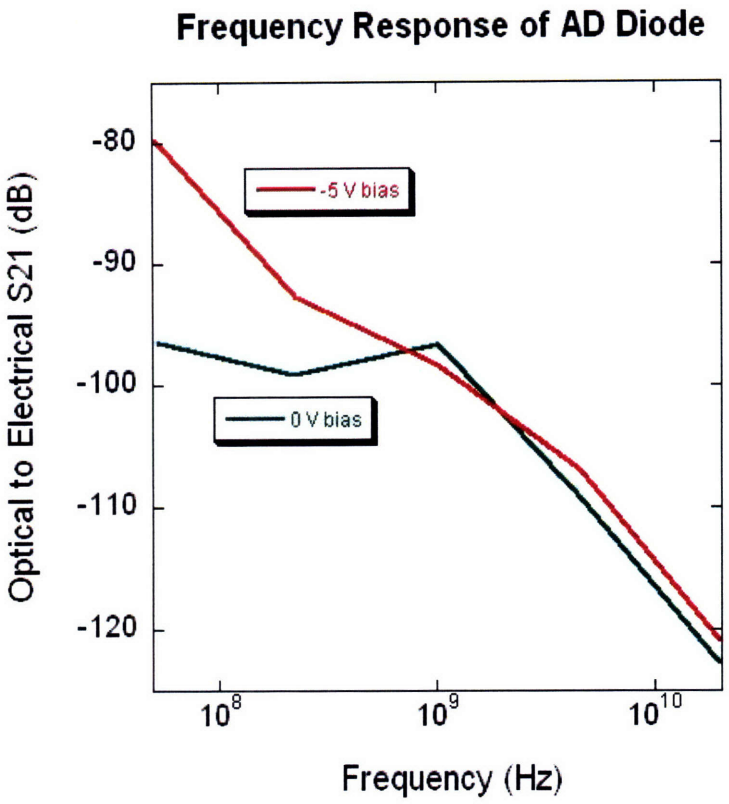

Figure B-2: **Frequency response of metallized AD diode.** This plot shows cutoff frequencies of ~1 GHz at 0 V and <0.1 GHz at -5 V. Measurements are courtesy of Jason Orcutt.

Again, these results were unexpected because of the excellent leakage characteristics. Junction depth and traps could explain this strange frequency response. In order to understand what is limiting the photoresponse and bandwidth, more work would need to be performed to characterize the device structure.

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