Radio Frequency dc-dc Converters: Device Characterization, Topology Evaluation, and Design

by

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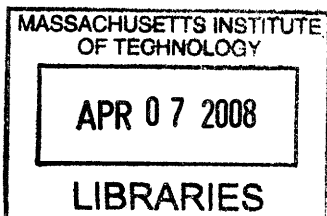
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Abstract

High frequency power conversion is attractive for the opportunities it affords for improved performance. Dc-dc converters operating at high frequencies use smaller-valued energy storage elements, which tend to be physically smaller and lower-cost, and this can result in improved transient performance while retaining high efficiency. One way to achieve high switching frequencies is by using resonant inverter and rectifier topologies and regulating voltage via on-off control.

This scheme requires a great deal of investigation of design practices appropriate to high frequency power conversion. The design issues were investigated for a 200 W 160-200 V input 33 V output converter. A comparison of resonant inverter topologies for the power stage was made. Appropriate devices were sought, compared, and characterized. A high frequency gate drive scheme for a large vertical MOSFET was developed. Several prototypes were built and these are also presented.

Acknowledgements

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Dc-dc Supplies

Modern electronic devices of all sorts share a dependence on regulating power supplies. In many applications, a stable energy source is provided by a dc-dc converter. Power processing can comprise a substantial portion of the size and cost of a system, and a low efficiency in a dc-dc converter can increase the overall power consumption (e.g. from a battery) substantially.

Many desirable improvements can be made by increasing switching frequency. The total energy storage requirement is reduced, which can improve the size of energy storage components, their cost, or both. Reduced energy storage can also improve converter transient response, because the time required to change the steady-state value of energy stored is smaller. Further, improvements in some of these areas can be traded off for improvements in efficiency. [6]

1.2 Resonant Power Conversion

A major barrier to increasing frequency is that some important losses are frequency-dependent and become prohibitively large at frequencies much above those of conventional converters. One way to increase frequency while maintaining acceptable efficiency is to use resonant power conversion techniques. The resonant power converters under investigation in this work consist of a resonant high frequency inverter matched to a resonant rectifier [5, 7–21]. The output voltage is regulated by modulating the converter on and off at a frequency much lower than the switching frequency [22–24]. This approach is outlined in the diagram of Fig. 1.1.

Resonant inverters use controlled impedances to shape the voltage and current waveforms present. A common aim is to cause the converters to switch at or near zero voltage (ZVS) and zero $\frac{dv}{dt}$. This controls frequency-dependent switching losses and so allows a marked
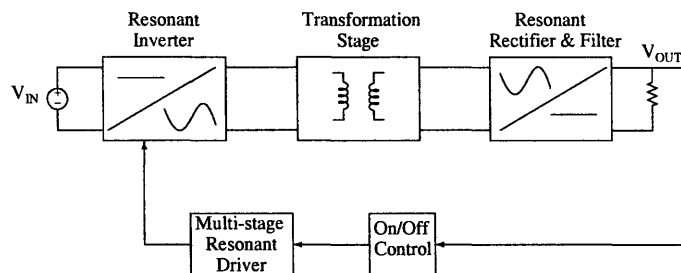
Figure 1.1: Block diagram of the power conversion scheme

increase in switching frequency. Such waveshaping techniques can also absorb some of the most problematic parasitic elements present in switching and other devices and use them in impedance networks to achieve the desired waveforms.

Finding magnetic elements which perform well at high frequencies can also be a challenge. Most magnetic materials maintain favorable properties only up to below 1 MHz or below. A few available RF magnetic materials may also be of use at frequencies as high as 10 MHz. These materials generally exhibit low permeability and large loss coefficients as compared to their lower-frequency counterparts. In all cases, the utility of the materials decreases with increasing frequency. However, if other factors allow a sufficiently large increase in frequency, inductances can become small enough to implement without use of a magnetic material (air-core or coreless). In an air-core inductor, the quality factor Q of the inductor increases with frequency.

Another concern when working at high frequencies is the added complication to the gate drive. Just as with switching losses, gating losses in traditional hard-switched converters are frequency-dependent and the associated loss can cause total efficiency to drop quickly. Several gate drive techniques were investigated for this converter, and a gate driver with comparatively small power requirement was implemented.

Work closely related to that in this thesis is found in [5, 25]. The approach described here is similar to that taken in [10, 11], albeit at substantially higher voltage and power levels.

1.3   Thesis Objectives and Contributions

This thesis addresses the design and construction of RF resonant dc-dc power converters. Design questions such as topology selection, device evaluation, and gate drive are investigated. In particular, these techniques were developed for a high-voltage, medium-power switching voltage regulator. The design techniques described in this thesis are applicable

to a wide range of RF power conversion problems.

1.4   Organization of this Thesis

A primary concern when designing any power converter is choice of topology. In this case, several switch-mode resonant inverters were evaluated for use in this application. The process of topology evaluation and selection is described in Chapter 2.

The component which exerts the most influence over the design of a resonant inverter is the main switching device, usually a MOSFET. Chapter 3 describes the process of comparing prospective devices and of extracting model parameters for the device in use.

The design and construction of the power stages that were the center of this work is treated in Chapter 4. Several prototypes were built in a collaboration between the author and others.

The gate drive and control of the converter is an important consideration in system design. A successful gate drive must drive the gate effectively at a power level low compared to the total output power. The gate drive developed in this work and prospects for control are discussed in Chapter 5. Chapter 6 concludes the thesis.

Topologies

2.1 Introduction

A perennially important consideration when designing power converters is the specific topology used. In this application, a high frequency resonant switching stage was used at a single operating point and regulation was achieved by way of on-off control. The specific topology used is a major determinant of the eventual form of the converter, dictating the size and type of components used, the converter transient performance, and the feasibility of the design at various design points. This section reviews the relative merits of the inverter topology options considered for this application.

2.2 Specifications

The application requires a regulating power supply with a 160-200 V input range and a 33 V output, delivering at least 200 W. The prototype was to be built with a commercial RF device. The target switching frequency is as high as possible, but at least 10 MHz. The converter comprises a resonant switching inverter matched to a resonant rectifier, as well as gate drive and control stages. This chapter concerns the inverter topology only. These specifications are also listed in Table 2.1. Because of the difficulty in driving switching devices at high frequencies, only inverters with a single, ground-referenced switch were considered here.

Attribute	Specification
Input Voltage	$160 - 200V$
Output Voltage	$33V$
Output Power	$> 200W$
Frequency	$> 10MHz$

Table 2.1: Inverter Specifications

2.3 Figures of Merit

In addition to meeting the specifications listed above, resonant topologies were evaluated for this application based on a number of figures of merit. The inverter topologies were compared using a common device; however, the all of the topologies should respond in a similar manner to improvements in the device. For device comparisons, see Chapter 3.

A primary consideration in power converters is always efficiency. The efficiency of a resonant inverter using parts of similar quality at a similar operating point is dependent upon the circulating currents that it sustains. Furthermore, where additional voltage transformation is necessary to match to the rectifier stage, this will incur additional loss.

The improved transient performance made available by using high frequency switching converters is a main advantage of this approach; for that reason, it is desirable to minimize the stored energy in the system and thus speed the transient response. Topologies with no bulk energy storage are well suited here. (Some blocking capacitance may be acceptable, particularly if it need not be charged/discharged each time the converter is turned on.) The component values must also be large enough that they will not be swamped by parasitic capacitances and inductances in the PCB. The lower limits on inductance and capacitance that were considered here were approximately 10 nH and 10 pF, respectively.

A final consideration is the flexibility of the topology. In some topologies, the frequency, the capacitance in shunt with the main switching device, and the power level are tightly coupled [26]. In these cases, there is a maximum operating frequency for a given power level and device. Some topologies have a higher frequency limit for the same device and power, and some topologies are not subject to this restriction. In general, the more flexible the topology, the more conducive it is to making design choices which improve the other figures of merit under consideration.

2.4 Representative Design Comparison

The designs treated here were aimed at an earlier but similar operating point of 200 W nominal output power for $V_{DD} = 240\ V$ with a loaded Q of 7. Since all of the resonant topologies have similar switch requirements, the results of a design comparison based on a single switch are widely applicable. Issues of frequency limits, relative losses, et c. will approximately scale from device to device, making a comparison at a single design point helpful. The switch parameters used for this comparison are based on estimates for a large silicon carbide MOSFET. This switch model featured a 1400 V breakdown voltage, an
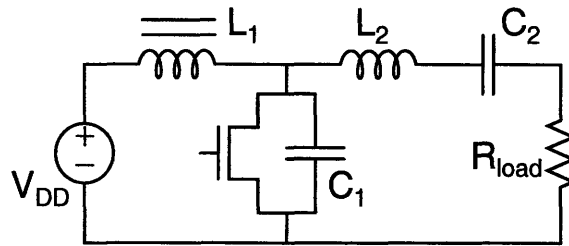
Figure 2.1: Schematic of the conventional class E topology described in [1].

equivalent linear output capacitance $C_{out} = 24.83$ pF with an equivalent series resistance (ESR) of 0.1Ω (which includes 5 pF of parasitic (board) node capacitance), and an on-state resistance $R_{DS,ON} = 0.98\Omega$.

Three primary inverter topologies were considered: the conventional class E [1]; the second harmonic class E [2,3]; and the class Φ_2 [25]. These topologies were compared based on the switch noted above. The comparison was made by way of simulation, with realistic component quality factors and parasitic values used so far as possible, and limiting the designs to those plausible to build. The efficiency of the resultant inverters, the circulating currents present, the main switch voltage stresses, the achievable power and frequency combinations, and the necessary component values were all considered.

2.5 Conventional Class E

The conventional class E converter [1,27] and has become a standard for resonant power conversion. The schematic is pictured in Fig. 2.1. It was used as a benchmark in this work, as well as evaluated for its merits in this application. The primary drawbacks of this topology are its large voltage stresses and its use of an RF choke (bulk) inductor. The class E is also not very flexible in frequency in the range we are investigating.

Standard class E component values, obtained from [1], are reprinted below. Numerical values for components of the classic class E topology are calculated for a loaded Q of 3, which is a small but feasible value. Note that C_1 is the capacitance in parallel with the switch in both cases, and that L_1 is the largest inductor in the second harmonic version of the class E.

$$R_{load} = \frac{2 \cdot V_{DD}{}^2}{P_{out} \cdot \left(\frac{\pi^2}{4} + 1\right)} \approx \frac{0.577 \cdot V_{DD}{}^2}{P_{out}} \tag{2.1}$$

$$C_1 = \frac{P_{out}}{2 \cdot \pi^2 \cdot f \cdot V_{DD}{}^2} \approx \frac{P_{out}}{\pi \cdot \omega \cdot V_{DD}{}^2} \tag{2.2}$$

$$C_2 = \frac{1 + \frac{1.42}{Q_L - 2.08}}{(2 \cdot \pi \cdot f)^2 \cdot L_2} \tag{2.3}$$

$$L_2 = \frac{Q_L \cdot R}{2 \cdot \pi \cdot f} = \frac{Q_L \cdot V_{DD}^2}{\omega \cdot P_{out} \cdot \left(\frac{\pi^2}{4} + 1\right)} \tag{2.4}$$

$$L_1 \gg L_2 \tag{2.5}$$

$$\tag{2.6}$$

Note that these are the theoretical values given by Sokal and Sokal in [1] for the approximation of very large loaded Q of the output network. Kazimierczuk et al. in [28] provide a more precise numerical derivation for these components for low loaded Q, which allows somewhat more capacitance for a given frequency, power level, and voltage (or a somewhat higher frequency for a given minimum capacitance, power level, and voltage). While this improves slightly the frequency capability of the conventional class E, the change is still much less than the improvement provided by the second harmonic class E. A numerical approximation can also be made for the current in the switch during the on state and during the off state in the high-efficiency limit [27].

$$I_{sw,on,RMS} \approx 1.168\sqrt{\frac{P_{OUT}}{R_{LOAD}}} \tag{2.7}$$

$$I_{C1,RMS} \approx 0.4600\sqrt{\frac{P_{OUT}}{R_{LOAD}}} \tag{2.8}$$

$$\tag{2.9}$$

The conventional class E topology delivers a minimum energy per cycle based on the capacitance in parallel with the main switch (C_1). That leads to a maximum frequency capability for a given power, input voltage, and device equivalent capacitance. In this design example, that maximum frequency is approximately 7.1 MHz. The values of the passive components at this maximum frequency are listed in Table 2.2.

Component	Value
C_1	24.83 pF (device capacitance)
C_2	114.2 pF
L_2	11.2 nH
L_1	$\gg L_2$
R_{load}	166.2Ω

Table 2.2: Required passive component values for a class E inverter; $P_{OUT} = 200W, f_{sw} = 7.08\ MHz$, $V_{DD} = 240V$, loaded $Q = 3$
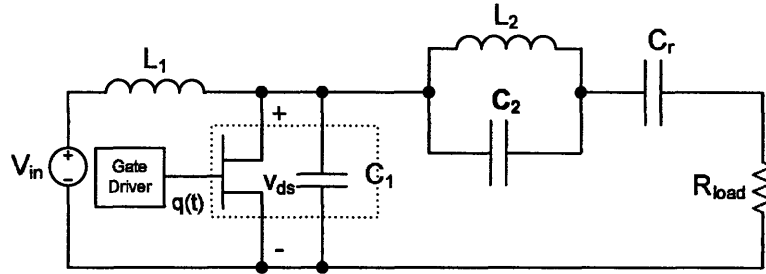
Figure 2.2: Schematic of the second-harmonic class E topology as described in [2].

2.6 Second Harmonic Class E

There exist in the literature several topologies which use resonant elements to create an input network and load network for an inverter similar to the class E but which do not require an RF choke. This work concentrates on the second-harmonic class E version, which drives a low load impedance, requires only resonant components in a reasonable range for this operating point, and maintains zero voltage and zero $\frac{dv}{dt}$ switching.

The second-harmonic class E converter [2, 3] is a variant of the conventional class E converter [1], which uses resonant networks tuned to the second harmonic of the switching frequency to produce standard class E voltage waveforms with different current waveforms and component values. A variant of this converter is described in detail in [2]. A schematic of this topology may be seen in Fig. 2.2.

A somewhat different variety of second harmonic class E converter is described by Grebennikov et al. in [3]. That design is also discussed in the context of the gate drive in Section 5.4. The Grebennikov design is not as desirable for the power stage as is the Iwadare design. Its maximum operating frequency is only slightly higher than that of the class E. It also is more sensitive to its load than is the Iwadare version, as the load comprises an important part of the waveshaping of the circuit. This application includes a low-Q intermediate stage and a rectifier equivalent load, making waveshaping by the load unattractive.

2.6.1 Design Equations

In [2], Iwadare et al. provide an analytical derivation of approximate design equations. The relevant equations follow. They are simplified using the assumption that the resonant tanks are tuned to the second harmonic, and not to a higher-order harmonic. This enables the use of the lowest loaded Q in the output tank.

$$R_{load} = \frac{V_{DD}{}^2}{18 \cdot P_{out}} \tag{2.10}$$

$$L_1 = \frac{\pi \cdot V_{DD}{}^2}{16 \cdot \omega \cdot P_{out}} \tag{2.11}$$

$$C_1 = \frac{4 \cdot P_{out}}{\pi \cdot \omega \cdot V_{DD}{}^2} \tag{2.12}$$

$$C_r = \frac{18 \cdot P_{out}}{Q_L \cdot \omega \cdot V_{DD}{}^2} \tag{2.13}$$

$$C_r \approx \frac{2.57 \cdot P_{out}}{\omega \cdot V_{DD}{}^2}; Q_L = 7 \tag{2.14}$$

$$L_2 = \frac{1}{24}\left[Q_L - \frac{32 + 3 \cdot \pi^2}{4 \cdot \pi}\right] \cdot \frac{V_{DD}^2}{\omega \cdot P_{out}} \tag{2.15}$$

$$L_2 \approx \frac{0.0874 \cdot V_{DD}{}^2}{\omega \cdot P_{out}}; Q_L = 7 \tag{2.16}$$

$$C_2 = \frac{6}{Q_L - \frac{32+3 \cdot \pi^2}{4 \cdot \pi}} \cdot \frac{P_{out}}{\omega \cdot V_{DD}{}^2} \tag{2.17}$$

$$C_2 \approx \frac{2.86 \cdot P_{out}}{\omega \cdot V_{DD}{}^2}; Q_L = 7 \tag{2.18}$$

The claim is made that $Q_L \geq \frac{32+3 \cdot \pi^2}{4 \cdot \pi} \approx 4.9$ permits proper operation, but in simulation a somewhat higher loaded Q was required in order to obtain appropriate waveforms. For these designs, a loaded Q of 7 was used, and produced the expected waveforms. These equations may be compared to those for the standard class E topology listed in Sec. 2.5.

Analytical expressions for the root mean square (RMS) currents in the switch ($I_{sw,RMS}$) and in the parallel capacitance C_1 ($I_{C_L,RMS}$) may be derived from the results in [2] and are listed below. The second harmonic class E drives a smaller equivalent load resistance than the conventional class E for the same power level and voltage. While the RMS of the current circulating in the switch during its on-state, $I_{sw,RMS}$, is slightly lower than that of the conventional class E, the RMS of the current in the parallel capacitance, $I_{C_L,RMS}$ (which usually comprises, at least in part, the relatively high-ESR device output capacitance) is
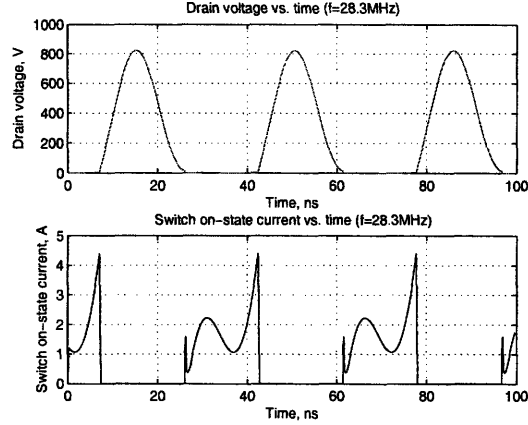
Figure 2.3: Simulated voltage and switch on-state current waveforms in the second harmonic class E inverter.

substantially higher, potentially leading to larger dissipation in the switch. These larger currents also circulate through the (smaller) passive magnetic components, possibly causing higher loss there as well.

$$i_{sw,RMS} = I_D \cdot \sqrt{\frac{65 \cdot \pi^2 - 576}{3 \cdot \pi^2}} \approx 1.49 \cdot I_D \tag{2.19}$$

$$i_{C_1,RMS} = I_D \cdot \sqrt{2 \cdot \left(1 + \frac{16}{\pi^2}\right)} \approx 2.29 \cdot I_D \tag{2.20}$$

$$I_D = \frac{1}{16} \cdot \frac{\pi \cdot V_{DD}}{\omega \cdot L_1} = \frac{P_{out}}{V_{DD}} \tag{2.21}$$

2.6.2 Waveforms

The drain-source voltage waveform of the second harmonic class E inverter is very similar to the standard class E waveform. Voltage and switch on-state current curves are shown in Fig. 2.3, assuming a linear device output capacitance. The switch on-state current waveforms differ significantly from those of the conventional class E. These waveforms are only scaled in time, and, for the off-state switch current, in magnitude, as frequency changes. The RMS currents in all components are also shown as a function of frequency in Fig. 2.4. The distribution of losses among components, based on the assumptions made for simulation, is shown in Fig. 2.5.
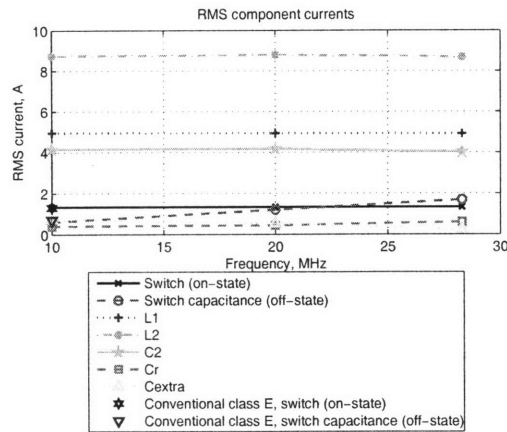
Figure 2.4: RMS currents for all components in the second harmonic class E inverter (Simulated).
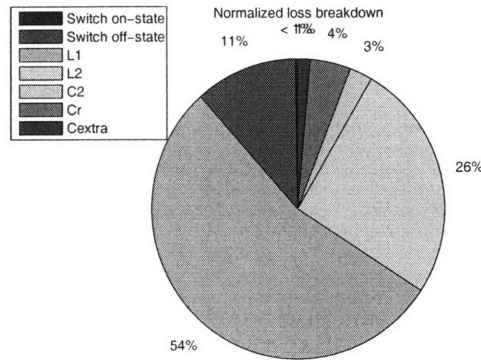
Figure 2.5: Normalized loss breakdown in the second harmonic class E inverter (Simulated).

2.6.3 Efficiency, Power, and Loss

The power delivered by the inverter at the output is listed in Table 2.3. Designs are calculated at 10, 20 and 28.3 MHz, the latter being the upper frequency limit for the given device, power level, and input voltage. The duty ratio is 0.46, which a sweep found produces highest overall efficiency; inductors have a Q of 160, and discrete capacitors have a very large Q (2000). The values of the passive components across frequency are shown in Figs. 2.6 and 2.7.

The major loss mechanisms for the second harmonic class E topology are on-state (conduction) loss in the switch, off-state (device capacitor ESR) loss in the switch, and conduction
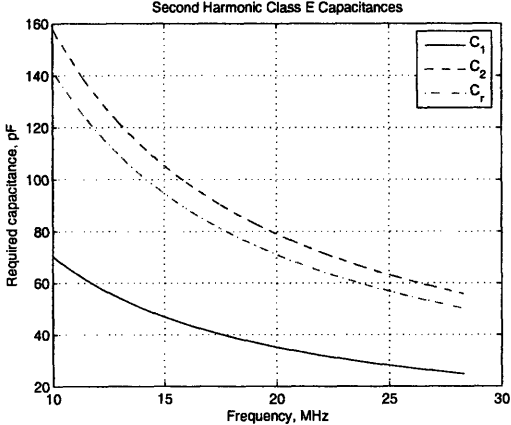
Figure 2.6: Capacitor values across frequency, second harmonic class E
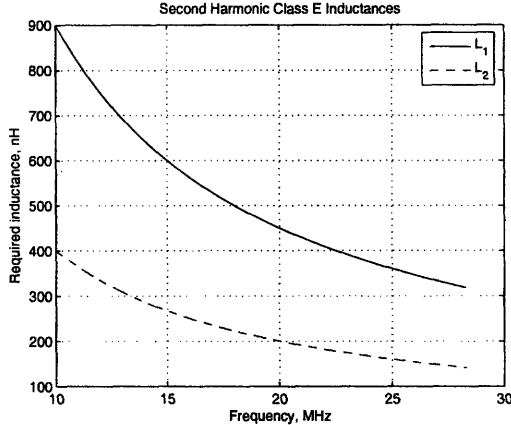
Figure 2.7: Inductor values across frequency, second harmonic class E

Frequency, MHz	Output Power, W
10	182.28
20	181.56
28.3	180.59

Table 2.3: Comparison of output power at a given voltage point across switching frequency. Output power from simulation for a 200 W nominal second harmonic class E inverter at various frequencies; $V_{DD} = 240V$, loaded $Q = 7$, inductor $Q = 160$, device capacitance $=24.83$ pF, device capacitance ESR$=0.1\Omega$, duty ratio$=0.46$

loss in the inductors. As the capacitors carry significant currents, there is also some loss in the discrete capacitors due to their ESR. All these losses are a function of frequency, and for the representative designs are plotted in Fig. 2.5 for 28.3 MHz.

2.7 Class Φ_2

The class Φ_2 inverter topology [4, 5, 11, 25] was also studied for use in this application. The design and advantages of this inverter are treated in the above references at length and the analysis will not be repeated here.

2.8 Comparison

A second-harmonic class E topology has potential advantages over the standard class E topology. Both types exhibit zero-voltage switching and can be operated at low loss, and both can be appropriate for high frequency applications. However, the required passive components have substantially different values and are most suitable for different applications. A major advantage of the second harmonic version is the absence of a large RF choke inductor at the input. This inductor is replaced by a much smaller one which together with the switch output capacitance is resonant at the second harmonic of the switching frequency, making it smaller in value even than the series resonant inductor in the standard class E. The parallel resonant tank at the output also is tuned to the second harmonic, making its components, especially its inductor, smaller in value than that of the standard class E.

While both class E topologies operate with a specific output capacitance for a given power level, frequency, and input voltage, the required capacitance for the second harmonic version of the class E is nearly 4 times higher than that for the conventional class E at a single

voltage, power, and frequency. This makes the second harmonic class E topology more suitable for switches with large output capacitance compared to the power and voltage of the application. For a given switch, output power and input voltage, the second harmonic class E inverter can operate at approximately three times the maximum frequency for the standard class E; likewise for a given frequency, output power and input voltage, the second harmonic class E can utilize a device with nearly three times the device area of a standard class E.

Another important difference between the conventional and second harmonic class E converters is the appropriate load resistance (and AC output voltage) at which the circuits operate. Each topology has a resistive load requirement (to which the external load must be matched) for proper operation. In each case, this load resistance is a function of input voltage and power. For the second harmonic version of the class E, however, this load resistance is about ten times smaller than for the conventional class E. As noted in [29], this makes the second-harmonic class E suitable for applications requiring a step-down in voltage.

The second harmonic class E topology also presents potential challenges. Unlike the conventional class E, capacitors C_2 and C_r form a high-frequency short from the load to ground through the output capacitance of the main switching device. While this is not a concern for a true resistive load, higher voltage harmonics generated by a rectifier load, for example, could propagate through the circuit and interfere with proper operation. Additionally, since the topology provides a step-down in voltage relative to a conventional class E, it circulates more current both in the two inductive elements and in the capacitance in parallel with the switch. Since some of the capacitance of the switch is formed by the high-ESR device output capacitance, capacitor ESR losses are more of a concern with this topology.

Another limitation relates to the device current waveform [3]. Unlike the conventional class E converter, the current in the switch peaks just as the switch is turning off, which could induce additional dissipation if the switch is soft-gated. Finally, both the second harmonic and the conventional class E topologies share the complication of subjecting the switch to a peak voltage stress of about 3.6 times the input voltage, making it undesirable for some applications where the rated switch voltage is not large compared to the input voltage.

2.9   Topology Selection

The class Φ inverter has a number of advantages which make it well-suited to this application. Its main advantage is its lower peak switch voltage stress. This is followed by its flexibility between power, capacitance, and frequency. This flexibility allows the design to be optimized for high efficiency, for low peak voltage, or for other desirable attributes. The second harmonic class E is also an appropriate candidate for high-frequency dc-dc converters at this power level, particularly in applications which do not require reduced switch voltage stress. However, because of the superior qualities of the class Φ inverter, it was used for the power stage of this converter.

Device Characterization and Selection

3.1 Attributes of Interest

The design of a power stage is heavily influenced by device selection. In the resonant topologies considered here, certain device parasitics are absorbed into the design and so a device must be chosen and thoroughly characterized prior to final power stage design. There are several requirements for a useable switch, based on the eventual design specifications listed in Table 3.1. First, for a dc input voltage of approximately 200 V, the minimum necessary device breakdown voltage is approximately 500 V (for a class Φ inverter with a peak voltage stress slightly higher than 2:1). For a class E converter or its variants, a breakdown voltage of up to nearly 800 V may be necessary. Second, it must be possible to transition the device from cutoff to deep triode rapidly compared to the switching frequency of the inverter, in order to avoid intolerably large losses and damage to the device. For this reason, the gate time constant must be small compared to the switching period. Low inductance at all terminals will help minimize parasitic ringing. The model used for the devices, including parasitics of interest, is pictured in Fig. 3.1.

In general, there is a shortage of high voltage RF parts appropriate to this application. Radio Frequency MOSFETS are optimized for high frequency use in both design and packaging. Standard (not RF-specific) MOSFETS were considered, but there are risks associated with their use. First, standard parts may not switch sufficiently quickly due to a high gate resistance and resultant large gate time constant. Second, a high lead inductance at the drain and source can interfere with proper switching waveforms. Preliminary measurements on some appropriately-sized standard devices led to the conclusion that an RF-specific MOSFET was required for this application.

Specification	Value
Input Voltage	150-200 V
Output Voltage	33 V regulated
Switching Frequency	30 MHz

Table 3.1: Specifications for the power stage, as available for device selection
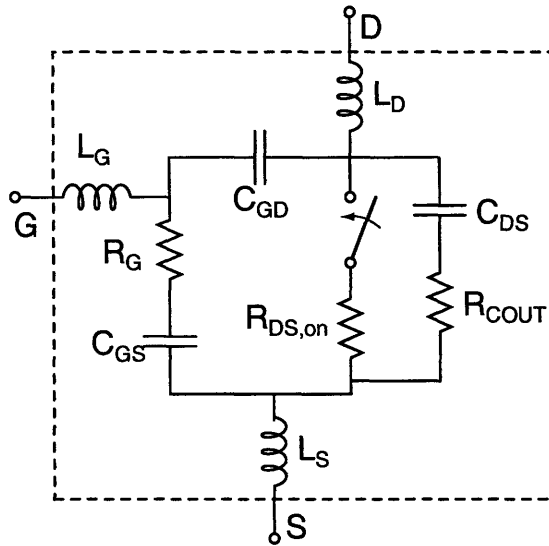
Figure 3.1: Model used for MOSFETS including (nonlinear) parasitic elements

For this work two types of devices were under consideration: those with a drain-source breakdown voltage of 450-800 V and thus suitable for class Φ inverters, and those with a drain-source breakdown voltage of $> 800V$ and so suitable for inverters with class E waveforms.

Several RF MOSFETS were measured for possible use in a different RF inverter in [4]. These devices included two which would be suitable for a 200 V class-E-waveform inverter, the 1000 V DE150102N02A and the 900 V ARF447, and several 450 V and 500 V devices which would be suitable only for a quasi-square-wave inverter like the class Φ_2. The recently released 500 V ARF521 was also a strong candidate. Once the class Φ topology had been selected, attention was focused on the lower-voltage devices. The relevant table, with the addition of the ARF521, is reproduced as Table 3.2.

3.1.1 Capacitances and Resistances

A main figure of merit which is of interest in the design of high frequency resonant inverters is given by $R_{DS,on} \cdot C_{OSS}$ [7]. A common tradeoff in device scaling is between the on-state (conduction) resistance $R_{DS,on}$ and the drain-source capacitance C_{DS}. When the device size is scaled, this $R_{DS,on}C_{OSS}$ product stays approximately constant for a given technology and so is a valuable metric. In some applications it may be possible to even use more than one device in parallel and take advantage of the device scaling in this manner. In fact, for this application, many of the devices under consideration are a similar size, and paralleling

Device	V_{br}	C_{GS}	R_G	C_{DS}, 25 V	$R_{DS,on}$	C_{GD}, 25 V
IXZ210N50L	500 V	857 pF	1180 $m\Omega$	248 pF	1.00 Ω	25 pF
IXFT21N50F	500	3190	56	514	0.25	160
IXFT12N50F	500	2069	72	308	0.40	90
IXZR16N60	600	2000	1000	500	0.44	45
ARF449A	450	1332	71	158	0.80	55
ARF520	500	1200	(Not Measured)	150	0.8	15
ARF521	500	780	120	165	0.55	12

Device	τ_{GS}	$R_{DS,on}C_{DS}$, 25V	Package	$V_{GS,max}$
IXZ210N50L	1010 ps	248 ps	IXYS RF	$\pm 30V$
IXFT21N50F	179	128	TO-268	± 30
IXFT12N50F	149	123	TO-268	± 20
IXZR16N60	2000	220	Modified TO-247	± 20
ARF449A	95	127	TO-247	± 30
ARF520	*	120	APT RF	± 30
ARF521	94	91	APT RF	± 30

Table 3.2: Devices under consideration; adapted from [4]

proved unnecessary.

It is difficult to directly measure the two-terminal capacitances C_{DS}, C_{GS} and C_{GD}. It is much more convenient to short terminals together two at a time and measure between the shorted terminal pair and the third terminal. The output capacitance C_{OSS} is that between the drain and the shorted gate-source pair, and is approximately the parallel combination of C_{DS} and the much smaller C_{GD}. The input capacitance C_{ISS} is that between the gate and the shorted drain-source pair and is approximately the parallel combination of C_{GS} and the much smaller C_{GD} (the reverse transfer capacitance C_{RSS} is simply a name for C_{GD} in this scheme). Likewise, by shorting the drain and the gate at frequencies of interest, one may measure the parallel combination of C_{GS} and C_{DS}, referred to here as $C_{(GD)S}$. The capacitance values available on datasheets are generally those of C_{OSS}, C_{ISS} and C_{RSS}. The values of C_{DS}, C_{GS} and C_{GD} can be approximately extracted from C_{OSS}, C_{ISS} and C_{RSS}.

Another important consideration in device selection is the reverse transfer capacitance C_{GD}. This capacitance is multiplied by the (nonlinear) gain of the inverter according to the Miller Effect. Minimizing this capacitance is important in RF design because of the great complications it introduces with gate drive. Unfortunately, the range of available high-voltage devices suitable for use in RF circuits is small and there is limited opportunity to minimize this reverse transfer capacitance.

In order to turn the device on and off in a small fraction of the switching period, the time constant of the gate – the product of gate capacitance and gate resistance – must be much smaller than the switching period. Otherwise, in order to switch the gate sufficiently quickly to minimize loss, the gate must be substantially overdriven at a large power cost. Further, the power required to drive the gate (even when the time constant is sufficiently small) is dependent on this resistance, on this capacitance, or on a combination of the two, and so a small time constant offers an additional benefit.

Unfortunately, gate resistance is often not listed on data sheets. It is then difficult to determine whether the gate time constant of a given device is appropriate to the application without performing measurements. Values of the gate resistance of several devices, gleaned from datasheets or determined by measurement, are listed in Table 3.2. In general, the devices under consideration had a gate time constant of fractions of a nanosecond, which is small compared to the 33 ns period at 30 MHz. In addition, both the drain-source resistance $R_{DS,on}$ and the gate resistance R_G are moderately strong functions of temperature.

Further complicating the device modeling is the nonlinearity of all the capacitances. Drain-gate and drain-source capacitances C_{GD} and C_{DS} are heavily dependent on the drain-source dc bias voltage. While C_{GS} is also a somewhat weaker function of drain bias, that effect is relatively small and C_{GS} was considered linear for purposes of device modeling. Finally, many of the devices have quite low impedances at 30 MHz, so driving the device gates at low power becomes a complicated problem.

3.1.2 Inductances and Packaging

Transistors designed and packaged for RF are particularly useful because they incorporate good high frequency design practice, especially with respect to inductance. When using discrete devices at VHF, packaging becomes very important. Traditional power MOSFET packages such as the TO-220, TO-247, et al. introduce considerable inductance (5-10 nH or more) at each of the leads. At 30 MHz, the impedance of this inductance starts to be comparable to that of the resonant capacitances and inductances of the topology. Additional inductance not absorbed into or canceled with circuit design often creates high-frequency ringing which distorts waveforms and in some cases can impact performance. Inductance at device terminals also can complicate diagnostics and potentially endanger devices because the instantaneous voltage at an external terminal can be very different from the voltage at the corresponding point on the silicon die. For these reasons, it is important to use packaging techniques developed with minimizing inductance in mind. RF specific packages have wide, low-inductance leads and are bonded to their dice in such a way to minimize inductance as well. The RF packages in which the ARF521 is available is shown in Figs. 3.2.

Figure   3.2:   Image   of   ARF521   RF   package.   Image   courtesy   of news.thomasnet.com/images/large/528/528787.jpg

The package for the IXZ210N50L is similar with a slightly different form factor [30].

3.2   Device Selection

Looking at the attributes of the available devices, only the ARF520 and the ARF521 combine a sub-nanosecond time constant with an RF package. Of these, the ARF521, being a newer device, is more attractive. The ARF521 has the lowest $R_{DS,on}C_{DS}$ product of any of the devices, including those in conventional packages. The reverse transfer capacitance C_{GD} of the ARF520 and ARF521 are the same and the lowest of any of the devices. The gate time constant of the ARF521 is one of the smallest under consideration and is very fast compared to the 33 ns period. For all these reasons, the ARF521 was selected for use as the main switching device.

3.3   Device Characterization

In order to accurately predict the behavior of the device when integrated into a resonant inverter, it is important to carefully characterize the device parasitics. These include the three main capacitances, between gate and source (C_{GS}), drain and source (C_{DS}) and gate and drain (C_{GD}); the three lead inductances, at the gate (L_G), drain (L_D), and source (L_S); and the parasitic resistances, primarily those associated with the gate lead (R_G) and with the drain-source connection, both when the switch is on ($R_{DS,on}$) and when it is off (ESR of C_{OSS}, here referred to as R_{COUT}).

These parameters were all measured so far as feasible prior to final design of the power stage. The methodology for each measurement is described in detail below. The results of these measurements and models are summarized in Table 3.3

Capacitance	C_0	m	ψ
C_{DS}, low voltage	1836.5 pF	0.58215	0.62893 V
C_{DS}, high voltage	1836.5 pF	0.60818	0.4808 V
C_{GD}, low voltage	641.60 pF	1.8809	8.5013 V
C_{GD}, high voltage	641.60 pF	0.92879	0.35942 V

Parameter	Value
C_{GS}	790 pF
$R_{DS,on}$	0.55 Ω
α_{RDSON}	6 $m\Omega/C$
R_{COUT}	0.3 Ω
R_G	120 $m\Omega$
L_D	1.5 nH
L_G	1.3 nH
L_S	1.1 nH

Table 3.3: Measured device parameters, as developed by the author

3.3.1 Capacitance Measurements

The device capacitances were measured using an Agilent 4359A Impedance Analyzer with a frequency range of 100 kHz-500 MHz. Measurements were made across frequency and bias voltage. Because the impedance of the capacitances decreases as frequency increases, and because the impedance analyzer measures impedances most accurately at magnitudes close to 50 Ω, the capacitance measurements were compared at 1.0234 MHz.

The gate-drain and drain-source capacitances in particular vary strongly with drain-source voltage. These capacitances can be approximately modeled by Eq. 3.1, which is appropriate to a reverse-biased PN junction [31].

$$C = \frac{C_{DS0}}{\left(1 + \frac{V_{DS}}{\psi}\right)^m} \tag{3.1}$$

For some models, the drain-source capacitance is also offset by a constant capacitance which is primarily significant at high voltage.

The extracted values are based primarily on two measurements. The first is a measurement between the drain and the source with the gate shorted to the source (C_{OSS}). The second is a measurement between the drain and source with the gate shorted to the drain at frequencies of interest ($C_{(GD)S}$). Both measurements rely on the ability of the impedance analyzer to introduce a dc bias voltage at its measurement terminals.

The listed capacitance values can be approximately extracted from the measurements according to the following equations:
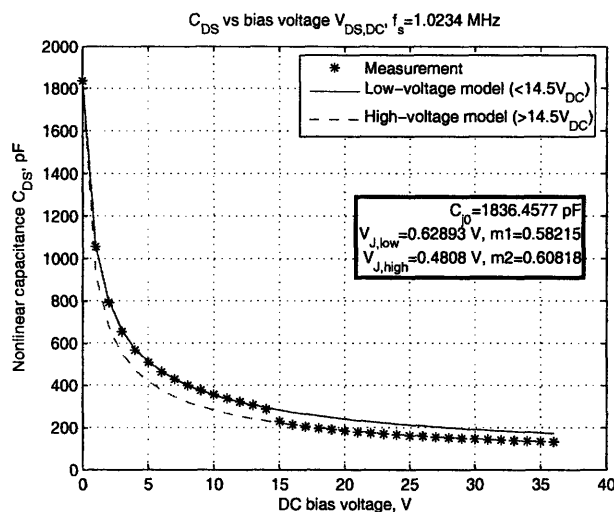
Figure 3.3: Drain-source capacitance vs. drain bias voltage

$$C_{GS} - C_{GD} \approx C_{(GD)S} - C_{OSS} \tag{3.2}$$

$$C_{GS} \approx [C_{GS} - C_{GD}]_{highvoltage} \tag{3.3}$$

$$C_{GD} \approx -[C_{GS} - C_{GD}] + C_{GS} \approx -C_{(GD)S} + C_{OSS} + C_{GS} \tag{3.4}$$

$$C_{DS} \approx C_{OSS} - C_{GD} \tag{3.5}$$

Once the drain-source voltage is quite large, the capacitances level off and so they were modeled as constant above a certain voltage. An unusual discontinuity is present in the drain-source and gate-drain capacitances of the ARF521 at approximately 14.5 V of drain-source bias. The reasons for this are not entirely clear; however, it is present in all components as well as on the part datasheet. In simulations, this was modeled by using two curves and switching from one to the other near the discontinuity. The capacitances were measured and fitted to curves. These curves are pictured in Figs. 3.3 and 3.4.

3.3.2   Resistance Measurements

The value of the on-state drain-source resistance has a pronounced effect on the converter efficiency. This resistance rises with temperature and is a pronounced function of gate-source voltage. The dc value of this resistance was measured by using a 4 wire resistance measurement on a digital multimeter (HP 34401A), and its variation as a function of temperature was evaluated by securing the device to a hot plate. The resistance was measured

C_{GD} vs bias voltage $V_{DS,DC}$, f_s=1.0234 MHz

Measurement
Low-voltage model (<14.5V_{DC})
High-voltage model (>14.5V_{DC})

C_{jo}=641.6015 pF
$V_{J,low}$=8.5013 V, m1=1.8809
$V_{J,high}$=0.35942 V, m2=0.92879
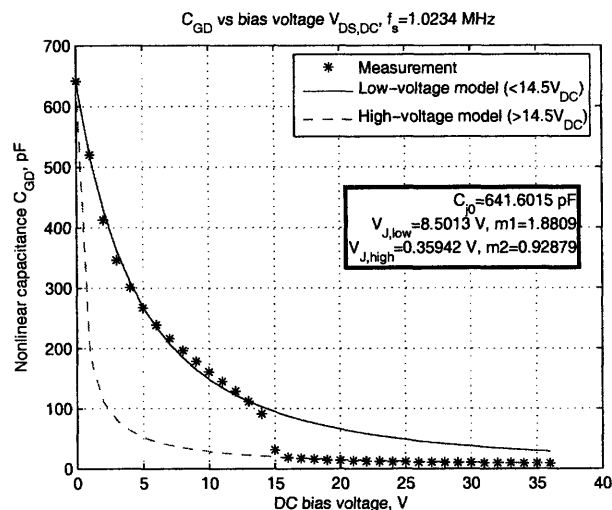
Figure 3.4: Drain-gate capacitance vs. drain bias voltage

for gate-source voltages up to 12 V (using a Tektronix PS2520 programmable power supply) and for temperatures up to 75°C (using a digital hot plate). The measured data are summarized in Figs. 3.5 and 3.6. The measurements indicate a fully-enhanced on-state resistance of approximately 550$m\Omega$ at 17°C and a temperature coefficient of approximately 6.5$m\Omega/°C$.

As was mentioned above, a small gate time constant is necessary in order to rapidly switch the MOSFET. In order to measure this gate time constant, the impedance of the gate-source connection, with the drain left open, was measured. At the self-resonant frequency of the loop, the magnitude of the impedance is approximately equal to the ESR of the gate. That minimum magnitude occurred at approximately 50 MHz, and was measured to be approximately 120 $m\Omega$. This is a somewhat crude measurement, but sufficient to give a good idea of how the device will behave.

Another important equivalent series resistance to measure, particularly for resonant converters, is that associated with the output capacitance. Strictly speaking, there are two lossy capacitances involved - that between the drain and source, and that between the gate and drain. Determining the proportion of loss in each one is difficult, but since the drain-source capacitance is substantially larger than the gate-drain capacitance, and since the gate-drain capacitance is not depended upon for power processing, a reasonable model includes all of the output capacitance losses as part of a single resistor R_{COUT}, which is in series with the drain-source capacitance.

Even then, measuring this resistance is not easy. The total impedance of the output capacitance at frequencies of interest is large compared to the ESR, and so a precise measurement
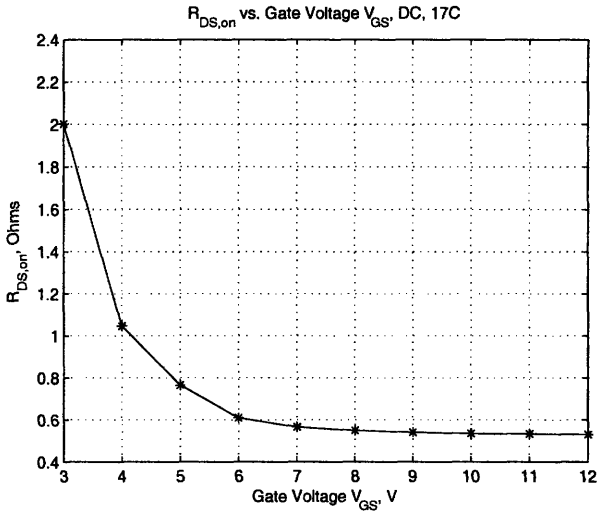
Figure 3.5: Measured on-state resistance vs. gate-source voltage at $17°C$
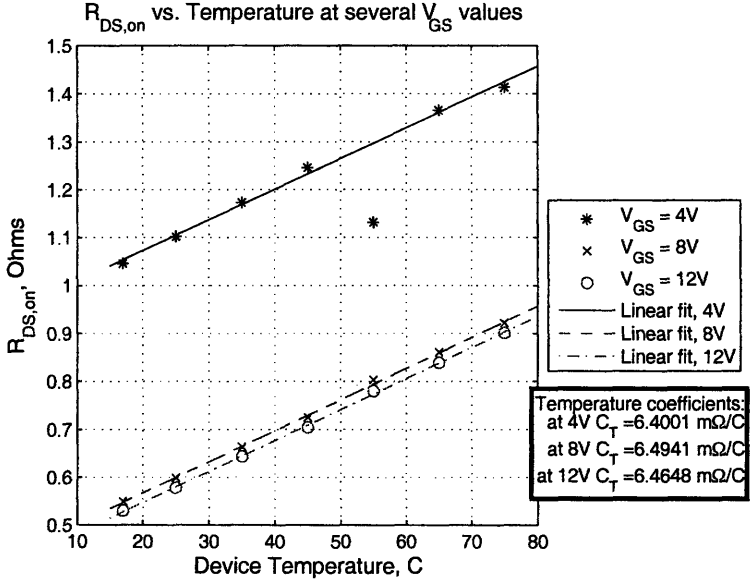
Figure 3.6: Measured on-state resistance vs. temperature

of this resistance requires a precise measurement of the impedance phase. R_{COUT} may thus be measured only moderately well by the available impedance analyzer. After a number of measurements at different bias voltages and temperatures, it was decided that the best approximate value was $R_{COUT} = 0.3\Omega$. Note that this resistance is on the order of the on-state resistance ($R_{DS,on}$) and current through this resistance can account for significant loss.

3.3.3 Inductance Measurements

The measurement of device lead inductances is complicated by their small values. At the frequencies at which the impedance analyzer operates, the impedance of the inductance in any given loop through the device is small or comparable compared to the impedance of the series capacitance of that loop. For this reason, the inductances were determined by measuring the low-frequency series capacitance of the loop and the self-resonant frequency. The extraction was also done with the instrument's equivalent circuit utility, and the values were compared to the inductance measurement at the instrument's highest available frequency (500 MHz).

This package has four terminals, of which two are connected to the source, with one each for the gate and drain. Six measurements are possible - from the drain to each source lead, from the gate to each source lead, between the gate and the drain, and between the two source leads. This results in an overconstrained problem well suited to MATLAB's least-squares fit utility. The measurements can be summarized by the following matrix equation:

$$
\begin{bmatrix}
0 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 \\
0 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 \\
0 & 1 & 1 & 0
\end{bmatrix}
\times
\begin{bmatrix}
L_{S1} \\
L_{S2} \\
L_G \\
L_D
\end{bmatrix}
=
\begin{bmatrix}
3.3nH \\
5.0nH \\
3.6nH \\
3.7nH \\
3.4nH \\
3.1nH
\end{bmatrix}
\tag{3.6}
$$

This results in inductance values of

Capacitance	C_0	m	ψ
C_{DS}, low voltage	1945 pF	0.5640	0.6606 V
C_{DS}, high voltage	3960 pF	0.6923	0.2064 V
C_{GD}, low voltage	546 pF	1.6619	6.1666 V
C_{GD}, high voltage	494 pF	0.5237	0.0232 V

Parameter	Value
C_{GS}	752 pF
$C_{DS}^{highvoltage}$	23 pF
$R_{DS,on}$	0.3 Ω
R_{COUT}	0.3 Ω
L_D	1.5 nH
L_G	1.3 nH
L_S	1.1 nH

Table 3.4: Most recent measured device parameters, as refined by JMR, JR

$$L_{S1} = 2.32nH$$
$$L_{S2} = 2.22nH$$
$$L_S = 1.13nH$$
$$L_G = 1.32nH$$
$$L_D = 1.52nH$$

3.3.4 Later Refinements

After these measurements were complete, while designing and building the power stage and gate drive, some additional measurements were performed by John Ranson and Dr. Juan Rivas. These measurements further refined the model for the ARF521. The best current estimate for the curve parameters and the other measured values are listed in Table 3.4.

Power Stage

This chapter discusses the design, construction, and performance of the power stage of interest in this application. Three prototypes were built to demonstrate the designs, and these are detailed in Section 4.3. The three prototypes were the result of a collaboration between the author and others, most notably Dr. Juan M. Rivas as well as Yehui Han and Prof. David J. Perreault. Much of this material is detailed in [5], and it is included here because of its relevance to the work detailed in other chapters.

A design concern which has not featured in other chapters but which was important for this application is suitability for high-temperature operation. This requirement of the application is not treated in detail, but it defines some of the design choices made in the power stage and so is mentioned here in passing.

4.1 Components

4.1.1 Magnetics

For the frequencies and inductance values of interest, the use of magnetic materials is not particularly helpful. The inductance values necessary are not large enough to require magnetic materials in order for the parts to remain small in size. The Q factor of the air-core inductors is often better than that of cored inductors at frequencies of interest and improves as frequency increases. Additionally, the power (current) rating for these air-core inductors is limited only by the wire gauge and the heat transfer, so high-voltage, high-current parts could be built without difficulty. Air-core inductors are also robust to high-temperature operation, which has little effect beyond increasing equivalent series resistance somewhat.

For simplicity and ease of manufacture, simple solenoids were used for the inductors in these designs. Formulas for approximating the inductance in such solenoids and guidelines for design may be found in [32–34]. In order to construct inductors in a repeatable fashion, threaded Teflon rods were used to form the windings. The Teflon form did not change

the magnetic properties of the inductor. The wire was seated between the threads, and the form kept both the diameter and the distance between windings fixed. The windings could then be glued to the form, either temporarily with hot glue or semipermanently with cyanoacrylate glue.

A peculiarity of working with (unshielded) air-core inductors is that care must also be taken to avoid unintentional flux coupling between different inductors. This was accomplished in this design, first, by keeping the inductors as far from one another as possible. Second, the inductors were positioned so that the main directions of flux of any two were not parallel. Third, each inductor was positioned so that raised conductors, including the other inductors, would not block the magnetic flux and thereby reduce the inductor's Q. This problem could be substantially avoided in a future design by using self-shielding air core inductors - essentially toroid-wound copper. Techniques for building such inductors are developed in [35].

In the high frequency dc-dc design, an autotransformer was used to provide additional impedance transformation. The design of an air-core autotransformer is somewhat more complicated than that of an air-core inductor, although most of the issues constraining air-core design inductors are also relevant to the autotransformer. The design of the auto-transformer is covered in detail in [5].

4.1.2 Switches

The selection and characterization of a MOSFET for use as a main (controlled) switching device is covered in Chapter 3. The ARF521 by Microsemi was in use in all of these designs.

The need to retain the capability for high temperature operation figured strongly into the selection of suitable diodes. Silicon carbide (SiC) devices in principle possess much higher temperature capabilities than their conventional silicon counterparts and so were of interest here. No suitable SiC MOSFETS are currently commercially available, although prototypes were being developed in parallel with this project. However, SiC Schottky diodes are available for purchase. These diodes exhibit somewhat poorer forward drop characteristics than comparable silicon PIN diodes, but the SiC parts were used here because of their high blocking voltage, high temperature capability, and lack of significant reverse recovery.

The diodes selected were the CSD10XXX SiC Schottky rectifier family from Cree. These parts have positive temperature coefficients allowing devices to be paralleled without danger of thermal runaway. Since the rectifier used the capacitance of the diode as a resonant element, modeling its value was important. The CSD10030 was selected for the lower

output voltage design, and the CSD10060 for the higher output voltage design.

4.1.3 Capacitors

In general, capacitors with good high-frequency performance are much more widely available and less expensive than inductors or active parts.

All of the high-frequency capacitors were multilayer porcelain dielectric. Ceramic capacitors are a good compromise between high capacitance and good frequency performance and Q. Many of the capacitors used NP0/C0G dielectric, which has better frequency stability than the X7R materials. Also available were high-voltage P90 ceramic capacitors from American Technical Ceramics.

4.2 Design and Construction

The design procedure of the class Φ_2 inverter is treated at length in [5,11]. The design and construction of the rectifier portion of the circuit, in particular, is not treated here.

All the designs described here were constructed on printed circuit boards (PCBs, 2-layer 0.62 in. FR4). When laying out high frequency circuits, close attention must be paid to the parasitics being introduced in the PCB. Parasitic inductance is particularly detrimental in some circuit loops, and these must be physically tight to minimize that inductance. Likewise, circuit performance is damaged by parasitic capacitance (usually to ground, though sometimes between nodes) at some nodes more than others, and care must be taken to minimize that capacitance. Overall, usually a layout as physically compact as possible is desirable, and usually a ground plane is helpful over most of the board area.

Once a design for the inverter is finalized in simulation and the board is laid out, the circuit is tuned with the help of the impedance analyzer (Agilent 4359A). Besides impedance measurements of individual components, most tuning measurements are made across the drain and source of the main switching device. Once appropriate physical components have been selected, they are themselves measured, along with the parasitic impedance of any particularly sensitive board node or loop. The simulation can then be updated with the newly measured values, and rechecked for operation within specifications. Thereafter, components are mounted one by one, and the impedance of the whole structure is again measured and compared to that predicted by the simulation. Estimated parasitic components can be adjusted to yield a better match between simulation and experiment. Once all the components
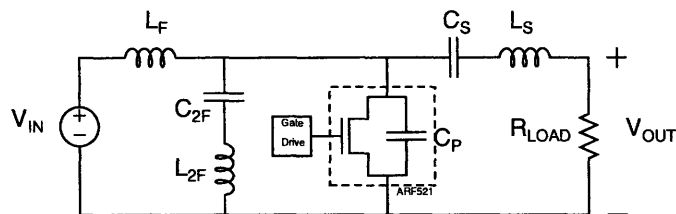
Figure 4.1: Schematic of the 30 MHz inverter as constructed

are mounted and when the simulated and measured impedance values are reasonably well matched, the time domain simulation is once again checked. If the simulation still performs acceptably, then the converter can be tested with a reasonable expectation of success. The time domain simulations often do a fair job of predicting converter transient waveforms, power, efficiency, and other metrics.

This tuning process is somewhat onerous, but it is necessary only during prototyping. Once a design has been finalized and demonstrated, subsequent instances need not be individually tuned.

4.3   Prototypes

4.3.1   High Frequency Inverter

In order to validate the use of the class Φ_2 inverter for this application, and to ease the construction process, a prototype of the inverter stage only was constructed. This was fed into an RF resistor load. This prototype could be used to measure the voltage waveforms at all nodes to determine if the system was working properly. The schematic of the inverter is shown in Fig. 4.1

The inverter is tuned to drive a resistive RF load of 33Ω. This was provided by three 100Ω resistors in parallel. The RF resistors available were RA1000-150-4Y 150 W 5% parts. They had measured resistances which varied from 100Ω by less than 0.5% at 25 C and had temperature coefficients of approximately $4.2m\Omega/C$, based on measurements performed up to 75 C. The measured data is provided in Fig. 4.2. The three load resistors were mounted on a printed circuit board and fixed to a finned aluminum heatsink which was also provided with two Zalman CNPS7700-Cu CPU cooler fans. An approximately impedance-matched interface between the inverter and the load several inches away was provided by the parallel combination of two 75Ω coaxial cables. Photographs of the entire setup are provided in Figs. 4.3 and 4.4.
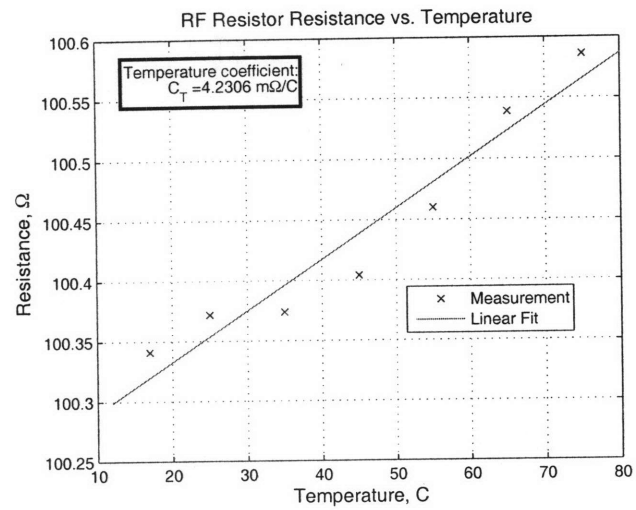
Figure 4.2: Measurements of RF resistors which serve as the load for the inverter
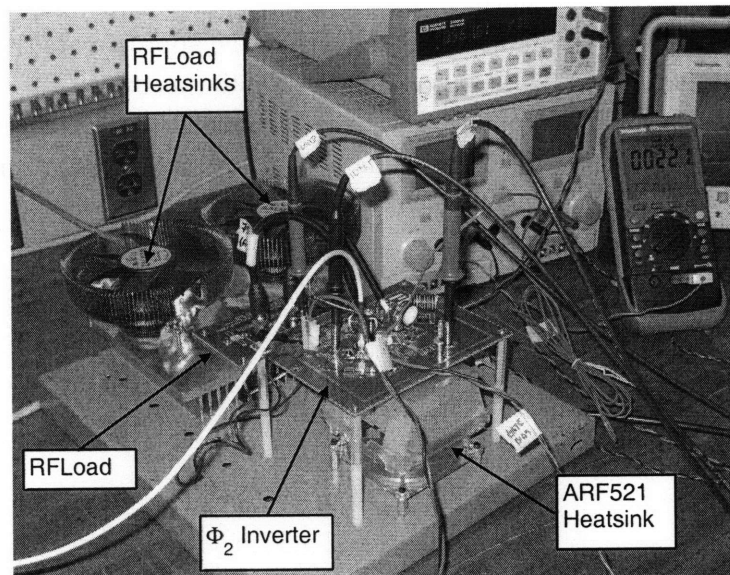
Figure 4.3: Photograph of the high frequency inverter setup. Image courtesy of Dr. Juan Rivas
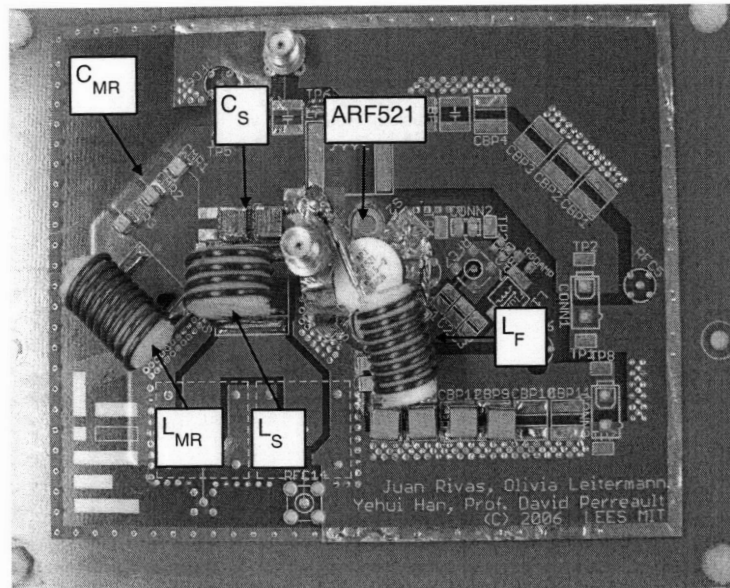
Figure 4.4: Photograph of the high frequency inverter board. Image courtesy of Dr. Juan Rivas

High efficiencies are in general quite hard to measure, and measuring RF power accurately is prohibitively difficult. An attempt was made to estimate the output power based on the voltage measured with the oscilloscope at the load and the (measured) resistance. Unfortunately, realtime measurements of the load resistor operating temperature were not available, so a first-order estimate of power was made using the approximate thermal resistance of the load. The measured load voltage was separated into its constituent harmonics using a fast Fourier transform, and the power delivered to the load was calculated for each harmonic, magnitude $|V|$ and angle ψ. The estimated output power and efficiency for the inverter, based on these calculations, are shown in Fig. 4.5.

$$\Delta T \approx PR_{th} \tag{4.1}$$

$$R \approx R_0 + \Delta T C_R \tag{4.2}$$

$$P \approx \frac{|V|^2 cos\,(\psi)}{R_0 + \Delta T C_R} \tag{4.3}$$

$$P \approx \frac{|V|^2}{R_0 + PR_{th}C_R} \tag{4.4}$$

$$P \approx \frac{-R_0 + \sqrt{R_0^2 + 4R_{th}C_R|V|^2 cos\,(\psi)}}{2R_{th}C_R} \tag{4.5}$$
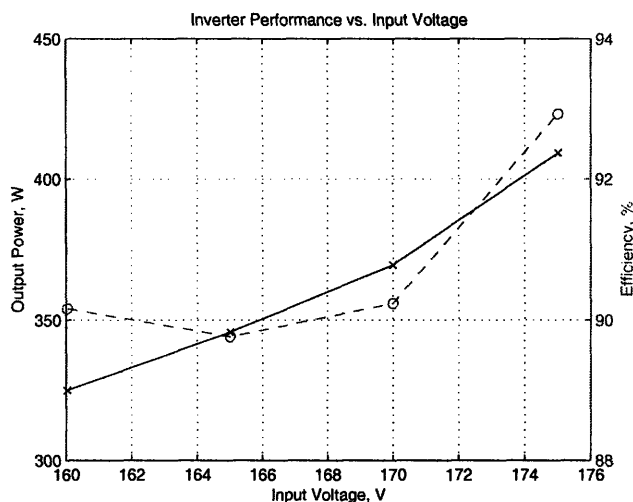
Figure 4.5: Estimate of output power and efficiency for 30 MHz inverter.

Component	Manufacturer	Part Number
Main Switch	Microsemi	ARF521

Inductor	Wire Gauge	Form	No. Turns	Measured L	Measured Q
L_F	AWG 16	3/8" (nom) 14 TPI	8	306 nH	194
L_{2F}	AWG 16	3/8" (nom) 14 TPI	9	414 nH	280
L_S	AWG 16	5/8" (nom) 12 TPI	4	193 nH	190

Capacitor	Manufacturer	Part Number	Nominal Value	Measured Value
C_{2F}	American Technical Ceramics	2 x ATC100B560JW ATC100B390JW	2 x 56 pF 1 x 39 pF	16.3 pF (series combination)
C_S	Cornell Dublier	2 x MC22FD102J-F	2 x 1 nF	2 nF

Table 4.1: Components used for the 30 MHz high frequency inverter-only prototype. Adapted from [5]

4.3.2   High Frequency Dc-dc Converter

Once the inverter had been tested, a prototype of the full dc-dc converter was designed and constructed. The inverter portion of this converter was very similar to the inverter described above. The specifications for the dc-dc converter are listed in Table 4.2. This was the primary design, and was the prototype used to test the gate drive scheme.

A schematic of the full dc-dc converter as constructed is shown in Fig. 4.6. The components used in the converter are listed in Table 4.3. Figure 4.7 shows a photograph of the system with its dc load. Power density calculations performed by Grace Cheung indicated that the prototype delivered 110 W/cu. in. or more (depending on accounting).
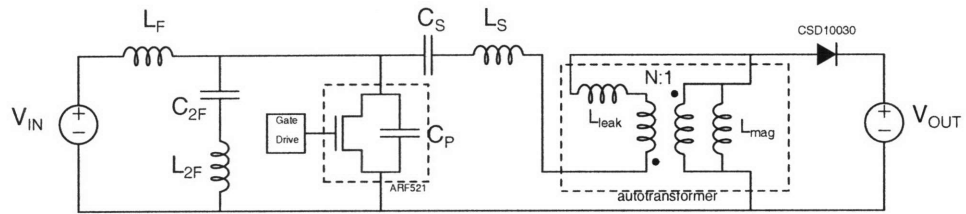
Figure 4.6: Schematic of the 30 MHz dc-dc converter power stage as constructed
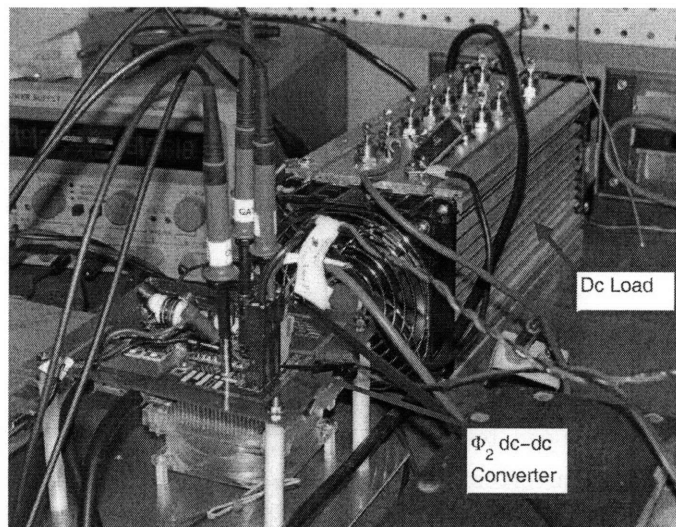
Figure 4.7: Photograph of high frequency converter setup. Image courtesy of Dr. Juan Rivas

Attribute	Specification
Input Voltage	$160 - 200V$
Output Voltage	$33V$
Output Power	$> 200W$
Frequency	$30MHz$

Table 4.2: High-frequency dc-dc converter prototype specifications

Component	Manufacturer	Part Number
Main Switch	Microsemi	ARF521
Diodes	Cree	2 x CSD10030

Inductor	Wire Gauge	Form	No. Turns	Measured L	Measured Q
L_F	AWG 16	3/8" (nom) 14 TPI	9 Turns	384 nH	197
L_{2F}	AWG 16	3/8" (nom) 14 TPI	9 Turns	414 nH	185
L_S	AWG 16	3/8" (nom) 14 TPI	5 Turns	175 nH	195

Capacitor	Manufacturer	Part Number	Nominal Value	Measured Value
C_{2F}	American Technical Ceramics	1 x ATC100B390JW 2 x ATC100B560JW	39 pF 2 x 56 pF	16.3 pF (series combination)
C_S	Cornell Dublier	4 x MC22FD102J-F	4 x 1 nF	4 nF

Table 4.3: Components used for the 30 MHz high frequency prototype. Adapted from [5]

4.3.3 High Efficiency Dc-dc Converter

In order to demonstrate the suitability of the proposed scheme for very high efficiency operation, a dc-dc prototype was built which maximized efficiency. The specifications for this prototype were somewhat different from those for the high frequency prototype and are listed in Table 4.4.

A number of techniques were employed to improve the overall efficiency. The switching frequency was reduced somewhat to 10 MHz, which raised the size of the energy storage components but decreased average currents and thus also resonating losses. Inductor design

Specification	Value
Input Voltage	160-200 V
Output Voltage	75 V
Switching Frequency	10 MHz
Output power	> 200 W
Efficiency	> 90%

Table 4.4: Specifications for the high-efficiency prototype
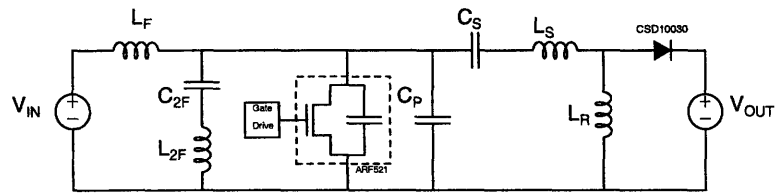
Figure 4.8: Schematic of the 10 MHz dc-dc converter as constructed

was changed, emphasizing high quality factor (Q) over small size. This resulted in larger-diameter coils. Finally, in order to bring the prototype above a symbolic 90% efficiency benchmark, the efficiency penalty due to the diode forward drop was slightly reduced by increasing the output voltage to 75 V. The load also draws less current at this increased output voltage for the same power level, so the resonating losses were slightly reduced. A reduction in conversion ratio also allowed for the removal of the autotransformer which provided a further improvement in efficiency.

The best-available MOSFET and capacitors were already in use, so these components remained largely unchanged. The diodes were retained in the high-efficiency prototype for their high temperature capability. The increased output voltage required the use of a higher-voltage part.

The components used in the 10 MHz high efficiency prototype are listed in Table 4.5. Measured values reflect a combination of the discrete element and some applicable board parasitics, extracted primarily from drain-source impedance measurements. Figure 4.8 shows the schematic of the high-efficiency prototype, which differs from that of the high-frequency converter only slightly. Figures 4.10 and 4.9 show the drain-source voltage waveforms of the converter at either end of the input voltage range. The power and efficiency performance of the converter is shown in Fig. 4.11. The rapid transient response of the converter can be seen in Fig. 4.12. Figure 4.13 shows a photograph of the completed converter board. The drain-source impedance of the converter, used for tuning, is shown in Fig. 4.14. A simulated loss breakdown is shown in Fig. 4.15 and the power loss in the semiconductors (also from simulation) is shown in Fig. 4.16. The code for SPICE simulations is available in Appendix C.3. Much of the efficiency and power measurement and loss simulation was performed by Dr. Juan Rivas. Power density calculations performed by Grace Cheung indicated the prototype delivering 110 W/cu. in. or more (depending on accounting).
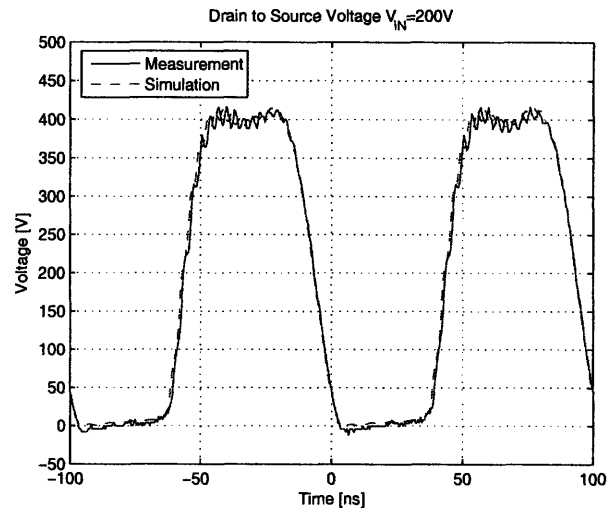
Figure 4.9: Experimental and simulated waveforms of the 10 MHz high-efficiency converter operating at 200 V input.
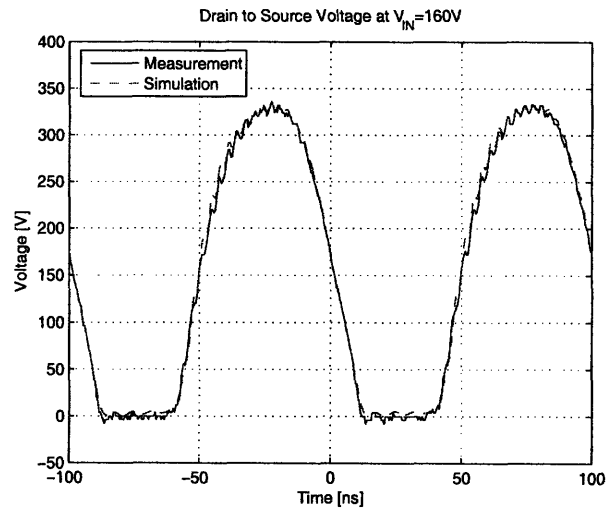
Figure 4.10: Experimental and simulated waveforms of the 10 MHz high-efficiency converter operating at 160 V input.
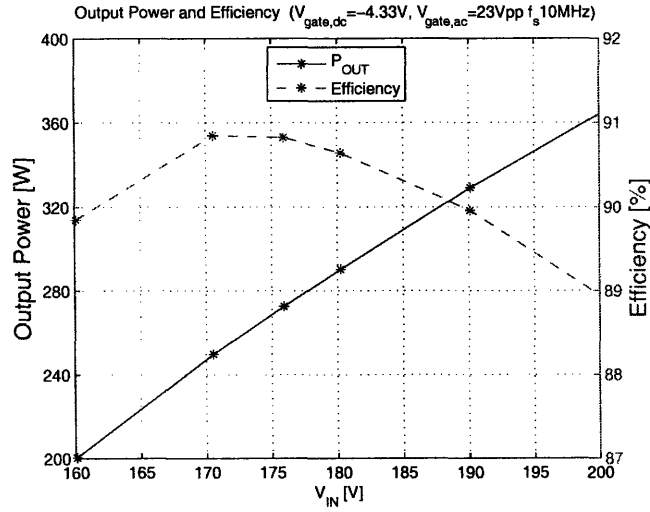
Figure 4.11: Experimental performance of 10 MHz high-efficiency converter.
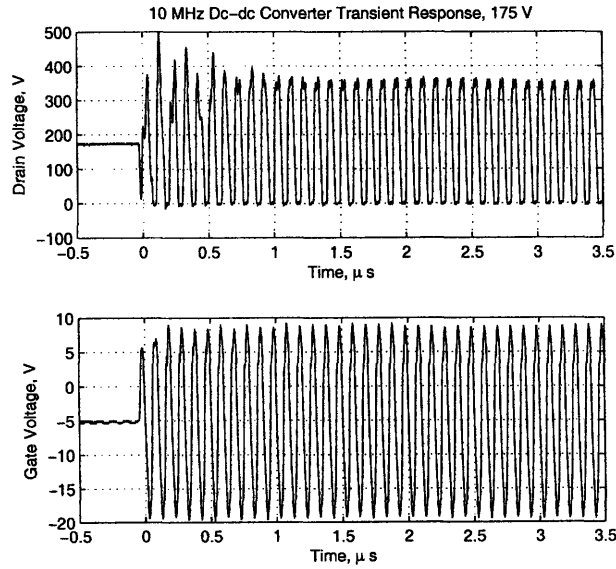
Figure 4.12: High frequency inverter transient response.
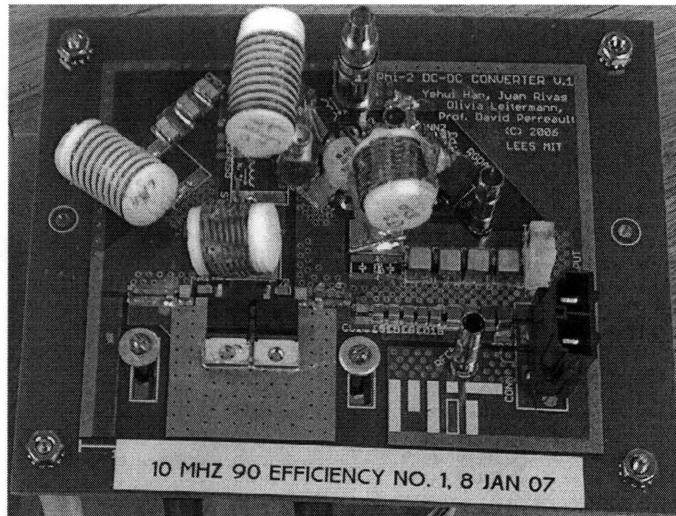
Figure 4.13: Photograph of high frequency dc-dc converter.
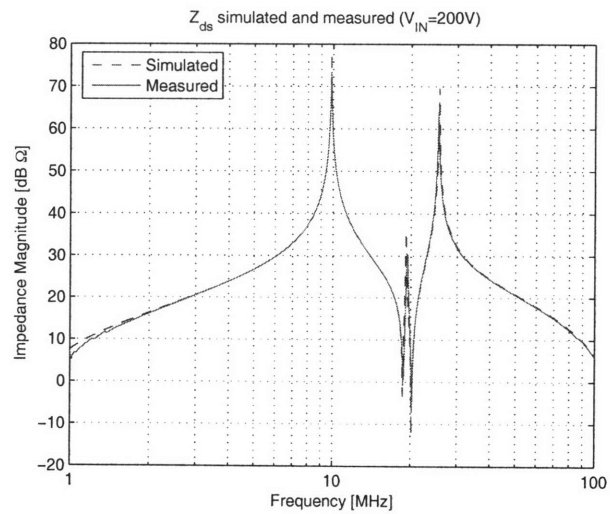
Figure 4.14: Measured and simulated drain-source impedance of 10 MHz high-efficiency converter at 200 V bias.
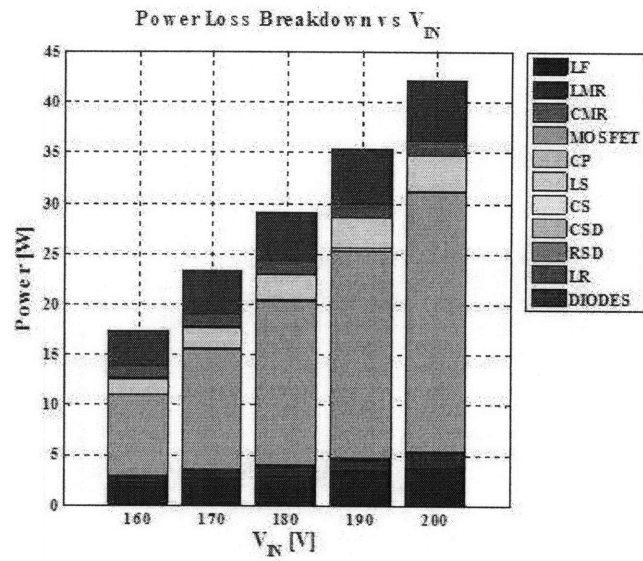
Figure 4.15: Simulated loss breakdown for high efficiency dc-dc converter. Figure courtesy of Dr. Juan Rivas
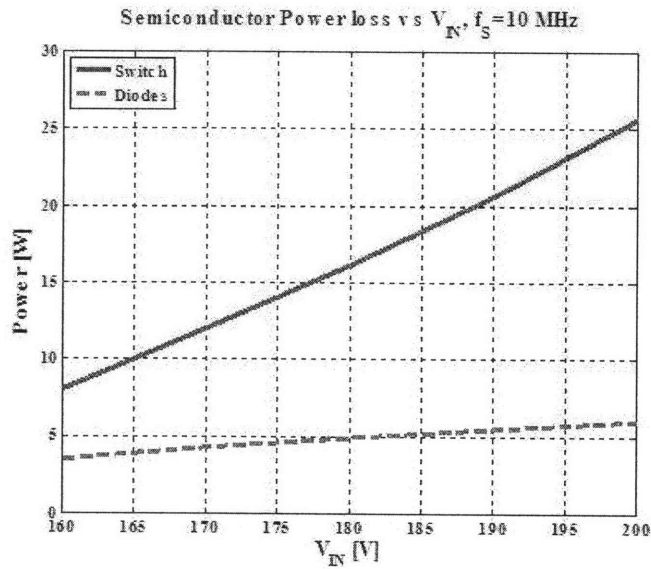
Figure 4.16: Simulated semiconductor loss for high efficiency dc-dc converter. Figure courtesy of Dr. Juan Rivas

Component	Manufacturer	Part Number		
Main Switch	Microsemi	ARF521		
Diodes	Cree	CSD10060		

Inductor	Wire Gauge	Form	No. Turns	Measured L
L_{2F}	20 AWG	5/8" 14 TPI	9	595 nH
L_F	18 AWG	5/8" 22 TPI	8	805 nH
L_S	18 AWG	5/8" 14 TPI	10	722 nH
L_R	16 AWG	5/8" 22 TPI	8	798 nH

Capacitor	Manufacturer	Part Number	Nominal Value	Measured Value
C_{2F}	ATC	9 x ATC100B-101JW	3 x 100 pF / 3	100.8 pF
C_P	ATC	2 x ATC100B-121JW	2 x 120 pF	245.3 pF
C_S	TDK	2 x C3225C0G2E153J	2 x 15 nF	30.0 nF

Table 4.5: Components used for the 10 MHz high-efficiency prototype

Gate Drive

In very high frequency power conversion, driving the switching device(s) fast enough and hard enough is a significant challenge. For example, the large gate capacitances of high-voltage vertical MOSFETS require high currents to switch fast enough. Further complicating the drive is the substantial feedback from the drain voltage through the gate-drain capacitance, especially in high-voltage designs. Additionally, the nonlinearities of all the device capacitances constrain the design of the gate drive. Finally, all these problems must be solved while driving the gate with a total power which is small compared to the output power in order to keep efficiency high.

5.1 Gate Drive Requirements

Building a complete dc-dc converter system with high efficiency imposes several constraints on the gate drive. The most important aspect of the gate drive is the effectiveness with which it switches the main device. Switching must be completed within a small fraction of the total switching period. When the device is on, the gate voltage must be large enough to hold the device in deep triode and obtain optimum switch on-state resistance. The drive must be able to achieve a low (0.3) duty ratio, and some benchtop control of duty ratio is desirable. The gate drive must maintain the gate voltage within its safe operating range. All this must resist the effects of feedback from the drain and nonlinear capacitance. Finally, the total gate drive power must be small compared to the converter output power. The specific targets for the prototype device and power converter are summarized in Table 5.1.

Table 5.1: Summary of Gate Drive Performance Requirements

Attribute	Value
Switching Time	$\ll 33ns$; $\approx 1ns$
Threshold Voltage	$\approx 2.5V$
Target On-state Gate Voltage	$8V$
Gate Voltage Limits	$\pm 30V$
Target Duty Cycle	0.3

5.2 Alternatives Considered

There are many established gate drive techniques for switched-mode power converters, though most are not aimed at high-frequency designs. Several promising gate drive techniques were considered for this application. Additionally, many of these schemes can be combined in various ways, but the approaches are discussed separately here for clarity.

5.2.1 Hard-Switched Drivers

The most common and straightforward solution for gate drives in switching power converters is a hard-switched driver. These drivers are simple and have undergone optimization for some time. Many good hard-switched drivers are available on commercial ICs.

The minimum theoretical gate loss in a hard-switched driver corresponds to the energy required to charge the gate capacitance once per cycle.

$$P_{gate,min} = Q_G V f_{sw} \approx C_{ISS} V^2 f_{sw} \tag{5.1}$$

For an ARF521 MOSFET driven at 30 MHz with 8 V gate voltage, this loss corresponds to only about 1.5 W, which is small compared to the converter output power. Unfortunately, the best commercial RF gate drivers achieve fast switching times by allowing some shoot-through loss, and as a result their power requirements are too large for a 200 W converter. For example, the power dissipation of a commercial hard-switched RF driver such as the IXYS DEIC420 is prohibitively large ($> 50W$) for a 200W dc-dc converter [36]. While the performance of this driver is probably sufficient for this application, its power requirement makes it unsuitable. Furthermore, this hard-switched driver requires more power and is able to switch less effectively as frequency increases, e.g., in a future design.

5.2.2 Half-Resonant Driver

One alternative for gate drive is the half-resonant driver [20]. This topology, illustrated in Fig. 5.1, stores energy in an inductor and uses that to ring charge on to the gate capacitance. When the current in the inductor falls to zero, the diode turns off and the gate is held high. The gate will remain high until the auxiliary switch turns on again, shorting the gate and dissipating the energy stored there. The length of the turn-on transition can be controlled by the resonant frequency of L_{ghr} and C_g.

ARF521 Gate Model
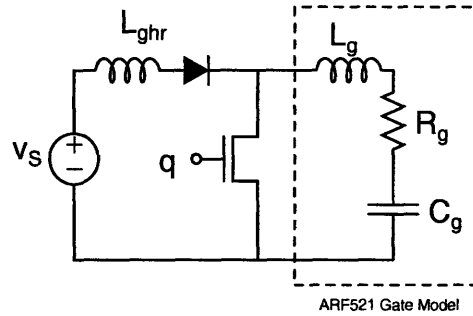
Figure 5.1: Half-resonant gate drive schematic.

The half-resonant driver features only resonant components for low energy storage, and startup may be achieved within one cycle. The number of components is minimal. The theoretical minimum loss is half that of a hard-switched driver, under the condition that the loss in resonantly charging the gate capacitance is small compared to the energy stored in the gate capacitance. Since the auxiliary switch dissipates all the gate energy each cycle, provision must be made for the dispersal of this heat. Changing the duty cycle at constant frequency changes the ratio between the gate supply voltage and the peak gate voltage because the inductor ramp-up time is changed.

A difficulty with a half-resonant converter is caused by the rapid switching transitions and current commutations. The inductor current must commute between the switch and the gate capacitance, and the gate is switched from its maximum value to ground. These rapid transitions excite resonances among the parasitic elements of the circuit, including the gate inductance, the auxiliary switch capacitance, and the diode capacitance. Also worrisome are the relative values of the resonant inductor and the parasitic inductances. In order to achieve a fast turn-on time with a large gate capacitance, the resonant frequency of the gate capacitance and the resonant inductance L_{ghr} should be faster than the switching frequency. For a gate capacitance of about 1 nF and a 3 ns rise time, $L_{ghr} \approx 4$ nH, which is only slightly larger than the parasitic gate-source loop inductance. This leads to the conclusion that the half-resonant driver is not appropriate for this application.

5.2.3   Half-Sine Driver

A related option for high frequency gate drive is a half-sine driver, pictured in Fig. 5.3. This topology is similar to the half-resonant driver, but uses the resonance of the added inductance with the gate capacitance to ring charge both on and off the gate. In this way, much of the power from the gate is recovered to the supply each cycle. The duty ratio of the driver is controlled by the resonant frequency of the added inductance L_{ghs} with the
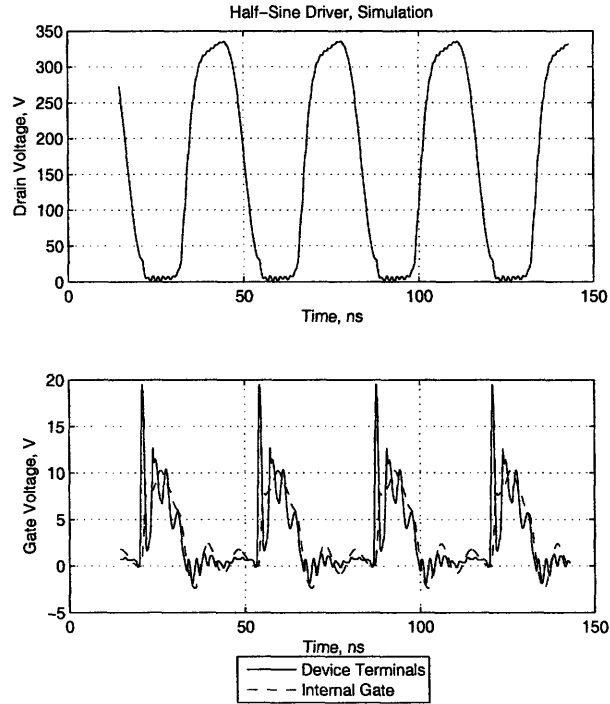
Figure 5.2: Simulated waveforms for half-sine gate drive. 30 MHz, 3 V dc input, $L_{ghs} =$ 5.77 nH, 3.7 W from dc supply.

gate capacitance C_g and cannot be altered without changing the inductance.

Unlike the half-resonant drive, this topology exhibits zero-voltage switching, turning on the auxiliary switch when the voltage is low and raising the voltage slowly after turn-off. However, it still requires the current from the inductor to commute quickly between the switch and the capacitance. These fast switching transitions can cause large ringing voltages due to the series inductance of both the auxiliary switch and the gate capacitance as well as the parasitic capacitance of the auxiliary switch. In SPICE simulations, this caused a ringing of the gate voltage during the off state which approached the threshold voltage of the main MOSFET. The SPICE results are pictured in Fig. 5.2. This design, at 30 MHz, used a dc input voltage of 3 V and dissipated a total of under 4 W. The SPICE code which generated the simulation may be found in Appendix C.4.

5.2.4 Sinusoidal Resonant Driver

An often-attractive option for high frequency gate drive is a sinusoidal resonant driver, as in Fig. 5.4. This scheme uses the gate capacitance of the main switching device along with an
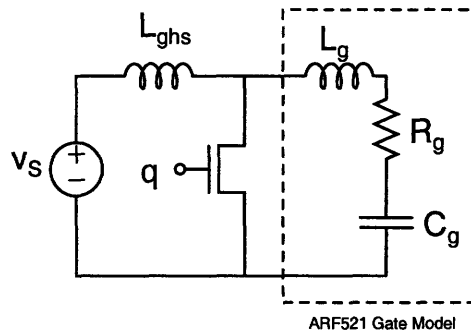
Figure 5.3: Half-sine gate drive schematic.
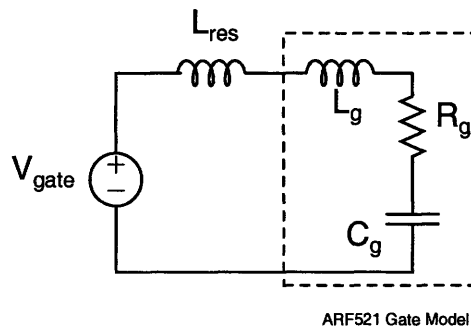
Figure 5.4: Sinusoidal resonant gate drive schematic.

external inductor to cause the circuit to resonate at the switching frequency. This resonance provides voltage gain at the fundamental between a driver and the gate, and allows recovery of the energy used to bring the gate voltage high.

A sinusoidal driver has several advantages for high-frequency operation. There are no rapid switching transitions that require large pulses of current and prompt ringing among parasitic energy storage elements. The switching transition is accomplished where the slope of the sinusoidal drive is approximately greatest. A blocking capacitor may be introduced to change the duty ratio achieved across a substantial range. The parasitic inductance of the gate may be absorbed into the resonant inductor, mitigating its negative effect on the circuit.

The peak voltage required with a sinusoidal drive is somewhat larger than with a square-wave or quasi-square wave drive. It also has substantial negative excursions, making this scheme unsuitable for driving devices with a protection diode limiting negative gate voltage. This scheme has not addressed the problem of feedback from the drain through the reverse transfer capacitance.
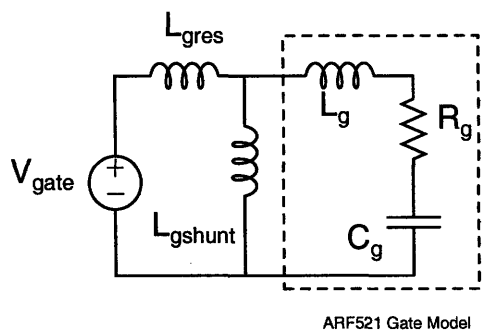
Figure 5.5: Sinusoidal resonant gate drive schematic with shunt leg.

A resonant driver incorporates some manner of driver structure such as a square-wave inverter. This external driver initiates the sinusoidal oscillations seen at the gate, and must carry the full gate current. This can be a major disadvantage if the driver has even a moderate output resistance. One way to circumvent this problem is to add a shunt inductor to the circuit, as indicated in Fig. 5.5 [10,11,26]. In this design, the two inductors are tuned to have a combined inductance which resonates with the gate capacitance at the switching frequency. (The inductors can be considered in parallel if the driver can be thought of as a voltage source). The shunt inductor is made smaller than the series inductor, causing it to carry the greater part of the gate current. This allows most of the reactive energy necessary to drive the gate to be carried through the shunt inductor, freeing the external driver to supply primarily real power.

Unfortunately, the drive requirements for the sinusoidal driver are still significant. If it is to be driven itself by a hard-switched driver, it draws approximately 0.3 A peak. In order to control duty ratio, this must either be supplied by a positive/negative driver with variable supplies or by adding a blocking capacitor with a (negative) bias on the gate. If this drive were supplied by the DEIC420, the power requirement could be estimated at upwards of 20 W [36]. While this is an improvement over a pure hard-gating scheme, it is still large compared to the output power.

A hard-switched sinusoidal driver was simulated, and the resulting waveforms may be seen in Fig. 5.6. This driver uses a 37 nH shunt inductor and a 250 nH series inductor, driven by totem pole switches. The SPICE code for the simulation may be found in Appendix C.5.

5.2.5 Self-Oscillating Driver

By intentionally feeding back the drain voltage to the gate, using the gate-drain capacitance, sometimes in combination with an external network, it is possible to cause the gate to
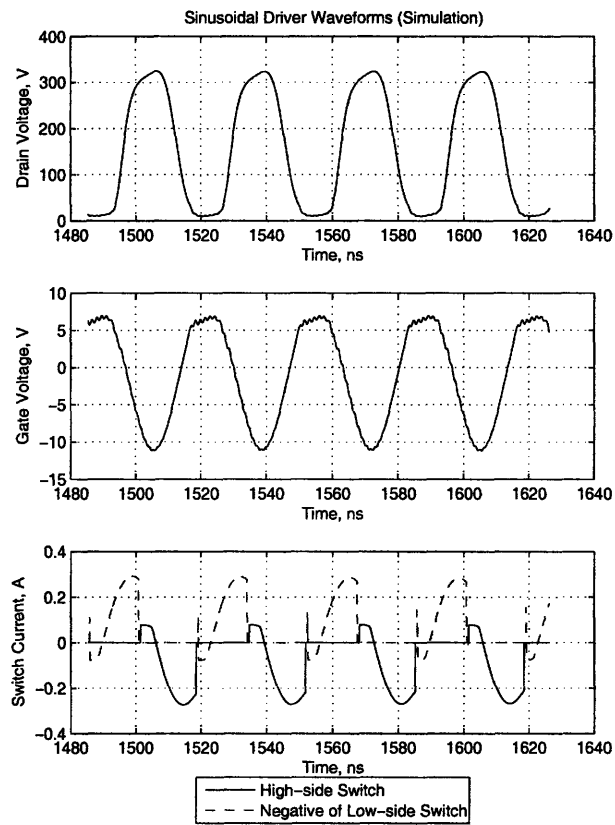
Figure 5.6: Simulated waveforms from a sinusoidal resonant gate drive driven by a a hard-switched totem pole inverter.

oscillate spontaneously at the switching frequency. Examples of this approach are described in [5,24]. This scheme in particular can be used to support a sinusoidal gate drive, as in [11].

This approach is attractive because it absorbs the effects of the often-troublesome reverse transfer capacitance and uses them for circuit operation. It has a small to moderate parts count, and is comprised almost entirely of passive elements, requiring no additional RF switches. The gate drive draws very little power. While startup and shutdown require special attention in a self-resonant circuit, reliable fast solutions for these are possible.

The biggest problem with a self-oscillating gate drive for this application is the large difference in magnitude between the gate drive voltages and the drain voltages. In [24], the peak drain voltage is twice the gate breakdown voltage. Here, the peak drain-source voltage is approximately 15 times the gate-source breakdown voltage. In this application, the input voltage also varies over a substantial range, and the feedback from the drain will vary with this input voltage. Furthermore, the low impedance of the gate constrains the possibilities for impedance shaping. The nonlinearity of the gate-drain capacitance combined with the lack of an analytical description of the drain waveforms of the power stage makes shaping the feedback to the gate difficult. A self-resonant gate drive scheme was not feasible in simulation for this design.

5.2.6   Drain Waveform Driver

This thesis studies a class of resonant inverters that generate drain waveforms which have properties similar to those desired in a gate drive. The drain waveforms have fast rise times and peak voltage values much greater than their dc supply voltages. The topologies are designed to incorporate a certain amount of capacitance between drain and source. Using the drain waveforms of a smaller inverter as a gate drive is an attractive option. The inverter can then be run into a high-impedance dummy "load" to complete the waveshaping. This scheme was successfully implemented in [5, 10, 37] where gate-source voltage was restricted to positive values.

The class Φ_2 converter, with its quasi-trapezoidal waveforms, has obvious advantages as a drain waveform gate driver [1]. However, other resonant converters are also of interest. The second harmonic class E converters under study are another choice.

Unfortunately, the extreme large combined gate-source and drain-source capacitance makes the design of a gate drive inverter of this sort infeasible. Peak voltage is limited by the

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[1] Trapezoidal waveforms are the theoretical ideal gate drive waveforms for linear gate capacitances. This argument is made in more detail in [5].

breakdown voltage of the gate as well. A further problem with the drain waveform driver in this application is caused by the parasitic gate inductance. The path from the drain of one switch to the gate of the other and back between the sources necessarily will imply a significant amount of inductance which is not addressed by the topology. There is danger of significant ringing around this loop and between the inductive parasitics and other circuit capacitances. Not only might such ringing interfere with proper circuit operation, sufficient ringing would bring the device into its linear region during the off state or into cutoff while current was flowing, and thereby dramatically change the power stage drain voltage waveforms. Finally, drain waveform drivers are not conducive to benchtop duty cycle variation without swapping out or tuning resonant components, making it difficult to achieve the proper duty cycle for the power stage.

5.2.7 Multistage Resonant Driver

In many fields, including RF amplifiers and digital drives, the use of multistage amplifiers or drives is a standard technique to deliver additional power gain, and it is a technique conducive to achieving the current gain necessary here.

Here we focus on the family of switched-mode single-switch resonant inverters that have been considered for the power stage. Just as a resonant switched-mode inverter is an effective way to supply power at 30 MHz, it is likewise an effective way to supply power to the gate at 30 MHz. These inverters can be designed to deliver any amount of current to the gate. Most of these topologies incorporate a resonant output tank which can absorb the gate inductance L_G and prevent it from interfering with the circuit. A number of topologies are available, with a range of resonant element values.

These topologies do introduce a good deal of complication. The process of tuning a resonant gate driver is at least as complicated as that of tuning the power stage. It may in fact be more so, if the inflexibility and nonlinearity of the passive elements embodied by the main switch are considered. The design of such a gate drive is made more difficult by the same factors that make it difficult to drive the gate in other fashions, particularly the low impedance of the gate capacitance. Finally, introducing a resonant gate drive inverter necessitates some structure to drive the gate of that gate drive inverter.

The primary inverters under consideration for the gate drive stage were the same as those investigated for the power stage. Some of the requirements are very similar. The inverter must be suitable for high frequency operation. A fast transient response is required because any delay in the gate drive stage will be in series with delay in the power stage, making low energy storage valuable. The power and voltage requirements are very different, as are the

suitable switches.

The class Φ_2 inverter is a promising choice for driving a sinusoidal output tank. A blocking capacitor can introduce a bias voltage to control duty cycle. However, the tuning process of the class Φ_2 inverter is complex and best practice tuning methods were still under development at the time of this work.

The second harmonic class E discussed in Section 2.6 [2, 3] is another option to drive a sinusoidal output tank. It had the advantage of a somewhat more well-defined design process. The larger peak drain voltages of class E style waveforms are not detrimental in a lower-voltage gate drive. The second harmonic class E inverter also has the advantage that impedance measurements for tuning can be made across the output (gate) port rather than across the drain-source, and so only one terminal pair need be readily accessible.

5.3 Scheme Selected

A multistage gate drive was implemented. In this driver, a small, hard-switching tapered inverter (the "hard-switching inverter") drives a larger resonant inverter (the "resonant drive inverter"), which in turn drives the gate of the main inverter switch via a matching network.

Schematics for the hard-switching inverter are shown in Fig. 5.7, while schematics for the resonant drive inverter are shown in Fig. 5.8. As will be shown, this structure is suitable for efficiently developing the required drive waveforms.

5.3.1 Hard-switched Stage

Use of a hard-switched inverter as a first driver stage is attractive because the resonant drive inverter it feeds operates at substantially lower voltage and power levels and has much smaller capacitances than the main resonant inverter. As illustrated in Fig. 5.7, the first stage drive includes an oscillator feeding a single CMOS gate whose output is modulated by an enable signal (providing a means for on-off control). This single gate in turn drives a stack of eight CMOS logic inverters in parallel, providing a tapered drive. The drivers were paralleled to reduce the drive resistance and to decrease the power requirement from each part [11]. The gate drive may be turned on or off with a logic-level ENABLE signal brought onto the board by an SMA connector. This feature is important for implementing on-off control in the future.
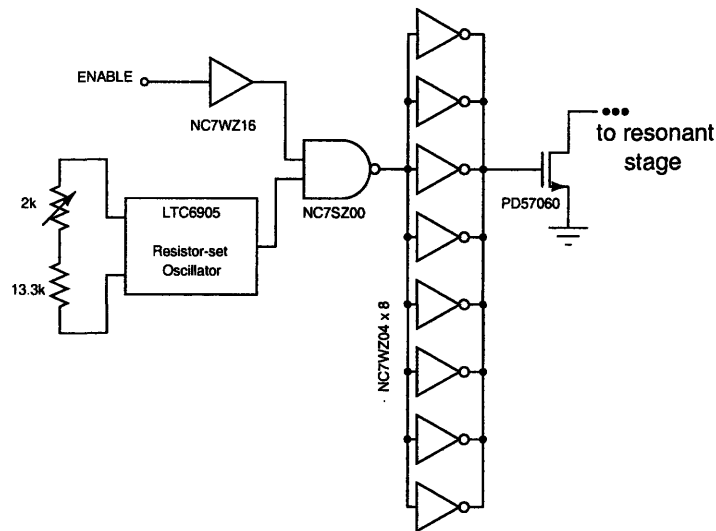
Figure 5.7: Auxiliary Hard-Switched Driver.
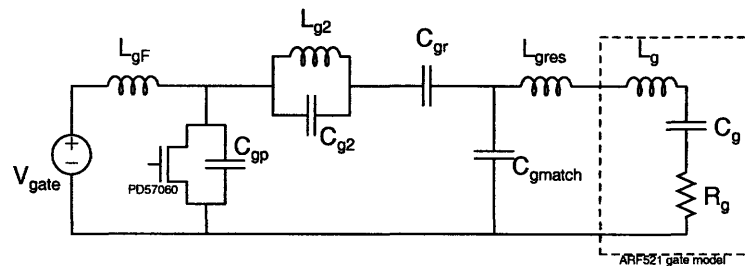
Figure 5.8: Resonant Second Harmonic Class E Gate Driver.

5.3.2 Resonant Gate Drive Stage

The CMOS hard-switched inverter drives the gate of the resonant drive inverter (Fig. 5.8), which is a second-harmonic class E inverter [2,3]. The second harmonic class E topology is also discussed in the context of the power stage in Chapter 2.

The second harmonic class E inverter is well suited to this problem. It includes only resonant components, which for this design can be made to be reasonably sized. This low energy storage is conducive to the fast start-up necessary for on-off control of the power stage. It is well-suited to driving low impedances, which is convenient given the very low gate resistance. A further convenience is the position of many of the resonant elements between the drain of the auxiliary device and the output to the gate, which enables tuning by measuring the impedance at the output port.

The second harmonic class E converter is designed to drive moderately small resistive im-
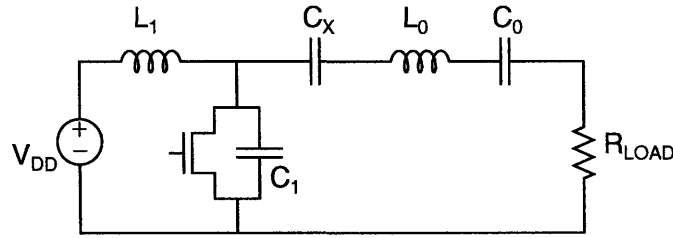
Figure 5.9: Schematic of Grebennikov Second Harmonic Class E Inverter [3].
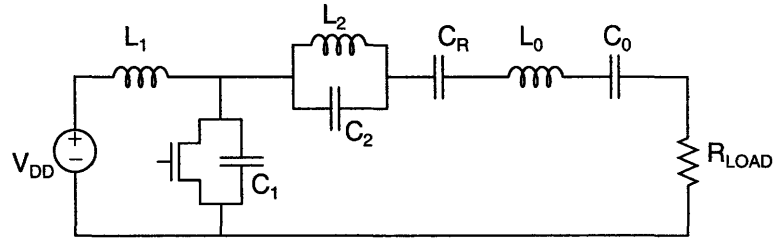
Figure 5.10: Schematic of Iwadare Second Harmonic Class E Inverter [2].

pedances via a resonant output tank. In the context of a gate drive, the gate capacitance can be absorbed into, or even comprise, the resonant output capacitance. The remaining gate resistance comprises the inverter load. This resistance is quite small and a converter design based on this resistance and on the amount of power that might be expected if the gate is driven to appropriate voltages results in inconveniently small inductors and large capacitors. This can be remedied by using an L-section matching network [38] to step up the impedance at the switching frequency. If a dc-pass matching network is used, the series inductance of the matching network can be combined with the resonant tank inductance and comprise a single physical inductor.

Two somewhat different versions of the second harmonic class E were investigated here. The version put forward by Grebennikov et al. [3] is indicated in Fig. 5.9, and that described by Iwadare et al. in [2] can be seen in Fig. 5.10. The Grebennikov converter includes fewer components, but this also makes the inverter more dependent on its output tank for waveshaping. If the loaded Q of the output network is not sufficiently large, ensuring output currents which are much more sinusoidal, the drain voltage waveform is corrupted. A simulation describing this effect is shown in Fig. 5.11. If the device gate capacitance is used as the entire resonant tank capacitance, then the loaded Q of the output tank is fixed (and is approximately 25). This makes the Grebennikov inverter unsuitable for this application, where spectral purity is of little consequence.

In contrast, the Iwadare version of the second harmonic class E inverter contains a parallel resonant tank in the power path to control impedance as well as a series resonant output

Effect of Q_L on Grebennikov Waveforms, Simulation
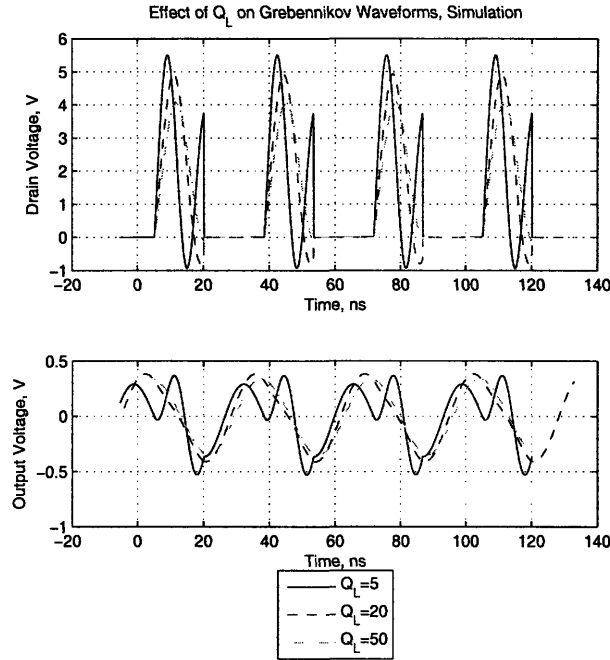
Figure 5.11: Effect of loaded Q on Grebennikov Second Harmonic Class E Inverter waveforms (Simulation) [3].

tank. Waveshaping is accomplished primarily by components other than the output tank, giving this topology a great deal of load insensitivity. For these reasons, the Iwadare second harmonic class E inverter was selected as the gate drive inverter.

5.4 Gate Drive Design

Some high-quality parts for lower power high frequency resonant inverters were available as a result of the work described in [11, 39]. This work sought an optimal RF MOSFET for use in very high frequency (VHF) class Φ_2 inverters. The PD57060 is a 65 V breakdown MOSFET with moderate capacitances. A previous gate drive design in [11] used CMOS inverters from the Fairchild TinyLogic family stacked in parallel to provide lower output resistance and to reduce the power dissipation of each part. These inverters were found to be a good choice for the drive of the auxiliary (gate drive) switch.

The inductors used in the gate drive were air-core solenoids from Coilcraft. At 30 MHz, the properties of magnetic materials are poor, and the inductance values required for the resonant design here are small enough to be implemented with air-core coils of a moderate size. Air-core inductors can be built with high Q that increases with frequency, and are
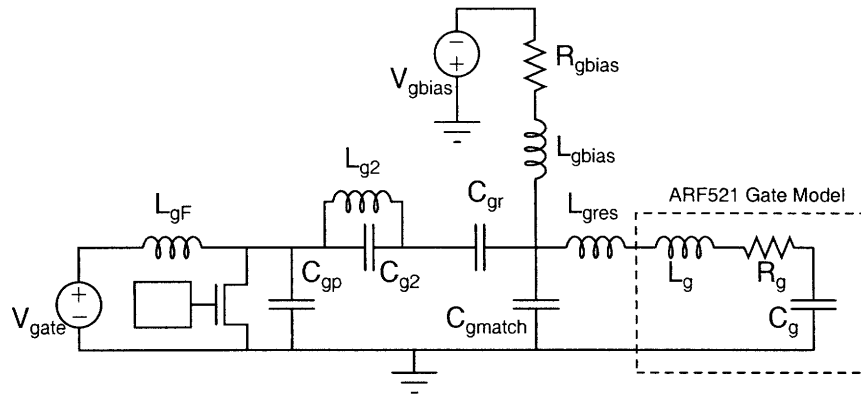
Figure 5.12: Schematic of gate drive resonant inverter stage, including biasing.

free from saturation limitations. The choice of air-core inductors in high frequency designs is also discussed in Section 4.1.1.

For the voltages of the gate drive, ceramic capacitors are available in many sizes and values. Surface mount chip capacitors with NP0/C0G dielectric were selected for their frequency stability and high Q. Surface mount capacitors also have very little equivalent series inductance, leading to self-resonant frequencies well above the frequencies of interest.

The design also included a bias at the output which enabled benchtop tuning of the duty ratio. This was implemented by coupling a negative bias supply to the gate at dc with a large impedance at frequencies of interest, as shown in Fig. 5.12. Very little current flows from this supply. It was also necessary to bypass the bias, logic, and resonant power supplies with larger ceramic capacitors, and to add a bypass capacitor to each digital gate part.

Table 5.2 contains the values and part numbers of the parts used. The components used to bypass power supplies and logic parts are listed in Appendix A.1.

5.5   Gate Drive Construction

The gate driver was constructed on a PCB (4-layer 0.62 in. FR4) designed to be soldered on to the gate terminal of the ARF521 main switching device on the 30 MHz dc-dc converter. This avoided the necessity of building a new power stage prototype on a new board which included a gate drive stage. In a future implementation, it is probably advisable to lay out the power stage and gate drive stage on the same PCB. The masks for the gate drive PCB may be found in Appendix B.1. A photograph of the finished gate drive board is pictured in Fig. 5.13.

Table 5.2: Components Used in Gate Drive

Device	Manufacturer	Part No.
Oscillator	Linear	LTC6905
NAND Gate	Fairchild	NC7SZ00M
Hard-switching Inverters	Fairchild	NC7WZ04
Auxiliary Switch	ST Micro	PD57060

Component	Value	Part No.	Measured Value
L_{gF}	68 nH	1812SMS-68N	72.5 nH
L_{g2}	16 nH	2508-16NJL	16.2 nH
C_{g2}	417 pF	GRM1885C2A391JA01D + GRM1885C2A270JA01D	445 pF
C_{gr}	220 pF	C1608C0G2A221J	209 pF
L_{gres}	≈ 25 nH	Custom 1812SMS-33N	-
C_{gmatch}	3 x 1 nF	3 x ATC100B102KW	3.26 nF
L_{gbias}	2 x 538 nH	2 x 132-20SM-L	-
R_{gbias}	2 x 1.5 kΩ	2 x RR08P1.5KDCT-ND	-

Supply	Value
V_{gate}	11.8 V
V_{logic}	4.8 V
V_{gbias}	-12.5 V
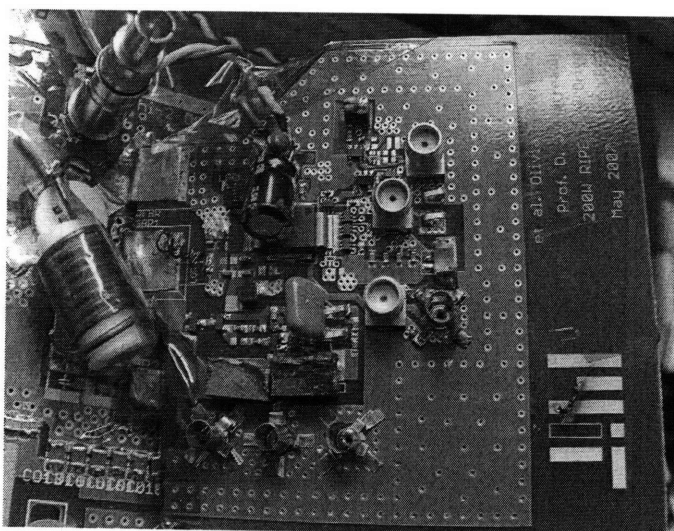
Figure 5.13: Photograph of the completed gate drive board, connected to the dc-dc converter.

The board layout considerations for the gate drive are very similar to those for the power stage, as described in Section 4.2. Namely, minimizing unwanted parasitic inductance and capacitance is of great importance. In particular, care was taken to make the loop around the switch, C_{g2}, C_{gr} and C_{gmatch} as physically small and as low-inductance as possible. Parasitic capacitance between the interconnection of L_{g2}, C_{g2}, and C_{gr} and ground is also of particular concern, and so the ground plane below this node was cut away to minimize that capacitance. Parasitic capacitance between other nodes and ground was much less important, as most other nodes have resonant capacitance to ground of which the parasitic would be a small part. Similarly, the amount of parasitic inductance in series with the resonant inductors of the circuit is of much less importance. The top copper layer was used for all of the resonant interconnections, with the second copper layer used for a ground plane. The logic signals of the hard-switched driver and the biasing circuit were also routed primarily on the top copper layer, with some signal and power interconnect moved to the third copper layer. Additionally, some signals were brought out on the third copper layer for measurement. The bottom copper layer was used as an additional ground plane.

The construction process for the gate drive was also very similar to that for the power stage (Section 4.2). Once a satisfactory simulation had been achieved, passive components were selected and measured with the impedance analyzer. The values for the resonant components, as determined by measurements of both the components and the board, are listed in Table 5.2. The components were then added to the gate drive board one at a time, and the impedance was measured after each addition and compared to simulation, with the simulation updated to reflect board parasitics. Figure 5.14 shows the simulated auxiliary drain waveform, the power stage gate waveform, and the power stage drain waveform. The corresponding SPICE code may be found in Appendix C.7.

Prefabricated passive components are available in only a discrete array of values, and this can be a problem if small-value tuning of the circuit is required. To achieve continuous tuning of the circuit, the output inductor L_{gres} was adjusted by separating its coils after removing its plastic sheath. This lowered its inductance to find the point where the load matching was best, but also lowered the inductor Q. A serious drawback of this method is that the deforming operations are not repeatable, and when tuning it is difficult to go back to a previous configuration. An alternative is to use a line of tuneable air-core inductors (Unicoil 5 mm series, also from Coilcraft) which may be adjusted by raising and lowering a slug of threaded aluminum, thereby blocking some flux. This design also results in lower inductor Q than that of the air-core coil with the slug removed.
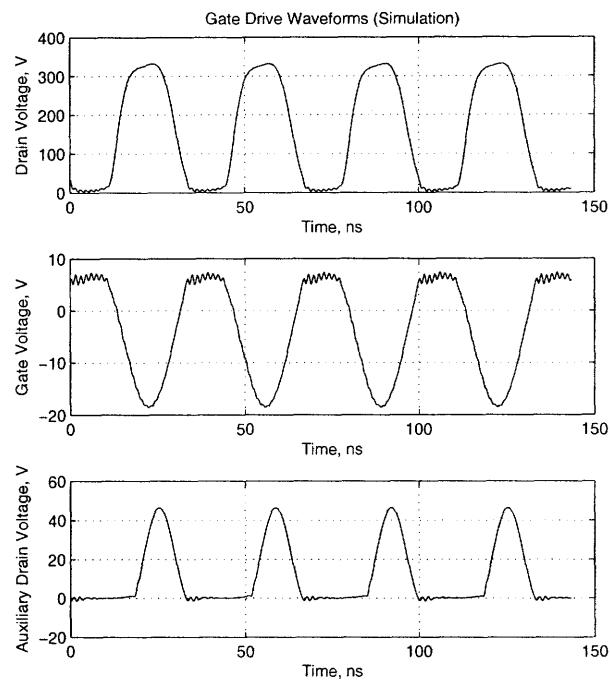
Figure 5.14: Simulated voltage at drain of auxiliary (gate drive) switch, at gate of main switch, and at drain of main switch.
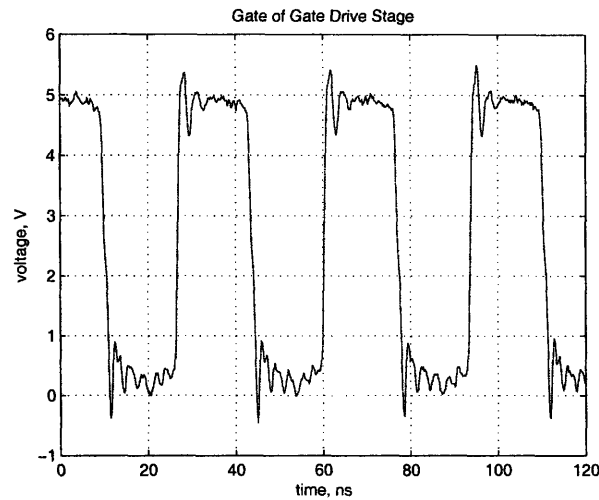
Figure 5.15: Voltage at gate of auxiliary (gate drive) device.

5.6 Performance

The series of voltage waveforms present in the multistage gatedrive is pictured in Figs. 5.15 through 5.18. Figure 5.15 shows the output of the hard-switched first stage. Figure 5.16 shows the drain waveforms of the auxiliary second harmonic class E gate drive inverter, which look like standard class E drain waveforms, switching at approximately zero voltage. The gate drive waveform of the power stage (and the output of the gate drive inverter) is shown in Fig. 5.17. Note the rapid switching times and the substantial gate voltage in the middle of the on state. Finally, Fig. 5.18 shows the drain waveforms of the power stage. As can be seen from the low voltage during on state, the switch is fully enhanced. Figures 5.19 and 5.20 compare the performance of the system, in terms of drain efficiency and output power, respectively, running with the gate drive as described here and with the gate driven by a power amplifier in preliminary testing. No gate losses are included in this figure for either drive. The gate drive required an input power of approximately 7 W, with approximately 6 W of this being drawn by the resonant inverter and approximately 1 W drawn by the hard-switched inverter.

5.7 Approach for Closed-loop Operation

In general, this design should be amenable to closed-loop operation, although this was not complete at the time of this thesis. A startup anomaly was observed in the gate drive circuit and has not yet been remedied, but is not believed to be fundamental. It is expected that
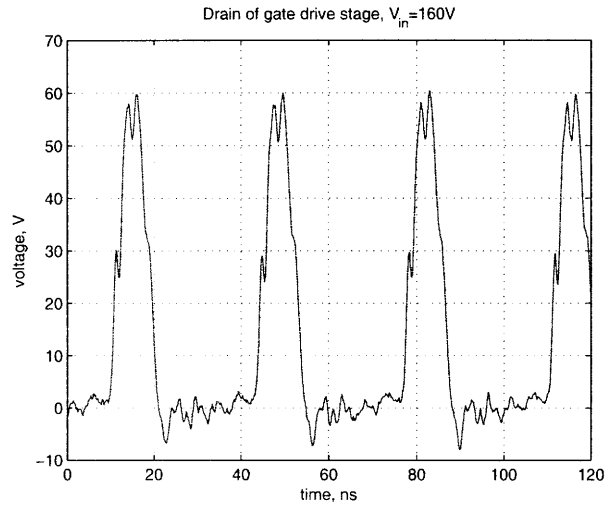
Figure 5.16: Voltage at drain of auxiliary (gate drive) device.
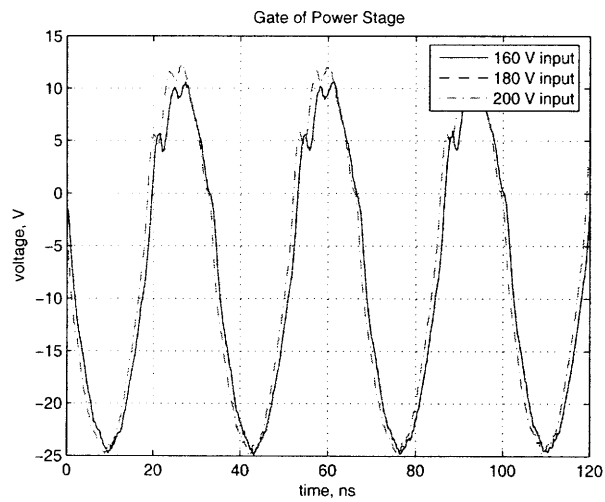
Figure 5.17: Voltage at gate of power stage device.
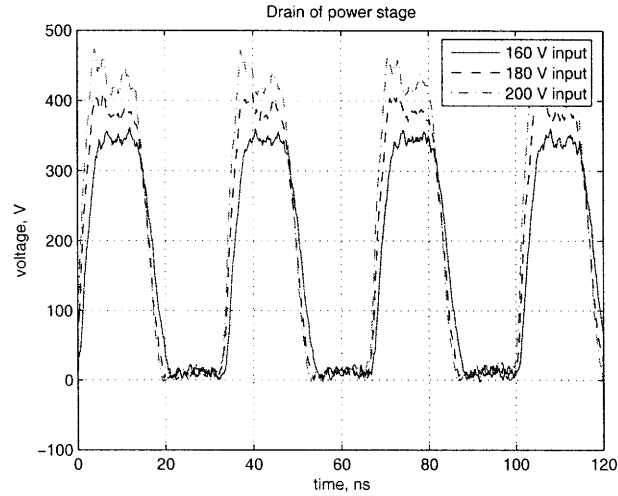
Figure 5.18: Voltage at drain of power stage device.
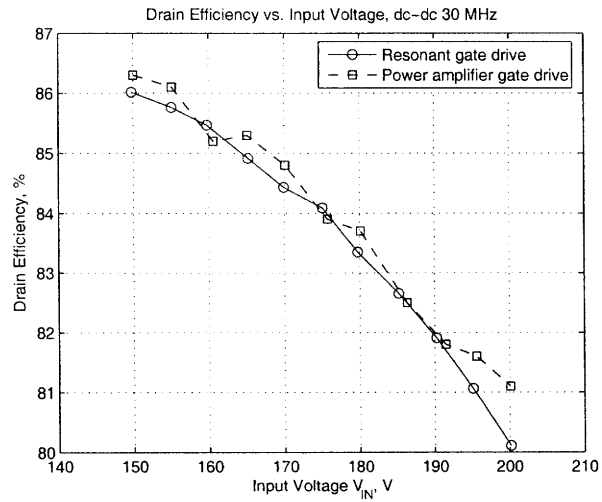
Figure 5.19: Drain efficiency of power stage, driven with power amplifier and with the gate drive of Chapter 5.
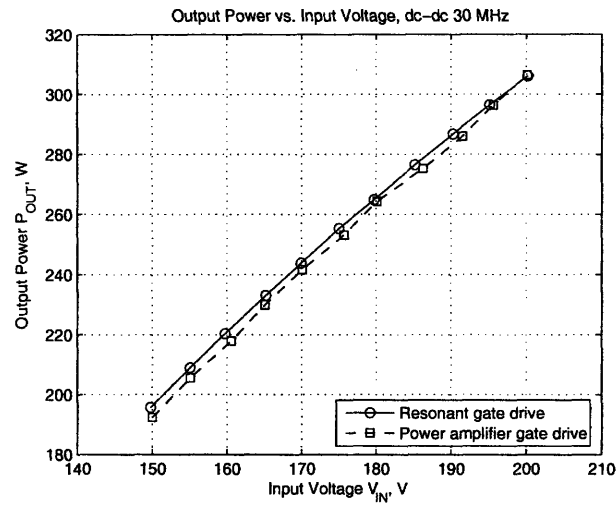
Figure 5.20: Output power of power stage, driven with power amplifier and with gate drive of Chapter 5.

it will be possible to use on-off control on the circuit, as in [5, 7, 11, 39]. The circuit and PCB used for [11, 39] with some modifications for voltage levels and frequency may prove an appropriate control board.

Chapter 6

Conclusions and Future Work

6.1 Objectives and Contributions

High frequency power conversion is attractive for the opportunities it affords for improved performance. This thesis addressed issues critical to design of high frequency switched mode dc-dc resonant power converters. Dc-dc converters operating at high frequencies use smaller-valued energy storage elements, which tend to be physically smaller and lower-cost, and this can result in improved transient performance while retaining high efficiency. One way to achieve high switching frequencies is by using resonant inverter and rectifier topologies and regulating voltage via on-off control.

This scheme requires a great deal of investigation of design practices appropriate to high frequency power conversion. The design issues were investigated for a 200 W 160-200 V input 33 V output converter. A comparison of resonant inverter topologies for the power stage was made. Appropriate devices were sought, compared, and characterized. A high frequency gate drive scheme for a large vertical MOSFET was developed. Several prototypes were built and these are also presented.

6.2 Future Work

A primary concern for future work on this topic is the refinement of the gate drive design and the implementation of closed-loop control. Achieving closed-loop load regulation with the high frequency dc-dc converter prototype is an important step in proving the efficacy of the system. In future prototypes, it may also be possible to make a modest reduction in the amount of power drawn by the gate drive. Some advantages could be gained by implementing power, gate drive, and control stages on a single printed circuit board and providing for the auxiliary supplies.

From a broader perspective, this work should facilitate the future design of high frequency power converters by addressing some of the primary difficulties. This could be of use in

applications where fast transient response or miniaturization is desired or where magnetic materials are not well-suited.

Gate Drive Bypass Parts

Table A.1: Parts used for bypass of gate drive.

Supply	Bypassing
V_{gate}	2 x 0.047 μF X7R + 2 x 8.2 nF C0G + 2.2 μF leaded tantalum + 330 μF leaded electrolytic
V_{logic}	2 x 0.047 μF X7R + 2 x 8.2 nF C0G + 0.1 μF X7R for each logic part
V_{gbias}	2 x 0.047 μF X7R + 2 x 8.2 nF C0G + 1 μF X7R + 22 μF leaded ceramic monolithic

PCB Layout

B.1   Gate Drive Board

B.2   Inverter and Dc-dc Boards

The layout for these boards is available in [5] and is not reprinted here.

MIT LEES   May 2007
200W RIPE Gate Drive
Prof. D. J. Perreault
Olivia Leitermann et al.
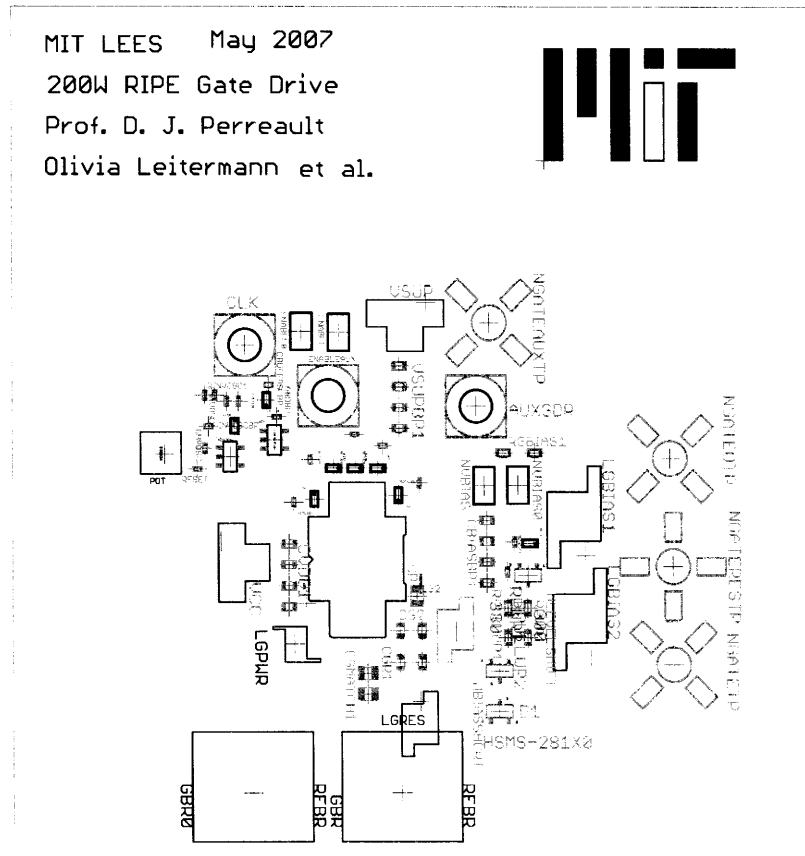
Figure B.1: Silkscreen layer of gate drive board.
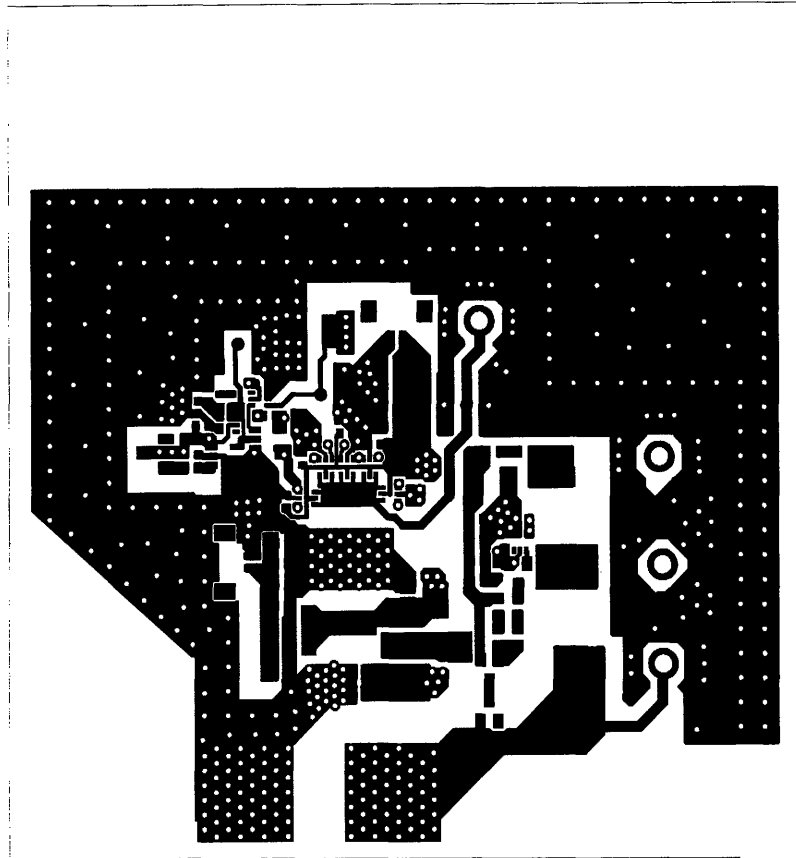
Figure B.2: Top copper layer of gate drive board.
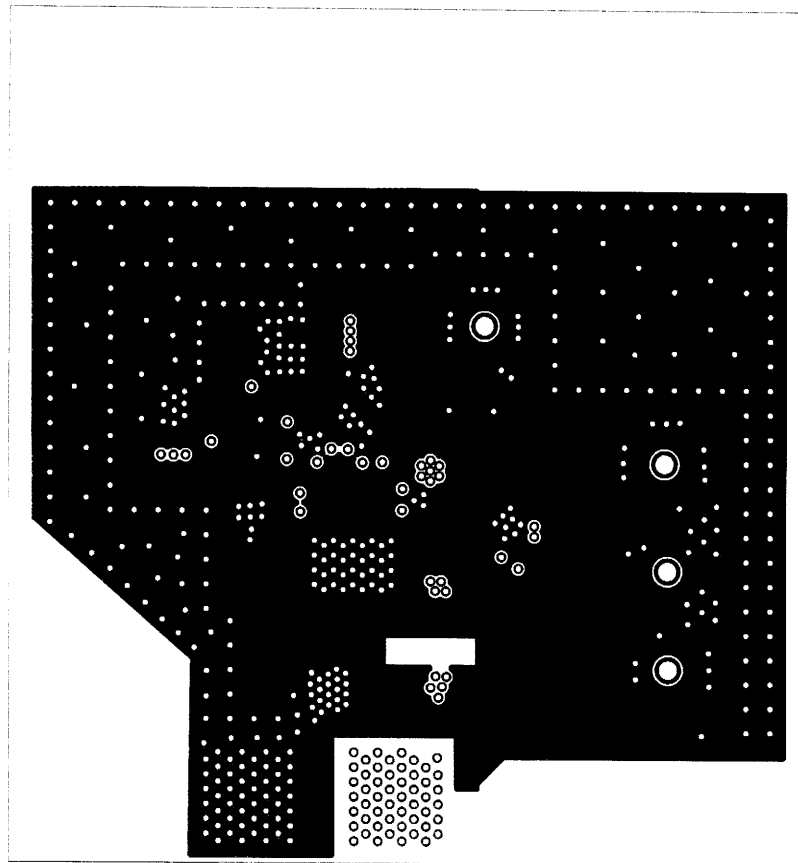
Figure B.3: Second copper layer of gate drive board.
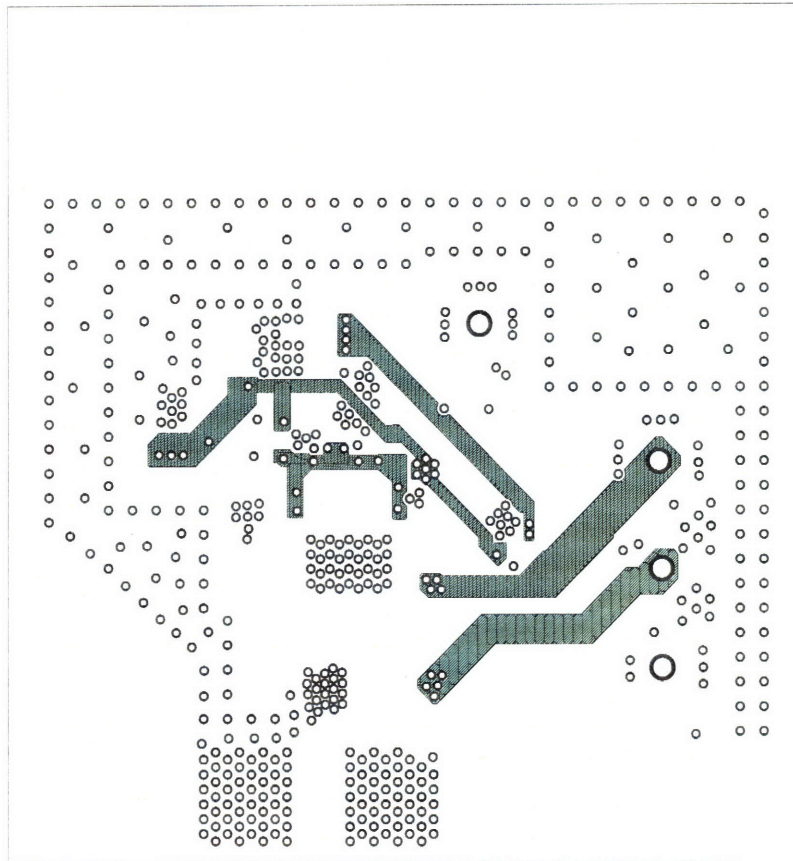
Figure B.4: Third copper layer of gate drive board.
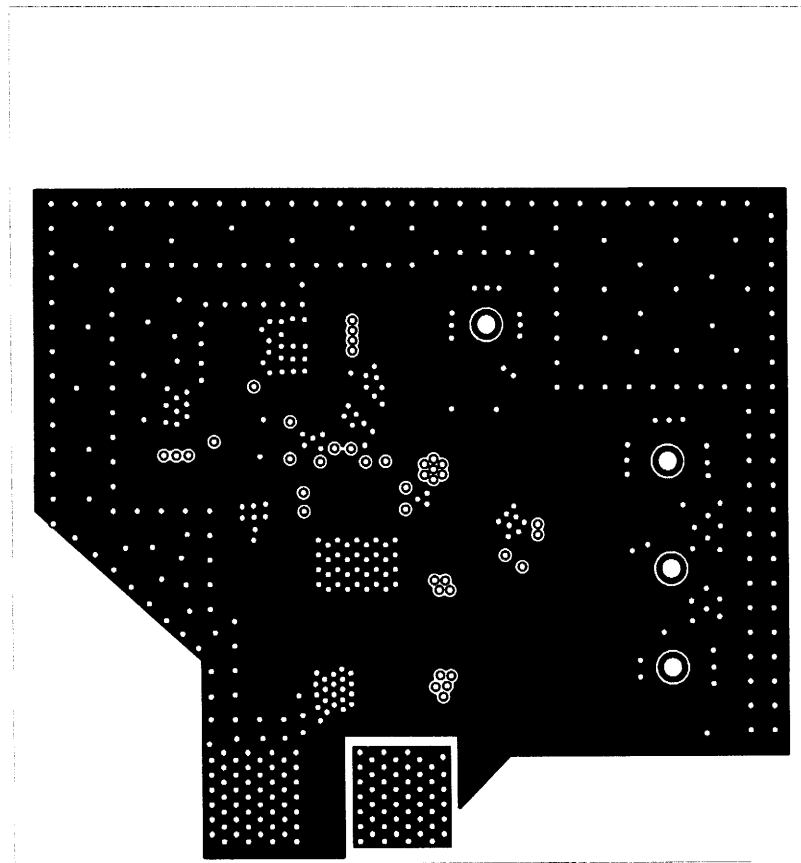
Figure B.5: Bottom copper layer of gate drive board.
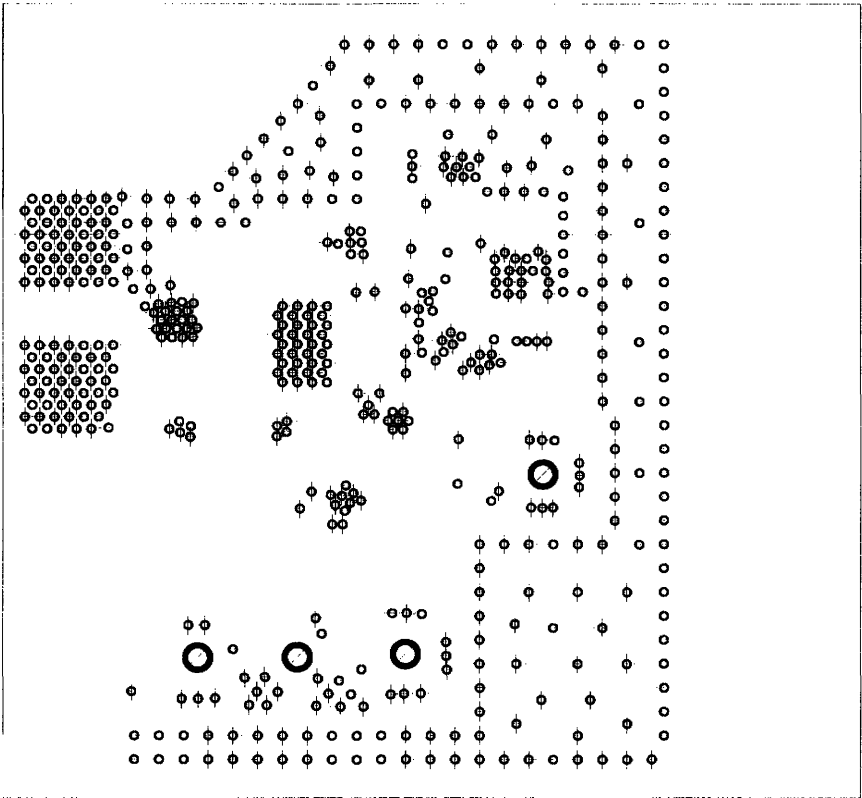
Figure B.6: Drill map, vias, and through-hole pads of gate drive board.

SPICE Simulation Code

C.1 Introduction

This appendix lists the SPICE code for all of the simulations pictured in this thesis. The code was run on Orcad PSPICE or on LTspice.

C.2 Second Harmonic Class E Inverter

```
secondE_firstcut_27sep05v1.cir
```

```
***************************************************
*** CIRCUIT FILE FOR TRANSIENT ANALYSIS OF THE      ***
*** ADIMENSIONAL CONVERTER STRUCTURE                ***
***                                                 ***
*** TRANSIENT SIMULATION V1.0                       ***
***                            ***
*** MADE BY: JUAN RIVAS               ***
*** CAMBRIDGE,MA 8/20/2004                   ***
***************************************************

**modified 8july05 by olivia leitermann
**to determine feasibility of using class phi converter
**for ripe pipp project

****modified 22 july 05 by olivia leitermann
****to determine feasability of using lumped multiresonant
****network in class phi converter

***modified 26 sep 05 by olivia leitermann
***to look at second harmonic class E inverter
```

```
**************************
*** LIST OF LIBRARIES   ***
**************************
.LIB "C:\Documents and Settings\Vivian\My Documents\My
Projects\DARPA RIPE PIPP\pspice\juan's libraries july05/CLASSE.LIB"
;LIBRARY OF CLASSE COMPONENTS  (included; change the path as
necessary)


***********************************************************
**** OPTIONS REQUIRED TO AVOID CONVERGENCE PROBLEMS   ***
***********************************************************

.OPTIONS ABSTOL=1nA +            GMIN=1p +            ITL1=6000 +
ITL2=4000 +           ITL4=5000 +          RELTOL=0.001 +
VNTOL=0.001mV .OPTION STEPGMIN


*********************************************
*** OPTIONS TO KEEP A SMALL OUTPUT FILE ***
*********************************************

.OPTIONS + NOPAGE + NOBIAS + NOECHO + NOMOD + NUMDGT=8 .WIDTH
OUT=132 ;TO PRINT MORE COLUMNS


*********************************************
*** SPECIAL PARAMETERS AND CONSTANTS    ***
*********************************************
.PARAM + PI=3.14159    ;GUESS WHAT


***********************
* CIRCUIT DESCRIPTION      *
***********************

***************given ckt specs
.PARAM +FS=10MEG ;SWITCHING FREQUENCY +Pout=200 +w={2*pi*FS}
+VINcalc=240;INPUT VOLTAGE for calculating designs +Vin=240;
+Qc=2000    ;capacitor Q +Qi=160 ;inductor Q; kinda high for now

*************me-defined parameters to play with
.PARAM +Ql=7   ;tank LOADED Q +duty=.47    ;duty cycle

**************self-defined parameters from equations
.PARAM +Cout=24.83p    ;switch output capacitance
+R={1/18*Vincalc^2/Pout} +C1={2/pi/9/w/R}
+L1={1/32/FS*Vincalc^2/Pout} +C1extra={C1-Cout}
```

```
+C2={1/3/(Q1-((32+3*pi^2)/4/pi))/w/R}
+L2={3/4*(Q1-((32+3*pi^2)/4/pi))*R/w} +Cr={1/Q1/w/R} +rdson=0.94
;nominal Rdson value +rcout={rdson/2}
```

```
****************** Circuit Description *************************
```

```
**DC source
```

```
VIN N101 0 {VIN} Rbig N101 0 10g ;big shunt resistance for DC ground
path
```

```
**Switch Parallel Resonant Tank
```

```
XL1 N101 N103 LQS + PARAMS: + L={L1} + QL={Qi} + FQ={FS} + IC=0
```

```
**SWITCH AND GATE DRIVE
```

```
CSW N103 N103a {Cout} RSW N103a   a   {rcout}
**to measure RSW/CSW current:
Vcsw a 0 0
```

```
SIDEAL N103 b GATE 0 SIDEAL
**to measure Sideal current:
Vsideal b 0 0 .MODEL SIDEAL VSWITCH(ROFF=1MEG RON={rdson} VOFF=0
VON=5)
```

```
.PARAM +TR={1/(100*FS)} +PWIDTH={(duty/(FS))-TR-TR} VGATE GATE 0
PULSE(0.1 12 0 {TR} {TR} {PWIDTH} {1/FS})
```

```
**extra, good capacitor in parallel with switch
```

```
XC1extra N103 0 CQS + PARAMS: + C={C1extra} + QC={Qc} + FQ={FS} +
IC=0
```

```
*Second harmonic blocking tank
```

```
XC2 N103 N104 CQS + PARAMS: + C={C2} + QC={Qc} + FQ={FS} + IC=0
```

```
XL2 N103 N104a LQS + PARAMS: + L={L2} + QL={Qi} + FQ={FS} + IC=0
**to measure L2 current:
VL2 N104a N104 0
```

```
**Resonant Series Capacitor
```

```
XCr N104 N106 CQS + PARAMS: + C={Cr} + QC={Qc} + FQ={FS} + IC=0

**Load resistance: just the inverter for now

Rload N106 N106a {R}     ;Resistance required for given output power
(at the fundamental) and loaded Q
**to measure rload current:
VRL N106a 0 0


*************************
***MEASUREMENT CIRCUITS ***
*************************
*hijacked direcetly from juan's phi13 circuit simulation

.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                              ;COMPONENT OF THE MEASURMENT
                              ;CIRCUITS TWO DECADES BEFORE THE
                              ;SWITCHING FREQUENCY

*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n101)*(-I(VIN))} LPI PIN01 PIN {LORC(FS)} CPI
PIN   0 {LORC(FS)} RPI PIN   0   1

*-----OUTPUT POWER MEASUREMENT
EPO PO01 0   VALUE={V(N106)*I(VRL)} LPO PO01 POUT {LORC(FS)} CPO
POUT 0    {LORC(FS)} RPO POUT 0    1  ;OUTPUT POWER

*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}

*----RMS MEASUREMENT SWITCH CURRENT
ERMS1sw RMS1sw 0 VALUE={I(Vsideal)**2} LRMS1sw RMS1sw RMS2sw
{LORC(FS)} CRMS1sw RMS2sw 0    {LORC(FS)} RRMS1sw RMS2sw 0    1
;RMS OUTPUT VOLTAGE ERMS2sw IsRMS 0 VALUE={SQRT(V(RMS2sw))} RRMS2sw
IsRMS 0  1

*----RMS MEASUREMENT SWITCH Capacitor
ERMS1co RMS1co 0 VALUE={I(Vcsw)**2} LRMS1co RMS1co RMS2co {LORC(FS)}
CRMS1co RMS2co 0    {LORC(FS)} RRMS1co RMS2co 0    1  ;RMS OUTPUT
VOLTAGE ERMS2co IcoRMS 0 VALUE={SQRT(V(RMS2co))} RRMS2co IcoRMS 0  1

*----RMS MEASUREMENT L1
ERMS111 RMS111 0 VALUE={I(Vin)**2} LRMS111 RMS111 RMS211 {LORC(FS)}
```

```
CRMS111 RMS211 0    {LORC(FS)} RRMS111 RMS211 0    1 ;RMS OUTPUT
VOLTAGE ERMS211 I11RMS 0 VALUE={SQRT(V(RMS211))} RRMS211 I11RMS 0   1


*----RMS MEASUREMENT L2
ERMS112 RMS112 0 VALUE={I(VL2)**2} LRMS112 RMS112 RMS212 {LORC(FS)}
CRMS112 RMS212 0    {LORC(FS)} RRMS112 RMS212 0    1 ;RMS OUTPUT
VOLTAGE ERMS212 I12RMS 0 VALUE={SQRT(V(RMS212))} RRMS212 I12RMS 0   1


****************************
*HIGH Q BAND PASS FILTERS  ***
****************************

*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM + QBP=100 .FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)} .FUNC
LBPQ(FS,QBP) {QBP/(2*PI*FS)}


*-----FUNDAMENTAL TANK CURRENT
EBP1  BP11  0    VALUE={I(VL2)} LBP1  BP11  BP12  {LBPQ(FS,QBP)}
CBP1  BP12  BP13 {CBPQ(FS,QBP)} RBP1  BP13  0     1


*-----FUNDAMENTAL OF SWITCH VOLTAGE
EBP2  BP21  0    VALUE={V(N103)} LBP2  BP21  BP22  {LBPQ(FS,QBP)}
CBP2  BP22  BP23 {CBPQ(FS,QBP)} RBP2  BP23  0     1


*************************************
*POWER LOST IN INDIVIDUAL COMPONENTS *
*************************************

*---POWER LOST IN L1
EPLL1 PLL1_1 0       VALUE={V(N101,N103)*(-I(VIN))} LPLL1 PLL1_1
PLL1 {LORC(FS)} CPLL1 PLL1  0       {LORC(FS)} RPLL1 PLL1  0
1

*---POWER LOST IN L2
EPL2 PLL2_1 0        VALUE={V(N103,N104)*(I(VL2))} LPL2  PLL2_1
PLL2   {LORC(FS)} CPL2  PLL2  0        {LORC(FS)} RPL2  PLL2   0
1

*---POWER LOST IN THE WHOLE SWITCH
EPLSW  PLSW1 0
VALUE={((V(N103)*I(Vsideal))+(V(N103a)*I(Vcsw)))} LPLSW  PLSW1 PLSW
```

```
{LORC(FS)} CPLSW  PLSW  0            {LORC(FS)} RPLSW  PLSW  0
1
```

```
*---PARAMETER EXTRACTION
VPL1 PL1 0 {L1} VPC1    PC1   0 {C1} VPL2    PL2  0   {L2} VPC2
PC2 0    {C2} VPCr    PCr 0   {Cr} VPRLOAD  PRLOAD 0  {R}
```

```
*FOR VISUAL TRANSIENT SIMULATION
.step param FS list 10meg 20meg 30meg
*.step param Vin 240 300 60
*.step param duty .45 .48 .01
*.step param Q1 5 10 1
.TRAN 30p 10U 9U 10p UIC .PROBE
```

C.3   High Efficiency Converter Simulation

```
Prototype_10MHz.cir
```

```
***********************************************************
*** SIMULATION OF PROTOTYPE  10MHZ PHI-2 CONVERTER    ***
*** BY: JUAN RIVAS, OLIVIA LEITERMANN, YEHUI HAN      ***
***     GRACE CHEUNG, JOHN RANSON, DAVID PERREAULT    ***
*** (c) MIT CAMBRIDGE, MA  2007                       ***
***********************************************************
*---STEP COMMAND
.step param vin   160 200 10
*---TRANSIENT COMMAND
.TRAN 120P 30U 29.5u 120P UIC .PROBE
********************************
***PARAMETERS AND CONSTANTS    ***
********************************
.PARAM: + PI=3.14159265358979    ;GUESS WHAT
*---CONVERTER PARAMETERS
.PARAM: +FS=10MEG   ;SWITCHING FREQUENCY +VIN=160    ;INPUT VOLTAGE
+DUTY=0.3   ;DUTY CYCLE +VOUT=75    ;OUTPUT VOLTAGE +LF=805n
LMR=595n CMR=100.8p CP=245.3p +LS=722n CS=30N  LR=798n +QIND=190
QCAP=10K RDC=5M +CparMR=2.9p CparR=.1p  CparBRD=13.5p RparBRD=3.2
************************
```

```
*LOW ORDER LUMPED NETWORK *
***************************
**---LF LEG
VDULF  NO1 NO2 0 XLF    NO2 NO3 LCHQC + PARAMS: L={LF} QL={QIND}
FQ={FS} RDC={RDC} + ICL=0 EPC=.001P ICC=0 EPR=10MEG
*---INPUT VOLTAGE
VIN    NO3 0   {VIN}
*---MR LEG
VDUMR NO1 NO5 0 XCMR    NO5 NO6 CQL + PARAMS: C={CMR} QC={QCAP}
FQ={FS} ICC={vin} + ESL=1P ICL=0


XLMR   NO6 0 LQCR + PARAMS: L={LMR} QL={QIND} FQ={FS} EPC={CparMR} +
EPR=10MEG ICL=0 ICC=0


VDUZMR NT NO1 0 ;DUMMY SOURCE TO MEASURE THE IMPEDANCE
              ;OF THE LOW ORDER LUMPED NETWORK
***********************
*SEMICONDUCTOR SWITCH  *
***********************
VDUSMOS NO1 NO7 0   ;DUMMY SOURCE TO MEASURE
                    ;THE DRAIN SWITCH CURRENT
XSIMOS    GATE NO7 0 0   ARF521_MOS8r
***********************
*RESONANT LOAD SECTION *
***********************
*---DUMMY TO MEASURE RESONANT LOAD
VDUZL   NT  MO1 0 VDUCP MO1 MO2 0 XCP  MO2 0 CQL + PARAMS: C={CP}
QC=3K FQ={FS} ICC={vin} ESL=4n ICL=0


VDUCS MO1 MO3 0 VDUCSY MO3  MO3Y 0 XCS    MO3Y MO4 CQL + PARAMS:
C={CS} QC={QCAP} FQ={FS} ICC={VIN} ESL=1P ICL=0


XLS MO4 MO5 LQCR + PARAMS: L={LS} QL={QIND} FQ={FS} EPC=.1P +
EPR=10MEG ICL=0 ICc=0
*---RESONANT RECTIFIER
VDUREC MO5 RO1 0 VDULR RO1 RO1X 0 XLREC RO1x 0 LCHQC + PARAMS:
L={LR} QL={QIND} FQ={FS} RDC={RDC} ICL=0 + EPC={CparR} ICC=0
EPR=10MEG Cbrd RO1x RO1y {CparBRD} Rbrd RO1y 0 {RparBRD} VDURECC RO1
RO2x VDUSEC RO2x RO2 0 ;DUMMY SOURCE TO MEASURE SECONDARY CURRENT
XD1 RO2 RO3 CSD10060_v6jan7 XD2 RO2 RO3 CSD10060_v6jan7 VOUT  RO3 0
{VOUT}
***********************
*SINUSOIDAL GATE DRIVE  *
***********************
```

```
.PARAM: DCOFFSET=-4.5 VRFAMP=17


VGATE GATEX 0 SIN (0 {VRFAMP} {FS} 0 0) RPOWER GATEX GATEy 3 CPOWER
GATEY  GATE .6U ic={-dcoffset} VBIAS  BIAS 0 {DCOFFSET} RBIAS  BIAS
BIASY 10K LBIAS  BIASY GATE  100N  ic=0
*---INCLUDE MEASUREMENT FILE
.inc "XFMEAS_TOT.CIR"
**************************************************
**** OPTIONS  TO AVOID CONVERGENCE PROBLEMS   ***
**************************************************
.OPTIONS ABSTOL=10nA GMIN=10p ITL1=6000 ITL2=4000 +
ITL4=5000 RELTOL=0.005 VNTOL=0.06mV .OPTION STEPGMIN
*************************
*** LIST OF LIBRARIES    ***
*************************
.LIB "PIPP022007.LIB"


Tuning_10MHz_final_jmr_nb4_p119.cir


*********************************************************
*** CIRCUIT FILE TO TUNE THE 10MHZ PHI-2 CONVERTER    ***
***                                                   ***
*** CAMBRIDGE,MA 12/23/2006                           ***
*********************************************************


***Includes board capacitance and its associated resistance at
***input to rectifier diodes 4 jan 07


*********************
* SIMULATION CONTROL *
*********************


*---STEP COMMAND
*.step param vin  list 160 200
*.step param vin    160 200 10
*.step param Cmr list 100p 105p
*.step param Lmr list 600n 620n


*---TRANSIENT COMMAND
*.TRAN 120P 35U 33U 120P UIC
*.TRAN 35P 6U 0U 35P UIC


VACT NTX 0 {vin} AC 1 LACT NTX NTY {LACT} RACT NTY NT {RACT} .AC DEC
```

```
1k 1MEG 100MEG


.PROBE


*******************************************
*** SPECIAL PARAMETERS AND CONSTANTS    ***
*******************************************


.PARAM: + PI=3.14159265358979     ;GUESS WHAT

*---CONVERTER PARAMETERS
.PARAM: +FS=10MEG    ;SWITCHING FREQUENCY +VIN=160 ;INPUT VOLTAGE
+DUTY=0.3   ;DUTY CYCLE +VOUT=75 +LF=805n +LMR=595n;selected for Ls
Lr match ; +CMR=100.8p;selected for Ls Lr match  ; +CFNOM=32P
+LS=722n;selected for Ls Lr match +CS=30N +CP=245.3p; match based on
LMR ;;; 243P was original +QIND=190 +CSDAMP=60N +RDAMP=20
+LR=798n;selected for Ls Lr match ;; +Lact=5.45n ;;reduced slightly
from 6n on 2 jan +RACT=1p    ;was briefly 244m +CparMR=2.9p;selected
for Ls Lr match ; +CparR=0.1p ;; +CparBRD=13.5p;selected for Ls Lr
match ; +RparBRD=3.2;selected for Ls Lr match
*+CtrimD=.01p;



**************************
*LOW ORDER LUMPED NETWORK *
**************************
**---LF LEG
*VDULF   N01 N02 0

*XLF     N02 N03 LCHQC
*+ PARAMS:
*+ L={LF}
*+ QL={QIND}
*+ FQ={FS}
*+ RDC=5M
*+ ICL=0
*+ EPC=.001P
*+ ICC=0
*+ EPR=10MEG

*---INPUT VOLTAGE
*VIN     N03 0   {VIN}
```

```
**---MR LEG
VDUMR  N01 N05 0


XCMR    N05 N06 CQL + PARAMS: + C={CMR} + QC=10K + FQ={FS} +
ICC={vin} + ESL=1P + ICL=0


XLMR    N06 0 LQCR + PARAMS: + L={LMR} + QL={QIND} + FQ={FS} +
EPC={CparMR} + EPR=10MEG + ICL=0 + ICC=0


*XCparMR N06 0 CQL
*+ PARAMS:
*+ C={CparMR}
*+ QC=100
*+ FQ={FS}
*+ ICC=0
*+ ESL=1P
*+ ICL=0


**added a


*---DUMMY SOURCE TO MEASURE THE IMPEDANCE OF
*   THE LOW ORDER LUMPED NETWORK


VDUZMR NT N01 0


************************
*SEMICONDUCTOR SWITCH  *
************************
VDUSMOS N01 N07 0   ;DUMMY SOURCE TO MEASURE
                    ;THE DRAIN SWITCH CURRENT



XSIMOS   GATE N07 0   ARF475FL_D_v5 + PARAMS: + RDSON=0.6 + RG=10m +
CGS=.1P + LG=.1P + LD=1.5N + LS=1N + RCOUT=0.3


**********************
*IDEALIZED GATE DRIVER*
**********************
*---GATE DRIVE PARAMETER
.PARAM: +TR={1/(100*FS)}                ;RISE TIME
+PWIDTH={(DUTY/(FS))-TR-TR}  ;PULSE WIDTH VGATE GATE 0 PULSE(-25 25
0 {TR} {TR} {PWIDTH} {1/FS})
```

```
**********************
*RESONANT LOAD SECTION *
**********************

*---DUMMY TO MEASURE RESONANT LOAD

VDUZL   NT   M01 0

VDUCP M01 M02 0

XCP  M02 0 CQL + PARAMS: + C={CP} + QC=3K + FQ={FS} + ICC={vin} +
ESL=0.1n +ICL=0

VDUCS M01 M03 0

VDUCSY M03  M03Y 0 XCS    M03Y M04 CQL + PARAMS: + C={CS} + QC=10K +
FQ={FS} + ICC={VIN} + ESL=1P + ICL=0

*VDUCSDAMP M03   M03D 0
*XCSDAMP    M03D M03DR CQ1
*+ PARAMS:
*+ C={CSDAMP}
*+ QC=10K
*+ FQ={FS}
*+ ICC={VIN}
*+ ESL=1P
*+ ICL=0

*RDAMP M03DR M04 {RDAMP}

XLS M04 M05 LQCR + PARAMS: + L={LS} + QL={QIND} + FQ={FS} + EPC=.1P
+ EPR=10MEG + ICL=0 + ICc=0


**------RECTIFIER WITH CANTELIVER TRANSFORMER

VDUREC M05 R01 0

VDULR R01 R01X 0 XLREC R01x 0 LCHQC + PARAMS: + L={LR} + QL={QIND} +
FQ={FS} + RDC=5M + ICL=0 + EPC={CparR} + ICC=0 + EPR=10MEG

Cbrd R01x R01y {CparBRD} Rbrd R01y 0 {RparBRD}

VDURECC R01 R02x VDUSEC R02x R02 0   ;DUMMY SOURCE TO MEASURE
```

```
                    ;SECONDARY CURRENT

XD1 R02 R03 CSD10060_v6jan7 XD2 R02 R03 CSD10060_v6jan7
*CtrimD R02 R03 {CtrimD}

VOUT   R03 0 {VOUT}

*.inc "XFMEAS_TOT.CIR"




************************************************
**** OPTIONS  TO AVOID CONVERGENCE PROBLEMS  ***
************************************************
.OPTIONS ABSTOL=10nA +          GMIN=10p +          ITL1=6000 +
ITL2=4000 +          ITL4=5000 +          RELTOL=0.005 +
VNTOL=0.06mV .OPTION STEPGMIN


*******************************************
*** OPTIONS TO KEEP A SMALL OUTPUT FILE ***
*******************************************
.OPTIONS + NOPAGE + NOBIAS + NOECHO + NOMOD + NUMDGT=8 .WIDTH
OUT=132        ;TO PRINT MORE COLUMNS


**************************
*** LIST OF LIBRARIES   ***
**************************
.LIB "THESIS.LIB"
```

C.4   Half Sine Gate Drive Simulation

```
gatedrive_dcdc_redphi2_cleaned.cir


*********************************************************
*** CIRCUIT FILE TO SIMULATE THE               ***
*** THE NEW PHI-2 (POTATO) INVERTER            ***
***                                            ***
*** TRANSIENT SIMULATION                       ***
```

```
*** WRITTEN BY: JUAN RIVAS, M.I.T.                    ***
*** CAMBRIDGE,MA 11/07/2006                           ***
*** Modified for half-sine gate drive test            ***
*** Olivia Leitermann, 12 Feb 2007                    ***
***********************************************************
*AUTOXFR MODEL  BASED ON MEASURMENTS ON THE PCB BOARD


*********************
* SIMULATION CONTROL *
*********************


*---TRANSIENT COMMAND
.param kres =2 .tran 30p 8u 6u 30p UIC


.PROBE


**************************
*** LIST OF LIBRARIES   ***
**************************
.LIB "THESIS.lib"   ;Main parts library, from JMR thesis .LIB
"CLASSE.LIB"  ;RF parts library, from JMR .lib "MOSNL3_ST.LIB"
;part model from AS for RF switch possibility .lib
"arf521_detail_121306.lib" ;newest ARF521 model


***********************************************
**** OPTIONS  TO AVOID CONVERGENCE PROBLEMS   ***
***********************************************
.OPTIONS ABSTOL=10nA +          GMIN=10p +           ITL1=6000 +
ITL2=4000 +          ITL4=5000 +         RELTOL=0.02 +
VNTOL=0.2mV .OPTION STEPGMIN


*********************************************
*** OPTIONS TO KEEP A SMALL OUTPUT FILE ***
*********************************************
.OPTIONS + NOPAGE + NOBIAS + NOECHO + NOMOD + NUMDGT=8 .WIDTH
OUT=132        ;TO PRINT MORE COLUMNS
*********************************************
*** SPECIAL PARAMETERS AND CONSTANTS     ***
*********************************************
*********************************************
.PARAM: + PI=3.14159265358979    ;GUESS WHAT


*---CONVERTER PARAMETERS
```

```
.PARAM: +FS=30MEG    ;SWITCHING FREQUENCY +VIN=160 ;INPUT VOLTAGE


**************************
*LOW ORDER LUMPED NETWORK *
**************************
*---LF LEG
VDULF  NO1 NO2 0 XLF    NO2 NO3 LCHQC + PARAMS: + L=384N  ;LF
INDUCTOR + QL=194 + FQ={FS} + RDC=5M + ICL=0 + EPC=.001P + ICC=0 +
EPR=10MEG


VIN    NO3 0   {VIN}


*---MR LEG
VDUMR NO1 NO5 0 XCMR    NO5 NO6 CQL + PARAMS: + C=16.29PF  ;CMR
CAPACITOR + QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0 XLMR    NO6
0 LQCR + PARAMS: + L=414n + QL=280 + FQ={FS} + EPC=.1P + EPR=10MEG +
ICL=0 + ICC=0
*---DUMMY SOURCE TO MEASURE THE IMPEDANCE OF
*   THE LOW ORDER LUMPED NETWORK
VDUZMR NT NO1 0
**********************
*SEMICONDUCTOR SWITCH  *
**********************
VDUSMOS NO1 NO7 0  ;DUMMY SOURCE TO MEASURE
                   ;THE DRAIN SWITCH CURRENT


*XSIMOS   GATE NO7 0 SOURCE2  ARF521_MOS5
*+ params:
*+ LS2={ls2}
*+ RS2=20M


*xsimos gate n07 0 0  ARF521_MOS8r
xsimos gate n07 0 0  ARF521_MOS8r +params: rg={rgate}
*+LG={Ltest*6}
*+ls={Ltest*5}
*+cgs={ctest*4}


*.param ls2=.1n
*.param ls2=1.1n
*.step param ls2 list .01n  9n
**********************
*      GATE DRIVE        *
**********************
```

```
.PARAM
*+ FS=30MEG      ;SWITCHING FREQUENCY
+ Cftuneaux = 900p; + Lfaux = {1/4/pi**2/FS**2/Cftuneaux} +
Vgatedrive =3; + Qlfaux = 20; + PW = 18n; +Lfgtune=-25.5n; + Rgate =
.4


***********************
*   HALF SINE DRIVE    *
***********************

XQaux auxgate gate 0 SPN1443;;MOSFETNLC;;;fakemos
*+params: kres=.5
*equiv capacitance ~900pF

Vauxgate auxgate 0 PULSE (0 10 0 1n 1n {PW} {1/FS}) Rgatedamp gate 0
1k

Vgatedrive gatepwr 0 {Vgatedrive}


XLfaux gate gatepwr LQCR + PARAMS: + L={Lfaux+Lfgtune} + QL={Qlfaux}
+ FQ={FS} + EPC=.1P + EPR=10MEG + ICL=0 + ICC=0



***********************
*RESONANT LOAD SECTION *
***********************

**equiv resistance 21.39 ohm

*---DUMMY TO MEASURE RESONANT LOAD
VDUZL  NT  M01 0 VDUCP M01 M02 XCP  M02 0 CQL + PARAMS: + C= 28.2P +
QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0

VDUCS M01 M03 XCS  M03 M04 CQL + PARAMS: + C=4N + QC=10K + FQ={FS} +
ICC={VIN} + ESL=1P + ICL=0 XCSDAMP  M03 M03X CQ1 + PARAMS: + C=12N +
QC=10K + FQ={FS} + ICC={VIN} + ESL=1P + ICL=0 RDAMP M03X M04 10 XLS
M04 M05 LQCR + PARAMS: + L=175N + QL=120 + FQ={FS} + EPC=.1P +
EPR=10MEG + ICL=0 + ICc=0 CPAR M05 0 3P
*-----RECTIFIER WITH CANTELIVER TRANSFORMER
VDUREC M05 R01 0 XTF1  R02x 0 R01 R02x 2WTRFCL_QCH + PARAMS: + N2 =
0.83 + RDCP=5M + RDCS=5M + LM=  78.511N + QP=  120 + LL2= 84.78N +
QS=  120 + FQ = {FS} + IC = 0
```

```
VDUSEC R02X R02 0   ;DUMMY SOURCE TO MEASURE
                              ;SECONDARY CURRENT
CSECPAR R02 0 6P XD1 R02 R03X CSD10030 XD2 R02 R03X CSD10030 LEXTOU
R03X R03  2.5N VOUT  R03 0 33


****equivalent resistor
*Rload R01 0 21.39


.inc "XF_MEAS.CIR"
```

C.5   Sinusoidal Resonant Gate Drive

```
gatedrive_dcdc_sin5_cleaned.cir


*****************************************************
*** CIRCUIT FILE TO SIMULATE THE              ***
*** THE NEW PHI-2 (POTATO) INVERTER           ***
***                                           ***
*** TRANSIENT SIMULATION                      ***
*** WRITTEN BY: JUAN RIVAS, M.I.T.            ***
*** CAMBRIDGE,MA 11/07/2006                   ***
***                                           ***
*** Gate drive added by Olivia Leitermann 14 Feb 07  ***
*****************************************************
*AUTOXFR MODEL  BASED ON MEASURMENTS ON THE PCB BOARD


*********************
* SIMULATION CONTROL *
*********************


*---TRANSIENT COMMAND
.tran 30p 8u 6u 30p UIC


.PROBE


************************
*** LIST OF LIBRARIES   ***
************************
.LIB "THESIS.lib" .LIB "CLASSE.LIB"  ;LIBRARY FOR THIS SIMULATION
```

```
.lib "MOSNL3_ST.LIB"    ;part model from tony for fet possibility
.lib "arf521_detail_121306.lib"


*.LIB "ARF521_detail_110406.LIB"
**************************************************
**** OPTIONS  TO AVOID CONVERGENCE PROBLEMS  ***
**************************************************
.OPTIONS ABSTOL=10nA +         GMIN=10p +          ITL1=6000 +
ITL2=4000 +         ITL4=5000 +         RELTOL=0.02 +
VNTOL=0.2mV .OPTION STEPGMIN


*******************************************
*** OPTIONS TO KEEP A SMALL OUTPUT FILE ***
*******************************************
.OPTIONS + NOPAGE + NOBIAS + NOECHO + NOMOD + NUMDGT=8 .WIDTH
OUT=132      ;TO PRINT MORE COLUMNS
*******************************************
*** SPECIAL PARAMETERS AND CONSTANTS    ***
*******************************************
*******************************************
.PARAM: + PI=3.14159265358979    ;GUESS WHAT


*---CONVERTER PARAMETERS
.PARAM: +FS=30MEG    ;SWITCHING FREQUENCY +VIN=160 ;INPUT VOLTAGE


*************************
*LOW ORDER LUMPED NETWORK *
*************************
*---LF LEG
VDULF  N01 N02 0 XLF    N02 N03 LCHQC + PARAMS: + L=384N  ;LF
INDUCTOR + QL=194 + FQ={FS} + RDC=5M + ICL=0 + EPC=.001P + ICC=0 +
EPR=10MEG


VIN     N03 0    {VIN}


*---MR LEG
VDUMR N01 N05 0 XCMR    N05 N06 CQL + PARAMS: + C=16.29PF  ;CMR
CAPACITOR + QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0 XLMR    N06
0 LQCR + PARAMS: + L=414n + QL=280 + FQ={FS} + EPC=.1P + EPR=10MEG +
ICL=0 + ICC=0
*---DUMMY SOURCE TO MEASURE THE IMPEDANCE OF
*   THE LOW ORDER LUMPED NETWORK
VDUZMR NT N01 0
*********************
```

```
*SEMICONDUCTOR SWITCH  *
************************
VDUSMOS N01 N07 0  ;DUMMY SOURCE TO MEASURE
                   ;THE DRAIN SWITCH CURRENT


*XSIMOS   GATE N07 0 SOURCE2  ARF521_MOS5
*+ params:
*+ LS2={ls2}
*+ RS2=20M

xsimos gate n07 0 0  ARF521_MOS8r
*+params:
*+LG={Ltest*6}
*+ls={Ltest*5}
*+cgs={ctest*4}

*.param ls2=.1n
*.param ls2=1.1n
*.step param ls2 list .01n  9n
************************
*  GATE DRIVE  *
************************

.PARAM
*+ FS=30MEG      ;SWITCHING FREQUENCY
+ Vgateave = -1.5;;;2.5 ;drive average voltage  (control duty ratio)
+ Vgateamp = 5  ;;drive amplitude (control average voltage) + duty =
.5;;.17;;.32 + Lgateres=0;;{5.23/2/pi/fs} + Lgateextra=250n;;117n +
QLgateextra = 100 + rswon={10/nswitches} + ctotem = {10p} + Lgatebp
= 37.25n + Qlgatebp = 100 + Cgatebp = 10n; + nswitches = 1;

*+ Voff = -.5        ;drive offset voltage
*+ Rdrive = 3   ;impedance of gate drive from power amp
*+ Vnudge = .6
*+ Lgate =90n ;83.2n ;;{5.23/2/pi/fs}
*+ Lgatebp = 62n
*+ Cgatebp = 10n;


**power supplies
Vgatepwr ngatepwr 0 {Vgateave+Vgateamp} Vgateneg nneggatepwr 0
{Vgateave-Vgateamp}
**switches
```

```
Stoptotem ngatepwr npreL contrgate1 0 Mtotemswitch Sbottomtotem
npreL nneggatepwr  contrgate2 0 Mtotemswitch .Model Mtotemswitch
Vswitch(Ron={rswon} Roff=1g)
** back diodes
Dlow nneggatepwr nprel backdiode .model backdiode D ;;;(IS= N= Rs=
CJO=1p Tt= BV= IBV=) Dhigh npreL ngatepwr backdiode
**control
Vcontrgate1 contrgate1 0 PULSE(0 5 1.2n 1n 1n {duty/FS-1.2n} {1/FS})
Vcontrgate2 contrgate2 0 PULSE(5 0 0 1n 1n {duty/FS+1.2n} {1/FS})

**lf oscillation damping
Rdampgate gate 0 10k


XLgateextra npreL gate LQCR + PARAMS: + L={Lgateres + lgateextra} +
QL={QLgateextra} + FQ={FS} + EPC=.1P + EPR=10MEG + ICL=0 + ICC=0

XLgatebp gate ngatea LQCR + PARAMS: + L={lgatebp} + QL={QLgatebp} +
FQ={FS} + EPC=.1P + EPR=10MEG + ICL=0 + ICC=0 Cgatebp ngatea 0
{Cgatebp}


Ctotempos npreL nneggatepwr {Ctotem} Ctotemneg npreL ngatepwr
{Ctotem}



**********************
*RESONANT LOAD SECTION *
**********************

*---DUMMY TO MEASURE RESONANT LOAD
VDUZL  NT  M01 0 VDUCP M01 M02 XCP  M02 0 CQL + PARAMS: + C= 28.2P +
QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0


VDUCS M01 M03 XCS  M03 M04 CQL + PARAMS: + C=4N + QC=10K + FQ={FS} +
ICC={VIN} + ESL=1P + ICL=0 XCSDAMP  M03 M03X CQ1 + PARAMS: + C=12N +
QC=10K + FQ={FS} + ICC={VIN} + ESL=1P + ICL=0 RDAMP M03X M04 10 XLS
M04 M05 LQCR + PARAMS: + L=175N + QL=120 + FQ={FS} + EPC=.1P +
EPR=10MEG + ICL=0 + ICc=0 CPAR M05 0 3P
*-----RECTIFIER WITH CANTELIVER TRANSFORMER
VDUREC M05 R01 0 XTF1  R02x 0 R01 R02x 2WTRFCL_QCH + PARAMS: + N2 =
0.83 + RDCP=5M + RDCS=5M + LM=  78.511N + QP=  120 + LL2= 84.78N +
QS=  120 + FQ = {FS} + IC = 0

VDUSEC R02X R02 0  ;DUMMY SOURCE TO MEASURE
```

```
                                  ;SECONDARY CURRENT
CSECPAR RO2 0 6P XD1 RO2 RO3X CSD10030 XD2 RO2 RO3X CSD10030 LEXTOU
RO3X RO3  2.5N VOUT  RO3 0 33


.inc "XF_MEAS.CIR"
```

C.6   Grebennikov Second Harmonic Class E

grebenn_e2_test_cleaned.cir

```
********************************************************
*** Circuit file to simulate the Grebennikov Second  ***
*** Harmonic Class E inverter (simplified)           ***
***                                                  ***
*** Effects of varied loaded Q                       ***
***                                                  ***
*** Olivia Leitermann 18 Apr 07                      ***
*** Based on older files from JMR                    ***
********************************************************


*---TRANSIENT COMMAND

.TRAN 30P 4u 0 30P UIC

.PROBE


*************************
*** LIST OF LIBRARIES   ***
*************************
.LIB "THESIS.lib"  ;Library from JMR for RF parts

.INC "OPTIONS.CIR"

*---CONVERTER PARAMETERS
.PARAM: +FS=30meg    ;SWITCHING FREQUENCY +w={2*pi*FS} +Rload=1
+QL=50 +CO={1/QL/Rload/w} +LO={QL*Rload/w} +Cx={0.204/w/Rload}
+C={0.071/w/Rload} +L={3.534*Rload/w} +Vdd=1 +duty=.5 +Rdson =10m

.step param QL list 5 20 50
```

```
Rload nout 0 {Rload}

CO ntank nout {CO}

LO nx ntank {LO}

Cx nd nx {Cx}

Cpar nd 0 {C}

Lpwr nd nvdd {L}

Vdd nvdd 0 {Vdd}

Smod nd 0 nsig 0 simp     ;;Using a simple switched-resistor model
with output capacitance .model simp Vswitch(RON={Rdson}, Roff=10meg)

Vsig nsig 0 PULSE(0 5 0 1n 1n {duty/FS} {1/FS})
```

C.7   Gate Drive Simulation

C.7.1   Main File

```
dcdc_master17.cir

*****************************************************
*** CIRCUIT FILE TO SIMULATE THE                 ***
*** THE NEW PHI-2 (POTATO) INVERTER only / mastersim ***
***                                              ***
*** TRANSIENT SIMULATION                         ***
*** WRITTEN BY: JUAN RIVAS, M.I.T.               ***
*** CAMBRIDGE,MA 11/07/2006                      ***
*** separated by ol 20 mar 07

*****************************************************
*AUTOXFR MODEL  BASED ON MEASURMENTS ON THE PCB BOARD

********************
```

```
* SIMULATION CONTROL *
*********************


*---TRANSIENT COMMAND
.param kres =2 .TRAN 30P 15u 13u 30P UIC


.PROBE


*************************
*** LIST OF LIBRARIES   ***
*************************
.LIB "THESIS.lib" .LIB "CLASSE.LIB"  ;LIBRARY FOR THIS SIMULATION
.lib "MOSNL3_ST_new.LIB"    ;part model from tony for fet
possibility .lib "arf521_detail_121306_new.lib"


*.LIB "ARF521_detail_110406.LIB"


.INC "OPTIONS.CIR"


*---CONVERTER PARAMETERS
.PARAM: +FS=30meg;;;;26meg;;30MEG    ;SWITCHING FREQUENCY +VIN=160
;INPUT VOLTAGE


*.step param Vin 160 200 40


*************************
*LOW ORDER LUMPED NETWORK *
*************************
*---LF LEG
VDULF  NO1 NO2 0 XLF    NO2 NO3 LCHQC + PARAMS: + L=384N  ;LF
INDUCTOR + QL=194 + FQ={FS} + RDC=5M + ICL=0 + EPC=.001P + ICC=0 +
EPR=10MEG


VIN    NO3 0   {VIN}


*---MR LEG
VDUMR NO1 NO5 0 XCMR    NO5 NO6 CQL + PARAMS: + C=16.29PF  ;CMR
CAPACITOR + QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0 XLMR    NO6
0 LQCR + PARAMS: + L=414n + QL=280 + FQ={FS} + EPC=.1P + EPR=10MEG +
ICL=0 + ICC=0
*---DUMMY SOURCE TO MEASURE THE IMPEDANCE OF
*   THE LOW ORDER LUMPED NETWORK
VDUZMR NT NO1 0
```

```
**To switch
VDUSMOS N01 N07 0  ;DUMMY SOURCE TO MEASURE
                   ;THE DRAIN SWITCH CURRENT


************************
*RESONANT LOAD SECTION *
************************


*---DUMMY TO MEASURE RESONANT LOAD
VDUZL  NT  M01 0 VDUCP M01 M02 0 XCP  M02 0 CQL + PARAMS: + C= 28.2P
+ QC=3K + FQ={FS} + ICC={vin} + ESL=1P + ICL=0

VDUCS M01 M03 0 XCS  M03 M04 CQL + PARAMS: + C=4N + QC=10K + FQ={FS}
+ ICC={VIN} + ESL=1P + ICL=0 XCSDAMP  M03 M03X CQ1 + PARAMS: + C=12N
+ QC=10K + FQ={FS} + ICC={VIN} + ESL=1P + ICL=0 RDAMP M03X M04 10
XLS M04 M05 LQCR + PARAMS: + L=175N + QL=120 + FQ={FS} + EPC=.1P +
EPR=10MEG + ICL=0 + ICc=0 CPAR M05 0 3P



******************************************
* Interface to gate drive at node "gate" *
******************************************


***************
* Other files *
***************


.inc "dcdc_rectifier.cir"
*VDUREC M05 R01 0
*Req R01 0 25.54

*.inc "gatesec_hard_sin1.cir"
.inc "gate_running_9jan07.cir"
*.PARAM
*+Vgatemag = 5
*+Vgatebias=-1
*Vgatesig gate 0 SIN({Vgatebias} {Vgatemag} {FS})

.inc "XF_MEAS.CIR"
*.inc "INV_MEAS.CIR"
```

C.7.2 Gate Drive File

gate_running_9jan07.cir

```
**********************************************************
*** CIRCUIT FILE TO SIMULATE THE                   ***
*** THE NEW PHI-2 (POTATO) INVERTER gate drive     ***
***                                                ***
*** TRANSIENT SIMULATION                           ***
*** WRITTEN BY: JUAN RIVAS, M.I.T.                 ***
*** CAMBRIDGE,MA 11/07/2006                        ***
*** separated ol 20 mar 07
**********************************************************



***********************
*SEMICONDUCTOR SWITCH  *
***********************


*XSIMOS    GATE N07 0 SOURCE2   ARF521_MOS5
*+ params:
*+ LS2={ls2}
*+ RS2=20M

xsimos gate n07 0 0  ARF521_MOS8R_IC +params: +VCGS0={Vgatebias}
*+LG={Ltest*6}
*+ls={Ltest*5}
*+cgs={ctest*4}

*Vmainbias n07 0 {Vin}

*.param ls2=.1n
*.param ls2=1.1n
*.step param ls2 list .01n  9n
*.step param Rgbias list 100 300 1k 3k
*.step param qcgmatch list 50 100 500
***********************
*  GATE DRIVE  *
***********************

**resonant parameters
```

```
.PARAM +Cgshuntsw = 8p;;parasitics +Lgpwr =
72.5n;;72.6n;;47.8n;;38.4n;;39.8n;;56n +Cgmatch =3.26n
;;3n;;3.31n;;3.84n;;4n;;3.15n
+Lg2=16.2n;;20.8n;;19.16n;;18.87n;;14.7n;;16.9n
+Cg2=445p;;417p;;406p;;417p +Cgr=209p;;228p;;228p


**incidental parameters
+QLgres=50 ;;120 +QLg=80
+Vgatebias=-4;;-1;;-4.5;;-7;;0;;-3.5;;-6.2;;0;;-3;;-6.2;;-3.5;;-3.75
*+Cqauxeq=125p
+Ctuneshunt=0;;30p +Lgbias = 1000n; +Rgbias = 3k;;100;;1k;
+Lgparval=38.2n;;36.4n;;32.7n;;;38.9n;;23.7n;;38.87n;;34.5n;;30n;;39.6n
+duty=0.5 +Vgate =12;;12;;20;;6;;3.5 ;;2.75;;3.27 +Rdson=1
+Vgatemag=1 +qcgmatch=500


*.step param Cgmatch list 3.1n 3.26n 3.4n
*.step param Lgparval list 38.5n 36.5n 34.5n

*.step param cg2 list 445p 430p
*.step param lg2 list 16.9n 19.16n


**resonant and matching network
XLgres gate ngateres LQS;;;LQCR + PARAMS: +
L={Lgparval};;;*Lgzpar/(Lgparval+Lgzpar)} + QL={QLgres} + FQ={FS}
*+ EPC=.1P
*+ EPR=10MEG
+ IC=0
*+ ICC=0

*XCgres gate ngateres CQL
*+Params:
*+ C={Cgzpar}
*+ QC=500
*+ FQ={FS}
*+ ESL=.1P
*+ ICL=0
*+ ICC=0


XCgmatch ngateres 0 CQS;;CQL + PARAMS: + C={Cgmatch} +
QC=qcgmatch;;;500 + FQ={FS}
**+ ESL=.1P
```

```
**+ ICL=0
+ IC={Vgatebias}


**dc offset
Vgatebias ngatebias 0 {Vgatebias} XLgbias ngatebias1 gate1
LQS;;;LQCR + PARAMS: + L={Lgbias} + QL={QLg} + FQ={FS}
*+ EPC=.1P
*+ EPR=10MEG
+ IC=0
*+ ICC=0
Rgbias ngatebias1 ngatebias {Rgbias}


***series capacitance
XCgr ngateres ngatepar CQS;;CQL + PARAMS: + C={Cgr} + QC=500 +
FQ={FS}
*+ ESL=1p
*+ ICL=0
+ IC={Vgatebias-Vgate}


**shunt tank

XCg2 ngatepar ngated CQS +params: +C={Cg2} +QC=500 +FQ={FS} +IC=0

XLg2 ngatepar ngated LQS +params: +L={Lg2} +QL={QLg} +FQ={FS} +IC=0


***capacitance in shunt with switch
XCgqshunt ngated 0 CQS;;CQL + PARAMS: + C={Cgshuntsw} + QC=500 +
FQ={FS}
**+ ESL=1p
**+ ICL=0
+ IC=0;;;{Vgate}


**switch

XQaux nauxgate ngated 0 MOSNLC_IC_SIMPLIFIED
*+params:
*+IC={Vgate}
*+CJO=150p


***simple switch model

*Saux ngated 0 nauxgate 0 simple
*.model simple Vswitch(RON={Rdson}, Roff=10meg)
```

```
Vauxgate nauxgate 0 PULSE (0 5 0 1n 1n {duty/FS} {1/FS})

**inductance in shunt with switch
XLgpwr ngated nVgate LQS;;;LQCR + PARAMS: + L={Lgpwr} + QL={QLg} +
FQ={FS}
*+ EPC=.1P
*+ EPR=10MEG
+ IC=0
*+ ICC=0


**gate power supply
Vgate nVgate 0 {Vgate}


*.PARAM
*+Vgatemag = .6
*+Vgatebias=-1

*Vgatesig ngateres 0 SIN({Vgatebias} {Vgatemag} {FS})
*Vgatesig ngateres 0 AC 1
```

C.7.3   Rectifier File

```
dcdc_rectifier.cir


********************************************************
*** CIRCUIT FILE TO SIMULATE THE                ***
*** THE NEW PHI-2 (POTATO) Rectifier             ***
***                                             ***
*** TRANSIENT SIMULATION                         ***
*** WRITTEN BY: JUAN RIVAS, M.I.T.               ***
*** CAMBRIDGE,MA 11/07/2006 ]
*** Separated by OL 20 mar 7                     ***
********************************************************

***Connection at M05 (or use Vdurec from M05 to R01 and R01)
***Equivalent resistance measured at 25.54 ohm, mar 07

*-----RECTIFIER WITH CANTELIVER TRANSFORMER
VDUREC M05 R01 0 XTF1  R02x 0 R01 R02x 2WTRFCL_QCH + PARAMS: + N2 =
```

```
0.83 + RDCP=5M + RDCS=5M + LM=  78.511N + QP=  120 + LL2= 84.78N +
QS=  120 + FQ = {FS} + IC = 0


VDUSEC RO2X RO2 0  ;DUMMY SOURCE TO MEASURE
                        ;SECONDARY CURRENT
CSECPAR RO2 0 6P XD1 RO2 RO3X CSD10030 XD2 RO2 RO3X CSD10030 LEXTOU
RO3X RO3  2.5N VOUT  RO3 0 33
**Req RO1 0 25.54
```

C.8   Subfiles Called by Other Scripts

C.8.1   Dc-dc Measurement Code

```
XF_MEAS.cir


***************************
***MEASUREMENT CIRCUITS ***
***************************
*JUAN RIVAS 030106


.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                                ;COMPONENT OF THE MEASURMENT
                                ;CIRCUITS TWO DECADES BEFORE THE
                                ;SWITCHING FREQUENCY
*-----INPUT POWER MEASUREMENT
EPI PINO1 0  VALUE={V(nO3)*(-I(VIN))} LPI PINO1 PIN {LORC(FS)} CPI
PIN  0 {LORC(FS)} RPI PIN  0  1
*-----OUTPUT POWER MEASUREMENT resistive load
EPO POO1 0    VALUE={v(RO3)*I(VOUT)} LPO POO1 POUT {LORC(FS)} CPO
POUT 0    {LORC(FS)} RPO POUT 0   1  ;OUTPUT POWER
*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}
****************************
*HIGH Q BAND PASS FILTER   ***
****************************
*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM + QBP=100 .FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)} .FUNC
LBPQ(FS,QBP) {QBP/(2*PI*FS)}
*-----FUNAMDENTAL OF THE RECT. VOLTAGE
```

```
EBPRV   BPRV1   0       VALUE={V(RO1)} LBPRV   BPRV1   BPRV2
{LBPQ(FS,QBP)} CBPRV   BPRV2   BPRV    {CBPQ(FS,QBP)} RBPRV   BPRV    0
1
*-----FUNDAMENTAL OF THE RECT. CURRENT
EBPRI   BPRI1   0       VALUE={I(VDUREC)} LBPRI   BPRI1   BPRI2
{LBPQ(FS,QBP)} CBPRI   BPRI2   BPRI    {CBPQ(FS,QBP)} RBPRI   BPRI    0
1


*-----fundamental of the inverter drain voltage
EBPDV   BPDV1   0       VALUE={V(NT)} LBPDV   BPDV1   BPDV2
{LBPQ(FS,QBP)} CBPDV   BPDV2   BPDV    {CBPQ(FS,QBP)} RBPDV   BPDV    0
1


*-----fundamental of the gate voltage
EBPGV   BPGV1   0       VALUE={V(gate)} LBPGV   BPGV1   BPGV2
{LBPQ(FS,QBP)} CBPGV   BPGV2   BPGV    {CBPQ(FS,QBP)} RBPGV   BPGV    0
1


*-----fundamental of the gate current
*HBPGI  BPGI1   0       VALUE={i(vgatesig)}
*LBPGI  BPGI1   BPGI2   {LBPQ(FS,QBP)}
*CBPGI  BPGI2   BPGI    {CBPQ(FS,QBP)}
*RBPGI  BPGI    0       1



***************************************
*POWER LOST IN THE INDUCTORS *
***************************************

**---POWER LOST IN LCHOKE
EPLLF PLLF1   0       VALUE={V(NO2,NO3)*(I(VDULF))} LPLLF PLLF1   PLLF
{LORC(FS)} CPLLF PLLF  0       {LORC(FS)} RPLLF PLLF  0       1

*---POWER LOST LMR
EPLLMR PLLMR1 0       VALUE={V(NO5,NO6)*(I(VDUMR))} LPLLMR PLLMR1
PLLMR  {LORC(FS)} CPLLMR PLLMR  0       {LORC(FS)} RPLLMR PLLMR  0
1

*---POWER LOST IN LS
EPLLS  PLLS1   0       VALUE={V(MO4,MO5)*(I(VDUCS))} LPLLS  PLLS1
PLLS    {LORC(FS)} CPLLS  PLLS  0       {LORC(FS)} RPLLS  PLLS   0
1

**---POWER LOST IN LR
```

```
*EPLLR   PLLR1   0        VALUE={V(R01,0)*(I(VDULR))}
*LPLLR   PLLR1   PLLR     {LORC(FS)}
*CPLLR   PLLR    0        {LORC(FS)}
*RPLLR   PLLR    0        1


*---POWER LOST IN THE WHOLE SWITCH
EPLSW  PLSW1 0            VALUE={V(N01)*I(VDUSMOS)} LPLSW  PLSW1 PLSW
{LORC(FS)} CPLSW  PLSW  0            {LORC(FS)} RPLSW  PLSW  0
1


*---POWER LOST IN THE DIODES
EPLD    PLD1  0           VALUE={V(R02,R03)*I(VOUT)} LPLD    PLD1   PLD
{LORC(FS)} CPLD   PLD   0            {LORC(FS)} RPLD    PLD    0
1
*****************************************
*DERIVATIVE CALCULATION               ***
*****************************************


*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
*.PARAM: LDER=.01U
*.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
*GDER   0    D1 VALUE={V(NT)}
*LDER   D1   0   {LDER}
*RDER   D1   0   {RDER(LDER,FS)}
*EDER   DER 0   VALUE={V(D1)/LDER}
*RDER2 DER 0   1K
}


********************************************************************

XFMEAS_TOT.cir


***********************************************************
*** FILE FOR OBTAINING PERFORMANCE OF THE CONVERTER   ***
*** AND OBTAIN POWER LOSS IN SEMICONDUCTORS AND       ***
*** INDUCTORS                                         ***
***                                                   ***
*** BY: JUAN RIVAS, OLIVIA LEITERMANN, YEHUI HAN      ***
***     GRACE CHEUNG, JOHN RANSON, DAVID PERREAULT    ***
*** (c) MIT CAMBRIDGE, MA  2007                       ***
***********************************************************
*************************
***MEASUREMENT CIRCUITS ***
*************************
```

```
.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY
*-----INPUT POWER MEASUREMENT
EPI PIN01 0  VALUE={V(n03)*(-I(VIN))} LPI PIN01 PIN {LORC(FS)} CPI
PIN   0  {LORC(FS)} RPI PIN   0   1
*-----OUTPUT POWER MEASUREMENT resistive load
EPO POO1 0    VALUE={v(RO3)*I(VOUT)} LPO POO1 POUT {LORC(FS)} CPO
POUT 0    {LORC(FS)} RPO POUT 0   1  ;OUTPUT POWER
*-----EFFICIENCY
EEFF    EFF   0     VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))} REFF    EFF
0     1K

****************************
*HIGH Q BAND PASS FILTER   ***
****************************
*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM + QBP=100 .FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)} .FUNC
LBPQ(FS,QBP) {QBP/(2*PI*FS)}
*-----FUNAMDENTAL OF THE RECT. VOLTAGE
EBPRV BPRV1 0      VALUE={V(RO1)} LBPRV  BPRV1  BPRV2
{LBPQ(FS,QBP)} CBPRV  BPRV2 BPRV   {CBPQ(FS,QBP)} RBPRV  BPRV   0
1
*-----FUNDAMENTAL OF THE RECT. CURRENT
EBPRI BPRI1 0      VALUE={I(VDUREC)} LBPRI  BPRI1  BPRI2
{LBPQ(FS,QBP)} CBPRI  BPRI2 BPRI   {CBPQ(FS,QBP)} RBPRI  BPRI   0
1

*************************************
*POWER LOST IN THE INDUCTORS *
*************************************
**---POWER LOST IN LCHOKE
EPLLF PLLF1  0      VALUE={V(N02,N03)*(I(VDULF))} LPLLF PLLF1   PLLF
{LORC(FS)} CPLLF PLLF  0      {LORC(FS)} RPLLF PLLF  0      1
*---POWER LOST LMR
EPLLMR PLLMR1 0      VALUE={V(N06)*(I(VDUMR))} LPLLMR PLLMR1 PLLMR
{LORC(FS)} CPLLMR PLLMR  0      {LORC(FS)} RPLLMR PLLMR  0      1
*---POWER LOST IN LS
EPLLS  PLLS1  0      VALUE={V(M04,M05)*(I(VDUCS))} LPLLS  PLLS1
PLLS   {LORC(FS)} CPLLS  PLLS  0      {LORC(FS)} RPLLS  PLLS   0
1
**---POWER LOST IN LR
EPLLR  PLLR1  0      VALUE={V(RO1X,0)*(I(VDULR))} LPLLR  PLLR1
PLLR   {LORC(FS)} CPLLR  PLLR  0      {LORC(FS)} RPLLR  PLLR   0
1
```

```
************************************
*POWER LOST IN THE SEMICONDUCTORS *
************************************
*---POWER LOST IN THE WHOLE SWITCH
EPLSW   PLSW1 0          VALUE={V(N01)*I(VDUSMOS)} LPLSW  PLSW1 PLSW
{LORC(FS)} CPLSW  PLSW  0          {LORC(FS)} RPLSW  PLSW  0
1
*---POWER LOST IN THE DIODES
EPLD    PLD1  0          VALUE={V(R02,R03)*I(VOUT)} LPLD    PLD1  PLD
{LORC(FS)} CPLD    PLD   0          {LORC(FS)} RPLD    PLD   0
1
*****************************************
*POWER LOST IN CAPACITORS AND RESISTORS *
*****************************************
**---POWER LOST IN CMR
EPLCMR  PLCMR1  0        VALUE={V(N05,N06)*(I(VDUMR))} LPLCMR
PLCMR1  PLCMR   {LORC(FS)} CPLCMR  PLCMR   0        {LORC(FS)}
RPLCMR  PLCMR   0       1
**---POWER LOST IN CP
EPLCP  PLCP1   0        VALUE={V(M02)*(I(VDUCP))} LPLCP  PLCP1  PLCP
{LORC(FS)} CPLCP  PLCP   0        {LORC(FS)} RPLCP  PLCP   0       1

**---POWER LOST IN CS
EPLCS  PLCS1 0          VALUE={V(M03Y,M04)*(I(VDUCSY))} LPLCS  PLCS1
PLCS    {LORC(FS)} CPLCS  PLCS   0        {LORC(FS)} RPLCS  PLCS   0
1
```

C.8.2   Inverter Measurement Code

```
INV_MEAS.cir


*************************
***MEASUREMENT CIRCUITS ***
*************************
*JUAN RIVAS 030106


.FUNC LORC(FS) {100/(2*PI*FS)} ;FUNCTION THAT PLACES THE FILTER
                               ;COMPONENT OF THE MEASURMENT
                               ;CIRCUITS TWO DECADES BEFORE THE
                               ;SWITCHING FREQUENCY
```

```
*-----INPUT POWER MEASUREMENT
EPI PINO1 0  VALUE={V(n03)*(-I(VIN))} LPI PINO1 PIN {LORC(FS)} CPI
PIN   0 {LORC(FS)} RPI PIN    0  1
*-----OUTPUT POWER MEASUREMENT resistive load
EPO POO1 0    VALUE={v(RO1)*I(Vdurec)} LPO POO1 POUT {LORC(FS)} CPO
POUT 0    {LORC(FS)} RPO POUT 0    1  ;OUTPUT POWER
*-----EFFICIENCY
EEFF   EFF   0    VALUE={IF(TIME<100N,0,V(POUT)/v(PIN))}
******************************
*HIGH Q BAND PASS FILTER   ***
******************************
*-----PARAMETERS FOR THE BANDPASS FILTER
.PARAM + QBP=100 .FUNC  CBPQ(FS,QBP) {1/(2*PI*FS*QBP)} .FUNC
LBPQ(FS,QBP) {QBP/(2*PI*FS)}
*-----FUNAMDENTAL OF THE RECT. VOLTAGE
EBPRV  BPRV1  0      VALUE={V(RO1)} LBPRV  BPRV1  BPRV2
{LBPQ(FS,QBP)} CBPRV  BPRV2  BPRV  {CBPQ(FS,QBP)} RBPRV  BPRV   0
1
*-----FUNDAMENTAL OF THE RECT. CURRENT
EBPRI  BPRI1  0      VALUE={I(VDUREC)} LBPRI  BPRI1  BPRI2
{LBPQ(FS,QBP)} CBPRI  BPRI2  BPRI  {CBPQ(FS,QBP)} RBPRI  BPRI   0
1

*-----fundamental of the inverter drain voltage
EBPDV  BPDV1  0      VALUE={V(NT)} LBPDV  BPDV1  BPDV2
{LBPQ(FS,QBP)} CBPDV  BPDV2  BPDV  {CBPQ(FS,QBP)} RBPDV  BPDV   0
1

*-----fundamental of the gate voltage
EBPGV  BPGV1  0      VALUE={V(gate)} LBPGV  BPGV1  BPGV2
{LBPQ(FS,QBP)} CBPGV  BPGV2  BPGV  {CBPQ(FS,QBP)} RBPGV  BPGV   0
1

**-----fundamental of the gate current
*HBPGI  BPGI1  0      VALUE={i(vgatesig)}
*LBPGI  BPGI1  BPGI2  {LBPQ(FS,QBP)}
*CBPGI  BPGI2  BPGI   {CBPQ(FS,QBP)}
*RBPGI  BPGI   0      1


***************************************
*POWER LOST IN THE INDUCTORS *
***************************************
```

```
**---POWER LOST IN LCHOKE
EPLLF PLLF1  0       VALUE={V(NO2,NO3)*(I(VDULF))} LPLLF  PLLF1   PLLF
{LORC(FS)} CPLLF  PLLF  0       {LORC(FS)} RPLLF  PLLF  0        1

*---POWER LOST LMR
EPLLMR PLLMR1 0      VALUE={V(NO5,NO6)*(I(VDUMR))} LPLLMR PLLMR1
PLLMR  {LORC(FS)} CPLLMR PLLMR  0      {LORC(FS)} RPLLMR PLLMR  0
1

*---POWER LOST IN LS
EPLLS  PLLS1   0      VALUE={V(MO4,MO5)*(I(VDUCS))} LPLLS   PLLS1
PLLS    {LORC(FS)} CPLLS  PLLS   0       {LORC(FS)} RPLLS  PLLS   0
1

**---POWER LOST IN LR
*EPLLR  PLLR1   0       VALUE={V(RO1,0)*(I(VDULR))}
*LPLLR  PLLR1  PLLR    {LORC(FS)}
*CPLLR  PLLR   0       {LORC(FS)}
*RPLLR  PLLR   0       1

*---POWER LOST IN THE WHOLE SWITCH
EPLSW  PLSW1 0           VALUE={V(NO1)*I(VDUSMOS)} LPLSW  PLSW1 PLSW
{LORC(FS)} CPLSW  PLSW  0           {LORC(FS)} RPLSW  PLSW  0
1

*---POWER LOST IN THE DIODES
*EPLD    PLD1   0          VALUE={V(RO2,RO3)*I(VOUT)}
*LPLD    PLD1  PLD        {LORC(FS)}
*CPLD    PLD   0          {LORC(FS)}
*RPLD    PLD   0          1
******************************************
*DERIVATIVE CALCULATION              ***
******************************************

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
*.PARAM: LDER=.01U
*.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
*GDER  0    D1 VALUE={V(NT)}
*LDER  D1  0  {LDER}
*RDER  D1  0  {RDER(LDER,FS)}
*EDER  DER 0  VALUE={V(D1)/LDER}
*RDER2 DER 0  1K
```

C.8.3 Options File

options.cir

```
********************************************************
*** CIRCUIT FILE TO BE INCLUDED FOR OPTIONS FIXING   ***
***                                                  ***
*** CIRCUIT FILE SUPPLEMENT                          ***
*** WRITTEN BY: OLIVIA LEITERMANN, M.I.T.            ***
*** BASED ON SIMULATIONS OF J.M.RIVAS, MIT           ***
*** CAMBRIDGE,MA, 9 MAR 07                           ***
********************************************************


*************************************************
**** OPTIONS   TO AVOID CONVERGENCE PROBLEMS   ***
*************************************************
.OPTIONS ABSTOL=10nA +          GMIN=10p +          ITL1=6000 +
ITL2=4000 +          ITL4=5000 +          RELTOL=0.02 +
VNTOL=0.2mV .OPTION STEPGMIN


*******************************************
*** OPTIONS TO KEEP A SMALL OUTPUT FILE ***
*******************************************
.OPTIONS + NOPAGE + NOBIAS + NOECHO + NOMOD + NUMDGT=8 .WIDTH
OUT=132        ;TO PRINT MORE COLUMNS
*******************************************
*** SPECIAL PARAMETERS AND CONSTANTS   ***
*******************************************
*******************************************
.PARAM: + PI=3.14159265358979   ;GUESS WHAT
```

C.9 Libraries

C.9.1 Library for ARF521

ARF521_detail_121306_new.lib

```
*includes only models used above *

*$
***********************************************************
*MODEL: ARF521_MOS8R_nlcgs                                *
* APPLICATION:                                            *
* MODEL OF THE APT DEVICE USING A FULL SEMICONDUCTOR      *
* MODEL AND MODELING THE THREE NON-LINEAR CAPACITNCES     *
* VERSION: MOS2                                           *
* 11/09/2006 JUAN RIVAS, MIT                              *
* KELVIN SOURCE                                           *
***********************************************************
* LIMITATIONS:                                            *
*    + RESISTANCE IN SERIES WITH COUT IS ADDED        *
***********************************************************
*NODES:                                                   *
* GATE:    GATE OF THE MOSFET                             *
* DRAIN:   DRAIN OF THE MOSFET                            *
* SOURCE: SOURCE OF THE MOSFET                            *
***********************************************************
***********************************************************
* PARAMETERS:                                             *
* LD: DRAIN LEAD INDUCTANCE                               *
* RD: DREAL LEAD RESISTANCE                               *
* LG: GATE LEAD INDUCTANCE                                *
* RG: GATE LEAD RESISTANCE                                *
* LS: SOURCE LEAD INDUCTANCE                              *
* RS: SOURCE LEAD RESISTANCE                              *
* RDMOS: DRAIN RESISTANCE                                 *
* CGS: GATE TO SOURCE CAPACITANCE                         *
*----NON-LINEAR PARAMETER OF CDS                          *
* CDSOA: CDS @ VDS=0                                      *
* VJDSA: CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* MDSA:  CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* VBREAKDS: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDS     *
* CDSOB: CDS @ VDS=0 WHEN VBREAKDS<VDS<VLIMDS            *
* VJDSB: CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* MDSB:  CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* VLIMDS: CDS REMAINS CONSTANT FRO VDS>=VLIMDS          *
*----NON-LINEAR PARAMETER OF CGD                          *
* CGDOA: CDG @ VDG=0                                      *
* VJGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD *
* MGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD  *
* VBREAKGD: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDG     *
```

```
* CGDOB: CDS @ VGD=0 WHEN VBREAKGD<VDG<VLIMGD          *
* VJGDB: CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD *
* MGDB:  CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD *
* VLIMGD:CDG REMAINS CONSTANT FOR VGD>=VLIMGD          *
*---DC PARAMETERS OF THE LEVEL 1 MOSFET               *
* KP: TRANSCONDUCTANCE COEFFICIENT                    *
* LAMBDA: CHANNEL-LENGTH MODULATION                   *
* VTO: ZERO-BIAS THRESHOLD VOLTAGE                    *
*---BACK-DIODE PARAMETERS                             *
* ISD: DIODE-SATURATION CURRENT                       *
* ND: DIODE EMISSION COEFFICIENT                      *
* RSD: DIODE OHOMIC RESISTANCE                        *
* BVD: DIODE BREAKDOWN VOLTAGE                        *
******************************************************


.SUBCKT ARF521_MOS8r_nlcgs  GATE DRAIN SOURCE SOURCE2 + PARAMS: +
LD=1.5n + RD=20m + LG=1.3n + RG=0.123    ;FROM APT SPICE MODEL (NEED
CONFIRMATION) + LS=1.1n + RS=20m + LS2=1.1n + RS2=20M
*+ RDMOS=0.213 ;FROM APT SPICE MODEL (NEED CONFIRMATION)
+ RDMOS=0.3
*replaced with nonlinear fit+ CGS=752PF   ;MEASURED BY JOHN RANSON
*----NONLINEAR PARAMETERS OF CGS: piecewise linear fit
+CGS0=686p +CGSm1=4.38p +CGSb2=768p +CGSm2=-110f +CGShv=750p
+Vbreakgs1=18.26 +Vbreakgs2=163.6
*----NON-LINEAR PARAMETER OF CDS
+ CDSOA=1945P + VJDSA=0.6606 + MDSA=0.5640 + VBREAKDS=15 +
CDSOB=3960P + VJDSB=0.2064 + MDSB=0.6923 + CDSOFFB=23P + VLIMDS=500
*----RESISTNACE IN SERIES WITH CDS
+ RCDS=0.3  ;CHECK!!!
*----NON-LINEAR PARAMETER OF CGD
+ CGDOA=546p + VJGDA=6.1666 + MGDA=1.6619 + VBREAKGD=15 + CGDOB=494P
+ VJGDB=0.0232 + MGDB=0.5237 + VLIMGD=500


*----LEVEL 1 MOSFET PARAMETERS
+ KP=0.7774 + LAMBDA=0.0105 + VTO=3.2
*----BACK DIODE PARAMETERS
+ ISD=41.5N + ND=1.5 + RSD=10M + BVD=500 + RDIODE=40M


**************************
***SUBCIRCUIT DESCRIPTION ***
**************************


*--DRAIN TERMINAL
```

```
LD DRAIN D1 {LD} ic=0 RD D1    D2 {RD}


*--GATE TERMINAL
LG  GATE  G1    {LG} ic=0 RG  G1    GMOS  {RG}
*CGS GMOS  SMOS  {CGS} ;LINEAR GATE TO SOURCE CAPACITANCE


*--SOURCE TERMINAL
LS SOURCE S1   {LS} ic=0 RS S1     SMOS {RS}



*---SOURCE TERMINAL 2
LS2 SOURCE2 S2 {LS2} ic=0 RS2 S2        SMOS {RS2}


*--NMOSFET MODEL
RDMOS D2  DMOS {RDMOS} M1    DMOS GMOS SMOS SMOS MOSFET L=1U W=1U
*.MODEL MOSFET NMOS (LEVEL=1 KP=0.7774 LAMBDA=0.0105 VTO=3.2)
.MODEL MOSFET NMOS (LEVEL=1 KP={KP} LAMBDA={LAMBDA} VTO={VTO})
*--BACK DIODE
DSD SMOS D2Z  DSUB RSD D2Z D2 {RDIODE}
*.MODEL DSUB D (IS=41.5N N=1.5 RS=60M BV=500)
.MODEL DSUB D (IS={ISD} N={ND} RS={RSD} BV={BVD})



*--NON LINEAR CDS
GDS D2 D2X    VALUE={ + IF(v(D2,SMOS)<=0,V(DER1)*(1/LDER)*CDSOA, +
IF(v(D2,SMOS)<=VBREAKDS,V(DER1)*(1/LDER)*CDSOA/(1+v(D2,SMOS)/VJDSA)**MDSA,
+ IF(v(D2,SMOS)<=VLIMDS,
+(V(DER1)*(1/LDER)*(CDSOB/((1+v(D2,SMOS)/VJDSB)**MDSB)+CDSOFFB)), +
V(DER1)*(1/LDER)*CDSOB/(1+VLIMDS/VJDSB)**MDSB + ) + ) + ) + }


*RESISTANCE IN SERIES WITH CDS
RCDS D2X SMOS {RCDS}


*--NONLINEAR CGS
GGS GMOS SMOS VALUE={ + IF(v(D2, SMOS)<=0, v(DER3)*(1/LDER)*CGSO, +
IF(v(D2, SMOS)<=Vbreakgs1, v(DER3)*(1/LDER)*(CGSO+v(D2,SMOS)*CGSm1),
+ IF(v(D2, SMOS)<=Vbreakgs2,
v(DER3)*(1/LDER)*(CGSb2+v(D2,SMOS)*CGSm2), + V(DER3)*(1/LDER)*CGShv)
+ ) + ) + }


**--NON LINEAR CRSS
GGD  DMOS GMOS VALUE={ + IF(V(DMOS,GMOS)<=0,V(DER2)*(1/LDER)*CGDOA,
+
IF(V(DMOS,GMOS)<=VBREAKGD,V(DER2)*(1/LDER)*CGDOA/(1+V(DMOS,GMOS)/VJGDA)**MGDA,
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```
+ IF(V(DMOS,GMOS)<=VLIMGD,
V(DER2)*(1/LDER)*CGDOB/(1+V(DMOS,GMOS)/VJGDB)**MGDB, +
V(DER2)*(1/LDER)*CGDOB/(1+VLIMGD/VJGDB)**MGDB + ) + ) + ) + }


****SUBCIRCUITS TO EVALUATE DERIVATIVE***
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.14159265358979

*--FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}

*--GETS THE DERIVATIVE OF V(DS) (INTERNAL NODES)
GDER1 0    DER1 VALUE={(v(D2)-V(D2X))} LDER1 DER1 0    {LDER} RDER1
DER1 0    {RDER(LDER,FS)}

*--GETS THE DERIVATIVE OF V(DG) (INTERNAL NODES)
GDER2 0    DER2  VALUE={(v(DMOS)-V(GMOS))} LDER2 DER2 0    {LDER}
RDER2 DER2 0    {RDER(LDER,FS)}

*--GETS THE DERIVATIVE OF V(GS) (INTERNAL NODES)
GDER3 0    DER3  VALUE={(v(GMOS)-V(SMOS))} LDER3 DER3 0    {LDER}
RDER3 DER3 0    {RDER(LDER,FS)}


*---INTERNAL NODE FOR PLOTTING INSTANTANEOUS CRSS
*---ADDED 11072006

*ECRSSINSTX NCRSSINSTX 0 VALUE={I(GGD)/V(DER2)}
*RCRSSINSTX NCRSSINSTX 0 1

*ECRSSINST NCRSSINST 0 VALUE={V(NCRSSINSTX)*LDER}
*RCRSSINST NCRSSINST 0 1
*ECDSINSTX NCDSINSTX 0 VALUE={I(GDS)/V(DER1)}
*RCDSINSTS NCDSINSTX 0 1

*ECDSINST NCDSINST 0 VALUE={V(NCDSINSTX)*LDER}
*RCDSINST NCDSINST 0 1

.ENDS ARF521_MOS8R_nlcgs

*$
********************************************************
*MODEL: ARF521_MOS8R_IC                              *
```

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* APPLICATION:                                          *
* MODEL OF THE APT DEVICE USING A FULL SEMICONDUCTOR    *
* MODEL AND MODELING THE THREE NON-LINEAR CAPACITNCES   *
* VERSION: MOS2                                         *
* 11/09/2006 JUAN RIVAS, MIT       mod OL 10apr07       *
* KELVIN SOURCE                                         *
********************************************************
* LIMITATIONS:                                          *
*   + RESISTANCE IN SERIES WITH COUT IS ADDED     *
********************************************************
*NODES:                                                 *
* GATE:   GATE OF THE MOSFET                            *
* DRAIN:  DRAIN OF THE MOSFET                           *
* SOURCE: SOURCE OF THE MOSFET                          *
********************************************************
********************************************************
* PARAMETERS:                                     `     *
* LD: DRAIN LEAD INDUCTANCE                             *
* RD: DREAL LEAD RESISTANCE                             *
* LG: GATE LEAD INDUCTANCE                              *
* RG: GATE LEAD RESISTANCE                              *
* LS: SOURCE LEAD INDUCTANCE                            *
* RS: SOURCE LEAD RESISTANCE                            *
* RDMOS: DRAIN RESISTANCE                               *
* CGS: GATE TO SOURCE CAPACITANCE                       *
* VCGSO: INITIAL CONDITION ON CGS
*----NON-LINEAR PARAMETER OF CDS                        *
* CDSOA: CDS @ VDS=0                                    *
* VJDSA: CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* MDSA:  CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* VBREAKDS: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDS    *
* CDSOB: CDS @ VDS=0 WHEN VBREAKDS<VDS<VLIMDS           *
* VJDSB: CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* MDSB:  CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* VLIMDS: CDS REMAINS CONSTANT FRO VDS>=VLIMDS          *
*----NON-LINEAR PARAMETER OF CGD                        *
* CGDOA: CDG @ VDG=0                                    *
* VJGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD *
* MGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD  *
* VBREAKGD: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDG    *
* CGDOB: CDS @ VGD=0 WHEN VBREAKGD<VDG<VLIMGD           *
* VJGDB: CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD  *
* MGDB:  CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD  *
* VLIMGD:CDG REMAINS CONSTANT FOR VGD>=VLIMGD           *
```

```
*---DC PARAMETERS OF THE LEVEL 1 MOSFET              *
* KP: TRANSCONDUCTANCE COEFFICIENT                   *
* LAMBDA: CHANNEL-LENGTH MODULATION                  *
* VTO: ZERO-BIAS THRESHOLD VOLTAGE                   *
*---BACK-DIODE PARAMETERS                            *
* ISD: DIODE-SATURATION CURRENT                      *
* ND: DIODE EMISSION COEFFICIENT                     *
* RSD: DIODE OHOMIC RESISTANCE                       *
* BVD: DIODE BREAKDOWN VOLTAGE                        *
***********************************************************


.SUBCKT ARF521_MOS8r_IC  GATE DRAIN SOURCE SOURCE2 + PARAMS: +
LD=1.5n + RD=20m + LG=1.3n + RG=0.123     ;FROM APT SPICE MODEL (NEED
CONFIRMATION) + LS=1.1n + RS=20m + LS2=1.1n + RS2=20M
*+ RDMOS=0.213 ;FROM APT SPICE MODEL (NEED CONFIRMATION)
+ RDMOS=0.3 + CGS=752PF    ;MEASURED BY JOHN RANSON + VCGSO=0
;INITIAL CONDITION ON CGS
*----NON-LINEAR PARAMETER OF CDS
+ CDSOA=1945P + VJDSA=0.6606 + MDSA=0.5640 + VBREAKDS=15 +
CDSOB=3960P + VJDSB=0.2064 + MDSB=0.6923 + CDSOFFB=23P + VLIMDS=500
*----RESISTNACE IN SERIES WITH CDS
+ RCDS=0.3   ;CHECK!!!
*----NON-LINEAR PARAMETER OF CGD
+ CGDOA=546p + VJGDA=6.1666 + MGDA=1.6619 + VBREAKGD=15 + CGDOB=494P
+ VJGDB=0.0232 + MGDB=0.5237 + VLIMGD=500


*----LEVEL 1 MOSFET PARAMETERS
+ KP=0.7774 + LAMBDA=0.0105 + VTO=3.2
*----BACK DIODE PARAMETERS
+ ISD=41.5N + ND=1.5 + RSD=10M + BVD=500 + RDIODE=40M


**************************
***SUBCIRCUIT DESCRIPTION ***
**************************

*--DRAIN TERMINAL
LD DRAIN D1 {LD} ic=0 RD D1     D2 {RD}

*--GATE TERMINAL
LG  GATE  G1    {LG} ic=0 RG  G1    GMOS  {RG} CGS GMOS   SMOS   {CGS}
IC={VCGSO} ;LINEAR GATE TO SOURCE CAPACITANCE

*--SOURCE TERMINAL
```

```
LS SOURCE S1    {LS} ic=0 RS S1      SMOS {RS}



*---SOURCE TERMINAL 2
LS2 SOURCE2 S2 {LS2} ic=0 RS2 S2      SMOS {RS2}

*--NMOSFET MODEL
RDMOS D2  DMOS {RDMOS} M1    DMOS GMOS SMOS SMOS MOSFET L=1U W=1U
*.MODEL MOSFET NMOS (LEVEL=1 KP=0.7774 LAMBDA=0.0105 VTO=3.2)
.MODEL MOSFET NMOS (LEVEL=1 KP={KP} LAMBDA={LAMBDA} VTO={VTO})
*--BACK DIODE
DSD SMOS D2Z  DSUB RSD D2Z D2 {RDIODE}
*.MODEL DSUB D (IS=41.5N N=1.5 RS=60M BV=500)
.MODEL DSUB D (IS={ISD} N={ND} RS={RSD} BV={BVD})



*--NON LINEAR CDS
GDS D2 D2X     VALUE={ + IF(v(D2,SMOS)<=0,V(DER1)*(1/LDER)*CDSOA, +
IF(v(D2,SMOS)<=VBREAKDS,V(DER1)*(1/LDER)*CDSOA/(1+v(D2,SMOS)/VJDSA)**MDSA,
+ IF(v(D2,SMOS)<=VLIMDS,
+(V(DER1)*(1/LDER)*(CDSOB/((1+v(D2,SMOS)/VJDSB)**MDSB)+CDSOFFB)), +
V(DER1)*(1/LDER)*CDSOB/(1+VLIMDS/VJDSB)**MDSB + ) + ) + ) + }




*RESISTANCE IN SERIES WITH CDS
RCDS D2X SMOS {RCDS}

**--NON LINEAR CRSS
GGD  DMOS GMOS VALUE={ + IF(V(DMOS,GMOS)<=0,V(DER2)*(1/LDER)*CGDOA,
+ IF(V(DMOS,GMOS)<=VBREAKGD,
+V(DER2)*(1/LDER)*CGDOA/(1+V(DMOS,GMOS)/VJGDA)**MGDA, +
IF(V(DMOS,GMOS)<=VLIMGD,
V(DER2)*(1/LDER)*CGDOB/(1+V(DMOS,GMOS)/VJGDB)**MGDB, +
V(DER2)*(1/LDER)*CGDOB/(1+VLIMGD/VJGDB)**MGDB + ) + ) + ) + }


****SUBCIRCUITS TO EVALUATE DERIVATIVE***
.PARAM: + LDER=.01U   ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.14159265358979

*--FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}
```

```
*--GETS THE DERIVATIVE OF V(DS) (INTERNAL NODES)
GDER1 0    DER1 VALUE={(v(D2)-V(D2X))} LDER1 DER1 0    {LDER} RDER1
DER1 0    {RDER(LDER,FS)}

*--GETS THE DERIVATIVE OF V(DG) (INTERNAL NODES)
GDER2 0    DER2  VALUE={(v(DMOS)-V(GMOS))} LDER2 DER2 0    {LDER}
RDER2 DER2 0    {RDER(LDER,FS)}


*---INTERNAL NODE FOR PLOTTING INSTANTANEOUS CRSS
*---ADDED 11072006

*ECRSSINSTX NCRSSINSTX 0 VALUE={I(GGD)/V(DER2)}
*RCRSSINSTX NCRSSINSTX 0 1

*ECRSSINST NCRSSINST 0 VALUE={V(NCRSSINSTX)*LDER}
*RCRSSINST NCRSSINST 0 1
*ECDSINSTX NCDSINSTX 0 VALUE={I(GDS)/V(DER1)}
*RCDSINSTS NCDSINSTX 0 1

*ECDSINST NCDSINST 0 VALUE={V(NCDSINSTX)*LDER}
*RCDSINST NCDSINST 0 1

.ENDS ARF521_MOS8R_IC


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*********************************************************
*MODEL: ARF521_MOS5                             *
* APPLICATION:                                  *
* MODEL OF THE APT DEVICE USING A FULL SEMICONDUCTOR   *
* MODEL AND MODELING THE THREE NON-LINEAR CAPACITNCES  *
* VERSION: MOS2                                 *
* 11/09/2006 JUAN RIVAS, MIT                    *
* KELVIN SOURCE                                 *
*********************************************************
* LIMITATIONS:                                  *
*    + RESISTANCE IN SERIES WITH COUT IS ADDED        *
*********************************************************
*NODES:                                         *
* GATE:   GATE OF THE MOSFET                    *
* DRAIN:  DRAIN OF THE MOSFET                   *
* SOURCE: SOURCE OF THE MOSFET                  *
*********************************************************
```

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*********************************************************
* PARAMETERS:                                          *
* LD: DRAIN LEAD INDUCTANCE                            *
* RD: DREAL LEAD RESISTANCE                            *
* LG: GATE LEAD INDUCTANCE                             *
* RG: GATE LEAD RESISTANCE                             *
* LS: SOURCE LEAD INDUCTANCE                           *
* RS: SOURCE LEAD RESISTANCE                           *
* RDMOS: DRAIN RESISTANCE                              *
* CGS: GATE TO SOURCE CAPACITANCE                      *
*----NON-LINEAR PARAMETER OF CDS                       *
* CDSOA: CDS @ VDS=0                                   *
* VJDSA: CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* MDSA:  CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* VBREAKDS: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDS   *
* CDSOB: CDS @ VDS=0 WHEN VBREAKDS<VDS<VLIMDS          *
* VJDSB: CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* MDSB:  CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* VLIMDS: CDS REMAINS CONSTANT FRO VDS>=VLIMDS         *
*----NON-LINEAR PARAMETER OF CGD                       *
* CGDOA: CDG @ VDG=0                                   *
* VJGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD *
* MGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD *
* VBREAKGD: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDG   *
* CGDOB: CDS @ VGD=0 WHEN VBREAKGD<VDG<VLIMGD          *
* VJGDB: CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD *
* MGDB:  CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD *
* VLIMGD:CDG REMAINS CONSTANT FOR VGD>=VLIMGD          *
*---DC PARAMETERS OF THE LEVEL 1 MOSFET                *
* KP: TRANSCONDUCTANCE COEFFICIENT                     *
* LAMBDA: CHANNEL-LENGTH MODULATION                    *
* VTO: ZERO-BIAS THRESHOLD VOLTAGE                     *
*---BACK-DIODE PARAMETERS                              *
* ISD: DIODE-SATURATION CURRENT                        *
* ND: DIODE EMISSION COEFFICIENT                       *
* RSD: DIODE OHOMIC RESISTANCE                         *
* BVD: DIODE BREAKDOWN VOLTAGE                         *
*********************************************************


.SUBCKT ARF521_MOS5  GATE DRAIN SOURCE SOURCE2 + PARAMS: + LD=1.5n +
RD=20m + LG=1.3n + RG=0.123    ;FROM APT SPICE MODEL (NEED
CONFIRMATION) + LS=1.1n + RS=20m + LS2=1.1n + RS2=20M
*+ RDMOS=0.213 ;FROM APT SPICE MODEL (NEED CONFIRMATION)
+ RDMOS=0.3 + CGS=789.63PF    ;FROM APT SPICE MODEL (NEED
```

CONFIRMATION) I GOT AROUND 789PF ON 10302006
*----NON-LINEAR PARAMETER OF CDS
+ CDSOA=1878P + VJDSA=2.1452262 + MDSA=0.8639769 + VBREAKDS=15 +
CDSOB=1878e-12 + VJDSB=0.612314175 + MDSB=0.64778395 + VLIMDS=1000
*----RESISTNACE IN SERIES WITH CDS
+ RCDS=0.3   ;CHECK!!!
*----NON-LINEAR PARAMETER OF CGD
*+ CGDOA=600p
+ CGDOA=2000P + VJGDA=0.04836 + MGDA=0.392688 + VBREAKGD=15 +
CGDOB=108p + VJGDB=0.04836 + MGDB=0.392688 + VLIMGD=1000
*----LEVEL 1 MOSFET PARAMETERS
+ KP=0.7774 + LAMBDA=0.0105 + VTO=3.2
*----BACK DIODE PARAMETERS
+ ISD=41.5N + ND=1.5 + RSD=10M + BVD=500 + RDIODE=40M

****
***SUBCIRCUIT DESCRIPTION ***
****

*--DRAIN TERMINAL
LD DRAIN D1 {LD} ic=0 RD D1   D2 {RD}

*--GATE TERMINAL
LG GATE G1   {LG} ic=0 RG G1   GMOS   {RG} CGS GMOS SMOS   {CGS}
;LINEAR GATE TO SOURCE CAPACITANCE

*--SOURCE TERMINAL
LS SOURCE S1   {LS} ic=0 RS S1   SMOS {RS}

*---SOURCE TERMINAL 2
LS2 SOURCE2 S2 {LS2} ic=0 RS2 S2   SMOS {RS2}

*--NMOSFET MODEL
RDMOS D2 DMOS {RDMOS} M1   DMOS GMOS SMOS SMOS MOSFET L=1U W=1U
*.MODEL MOSFET NMOS (LEVEL=1 KP=0.7774 LAMBDA=0.0105 VTO=3.2)
.MODEL MOSFET NMOS (LEVEL=1 KP={KP} LAMBDA={LAMBDA} VTO={VTO})
*--BACK DIODE
DSD SMOS D2Z DSUB RSD D2Z D2 {RDIODE}
*.MODEL DSUB D (IS=41.5N N=1.5 RS=60M BV=500)
.MODEL DSUB D (IS={ISD} N={ND} RS={RSD} BV={BVD})

*--NON LINEAR CDS
GDS D2 D2X   VALUE={ + IF(v(D2,SMOS)<=0,(V(DER1)*CDSOA)/LDER, +

```
IF(v(D2,SMOS)<=VBREAKDS,
+(V(DER1)*CDSOA/(1+v(D2,SMOS)/VJDSA)**MDSA)/LDER, +
IF(v(D2,SMOS)<=VLIMDS,
+(V(DER1)*CDSOB/(1+v(D2,SMOS)/VJDSB)**MDSB)/LDER, +
(V(DER1)*CDSOB/(1+VLIMDS/VJDSB)**MDSB)/LDER + ) + ) + ) + }

*RESISTANCE IN SERIES WITH CDS
RCDS D2X SMOS {RCDS}

**--NON LINEAR CRSS
GGD  DMOS GMOS VALUE={ + IF(V(DMOS,SMOS)<=0, +(V(DER2)*CGDOA)/LDER,
+ IF(V(DMOS,SMOS)<=VBREAKGD,
+(V(DER2)*CGDOA/(1+V(DMOS,SMOS)/VJGDA)**MGDA)/LDER, +
IF(V(DMOS,SMOS)<=VLIMGD,
+(V(DER2)*CGDOB/(1+V(DMOS,SMOS)/VJGDB)**MGDB)/LDER, +
(V(DER2)*CGDOB/(1+VLIMGD/VJGDB)**MGDB)/LDER + ) + ) + ) + }

****SUBCIRCUITS TO EVALUATE DERIVATIVE***
.PARAM: + LDER=1U   ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.14159265

*--FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}

*--GETS THE DERIVATIVE OF V(DS) (INTERNAL NODES)
GDER1 0    DER1 VALUE={(v(D2)-V(D2X))} LDER1 DER1 0    {LDER} RDER1
DER1 0    {RDER(LDER,FS)}

*--GETS THE DERIVATIVE OF V(DG) (INTERNAL NODES)
GDER2 0    DER2  VALUE={(v(DMOS)-V(GMOS))} LDER2 DER2 0    {LDER}
RDER2 DER2 0    {RDER(LDER,FS)}


*---INTERNAL NODE FOR PLOTTING INSTANTANEOUS CRSS
*---ADDED 11072006

*ECRSSINSTX NCRSSINSTX 0 VALUE={I(GGD)/V(DER2)}
*RCRSSINSTX NCRSSINSTX 0 1

*ECRSSINST NCRSSINST 0 VALUE={V(NCRSSINSTX)*LDER}
*RCRSSINST NCRSSINST 0 1
*ECDSINSTX NCDSINSTX 0 VALUE={I(GDS)/V(DER1)}
*RCDSINSTS NCDSINSTX 0 1
```

```
*ECDSINST NCDSINST 0 VALUE={V(NCDSINSTX)*LDER}
*RCDSINST NCDSINST 0 1


.ENDS ARF521_MOS5



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**********************************************************
*MODEL: ARF521_MOS8R                                    *
* APPLICATION:                                          *
* MODEL OF THE APT DEVICE USING A FULL SEMICONDUCTOR    *
* MODEL AND MODELING THE THREE NON-LINEAR CAPACITNCES   *
* VERSION: MOS2                                         *
* 11/09/2006 JUAN RIVAS, MIT                            *
* KELVIN SOURCE                                         *
**********************************************************
* LIMITATIONS:                                          *
*    + RESISTANCE IN SERIES WITH COUT IS ADDED      *
**********************************************************
*NODES:                                                 *
* GATE:   GATE OF THE MOSFET                            *
* DRAIN:  DRAIN OF THE MOSFET                           *
* SOURCE: SOURCE OF THE MOSFET                          *
**********************************************************
**********************************************************
* PARAMETERS:                                           *
* LD: DRAIN LEAD INDUCTANCE                             *
* RD: DREAL LEAD RESISTANCE                             *
* LG: GATE LEAD INDUCTANCE                              *
* RG: GATE LEAD RESISTANCE                              *
* LS: SOURCE LEAD INDUCTANCE                            *
* RS: SOURCE LEAD RESISTANCE                            *
* RDMOS: DRAIN RESISTANCE                               *
* CGS: GATE TO SOURCE CAPACITANCE                       *
*----NON-LINEAR PARAMETER OF CDS                        *
* CDSOA: CDS @ VDS=0                                    *
* VJDSA: CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* MDSA:  CHARACTERIZE NON-LINEAR CDS FOR 0<VDS<=VBREAKDS *
* VBREAKDS: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDS    *
* CDSOB: CDS @ VDS=0 WHEN VBREAKDS<VDS<VLIMDS           *
* VJDSB: CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* MDSB:  CHARAC. NON-LINEAR CDS FOR VBREADLS<VDS<=VLIMDS *
* VLIMDS: CDS REMAINS CONSTANT FRO VDS>=VLIMDS          *
*----NON-LINEAR PARAMETER OF CGD                        *
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```
* CGDOA: CDG @ VDG=0                                          *
* VJGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD *
* MGDA: CHARACTERIZE NON-LINEAR CDG FOR 0<VDG<=VBREAKGD  *
* VBREAKGD: BREAKPOINT IN NON-LINEAR BEHAVIOR OF CDG     *
* CGDOB: CDS @ VGD=0 WHEN VBREAKGD<VDG<VLIMGD            *
* VJGDB: CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD  *
* MGDB:  CHARAC. NON-LINEAR CDG FOR VBREAGD<VDG<=VLIMGD  *
* VLIMGD:CDG REMAINS CONSTANT FOR VGD>=VLIMGD            *
*---DC PARAMETERS OF THE LEVEL 1 MOSFET                 *
* KP: TRANSCONDUCTANCE COEFFICIENT                      *
* LAMBDA: CHANNEL-LENGTH MODULATION                     *
* VTO: ZERO-BIAS THRESHOLD VOLTAGE                      *
*---BACK-DIODE PARAMETERS                               *
* ISD: DIODE-SATURATION CURRENT                         *
* ND: DIODE EMISSION COEFFICIENT                        *
* RSD: DIODE OHOMIC RESISTANCE                          *
* BVD: DIODE BREAKDOWN VOLTAGE                          *
***********************************************************


.SUBCKT ARF521_MOS8r  GATE DRAIN SOURCE SOURCE2 + PARAMS: + LD=1.5n
+ RD=20m + LG=1.3n + RG=0.123     ;FROM APT SPICE MODEL (NEED
CONFIRMATION) + LS=1.1n + RS=20m + LS2=1.1n + RS2=20M
*+ RDMOS=0.213 ;FROM APT SPICE MODEL (NEED CONFIRMATION)
+ RDMOS=0.3 + CGS=752PF    ;MEASURED BY JOHN RANSON
*----NON-LINEAR PARAMETER OF CDS
+ CDSOA=1945P + VJDSA=0.6606 + MDSA=0.5640 + VBREAKDS=15 +
CDSOB=3960P + VJDSB=0.2064 + MDSB=0.6923 + CDSOFFB=23P + VLIMDS=500
*----RESISTNACE IN SERIES WITH CDS
+ RCDS=0.3  ;CHECK!!!
*----NON-LINEAR PARAMETER OF CGD
+ CGDOA=546p + VJGDA=6.1666 + MGDA=1.6619 + VBREAKGD=15 + CGDOB=494P
+ VJGDB=0.0232 + MGDB=0.5237 + VLIMGD=500



*----LEVEL 1 MOSFET PARAMETERS
+ KP=0.7774 + LAMBDA=0.0105 + VTO=3.2
*----BACK DIODE PARAMETERS
+ ISD=41.5N + ND=1.5 + RSD=10M + BVD=500 + RDIODE=40M


****************************
***SUBCIRCUIT DESCRIPTION ***
****************************


*--DRAIN TERMINAL
```

```
LD DRAIN D1 {LD} ic=0 RD D1    D2 {RD}


*--GATE TERMINAL
LG  GATE  G1    {LG} ic=0 RG  G1    GMOS  {RG} CGS GMOS  SMOS  {CGS}
;LINEAR GATE TO SOURCE CAPACITANCE


*--SOURCE TERMINAL
LS SOURCE S1   {LS} ic=0 RS S1     SMOS {RS}



*---SOURCE TERMINAL 2
LS2 SOURCE2 S2 {LS2} ic=0 RS2 S2      SMOS {RS2}


*--NMOSFET MODEL
RDMOS D2  DMOS {RDMOS} M1    DMOS GMOS SMOS SMOS MOSFET L=1U W=1U
*.MODEL MOSFET NMOS (LEVEL=1 KP=0.7774 LAMBDA=0.0105 VTO=3.2)
.MODEL MOSFET NMOS (LEVEL=1 KP={KP} LAMBDA={LAMBDA} VTO={VTO})
*--BACK DIODE
DSD SMOS D2Z  DSUB RSD D2Z D2 {RDIODE}
*.MODEL DSUB D (IS=41.5N N=1.5 RS=60M BV=500)
.MODEL DSUB D (IS={ISD} N={ND} RS={RSD} BV={BVD})



*--NON LINEAR CDS
GDS D2 D2X    VALUE={ + IF(v(D2,SMOS)<=0,V(DER1)*(1/LDER)*CDSOA, +
IF(v(D2,SMOS)<=VBREAKDS,
+V(DER1)*(1/LDER)*CDSOA/(1+v(D2,SMOS)/VJDSA)**MDSA, +
IF(v(D2,SMOS)<=VLIMDS,
+(V(DER1)*(1/LDER)*(CDSOB/((1+v(D2,SMOS)/VJDSB)**MDSB)+CDSOFFB)), +
V(DER1)*(1/LDER)*CDSOB/(1+VLIMDS/VJDSB)**MDSB + ) + ) + ) + }



*RESISTANCE IN SERIES WITH CDS
RCDS D2X SMOS {RCDS}


**--NON LINEAR CRSS
GGD  DMOS GMOS VALUE={ + IF(V(DMOS,GMOS)<=0,V(DER2)*(1/LDER)*CGDOA,
+ IF(V(DMOS,GMOS)<=VBREAKGD,
+V(DER2)*(1/LDER)*CGDOA/(1+V(DMOS,GMOS)/VJGDA)**MGDA, +
IF(V(DMOS,GMOS)<=VLIMGD,
V(DER2)*(1/LDER)*CGDOB/(1+V(DMOS,GMOS)/VJGDB)**MGDB, +
V(DER2)*(1/LDER)*CGDOB/(1+VLIMGD/VJGDB)**MGDB + ) + ) + ) + }
```

```
****SUBCIRCUITS TO EVALUATE DERIVATIVE***
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.14159265358979

*--FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {3000*2*PI*FS*LDER}

*--GETS THE DERIVATIVE OF V(DS) (INTERNAL NODES)
GDER1 0    DER1 VALUE={(v(D2)-V(D2X))} LDER1 DER1 0    {LDER} RDER1
DER1 0    {RDER(LDER,FS)}

*--GETS THE DERIVATIVE OF V(DG) (INTERNAL NODES)
GDER2 0    DER2   VALUE={(v(DMOS)-V(GMOS))} LDER2 DER2 0    {LDER}
RDER2 DER2 0    {RDER(LDER,FS)}


*---INTERNAL NODE FOR PLOTTING INSTANTANEOUS CRSS
*---ADDED 11072006

*ECRSSINSTX NCRSSINSTX 0 VALUE={I(GGD)/V(DER2)}
*RCRSSINSTX NCRSSINSTX 0 1

*ECRSSINST NCRSSINST 0 VALUE={V(NCRSSINSTX)*LDER}
*RCRSSINST NCRSSINST 0 1
*ECDSINSTX NCDSINSTX 0 VALUE={I(GDS)/V(DER1)}
*RCDSINSTS NCDSINSTX 0 1

*ECDSINST NCDSINST 0 VALUE={V(NCDSINSTX)*LDER}
*RCDSINST NCDSINST 0 1

.ENDS ARF521_MOS8R

*$
```

C.9.2   Library for PD57060 from AS

```
MOSNL3_ST_new.lib
```

```
*****************************************************
```

```
* MODEL: MOSFETNLC - For PD57060 in POWERSO-10RF package *
* APPLICATION:                                           *
* SIMPLIFIED MODEL USING A PIECEWISE SWITCH-RESISTOR     *
* COMBINATION TO GET TF, AND A NONLINEAR CAPACITOR       *
* VERSION 1.1                                            *
* LIMITATIONS:                                           *
* 26 Jan 06                                              *
*********************************************************
* PARAMETERS:                               *
* RDSON: ON RESISTANCE                                   *
* RG: GATE RESISTANCE                                    *
* CGS:  LINEAR GATE TO SOURCE CAPACITANCE                *
* COUT: NON-LINEAR DRAIN TO SOURCE CAPACITANCE           *
* RCOUT: RESISTANCE IN SERIES WITH D-S CAPACITANCE       *
* RSHUNT: DRAIN TO SOURCE RESISTANCE TO ACCOUNT FOR OFF  *
*         CURRENT                                        *
* KRES: RESISTANCE TEMP. SCALING COEF.                   *
*********************************************************
* NODES:                                          *
* GATE: GATE OF THE MOSFET                               *
* DRAIN: DRAIN OF THE MOSFET                             *
* SOURCE: SOURCE OF THE MOSFET                           *
*********************************************************

*$
.SUBCKT MOSNLC_IC_SIMPLIFIED  GATE DRAIN SOURCE + PARAMS: +
RDSON=0.373;0.233;0.118 ;Note:  this parameter doesn't do anything,
just for reference... + RG=195M + CGS=106P
**+ VCGS0=0
+ RCOUT={0.3275*KRES} + RSHUNT=12MEG + CJO=228.25P +
VJ=0.16803565837623 + M=0.22055813533587 + LDRAIN = 400P + LSOURCE =
200P + LGATE = 400P + CRSS = 10p + KRES = 2
****** NOTE ****** KRES is currently set assuming a worst case 2x
****************rise in Rdson vs. temp

LDRAIN DRAIN DRAINL {LDRAIN} RSHUNT DRAINL SOURCEL {RSHUNT} LSOURCE
SOURCEL SOURCE {LSOURCE}


*SW      DRAINL   SOURCEL   GMAIN   SOURCE   SWIDEAL
*.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5 ILIMIT=50)

.PARAM: + R1=RDSON;;    example, simplified model
*+ R1 = 65
```

```
+ VRD1 = 2.5


*************************************************************************

SW1      DRAINL  SOURCEL  GMAIN  SOURCE   SRD1 .MODEL SRD1 VSWITCH
(RON={R1*Kres} ROFF=1MEG VON={VRD1} VOFF={VRD1-1})


*************************************************************************



*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT SOURCE
GCNL  N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,
+CJO*V(201)*(1/LDER),
+V(201)*(1/LDER)*(CJO/((1+((V(DRAINL)-V(N101))/VJ))**M)))}

DIDEAL SOURCEL DRAINL DIODE
*.model DIODE D(N=.0001)
.model DIODE D(N=0.5 RS=0.2 TT=5n) ; Models chars of body diode

RCOUT N101   SOURCEL {RCOUT}

LGATE GATE GATEL {LGATE} ;RSER=10m RPAR=1MEG RG  GATEL GMAIN     {RG}
CGS GMAIN SOURCEL {CGS}   ;RSER=10m RPAR=1MEG
*RRSS DRAINL DRAINR 10
CRSS DRAINL GMAIN {CRSS} ;RSER=30 RPAR=1MEG



****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER} GY 0 201
VALUE={V(N101)-V(DRAINL)} L1 201 0 {LDER} R1 201 0 {RDER(LDER,FS)}
.ENDS MOSNLC_IC_SIMPLIFIED
*$
.SUBCKT MOSFETNLC_IC  GATE DRAIN SOURCE + PARAMS: +
RDSON=0.373;0.233;0.118 ;Note:  this parameter doesn't do anything,
just for reference... + RG=195M + CGS=106P + VCGS0=0 +
```

```
RCOUT={0.3275*KRES} + RSHUNT=12MEG + CJO=228.25P +
VJ=0.16803565837623 + M=0.22055813533587 + LDRAIN = 400P + LSOURCE =
200P + LGATE = 400P + CRSS = 10p + KRES = 2
****** NOTE ****** KRES is currently set assuming a worst
*******************case 2x rise in Rdson vs. temp

LDRAIN DRAIN DRAINL {LDRAIN} RSHUNT DRAINL SOURCEL {RSHUNT} LSOURCE
SOURCEL SOURCE {LSOURCE}


*SW      DRAINL   SOURCEL   GMAIN   SOURCE    SWIDEAL
*.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5 ILIMIT=50)

.PARAM: + R1 = 65 + VRD1 = 2.5 + R2 = 57.61 + VRD2 = 3 + R3 = 12.2 +
VRD3 = 3.5 + R4 = 6.93 + VRD4 = 4 + R5 = 0.916 + VRD5 = 4.5 + R6 =
0.523 + VRD6 = 5 + R7 = 7.55 + VRD7 = 5.5 + R8 = .881 + VRD8 = 6


***********************************************************************

SW1     DRAINL   SOURCEL   GMAIN   SOURCE    SRD1 .MODEL SRD1 VSWITCH
(RON={R1*Kres} ROFF=1MEG VON={VRD1} VOFF={VRD1-1})

SW2     DRAINL   SOURCEL   GMAIN   SOURCE    SRD2 .MODEL SRD2 VSWITCH
(RON={R2*Kres} ROFF=1MEG VON={VRD2} VOFF={VRD1})

SW3     DRAINL   SOURCEL   GMAIN   SOURCE    SRD3 .MODEL SRD3 VSWITCH
(RON={R3*Kres} ROFF=1MEG VON={VRD3} VOFF={VRD2})

SW4     DRAINL   SOURCEL   GMAIN   SOURCE    SRD4 .MODEL SRD4 VSWITCH
(RON={R4*Kres} ROFF=1MEG VON={VRD4} VOFF={VRD3})

SW5     DRAINL   SOURCEL   GMAIN   SOURCE    SRD5 .MODEL SRD5 VSWITCH
(RON={R5*Kres} ROFF=1MEG VON={VRD5} VOFF={VRD4})

SW6     DRAINL   SOURCEL   GMAIN   SOURCE    SRD6 .MODEL SRD6 VSWITCH
(RON={R6*Kres} ROFF=1MEG VON={VRD6} VOFF={VRD5})

SW7     DRAINL   SOURCEL   GMAIN   SOURCE    SRD7 .MODEL SRD7 VSWITCH
(RON={R7*Kres} ROFF=1MEG VON={VRD7} VOFF={VRD6})

SW8     DRAINL   SOURCEL   GMAIN   SOURCE    SRD8 .MODEL SRD8 VSWITCH
(RON={R8*Kres} ROFF=1MEG VON={VRD8} VOFF={VRD7})
```

```
***************************************************************************


*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT SOURCE
GCNL  N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,
+CJO*V(201)*(1/LDER),
+V(201)*(1/LDER)*(CJO/((1+((V(DRAINL)-V(N101))/VJ))**M)))}

DIDEAL SOURCEL DRAINL DIODE
*.model DIODE D(N=.0001)
.model DIODE D(N=0.5 RS=0.2 TT=5n) ; Models chars of body diode

RCOUT N101   SOURCEL {RCOUT}

LGATE GATE GATEL {LGATE} ;RSER=10m RPAR=1MEG RG  GATEL GMAIN   {RG}
CGS GMAIN SOURCEL {CGS} {VCGSO} ;RSER=10m RPAR=1MEG
*RRSS DRAINL DRAINR 10
CRSS DRAINL GMAIN {CRSS} ;RSER=30 RPAR=1MEG




****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER} GY 0 201
VALUE={V(N101)-V(DRAINL)} L1 201 0 {LDER} R1 201 0 {RDER(LDER,FS)}
.ENDS MOSFETNLC_IC
*$
.SUBCKT SPN1443  GATE DRAIN SOURCE + PARAMS: +
RDSON=.1;;0.373;0.233;0.118 ;Note:  this parameter doesn't do
anything, just for reference... + RG=.2;;195M + CGS=160P +
RCOUT=.2;;{0.3275*KRES} + RSHUNT=12MEG + CJO=240p +
VJ=1;;0.16803565837623 + M=.5;;0.22055813533587 + LDRAIN = 400P +
LSOURCE = 200P + LGATE = 400P + CRSS = 50p + KRES = 2
****** NOTE ****** KRES is currently set assuming a worst case
*****************2x rise in Rdson vs. temp

LDRAIN DRAIN DRAINL {LDRAIN} RSHUNT DRAINL SOURCEL {RSHUNT} LSOURCE
SOURCEL SOURCE {LSOURCE}
```

```
*SW       DRAINL   SOURCEL   GMAIN  SOURCE    SWIDEAL
*.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5 ILIMIT=50)


SW1       DRAINL   SOURCEL   GMAIN  SOURCE    SRD1 .MODEL SRD1 VSWITCH
(RON={Rdson} ROFF=1MEG VON={1} VOFF={0})


*.PARAM:
*+ R1 = 65
*+ VRD1 = 2.5
*+ R2 = 57.61
*+ VRD2 = 3
*+ R3 = 12.2
*+ VRD3 = 3.5
*+ R4 = 6.93
*+ VRD4 = 4
*+ R5 = 0.916
*+ VRD5 = 4.5
*+ R6 = 0.523
*+ VRD6 = 5
*+ R7 = 7.55
*+ VRD7 = 5.5
*+ R8 = .881
*+ VRD8 = 6


*******************************************************************************

*SW1       DRAINL   SOURCEL   GMAIN  SOURCE    SRD1
**.MODEL SRD1 VSWITCH (RON={R1*Kres} ROFF=1MEG VON={VRD1} VOFF={VRD1-1})


*SW2       DRAINL   SOURCEL   GMAIN  SOURCE    SRD2
*.MODEL SRD2 VSWITCH (RON={R2*Kres} ROFF=1MEG VON={VRD2} VOFF={VRD1})


*SW3       DRAINL   SOURCEL   GMAIN  SOURCE    SRD3
*.MODEL SRD3 VSWITCH (RON={R3*Kres} ROFF=1MEG VON={VRD3} VOFF={VRD2})


*SW4       DRAINL   SOURCEL   GMAIN  SOURCE    SRD4
*.MODEL SRD4 VSWITCH (RON={R4*Kres} ROFF=1MEG VON={VRD4} VOFF={VRD3})


*SW5       DRAINL   SOURCEL   GMAIN  SOURCE    SRD5
*.MODEL SRD5 VSWITCH (RON={R5*Kres} ROFF=1MEG VON={VRD5} VOFF={VRD4})


*SW6       DRAINL   SOURCEL   GMAIN  SOURCE    SRD6
```

```
*.MODEL SRD6 VSWITCH (RON={R6*Kres} ROFF=1MEG VON={VRD6} VOFF={VRD5})

*SW7       DRAINL    SOURCEL   GMAIN   SOURCE    SRD7
*.MODEL SRD7 VSWITCH (RON={R7*Kres} ROFF=1MEG VON={VRD7} VOFF={VRD6})

*SW8       DRAINL    SOURCEL   GMAIN   SOURCE    SRD8
*.MODEL SRD8 VSWITCH (RON={R8*Kres} ROFF=1MEG VON={VRD8} VOFF={VRD7})



*****************************************************************************



*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT SOURCE
GCNL   N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,
+CJO*V(201)*(1/LDER),
+V(201)*(1/LDER)*(CJO/((1+((V(DRAINL)-V(N101))/VJ))**M)))}

DIDEAL SOURCEL DRAINL DIODE
*.model DIODE D(N=.0001)
.model DIODE D(N=0.5 RS=0.2 TT=5n) ; Models chars of body diode

RCOUT N101    SOURCEL {RCOUT}

LGATE GATE GATEL {LGATE} ;RSER=10m RPAR=1MEG RG  GATEL GMAIN    {RG}
CGS GMAIN SOURCEL {CGS} ;RSER=10m RPAR=1MEG
*RRSS DRAINL DRAINR 10
CRSS DRAINL GMAIN {CRSS} ;RSER=30 RPAR=1MEG



****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER} GY 0 201
VALUE={V(N101)-V(DRAINL)} L1 201 0 {LDER} R1 201 0 {RDER(LDER,FS)}
.ENDS SPN1443
*$
.SUBCKT fakemos  GATE DRAIN SOURCE + PARAMS: +
RDSON=0.373;0.233;0.118 ;Note:  this parameter doesn't do anything,
```

just for reference... + RG=195M + CGS=106P + RCOUT={0.3275*KRES} +
RSHUNT=12MEG
*+ CJO=228.25P
*+ VJ=0.16803565837623
*+ M=0.22055813533587
+ Cds = 120p + LDRAIN = 400P + LSOURCE = 200P + LGATE = 400P + CRSS
= 10p + KRES = 2
****** NOTE ****** KRES is currently set assuming a worst case
*****************2x rise in Rdson vs. temp

LDRAIN DRAIN DRAINL {LDRAIN} RSHUNT DRAINL SOURCEL {RSHUNT} LSOURCE
SOURCEL SOURCE {LSOURCE}

.PARAM: + R1 = 65 + VT = 2
****

SW1   DRAINL   SOURCEL   GMAIN   SOURCE   SRD1 .MODEL SRD1 VSWITCH
(RON={R1*Kres} ROFF=1MEG VON={VT} VOFF={VT-1})

Cds Drainl sourcel {Cds}
****
Rgate gmain gate 1p Rgate2 gmain 0 1g

.ENDS fakemos
*$
.SUBCKT MOSFETNLC GATE DRAIN SOURCE + PARAMS: +
RDSON=0.373;0.233;0.118 ;Note: this parameter doesn't do anything,
just for reference... + RG=195M + CGS=106P + RCOUT={0.3275*KRES} +
RSHUNT=12MEG + CJO=228.25P + VJ=0.16803565837623 +
M=0.22055813533587 + LDRAIN = 400P + LSOURCE = 200P + LGATE = 400P +
CRSS = 10p + KRES = 2
****** NOTE ****** KRES is currently set assuming a worst case
*****************2x rise in Rdson vs. temp

LDRAIN DRAIN DRAINL {LDRAIN} RSHUNT DRAINL SOURCEL {RSHUNT} LSOURCE
SOURCEL SOURCE {LSOURCE}

*SW   DRAINL   SOURCEL   GMAIN   SOURCE   SWIDEAL
*.MODEL SWIDEAL VSWITCH (RON={RDSON} ROFF=1MEG VON=2.5 VOFF=1.5 ILIMIT=50)

.PARAM: + R1 = 65 + VRD1 = 2.5 + R2 = 57.61 + VRD2 = 3 + R3 = 12.2 +

VRD3 = 3.5 + R4 = 6.93 + VRD4 = 4 + R5 = 0.916 + VRD5 = 4.5 + R6 =
0.523 + VRD6 = 5 + R7 = 7.55 + VRD7 = 5.5 + R8 = .881 + VRD8 = 6

```
***********************************************************************

SW1      DRAINL    SOURCEL   GMAIN   SOURCE    SRD1 .MODEL SRD1 VSWITCH
(RON={R1*Kres} ROFF=1MEG VON={VRD1} VOFF={VRD1-1})

SW2      DRAINL    SOURCEL   GMAIN   SOURCE    SRD2 .MODEL SRD2 VSWITCH
(RON={R2*Kres} ROFF=1MEG VON={VRD2} VOFF={VRD1})

SW3      DRAINL    SOURCEL   GMAIN   SOURCE    SRD3 .MODEL SRD3 VSWITCH
(RON={R3*Kres} ROFF=1MEG VON={VRD3} VOFF={VRD2})

SW4      DRAINL    SOURCEL   GMAIN   SOURCE    SRD4 .MODEL SRD4 VSWITCH
(RON={R4*Kres} ROFF=1MEG VON={VRD4} VOFF={VRD3})

SW5      DRAINL    SOURCEL   GMAIN   SOURCE    SRD5 .MODEL SRD5 VSWITCH
(RON={R5*Kres} ROFF=1MEG VON={VRD5} VOFF={VRD4})

SW6      DRAINL    SOURCEL   GMAIN   SOURCE    SRD6 .MODEL SRD6 VSWITCH
(RON={R6*Kres} ROFF=1MEG VON={VRD6} VOFF={VRD5})

SW7      DRAINL    SOURCEL   GMAIN   SOURCE    SRD7 .MODEL SRD7 VSWITCH
(RON={R7*Kres} ROFF=1MEG VON={VRD7} VOFF={VRD6})

SW8      DRAINL    SOURCEL   GMAIN   SOURCE    SRD8 .MODEL SRD8 VSWITCH
(RON={R8*Kres} ROFF=1MEG VON={VRD8} VOFF={VRD7})

***********************************************************************

*NONLINEAR CAPACITANCE EVALUATED AS A CONTROLLED CURRENT SOURCE
GCNL N101 DRAINL VALUE={IF((V(DRAINL)-V(N101))<0,
+CJO*V(201)*(1/LDER),
+V(201)*(1/LDER)*(CJO/((1+((V(DRAINL)-V(N101))/VJ))**M)))}

DIDEAL SOURCEL DRAINL DIODE
*.model DIODE D(N=.0001)
.model DIODE D(N=0.5 RS=0.2 TT=5n) ; Models chars of body diode

RCOUT N101    SOURCEL {RCOUT}
```

```
LGATE GATE GATEL {LGATE} ;RSER=10m RPAR=1MEG RG  GATEL GMAIN    {RG}
CGS GMAIN SOURCEL {CGS} ;RSER=10m RPAR=1MEG
*RRSS DRAINL DRAINR 10
CRSS DRAINL GMAIN {CRSS} ;RSER=30 RPAR=1MEG




****SUBCIRCUIT TO EVALUATE THE DERIVATIVE***

*PARAMETERS AND DEFINITION FOR THIS SUBCIRCUIT
.PARAM: + LDER=.01U    ;INDUCT FOR THE DERIVATIVE SUBCIRCUIT +
PI=3.1416

*FUNC. FOR R OF THE DERIVATIVE SUBCIRCUIT
.FUNC RDER(LDER,FS) {1000*2*PI*FS*LDER} GY 0 201
VALUE={V(N101)-V(DRAINL)} L1 201 0 {LDER} R1 201 0 {RDER(LDER,FS)}
.ENDS MOSFETNLC
*$
```

C.9.3   Library for Rectifier from JMR

The file RECT.lib is available in [5] and is not reprinted here.

C.9.4   Library from JMR Thesis

The file THESIS.lib may be found in [5] but is not reprinted here.

Bibliography

[1] N.O. Sokal and A.D. Sokal. Class E—a new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE Journal of Solid-State Circuits*, SC-10(3):168–176, June 1975.

[2] Minoru Iwadare and Shinsaku Mori. Even harmonic resonant class E tuned power amplifer without RF choke. *Electronics and Communications in Japan, Part I*, 79(1):23–30, January 1996.

[3] Andrei Grebennikov. Load network design techniques for class E RF and microwave amplifiers. *High Frequency Electronics*, pages 18–32, July 2004.

[4] Joshua W. Phinney. *Multi-resonant Passive Components for Power Conversion*. Ph.D. Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., June 2005.

[5] Juan M. Rivas. *Radio Frequency dc-dc Power Conversion*. PhD thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, September 2006.

[6] S. Ajram and G. Salmer. Ultrahigh Frequency DC-to-DC converters using GaAs power switches. *IEEE Transactions on Power Electronics*, 16(5):594–602, September 2001.

[7] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault. New architectures for radio-frequency dc/dc power conversion. *Power Electronics, IEEE Transactions on*, 21(2):380–393, March 2006.

[8] Yehui Han, Olivia Leitermann, David A. Jackson, Juan M. Rivas, and David J. Perreault. Resistance compression networks for radio-frequency power conversion. *Power Electronics, IEEE Transactions on*, 22(1):41–53, January 2007.

[9] J.M. Rivas, D. Jackson, O. Leitermann, A.D. Sagneri, Yehui Han, and D.J. Perreault. Design considerations for very high frequency dc-dc converters. In *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pages 1–11, 18-22 June 2006.

[10] R.C.N. Pilawa-Podgurski, A.D. Sagneri, J.M. Rivas, D.I. Anderson, and D.J. Perreault. High-frequency resonant boost converters. In *IEEE Power Electronics Specialists Conference*, 2007.

[11] A. Sagneri. Design of a very high frequency dc-dc boost converter. Master's thesis, Massachusetts Institute of Technology, February 2007.

[12] David A. Jackson. Design and characterization of a radio-frequency dc/dc power converter. M. Eng., Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., June 2005.

[13] James Warren, III. Cell-modulated resonant dc/dc power converter. M. Eng. Thesis, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA., August 2005.

[14] R. Redl and N.O. Sokal. A 14 MHz 100 Watt class E resonant converter: Principles, design considerations, and measured performance. In *17th Annual IEEE Power Electronics Specialists Conference Proceedings*, pages 68–77, June 1986.

[15] S. Djukić, D. Maksimović, and Z. Popović. A planar 4.5-GHz DC-DC power converter. *IEEE Transactions on Microwave Theory and Techniques*, 47(8):1457–1460, Aug. 1999.

[16] W.C. Bowman, J.F. Balicki, F.T. Dickens, R.M. Honeycutt, W.A. Nitz, W. Strauss, W.B. Suiter, and N.G. Zeisse. A resonant dc-to-dc converter operating at 22 megahertz. In *Third Annual Applied Power Electronics Conference Proceedings*, pages 3–11, 1988.

[17] Chucheng Xiao. *An Investigation of Fundamental Frequency Limitations for HF/VHF Power Conversion*. Ph.D. Thesis, Virginia Polytechnic Institute and State University, 655 Whittemore Hall (0179), July 2006.

[18] R.J. Gutmann. Application of RF circuit design principles to distributed power converters. *IEEE Transactions on Industrial Electronics and Control Instrumentation*, IEC127(3):156–164, 1980.

[19] R.L. Steigerwald. A comparison of half-bridge resonant converter topologies. *IEEE Transactions on Power Electronics*, 3(2):174–182, April 1988.

[20] F.C. Lee. High-frequency quasi-resonant converter technologies. In *Proceedings of the IEEE*, volume 76, pages 377–390, April 1988.

[21] Wojciech A. Tabisz and Fred C. Lee. Zero-Voltage-Switching Multiresonant technique–a novel approach to improve performance of high-frequency quasi-resonant converters. *IEEE Transactions on Power Electronics*, 4(4):450–458, October 1989.

[22] Y.S. Lee and Y.C. Cheng. Design of switching regulator with combined FM and on-off control. *IEEE Transactions on Aerospace and Electronic Systems*, AES-22(6):725–731, November 1986.

[23] Y.S. Lee and Y.C. Cheng. A 580 kHz switching regulator using on-off control. *Journal of the Institution of Electronic and Radio Engineers*, 57(5):221–226, September/October 1987.

[24] J. M. Rivas, R. S. Wahby, J. S. Shafran, and D. J. Perreault. New architectures for radio-frequency dc-dc power conversion. *IEEE Transactions on Power Electronics*, 21(2):380–393, March 2006.

[25] J. M. Rivas, Y. Han, O. Leitermann, A. D Sagneri, and D. J. Perreault. A high-frequency resonant inverter topology with low voltage stress. In *IEEE Power Electronics Specialist Conference*, 2007.

[26] James R Warren, III, Kathryn A. Rosowski, and David J. Perreault. Transistor selection and design of a VHF dc-dc power converter. *Power Electronics, IEEE Transactions on*, 23:27–37, Jan 2008.

[27] Nathan O. Sokal. Class-E RF Power Amplifiers. *QEX*, pages 9–20, Jan/Feb 2001.

[28] M. Kazimierczuk and K. Puczko. Exact analysis of class E tuned power amplifier at any Q and switch duty cycle. *IEEE transactions on Circuits and Systems*, 34(2):149–159, Feb. 1987.

[29] Hirotaka Koizumi, Minoru Iwadare, and Shinsaku Mori. Class E^2 dc-dc converter with second harmonic resonant class E inverter and class E rectifier. In *Third Annual Applied Power Electronics Conference Proceedings*, pages 1012–1018, 1994.

[30] Ixz210n50l & ixz221n50l rf power mosfet. Datasheet, IXYS RF, Ft. Collins, CO, 2007.

[31] Roger T. Howe and Charles G. Sodini. *Microelectronics: An Integrated Approach*, chapter 3, pages 127–133. Prentice Hall, 1997. Depletion capacitance and three-parameter model.

[32] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*, chapter 4, Characteristics of Passive IC Components, pages 114–166. Cambridge University Press, 1998, 2004. Characteristics of Passive IC Components.

[33] Thomas H. Lee. *Planar Microwave Engineering*, chapter 6.5, Inductors, pages 138–147. Cambridge University Press, 2004.

[34] Philip R. Geffe. The design of single-layer solenoids for rf filters. *Microwave Journal*, 39(12):70–76, December 1996.

[35] Charles R. Sullivan, Weidong Li, Satish Prabhakaran, and Shanshan Lu. Design and fabrication of low-loss toroidal air-core inductors. In *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, pages 1754–1759, June 2007.

[36] Deic420 20 ampere low side ultrafast rf mosfet driver. Datasheet 9200-0230 Rev 3, IXYS RF, 2002.

[37] J. M. Rivas, D. J. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault. Design Consideration for Very High Frequency dc-dc Converters. In 37th *Annual Power Electronics Specialists Conference Proceedings*, pages 2287–2297, June 2006.

[38] W. L. Everitt and G. E. Anner. *Communication Engineering*, chapter 11, Impedance Transformation, pages 403–450. McGraw Hill, 1956.

[39] Robert C. N. Pilawa-Podgurski. Design and evaluation of a very high frequency dc/dc converter. M. eng., Massachusetts Instutute of Technology, February 2007.