Global Product Development in Semiconductor industry
Intel: Tick-Tock product development Cadence

by

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Submitted to the System Design and Management Program in Partial Fulfillment of the Requirements for the Degree of Master of Science in Engineering and Management

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Abstract

This thesis investigates on changes in semiconductor industry's product development methodology by following Intel's product development from year 2000. Intel was challenged by customer's preference change, competitors new enhanced product, internet bubble burst economy, and miss steps in the business strategy. Dynamics of these challenges drove Intel to develop a new product strategy: Tick-Tock product cadence. The paper discusses reasons why Intel landed at the Tick-tock strategy and results how strong product portfolio Intel ended up constructing. The thesis further discusses how the new "Global Product Development" strategy evolves, which can take advantage of Tick-Tock cadence and deliver it to the next level helped from the effective GPD and systems engineering deployment.

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Chapter 1. Introduction

I. Motivation

The product development in the high technology industry has been always considered as a challenging task. Challenges have been especially located at chasing for the product enhancement within a short time period. These two challenges drive the product development to the opposite directions. The development period would take longer if the product need more enhancements or vice versa. Low-tech products may have the similar type of challenge but the situation gets tougher for the high tech industry because the technology evolution speed is high, the price drops rapidly, and the products become obsolete fast. The fast eroding product price and profit advised high tech industry to think about the global product development (GPD) environment. GPD was considered as a smart move because it allowed companies to tap on lower wage work force and open a new market. However, not all companies have experienced the benefit of GPD in an extremely fast changing high technology industry environment.

The paper looks for the product development strategy learning from Intel's 21st product development strategy by investigating how they overcame from the short period performance dip and implemented new development platform, Tick-tock cadence. It will be also discussed how Intel changed their GPD structure for the sustainable product roadmap.

II. Research Objective and Method

The main objective of the paper is to acquire the knowledge about the efficient semiconductor product development structure for the sustainable future roadmap and the Global Product Development strategy's contribution. The paper collected market dynamics data for past 7 year to find out reasons for the good product development structure, which is suitable for the flexible product configuration as well as for the project management. Findings and analyses from this thesis would provide good strategic background for individuals looking for the product development strategy that combines traditional focused site development and multi sites collaboration in a GPD setting.

The thesis used extensive literature search in order to help the understanding of underlying background dynamics. Interviews with Intel microprocessor architects and project managers were performed to gather product architecture information and project management information. Design Structure Matrix (DSM) was used to enhance the product structure understanding and to find the potential development structure proposal.

III. Summary of Chapters

The thesis has three main parts; History, current, and future.

From chapter 2 to chapter 4 discuss Intel's struggle in the market from 2000 to 2006 that drove Intel's current product development strategy of Tick-tock cadence.

Chapter 5 provides the case of the first two products from Tick-tock and discusses how they were managed.

Chapter 6 and chapter 7 introduce discussions for the new product development organization and explain reasons for the new structure from interviews with product managers. Chapter 8 proposes the new organization adequate for global product development by introducing the systems department.

Here are brief descriptions of each chapter.

Chapter 2: Intel's business environment in early 21st century and decisions resulted successes and failures later in 2004

Chapter 3: Microprocessor business dynamics changes from 2001 to 2004. Intel enjoyed a short-lived blockbuster success in the mobile segment and stared to lose the fame from the server market by the AMD's Opteron® processor's performance and their product development strategy. This drove Intel to develop new Tick-tock cadence and modular building block approach named RHT (Right Hand Turn)

Chapter 4: Intel's acknowledge to the market shift and move to the new product development strategy; Tick-tock cadence. Intel realized the market's preference change to competitor's product and made decisions to adjust the situation as rapid as possible. Tick-tock produce development cadence was introduced and Converged Core/Uncore/Methodology initiatives started. However, Intel was focused on the short term come back and efficiency so the strategy employed the focused-site development strategy, which was effective to produce prompt result but possessed the sustainability question.

Chapter 5: The case review of the first two products developed by Tick-tock cadence strategy.

Chapter 6: Intel's current microprocessor design organization structure analysis. The structure was analyzed by DSM and the chapter leads the thesis to the systems department proposal.

Chapter 7: Tick-tock to the next level. This chapter contains interviews with Intel's product development managers. Managers in many different levels expressed the desire for the more flexible project management structure than focused-site strategy, the best way to utilize all Intel's available development resources, the concerns around sustainability of current focused site development strategy. While Intel managers mentioned the needs for the inter-site collaboration (global product development since they like the efficient structure lay even between multiple time zone sites), several obstacles were identified to deliver the preferred efficiency.

Chapter 8: Propose of the new organization including systems department. Two proposals are suggested in this chapter. Proposals are constructed to facilitate the inter-site communication via systems department by clear deliverable definition and dynamic task/resource allocation by well-understood metrics. Systems department is proposed as a project ownership organization as well as the imminent owner of platform and modular component definition.

Chapter 2. Intel at year 2000 horizon

Around year 2000, the high-tech industry was going thru the internet boom period that had experienced over 20% annual equity market gain for five years in a row (Figure 1) [1]. There were a lot of mixed hopes and concerns around the industry's rapid growth that people had experienced since late 1960s [2]. This market environment drove the technology industry sector to evaluate three basics of business and investment strategies: 1) solidify the current business bottom line for the probable downturn, 2) look for new opportunities aggressively to take the potential upside, 3) diversify the technology investment to pool new risks. Intel's management team wanted to make careful but smart decisions their product portfolio that would accomplish both short-term financial return and long term sustainable corporate growth goal amid tough competitions from smaller players like AMD and new young start-up like Transmeta.

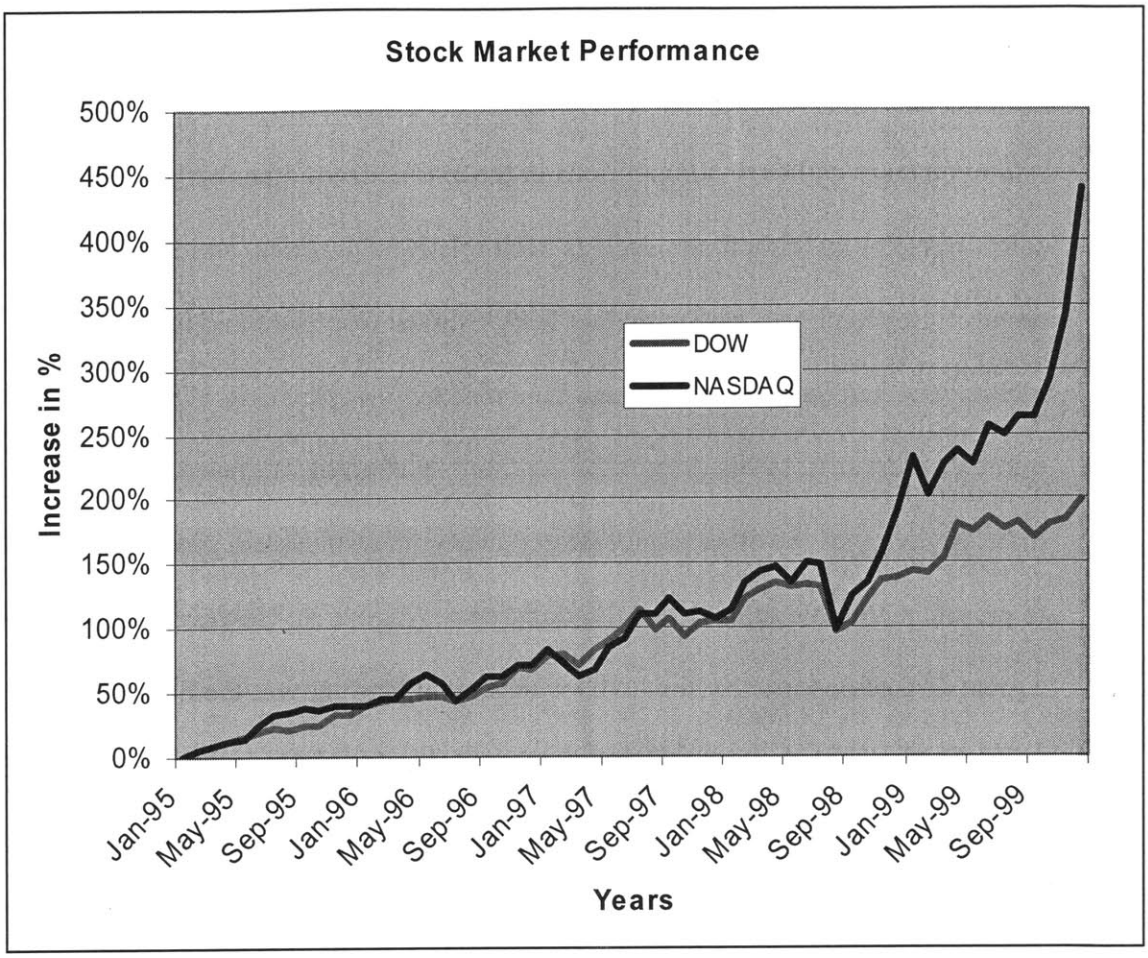

Figure 1 Stock market performance from 1995 to 2000

Intel confronted following competitions and market dynamics change at year 2000.

I. Competitions

- Challenge from Advanced Micro Devices (AMD)

  AMD had been a long time technology follower to Intel since it started as a small star-up right across the street from Intel in late 1960s. When IBM started new personal computer (PC) venture in early 1980s, Intel was forced to license the microprocessor technology to a second manufacturer and this requirement

essentially created the largest competitor Intel has today - Advanced Micro Devices [3].

Although there had been competitions in the market from other major semiconductor manufacturers such as Motorola (68000 series) and IBM PowerPC architecture) Intel became the market leader almost overnight and its x86 micro architecture had become a dominant from desktop/mobile PC in 1980s to mid/entry server in 1990s (Figure 2). As Intel's technology defused through the industry, many of the other manufacturers went out of business, merged or failed to present a credible threat to Intel's dominance (Figure 3). However, this opened a great deal of opportunity for AMD whose main product was the licensed x86 micro architecture clone. AMD eventually managed to catch up Intel for the product operating frequency which was made possible by the advanced manufacturing technology in late 1990s [4]. Around the beginning of 21st century, AMD initiated the first meaningful competition against Intel, which was the product frequency crown that broke the Giga-hertz barrier for the first time [5]. AMD claimed the pole-position with Athlon® product line and Intel had to play "reverse" catch up game with the aging Pentium 3 micro architecture. This competition drove Intel to develop new Pentium 4 architecture [6]. The Pentium 4 employed the new circuit and micro architecture called NetBurst that was mainly focused on the frequency increase [7]. Table 1 and Table 2 compare product architecture of AMD and Intel at year 2000 and 2001. The comparisons show that Intel launched Pentium 4 product at late 2000 and started to gain frequency crown back. However, Intel's Pentium 4 was blamed by users for no actual performance

benefit over the previous product [8]. NetBurst architecture had yet another problem that it consumed higher power compared to competitor's product to deliver the same level of performance [9]. This undesirable product characteristic made even harder for Intel to scale the architecture up toward higher frequency or massively integrated high performance computing cluster systems [10].

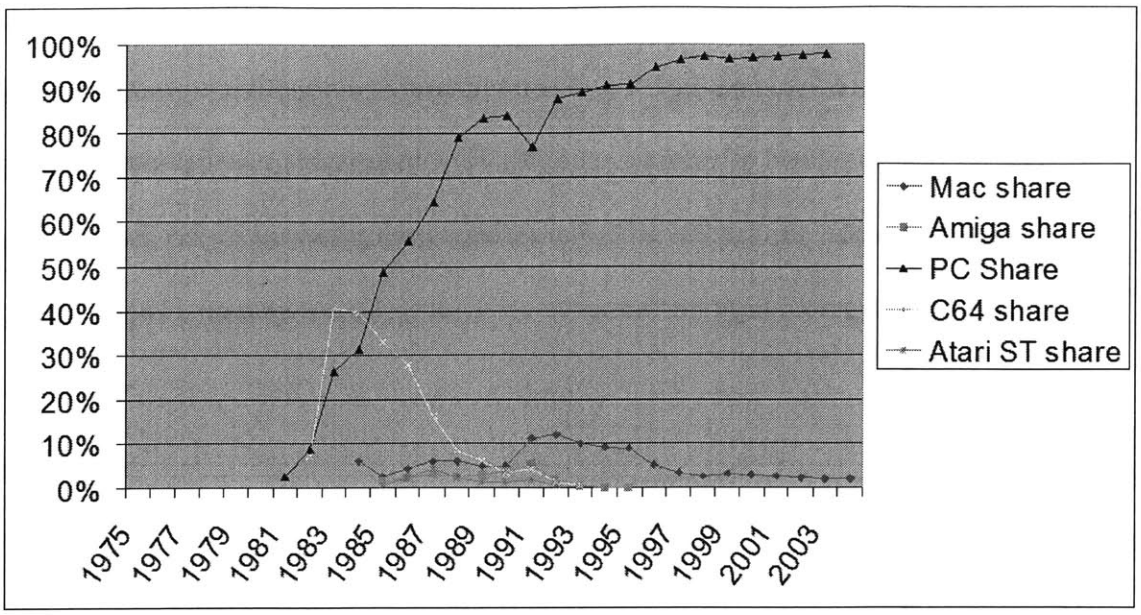

Figure 2 Historical total PC market share by architecture [11]

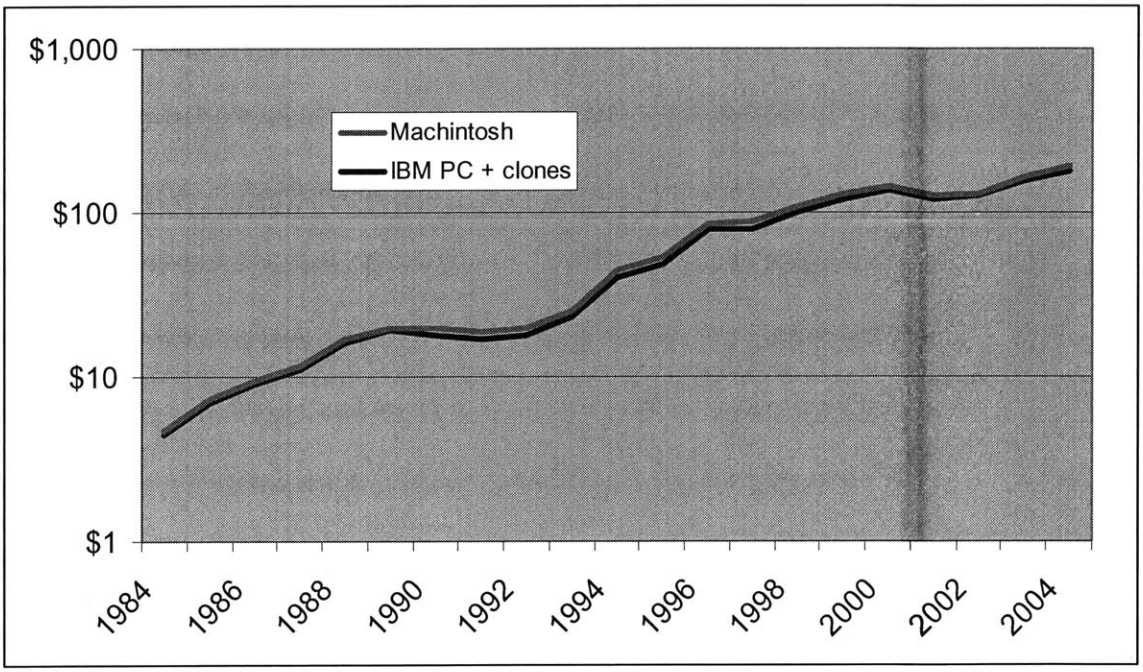

Figure 3 Historical total PC market in billion US $ by vendor [12]

CPU Specification Comparison								
	AMD Duron	**AMD Athlon**			**Intel Pentium III**		**Intel Celeron**	
Core	Spitfire	K7	K75	Thunderbird	Katmai	Coppermine	Mendocino	Coppermine128
Clock Speed	600 - 800 MHz	500 - 700 MHz	750 – 1000 MHz	750 - 1200 MHz	450 - 600 MHz	500 - 1000 MHz	300 - 533 MHz	533 - 600 MHz
L1 Cache	128KB				32KB			
L2 Cache	64KB	512KB		256KB	512KB	256KB	128KB	
L2 Cache speed	core clock	1/2 core	2/5 or 1/3 core	core clock	1/2 core	core clock		
L2 Cache bus	64-bit					256-bit	64-bit	256-bit
System Bus	100 MHz **DDR** (200 MHz effective) EV6				100 - 133 MHz GTL+		66 MHz GTL+	
Interface	Socket-A	Slot-A		Socket-A Slot-A (OEM only up to 800MHz)	Slot-1	Slot-1 Socket-370		Socket-370
Manufacturing Process	0.18 micron	0.25 micron	0.18 micron		0.25 micron	0.18 micron	0.25 micron	0.18 micron
Die Size	100mm^2	184 mm^2	102mm^2	120mm^2	128mm^2	106mm^2	153mm^2	106mm^2
Transistor Count	25 million	22 million		37 million	9.5 million	28 million	19 million	28 million

Table 1 Microprocessor product lines from Intel and AMD at October 2000 [13]

	Pentium III-S 1.13	Pentium III 1.0	Pentium 4 1.3	Pentium 4 1.4	Athlon 1.13	Athlon MP 1.2
CPU	Intel Pentium III-S 1.13GHz	Intel Pentium III 1.0GHz	Intel Pentium 4 1.3GHz	Intel Pentium 4 1.4GHz	AMD Athlon 1.13GHz	AMD Athlon MP 1.2GHz
Mainboard	ASUS TUSL2-C (i815EP B-step)		ASUS P4T (i850)		EPoX EP-8K7A (AMD-760)	
Memory	256MB PC133 SDRAM		256MB PC800 RDRAM		256MB PC2100 DDR SDRAM	
Graphics Card	Gigabyte GV-GF3000DF (NVIDIA GeForce3)					
HDD	IBM DTLA 307015					

Table 2 Typical PC configuration in September 2001 [14]

- Transmeta's smart idea.

  Transmeta was a small start-up that enlightened a new idea. Their idea was to develop a new hardware micro architecture to provide the binary level compatibility with Intel's x86 micro architecture by the software layer's help. This smart idea promised two major leapfrogs for the industry. 1) The new microprocessor development does not need to use Intel's proprietary hardware intellectual property (IP) while it delivers the similar performance of Intel's native x86 product and full software compatibility. 2) New micro architecture can be optimized for other product characteristics and market segment that Intel may have not well supported. For example, Transmeta marketed their product (Crusoe®) was optimized for the power consumption so it could deliver higher performance per power [15]. Transmeta's new venture allowed OEM system vendors to find the new application spaces like high density computing house or ultra low handheld device [16].

  Transmeta's smart idea opened new business opportunities that never explored by Intel or AMD and many technological innovations followed from OEM system vendors [17]. Crusoe® chip (Transmeta's product) was widely adopted by Japanese PC manufacturers like Sony, Sharp, and Toshiba because of Japan's unique consumer preference to the small form factor PC [18]. It also gained attractions from high-density server vendors and enabled them to introduce new "BladeServer" systems architecture [19].

Intel recognized a new challenge from a small start-up and the management started considerations to react properly for the potential market movement toward taking advantage of low power product [20].

- Competitions from system vendors: Proprietary 64 bit micro processors

  Pentium Pro® and Xeon® product line launch in 1997 was the Intel's first step to disrupt the high-end computing and server market space with x86 micro architecture [21]. This upscale computing product segment had been dominated by big system vendor's proprietary architectures (IBM mainframe, DEC VAX, Sun Sparc, HP Precision Architecture, Silicon graphics MIPS) since the beginning of the computer industry [22]. Intel's moving-up strategy was successful in a sense it was able to penetrate the market and drove clients to the industry standard architecture, which utilized Intel's x86 architecture with the commoditized system components [23]. The success started to appear in the workstation and single/dual CPU entry-level servers market, which was the relatively low-end and smallest market size in the upscale computing market. However, Intel's disruptive strategy faced tougher resistance to extend the territory further up to large server space, where all revenues and profits located. The part of the reason was the upscale market consisted of not only the microprocessor (single component) but also other complementary assets like software, service, technology deployment plan, relationship with customers, and customers legacy system support [24]. The other reason was that incumbents tried to protect the space by 64-bit computing capability, which was one of key technological advantage that Intel did not have the feature in the product line. Intel initiated the effort to enter

in this highly lucrative business by making the strategic alliance with HP and SGI. It was the pre-cursor to start new Itanium architecture (IA64). Itanium was the second computer architecture Intel explored [25]. It was generally assumed by the market that Intel's strategic effort was to win the not only high end computing market but also to place the harder entrance barrier in the lower end market so the small competitors like AMD, VIA, and other x86 clone manufacturers could not easily join into [26]. Intel decided to acquire Digital Equipment Corporation (DEC)'s advanced Alpha® microprocessor design group to accelerate the 64 bit microprocessor product development in year 2001 [27].

- Tide of the off-shoring

  In the midst of technology boom, there had been one clear product development strategy had risen, Outsourcing and global product development. Many of technology firms already established or were in the process of starting remote or satellite development sites in Asia mainly at India [28]. The outsourcing to offshore strategy was implemented mainly for the cost saving reason from lower wage and real estate but big multinational companies like Intel had the second reason. It was crucial to increase the business presence and establish relationship with the local government in the big growth potential markets such as India and China [29]. At the early stage, only the labor-intensive tasks were moved to overseas country but the tide were gradually driven to intellectually rich tasks, high technology, and eventually capital-intensive investments. Intel, just like any other technology company, felt intellectual talents in overseas and strategic investment needs (more specifically market presence

and potential subsidy contracts with local governments) [30]. The offshore outsourcing trend was apparent enough for Intel to be force to decisions rather quick. Intel made cautious steps to prepare the fully baked decisions so it could expect the better than average return without the fundamental product roadmap glitches [31]. Intel had a different outsourcing challenge that other companies with the same strategy did not have. Intel's main product line, advanced computer architecture and logic silicon design/manufacturing, had not been prosperous outside US while other outsourcing deals concentrated in software and IT that had been better developed in foreign countries. The outsourcing in the software technology business, it was easier to find experienced local talent and the outsourcing deployment did not require a huge financial asset installment. The intellectual talent in microprocessor (hardware) business, in contrary, was rarely found in low wage countries. In addition, it was assumed extremely risky to establish the advanced silicon development facility in the less-experienced locations because it required a substantial size of financial investment, the long period of technology ramp-up time, and operation risks like unstable electric power sources [32]. Intel did not have painless options to start the offshore development facilities, which it could leverage already existing local expertise by acquiring the foreign business or just fund business deals such as mergers and acquisitions (M&A).

Intel decided to start new advanced design facility at Bangalore India with the long-term site development plan. Intel also implemented proactive senior design staff relocation from experienced sites to new Bangalore design center so the local expertise could be groomed for the future product development [33][34].

- Investment diversification: Capture future growth and hedge the current market volatility.

  Around internet boom of year 2000, people's confidence in the high technology industry created the blown-up hypes and the build-up expectations for the future growth potential [35]. The market had to deal with new type of assets like "number of page views" and "number of subscribers". The valuation method for new assets was not well understood and market did not have past data to correlate. Investors concern that the technology hype might not be materialized followed naturally especially after five consecutive years of 20% equity market gain and high level price volatility [36][37]. Intel's management team needed a careful reaction strategy to take the growth opportunities while it could avoid any hiccups from some unexpected catastrophic events.

  Intel had been involved with several mergers and acquisitions in network business area and new optical technology investments as a part of effort to find the firm's next generation bread and butter segment [38][39][40]. Intel made internal efforts to cultivate the organic growth potential areas. "Intel® Play™" was launched in the hardware business sector to leverage Intel's current strength and to develop the ways to utilize the complementary assets [41]. "Intel® capital" in the strategic capital investment was started to find the better ways for accessing to the new opportunities [42]. These choices were mainly selected for the future growth potential.

  At the strategy side to make sure the current cash cow performance would persist to win the competition, Intel aggressively extended the manufacturing leadership plan

that mainly focused on the production cost reduction. Intel deployed more than 2 billion US dollar despite the economy down turn to build 300mm fabrication facility at Oregon and New Mexico [43]. The technology migration program from 130nm to 90nm technology was implemented while the industry was going under gloomy economy down turn. The combination of larger size wafer facility and smaller transistor technology manufacturing made Intel to maintain the best cost structure. These strategic manufacturing leadership program required sizeable amount of financial support so Intel's competitors could not easily imitate for the same strategy. Intel's goals to accomplish were the productivity increase and cost savings in order to make sure their excessive money was used to protect their current cash cow. The management team hoped the strategy could provide the momentum to win the competitions and the immunization to the unexpected external business environment shifts/changes [44].

II. Intel's choices at year 2000

- Decision to Pentium 4 micro architecture

  Intel made a product decision to focus its x86 product line for the frequency optimized after the surprising Giga Hertz combat with AMD's Athlon® microprocessor, which conquered the virgin land (Giga hertz) ahead of any Intel product [45][46]. Intel's new micro architecture, Pentium 4, was designed for the higher frequency from the planning to the project program execution [47]. Intel aligned all its design and manufacturing teams for the planned goal, High Frequency. The design team developed new micro-architecture called NetBurst® and the

manufacturing team accelerated for the advanced technology developments (130nm and 90nm technology) for the new design to take advantage of smaller dimension that could deliver the higher frequency. It is a widely known technique to improve the product microprocessor frequency by enhancing the manufacturing technology with no major design change [48]. This was clearly well harmonized effort to employ the best of design and manufacturing. Intel's new Pentium 4 was a successful product at the early stage of its product life because competitors (including AMD) could not match the level of frequency while Pentium 4 eventually achieved higher than 3 GHz [49]. Intel managed to reclaim the desktop x86 microprocessor unit market share from 72% before Pentium 4 to 88% after the product launch (Figure 4). However, there were the crowd of critics that Pentium 4's frequency only delivered the paper performance but not actual application performance boost compared to competitions and even its predecessor, Pentium 3® [50].

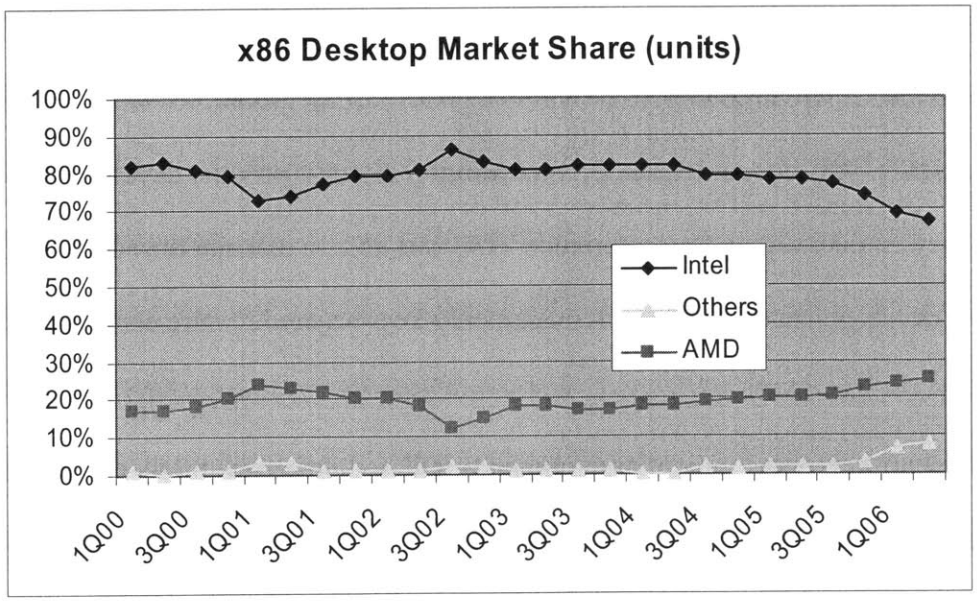

Figure 4 x86 microprocessor market share in Units, 2000-2006[51]

Intel's push for Pentium 4® could not be easily replicated by competitors because the strategy had a firm ground on Intel's famous and well-recognized operational strength that utilized the economies of scale and pre-emptive production capacity. This invincible strategy provided Intel the clear competition advantage for several years but at the same time Intel's obsessive reliance on operational strength provided AMD the disruptive space (Opteron® launch) [52][53].

- Funding for the Pentium M® (Pentium 3® extension)

  As a reaction to Transmeta's low power microprocessor product, Intel extended the aging Pentium 3® design to compete in the mobile market segment where the low power characteristic was important. Pentium 3® was old and defeated by AMD so Intel would have wanted to progress the mainstream product line to young Pentium 4®. However, it was a proven product in the market for a long time and the low power consumption characteristic was re-evaluated after Pentium 4® [54] [55]. The old Pentium 3 micro architecture provided a good starting ground for Israel Design Center (IDC). IDC demanded the first meaningful revenue product development while they could build up the experience. IDC was able to manage the accelerated the product development schedule by focusing only key-targeted feature changes [56] [57].

  The Pentium M® development assignment to IDC was Intel's cautious global product development deployment as well as a part of Intel's investment diversification strategy to support two micro-architectures. This successful strategy became a precursor to Intel's tick-tock product development cadence. Intel's tick-tock product

development cadence means that two main microprocessor product lines are under development at the same time and they use the same manufacturing technology. However, the decision to fund two x86 micro architectures (Pentium M® and Pentium 4®) at the same time created the efficiency issues. The overhead and complexity to several different architectures implied that all other complementary resources (such as chipsets development, marketing, and production) to be overlapped and duplicated investments. This multiple architecture for each market segment was challenged by AMD's new microprocessor, Opteron. AMD's strategy was to plan one modularized lead product and assemble the each part in different configurations to proliferate in other market segment. The market dynamics and tough competition compelled Intel to develop new innovative product development strategy, Tick-tock cadence. Intel The tick-tock product development cadence will be discussed in the separate chapter.

- New architecture, Itanium/IA64: alliance with system vendors

  As discussed earlier, Intel had been trying to edge into high-end server microprocessor business for the new revenue stream and the higher product profit, which only yielded the half success at the workstation and entry-level server market space. Intel's ambitious goal was to take the significant portion of the server market [58]. The brave strategy and the slow progress in the market success drove Intel to consider new computer architecture [59]. Intel established the strategic alliance to synergy Intel's silicon component technology with business partner's software, system expertise, and customer relationship for the success in the long-hoped high-

end server market. Intel also hoped the new architecture could have helped to leap away from the existing competitions with AMD and VIA by introducing new 64 bit computing architecture. It was deemed to be a smart move for Intel to leverage system vendors strength to start a big battle with well-armed (software and system products) heavyweight competitors like IBM, DEC, and Sun [60] [61] [62]. HP and SGI were attracted to a new venture with Intel because they felt the cost pressure to develop the proprietary architecture in-house up and compete with more advanced technology providers like Intel, AMD, and IBM. The advanced microprocessor development required not only the experienced chip design team but also the significant amount of manufacturing commitment. The deal was agreed among Intel, and two system vendors HP, SGI in a form that Intel would deliver the microprocessor solution and two vendors provide the financial and technology development support as well as exclusive use of new micro architecture to their high end server platform [63][64][65]. HP and Intel announced the co-effort to develop new micro architecture in 1994 and started to collect other business support [66]. The alliance introduced new computer architecture named Itanium that started with the big hype that this would change the skyline of the computer industry completely. It was a completely new architecture from the ground up that required 1) microprocessor design change and 2) the whole software stack needed to be redesigned and compiled to get it running on the new system [67][68][69]. This implied that the end customers, such as banks and governments needed to agree to change their complete computing structure. The scope of the project to use new Itanium architecture could have been unexpectedly large so customers' adoption

would be slow because clients feared about the cost, efforts, and risks associated with the new system.

The support of Itanium architecture has yet another implication for Intel that it supports the third micro-architecture development. Although Intel had a huge dream about Itanium as a future dominant platform of 64 bit computing, it had not picked up the presence in a mainstream market and AMD introduced less painful 64 bit computing architecture using x86 binary compatible instruction. The small volume product had good and bad at the same time. The good thing was that Intel did not need a separate manufacturing facility (no additional factory investment) but the bad thing was the revenue never covered a development cost, which was the identical reason why HP and SGI entered in the alliance with Intel. The business structure in the high-end computing market segment has been to charge customers higher premium price for the reliable system and comprehensive service for the flexible computing resource allocation. The system integration, software, and service made a huge value premium but the microprocessor only participated in the value addition as a small component and it was sold in a quantity [70]. This was not a beneficial situation to Intel. However, the system could enjoy the potentially sizeable payback from the new system hardware and the upgrade service revenue to revamp customers' computing infrastructures [71] [72] [73].

- Design center development in foreign country

  Intel was well aware that the establishment of technology development site at inexperienced offshore could be uncertain proposal because it would take very long

patient local expertise development and serious financial commitment. Intel implemented the global product development plan such that it set up the foreign design site while it kept the existing US domestic development sites. The careful approach to the off-shore outsourcing was a wise movement considering Intel's gross profit was still above 50% and human talents were mainly located in one geography, US. However, there would be other reasons for Intel to consider to moderate migration into global product development model.

1) May miss the boat [74]

If all competitors successfully develop the global product development expertise and take advantage of low cost, Intel would suffer eventually from a business model's point of view, which will take a lot of effort and time to revamp when it will be realized. Intel's CEO mentioned publicly in September 2001 that his company had been looking for outsourcing opportunities as ongoing efforts to look for the better expertise and cost structures [75].

2) Local market presence

Although Intel could not enjoy the direct benefit from the off-shore product development project, it would be a good corporate representation to have a local development sites in a sense Intel could combine the site presence with the local marketing effort so it can increase customer's total brand experience [76].

3) Local government contract and society contribution [77][78]

Multinational companies make a significant effort to establish the sustainable local business in the global market circumstance. If the local market were big enough, like

India and China, it would become more important to build up sound relationship with local government and society. One of the best and easiest ways to deploy the strategy is to share the local profit with the local community by making investment and hiring peoples [79] [80]. This can be used to groom the local market and economy as well. Sometimes, this type of investment is required by local government to enter the business.

Intel established the Intel India Development Centre (IIDC) from the early 21st century. Bangalore Design Center (BDC) was started as a part of IIDC as a site to develop the hardware chipset and microprocessor. Intel's management felt the crucial needs to accelerate the site development schedule and thought that they could leverage the experienced Indian community among the US design group to shorten the period for BDC to gain the expertise. Intel provided incentives for volunteered senior engineers, if they would like the relocation to BDC while it provided full collaborative support relationship between US design sites and BDC [81].

- Acquisition of new technologies and investment for manufacturing facilities

  One of the highlight among Intel's early 21st century strategies was very aggressive investment in new manufacturing technology. The several billion-dollar project deployments in the manufacturing might be dangerous especially the economy was going through the down turn [82]. Intel could have been locked-in by the long period investment under the uncertain business environment if there would be better investment opportunities. Intel implemented the investment for several reasons that are very tightly related to other strategies.

1) Market saturation and economies of scale

Intel was expected to have larger silicon production capacity than any of other competitors could have when the new expansion finished. It is well understood that the semiconductor business is all about "economies of scale" because it incurs the huge upfront fixed cost investment to install the top-notch manufacturing facility but the variable cost is significantly smaller than traditional brick and mortar manufacturing industry [83]. Intel exploited the huge capacity advantage as a double-sided sword to put the entrance barrier for competitors by saturating the market only by Intel's capacity and production cost reduction that would be enabled by miniaturized silicon fabrication. Intel's capable manufacturing R&D team has delivered the smallest size transistors and finest manufacturing technology [84]. Intel's financial strength enabled the aggressive investment in the facility expansion [85].

The accelerated manufacturing facilities expansion projects went right thru the dark internet bubble burst period but provided "stellar" pay back to Intel around 2004 and supported Intel to out-achieve over competitions by the cost advantage [86][87][88].

2) Room for silicon capacity demand from newly acquired technologies and prepare for the platform strategy

Intel had aggressively acquired new technologies in communication and optical infra structure business as discussed before. Since mid 1990s, Intel had computer chipset and graphics card offering. Intel developed a plan to push this chipset business further

up so it can dominate all computer components market to help Intel's core microprocessor business by owning all complementary personal computer component market. Intel wanted to be prepared for the potential growth in the invested business by being able to provide sufficient manufacturing capacity. The manufacturing expansion plan was crucial to support the movement to the chipset business and the future developed platform strategy [89] [90] [91].

This chapter discussed business dynamics Intel faced in early 21st century right before the dot-com bubble burst. Intel was one of only a few companies who kept the investment level through 2001 to 2004 period. Intel's investment choices discussed in the chapter was two categories. 1) Aggressive investment in the production technology and capacity, 2) diversified investment in several technology areas (Itanuim development and aggressive acquisition in the network technology) and geographic regions (Bangalore India and Moscow Russia). The first choice eventually returned a significant market success to Intel while the second choice only provided Intel the management nightmare and series of re-adjustment.

The next chapter will contrast Intel's investment choices to competitor AMD's choice, which selected efficient modular building block CPU design.

Chapter 3. Business dynamics changes from 2001 to 2004

Intel's strategic choices around year 2000 helped the firm for the safe pass through the gloomy internet bubble burst period more smoothly than competitors. Intel experienced the brilliant success of the strategy deployed in early 21st century. However, it appeared that the success was only limited within the mobile computing market segment [92]. Intel's mobile computing platform, Pentium M® and Centrino®, was a blockbuster success but the competition introduced new type of competition to the server and desktop market space and customers were attracted to competitor's new product offering, which provided lower power consumption and flexible system configurability [93]. AMD's new product line provided the superb performance/power characteristic for server and desktop systems and the comparable performance/power for the mobile systems to those of Intel's, while Intel only had focused on mobile line and production efficiency [94][95].

I. AMD's success

While Intel was concentrating on increasing the product frequency by leveraging the competitive manufacturing advantage, AMD developed the new microprocessor architecture and the development platform. AMD realized that they could not have as the same level of competitiveness in the manufacturing facilities and technology as Intel has. This meant that AMD could not have the same frequency product for the sustainable future and their cost structure was not suitable for the price war with Intel [96] [97]. AMD developed the product strategy that they would alter the game differently from the innovative design and the product development platform.

- Opteron® microprocessor: the first mainstream CPU product with 32/64 bit computing capability

  AMD developed a new product concept that was a serious departure from their microprocessor history, just catching up Intel's product. AMD's new product was named as Opteron® and it was different in two main perspectives from the previous mainstream x86 based microprocessor products [98].

  1) 32/64 bit hybrid computing architecture [99].

  Before AMD's new Opteron® microprocessor, microprocessors had only one of either 32 bit or 64-bit native computing capability. Intel's 32-bit microprocessors (Pentium® series) were not able to support 64 bit computing. IBM and Sun's high-end 64-bit microprocessors for servers only supported 32 bit computing capability by software's help. The software supported 32 bit computing was so slower compare to the native 64 bit computing that the 32 bit computing performance was only comparable to a decade old 32 bit CPUs like Intel's 486®. AMD's Opteron was the first microprocessor to make both 32 bit and 64 bit computing supported by the hardware and it outperformed any of Intel's higher frequency product [100][101]. Intel had the 64-bit architecture, Itanium. Itanium had the product positioning conflict for the similar 32/64 hybrid product concept and it appeared that Itanium® was losing market's traction to success in the market where Opteron® was successful [102]. It only forced Intel to keep the multiple architectures development support.

2) Modular component product platform

AMD employed the new product development concept, which was modular component design as opposed to Intel's market specific product optimization. AMD's modular design approach required them to develop each optimized modular building block and carefully managed interface so the product team can assemble for the required market segment. For example, the server product would integrate microprocessor core, memory controller, and inter CPU communication port for the larger system configuration while the mobile product would only integrate the core and memory controller for the power consumption optimization [103]. AMD's new development strategy enabled them to integrate all required components into a single monolithic integrated silicon product to accomplish the product optimization for the targeted market segment. This "systems engineering" type of design approach was a new concept in semiconductor development community because it demanded very careful component planning and long debugging before the actual product would be assembled and offered to market. Fast-changing high-technology market environment has allowed the first product launcher with rapid revisions to take and dominate the market by creating the network effect [104] [105]. The first movers also take the higher profit in the fast margin eroding high-tech space [106]. The product's design efficiency such as taking advantage of system platform for the product variation and rapid subsequent product development with smaller resources had not been a key product development planning consideration from the earliest-take-all situation. Intel apparently favored the faster development with huge resources and the product optimization for the targeted market segment. Therefore, Intel had maintained several

dedicated product development lines for server, desktop, mobile, and 64 bit. Each development group focused the product optimization for the earliest possible product launch as opposed to developing the common goal such as AMD's systems engineering approach.

AMD's new product development methodology may not provide the best optimized product for the targeted market but it enabled AMD to develop products for several market from one common platform architecture [107]. It would take long time to develop the modular component design that is suitable for the systems engineering approach but it might provide overall development efficiency with the smaller product organization [108]. AMD developed the Opteron®, server product, as the first sibling among the new product line. Opteron® was 32 bit and 64 bit hybrid computing capable and it was optimized not only for the pure performance but also for the performance per power such that the overall computer system (not only microprocessor) would consume the lower power than the other one with Intel's product. AMD developed integrated inter-processor component and memory controller that could be integrated with the CPU on same silicon to deliver the server level performance and scalability. New components were developed to meet the mobile market segment power budget and they can be disabled when it was not used for the power saving. Therefore AMD was able to operate several smaller product integration teams to serve server, desktop, and mobile segments from the one product platform while Opteron® provided the clear performance advantage, 64 bit computing [109]. AMD's product strategy was to start from the high-end server market to low-end desktop and mobile product using the same basic architecture. The

modular building blocks proved themselves that delivered reasonably optimized performance for each targeted market segment. The overall product strategy resulted in shorter development schedule by smaller group of peoples than Intel. It also accomplished higher computer system performance and attracted big OEM's interests from the super computer to entry level severs [110] [111].

AMD's system engineering approach clearly provided them the product development efficiency. AMD had more focused on desktop processor traditionally and offered inferior mobile CPU to the consumer market before Opteron®; the first system approached monolithic silicon CPU. AMD even did not have a product offered in the server market segment at all [112]. It was mainly due to AMD's corporate size (only $1/10^{th}$ compared to Intel) with very limited development resources [113] [114]. The new systems approach allowed AMD to start to offer very competitive products in the all market segment from low power mobile to very high end multi-cpu server systems with virtually the same engineering team size as the beginning of 21^{st} century (Figure 5) [115].

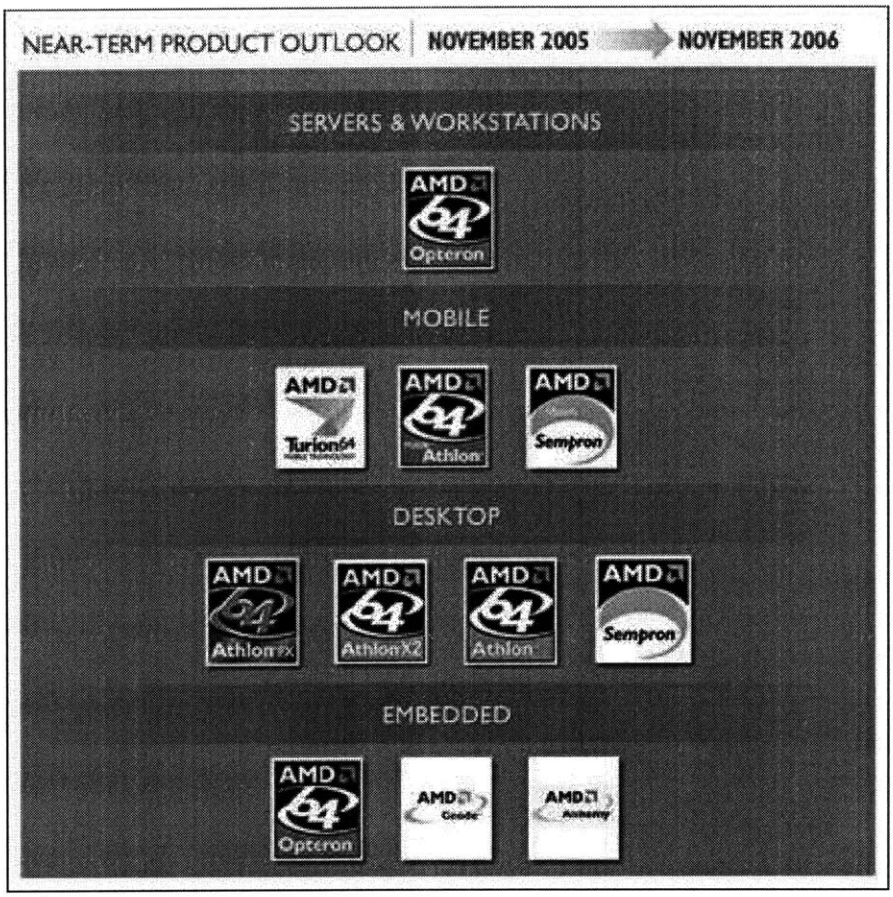

Figure 5 AMD's microprocessor product offering in 2006

3) OEM client's favor shift to AMD product

Nicely defined interfaces and well-optimized components, the key of new platform product strategy, allowed AMD not only development resource flexibility but also the resource budget for the product debug. One major obstacle that big OEM did not adopt AMD's product for the server computer system was simply that there had been no major AMD product use in the server system space. This brought OEMs the question if AMD's product would provide reliable performance, which was critical in the server market [116]. Opteron® provided the better system performance and configuration flexibility at lower total hardware cost relatively to Intel architecture based systems. This triggered early adopters to employ Opteron® as their entry level

server and this proved that Opteron® had the acceptable system level reliability for the server market segment [117][118]. This changed OEM system vendors and their customer's perception about AMD product's characteristic from an uncertain bet to dependable component provider. This was a significant customer shift that allowed AMD to achieve the server product market share from none to beyond 20% within 2 years from the product launch [119]. Figure 6 and Figure 7 show the stellar progress that AMD's Opteron made in the server market share and average selling price.

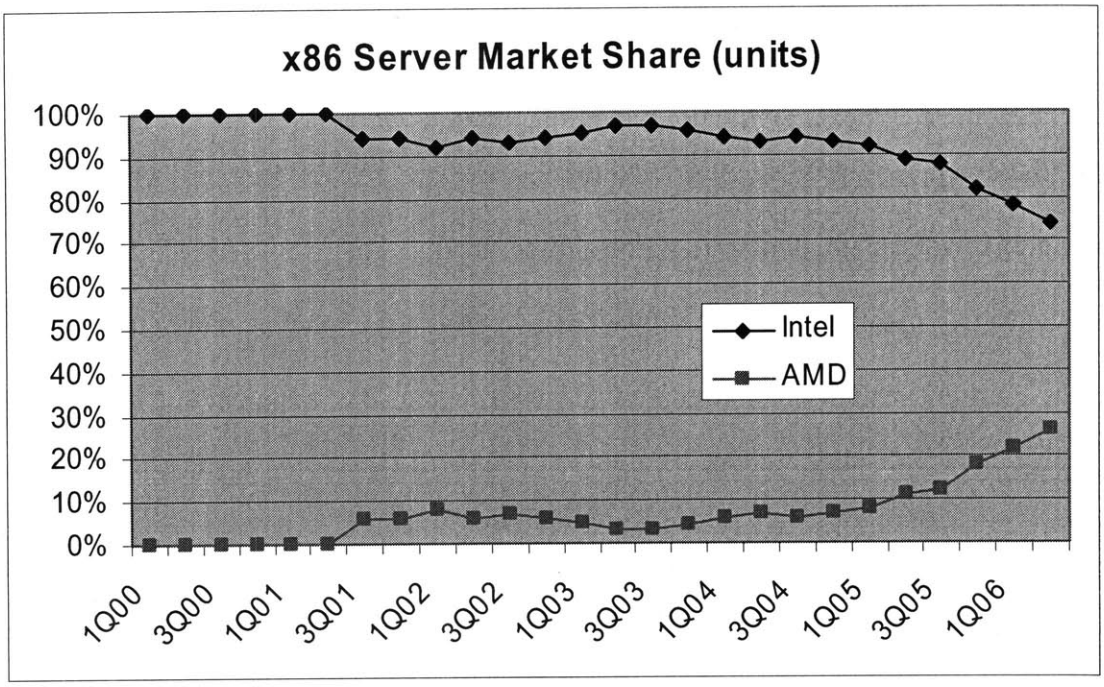

Figure 6 x86 microprocessor server market share [120]

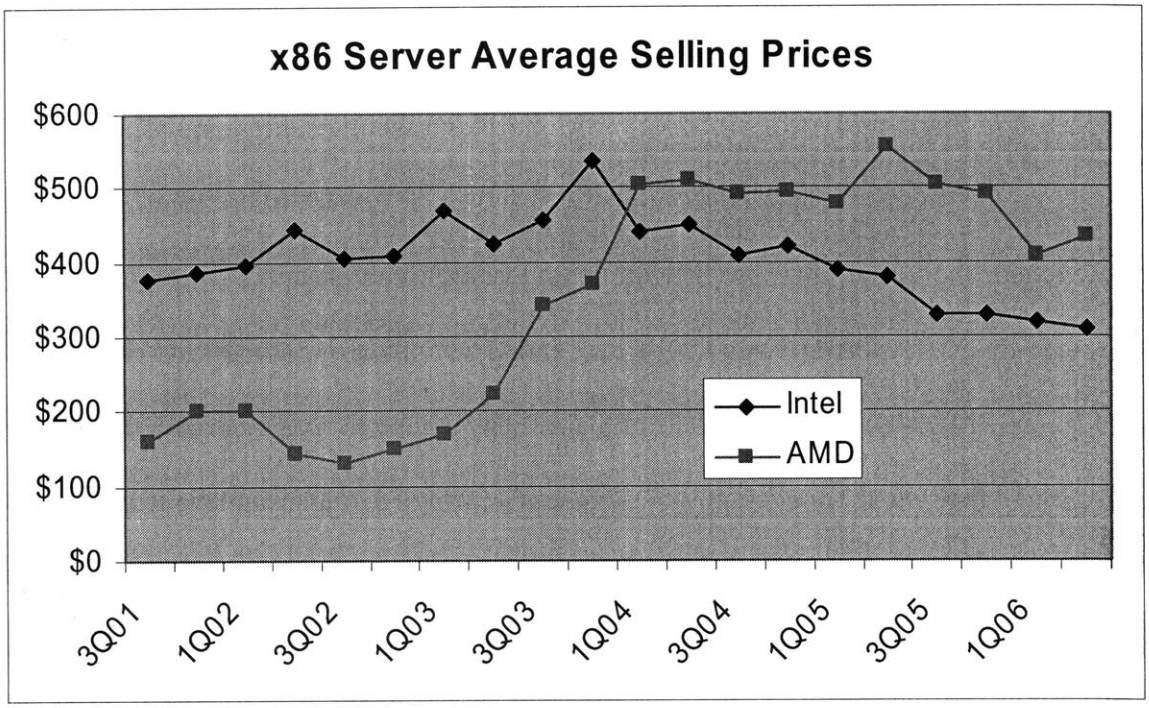

Figure 7 x86 microprocessor Average Selling Price (ASP) in server market [121]

II. Intel's defense

Intel, the incumbent, had to defend its market share and product position from AMD's young brave yet capable Opteron® product line. Intel's choices around year 2000 provided a significant competitive advantage. However, the product strategy relied on manufacturing capability and high frequency appeared as the weakness that needed to be reconsidered.

- Short joyful life

  Intel's aggressive manufacturing facilities investment returned a joyful pay-back helped by the low cost structure of 300mm wafer facility (bigger the size of a wafer, lower the cost of a unit) and the capacity headroom supported enough cushion to the rapid market recover after the internet bubble. Intel's fortunate product investment on Pentium M and the platform strategy of Centrino marketing campaign made a bold impression to market and led a big financial success [122][123]. However, Intel realized, short after, their product started to lose customer's support on their performance leadership from the highest end server products. AMD's attack using Opteron® only accounted the half of blame. The other half was contributed by Intel's mistake that relied on leveraging their manufacturing advantage and frequency increase too much. Intel's product did not deliver the impressive performance advantage over AMD's Opteron® while it consumed more energy [124] [125] [126].

- One, only one, clear advantage

AMD enjoyed their blockbuster Opteron® success but they could have been happier if they can serve all customers demand [127]. AMD was production capacity limited but clients demanded more computing power especially when the economy exited from the long-dark internet bubble and trended toward the recovery. AMD's production simply could not keep up with all excessive customer demand and their inventory had bottomed out for several quarters [128] [129]. Intel clearly benefited from the competitor's undesirable situation because unfulfilled customers orders for AMD Opteron® came back into Intel account. The situation was not desirable to AMD but it was bad for Intel. This production constraint situation drove AMD to prioritize the high-margin server product. It was a harmful situation for Intel because it eroded Intel's high margin product SKUs (Stock Keeping Units) so Intel suffered from lowered ASP (Average Selling Price) and smaller gross margin (Figure 7). However, it was apparent that AMD's situation provided Intel a breathing period to protect market share and prepare for the next counter punch.

- Push for the high frequency fiasco

  Intel dedicated the most experience design team (Oregon Design Center) for the high frequency microprocessor, Pentium 4, and optimized the manufacturing to support this product strategy [130]. The design team developed new circuit structure that was assumed to achieve over 5 GHz and the manufacturing team developed the world fastest silicon transistors to help the design community's effort [131][132]. There is Asian ancient proverb, "Too much is some times not as good as a bit less". This focused strategy ignored two important issues.

1) Will customers only demand the product performance?

The performance of the product is clearly one of most important characteristic that customers always value but customer's product preference changes often times. Not all drivers purchase the Ferrari just because it is the fastest car on the planet. What if the customer values the comfort of the system higher over the performance? Around year 2004, AMD's new product Opteron successfully educated customers that performance per power was more valuable metric for OEM and customer's sustainable business. Opteron® delivered superb power per performance that saves energy, lower the system cost and reduces the data center operation cost [133]. The famous search company that Intel's CEO had a board of director position, Google, showed the clear preference for AMD's Opteron® to Intel's Pentium family just because of the higher system efficiency provided by AMD solution [134].

2) Will manufacturing technology scale to support the high frequency design in the future?

Intel's director Gordon Moore created a famous law, Moore's Law, that predicted silicon technology would double the transistor capacity and the product performance in every 18 months [135]. This famous law had set the industry trend for past several decades since 1960s [136]. Moore made simplifications that there would not be any physical limit to miniaturize the size of transistor. Recent silicon technology challenges the size of one transistor to be only a few hundreds of the silicon atoms in a device. In this type of ultimate physical challenge, many things that used to work

before started not to function as predicted [137]. It became hard to enjoy all three historical advantages of the miniaturization (Higher speed, lower power, and cheaper cost) in the latest manufacturing technology. The transistor used to be assumed as an ideal switching element in the computational logic element that it would not consume any static power when the logic was in the static mode. However, it becomes only the dimmer that consumes not only the dynamic power but the leakage power even when the silicon chip is not doing any useful activity [138]. The combination of the aggressive circuit design and advanced miniaturization technique introduced high power consumption issues for Intel product, which eventually became a main reason for the market turned to the favor in AMD products [139][140][141].

- Multiple product development lines: Not-well harmonized

  It was discussed in the previous chapter that Intel tried to diversify the product development effort so the strategy would seize the growth potential and mitigate the possible fall back from the concentrated investment. Intel maintained three separate full-blown microprocessor projects, only one of which was a materialized success. Pentium M® enhanced from Pentium 3® and designed by Israel Design Center (IDC) made a sizeable win at the market. Pentium 4, targeted for the high frequency, was defeated by AMD Opteron because of its lower performance per power characteristic. Itanium, IA64 designed by Intel and HP alliance, has been all-time hidden rooky that never made meaningful return to Intel nor received any signs as a preferred architecture from the market [142] [143] [144]. Intel had struggled to finance all

three-product development projects and started to feel to look for more efficient product development organization.

- Global product development: efficiency desired

  Intel started Bangalore Design Center (BDC) and made effort to cultivate the local hardware expertise at India by transferring senior engineers and encouraging active collaboration across multiple development sites. BDC shared the responsibility for the key product development with several other sites that were located in all different time zones. For example, key component silicon designs and architecture were delivered and supported from Israel Design Center, Oregon Design Center, Santa Clara Design Center, and Massachusetts Design Center [145]. Intel realized the complexity of the communication between different time zone sites that introduced the time lag for inter-site discussions. The component integration for the product assembly was even harder problem because component designs were developed in different design styles, tools, and methodologies. It was a huge challenge for BDC to deliver the product commitment on-schedule [146].

- Tangled product roadmap

  Because of multi-site collaboration and multi architecture support, Intel's product development organization started to be fragmented over time. The product road map tied with the development plan became extremely hard to manage and follow-up. The support of the fragmented project structure incurred significant infra structure overhead for example different design tools, libraries, and system maintenances. The

effort to make sure the enough resource for the project was available became one of big management problem. The complicated product roadmap contributed to make the problem worse and the project management problems were fed back to make the complex product roadmap congested. Series of not-healthy feedback chains between product roadmap and project management ended up playing a significant role to inefficient product development process and delaying the project delivery at a higher cost level [147][148][149][150]. Figure 8 shows Intel's product roadmap presented in Intel Developer's Forum 2004. It shows that Intel kept the plan to support all three Pentium M®, Pentium 4®, and Itanium® architecture developments.

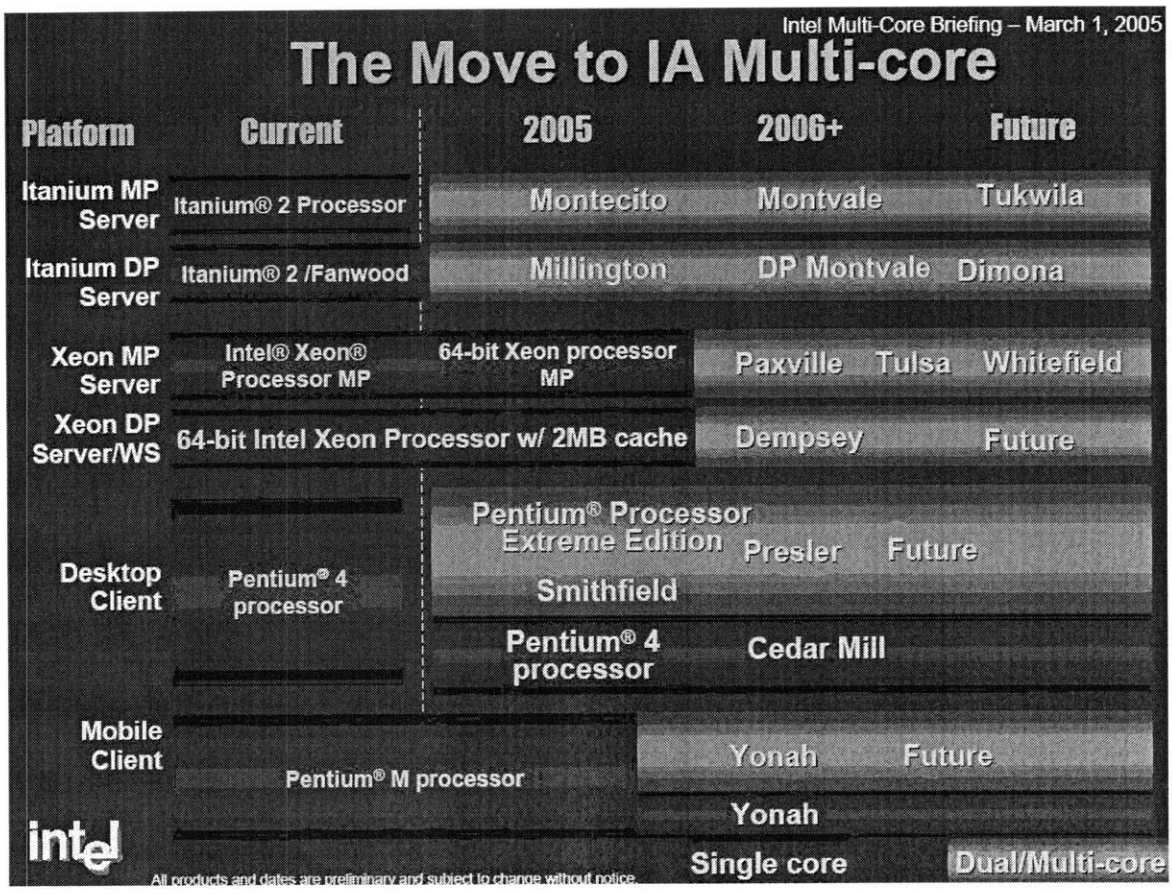

Figure 8 Intel Microprocessor product roadmap in 2004 [151]

The chapter reviewed the success of AMD's new product strategy employed systems modular component approach to deliver the better performance, performance/power and comparable number of product variants that Intel had with the only $1/10^{th}$ corporate size. Even though Intel enjoyed joyful success from the aggressive capacity expansion to pre-empt the market in the mobile computing space in 2004, it only worked as a defensive tools to plug unfilled demand by AMD in the high end server market in 2006.

Intel only had bitter failure experiences from the geographical and technological diversification so it had to cancel many projects and re-draw the product roadmap introduced by in-efficient organization structure[1].

Next chapter will discuss Intel's mistake acknowledgement and effort for the quick turn around the situation implemented by several efficiency projects, "Converged..." initiative, and Tick-tock cadence.

[1] "We canceled more than 50% of our project past 4 years," Intel's senior executive said in the conference

Chapter 4. Acknowledge miss steps and rapid product strategy change: Hatching the Tick-tock Cadence

Intel was still a smart incumbent. They quickly identified issues like what mistakes needed to be addressed, when to prepare the win-back plans, and how to deploy new strategies. It did not take long time for Intel to realize their poorer than expected market performance. The management team started to worry customer's new shift to AMD's product, performed the analyses why it happened, and established the plan to correct the situation. Intel's wake up to the situation was agile, candid, and earnest to make the effort to communicate to market and employees. Intel announced four main product development initiatives by acknowledging the miss-steps and affirming audience with the solid recovery solutions [152].

I. Right hand turn – product feature change [153]

Intel maintained 32 bit only computing high frequency strategy for x86 product line, which provided the disruptive window for AMD. AMD's Opteron® micro processor did not achieve as high frequency as Intel's Pentium 4 but demonstrated clear application performance advantage with better architectural features like 64 it computing, easier system upgrade path, and low power consumption [154][155]. Intel eventually introduced the first 64 bit computing capable Pentium 4 microprocessor code named Prescott in 2004 after a lot of struggle to reduced the product power consumption [156]. Prescott® delivered the highest operating frequency ever (3.8GHz) but failed to impress the market due to the delayed launch and poor performance/power [157]. The customer's preference shift back from AMD to Intel did not happen as Intel management hoped. Intel admitted

that the product push for the ultimate performance was not in-line with customer's preference and claim the product roadmap adjustment called "Right Hand Turn" [158][159]. Right Hand Turn (RHT)'s basic idea was to shift Intel's product line from frequency optimized Pentium 4® to power per performance optimized future product line which would be suitable for the wide range of platform strategy implementation [160][161]. The several product line cancellations followed their tails for a while from new desktop product line to high end server Xeon line and the series of restructuring efforts (project cancellations) were spread from US, Russia, to India geographically [162][163][164]. It was a major restructuring initiative that shatters close to 50% of Intel's all projects. The main goal of the activities were 1) simplify the number of product line support, 2) enhance the project management efficiency, 3) reduced the communication steps for the fast decision making, 4) provide the firm foundation for long term product development model.

II. Converged modular building block strategy: systems approach [165]

Before the RHT, Intel had maintained two separate product lines as basic building blocks for their main x86 IA (Intel Architecture) product line. The one was the mobile market application optimized microprocessor named Pentium M® and the other was the desktop and server market optimized microprocessor named Pentium 4®. Pentium M® started from old Pentium 3® micro architecture and Pentium 4® was a new scratch design started from late 1990s. Ironically, market had shifted to the direction of Pentium M®'s reasonable performance with supreme low power consumption characteristics while

Pentium 4® products suffered from the fierce competitions from AMD's new Opteron® [166].

Intel had a big dilemma that Pentium M® did not support 64 bit computing that the high-end market almost mandated while Pentium 4® did not have the right power characteristics [167]. Intel eventually started to develop the new common micro architecture that was suitable for both mobile and high-end computing market [168].Intel's responses had been, so far, to provide the board level systems engineering solutions that, however, required OEM's to integrate more parts to the system for the less efficient system and lower performance than AMD's offering. Intel felt the single silicon systems engineering solution to win the competition thus it initiated the "Converged ..." activities in a product development spaces that could be leveraged to several market optimized products by utilizing modular component building blocks. The idea behind the initiatives was to develop the single silicon product employing flexible key components for the market specific application spaces [169]. It was quite a contrast to the Intel's traditional product development strategy, which was that the one project was in charge of the component development and product optimization with the massive help from resources provided by other geographical sites [170][171]. Intel hoped that the new product development strategy would eventually expedite the project schedule and reduce the project overhead by encouraging the leverage and reuse components [172]. Intel understood that new strategy would require a lot of preparation works to define the components interface and develop the specifications [173]. Here are three main areas that Intel drove the "Converged ..." initiatives.

- Converged Core

It was obvious that Intel needed to change the product strategy from the frequency and production efficiency to enhanced feature and total system cost [174]. However, Intel's product development strategy did not support the agile systems engineering approach because Intel provided the market optimized solution. The strategy has not been flexible to provide features that market demanded such as 64 bit computing with low power consumption in a single product platform. Intel's product development structure was rather suitable to support the individual project group to design the isolated product than encourage the several project teams to work toward a common goal with the corporate level coherent product line strategy. However, the market started to prefer the balanced product characteristic and variations of products even within the one market segment when clients accrued the product experience and developed their use models. Intel's traditional product development strategy could not be able to response to the matured market's demand. The fast project ramp up and the earlier product delivery was a proven high tech industry product development strategy because it allowed the company to take the technology lead position resulted in the higher financial product profit from the first mover advantage [175]. Intel's recent learning from the market responded to AMD's Opteron® taught that the technology trend might have moved into more efficient design and flexible feature set enabled by set of reasonably optimized modular component collaterals [176][177]. It was very clear that the clients preferred AMD Opteron® to Intel's Pentium based products (Figure 7).

Intel decided to employ the power efficient Pentium M® as a foundation of the new microprocessor product strategy of "Converged Core" to serve from the mobile to server market [178]. Intel's idea was to break "Core (traditional microprocessor CPU)" from the actual product. They would like to develop a modular "Core" that could be used in multiple different products depending how the other components were configured with [179].

It was a new concept for Intel to separate the microprocessor core and the product development. The new "Converged Core" needed to be as cleanly and clearly defined as possible to support different customer segments by one component architecture. Intel started with the baby step to establish the concept of the "Converged Core" [180]. For example, Intel implemented the first native dual core product (project code: Yonah, product name: Core®) using the mobile and power optimized Pentium M® family [181] [182] [183]. The 64 bit computing and other high-end features like the virtualization were implemented into the first "Converged Core" product named Core2® (project code: Merome) [184][185]. Core 2® family (Merome/Conroe/Woodcrest) proliferated to high-end workstation market as well small size server systems market which used to employee Pentium 4® based server products [186][187]. Merome was the first implementation of Intel's "Converged Core". It produced a successful outcome in the market space due to its enhanced performance, superb power characteristics, and product configuration flexibility [188][189]. It is well recognized by the market that the second version of "Converged Core" (code name: Nehalem) will implement enhanced server features such as Hyper Threading®, integrated memory controller and QuickPath® technologies

[190][191][192][193]. Hyper Threading® technology allows the single microprocessor to run two separate software applications at the same time independently with no or negligible performance degradation and QuickPath® technology enables the glue-less inter-processor communication [194][195].

- Converged Uncore

The "Converged Core" strategy was to cover x86 product space so the one core component could be used for the different market segments. Intel has yet another architecture that is called as Itanium or IA64 family, which started with large OEM vendors like HP and SGI as an effort to take over the mainframe level system market. The consortium was named as Itanium alliance and invested by several system vendors and Intel to develop the business and establish the eco system [196]. Intel started the second "Converged ..." product development initiative that abridged x86 and IA64 product lines. Due to the difference in the high-level architecture, IA64 and x86 could not share the same microprocessor core component, otherwise it would introduce the significant performance degradation. Intel realized that the high-end x86 Xeon MP® and IA64 product lines had a common product characteristic. The both products supported very large system configuration and massive inter-microprocessor communication to deliver the hefty parallel computing capability using many microprocessors in a system. Server application generally requires the massive number of microprocessors (core) to be integrated in a single silicon wafer and each core to be connected by very capable and efficient interconnect (Uncore). Intel established two architectural layers of Uncore hierarchy. The first layer was

defined at a single microprocessor product or Central Processing Unit (CPU, traditionally it consisted of one core) socket. Uncore was the structure that could assemble multiple processor cores with integrated memory controller, and inter-socket communicator (chapter 6). Intel made good efforts to develop the common "Converged Uncore" that could be shared by two high-end microprocessor families of Xeon and IA64 Itanium product lines by defining the common Core to Uncore interface (IDI, Inter Die Interface). The converged Uncore is defined to work with any core structure that has the common IDI interface. The goal of the "Converged Uncore" was to become a structure to serve from the mobile to high-end products, which was named "Extensible Modular Converged Uncore". Intel's management team started to encourage product development team to use IDI from ultra low power core (LPIA, low power Intel architecture), Pentium M based new converged Core, and new IA64 Itanium microprocessors. The "Converged Uncore" structure was the product hardware platform. There was another effort to define the architectural interconnect layer for the system level integration, named QuickPath® [197]. The actual product implementation for the server market was required to include the QuickPath® support to be integrated to the system [198][199]. This QuickPath® architecture was developed to support from handheld mobile product all the way to the big datacenter computing environment.

- Converged Design Methodology and Tool

Two above "Converged ..." initiatives covered actual hardware space so the design team could expedite the components assembly processes with the minimum product

customization effort to optimize for the market segment . The components for the Core and Uncore should be augmented by the common design methodologies and tools in order to maximize the efficiency of the "Converged ..." strategy otherwise the product design team would spend sizable effort to integrate and verify the components designed by different tools and styles. Intel carefully identified the design tool suite based on the best project practices among design groups and made the conscious decisions between the tool efficiency and cost effectiveness. The new in-house tool developments were approved only if the investment could be justified. Otherwise, many commercially available vendor tools were selected and shared in the corporate software license pool. Intel managed to accelerate the "Converged Methodology and Tool" initiative deployment by the help of these careful selection processes. Several microprocessor development projects were expected to take advantage of the "Converged Methods and Tools strategy" to expedite the product integration.

III. Focused site development (SET) – near term product management strategy [200]

It was discussed in the previous section that Intel had maintained several product development sites and the project structure was located over several geographical regions and different time zones. It became a significant project overhead to keep the same project organization in multiple locations and time zones especially when the project required very intact communications such as defining a new structure, integrating components, or time critical component debug [201]. Intel tried to accomplish the significant project methodology milestones in global product development area by

delivering a key product by globally organized design teams in US, Israel, India [202]. Three US sites were involved to support cache, microprocessor core, system interface architecture, tool/methodology, analog circuit and Israel team supported design tool and verification, and India design center was in charge of the product integration and delivery. Intel had suffered from component integration issues mainly caused by communication difficulty over multiple time zones and geographical domains [203]. In addition, Intel had felt the need for high-level general management structure re-alignment. Intel maintained the unique management structure called "Two in a box" [204]. This represented two individuals in the same level management position to compliment each other's background weakness and achieve the better management efficiency from the collaboration [205]. While this management structure had many good promises and reasons to be justified, it actually slowed down the decision making process because sometimes the ownership of the issue to the resolution might not necessarily clear. Intel's Structural Efficiency Team (SET) initiative proposed to change the project management structure to correct the communication efficiency problem and hope to expedite the product development cycle. 1) Only one or two physical design site would be involved for the one product development project and both sites, if would be two sites for one project, should be in the same time zone to maximize the communication productivity. 2) Would recommend and suggest the single management structure wherever possible and the project ownership site should assume the full authority for the decision-making regarding to the project management. This SET initiative implemented to re-align the project management structure. Intel prepared another grand project management roadmap to provide the deep breath for the corporate to enhance the long-

term sustainable product development plan, Tick-tock product development cadence [206].

IV. Aggressive deployment of tick-tock cadence – long term product development strategy [207]

Intel wanted the sustainable long term the product development platform that could leverage Intel's well-acknowledged strong assets, such as manufacturing capability, x86 and IA 64 architecture, globally located design sites, in conjunction with more efficiently organized product development strategy.

Tick-tock product development cadence is to fund two main product development projects using the same manufacturing technology in order to provide the major product platform refresh per every 4 years, the major product update per every 2 years, and new product release per every year. Tock is a major product and platform feature update and tick is a performance enhancement of the product or platform. Tick-tock cycle of the product development is two years so Intel can release the major product refresh every two years and the product enhancement release in between of two major new product launches. The platform Tick-tock is managed in the same way but the cycle of the major refresh is every 4 year frequency [208]. Figure 9 and Figure 10 show the product development cycles align with the manufacturing development refresh and the platform by the implementation of the tick-tock cadence. Intel expects the Tick-tock product cadence strategy will bring benefits to following items.

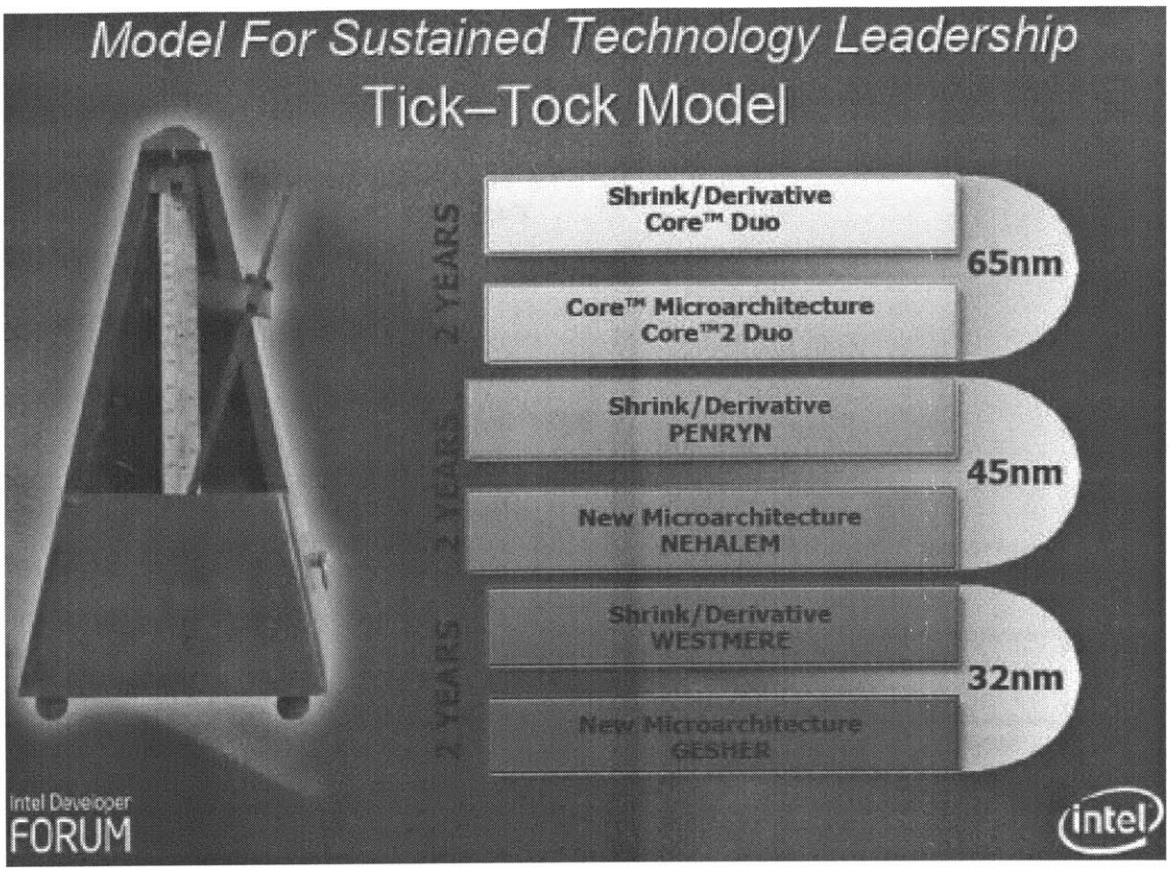

Figure 9 Intel's Tick-tock refresh cycles [209]

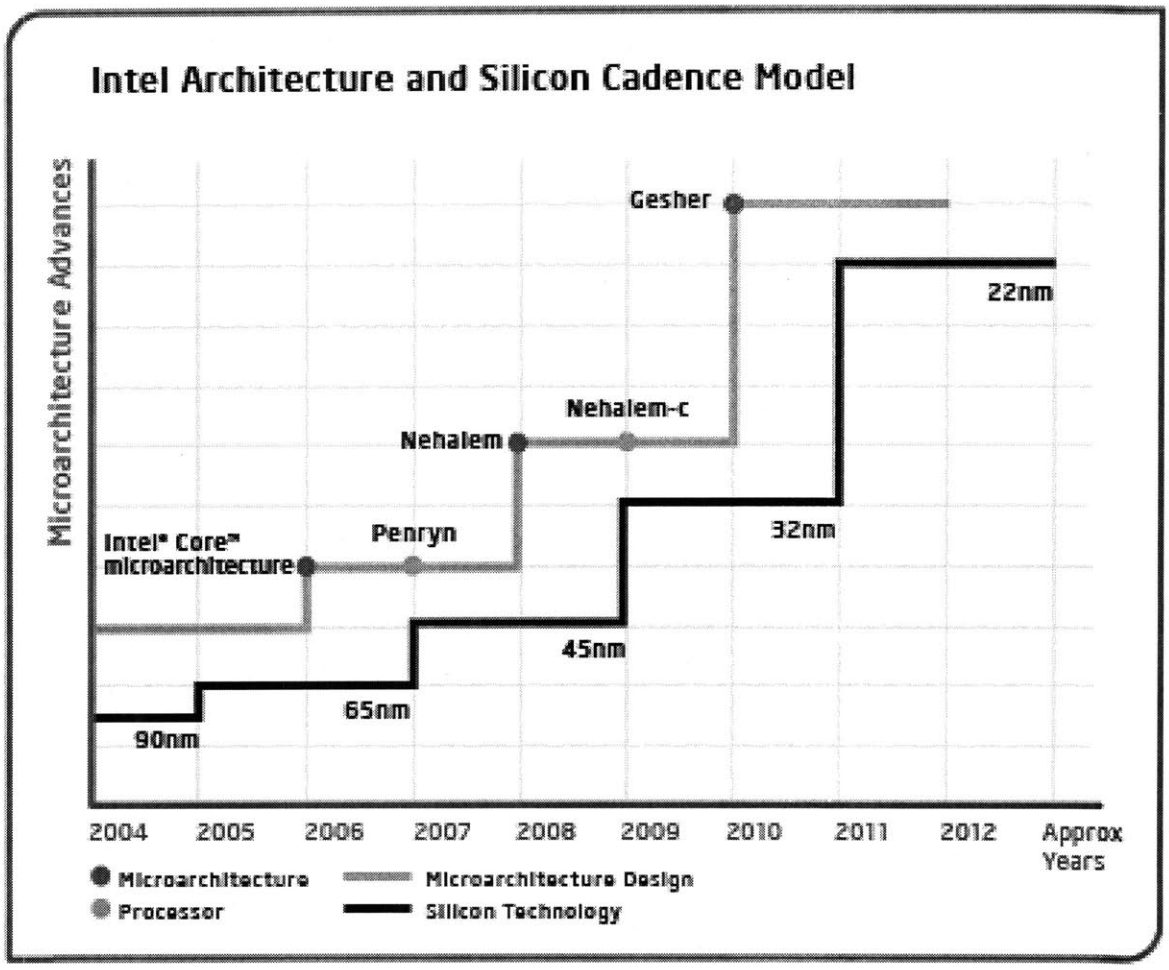

Figure 10 Intel's Product and manufacturing development alignment[210]

- Provide customers and investors long term product roadmap

Tick-tock allows the organized product development roadmap that appears to be feasible, sustainable, and credible to customers. In addition, they can align their product development plan with Intel's microprocessor roadmap. This long-term product development roadmap could not be easily duplicated by competitors because it leverages Intel's manufacturing and design strength heavily so investors could be assured for the Intel's long-range product outlook.

- Efficient Platform strategy management

Tick-tock product development platform not only takes care of the microprocessor product but also requires very careful project management from manufacturing technology to systems level platform development. The microprocessor product development plays a role as the bridge to harmonize all three main project managements. In other words, the microprocessor development schedule needs to align with manufacturing technology development and OEM vendors needs to understand Intel's progress to align their systems development. It should be noted that all efforts to shore up the tick-tock cadence progress are great tools to communicate with customers, investors, and Intel employees to highlight the significance of tasks and assure all processes are on-track by providing the reasonable transparency of the product roadmap.

- Product development risk mitigation

Tick-tock cadence is carefully designed product development plan in such a way that tasks with expected major obstacles don't overlap on to the single product development cycle. For example, new miniaturization manufacturing technology migration is not supposed to overlap with the tock project, which is a major design refresh cycle (Figure 10). There are always two tick and tock projects under the development using the same manufacturing technology. In the example of 45 nm technology, the tick project (Penryn, minor design update and product enhancement) is supposed to trail blaze the new manufacturing technology. Penryn will be manufactured and productized one year before the tock project (Nehalem) will get on

the market shelf. The manufacturing miniaturization develops and migrates to the new technology in every two-year cycle, which is one-year compliment to the major product design update. By managing the manufacturing technology and design feature upgrade in this way, Intel always finds out what to focus more in a given period and how to balance the risk profile to allocate resources. Figure 11 and Figure 12 show that the richer product portfolio than shown in Figure 8 was accomplished from variations of "Converged Core", which proves the successful strategy implementation result of Tick-tock cadence.

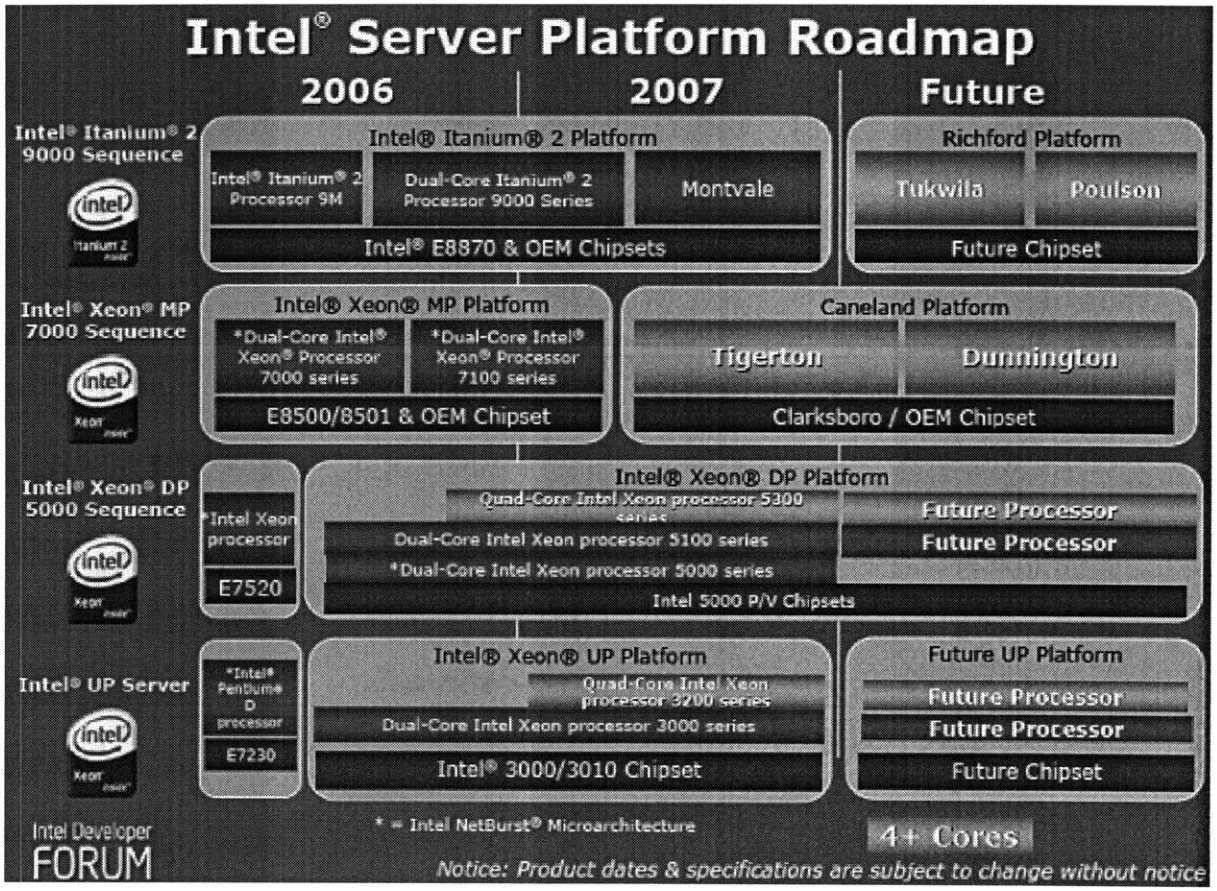

Figure 11 Intel Server Platform Roadmap [211]

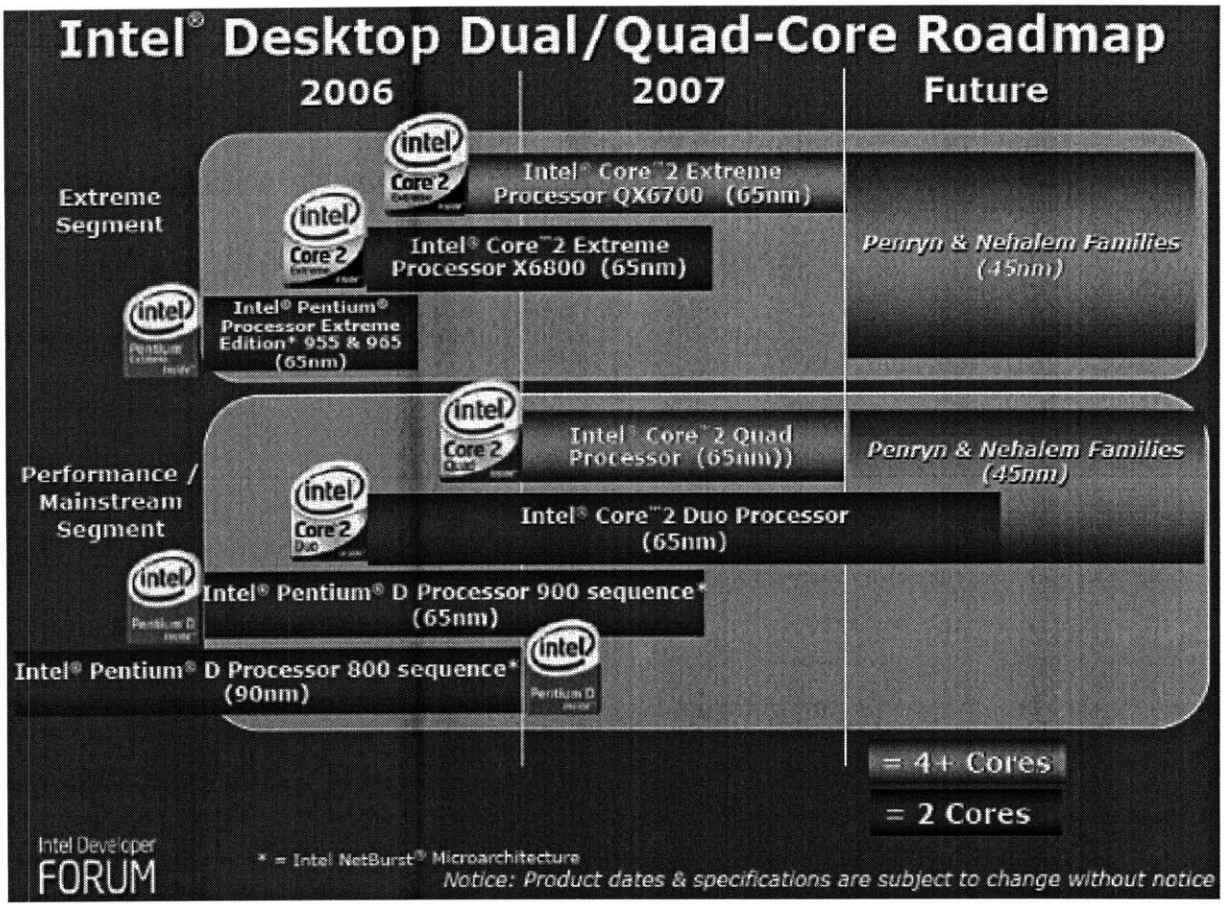

Figure 12 Intel Desktop Dual/Quad-Core Roadmap [212]

This chapter discussed steps Intel took to adjust the problems in the product development and organization structures. Intel's candid acknowledge of the mistakes and prompt reaction to fix them was brilliantly successful. Intel's CEO announced RHT (right hand turn) publicly and initialized several follow-on actions. Managerial and financial task force team was formed and delivered quick guidelines to reform the giant company and its product development strategy. There were three main themes. 1) Converged design block and methodology, 2) Focused site development, 3) the grand Tick-tock cadence. Next chapter will provide the case how the first two Tick-Tock products (Merome, MRN and Penryn, PRN) were planed and managed.

Chapter 5. Tick-Tock cadence: Review on Merome(MRM) and Penryn(PRN)

We have discussed the background how Intel landed to the Tick-tock product development strategy and the idea on what Tick-tock cadence is. This chapter discusses how the first version of "Converged Core" Tock (Merome, MRM) and Tick (Penryn, PRN) projects were managed. The case presented here is collected from interviews with two projects senior members.

I. The first ever "Converged Core", Merome (MRM)

- Back to focused site development from multi-sites collaboration

  Intel became well aware of the multi-sites project overhead, especially for the major feature update that would require close relationships and communications between disciplines, in a setting global product development environment. Therefore, it was a consensus that the focused site development for the first "Converged Core" was the best option and key factor for the program success. Pentium M® was chosen as a base architecture for the new milestone and Israel Design Center (IDC) was selected as a home site to leverage their experience with Pentium M® product development. The project implementation plan was solely owned by IDC. IDC team was authorized for the product feature selection as well as for the design tools and methodologies choices. This full authorization allowed IDC to manage them to be a fully self-contained development site for the product planning, design, methodology, and tools. The successful facilitation of the full ownership avoided any potential project overhead caused by corporate wide communication. It expedited the program

progress and permitted IDC to allocate all resources for the product enhancement and schedule reduction.

- Careful product planning and organized exercises for Tock

  Intel made sizeable amount of effort to plan the first "Converged Core" to revert the recent market perception upset by AMD's Opteron®. Intel managed to exercise the first native dual core product from Pentium M® processor using the same manufacturing technology as the "Converged Core" product. Intel's first native dual core product (Code name: Yonah, product name: Core®) was launched six moths ahead of the actual market launch of Merome, product named Core 2® [213]. Intel's Core® product short lived until the Core 2® product launch. It was a carefully pre-planned activity to mitigate any potential miss-steps for the major product development, which still needed to add serious feature updates such as dual cores and 64 bit computing.

- Conscious architecture trade-off

  Merome was the first implementation of Intel's "Converged Core" strategy. It was also the first product that was implemented by Tick-Tock cadence. The original micro architecture was started off the mobile product, Pentium M® that did not have enough architectural features like 64 bit computing, high bandwidth support, server level reliability, multithreading capability, and so on. Merome project team made very careful feature selections so they could manage to implement to the product. Merome team did not feel disgraceful to push any non-critical feature additions to

Tock product's future enhancement list. The team chose to implement only the critical functions to the first "Converged Core" that could provide server level computing capability, reliability, and basic infra structure support for the upscale market segment such as package level quad core integration and large size cache memory. Other architectural enhancements such as high bandwidth support and multithreading capability were moved to the future Tock update list. The following Tick project would only enhance the product performance and power optimization while qualifying the new manufacturing technology. Merome project team and Intel's careful selection on the feature list enabled the successful on-time delivery of the first "Converged Core" product and the proliferation into several different market segments (Figure 11 and Figure 12).

II. Transition to Tick program (PRN)

Intel prepared for the Tick of the "Converged Core" implementation by planning the product definition upfront and identifying the candidate development sites. It was believed that the Tick project did not require as much of communication as the Tock project. The product design could be broken into several-isolated building block, which drove Intel to select two design sites for the follow-on Tick project, code named Penryn. There was another constraint that IDC could not participate to the Penryn program. They would still work on the Merome project while Penryn project needed to ramp-up. Because of these considerations, Intel moved the program ownership to two US design sites that were located in the same west coast time zone. The one was Santa Clara Design Center (SCDC) and the other was Folsom Design

Center (FDC) that are located both in California USA. Two sites were located in the same time zone and there were many other ways to connect two sites intact via road and air. Two sites were separated by less than two hours driving distance and air shuttle was provided for any inter-site trips.

SCDC and FDC deployed key contributors to IDC for a several quarter period so the new program could start smoothly from a design perspective as well as tools perspective. As discussed, the Tick project implemented the minimal architectural changes while it focused on the performance enhancement and power optimization using the same set of design tools. Therefore, project learning and knowledge transfer by helping the Tock project delivery were considered as key activities for the Tick project success.

This was a new multi-site collaboration trial, which Intel did not experiment before. Intel's traditional multi-site project structure was to make the one program progress through geographically dispersed development sites by encouraging their parallel collaboration. Tick-tock (Merome and Penryn) cadence by definition enabled the geographically concentrated and chronically separated multi site collaboration. The new type of multi-site collaboration made major product upgrade and performance enhancement to be performed by geographically different sites by encouraging their serial collaboration while it kept the focused development site strategy. The tock program focused on feature update to win the competitions and to enable the follow on tick program. The tick program focused on the performance enhancement for higher profit margin and product manufacturability for lower cost and the tick path

cleared for the any manufacturing issues for the next major Tock product update, Nehalem.

This chapter provided the short case on how two projects were managed. These two projects were the first implementation of tick-tock cadence and delivered by the focused site development strategy, which requires either collocated design team or the same time zone. The next chapter will discuss how the tick-tock can be improved to suitable in the global product development situation. DSM was used to analyze the product structure and proposals in following chapters will be based on the next chapters' observation.

Chapter 6 Microprocessor Design at Intel: A study product development

Chapter 5 discussed how the first "Converged Core" projects were managed in a new Tick-tock development strategy setting. This chapter will discuss the architectural definition of the Converged Core and Uncore. The architecture will be analyzed by DSM and the discussion will lead into potential future project structure recommendation. The following chapters 7 to 9 will propose the project management structure introducing the systems department as either a guidance or project lead organization.

Data for the architecture and process analysis was gathered by interview with Intel's product groups' architects, first/second level managers, and product development leaders across three projects and collected over 50 feedbacks.

I. Intel's design center operation

Intel is involved in the design, fabrication and sale of microprocessors, amongst various other products. The design activities for microprocessors are currently done out of five facilities based in USA and Israel. These facilities are located at Hillsboro (OR), Santa Clara (CA), Fort Collins (CO), Hudson (MA) and Haifa, Israel (IDC). Recently Bangalore design center and Moscow design center established. Much as the design capabilities across the centers have been generalized (or made such that they can collaborate and transfer jobs between centers), there is a certain amount of expertise which exists in each centre with respect to the development of the architecture of the microprocessor, e.g. OR specializes in the Pentium series (Pentium 4 was design managed from there), MA and CO specialize in high end microprocessors which are solely used for industrial applications, and IDC specializes

in the microprocessors used in mobile technology. CA specializes in the desktop and server product. Penang in Malaysia specializes in the efforts producing the value desktop processor.

II. Microprocessor Contents by Converged strategy

Figure 13 shows the conceptual diagram of the Intel's Core 2 Duo® product that employed Converged Core/Uncore architecture. The Uncore architecture was designed to afford more than two microprocessor cores to enable multi-core products for the high-end server market. Multiple cores communicate each other thru Uncore via pre-defined inter Core architecture (IDI) and their communications to main memory (DRAM), storage (hard disks derives), or other CPU sockets will be served by Uncore via QuickPath.

The core is the heart of the microprocessor unit and is involved in retrieving information about the job to be executed, consolidating the information, executing the job on hand (integer execution and floating point execution) and maintaining the cache (feed instructions and hold data till the job is executed and the results transferred). The uncore, on the other hand, provides all the support that the core needs to execute the job. The uncore consists of the memory controller, provides coherency (both on socket and system interface off-socket), includes the inter-socket router for information flow between the different core (in case of multicore) and with the environment outside the microprocessor, the input/output pad and other miscellaneous units like power maintenance, testing, debugging, etc.

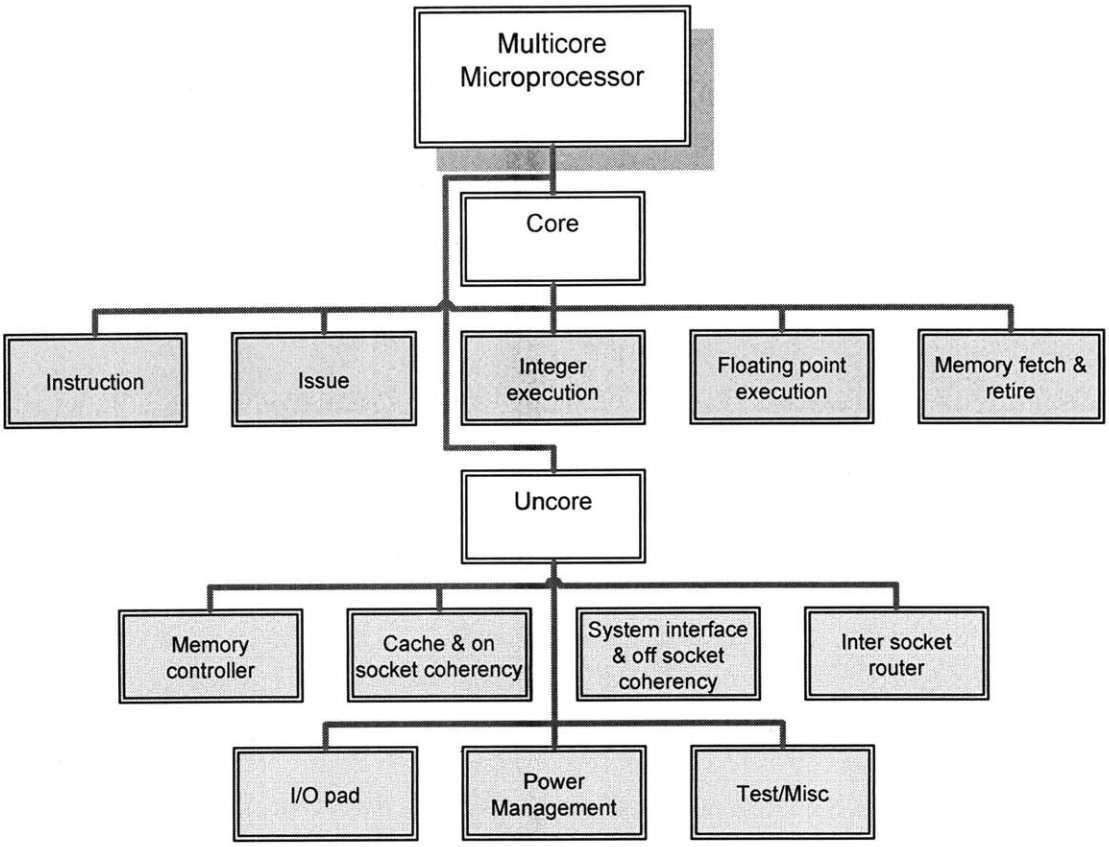

Figure 13 Structural decomposition diagram of modern multicore microprocessor

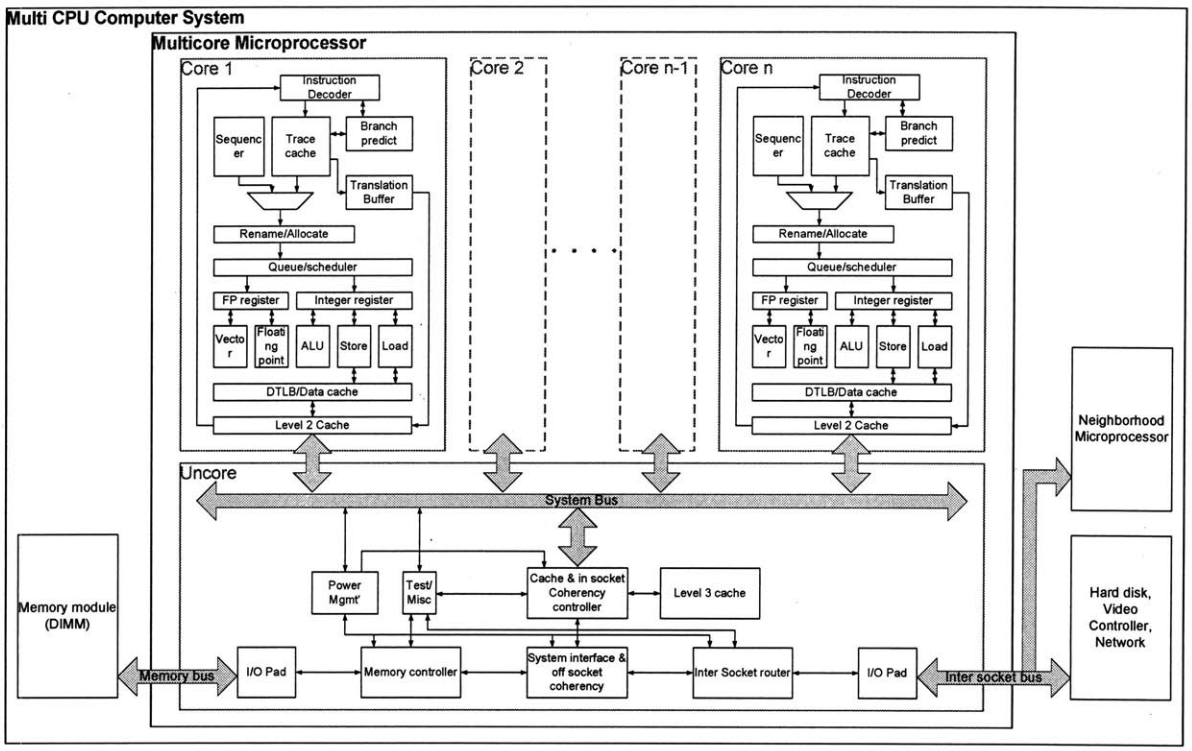

Figure 14 Typical structural and functional decomposition diagram of multi cpu computer system uses multicore microprocessor

III. Microprocessor Design

Microprocessor design primarily progresses along the following processes – architecture definition -> floorplan -> behavioral code -> circuit design -> functional structure layout -> functional structure integration -> unit integration -> cluster integration (core, uncore) -> full chip integration. Figure 15 shows the master DSM format and initial result that analyzes the current microprocessor development. The small fraction of full expanded DSM is shown in Figure 16 to present how the each units flow/architectural dependencies are analyzed.

Each unit of the core (instruction unit, issue unit, integer execution unit, floating point execution unit and store and load unit) and the uncore (cache coherency and uncore architecture unit, system coherency, inter-processor router unit, memory controller

unit, IO pad unit and the other blocks like testing, power management, etc.) goes through the above processes during development. Besides the core and uncore parts of the microprocessor, system integration efforts covering global architecture definition and leading to final functional structure integration, and chip integration were identified.

Figure 15 Intel Multi-core microprocessor DSM - fully expanded

	Core		1	1a	1b	1c	1d	1e	1f	1g	2	2a	2b	2c	2d	2e	2f	2g
1	Instruction unit	1																
1a	architecture definition	1a			B		C					C						
1b	floorplan	1b		A			C			A			C					
1c	behavioral code	1c		B	C		B			C								
1d	circuit design	1d		B	B	B		C	C	C								
1e	functional structure layout	1e			B	C	B		C	B								
1f	functional structure integration	1f			B		B	B		B								
1g	unit integration	1g			B		C	B	B									B
2	Issue unit	2																
2a	architecture definition	2a		C									B		C			
2b	floorplan	2b			C							A			C			A
2c	behavioral code	2c										B	C		B			C
2d	circuit design	2d										B	B	B		C	C	C
2e	functional structure layout	2e											B	C	B		C	B
2f	functional structure integration	2f											B		B	B		B
2g	unit integration	2g								B			B		C	B	B	

Figure 16 Detailed DSM entries for sub category of each function units (shows only the fraction of the whole structure)

IV. DSM Development

During the development of the DSM, the need to try and identify the strength of the relationships was felt. Thus ratings of A, B or C were assigned based on whether it was felt that the impact of an action on the other action could lead to revision of (A) 50-100% effort, (B) 20-50% effort or (C) <20% effort (see Figure 16 for the example). In addition, it was recognized that a pure architecture-based or pure process-based DSM would not suffice to explain the intricacies of the relationships present during microprocessor development. Hence, an architecture-based DSM was first developed and then the key processes in the development of each of the units were added. The relationships between various unit/processes were then identified and quantified. All identified interactions between units and tasks were aggregated at the group level. Figure 17 presents the quantified interaction by the values and Figure 18 shows the higher level extraction of quantified interactions. The each column entry values greater than 2 in Figure 17 became 'X' in Figure 18, which means the significant

interaction with other activity because groups have one strong dependency ("A") or more than one medium dependencies ("B").

			1	2	3	4	5	6	7	8	9	10	11	12	13
	Global architecture (Floorplan, Clock...)	1	19	8	8	8	8	8	8	8	8	8	6	5	3
CORE	Instruction unit	2	11	58	5	3	3	2	0	0	0	0	0	4	5
CORE	Issue unit	3	11	6	58	6	6	3	0	0	0	0	0	4	5
CORE	Integer execution unit	4	11	3	6	58	0	6	0	0	0	0	0	4	5
CORE	Floating point execution unit	5	11	2	5	0	58	6	0	0	0	0	0	4	5
CORE	Store & Load unit	6	11	2	2	6	6	58	6	0	0	0	0	4	5
UNCORE	Cache coherency and uncore architecture unit	7	11	0	0	0	0	6	58	4	0	0	0	4	5
UNCORE	System coherency	8	11	0	0	0	0	0	7	58	4	4	0	4	5
UNCORE	Interprocessor router	9	11	0	0	0	0	0	0	4	58	4	2	4	5
UNCORE	Memory controller	10	11	0	0	0	0	0	0	4	4	58	4	4	5
UNCORE	IO pad	11	11	0	0	0	0	0	0	0	4	4	58	4	5
UNCORE	Misc blocks (Test, Power management)	12	11	5	5	5	5	5	5	5	5	4	6	53	5
	Chip Integration	13	9	14	14	14	14	14	14	14	14	14	14	14	15

Figure 17 Summarized DSM of microprocessor development. Numbers represent the level of interactions among architectural units and efforts.

			1	2	3	4	5	6	7	8	9	10	11	12	13
	Global architecture (Floorplan, Clock...)	1		x	x	x	x	x	x	x	x	x	x	x	x
CORE	Instruction unit	2	x		x	x	x							x	x
CORE	Issue unit	3	x	x		x	x	x						x	x
CORE	Integer execution unit	4	x	x	x			x						x	x
CORE	Floating point execution unit	5	x		x			x						x	x
CORE	Store & Load unit	6	x			x	x		x					x	x
UNCORE	Cache coherency and uncore architecture unit	7	x					x		x				x	x
UNCORE	System coherency	8	x						x		x	x		x	x
UNCORE	Interprocessor router	9	x							x		x		x	x
UNCORE	Memory controller	10	x							x	x		x	x	x
UNCORE	IO pad	11	x								x	x		x	x
UNCORE	Misc blocks (Test, Power management)	12	x	x	x	x	x	x	x	x	x	x	x		x
	Chip Integration	13	x	x	x	x	x	x	x	x	x	x	x	x	

Figure 18 Intel Multi-core microprocessor DSM – extracted

V. DSM Analysis for the efficient Global Product Development

On analyzing the DSM, it is apparent that relationship between various processes across units has maximum strength B. Relationships of strength A primarily exist within the unit during development or affect the chip integration efforts. This could be assumed to have been because of Intel having developed microprocessors over a

number of years and the learning leading to controls that ensure control over revision of efforts. This reflects a typical architecture-based DSM wherein the various sub-systems are self contained but have strong relationships with the system integration units. In this DSM, the relationships across units are of type B and C only. In addition, most of these interactions happen upfront (during architecture definition or floorplan) or during unit integration. It is an important observation that that once the architecture and floorplan are well defined and accepted by the units, their respective designs can be done independently and with interaction required only at the final unit integration level. This also draws a potentially interesting conclusion that a unit's team that is responsible for activities from unit floorplan through unit integration (basically unit design) may be co-located (necessary as interactions of the type A exist e.g. weighted interaction value is '58' in Figure 17) but each unit design group is not necessarily required to be co-located with the other unit design group or project team during these activities. They may be needed to come back to the system integration team during the unit integration part of the process as co-location may be necessary then.

Figure 18 shows the clustered interaction within separate Core and Uncore design. The interaction between Core and Uncore happens between the store and load unit of core and the cache coherency and uncore architecture unit of uncore. There are interactions between other units of core and the miscellaneous blocks of uncore (power management, testing, etc.) but interactions are rather weaker compared to within Core or Uncore respectively. Thus, it may not be necessary for co-location of unit teams that belong across core and uncore systems. The analysis suggests another level of team groupings at Core and Uncore level.

Most of the interactions/dependencies of strength "A" that occur across units happen during architecture definition and floorplan phases when these actions at each of the units have strong impact on major bus definition. The only other cross-unit interactions/dependencies of strength A occur, again during architecture definition and floorplan phases, with actions of cache coherency and uncore architecture unit have strong impact on the similar phases of system coherency.

The DSM analysis seems to suggest two basic principles of team groupings for Intel's global product development and one idea of the system department which would be responsible for cross-unit interactions/dependencies during architecture and floorplan definition phases.

VI. Project organization suggestion

The presence of interdependencies and their relative strengths seem to suggest

- The formation of teams along units is natural
- Systems department: There is a lot of information sharing in the initial phases (architecture definition and floorplan) and this may call for the extremely effective communication. Intel's traditional approach is the focused-site development of the co-location of various teams (chapter 4 and 5). The strength of Intel's product development seems to stem from the efforts that go into these phases (they take about 50% of the typical total product development time) – the interactions across units and the arrival of a consensus architecture and floorplan leads to firm control of development in further phases. It was discussed that the co-location of each design group (may eventually be

dispersed in worldwide) is hard and expensive proposition. Note that, this phase requires the efficient communication not the co-location. This issue can be resolved by the systems engineering approach and the introduction of small group of advanced people.

- Subsequently, the unit teams may be co-located together but not necessarily with other unit teams. They can proceed on their respective developments with a communication link to the systems department (proposed in the previous bullet), which is responsible for central global architecture and chip integration teams. Thus, these teams can be located in any of the design facilities – based on economies and availability; it may be beneficial to transfer responsibilities by unit design to a particular design facility, e.g. Instruction unit team members may be from design site "A", the issue unit team members may be from design site "B", etc.
- For unit integration, it may be necessary for the unit teams to be represented with the chip integration group to ensure design completeness before the design is passed on for manufacturing feasibility, etc.

VII. Design Process/Structure Suggestion

Focused site development structure and each design sites desires prefer the each site to have full design capability. This could be very expensive to achieve and likely to introduce the redundant organizational overheads such as separate management structure to maintain each design functions in every sites. This strategy probably will hurt the long term low cost design capability by attempting design locations in more

experienced country where the cost is higher and long term engineering talent may deteriorate.

Here is the list of suggestion for Intel's global product development strategy.

- Keep site expertise: Intel's sites have built up site expertise so the expert site can serve other sites for special needs. For example a microprocessor for mobile technology is under development, whilst the specialized design team may take the lead for the same, they may enable other facilities to deliver a different product by delivering maybe the same component or consulting for the more efficient design.
- Maintain the resource flexibility: Though the various design facilities of Intel have specialized in the architecture development of various types of microprocessors, there are abundant engineering resources that can perform a general engineering task within the Converged Methodology context. As a result, during any project, it should be possible for the project leaders to draw resources from any of the design facilities. Intel regards such flexible resource availability as a strength contributing to its success in product development. During the development of a microprocessor, teams prefer being formed along units, and then there are the global architecture and chip integration teams. However, within the units, it is not necessary that the teams are constant in the organizational structure throughout the development. The team may be composed of members who may work during architecture definition, floorplan and behavioral code phases and then a different set of members may be brought in to work on circuit design, functional structure layout, functional

structure integration and unit integration. Though at many times the members get collocated with the project leaders, it may be possible for them to also work at home locations. Thus, Intel uses the flexibility available through the design facilities to develop products.

- Rotate site responsibility: It was commonly expressed among site managers that they want to groom the sites full capability to be able to responsible the whole product development cycle from the definition to product integration/qualification. They believed it would provide clear benefit to Intel as well as the site. 1) Intel can employ the focused site development strategy by allocating a complicated product development to the full capable site, if the site is available and the project requires a tight risk/schedule management. 2) Intel's multi site global product development strategy would get even higher development mobility because the Converged methodology trained people can be allocated to any progressing projects as needed basis. 3) The development site can participate to the bid for the important project participation and the increased visibility, which is important for the development site's future prosperity.

  It would be one of reasonable suggestion for Intel to operate the role/responsibility rotation program. For example, "A" site is responsible for Tick product in the technology generation and it will lead the collaboration to develop the future project definition with planning/marketing team. That will help each site to enhances the existing strength and improve weakness by delivering challenging tasks/products. If there is any need for critical

experienced resource, the flexible shared resource pool can help the responsible site (may be less experienced than other site temporarily).

Figure 19 shows the proposed Intel global product development structure from the DSM analysis. As discussed in this chapter, DSM analysis identified the project process structure that consists of three phases.

1) Global architecture definition: This step requires efficient communication among participant. Intel's conventional way to solve the problem is to co-locate design groups in one site or the same time zone; focused-site development. The thesis discusses the systems department's role to facilitate discussions with peer groups and other disciplines as a guidance or project owner in the later chapter.
2) Unit structure development/design: The second stage of the project is to develop the actual design. This stage can be divided into several small group structures. At the high level, there are two large groups of Core and Uncore. Each unit belongs to Core/Uncore as a sub group. It would be the best scenario, if the whole group could be co-located into a single site for the project progress. However, complex project management can sometimes prefer each unit to be remotely located in the different sites and time zone (or GPD). The DSM analysis provides the useful information that the effective GPD project structure even in top notch high technology microprocessor development.

3) Product integration: The final stage of the product development is the integration process. DSM analysis suggests that this effort may be required to be collocated because of the tight communication loop between tasks.

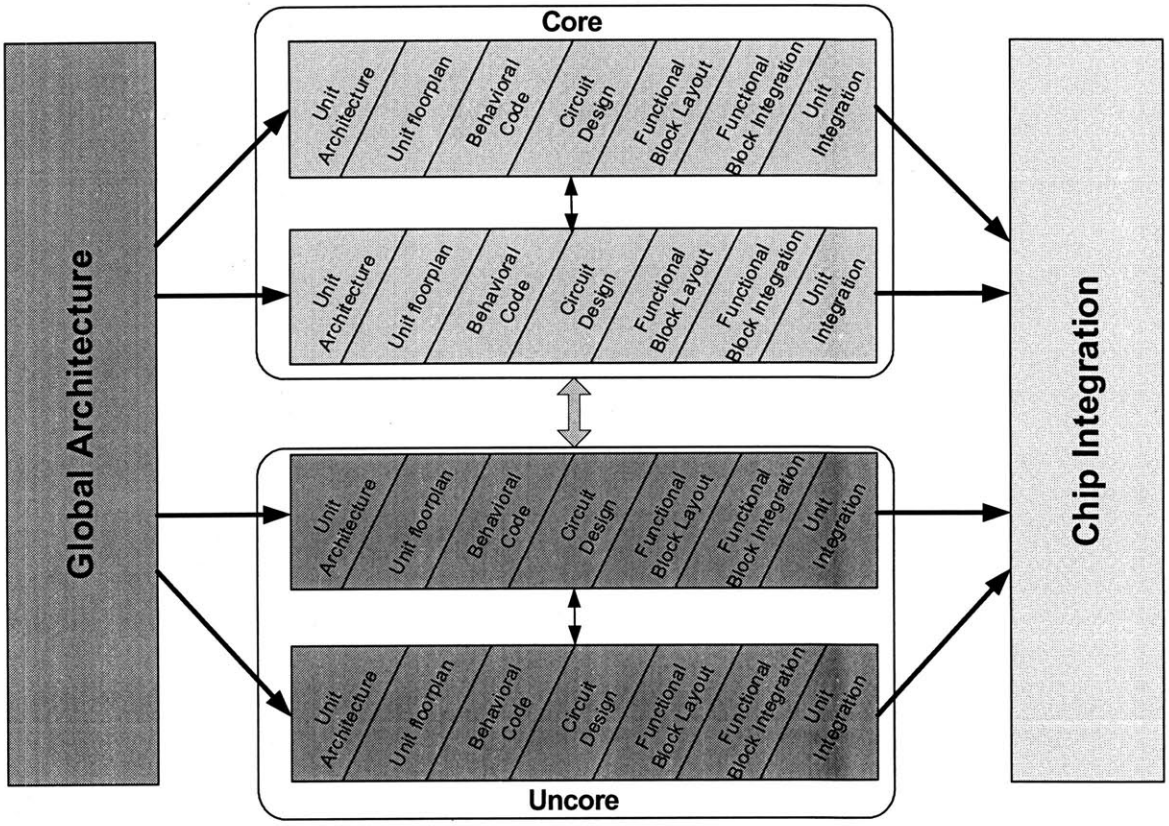

Figure 19 Proposed Product development structure

Intel has managed itself to get half way to the propose structure from the help of Converged initiatives (Core/Uncore/Methodology). It has experiment successfully in the focused site development setting and wants to expand the strategy suitable to global product development. The list below narrates the obvious obstacles to overcome to accomplish the desire.

- Clear interface definition

- Provide inter site communication path
- Tap to the future feature change
- Form the organization around the platform

The later part of the thesis proposes the systems department's contribution for the effective means to rise over the issues so it can accomplish the product development structure organized by architecture like

Figure 19 as opposed to the current geographic or skill based organization.

Chapter 7. Wishes of Tick-Tock to the next level

It was apparent that the Tick-Tock model has worked greatly for Intel to recover from the bitter shortfall to the returning stellar winning the competition by affirming the strong product roadmap and supporting seamless product launch streams [214][215]. "Our 'tick/tock' model of product and silicon technology development has emerged as a core asset of the company. It sets the pace not just for us, but has become the beat rate for the industry; ... It is this predictable, relentless cadence that has returned us to leadership...", said Intel's CEO Paul Otellini in his 2007-year end closing remark. While it seemed invincible strategy from competitor's view, there have been constructive complaints from Intel's internal product development community for the product development model enhancement. Figure 20 shows Intel's product development structure in 2006 and 2007 circa, which is built around tick-tock model. The drawing shows only the simplified interaction between design and silicon fabrication engineering team. The actual project structure is more complicated interface structures. For example, the design-engineering group has interface with product marketing and platform group. The fabrication community has connections with supply chain and facility construction group.

As shown in the Figure 20, Intel's tick-tock model requires extensive multi-disciplinary and long term planning. The long range planning could be somewhat cumbersome for the development teams who value rapid project ramp up and on-schedule product delivery. It was deemed very wasteful effort for project team to incorporate other project teams concerns and future project's potential need.

The focused site development strategy was hoped to be improve for product groups to allocate resources and construct the efficient multi-site collaboration. Most of all, the

product development groups would like the efficiency of the focused site strategy and the flexibility of the multi-site collaboration model.

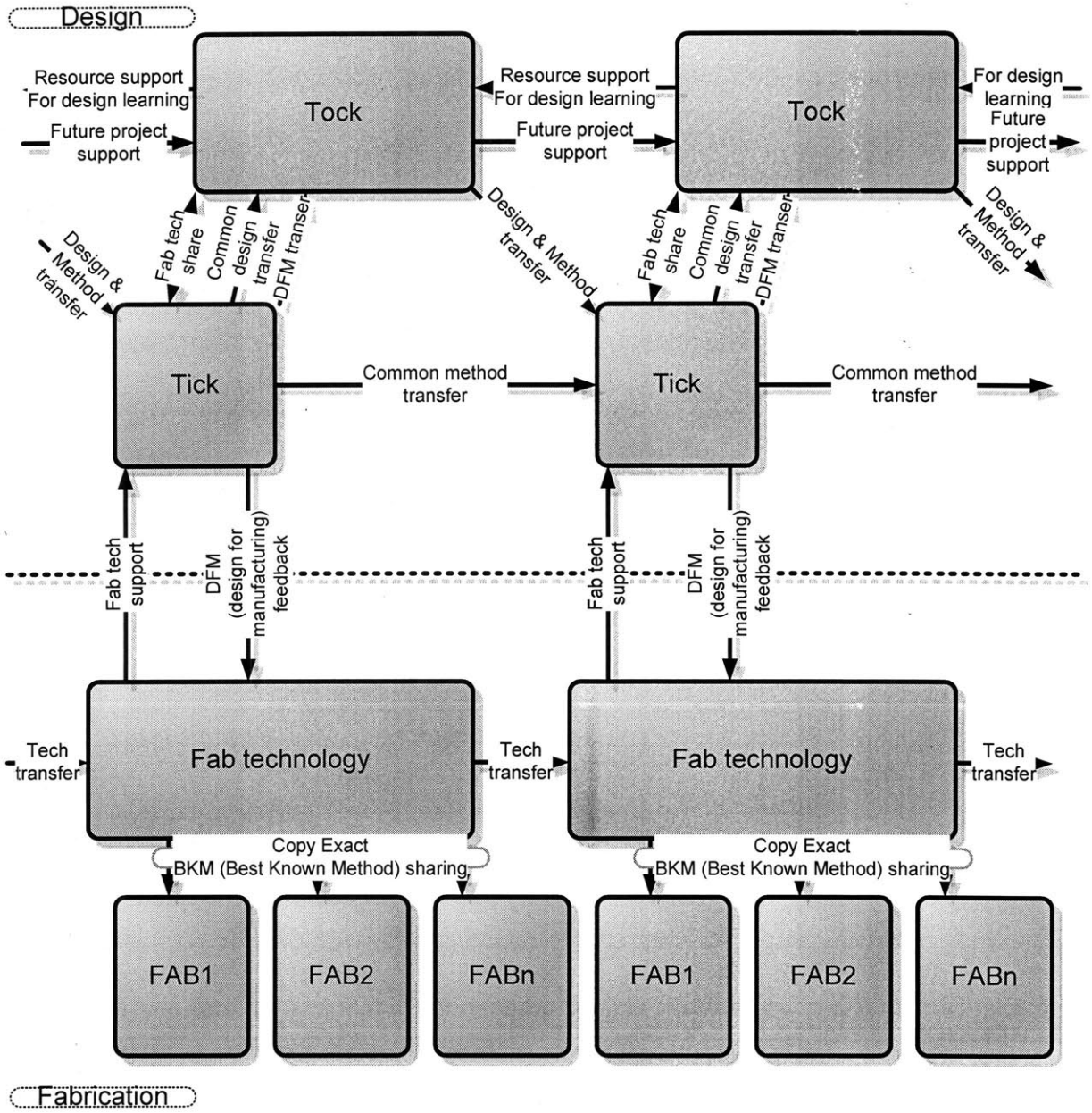

Figure 20 Intel's multi-project collaboration diagram in 2006 and 200

Here are issues and desires gathered from interviews.

I. Desire to the project management flexibility

It is ironically interesting that Intel's senior management team started to get requests to change back from focused site development to globally distributed development structure (GPD). One of Intel's senior product development manager said, "I am kind of disappointed for the focused site product development because it does not allow the dynamic resource allocation and it increases the overhead. Why don't we ask peoples to work on the stuff if they are already good as opposed to either develop the expertise in the focused site or shuffle peoples between sites? There must be ways to organize ourselves to perform the better in the current structure than to promise achieving by inventing us. Do we have to locate us in the same building or same time zone?"
Intel's managements was seeking for the to maximize the inter-site collaboration regardless teams are collocated in the same building or time zone by flexibly allocating tasks and resources to the right project at the right moment.
The management communities' sentiments are from

1) Reverse cost effective

   The focused-site development is expensive high-cost structure because it locks Intel to keep the development sites only in the developed country where the expertise is concentrated but the cost is multiple times higher than developing countries. The focused site strategy drives the company even further to locate the same geographic regions for example only in the west-coast of US where people's design experience and mainstream fabrication facilities are located. This may potentially put a stop for the corporate to find the best talent at the right time and the right cost.

2) Does not leverage the current corporate structure

Intel has already made several large investments to cultivate worldwide product development sites. It operates the product development sites in Malaysia Penang, India Bangalore and announced aggressive movement into fast developing countries like China to find new market as well as people's talent[2]. Intel's management would like to be efficient with the least pain and best cost structure. The leveraging the current corporate structure is considered as the best option even though Intel moved away from it to the focused site strategy a couple of years ago to accomplish the short-term goal[3]. "Catch up the competition by the focus" was Intel's comeback strategy when it was behind the competition. Intel's middle level project manager expressed a similar desire in the interview. "The recent tick was multi-site project mainly due to there was no one site with enough people to execute all project. This was not because the project was too big, but this is because at that time the other big sites were busy with other projects. We would like the focused site development but we are resource limited at the same time."

3) May lose long term competitiveness

It is a human nature to seek for the lower cost structure and look for the systematic organizational efficiency improvement to win the competitions. Winners in the most of business and sport games are determined by who plays the best and fastest in the same rule and game setting as opposed to who does things differently or invents new rules. The business trend is on the shift to the Global Product Development (GPD). The victory will be claimed by who will do it most efficiently. It will be only the matter of time. The current perceived shortfall of GPD is at

[2] See chapter 3 and chapter 6 for details and references
[3] See the chapter 5 for tick-tock case study

finding the efficient organization as opposed to finding the local low cost engineering talent. The efficient GPD structure requires long-term commitment and patient organization structure development and experiences build-up [216][217]. Intel selected the focused-site development strategy and hoped to extend it as a long-term solution. However, it started to realize that the industry move to GPD and be aware of the needs for the GPD like long-term solution while it still fears about the efficiency and agility to react to the fast market shift in the high-tech sector. Intel's management started to be in the search for the efficient GPD structure.

4) Could be focused site strategy sustainable?

Intel's managements slowly begin to realize the question that "how long the focus-sited development strategy would last? Would it be even sustainable in the global competition? Can we properly respond the disruptive technology from low cost country?" As discussed, it becomes clear that Intel needs an efficient way to manage the product development regardless of the site locations and project collaboration structures.

II. Fear of the collaboration and work credit

Intel product development's efficiency relies greatly on the component reuse from the previous project and share among projects. One of senior executive mentioned in his speech, "We have 23 products worked off the same open standard specification yet all 23 products engineered and implemented differently by separate engineering groups. We should not be doing it any more." The push for the collaboration and component reuse introduced several problems for the development community.

1) Many stake holders

The push for the collaboration and platform strategy required many different development communities to participate in the decision-making process. This contributed to the blames of slow decision-making and bureaucratic organizational politics. This was one of main driver for the focused site development strategy because it reduced number of interfaces with other departments and communication delays to develop the common goal. The situation may become worse in the new hoped flexible project structure since it will append more overhead of multi-site as well as multi time zone communication.

2) Prepare for the future when the current has issues?

The schedule and time-to-market for the project group is most precious value to keep, especially in the fast changing high-tech industry. The project ownership site is probably more than willing to defer the consideration about the future project support or the extensibility much beyond the near-term competition. Here is the comment from Intel's middle level manager. "I do not think there was anything up front. There was ramp and knowledge transfer when the project started." It should be noted that Intel suffered big market share lost from the competition with AMD Opteron® product when the product development community only focused near-term competition and was in the complete lack of future product feature preparation. Intel's senior management should pay more effort to develop the product group performance metrics balancing the near-term on-time project delivery and long-term sustainable product innovation.

3) Less clear and more fuzzy deliverables definition

"The component share is a management thing. It helps us nothing and only gives us the burden to support others. They will either throw the work away and laughing on us "stupid" or take the credit of delivering the product while we get only the salary," said a senior engineer. Intel highly encourages sharing the same/similar component among different projects. It happens occasionally that one team delivers a sharable but not the identical component for multiple projects while they belong to the one specific project. The management's dream is to have one team to serve several projects, if the component requirements are similar enough from different projects. However, the actual amount of work the project group feels is more than the single project support. The individual component team often makes the engineering trade-off to commit the quality for the main project but not for the other projects, they support. This may create the situation that the "served" projects make the almost the same effort to develop the component from the scratch but they start it much later than they could have started because they waited other team's component service. On the other hand, the "service" team needs to spend large enough effort for the seamless product integration of other project group, which the "service" team may be concerned for not taking enough work credit from the upper level management. This situation may result in project group's grief of not trusting in the collaboration and each individual worker's frustrations of being over-used. "It required my extreme care to manage loaned worker from other project," said one first level manager, "loaned workers don't exactly work for me or my project. Their primary concern is how to benefit their site project." This is a classic example of

'not my project (NMP) syndrome', which can be observed in many collaboration places.

"We can cut many ways to benefit for all of us from the collaboration. It is the matter of how clearly the deliverable is defined and collaboration is arranged. I have occasionally realized some conflicts of priorities among projects and individual workers. Most of times, the frustration could be avoided if the management team had done due diligence to define tasks and deliverables as clearly as possible," said one of the collaboration technical lead, "we have not particularly done good jobs on the planning the collaboration, which Intel needs to spend more effort. It was true that there were difficult situations required some special mediator department. We had suffered many project delays resulted in over resource allocations in the later stage of pretty much all projects."

It becomes more and more obvious that Intel needs to develop a systems department type of organization that overlooks all involved project groups as it wants to become more flexible product development structure leveraging GPD. It is also recommended for Intel to develop the sound reward system for the corporate wide efficiency contributors.

III. Project steps alignment

"We taped-out[4] the chip two months ahead of the original schedule but the package team was not ready so we could not run the single test for those two months. My team just concentrated in pulling the schedule in but did not pay attention to communicate our

[4] Tape-out: design database hand over from the chip design stage to silicon fabrication to prepare photo mask sets for the production

progress with other group for them to accept our service inquiry. This was the major drawback of the multi-disciplinary collaboration," regretted a mainstream product development manager, "I will do the best for the future project to avoid the same mistake."

As the interview points out, higher the collaboration complexity increases and the efficiency expectation goes up, harder the multi-disciplinary schedule and work arrangement becomes. Figure 20 only shows the arrangement requirement between design and fabrication technology to accomplish tick-tock cadence. The product development has interfaces beyond the engineering and technology. It interacts with internal/external disciplines such as marketing, customer relationship, supply chain, business partner, and OEMs. Intel wants to grow to the new market area because its traditional business is slowing the growth and shows the sign of saturation. Therefore, it wants to transit itself from the big single major product monopoly provider to the conglomerate silicon solution provider to keep the growth momentum [218][219]. Tick-tock cadence is suitable to manage a big volume and high profit product, which takes care of Intel's traditional product to be stronger by the tremendous attention and extensive investment. However, Intel hopes for the new growth engine (maybe lower profit product with many sku), which requires more than just tick-tock cadence and demands the systems approach built around GPD and tick-tock.

IV. Needs to the common measure the project progress

Intel's two senior executives said, "We run the 40 billion company on the spreadsheet. We got to have a better way to manage it", "we don't have a common metric to estimate the engineering task and measure the progress."

"We ask for the resources when we fall behind the schedule. Did not plan all details before the project start," said the project manage in the interview.

Intel's product development community employs mainly the senior engineer's experience to estimate the project schedule and resources. The estimated schedule data is rarely adjusted by peer project groups cross checks or by parametric method because of the fast growing product complexity, the product unique feature sets, and extreme schedule pressure. There is a competition among Intel product development sites to own/lead the next generation product development, which will return the larger credit, reward, and chances to be promoted. This incentive system tends to drive the product development communities to promise the light project structure (small number of peoples within the short time) at the start but to ask for the more people to accomplish the goal with the multiple times bigger project structure at the end. The most common excuse for the later project size increase is un-identified development risk because the project is always new and unexpected product feature change because the customer and market always changes. In other words, the past experience is not necessarily a good indication for the future project and it is not adequate especially for fast changing competitive high-tech market conditions. Intel's initiated effort to level the project budgeting exercise among product groups by introducing "Converged Core/Uncore and methodology" and tick-tock product roadmap strategy. These new initiatives provide the nice staring point to accumulate database but the effort has just started and only a few development sites had experienced

it. Intel management's potential goal is to resemble the successful copy-exact model successfully employed in the fabrication process and sustain low cost/flexible product development structure. Recently introduced "Converged..." product development strategy in previous chapters helped to address the project budgeting issue but the past learning was largely assumed to be good for the similar size problem set on the same fabrication technology. Intel's senior level management team still experiences difficulty to estimate the project budget for different project groups (which has different expertise and experiences), different fabrication technology (which will require different design style), or combination of these two. Management's effort to use the generally accepted project budget estimate metric is always negotiated by each product group's aggressive desire to lead the project, the lack of database for the less defined future risk/feature changes, and the need for the quick decision making. This has been one of the biggest reasons for the fragmented project structure spanning over the several geographic regions. Intel definitely wants to develop the systematic approach to estimate the schedule and resources as well as the standard way to measure the project progress.

There is no perfect organization and there always is a room to improve. Intel's tick-tock is viewed almost invincible at one point but Intel's internal started to develop wish list for it to be improved more. Issues around project management flexibility, global product development resource utilization, project steps alignment and common project progress metrics were discussed in this chapter as items to be overcome to bring Intel's product strategy to the next level.

Next chapter will suggest two organizational structures introducing the systems department to resolve identified issues.

Chapter 8. Systems engineering, GPD and Tick-tock

It is widely accepted that Global Product Development (GPD) is setting the new landmark in the collaborative product development arena because of its several unique advantages such as low cost, easy access to the local market, and task allocation flexibility [220][221][222]. It is also true that this evolving technique has been criticized for the potential unnecessary engineering overhead increase and less suitable for the fast changing high-tech products. Even with the moderate criticism, there are several recent examples (Apple's iPod, iPhone and Cisco's communication solution product line) to show the systems engineering in partnering with global product development can be a good harmonized market-winning solutions even in the high-end premium product space [223][224]. These are clear indications that systems engineering moves from the traditional complex avionics and governmental application area to proving itself as powerful tool in the commercial product space [225].

The thesis discussed in the previous sections Intel's new demand for the efficient Global Product Development strategy that allows the flexible site/resource allocations, long-term low cost product development while it keeps the agility to react to the fast changing market dynamics and the focused on-schedule product development[5]. The thesis proposes two organization example structures that take systems engineering department into account on top of the current development structure presented in the Chapter 6.

[5] It should be differentiated from the focused-site development. "Focused product development" is used to highlight the project's product focus not the specific geography or other constraints.

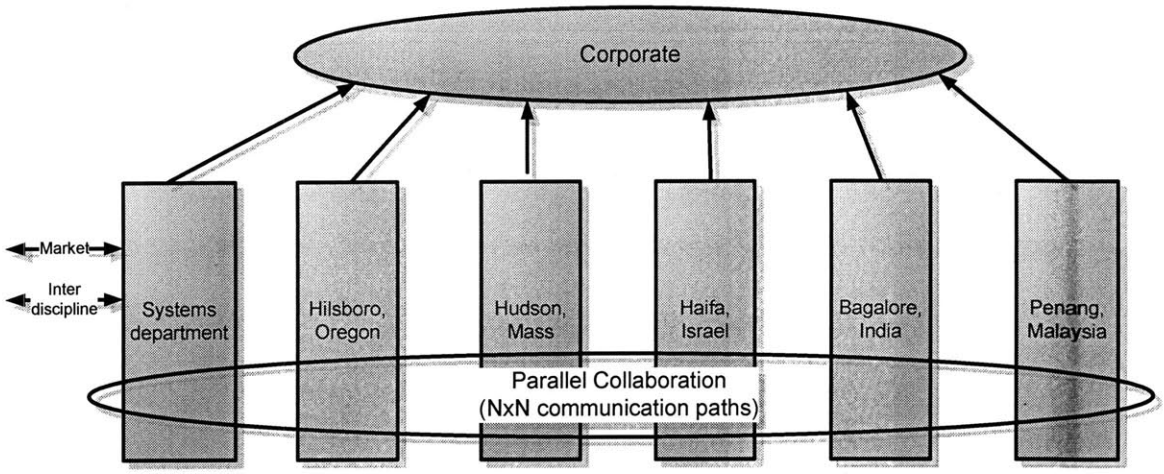

Figure 21 Intel's product development structure proposal #1 leveraging systems engineering and GPD

I. Proposal # 1: Systems department with the current development site structures

Figure 21 shows the proposal to introduce the systems department to the current Intel's product development sites. It is a just simple matrix type management structure that the system department may act a guiding role to the product sites. The proposal does not try to reduce the number of connections between development sites for the higher efficiency. It is designed to achieve higher efficiency by the systems department's communication facilitation and project guidance consulting.

Intel operates ten microprocessor development sites world wide as of year 2007. Five development US sites are located in Hillsboro Oregon, Santa Clara California, Folsom California, Fort Collins Colorado, and Hudson Massachusetts. There two Asia based development sites in Bangalore India and Penang Malaysia. There two development sites in Israel and one is located in Moscow Russia. As describe in the chapter 6, each of the product site has different variety of strengths and places to improve.

Intel has not traditionally differentiated each site's strengths. It has encouraged the knowledge shares among sites to groom the all sites to be similarly capable. This strategy introduced problems such as expert employee's commitment of the temporary move to the new location, conflict of priority, not-my-project symptom, communication overhead and not-negligible discretionary traveling charges. As shown in the Figure 21, the systems department is introduced to the existing structure to provide the following basic functions.

1) Provide product development guidance

One of the senior management's wish was to apply the common project resource/funding estimate tool so they can pre-plan the product line roadmap and resource/site allocation with no later stage surprises such as unexpected budget spending or product delay. The project team has the similar desire to the common metrics in order to run the product competitive scope and schedule trade-off analysis. It would help the product team to avoid the later unexpected budget spending to find the technical talent and provide proper accommodations. The systems department collects the database built up by multiple past projects and the experience gained by estimating the new complex projects. It will provide the project estimate guide based on the collected and processed information. The project team uses this as a benchmark for their project estimate.

2) Help the fast and effective decision making

The identification of the stakeholder's requirements and facilitation of decision-making process has been one of the big aspirations of Intel's management and product team. The systems department will connect interfaces among stakeholders

and help stakeholders' efficient decision making. It is very crucial for Intel's platform strategy and reuse/share component initiative to provide as efficient communications for the sound decision in a reasonable time as possible.

3) Arrange deliverables between projects

It was discussed how important deliverables definition for the collaborations involved various projects would be. It removes the potential peoples concern of overworking for the little credit and frustration to lead not-my-project symptom. The system department may not be the organization formulating the deliverables but it can mediate decisions and open discussions.

4) Multi-disciplinary steps alignment

The one example of mis-aligned project management event was provided in the previous chapter 6, which delayed the product testing by two months because the package team did not realize the product would be ready two months ahead of schedule. The systems department leverages their visibility over several disciplines and provides the proper warnings/arrangements to each group at the right moment.

5) Provide the potential future product requirement to the current project

It is easy for the product development team to overlook the crucial market and customer future demand shift because their first priority is to deliver the product, which tends to reduce the product scope. Intel had a bitter lesson from the competition with AMD. AMD's supports on 64 bit computing, integrated memory controller, and inter-processor communication ports were at least a year ahead of Intel. This event made Intel lose the significant portion of market share. Systems

department prioritizes important future product features and makes sure the crucial features to be added in the current product implementation.

6) Support and author the product specification

The systems department interfaces with many different organizations, customers, and engineering/marketing disciplines. This provides them a unique position to support the local product definition support and even to author the draft of the initial product specification. The systems department may be the organization to maintain the initial version of product specifications that can be shared by product groups and future discussions.

Intel has operated the engineering centric organizational structure that each localized product team has the power for the product feature decision and project budget estimation. It was mainly due to the past success of Intel's CPU product and fast emerging market/technology. Intel didn't necessarily feel to develop the long term strategy or platform thinking when the market was fast developing and it had won the market by rather inferior product but fast product revision than the competition. This previous product strategy worked effectively if the competitor's product was just marginally better for the short time period or product was not as complex so the fast revision allowed Intel to catch up or win the competition. Intel has relied on the upper level of management team for the complex decision making if there was conflicts from the product teams' interest or desire[6]. This was viewed as extremely bureaucratic between each groups and not-consistent ad-hoc type decision making process because there has been no department consistently arranging opinions and needs among product groups and projects.

[6] Intel's CEO Paul Otellini mentioned in his corporate internal blog, "we never been able to say NO to product groups, which led us to be bureaucratic, over-budget projects resulted in extreme in-efficiency."

While the role of the systems department in this proposal #1 is limited as opinion, data, and guidance provider as collaborative partner and consultant with the product group, the systems department should be able to provide consistent and reliable consultations to where their opinions are required. In this proposal, the current tick-tock cadence will be performed by searching for the attainable engineering resources as usual while all the processes are expected to be more fluent and smooth by the help of the systems department.

The second proposal will discuss the systems department's proactive role in the product development space.

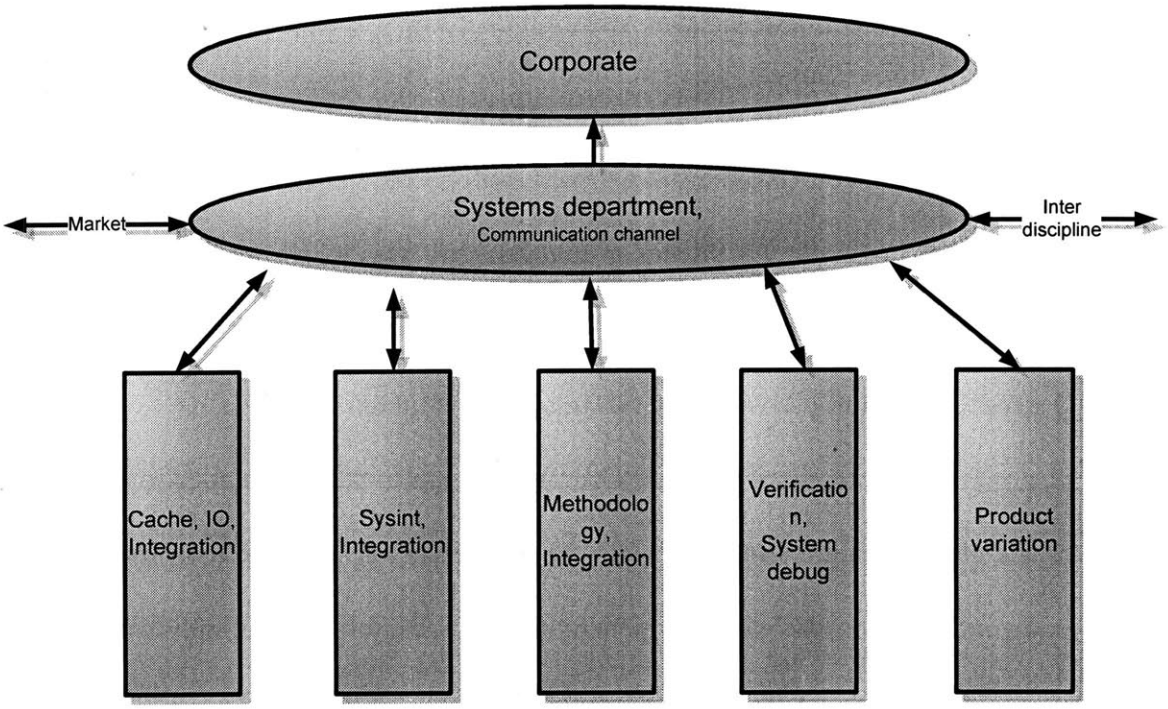

Figure 22 Intel's product development structure proposal #2 leveraging systems engineering and GPD

II. Proposal #2: Systems department as a product development group

Figure 22 shows the more radical change of the product development structure by introducing the systems department as a higher hierarchy organization of the existing product teams.

The proposal recommends changing the product groups to the specialized experts group depending on the level of experience, the current expertise, and the proximity with other disciplines such as fabrication technology and planning. Cache and analog input/output circuit design, for example, will be delivered by Hillsboro Oregon to all projects using the built-up engineering experiences and the fabrication technology development proximity (cache and analog design heavily depend on the technology characteristics). The product integration and design methodology development will be done in more experienced sites than the site that will be in charge of verification and systems debug.

The product miniaturization and derivatives will be allocated to the newly developed project sites as well.

This model suggests that the systems department will become an active product development team involved in the decision-making processes for the tasks described in the previous proposal.

1) Enable efficient global product development structure

One of the common fears about GPD strategy is multi-site communication. This organization structure allocates clearly defined tasks to each expertise product group and monitors the each component delivery progress for integration sites second stage work, product integration. Systems department utilizes its best position and collaborates with the integration product group to define product scope, nice component interface, schedule estimate, and resource allocation. The communication overhead between different engineering sites will be at the minimum level from the help of cleanly identified component interface, deliverables/work credit definition, and systems department's communication facilitation. Each engineering group's main communication channel will be the systems department so they can concentrate on the component delivery. Systems department should have a clear understanding about the capability/experience differences among product groups and be able to define deliverable interfaces to make the project successful. It should be realized that systems department's ability to understand overall product requirement and provide clear crisp specification is key to dynamic allocation of tasks and engineering resources so the communication

via systems department can be most efficient and not considered as yet another project management overhead from each product development groups.

2) Estimate the accurate product development budget and schedule

The systems department has all information about past projects and experiences for the new project resource budget. It may define financial cost, schedule budget, and probably actively be engaged to the product integration site selection. It will keep performing project progress audit and resource/schedule adjustment. It is also expected that the estimate will be more reliable because the same expert group will perform the similar task for the next project.

3) Expedite effective decision-making

The systems department should collaborate directly with the product integration site to define the inter-site deliverables. The integration site will only have one physical interface for the decision-making, systems department. And the systems department will potentially deal with less number of stakeholders mainly consist of other systems department group as opposed to all project groups.

This will allow the expedited decision-making process and probably more stable decisions since less of variety issues would pop-up.

4) Better product quality

Each product engineering group specializes in their expert component delivery. This will make not only more predictable schedule/budget estimate but also more consistent component quality possible. Each group can develop the methodology to engineer the component more efficiently and may eventually enable the earlier integrated product test, which will improve the overall product quality. Intel as a

corporate can take advantage of common design methodology and verification steps. The component design from the specialized group may not the best optimized when the initiative starts but the biggest advantage is it will create the design commonality among products so the design mistakes can be found (because of wider engineering/user base) easily and the common treatment can be applied, which can enhance the design process efficiency and product reliability. The other advantage of the specialized group is that their wide range of user's request (more component), feedback (on errors and bugs), and demand to the better quality (e.g. power, area and speed) will enable the specialized group to ramp up to the best optimized component design rapidly. Therefore, the unnecessary communication can be minimized, projects make faster progress at a lower development cost with the higher flexibility. Figure 23 shows the modern microprocessor design developed by Intel [226]. The photograph shows that the cache structure takes more than 30% of the total product foot print and IO PAD takes up significant area of the product. These structures are, for example, either very tightly coupled with fabrication technology or systems architecture. It is extremely important that they need to be very efficient design while they satisfy the other external constraints. If Intel operates the specialized group, it will provide great product competitiveness and potentially resource allocation flexibility.

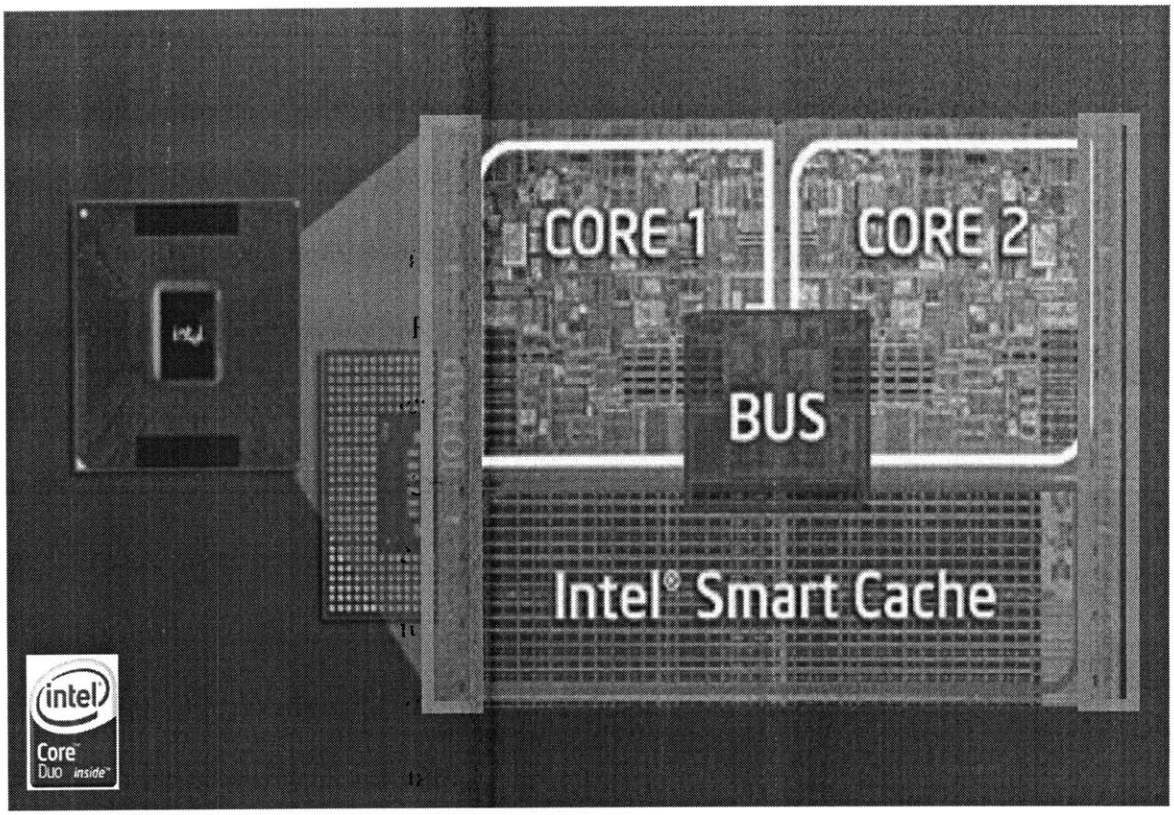

Figure 23 Intel's dual core product silicon die photograph

5) Owner of the inter-project deliverables and author of the product specification

In this proposal, the systems department is an empowered product co-ownership department collaborating with the integration product group. It should be entitled to the authority of driving the product feature decisions and defining multi-project deliverables. The systems department's intermediary position is well supported to provide the harmonized product feature decision that serves multiple/future projects requirements and drive the success of the current ownership project.

It is important to note that the shared-ownership assumes the shared-responsibility for the project success or failure to avoid the blames for the systems department, which is commonly criticized to only bothersome overhead for the product teams' activity.

The shared-responsibility by the systems department and the product integration team should work toward achieving the best efficiency to the corporate projects as well as it should keep the ownership project on the schedule.

6) Multi-disciplinary communication channel

Figure 22 shows the one important property of the systems department as a product development ownership department. The department interfaces with other business internal and external disciplines. The project structure with the systems department will have better capability to align inter-disciplinary issues and impose the higher chances to lead the overall discussions for the sound decisions. It will also be a benefit to the traditional product-engineering group because they can isolate the team from the distractive discussions while they keep the general visibility about the collaborative work by the help from the partnering systems department.

III. DSM Evaluation of the proposal

New DSM diagram is synthesized based on the assumption that two new groups will be introduced. Central technology group will deliver the optimized component to unit design teams and systems department will define the project and facilitate communications between groups. The same methodology used to create DSM analyses in the chapter 6 was employed. Each unit design was divided in the multiple different design stage and interactions between tasks were categorized in "A", "B", and "C" buckets. The level of interaction complexity was quantified as 3, 2, and 1 respectably to the each category. Note that the new DSM in Figure 24 has one more column and row compare to Figure 17. New DSM has one another column for the central technology and it becomes 14x14

matrixes from the original 13x13 matrixes. Global architecture group (Figure 17) receives the added responsibility and changes name to Systems department and global architecture (Figure 24). Figure 25 shows the extracted DSM information from Figure 24. If the matrix entry value in Figure 24 is greater than or equal to 3, then the entry in Figure 25 becomes "X", which indicates significant interaction. There are several observations to be mentioned in the comparison DSMs in chapter 6 and this chapter.

1) Systems department as a communication channel: the first column and row in Figure 24 shows the stronger interaction of the systems and global architecture department with other engineering teams. This synthesized result indicates that interactions communications among development groups use the new systems department as a communication channel either by pre-defined specification (first column in Figure 24 and Figure 25) or feedbacks from the each group for the current or future product definition (first row in Figure 24 and Figure 25).
2) Central technology team's role: While the activities via systems department increase, the flooding of requests to the systems departments are filtered by central technology team well developed component design and portfolio of offerings/variants. Central technology team maintains fairly high level of interaction with unit design group because of the components deliverables and planning work.
3) Reduced task complexity in the unit design: It should be noticed that the design complexity level within each unit team reduces from 58 (Figure 24) to 48 (Figure 25) because central technology team will deliver appropriate

component solutions to each unit team. This may indicate that further breakdown within the unit group can be performed and potentially unit group members can be located in different sites.

4) Reduced interaction among unit groups: Interactions among unit teams decrease noticeably in Figure 24 and Figure 25. This indicates that the overhead for each group to communicate with peer group reduces and main communication is performed in through systems department, central technology, or integration group. The extracted information in Figure 25 shows very little interactions between Uncore units. This suggests that globally dispersed location strategy (or GPD) for Uncore units development can be a prudent strategy. The potential GPD strategy would be to locate Core unit design team in reasonably homogeneous time-zone (e.g. within US or one country) and rest of unit designs can be flexibly allocated.
5) Reduction in number of significant interactions in DSM: Values in the DSM matrix entries in Figure 17 and Figure 24 represent the degree of interaction complexity. Total sum of values in each Figure 17 and Figure 24 are 1327 and 1326 respectably. In addition, "X" in Figure 18 and Figure 25 DSMs represent the significant architectural and procedural interactions between development tasks. Figure 25 includes less number of total "X" in the DSM than that of Figure 18. It should be noted that DSMs for the proposed management structure has more entries and categories while they contain less quantified aggregate interactions. This interesting analysis suggests that the proposed structure is more suitable to GPD. The proposed structure will

be even more efficient, if the synthesized scenario was to analyze multiple projects interaction. In such cases, systems department will be in charge of communications between projects and central technology team delivers the common design to multiple projects. Their interaction complexity may increase but the complexity will not be complicated as the scale they support several projects. As total aggregate effort, Intel certainly can take advantage of the proposed structure.

			1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Systems department & Global architecture	1	17	9	9	9	9	9	9	9	9	9	9	3	5	2
CORE	Instruction unit	2	13	48	4	2	2	1	0	0	0	0	0	2	4	4
CORE	Issue unit	3	13	3	48	5	5	2	0	0	0	0	0	2	4	4
CORE	Integer execution unit	4	13	2	5	48	0	4	0	0	0	0	0	2	4	4
CORE	Floating point execution unit	5	13	1	4	0	48	4	0	0	0	0	0	2	4	4
CORE	Store & Load unit	6	13	1	2	3	3	48	5	0	0	0	0	2	4	4
UNCORE	Cache coherency and uncore architecture unit	7	13	0	0	0	0	5	48	2	0	0	0	2	3	4
UNCORE	System coherency	8	13	0	0	0	0	0	4	48	2	2	0	2	3	4
UNCORE	Interprocessor router	9	13	0	0	0	0	0	0	2	48	2	1	2	3	4
UNCORE	Memory controller	10	13	0	0	0	0	0	0	2	2	48	1	2	3	4
UNCORE	IO pad	11	13	0	0	0	0	0	0	0	2	2	48	2	3	4
UNCORE	Misc blocks (Test, Power management)	12	13	2	2	2	2	2	2	2	2	2	2	48	3	4
	Central technology	13	9	8	8	8	8	8	8	8	8	8	8	8	35	7
	Chip Integration	14	5	7	7	7	7	7	7	7	7	7	7	7	9	10

Figure 24 Summarized DSM of microprocessor development with the proposed project management structure #2. Numbers represent the level of interactions among architectural units and efforts.

			1	2	3	4	5	6	7	8	9	10	11	12	13	14
	Systems department & Global architecture	1		x	x	x	x	x	x	x	x	x	x	x	x	
CORE	Instruction unit	2	x		x										x	x
CORE	Issue unit	3	x	x		x	x								x	x
CORE	Integer execution unit	4	x		x			x							x	x
CORE	Floating point execution unit	5	x		x			x							x	x
CORE	Store & Load unit	6	x			x	x		x						x	x
UNCORE	Cache coherency and uncore architecture unit	7	x					x							x	x
UNCORE	System coherency	8	x						x						x	x
UNCORE	Interprocessor router	9	x												x	x
UNCORE	Memory controller	10	x												x	x
UNCORE	IO pad	11	x												x	x
UNCORE	Misc blocks (Test, Power management)	12	x												x	x
	Central technology	13	x	x	x	x	x	x	x	x	x	x	x	x		x
	Chip Integration	14	x	x	x	x	x	x	x	x	x	x	x	x	x	

Figure 25 DSM – extracted for the proposed management structure #2

IV. Multi-project situation in the proposal

Figure 26 shows Intel's typical product development cycle for the microprocessor design, which can apply to any product development across industry. Intel's current focused-site (chapter 4 and chapter 5) has two significant problems with the figure below. 1) Redundant resources at early stage of project: At the beginning of the project, only small fraction of the peak resource (may occur at the later stage) is required to the high level tasks like architecture and product plan. The focused site strategy may run into situation that majority peoples in the project site are not working on the productive task or allocate idling peoples to the other project will be not-so-easy problem because Intel needs to re-locate peoples to the other leading project site. 2) Short of resources at late stage of project: It is commonly observed in the product development cycle that final stage tasks suffer from un-resolvable loop of unexpected work and more resources. In the likely case that the final stage of project requires more resources, Intel's focused-site strategy may not be able to react quickly because it requires helpers come in from the other geographic region.

It is really important for the successful GPD to keep resource allocation flexibility and liquidity, which can be maintained by the proposals in this chapter.

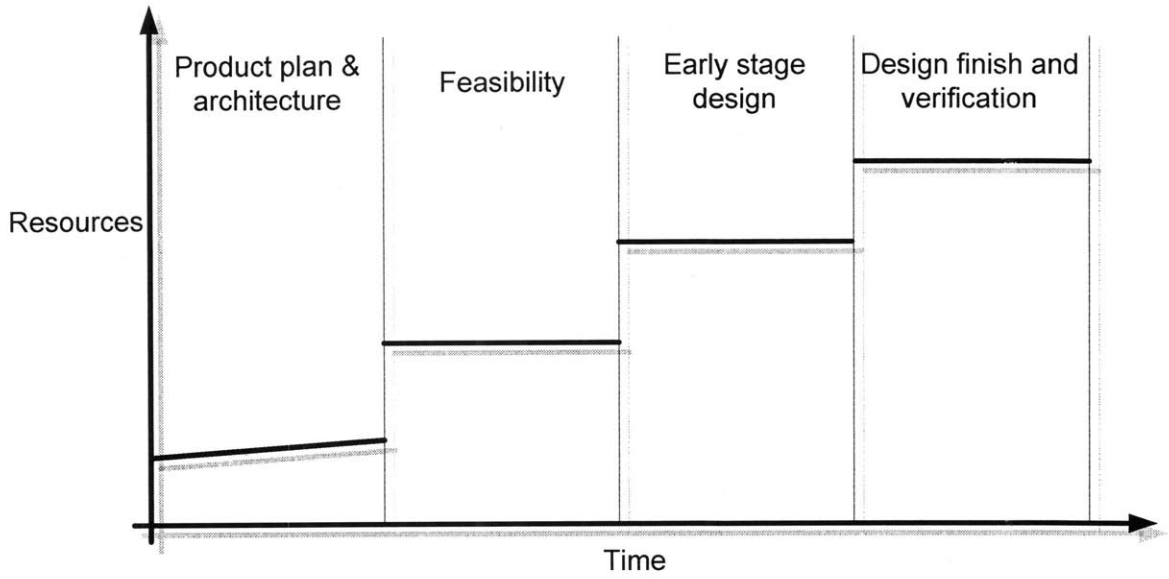

Figure 26 Intel's typical Product development cycle

Figure 27 and Figure 28 show the project progress comparison of Tick-tock cadence between the current focused site strategy and proposed systems department model #2. the scenario assumes 1) three projects led by tick-tock cadence, 2) three development sites, 3) started at the same time, 4) full capable development site in the focused-site strategy, 4) systems department and central technology team for the proposed structure. In the proposed project structure, responsibilities of developing each unit or product integration rotate among development sites to groom the full capable site as the site managers hoped. It should be notes that responsibility rotation is possible because the degree (or complexity) of unit development task is not as high as that of the focused site strategy[7]. And it is also assumed that the flexible support from the previous unit design team to the current team's potential path finding in the proposed model scenario.

[7] Compare Figure 17 and Figure 24

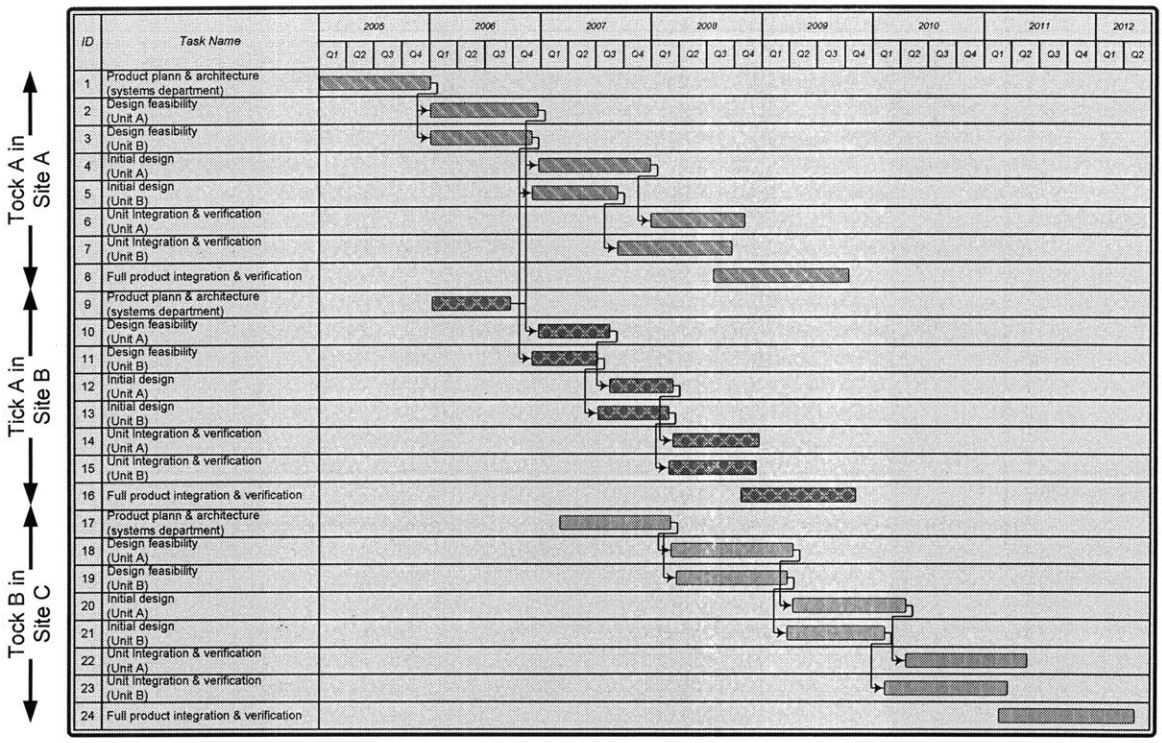

Figure 27 Project progress Gantt chart by the current Tick-Tock with focused site model

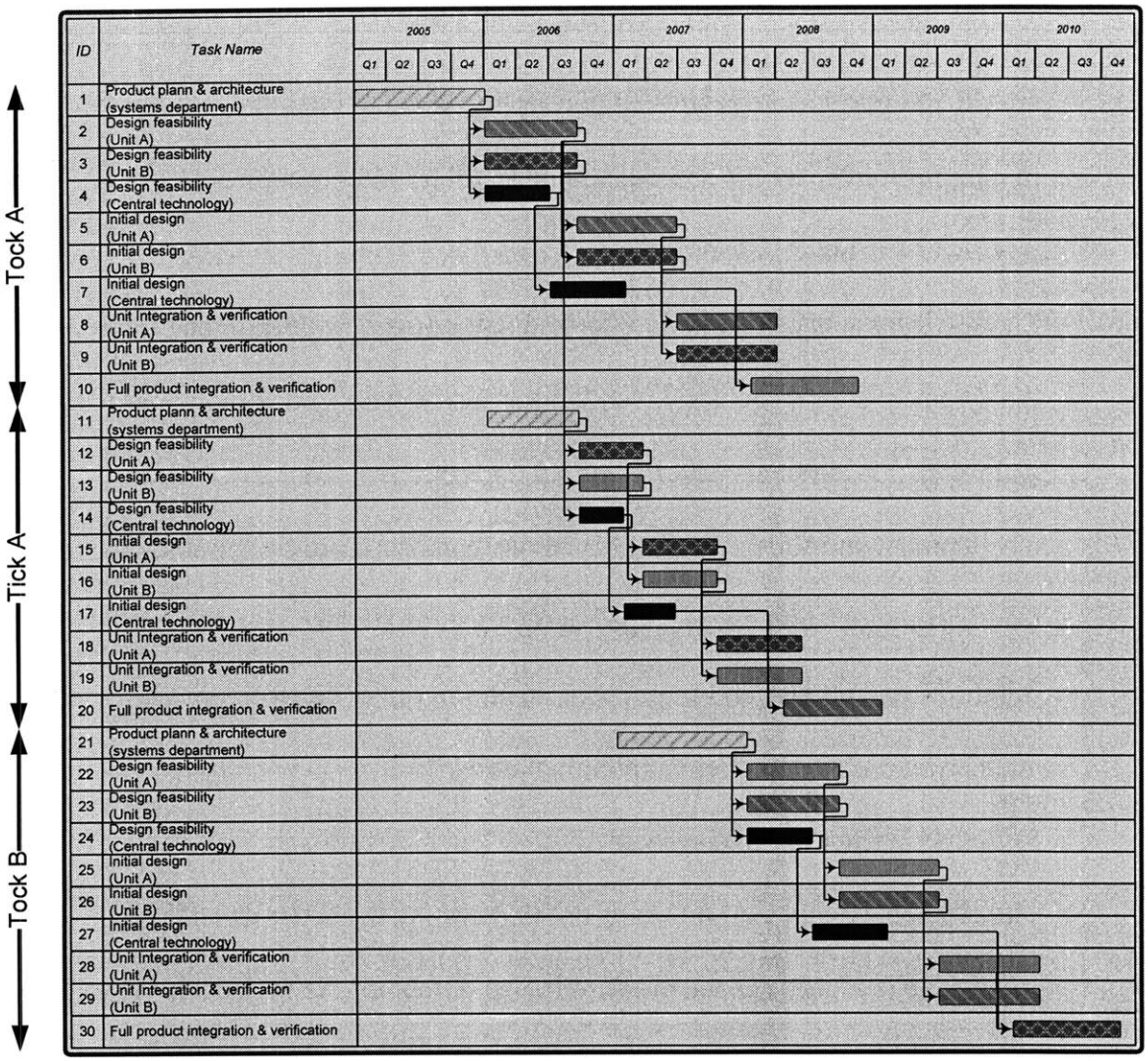

Figure 28 Project progress Gantt chart by the proposed structure and Tick-tock cadence

Here are several observations to be highlighted from Gantt chart analysis.

1) Faster project progress

Comparing two figures above, each tick or tock projects finish earlier in the proposed structure than the current model. It was assumed that planning and architectural definition took the same amount of time. The benefits were from two places. 1) The existence of the central technology team reduces feasibility period, unit integration and product integration/verification time by providing well-

optimized component design. 2) Systems department publishes cleanly defined specification and each group's responsibility, which reduces integration/verification overhead and unnecessary inter group communications.

2) Efficient resource allocation

Figure 28 show that all resources in the picture (systems department, three development sites and central technology) are fully utilized with no redundant waiting period. Systems department's fluent communications with each development site allows the flexible resource allocation and central technology team's common component helped design teams to reduce un-foreseen risks. Figure 27, in contrast, shows not consistent progresses between units (A and B) and between tasks (feasibility and initial design).

3) Better dependency management

The efficient resource allocation is enabled also by the better dependency management via centralized project progress structure. As noticed in Figure 25, significant cross dependencies among each group and task reduces and it happened more frequently via systems department and central technology group in Figure 28.

4) Gain experience through responsibility rotation

The responsibility rotation was enabled by the proposed structure by lowering the unit level task complexity and systems department's proactive task allocation[8]. This rotation strategy provides not only each development site to take the project ownership but also to gain experiences to become a full capable design site by participating many different projects and helping other teams challenges.

[8] Compare Figure 17 and Figure 24

The project structure may provide the good balance among the focused engineering tasks by well defined deliverables, the consideration for other and future projects, and the flexible site/resource allocation.

It should be noted that the systems department is best positioned to lead defining product platform architecture, which would result in the corporate level overall product development strategy. It is probably most important role that systems department would play and the systems department is best positioned to perform. As it was described in the previous chapters and Figure 20, the lead product group (tock project) maintains a connection to product marketing and platform development (chipset and board) group. This proposal suggests that Systems department should take the best advantage of horizontal (among product groups) / vertical (among different discipline) communication channel to lead the long range platform activities as well as short term product development ownership.

Chapter 9. Conclusion

Thesis started with the discussion how Intel landed to the Tick-tock product development strategy to lead the industry and challenge competitors. A small case study on how Intel managed the first version of "Converged Core" Tock (Merome, MRM) and Tick (Penryn, PRN) projects was provided to learn the successful product development example. The first implementation of Tick-tock cadence heavily leveraged the focused-site development strategy, which worked great for Intel to catch up the competitor and upset the market's product favor in very short time frame. The focused site based product development allowed Intel to comeback to the winning position quickly but the management started to possess the new desire for the flexible project structure.

The chapter 6 discussed the Intel product development communities' evolving concerns of the rigid focused site strategy, multi-stage collaboration overhead, and project management flexibility. While the chapter alluded the Global Product Development (GPD) as a potential new project structure, Intel's unappealing experience with the past multi-site project management made them rather contracting back with the expensive yet more controllable focused site strategy.

The chapter 8 proposes two project structures that introduce systems department as part of the product development organization.

The first moderate proposal limits the new organization's role as a mediator, facilitator, and consultant. The systems department will provide project groups schedule and product feature definition consulting as opposed to lead all activities. This proposal can be smoother for Intel to integrate with the current product development site organization in a near future since it does not require radical structure changes. However, it does not fully

utilize the whole function of the systems department and it has a potential risk of yet another matrix organization.

The second proposal is to allow the systems department the proactive project-leading role. It will actively participate the site/resource allocation discussions and product specification publications. The systems department will manage geographically dispersed GPD sites for the common project goals and seek for the best possible route to benefit the corporate by encouraging inter-site collaborations and interfacing multi-disciplinary organizations.

The benefits of the global product development led by the systems department were discussed in the previous chapter and verified by several analysis tools such as DSM and Gantt chart[9].

Here are several highlights.

- Enable efficient global product development structure
- Help the fast and effective decision making
- Accurate the product development budget and schedule
- Better product quality
- Arrange deliverables between projects
- Reduce the communication overhead
- Multi-disciplinary steps alignment and communication channel
- Provide the potential future product requirement to the current project
- Support and author the product specification

[9] See Figure 17, Figure 18, Figure 24, Figure 25, Figure 27, and Figure 28

Intel initiated Core/uncore converged methodology as responses to the competitor's superb product and started Tick-Tock production architecture to enable the efficient/strong product roadmap. The questions are if the current model is sustainable and what department will be in charge of enhancing the current strategies to the eternal unbeatable structures, which requires the constant effort to improve.

The thesis discovered that Intel's current strategy (Converged Core/Uncore/Methodology and Tick-tock model) is developed in the focused site assumption. It was also realized that Intel management team's desires for the flexible product development structure (dynamic resource allocation) in the global development structure, which will provide Intel potentially lower development cost and sustainable long term development resources[10].

The thesis suggests introducing the system department to lead the future Intel's product development strategy performed in the globally dispersed development sites (GPD). The unique position of the systems department should be able to minimize the communication overhead among product groups for the successful current product delivery and lead the future product definition by covering platform level requirements. It should be highlighted that the systems department proposal requires a strong commitment from the senior management to support the organization and the organization's own relentless effort to guide/help peer engineering groups so it would not be considered as another layer of overhead or the other type of matrix organization.

[10] And other advantage of GPD, such as local market access, will come together

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