The Fabrication of 3-D Photonic Band Gap Structures

by

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY

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ABSTRACT

Photonic bandgap (PBG) structures have emerged to provide exciting opportunities for new and improved devices covering the electromagnetic spectrum from microwaves to the optical region. A photonic bandgap crystal is a periodic dielectric structure that presents a range of frequencies within which photons fail to propagate. A defect state can also be introduced in the photonic band gap. PBG crystals are expected to be useful in making high-Q microcavities for single-mode light-emitting diodes and low threshold lasers. This project focuses on the fabrication of a class of three dimensional photonic bandgap structures exhibiting resonances at three midgap frequencies (4.3μm, 4.5μm and 4.7μm) using two material systems Si/air and Si/SiO_2/air. In the structure

under fabrication, the photonic bandgap is as large as 14% of the midgap frequency using Si/SiO_2/air and 23% using Si/air (after the SiO_2 is etched away).

In the process of building these structures, various fabrication issues have been investigated and addressed. The creation of trenches in polysilicon with straight side walls required the used of a low temperature oxide hard mask and a Cl_2-based plasma etch. The problems with various other masks and plasma etches that were used in a attempt to create the trenches, will be discussed. Various oxides were investigated in order to fill the poly Si trenches. Borophosphosilicate glass was found to completely fill the trenches, while oxides that were deposited by other means typically exhibited voids in the center of the trench. Chemical-mechanical polishing was used to planarize the surface after the deposition of borophosphosilicate glass. The chemical-mechanical polishing process requirements will be discussed as the PBG structure requires the complete removal of the oxide between the layers. Poly Si was then deposited on the planarized surface for the next layer and the process repeated. The use of oxygen ion implantation in order to always maintain a planarized surface and the use of a deep-UV stepper will be addressed.

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Chapter 1

Introduction

During the past 10 years, there has emerged a new class of materials called Photonic Band Gap Materials, or Photonic Crystals[1,2,3]. A photonic crystal is a periodic structure that presents a range of frequencies within which photons fail to propagate. This forbidden band of frequencies translates into a Photonic Band Gap (PBG), analogous to an electronic bandgap in a semiconductor crystal. Periodic dielectric structures have the ability to affect the density of electromagnetic states within their boundaries and to suppress all modes for a range of frequencies. They can greatly affect the radiative dynamics within the structures and lead to significant changes in the properties of optical devices. This has opened a new and fascinating area for potential applications in optoelectronic devices and has prompted research to find structures that would generate large photonic band gaps[4,5,6]. PBG structures have emerged to provide exciting opportunities for new and improved devices covering the electromagnetic spectrum from microwaves to the optical region.

A defect state can also be introduced in the photonic band gap when the dielectric periodicity of a photonic crystal is broken by the selective removal or addition of dielectric material[7,8]. This defect results in the spatial localization of the defect mode, yielding a high-Q electromagnetic microcavity. The realization of such a microcavity holds promise of vastly reducing the spontaneous and zero point fluctuations within an energy band.

A theoretical basis to the analysis of the structures was established where the concepts of reciprocal space, Bloch wave functions, Brillouin zones and dispersion relations became applicable. Experimentally, PBG crystals have been constructed for operation in the microwave region[9,10] and the fabrication of a two-dimensional photonic band gap nanostructure has been reported[11].

This thesis focuses on the fabrication of a class of three dimensional photonic band gap structures proposed by a group led by Professor John D. Joannopoulos at the Massachusetts Institute of Technology. The main problem with the microfabrication of a three-dimensional photonic crystal originates from the rather sophisticated geometry and intricate arrangement of holes and rods needed to open a band gap. These complex structures do not easily lend themselves to fabrication at submicron lengthscales. Furthermore, most applications for PBG structures require band gaps larger than 10% which, in turn, requires the use of materials with large index contrasts. For example, the 3-D PBG structure that is under investigation, is made of three materials (Si, SiO_2, and air) and consists essentially of a layered structure in which a series of cylindrical air holes are etched at normal incidence through the top surface of the structure. In the structure under fabrication, the photonic band gap is as large as 14% of the midgap frequency using Si, SiO_2 and air and 23% using Si and air (after the SiO_2 is etched away).

In this project, several difficulties arose during the fabrication of the three-dimensional photonic band gap structures. The first difficulty was the creation of the Si trenches with the correct geometry. This problem was alleviated by using a Low Temperature Oxide (LTO) as a hard mask as opposed to a photoresist mask and by using a special Cl_2 plasma etch. The second difficulty was the creation of voids in the SiO_2 that

was subsequently deposited into the Si trenches using a LTO or SiO_2 that was deposited by plasma-enhanced chemical vapor deposition. Through the use of 1 μm of boron phosphide silicate glass (BPSG) along with 1 μm of LTO, the Si trenches were completely filled with SiO_2 after the Chemical/Mechanical Polishing (CMP) step. The third difficulty that arose was in the etching of amorphous silicon. The non-uniformity of the chemical/mechanical polishing leads to the potential application of oxygen ion implantation. Also the difficulty in reproducibly creating proper alignment between the second layer Si trenches and the first layer Si trenches suggests using a contact aligner instead of the stepper. Future work includes the completion of the seven layers that are needed in the three-dimensional photonic crystal and the verification of the photonic bandgap.

Background and motivation are documented in Chapter 2. The experimental techniques using silicon technology are described in Chapter 3 and 4. Finally, the thesis closes with Chapter 5 and 6 which summarize and outline several possible extensions of the current work.

Chapter 2

Background and Motivation

2.1 Photonic Band Gap (PBG) Theory

A photonic crystal is a 3-D periodic dielectric structure possessing a frequency band or band gap over which all electromagnetic modes, spontaneous emission, and zero point fluctuations are forbidden, irrespective of propagation directions[12]. It is known that the rate of spontaneous radiative decay of an atom scales with the atom-field coupling and with the density of allowed states at the atomic transition frequency. By changing either the atom-field coupling or the density of states, the rate of spontaneous emission can be significantly affected. Since photonic crystals have the ability of suppressing every mode for a given range of frequencies, they can be used to control the rate of spontaneous emission. These crystals behave essentially like 3-D dielectric mirrors, reflecting light along every direction in space.

The most extensively studied examples of wave band gaps are electronic. In the field of solid-state physics, the allowed solutions of energy as a function of wave vector for this case are termed band structure, and the existence of gaps is most commonly illustrated by the splitting of energy states at Brillouin-zone boundaries. For electrons in solids, the scatterers are the periodic potentials of the lattice atoms, and the solutions are obtained by means of the Schrödinger equation. For electromagnetic-waves, we can

consider scatterers with any generalized dielectric and magnetic susceptibilities (dielectrics, metals, etc.), and the solutions are obtained by means of the four macroscopic Maxwell equations:

$$\nabla \bullet \mathbf{B} = 0 \qquad \nabla \times \mathbf{E} + \frac{1}{c}\frac{\partial \mathbf{B}}{\partial t} = 0 \qquad \nabla \bullet \mathbf{D} = 4\pi\rho \qquad \nabla \times \mathbf{H} - \frac{1}{c}\frac{\partial \mathbf{D}}{\partial t} = \frac{4\pi}{c}\mathbf{J}, \qquad (1)$$

where **E** and **H** are the macroscopic electric and magnetic fields, respectively, **D** and **B** are the displacement and magnetic induction fields, and ρ and **J** are the free charges and currents, respectively.

The photonic bandgap structure refers to a periodic array of dielectric scatterers for which the solution of Maxwell's equations over some frequency range consists of a evanescent propagation vector for all possible directions in space. Two approaches can be used to investigate PBG structures. The first solves Maxwell's equations in the frequency domain and the second solves the equations in the time domain. These two methods reveal different information. The frequency-domain method yields the frequency, symmetry, polarization and field distribution of every eigenmode. The time-domain method can be used to determine the coupling efficiency, the scattering and the quality factor.

2.2 Three - dimensional PBG design and basic results

Photonic crystals are expected to be useful in making high-Q microcavities for single-mode light-emitting diodes and low threshold lasers. However, the use of photonic crystals at optical frequencies requires the modulation of the dielectric constant at a submicron range, which represents a challenging fabrication task. Thus, it is equally as

important to find a geometry which lends itself to easier microfabrication as it is to design a structure that generates a large gap[13,14].

Figure 2.1 is a structure designed by the group led by Professor John D. Joannopoulos[15]. This is a simple layered structure made of two materials (Si, SiO_2). Only one series of holes are etched at normal incidence through the top surface of the structure. The cylindrical air columns can provide a large index contrast with the remaining material. This structure can be microfabricated by conventional techniques.

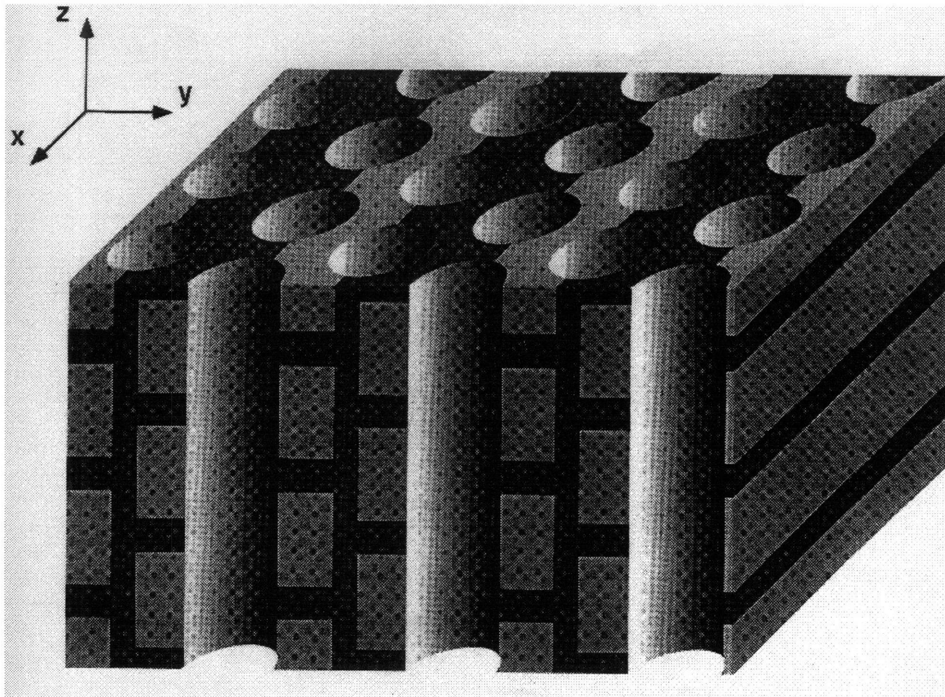


Figure 2.1: 3-D Photonic Band Gap (PBG) Crystal. A layered structure made of Si (black) and SiO_2 (light gray) in which a series of air columns are drilled into the top surface.

Figure 2.2 shows the same structure as Figure 2.1 but with the SiO_2 removed. The parameters of this structure are defined in Figure 2.3, where *w* and *d* are the width and depth of the SiO_2 - filled grooves (or Si trenches), respectively. It is convenient to choose

one of the lattice constants as the unit length scale. In this case, the period of Si trenches a is chosen to be the unit length scale and every other parameter is defined with respect to it. The size of the structure can be scaled to any wavelength simply by scaling a. For example, in the case where the gap is centered at 1.53μm (This wavelength is roughly equal to the one used in many optical devices for telecommunications today), a is equal to 0.79μm. And also, at λ=1.53μm, the dielectric constant is 12.096 for Si and is 2.084 for SiO_2.

We can achieve the maximum band gap by optimizing the parameters. In the Si/SiO_2/air structure (Figure 2.1), a gap as large as 14% of the midgap frequency can be achieved with $w = 0.40a$, $d = 0.49a$, $r = 0.21a$, $b = 0.71a$ and $h = 0.35a$, where r is the radius of the holes shown in the top surface of Figure 2.1 and b is the distance between them. In the above example where the gap is centered at 1.53μm (f = 196THz), the gap extends from λ=1.43μm to λ=1.64μm (f = 182THz to f = 210THz).

In the Si/air structure (Figure 2.2), after all of the oxide is removed, the gap can be further increased by reoptimizing the parameters. With $w = 0.36a$, $d= 0.51a$, $r = 0.24a$, $b = 0.71a$ and $h = 0.35a$, a gap of 23% can be obtained!

The corresponding band diagrams are shown in Figure 2.4. For simplicity, the bands are plotted along various directions of the irreducible Brillouin zone of a simple orthorhombic lattice.

How fabrication-related disorders affect the size of the photonic band gaps can be investigated theoretically. We can choose to study the following deviations which may arise during fabrication from a perfect photonic crystals: variations of layer thickness (h),

variation of trench depth (*d*), misalignment of the trenches between layers, overall surface roughness, etc. It is shown that the size of the gap is tolerant to significant amounts of deviation from the perfect structure[16].

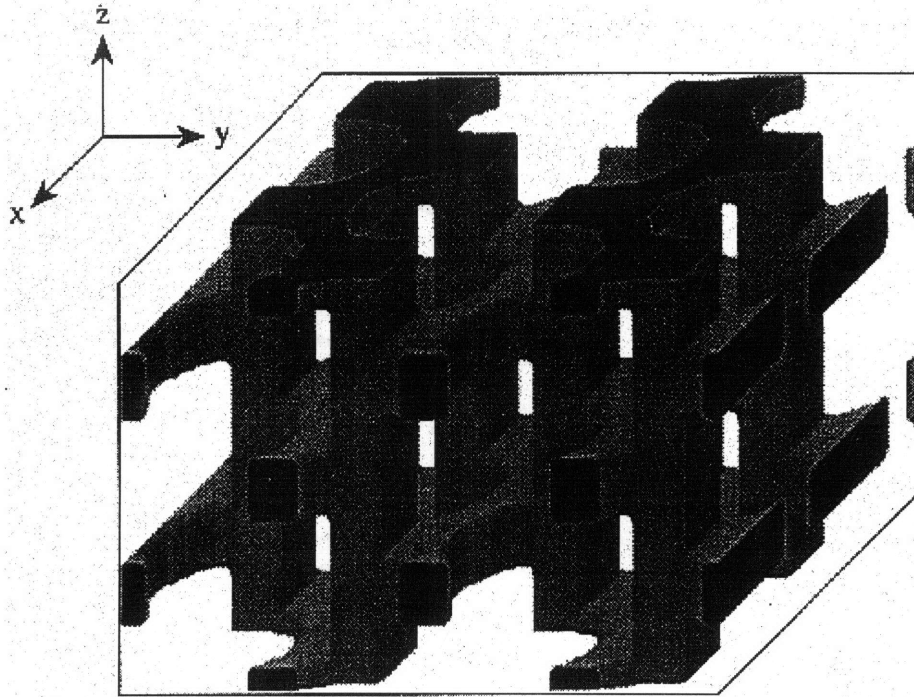


Figure 2.2: The same structure as Figure 2.1 except that all of the SiO_2 is etched away. Using only Si and air, the bandgap is as large as 23% of the midgap frequency. The entire structure is composed only of Si.

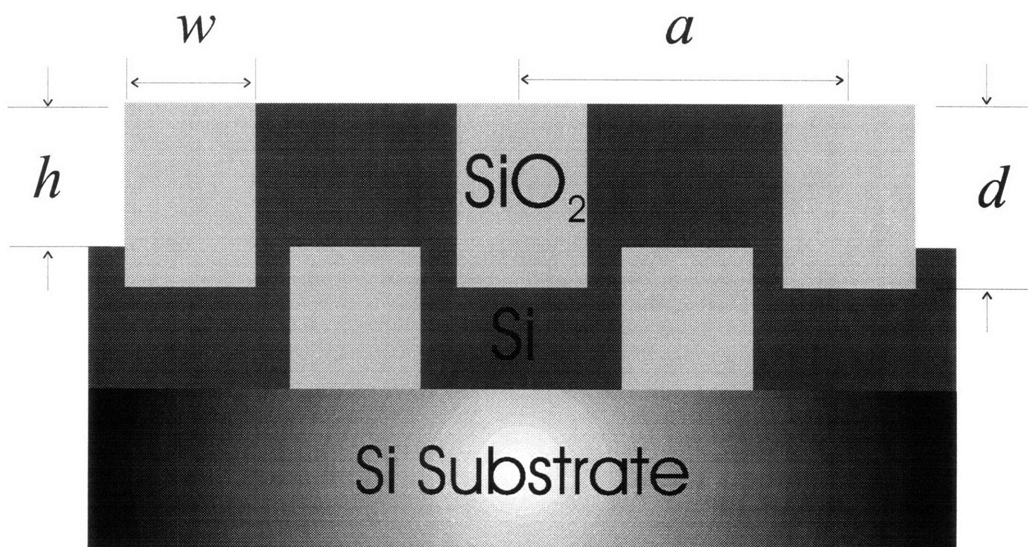


Figure 2.3: Definition of the parameters describing the PBG structure.

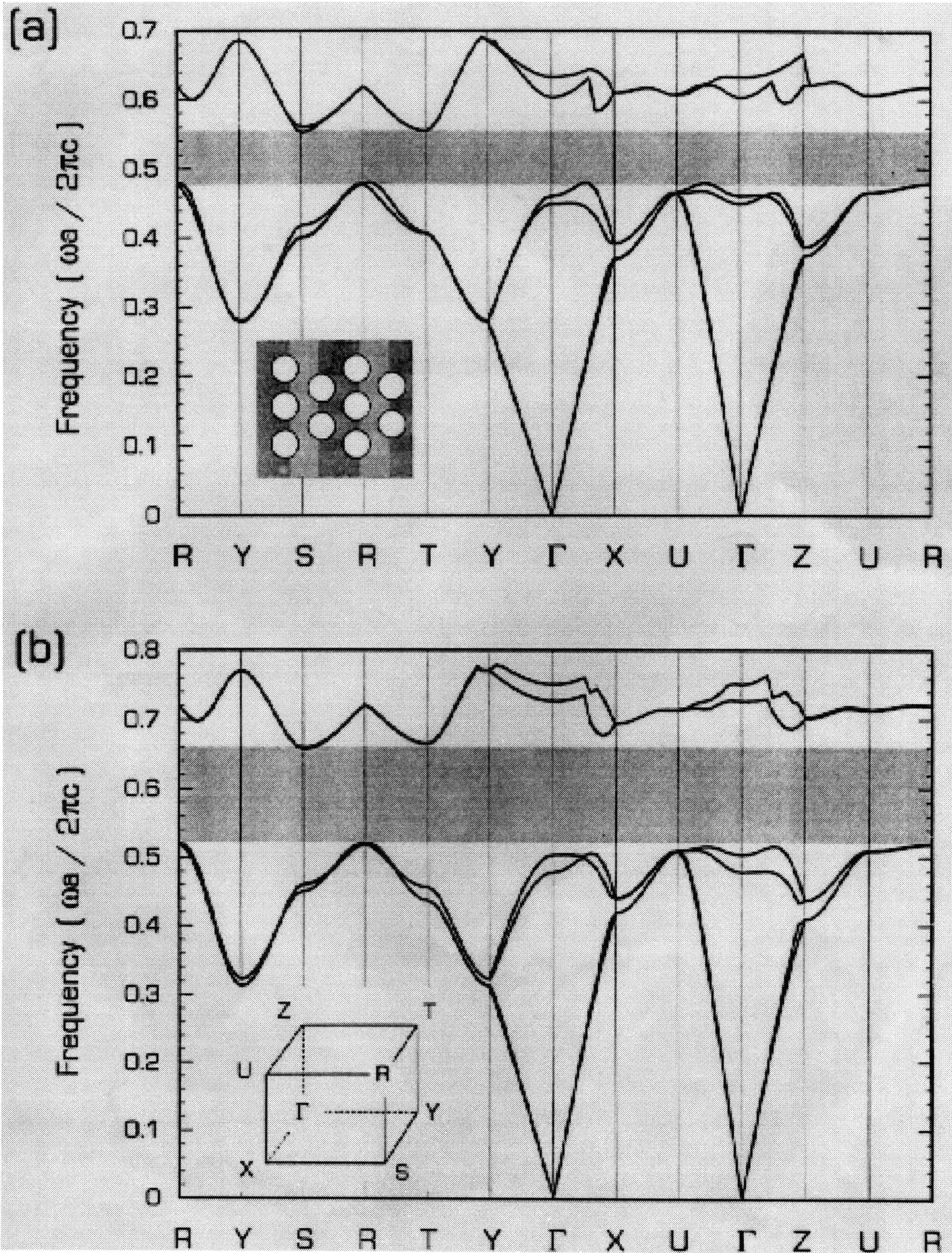


Figure 2.4: Energy band diagrams of the PBG structures: (a) corresponds to Figure 2.1 (Si/SiO_2/air structure); (b) corresponds to Figure 2.2 (Si/air structure).

2.3 Localization at defects

The introduction of a defect in a perfect PBG crystal can lead to the creation of sharp resonant electromagnetic states in the vicinity of the defect. The properties of these modes can be controlled simply by changing the nature and the size of the defect. A defect can be created by adding extra dielectric material into the structure, or by breaking a rib to remove some dielectric material from the structure. We might call the first a "dielectric defect", and the second an "air defect". Either of these defects could be implemented during fabrication. In the case of removing dielectric material (an "air defect"), the cavity mode evolves from the "air defect" and can be made to sweep across the gap by adjusting the amount of dielectric material removed. If the defect involves the addition of extra dielectric material (a "dielectric-defect"), then the cavity mode drops from the "dielectric-defect". In both cases, the defect state can be tuned to lie anywhere in the gap. This flexibility in tuning the position of the defects makes photonic crystals a very attractive medium for the design of novel types of filters, couplers, laser microcavities, etc.

Why does a defect localize electromagnetic modes? Actually, the defect is like a cavity with perfectly reflecting walls. If light with a frequency within the band gap somehow winds up near the defect, it cannot leave, because the crystal does not allow extended states at that frequency. So, if the defect allows a mode to be excited with a frequency within the band gap, that mode is forever trapped.

If the size of the defect is properly chosen, a localized state can appear in the gap. An example of such a state is shown in Figure 2.5. The cross-section of the energy

density is shown in the case where a rib is broken in the crystal. The state has a torus shape and is localized in all three dimensions. Its frequency, symmetry and field distribution can be changed by varying the size and the nature of the defect. In this case, the defect involves removing material (a single dielectric rib is broken at the center of the crystal), hence the resonance initially appears at the bottom of the gap, and moves up as the size of the defect is increased.

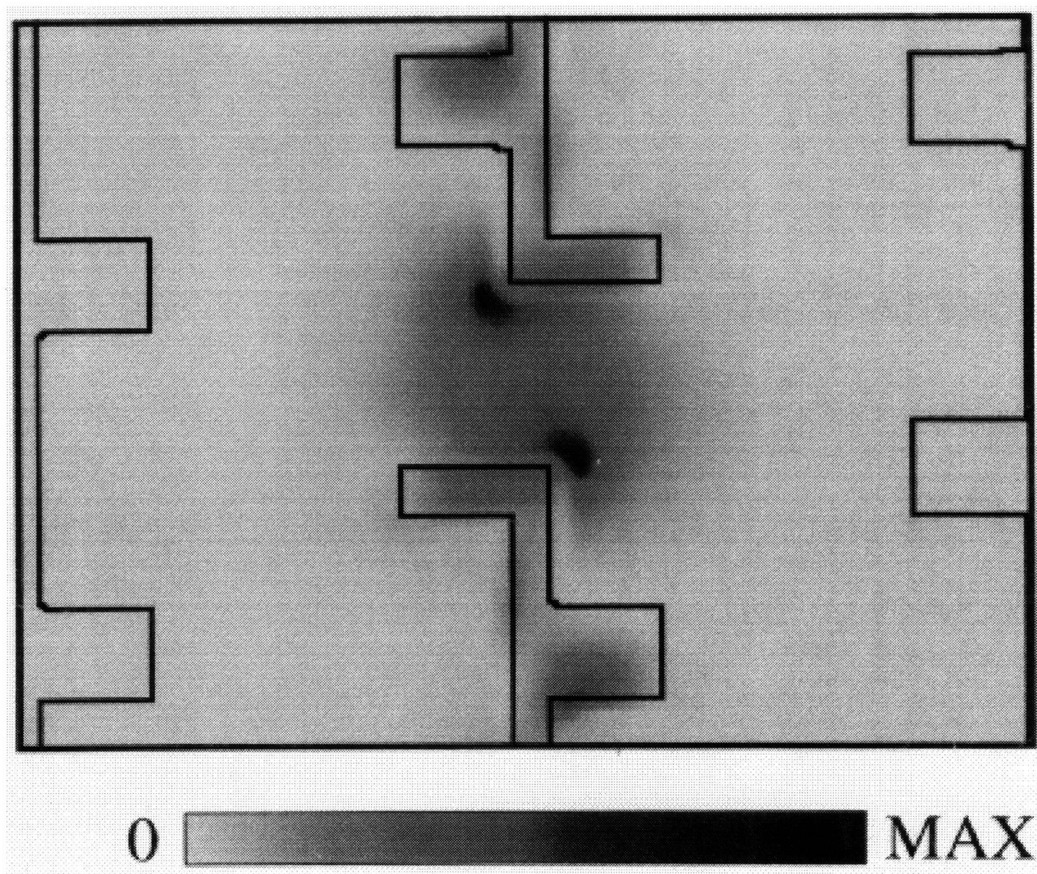


Figure 2.5: Cross section of the energy density of a defect state in the crystal shown in Figure 2.2. The defect is made by breaking one of the dielectric ribs. The overlay indicates the edges of the crystal.

Chapter 3

Fabrication Process of Generation I

3.1 Process Overview

How can we fabricate a three-dimensional structure using two-dimensional planar technology? The idea here is to fabricate patterned layers, one on top of the other, composed of materials having different dielectric properties. Together the multidecked "sandwich" of patterned layers on a supporting substrate is made to form various devices. An important aspect of planar technology is that each step of the fabrication process is applied to the entire wafer at the same time. The layering technologies include deposition, the pattern generation techniques of lithography, and the selective layer removal techniques of etching[17,18,19,20].

It is effective to achieve the necessary parameters and recipes by using monitor wafers before the real process. This is the reason why Generation I and Generation II are chosen. Generation I wafers are monitor wafers to determine the parameters and recipes for the real process of fabricating photonic crystals. Generation II wafers are processed for the real 3-D photonic band gap structures. Figure 3.1 is the fabrication process outline of Generation I. Here, we should emphasize the selection of Chemical and Mechanical Polishing (CMP). Previously, two other methods: (a) E-beam evaporation and lift-off and (b) PECVD deposition of SiO_2 and spin-on glass (SOG), were used in an attempt to planarize the surface. The schematic of these two methods is shown in Figure 3.2. For

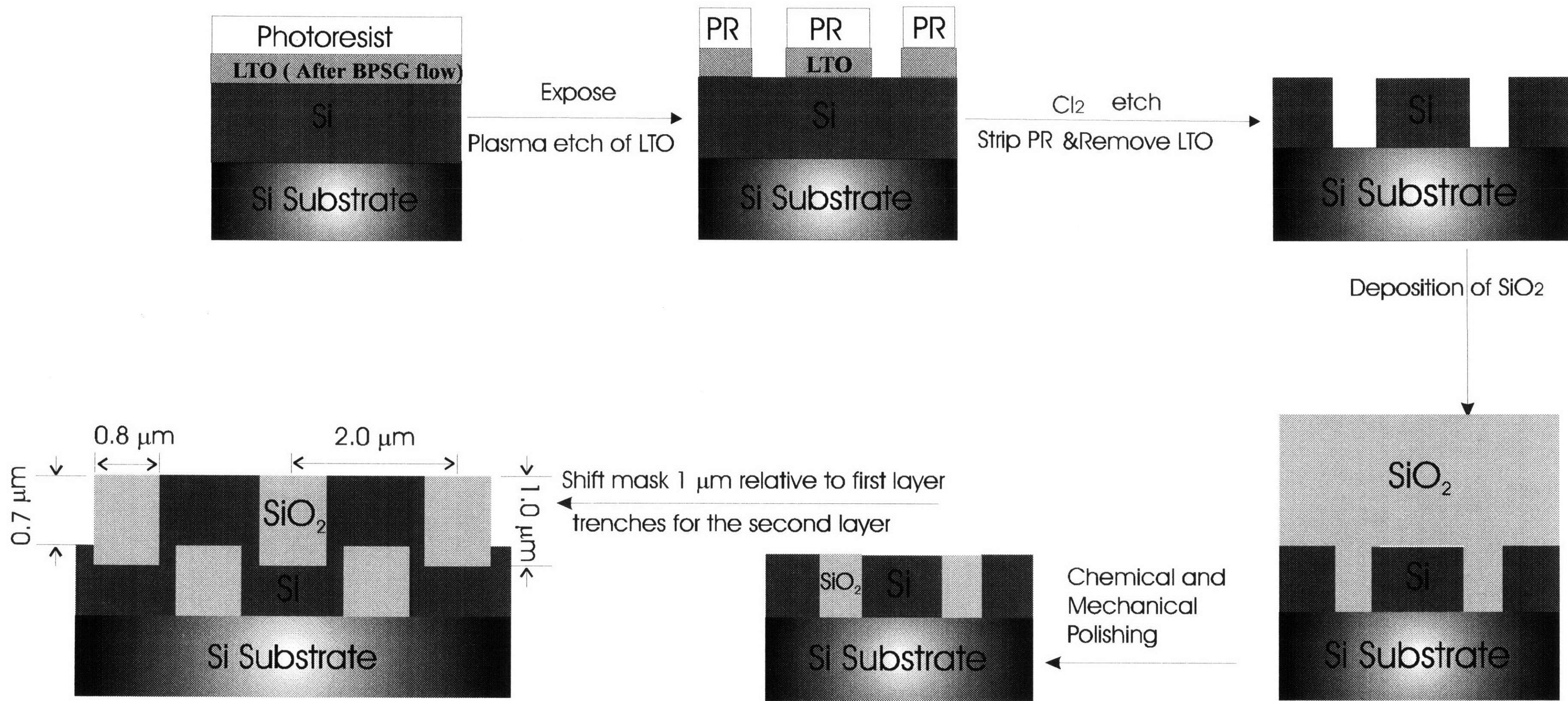
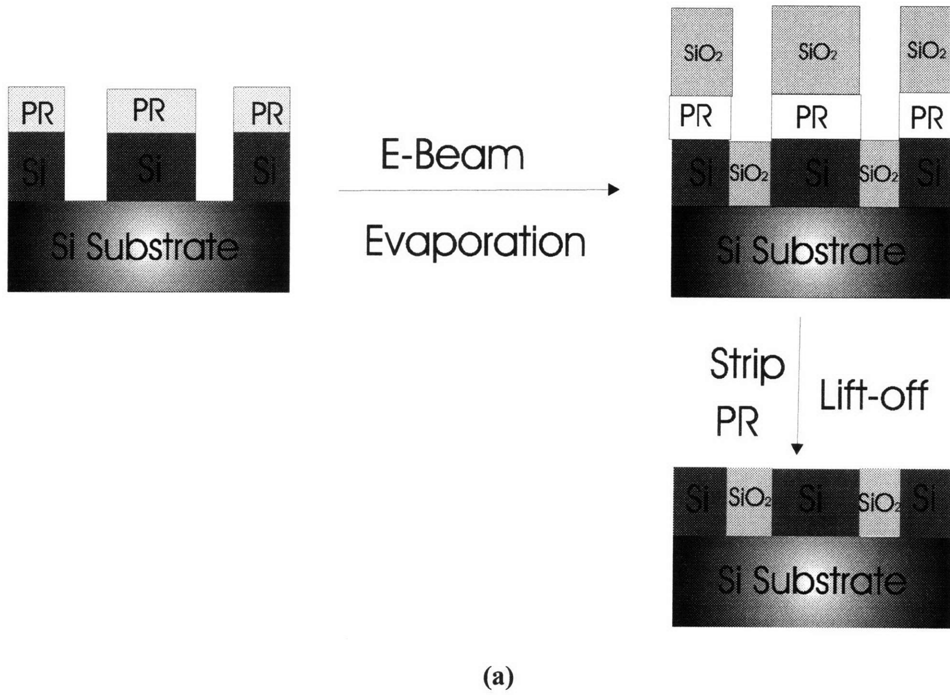
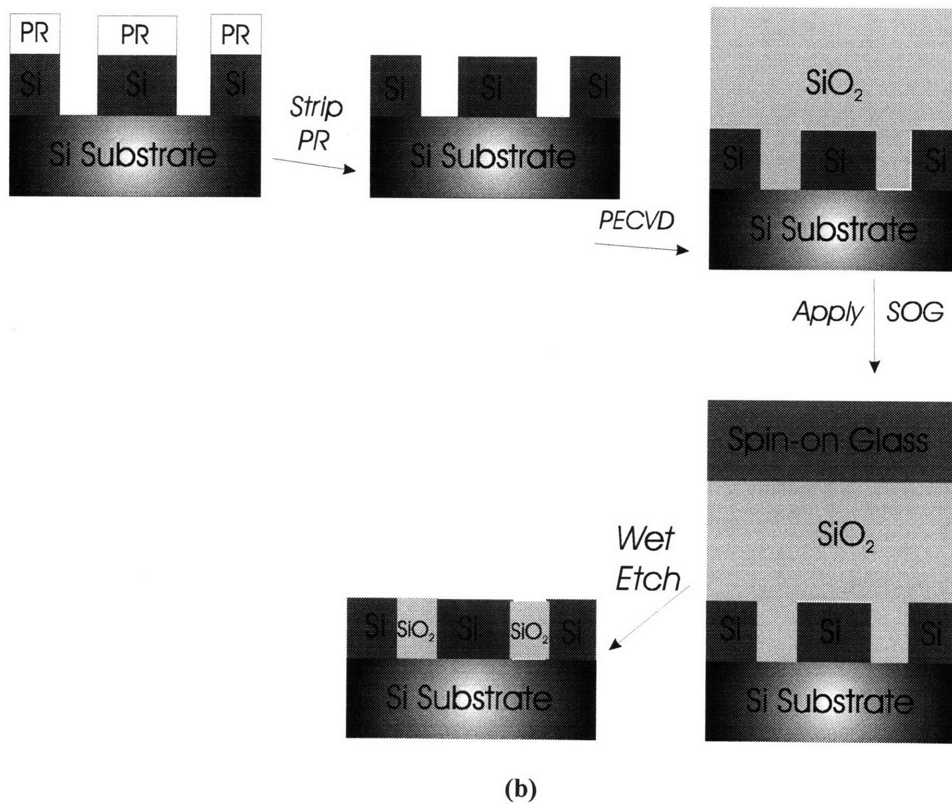


Figure 3.1: Process outline of Generation I.



(a)



(b)

Figure 3.2: Two alternative methods of SiO_2 deposition to fill in the Si trenches: (a) electron-beam evaporation and lift-off and (b) deposition of SiO_2 and spin-on glass (SOG).

the first method, SiO_2 covers the sidewalls of the photoresist making the lift-off of the top SiO_2 quite difficult. Also, a thick photoresist layer prevents SiO_2 from completely filling in the Si trenches. Furthermore, the profile of SiO_2 in the Si trenches is round on top rather than square as designed. The problems of using the second method are: (1) the difficulty of finding a spin-on glass which has the same etch rate as SiO_2 and (2) it is impossible for the wet etch to stop exactly at the top surface of the Si trenches.

CMP is one way to aid the planarization process. Chemical and mechanical polishing (CMP) for planarization has become one of the most rapidly growing segments of the semiconductor industry[21,22]. CMP can provide global planarization across the whole wafer[23,24]. Furthermore, the polishing can be terminated at the surface of an etch stop layer. In this process, a thin layer of Si_3N_4 is used as an etch stop.

3.2 Mask Design:

The schematic of the mask is shown in Figure 3.3. For this device, there are two parameters that are of key importance in the mask design: one is the trench width w, one is the period of trenches a. Corresponding to a midgap frequency of λ = 4.0 μm, the designed w is 0.8μm, whereas a is 2.0μm. One period of the mask is repeated 50 times.

In the mask, we have designed various structures that can be divided into two main groups: one group has fixed length of l = 10μm. The widths of the trenches w are 0.6μm, 0.7μm, 0.8μm, 0.9μm, 1.0μm, 1.5μm, 2.0μm and 3.0μm. The periods of the trenches are 1.5μm, 1.8μm, 2.0μm, 2.2μm, 2.5μm, 3.0μm, 3.5μm and 5.0μm. The other group has w =0.8μm and a =2.0μm, but different lengths l. The l's are 1μm, 2μm, 3μm, 5μm, 10μm, 20μm, 30μm, 50μm, 90μm. The macroscopic view of the layout of the

whole mask is shown in Figure 3.4, where the first group is shown as short lines and the second group is shown as long lines.

The best exposure time and focus depth are determined before the actual process wafers are processed. Special patterns are included on the mask to facilitate this task. In particular, the desired focus can be determined by comparing the mask objects which appear as both dark field and bright field patterns. For instance, the features in Figure 3.5 should all have the same width if the machine is in focus. To decide if a certain exposure time is satisfactory, one would look at the array of squares as illustrated in Figure 3.6. The coloration observed within the squares provides a good indication of whether the photoresist has been exposed to the right extent. Specifically, a pink coloration due to the photoresist will remain within the square patterns that have not been sufficiently exposed. In addition, the squares provide a gauge of the resolution limits in the lithography technique by determining the smallest squares and square separation with the highest pattern fidelity.

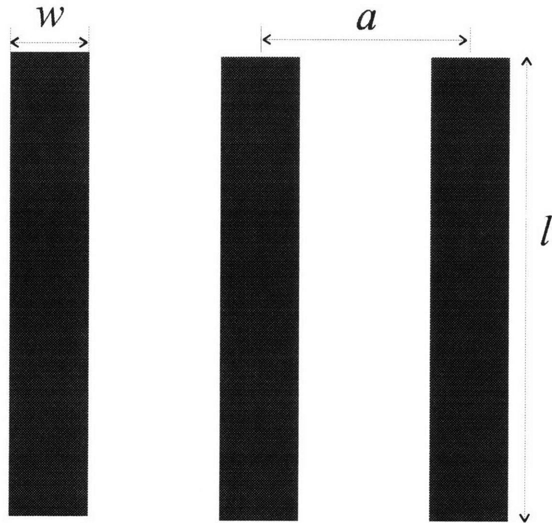


Figure 3.3: Schematic of the mask.

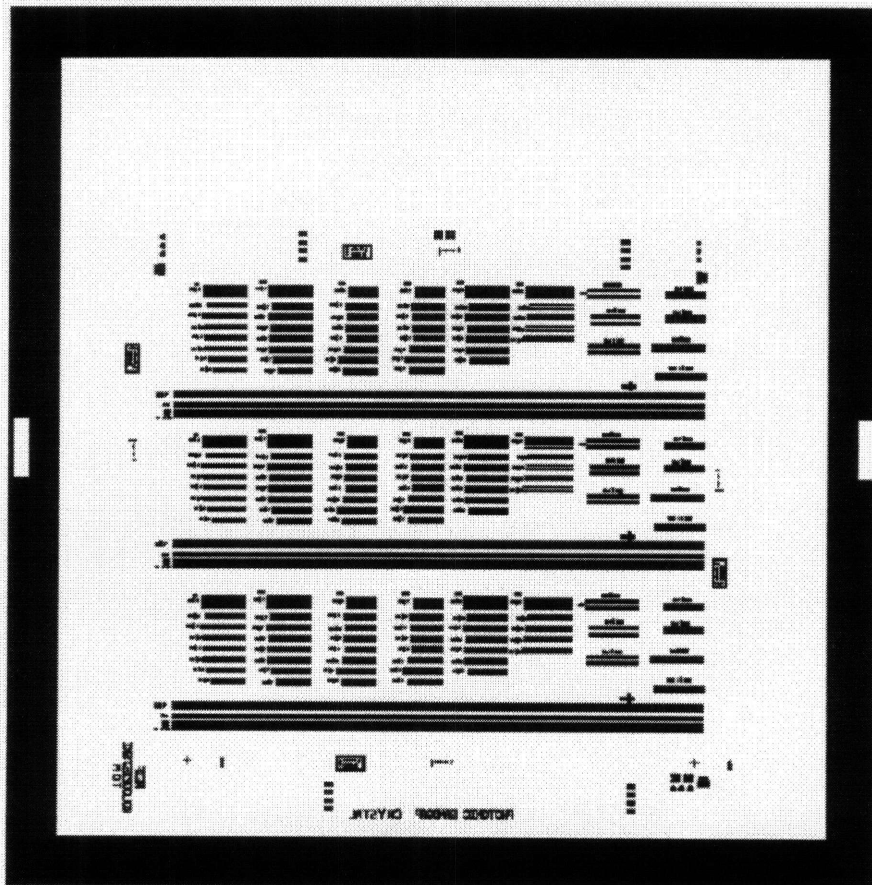


Figure 3.4: A macroscopic view of the layout of the whole mask for Generation I.

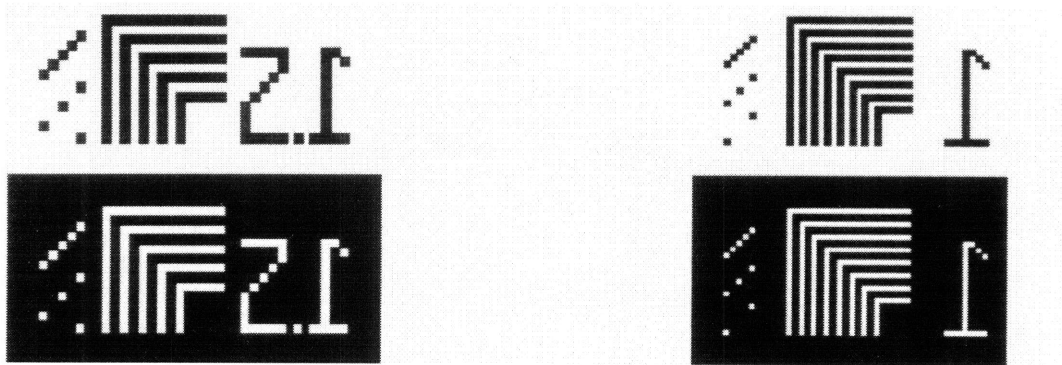


Figure 3.5: Special markers used for achieving the best depth of focus and exposure time.

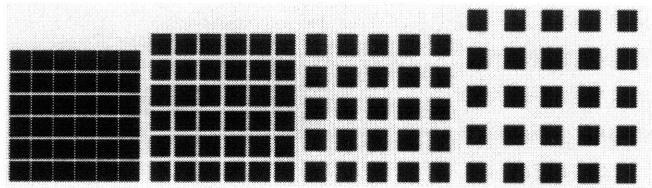


Figure 3.6: A series of squares useful in determining the limits of resolution and adequacy of exposure.

3.3 Define crystalline Si trenches

3.3.1 Using conventional photolithography and plasma etching

Since the dielectric constant for single crystal Si is near that of poly-Si, bare Si wafers (single crystal Si) are processed directly. Therefore Poly-Si is not deposited at the very beginning. Figure 3.7 is a schematic of the process using conventional photolithography and plasma etching to define the Si trenches in a Si wafer. Previously established recipes were first tried. The standard recipes in conventional photolithography

are coating recipe #11 (Table 3.1), and developing recipe #20 (Table 3.2) using standard developer. In plasma etching, recipe #10 (CCl_4 poly-Si etch), which is shown in Table 3.3, was used. In the main etch step, the system pressure is 200mTorr, the incident power is 300watts, and the flows of CCl_4, O_2, and Helium are 130, 20, 70 sccm, respectively. The poly-Si etch rate using recipe #10 is 50Å/second or 3000Å/minute. The nonuniformity across the whole wafer from the mean is ±4%. The etch ratio of poly-Si to photoresist is 2:1, and the etch ratio of poly-Si to oxide is 7:1.

After photolithography and plasma etching, the Si trenches are defined. The results are shown in Figure 3.8 and Figure 3.9. Figure 3.8 is a SEM micrograph of the cross-sectional view of the Si trench. Figure 3.9 is the top view.

It is found that even when the correct dimensions are achieved, the sidewalls are not straight. This problem can be solved using a combination of LTO as a hard mask, special recipes of photolithography, and Cl_2 plasma etching. LTO is more resistant to the dry etch gases than photoresist, which in turn protects the Si underneath the LTO from the attack of etching gases and avoids undercutting. Also special techniques of photolithography are used to create sidewalls of resist as straight as possible. While the etching gases (CCl_4 and O_2) in conventional plasma etching attack Si in both the vertical and horizontal directions, Cl_2 is used to produce straight sidewalls.

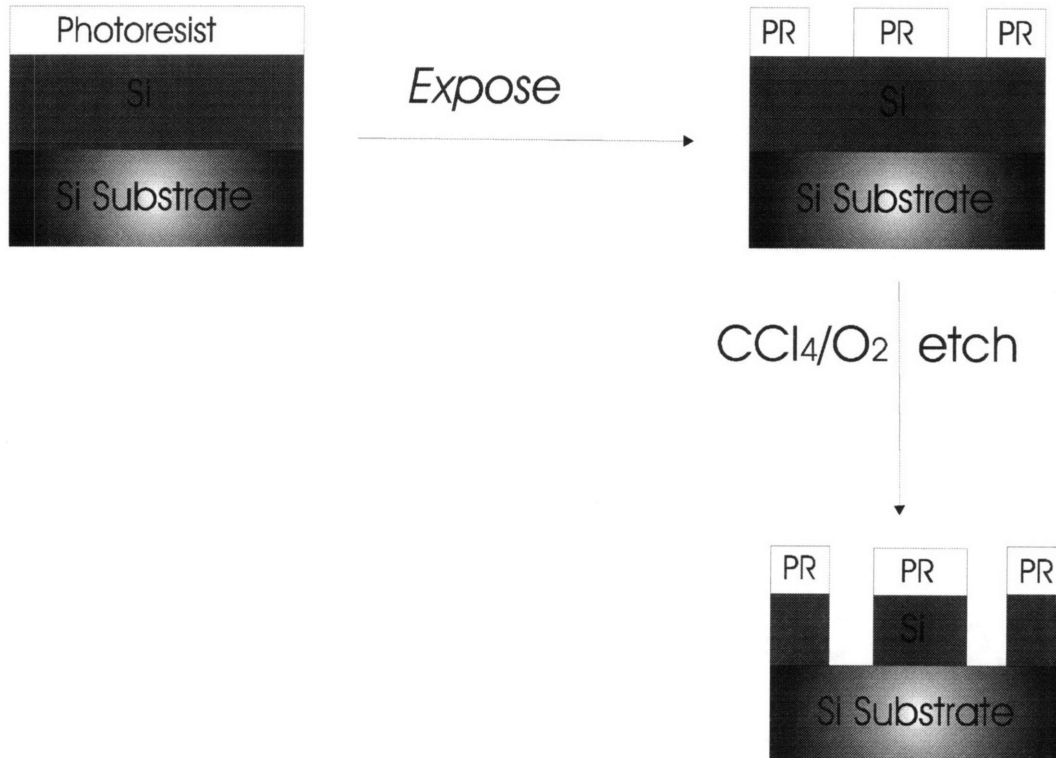


Figure 3.7 Schematic of process using conventional photolithography and plasma etching to define the Si trenches.

Step	Description	Conditions	Time
1	Dehydration bake	200°C	1 sec
2	Resist dispense	3 ml, 0 RPM	4 sec
3	Resist spread	200 RPM/sec, 250 RPM	3 sec
4	Resist spin coat	10000 RPM/sec, 5000 RPM	20 sec
5	Decelerate	-40000 RPM/sec, 900 RPM	2 sec
6	Spin dry	40000 RPM/sec, 2000 RPM	15 sec
7	Stop	-40000 RPM/sec, 0 RPM	1 sec
8	Softbake	115°C	60 sec

Table 3.1: Standard resist coat recipe #11.

Step	Description	Conditions	Time
1	Bake (no heat)	25°C	5 sec
2	DI H_2O wet	10000 RPM/sec, 500 RPM	5 sec
3	Developer spray	500 RPM	2 sec
4	Spin	-200 RPM/sec, 50 RPM	3 sec
5	Develop	0 RPM	10 sec
6	Develop spin off	10000 RPM/sec, 250 RPM	2 sec
7	Develop spray	-200 RPM/sec, 50 RPM	3 sec
8	Develop	0 RPM	30 sec
9	Develop spin off	10000 RPM/sec, 500 RPM	2 sec
10	DI H_2O rinse	800 RPM	15 sec
11	Spin dry	5000 RPM	20 sec
12	Hardbake	130°C	60 sec

Table 3.2: Standard resist develop recipe #20.

	Step #1	Step #2	Step #3	Step #4 (main etch)
Pressure (mTorr)	500	500	200	200
Power (watts)	0	300	0	200
Gap Spacing(cm)	1.5	1.5	1.5	1.5
CCl_4 (sccm)	0	0	130	130
Oxygen (sccm)	200	200	20	20
Helium (sccm)	100	100	70	130
	Stability	Time 6 sec	Stability	Time 3 min

Table 3.3: Recipe # 10 (CCl_4 poly-Si etch).

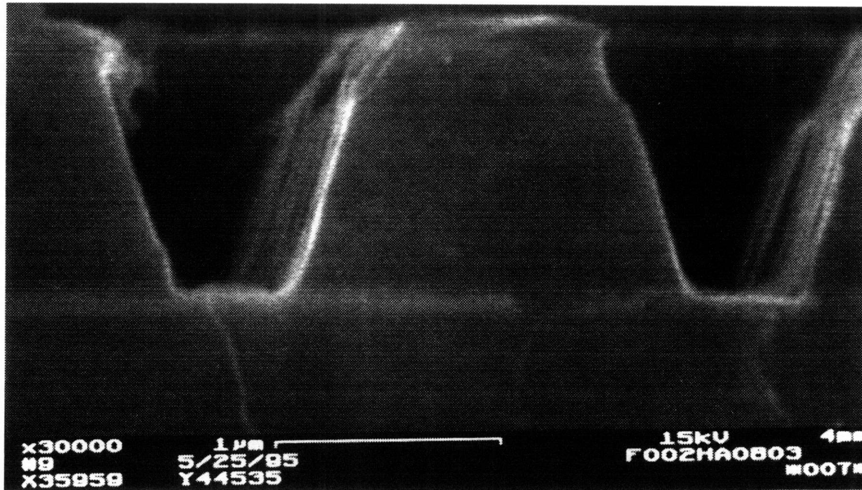


Figure 3.8: A SEM micrograph of the cross-sectional view of Si trenches. (after photolithography and plasma etching).

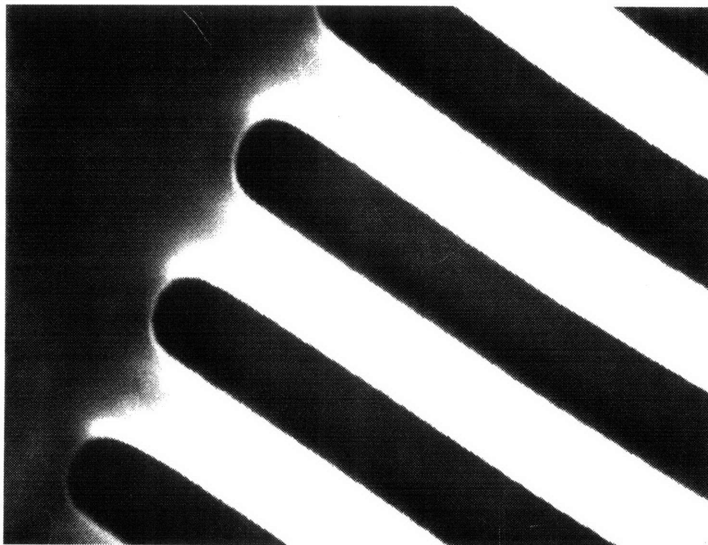


Figure 3.9: A SEM micrograph of the top view of the Si trenches. (The feature size is 0.8µm)

3.3.2 Using LTO as a hard mask and special recipes of photolithography and plasma etching

RCA clean

Before any processing work is carried out on the Si wafers, an RCA clean is performed in order to remove any ionic or organic contaminants. First the wafers are placed in a 5:1:1 DI:NH_4OH:H_2O_2 solution at 80°C for 10 minutes to remove organic contaminants. Then the wafers are placed in the first rinser to rinse off the organic clean solution (4 cycles automatically) and dipped in a HF solution (50:1 H_2O:HF) for 15 seconds to remove the surface oxide. Thereafter, the wafers are rinsed again (4 cycles) and placed in an ionic clean solution of 6:1:1 H_2O:HCL:H_2O_2 at 80°C for 15 minutes. After that, the wafers are rinsed in the second rinser. Finally, the wafer is spun dry in a spin rinser/dryer.

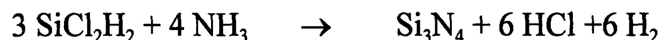
Si_3N_4 deposition

A thin layer of Si_3N_4 is used as an etch stop for the CMP step. A 300Å layer of Si_3N_4 is deposited by low-pressure chemical vapor deposition (LPCVD) in the Integrated Circuit Laboratory (ICL) of the Microsystems Technology Laboratory (MTL) at MIT. A batch of wafers are processed at the same time, and the deposition is performed in an automated furnace (Tube A5). The deposition recipe is #460 (Table 3.4). Since the deposition rate is about 27Å/min, 11 min is required to deposit 300Å. LPCVD Si_3N_4 is

Interval	Description	Time (min)
0	Idle	0
1	Boat in	30
2	Stabilize	7
3-7	Pump and Purge	39
8	Deposit Si_3N_4	11
9-20	Pump and Purge	24.5
21	Purge to atmosphere	11
22	Boat out	30

Table 3.4: LPCVD Si_3N_4 deposition recipe #460.

formed by reacting dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3) at temperature between 700°C-800°C according to the overall reaction:



$$3\ SiCl_2H_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$$

Si_3N_4 depositions by LPCVD are controlled by a large number of deposition parameters including temperature, total pressure, reactant ratios, and temperature gradients in the reactor. In general, LPCVD Si_3N_4 films have a density of 2.9-3.1 g/cm^3, and a dielectric constant of 6. Process parameters are shown in Table 3.5.

ratio	NH_3:$SiCl_2H_2$ = 3:1
Gas Flows (typical Gas)	NH_3 = 150 sccm, $SiCl_2H_2$ = 50sccm
Pressure	0.380 - 0.420 Torr
Temperature	center = 780°C

Table 3.5: Process parameters for Si_3N_4 deposition.

LTO deposition and reflow

The low temperature oxide layer acts as the hard mask for the plasma etching of Si. A 2500Å layer of LTO is deposited by LPCVD. The deposition is performed in Tube A7 using recipe #462 (Table 3.6). Since the deposition rate is about 52 Å/min, a 2500Å deposition requires 48 minutes. The deposition temperature is 400°C and the gas flow rates are : 30 sccm N_2, 31 sccm O_2 and 38.5 sccm SiH_4.

Interval	Description	Time (min)
0	Idle	0
1	Boat in	30
2	Stabilize	10
3-8	Pump and Purge	89
9	Deposit LTO	48
10-17	Pump and Purge	16
18	Purge to atmosphere	20
19	Boat out	30

Table 3.6: LPCVD low temperature oxide (LTO) deposition recipe #462.

The reaction between silane and oxygen forms SiO_2 and hydrogen by a heterogeneous surface reaction. Homogeneous gas-phase nucleation also occurs, leading to small SiO_2 particles that form a white powder on the inner walls of the furnace tube. The deposition rate increases slowly as the temperature is increased between 310 and 450°C. LTO films exhibit lower densities than thermal SiO_2, and have an index of refraction of ~1.44. They also exhibit substantially higher etch rates in buffered hydrofluoric acid (HF) solutions than thermal SiO_2.

LTO films are then annealed (reflow). The reflowing temperature is 925°C. In fact, subsequent heating of LTO films to temperatures between 700-1000°C causes

densification. That is, this step causes the density of the material to increase from 2.1 g/cm^3 to 2.2 g/cm^3, the film thickness to decrease, and the etch rate in HF to decrease. After this step, the schematic of the processing is summarized in Figure 3.10.

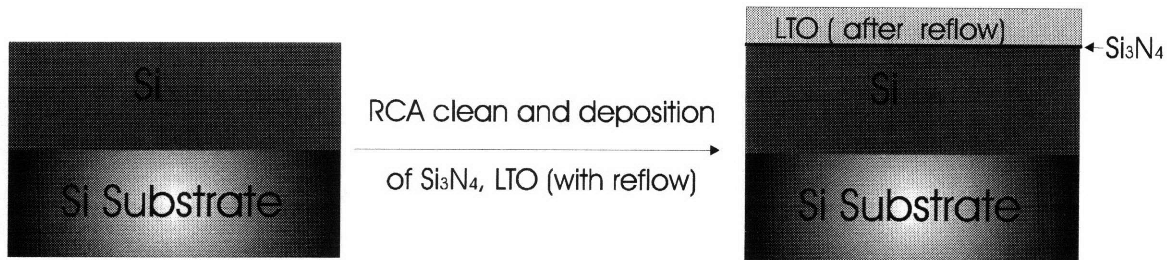


Figure 3.10: Schematic of the processing after LTO deposition (with reflow).

Photolithography

The photolithography step is probably the most critical of all the fabrication steps involved in this project. In particular, the definition of minimum feature size of 0.8μm, pushes the efficacy of optical lithography in MTL. However, in industry, the memory chips have been fabricated with 0.35μm feature sizes.

First, HMDS (Hexamethyldisilazane) is coated on the wafers to improve photoresist adhesion to the LTO layer. A batch of wafers are processed at the same time.

The GCA Wafertrac 1006 coater track automatically coats four inch Si wafers with photoresist and applies both a dehydration bake and a soft bake (or post bake) in a cassette-to-cassette operation. A backside solvent dispense is employed to remove the photoresist heads from the wafer's edge within the spinner module. All ICL coat processes use KTI positive photoresist OCG 820-35CS and OCG PBR1 for edge-bead removal. The "line program" is made up of three "module programs", two for the hotplates (UHP's) #80 and #82 and one for the spinner #112. All line and module

programs are kept in a program subdirectory. The coat program has a target thickness of 11,500Å. The treated wafers are subjected to a brief pre-bake at 200°C for 6 seconds. OCG 820-35CS positive photoresist is spun onto the wafers at 5000rpm for 20s (with an initial dynamic dispense). The coated wafers are then soft-baked for 60 seconds at 90°C.

The pattern transfer is performed with stepper #1 in ICL using a 10× reticule exposing an array of 8 - by - 8 dies (each die has a size of 0.5inch × 0.5inch) on the wafer. Projection printers that step the mask image over the wafer surface are called step-and-repeat systems. With these systems, the mask contains the pattern of one die which is enlarged 10 times. The image of this pattern is demagnified and projected onto wafer. After the exposure of one die, the wafer is moved or stepped on an interferometrically-controlled XY table to the next die, and the process is repeated.

An initial focus-exposure characterization is conducted by varying the stepper focus and exposure parameters across a test wafer. A careful visual examination of the "focus-expo" wafer is carried out with an optical microscope. The pattern that appears to be the most sharply defined and well exposed is selected and provides the focus depth and exposure time that is to be used for the actual process wafers. In the event that the outcome of the photolithography is unacceptable, the photoresist can be removed by the asher and the entire step is repeated.

The printed wafers are brought back to the Wafertrac 1006 where the wafers are developed with the OCG934 developer. The temperature of hot plate UHP84 is set at 110°C. The photolithography step is completed after a post-bake (in UHP86) of 30 seconds at 130°C. Figure 3.11 shows the schematic of the process after photolithography.

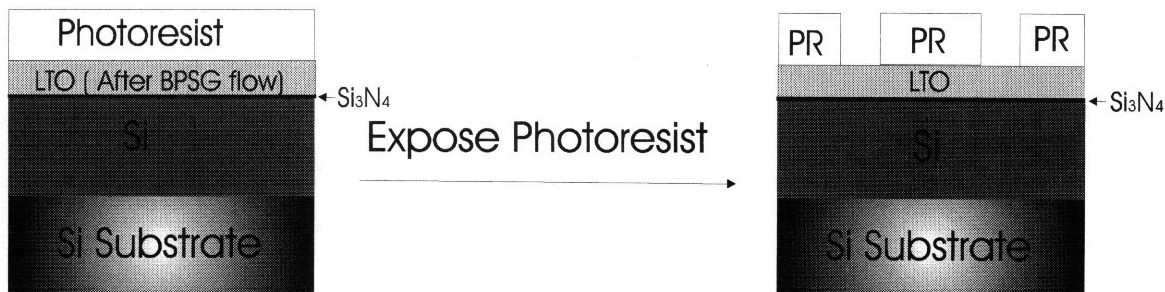


Figure 3.11: Schematic of process after photolithography.

Dry etch of LTO and Si_3N_4

During the dry etch, the incident energetic ions allow the substrate material to be removed in a highly anisotropic manner, so essentially vertical etch profiles are produced.

Etch-2 in ICL is used to perform the LTO dry etch. The etch recipe is #24 (Table 3.7). The descum step has a duration of 10 seconds in order to clear residual photoresist. The last step is set to overetch wafers for 20 seconds to make sure the side walls of the LTO are straight. Using recipe #24, the LTO etch rate is 44 Å/sec, while the resist etch rate is 37 Å/sec. Thus the time of the main etch is 60 sec. In the main etch step, the gas flow rates are 30 sccm for CHF_3, 130 sccm for CF_4, 30 sccm for N_2, 5 sccm for O_2, and 125 sccm for He. The system pressure is set at 3 Torr and an incident power of 900 Watts is used.

Etch-1 in ICL is used to etch the Si_3N_4. The etch recipe is #15 (Table 3.8). Nitride etch rate using recipe 15 is 39 Å/sec. The resist: nitride etch ratio is 1.2:1; while the oxide : nitride etch ratio is 0.4 : 1. The duration of main etch step is chosen as 10 sec. In the main etch step, the gas flow rates are 50 sccm for SF_6 and 20 sccm for Helium. The

system pressure is set at 0.375 Torr and an incident power of 250 Watts is used. Photoresist remains on wafers after this step.

	Descum Step	Main Etch Step	Overetch Step
Pressure	3 torr	3 torr	2 torr
RF Power	100 watts	900 watts	800 watts
Gap Spacing	0.5 cm	0.36 cm	0.4 cm
N_2	0 sccm	30 sccm	0 sccm
O_2	100 sccm	5 sccm	5 sccm
He	200 sccm	125 sccm	60 sccm
CHF_3	0 sccm	30 sccm	10 sccm
CF_4	0 sccm	130 sccm	0 sccm
	Time 10 sec	Time 60 sec	Time 20 sec

Table 3.7: Low temperature oxide (LTO) dry etch recipe #24.

	Step #1	Step #2	Step #3	Step#4
Pressure (mTorr)	500	500	375	375
RF Power (watts)	0	300	0	250
Gap Spacing (cm)	1.5	1.5	1	1
O_2 (sccm)	200	200	0	0
He (sccm)	100	100	20	20
SF_6 (sccm)	0	0	50	50
	Stability	Time (6 sec)	Stability	Time (10 sec)

Table 3.8: Si_3N_4 dry etch recipe #15.

Dry etch of Si (Cl_2 etch)

Plasma etching of Si is performed in Etch-3. The recipe is shown in Table 3.9.

	Step #1	Step #2	Step #3
Pressure (mTorr)	150	150	150
RF Power (Watts)	0	200	0
N_2 (sccm)	10	10	10
Cl_2 (sccm)	50	50	30
$CHCl_3$ (sccm)	0	0	10
Time	Stability	1 min 40 sec	Stability

Table 3.9: Etch recipe of Si (Cl_2 etch)

The duration of step #2 is variable depending on the etch rate. After this step, very little photoresist remains on wafers. Figure 3.12 shows the schematic of the process after the dry etching of LTO, Si_3N_4 and Si.

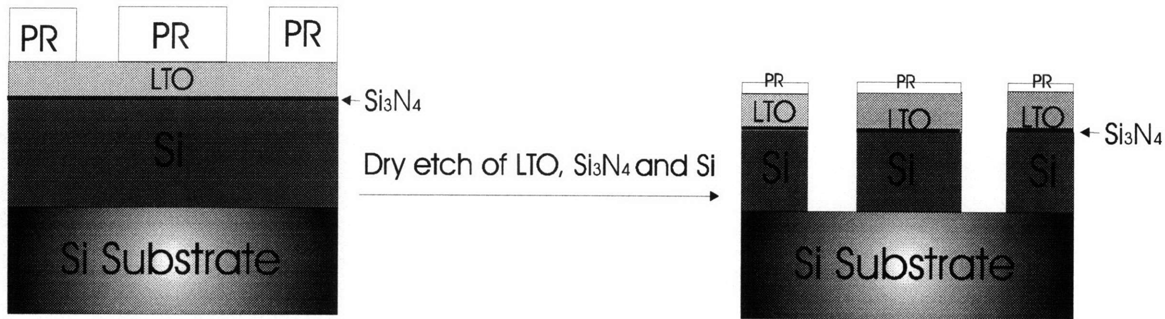


Figure 3.12: Schematic of process after the dry etch of LTO, Si_3N_4 and Si.

Stripping photoresist and oxide

The Drytek plasma asher in ICL is used to remove the photoresist. This is referred to as “ashing”. In plasma ashing, a radio frequency (RF) electric field breaks down the nonreactive gaseous molecules (O_2) into a plasma which contains reactive monoatomic oxygen radicals. The highly reactive radical reacts with the organic polymers in the photoresist to form gaseous products which are readily pumped away. The machine is set automatically. After the cycles start, the chamber will pump down to approximately 40-70 mTorr. A lavender plasma glow can be seen through the front window. The RF power level is typically 950 watts. The whole process takes about 45 min.

LTO is used as a hard mask, so after the etch of Si is finished, LTO should be removed. The wet etch of LTO is performed in the Oxide Strip Station in ICL. An 7:1 (DI:HF) BOE solution is used and the etch rate is 1600 Å/min. So, 2600Å requires 1min 40sec. After the BOE etch, the wafers are rinsed 4 cycles. Finally, the wafers are spun dry in a spin rinse/dryer. Figure 3.13 shows that the Si trenches are defined after photoresist is stripped and LTO is removed.

Figure 3.13: Si trenches are finally defined.

Final results

The following SEM micrographs (Figure 3.14) show that using LTO as a hard mask and special recipes of photolithography and plasma etching produces Si trenches that have straight sidewalls at the desired dimensions.

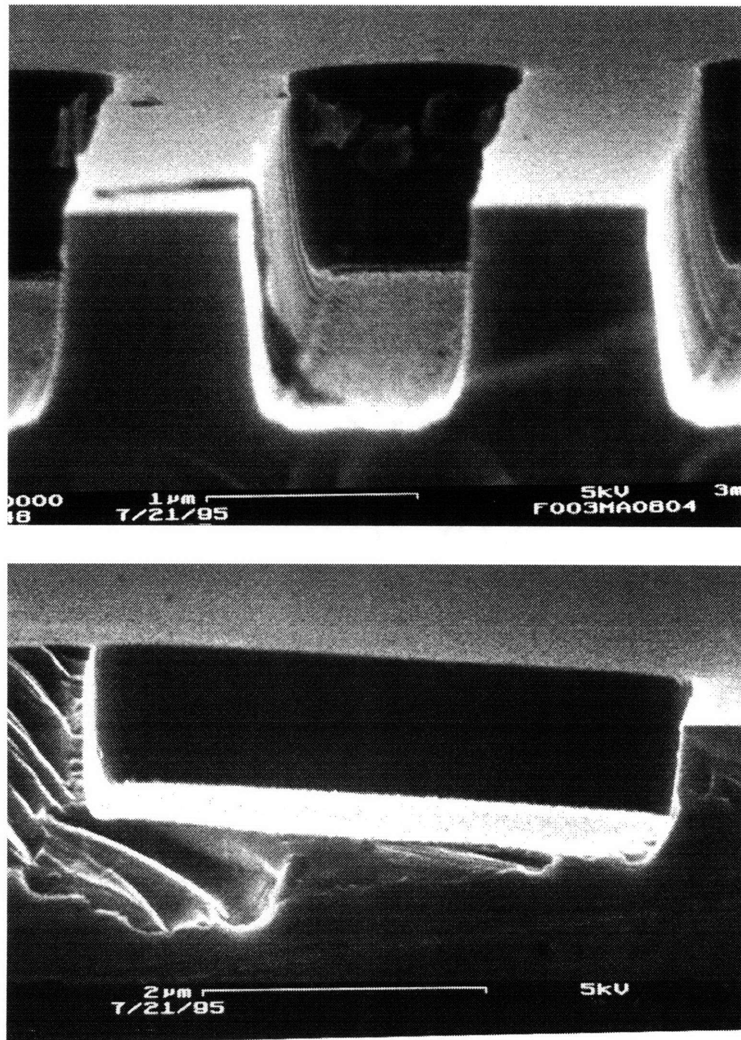


Figure 3.14: Two SEM micrographs of the cross-sectional view of Si trenches. The feature size at the top is 0.8μm. The feature size of the bottom is 3.0μm. It is obvious that these Si trenches have straight sidewalls at the desired dimensions. The depth in both cases is 1 μm.

3.4 Deposition of SiO_2 to fill in Si trenches

The schematic of the SiO_2-on-Si deposition process is shown in Figure 3.15. Three oxide deposition methods can be used to fill in the Si trenches: deposition of LTO, deposition of PECVD oxide, and deposition of borophosphosilicate glass (BPSG)/low temperature oxide (LTO).

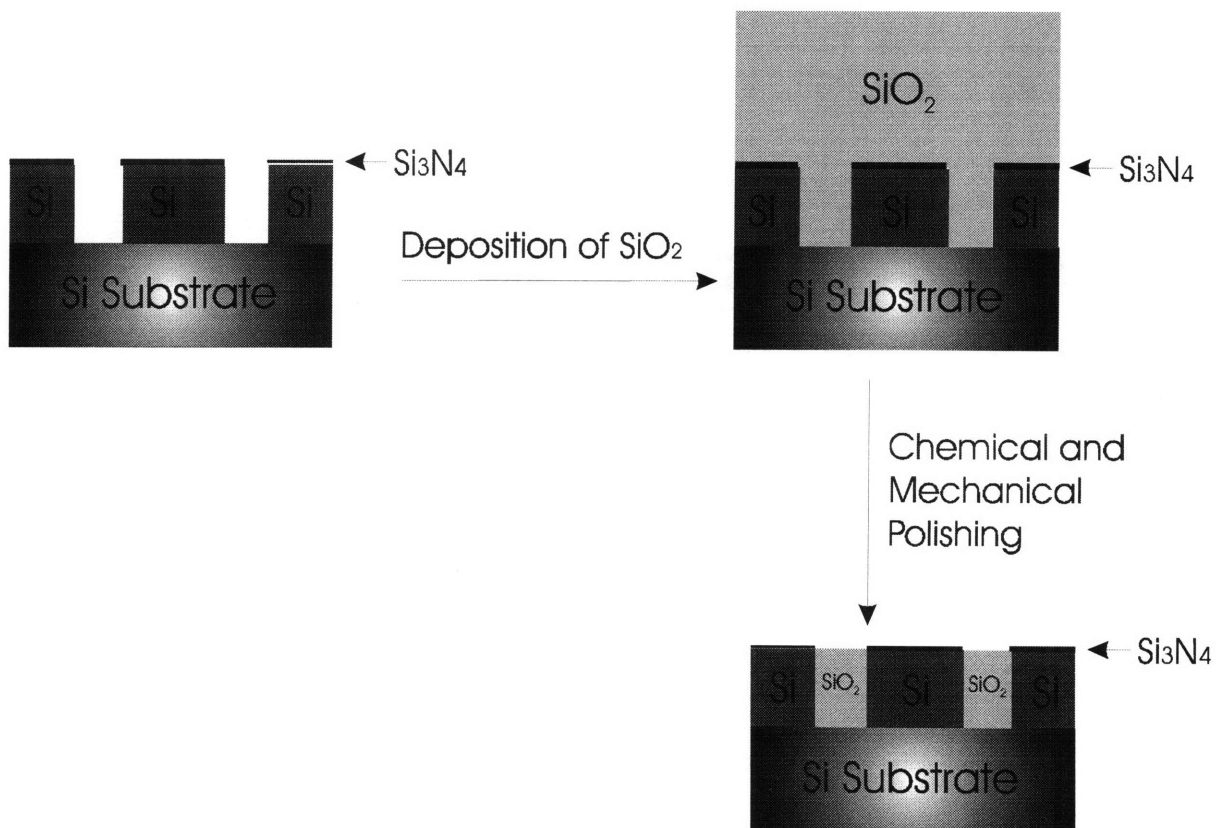
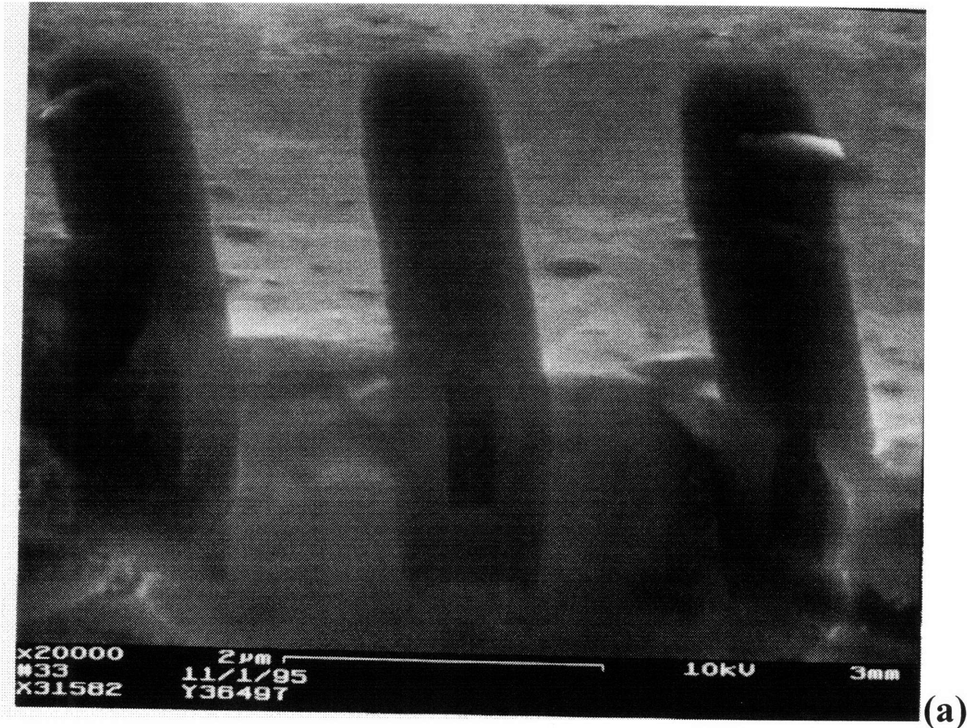


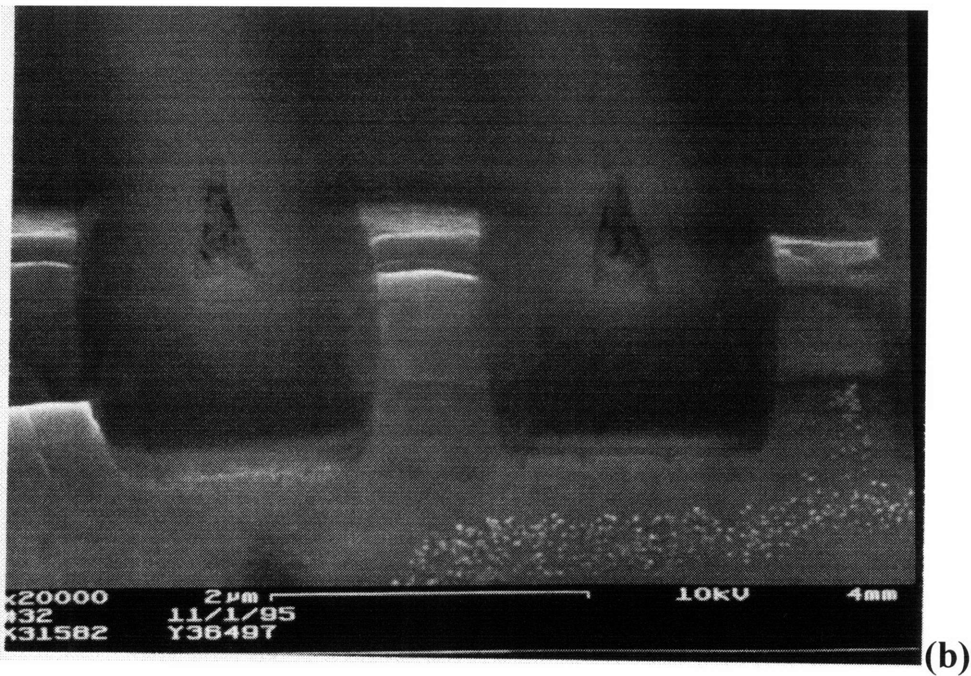
Figure 3.15: Schematic of SiO_2-on-Si deposition process. SiO_2 is deposited and then chemical and mechanical polishing (CMP) is used to planarize the surface.

3.4.1 Deposition of LTO

A 1.5μm layer of LTO is deposited by LPCVD. The deposition recipe is #462 and the deposition is performed in Tube A7. Since the deposition rate is about 52Å/min,



(a)



(b)

Figure 3.16: SEM micrographs of a planarized LTO SiO_2 deposited in Si trenches. Voids in SiO_2 are observed. (a). Cross-sectional view: trenches width = 0.8μm, period = 2μm, depth = 1μm. (b) Cross-sectional view: trenches width = 1.5μm, period = 2.5μm, depth = 1μm. Even with a trench width of 1.5μm, voids are still seen.

1.5μm requires 4 hours and 48 minutes. The results are shown in Figure 3.16 (after CMP).

In Figure 3.16, voids in the SiO_2 are observed. In Figure 3.16(a) with a trench width of 0.8μm, the voids are about 0.3μm. Even in Figure 3.16(b) with a trench width of 1.5μm, voids are still seen. The voids are due to the non-conformal coverage of LPCVD LTO. Conformal coverage means that an equal film thickness exists over all substrate topography regardless of its slope, i.e. vertical and horizontal surfaces are coated with equal film thickness. But due to the low operating pressure of the LPCVD reactor, the mean free path of the reactant gases is high, so that reactant molecules experience few collisions, and follow straight line trajectories over distances comparable to substrate topography dimensions. Substrate surface features near to points that are being impinged upon can block the straight paths of reactant molecules. Thus, such points can be shadowed from the reactant flux, and will experience less deposition, and thus less resulting film thickness, than those points which are not shadowed. Deposition temperature can affect adatom migration. In the LTO case, the low temperatures lead to little surface migration, which causes a more non-conformal coverage. However, due to the rapid surface migration, SiO_2 films prepared by high temperature reaction under LPCVD conditions, exhibit nearly conformal coverage.

3.4.2 Deposition of PECVD oxide

A 1.5μm PECVD oxide deposition is performed in TRL (Technology Research Lab) in MTL. PECVD is a combination of a glow discharge process and low pressure chemical vapor deposition in which highly reactive chemical species are generated from

gaseous reactants by a glow discharge and interact to form a thin solid film product on the substrate and electrode surfaces. The plasma assists or enhances the chemical vapor deposition reaction.

The result is shown in Figure 3.17. The voids are still observed. It seems that even if PECVD produces reactants which arrive at the substrate with more energy (obtained from the glow-discharge), and hence a larger adatom migration length than in LTO, low temperature and pressure in PECVD oxide deposition are enough to cause non-conformal step coverage.

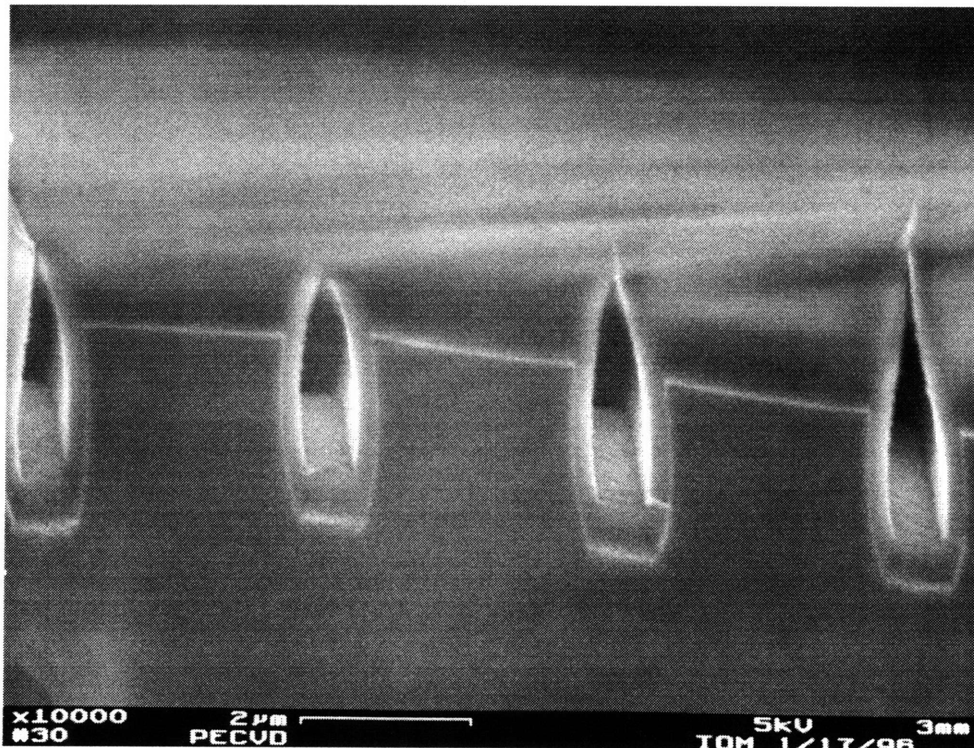


Figure 3.17: SEM micrograph (cross-sectional view): PECVD deposited SiO_2 in Si trenches (trench width is 0.8μm). Voids are still observed.

3.4.3 Deposition of BPSG and LTO

By adding a phosphorus dopant, typically in the form of phosphine, PH_3, and a boron dopant (e.g. B_2H_6) to the gas flow, the ternary oxide system B_2O_3 - P_2O_5 - SiO_2, borophosphosilicate glass (BPSG) is formed. A 1μm borophosphosilicate glass (BPSG) is deposited at ICL in Tube A8.

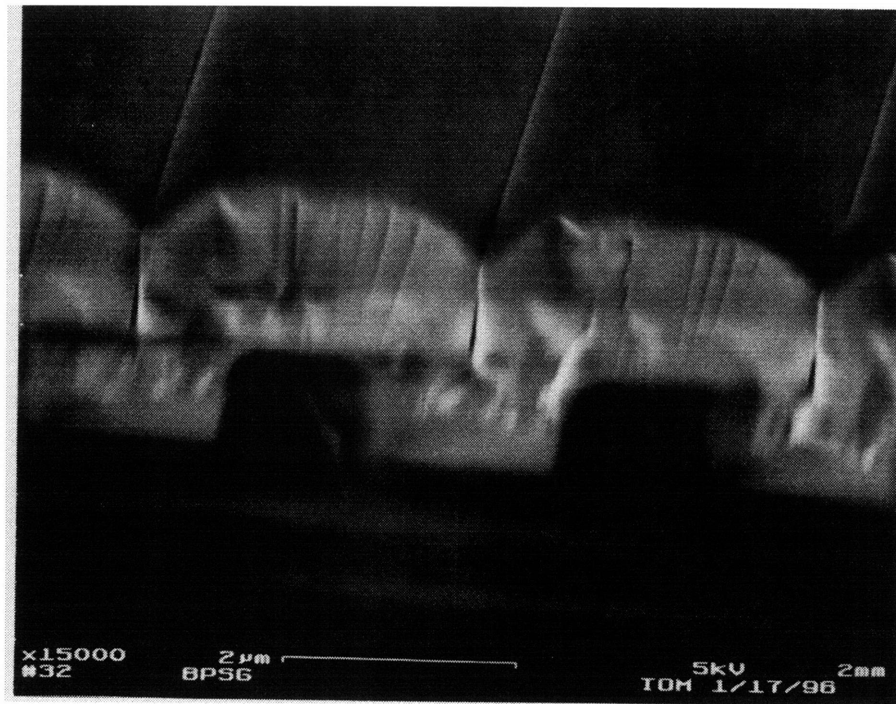


Figure 3.18: SEM micrograph (cross-sectional view): 1μm BPSG/1μm LTO SiO_2 deposited in Si trenches (trench width is 1.5μm).

After that, another 1μm of LTO is deposited in Tube A7 using recipe #462 with a 3 hour 12 minutes deposition time. The result is shown in Figure 3.15 (prior to CMP). The void is not a problem in this case, since the small hole is above the Si surface, which will be polished away by CMP.

BPSG is desirable for easing film coverage over abrupt steps in the substrate topography. Actually, the boron and phosphorus content in the glass composition can be increased within certain constraints to increase the flowability. One thing should be noted that theoretically, following anisotropic etching, Si trenches have sharp upper corners that are difficult to refill. A second thermal flow (reflow) can round these sharp edges, leading to significantly improved coverage of the SiO_2. But reflow in ICL generates a large amount of bubbles that completely destroys the structure. The reason is believed to be due to a BPSG that is too thick. It has been shown that below 0.5μm, the results are acceptable. Since the BPSG reflow step requires thicknesses of less than 0.5μm, BPSG reflow will not be suitable for fabrication of this structure.

3.5 CMP following SiO_2 deposition completes the first layer

3.5.1 Description of CMP

Techniques for planarizing the surface are increasingly important. These are commonly referred to as planarization techniques. CMP is global planarization, which is related to long-range variations in the topology, specifically changes which occur over the entire image field of the stepper. At the present time, CMP appears to be the only route for achieving truly global planarization over the entire substrate for microcircuits with minimum feature sizes below 0.35μm. This approach is conceptually simple. However, the process requires tight control of both the temperature and the pH of the polishing medium in order to maintain a consistent removal rate during the polishing

step, as well as from run to run. With careful control of these parameters, and choice of polishing solution, it is possible to obtain an etch stop action with CMP. In our project, a thin layer (300Å) Si_3N_4 is used as an etch stop. The CMP of silica and siliceous materials such as BPSG requires the use of an abrasive slurry in a solution with hydroxyl groups. Colloidal silica, in a KOH solution, is commonly used for this purpose, although sodium- and potassium-free slurries are also available. A polishing rate of about 750 Å/min is typical during this operation. Elaborate rinsing procedures are necessary for removal of particulate residues from the slurry and the polishing pads, after the CMP operation is completed.

3.5.2 CMP results

The CMP process was first carried out at Lincoln Labs and completed the first layer. Schematic and SEM of a single period 3-D PBG is shown in Figure 3.16 and 3.17, respectively. The Si trenches of these samples are filled in with LTO before polishing. In the later process, LTO is replaced with BPSG due to the demand for conformal coverage of the Si trenches.

Table 3.9 and Table 3.10 show the thickness of remaining LTO on the silicon nitride etch stop layer and the thickness of remaining LTO in the Si trenches, respectively. Figure 3.18 shows clearly the results of CMP.

Wafer Number	Mean	Standard Dev.	Minimum	Maximum
#1	765.99	576.39	0.000	1762.8
#2	821.02	520.84	0.000	1363.3
#3	976.24	506.46	0.000	1580.5
#4	1264.0	860.65	0.000	2670.0
#5	469.72	311.41	0.000	862.58

Table 3.9: The thickness of remaining LTO on the silicon nitride in the field (units of Å).

Wafer Number	Mean	Standard Dev.	Minimum	Maximum
#1	9596.1	830.14	7218.2	10570
#2	9147.9	998.97	7032.0	11123
#3	7945.0	3037.6	21.356	10605
#4	8564.8	3470.2	10.760	11588
#5	8699.3	792.72	6924.5	10052

Table 3.10: The thickness of remaining LTO in the Si trenches (units of Å).

Ideally, CMP would exactly stop at the surface of the thin layer of Si_3N_4. Therefore, the desired thickness of the remaining LTO on the Si_3N_4 is 0, and the desired thickness of the LTO in the Si trenches is 10000 Å. From these tables, it is obvious that the polishing is not uniform. In the last step of this project when all of the oxide is etched away to form the Si/air structure, the fact that LTO is still on top of Si_3N_4 could result in

all of the patterns above the residual LTO layer removed by etching. Variation of the remaining Si trench depth will affect the properties of photonic crystals.

We can solve these problems in the following ways: (1). Prime bare wafers can be used. Prime bare wafers have more parallel surfaces (front and back surfaces) which alleviate the non-uniform polishing problem. (2). A thicker layer of Si_3N_4 can be used. The thicker Si_3N_4 would act as a better etch stop of CMP, and cause less LTO to remain on the top of the Si_3N_4, and less over-polishing of the Si trenches. However, the presence of a thick layer of nitride will affect the optical properties of the structure. From this point of view, a thinner layer of nitride is better. In fact, 300Å Si_3N_4 is chosen as the etch stop of CMP. (3). The patterning area in the field can be reduced. From the data, the uniformity across a smaller area is acceptable. In the masks for generation II, patterns are created only on the center 1 inch × 2 inches.

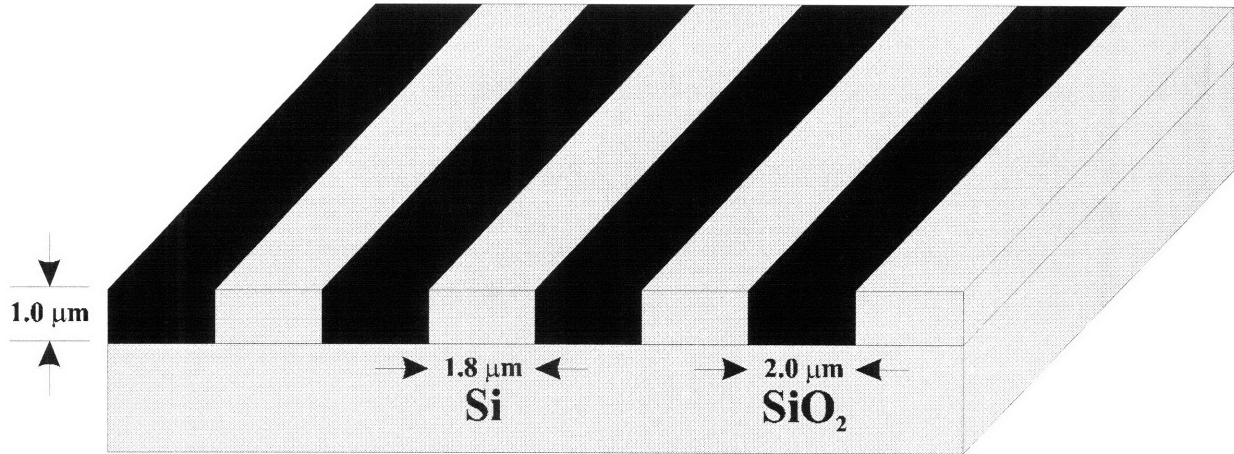


Figure 3.16: Schematic of single period of Si/SiO_2 3-D PBG.

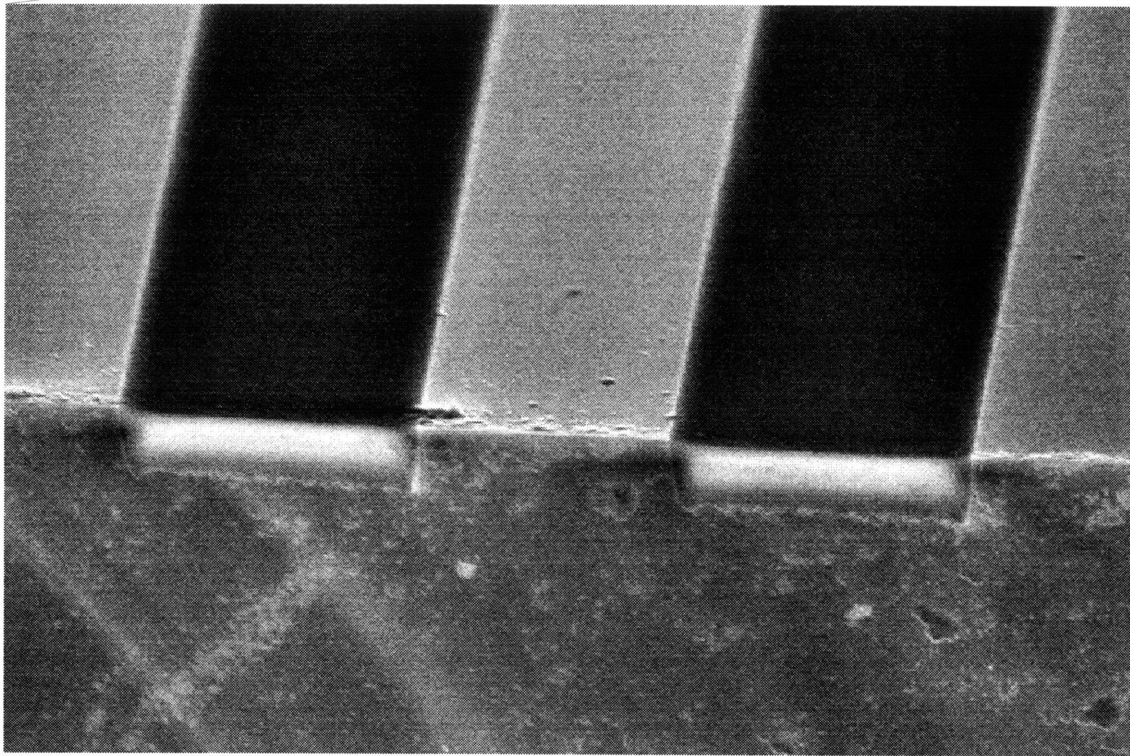


Figure 3.17: SEM of a single period 3-D PBG. Cross-sectional view: trench width=2μm.

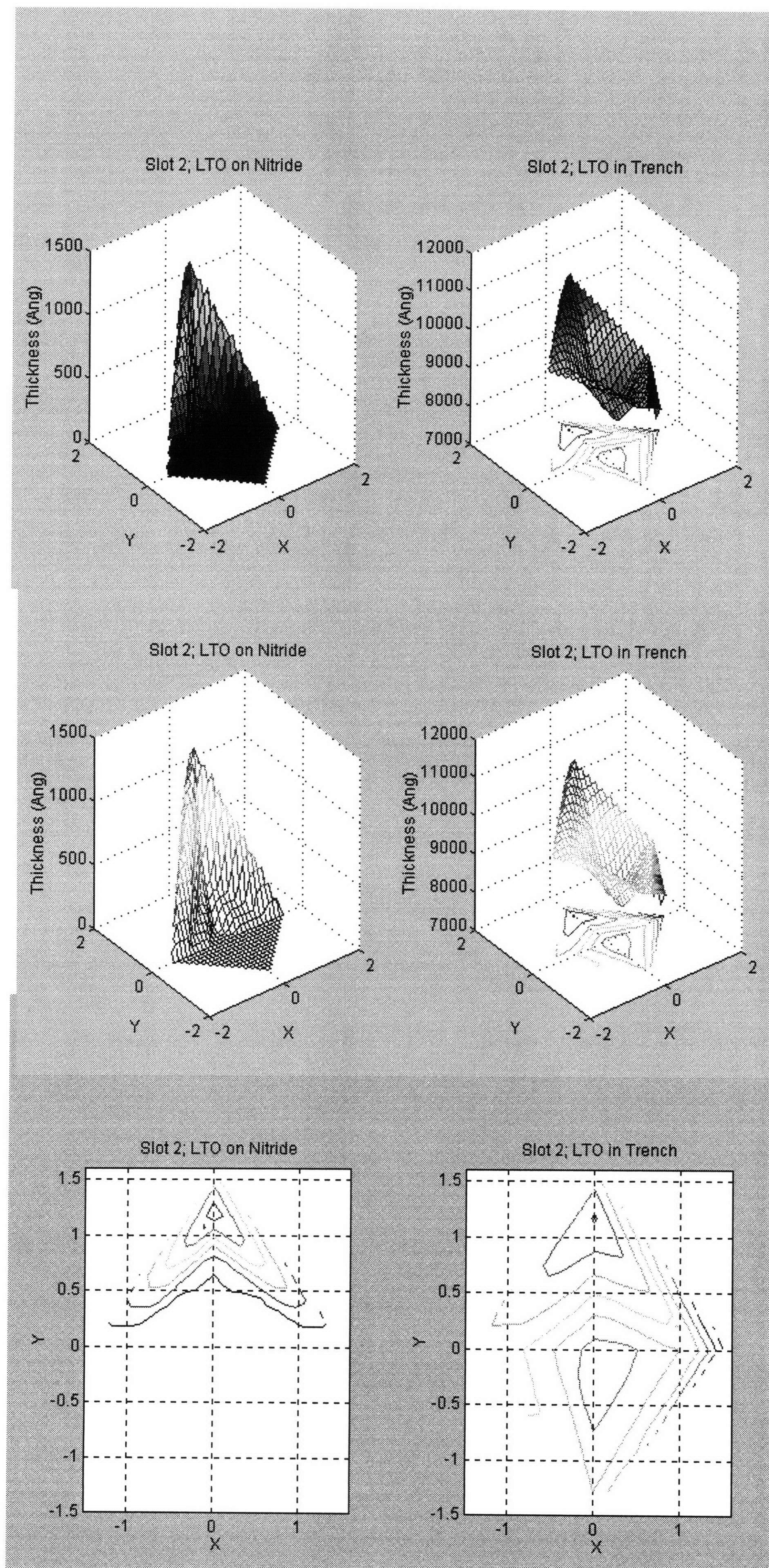


Figure 3.18: The thickness of remaining LTO on nitride and the thickness of remaining LTO in the Si tremches.

3.6 Fabrication of layer 2

Basically, the fabrication process for layer 2 is almost the same as layer one. The only difference is that the alignment between layer 2 and layer 1 is required during the photolithography step. Schematic of process for fabrication of layer 2 is shown in Figure 3.19.

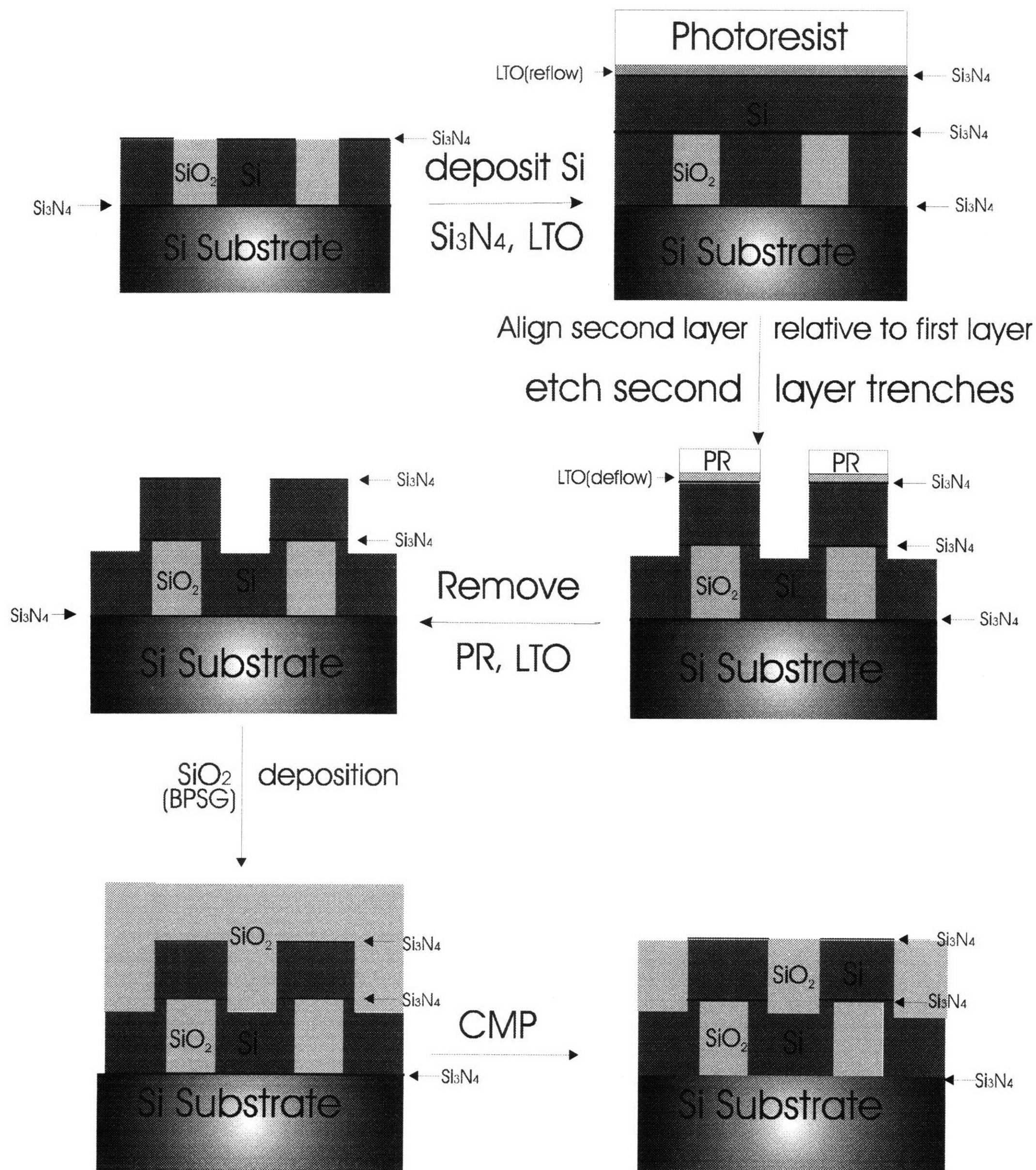
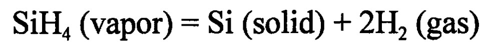


Figure 3.19: Schematic of process for fabrication of layer 2.

3.6.1 Deposition of polysilicon

Deposition of polysilicon is the starting point for the fabrication of layer two. A 0.7μm thick layer of polysilicon is deposited by LPCVD in Tube A6. The deposition recipe is #150 (Table 3.11). The deposition temperature is 580°C. Since the deposition rate is about 31.6 Å/min, 0.7μm requires 3 hour 42 minutes. The deposition reaction is generally given as:



$$SiH_4 \text{ (vapor)} = Si \text{ (solid)} + 2H_2 \text{ (gas)}$$

Some parameters are typical in polysilicon deposition. Gas flow of silane is 150 sccm. Pressure is about 0.250 - 0.260 Torr. And wafer spacing is 0.28 inch.

Interval	Description	Time (min)
0	Idle	0
1	Boat in	30
2	Stabilize	10
3-7	Pump and Purge	53
8	Deposit Poly-Si	222
9-15	Pump and Purge	14
16	Purge to Atmosphere	21
17	Boat out	30

Table 3.11: LPCVD poly-Si deposition recipe #150.

The structure and properties of poly-Si depend on the deposition temperature. At a temperature below 580°C, the as-deposited film is essentially amorphous. At temperatures above 580°C, the deposited film is polycrystalline, with a preferred orientation. It was found that as-deposited amorphous films tend to have smoother surfaces than do films grown at 600°C. The 580°C deposition temperature is chosen to achieve the desired results when Si is plasma-etched. Polycrystalline Si has a larger grain

size which would cause severe undercutting during the etching process. Deposition at 560°C has slower deposition rates and using soft Si is more difficult to achieve straight sidewalls. Another reason to choose 580°C is that poly-Si deposited at 580°C has better uniformity and lower residual stress. Since the PBG structure is very complicated (10 layers) and eventually, all of the SiO_2 will be etched away, to prohibit the collapse of the entire structure, smaller residual stress is highly desirable[22].

3.6.2 Deposition of LTO (reflow) and Si_3N_4

As described before, a LTO layer acts as the hard mask for plasma etching of Si. A 2500Å layer of LTO is deposited by LPCVD. The recipe is #462 and the deposition is performed in Tube A7. Since the deposition rate is about 52 Å/min, 2500Å requires 48 minutes. The reflow step is performed in Tube B6. The recipe is #280 and the process temperature is 925°C.

The thin layer of Si_3N_4 is used as etch stop of CMP. The deposition is performed in Tube A5 using recipe #460. Since the deposition rate is about 27 Å/min, 300Å requires 11 minutes.

3.6.3 Photolithography

After coating with HMDS, photoresist is coated on the wafers. Using the software program to shift the stepper 1μm and the same mask to expose the wafers, we can transfer the patterns required for the second layer. Figure 3.20 and 3.21 show that the photoresist pattern was successfully shifted 1μm relative to the first layer. However, the pattern can not be shifted 1 μm reproducibly. In Figure 3.22, the stepper shift is 0.7 μm, rather than

1.0μm. There are two reasons which can account for this problem: (1) In the projection aligner, the alignment marks are composed of 2μm lines, which are small on the screen, thus a small misalignment (e.g. ±0.1μm) between mask and wafer can not been distinguished. (2) The stepper stage is designed to move to within ±0.15μm of the desired location. So a 0.3μm misalignment in Figure 3.22 is reasonable for the stepper. It is impossible to reproducibly achieve 1μm shift without unacceptably large error. That is the limitation of the machine. Thus other methods of photolithography are required, e.g. use of the contact aligner or the deep UV stepper.

After exposure, recipe #25 is used to develop the wafers, which ends the photolithography step.

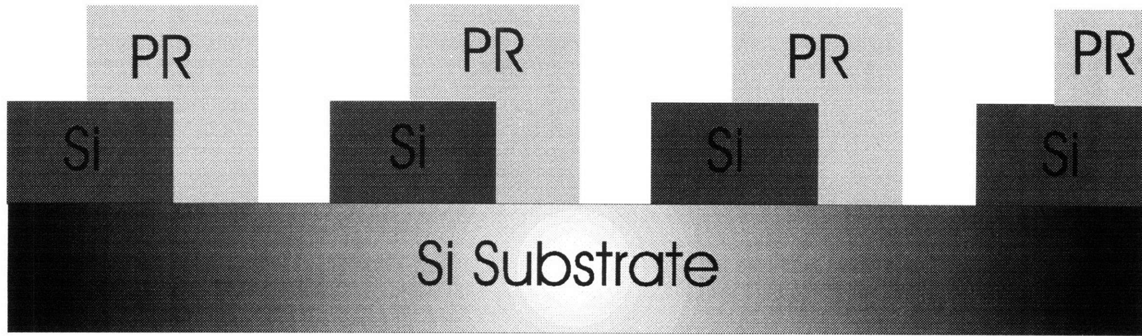


Figure 3.20: Schematic of the second layer photoresist on the first layer Si trenches. The trench width is 2μm.

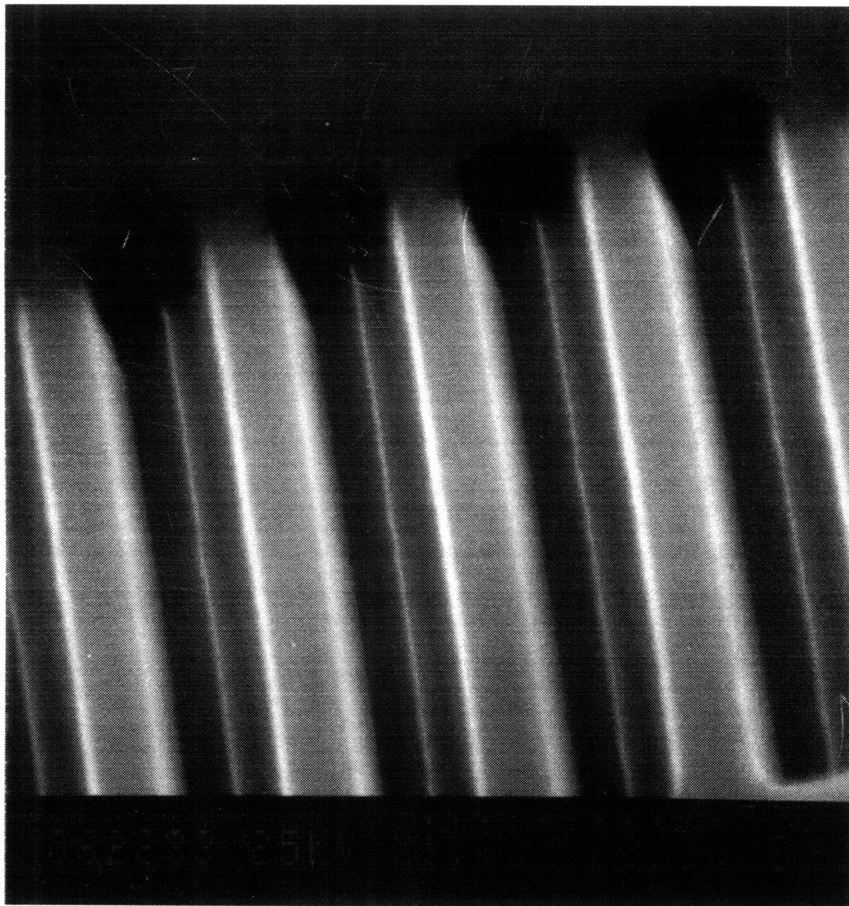


Figure 3.21: SEM micrograph of the second layer photoresist on the first Si trenches. The trench width is 2 μm.

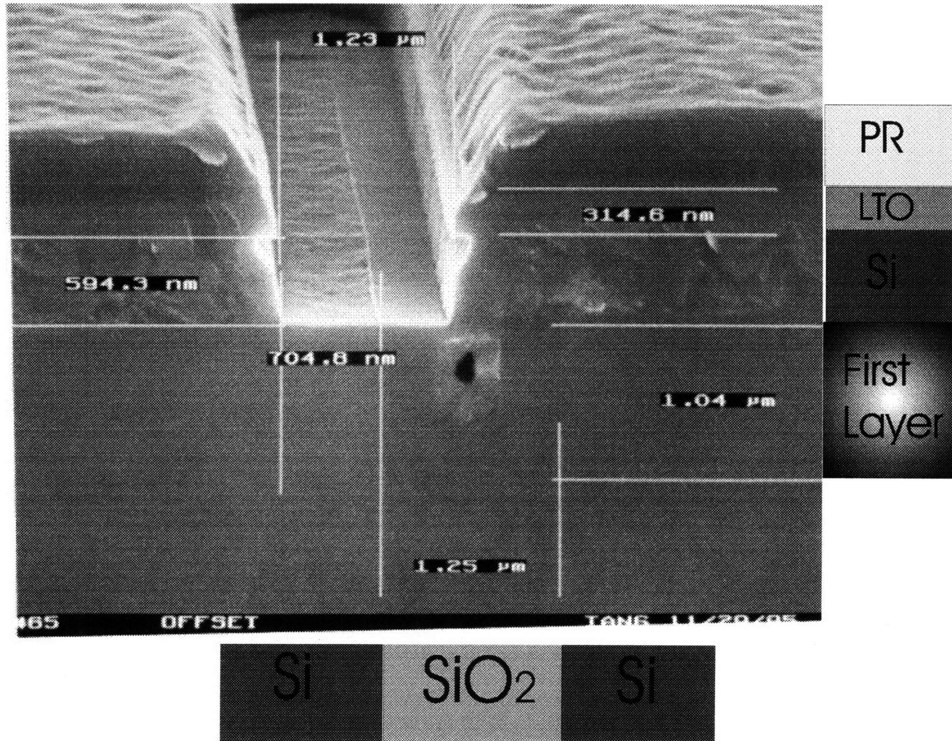


Figure 3.22: SEM micrograph of cross-sectional view: trench width = 1.2μm. The stepper shifted 0.7μm.

3.6.4 Dry etch of polysilicon

The Cl_2 recipe in Table 3.7 is used to etch the polysilicon. The etch is performed in Etch-3. But from Figure 3.22, it is obvious that there is severe undercut in poly-Si layer. The reason is that poly-Si is quite different from single crystal Si. Then we transferred from Etch-3 to AME5000. AME5000 is a RIE (Reactive Ion Etching) machine. Cl_2 etch recipe (poly-Etch-Std) is still used, but with a lower pressure (50 mTorr). The results are shown in Figure 3.23. Now the undercut problem is solved, but the sidewalls are not straight.

The following facts should be noted: (1) Resist would be burned if the incident power level is above 400W. And Higher HBr (hydrogen bromide) gas flow and more power help the etch profile to become anisotropic. (2) Varying pressure between 50mTorr

and 300mTorr has little effect. With Cl_2 : HBR = 50sccm : 50sccm setting, the profile depends on only the power level. The higher the power, the more anisotropic it is.

So the following methods are used to achieve good results of poly-Si etch.

First, etch LTO and Si_3N_4 in AME5000. The etch recipe is Chia-Lun Oxide. Using this recipe, the etch rate of LTO, photoresist and Si_3N_4 is 2500Å/min, 2000Å/min, and 1500Å/min, respectively. In the main etch step, the gas flow rates are 15 sccm of CF_4, 6 sccm of CHF_3, and 80 sccm of Ar. The system pressure is set at 400mTorr and the RF power at 400Watts. Since 2500Å of LTO requires 1 minute and 300Å of Si_3N_4 requires 12 seconds, the duration of main etch is 1 minute 20 seconds.

Then etch Poly-Si in AME5000 and the etch recipe of Chia-Lun Poly. Using this recipe, the etch rate of LTO, polysilicon, single crystal Si and Si_3N_4 is 60Å/min, 5000Å/min, 2000Å/min, and 70Å/min, respectively. In the main etch step, the gas flow rates are 50 sccm of Cl_2, and 50 sccm of HBR. The system pressure is set at 300mTorr and the RF power at 300Watts. Finally, strip resist in the asher and strip LTO oxide in BOE.

The results are shown in Figure 3.24. It is obvious that the poly-Si trenches have straight sidewalls at the desired dimensions. There is one thing that should be noted, the rough bottoms of the trenches can improved by using an etch stop (e.g. Si_3N_4).

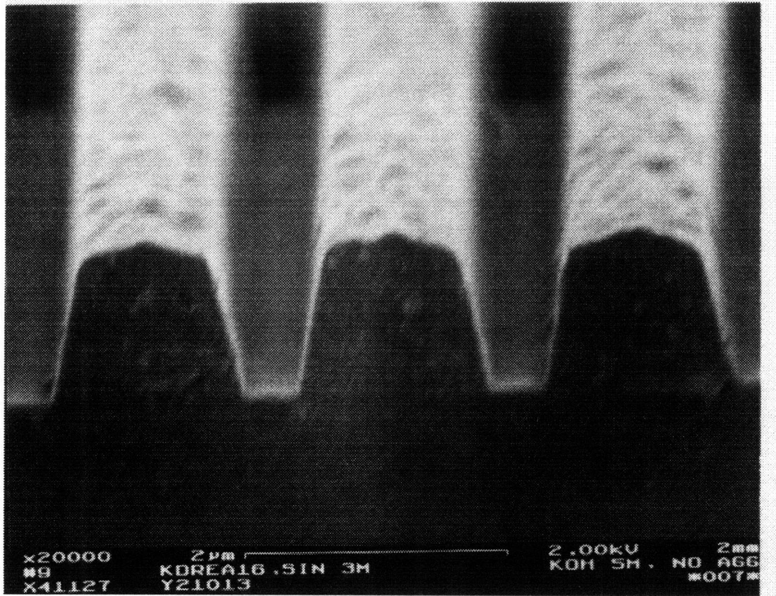


Figure 3.23: SEM micrograph of the cross-sectional view of the poly-Si trenches using the Cl_2 etch recipe.

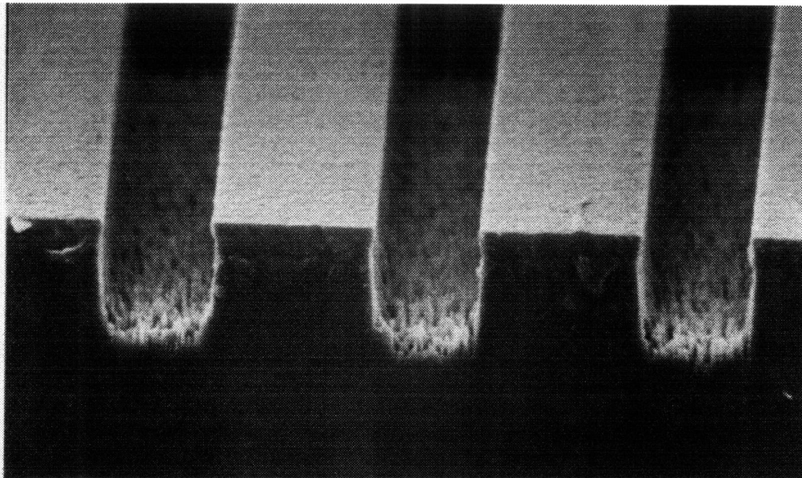


Figure 3.24: SEM micrograph of the cross-sectional view of the poly-Si trenches using the Cl_2/HBr etch recipe.

Chapter 4

Fabrication Process of Generation II

Generation I wafers are monitor wafers to determine the parameters and recipes for the real process of photonic crystals. Generation II wafers are processed for the real 3-D photonic band gap structures. The differences between Generation I and Generation II are: (1) In generation I, the trench width w varies from 0.6μm to 3.0μm, and the trench period a varies from 1.5μm to 5.0μm. While in Generation II, the periods of the trenches a are set at designed numbers and the widths of the trenches w are set at designed numbers with 10% variation. (2) In Generation I, the stepper is used to perform photolithography, while an electron-beam mask and a contact aligner are used to process the photolithography in Generation II. However, Generation II inherits a lot from Generation I, e.g. etch recipes, deposition recipes and parameters, etc.

4.1 Mask design

The macroscopic view of the layout of one unit cell is shown in Figure 4.1. The arrangement of 9 identical unit cells is shown in Figure 4.2. The width of the unit cell is 5.45mm and the length of the unit cell is 12.64mm. The separation between unit cells is 3mm.

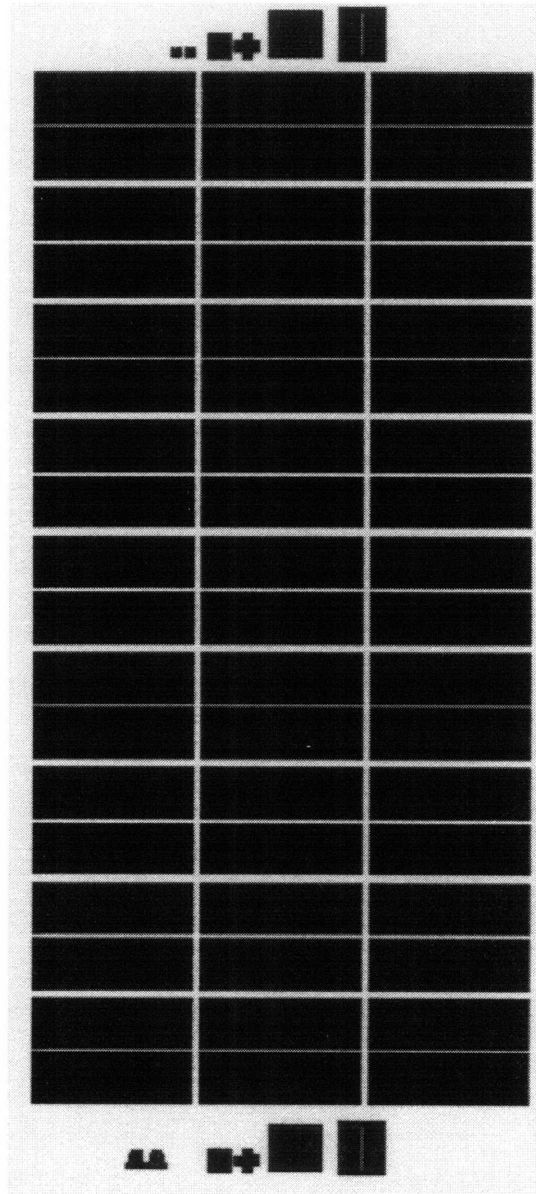


Figure 4.1: The macroscopic view of the layout of one unit cell for the Generation II mask.

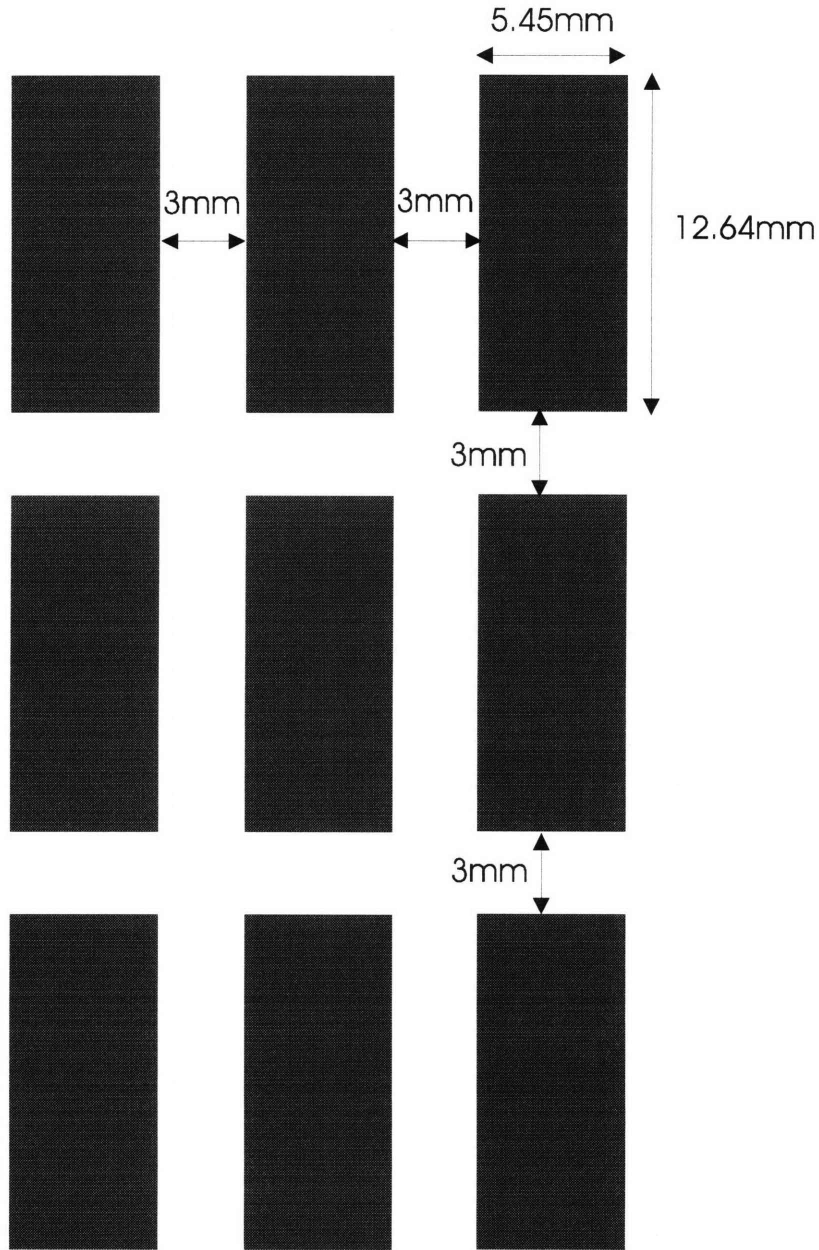


Figure 4.2: The arrangement of 9 unit cells.

For 3-D PBG structures, there are two parameters of key importance in mask design: the trench width, *w* and the period of trenches, *a*. Across the whole mask, *l* is fixed at 550μm. The three parameters *w*, *a*, and *l* are shown in the schematic of the mask (Figure 4.3).

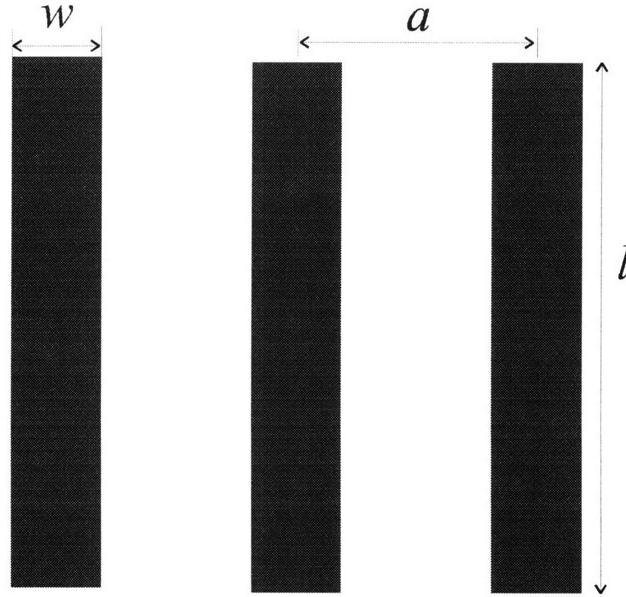


Figure 4.3: Schematic of mask. The three parameters *w, a, l* are shown.

The introduction of an air defect in a perfect PBG crystal can lead to the creation of sharp resonant electromagnetic states. If the size of the defect is properly chosen, a localized state can appear in the gap. In this project, the defects are inserted in layer #5. The arrangement of defects is shown in Figure 4.4. It should be noted that the whole box corresponds to one small box in Figure 4.1. All of the corresponding parameters that are varied in Generation II are shown in Table 4.1, where *w* is the trench width, *a* is the trench period and *r* is the radius of defects.

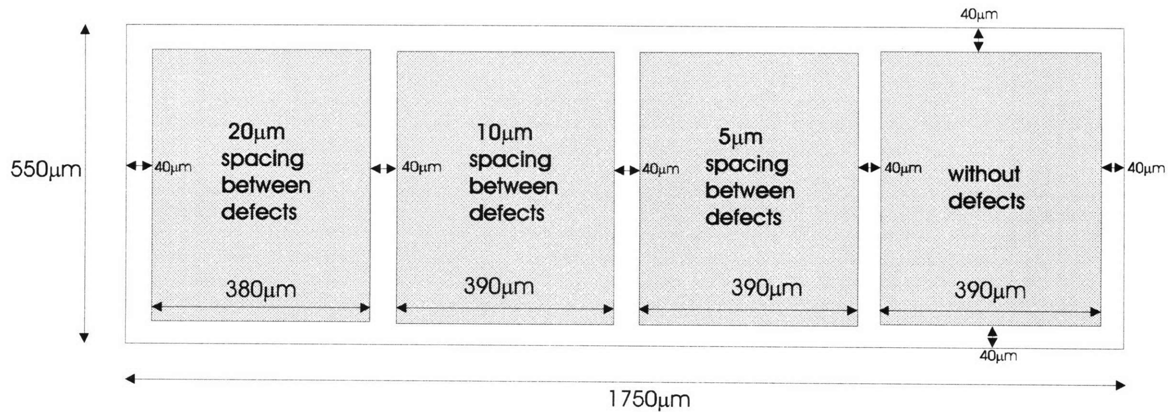


Figure 4.4: The arrangement of defects.

		$r = 0.9r_0$			$r = 1.0r_0$			$r = 1.1r_0$			
midgap frequency	material system	***w*** **(μm)**	***a*** **(μm)**	***r*** **(μm)**	***w*** **(μm)**	***a*** **(μm)**	***r*** **(μm)**	***w*** **(μm)**	***a*** **(μm)**	***r*** **(μm)**	
4.3 μm	Si/air	0.8	2.5	0.45	0.8	2.5	0.50	0.8	2.5	0.55	***w*=** **0.9*w***
	Si/SiO	0.8	2.3	0.65	0.8	2.3	0.70	0.8	2.3	0.75	
	Si/air	0.9	2.5	0.45	0.9	2.5	0.50	0.9	2.5	0.55	***w*=** **1.0*w***
	Si/SiO	0.9	2.3	0.65	0.9	2.3	0.70	0.9	2.3	0.75	
	Si/air	1.0	2.5	0.45	1.0	2.5	0.50	1.0	2.5	0.55	***w*=** **1.1*w***
	Si/SiO	1.0	2.3	0.65	1.0	2.3	0.70	1.0	2.3	0.75	
4.5 μm	Si/air	0.85	2.6	0.50	0.85	2.6	0.55	0.85	2.6	0.60	***w*=** **0.9*w***
	Si/SiO	0.85	2.4	0.65	0.85	2.4	0.70	0.85	2.4	0.75	
	Si/air	0.95	2.6	0.50	0.95	2.6	0.55	0.95	2.6	0.60	***w*=** **1.0*w***
	Si/SiO	0.95	2.4	0.65	0.95	2.4	0.70	0.95	2.4	0.75	
	Si/air	1.05	2.6	0.50	1.05	2.6	0.55	1.05	2.6	0.60	***w*=** **1.1*w***
	Si/SiO	1.05	2.4	0.65	1.05	2.4	0.70	1.05	2.4	0.75	
4.7 μm	Si/air	0.9	2.8	0.50	0.9	2.8	0.55	0.9	2.8	0.60	***w*=** **0.9*w***
	Si/SiO	0.9	2.5	0.70	0.9	2.5	0.75	0.9	2.5	0.80	
	Si/air	1.0	2.8	0.50	1.0	2.8	0.55	1.0	2.8	0.60	***w*=** **1.0*w***
	Si/SiO	1.0	2.5	0.70	1.0	2.5	0.75	1.0	2.5	0.80	
	Si/air	1.1	2.8	0.50	1.1	2.8	0.55	1.1	2.8	0.60	***w*=** **1.1*w***
	Si/SiO	1.1	2.5	0.70	1.1	2.5	0.75	1.1	2.5	0.80	

Table 4.1: The corresponding parameters of all the boxes in Figure 4.1. They are in the same order as in Figure 4.1.

In the mask design, three midgap frequencies 4.3μm, 4.5μm and 4.7μm and two material systems Si/air and Si/SiO_2/air are considered. Also, due to the variation of dimensions during fabrication, the size of defects r and the trench width w vary in the range of 90% to 110% of design size. The design of alignment marks is very important in this project. Three steps of alignment are used: (1) by using complementary alignment crosses shown in Figure 4.5, alignment to within 1.0μm can be achieved; (2) by using the coarse moire marks shown on the right side of Figure 4.6, alignment to within 0.3μm can be achieved; and (3) the fine moire marks shown on the left side of Figure 4.6 can achieve alignment to within 0.1μm. It's worthy to discuss the moire marks. The moire alignment marks consist of gratings with pitches p_1 and p_2 side by side, but with p_1 on the substrate facing p_2 on the mask, and p_2 on the mask facing p_1 on the substrate. In this way, when the mask and substrate marks are imaged, interference fringe patterns (often called a moire pattern, or beat pattern) are formed, having a period p, which is given by $p = \frac{p_1 p_2}{|p_1 - p_2|}$. Figure 4.7 is one part of the first layer of moire marks. For the fine moire marks, in the first layer, the period of the left side is p_1=2.0μm, and that of the right side is p_2=1.9μm; In the second layer, the periods of the left side and right side are p_2=1.9μm and p_1=2.0μm, respectively. Figure 4.8 is the composite of two layers of moire marks. A beat pattern is formed and the beat period is $p = \frac{p_1 p_2}{|p_1 - p_2|}$ = 38μm. So the fine moire marks provide a 20× magnification. So alignment to within 0.1μm is achievable. The two beat patterns on both sides should align with each other.

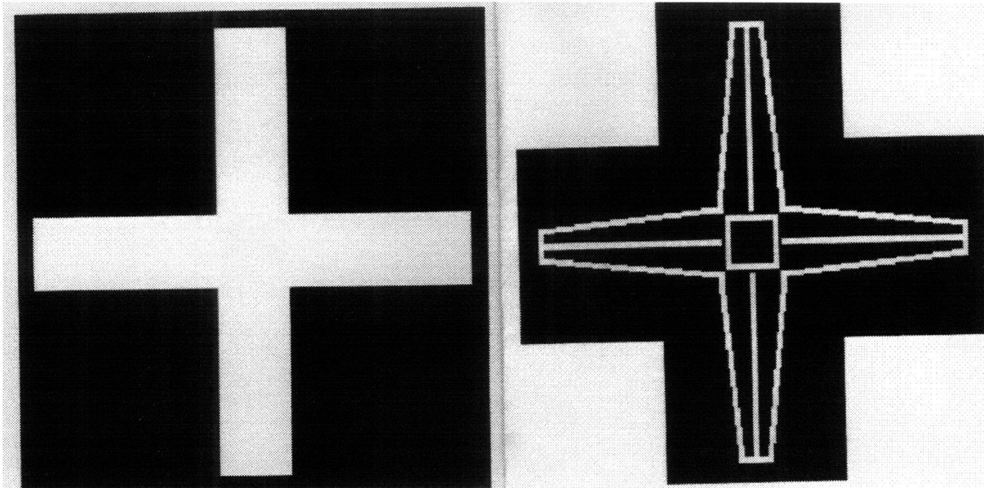


Figure 4.5: Complementary alignment crosses.

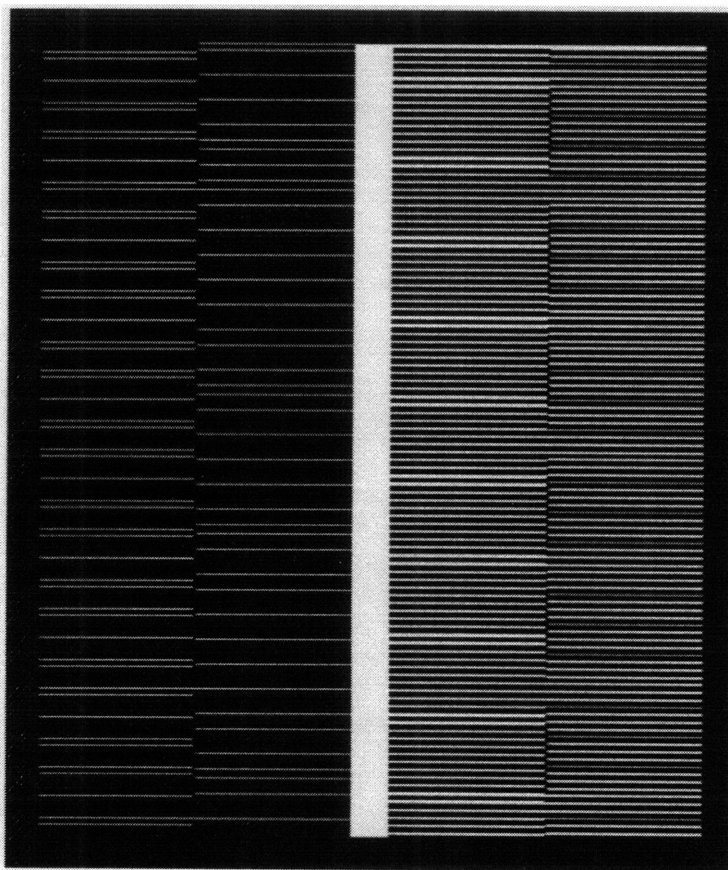


Figure 4.6: Moire alignment marks. The right side is the coarse moire marks and the left side is the fine moire marks.

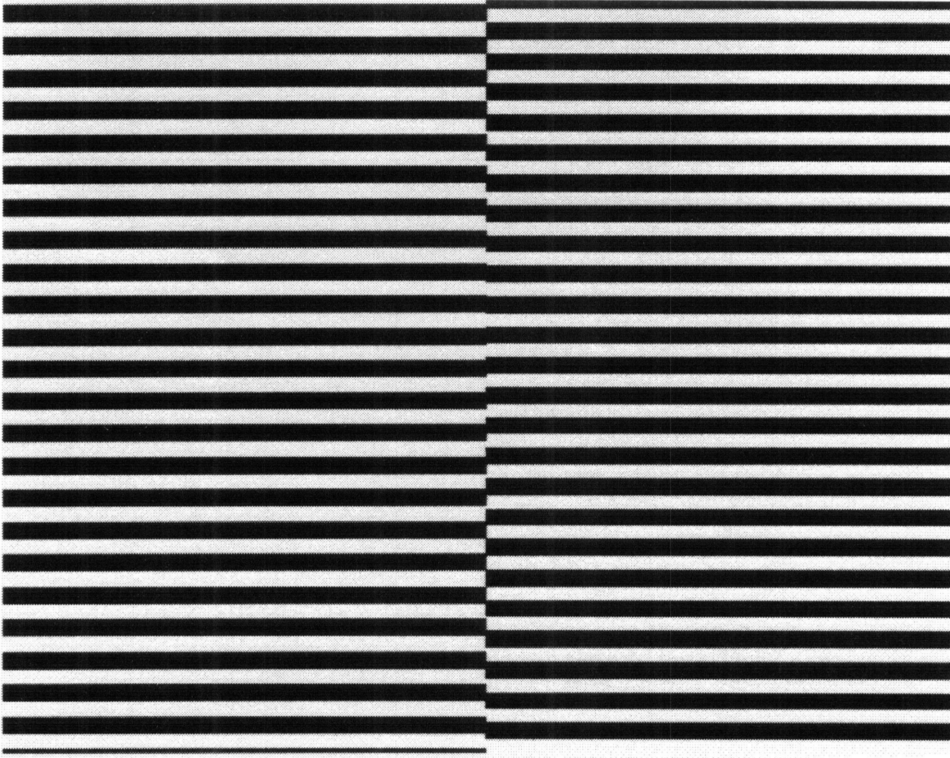


Figure 4.7: One part of one layer of moire marks. The period of the left side is p_1=2.0μm and the period of the right side is p_2=1.9μm.

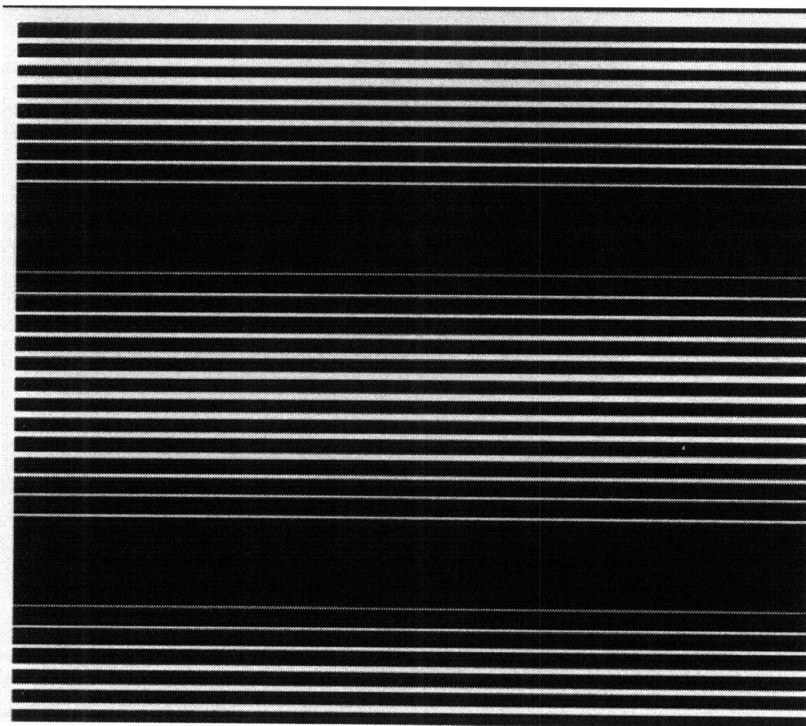


Figure 4.8: The composite of two layers of moire marks. The beat period is 38μm.

4.2 Fabrication process and results

4.2.1 Define polysilicon trenches

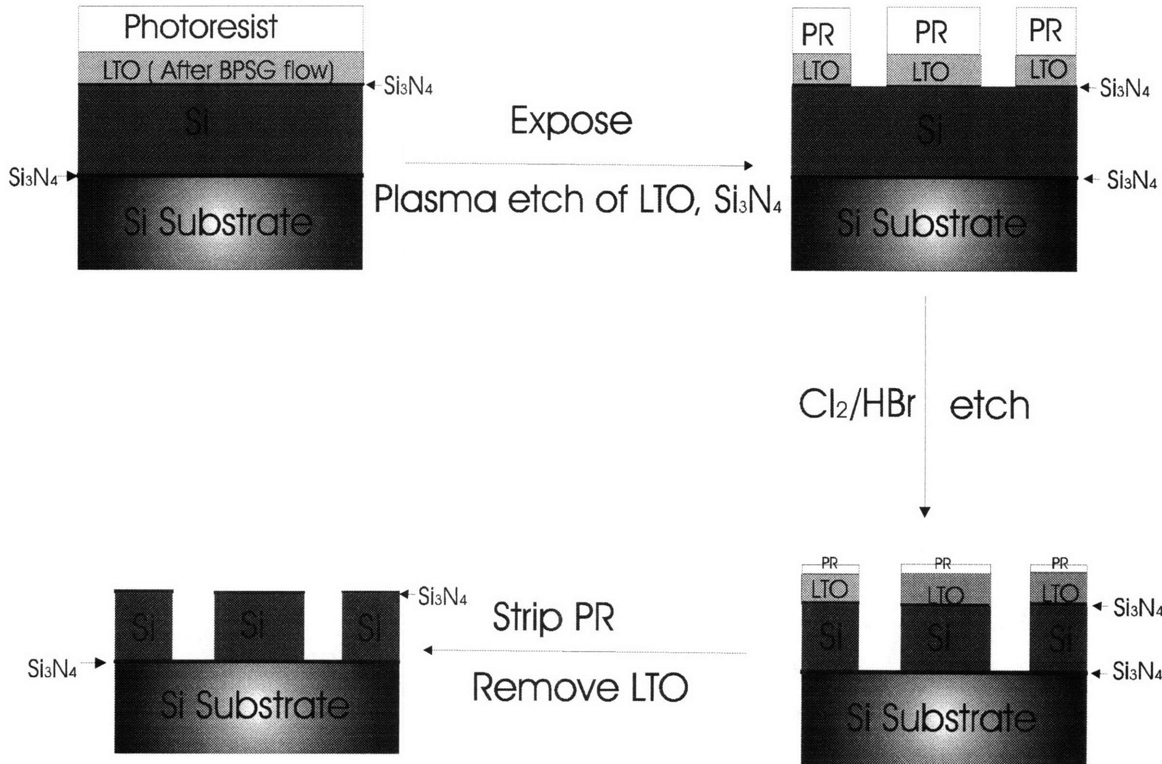


Figure 4.9: Schematic of process to define polysilicon trenches.

Deposition of Si_3N_4, polysilicon and LTO

A thin layer of Si_3N_4 is deposited in Tube A5 with recipe #460. Since the deposition rate is about 27Å/min, 300Å requires 11minutes. The thin layer Si_3N_4 is used as an etch stop for the polysilicon etch.

The polysilicon is deposited by LPCVD in Tube A6 using recipe #150. The deposition temperature is 580°C. In this project, there are two material systems Si/air and Si/SiO_2/air, which require 1.35μm and 1.16μm of poly-Si, respectively. Since the

deposition rate is about 31.6 Å/min, 1.16μm and 1.35μm of poly-Si require 6 hours 7 minutes and 7 hours 7 minutes, respectively.

LTO layer acts as the hard mask for the plasma etching of Si. A 2500Å layer of LTO is deposited by LPCVD. The recipe is #462 and the deposition is performed in Tube A7. Since the deposition rate is about 52 Å/min, 2500Å requires 48 minutes. We process the reflow in Tube B6 using recipe #280 and a temperature of 925°C.

The thin layer of Si_3N_4 is used as an etch stop for the CMP. The deposition is performed in Tube A5 using recipe #460. Since the deposition rate is about 27 Å/min, 300Å Si_3N_4 requires 11 minutes.

Photolithography

First, HMDS is coated on the samples to improve photoresist adhesion to the LTO layer. Then Shipley 1808 positive photoresist is coated on the sample, and the coating parameters are: (1) in spreading step, the duration is 6 sec and the speed is 750rpm and (2) in spinning step, the duration is 30s and the speed is 4000rpm. The expected thickness of photoresist is 7700Å. The coated wafers are then prebaked at 90°C for 30 mins.

The pattern transfer is performed with Karl-Suss MA4 Aligner. Hard vacuum contact and exposing parameters 2s expose-4s wait-15 cycles (at 6.0mW power) are used. There is one thing should be noted that the number of cycles will change from time to time, so always use testing wafers to achieve the most suitable cycle number at that time.

The printed wafers are placed in MF319 developer for 1 min. After rinsing in cascade rinser and blowing dry wafers with N_2 gun, inspect samples under microscope to

make sure the results are reasonable. Postbaking at 120°C for 20 mins finishes the photolithography step.

Dry etch of LTO and polysilicon and wet etch of Si_3N_4

The following techniques are used to achieve desired results using plasma etches.

1. Etch LTO in AME5000. The etch recipe is ISABELS LTO (Table 4.2), which is shown in Table 4.1. In the main etch step, the gas flow rates are 15 sccm of CF_4, 10sccm of CHF_3. The system pressure is set at 200mTorr and the RF power at 350Watts. Since 2500Å of LTO requires 130 seconds, the duration of main etch is 130 seconds.

Step	Time (sec)	Pressure (mTorr)	Power (Watt)	Magnet Field (Gauss)	Gas Name and Flows
1. Stability	10	100	0	0	O_2 (45sccm)
2. Descum	6	100	150	90	O_2 (45sccm)
3. Stability	10	200	0	90	CF_4 (15sccm) CHF_3 (10sccm)
4. Main Etch	130	200	350	90	CF_4 (15sccm) CHF_3 (10sccm)

Table 4.2: Process recipe (ISABELS LTO) for LTO etch.

2. Use Piranha (1 : 3 H_2O_2 : H_2SO_4) to strip photoresist (10 min). After that, the wafers are rinsed in the rinser (4 cycles) and spun dry in a spin rinser/dryer.

3. If the wafers are not processed for more than several hours, put them back to AME5000 and use ISABELS LTO recipe again (5 seconds) to clear the thin layer of oxide.

4. Wet etch the thin layer of Si_3N_4 using Transetch-N solution, which is a special reagent derived from orth-phosphoric acid and can selectively etch Si_3N_4. Etching 300Å of Si_3N_4 requires 5 minutes.

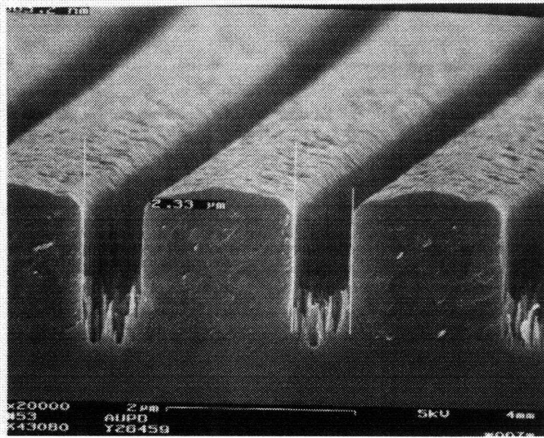
5. Etch Poly-Si in AME5000 and the etch recipe of UNDOPED-POLY-ETCH, which is shown in Table 4.3. In the main etch step, the gas flow rates are 20sccm of Cl_2, 20sccm of HBR, and 10sccm NF_3. The system pressure is set at 200mTorr and the RF power at 350Watts. Since the etch rate of poly-Si is about 1.1μm/min, 1.16μm of poly-Si requires about 1 min. Adding 10 sec over-etch, the duration of main etch is set at 70 sec.

Step	Time (sec)	Pressure (mTorr)	Power (Watt)	Magnet Field (Gauss)	Gas Name and Flows
1. Stability	10	200	0	50	Cl_2 (20sccm) HBR(20sccm) NF_3 (10sccm)
2. Main Etch	70	200	350	50	Cl_2 (20sccm) HBR(20sccm) NF_3 (10sccm)

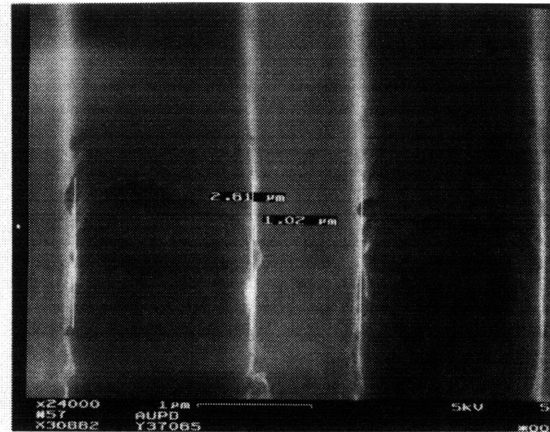
Table 4.3: Process recipe (UNDOPED-POLY-ETCH) for poly-Si etch.

6. Finally, strip LTO oxide in BOE. A 2500Å of LTO requires 1 min 30sec.

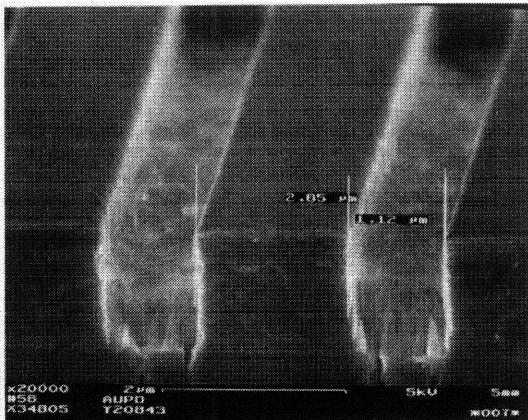
The final results using the above methods are shown in Figure 4.11. Figure 4.10 shows the results using the methods described in Section 3.6.4. Different exposure time (or cycles) are chosen in Figure 4.10. Figure 4.10(a) and (b) are a bit underexposed, while (d) is a bit overexposed. So we chose (c) with 15 cycles, or 30 seconds as the right exposure parameter. Comparing Figure 4.10 with Figure 4.11, it's obvious that Figure 4.11 is much better than Figure 4.10 The new etching methods which described in this section can not only produce smooth bottom, better sidewalls, but also control the etching very well. From the microscope, the old methods will make the wafers black and rough; while the new methods will produce white and smooth surface.



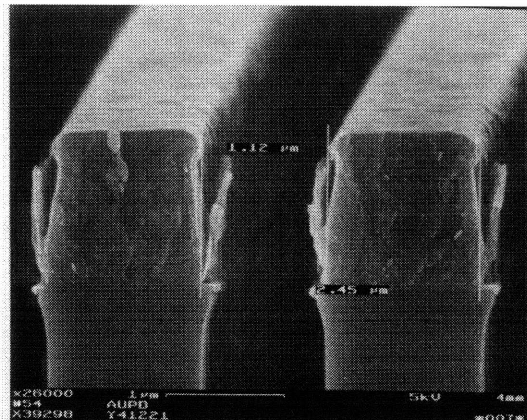
(a)



(b)

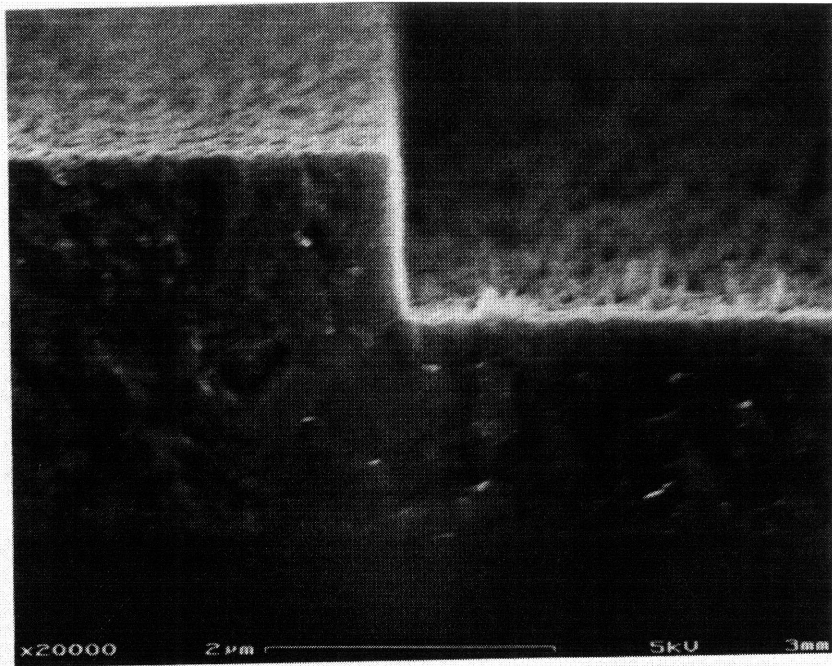


(c)

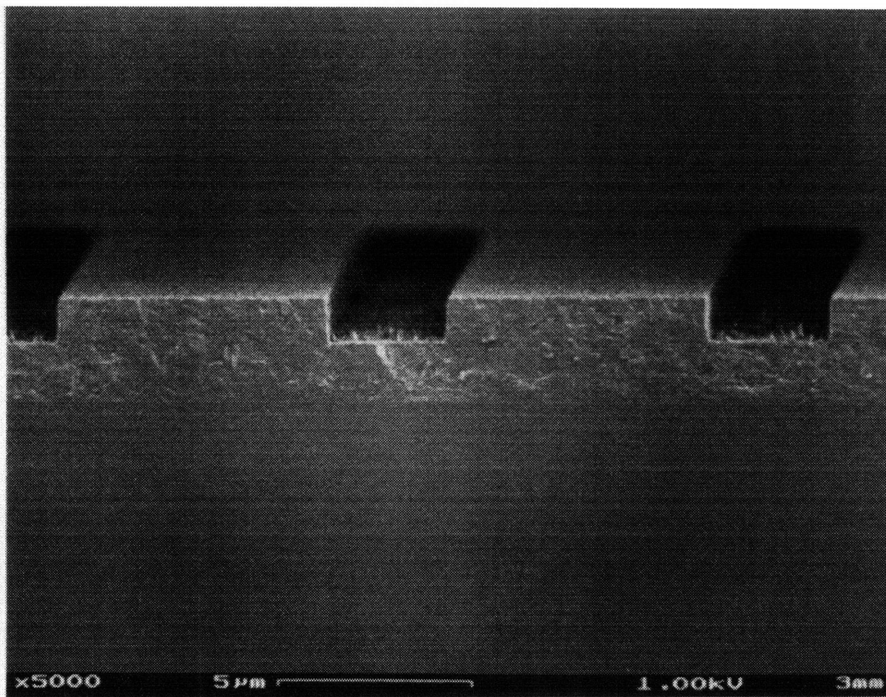


(d)

Figure 4.10: SEM micrographs of the cross-sectional view of poly-Si trenches: (a) has 8 exposure cycles (16 seconds); (b) has 12 exposure cycles; (c) has 15 exposure cycles; and (d) has 18 exposure cycles.



(a)



(b)

Figure 4.11: SEM micrographs of the cross-sectional view of poly-Si trenches using new etching methods which are described in Section 4.2.1.

4.2.2 Deposition of SiO_2 to fill in poly-Si trenches

A 2μm layer of BPSG is deposited in Tube A8 using recipe #780. CMP is used to planarize the surface. The schematic of process is shown in Figure 4.12.

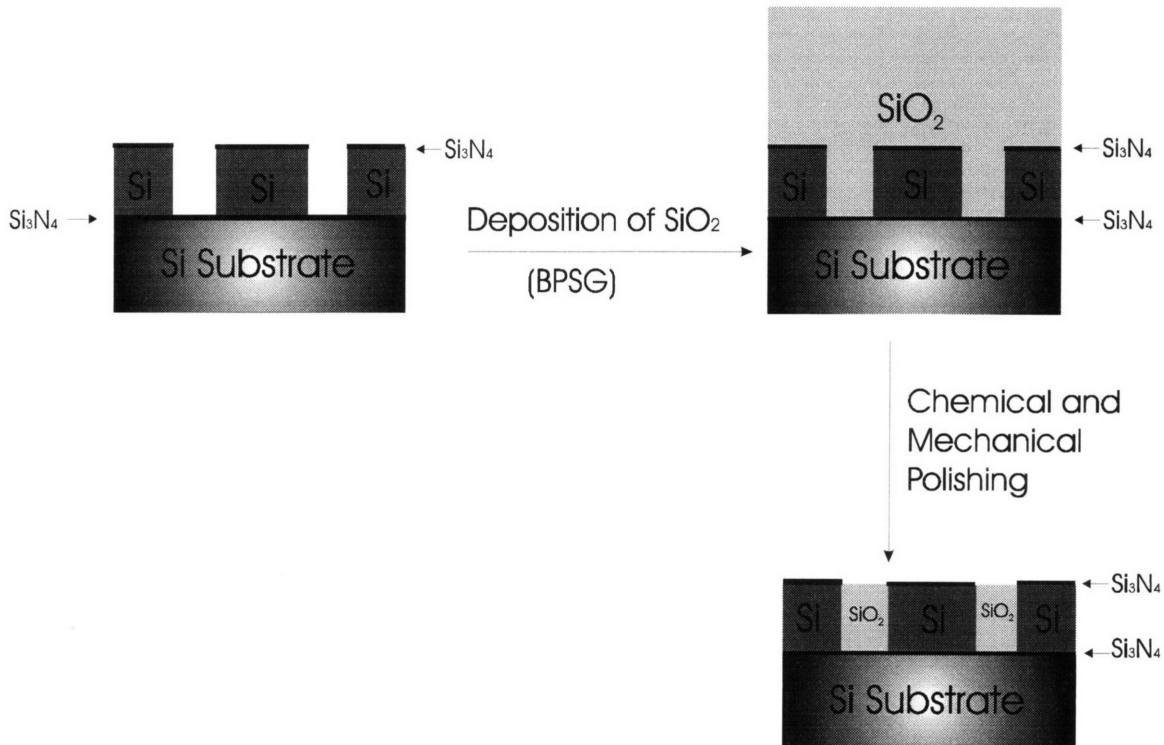


Figure 4.12: Schematic of process. Deposit SiO_2 and then use CMP to planarize the surface.

4.2.3 Fabrication of layer 2

The schematic of process for fabrication of layer 2 is shown in Figure 4.13. The results are shown in Figure 4.14.

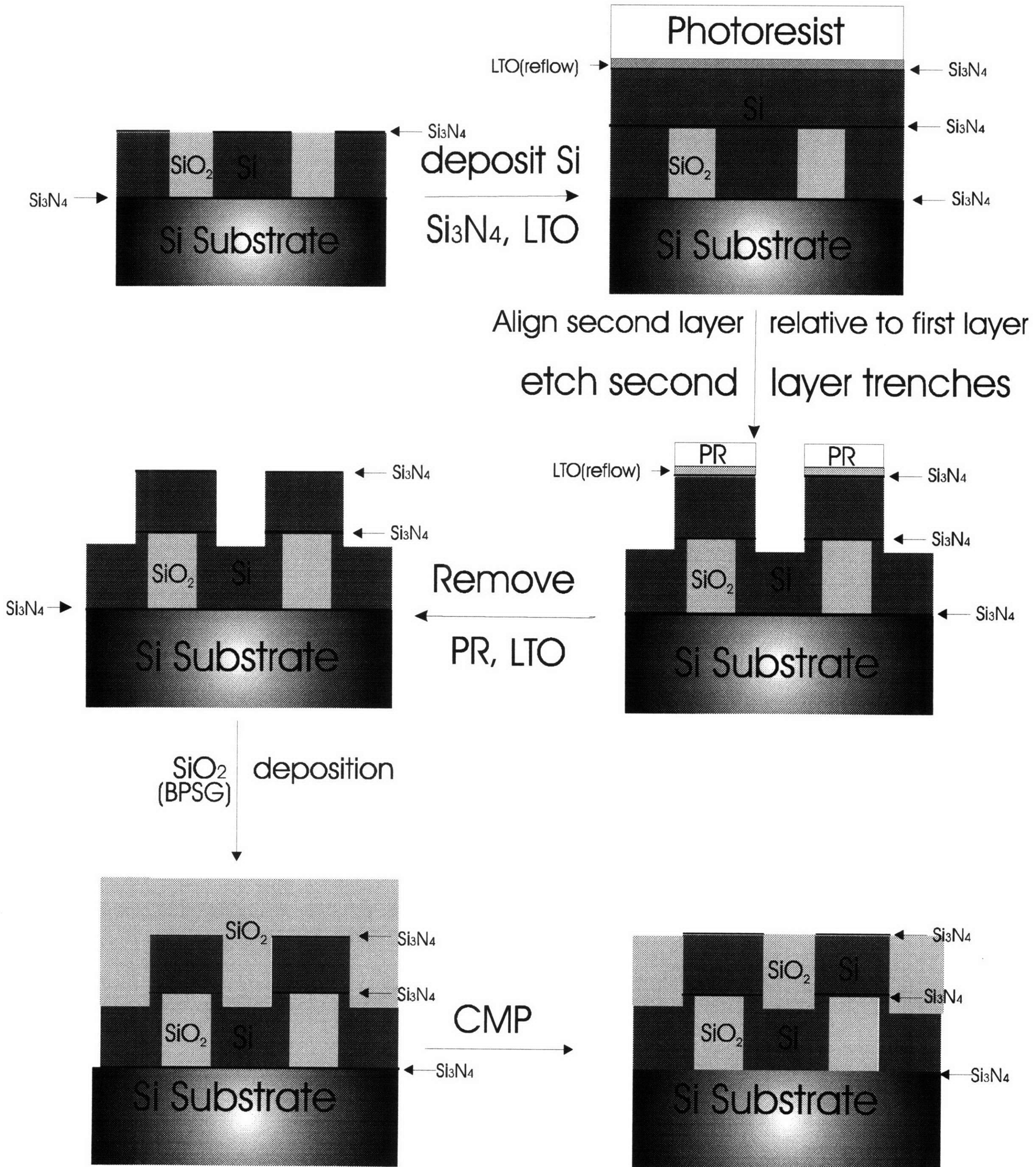
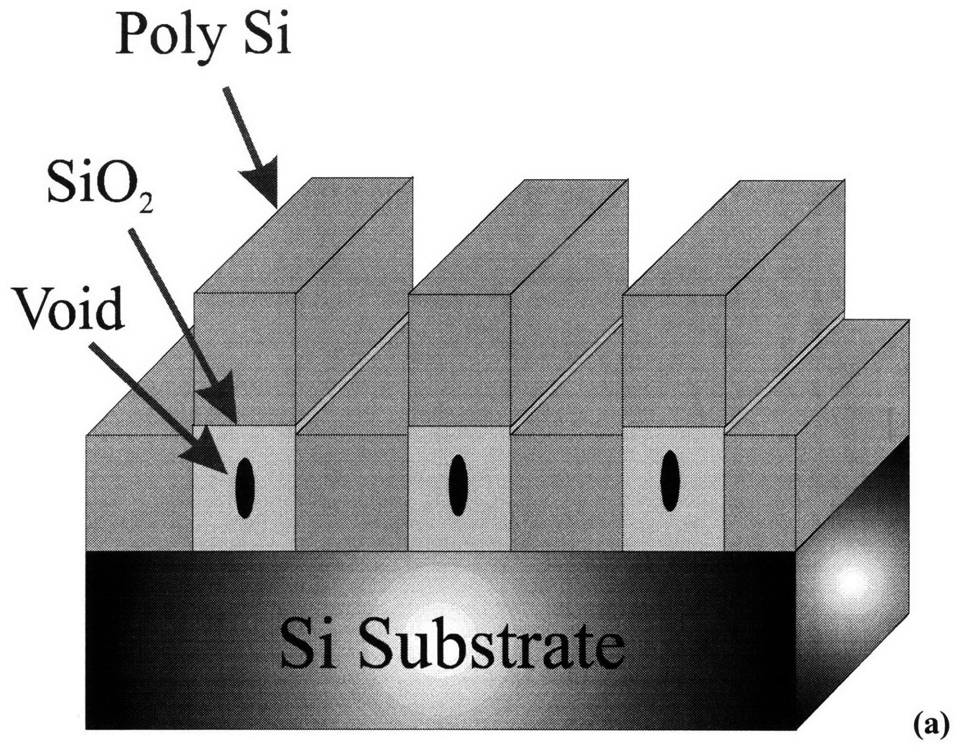
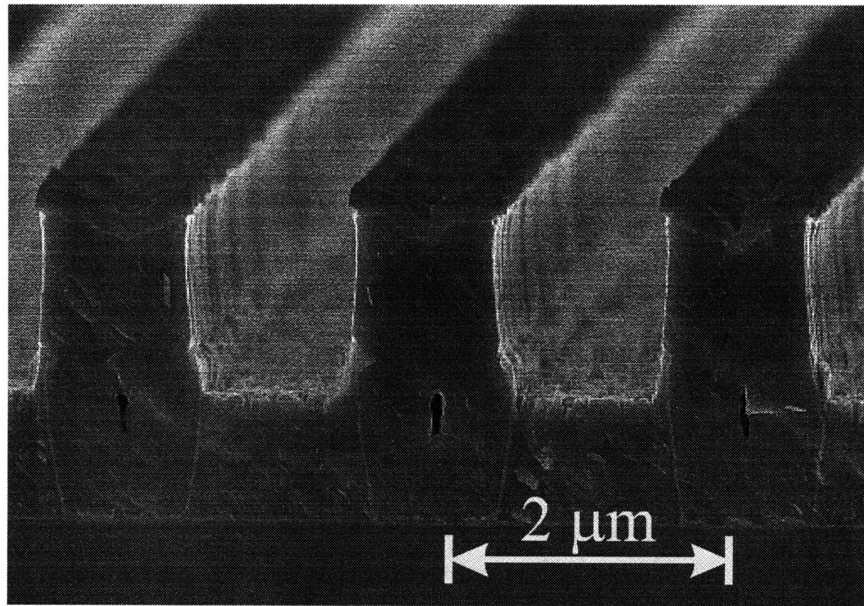


Figure 4.13: Schematic of process for fabrication of layer 2.





(b)

Figure 4.14: Completion of layer #2 trench. (a) is schematic and (b) is the SEM of cross-sectional view.

Chapter 5

Future directions

5.1 If CMP does not work, what about oxygen ion implantation?

If CMP does not work, oxygen implantation could be used instead[23,24,25,26]. The outline of the fabrication process is shown in Figure 5.1. First, the photoresist is coated on the Si surface. Then a metal layer is deposited (or sputtered) on the photoresist layer. Through photolithography and plasma etch of metal, the desired patterns are printed on wafers. The oxygen ion implantation uses a high-energy O^+ beam, typically in the 40- to 1000-keV range, resulting in penetration under the silicon to a depth of about 1.3μm. Additionally, a heavy dose, $1\text{-}2\times10^{18}$ ions cm^{-2}, is used to produce SiO_2 grooves within the Si layer. Multiple implantations are used to produce a dopant distribution profile other than a Gaussian. In our case, a flat doping profile (Figure 5.2) can be produced by 6 discrete implants with energies ranging from 40kev to 900kev (Table 5.1).

There are several issues needing discussion here.

(1) Projected range, longitudinal straggle, and lateral straggle:

An individual implanted ion undergoes scattering events with electrons and atoms in the target, reducing the ion's energy until it comes to rest. The total path length of the

ion is called the range. A typical ion stops at a distance normal to the surface, called the projected range. Some ions come to rest beyond the projected range, and some ions come

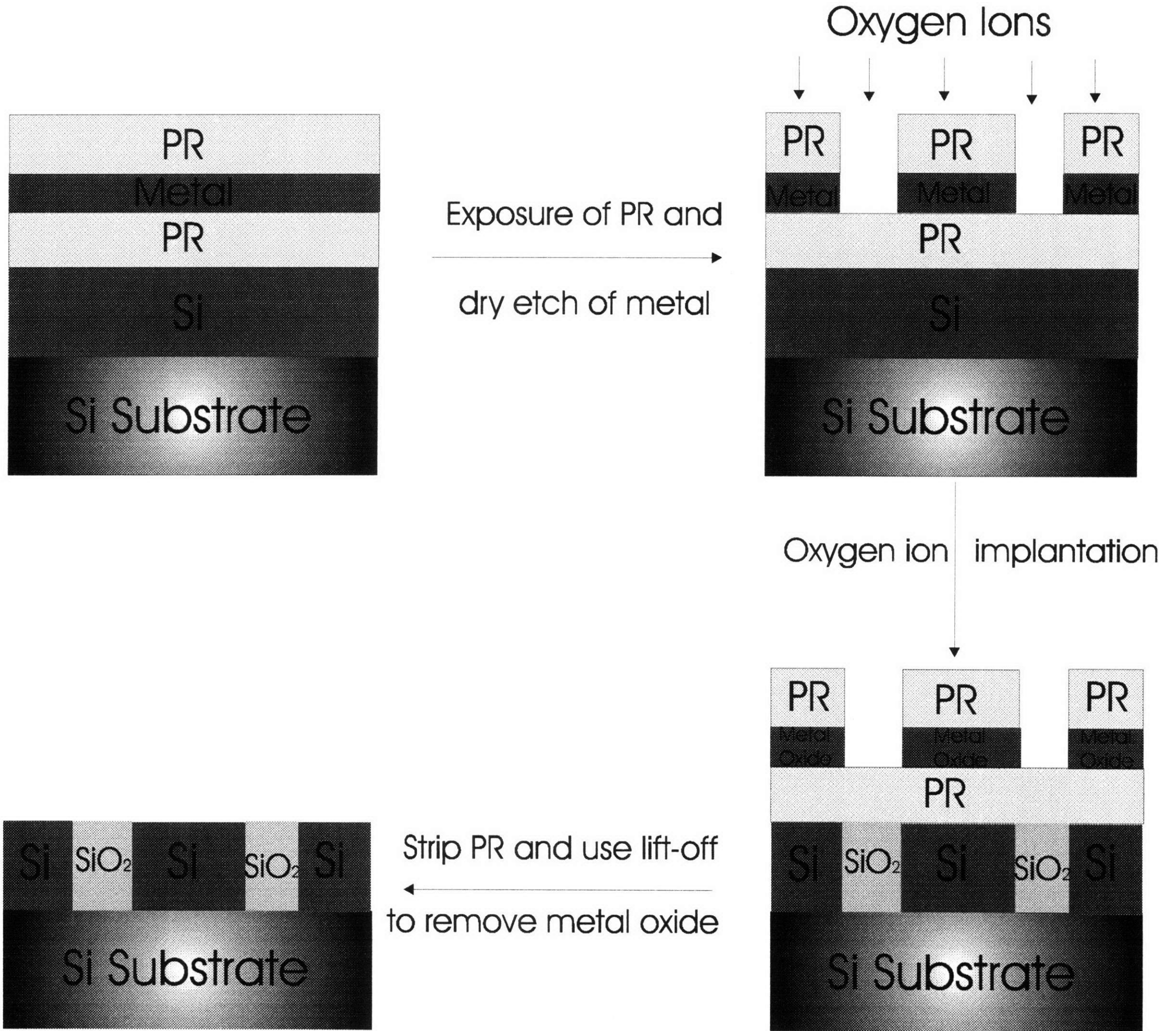


Figure 5.1: Outline of fabrication process using oxygen ion implantation (one layer is shown).

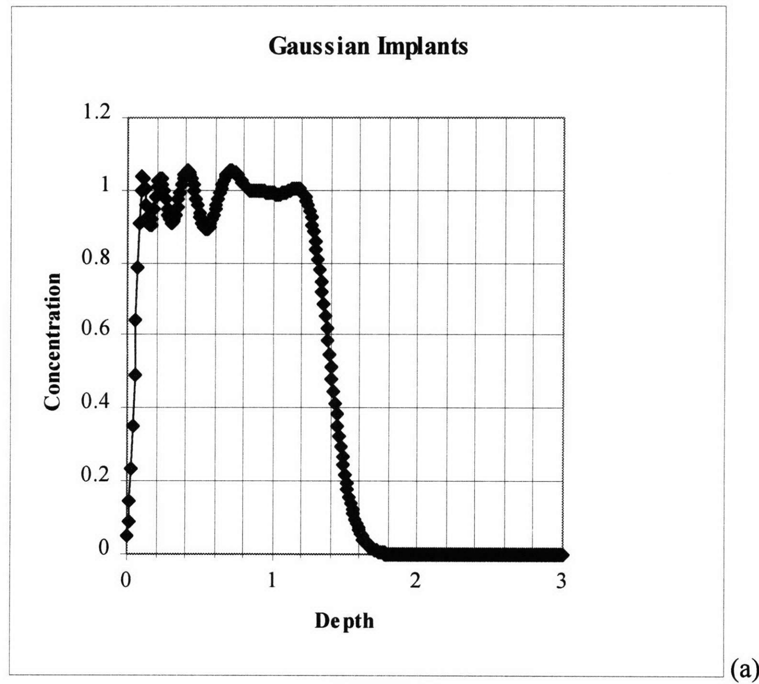
to rest between the surface and the projected range. The fluctuation or straggle in the projected range is longitudinal straggle. There is also a fluctuation in the final ion's position perpendicular to the incident ion's direction, called the lateral straggle.

(2) The data in Table 5.1 come from company IICO. They used TRIM simulation and assumed oxygen ions on Si target, which has the density of 2.321g/cm^3.

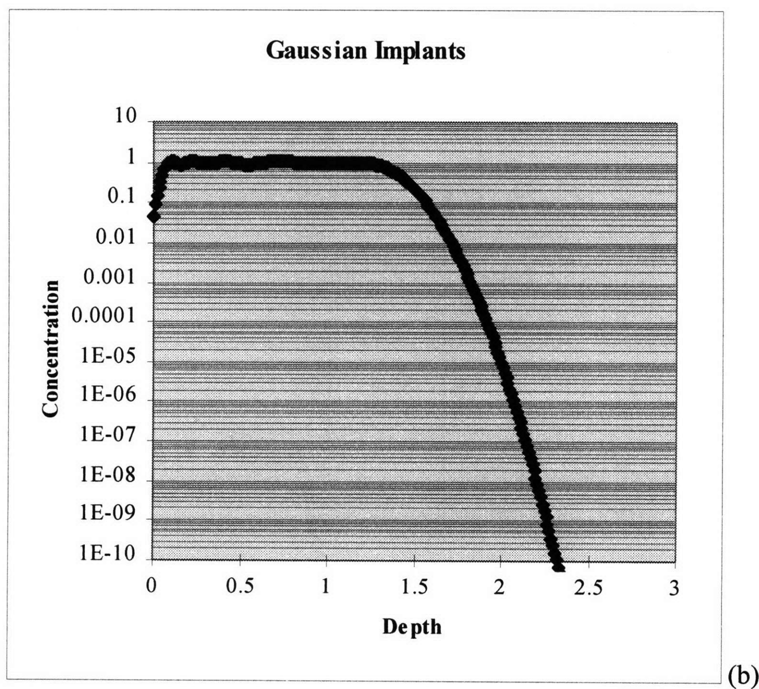
(3) Six discrete implants are chosen to achieve the flat doping profile. If only two kinds of implants are used, it's impossible to achieve desirable doping profile. The more discrete implants, the easier to achieve the flat doping profile. However, it is unnecessary to go beyond 6 implant steps.

Components	**#1**	**#2**	**#3**	**#4**	**#5**	**#6**
Ion Energy (keV)	40.00	90.00	180.00	330.00	550.00	900.00
Projected Range (Å)	915	2020	3888	6511	9164	12300
Longitudinal Straggle (Å)	375	656	984	1292	1479	1614
Lateral Straggle (Å)	286	547	909	1318	1631	1883
Peak Concentration	0.79	0.85	0.92	0.84	0.76	0.89

Table 5.1: 6 discrete implants to produce desired profiles.



(a)



(b)

Figure 5.2: Uniform O-profile calculated using 6 discrete implants shown in Table 5.1. Concentration axis is linear in (a) and is logarithm in (b).

Acetone can be used to strip the photoresist so that the metal oxide layer can be lifted off. At this point, a single period of a PBG structure is made. Compared to the methods described before, ion implantation can reduce a lot of steps, such as depositions of Si_3N_4 (etch stop of CMP), LTO (hard mask of Si etch) and BPSG, plasma etch of Si_3N_4, LTO and polysilicon and CMP. This method has more possibility to be successful due to its simplicity. However, the main problem is the difficulty in controlling the oxygen profiles during implantation.

5.2 If contact aligner does not work, what about deep UV stepper?

Standard photolithography is normally carried out in the 3100Å to 4500Å spectral region, with practical resolution about 1μm in MTL. Resolution can be increased by reducing the wavelength of the exposure radiation to the 2000Å to 3000Å spectral region, called "deep UV." Using conventional optical lithographic equipment that has been modified to operate at shorter wavelengths, and using mask substrates made of quartz instead of glass, resist images on the order of 0.5 μm have been printed. Commercial deep-UV exposure sources are available, e.g. xenon-mercury lamps. Whether deep-UV lithography can be practical depends on the availability of a suitable photoresist. The match between the output spectrum of the exposure tool and the absorption spectrum of the resist determines the throughput capability of the technique. To achieve straight-walled resist image profiles, the resist must absorb only a small percentage of the incident radiation, usually less than 20%. On the other hand, too little absorption significantly

increases exposure time. In general, any e-beam resist is a candidate for a deep UV-resist, e.g. PMMA. Actually, because of the low absorption, PMMA forms straight-walled resist images.

For this project, the reasons why the deep UV stepper could become the most suitable candidate are: (1) Alignment can be achieved on each die, which eliminates the errors caused by the mechanical movement of stepper. (2) The patterns in wafers can be shown clearly on the screen, which makes alignment easier and more precise. (3) The mask contains the pattern of one large chip which is enlarged several times (e.g. 7×). Optical mask rather than e-beam mask could be used, which reduces the cost of mask making. Also small features can be printed with more accuracy.

Chapter 6

Summary

In summary, 3-D photonic bandgap structures are fabricated with both Si/SiO_2/air and Si/air material systems and with three different midgap frequencies (4.3μm, 4.5μm and 4.7μm). Various configurations consisting of different dimensions of the trenches have been built. These 3-D PBG structures can potentially be used in making high-Q microcavities for single-mode light-emitting diodes and low threshold lasers.

In the process of building these structures, various fabrication issues have been investigated and addressed. First, device dimensions approaching the limits of the photolithography have been attained. A LTO hard mask and Cl_2/HBr plasma etch are used to produce Si trenches that have straight sidewalls at the desired dimensions. BPSG oxide can fill in the Si trenches without voids, which appear in LTO or PECVD SiO_2 deposition. The fabrication of first layer ends with a CMP step. Using complementary alignment crosses and Moire marks, we can achieve good alignment between the mask and the patterned wafer. After plasma etch, BPSG deposition and another CMP, the fabrication of two layers 3-D PBG is completed. The same methods can be repeatedly used until finishing the fabrication of the whole 10-layer structures. There are two other interesting issues that should be addressed: the use of oxygen ion implantation and the use of deep UV stepper. Ion implantation has more possibility to be successful since it saves a lot of steps, such as deposition of Si_3N_4, LTO and BPSG, plasma etch of Si_3N_4,

LTO and polysilicon and CMP. Deep UV stepper seems to be most suitable for photolithography as for achieving more accuracy in printing small features and better alignment.

This project has been exciting and will provide a base for more exciting results and deeper understanding of the intrinsically intriguing physical phenomenon. The experience of the fabrication of a 2-layer PBG structure is very important, since it can provide the successful recipes and parameters, which are the cornerstones for the completion of the ten layers that are needed in the 3-D PBG structure and the verification of the photonic bandgap.

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