Fabrication and Measurement of Linear Arrays of Quantum Dots

by

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Submitted to the Department of Electrical Engineering and Computer Science in partial fulfillment of the requirements for the degree of

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Abstract

This thesis describes the first realization and initial measurements of a linear array of seven quantum dots. The device was fabricated on a high mobility GaAs/AlGaAs heterostructure. Electron beam lithography was used to pattern critical features of the device, and 70 nm resolution was achieved. A ^{3}He probe was used to measure the device at 300 mK. The design of the device allowed individual control over each Quantum Point Contact that defines the dots. It also allowed creating systems of N quantum dots with N ranging from 1 to 7. Conductance oscillations as a function of gate voltage were seen for all gates in a single dot configuration and the capacitances of these gates to the dot were extracted. Temperature dependence of the conductance peak width was investigated. Current voltage measurements of the single dot system were made which allowed measurement of the total capacitance and the lead-to-dot capacitance. A double dot system was also investigated. For a pair of the weakly coupled quantum dots the period of conductance oscillations is essentially the same as for the single dot. As the coupling increases each peak splits into two peaks, and for a very strong coupling, when the two dots merge into one large dot, the peak period is the same as for a single large dot with twice the capacitance to the gate.

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A special thanks goes to Dave Carter who introduced me to the NSL and measurement labs. It would not be too much to say that everything I learned about fabrication I learned from Dave. Thanks to Chagarn Whan for countless discussions about quantum dots and about life in general. Thanks to Mark Schweizer who rebuilt and upgraded the thermal evaporator.

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To my parents, I thank you for you support and understanding during these two years.

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Chapter 1

Introduction

1.1 Need for new paradigms in the semiconductor industry

The rapid miniaturization of field-effect transistors to the submicron regime has led to high-speed and low-power digital logic, the mainstay of today's computers. If the electronics revolution is to continue by increasing the packing density of integrated circuits, the feature size of transistors must be correspondingly scaled down. As conventional field-effect transistors are shrunk, however, they suffer from a number of ailments, such as hot-electron and short-channel effects. A second, and more threatening, obstacle to further miniaturization is the "wiring crisis": the interconnects between transistors become highly congested as progressively more components are crowded onto an integrated circuit.

One way to bypass these roadblocks is to seek a radically different approach to electronics. One candidate is quantum-effect electronics [19], which seeks to exploit quantum-mechanical phenomena in semiconductor nanostructures to achieve enhanced functionality of devices. In a quantum dot, electrons in a two-dimensional electron gas (2DEG) are electrostatically confined in three spatial dimensions to create a small, nanometer-scale conducting island. Because the charge on the island can only change discretely in integer multiples of the electron's charge, the current through the island is impeded by the Coulomb charging energy required to add a single electron to a quantum dot. Because the blockage of current can be controlled by a gate electrode, devices based on this effect have potential applications as amplifiers, detectors, and switches. In contrast to conventional field-effect transistor action, charging effects due to single electrons improve, rather than degrade, with shrinking dimensions. Finally, the natural discreteness of parameters such as charge, energy, and spin in a quantum dot could be exploited to encode bits.

Because of the interconnect problem described above, however, it is not sufficient to simply replace a conventional transistor by a quantum-mechanical transistor [20]. Already the delay time due to interconnects limits the switching speed in modern digital circuits, since interconnects cannot be scaled down in proportion to minimum feature size. To circumvent this problem, a possible approach would be a design in which neighboring quantum elements could interact directly with each other, without the use of an interconnect.

1.2 Computational schemes with quantum dots

Several different quantum-effect computational architectures have been proposed. A common basis for all of these computational paradigms is that a computation is performed by a large array of quantum dots interacting in some way.

A proposal by Lent [7] exploits the idea of cellular automata. In this architecture computation is performed by an array of cells. Each cell can switch between several allowed states, and the cells interact with their neighbors at regular time intervals according to certain rules. It was shown [9] that if a physical representation for the cells was found, such architectures could perform useful computation.

Lent proposed to use a cluster of 4 or 5 interacting quantum dots as a cell. Each cluster, shown in Figure 1.1, would contain exactly two electrons, which would be able to tunnel from dot to dot within the cluster, but would not be allowed to tunnel outside the cluster. Two electrons tend to occupy antipodal sites in one of two configurations, shown in the Figure 1.1 as the P=+1 and P=-1 configurations. Switching between these configurations is very abrupt, and therefore, the cell can contain a bit of information encoded in its polarization. When two of such cells are placed in close proximity, even small polarization of one cell causes, through the coulomb interaction, almost total polarization of the neighboring cell. This makes it possible to transmit signals along the chains of quantum dot

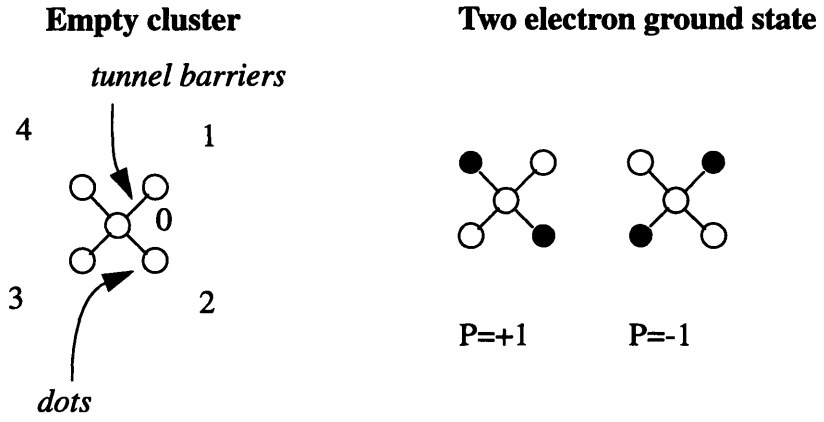

Figure 1.1: The quantum dot cell consisting of five quantum dots which are occupied by two electrons. The mutual Coulombic repulsion between the electrons results in two stable polarization state labeled by P=+1 and P=-1. After ref. [8].

clusters. It is furthermore, possible to design logical elements such as inverters, AND and OR gates.

An alternative proposal by A. Korotkov [10] exploits polarization of short chains of quantum dots to perform computation. An array of quantum dots can be polarized by an external electric field causing electrons to redistribute inside the array. The polarization state of the array is hysteretic and can be used to represent information. If the external field is close to the threshold field which causes spontaneous polarization, then the polarization field of the array can polarize the neighboring array by electrostatic interaction. This makes it possible to transmit information along the lines of such quantum dot arrays, as shown in Figure 1.2. Note, that direction of the field makes a 45 degree angle with the direction of the array. This enables arrays to be oriented in two perpendicular orientations. If the transmission line of the arrays is properly designed, the polarization of one array can trigger more than one array to be polarized, so it is possible to fan-out the signal. Similarly it is possible to design AND and OR gates, and other logical building blocks.

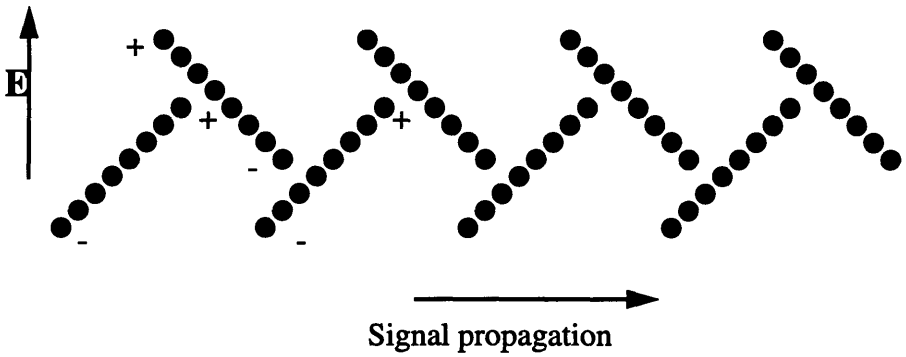

Figure 1.2: A line of the short quantum dot arrays used to transmit information. The electric field E is such that polarization of the left-most array triggers the polarization of next array in line and so forth. After Ref. [10].

The advantage of this architecture over the one proposed by Lent, is that it uses sequential switching of neighboring elements rather then global relaxation to a system's ground state. Therefore, it is expected to be more robust, than the ground state computing architecture.

1.3 One dimensional arrays and thesis outline

In order to be able to design computationally useful quantum dot systems which will have an arbitrary interaction geometry, we have to be able to understand the basic physics of the systems with regular interaction geometry; e.g., arrays of quantum dots. While there has been some work done on Lateral Surface Superlattices [4], and with 2-d arrays of Quantum dots [8], 1-d arrays of quantum dots have not yet been investigated.

Therefore, there exists a need to study and understand the behavior of the one dimensional arrays of quantum dots. In fact, both of the proposals described above incorporate 1-d quantum dots array sub-systems.

In this thesis I will describe the fabrication technology necessary to fabricate such arrays, and experimental results obtained from such an array. Chapters Two and Three

describe the design issues and fabrication procedures developed in order to successfully fabricate working devices. Chapter Four describes the initial experimental results. Chapter Five concludes the thesis with a summary and suggestions for future work.

Chapter 2

Design

This chapter deals with the issues involved in the design of the quantum dot array device. The chapter first explains why a particular material system and fabrication technology was chosen to realize a quantum dot array. It then describes particular array geometries that were designed and implemented, and the engineering trade-offs that were made in the design process.

2.1 The choice of material system and fabrication technology

At the present time, there are numerous technologies for fabrication of the quantum effect devices. Historically, the Coulomb blockade was first observed in Al/Al_20_3 Single Electron transistors. They were first proposed by K. Likharev [21] and first observed by Fulton and Dolan [18]. Next step in terms of fabrication technology was a Si split-gate MOSFET transistor investigated by Scott-Thomas et al. [22]. Then a systematic study of a quantum dot fabricated on a high mobility GaAs/AlGaAs heterostructure by a split-gate technique was performed by Meirav et al. [12]. This method became and still is the most popular technique for the fabrication of the quantum dot systems.

Recently, several new techniques were developed. They allow fabrication of extremely small quantum dots, whose operational temperatures are approaching room temperature. One of the techniques, pioneered by Y. Takahashi [11], uses pattern dependent oxidation of Si to form a 30 nm diameter Si dot. Such dots have a charging energy comparable to the room temperature. The other technique, developed by K. Matsumoto [13] uses oxidation of the thin Ti film under the tip of the STM to define a 30 nm size metal dot.

For a fabrication of a coupled Coulomb blockade devices, in general and arrays in particular, the best choice of technology at the present time are split-gates on GaAs/AlGaAs heterostructure. Unlike Al/Al_2O_3 systems, transmission through the tunneling barriers can be controlled by voltages on the gates. GaAs/AlGaAs heterostructures have much higher mobilities than Si MOSFETs, so that devices with lengths less than the scattering length can be made. New technologies using pattern dependent and STM oxidation currently suffer from poor yields and also lack the ability to control the tunnel barriers.

Therefore, the conventional split-gate technique on GaAs/AlGaAs heterostructure was chosen for the quantum dot array fabrication. Figure 2.1 illustrates how a quantum dot is

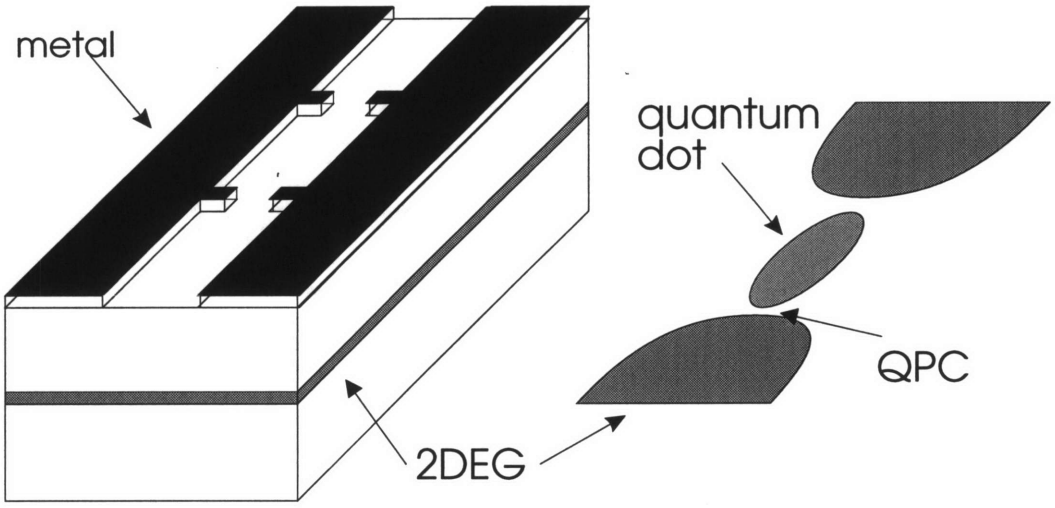

Figure 2.1: A quantum dot created by split-gate technique on GaAs/AlGaAs heterostructure.

created by a split-gate technique on GaAs/AlGaAs heterostructure. The GaAs/AlGaAs heterostructure contains a layer of two-dimensional electron gas (2DEG) about 100 nm from its surface. Schottky gates are deposited, and when a negative voltage is applied to them, the 2DEG below is depleted. The geometry of the gates is such that there remains a

small conducting channel connected to the rest of the 2DEG by two tunneling barriers. The points of the narrowest constriction of the 2DEG, where the tunneling barriers are located, are called Quantum Point Contacts (QPCs).

2.2 Array geometries

In most of the experiments with single-electron devices one needs to be able to control the Fermi energy of the quantum dot (or dots). This can be achieved in several ways. Usually one incorporates a small plunger-gate into the dot confinement structure. When the voltage on this plunger-gate is swept, it changes the shape of the quantum dot, and thus its Fermi energy. The coupling from the plunge-gate to the QPCs is not very strong, so transmission through the QPC's remains essentially unchanged. This technique is difficult to use for arrays of several quantum dots as it would require too many gates to be used in the design. An alternative technique is to use a conductive substrate separated from the 2DEG by an insulating layer. When the voltage is applied to the back-gate, it controls the density of the 2DEG, and thus changes the Fermi energy of all quantum dots simultaneously. In that case only one electrical connection is needed regardless of the number of the quantum dots. Another advantage of the back-gate is that it allows separating the effect of the changing size of the quantum dot from the effect of changing its Fermi energy.

My design uses back-gated heterostructures, described in detail later in Section 3.1, although a back-up solution is incorporated in the design in case difficulties with back-gated heterostructures are encountered. The back-up solution is to place an extra Schottky gate along the whole length of the array. This gate has similar capacitive coupling to all the dots in the array, and therefore, also allows one to sweep the Fermi energy of all the dots in the array.

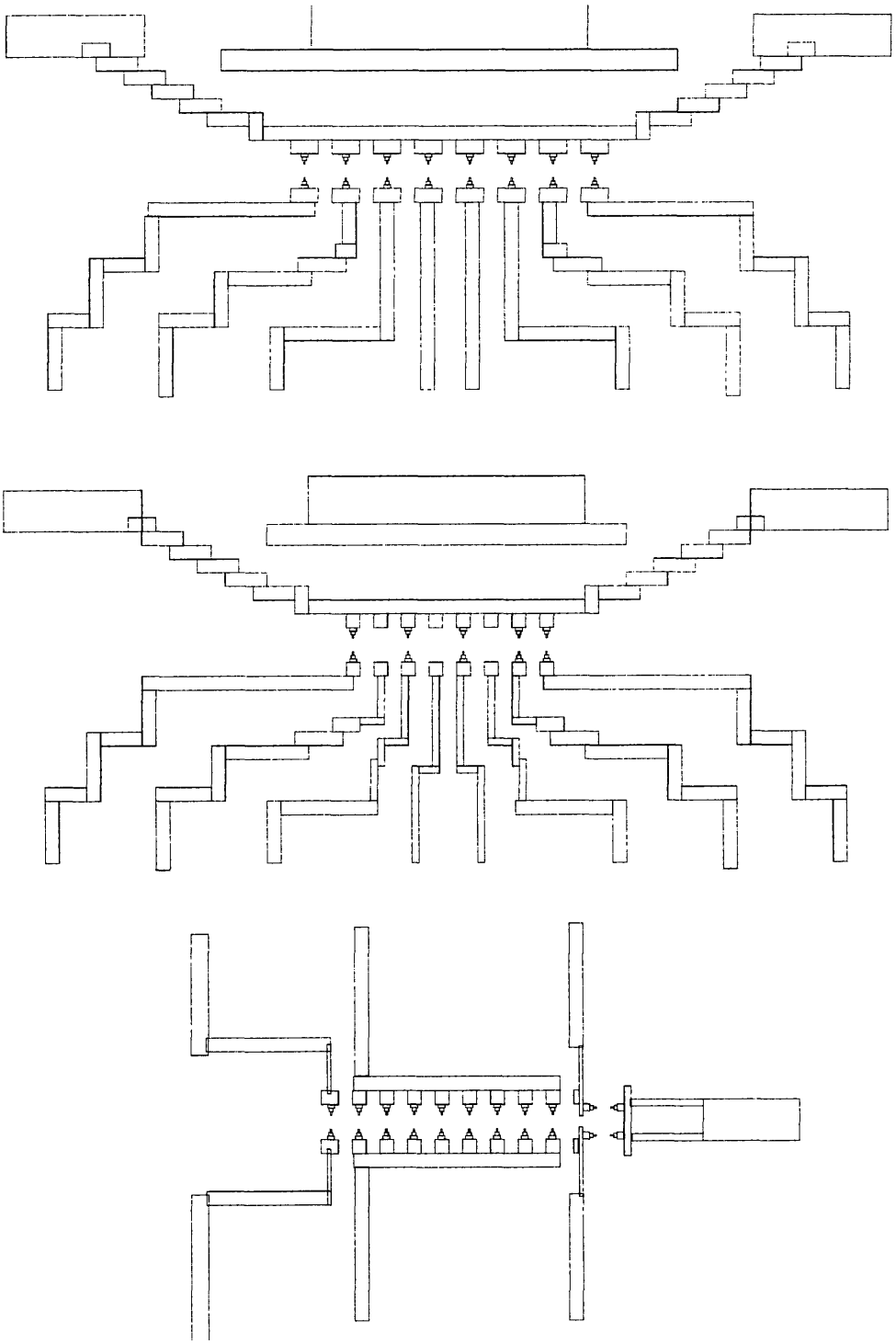

Figure 2.2: Layout of the quantum dot array devices. (a) Basic array geometry. (b) Triple dot with plunger-gates. (c) Polarization device

Impurities in the semiconductor strongly affect the characteristics of QPCs. Even a single impurity atom located near the QPC channel can significantly shift the conductance threshold or cause scattering in the QPC. It is essential for our experiments that the tunneling conductance of each QPC in the array be the same. Therefore, each QPC has to be controlled by a separate voltage source. This consideration limits the designed length of the array to 7 quantum dots (8 QPCs). This device has a total of 11 electrical connections (plus one extra connection for a side-gate), which makes its electrical connections compatible with earlier coupled dot devices designed by A. Kumar and D. Carter [1].

Figure 2.2 shows several designed device geometries. Geometry (a) is a regular 7-dot array. The width of the quantum dots is 500 nm, the length varies from 400 nm to 800 nm for different devices, and the spacing between the QPC fingers is 200 nm. The size of the dots was chosen to be small enough to give a 1-2 meV total charging energy, but large enough to avoid interference between charging effects and quantum confinement effects. Davies [14] has derived a useful expression for the ratio of the threshold voltages of split-gate and continuous gate devices:

$$\frac{V_{1d}}{V_{2d}} = \left(1 - \frac{2}{\pi}\operatorname{atan}\frac{w}{2d}\right)^{-1}, \tag{2.1}$$

where V_{2d} is the voltage required to deplete 2DEG under a large area continuous gate, V_{1d} is the voltage required to pinchoff a 1-d channel in a split-gate device, w is the spacing between the gates, and d is depth of 2DEG. For a typical heterostructure with the 2DEG located 55 nm below the surface, $V_{2d} \sim -0.4$ V, so a width of 200 nm, yields a reasonable value of $V_{1d} \sim -1.2$ V.

Array of geometry (b) in Figure 2.2 is a triple dot with plunger-gates. It was created by converting some QPC's in the original design to plunger-gates. This device was intended to serve as a test device. It offers more flexibility at the expense of the array length.

Figure 2.2(c) shows an array designed as a polarization device. It is intended to demonstrate the hysteretic character of the polarization state of the short array of quantum dots. The tunneling barriers on both ends of the array will be tuned to exclude the possibility of electrons tunneling in or out of array. A quantum dot electrometer, located next to one end of the array is used to probe the polarization state of the array. This version of the polarization device does not have separate quantum point contacts, and was not imple-

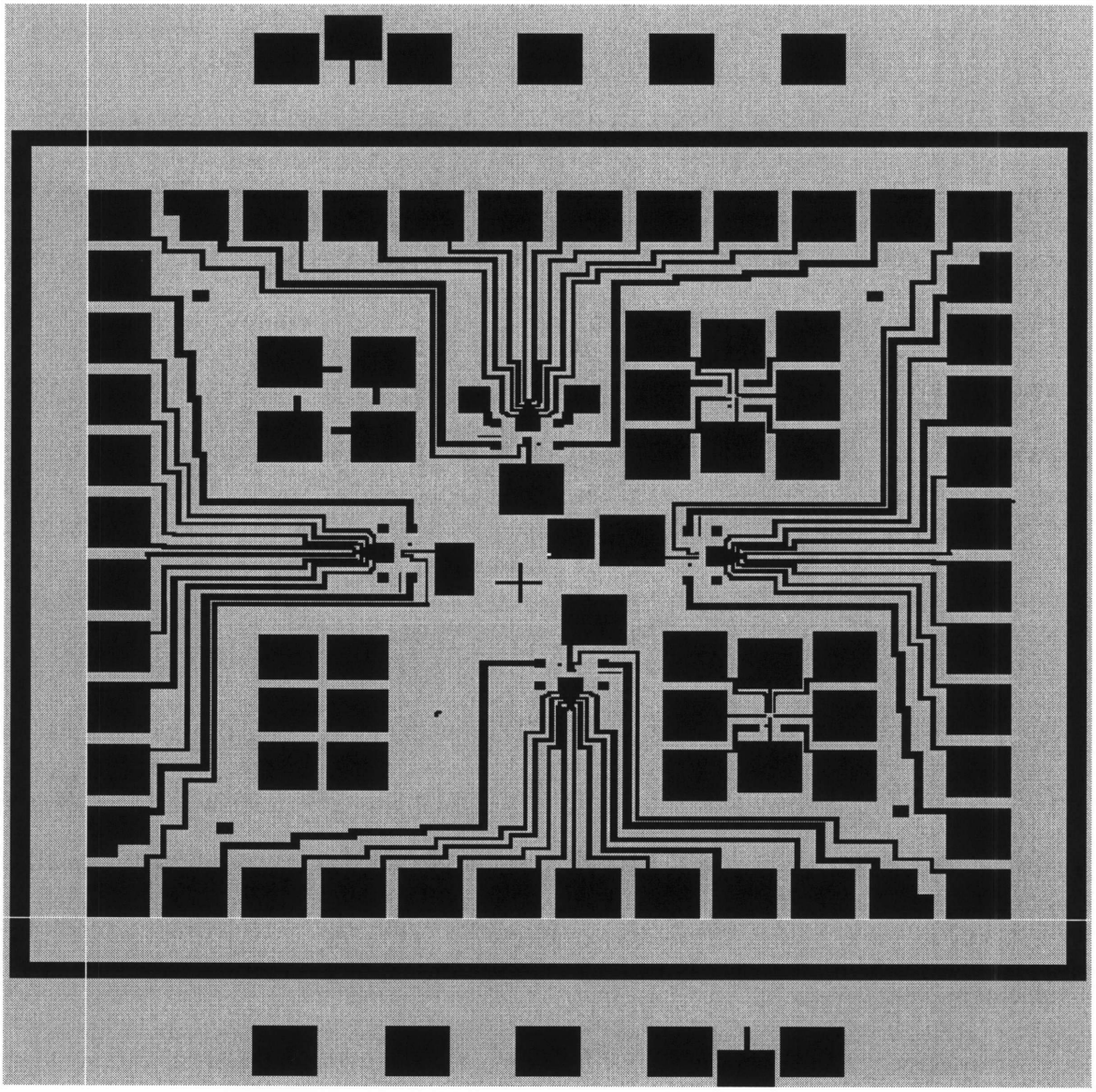

Figure 2.3: One die from the mask set design (first metal layer). The mask set is designed to facilitated bonding of 4 interior devices to a 44-pin chip carrier. If side-gates are used, then only 2 devices can be bonded at one time.

mented. However, the e-beam dose matrix runs, used to correct for proximity effect, were made.

Figure 2.3 shows a sample die from the optical mask set design. It is designed to facilitate the bonding of 4 interior devices to a 44-pin chip carrier. However, if side-gates are used, only two devices can be bonded at one time.The structure in the upper left corner is a van der Pauw structure for measuring the carrier density and mobility [15]. The structure in the lower left corner is a transmission line model which allows measurement of contact resistance. The structures in the upper and lower right corner are auxiliary devices with fewer connections than the 4 regular devices. The upper auxiliary device has 3 ohmic contacts and 5 gates and is intended for tests of polarization device. The lower auxiliary device has 2 ohmics and 6 gates and is intended for a 4 dot array.

Chapter 3

Fabrication

This chapter describes the fabrication process that was used to make quantum dot array devices. It starts by describing two GaAs/AlGaAs heterostructure wafers that were used to fabricate devices. It then continues with the general description of the fabrication process flow. Finally, it gives detailed descriptions for the electron-beam lithography procedures and e-beam level metal deposition and lift-off.

3.1 GaAs/AlGaAs Heterostructures

The high mobility 2DEG is created using modulation-doped GaAs/AlGaAs heterostructures grown by molecular beam epitaxy. In this structure the 2DEG is physically separated from the ionized dopants by a spacer layer. The cross sections of two GaAs/AlGaAs heterostructures used in this work are shown on Figure 3.1. The calculated conduction band edge of these heterostructures is plotted as a function of depth in Figure 3.2. The conduction band discontinuity at the GaAs/AlGaAs interface created a triangular potential well, of which only the lowest subband is occupied by electrons. The vertical extent of the electron wavefunction in the well is less then 10 nm, and, therefore, the electrons in the well exhibit two dimensional behavior. The density of carriers in the 2DEG is proportional to the total dopant number in the AlGaAs. Surface states pin the fermi level at the surface at -0.7 eV below the conduction band.

Both heterostructures were grown by Professor M. Melloch at Purdue University. The non-backgated heterostructure, MBE33, has a low temperature (T=4.2K) electron mobility $\mu = 4\times10^5 cm^2V^{-1}s^{-1}$, and a 2DEG density $n = 3.2\times10^{11}\ cm^{-2}$. The corresponding electron mean free path is $3.75\ \mu m$. Heterostructures of that type were successfully used in our

group previously by A. Kumar [1] and M. Burkhardt [2]. The backgated heterostructure, MBE32, has a larger spacer layer between the 2DEG and the dopant layer, as well as a thicker dopant layer. Therefore, it is expected, that it will have both higher mobility and larger electron density. Electrical insulation between the 2DEG and conducting substrate was achieved by using a layer of Low Temperature Grown GaAS (LTG-GaAS). This

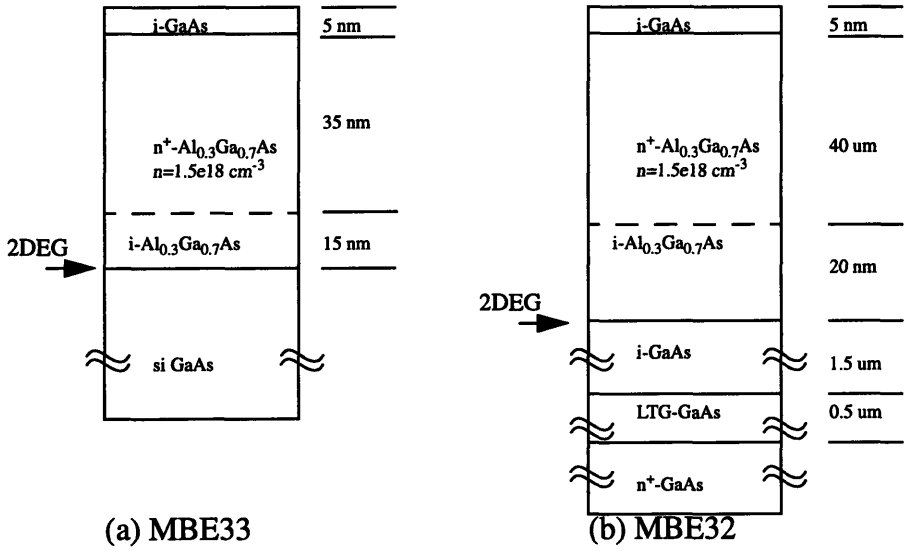

Figure 3.1: GaAs/AlGaAs heterostructures used in this work. (a) Non-backgated heterostructure with mobility $4\times10^5 cm^2V^{-1}s^{-1}$. (b) Deeper backgated heterostructure.

layer, grown at 225 C, as opposed to the normal growth temperature of 675 C has a very large trap density which makes the material highly resistive. The LTG-GaAs remains insulating even when moderately doped, which prevents the short between the substrate and the ohmic contacts to the 2DEG. The detailed analysis of using LTG-GaAs for back-gate isolation is give in Ref. [16].

3.2 Fabrication process

Device fabrication process flow is shown in Figure 3.3. The fabrication process consists of five main steps:

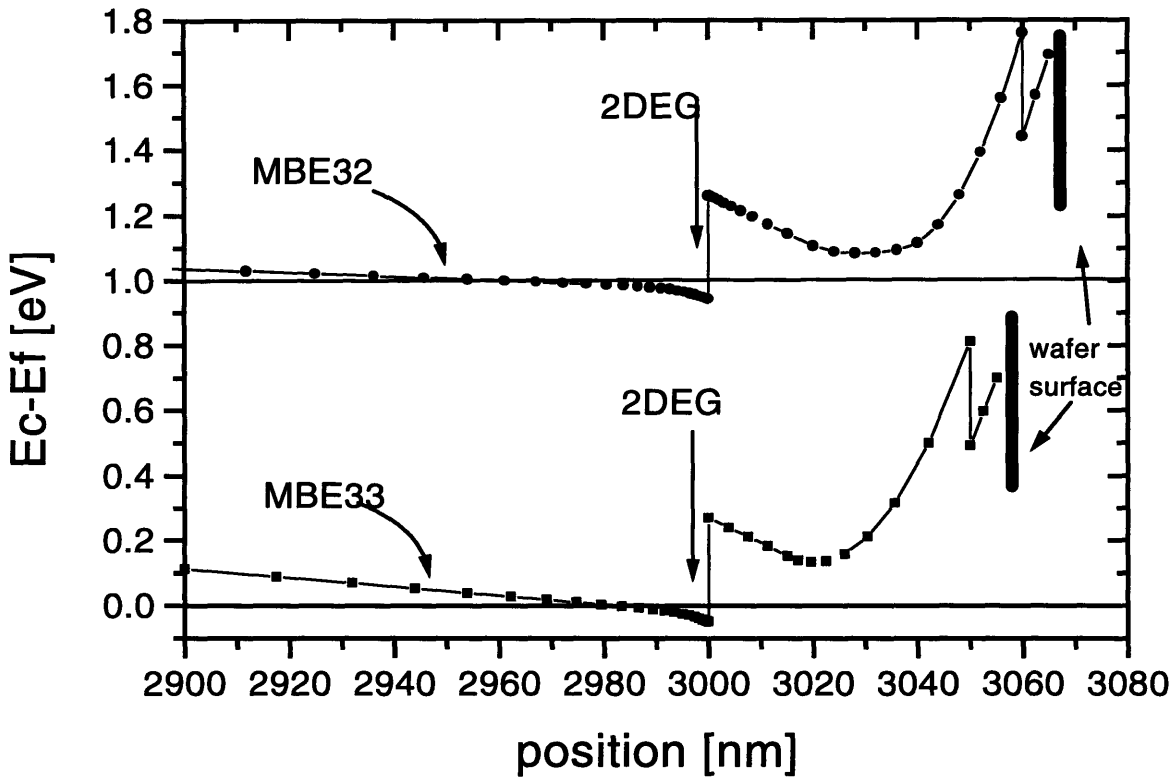

Figure 3.2: Calculated conduction band edge as a function of depth for heterostructures MBE33 and MBE32 (offset by 1 eV for clarity), found by solution of Poisson equation. Surface states pin the Fermi level at the surface at -0.7 eV below the conductions band edge. The conduction band discontinuity at GaAs/AlGaAs interface creates a triangular quantum well with 2DEG in it.

1. Mesa etch for device isolation,
2. Formation of ohmic contacts,
3. Optical level of gate metallization,
4. E-beam level of gate metallization, and
5. Bonding of completed device to a chip carrier.

Steps (1), (2), and(3) which involve features of several microns, were done using contact optical lithography at 400 nm wavelength. The processing recipe for these steps was adapted from Refs. [1] and [2] with some modifications, and is reprinted in Appendix A; the highlights are summarized below.

For mesa isolation, optical lithography and development were performed with the MESA mask, which was followed by an etch in 1000:20:6 solution of H_2O, NH_4OH, and H_2O_2. For this solution an 18 second etch results in 70 nm to 80 nm mesa.

To form ohmic contacts, photolithography was performed with the Ohmic mask. The development was followed by a de-scum in a UV-zone cleaning station and removal of oxide from the sample surface using a dip in 5% ammonium hydroxide solution. Then metal layers were deposited as follows: Ni(5 nm), Au (60 nm), Ge(120 nm), Ni(30 nm), Au (30 nm). The thermal evaporator was used to perform metal deposition, because the e-beam evaporator is known to often cause mobility damage to shallow 2DEG samples. This damage prevents formation of good ohmics contacts; the contact resistance is high at room temperature (>1 ohm-mm), and becomes infinite at 77K. After evaporation and lift-off, ohmics were annealed in a strip heater for 30 seconds at 420 C in the nitrogen atmosphere. During the anneal, germanium diffuses into the substrate, doping it, and creating a conducting path to the 2DEG. The chemistry of the Ni/Au/Ge ohmic contacts is discussed in Ref. [17] in greater detail. The contact resistance was then measured using a transmission line model structure. To make sure that ohmic contacts do not freeze out at low temperatures each device was tested at liquid nitrogen temperature. A special probe station equipped with liquid nitrogen cooled stage was used to measure the contact resistance at 77K.

The optical level of metallization consists, primarily, of the bonding pads and connecting lines going from the bonding pads on to the device mesas. Optical lithography was performed and Ti/Au layers (10 nm of Ti and 140 nm of Au) were done in the e-beam evaporator. In this case the active area of devices was covered by a layer of photoresist, and there was no danger of mobility damage by e-beam evaporation.

3.3 Electron Beam Lithography

The fine gates in step (4) of the fabrication sequence were patterned using electron beam lithography. A single layer of 3.5%, 950K PMMA (polymettylmethacrylate) was spun onto the substrate to a thickness of 200 nm and baked for an hour at 180 C. The pat-

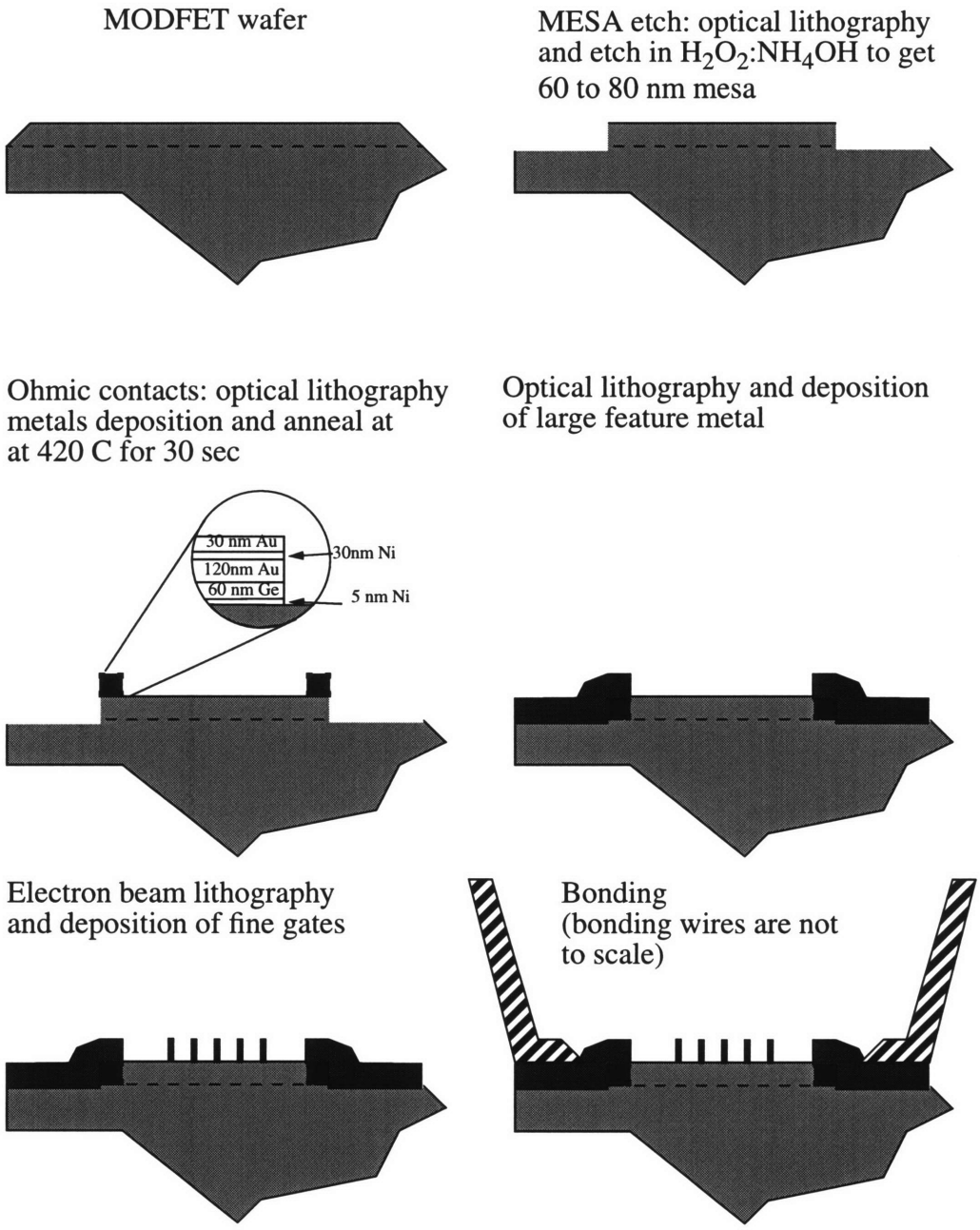

Figure 3.3: Device fabrication flow diagram

terns were written directly onto the substrate by a JEOL 6400 scanning electron microscope equipped with pattern generation system NPGS. NPGS uses a personal computer (486 PC) with 16 bit DAC cards to control the position of the electron beam in the SEM. To minimize the line width, 40 kV accelerating voltage was used for lithography. The

scanning electron micrograph in Figure 3.4 shows that a line width of 69 nm is attainable with this instrument and photoresist.

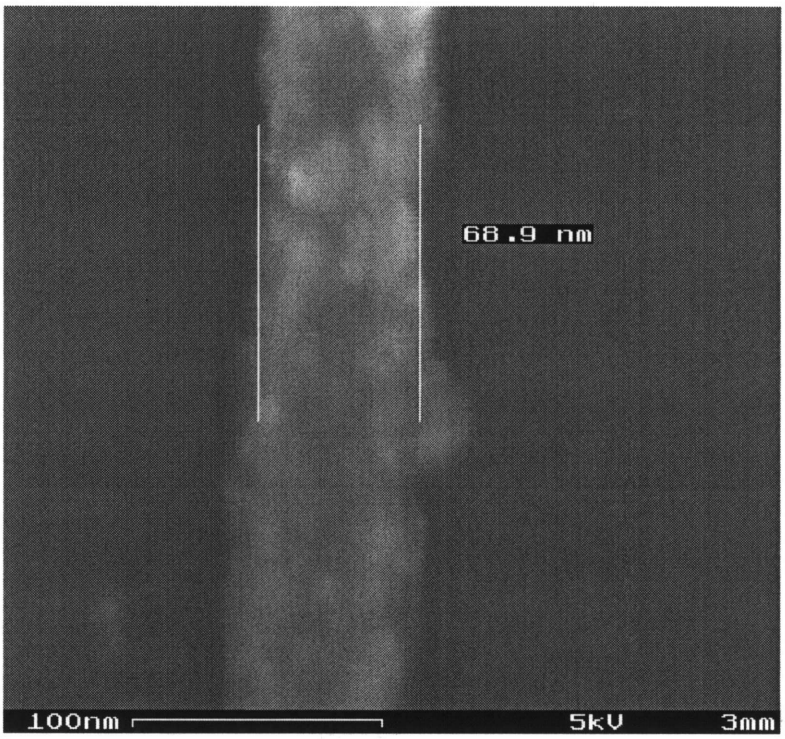

Figure 3.4: Scanning electron micrograph showing 69 nm line.

The procedure for e-beam writing is summarized below.

Two samples are loaded in the SEM chamber. The first one, is a special sample with very fine (less then 100 nm in diameter) gold particles on graphite substrate. It is used for stigmation of the electron beam. The second sample is the one being exposed.

The stage is moved to a 6 mm working distance (minimum allowed by the instrument) from the final lens of the SEM, and the beam current is set to 10 pA. Such small beam current and relatively small working distance are necessary to minimize the beam diameter of the SEM. Next, stigmation is done using gold-on-carbon sample at 300,000X magnification. The signal-to-noise ratio of the image at 10 pA beam current is very low, and the gold-on-carbon sample provides good contrast for the image. Good stigmation and focus-

ing are the major factors affecting the quality of e-beam lithography. Furthermore, stigmation parameters depend hysteretically on both current and focus parameters. Therefore, after stigmation is done, neither current nor electronic focus can be changed significantly.

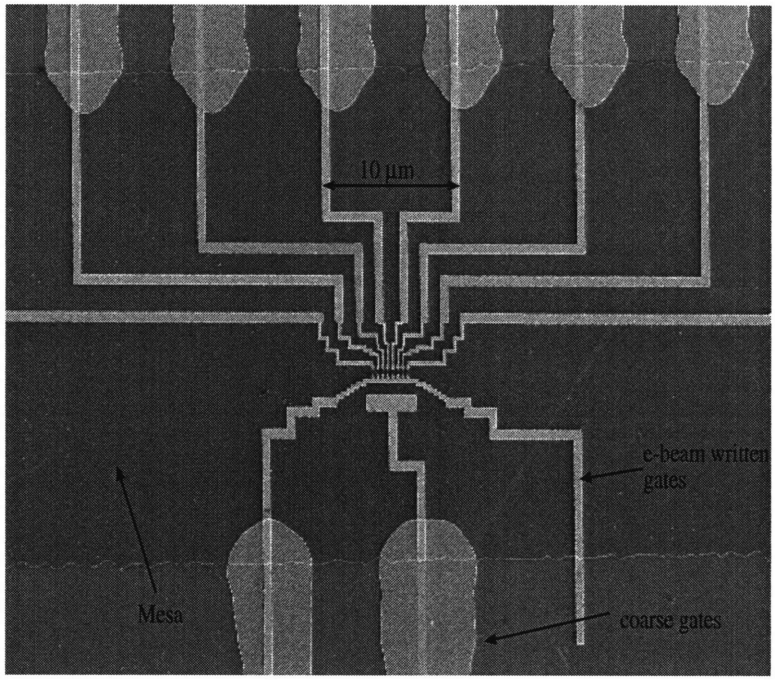

Figure 3.5: Scanning electron micrograph of the aligned device.

During writing, a 1000X magnification is used to obtain a $100 \times 100\ \mu m^2$ field size. However, at this magnification the contrast of the image is very poor, so I usually use 5000X magnification for alignment. After the stigmation process, described above, the stage is moved to a position of the sample to be written, and the surface of the sample is brought into the focus plane by moving the stage in the vertical direction. The x-y positioning of the stage is done using micrometers with $2\ \mu m$ resolution. However, the dials are not very linear, and therefore, the final alignment marks in the optical level metal have to be located less then $200\ \mu m$ from the writing area. On the other hand, placing them inside the writing area would introduce uniform background exposure dose, so careful bal-

ance had to be achieved. With X and Y alignment marks located about 100 μm from the center of the writing area, a necessary placement accuracy of ±2 μm was achieved in 90% of the cases. The scanning electron micrograph in Figure 3.5 shows alignment of the e-beam level gates to the optical level gates and the mesa. There is an intentional large overlay between the e-beam level gates and optical level gates, which insures continuity of the gates even in the case of slight misalignment. In the later versions of the design, the contact area between e-beam and optical level gates was increased by widening the e-beam lines. This was done to eliminate the possibility of the e-beam line breaking when making a 150 nm up-step to the optical gate.

Since the sample stage is not leveled relative to electron beam, focusing had to be done close to each device. The edge of the alignment mark was used for focusing at 50,000X in the line mode. Even when only the Z micrometer of the stage was used for focusing, adequate focus could be obtained with care. Alternatively, after the best focusing with the Z micrometer is obtained, the electronic focus could be tweaked a little, to improve the final focus.

In e-beam lithography it is impossible to assign a uniform exposure dose to all features of the pattern. Because of the proximity effect, the dose is dependent on the feature size and proximity of other neighboring geometries. While the clearing dose for large pads in my process is about 160 $\mu C/cm^2$, the optimal dose for an isolated single pass line, such as shown in Figure 3.4, is 1.5 nC/cm which is equivalent to 1500 $\mu C/cm^2$. While special software exists for proximity correction, it was not available to our group, and optimal dose-matrix was determined experimentally. All features in the device were split into three groups: small features (less then 100 nm), medium features (100 to 500 nm) and large features (more then 500 nm). The optimal dose for each group were determined separately. For the quantum dot array device the optimal doses were found to be 200 $\mu C/cm^2$ for large

features, 250 ($\mu C/cm^2$) for the medium features, and 330–370 $\mu C/cm^2$ depending on the size of the quantum dots in the array. Since the dose-matrix is particular to the device geometry, it is quite different for the polarization device. In fact, the 3 level dose matrix was not adequate for the polarization device to get all the features develop to the right size.

3.4 E-beam level development, metal deposition, and lift-off

After the sample was exposed by e-beam lithography it was developed in a 2:3 MIBK:IPA solution at 21 C for 90 seconds. The development was followed by a UV-ozone cleaning step and the dip in 5% NH_4OH solution. After this cleaning step the sample is loaded immediately into the evaporator chamber. Evaporations were done at base pressures less then 2×10^{-6} Torr. Typically 50 to 60 nm of gate metal were evaporated. After the evaporation was complete, gates were lifted-off in acetone.

As noted above, only the thermal evaporator could be used for fine feature evaporation in order to avoid mobility damage to the 2DEG. When using thermal evaporation on GaAs surface, it is possible to evaporate either aluminum or gold-palladium alloy. Initially, aluminum evaporation was used because of Al evaporation pellets were readily available. However, devices made with aluminum fine gates suffered from poor continuity between optical and e-beam level gates at low temperatures. The gates would modulate conductance at room temperature, but would loose contact when the device is cooled to 4 K. The gates then would not modulate even after the device was warmed back to room temperature.

The probable explanation for this failure is the follows. It is known that when low density metals like aluminum are being evaporated, they are usually under stress. When the sample is cooled, the stress is significantly increased because of thermal expansion coeffi-

cients mismatch. Therefore, the stress exceeds the threshold, and the line breaks at the weak point -- on the up-step to the optical gate.

High density metals like gold or gold-palladium do not typically have high stress at the deposition, and, therefore, can be used to circumvent the problem of gate continuity. Indeed, samples AuPd gates, and test samples with Ti/Au e-beam evaporated gates did not lose continuity when cooled to 4.2 K.

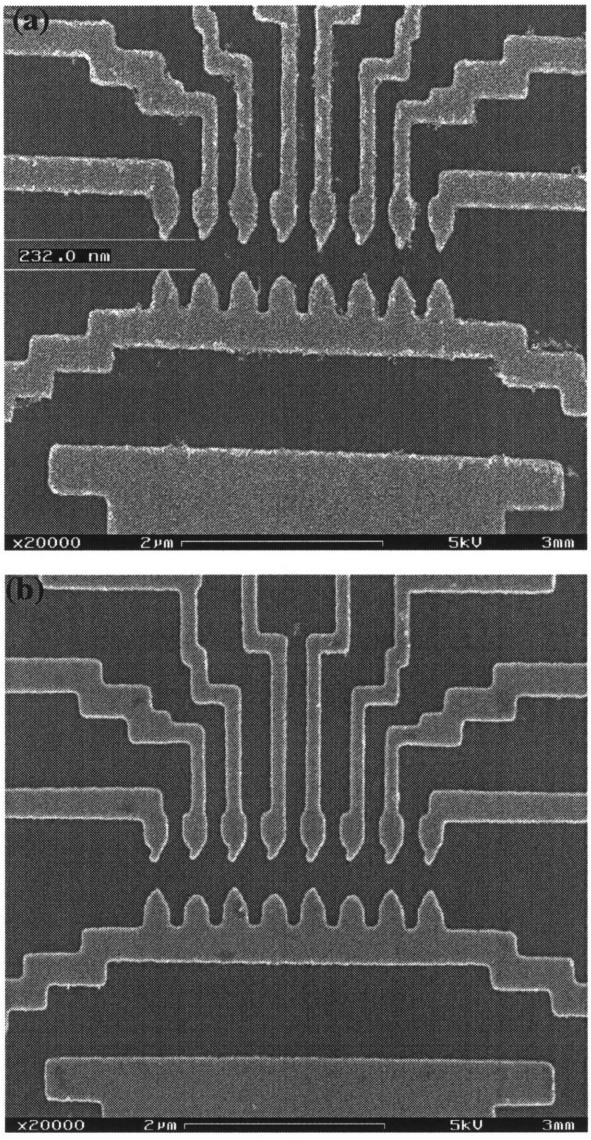

Figure 3.6: (a) AuPd evaporated gates with regular (soaking) lift-off. (b) AuPd evaporated gated with spray lift-off.

Gold-palladium is preferred for extremely fine feature sizes because of its small grain size. However, its lift-off process is more complicated. When thermal evaporation is used for subsequent lift-off process, there always is some side wall coating. This coating occurs because in the thermal evaporator the source has a finite extent — about 5 to10 mm in diameter, for our boat type, while in the e-beam evaporation the source is much closer to a point source — about 1 mm in diameter. The wall coating thickness W is then given by

$$W = t\frac{D_s}{H_s}, \tag{3.1}$$

where t is evaporated metal thickness, D_s is the source diameter, and H_s is the height of the sample above the source. For the 50 nm film evaporated in our evaporator W=1 nm. This is smaller than the grain size for most metals, and the film of the side-walls does not form. However, for AuPd grain size is smaller, and apparently because of it some sort of side-wall coating occurs. The side-wall coating is not continuous, because the lift-off process is always successful, but the very small particles from this coating tend to fall back onto the substrate as shown in Figure 3.6 (a).

To overcome this problem spray lift-off was used. A usual way to lift-off nanometer scale features from PMMA resist is to soak the sample in a solvent for some time. Typically, acetone is used as a solvent, and soaking times as long as 2 hours are needed. Spray lift-off is always preferable to soaking lift-off, because there is less chance for redeposition. Nevertheless it is not normally used since it is impossible to spray the sample continuously for 2 hours. It was found, however, that when the sample is sprayed with acetone for about 2 minutes, the area in the close proximity (few microns) to the gates are cleared of metal. This means that there is no more danger of redeposition of gate metal in the active device area. The sample is then put into acetone, and lift-off is continued in the soak

mode. Figure 3.6 (b) shows that use of spray in the initial part of the lift-off process solves the problem of particles redepositing back onto the substrate.

Figure 3.7 shows a test quantum dot array device. The dots in the array have size of 500 by 800 nm.Figure 3.8 shows the test polarization device made for dose-matrix determination.

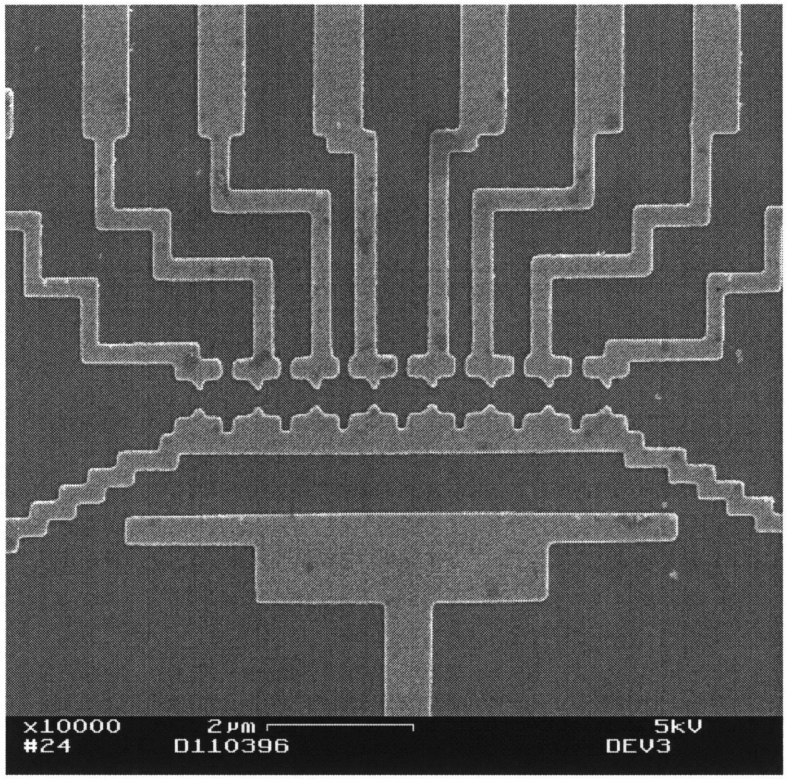

Figure 3.7: SEM micrograph of the quantum dot array with 800x500 nm quantum dots.

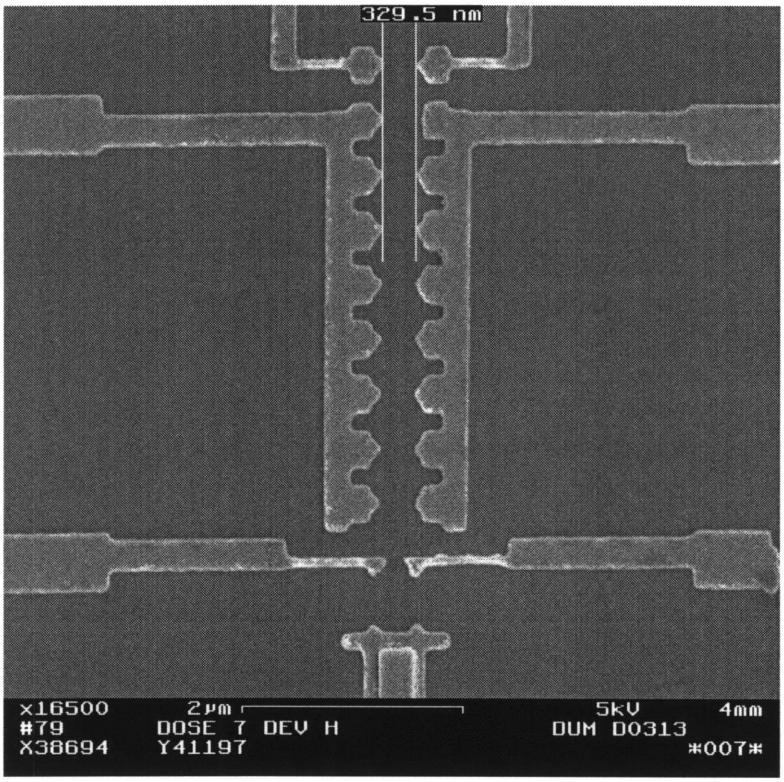

Figure 3.8: SEM micrograph of the test polarization device. The device was made for dose-matrix determination, so not all dimensions are as designed.

Chapter 4

Experimental Results

This chapter describes the measurement results of single and double dot systems. It starts by providing the necessary background of the Coulomb blockade theory. It then presents the data and provides its theoretical interpretations. Finally, it discusses the problem of drifting QPC conductances encountered in the course of measurements.

4.1 Introduction to Coulomb Blockade

The basic physics of the Coulomb blockade can be understood as follows. Consider a metal grain with charge Q and at potential ϕ capacitively coupled to several conductors, as depicted in Figure 4.1(a). The other conductors may be gate electrodes or the leads from which electrons can tunnel on to or off of the grain. The charge Q is related to the voltages on other conductors by capacitances $\{C_i\}$:

$$Q = \sum_i C_i(\phi - V_i) \tag{4.1}$$

Thus the electrostatic potential on a grain is

$$\phi(Q) = \frac{Q}{C_\Sigma} + \frac{1}{C_\Sigma}\sum_i C_i V_i \tag{4.2}$$

where $C_\Sigma = \sum_i C_i$. The electrostatic charging energy of the system is found by integrating over charge Q:

$$W(Q) = \int_0^Q \phi(q)dq = \frac{Q^2}{2C_\Sigma} + \frac{Q}{C_\Sigma}\left(\sum_i C_i V_i\right) \tag{4.3}$$

The grain can contain only integer number of electrons, therefore, the charge is $Q = -Ne$. In a typical experiment the voltage on one gate V_g is swept, while the voltages on all other

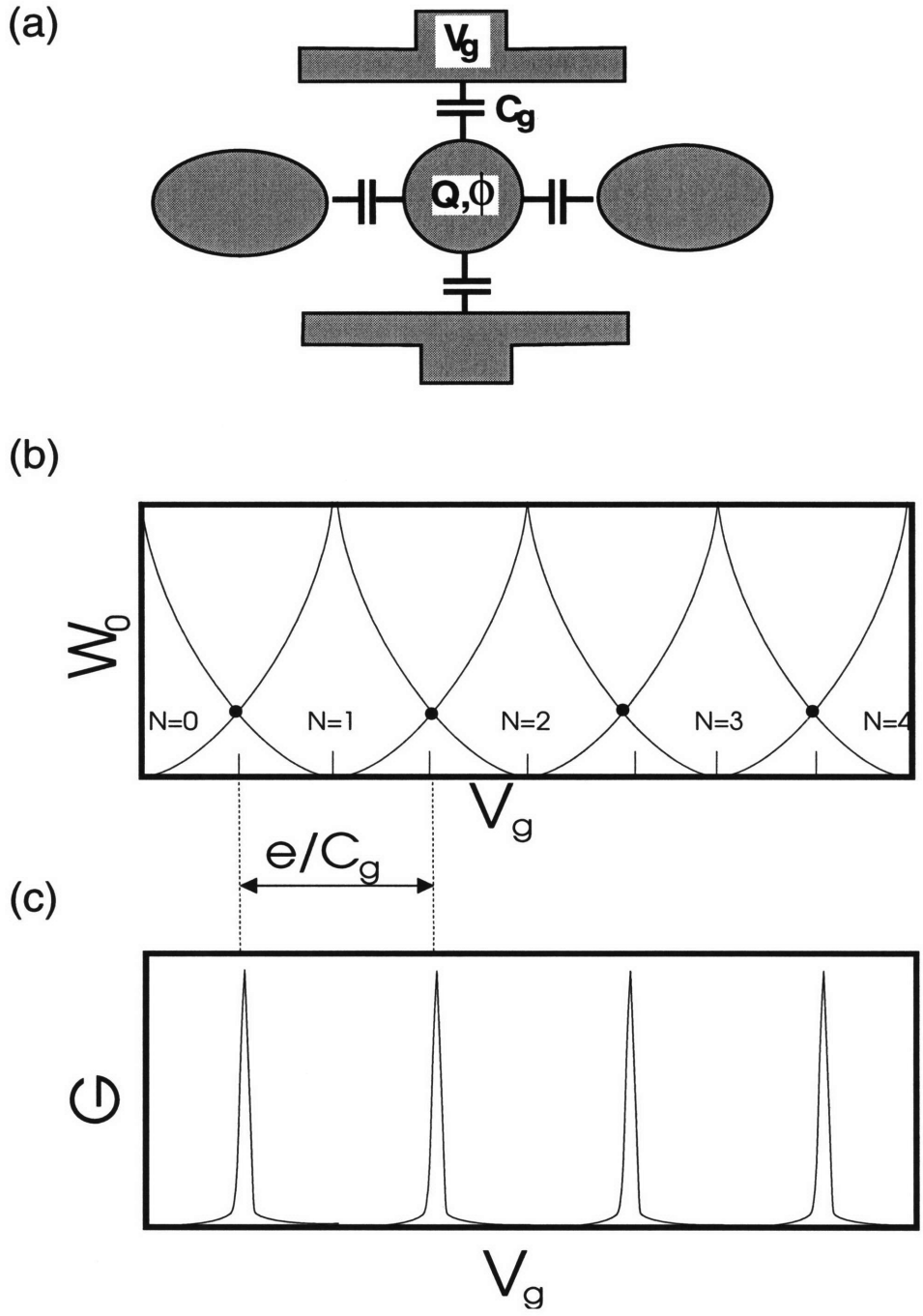

Figure 4.1: (a) Metal grain with charge Q and potential ϕ capacitively coupled to a number of other conductors, which may be leads or gates. (b) Charging energy W_0 as a function of the gate voltage V_g for several values of N. (c) Corresponding conductance through the dot as a function of V_g. Conductance peaks occur when $W_0(N, V_g) = W_0(N \pm 1, V_g)$.

gates are kept constant. Therefore, the term $\sum_i C_i V_i$ can be written as $\sum_i C_i V_i = C_g V_g + eN_0$, where $N_0 = \frac{1}{e}\sum_{i \neq i_g} C_i V_i$. The charging energy can then be expressed as a function of the electron number N and the gate voltage V_g:

$$W(N, V_g) = \frac{e^2}{2C_\Sigma}\left(N - \frac{C_g V_g}{e} - N_0\right)^2 - \frac{e^2}{2C_\Sigma}\left(\frac{C_g V_g}{e} + N_0\right)^2 \qquad (4.4)$$

We are only interested in the part of the charging energy that depends on N. Therefore, we can write the simplified charging energy W_0 as

$$W_0(N, V_g) = \frac{e^2}{2C_\Sigma}\left(N - \frac{C_g V_g}{e} - N_0\right)^2 \qquad (4.5)$$

As shown in Figure 4.1(b), the charging energy W_0 has a parabolic dependence on V_g for each value of N. For a given V_g, there is a certain N which is lowest in energy, except at the points where $V_g = \frac{e}{C_g}(N - N_0)$, where the parabolas $W_0(N)$ and $W_0(N+1)$ cross each other. As result, at low temperatures current is suppressed everywhere except at the crossing points, giving rise to the peaks in G_{dot} as shown in Figure 4.1(c). The peaks are periodic with a period $\Delta V_g = e/C_g$.

4.2 Measurement electronics.

A schematic of a typical measurement setup is shown in Figure 4.2. A low frequency AC voltage is applied to the source of the device, and the current is measured at the drain. The frequency is typically 77 Hz, and the amplitude is 50 μV. The amplitude was chosen to be less than the thermal excitation 3 k_BT, which is approximately 75 μV at 300 mK. The choice of frequency is a result of a compromise between the desire to use a lower frequency in order to eliminate capacitive coupling between source and drain on one hand, and the desire to use a higher frequency in order to decrease the 1/f noise on the other hand. The drain current is amplified by an Ithaco 1112 low noise current preamplifier,

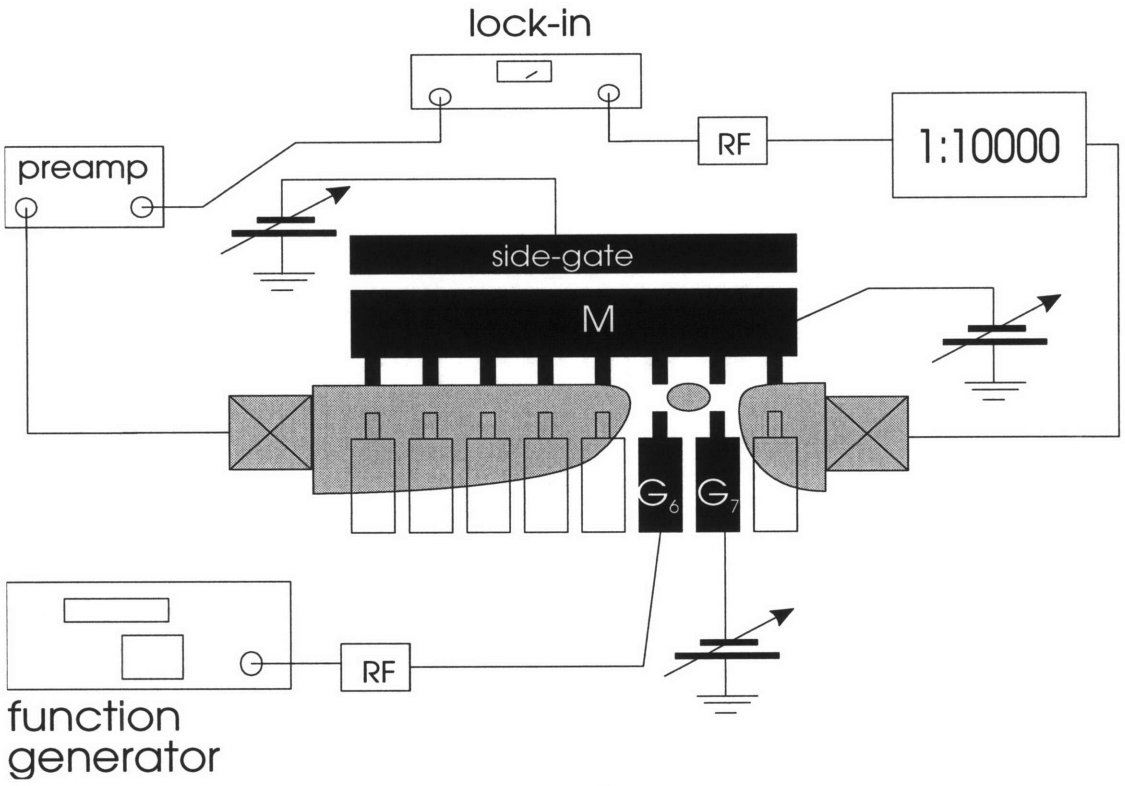

Figure 4.2: Schematic of measurement setup

operating on battery power, and then measured by PAR 5210 lock-in amplifier. The AC excitation voltage is generated by the internal function generator of the lock-in, and then reduced by a passive 1:10000 divider/bias box. The reader is referred to Appendix B for the detailed description of the electronic circuitry.

A quantum dot is created by applying negative DC voltages on the gate M and any pair of the adjacent gates $G_1 \ldots G_8$. Double dot and larger systems are created by energizing appropriate number of adjacent numbered gates. The constant gate voltages were set using battery-operated voltage sources and occasionally computer controlled DAC board with appropriate filtering system, all described in more detail in Appendix B. The variable gate voltage was set using an HP 3325B function generator.

It is essential in my experiments that electrical noise level does not exceed the thermal energy of 75 μV at 300 mK. Therefore, great care was taken to use only shielded twisted

pair leads, and to put a commercial Pi RF filter (30 kHz cut-off) on every lead in order to eliminate digital noise coming from the measurement electronics.

4.3 Single Dot Experiments

4.3.1 Preliminary Experiments

The sample MBE33ab1 was bonded to a 44 pin chip carrier, loaded into ^{3}He cryostat and cooled to 300 mK. The operation of the cryostat is described in detail in Ref. [1] and [2]. The first device investigated was a 600 nm period array.

The first step in measuring the fabricated device was to characterize independently each of the eight Quantum Point Contacts (QPC's). To this end, gate M was swept together with each of the gates $G_1 \ldots G_8$. As shown in Figure 4.3, the pinchoff characteristics are marked by a clear 2-d to 1-d transition at $V_g \approx -0.3$ V. In the 1-d regime an ideal QPC is supposed to show well resolved conductance steps quantized in multiples of

$$\sigma_Q = \frac{2e^2}{h} = 77.48\ \mu\text{S} \tag{4.6}$$

In our case, most of the steps are washed out by a series of bumps and dips, which are different for each QPC, but reproducible within a period of time of several hours. This indicates the presence of scattering centers in the 1-d channel. The presence of scattering centers, however, does not prevent us from proceeding with further measurements since it was shown in Ref. [3] that the Coulomb blockade effects can be seen in a MOSFET inversion layer even when all the transport is diffusive. Since gates G_6 and G_7 have the cleanest pinchoff characteristics, they were chosen for further experiments to form a single quantum dot.

4.3.2 Gate capacitances

Next important step in the investigation was to observe Coulomb blockade oscillations and measure gate-to-dot capacitances for each of the gates. The gate-to-dot capacitance of a particular gate is determined from a period of Coulomb blockade peaks when this gate is

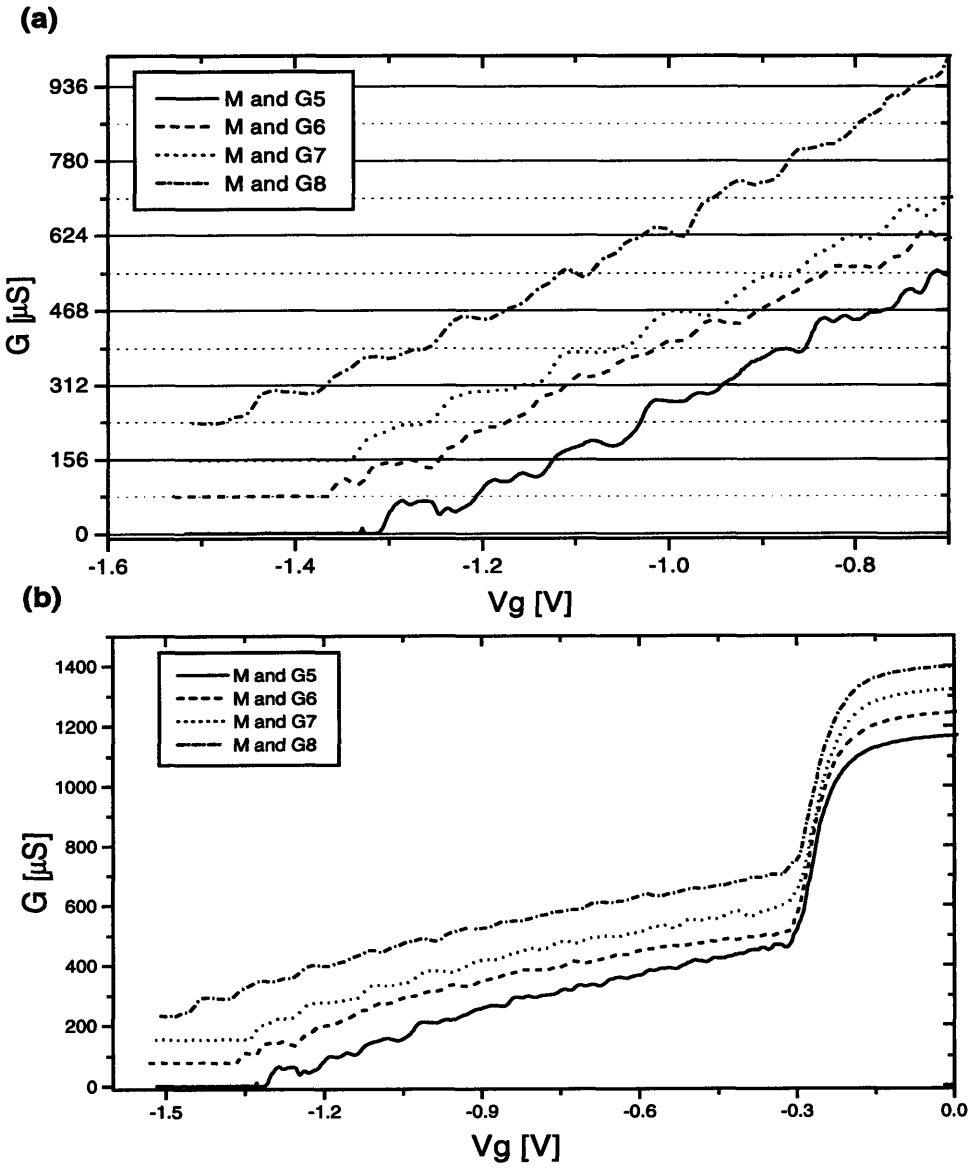

Figure 4.3: (a) Pinchoff curves for gates G5-G8 showing quantized conductance steps. (b) Demagnified view of the pinchoff curves showing 2-d to 1-d transition. Successive curves are offset by 77 μS for clarity.

being swept e.g.

$$C_{gd} = \frac{e}{\Delta V_g} \tag{4.7}$$

The conductance oscillations are strongest when both barriers are tuned to be identical in transmission, and each one has a conductance $G_{barrier} \approx 77\ \mu S$. I used the following method to tune the barriers. First, the voltage on gate M was set to -1.2 V (or sometimes

some other fixed value). Then, voltages on gates G_6 and G_7 were set to -1.0 V. Since all gates pinch off at below -1.2 V, the conductance of the device would still be about 100 μS. After that, the voltage on gate G_6 was made more negative until the conductance fell to 10 μS. The voltage on G_6 was recorded, the gate was returned to -1.0 V, and the procedure was repeated for G_7. Because of the small spacial extent of the device, voltage on one gate strongly influences the conductance through the barrier created by the other gates. Thus the final conductance through each QPC will be smaller than 10 μS. However, since the voltage on each gate is only changed by 200-300 mV, from their initial -1.0 V value, the cross-coupling is minimized.

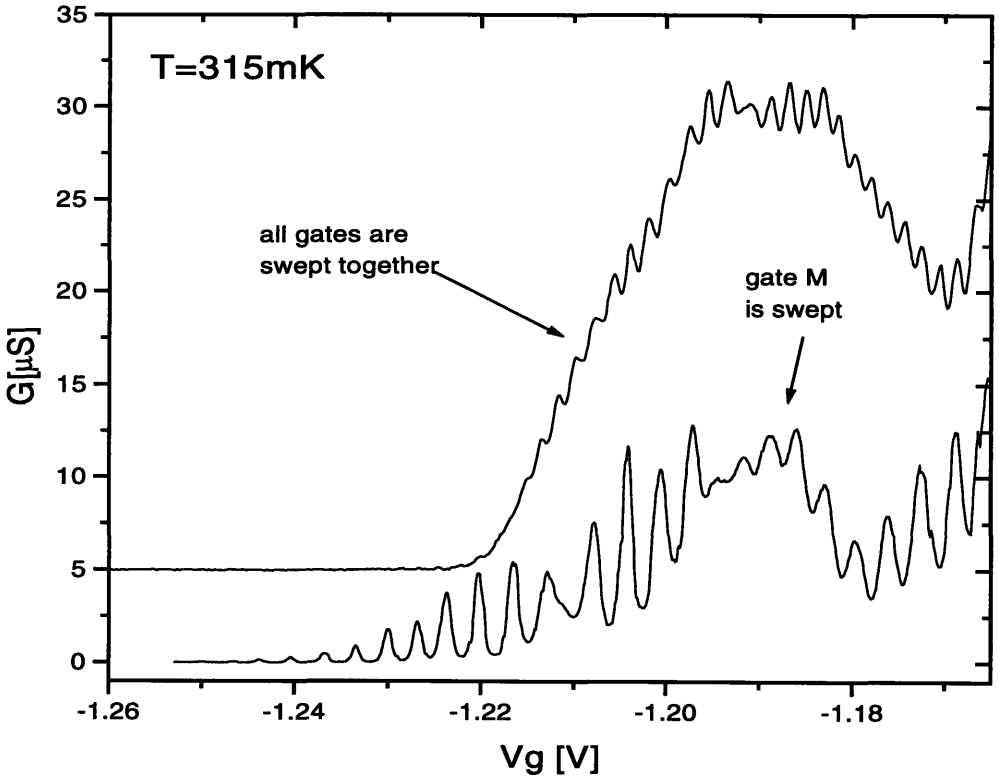

Figure 4.4: Conductance of a single 600x500 nm dot. Bottom curve: gate M is swept. On the top curve, offset by 5 μS for clarity, all gates are swept simultaneously.

Figure 4.4 and Figure 4.5 show a plots of conductance for the dot with gates M, G_6, G_7 being swept. The capacitances calculated from the peak spacing are: $G_{G6\text{-}d}$=23 aF,

$C_{G7\text{-}d}$=24 aF and $C_{M\text{-}d}$= 48 aF. Note, that from geometrical considerations we should expect capacitances of gates G_6 and G_7 to be very close to each other, and they sum to be approximately equal to capacitance of gate M, which is indeed the case.

In order to validate the previous capacitance values, conductance of the dot was also measured when all three gates G_6, G_7 and M are swept simultaneously. In that case the transmission through the left and right QPCs is not going to be the same. Nevertheless, weak periodic oscillations in conductance were observed, as shown in Figure 4.4. The period of these oscillations corresponds to total capacitance of gates G_6, G_7 and M of 96 aF, which is in excellent agreement with the sum of the gate capacitances measured individually.

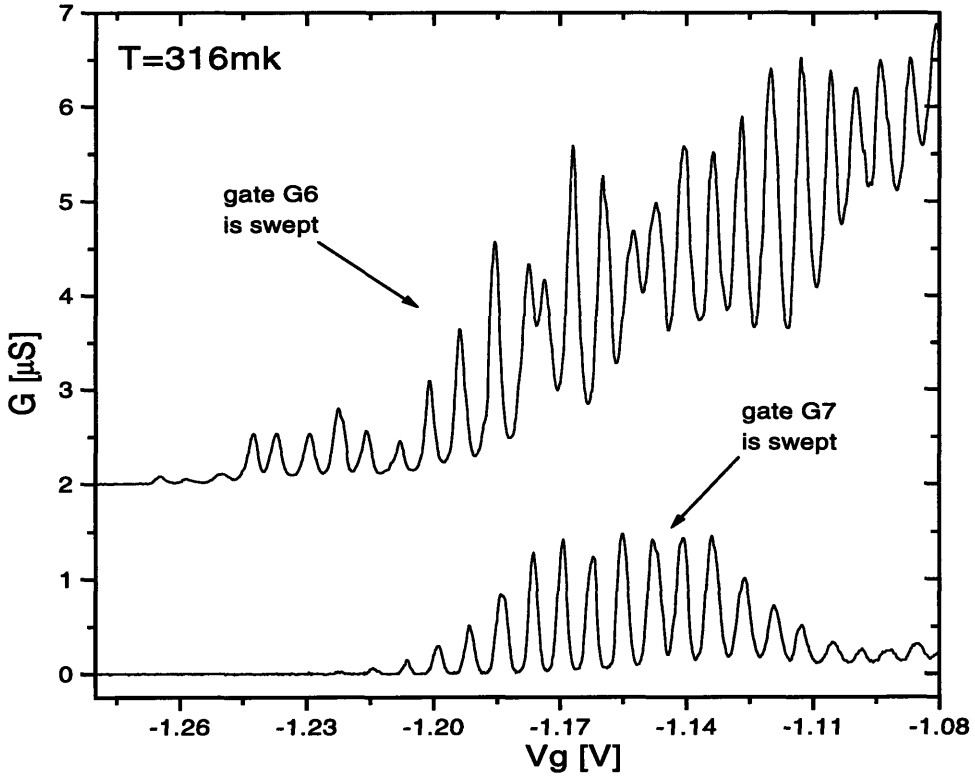

Figure 4.5: Conductance of a single 600x500 nm dot. Gates G_6, G_7 swept. The curve of G_6 being swept is offset by 2 μS for clarity.

The gate-to-dot capacitance of the side-gate was similarly measured by sweeping it. Figure 4.6 shows a plot of conductance for the dot with side-gate being swept. The side-gate capacitance calculated from the peak spacing is C_{sg-d}=9 aF. Whenever the side-gate was used in subsequent experiments, it was always biased below the 2-d to 1-d transition, typically in the -0.4 V to -0.8 V range. This was done because in the 2-d regime the side gate also controls the density of 2DEG directly under it. But since this region of 2DEG directly under the side-gate acts as a partial shield between the dot and the side gate, the gate to dot capacitance might be dependent on the side-gate voltage.

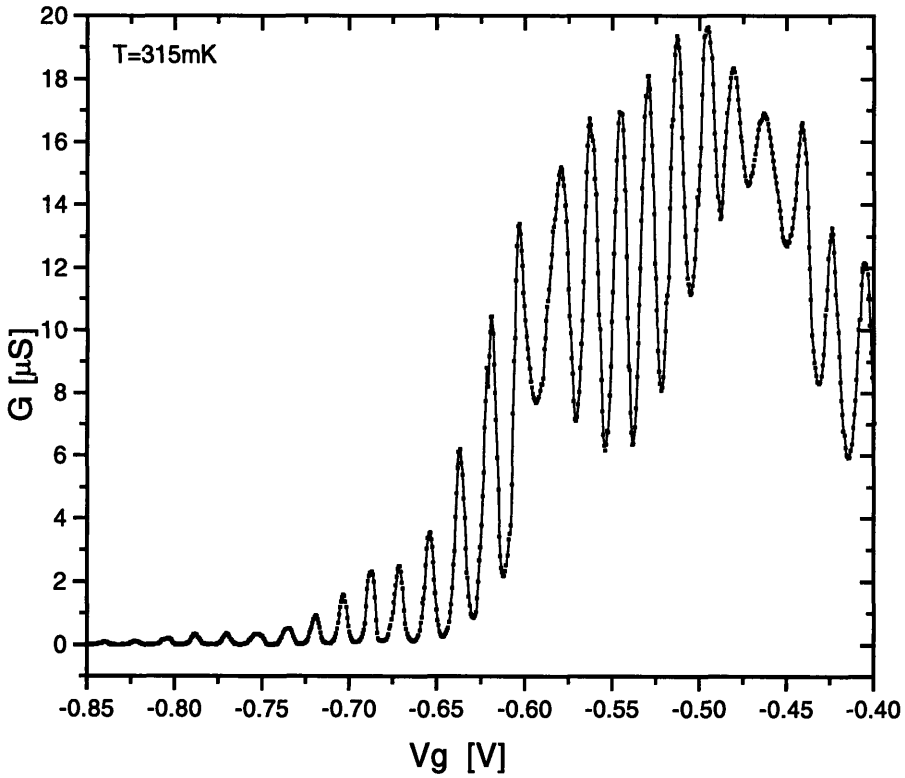

Figure 4.6: Conductance of a single 600x500 nm dot. Side-gate is swept.

4.3.3 Temperature dependence of the peak width

The temperature dependence of the peak height and shape was studied in several references by Kulik and Shekhter [23], van Houten, Beenakker, and Staring [24] and others. In the classical limit the thermal energy is significantly larger then the quantum energy level

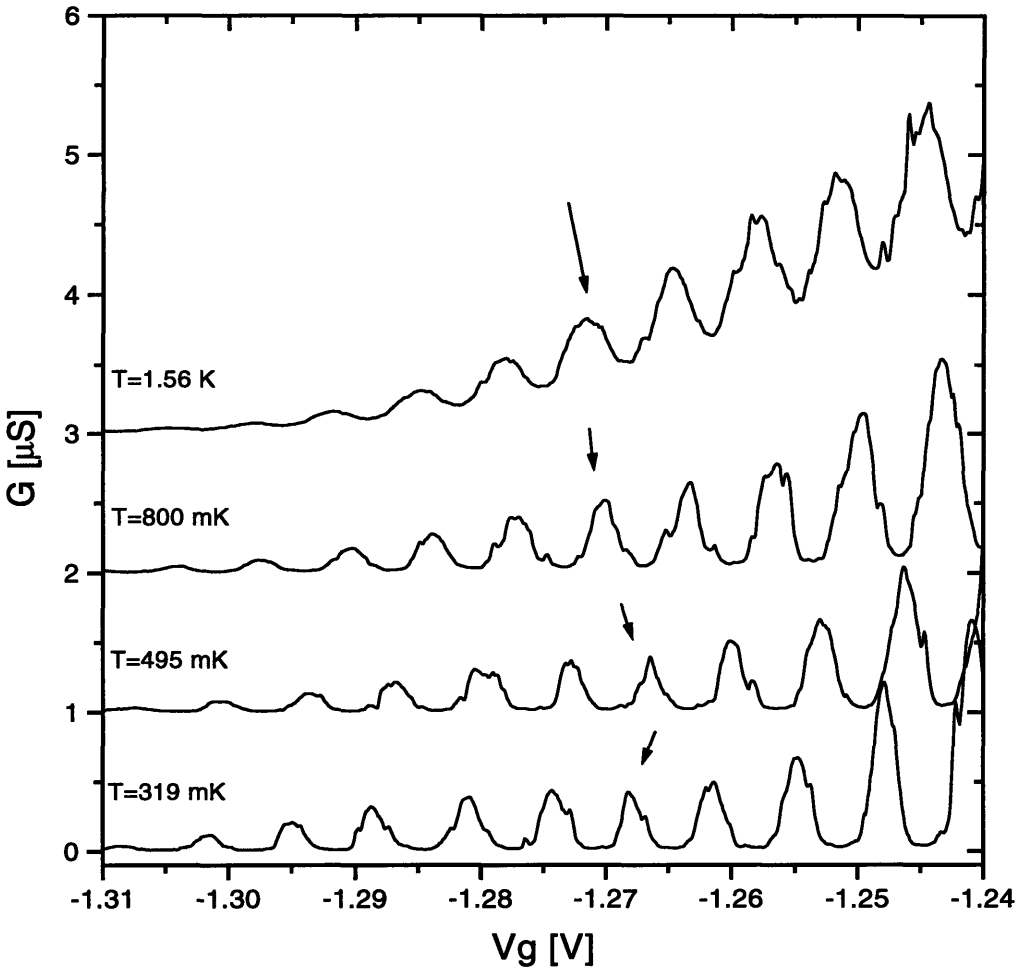

Figure 4.7: First few peaks in the single dot conductance curve measured at different temperatures from 320 mK to 1.6 K. Peak positions have drifted in the course of measurements. Peaks marked by arrows were used for the curve fits the eq. (4.8)

spacing in the dot, but is still much the smaller then the charging energy, e.g. $\Delta E \ll k_B T \ll e^2/C_\Sigma$. In that case the line shape of the peak is given by

$$G(V_g) = G_{max}\cosh^{-2}\left(\frac{e\alpha(V_g - V_0)}{2.5k_B T}\right) \tag{4.8}$$

$$G_{max} = \frac{e^2}{2\Delta E}\frac{\Gamma_l \Gamma_r}{\Gamma_l + \Gamma_r} \tag{4.9}$$

where $\alpha = C_g/C_\Sigma$ and $\Gamma_{l(r)}$ are tunneling rates between the dot and the left (right) lead[1].

1. A factor of 2.5 in equation (4.8) comes from the approximation $x/\sinh(x) \approx 1/\cosh(x/2.5)^2$.

Therefore, the total capacitance of the dot C_Σ can be extracted from the fits of the peak shape with the equation (4.8). Figure 4.7 shows a few peaks in the conductance curve of the dot formed by gates M, G_6 and G_7 measured at different temperatures from 320 mK to 1.6 K. Gate G_7 was swept in that experiment. As expected, peaks became wider at higher temperatures, and at T=1.56 K there is a monotonically increasing background. The presence of the background indicates that at this temperature thermal energy of the electrons exceeds the height of the tunnel barrier. Note also, that the peak positions have drifted in the course of the measurements. Peaks marked by arrows were used for the curve fitting. Figure 4.8 shows the resulting fits of the data to the equation (4.8) with three fitting param-

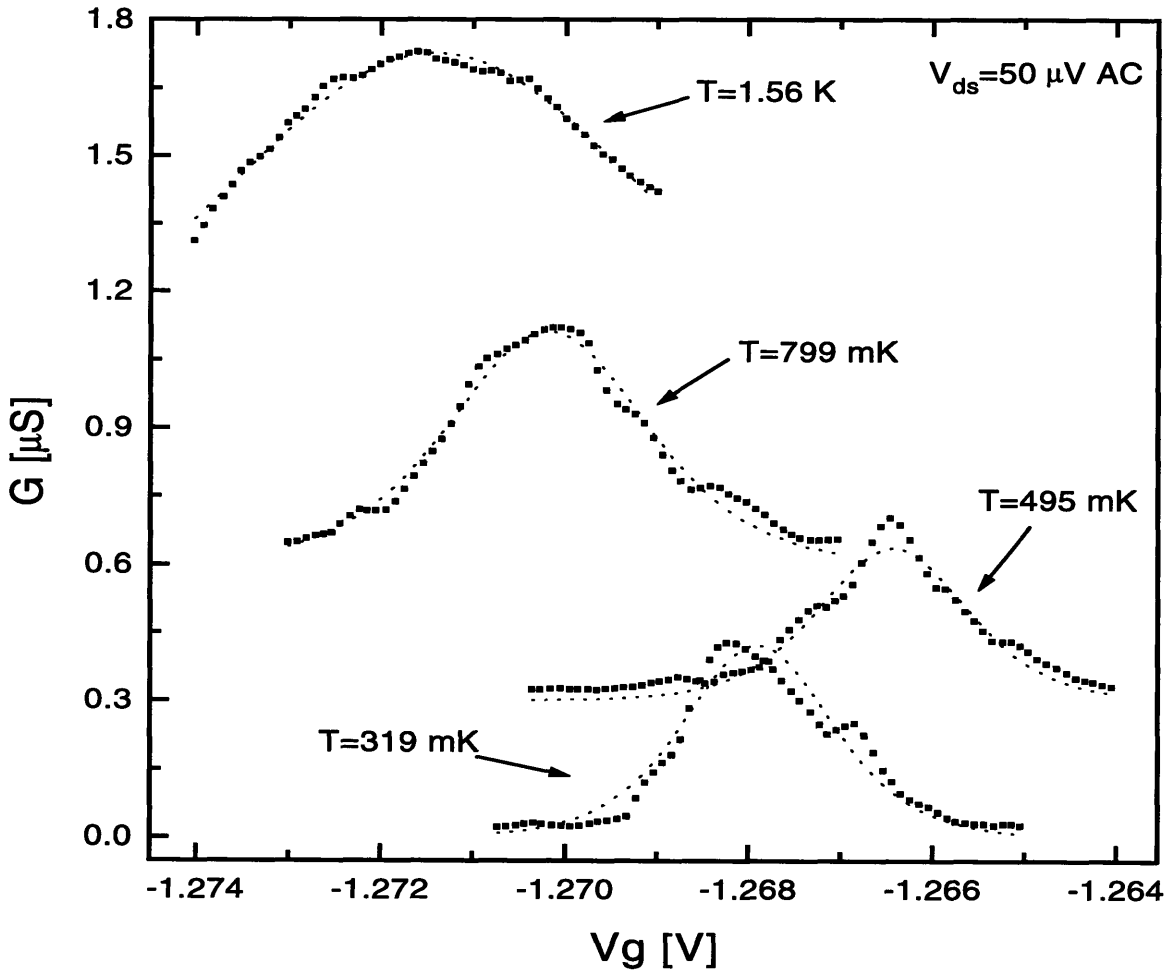

Figure 4.8: Fits of the dot conductances measured at different temperatures with eq. (4.8). Curves are offset by 0.3 μS for clarity.

eters: G_0, V_0, and T/α. Where G_0 controls the height of the peak, V_0 controls its position, and T/α controls the width of the peak. At the temperatures below 1 K the temperature measured by the thermometer is not necessary the same as the temperature of the 2DEG. This is due to the fact that the resistor used for the temperature measurements is located a few centimeters away from the sample, and also partially due to the thermal de-coupling of the 2DEG from the lattice. Therefore, it is necessary to include the temperature T in the fitting parameters.

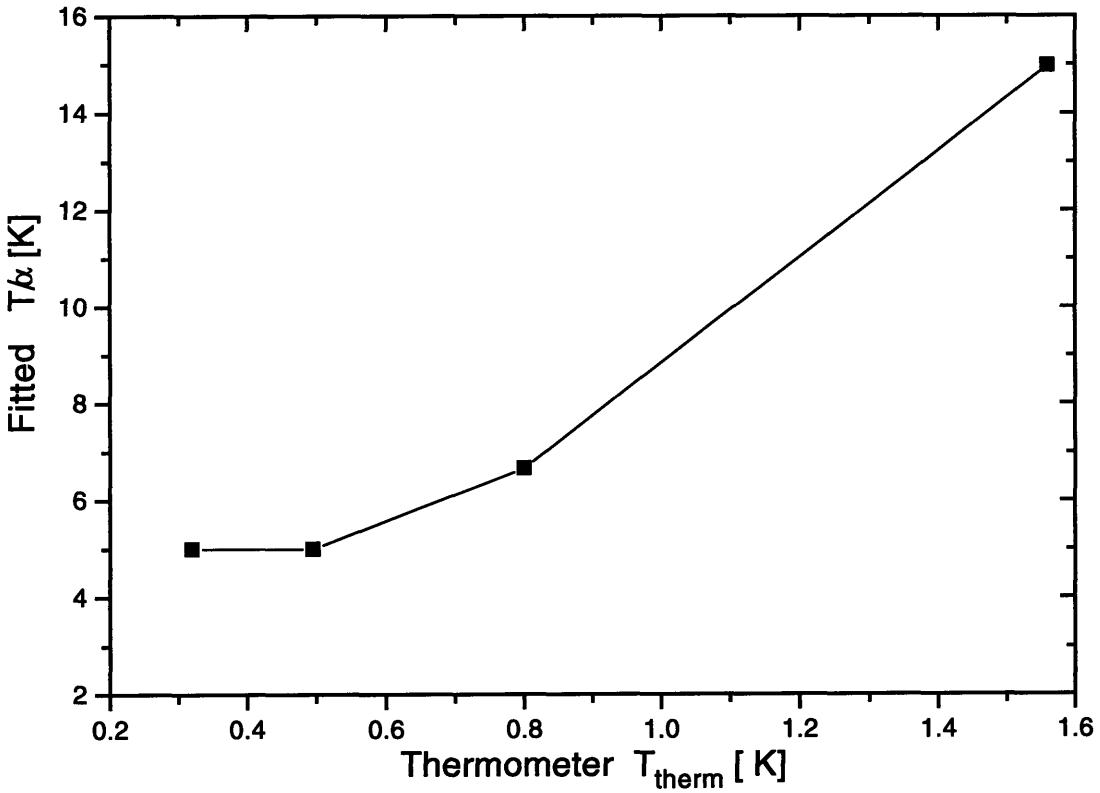

Figure 4.9: Fitting parameter T/α versus thermometer temperature T_{therm}.

Figure 4.9 shows the fitting parameter T/α plotted versus measured thermometer temperature T_{therm}. The dependence is not linear as it would be if $T_{therm}=T_{2DEG}$, but the curve saturates at T_{therm}=500 mK. That indicates that the 2DEG temperature saturates at about 500 mK, and it never reaches the nominal base temperature of 300 mK. To estimate the

total capacitance of the dot C_Σ the value of $\alpha = 0.11$ at T_{therm}=1.56 K was used because at this high temperature the 2DEG and thermometer temperatures have to be the same. That value of α results in the value of $C_\Sigma = 250$ aF. This value is in good agreement with the estimated total capacitance of the disk with diameter D, which can be found as $C_\Sigma = \pi\varepsilon\varepsilon_0 D = 198$ aF for a 500x600 nm dot.

4.3.4 Current-Voltage measurements

Current-voltage measurements provide a more direct way of measuring the total dot capacitance C_Σ and the dot-to-lead capacitance C_L. Assume that we now have a finite voltage V_{ds} on the drain. The charging energy W in the equation (4.3) can be rewritten to include V_{ds} explicitly as

$$W_0(N, V_g) = \frac{e^2}{2C_\Sigma}N^2 - \frac{e}{C_\Sigma}N(C_g V_g + C_l V_{ds} + eN'_0) \tag{4.10}$$

The change in free energy when the electron tunnels between one of the leads and the dot can be found as the difference between the charging energies of initial and final states minus the work done by the batteries on the leads e.g. $\Delta F = \Delta W_0 - W_{leads}$. Assuming that the dot is at the same potential as source and that source and drain capacitances are the same, we can write

$$\Delta F_l(N \to N+1) = W_0(N+1) - W_0(N) - (-eV_{ds}) \tag{4.11}$$

$$\Delta F_l(N \to N-1) = W_0(N-1) - W_0(N) - (eV_{ds}) \tag{4.12}$$

$$\Delta F_r(N \to N+1) = W_0(N+1) - W_0(N) \tag{4.13}$$

$$\Delta F_r(N \to N-1) = W_0(N-1) - W_0(N) \tag{4.14}$$

If in all four cases the change in free energy is positive, there are no energetically favorable transitions, and the current is suppressed by the Coulomb blockade. Substituting equation (4.10) into equations (4.11)—(4.14) we obtain the following conditions for the dot to be in the Coulomb blockade region:

$$N - N'_0 + \frac{1}{2} > C_g \frac{V_g}{e} - (C_\Sigma - C_l)\frac{V_{ds}}{e} > N - N'_0 - \frac{1}{2} \tag{4.15}$$

$$N - N'_0 + \frac{1}{2} > C_g \frac{V_g}{e} + C_l \frac{V_{ds}}{e} > N - N'_0 - \frac{1}{2} \tag{4.16}$$

Thus, the Coulomb blockade region has a shape of a parallelogram, and the borders between the conducting and non-conducting regions have slopes

$$S_+ = C_g/(C_\Sigma - C_l) \tag{4.17}$$

$$S_- = -C_g/C_l \tag{4.18}$$

as shown in Figure 4.10 .

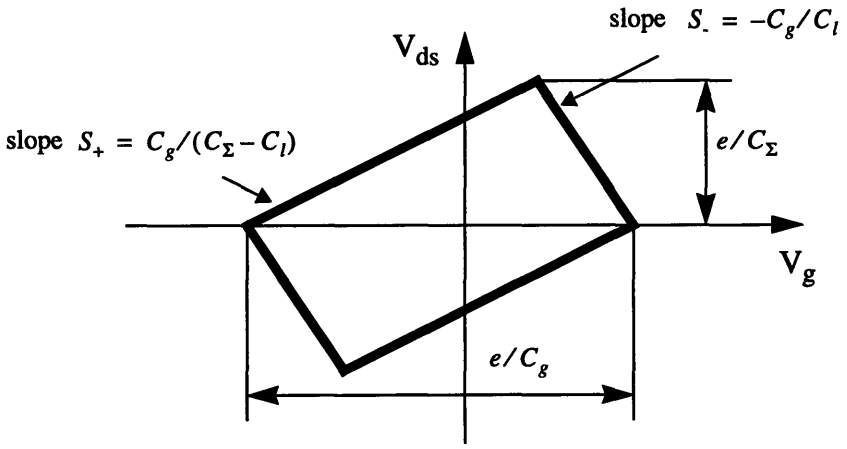

Figure 4.10: Schematic of one region of Coulomb blockade illustrating how various dot capacitances are determined.

The measurements of I_{ds} vs. V_{ds} in DC mode suffered from poor signal-to-noise ratios, and, therefore, the deferential conductance $\frac{dI}{dV}$ was measured instead. In this experiment small AC excitation (50 μV) is applied on top of the DC drain voltage. This was done using the passive bias box described in Appendix B. The AC current signal measured by the lock-in amplifier is then proportional to the differential conductance $\left.\frac{dI}{dV}\right|_{V_{ds}}$.

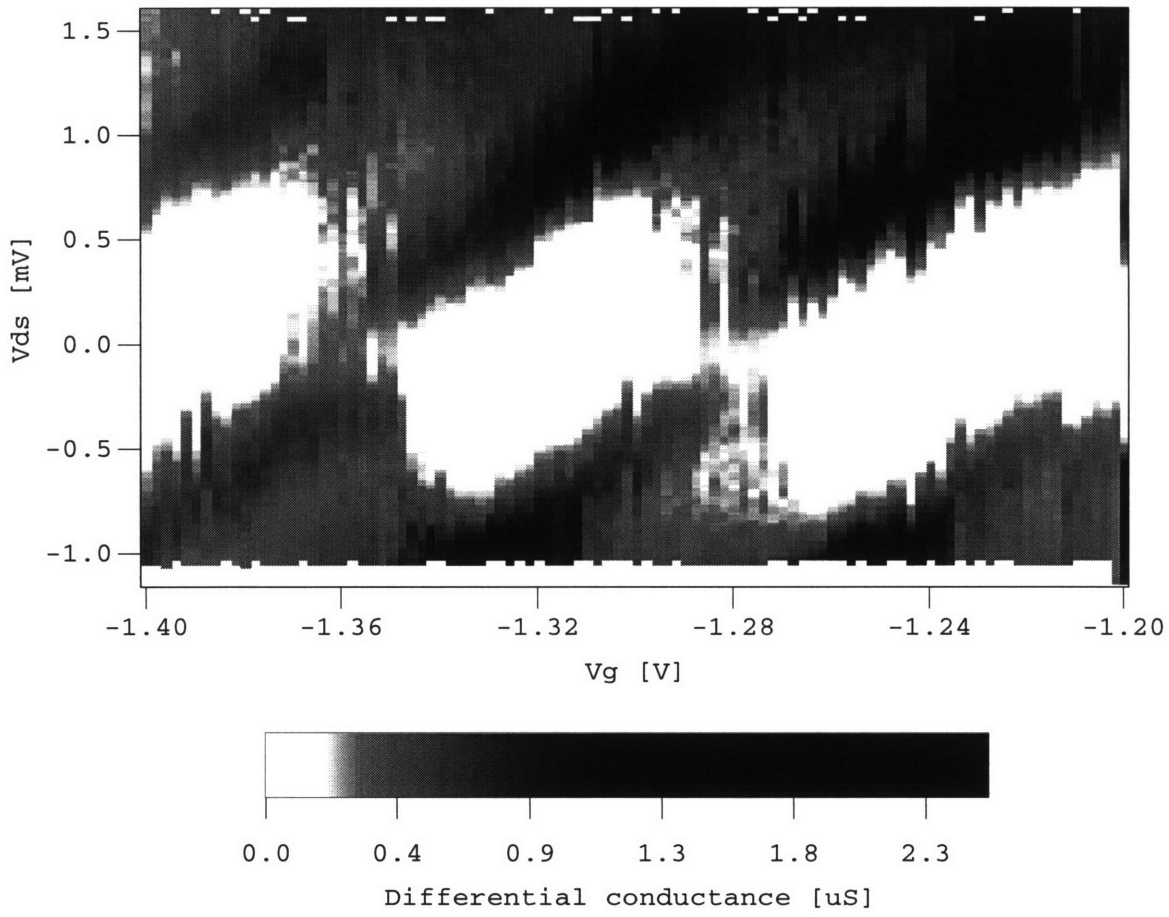

Figure 4.11: Grayscale plot of the differential conductance of the dot formed by gates M, G_6, G_7 as a function of gate and drain voltages.

Figure 4.11 shows a grayscale plot of the differential conductance of the dot formed by gates M, G_6, G_7 as a function of side-gate and drain voltages. The white regions in the plot represent the regions of the Coulomb blockade where no conduction is possible. From this Figure we can estimate $C_g = 2.1$ aF , $C_l = 58$ aF, and $C_\Sigma = 208$ aF. Note, that the value of $C_g = 2.1$ aF is inconsistent with the one obtained from the linear conductance measurements $C_g = 9$ aF. The major difference in the two experiments is that while in the linear conductance measurements it takes about 2 minutes to complete the sweep, in the differential conductance measurement it takes about 2 hours to sweep V_g by the same amount. Thus, the rate of sweeping the V_g becomes comparable to the drift rate of the sample, and

as result, the value of C_g is grossly distorted. Note, that in the Figure 4.10 the values of C_l and C_Σ are invariant under transformation $V_g \to \alpha V_g$. Therefore, the values of C_l and C_Σ should not be affected by the sample drift.

4.4 Double dot experiments

After we have made sure we do indeed have a quantum dots with a reasonable values for their capacitances, we proceeded to repeat a double dot experiment first reported by Waugh et al. [6].

To understand conductance mechanisms through the double dot system, consider the circuit schematics shown in Figure 4.12. I will assume that the dots have the same size, and that the capacitances from the dots to the side gate are the same, which is a good approximation for my system. Therefore, $C_{\Sigma 1} = C_{\Sigma 2} = C_\Sigma$, $C_{g1} = C_{g2} = C_g$ and $C_{l1} = C_{l2} = C_l$. The dots are coupled through the capacitance C_{dd}, and the capacitance

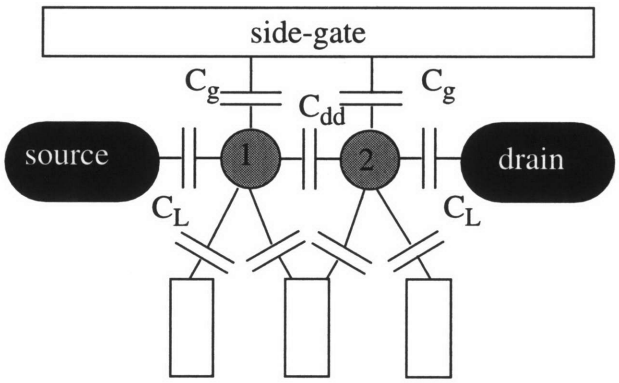

Figure 4.12: Schematics for the double dot system

between the dot i and the gate j will be denoted as C_{ij}. As in the case one quantum dot the charges on the dots can be written as

$$Q_1 = \sum_i C_{1i}(\phi_1 - V_i) + C_{dd}(\phi_1 - \phi_2) \tag{4.19}$$

$$Q_2 = \sum_i C_{2i}(\phi_2 - V_i) + C_{dd}(\phi_2 - \phi_1) \tag{4.20}$$

We can solve these equations for the dot potentials to get

$$\phi_1 = \frac{1}{C_\Sigma(1-\alpha^2)}\left(Q_1 + \alpha Q_2 - \sum_i (C_{1i} + \alpha C_{2i})V_i\right) \tag{4.21}$$

$$\phi_2 = \frac{1}{C_\Sigma(1-\alpha^2)}\left(Q_2 + \alpha Q_1 - \sum_i (C_{2i} + \alpha C_{1i})V_i\right) \tag{4.22}$$

where $\alpha = C_{dd}/C_\Sigma$. The charging energy can then be found by integrating along the path in a two dimensional charge space (Q_1,Q_2)

$$W(Q_1, Q_2) = \int_0^{Q_1} \phi_1(q_1, q_2 = 0)dq_1 + \int_0^{Q_2} \phi_2(q_1 = Q_1, q_2)dq_2 \tag{4.23}$$

As in the case with the single dot we are only interested in the part of the charging energy W_0 which depends on the number of electrons on the dots N_1 and N_2 and the voltage on the gate being swept V_g. The simplified charging energy W_0 is found using equation (4.23) to be

$$W_0(N_1, N_2) = \frac{e}{C_\Sigma(1-\alpha^2)}\left[\left(N_1 - C_g\frac{V_g}{e}\right)^2 + \left(N_2 - C_g\frac{V_g}{e}\right)^2 - 2\alpha\left(N_1 - C_g\frac{V_g}{e}\right)\left(N_2 - C_g\frac{V_g}{e}\right)\right] \tag{4.24}$$

The charging energy of each electron configuration (N_1,N_2) is a parabola. However, the configurations which have $N_1 = N_2 \pm 1$ have higher lowest point energy than the configurations which have $N_1 = N_2$, as illustrated in Figure 4.13. This comes from the energy cost of interdot charging when $N_1 \neq N_2$. The conductance peaks now occur when $W_0(N, N) = W_0(N, N \pm 1)$ or $W_0(N, N) = W_0(N \pm 1, N)$ which corresponds to the gate voltages

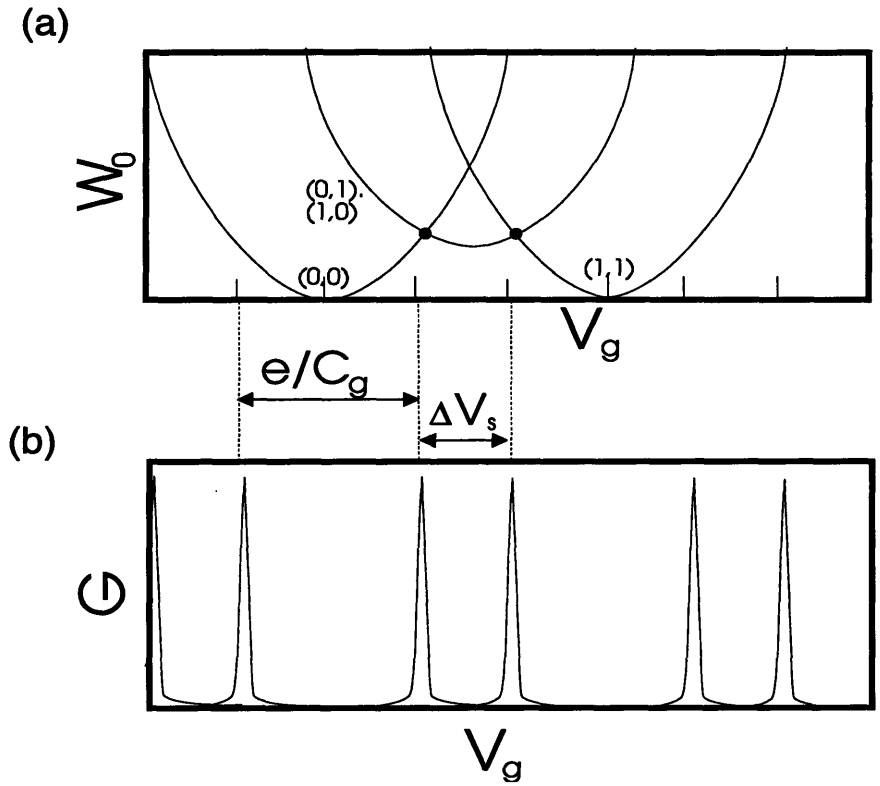

Figure 4.13: (a) Double dot charging energy vs. gate voltage. Finite interdot capacitance makes the parabolas for the odd states ($N_1 = N_2 \pm 1$) to lie higher then for the even states ($N_1 = N_2$). (b) Corresponding linear conductance. Each peak is split in two.

$$V_g = \frac{e}{C_g}\left(N + \frac{1}{2}\left(1 \pm \frac{\alpha}{1+\alpha}\right)\right) \tag{4.25}$$

The separation of the two parts of the split peak is given by

$$\Delta V_s = \frac{e}{C_g}\frac{C_{dd}}{C_{dd} + C_\Sigma} \tag{4.26}$$

We see that when $C_{dd} = 0$ (the dots are uncoupled) the period of oscillations is the same as for a single dot. As the capacitive coupling increases, the peaks are split stronger and stronger. Finally, as $C_{dd} \to \infty$ the peaks become uniform with a period of $\Delta V = \frac{e}{2C_g}$. This corresponds to a case where the dots have merged into one large dot with twice the capacitance to the gate.

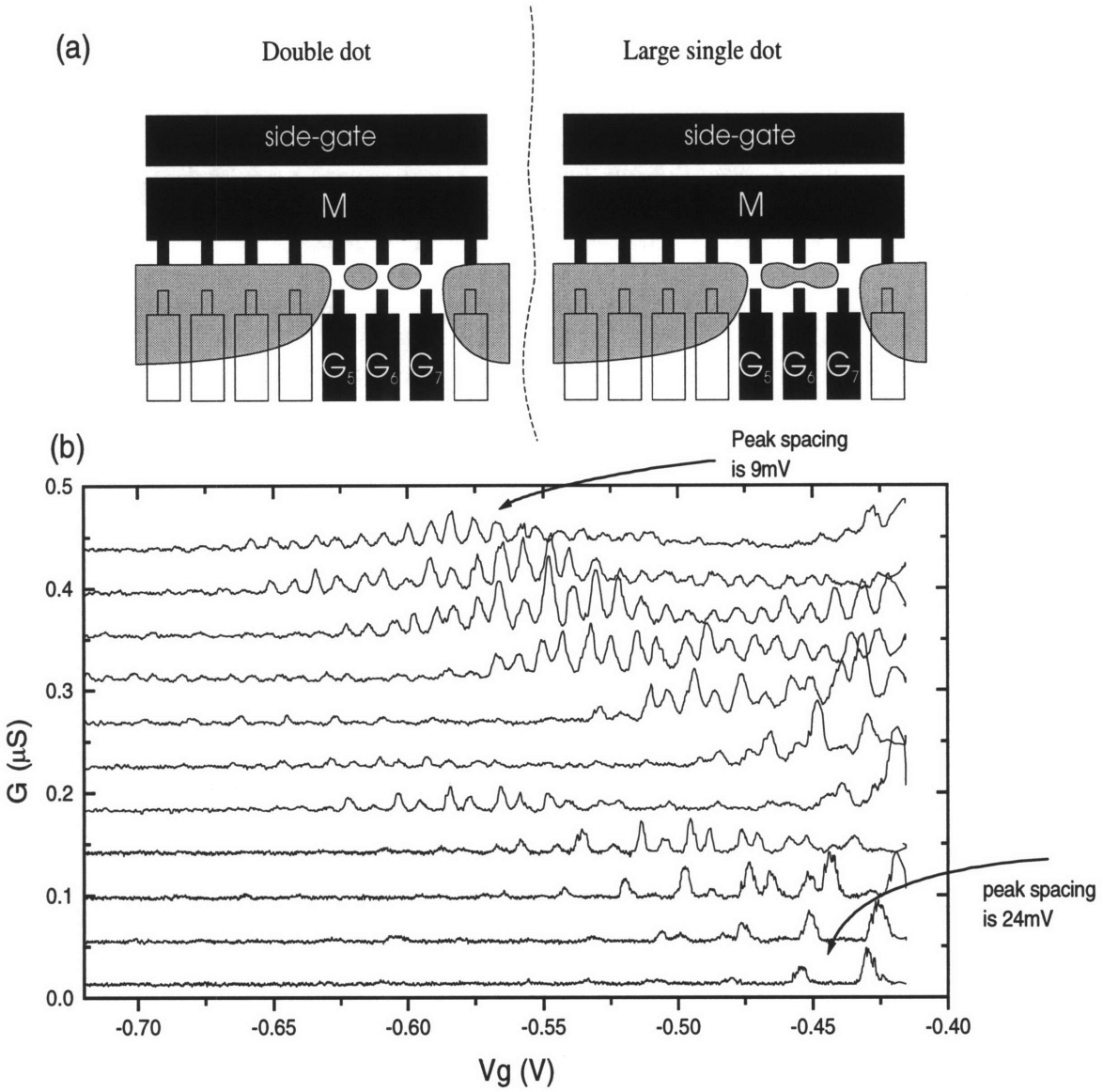

Figure 4.14: (a) Schematics of double dot experiment. By applying appropriate voltages to gates M, G_5, G_6, and G_7 we can create either a double dot or single large dot depending of the voltage on G_6. (b) Experimental results. On the bottom curve QPC G_6 is closed, so we have a double dot. As the conductance of QPC G_6 is increased for each subsequent curve each peak is split into two. When QPC G_6 is open enough so that we have a single dot, the peak spacing becomes approximately half of the period for the double dot.

The schematics of experiment is shown in Figure 4.14(a) A double quantum dot was created by applying appropriate voltages to gates M, G_5, G_6, G_7. The side-gate was then swept and Coulomb blockade oscillations were observed. Figure 4.14(b) shows changes in the pattern of Coulomb blockade oscillations with increasing inter-dot coupling. The volt-

age on G_6 was increased by 20 mV for each subsequent curve increasing conductance through QPC_6 and thus increasing inter-dot coupling. We see that for a bottom curve the period oscillations is 24 mV (corresponding to C_{sg}= 7 aF). Thus, for a system of two identical quantum dots we observe the regular peak period equal to the peak period a single dot. On the next several curves each peak is split into two peaks which move farther apart as the interdot coupling increases. Finally, on the top curve we again see regular Coulomb blockade peaks, but with a different period — 9 mV (corresponding to C_{sg}=18 aF). For this curve, the two original dots merged into one large dot which has approximately twice larger capacitance to the gate.

4.5 Drift in the sample conductances

The fact of drifting conductances in the QPCs was reported by several groups [25],[26]. In our sample, the conductance of a QPC keeps changing significantly on the scale of hours. This drift can be seen in Figure 4.7 and Figure 4.14(b). It also explains the inconsistency in the side-gate capacitance measured by linear conductance measurements and by differential conductance measurements. The drift exists at cryogenic and room temperatures in both quantum point contacts and the continuous gate FET's.

It was reported that in the samples with deeper 2DEG and higher mobilities the drift is less prominent [26]. Also, some samples from the same lot behave better then others, so the effect is not very systematic. The two major ways used to overcome this problem in the previous work were to look for the sample in which the drift is less prominent, and to take data fast, so the parameters of the QPC's do not change significantly during the course of measurements [25].

As the number of the quantum dots in the system grows, the number of gates needed to control them grows too. Therefore, it becomes increasingly difficult to bias them all cor-

rectly and take measurements in a short time. Thus, it is important to understand the physical nature of the QPC conductance drift and find ways to eliminate it.

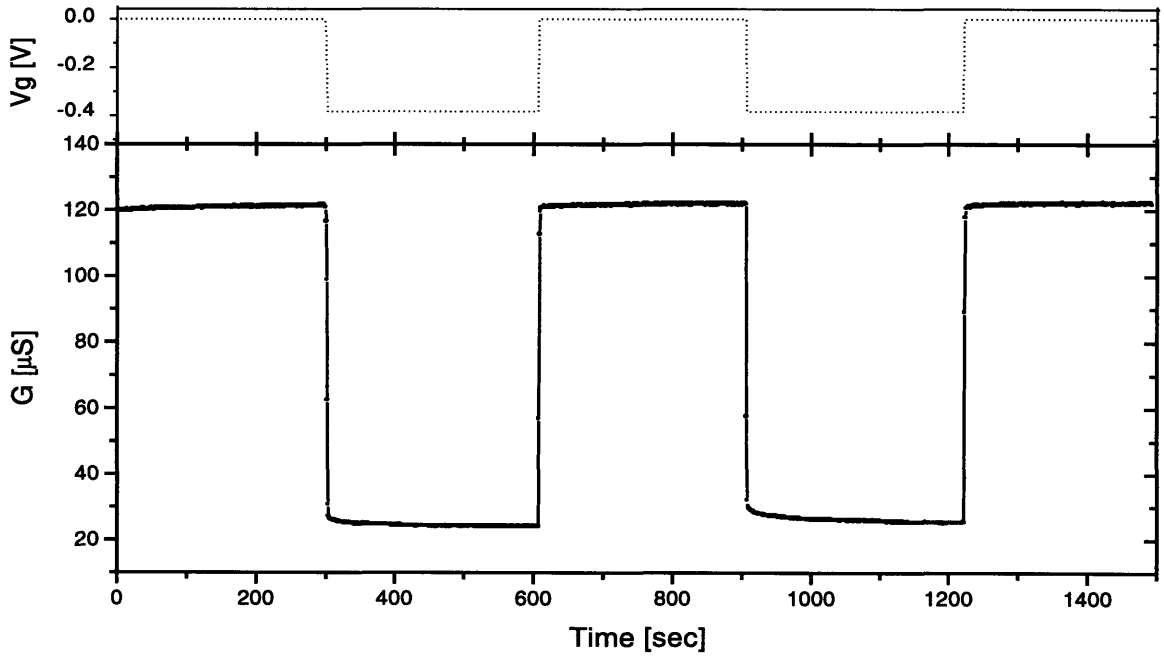

Figure 4.15: Top curve: the voltage on the gate of the FET is being periodically switched on and off. Bottom curve: Corresponding conductance of the FET measured with 50 μV AC excitation at room temperature.

We have conducted preliminary experiments aimed to obtain more understanding of the nature of the conductance drift. Figure 4.15 shows the conductance of the continuous gate FET versus time as the gate voltage was switched ON and OFF. The conductance exhibits a transient behavior after switching both from ON to OFF and from OFF to ON states.

Figure 4.16 shows the conductance of the continuous gate FET versus time for a fixed gate voltage measured at room temperature. The conductance is non monotonic — it first drops relatively fast, and then continues to rise back for the rest of the measurement. This might be an indication that there are two competing processes going on simultaneously,

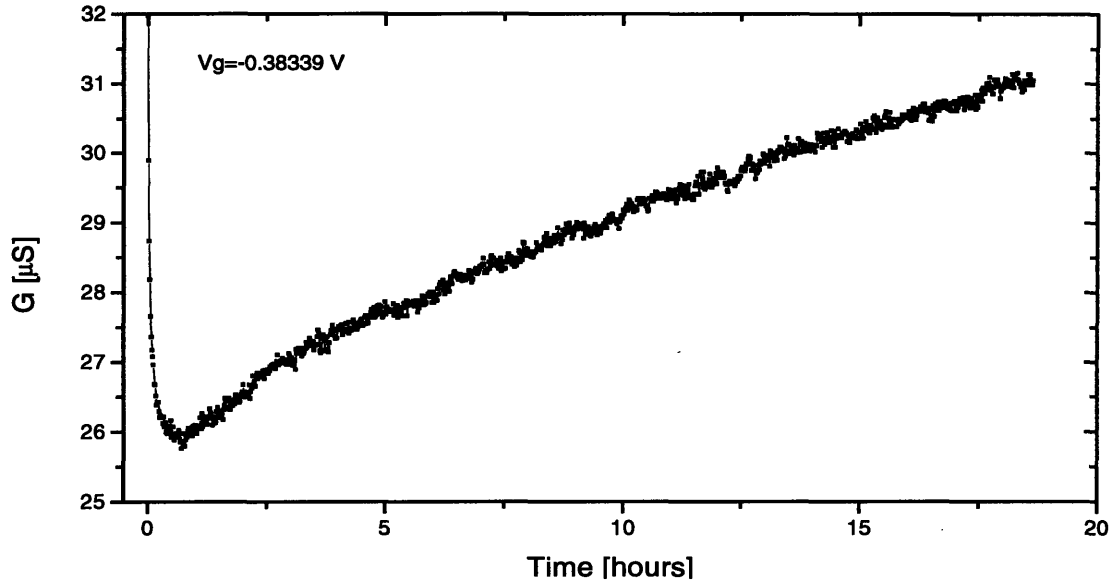

Figure 4.16: Conductance of the continuous gate FET vs. time at room temperature for a fixed gate voltage. The gate length of the FET is 5 μm. The drain-to-source voltage is 50 μV AC.

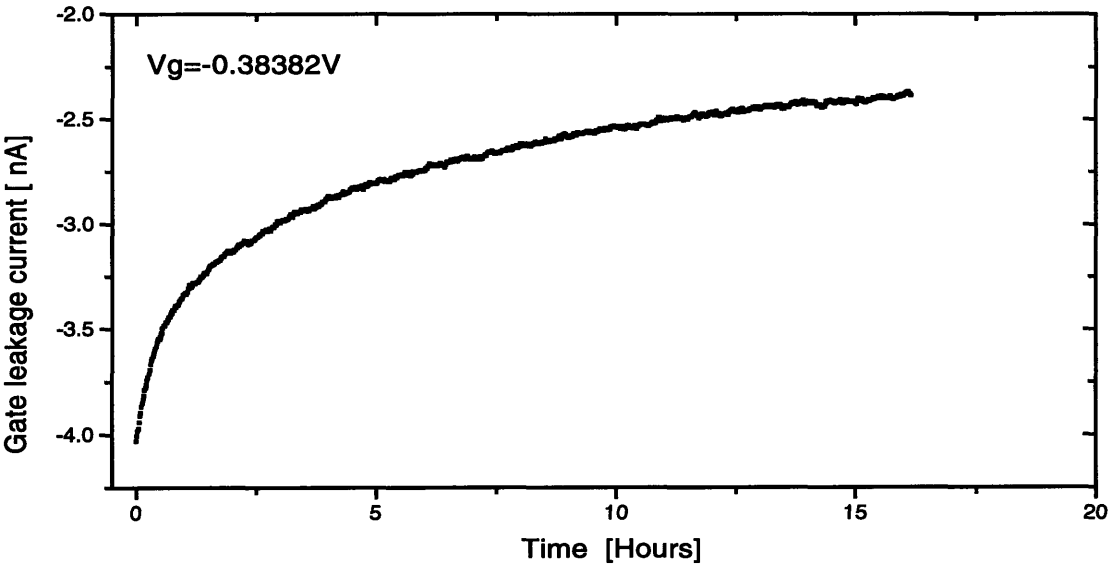

Figure 4.17: Gate leakage current of the continuous gate FET vs. time at room temperature for a fixed gate voltage. The gate length of the FET is 5 μm.

one, with the smaller time constant, which tends to decrease the conductance, and another, with larger time constant, which tends to increase the conductance.

Figure 4.17 shows the gate leakage current of the continuous gate FET versus time at room temperature for the same gate voltage as in Figure 4.16. The leakage current decreases in absolute value which indicates that a slow charging process in the bulk of the semiconductor occurs. The extra charge which probably results from the electrons being trapped by the impurities in the bulk of the semiconductor. The extra charge reduces the electric field, and thus reduces the gate leakage current.

At the present time we do not have an explanation for the above data. Clearly, more research is needed to understand the nature of the drift in the FET and QPC conductances and to find ways to minimize them.

Chapter 5

Conclusions and future work

5.1 Summary

This thesis has described the first realization and initial measurements of a linear array of seven quantum dots. The largest linear quantum dot array investigated previously contained three quantum dots.

The device was fabricated on a high mobility GaAs/AlGaAs heterostructure. Electron beam lithography was used to pattern critical features of the device, and 70 nm size resolution was achieved. A device consisting of seven quantum dots in series was built and measured at cryogenic temperatures. A commercially available ^{3}He probe was used to measure the device at 300 mK. The design of the device allowed individual control over each QPC. It also allowed creating systems of N quantum dots with N ranging from 1 to 7. Conductance oscillations as a function of gate voltage were seen for all gates in a single dot configuration and the capacitances of these gates to the dot were extracted. Temperature dependence of the conductance peak width was investigated. Total capacitance of the dot was extracted to be 250 aF. Non-linear current voltage measurements of the single dot system were made which allowed independent measurement of the total capacitance and the lead-to-dot capacitance. The total capacitance from I-V measurements was found to be 208 aF and the lead capacitance was found to be 58 aF. A double dot system was also investigated. A peak splitting was observed as the coupling between the dots is increased. For a couple of the weakly coupled quantum dots the period of conductance oscillations is essentially the same as for the single dot. As the coupling increases each peak splits into two peaks, and for very strong coupling, when the two dots merge into one large dot, the peak period is the same as for a single large dot with twice the capacitance to the gate.

5.2 Future work

Although the fabricated device can be biased to contain seven quantum dots in series, only single and double dot systems were investigated in this thesis. Therefore, a logical continuation is the investigation of the same device biased to contain three and more quantum dots. However, before this can be done the problem of drifting quantum point conductances has to be solved.

The short term solution is to take data fast, so the system does not change significantly in the course of the measurements. In order to improve the data acquisition rate one needs to by-pass the GPIB interface which constitutes the major bottle neck. Plug-in DAC and ADC cards directly controlled by computer can be used to sweep the gates and read analog outputs on the lock-in as it was done in ref [25].

In the long run, fast data acquisition is not an adequate solution. As experiments became more complicated, they require more and more time to perform them. Thus, it is important to understand the physical nature of the QPC conductance drift and find ways to eliminate it.

Appendix A

Fabrication Sequence

A.1 MESA ISOLATION

A.1.1 Solvent Cleaning of Sample and Surface Clean:

- For solvent clean, use 'TCA' 'ACE' 'METH' beakers and 'djc-solv' dipper.
- Prerinse beakers with solvent.
- Rinse sample in TCA.
- Boil in TCA for 10 min (hotplate designation ~90 deg.) It's usually a good idea to place tweezers in TCA to provide a nucleation point for boiling.
- Ultrasound in acetone for 10 min.
- Ultrasound in methanol for 10 min.
- Blow dry (run gun for a bit to get rid of particles first).
- Post-rinse beakers with solvent, let beakers dry in hood.

A.1.2 Etching GaAs/AlGaAs mesas:

- Spin Shipley 1813 resist at 4500 rpm for 30s. Use filtered syringe located in drawer below Next station.
- Bake at 90 C for 30 min. Use quadrant bowl located near ovens.
- Expose resist with mesa mask in the OAI for 3-4 sec. Exact exposure time should be determined each time using Si monitors.
- Develop exposed resist for 30s with straight Shipley CD-30 developer. Use dipper labelled 'DJC'. Rinse for 1 min rinse in DI. Use '351-1' beaker for developer and '351-2' beaker for DI. Transfer to running DI.
- Inspect in microscope.
- Continue developing in 10-15 second increments until pattern clears. Total development time should be ~45-60 sec. Pay attention to corners where resist is thickest.
- Spray mask with acetone/methanol, blow dry mask.
- Ammonium hydroxide/hydrogen peroxide etch:500 DI: 10 NH_4OH: 3 H_2O_2 in large RCA beaker (put H_2O_2 last); mix well and put small amount into 'acid' beaker. Run a monitor sample first to calibrate etch rate. Etch ~17s (=600-750A).
- Rinse in DI for 2 min. Transfer directly to running DI water in sink if possible.
- Blow dry.
- Inspect in microscope.
- Strip resist: Spray with acetone, methanol, and blow dry.
- Inspect in microscope.
- Measure mesa height in Alpha-Step.

A.2 OHMIC CONTACTS

- Solvent clean, spin and bake photoresist, expose with the OHMIC mask, and develop

(same as above).

• UV ozone for 1 min (run UV ozone for 1min before putting samples).

• Rinse in DI water for 1 min.

• Rinse in 5% NH_4OH for 15 sec Use 'SEM' beaker.

• Blow dry.

• Immediately load the sample and Si monitor into the thermal evaporator.

• When the pressure reaches 1e-6 torr, evaporate 5 nm Ni/60 nm Au/120 nm Ge/ 30 nm Ni/30 nm Au.

• Liftoff by soaking for ~10 minutes in acetone in 'L1' beaker. Then place beaker in ultrasound for ~10 sec for full liftoff. Do not use a dipper for this step. Quickly remove sample from 'L1' beaker and transfer to 'L2' beaker (also filled with acetone), spraying with acetone in-between. Remove from 'L2' beaker at your leisure, spray with acetone, then methanol, then blow dry.

• Solvent clean the sample.

• Transport the sample to the Rm 13-2111 in the vacuum container.

• Sinter in the strip heater under nitrogen atmosphere at 420 C for 30 sec. Place sample face down on solvent-cleaned piece of semi-insulating (SI) GaAs.

• Check TLM resistances at 77K using the cold probe station.

A.3 Coarse gate metallization

• Solvent clean, spin and bake photoresist, expose with the E3 mask, and develop (same as above). There are two coarse metal masks — E3 and MET. The E3 mask has alignment marks used during e-beam lithography, while MET mask is to be used to deposit second layer of the coarse metal in case there is no continuity between the first coarse metal and e-beam metal.

• Surface clean the sample before the evaporation as above.

• Evaporate 10nm Ti/ 140 nm Au in e-beam evaporator.

• Liftoff metal.

A.4 Electron beam lithography

• Solvent clean the sample.

• Spin 3.5% solution of 950K PMMA at 6000 RPM for 60 seconds for a 200 nm layer of PMMA. Bake at 180 C for 1 hour.

• Expose patterns.

• Develop in 2:3 IPA:MIBK at 21 C for 90 sec. Rinse in IPA for 30 sec and blow dry.

• Surface clean the sample before the evaporation as above. Note, that 60 seconds of UV ozone widens lines by about 20 nm. If this is not acceptable 30 sec of UV ozone might be enough, but less then 30 sec of UV ozone definitely leave the surface dirty.

• Evaporate 50-60 nm of AuPd in thermal evaporator.

• Do a spray liftoff. I have made a small mounting plate with a clip, so that a sample can be mounted on a clip and then the plate can be held comfortably with large tweezers. Held the plate with the sample over the beaker with acetone, and spray the sample with

acetone using the air brush available in the outer lab. When the acetone level in the air brush gets low, dip the plate in the beaker. (it is important not to dry the sample accidently which can happen if the acetone in the air brush runs out). Continue liftoff either by soaking in acetone for 2 hours or by soaking in hot NMP for about 10 min. When done, spray with methanol and blow dry.

• Glue the sample to the chip carrier by silver paints and bond the connecting wires. The sample is now ready.

Appendix B

Electronic circuitry

Figure B.1 shows the circuit diagram for the passive divider/bias box. The AC signal is

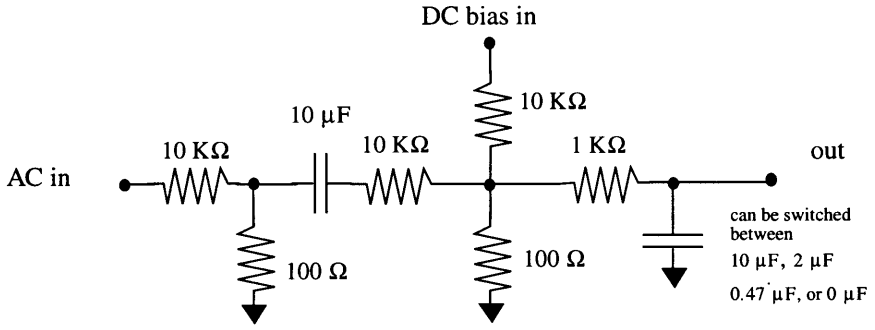

Figure B.1: Circuit diagram for the divider/bias box.

divided by a factor of 10,000, and the DC bias signal is divided by a factor of 100. The box includes a low-pass filter with a variable cut-off frequency.

Figure B.2 shows the circuit diagram for the stabilized battery powered voltage source. The AD580 voltage reference provides a fixed 2.5V voltage output independent on the

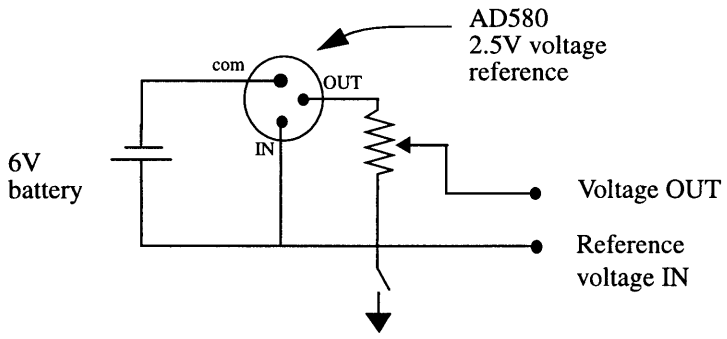

Figure B.2: Circuit diagram for the stabilized battery powered voltage source.

voltage on the battery, and the temperature. This voltage is further divided by means of a 10 turn potentiometer. The ground of the voltage source can be switched to be a external reference voltage. This is very convenient when the gate voltage is swept around some fixed value.

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