A Resonant Tunneling Diode Based Monostable Multivibrator

by

Lee Zamir

Submitted to the Department of Electrical Engineering and Computer Science
in partial fulfillment of the requirements for the degree of
Master of Engineering in Electrical Engineering and Computer Science

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ABSTRACT

Ultrafast optical time-division-multiplexed (TDM) networks will soon be capable of providing data bandwidth at rates exceeding 100Gb/s. Electronic subsystems that will perform routing and computation operations on this data currently reach speeds of 10Gb/s. An electro-optical TDM network is currently being developed at MIT's Lincoln Lab that will optically demultiplex the 100Gb/s data from the network and distribute it to the various slower electronic subsystem. In achieving this goal, one technical challenge that arises is that of buffering and extending the high-speed demultiplexed pulses to levels suitable for the electronic logic. A solution to this problem is proposed, analyzed, constructed and tested. The solution comes in the form of a circuit that uses the high-speed switching capabilities of a resonant tunneling diode (RTD) to interface with the short demultiplexed pulses. A GaAs FET of the type present in the subsequent logic systems is used as a dynamic load for the RTD. The presence of a DC bias voltage allows for a robust design that can accommodate substantial device tolerances. This DC bias also provides a simple method for controlling output pulse characteristics.

Thesis Supervisor: J. K. Roberge, Professor of Electrical Engineering, MIT

Acknowledgments

Ahh, the fun part of writing a thesis. It is to be saved till the very end as an incentive for completion. And now that the writing and editing are done, *(and with it all compiled to postscript, the ^D that Microsoft so thoughtfully puts in has been deleted, and with it downloaded to my near quota Athena account, ready to be queued to -Pthesis)* I can begin to thank the various people who have helped me reach this moment of joy.

To my parents, Alisa and Zeev, otherwise referred to as Mom and Dad, I would like to express my most sincere gratitude. You put up with a lot and *(put forth a lot... of tuition)*. With your help, I was able to get through these college years unscathed . . . except for a few scars of Jewish guilt. I'd say it was worth it.

To my Lincoln Lab advisor, the man with many first names, T. C. L. G. Sollner. Thank you for the opportunity to work with such nifty little devices and for supporting my quest to find some practical use for them. And of course to all the members of Group 86 and especially Rick Mathews for listening to me complain about those little quantum devils we call RTD's.

To my thesis supervisor, mentor, professor, and general analog guru, Prof. Roberge. It was another end-of-term season and I had to pick a class to take. With not much though I chose 6.301 and the rest is history. You taught me how to be an engineer, how to think, and how to use a Lobdell napkin to do short-circuit time-constants. Thank you for all the above and all that limited space prevents me from mentioning.

To Simon Verghese, for thinking of RTD's and my thesis needs. Thank you and good luck with fatherhood.

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And to all my friends. Due to the brevity of my thesis, I feel I can not thank you all individually for fear of having my acknowledgments run longer than my results. So to Eric 'pick a card - any card' Scharin, Tim 'shammy-sham' Tuttle, Mike 'doggy - morphin' Jones, Upe 'truth generatin' Shardinand, Michael 'thanks for letting me solder' Mermelstein, John 'aquainted with the night' Kaufhold, John 'Mazel Tov on the eddingway' Fini, and Kent 'a truly faithful servant' Lundberg - just a simple thanks for now and a free drink from me at my end of thesis celebration.

And for those that fatigue and lack of sleep has caused me to leave out - Thank You.

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Chapter 1 - Introduction

1.1 Motivation

Even the briefest survey of the electronics revolution will surely make note of the tremendous progress made in speeds of operation. While only fifteen years ago, a PC would be considered fast with a clock speed of 1 MHz, today 200 MHz CPU's are common.

High density digital content is now found globally and it is becoming increasingly crucial for commercial, industrial and defense purposes, to be able to transfer large amounts of that data quickly and efficiently. Put forth here is a potential solution to one of the technical challenges associated with this goal of rapid data transfer.

1.2 Overview

The next generation of high speed data networks will rely on both optical communication, for its high bandwidth, and electronic processing for its relative maturity and versatility. In joining these two systems, several hurdles arise. This thesis addresses one specifically related to the demultiplexing of optical data to electronic subsystems. This problem is presented in more detail in section 1.3. The solution to this hurdle comes in the form of a hybrid circuit that is capable of monostable operation from very short trigger pulses. The enabling technology for this particular topology is the resonant tunneling diode. Section 1.4 describes this device and reasons for its suitability to the task of responding to very short pulses. Chapter 2 describes the monostable circuit topology and its modes of operation. This analysis results in a model whose performance is compared against measurements made on a discrete prototype. The method and results of this comparison are the subjects of Chapter 3. This chapter also raises interest into further research on a fully integrated version of the proposed topology. Finally, conclusions are drawn as to the possible speeds of operation given state-of-the-art devices in an integrated process.

1.3 The Challenge

To meet the demands of faster communications between devices containing denser information many researchers are looking to optical networks.[1] However, the electronics available at the receiving end of such a network cannot currently work at the data rates of the fast optical networks currently being developed. To make best use of the advantages of an optical network, a method must be developed to demultiplex the optical data to a rate suitable for the electronic subsystems. Even after demultiplexing to a slower pulse rate, however, the short duration of these pulses are inadequate to drive even the fastest electronic logic circuits. A means is required to extend the duration of these pulses

Both all-optical[1,2] and all-electronic[3] demultiplexers have been proposed and constructed. Considering the benefits of each system allows conversion from the optical to the electrical domain at the point that best maximizes these benefits. An advantage of demultiplexing optically is that clock distribution at the high data rates occurs in optical fiber and is therefore relatively immune to crosstalk and skew. Converting to voltage pulses initially and carrying out the demultiplexing electronically has the advantage of allowing for relatively compact circuit layout. The disadvantage of this type of system results from radiative crosstalk between the clock signals that would be used for demultiplexing.

A system approach currently being considered at MIT's Lincoln Laboratory will call for the 100Gb/s optical data stream to be converted to a stream of voltage pulses by a low-temperature-grown (LTG) InGaAs photoconductor embedded in a coplanar waveguide. These voltage pulses will then be demultiplexed by tapping the waveguide with LTG InGaAs photoconductive switches. These switches will be illuminated by optical clocks that will cause any voltage pulse coincident with an optical one to propagate down the tap. This system is shown in Fig. 1.1 with four taps indicating a 4:1 demultiplexing operation.

The demultiplexed voltage pulses traveling down the taps, however, are still quite narrow (~5ps corresponding to the 50% duty cycle 100Gb/s initial data stream). Pulses this narrow will be ignored by electronic logic subsystems that will reside at the end of the taps. It is therefore necessary to include a circuit that will take these short pulses of low duty cycle (~5ps every ~40ps for a 4:1 demultiplexing of a 100Gb/s data stream) and extend them (~20ps every ~40ps).

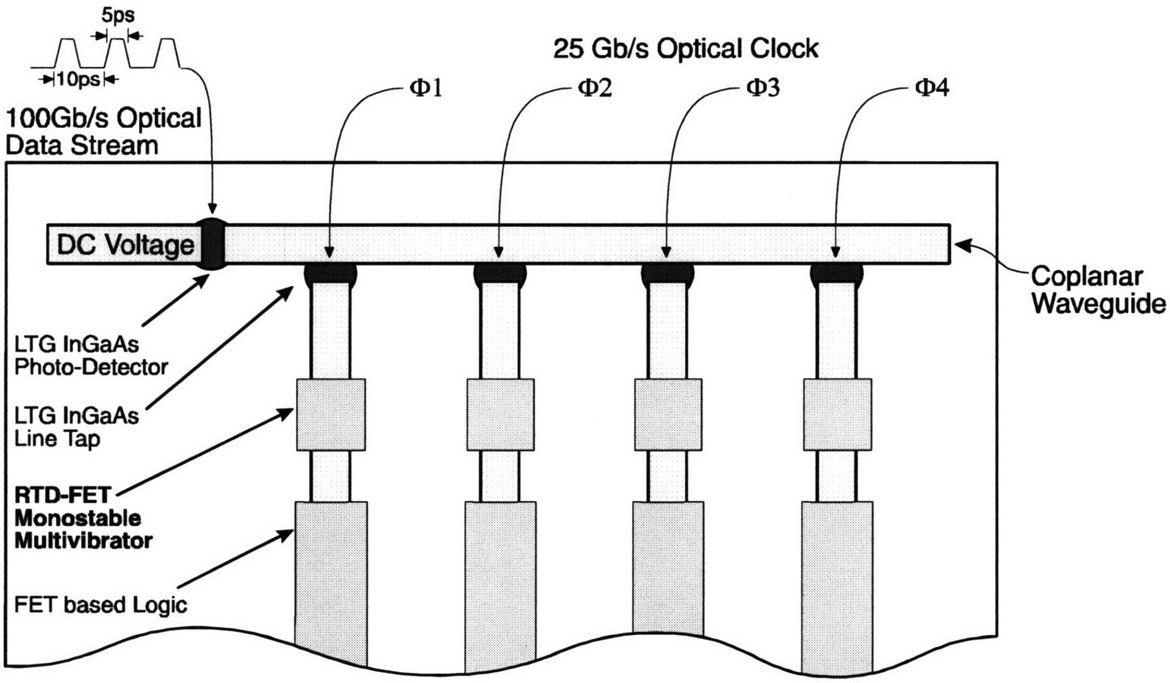

Figure 1.1 - Optoelectronic Demultiplexer (ground plane not shown for clarity)

The general type of circuit that will accomplish this function is a monostable multivibrator sometimes referred to as a one-shot. In general, a one-shot takes short duration trigger pulses and generates longer fixed-width output pulses. This particular application requires a topology capable of triggering from extremely narrow pulses. The resonant tunneling diode is currently one of the fastest switching solid state devices,[4] and as a result is well suited for use in solving this problem.

1.4 The Resonant Tunneling Diode

Similar to the tunnel diode discovered by Esaki in 1957[5], the resonant tunneling diode (RTD) is a two terminal non-linear device with an N-shaped current-voltage (I-V) characteristic. A typical I-V curve for an RTD is shown in Figure 1.2. It was first demonstrated by Chang *et al.*[6] in 1974 and has since shown promise in applications ranging from multivalued SRAM[7] to signal processing.[8]

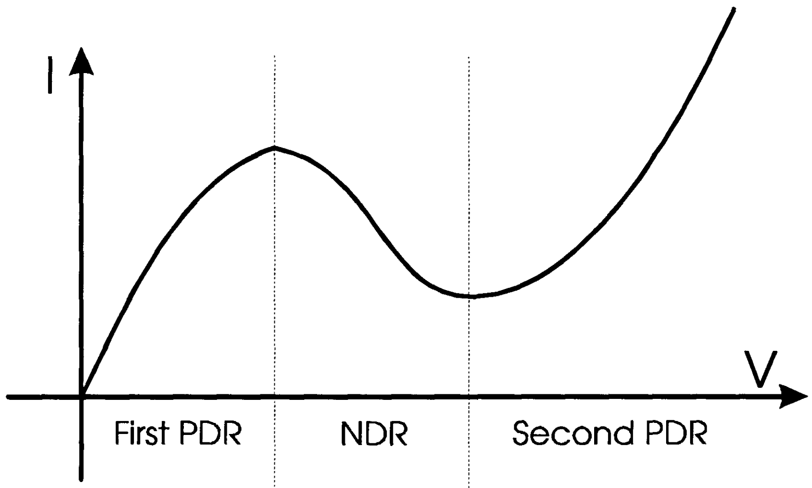

Figure 1.2 - Typical RTD I-V Curve

Throughout this thesis, the three main regions of an RTD's I-V curve will be referred to as the first positive differential resistance (PDR), the NDR and the second PDR regions.

From a circuit design point of view, an attractive and potentially useful feature of this device is its negative differential resistance (NDR) region. With proper biasing, a transition across this region can happen very rapidly. Transition times under 2ps have been reported.[9] This high speed switching is a result of the RTD's low device capacitance, high current density, and the fast nature of the quantum effects that govern this device's operation. With a capability for such fast transition times, the RTD is an ideal device for use in the proposed technical challenge.

Chapter 2 - Analysis of Operation

2.1 The Basic Topology

Figure 2.1 shows the basic topology for the FET-RTD one-shot. This circuit takes advantage of the relatively large gate-to-source capacitance of a typical FET to hold it on for a controlled period of time. The capacitance is shown here as an external component, Cbig. In a final integrated circuit, however, Cbig can potentially be left out with Cgs of the FET providing the needed capacitance.

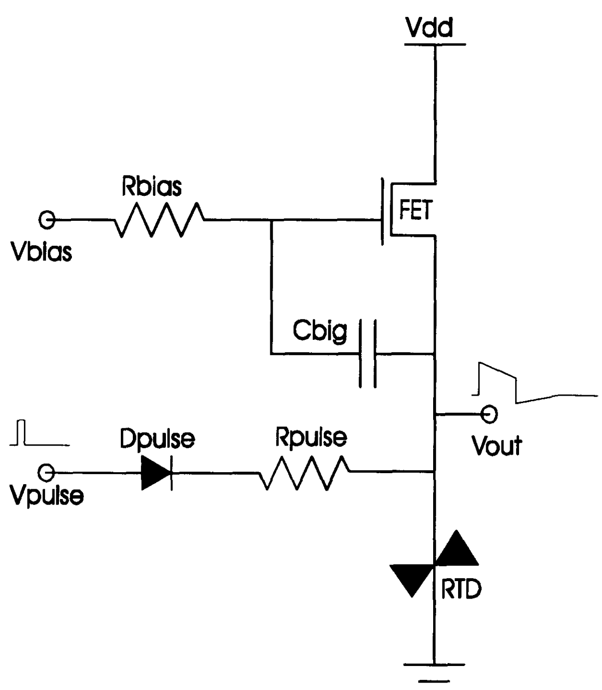

Figure 2.1 - RTD-FET one-shot

2.2 Overview of Operation

In Figure 2.2a, the solid load line, provided by the FET load, indicates the steady-state condition prior to an input pulse. The operating point is the black dot in the first positive resistance region of the RTD. When an input pulse arrives, the extra current causes the FET load line to rise *(dashed line)* above the peak, and a low-to-high transition is seen on Vout. Cbig in Figure 2.1 is large enough so that on the time scale of the low to high transition, Vgs remains constant, keeping the FET load line the same.

It is assumed that the input pulse ends by this point and eventually, Cbig begins to discharge, lowering the FET load line. During this period (Figure 2.2b) the operating points drifts down the second positive resistance region of the RTD. If biased correctly, the load line will dip below the valley and cause a high-to-low transition (Figure 2.2c). At this point, Vgs has undershot its steady state value, and Cbig charges up until it reaches the state shown in Figure 2.2a.

Many advantages to this topology can already be seen from this simple overview of operation. Once the circuit is tripped into the output high state, it is insensitive to noise on the input. This insensitivity also extends into the recovery period but diminishes, however, as the operating point approaches the peak of the RTD.

In addition, device matching between the FET and RTD becomes less critical because of the DC bias, which effectively determines how 'on' the FET is. Furthermore, Vbias sets the steady-state operating point, which can be used to trade off noise sensitivity for input-pulse amplitude requirements.

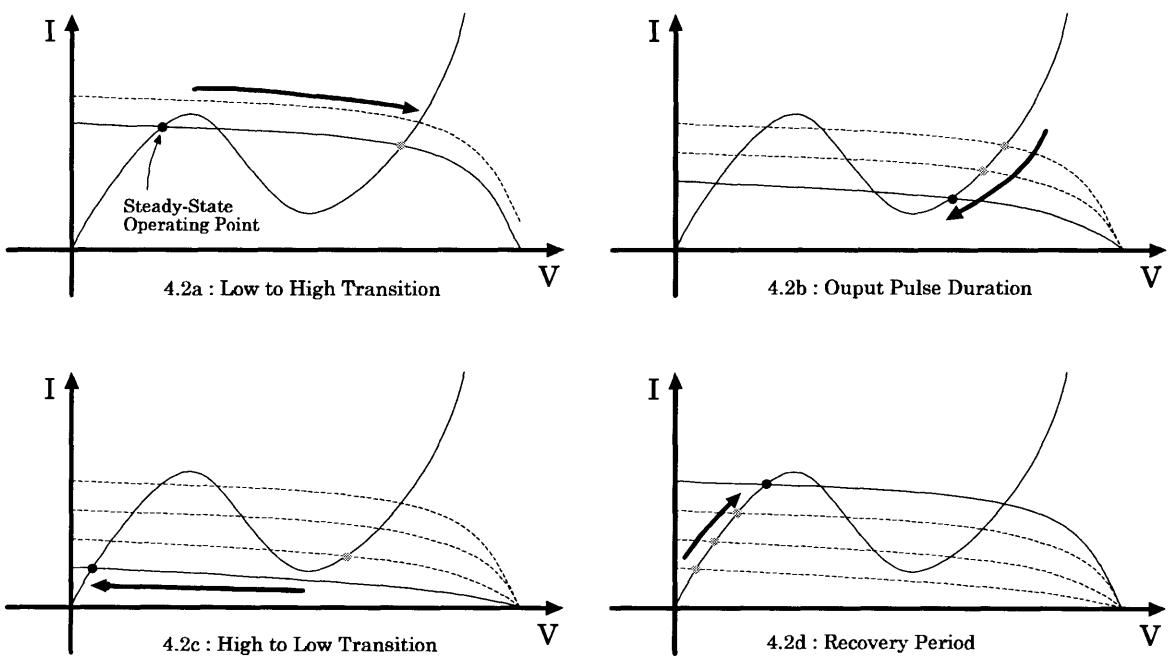

Figure 2.2 - Four phases of operation

2.3 Ensuring Monostability

It is possible to bias the circuit of Figure 2.1 in such a way that, upon the application of an input pulse, a second stable state can be reached in the second PDR region of the RTD. It is easiest to consider this problem graphically by looking at the DC load line of the FET.

Figure 2.3a shows three DC FET load lines corresponding to three DC bias voltages, superimposed on a simulated RTD I-V curve. These curves are generated by slowly sweeping the output voltage and plotting against it the RTD and FET current. The bottom two curves are monostable with respect to the RTD I-V curve. The upper one, however is bistable in that there are two stable operating points. The third intersection in the negative resistance region is unstable since any perturbation from it will drive the system to one of the outer two operating points.

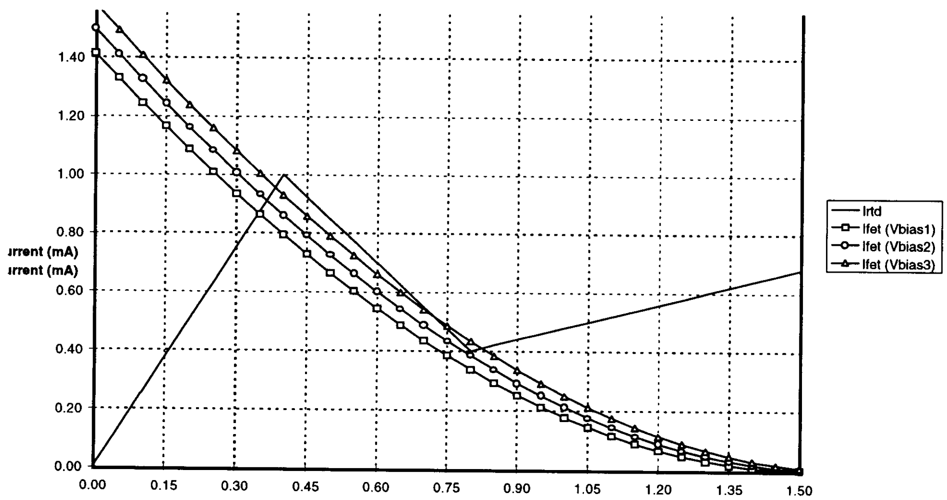

Figure 2.3a - DC load lines for various bias voltages

The resulting transient responses to an input pulse are shown in Figure 2.3b. Two of the three curves return to their initial steady state. The one which corresponds to the bistable case above, exhibits the latch-up condition we expect from the DC load-line analysis. Prevention of such a latch-up condition, then, is simply a matter of biasing the particular FET-RTD pair for monostable operation.

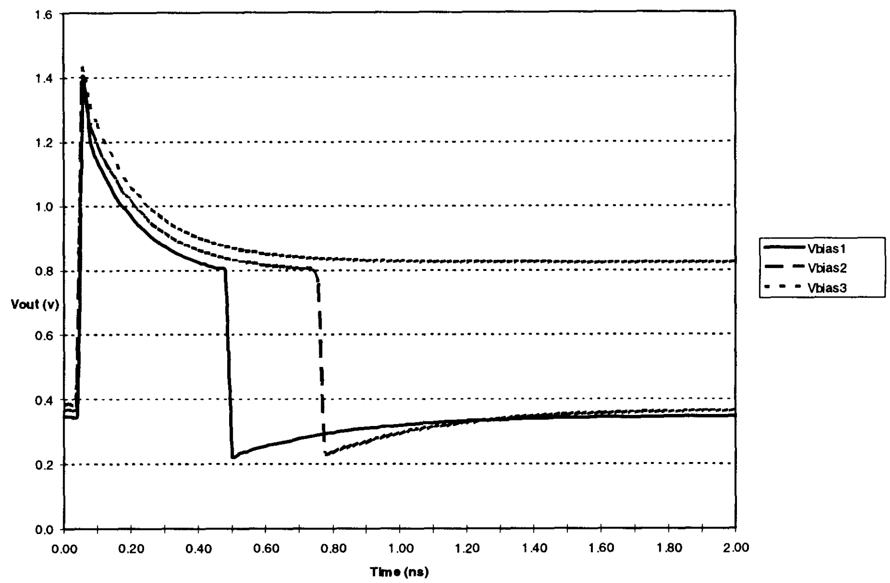

Figure 2.3b - Transient response to input pulse for various bias voltages

2.4 Requirements on the Input Pulse

Given the intended application for this circuit, that of demultiplexing a fast optical network to several slower electronic ones, the minimum duration required of the input pulse is of critical importance. From the optical network for which this circuit was developed, the input pulses can be as short as a few picoseconds. It is important, then, to understand the mechanism by which this circuit switches and, from there, determine what can be done to the topology and/or devices to shorten this time as needed.

For simplicity, we will assume a piece-wise-linear RTD model as shown in Figure 2.4a. The lumped series resistance, Rs, includes contact resistance as well as semiconductor bulk resistance. The RTD capacitance is Crtd. In practice, this is a nonlinear depletion layer capacitance which is at a maximum when the device is biased at its peak. For ease of calculation and to yield a conservative result, we will assume a constant capacitance of the maximum value at the peak. In addition, the FET load will be considered constant on the time scale of low-to-high transitions.

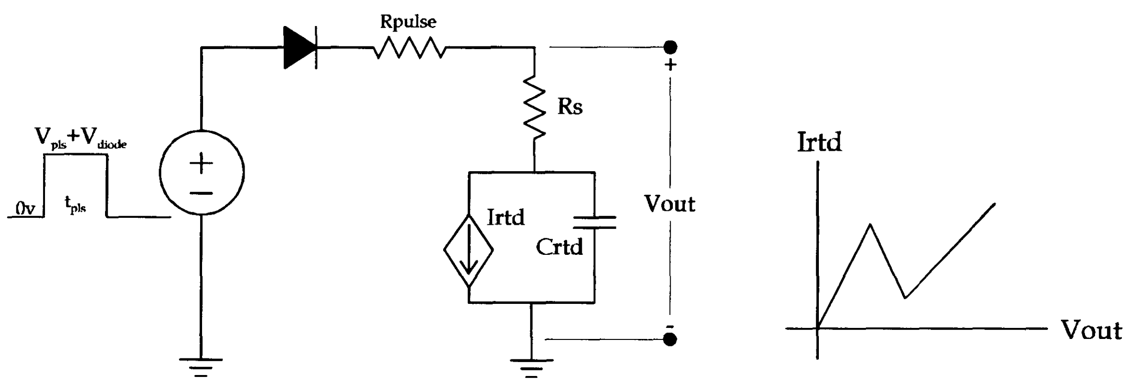

Figure 2.4a - Piece-wise linear RTD model

Figure 2.4b shows the steady-state FET load line and the piece-wise-linear RTD IV curve. Point A is the initial operating point, and B represents the absolute minimum point that must be reached by the end of the input pulse for a transition to be triggered. If the input pulse ends prior to reaching B, the net current available to charge Crtd *(the difference between the FET curve and the RTD curve)* will be negative, and the RTD will discharge back to point A. If B is exceeded, the net current will be positive, and the RTD will charge to operating point C.

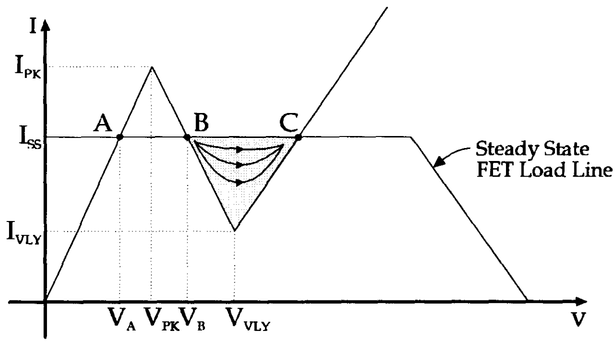

Figure 2.4b - Points of interest for low to high transition

Providing a pulse of duration just long enough to reach B, however, is impractical. For one, point B is an unstable point that can be difficult to reach repeatedly and reliably. Moreover, if point B were incrementally exceeded, the current available for charging Crtd, while positive, would be very small, resulting in a long rise time. A more suitable point to use to determine a reasonable lower limit on pulse duration would be the valley. Not only is the valley voltage and current easy to measure, it is also the point where the shaded region in Fig. 2.4b is thickest indicating a large excess current. This large current provides a swift transition through the valley.

It is now possible to calculate a lower limit on the pulse width by considering the voltage change that must appear across Crtd. In steady state, the voltage across Crtd is:

$$Vc_{initial} = V_A - Iss \cdot Rs \tag{2.41}$$

Using the valley point as the upper voltage, the voltage across Crtd is:

$$Vc_{final} = Vvly - Ivly \cdot Rs \tag{2.42}$$

To calculate the current available for charging Crtd, we assume that the voltage of the input pulse is large compared to changes in Vout and that Vout~Vp through this low to high transition. The latter assumption will serve to yield a slightly conservative estimate. With these assumptions, the current available to Crtd is:

$$Ia = \frac{Vpulse - Vpk}{Rpulse} - Ipk \tag{2.43}$$

Combining Eqs. 2.41, 2.42 and 2.43 with the state relation for a capacitor, $t_{pls} = \frac{dV}{dI} Crtd$, we arrive at an expression for a lower limit on the pulse duration:

$$t_{pls} = \frac{\left[(Vvly - Ivly \cdot Rs) - (V_A - Iss \cdot Rs)\right] \cdot Crtd}{\frac{Vpulse - Vpk}{Rpulse} - Ipk} \tag{2.44}$$

Assuming an RTD with Vpk = 1v, Vvly = 2v, Vpulse = 3v, Rs = 200Ω, V_A = 0.75v, Ipk =1mA, Ivly = 400μA, Iss = 750μA, Rpulse = 500Ω and Crtd = 32fF, $\underline{t_{pls} = 14.08ps}$. While this may not be fast enough for the initial application, it is clear from Eq. 2.44 what types of improvements in devices will be needed to achieve the seven fold increase in speed. Specifically, by rewriting Eq. 2.44 in terms of RTD current density, size, and device capacitance per unit area, it becomes clear that the most effective way to decrease t_{pls} is to reduce Crtd. It should be noted however, that the above calculation was made with several approximations all of which tend to yield an conservative result.

The loading of this circuit will ultimately involve the addition of a FET voltage follower to the output node of Figure 2.1. For relatively small RTD series resistance, the effects of this loading can be adequately modeled by including the load capacitance in the value for Crtd. To yield better performance, then, will require FET's with small Cgs. These FET's, however, need only be as good as the FET's used in the logic stages that follow it. The faster the FET logic, the smaller the load to the monostable.

Equation 2.44 only gives an estimate for the input pulse duration, but the full low-to-high transition will take substantially longer. An expression for the time spent in the regenerative portion of the transition can be obtained by calculating the current available to charge Crtd and the voltage change Crtd must go through. Once again, a conservative estimate is made by assuming $\Delta V = V_{final} - V_{pk}$ and $\Delta I = I_{pk} - I_{vly}$, where V_{final} corresponds to the voltage of the gray dot in Fig. 2.2a. With these approximations, the rise time becomes:

$$t_{rise} = Crtd \cdot \frac{V_{final} - V_{vly}}{I_{pk} - I_{vly}} \tag{2.45}$$

With the values used to calculate t_{pls} above, and with V_{final}=3v, <u>t_{rise} = 53.3ps</u>. This rise time is nearly four times t_{pls}. From Eqs. 2.44 and 2.45, however, it is clear that to reduce both t_{pls} and t_{rise}, an RTD with low capacitance and high peak current density would be ideal. The numbers used in this case were 2fF/μm^2 for the device capacitance and 6.25×10^3 A/cm^2 for Jp. While the capacitance is near the state of the art, there are many devices currently being grown with significantly higher current densities.

2.5 Output Pulse Duration

Once the one-shot is triggered into the high state, Cbig begins to discharge causing Vout to scan down the second PDR region of the RTD. Until the valley point is reached, this phase of operation is simply an exponential decay. Solving for τpls, the time constant of this decay, is straightforward and shown below.

Time constant τpls is obtained by calculating the resistance seen by Cbig. Figure 2.5a shows the simplified schematic used to calculate this. Once again a piece-wise-linear RTD model is used and Rrtd models the resistance of the second PDR region (zero offset is assumed).

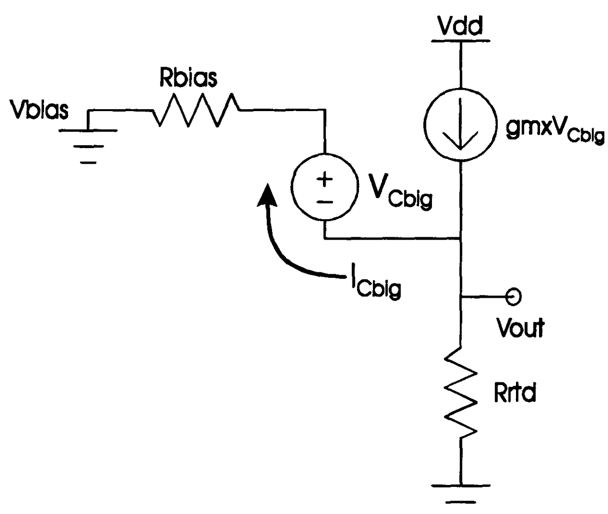

Figure 2.5a - Calculating resistance seen by Cbig

We write an expression for I_{Cbig} by finding the voltage across Rbias:

$$\frac{(gm \cdot Vgs - I_{Cbig})Rrtd + Vgs}{Rbias} = I_{Cbig} \tag{2.51}$$

Solving for the incremental resistance seen by Cbig, we get τpls:

$$\tau_{pls} = \frac{V_{Cbig}}{I_{Cbig}} \cdot Cbig = \frac{Rbias + Rrtd}{gm \cdot Rrtd + 1} \cdot Cbig \tag{2.52}$$

An expression for Vout during this phase of operation is simply an exponential of the form:

$$Vout = (V_{initial} - V_{final})(1 - e^{-t/\tau pls}) \tag{2.53}$$

The final value of this decay, V_{final}, is dependent on many variables, including Vto and gm of the FET as well as the supply voltage. An expression including all of these variables would yield little insight. What is of more value is a qualitative analysis of the output pulse and its relation to Vbias.

After a low-to-high transition (points A to B in Figure 2.5b), Cbig discharges, turning the FET off. If the RTD were simply a resistor, shown as a dashed line, this exponential decay would settle to point C.

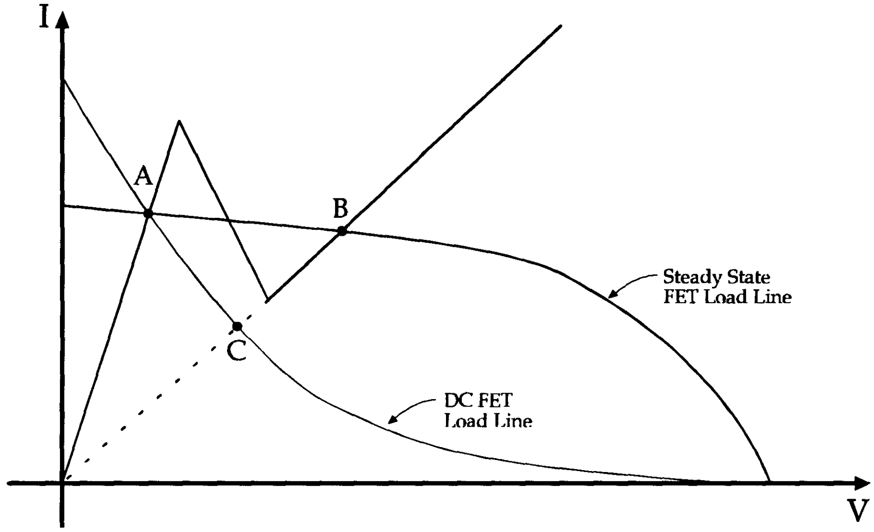

Figure 2.5b - Output pulse dynamics

Point C is controlled by the FET characteristics but is also dependent on Vbias, as shown in Figure 2.3a. As a result, point C can be placed with a fair amount of control. If its location is far enough away from the valley point, the output pulse decay will be nearly linear and an estimate for its duration can be made easily.

$$t_{pls} = \frac{V_{final} - V_{vly}}{V_{final}} \cdot \tau_{pls} \tag{2.54}$$

In practice, nonlinearities and the proximity of point C to the valley point will cause Eq. 2.54 to yield a slightly smaller estimate than the true pulse width.

2.6 Recovery Time

After scanning past the valley point, the one shot jumps back across the NDR region and recovers back to point A of figure 2.5b. The time constant for this recovery is the same as in Eq. 2.52 except that Rrtd is now the resistance of the *first* PDR. As the one-shot recovers, it will once again become sensitive to input pulses. This, of course, is true as long as the input pulse is sufficiently large to get past point B of Figure 2.4b.

2.7 Conclusions

This chapter has discussed the general operation of the one-shot. Where appropriate, engineering approximations were made to yield insightful solutions to the various phases of operation. Many advantages of this topology were made apparent, most notably the availability of a DC bias to control many of the circuit's dynamics. With the results from this chapter in mind, the one shot was constructed with discrete components. The results are presented in Chapter 3.

Chapter 3 - A Discrete Prototype

3.1 The Components and Their Models

The prototype circuit that was built and tested is shown in Figure 3.1a. Resistors used were 1% precision and the 210pF capacitor was of the ceramic surface-mount type suitable for UHF and microwave application.

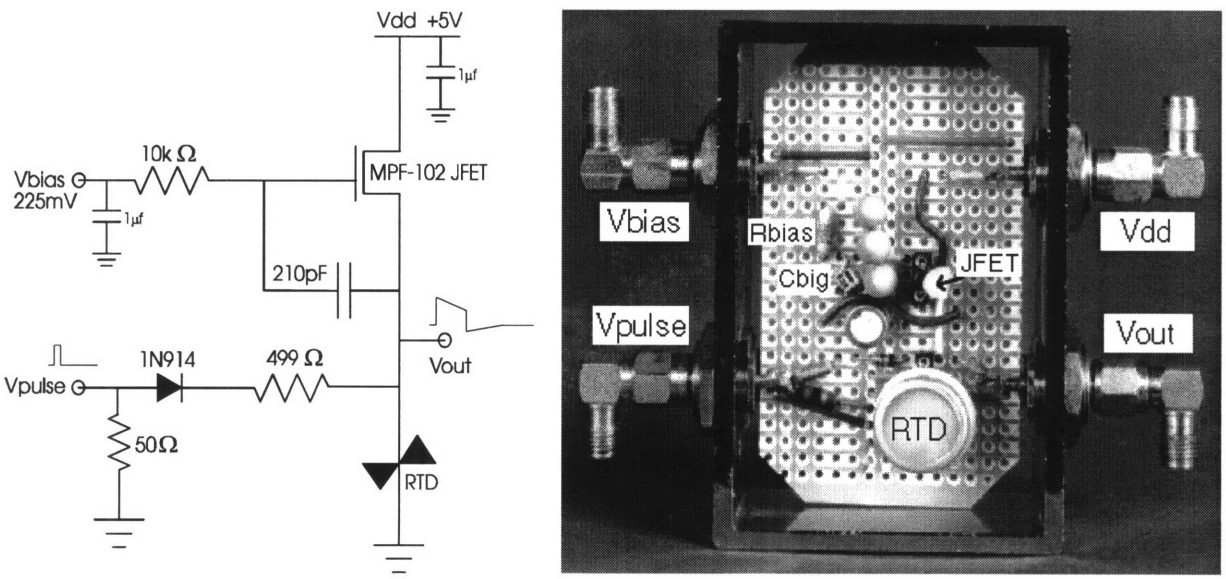

Figure 3.1a - The constructed monostable

An MPF-102 JFET from Motorola was used as the load, and a family of I-V curves is shown in Figure 3.1b. SPICE parameters were extracted from the data sheet and the same set of I-V curves was simulated and is shown in Fig. 3.1c.

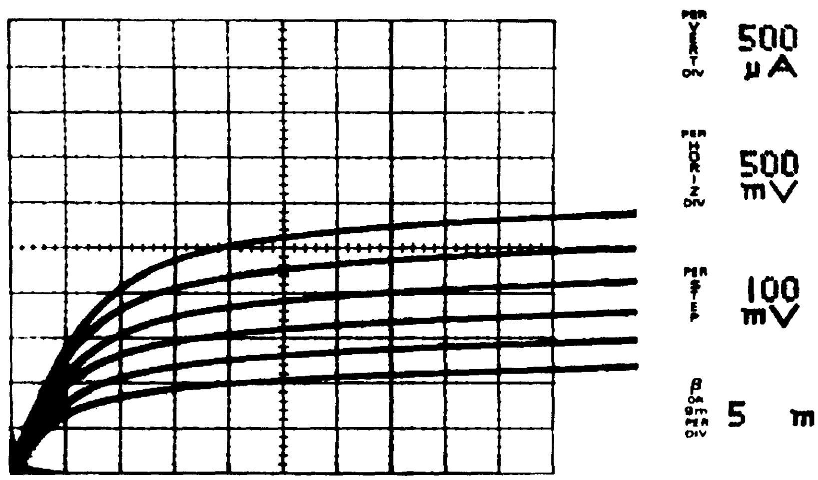

Figure 3.1b - Measured JFET IV Curves

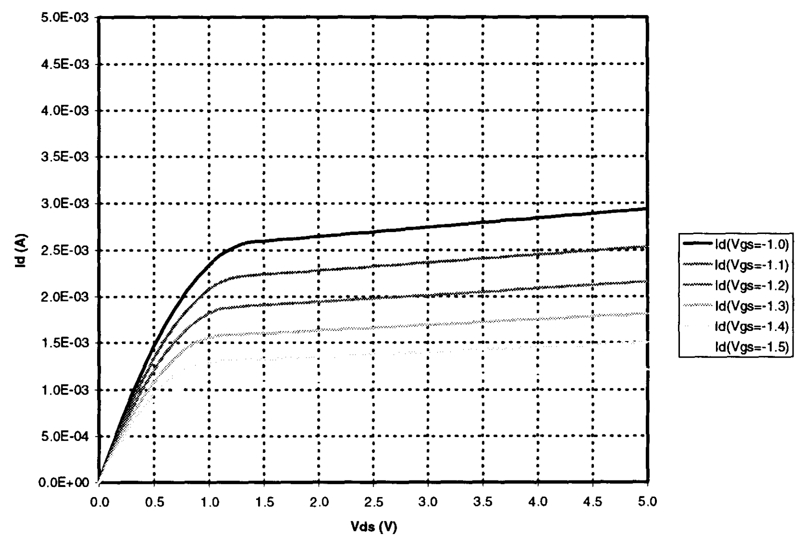

Figure 3.1c - Simulated JFET IV Curves

A model similar to that shown in Figure 2.4a was used for the SPICE simulations. Both the measured and simulated curves are shown in Figures 3.1d and e, respectively. The package capacitance was modeled by a fixed capacitor across the two terminals of the device. Although some inductive ringing was seen in the final system measurements, parasitic inductance was left out due to its small affect on circuit dynamics.

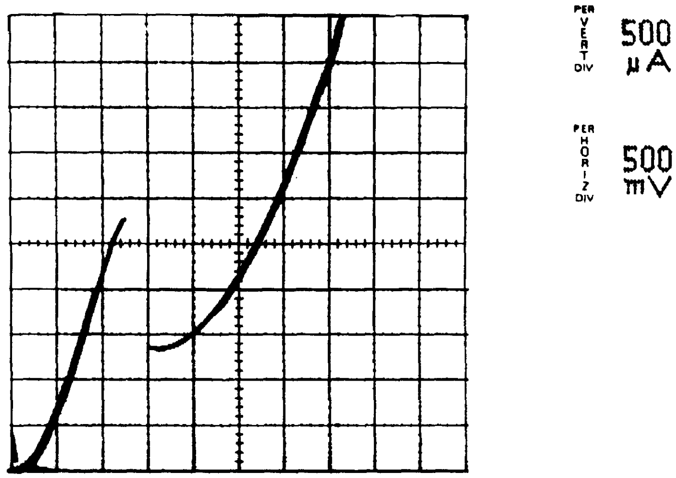

Figure 3.1d - Measured RTD IV Curve

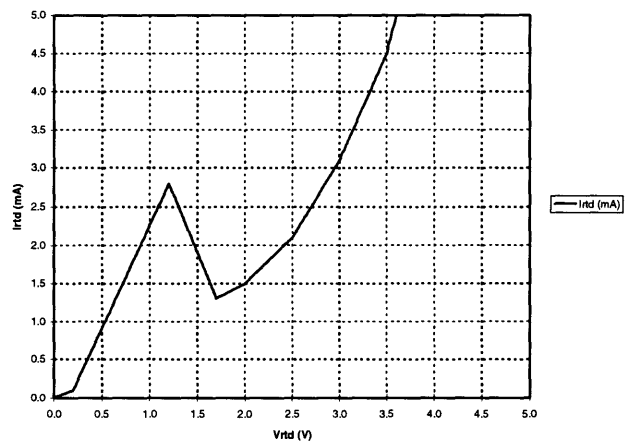

Figure 3.1e - Simulated PWL RTD IV Curve

3.2 Comparison of Measured and Simulated Results

An input pulse with height 3.25v, rise and fall times approximately 1ns, and duration 1ns was fed into the monostable. Both the input and output pulses are shown below. Figure 3.2a has a horizontal scale of 5ns/div to show the low-to-high transition. Figure 3.2b *(horizontal scale 200ns/div)* shows the dynamics of the output pulse and recovery. Table 3.2 below summarizes the measured vs. simulated results.

	Measured	Simulated	% Error
10%-90% Rise Time	17ns	16ns	**5.90%**
Output Pulse Width	800ns	760ns	**5.00%**

Table 3.2 - Summary of Simulated vs. Measured Results

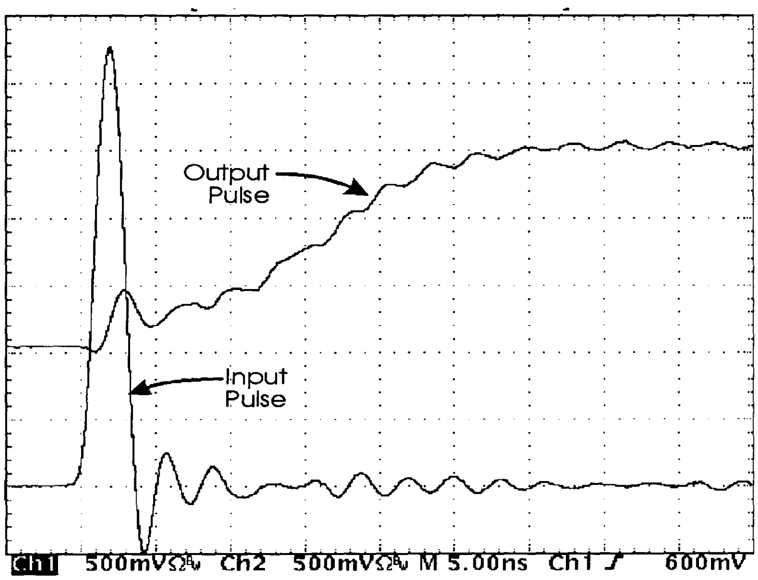

Figure 3.2a - Measured low-to-high transition

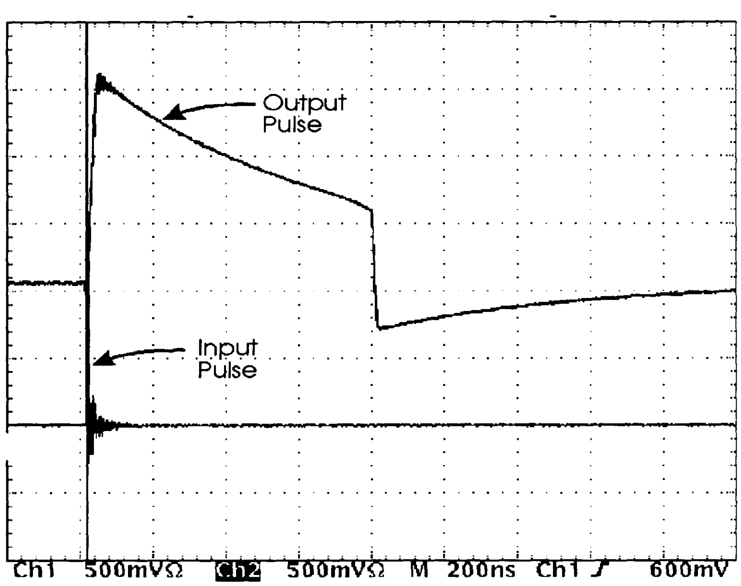

Figure 3.2b - Measured output pulse

The same input was used in SPICE simulations, and care was taken to model parasitics including probe capacitance. The results are shown below. There is excellent agreement between these plots and those of the actual circuit above. In addition, all the equations of Chapter 2, which were developed using linearized approximations, yield solutions that correspond well to the dynamics of this circuit, both measured and simulated.

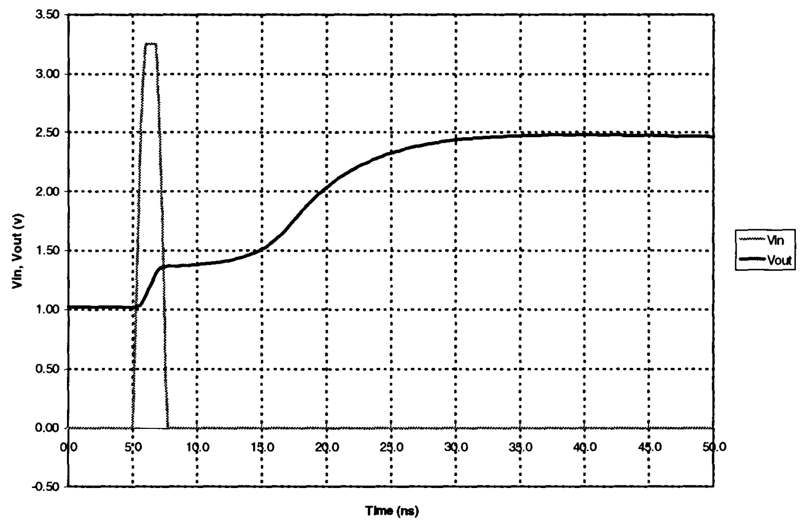

Figure 3.2c - Simulated Low-to-High Transition

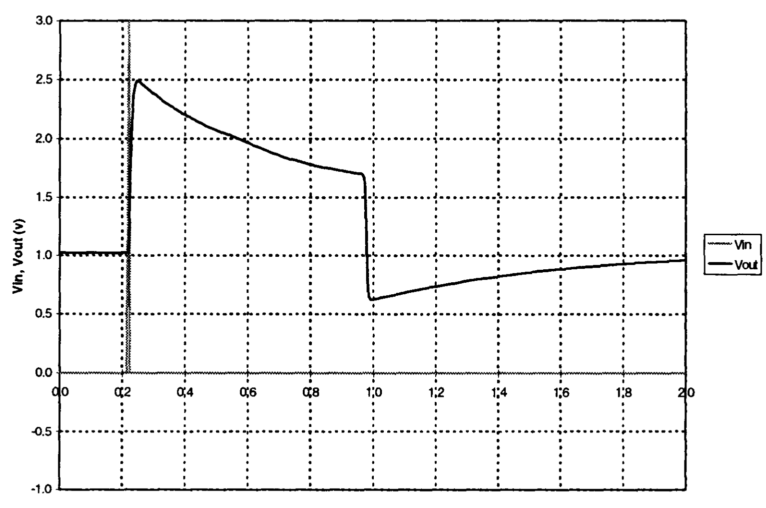

Figure 3.2d - Simulated Output Pulse

3.3 Triggering off 100 GHz Data

Further experimentation was done, and with this fully discrete design the fastest achieved speeds corresponded to input pulses with amplitude of 2.5v and pulse widths including rise and fall times of 250ps. These specs would allow for triggering off data rates as high as 2Gbits/sec. Currently, the RTD package capacitance and the subsequent load capacitance associated with the FET follower are the primary limiting factors to the circuit's speed. This is most apparent in Figures 3.2a&c, which both show approximately 15ns of rise time. This rise time corresponds to the charging of Crtd through the valley region and agrees with that calculated from Eq. 2.45. To meet the intended data rate of 100 Gbits/sec would require a substantial reduction in these parasitics. This reduction can be achieved once processing steps are developed to fully integrate this topology. By using equations 2.44 and 2.45, it is possible to get a estimate for the type of RTD and parasitics that will be needed to realize this speed of operation.

For a 100 Gbit/sec data rate and a 10:1 demultiplexing of that data, we expect the input pulses to have durations of 3ps and amplitudes of 5v. For the output pulse, subsequent logic systems could handle an additional 7ps of rise time corresponding to ten percent of the total pulse period spent in transition. With these performance specifications, equations 2.44 and 2.45 estimate that an RTD with the following characteristics be used:

Size: $2\mu m^2$ *P/V Ratio : 4* *Jp :* $1x10^5\ A/cm^2$

Cload : 10fF *Cap/Area :* $2fF/\mu m^2$

Of particular note is the low load capacitance that is required to make t_{rise} at least somewhat shorter than t_{pls}, (the duration of the output pulse). Obviously, if t_{rise} were longer than t_{pls}, the monostable would not have a chance to transition high before Cbig discharged enough to cause a high-to-low transition.

All of the above RTD parameters have been achieved singularly. Recent work is now showing that single devices having or exceeding all these parameters are capable of being produced. At MIT's Lincoln Laboratory, a current density of $1.7 \times 10^5 A/cm^2$ and a P/V ratio of 12 has been achieved in an InGaAs RTD with AlAs barriers. Devices such as this make the monostable proposed here an attractive and realizable solution to the technical challenge that motivated it, that of stretching ultra-narrow pulses in an electro-optical demultiplexer.

Chapter 4 - The Next Step

4.1 Integration

At the end of Chapter 3, an estimate was given for the device specifications needed to achieve the intended performance of the monostable. Past research has produced and tested individual RTDs meeting several, and most recently all, of these requirements.[10,11] The needed integration of these RTDs with FETs, however, has only recently been achieved.[12,13] It remains the topic of further work to produce an integrated version of the proposed topology to verify its application at higher speeds.

Perhaps the most significant result of high speed testing of an integrated monostable will be the verification of the model developed in Chapter 2. In this model, all capacitances associated with the RTD were lumped into a single fixed capacitor Crtd. This included all load capacitance as well as device capacitance across the well. The latter component is already known to vary with bias level. While this model produced exceptional agreement with measured results at the speeds tested in Chapter 3, it will require further testing of an integrated circuit to determine if such a simple treatment of parasitics will remain valid at higher frequencies.

4.2 Conclusion

To achieve the higher speed required by the next generation of electronics, it becomes increasingly difficult to obtain solutions with transistors alone. The use of novel devices that rely on quantum effects for high speed switching may provide the answer.

One such devices, the resonant tunneling diode (RTD), is used here in conjunction with a FET to create a monostable multivibrator. A discrete version of this topology was constructed and a model was proposed, analyzed and verified with considerable success against measured performance. With this model, estimates were made for the device specifications needed for a fully integrated version of this topology to meet the needs of a proposed 10:1 electro-optical demultiplexer operating at a data rate of 100Gbits/sec. Current technology yields devices that can, according to this model, achieve these high data rates and it is hoped that future advances in devices fabrication will improve on this. In addition, current work shows promise for the effective integration of RTDs with FETs which will allow for much higher performance versions of the circuit proposed here to be realized.

In general, RTDs show promise in achieving the higher performance demands of tomorrow's technology and with careful and clever circuit design, they can provide unique solutions to these future challenges.

Appendix - Spice Files

Code for Figure 3.1c
Simulated JFET IV Curves

```
J1 2 1 0 MPF102

.PARAM Vgs=1v
Vdd 2 0 5v
Vt 1 0 {Vgs}

.model MPF102 NJF
+ Beta=1.22e-3
+ Vto=-2.4
+ Cgs = 7e-12
+ Cgd = 3e-12
+ Lambda = 0.04

.DC Vdd 0v 5v .05v
.STEP PARAM Vgs -1.5v -1.0v 0.1v
.PROBE
.END
```

Code for Figure 3.1e
Simulated PWL RTD IV Curve

```
X1 1 0 Rtd
Vs 1 0 1v
.DC Vs 0v 5v .01v
.PROBE
.print dc i(x1.rs)

; RTD piece wise linear I-V model
; Unit Size -> 4um x 4um
; Model for packaged RTD in Metal One Shot
.PARAM
+       Rsnorm      = {200}
+       Cap         = {32f}
+       PackageC    = {8.0pf}

.SUBCKT   Rtd  1  3  PARAMS: Area=1
Rs             1  2  {Rsnorm}
Grtd           2  3  Table {V(1,3)} =
+       (0.0,0.0m)
+       (0.2,0.1m)
+       (1.2,2.7m)
+       (1.7,1.3m)
+       (2.0,1.45m)
+       (2.5,2.0m)
+       (3.0,2.9m)
+       (3.5,4.5m)
Cap            2  3  {Cap}
Cpackage       1  3  {PackageC}
.ENDS    Rtd
.END
```

Code for Figure 3.2c
Simulated Low-to-High Transition

```
Vdd 30 0 5
Rdd 30 3 25
J1 3 2 1 MPF102
X1 1 0 RTD
Cload 1 0 3pf
Rbias 4 2 10k
Vbias 4 0 -120mv
Vpulse 10 0 pulse(0v 3.25v 5ns 1ns 1ns 1ns 2u)
Dpulse 10 11 Dnom
Rpulse 11 1 499

Cbig 2 1 210pf
.tran 0.2ns 50ns 0 1ns
.PROBE
.print tran v(1) v(10)
.model Dnom D[Is=1e-14]

.model MPF102 NJF
+ Beta=1.25e-3
+ Vto=-2.4
+ Cgs = 7e-12
+ Cgd = 3e-12
+ Lambda = 0.04

; RTD piece wise linear I-V model
; Unit Size -> 4um x 4um
; Model for packaged RTD in Metal One Shot
.PARAM
+       Rsnorm        = {200}
+       Cap           = {32ff}
+       PackageC      = {4pf}

.SUBCKT    Rtd  1  3   PARAMS: Area=1
Rs              1  2   {Rsnorm}
Grtd            2  3   Table {V(1,3)} =
+       (0.0,0.0m)
+       (0.2,0.1m)
+       (1.2,2.8m)
+       (1.7,1.3m)
+       (2.0,1.5m)
+       (2.5,2.1m)
+       (3.0,3.1m)
+       (3.5,4.5m)
Cap             2  3   {Cap}
Cpackage        1  3   {PackageC}
.ENDS    Rtd
.END
```

Code for Figure 3.2d
Simulated Output Pulse

```
Vdd 30 0 5
Rdd 30 3 25
J1 3 2 1 MPF102
X1 1 0 RTD
Cload 1 0 3pf
Rbias 4 2 10k
Vbias 4 0 -120mv
Vpulse 10 0 pulse(0v 3.25v 220ns 1ns 1ns 1ns 2u)
Dpulse 10 11 Dnom
Rpulse 11 1 499

Cbig 2 1 210pf
.tran 5ns 2us 0 5ns
.PROBE
.print tran v(1) v(10)
.model Dnom D[Is=1e-14]

.model MPF102 NJF
+ Beta=1.25e-3
+ Vto=-2.4
+ Cgs = 7e-12
+ Cgd = 3e-12
+ Lambda = 0.04

; RTD piece wise linear I-V model
; Unit Size -> 4um x 4um
; Model for packaged RTD in Metal One Shot
.PARAM
+       Rsnorm        = {200}
+       Cap           = {32ff}
+       PackageC      = {4pf}

.SUBCKT    Rtd  1  3   PARAMS: Area=1
Rs              1  2   {Rsnorm}
Grtd            2  3   Table {V(1,3)} =
+       (0.0,0.0m)
+       (0.2,0.1m)
+       (1.2,2.8m)
+       (1.7,1.3m)
+       (2.0,1.5m)
+       (2.5,2.1m)
+       (3.0,3.1m)
+       (3.5,4.5m)
Cap             2  3   {Cap}
Cpackage        1  3   {PackageC}
.ENDS    Rtd
.END
```

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