Using Statistical Metrology to Understand Pattern-Dependent ILD Thickness Variation in Oxide CMP Processes

by

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Abstract

A statistical metrology framework is used to understand pattern-dependent variation of inter-level dielectric (ILD) thickness variation in oxide CMP processes. Statistical metrology can be used to identify, assess and quantify the sources and magnitude of ILD thickness variation. The experimental approach emphasizes circuit-like environments and enables modeling of the polishing behavior of the final ILD thickness over fine-linewidth features. Electrical test structures are used to infer the ILD thickness between metal layers. In this experiment we focus on key layout factors that affect ILD thickness variation in typical microprocessor designs. These factors are: local metal density, metal pitch and surrounding dummy-line environment. With these factors, we examine how the geometry of layout patterns affects the planarity of an ILD layer within a die. A 15 mm x 15 mm test die containing these electrical test structures was fabricated using a short-flow CMP process. The ILD thickness data is extracted from the capacitance and linewidth measurements by interpolation on empirical capacitance formula calibrated using TCAD simulations. The experimental results show that, even at small dimensions, global pattern density plays a major role in determining the final polished oxide thickness. In addition, differences in the initial dielectric deposition profile for small features produces an apparent pitch effect which must also be taken into account for accurate pattern-dependent polish prediction.

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Chapter 1

Introduction

1.1 Background

Parametric variation in semiconductor manufacturing is becoming an increasing concern in VLSI circuits as devices are scaled down to the deep sub-micron regime along with a corresponding increase in the levels of integration. This concern is further accentuated as the wafer size is increased to 200 mm and 300 mm without an increase in the equipment tolerance. Stringent control of both device and interconnect parameters such as poly CD or inter-level dielectric thickness, is critical, not only for ensuring adequate yield, but also to achieve increasingly aggressive performance and reliability requirements [1, 2]. Maintaining process uniformity and compensating for deeply confounded interactions at each processing step is increasing in importance and complexity.

Parameter variation has both systematic and random components [3, 4]. The raw distribution of a parameter typically includes large amount of systematic variation which has different physical causes. For example, etch variation typically exhibits a traditional "bulls eye" effect, which is due to loading effects in the etch process. Sometimes systematic variation, upon initial examination, cannot be explained or modeled. As a result, all these systematic components tend to be lumped together and simply treated as random variation. By doing so, valuable process information is then lost. It is therefore critical that the different sources of systematic variation be understood and modeled so that they can be minimized either by controlling the necessary process and/or equipments parameters or by designing around the known variation.

Previous attempts to study intra-die variation have been hampered by the lack of the large amount of statistically significant data needed to model and predict the effects of various factors on device and process parameters. Zaghlou et al. studied variation in line width at both the die-level and wafer-level using a tree-based classification to correlate end-of-line parameters with dedicated electrical test structures [5]. Additional work has also been reported that focuses on intra-die polysilicon and metal CD variation [6, 7].

1.2 Review of Pattern-dependent Variation in CMP

As device and interconnect geometries continue to shrink into the deep sub-micron regime, planarity is becoming both increasingly important and difficult to achieve [9, 10]. Due to the increasing numerical aperture of lenses and larger image field used in optical lithography, advanced processes are increasingly constrained by a smaller depth of focus. Traditional ILD planarization techniques such as spin-on-glass (SOG) and reflow techniques cannot achieve the global planarization required to meet lithographic error-budget requirements. Without global planarization, die-level and wafer-scale ILD thickness variation could become significant enough to cause concerns in design of high-performance VLSI circuits [11].

It has been established that CMP achieves both global and local planarization compared to conventional technologies; however, it still remains hampered by systematic and random variation at the wafer- and die-level. Some of the systematic variation at the wafer-level is due to the particular equipment design as well as perturbations in process settings, whereas layout patterns within a die give rise to systematic die-level variation and is due to pattern sensitivity issues [12, 13].

The conformity of the pad to the wafer surface leads directly to the issue of CMP's pattern sensitivity. It has been found that small, high, and isolated features polish very quickly when compared to much wider but still raised features. Also, increased pressure at the corners of these features results in a rounding effect. Previous works have identified underlying metal pattern density as a key factor affecting ILD thickness variation across a chip [14, 15]. The less metal dense part of the chip tends to polish faster than the areas of the chip that have high metal density. One approach to understand this pattern-dependent variation is to use a statistical metrology methodology which incorporates traditional metrology techniques combined with new analysis and modeling elements described in the next section.

1.3 Statistical Metrology Methodology

Statistical metrology is emerging as a methodology to identify, assess and quantify the sources and magnitude of parameter variation. Variation assessment is achieved by identifying and quantifying explicitly the individual sources of variation. The assessment is followed by modeling the various variation components. Statistical metrology can be used in three phases of inter-linked statistical experiments [8]. First, a screening experiment explores a large space of possible layout or process factors that potentially affect a particular device or process parameter. This experiment enables identification of key factors that affect the parameter of interest. Second, a model generation experiment uses additional levels for the identified key factors to build semi-empirical models of parameter variation. Third, a "domain-specific" or environmental experiment can be designed to mimic real products and to focus on the factor levels that typically arise in microprocessor or ASIC designs.

Key elements of statistical metrology include development of electrical or optical test structures to capture the parameter of interest, for example, linewidth structures for critical dimension (CD) variation or capacitance structures for dielectric film thickness, and to gather the volume of data necessary for statistical modeling. The use of short-flow processes to fabricate these test structures is important to insure that minimum variation is introduced to the parameter of interest from the confounding interactions between processing steps. Close coupling to TCAD tools is sometimes necessary for extracting the desired parameters from electrical data as well as for subsequent analysis. This methodology has been applied successfully in the area of poly CD variation [3, 7] and Inter-level Dielectric (ILD) thickness variation in CMP [8].

Previous experiments that utilized this statistical metrology framework to characterize ILD thickness variation have fallen into one or more of the above three experimental design phases. Maung's [16] work laid out a basic foundation for statistical metrology to characterize ILD thickness variation in dielectric planarization processes including BPSG reflow and CMP processes. The focus, however, was an initial screening experiment to help identify key layout factors such as linewidth, linespace, finger length, number of fingers, geometric orientation and an interaction ring responsible for ILD thickness variation. The basic test structure and statistical experimental design methodology were introduced. The work was also extended to study the systematic and random sources of variation including inter- and intra-die variation.

Chang's work [17], on the other hand, was an improved screening experiment but also had elements of modeling and environmental phases. The experiment was designed to model the notion of "interaction distance" or neighborhood distance between the struc-

tures in addition to other key layout factors. The interaction distance refers to the minimum distance between layout patterns such that planarity over one pattern is not affected by the presence of another in that neighborhood. The experiment was also representative of a typical ASIC- type circuit environment so that process effect could be realistically evaluated.

More recent works by Stine et al., have focused on understanding and modeling pattern-dependencies in CMP process using simple test masks [15]. The use of optical test structures were emphasized for rapid data collection and analysis. The test structures, however, are large so that they can be reliably measured given the resolution limits of the optical measurement tools. These studies provide insight into pattern-dependent variation, and introduce concepts and methods of computing global pattern density for ILD thickness variation modeling.

1.4 Contributions of this thesis

As described in the previous section, the importance of polishing the underlying topography in multilevel interconnects for leading-edge technologies is well recognized. The details of pattern dependent polishing, however, are not well understood. First, definitions of pattern density definitions have been ambiguous. Second, little has been reported on the effect of density for the small features typically encountered in realistic chip layouts. In this thesis, we study oxide polishing characteristics over small features (down to 2 μm pitch) and spaces in contrast to the larger features and spaces typically reported (e.g. [18]). Finally, additional enhancements to the statistical metrology framework provide effective methods to understand, characterize and model ILD thickness variation.

This thesis builds upon the previously developed elements of statistical metrology for CMP induced ILD thickness variation reported in earlier works. We emphasize the use of electrical capacitor test structure to infer ILD thickness. However, the test structure is modified to better fit the nature and scope of this experimental design. This statistical experimental design falls within the modeling and environmental phases, where specific layout factors including local density, narrow metal pitch and surrounding dummy-line environment have already been selected. With these factors, we carefully examine how the geometry of the layout patterns affect the planarity within a die. A test mask is designed using realistic layout patterns to mimic chip layouts in high-performance microprocessors. In this way, the impact of CMP process and consumable set on various families of actual layouts can be evaluated using models generated from this experimental mask. Another improved element of the methodology is the procedure used to fit the calibration curves obtained through TCAD simulations to an assumed empirical model form; the major advantage of using such model forms for canonical structures is a reduction in time-consuming simulations. More accurate methods for low-capacitance value measurements are also presented.

1.5 Thesis Organization

An experimental design framework using statistical metrology is presented in Chapter 2. The key elements of the methodology are described including a modification to the design of the electrical test structures used to infer ILD thickness over various local pattern densities. The specific design of the probe layout and test mask is presented and the short-flow process used to fabricate the test die is described. An improved methodology for data conversion using TCAD simulations and better techniques for efficient data

collection using an automated measurement system are also presented. In Chapter 3 the results from the experiment and extensive data analysis for the die-level pattern dependencies are presented. Finally, Chapter 4 presents the summary of the work and its impact in process and device/interconnect characterization. A future direction and extension of this work is also suggested at the end of this chapter.

Chapter 2

Experimental Methodology

This chapter describes elements of the statistical metrology framework utilized to characterize ILD thickness variation. Using this framework, a two-phase inter-linked statistical experimental approach is used. The two-phases of experimental design are model generation and a "domain specific" or environmental experiment. Model generation is supported by exploring in detail the design space of selected factors of interest. The essence of environmental experimentation is captured by designing the mask to mimic realistic chip layouts such as high-performance microprocessors, and by focusing on the design factor levels that typically arise in these chip layouts. In order to design an experiment that combines elements of both phases, several modifications have been made to the existing methodology. These include modification of the existing electrical test structures and test mask design to capture effectively the pattern-dependent ILD thickness variation. Accurate methods for electrical testing are implemented to measure accurately low-capacitance structures. Efficient methods and algorithms are used to generate calibration curves using Technology-Computer-Aided-Design (TCAD) tools in order to extract the desired parameters from the electrical measurements. These methods have an advantage over the previous work [16, 17] in that very few time-consuming simulations are needed to generate such calibration curves.

2.1 Experimental Test Structures: Capacitance and Resistor Structures

The core strength of a statistical metrology experiment is the short-flow test structures that provide large amounts of data for statistical analysis. In this study of CMP, ILD

thickness variation is extracted from electrical measurements using a large set of metal-to-metal capacitors. The test-structure capacitors have a uniform top plate and a bottom layer shown in Figure 2.1(a) consisting of an edge-connected ladder structure which can be arranged in various combinations of layout patterns. This test structure is designed to assess the impact of a set of possible layout factors on the ILD thickness. The primary layout factors examined by the structure itself are the metal pitch and local metal density. In this design, the *metal pitch* is defined as the sum of linewidth and line-space, whereas the l*ocal metal density* is defined as the ratio of linewidth to the metal pitch. Figure 2.1(b) shows the top-view of a bottom-plate of a typical capacitor structure in which the factors are examined by careful manipulation of linewidth and line-space.

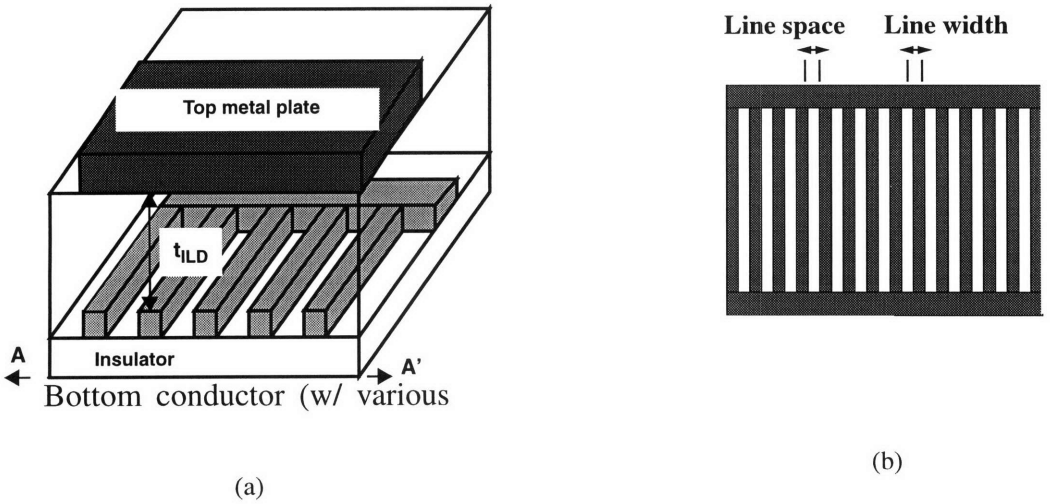

Figure 2.1: (a) Cross-section and (b) top-view of a capacitor test structure showing the metal pitch and local metal density layout factors studied here

The other critical test structures in the electrical measurement approach used here are Kelvin resistors and Van der Pauw structures. The Kelvin resistors are used to calculate the linewidth of the underlying capacitor structure. Linewidths have been found to be very sensitive to systematic variation due to photolithography and etch; the Kelvin resistors

provide direct information regarding the linewidth variation which can then be taken into account in determining the final ILD thickness. The Van der Pauw structure is used to measure the local sheet resistance of the deposited metal layer.

2.2 Experimental Design

A factorial experimental design strategy is utilized to characterize and model effects of layout factors on interconnect ILD thickness variation. This experiment is focused to understand, characterize, and model the effects of fine-feature local metal density, metal pitch and surrounding environment on CMP induced interconnect ILD thickness variation. However, by using just the definition of local metal density presented in section 2.1, the metal pitch becomes dependent on linewidth and linespace factors. For instance, 50% local metal density can be achieved by using metal pitch of 5 μm (linewidth = linespace = 2.5 μm) as well as 2 μm (linewidth = linespace = 1.0 μm). Typical design rules for particular metal layers are described in terms of minimum linewidth, line-space and pitch. Metal pitch is chosen to be the second independent factor so that local metal density can be achieved in a systematic manner. In this way, effects due to both metal pitch and local density can be studied. The final independent factor is the surrounding environment; this is considered for three reasons: First, this factor is chosen to give additional quantitative information regarding the impact of surrounding environment on ILD thickness. Second, this factor allows us to explore issues in longer range density dependence and finally, the neighborhood dummy-line environment acts as a buffer zone from structure to structure, thus eliminating any unintentional neighborhood interaction that would, otherwise, be difficult to quantify and model.

Table I: Summary of Experimental Layout Factors

Structure	Density (%)	Pitch (μm)	Width (μm)	Space (μm)	Number of fingers
1	30	2	0.6	1.4	250
2	30	5	1.5	3.5	100
3	30	10	3.0	7.0	50
4	30	15	4.5	10.5	33
5	40	2	0.8	1.2	250
6	40	5	2.0	3.0	100
7	40	10	4.0	6.0	50
8	40	15	6.0	9.0	33
9	50	2	1.0	1.0	250
10	50	5	2.5	2.5	100
11	50	10	5.0	5.0	50
12	50	15	7.5	7.5	33
13	60	2	1.2	0.8	250
14	60	5	3.0	2.0	100
15	60	10	6.0	4.0	50
16	60	15	9.0	6.0	33
17	70	2	1.4	0.6	250
18	70	5	3.5	1.5	100
19	70	10	7.0	3.0	50
20	70	15	10.5	4.5	33
21	80	5	4.0	1.0	100
22	80	10	8.0	2.0	50
23	80	15	12.0	3.0	33
24	55	12	6.5	5.5	42
25	100	-	-	-	-

Table II: Summary of Surrounding dummy-line Layout

Position in the die	Density of dummy-lines (%)	Pitch (μm)	Width (μm)	Space (μm)
Top	100	-	-	-
Middle	75	20	15	5
Bottom	50	20	10	10

The design challenge is to define the realistic levels of factors for metal pitch and local metal density as well as the size of the structure described in the previous section. At the time of the design, it was assumed that the pattern effects could be explained by consideration of a 500 μm by 500 μm region. Since this experiment is designed to study the pattern density effects using our local pattern density definition, the area for each local structure is fixed at 500 μm by 500 μm so that unintentional area effects are avoided. In order to keep the size of the structure fixed, the number of lines are varied accordingly.

Realistic levels for metal pitch and local density are chosen based on a typical metal interconnect layer of a microprocessor. The values of local metal density range from 30% to 80% in steps of 10%. The metal pitches for each local metal density are 2 μm, 5 μm, 10 μm and 15 μm. An additional 100% local density structure, consisting of a parallel-plate capacitor is also included. The chosen levels of factors span a complete design space of local density and metal pitch. With 4 levels of metal pitch and 6 levels of local density, we obtain 24 unique capacitor structures. Additionally, a center-point structure made up of 55% local density and 12 μm metal pitch is also included to determine the non-linearity of the response.

Other unintentional experimental factors include the spatial location of the structures within a die and within a wafer. Table I summarizes the experimental layout factors.

2.3 Probe & Reticle Design

The probe layout refers to the collection of devices put together in a layout so that all of the devices can be efficiently measured using a probe card at the same time. The probe pattern in this experiment began with a standard 12 by 2 pad configuration (as shown in Figure 2.2). We modified the previous probe pad design [14] by including four extra pads to connect the Van der Pauw structure. Four capacitor structures are combined

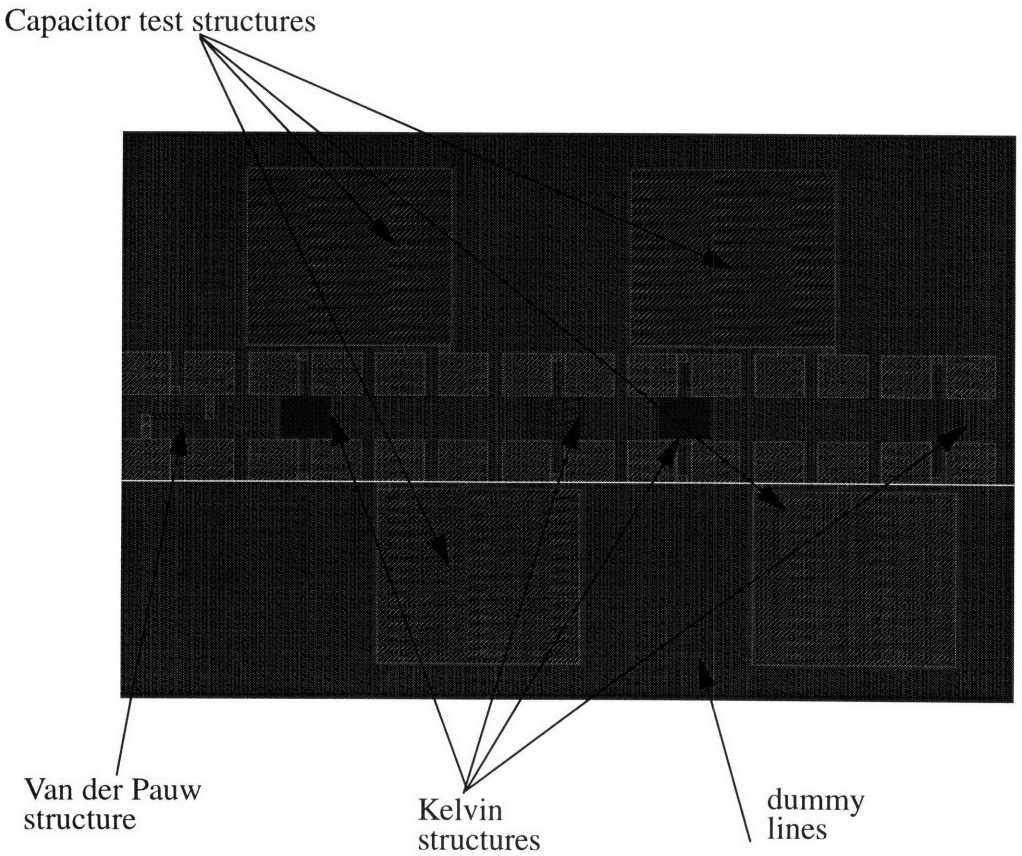

Figure 2.2: A typical probe layout showing the arrangements of capacitor test structures together with Kelvin resistors and a Van der Pauw structure for linewidth and sheet-resistance measurement

together in each probe layout as shown in Figure 2.2. Each probe layout also includes Kelvin resistors and a Van der Pauw structure in order to account for local line-width variation using resistive measurements. The Kelvin resistors are located in the midst of dummy lines which mimic the underlying topography of the corresponding nearby capacitor structure. Each probe layout is replicated three times and placed in a surrounding dummy-line environment of 100%, 75% and 50% densities which are made up of 20 μm metal pitch lines of varying linewidths. Certain probe layouts also contain the center-point experimental design structure which is replicated six times within each dummy-line environment. The specific values of these dummy-line densities are shown in Table II.

These dummy-lines are electrically floating structures and are laid out to be 10 μm from the edges of the active bottom electrode so that there is negligible coupling capacitance between the dummy-lines and structure. However, a probe pad is assigned locally within each probe layout to provide a local ground connection for the entire field of dummy-lines. Additional unused pads are also available to measure parasitic capacitance between the pads and the substrate.

All of the described probe layouts and dummy-line environments are placed in a 15 mm square die as shown in Figure 2.3. In order to fit all the probe layouts, the die is roughly partitioned in such a way that the top third is filled with 100% dummy-line environment and the middle and lower third are filled with 75% and 50% dummy-line environment. To minimize the neighboring die interaction with structures, the scribe-line of the die is also filled with the dummy-lines of the nearby surrounding dummy-line densities.

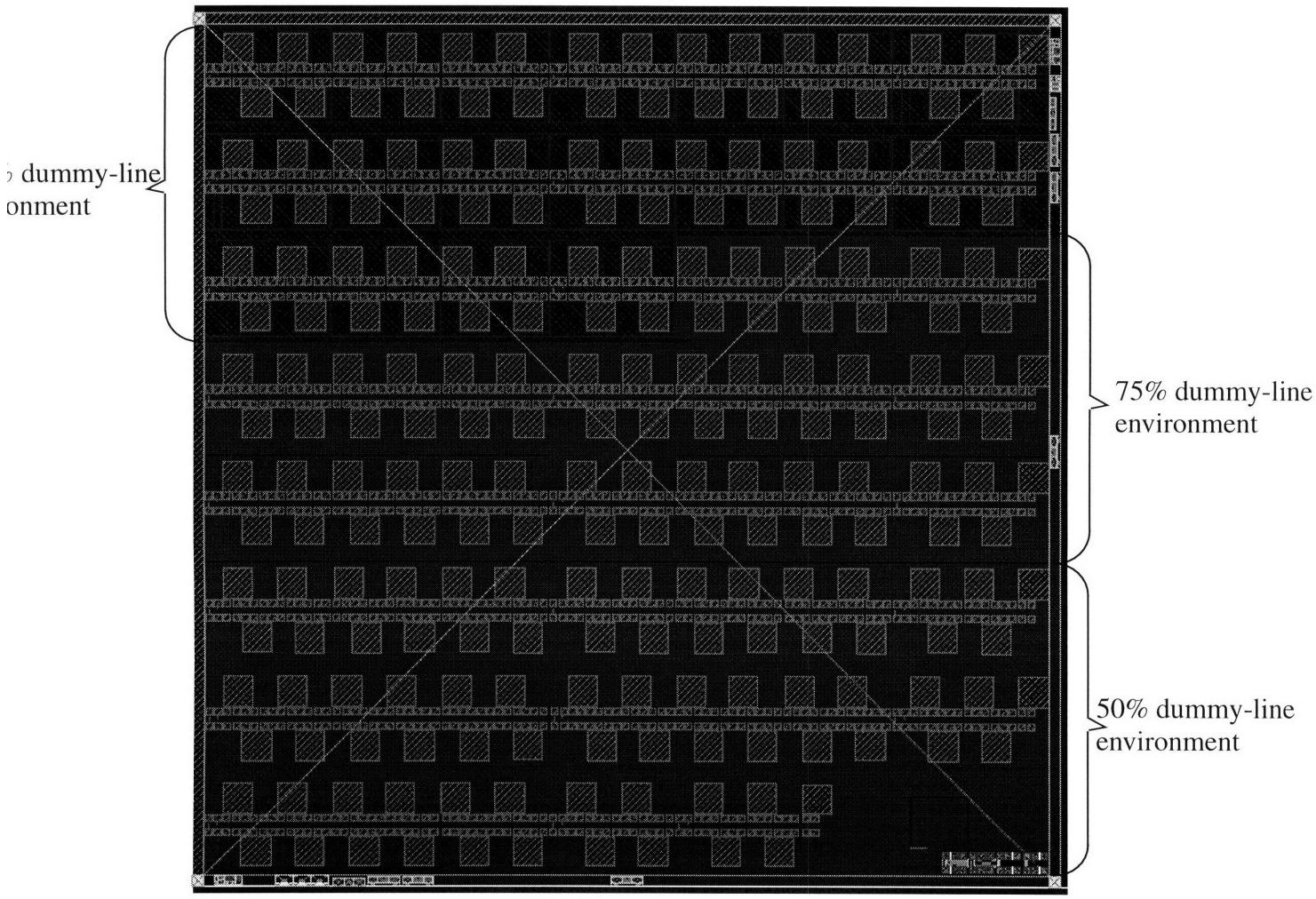

Figure 2.3: Short-loop CMP/ILD die layout showing the arrangement of all the probe layouts and surrounding dummy-line environments

2.4 Short-Flow Process

A short-flow process is desirable to minimize disturbances to the final ILD thickness by preceding processing steps. The short-loop test-die of Figure 2.3 is fabricated on 6" wafers each containing forty-eight dies. A PECVD TEOS layer is initially deposited on bare p-type silicon to provide electrical isolation from the substrate to the next metal layer. Next, a first-layer metal stack (Al:1% Cu with TiN as a barrier layer) is deposited and patterned to form the bottom electrode of the capacitor. A thick PECVD TEOS layer forming the ILD is then deposited and CMP planarized down to the target dielectric thickness. A standard recipe, process and consumable set is used for polishing. This step is followed by etching via holes in the oxide. Contacts are formed by filling the vias with tungsten plugs using TiN glue layer. After tungsten plug formation, a second-layer metal stack is deposited and patterned forming the top capacitor electrode.

2.5 Measurement Metrology & ILD Thickness Extraction Procedure

The electrical measurement metrology, using an autoprobing system and semiconductor parametric analyzer, are very important to gather a large volume of statistically meaningful data. The ILD thickness extraction procedure couples traditional metrology and TCAD simulations to convert the capacitance data into ILD thickness.

2.5.1 Measurement Setup

The measurement programs are defined using HP's ICMS (Integrated Circuit Measurement System) which has a graphical user interface and involves a hierarchical method of defining the measurement test [19]. The Wafer-reference file stores the spatial positions of the dies, the die-stepping distance and wafer diameter. The Die-reference contains the

spatial coordinates of all the probe layouts or modules to be probed. The Module-reference, on the other hand, contains the information about each device and the node connection for each terminal of the device. Finally, Test Definition files are created in which algorithms are specified for each device in the module as well as the number of dies to probe.

2.5.2 Measurement System

For each probe layout on a die, the following automated electrical measurements are performed: high-frequency (100kHz) AC capacitance, line resistance and sheet resistance. These electrical parameters are used to infer the ILD thickness as described in detail in the following section. The capacitance, line resistance and sheet resistivity measurements are performed using an Electroglass wafer probing system interfaced to HP4062C Semiconductor Parametric Tester. The HP4062C consists of a 3488A switching matrix controller, 3458A Multimeter and HP4284A Precision LCR Meter. The connections between the source management units (SMUs) and the probe card pins are made via the switching matrix and are predefined in the ICMS.

The test structures are designed to yield a nominal capacitance of approximately 5pF. Performing low capacitance-value measurements requires attention to several details. Stray capacitances, interference of the measurement signals and other noise are major issues to be considered when performing low-capacitance measurements at high frequency using the HP4284A. These parasitic capacitances are accounted for by measuring the capacitance between the measurement pins before they touch the Device Under Test (DUT). This capacitance is then subtracted from the actual measurement on the DUT. HP4284A typically uses the four-terminal pair measurement configuration which

produces stable and accurate measurements. However, the presence of the substrate will influence the measurement. It is therefore important to isolate the substrate from the measurement by connecting the chuck and subsequently the substrate to the guard terminal. Although the fingered structure on the bottom metal-electrode acts as a shield between top metal-electrode and the substrate, care must still be taken to ensure that the substrate is guarded. Figure 2.4 further illustrates the need for connecting the guard to the substrate. Typically the pad of the top electrode is connected to a HIGH terminal (CMH) and the pad of the bottom electrode is connected to LOW terminal (CML). When the chuck and subsequently the substrate is electrically floating, the combination of parasitic capacitance will influence $C_{measured}$. By guarding the subtracting, $C_{measured}$ is free from the terminal parasitic [20].

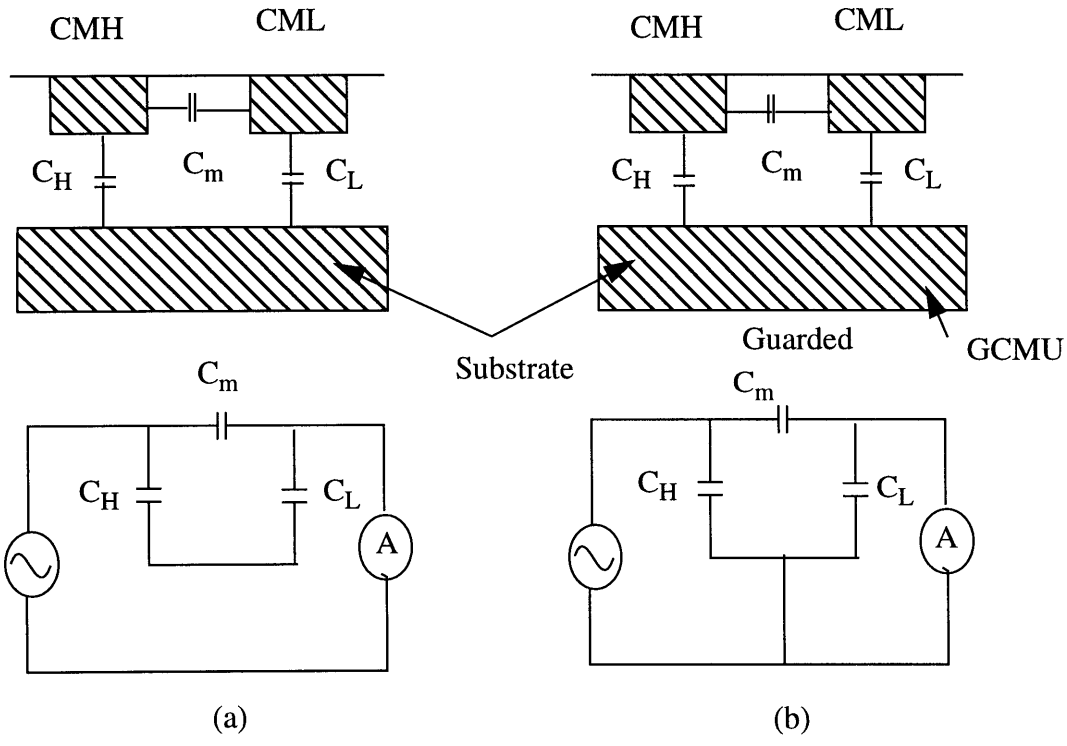

Figure 2.4: (a) When the guard (GCMU) is not connected, C_H and C_L affect C_m (b) with the guard connected to the substrate, C_H and C_L is minimized

The traditional four-point probe technique was used on both the Kelvin and Van der Pauw structures to obtain the resistance values. In this technique, current of 10 mA is forced between the contacts at the opposite ends of the Kelvin linewidth structure and the voltage drop across the line is measured from the two contacts located between the contact taps. The magnitude of the current is chosen so that the measured voltages for all the structures with varying linewidths are between 2.0 and 40 mV [21].

2.5.3 Linewidth Estimation

As described in the previous subsection, we use a Van der Pauw structure in each probe layout to measure the local sheet resistance. Since variation of sheet-resistance is a wafer-level quantity, we assume that the sheet resistance variation within a particular probe layout is small and apply the measured value directly to the associated nearby line-resistance test structure. Based on the specific line resistance and local sheet resistance, local estimates of line width are obtained for each capacitor test structure using Equation 2.1.

$$lw = \frac{R_{Kelvin}}{R_{sheet}} \cdot L \tag{2.1}$$

where lw is the width of the line, L is the known length of the line, R_{Kelvin} is the specific resistance of the Kelvin resistor structure and R_{sheet} is the local sheet resistance obtained from the nearby Van der Pauw test structure.

2.5.4 ILD Thickness Conversion & TCAD Simulations

The second step in the data extraction procedure is the conversion of capacitance and line-width data to ILD thickness values. Since the capacitor test structures are not parallel-plate capacitors, the two-dimensional capacitance simulator, RAPHAEL

[22], is used to generate ILD thickness versus capacitance and line-width lookup tables for each canonical test structure as shown in Figure 2.5.

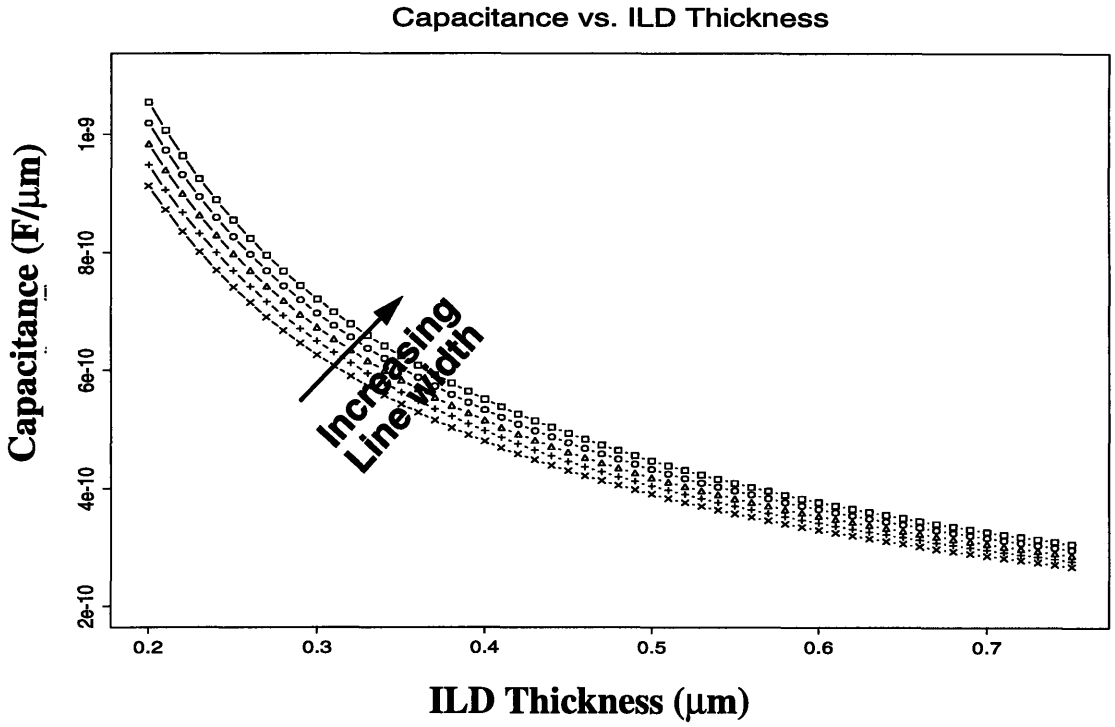

Figure 2.5: Capacitance vs. ILD thickness curves generated using RAPHAEL simulator for a canonical structure from the design

Since these numerical simulations are computationally intensive, we do not simulate the entire test structure; as shown in the Figure 2.6, we simulate a periodic structure of one-half line on each side of a full middle line. Reflecting boundary conditions are used at the outside edges of the half-metal lines; the half-metal lines on the sides are needed to account for fringing fields. The simulation yields the capacitance per unit length of the middle line to the top plate (C_{12}) as a function of the main geometric design parameters:

$$C_{12} = f(lw, ls, t_{ild}, t_m, t_{fox}, \varepsilon) \tag{2.2}$$

where *lw* is the linewidth, *ls* is the line spacing, t_{ild} is the ILD thickness, t_m is the metal thickness, t_{fox} is the field oxide thickness and ε is the dielectric constant of the interlevel dielectric.

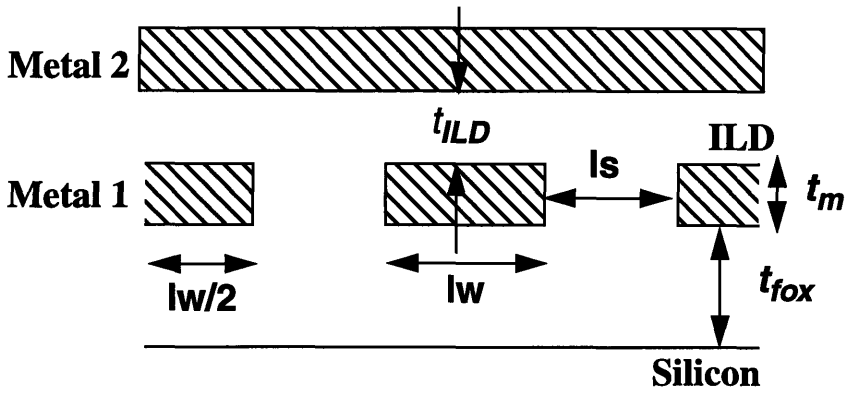

Figure 2.6: 2D RAPHAEL simulation of a typical structure using a planarized ILD

Since the metal and field oxide thickness dimensions are typically controlled to within satisfactory tolerances, they are fixed at their nominal values in the simulation; independent verification through simulation is also done to verify minimal sensitivity of the capacitance C_{12} to the conductor thickness. We assume that the relative dielectric constant of the planarized TEOS dielectric does not vary substantially across the wafer; we also assume the TEOS to be isotropic with fixed $\varepsilon = 4.0$. The capacitance of the entire structure can be computed using Equation 2.3, which incorporates the capacitances of the connecting edges of the structures:

$$C_{tot} = (C_{12} \times nof \times fl) + C_{edge}. \tag{2.3}$$

Using the above strategy, a family of capacitance curves can be generated for different values of $lw \pm \Delta lw$ for constant pitch. Equation 2.2 can be modified as:

$$C_{12} = f(lw + \Delta lw, ls - \Delta lw, t_{ild}). \quad (2.4)$$

Figure 2.5 shows typical calibration curves for a canonical 2D test-structure geometry.

In order to reduce the number of time consuming simulations required to generate the calibrate on curves, a modified approach to that in [16, 17] is utilized. Since the curves shown in Figure 2.5 are continuous and smooth, there exists a well-behaved relationship between the capacitance and ILD thickness for various canonical structural parameters such as line-width and metal pitch, assuming all other process parameters do not vary substantially. We use the empirical formula of J. Chern et al. for line-to-ground capacitance for two-ground planes [23]. We retain the basic form of the formula and refit the parameters in line-width and metal pitch only. Using this approach we simulate only a few selected curves for various canonical structures and fit the simulated data to the formula using a non-linear regression technique. In particular, a set of four linewidth curves are simulated for each metal pitch. For example, for a 2 μm metal pitch, the capacitance curves are simulated for linewidths of 0.6 μm, 1.0 μm, 1.4 μm and 2.0 μm. Using this technique, we generate the capacitance formula for all four different pitch values. The model R^2 for the formula is 0.9999967. The basic formula for a canonical structure is shown in Equation 2.5:

$$\frac{C_{12}}{\varepsilon} = \frac{lw}{t_{ild}} + 0.5357\left(1 + 1.8698e^{\frac{-0.5660}{pitch - lw}} - 1.6157e^{\frac{-0.7456(pitch - lw)}{t_{ild}}}\right) \quad (2.5)$$

$$\left(\frac{pitch - lw}{t_{ild}}\right)^{-0.3246}\left(\frac{0.76}{t_{ild}}\right)^{0.7456}$$

where *pitch* is metal pitch, *lw* is the linewidth, t_{ild} is ILD thickness, C_{12} is the capacitance per unit length and ε is dielectric constant of interlevel dielectric. The range of the validity of the formula is shown below: $0.6\mu m \leq lw \leq 12\mu m$ and $2\mu m \leq pitch \leq 15\mu m$. Figure 2.7 shows the verification of the formula and simulations for various linewidths and pitches. In all cases, the correlation is very close to 1.0.

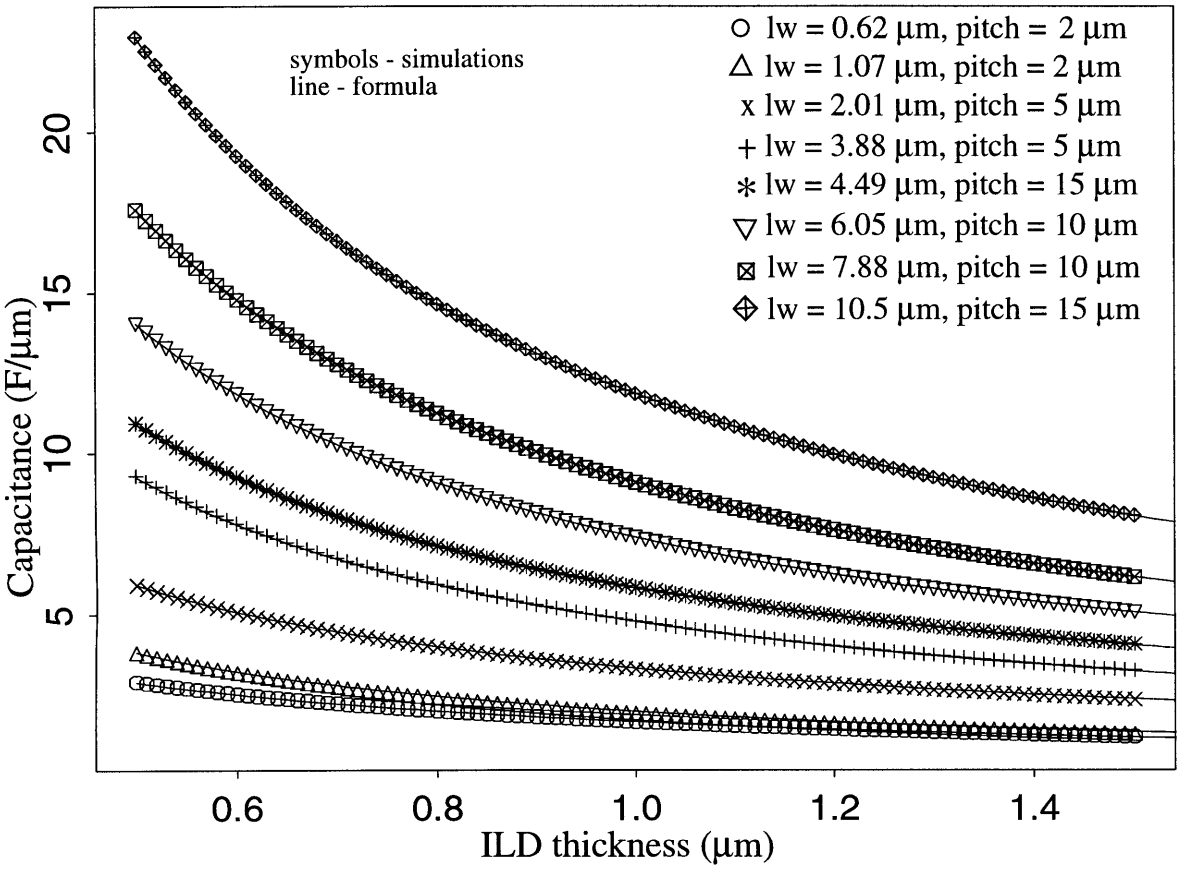

Figure 2.7: The calibration curves for various canonical structures showing a very good agreement between direct simulations and empirical formula

From the measured capacitance data and the corresponding linewidth obtained from the formula, the ILD thickness can then be estimated via two-dimensional linear interpolation as shown in Equation 2.6:

$$t_{ild} = f(C_{tot}, lw \pm \Delta lw). \tag{2.6}$$

2.5.5 Data Collection/ Organization

The data from the measurement system is in a "flat" format which must be processed and organized before applying the methodology described above. Data sorting is facilitated by using a series of parser programs written in PERL and C. The PERL script takes as its input the raw data file and the wafer number, and splits it into 25 different files, each file represents one of the 25 unique structures. Each file contains the complete data for the measured die of a particular wafer. The file contains the capacitance value, linewidth value, die number, subdie number, x and y-coordinates of the measurement site. Next, batch processing is done to convert the capacitance to ILD thickness data. This is achieved through a C program that takes each of the data files and its associated look-up table and performs a linear interpolation to Equation 2.6. Prior to the data analysis, each structure file is appended with the factor labels and combined into a database containing about 9000 data points for a particular wafer. Once this database is built, the data is ready for statistical analysis using the Splus Statistical software.

Chapter 3

Experimental Results and Analysis

This chapter presents the experimental results of extracted ILD thickness for a representative wafer (BXD11-2) processed and measured using the procedures of Chapter 2. Since the focus of this chapter is to examine the effects of intra-die pattern dependencies, the raw data from one die near the center is first presented. The data from one die is sufficient to explain the trends and effects of pattern variation. However, a complete dataset for an entire wafer is needed for statistical analysis; and future work will examine such wafer data in order to make conclusive statements about variation.

3.1 Extracted ILD thickness Data

This section presents the extracted ILD thickness data for one die near the center of the wafer BXD11-2. All final ILD thickness data presented in this chapter has been consistently normalized by an arbitrary constant to protect proprietary technology information. Lines drawn in the figures are a spline fit through the mean of the measured data points.

Figure 3.1 shows the ILD thickness data for all the structures within the die. As can be seen from the plot, there is a considerable variation of ILD thickness within the die. This can be further seen from the histogram of ILD thickness in Figure 3.2 which shows a large spread in the data. The mean of ILD thickness in a given die is about 7865 angstroms with an associated standard deviation of 727 angstroms. The range of thickness from the lowest spot on the die to the highest spot is 3150 angstroms. While wafer-level variation due to process variations or disturbance in equipment and/or consumable set is small, the

die-level variation is largely due to the underlying layout patterns. The following section presents key effects of underlying layout patterns on ILD thickness variation.

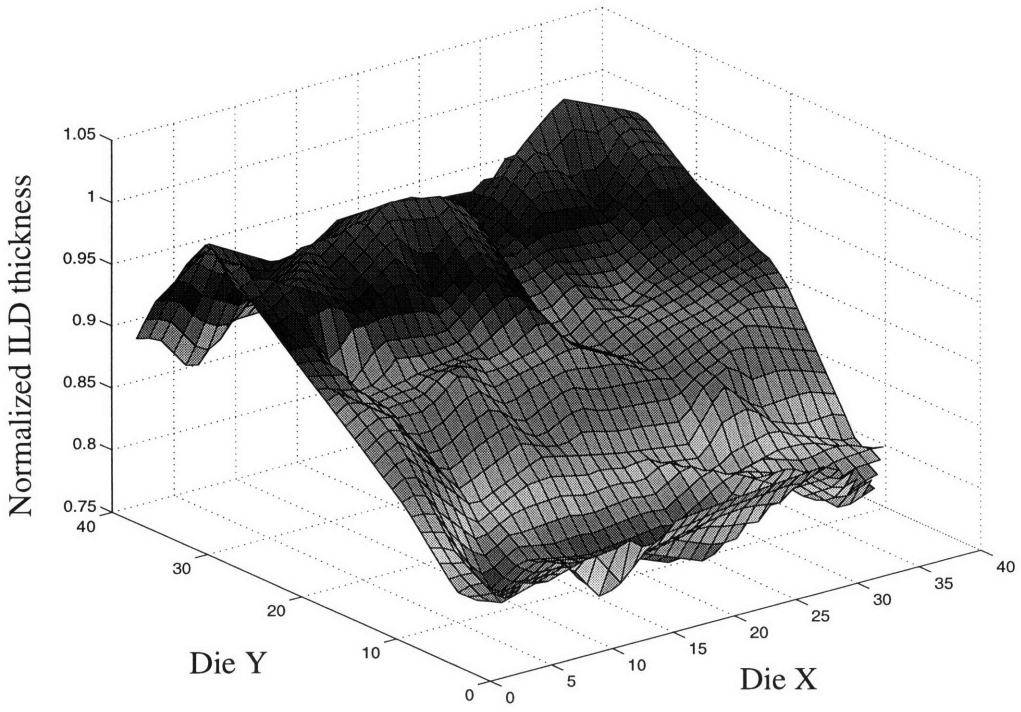

Figure 3.1: Perspective plot of ILD thickness of all structures in die 17

3.2 Effects of fine-feature patterns on ILD thickness variation

In this section we will examine the various dependences of extracted ILD thickness on the designed layout factors. The key dependences that we want to explore are the role of surrounding dummy-lines and metal pitch on ILD thickness variation.

3.2.1 Impact of surrounding dummy-lines

The major function of the dummy-lines in this design is to explore the longer range or global density issues. Figure 3.3 (a,b,c,d) shows the normalized ILD thickness as a function of local density; each line in the plot corresponds to one of the three surrounding dummy-line environments. Each of the subplots refers to the specific designed metal pitch. As the local metal density increases, the final ILD thickness is observed to increase monotoni-

cally, except for the case of 2 μm pitch where the ILD thickness appears to be nearly constant.

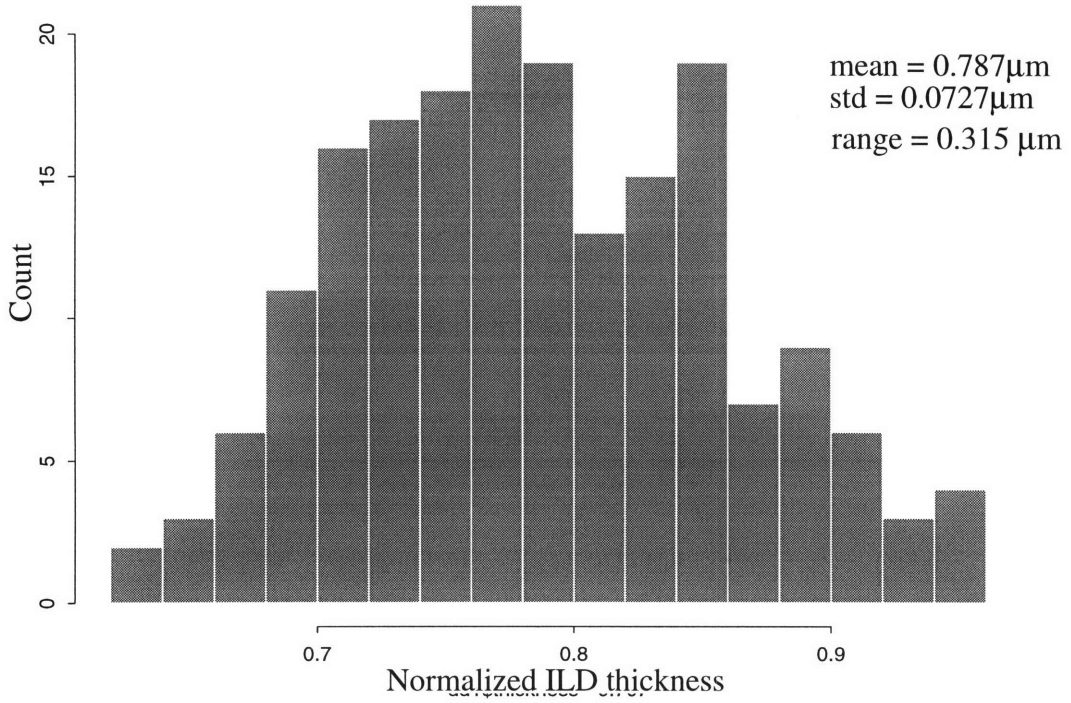

Figure 3.2: Histogram of ILD thickness in die 17 (Wafer BXD11-2)

At each particular pitch, we observe significant differences in the final thickness for the three dummy-line environments as shown by the pronounced separation between each line.

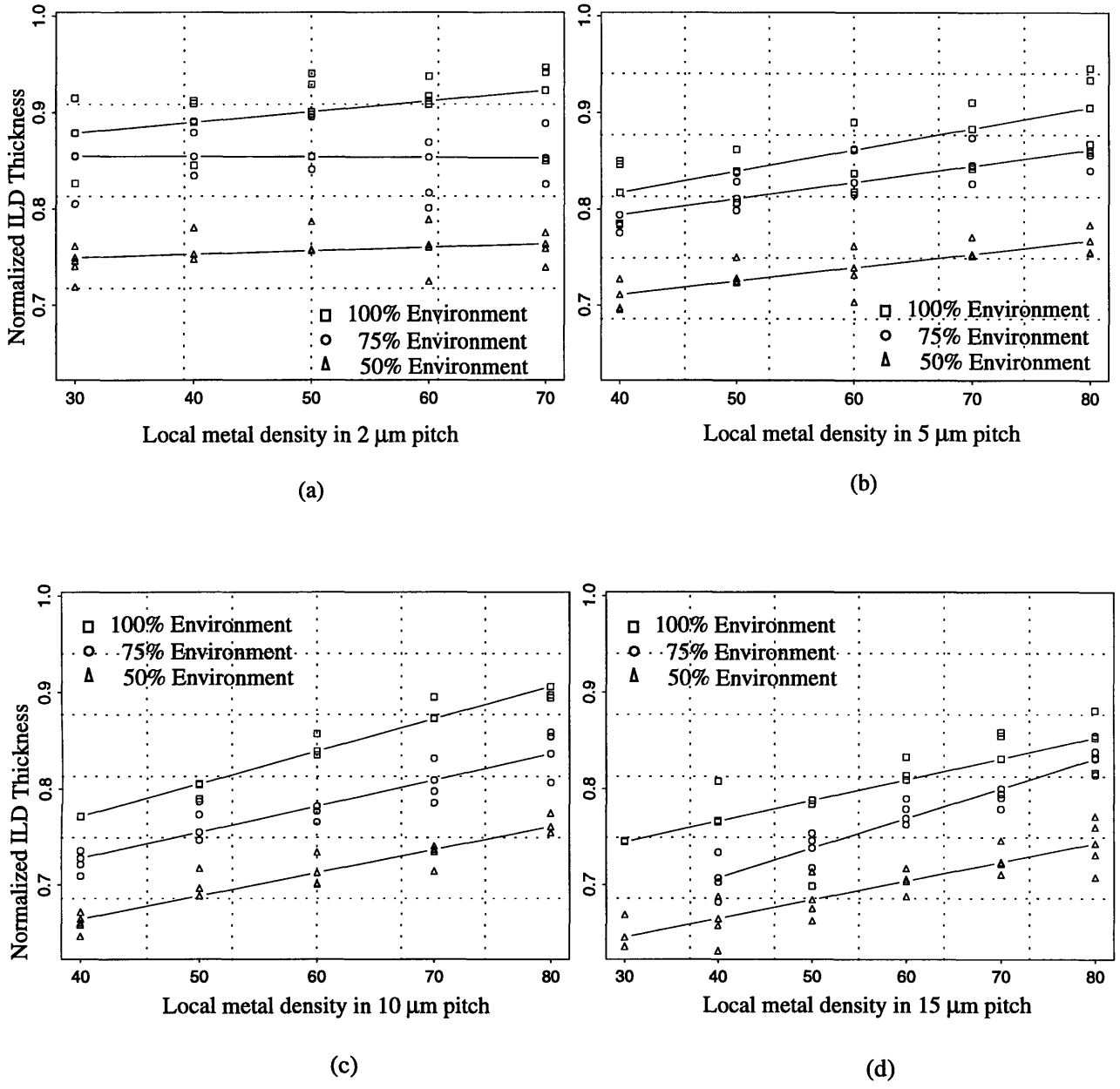

Figure 3.3: ILD thickness as a function of local metal density for (a) 2 μm (b) 5 μm (c) 10 μm and (d) 15 μm metal pitch

The magnitude of the thickness variation implies that the surroundings have a substantial impact on the thickness variation and that local density alone is not sufficient to explain this variation. In order to explain the longer range pattern density issues, there is a need for

a generalized density metric which integrates the effects of local densities and surrounding dummy-line densities; this will be discussed further in section 3.3.

3.2.2 Impact of narrow metal pitch

The impact of narrow metal pitches is important because such fine lines and spaces are often found in realistic chip layouts at intermediate interconnect layers (for example Metal1 to Metal4 layers). It is hypothesized that arrays of lines made up of 50% metal density and tight pitch (e.g. 2 μm) may have different polishing characteristics than a sparse pitch (e.g. 50 μm). One potential mechanism is acceleration of the polish near feature edges; the tighter pitch areas present more edge contact area and thus may polish at a faster rate than sparse pitch lines. Alternatively, local stresses may be greater for large pitch lines (due to less nearby structural support for the pad), so that sparse pitch lines may polish more rapidly.

Figure 3.4(a,b,c) shows the final ILD thickness as a function of the local metal density; in these plots, each line corresponds to a specific designed metal pitch. Each subplot is for one of the three surrounding dummy-line environments. Figure 3.4(b), for example, shows ILD thickness vs. local metal density in a 75% environment. We observe a linear trend for each designed metal pitch with the exception of the 2 μm pitch structures, where a relatively constant dependence on local density is observed. Also, as can be seen from the spacing between the different lines, the sensitivity to the metal pitch value decreases for larger pitches (e.g. the difference between the 2 μm and 5 μm pitch is much greater than the difference between the 10 μm and 15 μm lines). Similar behavior is also observed for the other dummy-line environments (Figures 3.4 (a) & 3.4 (c)).

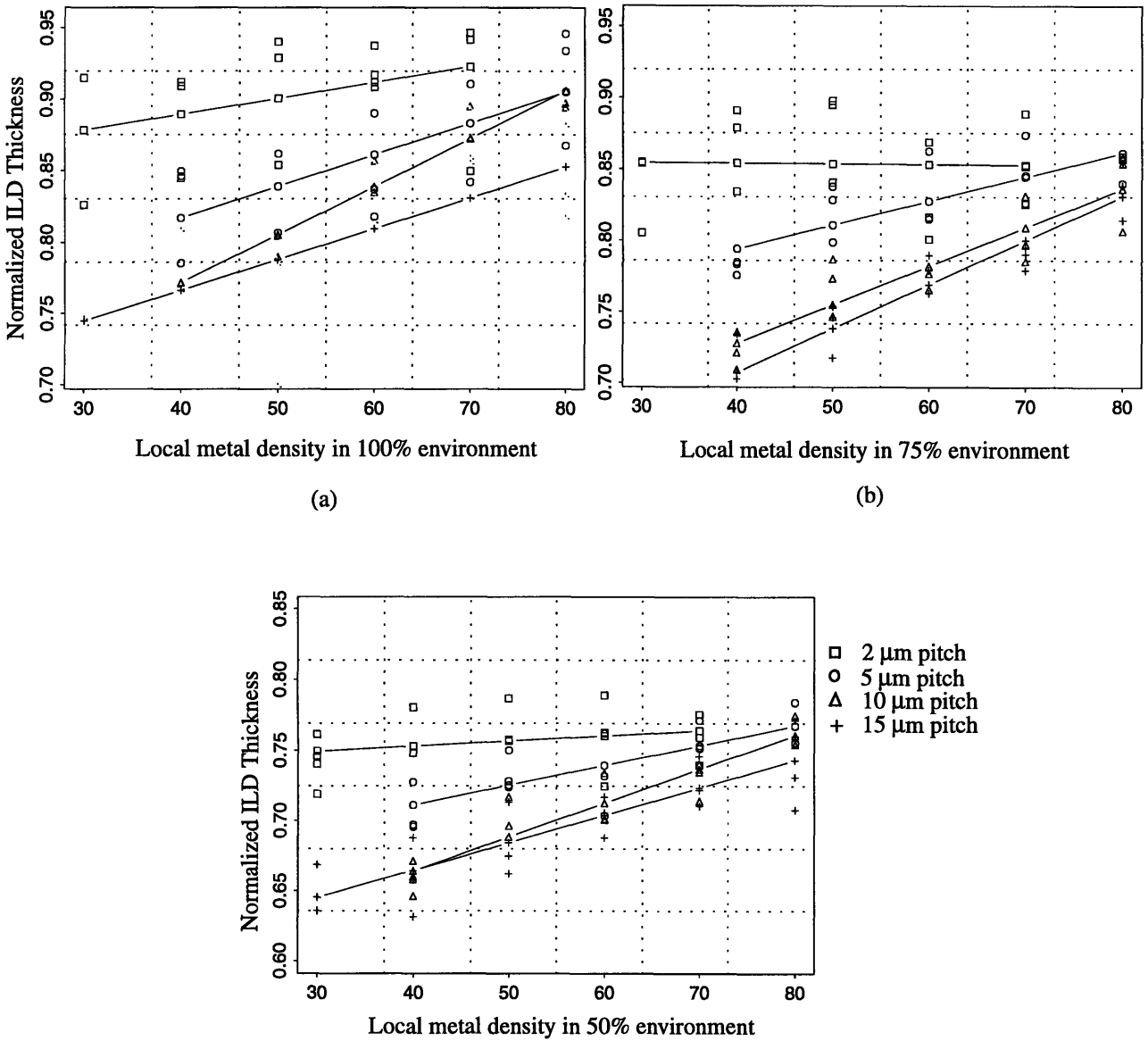

Figure 3.4: ILD thickness as a function of local metal density in (a) 100% (b) 75% (c) 50% surrounding environment

3.2.3 ILD thickness variation assessment

A qualitative results above show that surrounding environment has quite an impact on ILD thickness variation. In order to quantify the effect of various layout factors on ILD thickness, an ANalysis-Of-VAriance (ANOVA) method can be employed. Table III provides insight into the specific layout factors that affect the die-level thickness variation. In Table III the surrounding environment appears to contribute the most to the variation in ILD thickness, followed by the pitch and local density. The significance of these terms is indicated by the F and probability values in the Pr(F) column indicating that the observed differences between the terms could not have arisen by chance alone.

Table III. ANOVA Table for Wafer BXD11-2

Layout factors	Df	Sum of Squares	Mean Squares	F-Value	Pr (F)
Environment	2	0.9410006	0.4705003	348.2612	0.000000
pitch	4	0.4578707	0.1144677	84.7282	0.000000
local density	5	0.3081254	0.0616251	45.6145	0.000000
local density: pitch	12	0.0585056	0.0048755	3.6088	0.000084
Residuals	165	0.2229147	0.0013510		

3.3 Analysis and Discussion

In previous section we established some of the key layout factors that impact ILD thickness variation. Specifically, the significant impact of surrounding dummy-lines suggests that there is a need to evaluate a global pattern density effects that come into play during CMP processes. In this section, we explore in detail the evaluation of global density from the layout using available CAD or mask-generation tool.

3.3.1 Global density evaluation

The results in the previous subsection suggest that the polishing characteristics of a particular structure are largely a function of the combined local density of the structure and its environment. The global density is determined by an effective area over which the pad "responds" to surface topography and transmits this response (e.g. through pad bending) to nearby polish behavior. As seen from the plots of Figure 3.3, different environments around a particular structure have a large influence on the local polishing behavior. As a result the effective area within which the density needs to be calculated is seen to be larger than the particular structure size in our layout (500 μm by 500 μm in this case). Each structure is large enough, however, that the effective global density in and surrounding that structure is also significantly impacted (and experimentally probed) by the structure itself. We thus find that careful evaluation of the global density is necessary in order to understand the polishing behavior of an arbitrary structure within a particular environment.

A general metric for global pattern density can be defined as the ratio of metal area in an arbitrary square window to the area of the window. We use a square window to perform global density evaluation, because it is easier for a CAD tool to do computation using a square window compared to a circular window or a tapered window. The main drawback of this approach is that we assume that the polishing pad "sees" the density in a square region. However, the polishing pad is elastic in nature and can conform to the surface and as a result it may see the density in some form of a tapered circular window. In this study, we calculate pattern density for a square window from the center of a structure. The global density profile of the our layout, calculated using a 4.0 mm square window, is

shown in Figure 3.5. The density profiles of our layout for several window sizes are available for analysis.

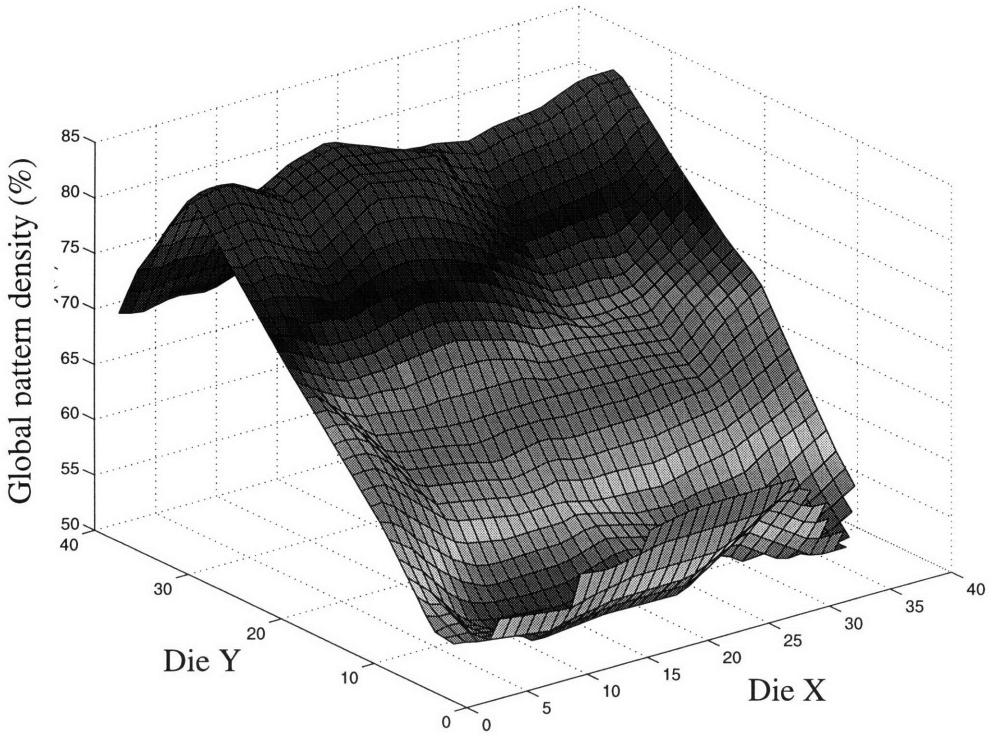

Figure 3.5: Global pattern density evaluated in a 4.0 mm square window

Using these density profiles, ILD thickness is regressed onto the global pattern density using a linear model and the model correlation is examined. As the window size increases the model correlation between ILD thickness and global density improves, reaches a maximum value and then decreases. Figure 3.6 shows the correlation (R^2) of ILD thickness vs. a window size showing an appropriate choice of window for global density calculation. Since the window is assumed to be square, its size can be represented by the length of one side of the window. The figure shows that the model correlation of ILD thickness and global density is maximum for a square with an edge of 4.0 mm. We thus

conclude that, for the representative CMP process and consumable set used in this study, a 4.0 mm window

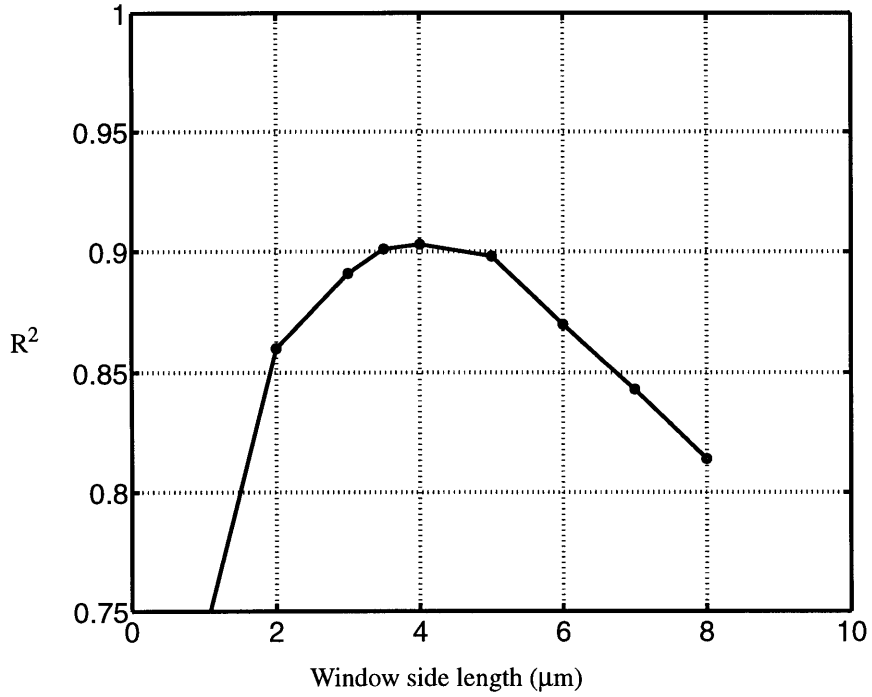

Figure 3.6: R^2 vs. window side length showing an appropriate choice of window for global density computation

is an appropriate window size to evaluate global density from the layout for each structure. Considering the structures with line-spaces greater than 3 μm in the figure, we find that a general linear trend in ILD thickness is observed as a function of the calculated combined global density using the 4.0 mm window size.

3.3.2 Narrow line-space issues

In Figure 3.7, we see two distinct groups of structures that exhibit different dependencies upon the global pattern density, those structures with line-spacing of greater than 3 μm and those with line-spacing less than 3 μm. We propose that this density dependence is

due to differences in the ILD deposition profile between the small and large line-space structures.

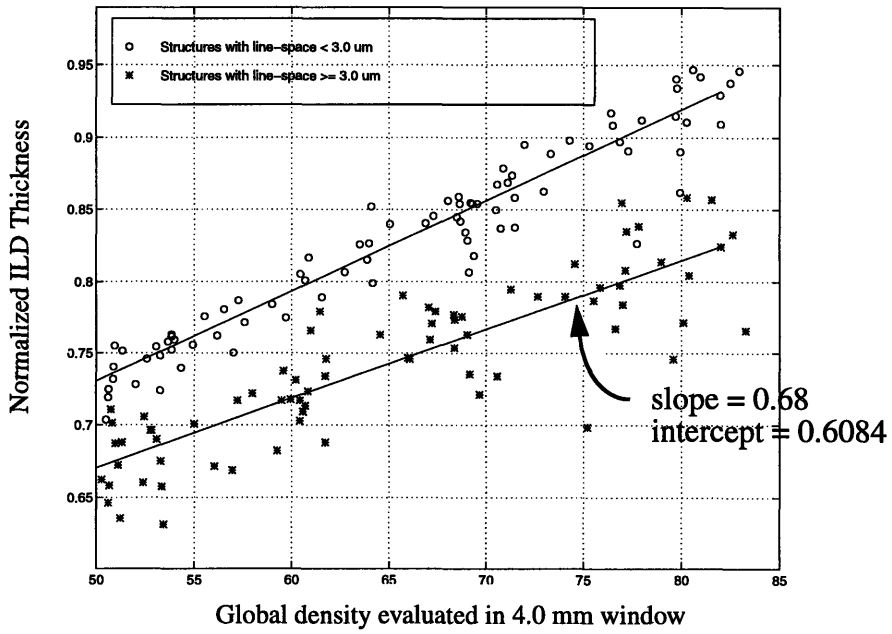

Figure 3.7: ILD thickness as a function of global pattern density evaluated in a 4.0 mm square window

The SEM images in Figure 3.8 contrast the initial deposition profile for structures with narrow line-spaces and large line-spaces. The smaller features exhibit substantial lateral deposition, resulting in a relatively flat topography compared to the larger features which have a more conformal deposition. In addition, we find that the initial step-height of the before-polish deposited dielectric film is a function of line-spacing, as shown in Figure 3.9. As a result of these step-height differences, small and large line-spaces structures will have different polishing behavior. The apparent pitch/line-spacing dependence in Figures 3.4 and 3.7 is also a manifestation of these differences in the initial deposition profile. The effect of initial step-height on profile evolution can be accounted for using the model in [24], and will be considered in the next section.

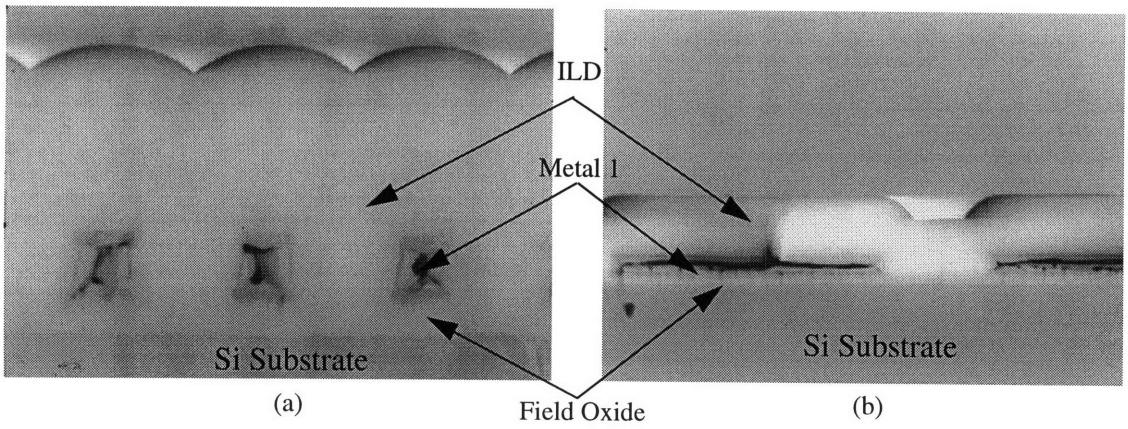

Figure 3.8: Cross-section SEM of a structure with (a) narrow line-space (b) large line-space showing the deposition profile before CMP

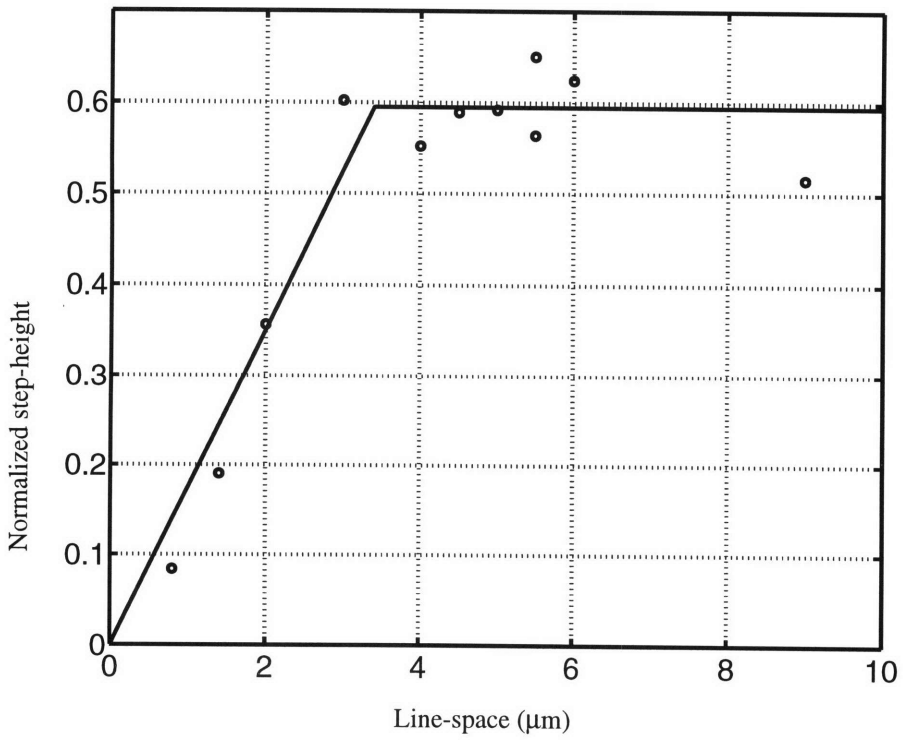

Figure 3.9: Pre-CMP step-height as a function of line-space for various structures

3.3.3 Empirical modeling of ILD thickness variation

Having established systematic ILD thickness dependence due to the layout factors, the next step is to model the layout-dependent ILD thickness variation. A closed-form analytical model has been proposed by Stine et al. which takes into account the topographical profile evolution with time and which can incorporate the details of the initial deposition profile such as in Figure 3.8. The model is very simple and has a few deterministic parameters which are readily available from the process-line.

The model for thickness after a sufficiently long polish time when all the patterns have been polished away is shown in Equation 3.1

$$z = z_0 - z_1 - Kt + \rho(x,y) \cdot z_1 , Kt > \rho(x,y) z_1 \quad (3.1)$$

where *z0* and *z1* are the initial step-heights over and between the metal regions, *K* is the average blank wafer removal rate, and *d* is the global pattern density evaluated in an appropriate window size. For this process the blank wafer removal rate, *K*, is 1357 angstroms/min, and polish time was about 2.96 minutes for given process settings and consumable set. The height above the metal is 1.63 μm whereas the step-height, *z1*, is pattern-dependent as shown in Figure 3.9. As a result, *z1* can be only expressed as an effective step-height from the layout. One way to compute an effective step-height from the layout is to examine the percentage of the layout covered by the patterns that have line-space of greater than 3 μm. Since the surrounding dummy-line environments with 20 μm pitch cover roughly about the two-thirds of the layout, we expect the effective *z1* to be about 0.6 μm. Using these parameters we find that the model predicts the intercept and the slope of the model for structures with line-space greater than 3.0 μm to be 0.63 and 0.6. Comparing these parameters with the ones obtained by a linear model in Figure 3.7, we find that

the model by Stine et al. matches very closely to the empirical, statistical model for this process and consumable set.

Chapter 4

Conclusion

4.1 Summary

Improving the yield levels in semiconductor manufacturing involves reducing the variabilities associated with each processing step. In order to reduce variation, there is a need to identify and quantify the sources of variations by improving data collection and analysis methods. In this thesis a working methodology for statistical metrology is presented to understand, characterize and model systematic and random sources of ILD thickness variation in oxide CMP processes. The experimental design emphasizes both modeling needs and circuit-like environments to characterize and model ILD thickness variation.

We have studied oxide polishing over fine pitch metal features using dedicated electrical test structures. The experimental results show that the final polished oxide thickness for a particular structure in an arbitrary surrounding may be effectively modeled as a function of global density over an empirically determined square window. The pitch/line-spacing effect observed suggests that the deposition profile shape needs to be taken into account in CMP modeling. The characterization of CMP-induced variation sources via statistical metrology will become increasingly necessary for accurate pattern dependent ILD thickness prediction, and for layout and process design optimization, improved process control, interconnect simulation, and robust circuit design.

4.2 Future work

There are several issues that remain to be explored in this experiment. Since we have

found that initial deposition profile plays a key role in polishing behavior, there is a need to explore this in more detail. Further work needs to be done in quantifying the apparent pitch effect by taking into account the initial lateral deposition effects. A simple approach is to bias all the linewidths in the layout by a factor that represents the lateral deposition effect and re-compute the global pattern density using appropriate CAD tools.

Moreover, the results presented in this thesis represents a fixed process condition and a consumable set. In order to make the results generalizable, several process conditions and consumable sets must be examined.

In this thesis we have only examined the pattern-dependent effects in one die. A thorough analysis should be done to account for die-to-die and within-wafer variation. It is equally important to quantify various components of variation such as wafer-level vs. die-level. These results will be very useful in accurate pattern-dependent ILD thickness prediction and for layout and process design optimization.

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