SILICON MICROACCELEROMETER FABRICATION TECHNOLOGIES

by

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Submitted to the

DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

September 1997

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August 1997

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Submitted to the Department of Electrical Engineering and Computer Science
on August 5, 1997, in Partial Fulfillment of the Requirements
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ABSTRACT

This thesis describes the development of silicon microaccelerometers fabricated from single-crystal silicon using the electrochemical junction etch-stop technique and silicon wafer bonding. The goals of this thesis are two-folded. The first goal is the development of *"surface-micromachining-like"* structures such as tuning fork gyroscopes and accelerometers fabricated from single-crystal silicon using silicon wafer bonding. These micromechanical devices can be integrated monolithically with electronics using a wafer-bonded sealed cavity process and a low-temperature thermocompression metal-to-metal bonding technique. The second goal is the development and characterization of the MEMS-CMOS integrated sensor technology based on the wafer-bonded sealed cavity process. This development was conducted in collaboration with the Ph.D. research of L. Parameswaran. The unique contribution of this author was the detailed characterization of the mechanical properties of the bonded silicon membrane through the complete CMOS flow.

The integrated MEMS-CMOS process is partitioned into three sections: front-end micromachining, integrated circuit formation, and back-end micromachining. Front-end micromachining consists of using silicon wafer bonding to make a sealed cavity microstructure that is the base element of the transducer. Back-end micromachining steps consist of release etches from the front and backside of the wafer to form surface and bulk-micromachining-like structures respectively, and the formation of a top capacitive electrode. The wafer-bonded sealed cavity process utilizes either silicon-on-insulator (SOI) wafers or electrochemical etch technology to obtain electrically-isolated, three-dimensional micromechanical structures. A variety of microelectromechanical structures with arbitrary shapes, various die sizes, and mechanical structure layers specified over a range of thicknesses can be fabricated with this technology. This process is demonstrated by fabricating capacitive microaccelerometers whose structures are implemented using design features intended to reduce overall die size, improve output linearity, improve insensitivity to external stresses, and control the effects of squeeze-film damping in small gap microstructures.

A number of 5g and 50g microaccelerometers with two different tether designs were successfully fabricated. Experimental results on 5g and 50g folded pinwheel tether devices with proof masses of 515μm×515μm×10μm, and a nominal gap spacing of 1μm, yielded DC sensitivities of 0.062 and 0.002pF/g, and amplitude responses (measured dynamically using sinusoidal input accelerations) with linearity of < 2% FSO. The frequency response of these devices indicate that the devices are overdamped at atmospheric pressure, but the damping control perforations implemented in the design of structures' proof mass were successful in dramatically reducing (by more than two orders of magnitude) the expected worst-case damping due to squeeze-film effects.

Thesis Supervisor: Martin A. Schmidt
Title: Associate Professor, Department of Electrical Engineering and Computer Science

Acknowledgments

First, I have to thank *Min-Min-Shang-Ti* (God), the source of all things, for blessing me with the talents and abilities to make it through MIT, strength, and the encouragement of family and friends.

The completion of this long and sometimes laborious course of graduate studies could never of been accomplished without the consistent support of the many people in my life. Tremendous thanks and appreciation go to the *Hsu's family* who always believed in me and supported me anyway they could. But especially, my love and gratitude go to my Parents, Hsu-Sun Hsu and Mei-Chi Huang Hsu, for their unconditional love and their seemingly limitless emotional, moral, and financial support. They introduced me to *Tao* (the Natural Goodness of Man's Heart) and taught me the value of hardwork, perseverance, dignity and, most of all, to love and respect myself and others.

I owe a special thanks to Professor Martin Schmidt, my thesis advisor, whose guidance always kept me on the right track and whose faith in me and my abilities was both a source of strength and a source of motivation. I admire his technical know-how's, his intelligence, and his empathic manner; all of which in conjunction with his excellent communication skills made him the commanding leader in our ever-growing MEMS research group. I would also like to acknowledge the other members of my thesis committee, Professors Stephen Senturia and Charles Sodini for their suggestions and comments, as well as Professors Hae-Seung (Harry) Lee and Akintunde Ibitayo (Tayo) Akinwande who were kind enough to help me with the last-minute accelerometer detection circuit analysis and accelerometer natural frequency testing, respectively, on somewhat short notice.

I was fortunate to be associated with a wonderful group of people in the Schmidt Group both past and present, including Errol Arkilic, Arturo Ayon, Christopher Bang, Ted Bloomstein, Roberto Devoto, Samara Firebaugh, Albert Folch, Reza Ghodssi, Howard Goldberg, Michael Huff, CC Lin, Vince McNeil, Mitch Novack, Aravind Padmanabhan, Lalitha Parameswaran, Mark Sheplak, Ravi Srinivasan, Joel Voldman, and Joey Wong. I benefited greatly from their collective knowledge, as well as the breadth of discussion topics of both technical and sometimes more personal ones. I'd like to thank Lalitha in particular for the joint work we did in process development and other collaborative work. I would also like to thank Michael Ashburn, who spent much effort in designing his circuit to operate in conjunction with my sensor, as well as for providing some of the hybrid-accelerometer test data. I think they, along with all the other students

in the Microsystems Technology Laboratories, that I've come to know, are one of the nicest groups of people I've had the chance to work with and I wish them the very best in all of their endeavors.

The technical contribution of my colleagues in the Schmidt Group, the Senturia Group, and the Smith Group, past and present, cannot be belittled. A tremendous amount of credit must be given to Mitch Novack and Vince McNeil who did a fantastic job in paving the way for the successful design and fabrication of the current accelerometers. A special thank you goes to Peter Osterberg for being one of my best friends at MIT and for his tireless pursuit in perfecting the M-Test structure design and the pull-in technique. Thanks to Joseph Young for a highly successful modeling work on the squeeze-film damping study. A sincere thank you to Errol Arkilic for design and construction of a number of versions of our ECE etch-jigs. Thanks to Euclid Moon for being another close personal friend and for his wonderful inputs and suggestions during my Area Exam preparation. A word of sincere appreciation goes to our Group administrator Pat Varley, who dealt with the day-to-day administrative tasks which were a necessary evil in keeping the Group happy and productive.

ICL and TRL staff, past and present, were instrumental in training me and maintaining the equipment needed to conducted my research. I have to thank them all for their patience, humor, friendship, and technical expertise which made the long hours in lab more bearable. Thanks to MTL lab staff Dan Adams, Bernard Alamariu, Jim Bishop, Kurt Broderick, Pat Burkhart, Rob Cuikay, Joe DiMaria, Brian Foley, Octavio Hurtado, Mark Laroche, Paul McGrath, Nestore Polce, Paul Tierney, Tim Tyson, Joe Walsh, and Dick Westberg. Our Lab Managers, Dr. Linus Cordes and Dr. Vicky Diadiuk, deserve thanks for technical advice and keeping the labs running. Technical support for my thesis was also generously given by Dr. Andy Mirza and Dr. David Bosch of Motorola who provided the Motorola SOI wafers, and William Easter of AT&T who provided the AT&T SOI wafers for this research.

To the many other students and support staff in Microsystems Technology Laboratories who have provided me help or assistance at some time or another, I like to say a general *thank you* to all, but I would like to particularly say thanks to G. K. Ananthasuresh (Suresh), Roxann Blanchard, Mike Chou, Steve Decker, Jeff Gealow, John Gilbert, Raj Gupta, Ken Liao, Jen Lloyd, Joe Lutsky, Philip Nee, Vladimir Rabinovich, Melanie Sherony, Dan Sobek, Lisa Su, Albert Young, and Paul Yu. I should also thank Professor Hank Smith for allowing me access to equipment in NSL, and to Jimmy Carter, Mark Mondol, and Jeannie Porter for training and technical support. Thanks to our present and past computer system managers.

The majority of this work was supported by the Semiconductor Research Corporation under contracts 92-SC-309 to 96-SC-309.

Finally, I'd like to thank Chi-Chi, my newly wedded wife, for her patience, love, and unshakable belief in me over these last couple of years. Your being there helped me in ways I can barely begin to thank you for.

Dedication

This thesis is dedicated to the White Water Elder, Yu-Ling Han, my grandmother, Lian-Bung Hsu, to all my family, my wife, and to all my Dao-Ching who gave me the courage to march proudly to finally see the light at the end of the tunnel.

Contents

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 5

Appendix A

Appendix B

Appendix C

List of Tables

Chapter 1

Introduction

Silicon has become synonymous with IC (integrated circuit) technology in the past forty years thanks to its electronic properties. Silicon integrated circuit technology has been responsible for creating an entirely new industry in electronics and for revolutionizing the information processing field. Silicon-based microelectronic devices are everywhere in modern life, with some manner of electronic interface being found in virtually every environment, to control and enhance the performance of electronic equipment of all varieties. Most of these electronic systems interact in some way with the physical world through sensors to convey input to the machine's controller and actuators which in turn provide output to act on the external world. These sensors and actuators are categorized generally as transducers. A subset of microfabrication-based transducers has drawn much attention in the past decade and has come to be known generally as MEMS (MicroElectroMechanical Systems). An excellent introduction to MEMS and an overview of the different MEMS technologies can be found in [1–3].

There has been a tremendous amount of research and development in microelectronics technology, much of which is being assimilated and widely used to develop and increase the capabilities of MEMS. MEMS devices are generally fabricated using manufacturing processes that are similar to those used in a modern IC foundry. However, new innovations in process technology and modeling have been developed to meet the needs of a wide variety of transducer applications. The development of microscale mechanical devices was predicted as far back as 1959 by Feynman [4], and MEMS devices had expanded to encompass numerous applications by the time a review paper by Petersen was published in 1982 [5], summarizing the state of the art at the time.

Since the bulk of solid state electronics is made from silicon, it is natural to utilize silicon for transducers also. Silicon has an elastic modulus comparable to that of stainless steel ($E_{Si,\,(100)}$ = 190GPa, E_{steel} = 210GPa) and a yield strength that is about twice that of steel ($\sigma_{Si,\,yield}$ = 7,000MPa, $\sigma_{steel,\,yield}$ = 4,200MPa). It surpasses aluminum in strength to weight ratio and the lack of hysteresis in single-crystal silicon (SCS) makes it a perfect material for making micromechanical devices. Furthermore, silicon exhibits a number of transduction effects, such as piezoresistivity, photoconductivity, magnetoresistivity, and thermoresistivity [6], all of which are exploited in various sensors. Perhaps most importantly, silicon can be manipulated into a variety of shapes through the use of the same lithography and etching tools used to fabricate ICs, as will be described in subsequent sections.

The goals of this thesis are two-folded. The first goal is the development of *"surface-micromachining-like"* structures such as tuning fork gyroscopes and accelerometers fabricated from single-crystal silicon using silicon wafer bonding. These micromechanical devices can be integrated monolithically with electronics using a wafer-bonded sealed cavity process and a low-temperature thermocompression metal-to-metal bonding technique. The second goal is the development and characterization of the MEMS-CMOS integrated sensor technology based on the wafer-bonded sealed cavity process. This development was conducted in collaboration with the Ph.D. research of L.

Parameswaran [7]. The unique contribution of this author was the detailed characterization of the mechanical properties of the bonded silicon membrane through the CMOS flow. The wafer-bonded sealed cavity process utilizes either silicon-on-insulator (SOI) wafers or electrochemical etch technology to obtain electrically-isolated, three-dimensional micromechanical structures. A variety of microelectromechanical structures with arbitrary shape, various die sizes, and mechanical structure layers specified over a range of thicknesses can be fabricated with this technology. This process is demonstrated by fabricating capacitive microaccelerometers whose structures are implemented using design features intended to reduce overall die size, improve output linearity, improve insensitivity to external stresses, and control the effects of squeeze-film damping in small gap microstructures.

1.1 Integrated Sensor Technologies

In recent years, research efforts have been growing steadily in the field of integrated microelectromechanical systems. The large demand for integrated sensors has been fueled by the strong economic incentive to replace bulky and usually pricy transducers with a more compact integrated version at a lower cost. Earlier work in microelectromechanical sensors focused mainly on the development of silicon diaphragm pressure transducers. Today, working from the vast knowledge base accumulated over decades of silicon process development supplemented by specialized lithography, deposition and etching techniques, significantly more complicated microstructures have been designed and fabricated. These transducer applications include nozzles for ink-jet printers, inertial sensors, actuators for optical alignment, and complex flow systems for chemical and biomedical applications.

This section reviews some of the current approaches to achieve sensor-circuit on-chip integration. Three approaches are discussed here: circuits-first, micromachining-first, and a partitioned approach. Furthermore, a choice is also needed as to the micromachining toolset to be used, commonly one of bulk micromachining, surface micromachining, dissolved wafer, or wafer bonding processes. Examples of each of these categories are given in the following sections.

Circuit-First Approach

This may be the most commercially successful approach to date. Both bulk and surface micromachined integrated sensors have been demonstrated with this circuit-first approach. This approach consists of fabrication of the integrated circuit on the substrate and passivation of the circuit, followed by micromachining steps, and finally with dicing and packaging.

When bulk micromachining is employed, the sensor is fabricated from the same silicon wafer that eventually houses the circuitry. This requires that the silicon substrate be of an impurity type and concentration compatible with integrated circuits, while allowing micromachining steps to be incorporated for the precise fabrication of the required microstructures. One of the techniques that has been utilized to satisfy these requirements utilizes an electrochemical etchstop to create microstructures such as diaphragms [8]. Figure 1–1 shows the cross-section of a typical integrated sensor implemented using this technology. The microstructure in this process is usually formed from single-crystal silicon material of one type (n- or p-type) grown epitaxially over a standard silicon substrate of opposite impurity type (p- or n-type). The epi layer is grown to the proper thickness dictated by the sensor requirements, and has the appropriate impurity concentration required for the fabrication of active devices. The circuit process is then performed on the silicon wafer to implement the desired functions. Following circuit integration, the sensor microstructure is formed using an electrochemical etchstop through the back of the silicon substrate. One of the drawbacks to this method is

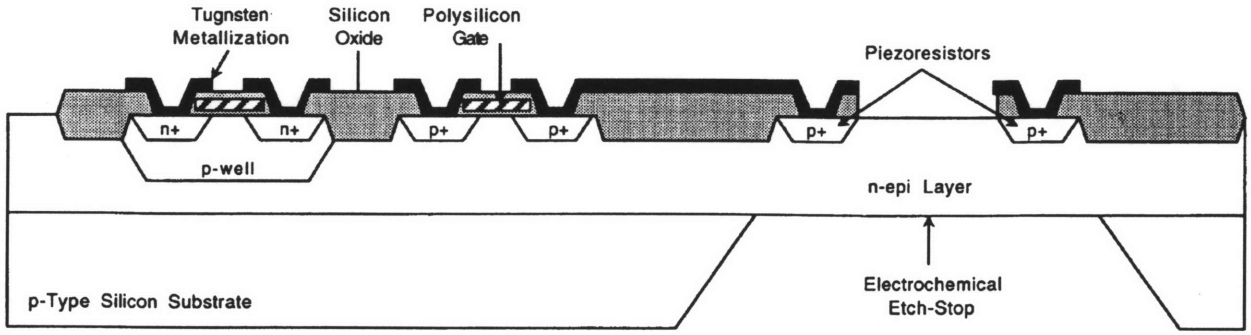


Figure 1–1: Custom technologies for solid-state integrated sensors: cross-sectional view of integrated sensors fabricated using p-n junction electrochemical etch-stop (after *Ref. 8*).

that it produces a low device density, since the size of the opening on the back of the wafer is much larger than the sensor (active area) as a result of the anisotropic nature of the etch. With the progression to larger diameter (and thicker) wafers, this problem can only become worse.

An alternative bulk micromachining process that alleviates the device density issue is that of performing the final silicon removal on the front of the wafer, after encapsulating the structure in layers of suitable mask materials (Figure 1–2) [9–10]. The silicon etch is done with a conventional anisotropic etchant such as potassium hydroxide (KOH), ethylene-diamine pyrocatechol (EDP), or tetramethyl ammonium hydroxide (TMAH). This method is most attractive for devices that require thermal isolation as evidenced by its use in infrared sensors and thermopiles; however, it may not be as suitable for mechanical sensors since layers of different films (as masking materials) are left on the active areas, thus with associated stress issues. This process has been standardized so that the circuits and structural layers are fabricated in a commercial foundry, and the final release etch is the only step that is micromachining specific.

Conventional surface micromachined integrated sensors are also circuit-first process. The circuit process is usually carried through the metallization step, at which point the micromachining process begins. Since several high-temperature steps have to be performed to complete the sensor process, the metallization material used in the circuit should be capable of tolerating these steps. Therefore, refractory metal silicides are usually employed. A process developed at the University of California, Berkeley, uses a combination of titanium nitride and titanium silicide to form a high-quality contact region, and a layer of CVD tungsten to form the metal interconnects [11–12]. After the circuit process is completed, the entire wafer is covered with a low-temperature oxide and silicon nitride passivation layer to protect the electronics from the etchants used in the sensor-fabrication process. Sensor fabrication utilizes two layers of low-pressure CVD polysilicon that are patterned in a standard surface micromachining technology, with a silicon dioxide sacrificial layer between them. The sacrificial layer is finally etched in

hydrofluoric acid to finish sensor processing and release the microstructures formed to implement the sensor (Figure 1–3). Note that the circuitry is protected from the HF etch using the nitride passivation layer deposited previously. This process has been used to develop an integrated accelerometer [12], and a modification of the process has been used by Analog Devices, Inc. (ADI) to produce a commercially available accelerometer [13]. Please note that though ADI's BIMOS II integrated accelerometer process employs aluminum (Al) for all metal lines, platinum (Pt) silicide and titanium-tungsten/aluminum-copper (TiW/AlCu) are also used for the necessary thin-film resistors. Yun *et al.*' surface micromachined integrated sensor process is also available as a foundry-based service [14], with a fairly well-established set of design rules within which the designer can construct any structure that can be defined by a mask. While this technique is fairly widely used, it is difficult to make high aspect ratio structures as they require thick film depositions. Furthermore, control of the structural properties of the thin film(s) is extremely important and somewhat difficult to control from run to run. Also, the high temperature polysilicon deposition and anneal steps impose constraints on the circuit process due to the larger thermal budget needed.

Silicon-on-insulator (SOI) substrates can also be used to make single-crystal silicon surface micromachined devices, by treating the buried oxide layer (BOX) as the sacrificial layer. This method has been employed to make an accelerometer [15] and a microphone [16]. Pressure sensors have also been made by growing epitaxial silicon on top of the SIMOX (separation by implantation of oxygen) silicon layer, after which the buried oxide is removed [17].

Micromachining-First Approach

The micromachining-first approach is to fabricate the microstructures (i.e., sensing elements) prior to any circuit processing steps. This approach integrates the micromechanical structures and the electronics modularly; thus no major modifications of either process are needed for the process integration. However, due to the standard

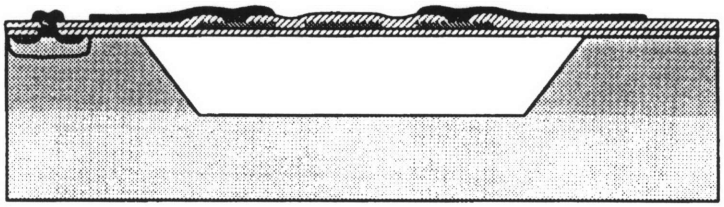


Figure 1–2: Bulk micromachined pressure sensor: frontside bulk etching using TMAH (after *Refs. 9–10*).

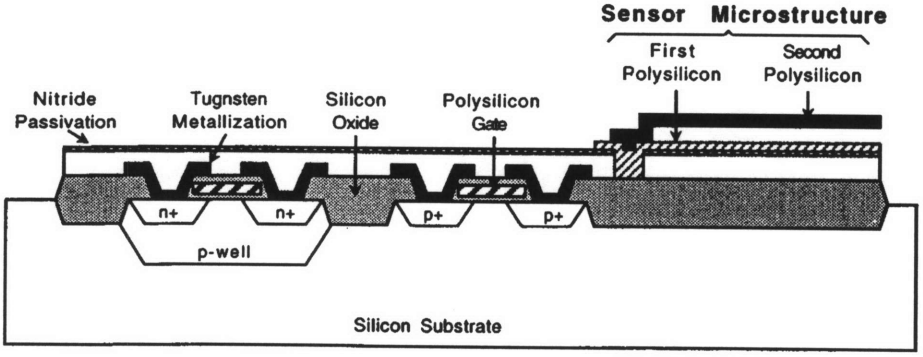


Figure 1–3: Surface micromachined integrated sensors (after *Ref. 11*).

CMOS/Bi–CMOS fab-line lithography and handling constraints, the very large topographies or unusual materials encountered in many types of sensors must wait until the circuitry is completed and simply cannot be processed via this approach. Thus, this approach finds limited use in today's integrated sensor applications.

Partitioned Approach

As the first example for a partitioned approach, an interleaved approach has been proposed, where the micromechanical element is partially fabricated, stabilized in some manner to protect it during the circuit process, and then exposed at the end of the process. Sandia Laboratories has recently developed such a process utilizing polysilicon as the structural element [18]. The polysilicon structures are formed in a trench initially etched in the starting substrate, after which they are completely embedded in a deposited oxide which fills the trench (Figure 1–4). This oxide layer is planarized with CMP (chemical-mechanical polishing) and sealed with a silicon nitride cap, and CMOS processing then proceeds. After the circuit fabrication, the polysilicon structures are released with a conventional wet sacrificial oxide etch. This method offers advantages of process modularity but requires CMP, as well as having the same release and thin-film control issues of conventional surface micromachining.

Another example of the partitioned approach is the dissolved wafer process in which the structural regions are defined with the formation of recessed areas and p^{++} diffusions. The wafer is then patterned and anodically bonded to another substrate. The wafer containing the diffused layer is etched from the back leaving the heavily doped layer intact (Figure 1–5). In order to incorporate circuitry into such process, an active-dissolved wafer process has been designed, using electrochemistry to protect selected lightly doped areas of the silicon substrate during the bulk removal step. These areas contain the circuits as well as some additional resistors to assist in the electrochemical etch. This process has been successfully implemented to make accelerometers integrated with CMOS op-amp's (operation amplifier) [19].

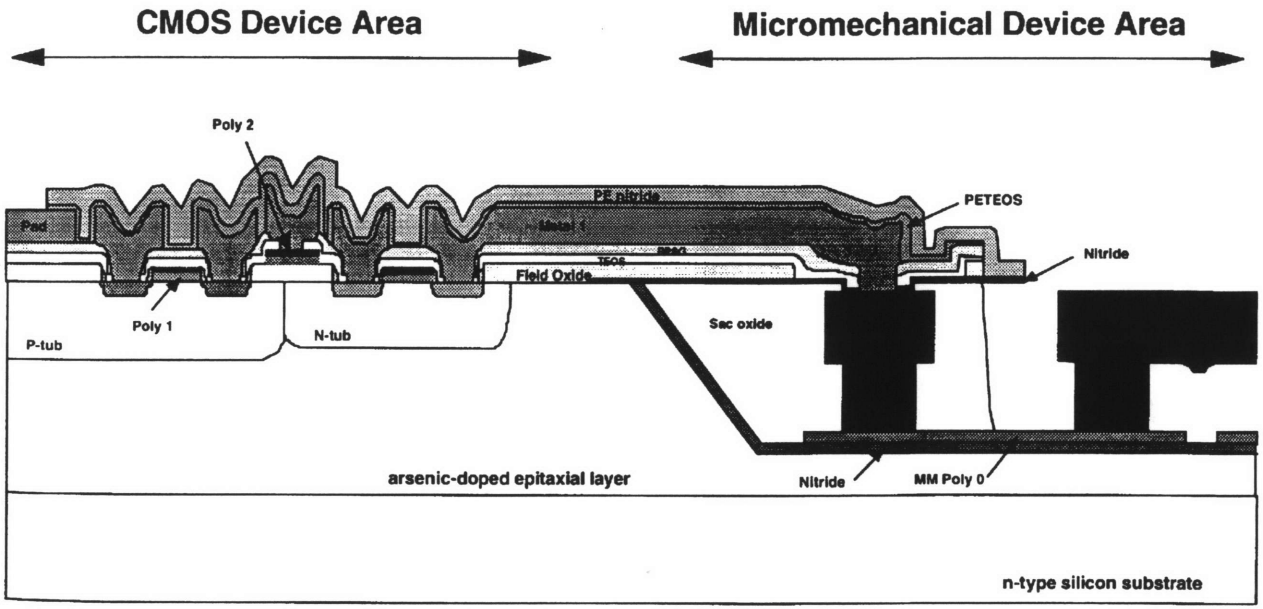


Figure 1–4: A cross-sectional schematic of the subsurface, embedded MEMS integrated technology (after *Ref. 18*).

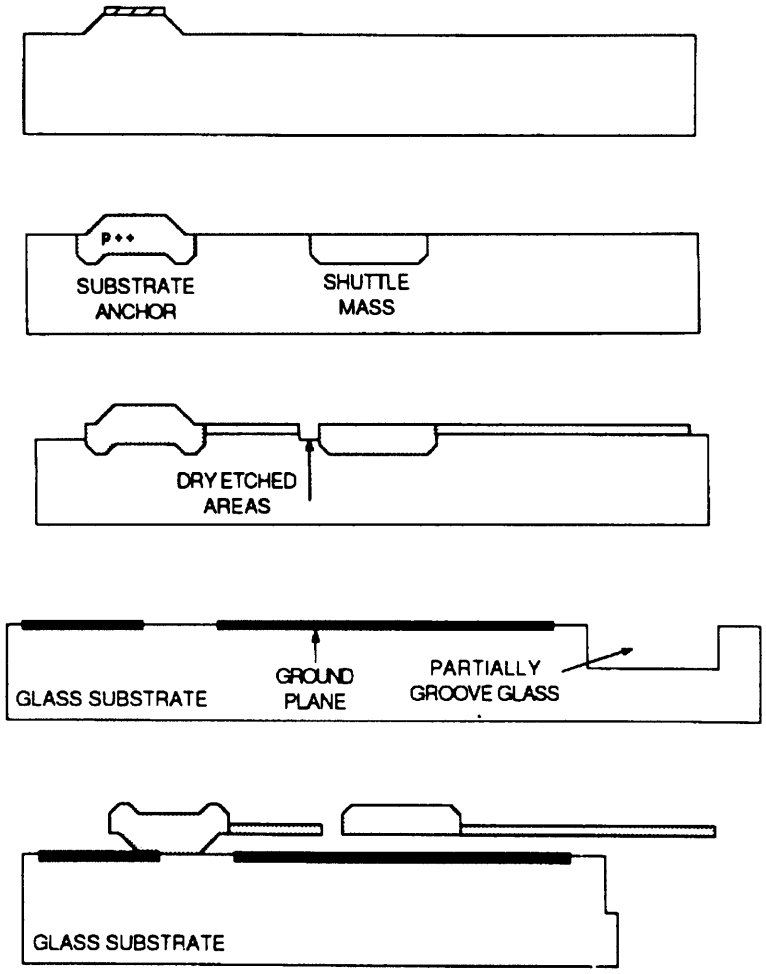


Figure 1–5: Thin layers of single-crystal silicon made by bonding and back etching. The process involves the selective doping of silicon with high doses of boron, anodic bonding, and release etch (after *Ref. 19*).

Silicon wafer bonding combines the advantages of bulk micromachining (single-crystal structural material) and surface micromachining (small device structures). In this case a thin silicon structural layer is added to a base substrate with predefined cavities. Therefore no wet release to remove sacrificial material is required, and the suspended layer thickness can range from <1μm to a full-wafer thickness. Furthermore, annealing is not needed for stress relief of the thin film, and since the substrate and the structural material are identical, there is no mismatch in thermal coefficients to consider. The mechanisms of wafer bonding, as well as studies of the bond interface, are explained in detail in [20–22] and will not be repeated here. However, since the integrated sensor process (co-developed with Parameswaran) proposed in this thesis utilizes silicon wafer bonding and various etching methods to fabricate sensors, the wafer-bonded integrated sensor technology is described next.

Wafer-Bonded Integrated Sensor Technology

Forerunners in the integrated sensor field have proclaimed that it is critically important for any process technology intended for the integrated sensor application to have an effective *process partitioning* scheme. In particular, it is highly desired to partition the fabrication processes such that the integrated circuit fabrication sequence is not perturbed by the micromachining. In order to achieve the above objective, it is crucial for integrated sensor researchers to have an intimate knowledge of the details of the IC processes used in the IC fab-line, as well as the basic understanding of the limitations of current circuit manufacturing technologies. A generalized yet versatile process partitioning scheme plays an important role for the success of the particular integrated sensor family being designed and implemented in a research or industrial laboratory. To summarize, the processing sequence of a circuit fab-line should not be interrupted to perform special processing functions for sensors (i.e., micromachining processes). Pulling wafers out of a circuit fab-line, doing a special process, and re-introducing them midway through the sequence may compromise the circuit performance, yield, and reliability. Instead, special

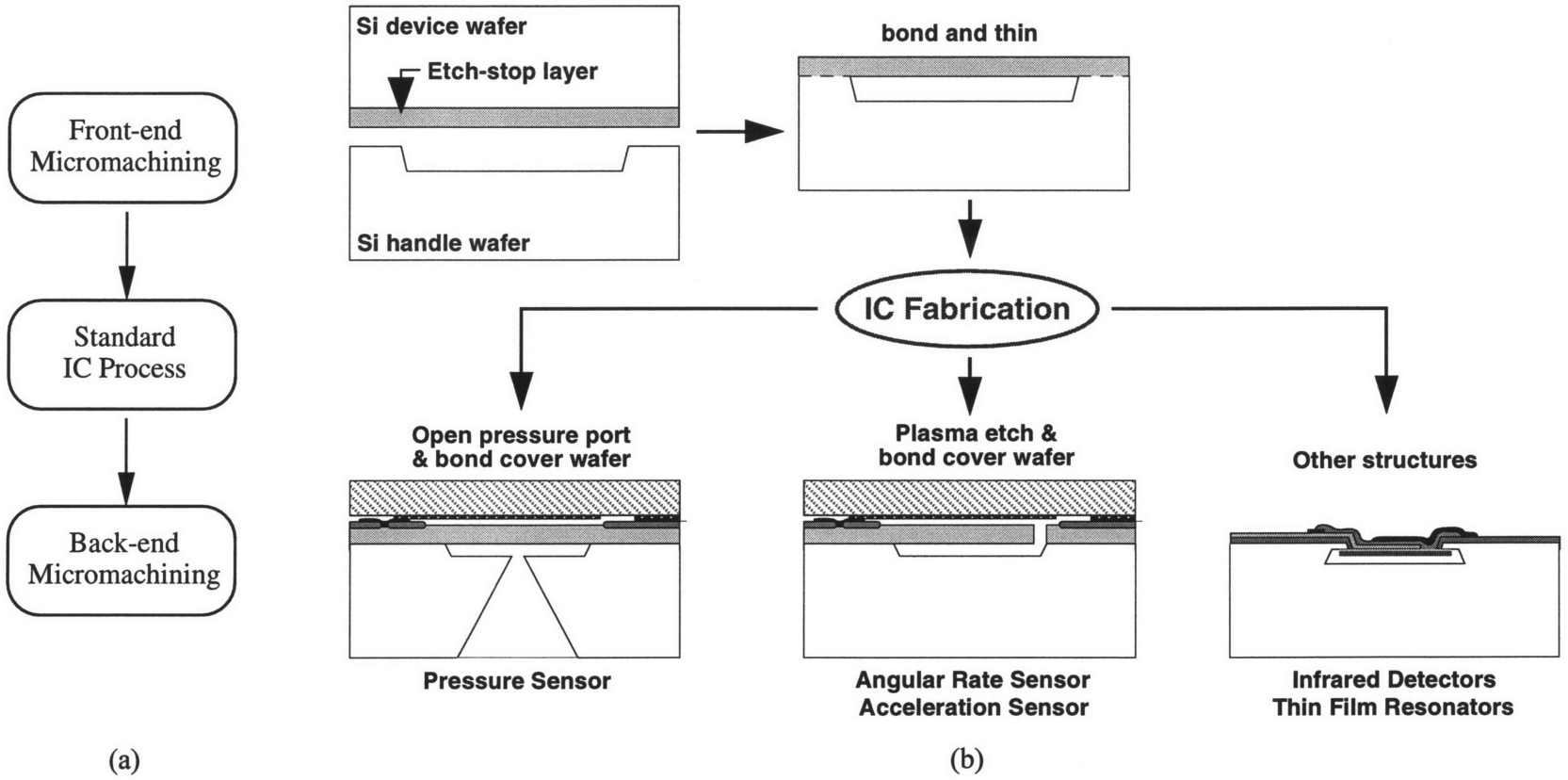


Figure 1–6: (a) Partitioning of process and (b) generalized sealed cavity approach.

micromachining processing steps should be implemented prior to the start of the circuit fabrication or after the complete circuit fabrication.

In light of the previous discussion regarding the importance of process partitioning, an integrated sensor fabrication process as illustrated in Figure 1–6 is proposed for this research work. This general process partitioning scheme was described by Petersen [23] and Senturia [24–25] in the early 80's. This version of the integrated sensor fabrication process consists of some front-end micromachining performed prior to the wafer entering the IC fab. It is of most importance that wafers entering the IC fabrication facility do not require customized handling or processing. Following the IC fabrication, the wafer returns to a micromachining facility to complete the process.

We will be using a silicon wafer bonding and etching technology to achieve this process partitioning. This process technology is a derivative of the silicon fusing bonding technology used in various research and industrial laboratories in the early 1990's [26–27]. Figure 1–6(b) illustrates the general flow of this process. The following technology strategy is employed to fully appreciate the benefits of integrated sensors. This wafer-bonded integrated sensor technology uses existing IC facilities and processes; it integrates package function at the wafer level; it partitions the fabrication processes so that the micromachining processes and electronics processes do not interfere; it uses materials and processes with reproducible and transferable properties. As a result, a large class of sensors and actuators can then be built upon this technology (i.e., pressure sensors, accelerometers, flow sensors, angular-rate sensors, and IR detectors).

As for the general process flow, we begin by joining two silicon wafers, a device wafer containing an etchstop layer and a handle wafer containing etched cavities, using wafer bonding. The bulk of the device wafer is then thinned to produce a wafer with sealed cavities which resembles an unprocessed wafer with the exception of the cavity dimples caused by the reduced pressure in the cavity. At this point the bonded and thinned structure can be returned to a standard IC facility for electronics fabrication. Following circuit processing, low-temperature back-end processes are performed to

functionalize the sensors. The process has two significant features. First, the mechanical layer which results from this process has reliable, reproducible mechanical properties [28] since it is basically a single-crystal silicon layer. Second, the electronics integration strategy is compatible with standard IC processes and equipment. Two major front-end technology issues in using wafer bonding for the fabrication of sensors and actuators, wafer thinning processes, and the control of the residual pressure in cavities formed by bonding and etchback, have been discussed in detail previously [29–30]. The back-end processes entail etching of the mechanical layer for accelerometers or etching of a pressure inlet port for the pressure sensor, followed by the low-temperature bonding of a capping wafer.

The integrated sensor process proposed in this thesis provides a very effective isolation of the sensor and the circuit processing. The wafer which enters the IC fabrication facility looks very much like a standard silicon wafer (except for the cavity dimples as previously described), and it contains no materials which would be affected by subsequent high temperature processing. Thus, it can be processed through a standard IC fabrication line without any perturbation of the processing steps or the equipment. The wafer is then customized to complete the mechanical sensors or/and actuators once it exits the IC fab. If the processing temperatures of the back-end micromachining can be limited, then the final mechanical fabrication and packaging should not affect the IC circuitry. Before we proceed to describe the microaccelerometers that we will fabricate using the wafer-bonded integrated sensor technology, a brief introduction of the silicon microaccelerometer is presented in the following section.

1.2 Silicon Microaccelerometers

An accelerometer is a sensor for measuring static and time-varying accelerations and has many applications in various industries; from inertial navigation to shock measurement and from robotics control to vibration measurement [11, 31–41]. The technologies for macro-scale accelerometers are well understood, and the macro-scale accelerometers are often incorporated into systems used for measurement, monitoring, and control in many industries. With airbags in a large number of cars manufactured today, there is a growing demand for low cost accelerometers for use as collision detectors. By placing several acceleration sensors in different locations throughout a vehicle, a microprocessor can determine when a collision has occurred and whether or not to deploy the airbags. Threshold deceleration for airbag deployment ranges from 20g to 50g (medium g range), depending on the vehicles [33–34]. In addition to collision detection, accelerometers can also be used in antilock braking systems (ABS), four-wheel steering (4WS) systems, and active suspension (AS) systems [33–34]. Aside from collision detection, most acceleration sensor applications in automobiles require an input range of ±2g (low g range) and a bandwidth of 50Hz [34]. Other non-automotive related applications for accelerometers include industrial, railway, medical, and inertial guidance (spacecraft) applications [34, 37–40, 42–44]. It is not difficult to see why there has been an intense interest, particularly in the automotive industry, in the production of small, robust, low-cost (e.g., $5.00 or less per accelerometer), reliable, low to medium g range (e.g., input range of 1–50 g), and medium to high resolution (e.g., *automotive grade* accuracy of 2–5% and *instrument grade* accuracy of less than 1%) silicon accelerometers in high volume over the past few years.

Since microaccelerometers are based on integrated circuit technology, they can be manufactured in large quantities and at potentially lower cost compared to their bulkier counterparts. In addition, microaccelerometers are much smaller and lighter than their

macro-scale counterparts. Microaccelerometers will have many new industrial and commercial applications where size, weight, or cost is critical. However, realization of low-cost and reliable accelerometers, even in the low-to-moderate performance range (i.e., medium accuracy of 2–5% and medium input range of 10–50 g) has proven challenging [11, 31–33]. Among the many obstacles are design of squeeze-film damper, over-acceleration and shock stops, temperature compensation, and decoupling of the device from packaging-induced stresses. Sophisticated mechanical modeling and, in some cases, development of new fabrication techniques are required to overcome these obstacles. Another important advantage silicon microaccelerometers have over the conventional accelerometers is that there is the potential of integrating signal conditioning circuitry onto the same substrate as the sensor itself to produce *integrated* or *smart* sensors which can be interfaced directly with a microprocessor.

1.2.1 Performance Criteria

There are a number of performance criteria or characteristics by which all accelerometers are compared or specified. These different criteria must be examined and addressed in the process of designing a silicon microaccelerometer.

Input Range

The measured values over which one would like a sensor to measure is commonly referred to as the *input range.* Accelerometers are used for a variety of different applications and therefore, specifying the input range is an important consideration in the design process. An accelerometer's measurement range is often broken down into three general categories, usually given in terms of g's (1g = 9.8m/sec^2); low g: (0–10g); medium g: (10–100g); and

high g: (> 100g). It is the goal of this thesis to implement low g and medium g microaccelerometers, both in discrete and hybrid forms, using the same wafer-bonded sealed cavity process.

Sensitivity

Sensitivity is defined as the ratio of the change in the sensor's output per unit change in input acceleration (e.g., 100mV/10g's). An accelerometer's sensitivity is perhaps one of the most important performance characteristics that one specifies in a design. Sensitivity is usually defined at a specific excitation frequency (e.g., 100Hz). Depending on the output of the detection scheme used, sensitivity is specified in mV/g•V_{supply}, mV/g, fF/g, pC/g, or, Hz/g.

Frequency Response (Bandwidth)

A sensor's frequency response is defined as the change with frequency of the output/measurand amplitude ratio (and of the phase difference between output and measurand) for a sinusoidally varying measurand applied to the sensor within a stated range of measurand frequencies. In more basic terms, a sensor's bandwidth is the frequency range over which the response of the sensor can continue to follow any changes in the input to the sensor. An accelerometer's frequency response is a function of the mechanical resonance and damping coefficient of the sensor. Frequency response or bandwidth is usually specified as being within a certain percent (e.g., ±5%) over a fixed frequency range (e.g., 10Hz to 1kHz), and is referred to a measurement at a specific frequency (reference frequency) at a specific amplitude (reference amplitude).

Linearity

In order for a sensor to be most useful, it should exhibit a well behaved output versus measurand relationship (e.g., 100mV/10g, 200mV/20g, etc.). Generally, a linear change in sensor output for a linear change in measurand is highly desirable. This is because such a

relationship, in general, facilitates data reduction. The closeness in match between a sensor's calibration curve and a specified straight line is commonly termed linearity. Linearity (or occasionally referred to as *nonlinearity)* is frequently specified in terms of the maximum deviation (usually given in %FSO (full-scale output)) between any point on the actual calibration curve, and the specified "best-fit" line.

Details about other important performance criteria such as cross-axis sensitivity, over-acceleration and shock resistance, packaging and temperature effects, and stability and drift can be found in [31] and are not repeated here.

1.2.2 Performance and Structure Design Goals

Performance Goals

Though the fabricated microaccelerometers shown in this thesis are only intended as a demonstration vehicle for the successful implementation of the MEMS-CMOS integrated sensor technology based on the wafer-bonded sealed cavity process, understanding their performance goals is important for designing the appropriate microstructure and deciding on the related detection scheme.

The main performance design goals for an accelerometer are to maximize sensitivity, bandwidth, input range, and shock resistance, while at the same time minimizing undesirable (or second order) effects such as cross-axis sensitivity, temperature sensitivity, and drift. However, a tradeoff is often made in order to optimize the characteristics of the accelerometer for the particular intended application. For example, airbag crash sensors are typically specified to work over the ±50g range, while ride

control sensors are specified to work only over the ±5g range but with a much greater demand in device sensitivity and resolution.

Thin-film (surface-micromachining-like) microstructures are felt to have a number of advantages which lend themselves to better performance characteristics than would be obtainable in a bulk micromachined design. A thin-film accelerometer's co-planar design means less susceptibility to cross-axis sensitivity and failure due to shock in the cross-axis. However, thin-film accelerometers also have much smaller proof masses, making the induced stresses in the supporting tethers perhaps too small for piezoresistive detection to be practically used. On the other hand, displacement of the proof mass can still be made "large", so, for these microstructures, capacitive detection is considered to be the simplest and most effective detection scheme. In addition, capacitive detection offers superior temperature performance compared to piezoresistive designs. With a nominal sense capacitance of 2-5 pF, 0.5-1.0% resolution was considered achievable, even with off-chip circuitry. Although the frequency response of a crash sensor only has to be about 500Hz, a frequency bandwidth of 3kHz was chosen as a design target. As mention earlier, an accelerometer may be exposed to large extremes in temperature, so it must have a very small temperature sensitivity. Most silicon microaccelerometers designed today employ electrostatic bonding of the silicon structure to Pyrex #7740 glass as part of their sensor packaging. The mismatch in thermal coefficients of expansion between these two materials invariably becomes a source of temperature-induced stresses and long-term drift, even at room temperature. In order to avoid this problem, a goal toward an all-silicon design was taken. To address the issue of long-term stability (reliability), silicon wafer bonding and several etchstop techniques were chosen as the fabrication technologies to implement this structure because they offer the chance to produce the accelerometer entirely from moderately-doped, single-crystal silicon. This would avoid any of the potential drift problems that might occur from fabricating the accelerometer from polysilicon or p^{++}-doped silicon.

Accelerometer Structure

A simple schematic of the proposed accelerometer structure is shown in Figure 1–7. It is a symmetrical, 4-tether design with a square proof mass in the center and a surrounding frame. The primary sensing axis is in the z-direction, perpendicular to the substrate. A 4-tether design was chosen because it offers greater improved cross-axis stiffness and reduces cross-axis sensitivity. Although the inherent co-planarity of surface-micromachining-like structures is in many ways a benefit over bulk micromachined designs, the loss in total volume of the accelerometer structure greatly reduces the inertia of the accelerometer's proof mass. Consequently, the supporting tethers have to be made much softer in order to achieve comparable sensitivities. To reduce tether stiffness without significantly increasing their length, a design with *folded* tethers was pursued. Most bulk micromachined accelerometers have die sizes on the order of 3-5 mm on each side. In order to maintain the benefit of batch fabrication, a thin-film microaccelerometer's overall die size was kept under 4mm on each side. In Figure 1–7, one can see the gap between the proof mass and the bottom electrode. The gap serves as part of the sensing capacitance, but it is also critical to determining the damping, and hence the bandwidth, of the accelerometer.

The global theme of the design of the fabrication process was to create a fabrication sequence which could eventually be implemented in an actual production environment (i.e., avoid exotic, or overly customized, solutions). To meet the requirements for an inexpensive, high-yield batch fabrication process, it was felt that the design of the accelerometer should avoid using a fabrication process with a requirement for *aligned bonding* of two micromachined substrates. The electrochemical etchstop was chosen as a key technology in the creation of the structure. Details of the microaccelerometer fabrication process are given in Chapter 4, and its central element is the sealed cavity with a suspended single-crystal silicon plate which will be used to make the sensor/actuator element. The cavity has been designed to be robust enough to

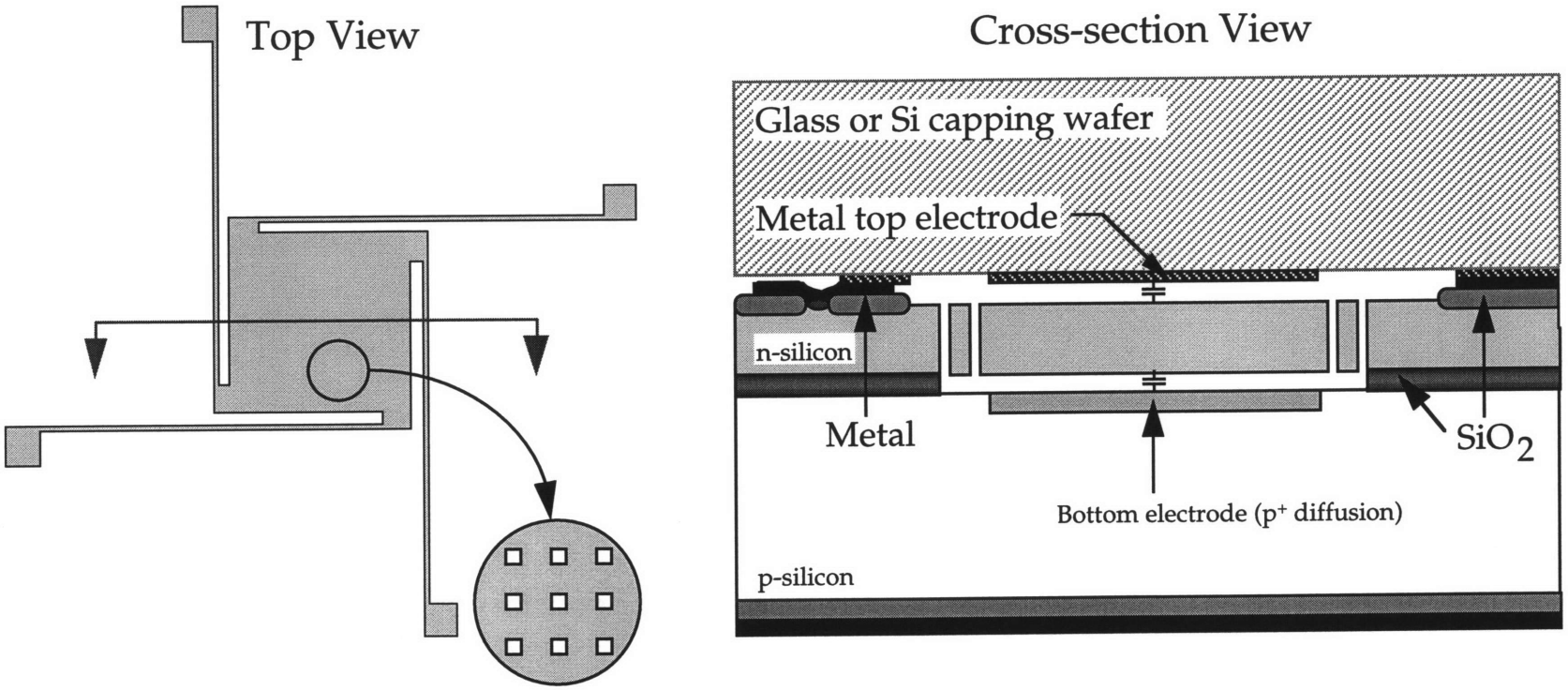


Figure 1–7: Schematic of proposed wafer-bonded sealed cavity silicon microaccelerometer.

withstand conventional circuit fabrication, and the process is versatile enough to be used to make a wide variety of devices as illustrated in Figure 1–6(b) previously.

Signal Detection: Hybrid vs. Integrated

One of the primary obstacles which has prevented capacitive detection schemes from achieving their expected superior performance compared to piezoresistive detection schemes has been the limitations in implementing capacitive detection circuitry which could detect the small variations in a sensor's sense capacitance in the presence of large parasitic capacitance. An obvious solution to this problem is to move toward a fully integrated sensor design, hence eliminating the parasitics. Another benefit of the proposed accelerometer approach is its amenability toward integration. However, a hybrid (two-chip) approach offers a reasonable compromise for a first generation implementation, because it allows both sensor and circuit designers to work on two major pieces of the puzzle independently while maintaining a sense of "connection" through the hybrid approach. It also give the flexibility to explore both analog and digital feedback control schemes, without requiring a major change in sensor structure [45]. In addition, this hybrid approach was viewed to have a greater chance to succeed due to the time-constraints we had when the project began in late 1994. In this thesis, an off-chip detection circuit is built to demonstrate the functionality (specifically the frequency response) of the accelerometer. In addition, a custom-designed VLSI chip was fabricated by M. Ashburn for the two-chip-version accelerometer testing [45].

1.3 Thesis Outline

The organization of this thesis is a follows; Chapter 1 provided an overview of current integrated sensor processes, an introduction of the integrated MEMS-CMOS process utilizing silicon wafer bonding that is a primary focus of this thesis, a review of the current state of work on silicon microaccelerometers and a discussion of issues pertinent to the design and fabrication of accelerometers. Chapter 2 deals with the mechanical analysis and specifications for the design of the accelerometer structures. It focuses specifically on the issue of tether design and the problem of squeeze-film damping as it affects the performance of the surface-micromachining-like accelerometers. This chapter will draw heavily on previous analyses carried out in the research group during the course of this thesis [31–32]. Chapter 3 starts off with the process overview of the proposed integrated MEMS-CMOS process. The main focus of this chapter is the necessary process enhancements developed to successfully fabricate test structures; M-Test, lateral resonator, and diode structures. Chapter 4 discusses the overall fabrication process sequence created in order to fabricate the accelerometers (both for discrete and for hybrid-version). In this chapter, mask design and the layout of the structure will be presented, as well as some of the unusual phenomena encountered during the development of this process. Chapter 5 is the device testing chapter and the results of static and dynamic testing of the accelerometers and other test structures will be discussed. Finally, Chapter 6 contains some overall discussion, conclusions, and suggestions on the future work.

Chapter 2

Mechanical Sensor Design and Analysis

2.1 Overview

A MEMS sensor designer must be able to understand and predict the electromechanical behavior of the sensor structure in order to design and satisfy the set performance goals for the particular sensor s/he is working on. Closed-form analytical expressions, based on well-known mechanical theories, numerical analysis, finite element modeling (FEM), and finite element analysis (FEA) can help designers to understand, design, and characterize the static and dynamic characteristics of the micromechanical structures. In this chapter, analytical calculations and FEM/FEA are used to model and predict the behavior of our *"surface-micromachining-like"* structures. During the course of this research work, MATLAB [46] and MEMCAD [47] analytical tools have been used extensively to model

and predict the behavior of numerous micromachined devices/sensors. In particular, a comb-drive based lateral resonator (tuning fork gyroscope), a micromachined acceleration sensor (microaccelerometer), and three MEMS drop-in test structures (so-called "M-Test" structures) [48] have been carefully examined; however, the following sections only highlight the important results of the analytical and finite element modeling for the microaccelerometer. More in-depth details of the derivation of these results can be found in [31–32]. The extensive modeling work of Novack and McNeil was drawn upon during the design phase of this thesis [31–32]. Details of the analytical and simulation results for the comb-drive based lateral resonator and M-Test structures are presented in Chapter 3.

2.2 Simple Analytical Models

The structure of the micromechanical accelerometer can be characterized by an inertial mass, a spring, and viscous damping as shown in Figure 2–1. This simplified model assumes single-degree-of-freedom operation. The spring models the restoring force provided by the four silicon tethers attached to the proof mass while the damper models

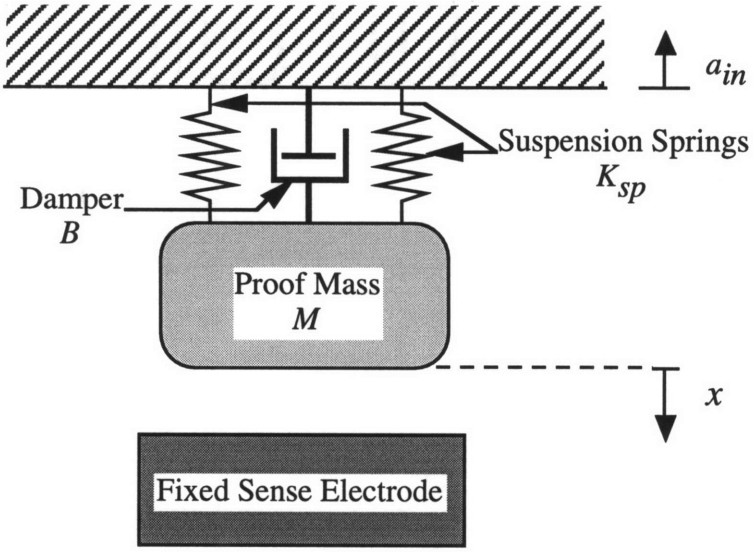


Figure 2–1: Basic mechanical system model.

viscous damping from gas (air) surrounding the proof mass. Summing the forces acting on the inertial mass, a relation between input force and displacement can be derived.

$$F_{ACC} = M\ddot{x} + B(x)\dot{x} + K_{sp}(x)x \tag{2.1}$$

where $F_{ACC} = Ma_{in}$. $B(x)$ and $K_{sp}(x)$ represent the viscous damping and spring coefficients, respectively, both of which are nonlinear functions of proof mass deflection. The damping coefficient $B(x)$ can usually be approximated to be a constant, B_0, since the maximum deflection of the proof mass, x_{max}, is usually kept below 10% of the gap spacing, d. The first order gas damping term, B_0, between two square plates can be calculated analytically using [32]

$$B_0 = 0.4217\frac{\mu L^4}{d^3} \tag{2.2}$$

where μ is the viscosity of the gas (air) surrounding the plates, L is the plate length, and d is the gap separation. The spring coefficient $K_{sp}(x)$ varies only slightly as a function of x (less than 50ppm nonlinearity [32]) and for now will be modeled as a constant, K_{sp}.

The displacement of the proof mass is sensed via the variable capacitance formed between the inertial mass and fixed electrodes. The capacitance sensor can be implemented by either sensing differentially between the upper and lower variable capacitors or by sensing differentially between the variable sense capacitors (from the sense accelerometer) and fixed reference capacitors (from the reference accelerometer). The reference capacitors are formed by fabricating a structure identical to that of the mechanical system except using very short silicon anchors instead of flexible silicon tethers like the mechanical system. The short silicon anchors hold a reference mass immobile thus producing a fixed capacitance. Since the sense and reference accelerometers are fabricated side-by-side and identically, the capacitance values should match well even with process variation.

The specific accelerometers that we have studied are shown in Figure 2–2 in their 3-D form. In both designs, the proof mass is a square plate, and the springs are the four tethers supporting the proof mass. The proof mass is suspended over the substrate (of the handle wafer) and below the capping wafer, and moves relative to both the handle wafer and the capping wafer when accelerated. This produces changes in capacitances between the proof mass and the handle wafer (bottom electrode) and between the proof mass and the capping wafer (top electrode). The capacitance changes result in the measurement of the acceleration via either the *off-chip* PC board-based capacitance detection circuit (open loop system) or the *hybrid-version* IC chip designed by Ashburn (closed loop system) [45].

Equation 2.1 can be solved to find the static and dynamic behavior of the system. The static analysis presented in the next section is used to look at the sensitivity of the system.

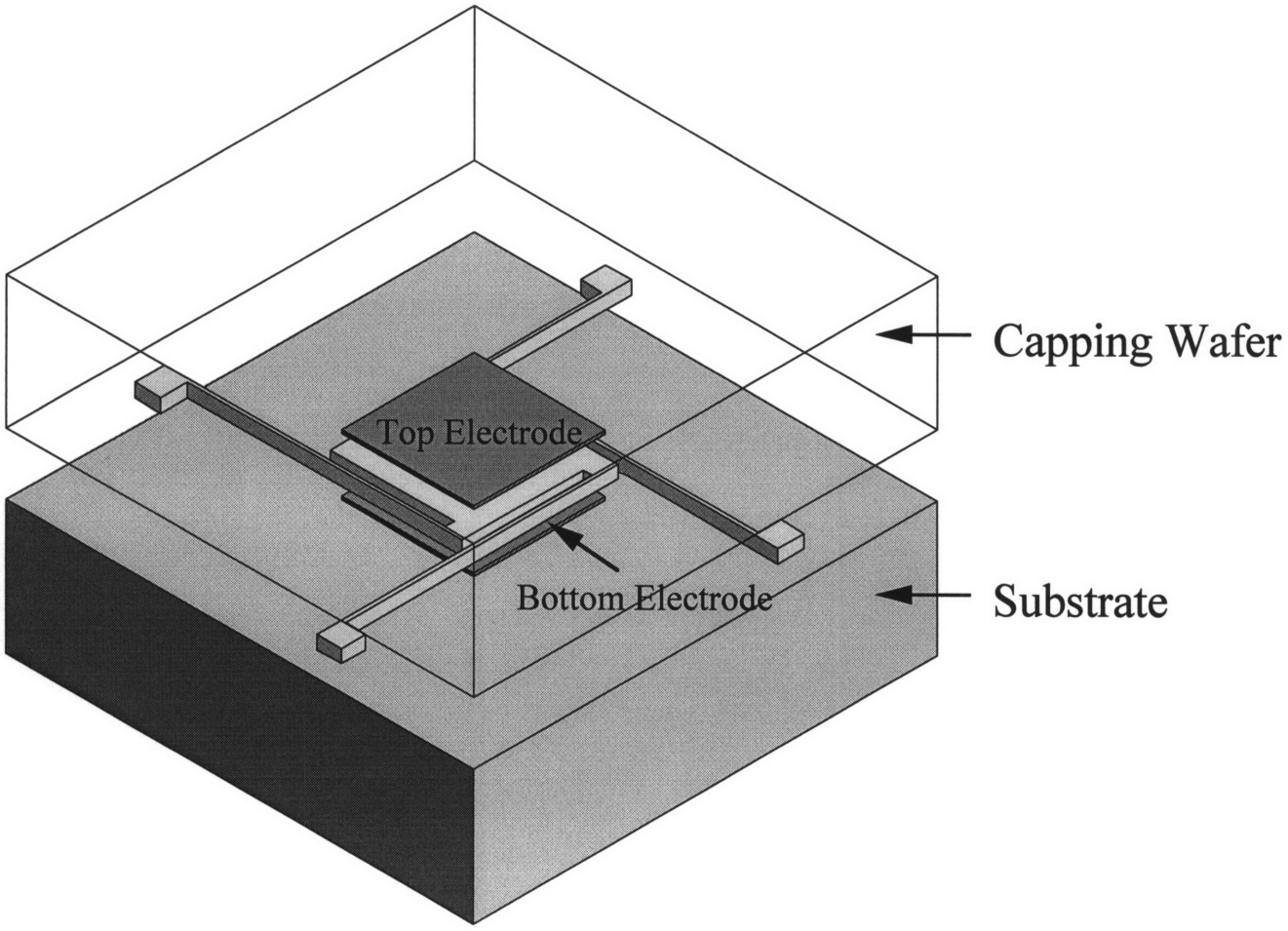


Figure 2–2(a): A *simple* pinwheel microaccelerometer in its 3-D form.

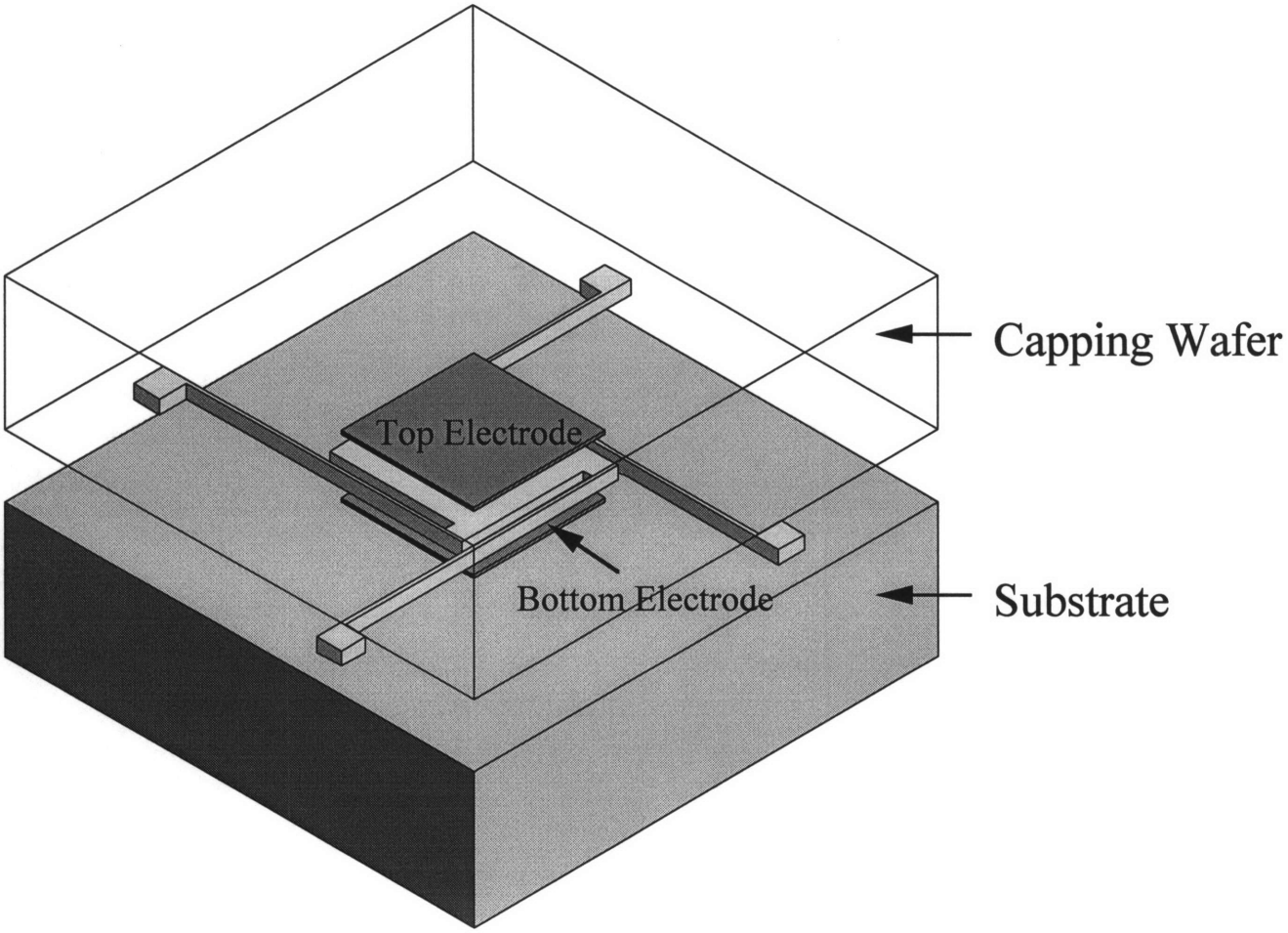


Figure 2–2(a): A *simple* pinwheel microaccelerometer in its 3-D form.

2.2.1 Accelerometer Scaling – Static Sensitivity *vs.* Dynamic Range

The static displacement of the proof mass from its equilibrium position can be intuitively stated below by observing that Newton's first and second laws must be satisfied:

$$F_{ACC} + F_{spring} = 0 \tag{2.3}$$

$$F_{ACC} = MA_0 \quad \text{and} \quad F_{spring} = -K_{sp}X_0 \tag{2.4}$$

$$\Rightarrow \quad \frac{M}{X_0} = \frac{K_{sp}}{A_0} \tag{2.5}$$

where X_0 is the static displacement and A_0 is the magnitude of the input acceleration. The sensitivity of an accelerometer can be defined as the amount of the proof mass displacement per unit input acceleration:

$$S \equiv \frac{X_0}{A_0} \tag{2.6}$$

From Equation 2.6, one can see that the overall sensitivity of an accelerometer can be specified by the appropriate scaling of the proof mass and the spring constant of the system. Solving the differential equation used to describe the spring–damper–mass system (and assuming zero damping), the undamped natural frequency of the system can be found to be

$$\omega_n = \sqrt{\frac{K_{sp}}{M}} \tag{2.7}$$

$$f_n = \frac{1}{2\pi}\omega_n \tag{2.8}$$

The undamped resonant frequency, ω_n, is the frequency at which the first mechanical resonance of the system occurs, thus, specifies the maximum usable frequency

(bandwidth) for the accelerometer. The bandwidth can be increased simply by increasing K_{sp} or/and decreasing M. However, an accelerometer's sensitivity and bandwidth are coupled, and cannot be optimized independently:

$$S\omega_n^2 = 1 \tag{2.9}$$

Therefore, there is always a tradeoff between sensitivity and bandwidth in determining the performance characteristics of an accelerometer.

2.2.2 Dynamic Behavior

The dynamic response of the accelerometer can be best described in more detail by looking at the full frequency response of the system. First we assume that the spring–damper–mass system is excited by a periodic input acceleration of the form $A_i = A_0 \sin\omega t$, then the system responds with the sinusoidal displacement of the proof mass whose equation of motion is of the form $x = X_0 \sin(\omega t + \theta)$. Equation 2.7 can be solved to give the amplitude response of the displacement of the proof mass as a function of excitation frequency ($M(\omega)$) and its phase relationship with respect to the drive frequency ($\theta(\omega)$) as shown below:

$$M(\omega) = \frac{K_{sp}}{M}\left|\frac{X_0}{A_0}\right| \frac{1}{\sqrt{\left(1-\frac{\omega^2}{\omega_n^2}\right)^2 + \left(2\zeta\frac{\omega}{\omega_n}\right)^2}} \tag{2.10}$$

$$\theta(\omega) = -\tan^{-1}\left(\frac{2\zeta\frac{\omega}{\omega_n}}{1-\frac{\omega^2}{\omega_n^2}}\right) \tag{2.11}$$

$$\omega_n = \sqrt{\frac{K_{sp}}{M}}$$

$$\zeta \equiv \text{damping ratio} = \frac{B}{2\sqrt{K_{sp}M}} = \frac{B/M}{2\omega_n} \tag{2.12}$$

When the damping ratio $\zeta = 1/\sqrt{2}$, *critical damping* has been achieved and $B = 2\sqrt{K_{sp}M} = B_{cr}$. On the other hand, from a design standpoint, the accelerometer can best be thought of as a low pass filter [45]. Modeling Equation 2.1 in the frequency domain, approximating $B(x)$ as a constant:

$$\frac{X(s)}{F(s)} = \frac{1}{Ms^2 + Bs + K_{sp}} = \left(\frac{1}{M}\right)\frac{1}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{2.13}$$

where ω_n is the undamped natural frequency of the system.

Examining Equation 2.13, the response of the accelerometer (mechanical system) has two poles which "roll off" the mechanical response above ω_n at a rate of 40dB/decade. The placement of ω_n, critical in the design of the accelerometer, is set by the spring constant, K_{sp}, and mass, M, of the spring–damper–mass system.

The mass, M, can be calculated from the volume of the proof mass and density of silicon (2.33 g/cm^3) with some error resulting from the nonzero mass of the springs. The spring constant, K_{sp}, is set by the length and shape of the silicon tethers. Qualitatively, the predominant mechanism for controlling the spring constant is by varying the dimensions of the two long thin sections of silicon in each tether (Figure 2–3(b), sections 1 & 2, assuming folded pinwheel design). Tether sections 3, 4, and 5 also contribute to the

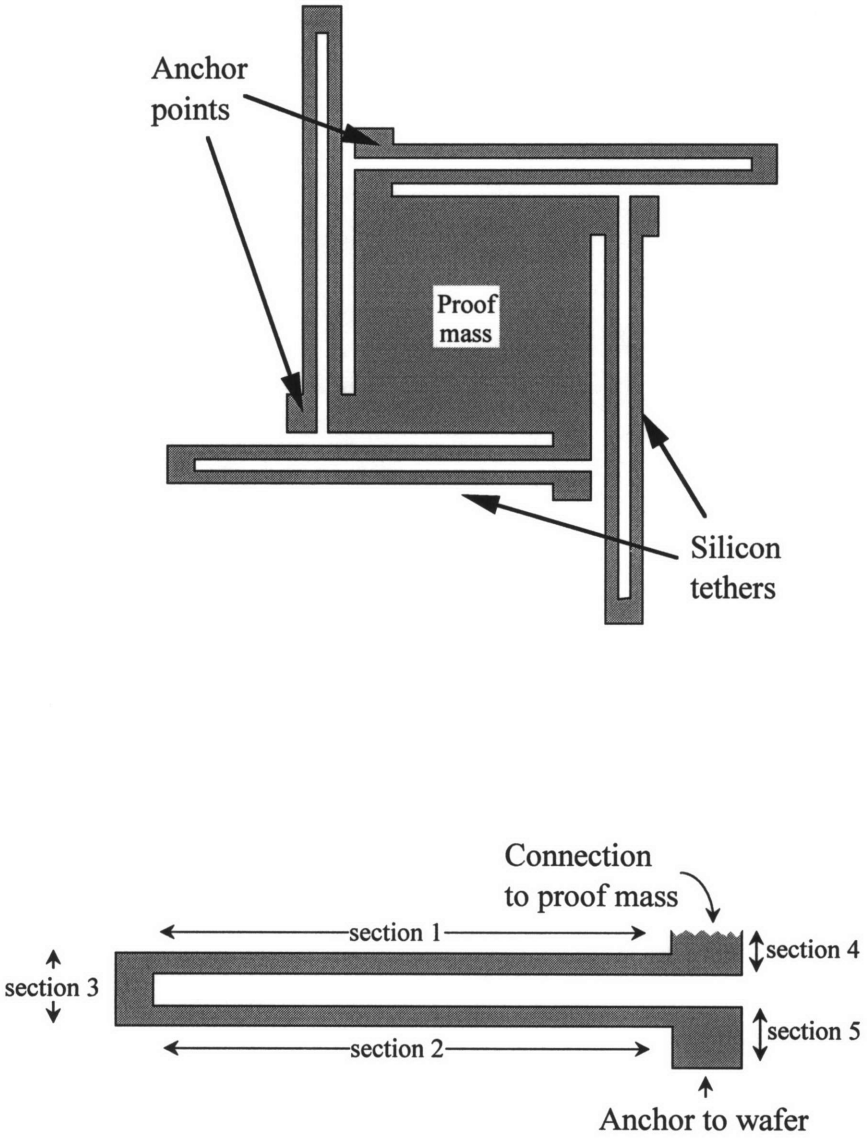


Figure 2–3: (a) Top view of a folded pinwheel microaccelerometer. (b) Detailed view of the folded beam sections.

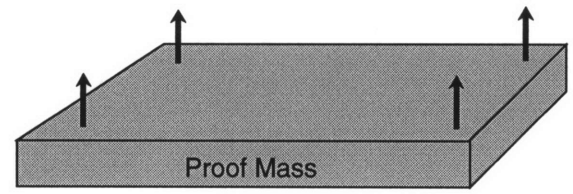
effective spring constant, however, they are all relatively "stiff" with respect to the long sections of tether. The spring constant for a single section of tether is given by [32]:

$$K_{eff} = \frac{4Ebt^3}{l^3} \tag{2.14}$$

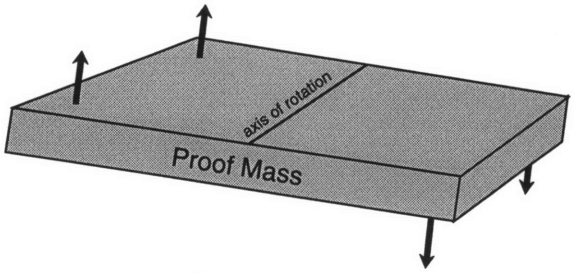
where E is the modulus of elasticity, b is tether width, t is tether thickness, and l is the section length. Though it is a huge oversimplification to calculate the folded pinwheel tether spring constant as just two straight tethers in series, Equation 2.14 lends qualitative information which justifies the shape of the silicon tethers. To decrease the spring constant, K_{sp}, both the tether width (b) and thickness (t) should be increased while the tether length (l) should be increased. Likewise, to increase the spring constant, increase both b and t and decrease l.

In the actual design of the mechanical sensor, FEM analysis was used to predict the resonant frequency of the mechanical structure. The measured resonant frequencies of the mechanical sensor displayed matching to within 2% of the FEM calculated values.

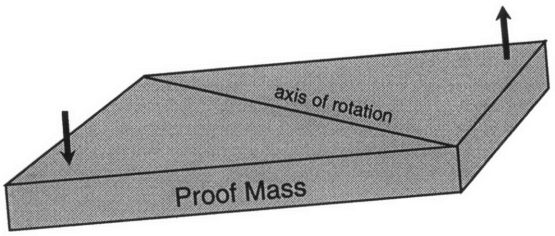
To this point, the discussion of dynamics has been limited to the fundamental resonance of the mechanical system. Equation 2.13, used to model the second order response of the sensor, models only single degree of freedom movement (up-and-down motion illustrated in Figure 2–4(a)). In actuality, the proof mass has several secondary resonances which include responses to torque and lateral acceleration [31–33, 49]. The lateral resonance modes are at very high frequencies and can be ignored for all practical purposes in the system design. The torsion mode resonances are at lower frequencies which can affect the performance of the accelerometer (illustrated in Figure 2–4(b) and (c)). The possible effects of these resonances on system performance are discussed in section 3.6 of Ashburn's thesis [45] and will not be repeated here.



a) Resonance Mode 1



b) Resonance Mode 2



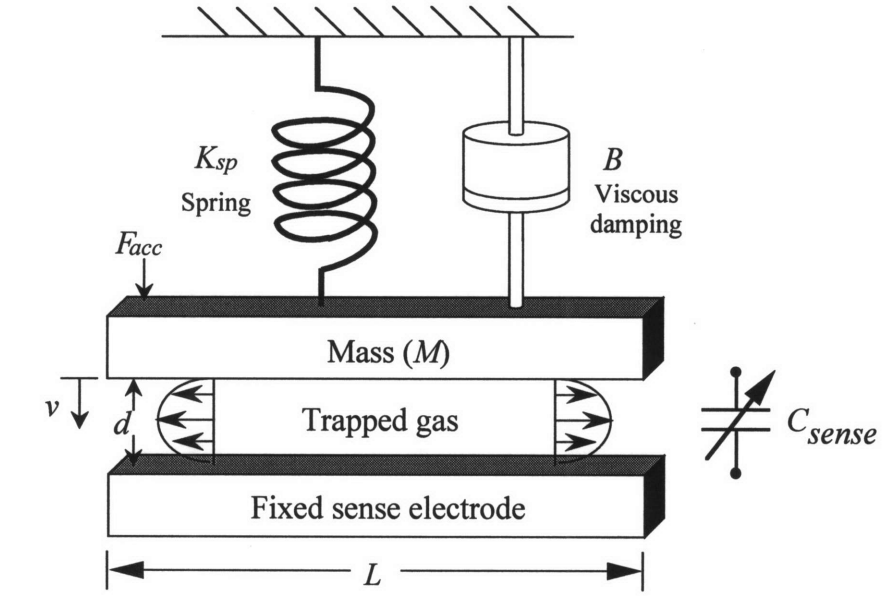
c) Resonance Mode 3

Figure 2–4: Microaccelerometer resonance modes.

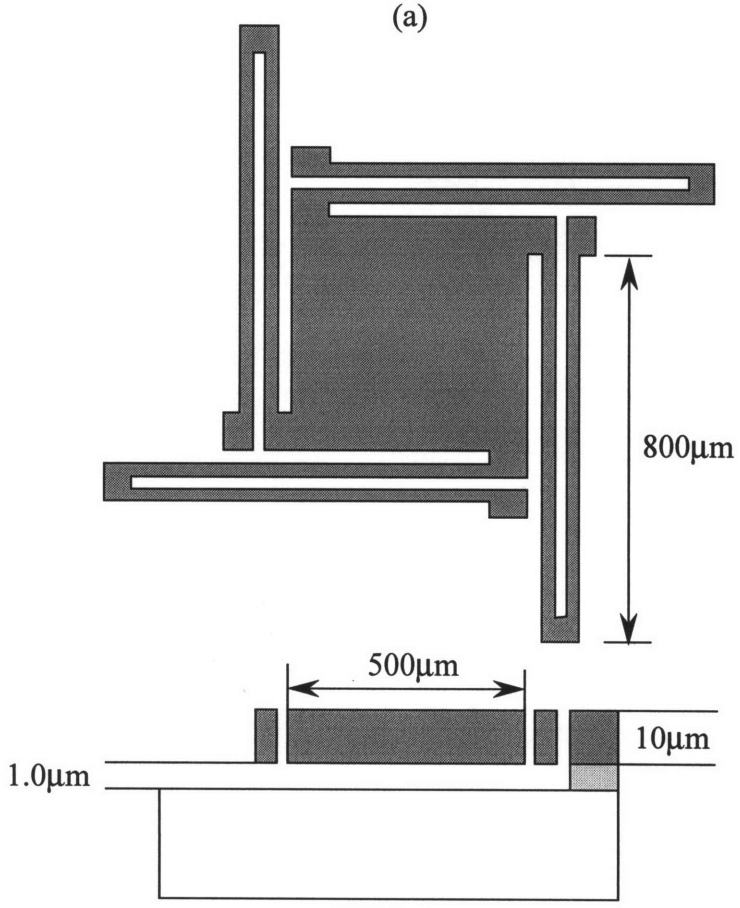
2.3 Dynamic Response and Squeeze-Film Damping

The dominant damping force most often encountered in the silicon micromechanical devices is the viscous damping phenomena known as *squeeze-film damping*. Squeeze damping forces are generated when two solid, flat surfaces are brought together, and the viscous fluid between them is forced or squeezed in and out. Squeeze-film damping is of particular concern for our accelerometers which use capacitive-sense and electrostatic drive because large sensing/feedback electrode areas and small proof mass-to-electrode gaps are required to obtain necessary sensing capacitance for the pick-up circuit and/or large enough electrostatic actuation forces. This section explains briefly how to calculate, and how to (possibly) control the squeeze-film damping. Furthermore, we will focus on *minimizing damping* while *maximizing detection capacitance* used in the perforated proof mass design.

Figure 2–5(a) illustrates the effects of squeeze film damping on a microaccelerometer structure while Figure 2–5(b) illustrates the schematics of a typical microaccelerometer structure. Equations 2.10, 2.11, and 2.12 describe the magnitude, phase, and damping relationships of the response of the accelerometer system to a periodic input signal. In order to obtain the best overall response characteristics for our accelerometer designs, the damping ratio ζ should be kept close to 0.707. Since ω_n is fixed primarily by bandwidth and sensitivity requirements, ζ can be modified by varying the ratio of *B/M*. For a square plate, the damping coefficient *B* is expressed in Equation 2.2, and the ratio *B/M* can be expressed as



(a)



(b)

Figure 2–5: (a) Schematic showing viscous damping due to the squeeze film damping effect. Proof mass M, of side length L, move toward bottom-electrode with velocity v. The gap height between the proof mass and the bottom-electrode is d. (b) Schematic of a typical micro-accelerometer.

$$M = L^2 T \rho_{Si}$$

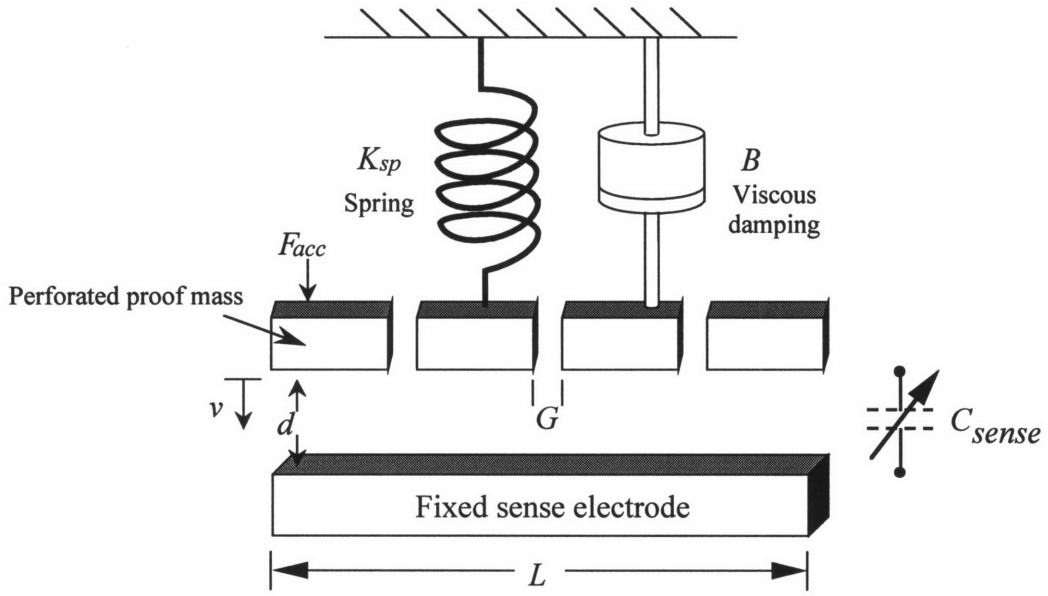
$$B/M = \frac{(0.4217)\mu}{T\rho_{Si}} \frac{L^2}{d^3} \tag{2.15}$$

where M is the inertial mass of the proof mass, T is the thickness of the proof mass, and ρ_{Si} is the density of silicon. As shown in Equation 2.15, it is clear that we can modify B/M using a variety of approaches. However, the ratio B/M can be most strongly influenced by modifying the proof mass length L and the gap height d. Decreases in L or/and increases in d would decrease the ratio B/M but at the same time decrease the nominal sense capacitance C_0. Furthermore, increases in d is bounded by the physical limits of the fabrication process.

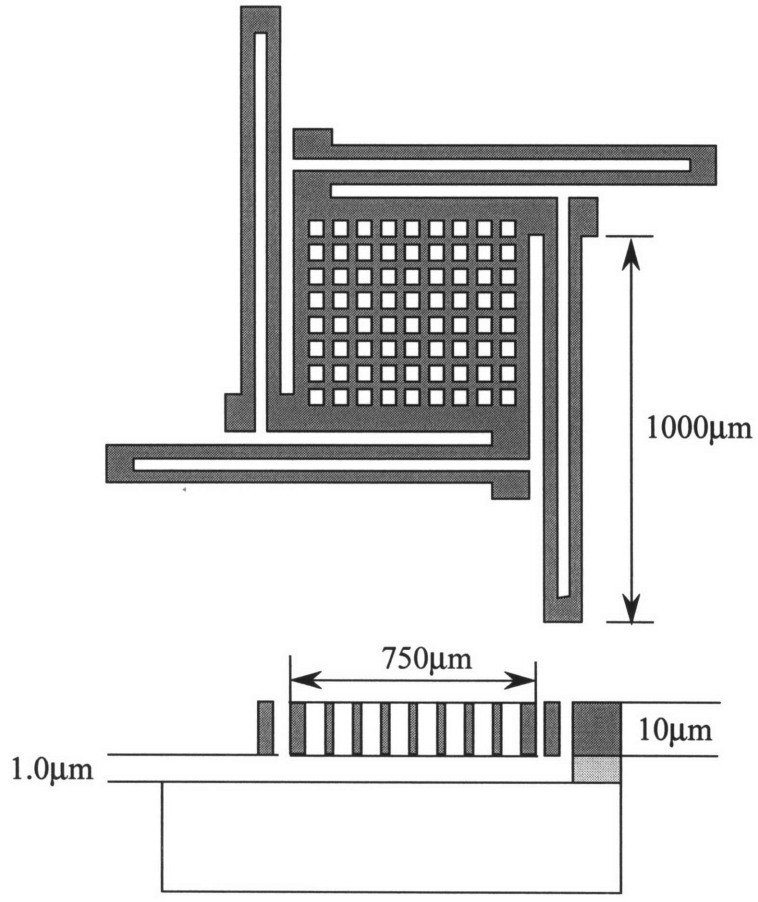
As proposed by Novack *et al.*, the key to solving the viscous damping problem was to reduce the proof mass length L, over which the viscous fluid had to travel to equalize pressure differences, while at the same time maintaining enough area to obtain a reasonably large sense capacitance. This problem was solved by using a *perforated* proof mass shown in Figure 2–6. Novack's results are summarized in the following: for analytical calculations, the perforated proof mass structure was approximated as an ensemble of small square plates working independently of each other. The equations for N such small square plates are:

$$C = N\left(\varepsilon_0 \frac{(L')^2}{d}\right) \tag{2.16}$$

$$\begin{aligned} B/M &= \frac{N(0.4217)\mu}{NT\rho_{Si}} \frac{(L')^2}{d^3} \\ &= \frac{0.4217\mu(L')^2}{T\rho_{Si}d^3} \end{aligned} \tag{2.17}$$



(a)



(b)

Figure 2–6: Schematic of accelerometer with a perforated proof mass used to achieve critical damping.

where L' (the distance between perforations) is the new distance over which a viscous fluid must travel to equalize its pressure. In order to increase the sense capacitance, we increase N, yet the ratio B/M stays the same. Thus, by designing one small square plate with the appropriate value of B/M, we can then multiply by the appropriate number N to get a sufficient large sense capacitance for our detection circuit. ABAQUS FEA package was used to optimize the designs in Novack *et al.*'s studies while I-DEAS FEA package was used here for our accelerometer design.

By following Novack's design procedure demonstrated in [32], the following "quarter" cell was constructed in I-DEAS (shown in Figure 2–7) while a 2-dimensional heat transfer analysis was employed to solve for gas damping since I-DEAS does not have an element formulated specifically for gas damping. The heat transfer elements solve the heat conduction equation for temperature, T.

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}=Q$$

T = temperature
Q = heat source per unit volume
x, y = cartesian coordinates (2.18)

This is analogous to Reynold's equation for the squeeze film damping pressure, P.

$$\frac{\partial^2 P}{\partial x^2}+\frac{\partial^2 P}{\partial y^2}=\frac{-12\mu V}{h^3} \tag{2.19}$$

where μ is the air viscosity, V is the velocity term (set to be 1000μm/s in our case), and h is the gap spacing. The boundary conditions are shown in Figure 2–7. The pressure at all nodes around the damping aperture was set to zero while the symmetrical boundaries are zero-flux boundaries.

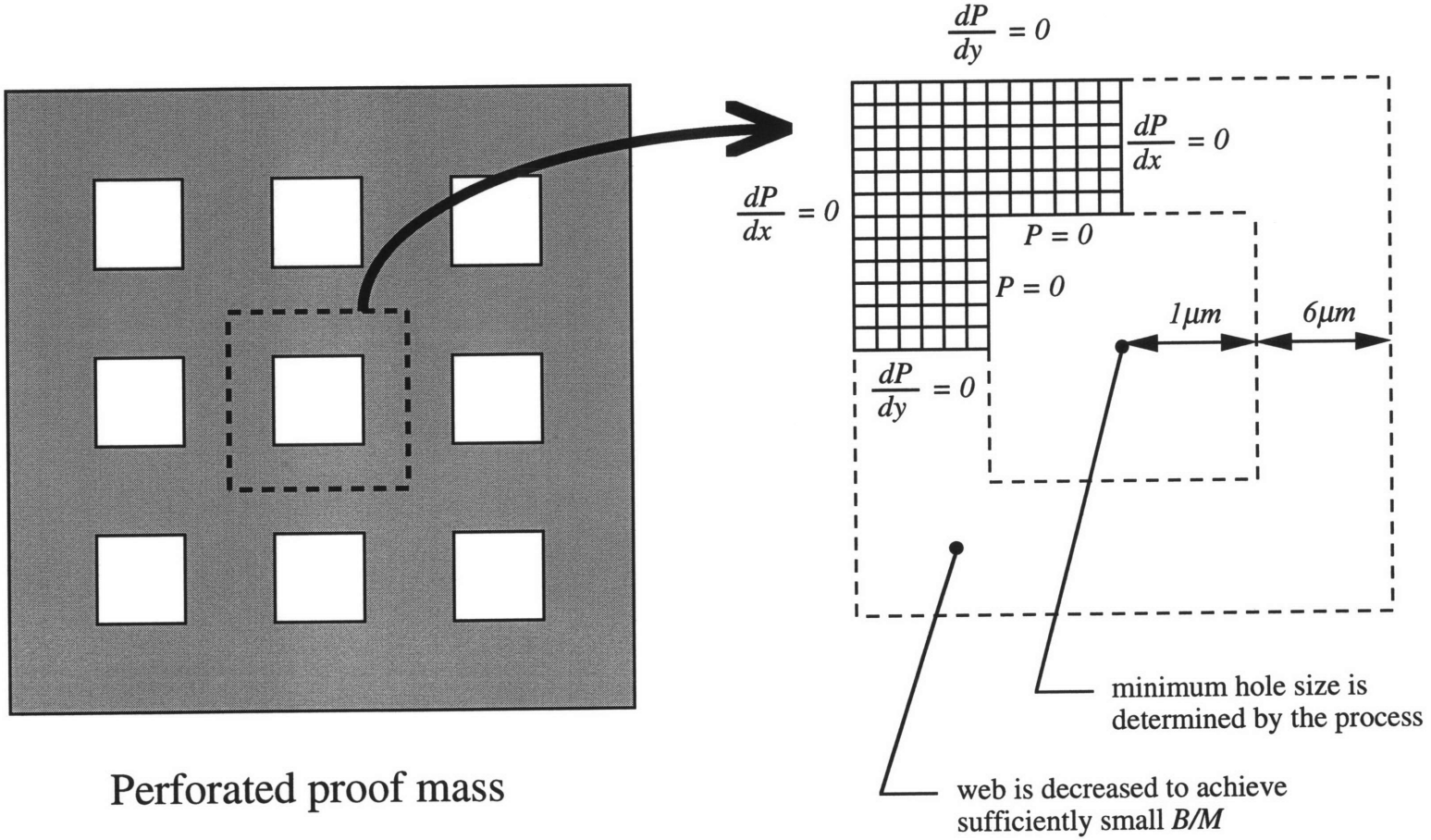


Figure 2–7: "Quarter" cell model used in I-DEAS FEA package to simulate the gas damping effect. The hole size is 2μm×2μm and the distance between damping aperatures is 12μm.

Novack's FEA procedure was used and is summarized briefly in the following:

1. Construct the finite element mesh of the "quarter" cell. Use the I-DEAS element for 2-dimensional heat transfer. There is one degree of freedom per node element, with temperature (or pressure in the gas damping case) as the unknown.
2. Apply the boundary conditions as indicated previously.
3. Specify the thermal conductivity, set it equal to 1.
4. Apply the "loads". Enter the loads as if they were sources of heat generation per unit volume. On each element, enter $Q = (-12\mu V)/h^3$. The velocity term is arbitrary since we divide it out in the calculation of the damping coefficient, $B = F/V$.
5. Run the analysis to solve for the pressure distribution.
6. Integrate the pressure over the plate area to get the damping force, F.
7. Calculate the damping coefficient, $B = F/V$.
8. Calculate the damping ratio, $\zeta = \frac{B/M}{2\omega_n}$, where M is the mass of the plate.

It is important to note that this model does not account for the "edge" effect, where the pressure at all the nodes around the perimeter of the proof mass plate should be set to zero. In addition, this 2-dimensional model does not include the "pipe flow resistance" of the damping holes, which may play a significant role in the actual damping ratio values obtained from the experiments. This model, however, does take the "slip-flow" condition into consideration. The "slip-flow" effect can best be considered as a reduction in the effective viscosity of the fluid due to slip at the boundary, here the effective air viscosity is $\mu = 1.2 \times 10^{-5} \frac{kg}{m \cdot s}$ instead of $1.8 \times 10^{-5} \frac{kg}{m \cdot s}$. The geometrical parameters of the fabricated accelerometers were carefully measured and were used in the model to obtain the "designed" damping ratio values for the three accelerometers studied in this research.

This approach is a very powerful tool because it not only allows us to reduce the damping ratio of thin-film microaccelerometers, but also gives us an approach to "tuning" this damping. Using this analysis, two accelerometer structures with sensitivity in the 5g

range and one accelerometer structure with sensitivity in the 50g range were specified and designed. The specific geometries and dimensions of the accelerometers are shown in Table 2.1. It is important to note that two versions of the damping control apertures were designed during the course of this research and both are shown in Appendix A. The damping ratio values shown in Table 2.1 are the ones associated with damping control aperture design *version 2* (shown in Figure A–9). In addition, Appendix A includes lateral dimensions of all three accelerometer structures studied in this research (Figures A–5, A–6, and A–7). The hybrid-accelerometers were designed with sensitivity in the 20g range and without any perforation since those accelerometers were designed to be sealed and operated in vacuum, and the design specifications are shown in Table 2.2.

Recently, Young *et al.* have revisited this important topic of squeeze-film damping [51–54]. The main differences between Young *et al.*'s model and Novack *et al.*'s model is that the new model takes the effect of "pipe flow resistance" into consideration. The 3-dimensional simulation results from Young *et al.* should be available in the near future. It is very desirable to use an actual 3-dimensional fluid dynamics simulation package to reinvestigate the damping control approach. In particular, it would be interesting to address whether or not the vertical fluid resistance for gas that must flow through the full thickness of the proof mass is insignificant and can be ignored, as was done in Novack's 2-dimensional model.

Table 2.1

Parameter	Accel #1	Accel #2	Accel #3
STRUCTURAL DIMENSIONS			
Proof mass dimensions	515μm×515μm ×10.8μm	515μm×515μm ×10.8μm	515μm×515μm ×10.8μm
Gap spacing	1.1μm	1.1μm	1.1μm
DYNAMICS			
Resonant frequency	2.96kHz	3.17kHz	15.12kHz
Damping ratio 2-D FEM	4.34	4.06	0.86
ELECTRICAL CHARACTERISTICS			
Sense capacitance	2.347pF	2.347pF	2.347pF
Parallel stray capacitance	<<10pF	<<10pF	<<10pF
Resistance to electrodes	<50Ω	<50Ω	<50Ω

Table 2.1: Design specifications for the three discrete, dielectrically isolated microaccelerometers.

Table 2.2

Parameter	Structure 1	Structure 2
	STRUCTURAL DIMENSIONS	
Proof mass dimensions	750μm×750μm ×10.8μm	500μm×500μm ×10.8μm
Gap spacing	1.0μm	1.0μm
Electrode dimensions	730μm×730μm	480μm×480μm
	DYNAMICS	
Resonant frequency	3.23kHz	6.78kHz
	ELECTRICAL CHARACTERISTICS	
Sense/feedback capacitance	4.716pF	2.039pF
Parallel stray capacitance	<<10pF	<<10pF
Resistance to electrodes	<10Ω	<10Ω
Resistance to proof mass	~500Ω	~500Ω

Table 2.2: Design specifications for the two microaccelerometers designed to be stitch-bonded to Ashburn's custom-designed chip.

2.4 Summary

The mechanical design and analysis of the microaccelerometer began with use of a simple mass-spring-damper system to model the behavior of the device. Through simple models and calculations, design equations which relate the physical dimensions of the accelerometer structure to key accelerometer characteristics, such as sensitivity and bandwidth were derived. The capabilities/limitations of our chosen fabrication technology, as well as a decision to use capacitive detection were used to further refine the design space for specifying the accelerometer structure. The design analysis then focused on the primary aspect of the accelerometer design: the addressing of the squeeze-film damping problem. An approach to reduce the squeeze-film damping problem found in many micromechanical structures was presented. By appropriate placement of "damping control apertures", the damping in an severely over-damped accelerometer structure (~1420) could be reduced to a much smaller damping ratio (~4.34) with only a 3% increase in edge length of the proof mass. This design approach demonstrates how the damping in these structures can be "tuned" by appropriate selection of damping apertures. Two squeeze-film damping models were presented in this chapter as well. The majority of the work cited in this chapter was developed by Novack and McNeil in [31–32].

Chapter 3

Process Enhancements

3.1 Overview

This chapter gives a detailed description of the wafer-bonded sealed cavity process which serves as the platform for the integrated MEMS-CMOS process described in this chapter. A brief discussion on wafer bonding follows the integrated MEMS-CMOS process flow. Two specific process enhancements are then discussed; electrical isolation of the mechanical structure from the substrate, and dry release of the mechanical structure. For electrical isolation of mechanical structure from the substrate, detailed discussions on the junction isolation scheme and the dielectric isolation scheme are shown in Sections 3.4 and 3.5 respectively. The dry release method serves as an important "back-end micromachining" process in order to functionalize the surface-micromachining-like microstructures. Detail of this plasma dry release etch is shown both in Section 3.6 and in Chapter 4. Junction isolation and dry release facilitate the successful fabrication of

lateral comb-drive resonators, which in turn provide a material property study opportunity. In addition, diodes formed with junction isolation and dry release process help in understanding the electrical properties of the bonded interface. Combination of dielectric isolation and dry release ensures successful fabrication of M-Test structures which in turn complete the MEMS-CMOS process verification presented in this thesis and in Parameswaran's Ph.D. thesis [7].

3.2 Integrated MEMS-CMOS Process

A process for fabricating integrated silicon micromachined sensors is demonstrated in this section. This process uses silicon wafer bonding to create a substrate that can be inserted into an existing IC fabrication line without perturbation of the line. After circuits are completed, micromachining steps are performed to release the silicon membranes and form the sensors. A variety of test structures including MOSFETs, piezoresistive pressure sensors and cantilever beams were successfully fabricated, and all were functional, indicating that the additional micromachining steps and CMOS thermal cycles caused no adverse effects to the devices.

The integrated MEMS-CMOS process flow is partitioned into 3 sections, as previously shown in Figure 1–6 in Chapter 1. Figure 1–6 illustrates the general process flow, in which the front-end micromachining process steps are used to form a sealed cavity substrate. The IC fabrication can be any existing foundry process, since the cavity is internal to the substrate so no special fixturing is required. The cavities are formed by contacting the wafers in a controlled ambient, resulting in membranes that are able to withstand the high temperatures seen in an IC process flow. The back-end micromachining steps are designed to be low temperature, predominantly dry processes.

The complete process flow is illustrated in Figure 3–1 [7], as developed to make a pressure sensor, an accelerometer, and CMOS circuitry. The front-end micromachining steps start with two <100> silicon wafers. The handle wafer is an n-type substrate with shallow plasma-etched cavities, some of which contain a stack of stress-relief oxide and silicon nitride at the base of the cavities (Figure 3–1(a)). The device wafer is a p-type substrate, with a 10 μm-thick n-type epitaxial layer (the epitaxial layer thickness defines the thickness of the sensor). The two wafers are cleaned, contacted in an oxygen ambient, and annealed at 1100°C for 1 hour. Subsequently, the device wafer is thinned using grinding and polishing followed by electrochemical etching which stops at the n-epitaxial layer, resulting in uniform 10 μm-thick membranes over enclosed cavities. The wafers are next run through a 1.50μm twin-well CMOS flow, with completed substrates as shown in Figure 3–1(b).

The post-CMOS back-end micromachining steps are shown in Figures 3–1(c) and 3–1(d). First, backside pressure inlet holes for pressure sensors are formed with an anisotropic etch in potassium hydroxide, using a layer of PECVD silicon nitride as an etch mask to protect the rest of the wafer. The etchant stops on the buried silicon nitride layer inside the cavities. Next, the silicon nitride etch mask is removed from the front of the wafer after which the frontside dry-release etch can be done. This is a two-step plasma etch in SF_6 through the silicon membrane that results in the formation of "surface-micromachined" structures [60]. Finally, the remaining silicon nitride etch mask on the back of the wafer is removed, again with a dry etch, thus releasing the pressure sensor membranes. The wafers tested for this work did not have the backside pressure inlet hole implemented; however, this technique has been successfully demonstrated in a non-integrated capacitive pressure sensor [7].

In more details, back-end process steps are divided into three categories: back and frontside releases, and the formation of a top electrode for capacitively detected devices. The backside release step is used to form membranes for pressure sensors, and requires a modification to the basic sealed cavity process - the formation of an etch-stop layer inside

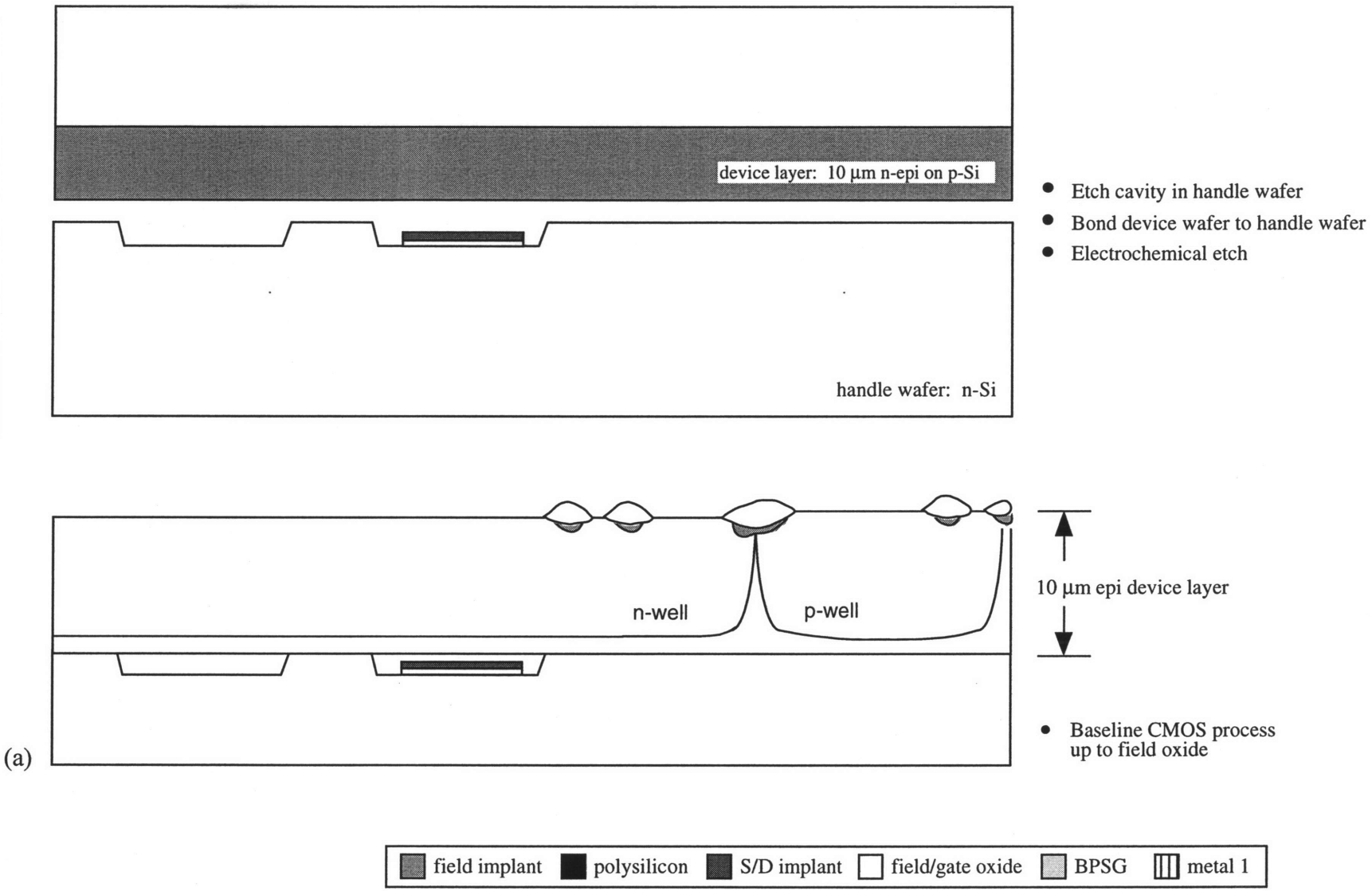


Figure 3–1: Integrated MEMS-CMOS process flow.

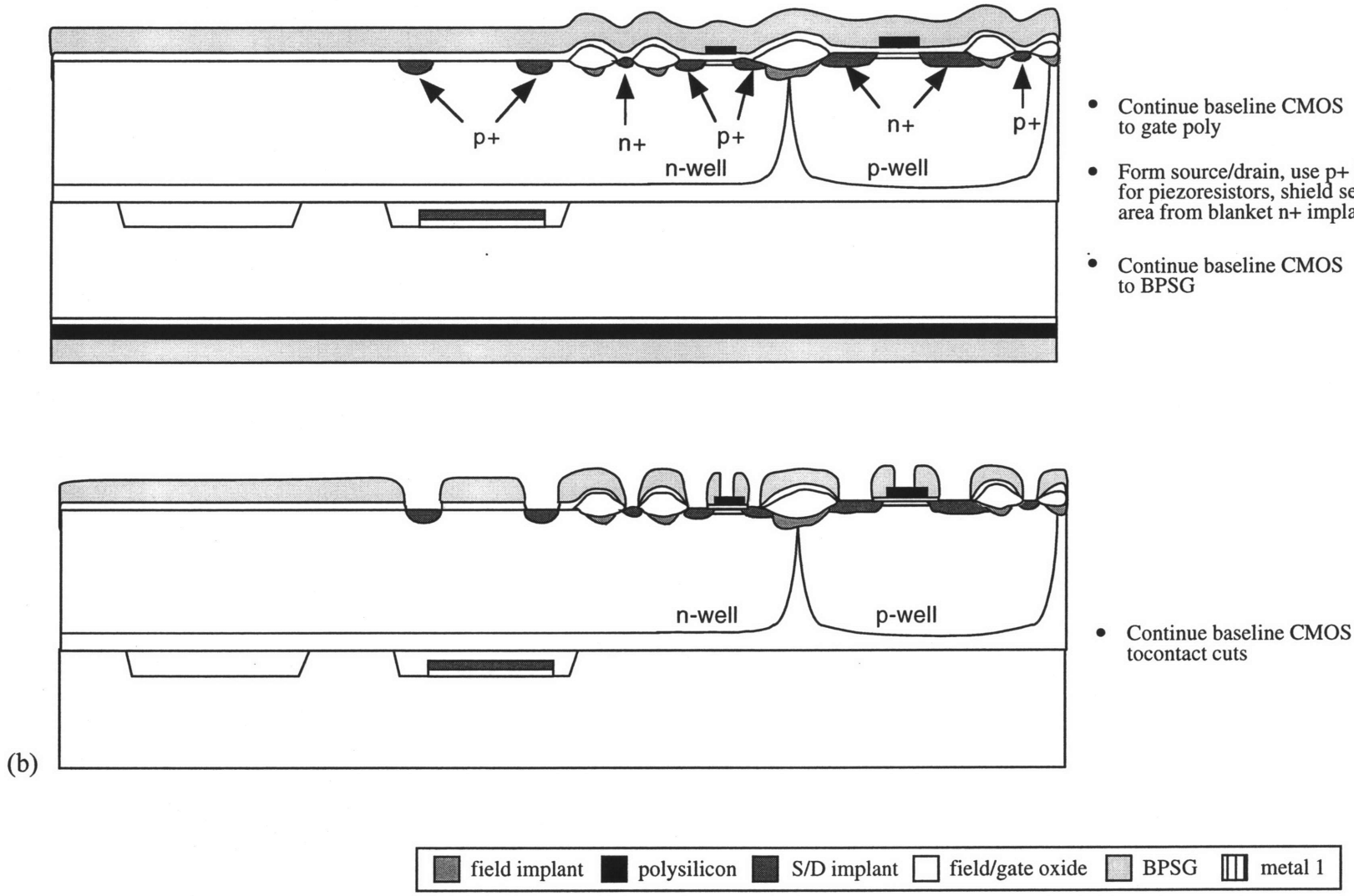


Figure 3–1: Integrated MEMS-CMOS process flow (cont.).

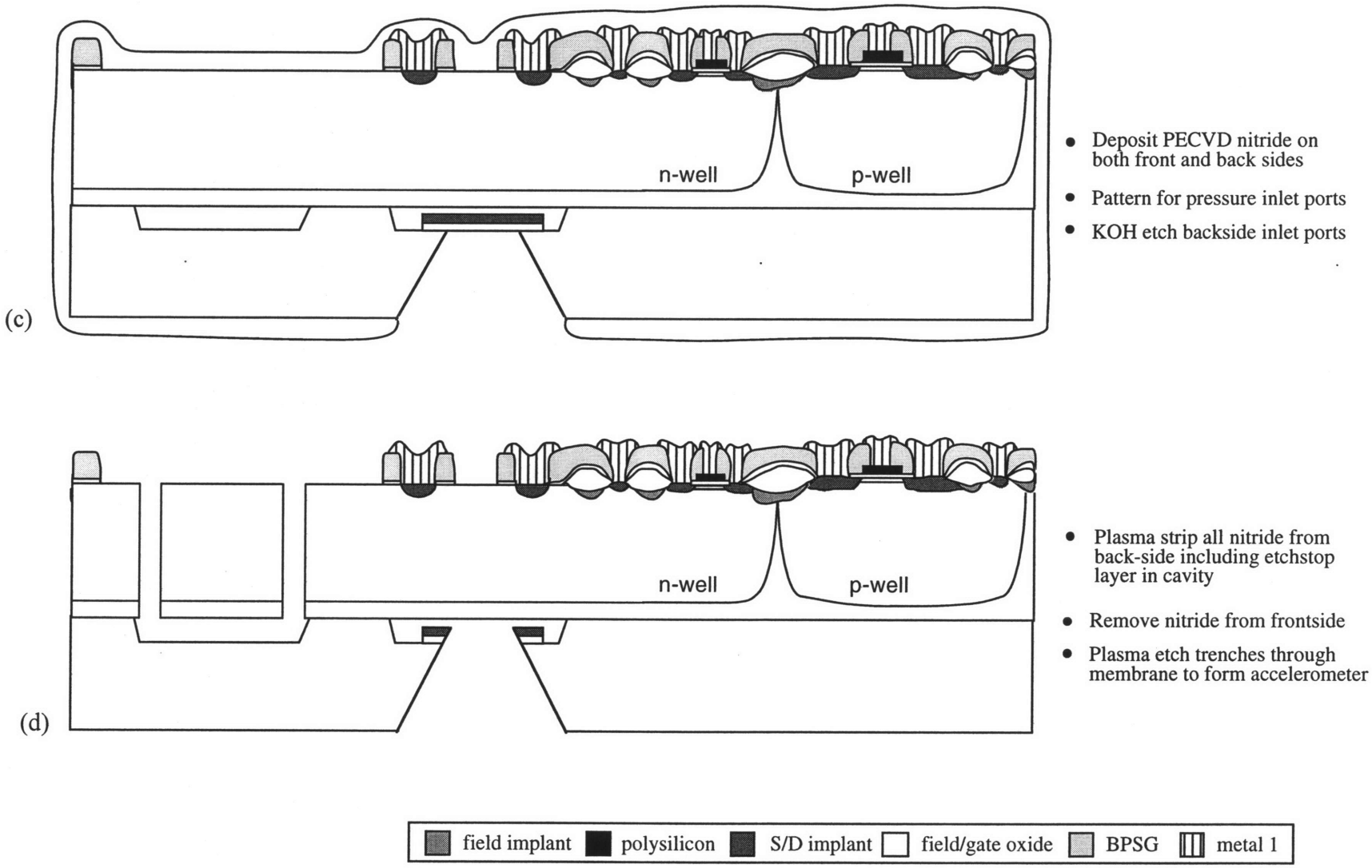


Figure 3–1: Integrated MEMS-CMOS process flow (cont.).

the cavity prior to bonding. This consists of a stack of 430Å of thermal silicon dioxide and 1500Å of LPCVD silicon nitride, patterned and etched to remain only inside the cavity. The wafers are then bonded and thinned as previously shown, followed by circuit processing, up to and including metallization. A layer of low temperature PECVD silicon nitride is deposited over the entire wafer and patterned on the backside in preparation for the backside release etch done in KOH, which stops on the buried stack of oxide and nitride. The nitride membrane is strong enough to avoid rupture during photolithography for the subsequent frontside release and metallization steps, thus preventing liquid from entering the region under the membrane. After the etch, the nitride is removed from the front of the wafer with a plasma etch in SF_6.

Next, the frontside release etch is done, followed by a final plasma etch to remove the buried nitride inside the cavity. This step is used to fabricate surface-micromachining-like structures, and consists of a two-step plasma etch in SF_6 through the silicon membrane, thereby releasing the suspended structure. Because the etch is dry, stiction of the released devices is avoided.

The capacitive electrode was developed to facilitate the integration of on-chip amplification and/or signal conditioning circuits that are often required for capacitive sensors which usually have low signal levels. Since it is to be formed in the final stages of the process, only low temperature dry process steps are used, as it is done after aluminum metallization for the circuits. The top electrode consists of a metal layer on a glass substrate. This glass cap is attached to the silicon substrate via a metal thermocompression bond, between two layers of gold. The capping wafer is a Pyrex 7740 glass wafer, but can also be a silicon wafer for better thermal matching, provided that suitable means are available for alignment of this nontransparent wafer to the substrate. The front of both the substrate and cap wafer are metallized with 6000Å of gold over an adhesion layer of 100Å of chromium, patterned using liftoff. Gold is selected as the metallization for two reasons: first, it does not form a surface oxide in air, so that scrubbing/ultrasonic action is not needed to break through the oxide to achieve contact,

and second, it can be bonded at a relatively low temperature. The metal surfaces are cleaned with an exposure to ozone under UV light, aligned and contacted, and heated to 350°C while a pressure of about 20psi is applied for a period of 2 minutes.

The strength of the thermocompression bond in a shear test is in excess of 1000psi, with failure usually occurring in the bulk of the substrates, not at the metal-metal interface. This value corresponds with similar values given for standard shear test of wire bonds.

3.3 Wafer Bonding

Silicon wafer bonding, also known as silicon fusing bonding or direct wafer bonding was developed in the 1960s [55] and is an adhesiveless wafer-to-wafer bonding technique employed by Lasky at IBM and Shimbo at Toshiba in 1985 [56–58]. This technique was quickly exploited for the production of a host of power and SOI devices. In addition, this fabrication technique began to be used as a powerful new tool for fabricating silicon microsensors. The development of new microsensors using silicon wafer bonding technique continues, and has resulted in the creation of shear-stress sensors, microvalves, microswitches, pressure sensors, gyroscopes, and accelerometers.

The creation of micromechanical devices often requires cavities or trenches to be etched into the handle wafer before the device wafer is bonded (see Figure 1–6). These cavities can be created using either bulk micromachining or standard dry etching techniques. Once the handle and device wafers are bonded, controlled thinning is performed to remove most of the device wafer, and leave a thin membrane over the cavity. It is possible to repeat bond, thin, polish, and etch steps needed to create very complex laminated silicon structures.

3.3.1 Process Enhancements

The sealed cavity wafer-bonded process used in this research is a derivative of the silicon fusing bonding technology used in various research and industrial laboratories in the early 1990's [26–27]. Figure 1–6 illustrates the general flow of this process. Two major front-end technology issues in using wafer bonding for the fabrication of sensors and actuators; wafer thinning processes, and the control of the residual pressure in cavities formed by bonding and etchback, have been discussed in detail previously [7, 29–30]. The back-end processes entail etching of the mechanical layer for accelerometers or etching of a pressure inlet port for the pressure sensor [29–30], followed by the low-temperature bonding of a capping wafer.

In order to realize this process, as briefly described in Chapter 1 of this thesis, the following important steps must be taken:

- Controlled-ambient wafer bonding
- Wafer thinning
- ✔ ***Electrical isolation of the mechanical structures from the substrate***
- ✔ ***Dry release process***
- Upper electrode formation

The controlled-ambient wafer bonding process has previously been studied and used extensively; however, it will be discussed briefly in the following section for completeness. Various wafer thinning and etch-stop technologies have also been carefully examined and discussed by McNeil [31], and the ECE technique will be briefly discussed in Section 3.3.3. Here we shall focus our attention to two key process enhancements: electrical isolation of the mechanical structures from the substrate and the dry release process. We utilize electrochemical etch-stop, SOI buried oxide etch-stop, or mechanical/chemomechanical polishing technique to achieve the first process enhancement. A large class of sensors and actuators will benefit from the ability to electrically isolate the mechanical structures from the substrate. Two isolation schemes

are employed in this study; namely, a junction-isolation scheme and a dielectric-isolation scheme. A dry release process is an attractive choice to form thin-film micromechanical structures since the *stiction* problem associated with many wet release processes no longer plays a vital role in the yield of the released microstructures. A completely dry process is used to pattern the bonded mechanical layer to form various "surface-micromachining-like" structures [60–63] and is detailed in a Section 3.6.

3.3.2 Controlled Ambient Bonding

Silicon is desirable as a mechanical material for microstructures because of its high strength and reliability, and well-characterized electrical properties. Its mechanical properties have been studied extensively, and its elastic-plastic behavior is fairly well known. At temperatures below approximately 600°C, silicon is a brittle material with a fracture strength of 0.7GPa. Above this temperature, it becomes ductile and exhibits a stress-strain curve characteristics of most semiconductors, schematically illustrated in Figure 3–2. As indicated in Figure 3–2, when the induced stress in silicon exceeds the upper yield stress for a given strain rate, the silicon will plastically deform, after which the deformation is sustained if the stress in the material stays above the flow stress. The plastic deformation is manifest as a warpage of the silicon when cooled back to room temperature, as well as an increased concentration of dislocations.

Plastic deformation in sealed cavities arises from the expansion of trapped gas inside the cavity at high temperatures. Its onset is dependent on the device geometry as well as the pressure of the gas trapped inside the cavity. The expansion of this trapped gas causes a pressure load on the membrane as it is heated past the transition temperature

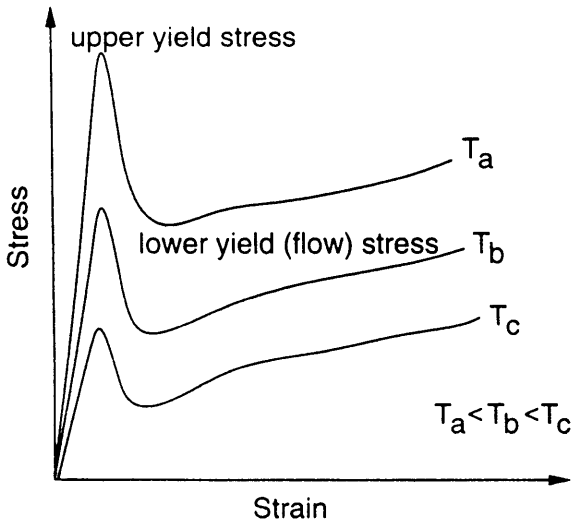


Figure 3–2: Qualitative stress *vs.* strain behavior of silicon.

of the silicon from the brittle to the plastic regime. The effect of heating a sealed cavity is illustrated very simply in [7], where the sealed cavity is formed by contacting the wafers in room air and annealing. After thinning of the top wafer, the silicon plate is deflected downwards into the cavity. The initial downward deflection of the plate into the cavity occurs as a result of the wafer bonding process, in which the oxygen content of the trapped air inside the cavities is consumed by oxidation of the surrounding silicon sidewalls during the high temperature bonding anneal, thus leaving a reduced partial pressure inside the cavity at room temperature. Upon heating, gas expansion causes the plate to deflect upwards. If the maximum temperature is kept below about 600°C, the membrane will either return to its original shape upon cooling, or rupture if the load exceeds the fracture strength. However, if the maximum temperature is greater than 600°C and the stress in the plate exceeds the yield stress, plastic flow commences and the plate will not return to its original shape upon cooling but will maintain its upwardly deflected shape.

The phenomenon of plastic deformation in thin silicon plates was described in detail by Huff [64] in which a model was developed to predict the onset temperature of plastic deformation of these plates under high temperature anneals. From this model, it is

apparent that one method of avoiding plastic deformation is to reduce the gas expansion loading of the plate, by reducing the trapped gas pressure inside the cavity. This is achieved by controlling the ambient in which the wafers are contacted, either by contacting in a partial vacuum or in an oxygen-rich environment.

In this research work the latter approach was taken, and the setup used to contact the wafers is illustrated in Figure 3–3. The chamber holds the two wafers to be bonded, separated by Teflon shims, and is flooded with a controlled mixture of oxygen and nitrogen gases. The separators are removed and bonding is initiated with a point contact at the center of the wafers, after which they are annealed at 1100°C in an inert or oxidizing ambient and electrochemically thinned. The measured deflection of the plates, along with the equations given in [65] are used to calculate the residual pressure inside the cavities, results of which are shown in Table 3.1 [7]. Uncertainties in the calculated residual pressure are attributed to errors in the deflection measurement, and the variation in the plate thickness. As the table indicates, a range of cavity pressures is obtainable using this setup. All wafers fabricated for this research work were bonded in a pure oxygen ambient, thus the residual cavity pressure is below 0.5 atmosphere.

Table 3.1: Residual pressure for various bonding ambients

Ambient	Residual cavity pressure
Air	0.77 ± 0.05 atm
50%N_2 / 50%O_2 mix	0.56 ± 0.05 atm
30%N_2 / 70%O_2 mix	0.38 ± 0.05 atm
20%N_2 / 80%O_2 mix	0.17 ± 0.05 atm
100% O_2	0.05 ± 0.05 atm

(after *Refs. 7 & 30*)

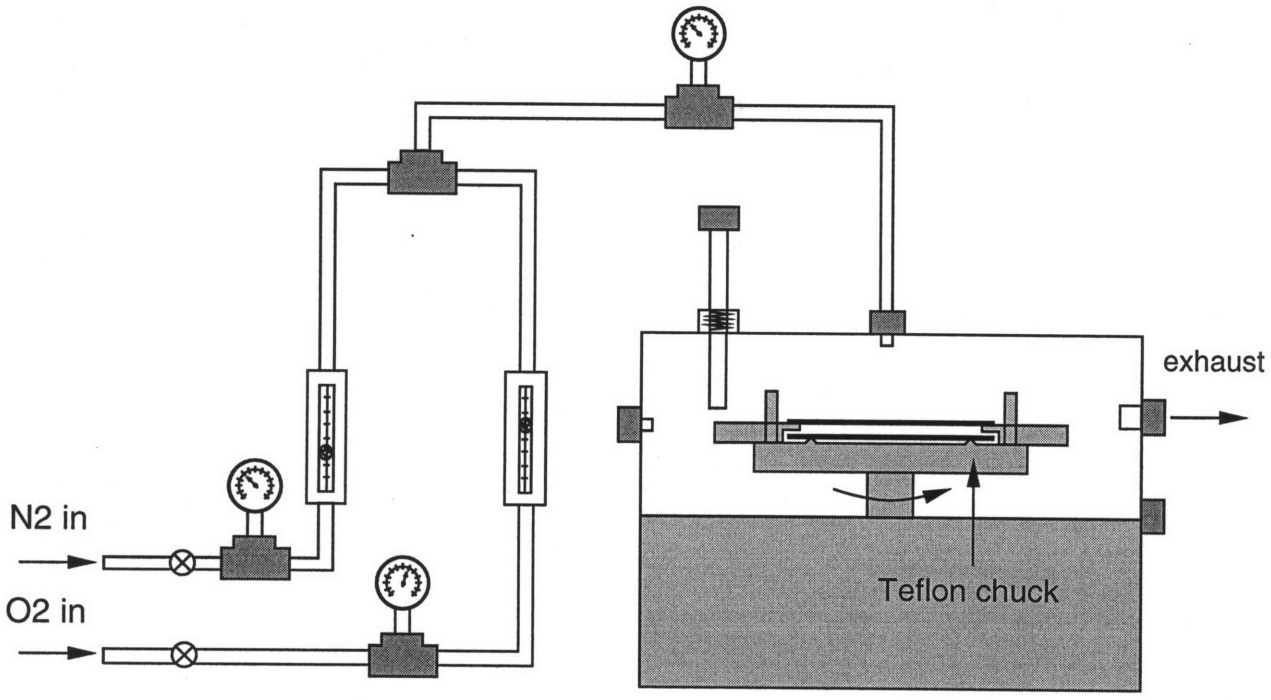


Figure 3–3: Setup for controlled ambient bonding (courtesy of L. Parameswaran).

3.3.3 Wafer Thinning

The sealed cavity is formed by wafer bonding and thinning of the device or active wafer as indicated in Figure 1–6. One of two methods can be used for wafer thinning, each of which requires a particular type of active wafer. The first is electrochemical etching, which is the bias dependent selective etching of p-type silicon over n-type. For use in making sealed cavities, the technique constrains the dopant type of the active layer (membrane layer) to be n-type. To circumvent this, another approach is to use an SOI wafer as the active wafer, in which case the buried oxide serves as the etch-stop layer and the active layer can be any dopant type. This also permits the formation of silicon structures that are dielectrically isolated from the substrate. In both methods, the chemical etch is preceded by a bulk material removal via grinding and chemo-mechanical polishing, and etching is done in an anisotropic etchant such as KOH. The electrochemical etch technique as applied to full wafer thinning will be discussed in this section and the application of an SOI substrate as the active wafer to make dielectrically isolated devices is considered in a later section of this chapter.

The electrochemical etch-stop is used to define the membrane thickness because of the fact that it does not require a heavily doped layer to act as an etch-stop. It does however require the presence of a diode, which as mentioned before, constrains the active layer to be n-type. The difference in passivation voltages required to anodically oxidize n and p-type silicon permits the selective etching of p-type silicon. Parameswaran and McNeil have presented detailed description of the ECE setup used in a p-n junction etch-stop configuration, and their work will be summarized as follows [7, 29–31].

A standard three-terminal configuration is used for etching (shown in Figure 3–4), with the wafer held in a Teflon chuck by means of a vacuum hold. The surface of the chuck is covered with a fine platinum wire mesh to provide electrical contact to the backside of the wafer. The etchant is a 20% (by weight) solution of KOH, heated by

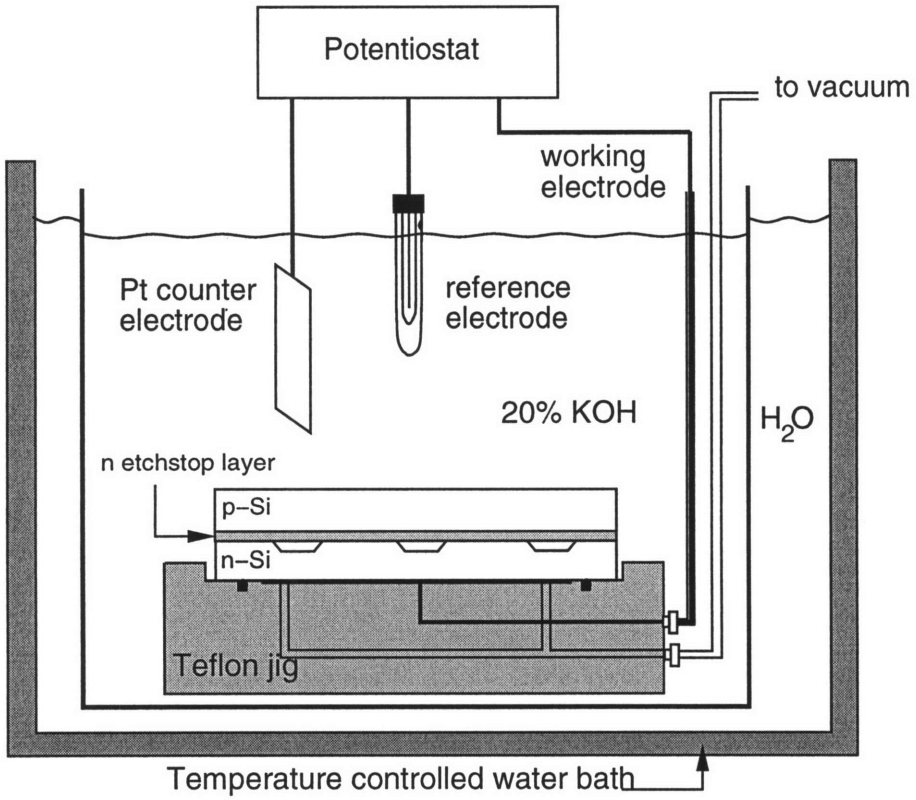


Figure 3–4: Schematic of three-terminal junction electrochemical etch-stop setup.

means of a water bath with a temperature control of ±0.1°C. A PARC EG&G potentiostat is used to maintain a constant bias on the n-type silicon, and a platinum counter electrode and double junction Ag/AgCl reference electrode complete the circuit. In order to decrease the surface roughness, a surfactant FC-129 was added in the ratio of approximately 2g/L of KOH solution.

Ideally the etch should stop at the metallurgical junction between the n and p-type silicon, but it has been found that membranes thus obtained are sometimes thicker than the etch-stop layer thickness. The membrane thickness also varies with the temperature of the etchant. Spreading resistance analysis (SRA) of wafers etched at various temperatures was done to determine the amount of p-type silicon left remaining after the etch. As presented by Parameswaran [30], Table 3.2 gives a summary of the results from SRA of the samples. The spreading resistance data indicates that as the etchant temperature is increased, the etch stop occurs closer to the metallurgical junction. It was observed that an etchant temperature of 95°C is required to remove all of the p-type silicon for the samples used. Previous work has indicated that the successful completion of the etch depends on two factors, these being the maintenance of a sufficient potential to reverse bias the diode junction, and the presence of a low diode leakage current. As the etch front approaches the junction, the reverse diode leakage increases until it exceeds the current density required for passivation, at which point etching will cease. Under ideal conditions the leakage current will remain negligible until the metallurgical junction has been reached; in reality the leakage current is a function of the etchant temperature, concentration, and amount of unetched p-Si remaining.

Table 3.2: Electrochemical etch temperature experiment

Etchant temp. (°C)	x_p from SRA (μm)
95	0.1 ± 0.05
90	0.5 ± 0.05
80	1.2 ± 0.10
70	1.7 ± 0.10

(after *Refs. 7 & 30*)

The results obtained here indicate that for the given concentration of KOH, the passivation current density is a stronger function of temperature than the diode leakage, meaning that a higher etch temperature leads to a larger increase in the required peak passivation current than the diode leakage current. Thus etching at higher temperatures should yield an etch-stop layer thickness which is less sensitive to diode leakage current. We shall point out here that similar results are observed for p-n-p electrochemical etch-stop discussed in the next section.

3.4 Junction Isolation Scheme

Wafer thinning methods are critically important in wafer bonded micromachining processes since the thickness tolerance of the mechanical parts will be defined by this step. In our previous work [29], we described an electrochemical thinning process that produces a n-type mechanical layer on a n-type substrate in Section 3.3.3. However, electrical isolation is important for a class of structures built in this technology (accelerometers and gyroscopes, for example). Two technical approaches are either to use

a junction electrochemical etch-stop and a p-type substrate wafer (*junction-isolation*) or to use a buried chemical etch-stop (p^{++} doping or oxide) and bonding to an oxide coated substrate wafer (*dielectric-isolation*) as illustrated in Figure 3–5. While the chemical etch-stop permits formation of dielectrically isolated mechanical parts, the availability, quality, and cost of either SOI starting material or buried p^{++} epi is a limiting factor. However, the dielectric isolation scheme facilitates the fabrication of M-Test structures and will be discussed in Section 3.8 in detail. Electrochemical etch-stop methods are known to produce high quality mechanical structures, but the layers are most conveniently formed by silicon-silicon bonding, where the lower wafer provides an accessible electrical connection during the etch-stop process. This process thus precludes electrical isolation of the mechanical parts from the substrate. In an attempt to capitalize on the convenience of a silicon-silicon bonded electrochemical etch-stop, while still achieving electrical isolation of the mechanical layers, we have implemented a p-n-p structure for the etch-stop. Details of the p-n-p electrochemical etch-stop process have been presented before [60], and the effectiveness of the resultant junction-isolation scheme are presented here for completeness.

3.4.1 As-Bonded Junction Isolation

The process starts with two wafers, a handle wafer containing etched cavities, and a device wafer containing the mechanical layer. Figure 3–5(a) illustrates the sealed cavity process with as-bonded junction-isolation. Epi wafers were composed of an n-type (5Ω-cm) layer with an average thickness of 11μm on a p-type (10-20Ω-cm) substrate. The handle wafers are subjected to a boron blanket implant and drive-in to heavily dope the back surface ($>5\times10^{19}cm^{-3}$) in order to ensure good electrical contact during the

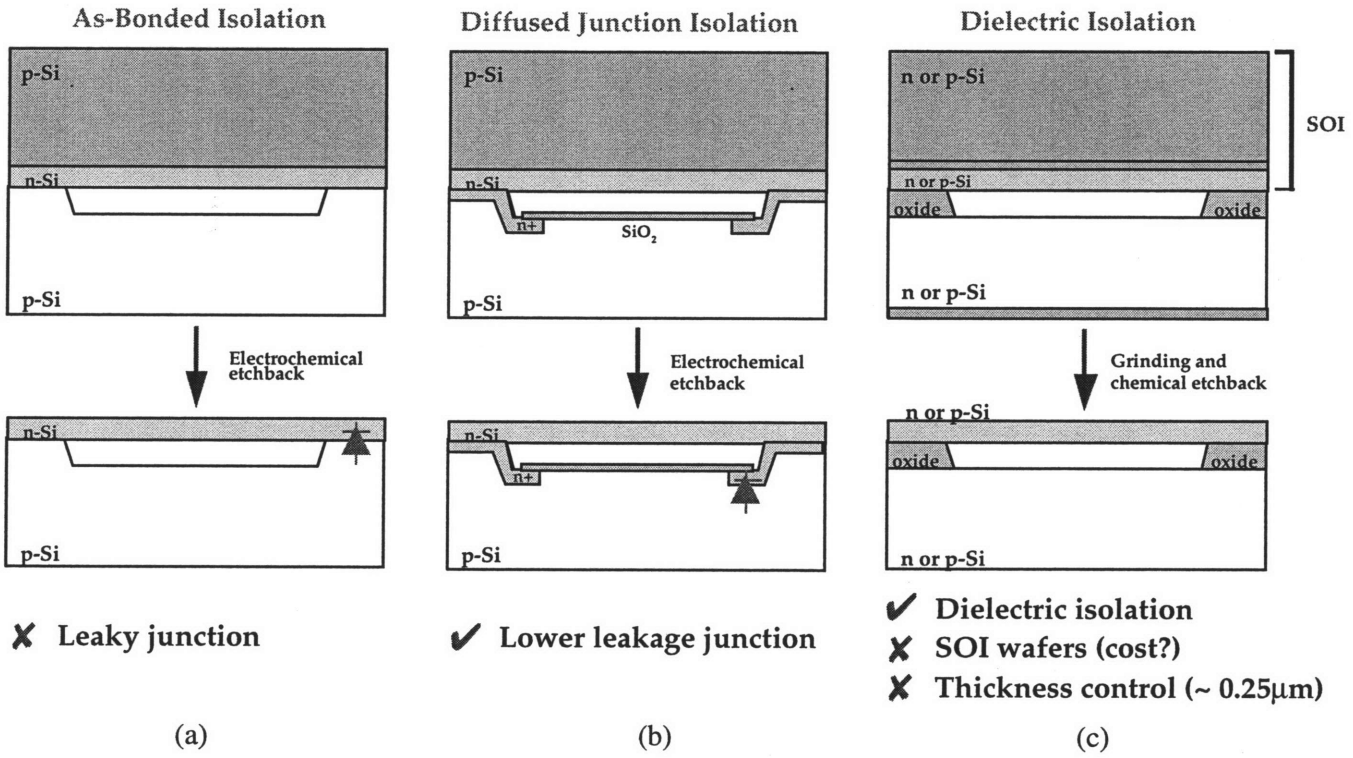


Figure 3–5: Electrical isolation schemes.

electrochemical etch and to provide ohmic contact for backside metallization later in the fabrication process.

Two sets of as-bonded junction isolation samples were prepared for this study: *hydrophilic vs. hydrophobic.* The difference between them is that after being hydrated with a standard RCA clean, *hydrophobic* samples were dipped in diluted HF solution before bonding to remove native oxide. Device wafers and patterned handle wafers were contacted in a pure oxygen ambient using the controlled ambient bonder described in Section 3.3.2. After the bonded wafers were inspected for the presence of voids using an infrared camera, they were subjected to a high temperature anneal for one hour at 1100°C in a nitrogen ambient to strengthen the bond.

Subsequently, the device wafer is thinned back using a two-step process. First, the wafer pair is ground and polished to remove about 400μm of silicon from the device wafer. The wafer surface is chemically polished until a mirror smooth finish is obtained. The wafer pair is then electrochemically etched using the procedures and apparatus described previously [60]. The sample differs from previous work in the existence of an additional diode (diode #1 in Figure 3–6) which is incorporated to provide electrical isolation in the final structure. The electrochemical etch, however, requires positive bias on the handle wafer, which acts to forward bias this extra diode. In its forward biased state, the diode has very little impact on the operation of the electrochemical etch. Thus the etch will still terminate at the junction formed between the n-epi and the p-type substrate, and will result in an n-type mechanical layer sitting on a p-type substrate.

It is important to be able to accurately control the thickness of the bonded and etched back layer over the cavity in order to make well-defined mechanical parts. We have previously reported that the position of the "standard" n-p electrochemical etch-stop relative to the metallurgical junction is a function of etchant temperature, such that an increase in the temperature results in a stop closer to the junction [60].

In order to verify this temperature dependence for p-n-p electrochemical etch-stop process, full wafer samples, fabricated as described above, were etched at various

etchant temperatures. A cross-sectional schematic of the sample after etchback is given in Figure 3–6. Of interest is the value of x_p, the amount of p-type silicon remaining unetched above the metallurgical junction, since if this value is zero, the thickness of the bonded layer is determined solely by the junction depth of the etch-stop layer. Spreading resistance analysis (SRA) of the etched-back wafers was done to determine x_p. Table 3.3 gives a summary of the results from SRA of the samples. At our usual etching temperature (95±1°C), the etch stopping point does reach the metallurgical junction. The measured roughness of the etch-stop surface is somewhat dependent on etch-conditions, but roughnesses between 50Å and 200Å are typical, with the use of a surfactant in the KOH etchant.

3.4.2 Diffused Junction Isolation

The diffused junction isolation process is very similar to that of the as-bonded junction isolation process; however, now the "junction" has been moved into the bulk of the silicon handle wafer as illustrated in Figure 3–5(b), thus additional phosphorus doping in the handle wafer is required. The first step in the fabrication involves the plasma etching of 1μm trenches in a <100> p-type silicon handle wafer. The backside of the handle wafer is subjected to the same high dose blanket boron implant and drive-in as described in Section 3.4.1. The diffused junction is then formed by a patterned implant of phosphorus (90keV, $5\times10^{15}cm^{-2}$) through a 430 Å-thick thermal oxide (stress-relief-oxide, SRO) after a blanket light boron implant (70keV, $8\times10^{11}cm^{-2}$) on the handle wafers. This light boron implant is necessary to prevent inversion on the silicon surface. The junction depth of the diodes formed by the implant and drive-in is x_j = 2.1μm.

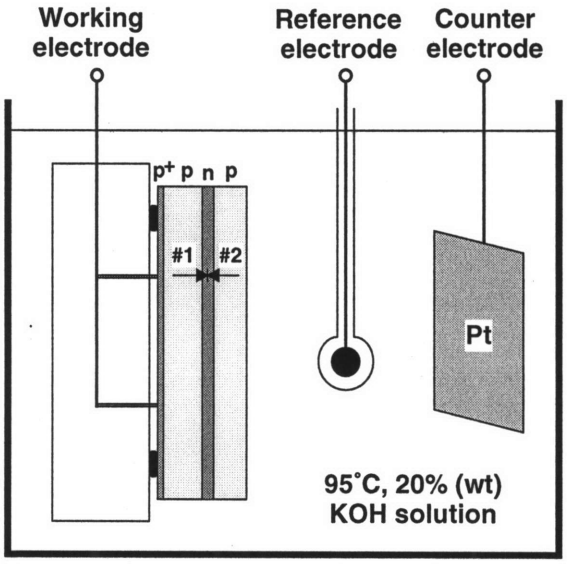


Figure 3–6(a): P-n-p electrochemical etch setup.

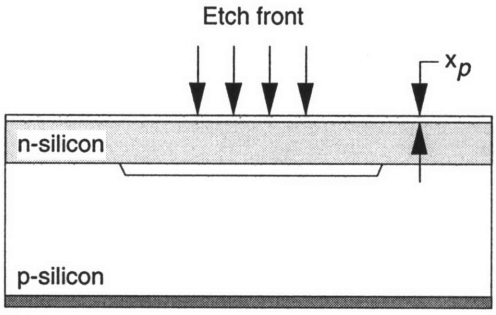


Figure 3–6(b): Sample cross-section after p-n-p ECE.

Table 3.3: x_p results from SRA

Etchant Temp. (°C)	x_p form SRA (μm)
95 ± 1	0.0 ± 0.05
90 ± 1	0.0 ± 0.05
85 ± 1	0.3 ± 0.10
75 ± 1	0.5 ± 0.10

Four sets of diffused junction isolation samples were prepared for this study. Aside from the *hydrophilic* and *hydrophobic* sets, each set also includes samples with different oxide passivation layers, as illustrated in Figure 3–7. A thin oxide layer (densified LTO only or densified LTO on top of SRO) is grown or deposited on the handle wafer after the cavities have been etched. The function of this thin oxide layer is to electrically passivate the trench surfaces. This thin oxide layer also helps to minimize the plasma damage to the wafer surface during the final deep Si etch. However, this oxide passivation layer still does not passivate the trench sidewalls. After removing the oxide from the field area, the handle wafer is then contacted to a device wafer in a pure oxygen ambient to form a sealed cavity. The contacted wafer pair is subsequently annealed and processed as described in Section 3.4.1.

3.5 Dielectric Isolation Scheme

SOI wafers with 0.4μm buried oxide, 9.85–10.42 μm-thick n-Si (6Ω-cm) device layers, and n-Si (6Ω-cm) substrates are used as device wafers for this process. The sealed cavity process with dielectric-isolation is illustrated in Figure 3–5(c). The handle wafer is subjected to boron implant and drive-in as described in the previous section. Next, a layer of 1 μm-thick thermal oxide is grown on the handle wafer. This oxide layer is then patterned and etched (BOE etch) to form cavities. The backside oxide layer is protected by a resist mask during the patterning BOE etch. This oxide layer is used as a masking material during the wafer thinning process. The device wafer and handle wafer are brought to contact in a controlled ambient as described in the previous section. After initial contact, the wafer pair is then annealed for one hour at 1100°C in a nitrogen ambient to strengthen the bond.

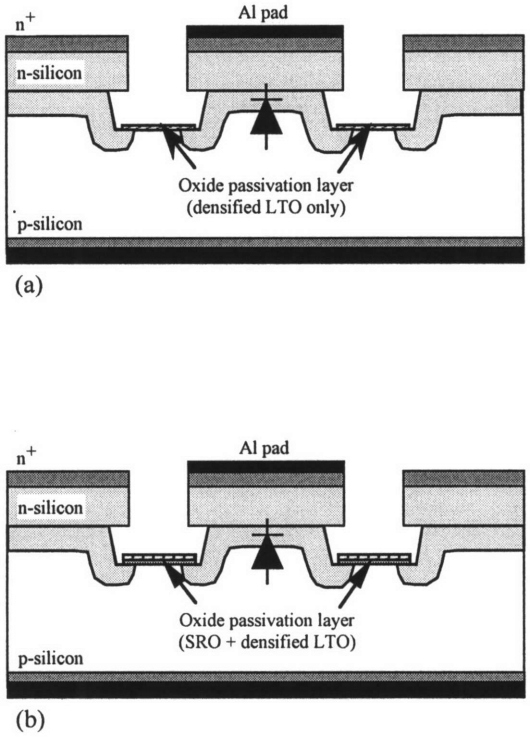


Figure 3–7: (a) Passivation layer consists of 1000Å densified LTO only.
(b) Passivation layer consists of 1000Å densified LTO on top of 430Åof SRO.

The device wafer is then ground to remove approximately 480μm of silicon. Next, the wafer pair is chemically etched in a 95°C, 20% (by weight) KOH solution until the etch terminates at the buried oxide etch-stop. The oxide etch-stop is then removed by wet-etching in BOE. Finally, the etched-back wafers are subjected to the post-KOH clean before they are returned to the IC fabrication line. Dielectrically isolated test structures enable us to formulate an attack plan to extract key material properties from this bonded silicon membrane layer. Details of the material property extraction methods and experiments are shown in Section 3.8.

3.6 Dry Release Method

An important feature for the wafer-bonded sealed cavity process is the ability to fabricate the mechanical parts using a completely dry release process as shown in Figure 3–8. A resist mask is used for device patterning followed by a deep Si plasma etch (~10–15μm) to pattern the mechanical structure. The sealed cavity has a partial vacuum and is etched at reduced pressure. Thus a differential pressure can exist across this mechanical layer which can cause it to fail catastrophically as the etch nears completion, particularly on very fragile structures. To eliminate this problem, a two-step approach is taken in the etching process.

A 1.1 μm-thick resist mask is used to pattern "vent holes", as shown in Figure 3–8(a), on the n-type mechanical layer. These vent holes range from 3μm×3μm to 10μm×10μm, and they are located in remote areas far from the devices. A 5 μm-deep Si plasma etch is used to pattern the vent holes. A 2 μm-thick resist mask is then used for device patterning followed by the 10–15 μm-deep Si etch (Figure 3–8(c)-(d)). Both of

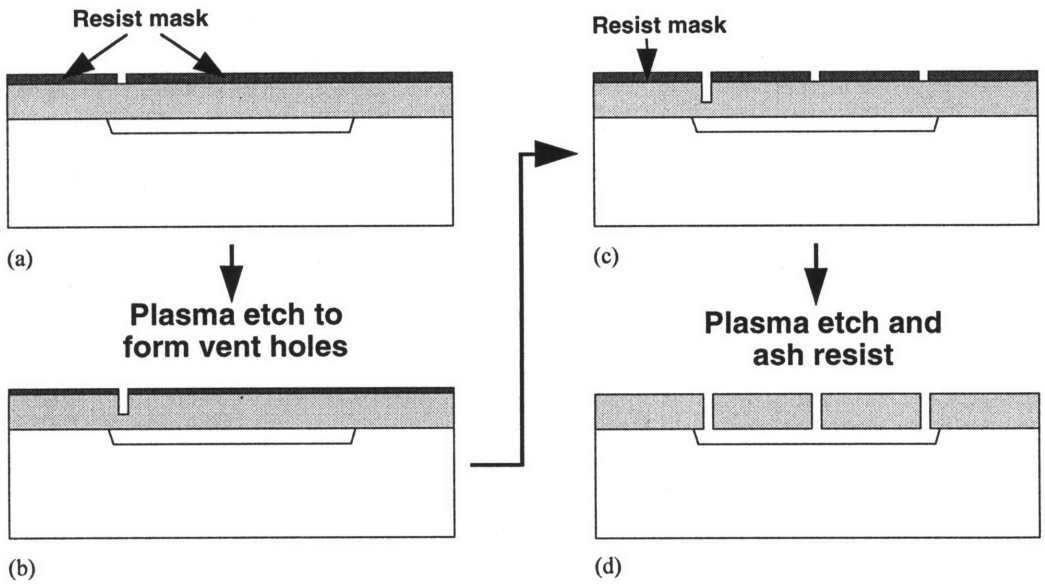


Figure 3–8: Two-step dry release process.

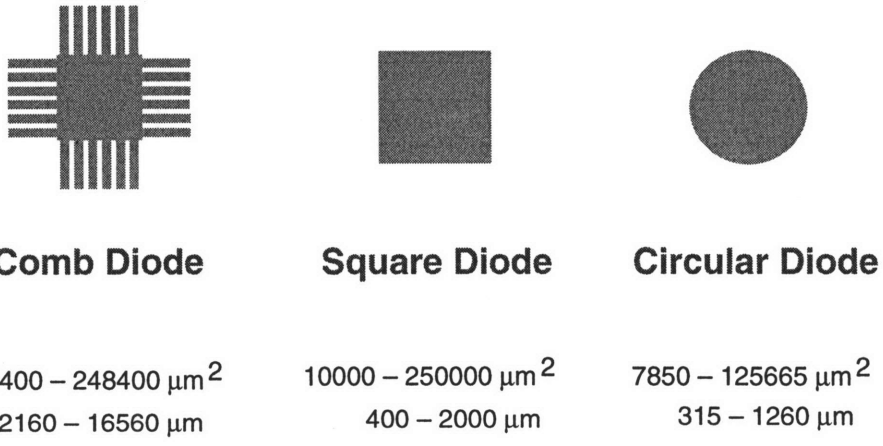


Figure 3–9: Three types of diode test structures.

these etch steps are based on an SF_6:CCl_4 chemistry which gives an average sidewall angle of between 83° to 87°, an average Si etch rate of 71.4Å/s, and a Si:resist selectivity between 7:1 to 12.5:1. The vent holes are etched through first during the deep Si etch thus balancing the pressure difference across the membrane and preventing its potential rupture. A "destructive" test was performed on all wafers fabricated using this "vent hole" etch process; mechanical devices (e.g., accelerometers, laterally-driven resonators, and M-Test structures) were intentionally pulled out from the wafers so we may observe the surface underneath for any particulate or residue possibly caused by the "blow-out" of the vent holes when they were finally etched through in the plasma etching chamber. Under careful inspection with a scanning electron microscope (SEM), no residue was found under the mechanical devices. We believe that the small size of the vent holes, typically 3μm×3μm, makes the membrane resistant to shattering.

After the deep Si etch, the resist mask can easily be removed with an oxygen plasma. Since this is a completely dry process, no adhesion problems are observed, and we routinely fabricate suspended plates as large as 1mm×1mm to serve as tuning fork tines and accelerometer proof masses.

3.7 Diode Characterization

1. Diodes Formed with As-bonded Junction Isolation Scheme

In order to evaluate the effectiveness of the junction-isolation scheme used in this study, the characteristics of diodes formed between the n-type bonded layer and the p-type substrate were measured. A total of 64 diodes per die, with variations in junction areas

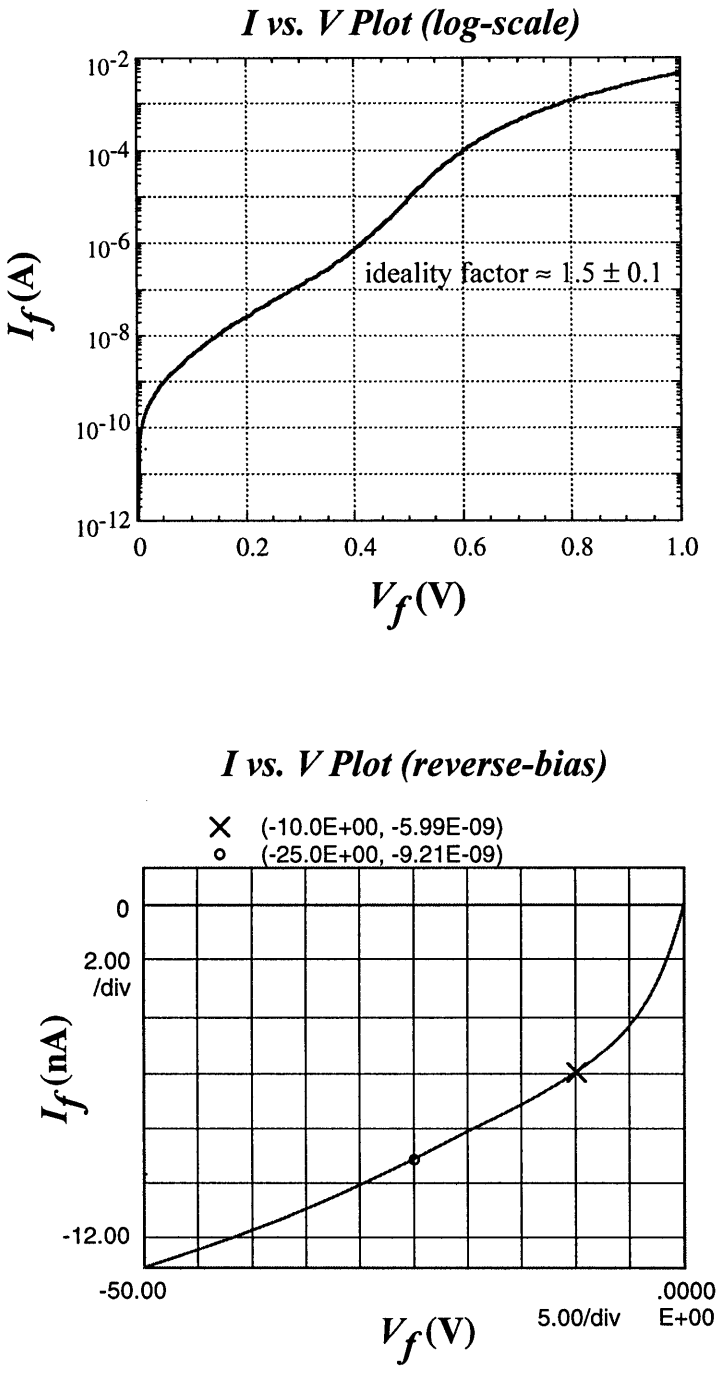
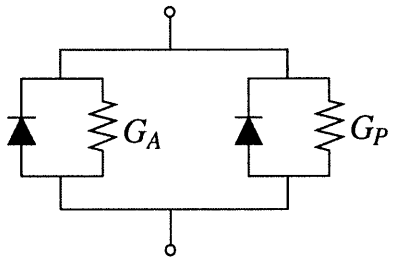


Figure 3–10: (a) Forward-bias & (b) reverse-bias characteristics of as-bonded junction diodes.

and perimeters, were fabricated. On average, more than 180 diodes with different geometry as shown in Figure 3–9 were tested per wafer. Figure 3–10(a) illustrates a typical forward-bias characteristic while Figure 3–10(b) is a typical reverse-bias characteristic. For the forward-bias I-V plot shown in Figure 3–10(a), the linear region lies between 0.45V and 0.55V. Just below 0.45V, it is the space charge recombination region, and just above 0.55V, we have the series resistance region. For the 11μm n-epi samples, the ideality factor is about 1.5 for the linear region, the average breakdown voltage is greater than 60V with a typical current density of 0.016pA/μm^2 at 1V reverse-bias and 0.082pA/μm^2 at 25V reverse-bias. With an average operating voltage of ±2.5V for our capacitive microaccelerometer, this level of reverse-bias leakage current is relatively high but acceptable. The success of this junction- isolation scheme enables us to fully utilize silicon-silicon bonding yet obtain adequate electrical isolation of the mechanical parts from the substrate. Note that all of the diodes tested exhibited *soft breakdown* and leakage currents much greater than conventional diodes produced on CMOS processes. Two contributors to this higher leakage current are the imperfections in the silicon-silicon interface, and the dangling bonds located on the unpassivated diode pedestal surfaces. Furthermore, the reverse-bias current is initially exponential with respect to the applied voltage and appears to increase nearly linearly across the entire voltage range (0–100V reverse-bias). The extracted incremental resistance under reverse bias is between 1.25GΩ and 6.25GΩ.

A model was proposed for the current of the diodes as a function of applied bias, junction area, and junction perimeter. The semi-empirical model is shown in Figure 3–11. This model separates the current into an area component and a perimeter component.



$$\boxed{I = J_A \cdot A + G_A \cdot V + J_P \cdot P + G_P \cdot V}$$

$$J_A = j_A(e^{qV/nkT} - 1) \qquad G_A = g_A \cdot A \qquad J_P = j_P(e^{qV/nkT} - 1) \qquad G_P = g_P \cdot P$$

where A = junction area P = junction perimeter

Figure 3–11: Semi-empirical diode model proposed to characterize the as-bonded junction isolation scheme. The current of the diodes is modeled as a function of applied bias, junction area, and junction perimeter. This model separates the current into an area component (J_A) and a perimeter component (J_P).

$$I = J_A \cdot A + G_A \cdot V + J_P \cdot P + G_P \cdot V$$

$$\begin{aligned} \text{where } J_A &= j_A\left(e^{qV/nkT} - 1\right) \\ G_A &= g_A \cdot A \\ J_P &= j_P\left(e^{qV/nkT} - 1\right) \\ G_P &= g_P \cdot P \end{aligned} \tag{3.1}$$

and A = junction area
P = junction perimeter

Note that J_P has the units of current per length, and represents the current due to the dangling bonds on the diode pedestal surface. The area component, J_A, has the units of current per area, and it represents the current across the bonded interface. We may use the forward-bias characteristics to obtain the *ideality factor* (n), assuming $n_A = n_P$.

$$I_f \approx J_A \cdot A + J_P \cdot P = \left(j_A A + j_P P\right)e^{qV_f/nkT} \tag{3.2}$$

We can then use the reverse-bias characteristics to get j_A, j_P, g_A, and g_P.

$$\begin{aligned} I_r &\approx \left(j_A A + j_P P\right) + \left(g_A A + g_p P\right) \cdot V_r \quad \text{for } V_r >> \tfrac{nkT}{q} \\ &= \left[j_A + g_A V_r\right]A + \left[j_P + g_P V_r\right]P \end{aligned} \tag{3.3}$$

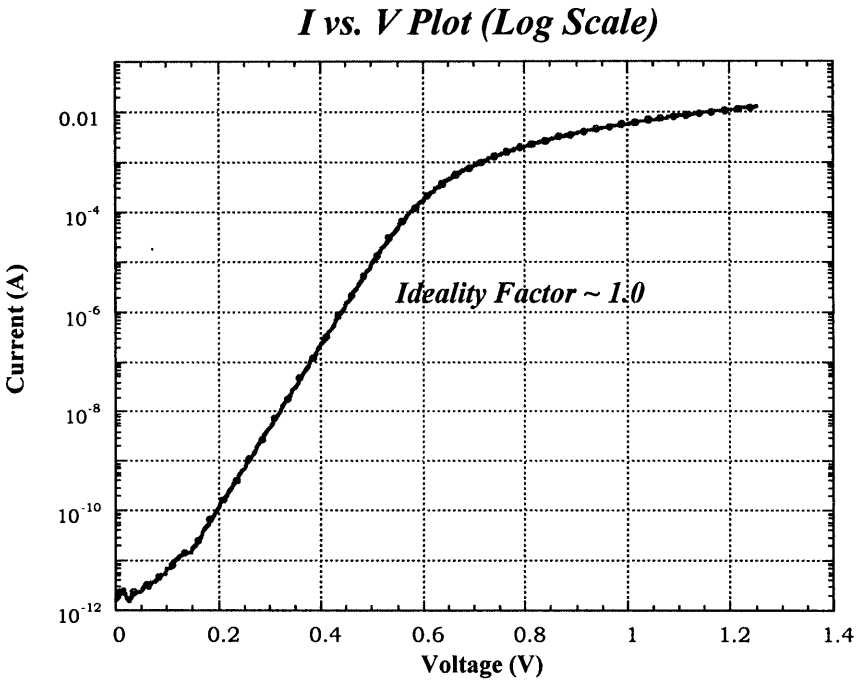
As we can see clearly from Figure 3–10, wafer-bonded diodes behaved quite differently than diodes produced in a standard CMOS process. The distinguishing features of the diodes are the bonded junction interfaces, and the pedestals upon which the n-type sides of the diodes sit. Both of these are likely sources of charge trapping, leakage paths, and other undesired behavior. Equations 3.2 and 3.3 attempt to include these features and quantify their effects. The four parameters, J_A, J_P, g_A, and g_P are found to be j_A = 40nA/cm^2, j_P = 2nA/cm, g_A = 0S/cm^2, and g_P = 4×10^{-10}S/cm. Furthermore, we have obtained G_P^{-1} (or R_P) = 1.25GΩ for a 500×500μm^2 square diode and G_P^{-1} (or R_P) = 6.25GΩ for a 100×100μm^2 square diode from our measurements. We conclude that nearly

all reverse-bias leakage current is due to the perimeter component, which represents the dangling bonds on the *un-passivated* diode pedestal surfaces. The inherent series resistance associated with these as-bonded p-n junction diodes was measured to be ≤ 100Ω and was not included in the semi-empirical model shown in Figure 3–11. Finally, we did not observe any noticeable difference between *hydrophilic* and *hydrophobic* diode samples.

2. Diodes Formed with Diffused Junction Isolation Scheme

A similar study was done to evaluate the effectiveness of the diffused junction approach. We again utilize diodes of various geometry described previously for this experiment. We have tested approximately 180 diodes (60 diodes per diode type) per wafer, and the representative results are shown in Figure 3–12. As we can see from the forward-bias characteristic shown in Figure 3–12(a), the ideality factor is exactly 1.00. For all fabricated diodes the ideality factor were measured to be in the range of 1.00–1.01. More important though is the reverse-bias characteristic shown in Figure 3–12(b). The diffused junction diodes behave like ideal diodes with an average breakdown voltage near -160V. Furthermore, the leakage current stays very small, approximately 1nA/cm^2 at 2.5V reverse-bias, across the entire voltage range until breakdown. In general, diodes with only thin densified LTO as passivation layer exhibit lower breakdown voltage than ones with thin SRO and LTO as passivation layer. Furthermore, there is no observable difference between *hydrophilic* and *hydrophobic* samples.

Diffused junction isolation appears to be the best junction isolation scheme that we have investigated so far. The near CMOS-grade diode characteristics exhibit an extremely low leakage current and high breakdown voltage providing a junction isolation scheme for fabricating the junction-isolated bottom electrode of the microaccelerometer described in Chapter 4.



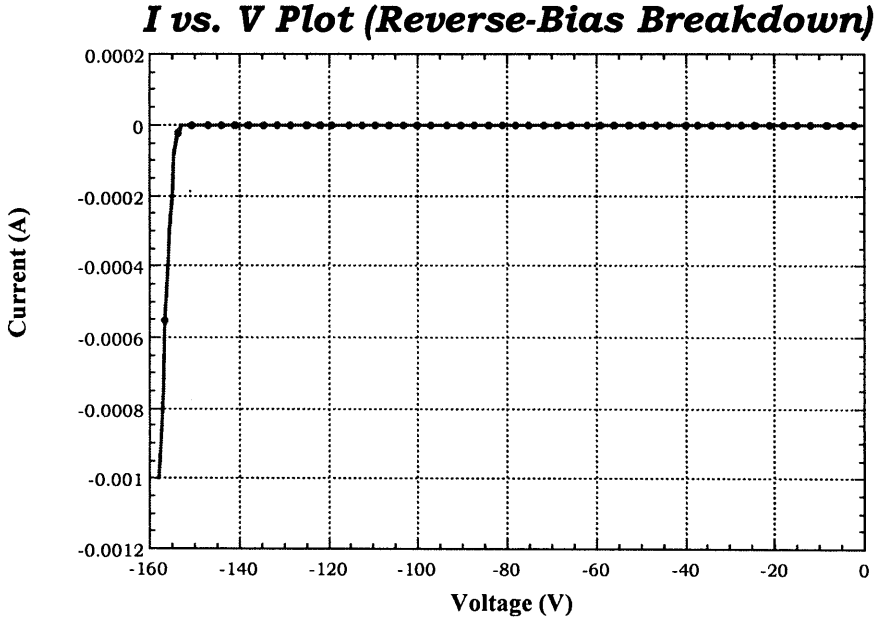


Figure 3–12: (a) Forward-bias & (b) reverse-bias characteristics for diffused junction diodes.

3.8 Material Property Extraction

3.8.1 Lateral Comb-Drive Resonator

Several lateral resonant structures were fabricated and tested to demonstrate the process and measure the material properties. These tuning-fork-gyroscope-like lateral resonators (illustrated in Figure 3–13) were driven to resonance by means of comb-drive. All three types of resonators have measured resonant frequencies within 5% of the FEM calculated values, as shown in Table 3.4, using published values for the modulus of single-crystal silicon (160–180GPa).

3.8.2 M-Test Structures

1. Electrostatic Pull-in Method

With the recent growth of micromachine processing technology for MEMS, there has developed a need for simple, accurate and standardized process monitoring and material property extraction capability (e.g. Young's modulus, plate modulus and residual stress) at the wafer-level. Integration of a microelectromechanical "drop-in" test pattern (or "M-Test") incorporating the electrostatic *pull-in* of standard test beams and diaphragms shows particular promise for realizing this goal. This idea is analogous to standard electrical MOSFET test structures (known as "E-Test") used for extraction of MOS device parameters where, in both cases, the intent is to measure fundamental electrical, mechanical or material properties *in-situ*. The overall goal of this section is to demonstrate

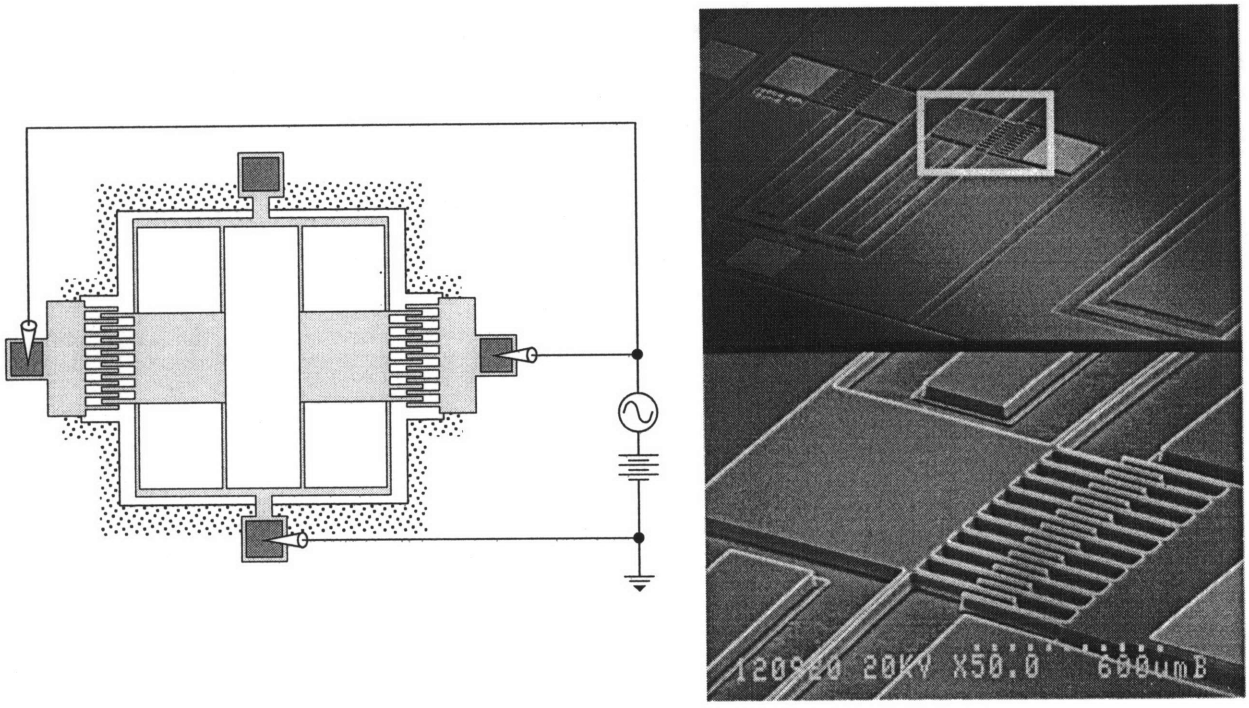


Figure 3–13: Lateral comb-drive resonator: (a) schematic and (b) SEM of the fabricated device.

Table 3.4

Device	Tine Size (μm^2)	Resonant Frequency (calculated)	Resonant Frequency (observed in vacuum)
Gyro Type 1	200 x 200	20 kHz	19,997.40 ± 0.05 Hz
Gyro Type 2	500 x 500	2 kHz	2047.50 ± 0.05 Hz
Gyro Type 3	1000 x 1000	2 kHz	1997.50 ± 0.05 Hz

Table 3.4: Lateral resonator experimental results (10 devices per type were measured)

the M-Test concept of integrated wafer-level material property monitoring for MEMS semiconductor processes based on the electrostatic pull-in of microelectromechanical test structures.

Electrostatic pull-in is a well-known sharp instability in the behavior of an elastically supported structure subjected to parallel-plate electrostatic actuation. Because the event is sharp, accurate measurements of the actuation voltage required to reach pull-in can be easily made at the wafer level using standard electrical test equipment and a microscope. The M-Test concept is based on an array of microelectromechanical test structures of varying dimensions. Three specific structures are used here: cantilever beams (CBEAM's), fixed-fixed beams (FFBEAM's), and clamped circular diaphragms (DIAPHRAGM's), all suspended above a fixed ground plane by a gap (see Figure 3–14). In each case, a voltage is applied to the upper movable conductor causing it to deflect downward towards the underlying fixed ground plane due to the electrostatic attraction. At a critical "pull-in" voltage, V_{PI}, the upper conductor becomes unstable and spontaneously collapses (or pulls-in) to the ground plane. The pull-in voltage is related to the test structure's geometry and intrinsic material properties. Therefore, the pull-in data provides a direct indication of the uniformity and repeatability of a given process. When supplemented with models and geometric metrology data, the variation of pull-in voltage with device geometry can also be used to extract material properties.

2. Experimental Procedure

The two-part M-Test experimental test procedure is outlined in Figure 3–15. The first part is the measurement of pull-in and the extraction of S and B parameters, which are the fundamental quantitative measures of process uniformity. The second part is the extraction of material properties from these S and B parameters using metrology data. Comprehensive description of the theoretical models and experimental procedures were presented in [48] and will not be repeated here. However, actual pull-in experiment and material property extraction data are described in this section for completeness.

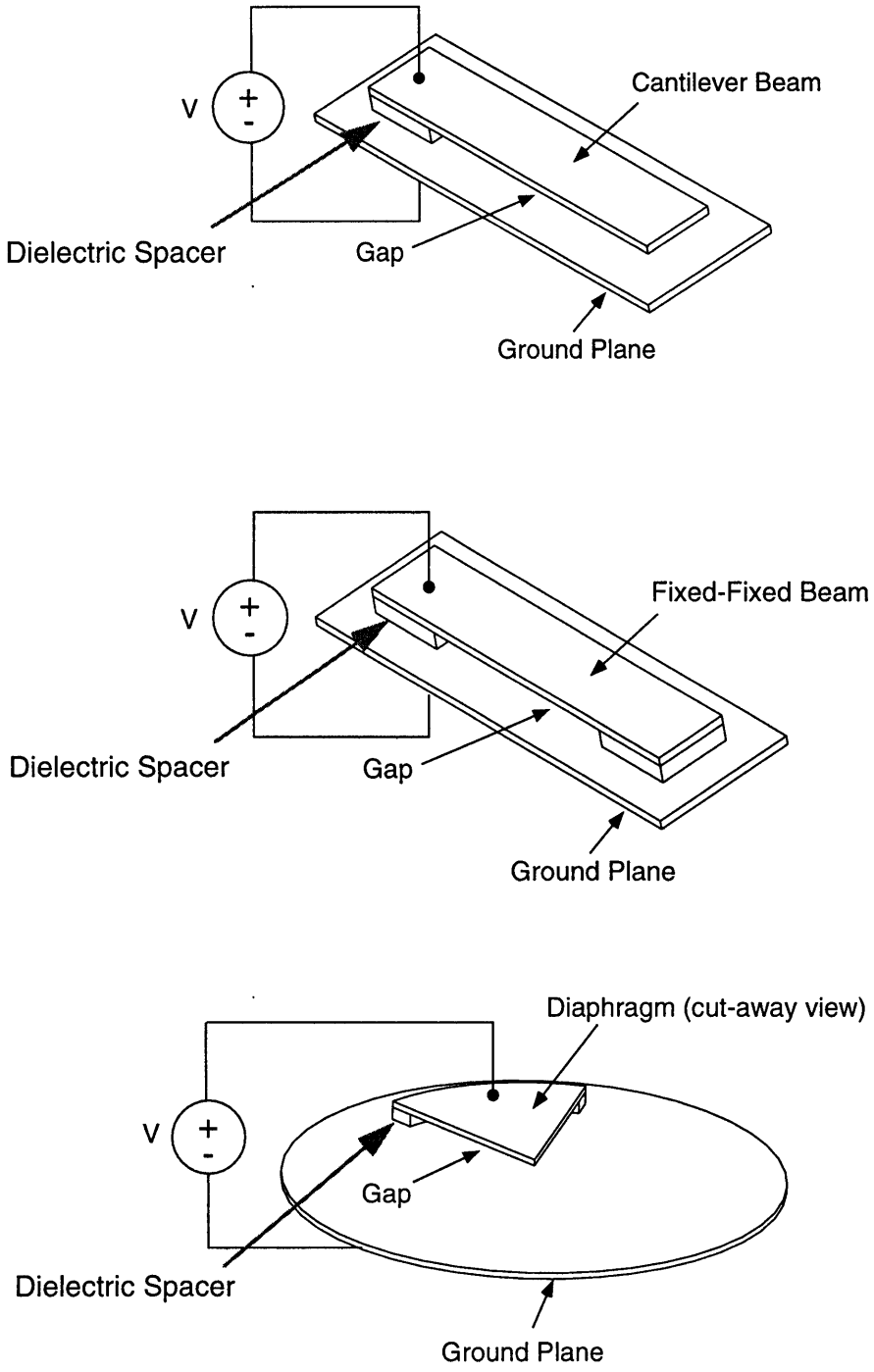


Figure 3–14: Three M-Test pull-in test structures (courtesy of P. Osterberg).

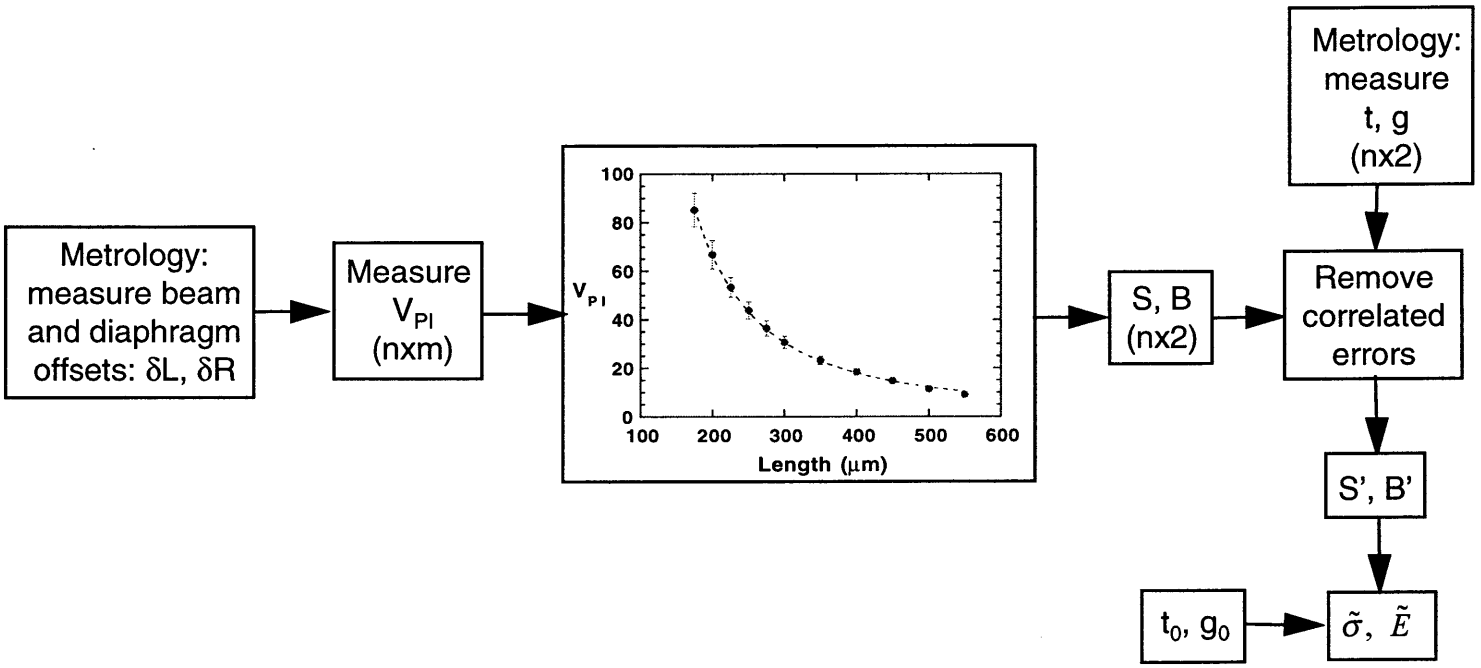
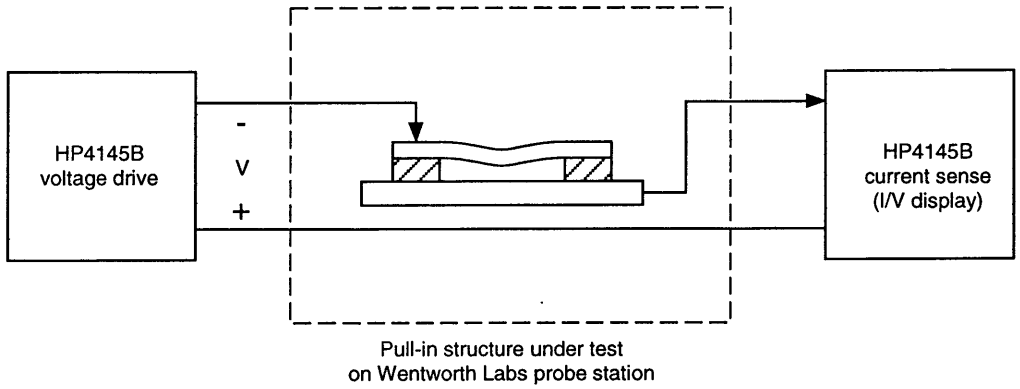


Figure 3–15: M-Test experimental test procedure block diagram (two parts) where n = number of die tested per wafer and m = number of pull-in measurements per die (courtesy of P. Osterberg).

a) Pull-In Measurements: An experimental set-up for structures which make ohmic contact at pull-in is shown in Figure 3–16. If the structures have an insulating film between the two electrodes, ohmic contact cannot be used, and either direct visual observation or C-V measurements are needed to detect pull-in. For the devices studied here, V_{PI} is measured on a Wentworth Labs probe station with a Hewlett-Packard HP4145B Semiconductor Parametric Analyzer configured in a "force-voltage/measure-current" mode. The HP4145B is programmed to slowly ramp the voltage on each test structure at 1 volt/second over a specified voltage range until pull-in is detected on the HP4145B I/V screen output interface as a sudden step in the current (see typical data in Figure 3–16). For the particular beam and diaphragm test structures used in this work, the upper movable conductor is n-type material while the underlying fixed ground plane is p-type. The measurement must be made with the moving conductor negative so that accumulation layers form on the semiconductor surfaces. If depletion of either conductor occurs, then a correction to the measured V_{PI} would be needed to account for the field penetration into the semiconductor. Because the onset of pull-in is very sharp, the accuracy of the measurement is determined by the voltage ramp step increment, which was 100mV or less in our experiments. The ramp speed of 1 volt/second is slow enough to insure no dynamic effects during the bending of the test structures.

b) S and B Parameter Extraction: The next step is to vary S and B to fit the V_{PI} *vs.* L (or R) data for each test structure type on each die to the closed-form model [48] using the L and R drawn mask dimensions modified by the measured offsets. We have used the non-linear least squares curve fit for this purpose. An example V_{PI} *vs.* L plot and corresponding curve fit is shown in Figure 3–17 for two sets of FFBEAM's, one oriented along the [011] direction in a <100> plane of single crystal silicon, the other oriented along the [010] direction.

c) Material Property Extraction: To extract material properties from the S and B parameters, additional metrology is required: (1) beam and diaphragm thicknesses, t, preferably measured on each die; and (2) spacer thickness or undeformed gap, g_0, also



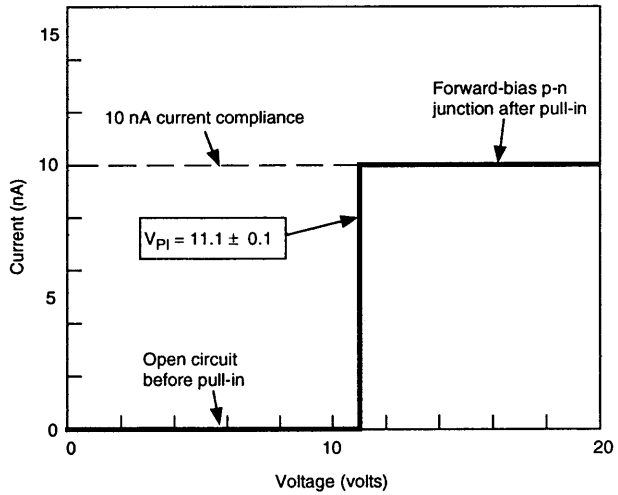


Figure 3–16: Pull-in test experimental setup.

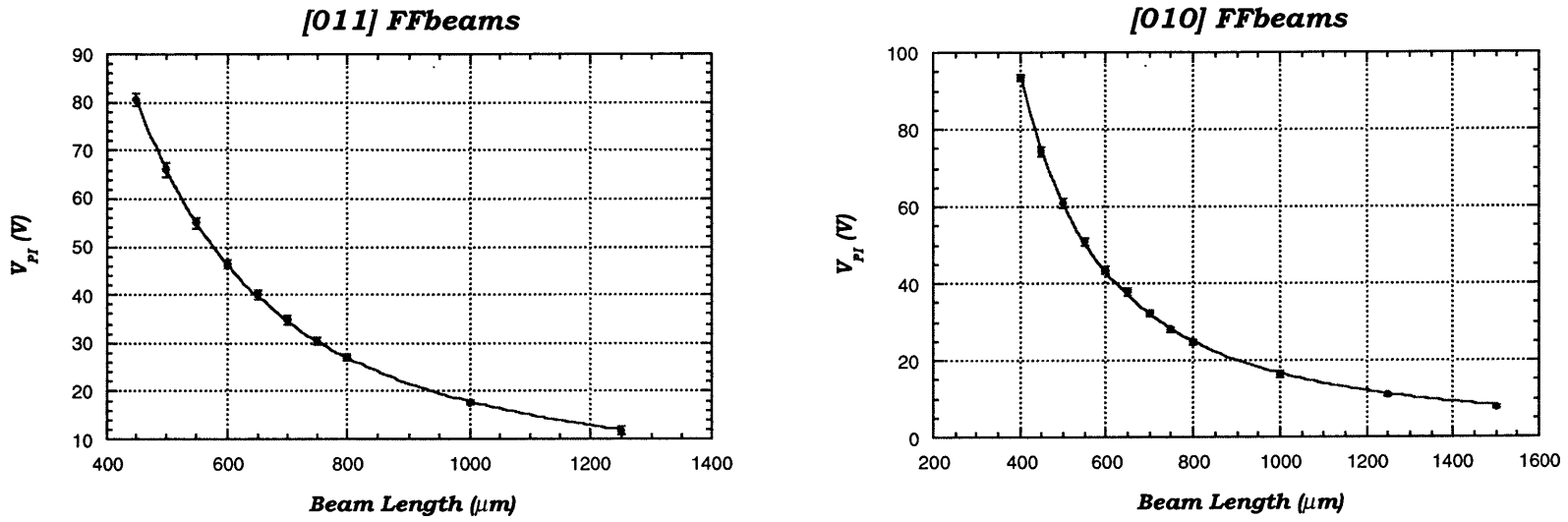


Figure 3–17: V_{PI} *vs.* L plots for FFbeams along [011] and [010] directions.

preferably measured on each die. These quantities are needed, first, to remove systematic errors from the S and B parameters and, second, for extracting the final material properties from these error-corrected values.

In this work, thickness measurements were made on each die using a Dektak II Surface Profilometer, providing accuracy of ±0.01μm. The oxide spacer thickness was measured ellipsometrically, and should correspond to the gap dimension for an oxide-isolated silicon-wafer-bonded process.

Because S and B depend on thickness and gap, some of the observed variation in these quantities can be attributed directly to die-to-die variations in geometry. To eliminate these correlated errors, we plot the individual S and B parameter values *vs.* thickness for each die (and *vs.* gap, if available for each die) and determine if any correlation exists. We then scale the raw S and B values to the values they would have if their thickness (and gap) were exactly the global mean thickness t_0 (and the global mean gap g_0), and compute the average of the scaled parameters, now referred to as S' and B'.

Using the S' and B' mean values (S'_0 and B'_0), and the global mean thickness (t_0) and gap (g_0), the effective Young's modulus is calculated from $\tilde{E} = B'_0/(t_0^3 g_0^3)$ and the effective residual stress is calculated from $\tilde{\sigma} = S'_0/(t_0 g_0^3)$. This completes the M-Test procedure.

3. Experimental Results

A specific M-Test mask set was designed for use with the dielectrically isolated wafer-bonded process [48, 60]. Fabrication processes have been presented previously. Complete experimental results from four different wafer samples will be discussed in the following section.

a) M-Test Mask Set: The test structures described earlier were incorporated into a mask set called M-Test, designed for the MIT dielectrically isolated wafer-bonded process [60]. M-Test is an array of three test chips alternating across a full wafer, one each for CBEAM's, FFBEAM's, and DIAPHRAGM's. The mask layout for the FFBEAM's

chip is shown in Figure 3–18. Notice that the beam lengths, widths and crystal orientations are varied. When built in a <100> oriented wafer-bonded process, the two sets of beams are oriented along [011] and [010]. The full 4" wafer contains 20 dies each from CBEAM's, FFBEAM's, and DIAPHRAGM's for a total of 60 dies.

b) Sample Description: Four sample wafers were fabricated for this study. After careful evaluation of the previously described process enhancements, we have chosen the best wafer thinning method and the most effective isolation scheme as the base to fabricate the M-Test structures shown here, and a microaccelerometer as the other demonstration device (details shown in Chapter 4) for the integrated MEMS-CMOS process which will be described in detail in the next section. Most importantly, CMOS unit step experiments are performed on the material property test structures to evaluate the unit process sensitivity of the proposed integrated MEMS-CMOS process.

CMOS unit step experiments are important because they ensure a 100% compatibility of the desired sensor processes with the standard MIT baseline twin-well, 1.50μm, single metal CMOS process. This confirmation is vital to the success of MIT's MEMS-CMOS integrated sensor projects. The following CMOS unit step process will be used to evaluate such compatibility, the process is also shown graphically in Figure 3–19:

(i) Well Formation: This unit process experiment consists of SRO, LPCVD nitride, n-well implant, n-well cover oxidation, and well-drive processes. It is important to carefully evaluate this unit step process because mechanical devices such as pressure sensors and accelerometers are formed in the n-well region. The long Dt step is the well-drive step since the well-drive occurs at 1150°C for about 16 hours. The material properties and the surface quality of the 10 μm-thick n-epi layer after this experiment are also important when evaluating the finished test structures. Sample wafer #1 was taken out of the CMOS baseline process at this point and followed by M-Test structure back-end processes.

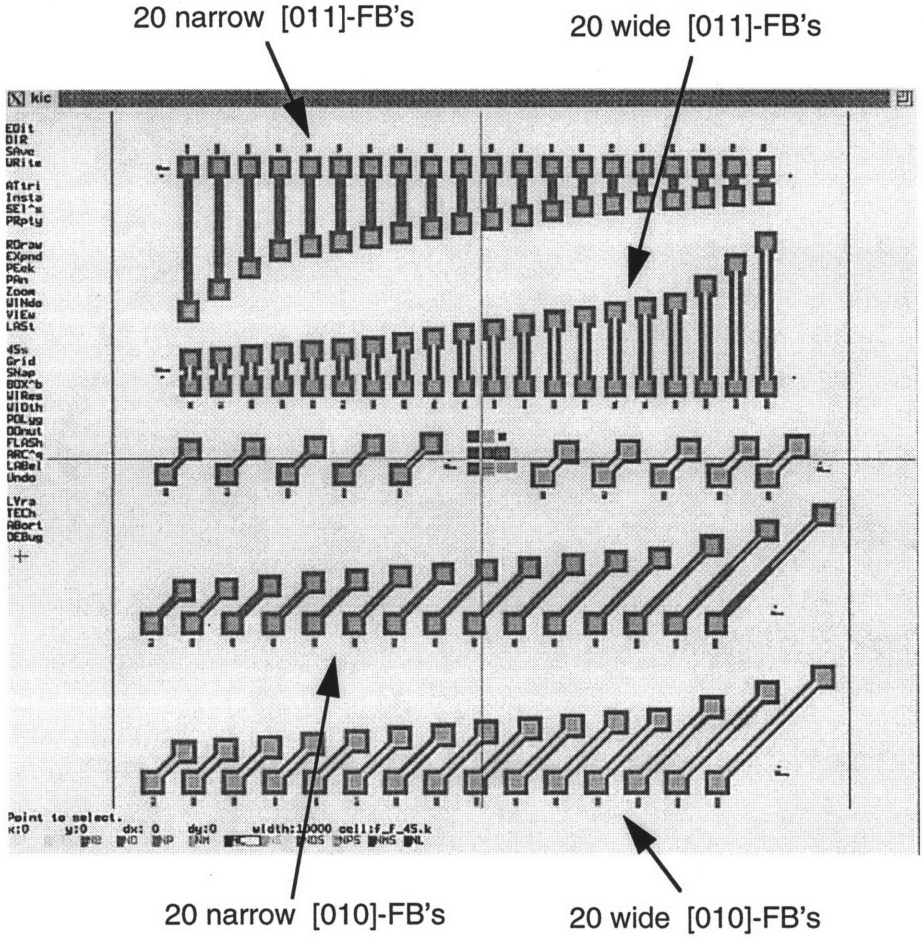


Figure 3–18: Mask layout of the FFbeam chip.

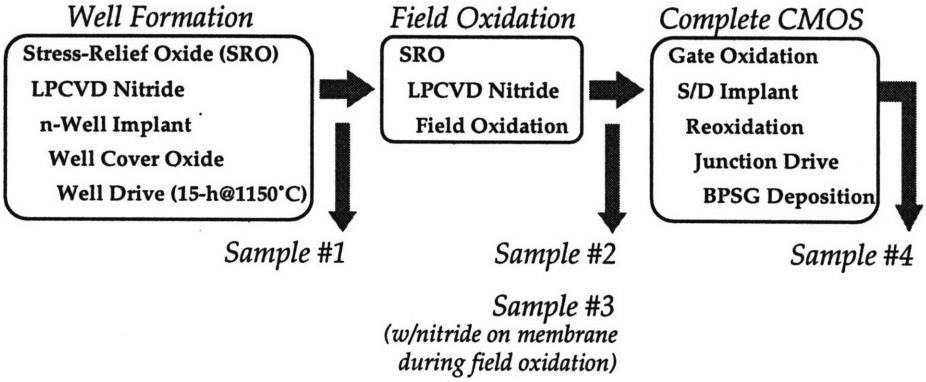


Figure 3–19: CMOS unit-step process sample wafer description.

(ii) Field Oxidation: This experiment consists of SRO, LPCVD nitride, and field oxidation. The field oxidation occurs at 950°C for about 4.5 hours. We had a split in this experiment; sample wafer #2 received field oxidation on the membranes directly on top of the sealed cavities (no silicon nitride on the device region), and sample wafer #3 did not have oxide grown on the sealed cavity region (silicon nitride stays on the device region).
(iii) Complete CMOS Process: After field oxidation, sample wafer #4 went through the rest of the CMOS baseline processes including gate oxidation, source/drain implant, reoxidation, junction drive, and BPSG deposition. This completes the CMOS baseline unit step experiments. Note that all grown or deposited oxide and nitride films were removed before the backend M-Test fabrication process began.

c) Results: The FFBEAM's results (both in the [011] and [010] directions) and the DIAPHRAGM's results are shown in Table 3.5 and Table 3.6 respectively. For every sample wafer, approximately 240 M-Test structures were tested (approximately 80 devices for each class of test structures) and extracted the material properties from the pull-in data. Please note that we have omitted a lengthy discussion regarding the M-Test structure design strategy in this paper; however, the comprehensive discussion can be found in [48]. In short, with our designed M-Test structure dimensions, using the equations presented in Table 3.7, we can solve for the resulting $\tilde{E}_{min}$ and $\tilde{\sigma}_{min}$, minimum resolvable bending and stress values. For FFBEAM's, we get $\tilde{E}_{min}$= 1GPa and $\tilde{\sigma}_{min}$= 30MPa. For DIAPHRAGM's, we get $\tilde{E}_{min}$= 1GPa and $\tilde{\sigma}_{min}$= 18MPa. In both cases, the minimum resolvable bending value is well below the expected value (170GPa), indicating that this value can be extracted with high accuracy. However, the minimum resolvable stress value is two to three times larger than our expected value (1 to 10MPa), indicating that this parameter is far from the threshold of resolution and therefore its accuracy will be very low. This is a bending-dominated design for the expected material properties, which was appropriate in this case, because the expected residual stress was quite small.

The term *accuracy* and *precision* are often used to distinguish between *systematic* and *random* errors. If a measurement has small systematic errors, we say that it has high

Table 3.5

Unit step	FFBeams [011] Lit. E=170GPa		FFBeams [010] Lit. E=141GPa	
	E (GPa)	σ (MPa)	E (GPa)	σ (MPa)
Pre-CMOS	170±2	9±1	141±2	9±1
Sample #1	168±2	9±1	139±2	10±1
Sample #2	168±3	9±2	141±2	10±1
Sample #3	169±5	9±2	138±2	10±2
Sample #4	167±6	10±3	—	—

Table 3.5: CMOS unit step experiment results: summary of modulus (E) and residual stress (σ). 200 devices tested per data set.

Table 3.6

Unit step	Diaphragms Lit. E=155GPa	
	E (GPa)	σ (MPa)
Pre-CMOS	155±2	9±1
Sample #1	153±3	9±1
Sample #2	153±2	9±1
Sample #3	155±2	9±2
Sample #4	—	—

Table 3.6: CMOS unit step experiment results: for diaphragms. 200 devices tested per data set.

accuracy; if small random errors, we say it has high precision [84]. In our case, we can say that we *expect* to see the extracted Young's modulus values have both high accuracy and high precision; on the other hand, the extracted residual stress values would have low accuracy but still high precision due to the highly precise pull-in method employed here. It is important to comment on the extracted material properties shown in Tables 3.5 and 3.6. The extracted Young's modulus values are both *accurate* and *precise* since these measurements have small *systematic* errors and small *random* errors respectively. However, the extracted residual stress values are not accurate yet precise since our measurements have inherently poor accuracy (or large systematic errors as indicated previously) yet still exhibit small random errors due to the precise pull-in measurement method employed and careful measurements made by the author.

Table 3.7

Expressions for: (1) the "center-design" dimension, and (2) the minimum resolvable effective Young's modulus and residual stress for both the FFBEAM and DIAPHRAGM test structures.

	FFBEAM	DIAPHRAGM
L_{center} or R_{center}	$\sqrt{\frac{4\tilde{E}t^2}{\tilde{\sigma}}}$	$\sqrt{\frac{4\tilde{E}t^2}{3\tilde{\sigma}}}$
$\tilde{E}_{\min}$	$\frac{\tilde{\sigma}L_{\min}^2}{4t^2}$	$\frac{3\tilde{\sigma}R_{\min}^2}{4t^2}$
$\tilde{\sigma}_{\min}$	$\frac{4\tilde{E}t^2}{L_{\max}^2}$	$\frac{4\tilde{E}t^2}{3R_{\max}^2}$

where t = thickness of the beam or diaphragm
L_{min} = minimum beam length
L_{max} = maximum beam length
R_{min} = minimum diaphragm radius
R_{max} = maximum diaphragm radius

(after *Ref.* 48)

It is important to note that the *simple* pinwheel and *folded* pinwheel designs used in this research effectively attenuate external stresses and strains; thus, the extracted 10MPa residual stress would have minimal effect (stress stiffening effect) on the microaccelerometer sensitivity [31–32]. However, if a *straight* tether design was employed, this 10MPa residual tensile stress might reduce the accelerometer sensitivity significantly. In order to quantify this effect, an analytical model was borrowed from [85] and modified for our accelerometers as shown in Figure 3–20. The straight-tether accelerometer has a surface area of A, and it is loaded by a 1g force which causes it to deflect a vertical distance δ. The surface area is the product of L and W, the length and the width of the proof mass. The tethers are each of length l, width w, and thickness t. According to the model, the sensitivity (in μm/g) of a straight-tether microaccelerometer can be calculated:

$$\frac{\delta}{g} = \frac{W \cdot L \cdot l \cdot d_{Si}}{4 \cdot \sigma \cdot w \cdot (9.81)} \left[1 + 2\frac{w \cdot l}{W \cdot L}\right] \left\{1 - \frac{\tanh\left(\frac{u}{2}\right)}{\frac{u}{2}}\right\} \tag{3.4}$$

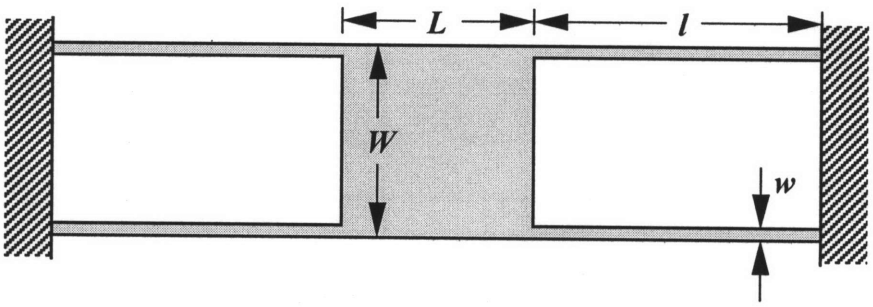
$$\text{where} \quad u = l\left[\frac{S}{EI}\right]^{\frac{1}{2}}$$

$$I = \frac{1}{12} wt^3$$

$$S = \sigma t w$$

where I is the bending moment of inertia of the tether, S is the effective axial tension load representing the effect of the tensile residual stress, σ is the residual stress of the silicon mechanical layer, and d_{Si} is the silicon mass density. A plot of the accelerometer sensitivity as a function of the silicon residual stress is shown in Figure 3–21 with the dimensions, $W = L = 510\mu m$, $w = 10\mu m$, $l = 1mm$, $t = 10\mu m$, and $E = 170GPa$. Since the residual stress extracted from the pull-in data is approximately 10MPa, it is important to recognize the role that this stress plays in the mechanical response for a straight-tether

Top View



Cross Section

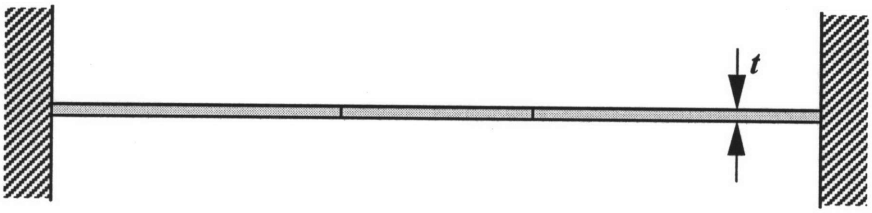


Figure 3–20: Straight-tether accelerometer design.

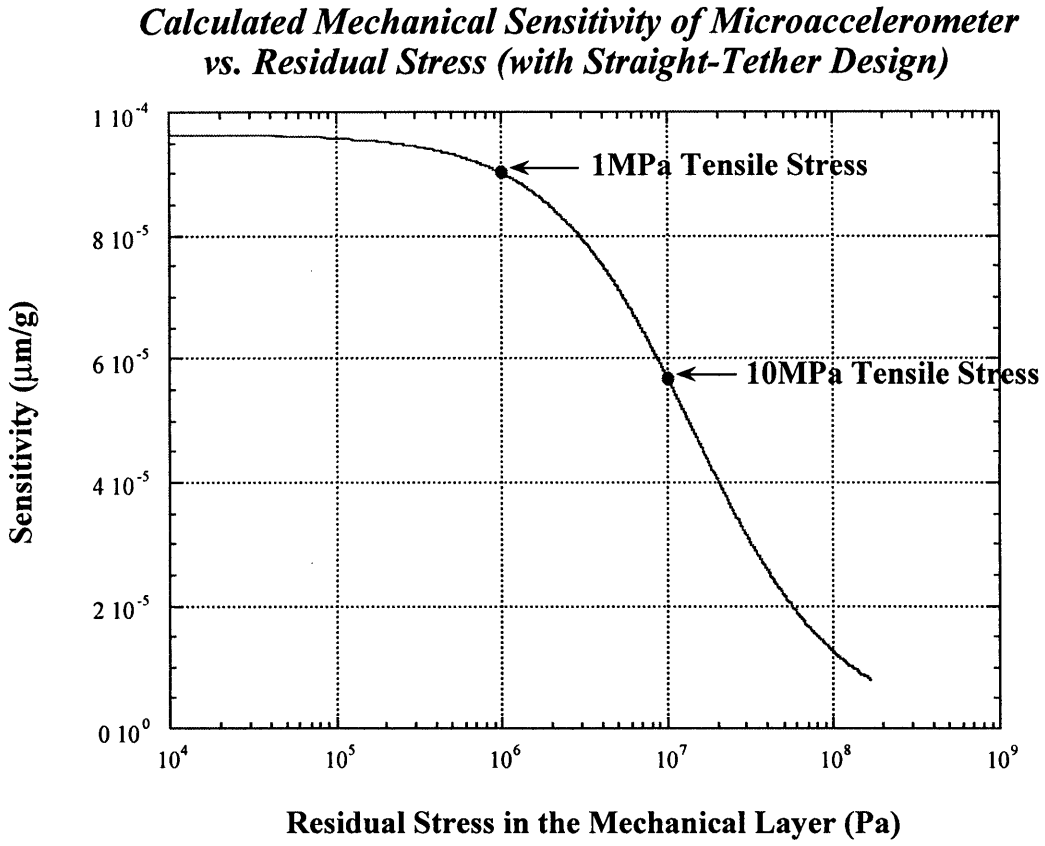


Figure 3–21: Calculated mechanical sensitivity of straight-tether accelerometer.

accelerometer design. The expected sensitivity for this value of residual stress is 0.057nm/g while the zero-stress expected sensitivity is 0.097nm/g.

3.9 Summary

Detailed description of the wafer-bonded sealed cavity process was presented. A summary of the integrated MEMS-CMOS process flow was presented next. Two specific process enhancements, electrical isolation of mechanical structure from the substrate, and dry release of the mechanical structure, were fully disclosed. Diodes formed with junction isolation and dry release process were fully characterized and the electrical property of the bonded interface was investigated. Successful fabrication of lateral comb-drive resonators and M-Test structures provided important information on material properties associated with the bonded silicon layer, which in turn complete the MEMS-CMOS process verification.

Chapter 4
Device Fabrication

4.1 Overview

This chapter presents the microaccelerometer fabrication in depth. The chapter begins by showing that the microaccelerometer fabrication process is a "sealed cavity process" and therefore lends itself to easy integration with a standard IC process as described in Chapter 3. The rest of this chapter discusses the actual fabrication process itself, with the aid of schematic cross-section drawings. At each stage the following three aspects of the process are presented: i) the description of that step; ii) process development issues; iii) any other issues associated with process optimization.

An objective of this thesis was to exploit the enhanced capabilities offered by *wafer bonding* and the associated *front-end micromachining* and *back-end micromachining* techniques to create a process flow to fabricate microaccelerometers, which could eventually be practically implemented in a production environment. With

this self-insisted constraint in mind, we specifically avoided fabrication process flows, or designs of microaccelerometer structures which involved the *aligned bonding* of two or more patterned wafers (i.e., when patterned features in one wafer must be spatially aligned to the patterned features of another wafer with tolerances of < 100μm). While aligned wafer bonding has proven to be feasible and is now available in several fabrication facilities including MIT's Technology Research Laboratory (TRL), it was not employed in this particular fabrication process. We have instead focused our attention on using *unaligned* wafer bonding in conjunction with IC standard fabrication steps such as ion implantation and thermal oxidation implemented using standard fabrication equipment available in MIT's Integrated Circuit Laboratory (ICL) and on understanding and using the thermocompression bond (between a layer of metal on the silicon substrate and a complementary layer on a Pyrex wafer) as an additional technology for achieving our goals. Although wafer bonding and other related fabrication techniques used in our process flow (such as electrochemical etch-stop and thermocompression bonding) are not considered traditional or standard integrated circuit fabrication technologies, products manufactured by microsensor companies such as Lucas NovaSensor and Honeywell support the contention that wafer bonding and electrochemical etch-stop can be practically implemented in a production environment.

Two device fabrication process flows are shown in this chapter: one is for the junction-isolated, top-and-bottom electrode accelerometer designed to be stitch-bonded with Ashburn's processing circuit chip (*Hybrid-Accelerometer Process Flow* shown in Section 4.3), and the other is the dielectrically isolated accelerometer with off-chip detection circuit (*Discrete Accelerometer Process Flow* shown in Section 4.4). The process flows are similar yet with subtle differences. Careful readers should find the processing details useful when attempting to duplicate those accelerometers in their own laboratories. The chapter ends by mentioning two processing issues that led to significant yield problems and proposes how these issues may be resolved in future work. Mask layout designs for both accelerometer designs are shown in Appendix A. A detailed

process traveler which lists MIT specific information (such as lab used, equipment used, etc.) is included in Appendix B.

4.2 Silicon Wafer Bonding

Sensors and Actuators can be manufactured using a silicon-to-silicon direct wafer bonding or a sealed cavity process. In this section we present a brief description of the wafer-bonding process performed at MIT's TRL. An excellent overview of wafer bonding can be found in [3, 57], A good review of the application of the wafer-bonding technology for the fabrication for micromechanical devices can be found in [3, 66–67].

4.2.1 The Bonding Process

At MIT's TRL, silicon wafer bonding process begins when the mirror-polished surfaces of a pair of silicon wafers are contacted together in a particle-free environment immediately after a standard RCA treatment ($NH_4OH:H_2O_2:H_2O$ [1:1:5] and $HCl:H_2O_2:H_2O$ [1:1:6]) to form *hydrophilic* surfaces. This hydration step creates a high density of OH groups which attach themselves to the dangling bonds at the silicon surface. The hydrated surfaces are then brought into proximity and pressed together. Once contacted, the wafers exhibit an electrostatic attraction which holds the wafers together. This initial room-temperature bond is further strengthened by post-contact high

temperature annealing. Bonded wafer pairs are typically annealed in a furnace in a nitrogen or dry/wet oxidation ambient at temperatures ≥ 1000°C. Following this anneal the wafers cannot be separated without fracturing the silicon substrates, and bond strength measurements indicate that for temperatures ≥ 1100°C, the strength of the inter-wafer bond approaches the fracture strength of bulk silicon. Bonding is possible not only between bare silicon and silicon (Si-Si), but can also be achieved between Si-SiO_2, SiO_2-SiO_2, Si-Si_3N_4, and SiO_2-Si_3N_4. The key parameters for achieving good bonding on a routine base are that the two surfaces must be free of any particles, defects, or contaminants (organic or inorganic), and the surfaces must be microscopically smooth and flat.

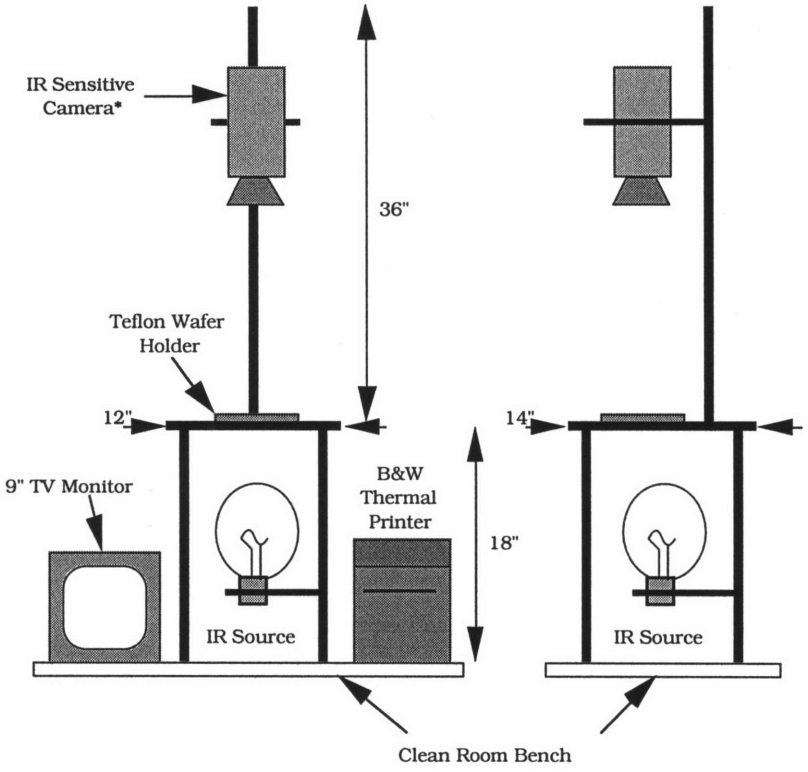
Silicon wafer bonding is useful for creating electronic or micromechanical devices by further augmenting the basic bonding process. For the creation of micromechanical devices, cavities or trenches may be etched into the handle wafer before the device wafer is bonded. Repeated bond, thin, polish, and etch steps have allowed sensor designers to fabricate very complex laminated silicon structures. But, the process step critical to fully exploiting this technology for the creation of either electronic or micromechanical devices is the technology used to carry out controlled thinning and etching.

4.2.2 Bond Inspection

Intimate contact across the entire surface between a pair of wafers undergoing bonding is essential to the complete success of the bonding process. In order to get a good bond, both wafer surfaces must be meticulously clean and free of defects, microscopically smooth, and flat. If two wafers which do not meet these criteria are brought together after hydration, then small to moderately large local regions where the silicon surfaces do not

physical contact, and consequently do not achieve bonding, can result. These unbonded regions are generally referred to as *voids.* Voids can be caused by any of the aforementioned imperfections, but the most common source of voids is particles. If particles as small as 0.5μm are present on the surface of either wafer, then contact between surfaces can be inhibited over a region of several millimeters [31]. After contact, but before thermal annealing, bonded wafer pairs can usually be separated by re-immersing the wafers into DI water until they separate. After they separate, these wafers can, on occasion, be re-cleaned, re-hydrated, and re-contacted. Significant time and cost is often invested in the fabrication of the device and/or handle wafer before the room-temperature bonding step, if not for the reversibility of the bonding process after room-temperature contact, this investment might otherwise be lost due to bad bonding caused by the presence of one or two particles on the surface of the wafer at the time of contacting. Monitoring the quality of the bonding process is therefore of critical importance.

There are a number of techniques available for inspecting bonded wafers for voids before and after annealing, including x-ray imaging, ultrasonic imaging, and infrared imaging. Both x-ray and ultrasonic imaging offer higher resolution than infrared imaging, yet both are expensive and time consuming. Infrared imaging offers the best compromise between expense, speed, and ease of use and implementation. However, the resolution for an infrared system is limited to void diameters of about 1mm. A very simple, but effective infrared void inspection system was constructed by our group as shown in Figure 4–1. The system consists of a simple black-and-white CCD camera, a visible light filter, an infrared source (a common incandescent light), and a video monitor. Voids usually appear as dark rings or splotches, while good bond regions are usually characterized by bright, uniformly illuminated regions (see Figure 4–2). The IR (infrared) inspection system also allows one to easily image patterned structures such as cavities, trenches, and even heavily diffused regions.



*Note: the IR sensitive camera consists of a standard B&W CCD camera with the IR cut filter removed. A 2" silicon wafer is used as the IR sensitive lens for the setup.

Figure 4–1: Schematic of an infrared void inspection system. Voids are imaged on the video monitor using a black-and-white video camera and can be captured in hardcopy using the thermal video image printer.

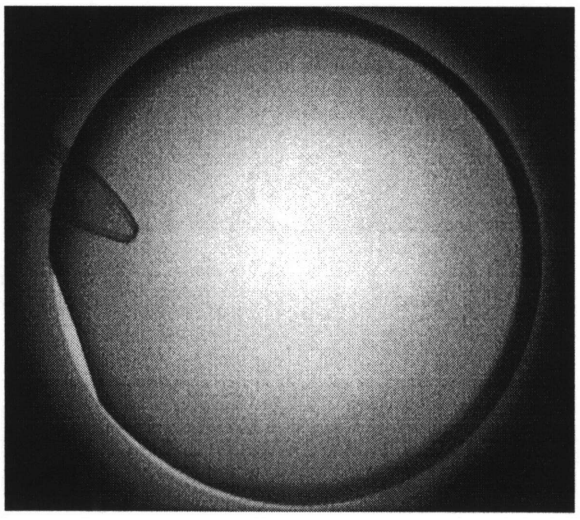


Figure 4–2: Infrared image of a bonded wafer pair with no voids. This particular sample demonstrates Si-Si bonding.

4.3 Hybrid-Accelerometer Process Flow

This section describes (in sequence) the details of the various process steps involved in the fabrication of the hybrid-accelerometer. The process starts on two wafers: a handle wafer and a device wafer. Each of these wafers are processed separately up to the wafer bonding step, after which they are processed together. Please note that in the following process description the step numbers refer to the numbers in the process traveler (Appendix B). In addition, representative wafer cross-sectional views are illustrated in Figure 4–3.

4.3.1 Handle Wafer Processing – Up to Wafer Bonding

Starting material

The handle wafer starting material is:

<100> boron doped (10-20Ω-cm) double-side polished 4" silicon wafer (525±25μm thick).

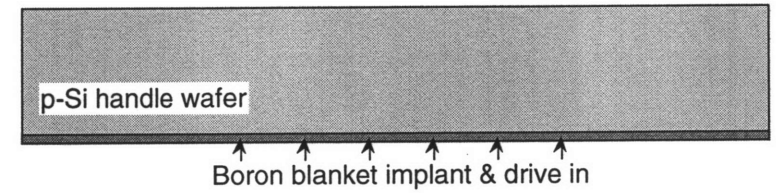
Backside contact formation (steps 1–4)

These steps form the handle wafer backside contact necessary for the electrochemical etch.

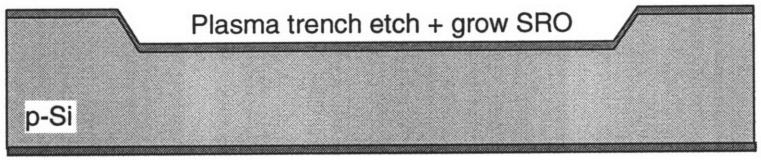
Process

1. Grow a 430Å screening oxide

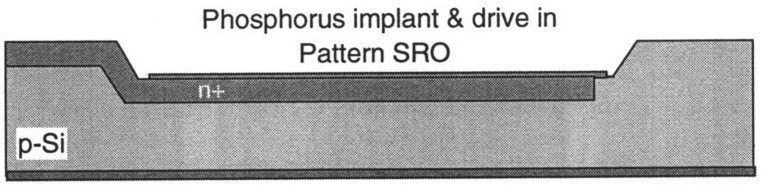
2. Backside blanket implant – species: boron, dose: $5\times10^{15}cm^{-2}$, energy: 100keV



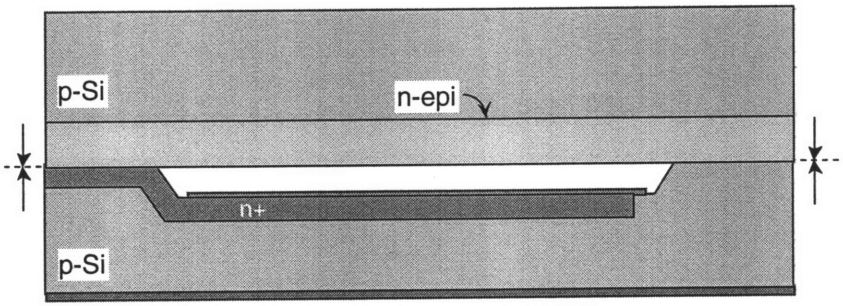
a) Form backside contact (process steps 1–4)



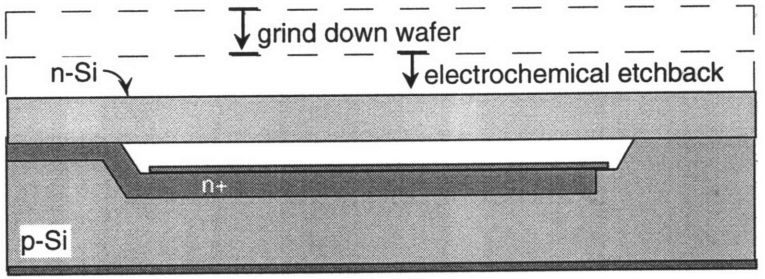
b) Trench etch and grow SRO (process steps 5–8)



c) Form junction-isolated bottom electrode
(process steps 9–15)

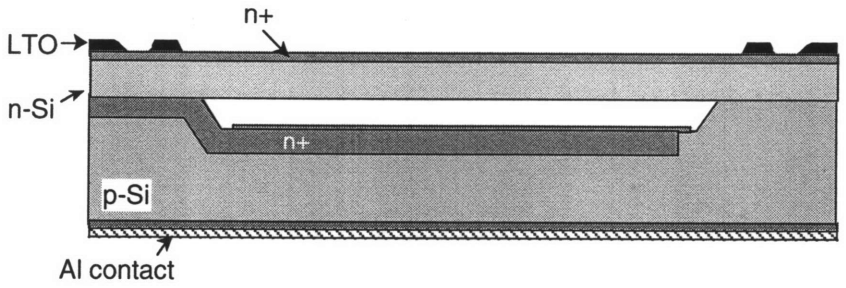


d) Bond device (p/n) wafer to handle (p-Si) wafer
(process steps 20–21)

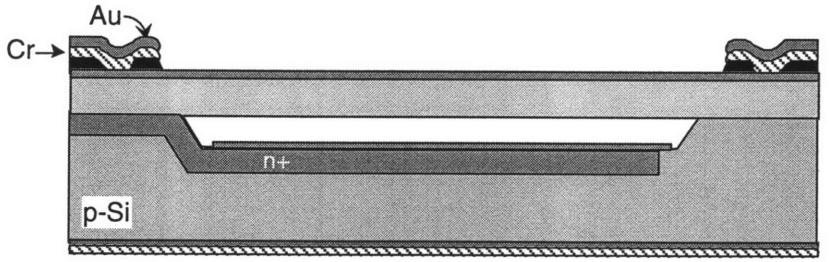


e) Remove p-silicon from device wafer
(process steps 22–24)

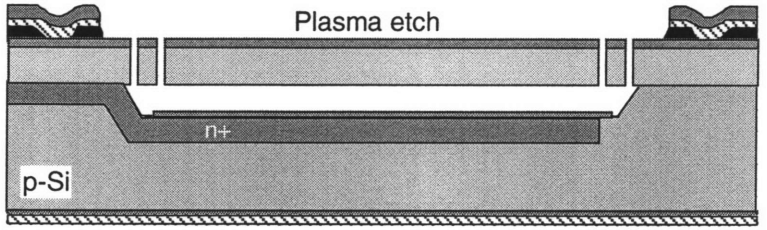
Figure 4–3: Hybrid-accelerometer fabrication process flow.



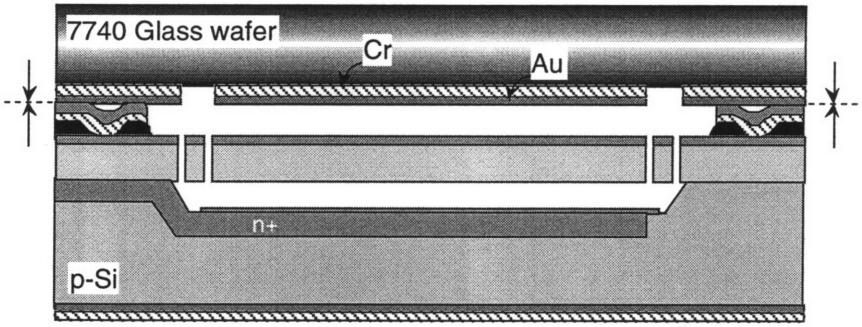
f) LTO deposition and patterning (process steps 33–37)



g) Electron-beam deposition (process steps 41–46)



h) Free mechanical structure with plasma etch (process steps 60–63)



i) Bond glass wafer with top electrode (Cr/Au) (process steps 64–66)

Figure 4–3: Hybrid-accelerometer fabrication process flow (cont.).

3. Drive-in – temperature: 1150°C, time: 2hrs, inert ambient

4. Strip oxide with a buffered oxide etch (BOE)

Process Development

The first step in the process was the growth of a thermal screening oxide (SRO) layer that is 430Å thick. The next step involved a high dose and high energy blanket boron implant (species = boron, dose = $5\times10^{15}cm^{-2}$, energy = 100keV, 7° tilt) and drive-in (temperature = 1150°C, time = 2hrs, N_2 ambient) of the backside of the handle wafers. This provides an ohmic contact for the backside metallization for the accelerometer bottom electrode contact and also ensures a good electrical contact during the electrochemical etch (ECE) that is used to thin back the device wafer. The screening oxide helps to minimize implant channeling and prevent out-diffusion of the implanted species during the drive-in process. The SUPREM process simulation software was used to determine the surface concentration and the sheet resistance in the implanted layer. The SUPREM input and output files that give the electrical characteristics of this layer is also included in Appendix B.

Frontside cavity etch (steps 5–7)

These steps form 1μm deep cavities in the handle wafers.

Process

5. Pattern 1.1μm standard resist using mask #1 HYBRID CAVITY

6. Plasma etch 1μm deep cavities in the handle wafers using a timed SF_6-based etch (Recipe 19, Appendix B)

7. Piranha strip resist (1:3 H_2O_2:H_2SO_4)

Process Development

The handle wafers were first coated with a 1.1μm photoresist. Before being coated with photoresist the wafers were primed in an automatic HMDS (hexamethyldisilazane) vapor prime oven. HMDS is widely used in the semiconductor industry to improve photoresist

adhesion to oxides. The stable state of silicon always has a thin layer of native oxide on the surface and hence the use of HMDS improves the adhesion of the photoresist. This HMDS coating process is assumed for all subsequent photolithography steps. The wafers were then patterned (mask #1 HYBRID CAVITY) in a Karl Suss Model MA4 contact aligner (note: all the subsequent photolithography steps were performed on the contact aligner). This layer was aligned to the major flat on the wafer. All the subsequent mask layers align to this layer.

The next step involved the plasma etching of 1.0 μm-deep cavities in the handle wafers, as shown in Figure 4–3(b). The plasma etching was carried out in a LAM480 etcher using the etch parameters given in Appendix . The etching chemistry is based on a SF_6/CCl_4 based plasma. The etch rate of silicon using this chemistry was highly geometry-dependent, ≈ 50Å/s for large geometries and ≈ 27Å/s for the smaller ones. This is referred to as the "loading effect". Typically, much higher etch rates were observed in larger areas. The etch rates varied by almost an order of magnitude as the pattern size was changed by an order of magnitude. This made it difficult to achieve uniform trench depths across different pattern sizes. The wafers were rotated halfway through the etch in order to achieve better uniformity in the etch depth across the wafer. The measured cavity depths on the wafer were in the range of 1.00 ± 0.02μm. The bottom of the cavities was found to be quite rough when the standard plasma SF_6/CCl_4 (SF_6 = 95sccm; CCl_4 = 3sccm; sccm = standard cubic centimeter per minute) chemistry was used. We believe this was due to the "micromasking" effect of the photoresist, which is "sputtered" from the top surface of the wafer into the bottom of the cavities. This problem was overcome by increasing the flow rate of CCl_4 from 3sccm to 10sccm. This considerably minimized the surface roughness on the bottom of the cavities. After the etch the photoresist was stripped in a piranha solution.

Bottom electrode implant (steps 8–12)

These steps form the accelerometer bottom electrode.

Process

8. Grow 430Å screening oxide

9. Frontside blanket implant to prevent inversion – species: boron, dose: $8\times10^{11}cm^{-2}$, energy: 70keV

10. Pattern 1.1μm standard resist using mask #2 HYBRID DIFFUSION

11. Patterned implant to form accelerometer bottom electrode – species: phosphorus, dose: $7\times10^{15}cm^{-2}$, energy: 90keV

12. Piranha strip resist

Process Development

The first step was to grow a 430Å of screening oxide. The wafers were then blanket boron implanted (species = boron, dose = $8\times10^{11}cm^{-2}$, energy = 70keV, 7° tilt). This implant was to increase the surface boron concentration, thereby increasing the threshold voltage for surface inversion thus preventing surface inversion.

A 1.1μm photoresist layer was then patterned using mask #2 HYBRID DIFFUSION. The wafers were then phosphorus implanted (dose = $7\times10^{15}cm^{-2}$, energy = 90keV, 7° tilt). All parameters for the implant, the species, dose, energy and drive-in time were obtained from SUPREM simulations. It must be noted that the parameters were chosen to obtain a junction depth of 2.1μm. The drive-in for this implant is the same as the bonding-anneal step (step #21). The resulting structure is shown in Figure 4–3(c).

Electrical passivation and patterning of the passivation oxide (steps 13–15)

These steps pattern the passivation oxide (SRO) in the cavities.

Process

13. Pattern 1.1μm standard resist using mask #3 HYBRID SRO

14. Etch oxide with BOE

15. Piranha strip resist

Process Development

Surface electrical passivation is the process of reducing the surface state density of silicon by tying up the "dangling" bonds (or unterminated surface states). The presence of dangling bonds that are not tied up results in leakage currents. This is because these unterminated surface states contribute to energy levels in the center of the band gap region of silicon (donors and acceptors contribute to energy levels towards the edges of the band gap). These mid-band gap energy states act as sites for recombination-generation (*R-G*) and are thus responsible for increased leakage current (the *R-G* centers are also sometimes referred to as traps). Thermally grown oxides (*not* deposited oxides) have been shown to considerably reduce the charge density (or surface trap density) at the $Si\text{-}SiO_2$ interface, thereby reducing the leakage currents. It has been found that when a thin layer of SiO_2 is grown on the surface of silicon where a *p-n* junction intercepts the surface, the leakage current of the junction was reduced by an order of magnitude. This is because the passivation oxide reduces and stabilizes interface traps.

The process steps show here provide electrical passivation of the cavity surfaces, thereby helping to minimize the individual *p-n* junction leakage currents. The plasma etching process that was used to etch the cavities, left behind dangling bonds on the surface. These unterminated surface states increased the surface leakage current density. This problem was overcome by "terminating" these bonds with a thermally grown oxide layer as described above.

This thin oxide layer was patterned using a 1.1μm photoresist layer (mask #3: HYBRID SRO). The pattern ensures that (after BOE oxide etch step) the screening oxide is left behind only in the cavities and is completely removed from the field regions. In order for the wafer bonding step to be successful, the oxide layer must be completely removed from the field regions of the wafer and be left only in the cavities. Any oxide "islands" remaining in the field regions will translate to bonding voids. In addition, any misalignment of this pattern could also result in oxide being left behind in the field regions and the above mentioned problems. The main concern for this photolithography step is

then to eliminate any photoresist from the field regions. Any photoresist in the field regions would correspond to oxide islands remained in the field after the BOE etch, thereby resulting in bonding defects (voids/debond regions). The following steps were therefore taken to thoroughly clear the field regions of any photoresist. First, this mask layer was designed to be tolerant to misalignments of the order of 10μm. Second, two 10X emulsion plates were generated from the same KIC file. Each of the emulsions was then stepped out to generate its own 1X chrome contact mask, which was then used in the photolithography process. Each wafer is exposed using both the chrome masks. This "double exposure" procedure helps eliminate any photoresist from the field regions that may arise due to mask imperfections. The probability of two independently generated chrome masks to have imperfections at the same location is very small. Hence any resist left behind in the field region of the wafer due to an imperfection in one of the masks will be exposed away during one of the two exposures. One major effect of the "double exposure" scheme used in this process is that the clear-field areas on the wafers become slightly larger than what was designed due to over-exposure. However, the misalignment tolenrance for this particular mask was designed to be at least 10μm on all sides, thus, slight over-exposure would not alter our design nor the device functionality. Third, a "ring" mask (which blocks the central regions of the wafer and exposes a ring-region about 1cm from the wafer edge) was used to expose the edges of the wafer, a region where resist tends to accumulate and thicken during the coating process. While the edge-bead removal solvent removes most of this photoresist, it does not completely remove it. The "ring" mask is used to expose this photoresist layer. Typically, a very long exposure and development time is used to completely remove any photoresist from the edges of the wafer. This third step was found to help considerably in improving the quality of the wafer bonds between the device and handle wafers. The resulting structure is shown in Figure 4–3(c).

4.3.2 Device Wafer Processing – Up to Wafer Bonding

Starting material

The device wafers are one of the following:

1) junction etch-stop wafers:

a. <100> boron doped (10-20Ω-cm) double-side polished 4" silicon wafer (525±25μm thick). These wafers were thinned-back using ECE.

b. 4" Motorola supplied type C21 epi wafers. These device wafers comprise a p-type <100> substrate (resistivity ≈ 10-20Ω-cm) with 10.82 ± 0.05μm epitaxial layer, arsenic doped (average resistivity ≈ 4.7Ω-cm). There wafers were thinned-back using ECE.

2) oxide etch-stop (SOI) wafers:

4" silicon-on-insulator (SOI) wafers supplied by Motorola [68] of thickness 10.80 ± 0.05μm (on an average of five SOI wafers with very well-matched thicknesses) with a n-type <100> silicon device layer on top of a 4000Å buried oxide (BOX) layer which is on top of a 385 μm-thick n-type silicon substrate. The typical resistivity of the 10.8μm device layer is 1-10Ω-cm (arsenic doped). These wafers were thinned-back using a KOH etch. It must be noted that if SOI wafers are used, the device wafers require no further processing before the wafer bonding step (step #20).

Etch-stop definition (steps 16–19)

These steps form the 10 μm-thick junction etch-stop wafers (type 1(a)) shown above.

Process

16. Grow a 430Å screening oxide

17. Blanket implant – species: phosphorus, dose: $1\times10^{14}cm^{-2}$, energy: 160kev

18. Drive-in – temperature: 1150°C, time: 15hrs, inert ambient

19. Strip oxide with BOE

Process Development

The processing steps shown here are required only for junction etch-stop wafers type 1(a) that are thinned-back using an electrochemical etch-stop technique. The first step was to grow a screening oxide on the wafers. The frontside was then blanket implanted with phosphorus (dose = $1\times10^{14}cm^{-2}$, energy = 160kev, 7° tilt) and annealed (time = 15hrs, temperature = 1150°C, N_2 ambient) to obtain a 10 μm-thick *n-type* junction on a p-type substrate. The SUPREM simulation package was used to determine the dose, energy, drive-in time and drive-in temperature. A 0.25" ring-region (from the edge) of the wafer was then patterned and plasma etched to a depth of 2μm. The wafer was held along the 0.25" ring-region during the implant and hence was not implanted in this region. For the electrochemical etch (step #23) to work properly, this p-type region should not be in contact with the handle wafer after the wafer bonding step. The 2 μm-deep etch prevents the ring-region of the device wafer from being in contact with the handle wafer. This completes the device wafer processing steps for non-SOI device wafers. The resulting structure is shown in Figure 4–3(d).

4.3.3 Bonding of Handle and Device Wafers

Wafer bonding (steps 20–21)

These steps bond the device wafer to the handle wafer.

Process

20. RCA clean the handle and device wafers and then contact in a 100% oxygen ambient

21. Bonding anneal – temperature: 1100°C, time: 70 minutes, inert or dry O_2 ambient

Process Development

The processed handle wafers and the device wafers were first RCA cleaned to hydrate their surfaces. The wafers were then loaded into a controlled-ambient single-wafer bonder, which allows the frontsides of the two wafers to be brought into intimate contact. The ambient in the bonder can be controlled to be pure oxygen, pure nitrogen, or a mixture of both. In our case, the wafers were contacted in a pure oxygen (100% O_2) ambient, and hence this is the ambient within the sealed cavity that is formed between the handle and device wafers.

Figure 4–4(a) shows the interface of a bonded wafer imaged using the IR inspection system. It can be seen that the interface is free of any voids. It must be noted that the absence of voids in the output of an IR imager does not mean that the interface is completely free of voids. The same interface (shown in Figure 4–4(b)) now imaged using an ultrasonic imaging system shows some voids on the wafer periphery. Since the voids are on the edge (and not in the active device area), this wafer is acceptable for subsequent processing.

The contacting process was followed by a high-temperature anneal for 70 minutes at 1100°C in either a dry O_2 or N_2 ambient. During the annealing process most of the oxygen that is trapped in the sealed-cavity is consumed to form a thin layer of silicon dioxide, which coats the walls of the sealed cavity. The consumption of the trapped oxygen reduces the pressure in the sealed cavity. The low pressure in the cavity, typically 0.05atm or lower, prevents the rupturing of the thin membranes during any high-temperature or low-pressure step that is carried out after the thinned-back process and prior to the microstructure release. The annealing step results in a permanent bond between the two wafers, as shown in Figure 4–3(d). This annealing step was also used to drive in the bottom electrode implant discussed in steps #8–12.

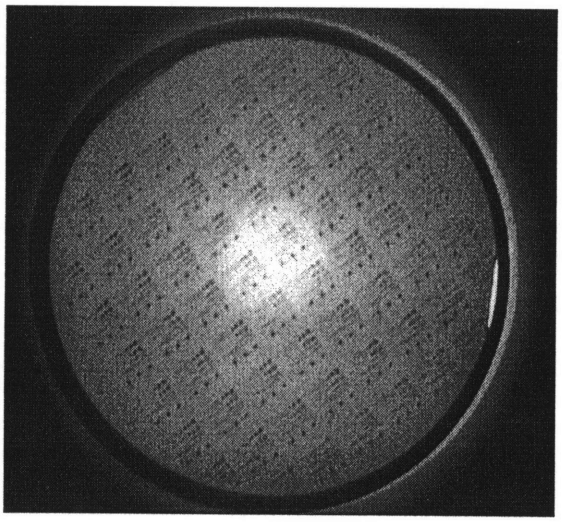


Figure 4–4(a): Infrared image of a bonded wafer pair with no apparent voids.

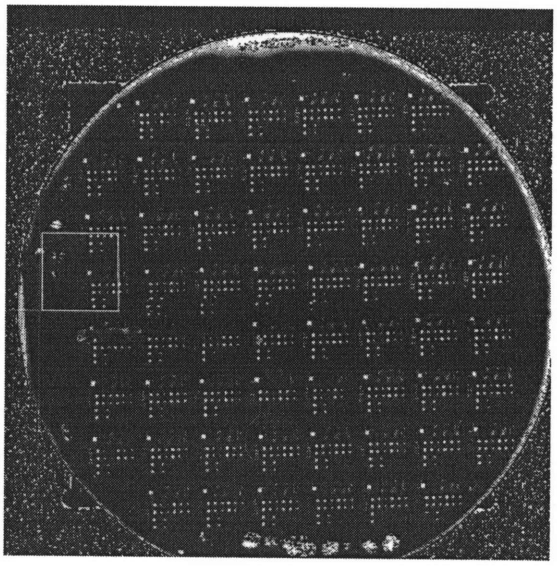


Figure 4–4(b): Image of the same bonded interface when viewed with an ultrasonic imaging system showing some small voids on the wafer periphery.

4.3.4 Sealed Cavity Wafer Processing

Thin-back of device wafer (steps 22–24)

These steps form the sealed cavity wafer by thinning back the bonded wafer pair.

Process

22. Grind and polish the device wafer of the bonded wafer pair

23. KOH etch with ECE

24. KOH post-processing clean

Process Development

The first step in the thin-back process involved the mechanical grinding and polishing of the device wafer surface of the bonded pair. Typically, about 450μm of silicon was removed from the junction etch-stop device wafer leaving behind a 90 μm-thick layer. In the case of SOI wafers, typically about 300μm of silicon was removed from the device wafer leaving behind a 80 μm-thick layer (note that the starting thickness of the SOI wafers is approximately 385μm). The mechanical grinding and polishing was performed to minimize the etch time during step #23. It is important to note that we intentionally leave about 80–90μm of silicon on the device wafer before the thin-back process to give us a larger processing window when preparing and conditioning the necessary ECE setup and the etch-stop measurement system while the wafers are already exposed to a relatively rigorous silicon etchant (95°C, 20% by weight KOH:H_2O solution). In addition, grinding and polishing could leave a "damage zone" as deep as 30μm down from the wafer surface, a thicker layer left on the device wafer ensures a nearly "damage free" smooth surface after the thin-back process described in the following.

The next step in the thin-back process of the junction-isolated wafers was the electrochemical etch to remove the rest of the device wafer leaving behind a 10μm device

layer. In the case of the oxide etch-stop, the wafers were etched in a 20% by weight KOH:H_2O solution. The thinned-back wafer is shown in Figure 4–3(e).

It is appropriate at this point to mention that there is another way we could prepare the bonded wafer pairs prior to thin-back. After the bonding anneal, a layer of silicon nitride was deposited on the bonded wafer pairs (oxide etch-stop device wafer + handle wafer). This nitride layer was then etched away from the device-wafer side of the bonded pair using a dry plasma etch. The nitride layer acts as an etch-stop layer during the KOH etch. This nitride etch-stop layer was employed to eliminate the need for mechanical grinding and chemomechanical polishing of the bonded wafer pairs. The nitride masking method is now being used regularly in our research group for the thin-back process when the oxide etch-stop device wafer is employed.

The final step in the thin-back process was the post-KOH-etch cleaning procedure. This cleaning procedure permits the re-introduction of the wafers into the IC fabrication line. The cleaning procedure is as follows: 1) wafers were first rinsed in DI water for 10 minutes; 2) piranha clean followed by a 10-minute rinse in DI water; 3) oxide etch in 50:1 DI H_2O:HF solution followed by 10-min rinse in DI water; 4) RCA clean.

Transfer alignment marks (steps 25–27)

These steps transfer the alignment marks from the 10μm device layer/handle wafer interface to the surface of the sealed cavity wafer. IR alignment is necessary.

Process

25. Pattern 1.1μm standard resist using mask #4 HYBRID STRUCTURE and IR alignment

26. Plasma etch 0.5μm deep alignment marks in the silicon using a timed SF_6-based etch (recipe 19)

27. Piranha strip the resist

Process Development

These steps were used to transfer the alignment marks from the sealed-cavities of the handle wafer on to the top surface of the device wafer. This procedure eliminates the need of using IR alignment for all the subsequent photolithographic steps. The transfer allows all the subsequent photolithographic steps to be aligned to the patterns in the sealed cavities in the handle wafer. The alignment for this step was done using an infrared (IR) alignment procedure. The IR radiation (which is transmitted through the thickness of silicon) illuminates the backside of the handle wafer and the transmitted beam is picked up by an IR imaging CCD camera. The image can be viewed on a TV monitor. Hence the alignment marks in the sealed cavity can now be viewed on the TV monitor. The alignment marks on the alignment-marks-mask (mask #4 HYBRID STRUCTURE) were then aligned to the original alignment marks seen on the TV monitor. The patterned frontside was then plasma etched (depth $\approx$ 0.5μm), and this completed the process of transfer of alignment marks from the sealed-cavities to the top surface of the device wafer.

Backside scribe line etch (steps 28–30)

These steps form the backside scribe lines used for backside partial dicing in steps #47–50.

Process

28. Pattern 1.1μm standard resist using mask #5 HYBRID SCRIBE and IR alignment

29. Plasma etch 2μm deep scribe line pattern in the silicon using a timed SF_6-based etch (recipe 19)

30. Piranha strip the resist

Process Development

These steps were used to form scribe lines on the backside of the sealed cavity wafer. Those scribe lines will be used for backside dicing operation in steps #47–50. The alignment for this step was done using an infrared (IR) alignment procedure, and the mask used was mask #5 HYBRID SCRIBE. The patterned backside was then plasma etched

(depth ≈ 2μm), and this completed the process of forming the scribe lines on the backside of the sealed cavity wafer.

Surface-replenish implant (steps 31–32)

The following steps provide an extra phosphorus implant in the device layer to ensure an ohmic contact after the frontside metallization.

Process

31. Grow a 430Å screening oxide

32. Blanket implant – species: phosphorus, dose: $7\times10^{15}cm^{-2}$, energy: 90kev

Process Development

The process steps are used to increase the surface phosphorus concentration of the frontside (device layer side) of the thinned-back wafer (note that after the thin-back process the frontside is the 10μm n-type layer). This implant ensures an ohmic contact after the frontside metallization (steps #41–46).

The first step was to grow 430Å of screening oxide on the sealed cavity wafer. The device layer then received a blanket implant (species = phosphorus, dose = $7\times10^{15}cm^{-2}$, energy = 90keV, 7° tilt). The implanted species were to be driven-in by the LTO densification step shown next.

5kÅ LTO spacer formation (steps 33–37)

These steps form the 5kÅ low-temperature-oxide (LTO) spacer and drive-in all of the previous implants.

Process

33. Deposit 5kÅ LTO

34. LTO densification – temperature: 1000°C, time: 1hr, inert ambient

35. Pattern 1.1μm standard resist using mask #6 HYBRID LTO

36. BOE etch all oxides on the sealed cavity wafer

37. Piranha strip resist

Process Development

The first step in the LTO spacer formation was the deposition of 5kÅ LTO on the sealed cavity wafers. The average deposited LTO thickness prior to densification was 4820Å. It is important to know the spacer thickness quite accurately since this spacer along with the gold spacer/electrical contact determine the final gap dimension between the top gold electrode and the accelerometer proof mass. Immediately after the 5kÅ LTO deposition, the wafers were annealed for one hour at 1000°C in a nitrogen ambient. During the annealing process all of the previous implants were driven-in at the same time. The average thickness of the densified LTO spacer was 4680Å.

The LTO spacer was then patterned using a 1.1μm photoresist layer and mask #6 HYBRID LTO. BOE was then used to etch away all oxide layers from the sealed cavity wafers. Please note that there is no oxide left on the accelerometer areas after the oxide etch (5-min etch in BOE), except for small contact pad areas around the contract pads themselves. Piranha was used to strip the photoresist. The resulting structure is shown in Figure 4–3(f).

Backside metallization (steps 38–40)

The following steps metallize the backside of the wafer. This metal layer is the common ground for all the accelerometers on the wafer.

Process

38. Pre-metallization HF dip – 50:1 diluted HF solution, time: 30sec

39. E-beam evaporate 1μm of aluminum

40. Sinter the aluminum metal – temperature: 450°C, time: 15min, inert ambient + 15min, forming gas ambient

Process Development

Aluminum was the metal of choice because of its common use in IC fabrication. The wafers were first dipped in a diluted HF solution (50:1 DI H_2O:HF) to remove the native oxide layer immediately before they were loaded in the e-beam evaporation chamber. A 1μm aluminum layer was then evaporated on the wafers. The planetary rotation was used to achieve a uniform coating of metal across all wafers. This aluminum layer serves as the common ground for all the accelerometers on the wafer. The wafers were then subjected to a 450°C sintering step. The sintering step was performed at 450°C in a forming gas (H_2/N_2) ambient, and it helps to achieve an ohmic contact between the metal layer and the underlying silicon substrate.

Frontside metallization (steps 41–46)

The following steps metallize the frontside of the sealed cavity wafer and a Pyrex 7740 glass wafer (as the capping wafer). This chrome/gold metal spacer layer along with the LTO spacer layer define the gap between the top electrode and the accelerometer itself.

Process

41. Pattern 1.4μm image reversal photoresist (AZ 5214-E) using mask #7 HYBRID Si_Au on the sealed cavity wafer and mask #8 HYBRID Glass_Au on a Pyrex 7740 glass wafer

42. Descum ash for 2min

43. 50:1 HF dip for 30sec

44. E-beam evaporate 100Å chrome + 5kÅ gold on both silicon and glass wafers

45. Acetone lift-off

46. Nanostrip clean for 5min

Process Development

The first step for the frontside mtalization process was to pattern a 1.4μm layer of image reversal photoresist AZ 5214-E. The process of producing negative images from a positive resist is referred to as image reversal. The AZ 5214-Z photoresist is a positive

working aqueous alkali developable resist. Patterning of this resist requires two extra processing steps (when compared with standard resist patterning process): a post-exposure bake and a flood exposure. The initial exposure step causes a photoactive compound in the resist to generate an acid. Following the post-exposure bake at a relatively high temperature, the acid diffuses through the resin system of the resist film and causes acid catalyzed crosslinking. This crosslinking results in a "UV hardened" resist that is inert to further photochemical processing and is insoluble in the developer. The wafer in process is then flood exposed, making the non-UV-hardened resist extremely soluble in the developer (AZ 422MIF). After developing, only the UV hardened resist pattern is left.

The main reason for using AZ 5214-E for this lift-off process is due to its ability to produce a negative slope (that is an angle greater than 90° with respect to the substrate) on the sidewall. The exact angle of the negative profile can be controlled by adjusting the exposure time. Typically a lower exposure time gives a more negative profile. The negative slope of the photoresist sidewall is desirable for the lift-off process as it prevents good coverage of the walls with chrome/gold metal layer during the evaporation process, thereby facilitating the easy lift-off of the metal layer in our process.

After image reversal resist patterning, the wafers were then subjected to a 2min descum in an O_2 plasma. This was to make sure that the areas that are supposed to be clear of any photoresist were completely free of any resist. Any remaining photoresist in the clear regions will affect the quality of electrical contact of the metal to the underlying silicon. In addition, the adhesion of the metal to the substrate will be poor and the metal in these regions will tend to lift-off. The wafers were dipped in a diluted HF solution to strip the native oxide layer, immediately before the metal deposition step. A 100 Å-thick layer of chromium was e-beam evaporated on the wafers (both silicon and glass wafers) first prior to the 5 kÅ-thick of gold was evaporated on. The thin chromium layer acted as an adhesion layer as discussed in details before [7]. A custom-made "flat" planetary plate was used to hold the wafers "flat and face down" in the evaporation chamber. The

standard planetary and the planetary rotation were typically used to achieve a uniform thickness of metal across all the wafers and to provide a good step-coverage of the metal. Since in this case we were going to do a lift-off of the metal, a good step-coverage was not desirable.

The lift-off of the metal was accomplished by immersing the wafers in acetone. An important observation regarding the lift-off process should be mentioned here. The wafers were not subjected to any ultrasonic agitation, a process that is commonly used to facilitate the lift-off of metal. The reason for not using ultrasonic agitation is because this was found to be responsible for crack initiation and crack growth at membrane-corners (regions of stress concentration). The lift-off process (without ultrasonic agitation) was successful but took more time to be completed (approximately 3–12 hours).

The final step in the lift-off process was to perform a 5-min nanostrip (diluted piranha) clean of the wafers. This was to remove any remaining traces of photoresist from the wafers. The resulting structure is shown in Figure 4–3(g).

Silicon wafer backside partial dicing (steps 47–50)

The following steps partially dice the backside of the sealed cavity wafer so the dies can be separated easily at the completion of the process flow.

Process

47. Coat 5μm AZ 4620 resist on the frontside of the wafer

48. Partially dice the backside of the wafer (150μm into the wafer)

49. Acetone strip resist

50. Nanostrip clean for 2min

Process Development

The first step in preparing the sealed cavity wafers to be diced with a diesaw was to coat the frontside of the wafers with a 5 μm-thick AZ 4620 photoresist. AZ 4620 is a much more viscous resist compared with the standard OCG 825-20CST resist we have been

using throughout this fabrication process. The AZ 4620 resist coating on the frontside of the wafers protect the surface during the dicing operation. The wafers were then subjected to a partially dicing with a diesaw. The dicing depth was controlled to be 150μm into the backside of the silicon wafers. The wafers were then DI rinsed before they were soaked in acetone to strip the resist. After the acetone strip, nanostrip was used to clean the wafers for further processes.

Glass wafer dicing (steps 51–54)

The following steps dice the glass wafer.

Process

51. Coat 5μm AZ 4620 resist on the frontside of the glass wafer

52. Dice the glass wafer

53. Acetone strip resist

54. Nanostrip clean for 2min

Process Development

The first step in preparing the glass wafers to be diced with a diesaw was to coat the frontside of the wafers with a 5 μm-thick AZ 4620 photoresist. The AZ 4620 resist coating on the frontside of the wafers protected the surface during the dicing operation. Furthermore, the fine dust created during the dicing operation tend to collect in the resist coating, thus easily removed from the glass surface with the subsequent acetone strip. The separated dies were then DI rinsed before they were soaked in acetone to strip the resist. After the acetone strip, nanostrip was used to clean the dies.

Vent hole etch (steps 55–59)

The following steps are used to pattern and etch vent holes.

Process

55. Pattern 2.2μm double-thickness resist using mask #9 HYBRID VENT

56. Descum ash for 2min

57. Reactive ion etch (RIE) 5μm of silicon in the vent hole area

58. RIE O_2 plasma ash resist

59. Nanostrip clean for 2min

Process Development

These process steps were used to pattern and etch vent holes. The vent holes help to *vent* the sealed-cavities to atmosphere (before the accelerometer structure is released) during the final structure release step. The reason for doing this is as follows: during the final release etching process (step #62), which is used to release the microstructure, all the membranes on the wafers are subjected to a pressure load that is equal to the difference of the pressure in the sealed-cavities, P_{cavity}, and the pressure in the reactive ion etching chamber, $P_{chamber}$. In our case $P_{cavity} \approx$ 0.05atm or less (or about 38Torr or less) and $P_{chamber} \approx$ 90mTorr or less. Since $P_{cavity} - P_{chamber}$ is positive the membranes are subjected to an upward pressure load. The upward force is equal to the product of the upward pressure and the membrane area on which this pressure acts. Hence larger the membrane area the larger the upward force. During the final moments of the structure-release etch the thickness of silicon remaining in the etch areas is small. If a large upward force acts on this remaining silicon, it could cause a catastrophic rupture resulting in broken accelerometer proof mass plates. To avoid this problem, the sealed cavities are vented before the final structure is going to be released. This is to ensure that at the time of the microstructure release, the pressure on either side of the membrane has equalized and there is no danger of rupturing the membrane. The vent hole is located far away from the microaccelerometer structure. Hence any catastrophic event when the vent hole is being punched-through will not affect any of the devices on the wafers.

The first step in this process was to pattern the vent holes. A double-thickness resist layer was used (2.2μm). The patterned wafers were then etched in a SF_6/C_2ClF_5

plasma in the RIE chamber for about 15 minutes. This resulted in 5 μm-deep vent holes. It must be noted that the etch depth of 5μm is half the thickness of the device layer. Hence during the final structure-release step (which also etches the pre-etched vent holes) the vent holes are punched through in about half the time it takes for the microstructure to be released. This ensures pressure equalization across the microstructures during the release step. After the etch the photoresist was ashed in an O_2 plasma in the same RIE chamber. Finally the wafers were cleaned with nanostrip for 2 minutes to completely remove photoresist from the wafer surface.

Structure-release etch (steps 60–63)

The following steps are used to release the accelerometer structure using a dry plasma etching process.

Process

60. Pattern 2.2μm double-thickness resist using mask #4 HYBRID STRUCTURE

61. Descum ash for 2min

62. Reactive ion etch (RIE) 10μm of silicon to release the microstructure

63. RIE O_2 plasma ash resist

Process Development

The wafers were patterned with the structure release mask (mask #4 HYBRID STRUCTURE). A double-thickness resist layer was used (2.2μm). These processing steps were used to release the accelerometer structure using a dry plasma etching process. The etch depth was 10μm, which is the thickness of the desired accelerometers. The plasma chemistry is SF_6/C_2ClF_5 (75%:25%). This is the same chemistry that was used for the vent hole etch. This silicon etch chemistry resulted in 87° vertical side walls for all the released structures, which is adequate for our application. The etch lasted for about 37.5mins, including 2.5mins of overetch time. Since there was some variation in the etch rate across the wafer, 2.5mins of overetch was necessary to ensure the release of all the

devices on the wafers. The resulting structure is shown in Figure 4–3(h). After the etch, the wafers were ashed in an O_2 plasma for 30 minutes to remove the remaining photoresist. Please note that no wet etching chemistry should be used after the structure release since *stiction* might occur, and that is exactly what we tried to avoid.

Thermocompression bond (steps 64–66)

The following steps are used to bond the top Pyrex glass wafer (hosting the complementary top electrode) to the base silicon substrate (hosting the accelerometer structure and the bottom electrode).

Process

64. Separate the silicon accelerometer dies by manually breaking the wafer along the backside scribed lines (steps #47–50)

65. Ultraviolet ozone clean of both silicon and glass dies

66. Thermocompression bonding of the silicon and glass dies

Process Development

The metal used for the thermocompression bonding technique is a layer of 5kÅ of gold (over an adhesion layer of 100Å chromium) deposited by e-beam evaporation and patterned using liftoff. Gold is selected as the metallization for two reasons: first, it does not form a surface oxide in air, therefore scrubbing/ultrasonic action is not needed to break through the oxide, and second, it can be bonded at a relatively low temperature due to its softness. Since the bond quality is adversely affected by the presence of any organic material adsorbed on the gold surfaces, both silicon and glass dies were first cleaned with an ultraviolet ozone exposure, after which the surfaces were aligned, contacted, and heated to 350°C on a hotplate while a pressure of about 20psi was applied for a period of 2 minutes. The resulted structure is shown in Figure 4–3(i). Studies of the strength of the thermocompression bond [30] have indicated that the shear strength is comparable to that

of conventional wire bonds, and that failure of the bond usually occurs in the bulk of the silicon or glass, not at the gold-gold interface.

Currently the thermocompression bonding is done on a chip level using a jig setup to hold and align the chips prior to bonding. This sometimes results in problems with particulate generation during handling. However, the process can be transferred to wafer level with suitable equipment that is capable of applying enough uniform pressure over the whole wafer to initiate the bond. This necessitates the machining of holes in the capping wafer prior to bonding for access to bond pads on the silicon chip. To prevent water from entering between the two wafers during the sawing operation, the chip edges should be sealed with gold as indicated in Figure 4–5. Internal areas that require vacuum sealing can also be formed with appropriate gold patterns. Electrical contacts to internal vacuum sealed areas can be achieved by means of diffused or polysilicon bridges leading out to exposed bondpads. By covering the glass side of the wafer pair with tape during the sawing operation. the chip is protected from the saw slurry. The schematic in Figure 4–5 gives representative gold sealing pattern as required for a chip with an integrated capacitive pressure sensor and accelerometer.

4.4 Discrete Accelerometer Process Flow

This section describes (in sequence) the details of the various process steps involved in the fabrication of the discrete accelerometer. The process starts on two wafers: a handle wafer and a device wafer. Each of these wafers are processed separately up to the wafer bonding step, after which they are processed together. Since this discrete accelerometer process flow is similar to the one shown in Section 4.3, only key processing steps different form the hybrid-accelerometer process flow are shown in the following section.

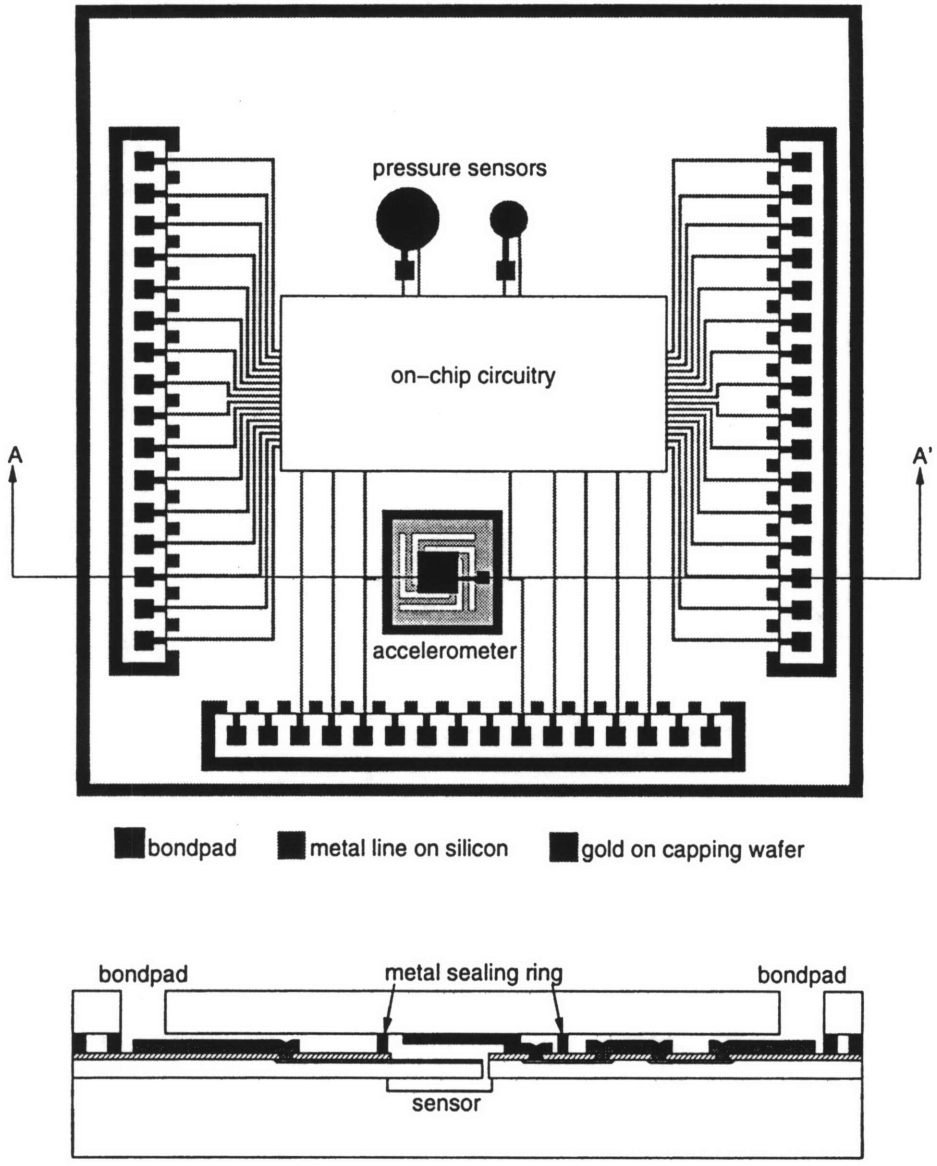


Figure 4–5: Proposed metallization pattern for wafer-level thermocompression bond (courtesy of L. Parameswaran).

Please note that the process step numbers shown below corrspond to the process traveler shown in Appendix B, and the representative processing steps are schematically shown in Figure 4–6.

4.4.1 Handle Wafer Processing – Up to Wafer Bonding

The starting material and the backside contact formation steps are identical to those described in Section 4.3.1 (steps #1–4) and will not be repeated here.

Thermal oxide spacer formation (steps 5–8)

These steps form 1 μm-thick oxide spacer in the handle wafer.

Process

5. Grow 1μm thermal oxide on the wafer – temperature: 1100°C, time: 2hrs 15mins, dryO_2/wetO_2/dryO_2 ambient

6. Pattern 1.1μm standard resist using mask #1 ACCEL CAVITY

7. Wet etch 1μm oxide with BOE

8. Piranha strip resist

Process Development

A 1 μm-thick thermal oxide was grown on the handle wafers. The actual oxide thickness was measured to be 1.010 ± 0.005μm. The handle wafers were then coated with a 1.1μm photoresist and patterned with mask #1 ACCEL CAVITY. BOE was then used to etch away the unpatterned thermal oxide from the handle wafers. The resist was then stripped with a piranha solution. It is important to control the final thermal oxide spacer thickness since this spacer determines the "gap spacing" between the accelerometer proof mass and

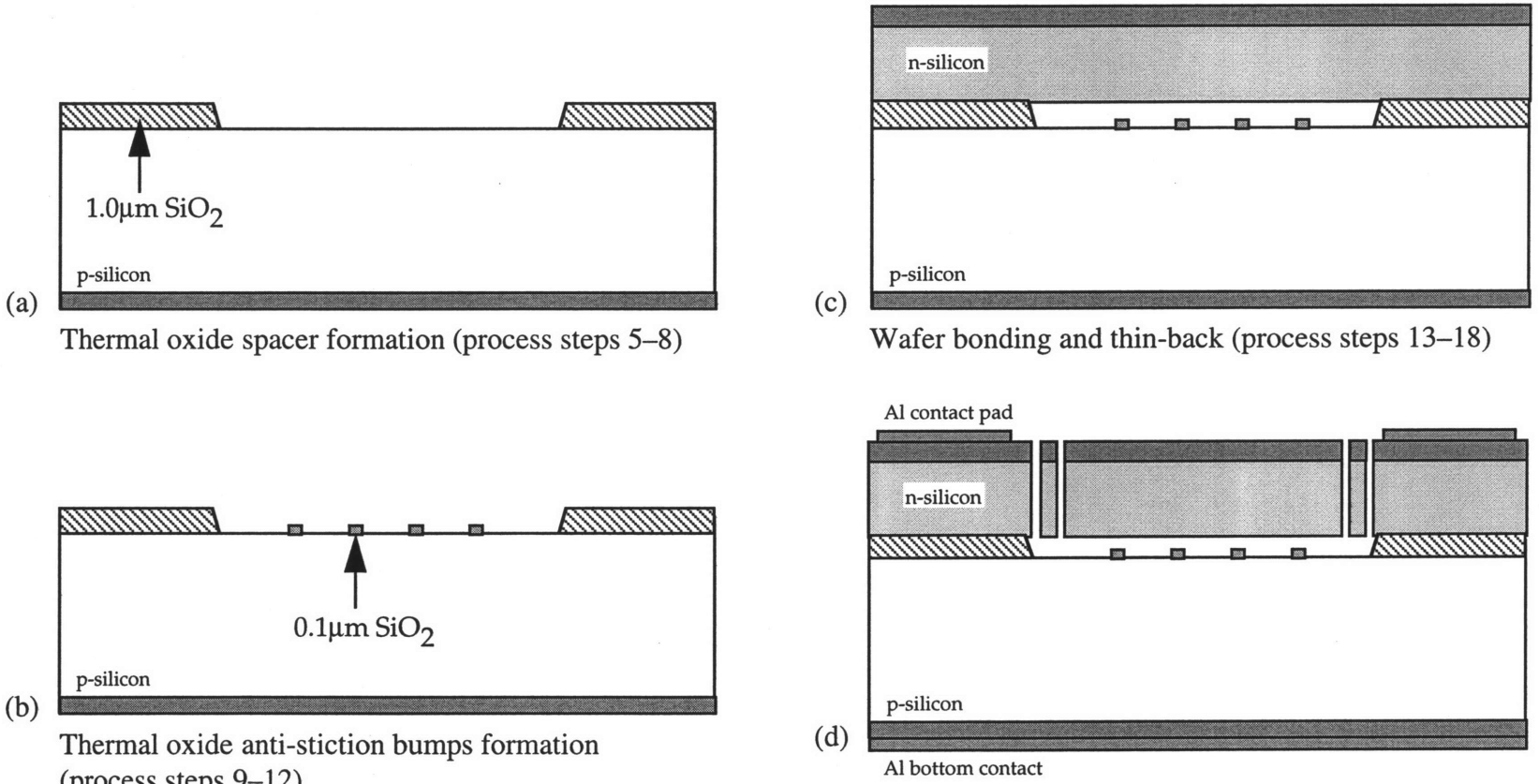


Figure 4–6: Dielectrically isolated accelerometer fabrication process flow.

the bottom electrode (on the substrate). SUPREM package was used to determine the oxidation condition and is shown in Appendix B. The resulted structure is shown in Figure 4–6(a).

0.1μm thermal oxide anti-stiction bumps formation (steps 9–12)

These steps form 0.1 μm-thick oxide anti-stiction bumps in the cavity.

Process

9. Grow 0.1μm thermal oxide on the wafer – temperature: 800°C, time: 40mins 12secs, dryO_2/wetO_2/dryO_2 ambient

10. Pattern 1.1μm standard resist using mask #2 ACCEL BUMPS

11. Wet etch 0.1μm oxide with BOE

12. Piranha strip resist

Process Development

On some of the handle wafers, a 0.1 μm-thick thermal oxide was grown on the handle wafers after the 1μm oxide spacer was defined. The actual oxide thickness was measured to be 0.100 ± 0.005μm. These measurements were made via 5-point method (measuring five points on the wafer) on five wafers using ellipsometry. The handle wafers were then coated with a 1.1μm photoresist and patterned with mask #2 ACCEL BUMPS. BOE was then used to etch away the unpatterned thermal oxide from the handle wafers. The resist was then stripped with a piranha solution. This completed the handle wafer process. The resulted structure is shown Figure 4–6(b).

4.4.2 Device Wafer Processing – Up to Wafer Bonding

The device wafers used are 4" silicon-on-insulator (SOI) wafers supplied by Motorola [68] of thickness 10.80 ± 0.05μm (on an average of five SOI wafers with very well-matched thicknesses) with a n-type <100> silicon device layer on top of a 4000Å buried oxide (BOX) layer which is on top of a 385 μm-thick n-type silicon substrate. The typical resistivity of the 10.8μm device layer is 1-10Ω-cm (arsenic doped). It must be noted that if SOI wafers are used, the device wafers require no further processing before the wafer bonding step, thus this completes the device wafer processing prior to wafer bonding.

4.4.3 Bonding of Handle and Device Wafers

Wafer bonding (steps 13–14)

These steps bond the device wafer to the handle wafer. These steps are identical as described in Section 4.3.3 (steps #20–21) and are not repeated here.

Process

13. RCA clean the handle and device wafers and then contact in a 100% oxygen ambient

14. Bonding anneal – temperature: 1100°C, time: 70 minutes, dry O_2 ambient

4.4.4 Sealed Cavity Wafer Processing

Thin-back of device wafer (steps 15–18)

These steps form the sealed cavity wafer by thinning back the bonded wafer pair.

Process

15. LPCVD 1500Å silicon nitride (Si_3N_4) on the sealed cavity wafer

16. Plasma etch silicon nitride from the device-wafer side of the sealed cavity wafer

17. KOH etch

18. KOH post-processing clean

Process Development

After the bonding anneal, a layer of silicon nitride was deposited on the bonded wafer pairs (oxide etch-stop device wafer + handle wafer). This nitride layer was then etched away from the device-wafer side of the bonded pair using a dry plasma etch. The nitride layer acts as an etch-stop layer during the KOH etch. This nitride etch-stop layer was employed to eliminate the need for mechanical grinding and chemomechanical polishing of the bonded wafer pairs. The final step in the thin-back process was the post-KOH-etch cleaning procedure described previously. The resulted structure is shown in Figure 4–6(c).

Transfer alignment marks (steps 19–21)

These steps transfer the alignment marks from the 10μm device layer/handle wafer interface to the surface of the sealed cavity wafer (mask #3 ACCEL STRUCTURE). IR alignment is necessary. These steps are identical to steps #24–27 described in Section 4.3.4.

Surface-replenish implant (steps 22–25)

These steps provide an extra phosphorus implant in the device layer to ensure an ohmic contact after the frontside metallization (same as steps #31–32, Section 4.3.4). The

difference between this process and the one described in Section 4.3.4 is that the implant drive-in is done immediately after the implant step.

Process

22. Grow a 430Å screening oxide

23. Blanket implant – species: phosphorus, dose: $7\times10^{15}cm^{-2}$, energy: 90kev

24. Implant drive-in – temperature: 800°C, time: 4hrs, inert ambient

25. BOE etch oxide

Process Development

The implant drive-in was performed immediately after the blanket implant since no LTO spacer layer would be used for the discrete accelerometers; thus, no LTO densification anneal would be performed. The drive-in was kept at a relatively low temperature for a relatively long time to obtain the same Dt as the LTO densification anneal (1000°C, 1hr) would have.

Frontside and backside metallization (steps 26–31)

The following steps metallize the frontside and the backside of the sealed cavity wafer.

Process

26. Pattern 1.4μm image reversal photoresist (AZ 5214-E) on the frontside of wafer using mask #4 ACCEL METAL

27. Descum ash for 2min

28. 50:1 HF dip for 30sec

29. E-beam evaporate 1μm aluminum on both sides of silicon wafer

30. Acetone lift-off

31. Nanostrip clean for 5min

Process Development

The first step for the frontside metallization process was to pattern a 1.4μm layer of image reversal photoresist AZ 5214-E. After image reversal resist patterning, the wafers were then subjected to a 2-min descum in an O_2 plasma. This was to make sure that the areas that are supposed to be clear of any photoresist were completely free of any resist. The wafers were dipped in a diluted HF solution to strip the native oxide layer, immediately before the metal deposition step. A layer of 1 μm-thick aluminum was first evaporated on the frontside of the wafers, then the wafers were flipped and the backside was metallized. A custom-made "flat" planetary plate was used to hold the wafers "flat and face down" in the evaporation chamber.

The lift-off of the metal was accomplished by immersing the wafers in acetone. The final step in the lift-off process was to perform a 5-min nanostrip (diluted piranha) clean of the wafers. This was to remove any remaining traces of photoresist from the wafers.

Vent hole etch (steps 32–36)

The following steps are used to pattern and etch vent holes.

Process

32. Pattern 1.1μm standard resist using mask #5 ACCEL VENT

33. Descum ash for 2min

34. Plasma etch 5μm of silicon in the vent hole area

35. O_2 plasma ash resist

36. Nanostrip clean for 2min

Process Development

These process steps were used to pattern and etch vent holes. The first step in this process was to pattern the vent holes. A double-thickness resist layer was used (2.2μm). The patterned wafers were then etched in a SF_6/CCl_4 plasma in the plasma etch chamber for about 15 minutes. This resulted in 5 μm-deep vent holes. It must be noted that the

etch depth of 5μm is half the thickness of the device layer. Hence during the final structure-release step (which also etches the pre-etched vent holes) the vent holes are punched through in about half the time it takes for the microstructure to be released. This ensures pressure equalization across the microstructures during the release step. After the etch the photoresist was ashed in an O_2 plasma. Finally the wafers were cleaned with nanostrip for 2 minutes to completely remove photoresist from the wafer surface.

Structure-release etch and device sintering(steps 37–41)

The following steps are used to release the accelerometer structure using a Surface Technology Systems (STS) densified plasma etching/deposition process.

Process

37. Pattern 1.1μm standard resist using mask #3 ACCEL STRUCTURE

38. Descum ash for 2min

39. STS plasma etch 10μm of silicon to release the microstructure

40. O_2 plasma ash resist (twice)

41. Sinter the aluminum metal – temperature: 450°C, time: 15min, inert ambient + 15min, forming gas ambient

Process Development

The wafers were patterned with the structure release mask (mask #3 ACCEL STRUCTURE). These processing steps were used to release the accelerometer structure using an STS densified plasma etching/deposition process. The etch depth was 10μm, which is the thickness of the desired accelerometers. The plasma chemistry is SF_6/C_4F_8 (100sccm:80sccm). The STS plasma etching system provides an etching-deposition-etching process to ensure a 90° sidewall angle. Furthermore, the selectivity to resist is approximately 85:1 or higher, and the etch lasted for about 13mins, including 1.25mins of overetch time. Since there was some variation in the etch rate across the wafer, 1.25mins of overetch was necessary to ensure the release of all the devices on the wafers. This

densified plasma etching process had an average silicon etch rate of 1.36μm/min and a uniformity of 8.09% was measured. The STS etching system configuration and specifics are shown in Appendix B. The resulted structure is shown in Figure 4–6(d). After the etch, the wafers were ashed in an O_2 plasma for 30 minutes (twice) to remove the remaining photoresist. Please note that no wet etching chemistry should be used after the structure release since *stiction* might occur, and that is exactly what we tried to avoid.

The wafers were then subjected to a 450°C sintering step. The sintering step was performed at 450°C in a forming gas (H_2/N_2) ambient, and it helps to achieve an ohmic contact between the metal layer and the underlying silicon substrate.

It is important to point out here that due to the excellent selectivity (silicon over resist or/and oxide mask) of the STS deep silicon etch, wafers and the etching chamber should be prepared so that no "micromasking" would occur. Any resist or oxide "dust" left on the etching field would result in a tall unetched silicon column (with a diameter about 1μm). Figure 4–7 illustrates typical "micromasking" etching result. Another important point to note is that since STS deep silicon etching is performed via etch-deposit-etch sequence, "steps" can be observed on the etched vertical sidewalls. Figure 4–8 illustrates such "steps". These steps can be varied via different etching recipes, and we general choose a "smoother" yet slower etching recipe (shown in Appendix B) for our accelerometer etch.

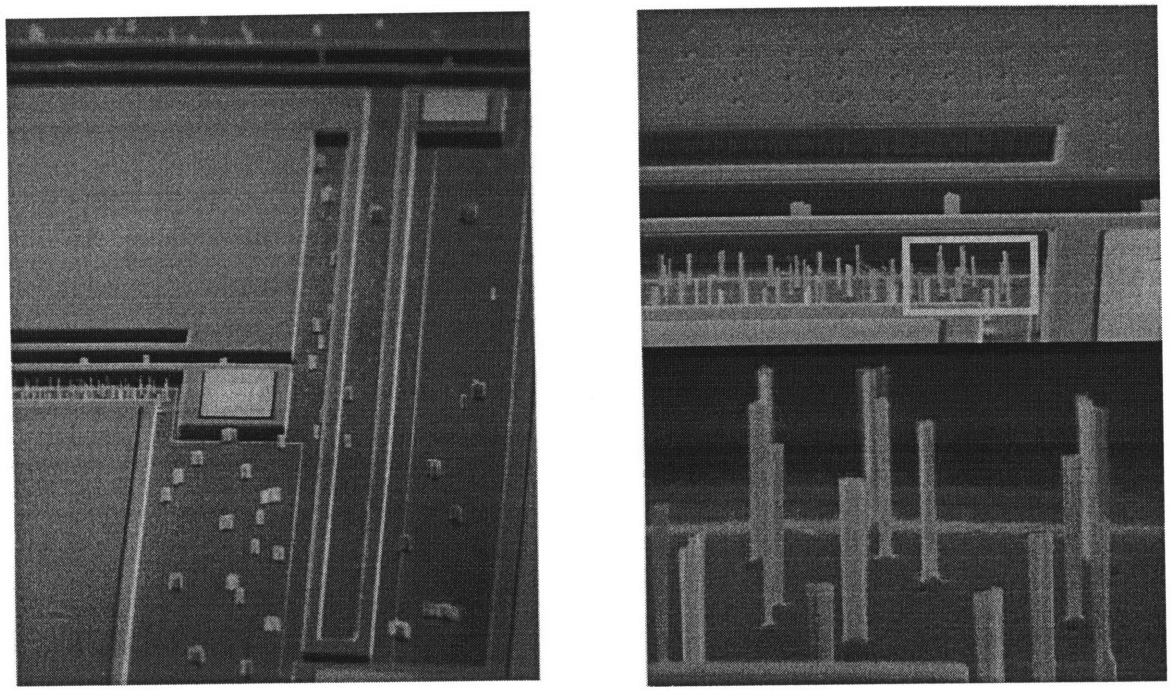


Figure 4–7: Evidence of "micromasking" during the STS deep silicon etch.

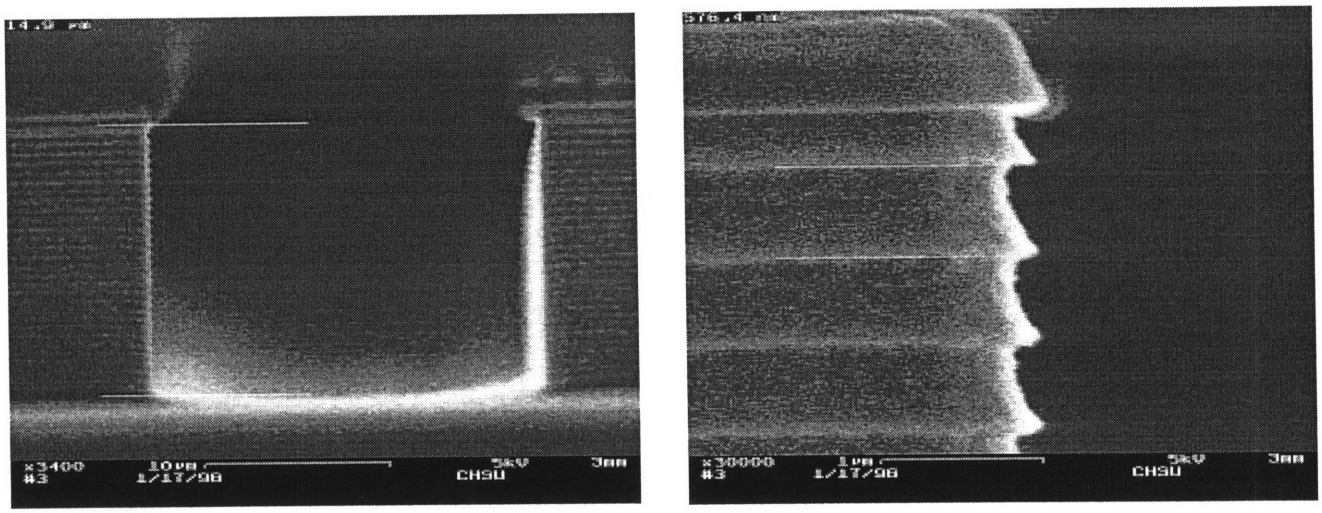


Figure 4–8: Evidence of "etch-deposit-etch" steps formed during the STS deep silicon etch.

4.5 Discussion

Hybrid-accelerometer fabrication process:

The die yield (on a wafer) for the hybrid-accelerometer fabrication process was near 100% prior to the final die-level thermocompression bond. The main factors that affected the final yield of the devices are:

1) Die separation: the hybrid-accelerometer wafers were diced partially on the back (steps 47–50) so individual chips can be separated at the end of the fabrication process. This separation process was not difficult, indeed it was quite easy to separate the dies and to prepare for the die-level thermocompression bonding process. However, since the chips could not be "wet" cleaned further, silicon dusts generated during die separation could not easily be removed from the die surface. This particle problem severely reduced the yield. Any dust trapped between the top capping glass die and the silicon device die resulted in non-functional devices. This problem could be corrected with the proposed wafer-level thermocompression bonding technique illustrated in Figure 4–5.

2) Stitch bonding: electrostatic discharge (ESD) damaged quite a few of the IC chips (designed by Ashburn and fabricated by Mosis) before the ESD problem was corrected. Accordingly, those dies which were functional after the thermocompression bonding process rendered useless when they were wire bonded to damaged IC chips. The resultant stitch-bonded hybrid accelerometer is shown in Figure 4–9. Only a few chips survived all the fabrication (including stitch bonding) processes, and the limited testing results will be presented in Chapter 5.

Discrete accelerometer fabrication process:

The die yield for the dielectrically isolated discrete accelerometer fabrication process is again nearly 100% prior to the die separation and packaging. The biggest problem associated with the process flow shown in this chapter is the difficulty in die separation.

To avoid stiction, diesaw was not employed to dice the processed wafers. Instead, hand cleaving of the wafers was performed to separate the chips. It was not extraordinarily difficult to do, and we had relatively successful results to prove the feasibility of such "manual" process. However, silicon dusts generated during the cleaving process might get stuck between the proof mass and the bottom electrode (the substrate) rendering the device useless. Successfully fabricated and tested discrete accelerometers are illustrated in Figure 4–10.

A *wet* release (solvent release) die separation technique is proposed in Appendix B and has been tried on a few wafers during the course of this research. The yield of the discrete accelerometer was again near 100% when this technique was employed. It must be noted that this die separation issue is critically important to the successful manufacturing of the accelerometers when the fabrication processes shown in this chapter is employed by industry.

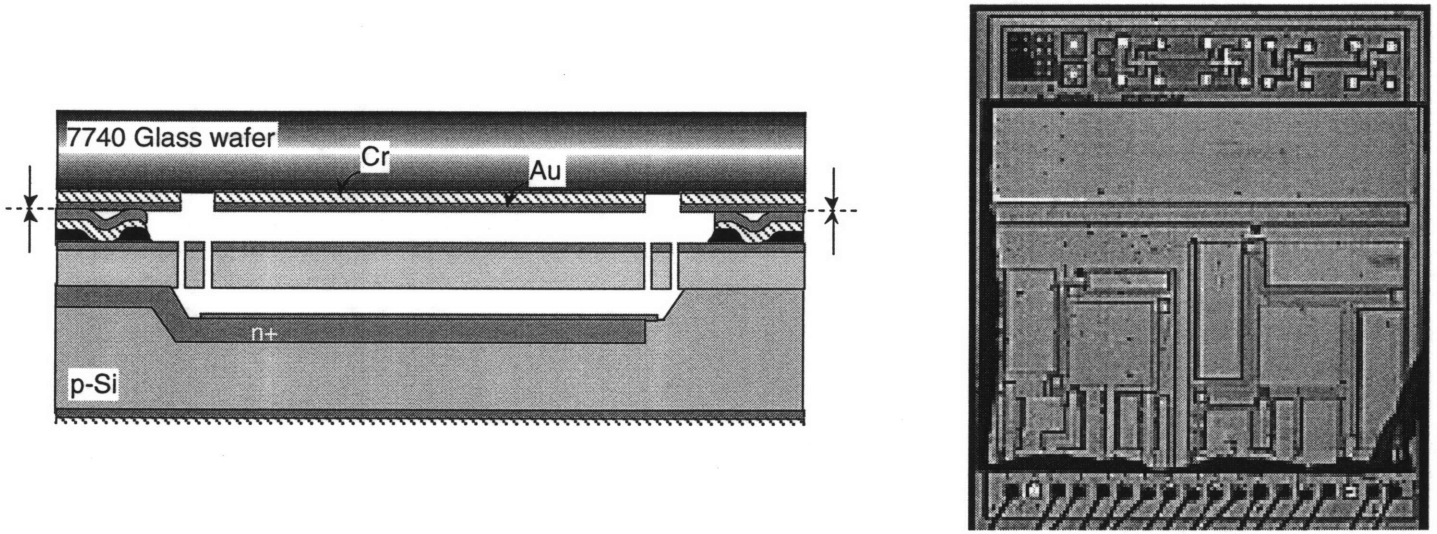


Figure 4–9: A successfully fabricated hybrid accelerometer microstructure.

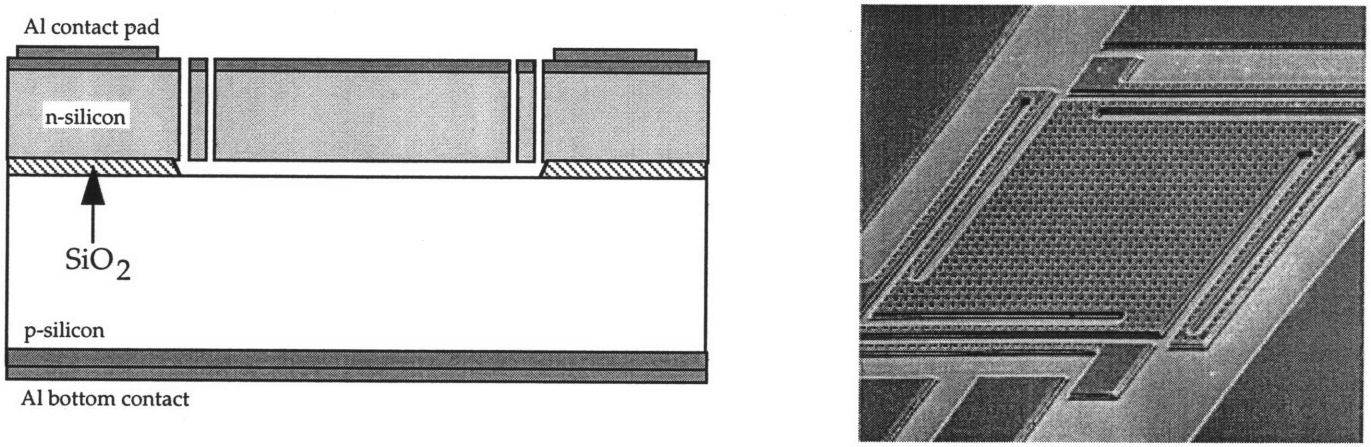


Figure 4–10: A successfully fabricated dielectrically isolated accelerometer microstructure.

Chapter 5
Device Testing

5.1 Overview

The goal of this chapter is to describe the tests used to verify and characterize the functionality of the accelerometer structures. The experimental results of these tests are compared with the initial analytical and finite-element calculations to examine the models and assumptions which were used for the sensor design process.

The testing of accelerometers can be separated into two categories: static tests and dynamic tests. Static tests can give initial verification of the functionality of the accelerometers (even before packaging, in the case of the electrostatic pull-in test), and they help measure critical device parameters such as tether stiffness (K_{sp}) and DC sensitivity (i.e., $\frac{\Delta C}{g}$). Dynamic tests look extensively at the accelerometer's response as a function of frequency for sinusoidal acceleration inputs. Discrete dielectrically isolated accelerometers are tested first and presented in the following sections. A brief summary

describing the testing results of hybrid-accelerometers stitch-bonded with a custom-designed detection chip is presented at the end of this chapter.

5.2 Preliminary Electrical Tests

The electrical functionality of the microaccelerometers and other electrical test structures were first examined by conducting electrical probe measurements at the full-wafer level. After these initial tests, the wafers were cleaved or sawed into individual dies, and additional tests were conducted on released and packaged accelerometer microstructures.

5.2.1 Low Impedance Contacts

One of the first testing concerns was to verify that good electrical contact to the membrane n-type silicon surface (the accelerometer itself) could be established. The test was conducted on a Wentworth (Model #MP0920) probe-station. When two probes were simultaneously contacted onto the metal (Al) surface of one of the large capacitors (500μm×500μm), an inter-probe resistance of $\leq 2.5\Omega$ was measured using a Keithley 175 multimeter. A merged cross-bridge van der Pauw/cross-bridge Kelvin resistor structere (shown in Figure 5–1) was fabricated along with the accelerometers. Using this structure, sheet resistance, as well as linewidth information on the 10 μm-thick bonded silicon layer could be extracted. In addition, contact resistance information could be extracted from the

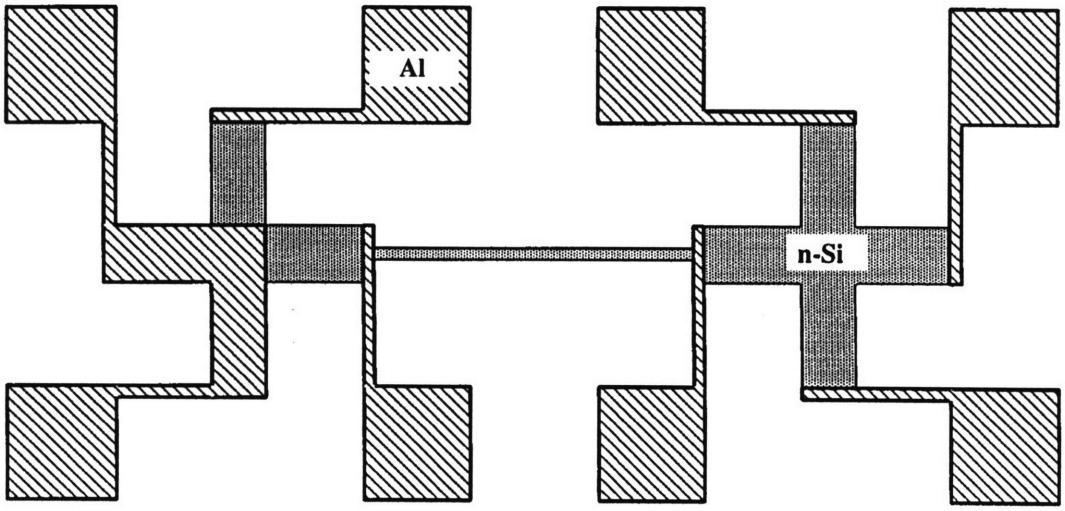


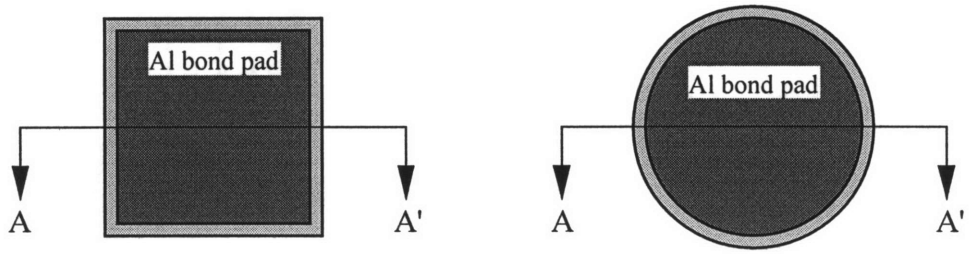
Figure 5–1: Schematic of merged cross-bridge van der Pauw/cross-bridge Kelvin resistor structure for measuring sheet resistance, linewidth, and contact resistance.

Kelvin resistor portion of the structure. The sheet resistance of approximately 18Ω/□ for the n^+ doped silicon bonded layer was measured. Furthermore, the contact resistance (metal to n^+ diffusion) of ≤ 22Ω was measured using the test structure. These measurements verify that good ohmic contact to both the n-type silicon surface and the sintered metal contacts could be established.

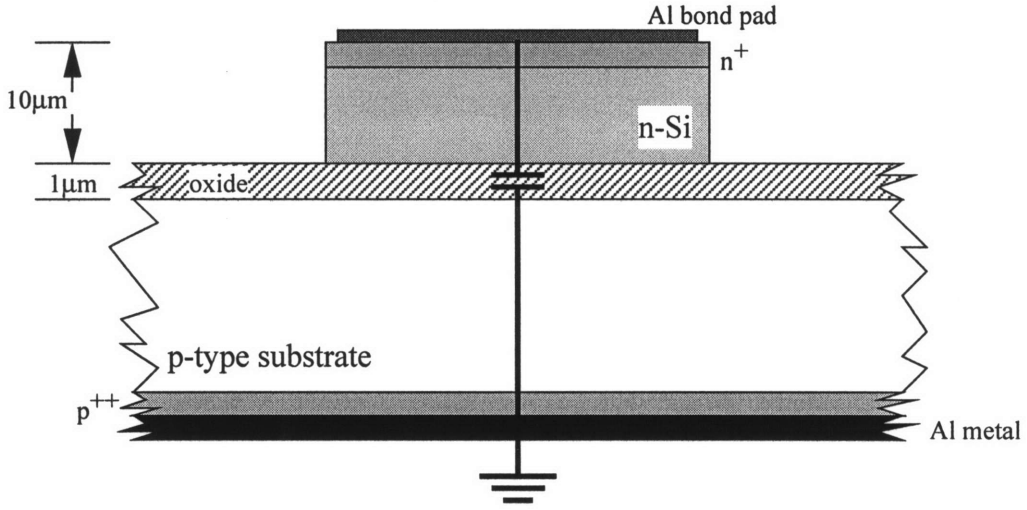
5.2.2 SOS Dummy Capacitors

After verifying ohmic contacts to the membrane silicon, capacitance measurements were conducted at full-wafer level on the SOS (silicon-oxide-silicon) dummy capacitors as shown in Figure 5–2. Capacitance measurements were taken on a Hewlett-Packard capacitance meter (HP4280A) which uses a 30mV RMS ac signal at 1MHz. Before measuring a device, parasitic cable inductances and capacitances were canceled out from the measurement using an auto-calibration procedure. Measurements were taken on a number of dies from two separate wafers; each die has a total of six capacitors being tested. Table 5.1 summarizes the results of measurements of the dummy capacitors. Note that two sets of measurements were made: one on two wafers without the anti-stiction oxide bumps (oxide thickness is ≈ 1.00±0.01μm) and the other on two wafers with the anti-stiction oxide bumps (oxide thickness is ≈ 1.10±0.01μm). The oxide thickness was measured via the 5-point method (described in Chapter 4) using ellipsometry.

Optical linewidth measurements on structures defined with the ACCEL STRUCTURE photolithographic processing step consistently had linewidths that were within 1μm of the mask-level dimensions. All experimental capacitance values match calculated capacitance values within 2.5%. Besides the variation in oxide thickness,



(a)



(b)

Figure 5–2: (a) Plane view of wafer-bonded SOS (silicon-oxide-silicon) capacitor test structures. (b) Cross-section of SOS capacitor structures.

Table 5.1(a)

Capacitor	Calculated Value (pF)	Measured Value (pF)	"Expected" Standard Deviation (pF)
C1	19.42	19.44 ± 0.20	± 0.19
C2	8.63	8.70 ± 0.12	± 0.09
C3	2.16	2.14 ± 0.03	± 0.03
C4	15.26	15.11 ± 0.29	± 0.17
C5	6.78	6.79 ± 0.07	± 0.09
C6	1.70	1.70 ± 0.03	± 0.03

Table 5.1(a): Electrical measurement results for wafer-bonded SOS capacitors (wafers without anti-stiction oxide bumps underneath accelerometer proof mass plates).
Square capacitors: C1 = 750μm×750μm, C2 = 500μm×500μm, C3 = 250μm×250μm.
Circular capacitors: C4: r = 375μm, C5: r = 250μm, C6: r = 125μm.
5 center dies tested per capacitor type per wafer (total of 2 wafers).
Errors on measured values are ±1 standard deviations of the means. The "expected" fractional standard deviations of the means are also shown in the table.

Table 5.1(b)

Capacitor	Calculated Value (pF)	Measured Value (pF)	"Expected" Standard Deviation (pF)
C1	17.66	17.67 ± 0.22	± 0.16
C2	7.85	7.82 ± 0.10	± 0.08
C3	1.96	1.94 ± 0.03	± 0.02
C4	13.87	13.83 ± 0.20	± 0.15
C5	6.16	6.15 ± 0.10	± 0.08
C6	1.54	1.53 ± 0.01	± 0.03

Table 5.1(b): Electrical measurement results for wafer-bonded SOS capacitors (wafers with anti-stiction oxide bumps underneath accelerometer proof mass plates).
Square capacitors: C1 = 750μm×750μm, C2 = 500μm×500μm, C3 = 250μm×250μm.
Circular capacitors: C4: r = 375μm, C5: r = 250μm, C6: r = 125μm.
5 center dies tested per capacitor type per wafer (total of 2 wafers).
Errors on measured values are ±1 standard deviations of the means. The "expected" fractional standard deviations of the means are also shown in the table.

fringing effects may also make an additional contribution to the differences between the theoretical and experimentally observed capacitances.

In order to understand the error sensitivity of the measured capacitance values (and all other measured data shown in this thesis) and the propagation of errors resulted from the measurements of geometrical parameters, fractional standard deviations (or fractional errors) of the means in all reported data will be included (in a separate column, as shown in Table 5.1). Fractional standard deviations of the means are derived from statistics theory [84]:

$$\text{if } Q = a^m b^n c^p \cdots$$

$$\text{then } \left(\frac{\sigma_Q}{Q}\right)^2 = m^2\left(\frac{\sigma_a}{a}\right)^2 + n^2\left(\frac{\sigma_b}{b}\right)^2 + p^2\left(\frac{\sigma_c}{c}\right)^2 + \cdots \tag{5.1}$$

This Pythagorean sort of addition of fractional standard deviations makes them very convenient for practical calculations.

Here is an example of the method discussed above. For a rectangular SOS dummay capactiors, we may treat them simply as parallel-plate capacitors:

$$C = \frac{\varepsilon_{ox} A}{d} = \frac{\varepsilon_{ox} \cdot l \cdot w}{d}$$

$$\text{and } \left(\frac{\sigma_C}{C}\right)^2 = (1)^2\left(\frac{\sigma_l}{l}\right)^2 + (1)^2\left(\frac{\sigma_w}{w}\right)^2 + (-1)^2\left(\frac{\sigma_d}{d}\right)^2 \tag{5.2}$$

where C is the measured capacitance, l and w are the length and the width of the capacitor being measured, d is the gap distance between the two parallel plates of the capacitor, and $\varepsilon_{ox} = K_{oxide}\varepsilon_0$, where K_{oxide} is the dielectric constant of oxide and ε_0 is the permittivity of free space. ε_{ox} is known very well, but all other parameters are measured and would have their own *means* and *standard deviations*. For a square SOS dummy capacitor with $l = w$ = 750±1μm and d = 1.00±0.01μm (where the "±" in each case refers to the standard

deviation of the mean), the resulting fractional standard deviation of C (measured mean = 19.44pF) is:

$$\left(\frac{\sigma_C}{C}\right)^2 = (1)^2\left(\frac{1}{750}\right)^2 + (1)^2\left(\frac{1}{750}\right)^2 + (-1)^2\left(\frac{0.01}{1.00}\right)^2$$

$$\left(\frac{\sigma_C}{C}\right) = 0.01 \quad \text{and} \quad \sigma_C = 0.19\text{pF}$$

Thus, we may calculate the "theoretical" fractional standard deviations of our measured means for all measured data presented in this chapter by using Equation 5.1.

5.2.3 Device Packaging

After initial probing, the devices required packaging before static g flip tests or dynamic shake tests could be performed. Individual device dies were packaged in a 64-pin PGA package. The dies were bonded into the packages using H2OE silver epoxy (Epoxy Technology Inc., Billerica, MA) and were wirebonded using either an aluminum wedge bonder using 1mil (25.4μm) diameter aluminum wire or a gold ball bonder using 1mil diameter gold wire.

After wirebonding, the resistance between an accelerometer or an on-chip dummy capacitor and the substrate was again measured to check for accidental shorts or bad contact. The capacitance of the structure after packaging was also checked. Both accelerometers and dummy capacitors typically exhibited an additional 1.5–2.5pF of parasitic capacitance after being packaged.

5.3 Static Tests

There are three basic static tests that can be performed on a capacitive accelerometer. The first test is the electrostatic *pull-in* test which uses an applied voltage to simulate an applied acceleration. This test can be carried out on released accelerometers at the die level using a probe station. By measuring the nominal capacitance and the pull-in voltage, the proof mass-electrode gap spacing and overall tether stiffness (which directly influences sensitivity) can be inferred. The second class of static tests are typically referred to as a *flip test* or *tumble test*. In the most simple implementation (the flip test), the DC sensitivity of an accelerometer can be measured by aligning its sensitive axis in the same direction as gravity. When the accelerometer is aligned so that gravity pulls the proof mass toward the bottom electrode (i.e., aligned at 0°), then the accelerometer is subject to a +1g acceleration. The device can then be flipped over such that the sensitive axis is now rotated 180°, and the proof mass of the accelerometer is now under the influence of a -1g field. Because gravity varies very little as a function of location across the world [78], this is a very simple and reliable way of subjecting an accelerometer under test to a known constant acceleration.

The tumble test uses the same basic principal as the flip test, but involves mounting the test device on a dividing head which is an indexed wheel which can accurately rotate the accelerometer through earth's +1g field. The tumble test is good not only for getting very accurate low-g DC sensitivity measurements, but is excellent for looking at cross-axis acceleration sensitivity, repeatability, and drift of a device. The third type of static test involves using a centrifuge to create constant acceleration forces larger than ±1g. A centrifuge can accurately vary the static acceleration applied to an accelerometer by varying the speed of centrifuge's rotor. A centrifuge test is very good for looking at long-term drift or bias shifts in DC sensitivity of an accelerometer. For the static testing of the accelerometers in this thesis, we did not have easy access to a

centrifuge or dividing head, so our testing options were limited to the electrostatic pull-in test and the ±1g flip test.

5.3.1 Electrostatic Pull-in Test

Electrostatic pull-in is a well-known sharp instability in the behavior of an elastically supported structure subjected to parallel-plate electrostatic actuation. Because the event is sharp, accurate measurements of the actuation voltage required to reach pull-in can be easily made at the wafer level using standard electrical test equipment and a microscope. Some of the fabricated accelerometers are suspended above the substrate by a gap (without the anti-stiction oxide bumps). Rather than using a time-varying or constant acceleration input, the proof mass of the accelerometer can be deflected from its equilibrium position using an applied electrostatic force. When any potential is applied between the proof mass and the bottom electrode, an electrostatic force, which wants to narrow the gap between them, is created. As shown in Figure 5–3, when this electrostatic force is large enough, it causes the proof mass to deflect downward. At a critical "pull-in" voltage, $V_{Pull\text{-}in}$, the upper conductor becomes unstable and spontaneously collapses (or pulls-in) to the substrate. A detailed description and analysis of the pull-in test can be found in [48] and Chapter 3 of this thesis.

I-V Test

For the particular accelerometers (accelerometers without oxide anti-stiction bumps) studied here, $V_{Pull\text{-}in}$ was measured on a Wentworth probe station with a Hewlett-Packard Semiconductor Parametric Analyzer (HP4145B) configured in a "force-voltage/measure-current" mode. The HP4145B was programmed to slowly ramp the voltage on each

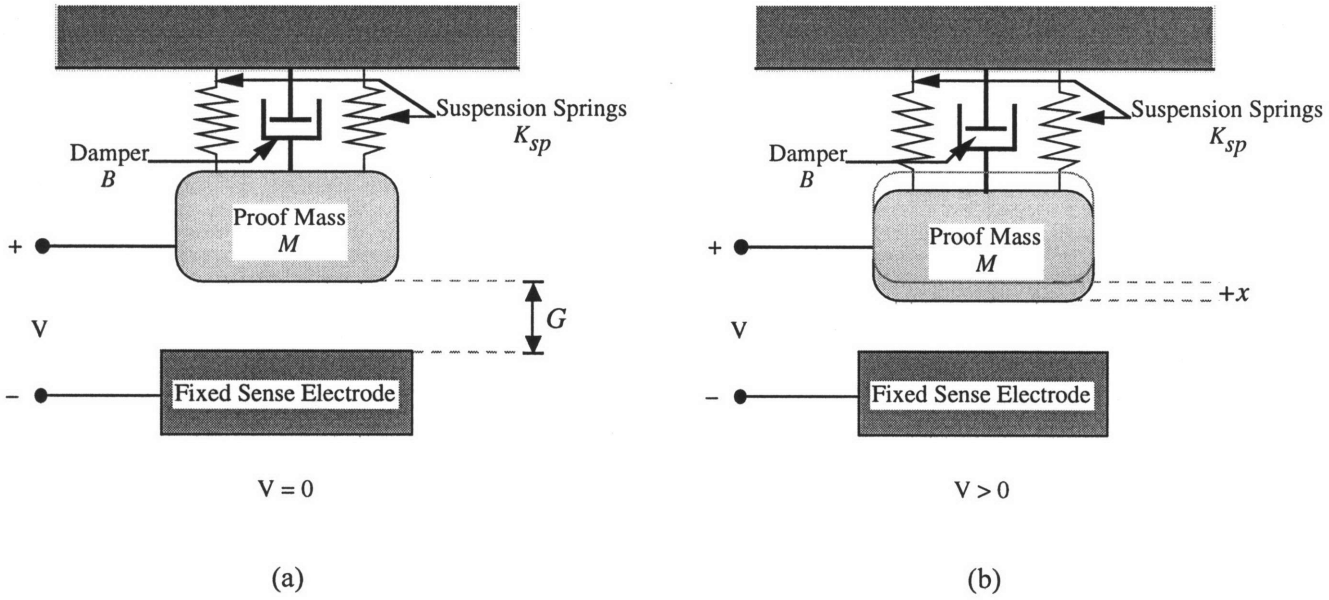


Figure 5–3: Schematic showing the effect of an electrostatic force on the accelerometer structure. (a) is the accelerometer with no applied potential between the proof mass and the bottom electrode. *G* is the initial gap spacing with no applied potential. (b) Proof mass being pulled in under the influence of an applied potential. The initial gap, *G*, has been reduced by an amount *x* by the electrostatic force created by the applied potential V.

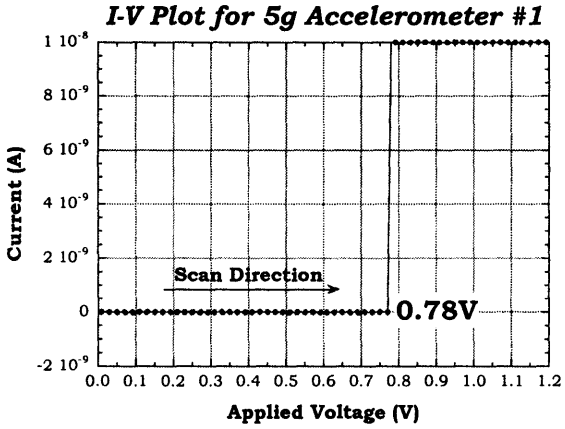
device at 0.1volt/second over a specified voltage range until pull-in is detected on the HP4145B I/V screen output interface as a sudden step in the current (see typical data in Figure 5–4). For the accelerometers studied in this work, the upper movable proof mass is n-type material while the underlying fixed ground plane is p-type. The measurement must be made with the moving proof mass negative so that accumulation layers form on the semiconductor surfaces. If depletion of either conductor occurs, then a correction to the measured $V_{Pull\text{-}in}$ would be needed to account for the field penetration into the semiconductor. Because the onset of pull-in is very sharp, the accuracy of the measurement is determined by the voltage ramp step increment, which was 10mV or less in our experiments. Please note that since there are no anti-stiction oxide bumps present in those particular accelerometers, some proof masses were shorted to and stuck down to the substrate after the pull-in experiment; thus, the pop-up experiment was ill-defined and was not conducted for those accelerometers. However, this I-V pull-in test demonstrated the functionality of the fabricated discrete accelerometers. The testing results are summarized in Table 5.2.

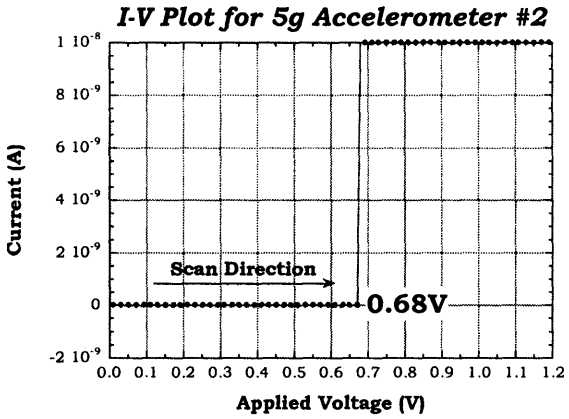
It is important to note that the accelerometers subjected to this I-V pull-in test were fabricated with damping control aperture design *version 1* as shown in Figure A–8 while all other accelerometers tested in this chapter were fabricated with damping control aperture design *version 2* as shown in Figure A–9.

C-V Test

Another initial test of the mechanical functionality of the released accelerometers was conducted by doing a capacitance-voltage (C-V) test. This test is especially useful for those accelerometers fabricated with anti-stiction oxide bumps underneath the proof mass plates since I-V test cannot be easily applied.

The electrostatic force (F_{elec}) created by the applied voltage is balanced by the restoring spring force (F_{spring}) of the tethers.





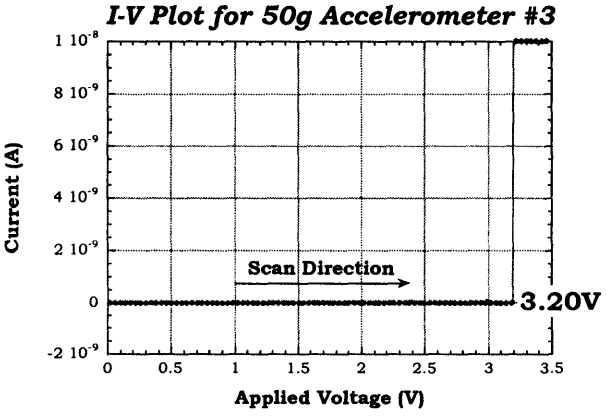


Figure 5–4: Electrostatic pull-in I-V test results for three different accelerometers.

Table 5.2

	$\lvert V_{Pull\text{-}in} \rvert$ *(volts)*		
	Calculated Value	***Measured Value***	***"Expected" Standard Deviation***
5g Accel #1	0.77	0.76 ± 0.02	± 0.01
5g Accel #2	0.66	0.66 ± 0.02	± 0.01
50g Accel #3	3.21	3.22 ± 0.02	± 0.05

Table 5.2: Table of experimental pull-in (I-V) voltages for three types of accelerometer structures (without anti-stiction oxidebumps underneath the proof mass plates). 10 devices tested per accelerometer type for pull-in measurement. Errors on measured values are ± 1 standard deviations. Calculated pull-in values have been verified with MEMCAD 3.0.

$$F_{spring} = -K_{sp}x;\ C = \frac{\varepsilon_0 A}{(G-x)} \tag{5.3}$$

$$F_{elec} = \frac{1}{2}\frac{\partial C}{\partial x}V^2 = \frac{1}{2}\frac{\varepsilon_0 A V^2}{(G-x)^2} \tag{5.4}$$

K_{sp} = total linear spring constant of the parallel tethers
V = applied voltage between proof mass and bottom electrode
G = initial gap between proof mass and bottom electrode
A = area of the proof mass
ε_0 = permittivity of the air in the gap
x = distance the proof mass has deflected from its equilibrium position

The pull-in voltage can be calculated by equating the electrostatic force and spring force (i.e., assuming no other external forces act on the system) and solving for the roots of the resulting nonlinear differential equation. The equation has been presented in [48] and in Chapter 3 and is repeated here for completeness.

$$\left|V_{pull-in}\right| = \left[\frac{K_{sp}\left(\frac{2}{3}G\right)^3}{\varepsilon_0 A}\right]^{1/2} \tag{5.5}$$

From Equations 5.4 and 5.5, one can see that, due to the non-linear nature of the electrostatic force, the proof mass pulls in completely when the electrostatic force-induced deflection has reduced the initial gap to $\frac{2}{3}G$. The pull-in voltage ($V_{pull\text{-}in}$) for a structure is easily identified by conducting a capacitance-voltage (C-V) scan and observing the voltage at which a sudden jump in capacitance occurs.

The pull-in voltage, as described in Equation 5.5 was derived under the assumption that the proof mass was being pulled in from an initial gap spacing G. However, when the proof mass is *initially* pulled in, the initial gap spacing is *fixed* at G' (e.g., accelerometers with oxide anti-stiction bumps shown in Figure 5–5(b)). Because

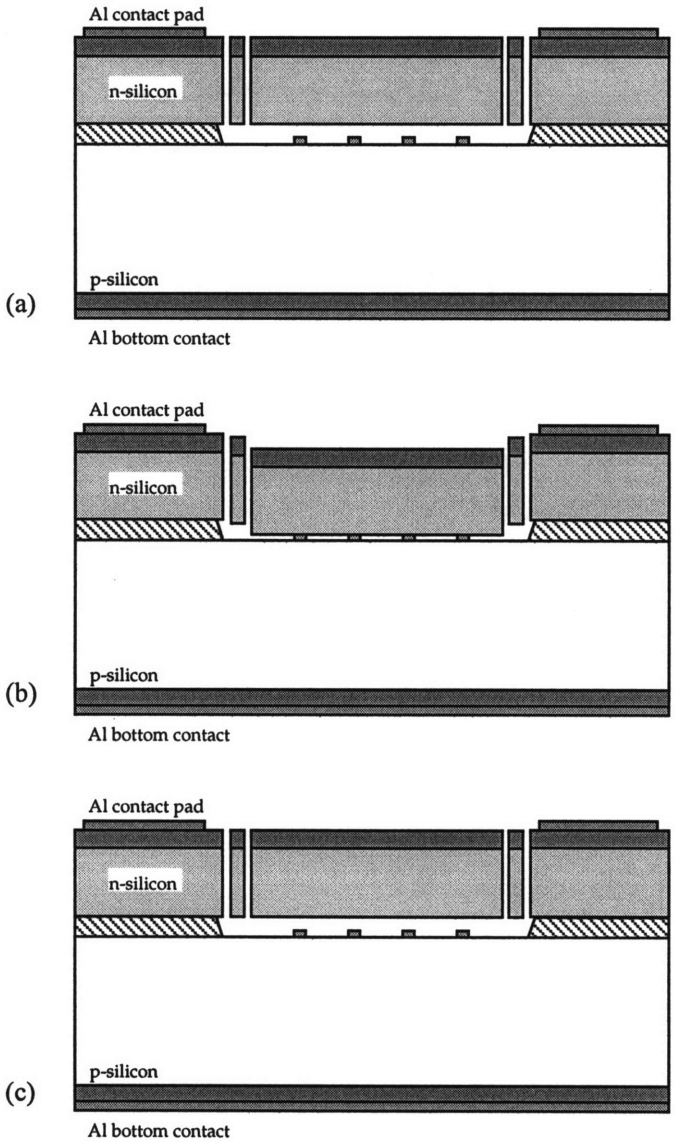


Figure 5–5: Cross-sectional schematic of an accelerometer undergoing deformations due to the effects of electrostatic pull-in: (a) the accelerometer in its undeflected state (V = 0). The initial gap spacing is G. (b) Schematic of the accelerometer after an applied bias $V \geq V_{pull\text{-}in}$ causes the proof mass to pull in and to rest against the oxide anti-stiction stubs. The new gap spacing is now G', the thickness of the anti-stiction stubs. (c) The accelerometer pops back to its undeflected state when the electrostatic force becomes less than the restoring spring force.

$G' < G$, then for the same applied bias, the electrostatic force for the smaller gap spacing (G') is much larger. Indeed, because the proof mass has already pulled in, then $G' < \frac{2}{3}G$. The proof mass will pop-up when the electrostatic force becomes less than the restoring spring force.

The spring force is also known. Since the proof mass is clamped down, we know that the spring has been deformed by an amount $\Delta x = (G - G')$. The expected pop-up voltage, $V_{pop\text{-}up}$, can be calculated by replacing the term (G–x) in Equation 5.4 with G' and replacing the term x with (G–G') in Equation 5.3. Re-deriving the equation one finds

$$|V_{pop-up}| = \left[\frac{2K_{sp}(G-G')(G')^2}{\varepsilon_0 A}\right]^{1/2} \tag{5.6}$$

It is important to note that special care should be observed for sample storage and during testing. The samples should be stored in either a continuous-nitrogen-flowing dry box or in vacuum to ensure the complete dryness of the samples. The probe station should be enclosed in a continuous-nitrogen-flowing chamber to avoid possible stiction between the proof mass and the anti-stiction oxide bumps during the C-V test. Furthermore, the time in transporting the samples from the dry box to the probe station should be kept to a minimum to further ensure the integrity of the measured data. Finally, a 30-minute bake of the samples in a continuous-nitrogen-flowing oven at 120°C may be used to "re-condition" the samples for further testing even when "stiction" was observed.

Electrostatic pull-in voltages were measured using the HP4280A C-V meter (using a 30mV RMS ac signal at 1MHz) controlled by a Dell Pentium–200 computer running Windows 95 and LabVIEW 4.0. LabVIEW programs were written to scan the applied potential between the accelerometer proof mass and bottom electrode while measuring the corresponding capacitance. For the 5g accelerometers, voltages were typically scanned between 0.0V and +1.5V (in 20mV steps) with the proof mass referenced to the negative terminal and the driven bias being applied to the bottom electrode. A 750ms delay at each

voltage point was implemented to make sure the structure had reached equilibrium before moving on to the next voltage point. Figure 5–6 is a plot of three consecutive C-V scans performed on one of the 5g accelerometers (type Accel #1).

As expected, there is a gradual increase in capacitance as the gap between the proof mass and bottom electrode is decreased. A sharp jump in capacitance occurs when the applied voltage exceeds $V_{pull\text{-}in}$. At this point, the proof mass has been pulled down until its bottom surface rests against the oxide anti-stiction bumps. Figure 5–7 is another C-V scan on the same device, but in this case, the applied bias was scanned from 0.0V to +1.5V and back to 0.0V. To evaluate the dependence of the C-V measurement on scan direction, a second scan was applied to the accelerometer, this time the applied bias was scanned from +1.5V to 0.0V and back to +1.5V. By starting the scan at +1.5V, the accelerometer's proof mass was initially pulled-in. The proof mass poped up as the applied voltage difference (relative to the negative terminal) was reduced as the applied bias approached 0.0V. As applied bias continued to scan past 0.0V to larger positive voltages, the proof mass was again pulled in. A third scan, from 0.0V to +1.5V and back to 0.0V (same as the first scan), completed the C-V measurement for the accelerometer. Close inspection of Figure 5–7 reveals that there is an asymmetry in the C-V scan. The absolute value of the pull-in and pop-up voltages are different. Experimental data of this hysteresis phenomena in electrostatically deformed microelectromechanical structures has been reported in a few papers in the literature [70–72]. However, this hysteresis behavior has been well predicted using numerical simulation, MEMCAD 3.0 FEM simulation, and can be explained by re-examining the force equations used to derive the pull-in voltage [73] as shown previously (Equations 5.5 and 5.6). The testing results for accelerometers with oxide anti-stiction bumps are summarized in Table 5.3.

It is important to re-examine the effect of the oxide anti-stiction bumps might have to the pull-in/pop-up experiments. From Equations 5.5 and 5.6, we know that the measured pull-in and pop-up voltages are functions of the gap (G), the area (A), the spring constant (K_{sp}), and the permitivity of the air in the gap (ε_0). Since the total area of

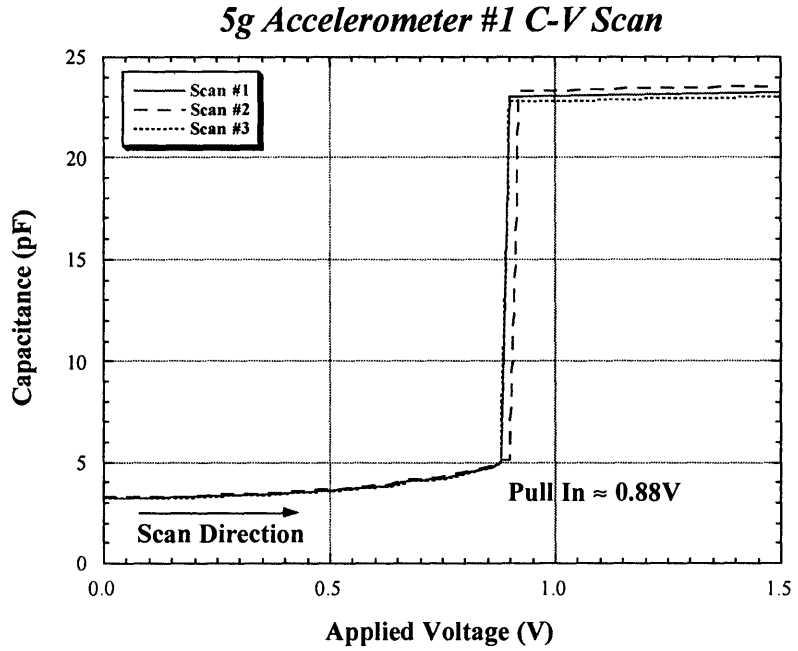


Figure 5–6: C-V plot of a 5g Accelerometer #1 folded pinwheel tether accelerometer demonstrating pull-in. Three consecutive scans on the same device.

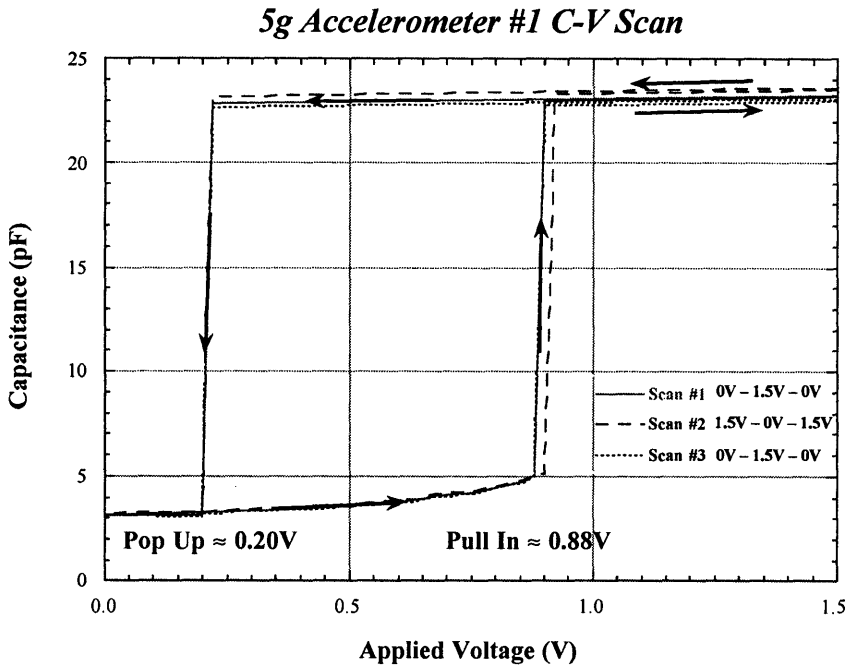


Figure 5–7: C-V plot of the same device. Applied voltage was scanned in 20mV steps. Plot shows histeresis in recovery (pop-up) of device after being pulled in.

Table 5.3

	$\lvert V_{Pull\text{-}in} \rvert$ (volts)			$\lvert V_{Pop\text{-}up} \rvert$ (volts)		
	Calculated Value	*Measured Value*	*"Expected" Standard Deviation*	*Calculated Value*	*Measured Value*	*"Expected" Standard Deviation*
5g Accel #1	0.89	0.88 ± 0.01	± 0.01	0.20	0.20 ± 0.01	± 0.02
5g Accel #2	0.76	0.76 ± 0.01	± 0.01	0.17	0.17 ± 0.01	± 0.01
50g Accel #3	3.70	3.69 ± 0.02	± 0.05	0.83	0.82 ± 0.02	± 0.02

Table 5.3: Table of experimental pull-in and pop-up (C-V) voltages for three types of accelerometer structures (with anti-stiction oxide bumps underneath the proof mass plates). 10 devices tested per accelerometer type for pull-in/pop-up measurement. Errors on measured values are ±1 standard deviations. Calculated pull-in/pop-up values have been verified with MEMCAD 3.0.

the oxide anti-stiction bumps is only about 0.03% of the proof mass area (approximately $81\mu m^2$ *vs.* $2.65\times10^5\mu m^2$ respectively), the effect of these anti-stiction bumps should not be significant as verified by the MEMCAD simulation results shown in Table 5.3. Please note that MEMCAD 3.0 (in particular, MemBuilder and CoSolve-EM simulator) does not predict any "stiction" behavior, thus the previously mentioned sample handling and storage procedures are very important to ensure minimum perturbation to the "ideal" behavior of the device under test. In addition, the author wishes to point out that all the "calculated" values presented in Tables 5.2 and 5.3 are calculated (or simulated) using MEMCAD 3.0 with measured geometrical parameters (i.e., accelerometer overall dimensions, gap dimension, and anti-stiction oxide bump dimension) as inputs for the simulations. Thus, the calculated values presented here are considered "post-fabrication" results. However, the "measured" and the "designed" geometrical dimensions show great agreement with each other. This demonstrates that the fabrication processes presented in Chapter 4 are under enough control so "average" values for the dimensions can be used for the simulator. Furthermore, excellent agreement between the simulated and the measured results give the MEMS designers enough confidence to fully utilize MEMCAD package before actual device fabrication begins.

Another interesting observation should be reported here. Aside from the accelerometer structures (especially the dielectrically-isolated discrete accelerometers examined here) described in Chapter 4, we have also fabricated another dielectrically isolated accelerometer wafer with its cross section illustrated in Figure 5–8. The major difference between this particular accelerometer structure and the previously shown accelerometers (Figures 4–6 and 4–10) is the extra n^+ and p^+ doping (the doping level is approximately $5\times10^{19}cm^{-3}$) on the device and handle wafers respectively. These extra dopings are used to simulate "metal-like" conductor surfaces on both the proof mass and the bottom electrode. Such perfect-conductor-like surfaces are needed if we force the I-V or C-V test into the depletion region as described previously. Similar C-V scans were conducted on a few accelerometers fabricated in this fashion. This time, voltages were

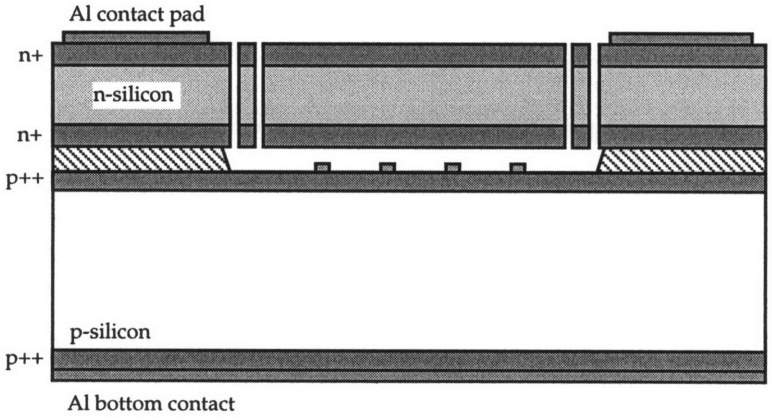


Figure 5–8: Specially designed dielectrically-isolated discrete accelerometer. Note extra n^+ and p^+ doping on the proof mass and the bottom electrode surfaces.

typically scanned between -1.5V and +1.5V (in 20mV steps) with the bottom electrode referenced to the negative terminal and the driven bias being applied to the proof mass. A 750ms delay at each voltage point was implemented to make sure the structure had reached equilibrium before moving on to the next voltage point. Figure 5–9(a) is a plot of two consecutive C-V scans performed on one of the 5g accelerometers (type Accel #1). The first C-V measurement scanned the applied potential from -1.5V to +1.5V while the second curve scanned the applied potential from +1.5V to -1.5V. The depletion effect was quickly calculated and the results were combined with MEMCAD simulation to give us the predicted device behavior. Please note that this depletion effect is more pronounced for the 50g Accel #3 since the pull-in and pop-up potentials are generally larger than its 5g counterparts. Figure 5–9(b) illustrates a typical C-V plot for Accel #3, where the depletion effect can be observed from the hysteresis and the dependence on the scan direction.

5.3.2 Accelerometer Sensitivity

A capacitive microaccelerometer responds to an input acceleration with a change in the nominal value of its capacitance. This change is read by a detection circuit which converts capacitance into an output voltage or current. The sensitivity of the total sensor system (i.e., capacitive accelerometer and detection circuitry) can therefore be defined as:

$$S_{Total} = \frac{\Delta V}{\Delta a} = \frac{\Delta V}{\Delta C}\frac{\Delta C}{\Delta a} = S_{ckt} S_{sen} \tag{5.7}$$

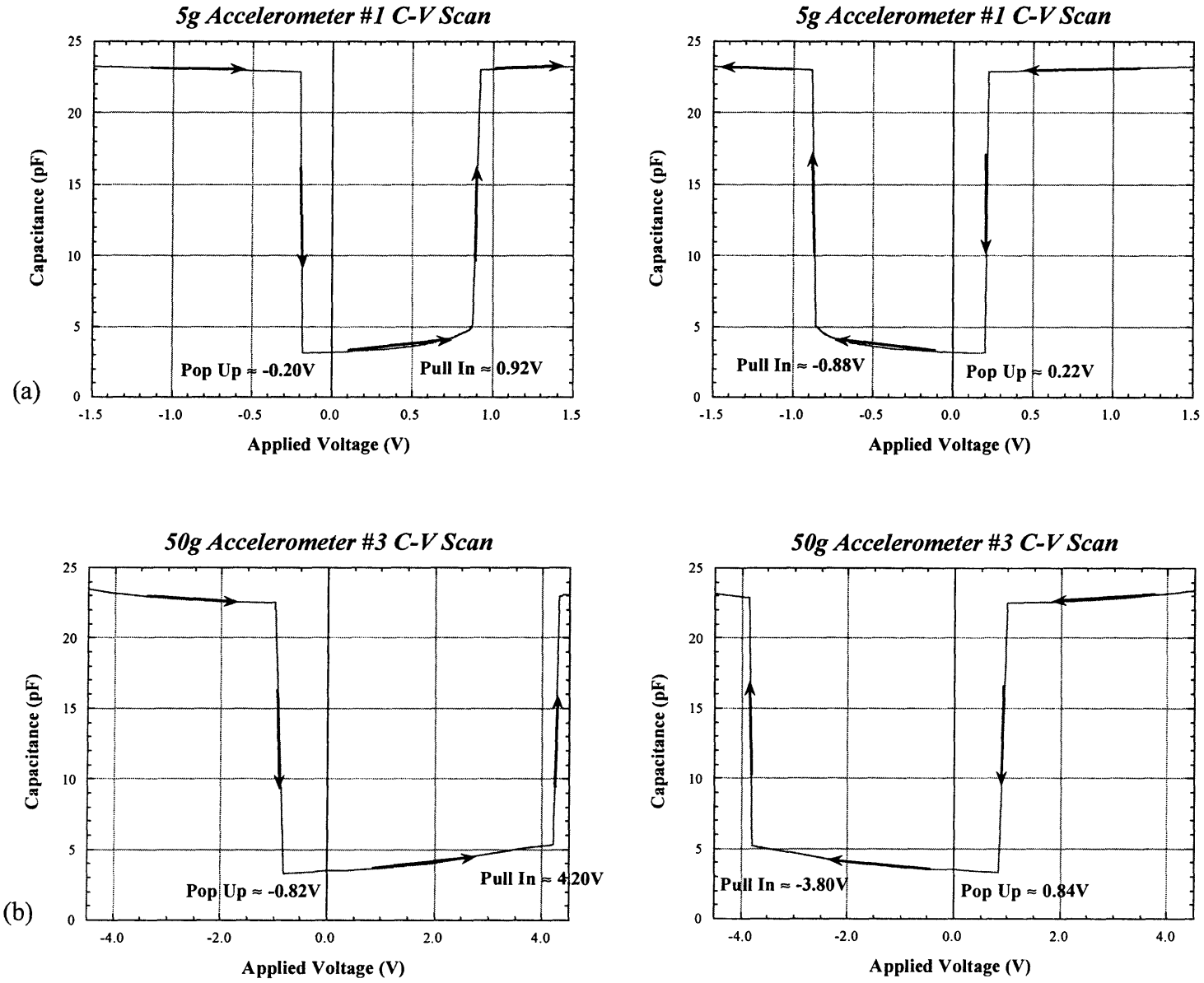


Figure 5–9: C-V scans for the dielectrically isolated accelerometers shown in Figure 5–8. (a) C-V scans for 5g Accelerometer #1 and (b) C-V scans for 50g Accelerometer #3.

where S_{ckt} is the transfer function for the detection circuitry, and S_{sen} is the transfer function for the accelerometer which can be derived from the accelerometer's physical dimensions.

An accelerometer's capacitance changes when its initial gap spacing G varies under the influence of an acceleration. The net change in capacitance for the sensor can be expressed as:

$$\Delta C = C_0\left[\frac{x}{G-x}\right] \tag{5.8}$$

where,

$$C_0 = \frac{\varepsilon_0 A}{G} \tag{5.9}$$

and G is the initial gap spacing, x is the distance the proof mass deviates from its null position, and A is the surface area of the proof mass.

In the regime of small deflections ($x << G$) where these devices typically operate, Equation 5.8 can be simplified to:

$$\Delta C \approx C_0\left(\frac{x}{G}\right) \tag{5.10}$$

From Chapter 2, we know that proof mass deflection x, is proportional to total tether stiffness, inertial mass of proof mass, and magnitude of input acceleration.

$$x = \frac{Ma}{K_{sp}} \tag{5.11}$$

Using this relationship, Equation 5.10 can be re-written as:

$$\Delta C = \frac{C_0}{G}\left(\frac{Ma}{K_{sp}}\right) \tag{5.12}$$

$$\Rightarrow \frac{\Delta C}{g} = \left[\frac{9.81\varepsilon_0 A}{G^2}\right]\left(\frac{M}{K_{sp}}\right) \tag{5.13}$$

which allows the accelerometer's sensitivity S_{sen} in pF/g to be easily calculated.

Static Flip Test

The DC sensitivity of the microaccelerometers was measured by performing a simple flip test on the accelerometers. A rotating platform, constructed from precision parts supplied by Newport, Inc., was used for the flip test. The platform can be rotated 360° about its axis with a 0.1° accuracy. Before measuring a device, parasitic cable inductances and capacitances were canceled out from the measurement using an auto-calibration procedure. The static capacitance between the proof mass and the substrate was first measured under the downward +1g earth gravity (at the 0° position). Next, the platform was rotated to the 90° position, thus the accelerometer was on its side and should theoretically experience a 0g force. Then the platform was rotated further to the 180° position, where the accelerometer under test should experience the -1g force. The platform was then rotated to the 270° position, where the accelerometer was on its side again and experiences the 0g force. To complete the flip test, the platform was finally rotated back to its original position, after a full 360° rotation, and the capacitance was measured. The capacitance values were recorded and analyzed to give the accelerometer DC sensitivity in pF/g as shown in Equation 5.11. Summary of the measured DC sensitivity for three types of accelerometers fabricated (two 5g accelerometers and one 50g accelerometer) is presented in Table 5.4.

Table 5.4

	Static Sensitivity *(pF/g)*		
	Calculated Value	***Measured Value***	***"Expected" Standard Deviation***
5g Accel #1	0.061	0.062 ± 0.001	± 0.011
5g Accel #2	0.051	0.052 ± 0.001	± 0.010
50g Accel #3	0.002	0.002 ± 0.001	± 0.0003

Table 5.4: Table of experimental static sensitivity for three types of accelerometer structures (with anti-stiction oxide bumps underneath the proof mass plates). 3 devices tested per accelerometer type for static sensitivity measurement. Errors on measured values are ±1 standard deviations. Calculated values have been verified with MEMCAD 3.0.

5.4 Dynamic Vibration Tests

The dynamic response of the accelerometers is tested by placing the devices on a *shaker* and subjecting them to known accelerations at different frequencies. A shaker (or shake table) is an electromechanical device which can vibrate or shake a device or structure with a known amount of force/acceleration.

5.4.1 Testing Apparatus

Microaccelerometers were subjected to accelerations of known amplitude and frequency using a Ling Dynamic Systems 456 Vibrator driven by a Ling Dynamics PA-1000 power amplifier. The motion of the shake table (amplitude and frequency of excitation) was varied by modulating the input of the power amplifier with a HP3314A function generator. Because the shaker is driven in an open-loop configuration, the actual amplitude of acceleration was monitored continuously with a B&K (Brüel & Kjær) 4379 Delta Shear piezoelectric accelerometer. The B&K4379 was calibrated at the factory, and has a specified sensitivity of 303pC/g. Furthermore, the certificate of calibration of the B&K4379, including the gain (gain *vs.* frequency) and sensitivity (charge sensitivity *vs.* frequency) plots, is presented in Appendix C. The output of the B&K accelerometer was amplified using a B&K2651 charge amplifier. The charge amplifier has fixed gains of 0.1, 1.0, and 10mV/pC. The output voltage of the custom-built capacitive detection circuit was measured using a Tektronix TDS540B digital storage oscilloscope. Figure 5–10 is a schematic of the dynamic vibration testing system.

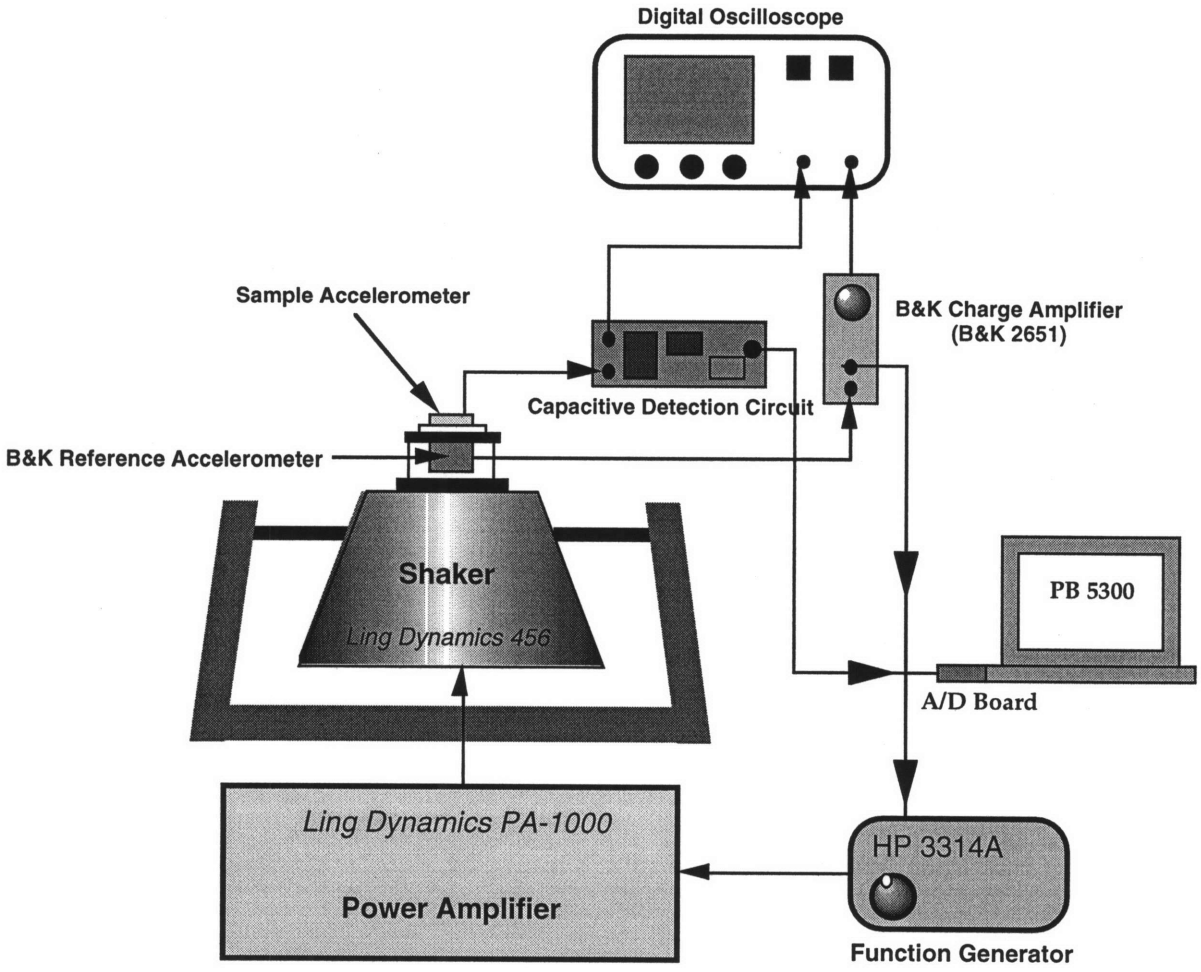


Figure 5–10: Schematic of the vibration testing system.

5.4.2 Capacitive Detection Circuit

The maximum measurement frequency of the HP4280A in the capacitance-time mode (C-t) mode is rather slow (on the order of 100Hz in burst mode), so it was necessary to design and build a capacitive detection circuit to measure the dynamic response of the accelerometer. Because the detection circuitry was implemented off-chip, it was desirable to try to implement a detection scheme which is first-order insensitive to large parasitic capacitances. In addition, the detection circuitry must be able to measure capacitance changes over the bandwidth of the system. The accelerometer itself is capable of measuring down to DC, but for dynamic tests, the low frequency limit of the system is limited by the low frequency roll-off of the shaker, which is about 30Hz. The upper frequency limit is set by the mechanical frequency response of the accelerometer and the shaker. The 5g accelerometers were designed to have a first natural resonant frequency of 3kHz while the 50g ones have a first natural resonant frequency of 15kHz. The response of the shaker is good to about 2kHz (with the aluminum platform holding the accelerometer under test and the reference B&K accelerometer attached).

A functional diagram of the selected circuit topology is shown in Figure 5–11. The circuit consists of a capacitive charge amplifier and uses synchronous demodulation and low-pass filtering to obtain a DC output proportional to the capacitance of the accelerometer. The input to the circuit is a low-level (e.g., 50-200mV) sinusoidal drive signal with a frequency significantly higher than the mechanical response of the accelerometer (e.g., >> 3kHz or 15kHz). Drive voltage levels of adequately small magnitude must be chosen so that they do not cause the accelerometer to pull-in, or appreciably reduce the mechanical stiffness of the tethers. As the proof mass displaces, it changes the value of C_s (sensor capacitance) which changes the gain of the charge amplifier. Under the influence of a time-varying acceleration input, the value of C_s, and hence the gain of the charge amplifier also changes with time. In essence, the output signal

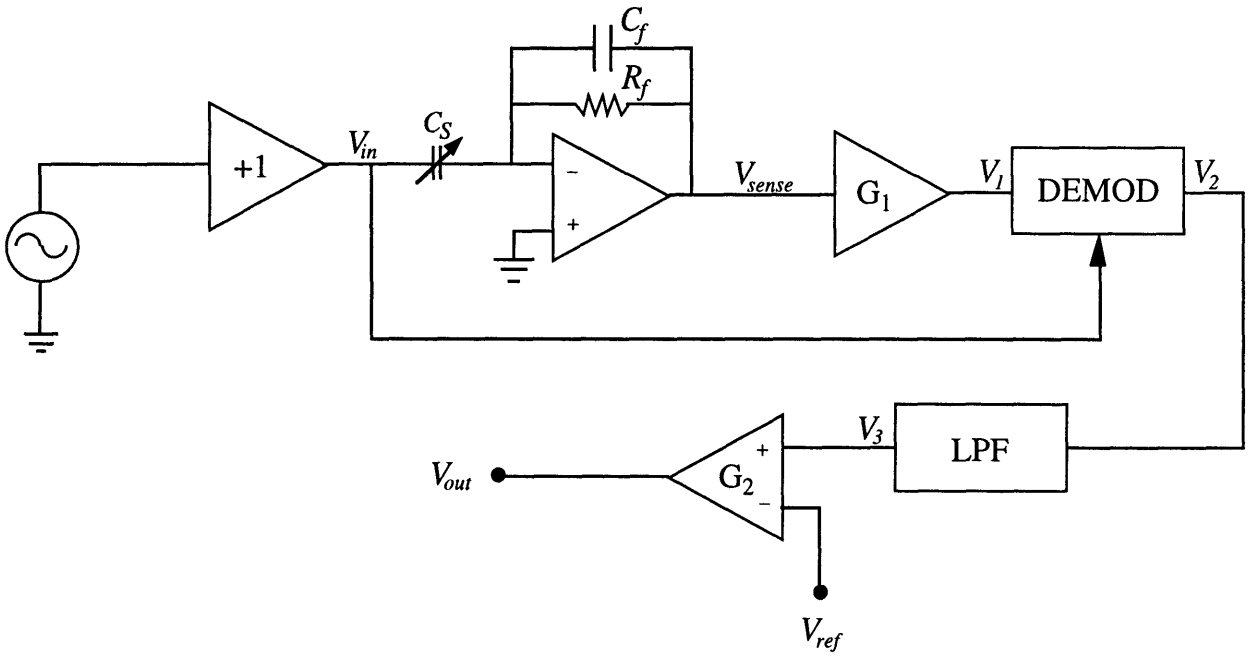


Figure 5–11: Functional block diagram of capacitive detection circuit for accelerometer. Input drive voltage is a sinusoidal with a frequency of 150kHz.

from the charge amplifier is an amplitude modulated (AM) signal with the drive signal as the carrier signal and the time-varying gain of charge amplifier performing the amplitude modulation. The output of the charge amplifier is then passed through an additional gain/buffer stage and then into a demodulator. The demodulator produces a rectified output waveform which is at twice the frequency of the original drive signal. This signal is then passed through a low-pass filter whose output is a DC voltage which is the average of the output of the demodulator. This voltage is finally passed through a differential amplifier which can be used to null out any undesirable offsets, or simply to adjust the DC voltage level of the output signal. Furthermore, additional gain may be realized through this final amplification stage.

The amplitude gain of the detection circuit (shown in Figure 5–11) can be calculated as follows:

$$\begin{aligned} &\text{let} \quad V_{in} = v_0 \sin\omega_0 t \\ &\text{then} \quad V_{sense} = -\frac{C_s(t)}{C_f} v_0 \sin\omega_0 t \quad \text{and} \quad V_1 = -\frac{G_1 C_s(t)}{C_f} v_0 \sin\omega_0 t \end{aligned} \tag{5.12}$$

where G_1 is the gain of the buffer/gain stage and ω_0 is the input drive frequency. The output of the demodulator (V_2) is given by:

$$\begin{aligned} V_2 &= -\frac{G_1 K_{dm} C_s(t)}{C_f} (v_0 \sin\omega_0 t)^2 \\ &= -\frac{G_1 K_{dm} C_s(t)}{C_f} v_0^2 \left[\frac{1}{2}(1-\cos 2\omega_0 t)\right] \end{aligned} \tag{5.13}$$

where K_{dm} is the gain of the demodulator. The output after the low-pass filter is given by:

$$V_3 = -\frac{1}{2}\frac{G_1 K_{dm} C_s(t)}{C_f} v_0^2 \tag{5.14}$$

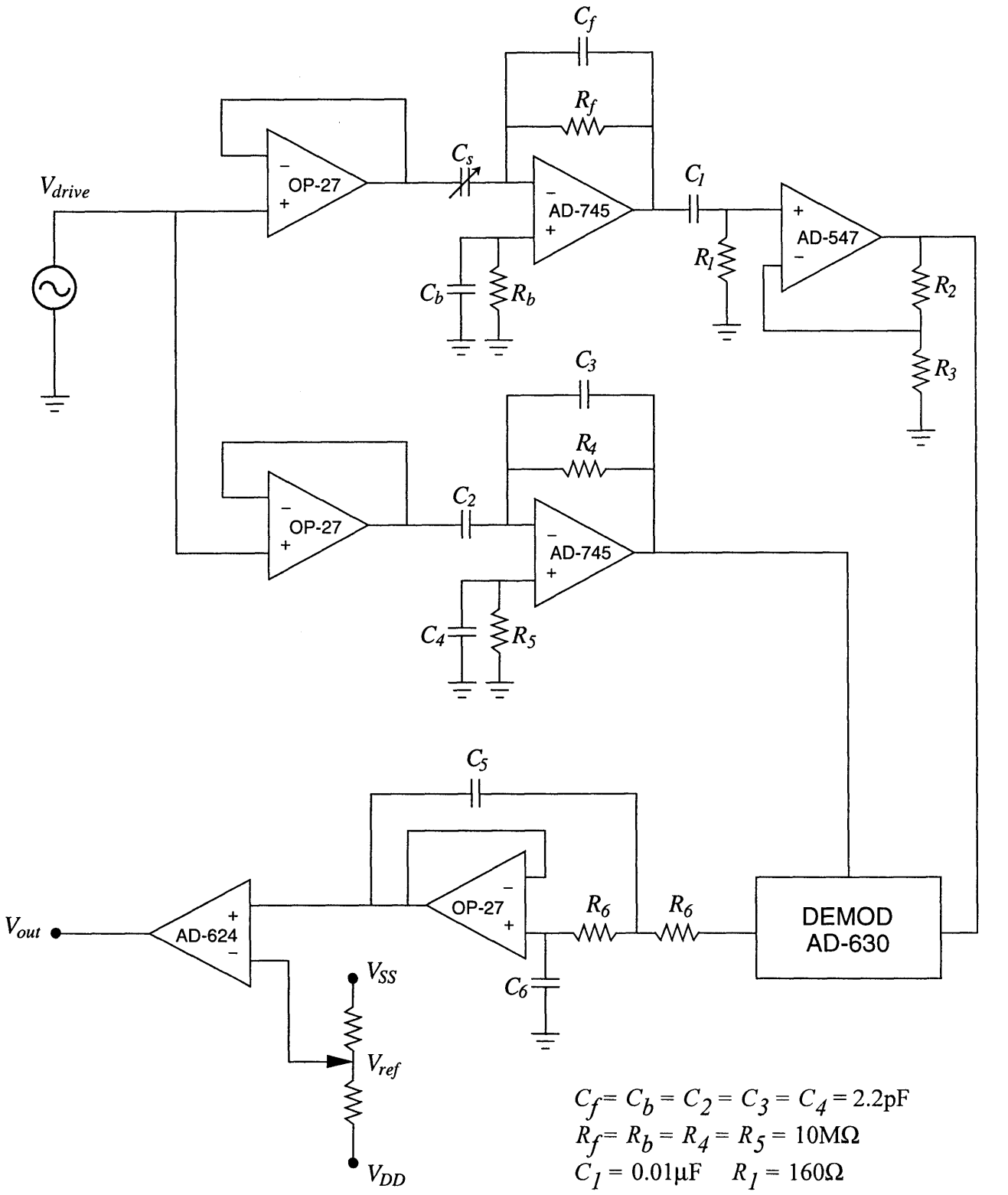
and finally V_{out} is given by:

$$V_{out} = -\frac{1}{2}\frac{C_s(t)}{C_f} G_1 G_2 K_{dm} v_0^2 \tag{5.15}$$

The amplitude gain of the detection circuit is then:

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{2}\frac{C_s(t)}{C_f} G_1 G_2 K_{dm} v_0 \tag{5.16}$$

Figure 5–12 is a more detailed schematic of the detection circuit. The input drive signal is a 50-200mV, 150kHz sine wave which comes from an external waveform generator. This signal is buffered using OP-27 ultralow noise, precision operational amplifiers (op amps). The charge amplifier was built using the AD745, an ultralow noise, high-speed, BiFET op amp. The sense capacitance C_s, has a nominal value of 4-5pF (about 1.6pF is the parasitic capacitance due to the tether pads) for the accelerometers. These values, however, increase or decrease depending on the level of acceleration input. A value of 2.2pF was chosen for the feedback capacitance C_f. R_f the feedback resistance, is nominally 10MΩ. The impedance at both inputs nodes is nominally balanced by R_b and C_b (10MΩ and 2.2pF respectively). These components are added to try and minimize bias current induced voltage offsets at the output of the op amp. The charge amplifier is followed by a passive high-pass filter formed by R_1 and C_1 network and a non-inverting op amp gain stage. The high-pass filter network is used to block any DC voltages from the charge amplifier due to residual offset voltages. An AD630 is used as the synchronous demodulator. The AD630 is used in its +2 gain configuration. The output of the demodulator is filtered with either a simple passive (R-C network) low-pass filter or a two-pole Butterworth low-pass filter. The output of the low-pass filter is finally passed through an AD624 instrumentation amplifier. An adjustable reference voltage input to the AD624 is provided by using a potentiometer. The power supply terminals of all IC's are filtered with 0.1μF ceramic capacitors and 22Ω resistors. All resistors used are 1% tolerance metal-film resistors while the capacitors are high-precision capacitors.



$C_f = C_b = C_2 = C_3 = C_4 = 2.2\text{pF}$
$R_f = R_b = R_4 = R_5 = 10\text{M}\Omega$
$C_1 = 0.01\mu\text{F}$ $R_1 = 160\Omega$
$R_2 = 20\text{k}\Omega$ $R_3 = 10\text{k}\Omega$
$R_6 = 3.75\text{k}\Omega$ $C_5 = 0.02\mu\text{F}$ $C_6 = 0.01\mu\text{F}$

Figure 5–12: Detailed schematic of the capacitive detection circuit.

Circuit Characterization

The performance of the detection circuit was verified by measuring a set of fixed capacitors. Discrete capacitors with nominal values of 10pF, 7pF, 5pF, 2.2pF, 2.0pF, and 1.0pF were measured using the HP4280A C-V meter, and then measured using the detection circuit. The circuit gave a sensitivity of 498mV/pF at an input drive amplitude of 200mV.

To examine the frequency response of the detection circuit, first, a fixed capacitor was placed in place of C_s (the accelerometer), and the input drive frequency was scanned from 145kHz to 155kHz in 1kHz interval to obtain the frequency response. The response was completely flat to the measurement resolution. Second, a fixed SOS capacitor was placed in the circuit as C_s. The SOS capacitor was then mounted on the accelerometer testing platform on top of the shaker along with the reference accelerometer (B&K4379). Both the SOS capacitor and the reference accelerometer were then shaken by sinusoidal accelerations at various g levels. The response of the SOS capacitor to sinusoidal accelerations was a completely flat line (within the measurement resolution) from 50Hz to 1.55kHz in 100Hz intervals. This measurement is important since now we have a good handle of the detection circuit performance and its frequency response before the fabricated accelerometers are tested. The results from these two experiments are shown in Figure 5–13. Please note the V_{ref} value shown in Figure 5–13 is the output voltage when the fixed discrete capacitor (or the SOS capacitor) was placed in the circuit as C_s for the calibration experiments. Since V_{out} did not change at all either when the input drive frequency was scanned from 145kHz to 155kHz (Figure 5–13(a)) or when the shaker frequency was scanned from 50Hz to 1.55kHz (Figure 5–13(b)), V_{out}/V_{ref} is 1 (or 0dB) as indicated in the plots.

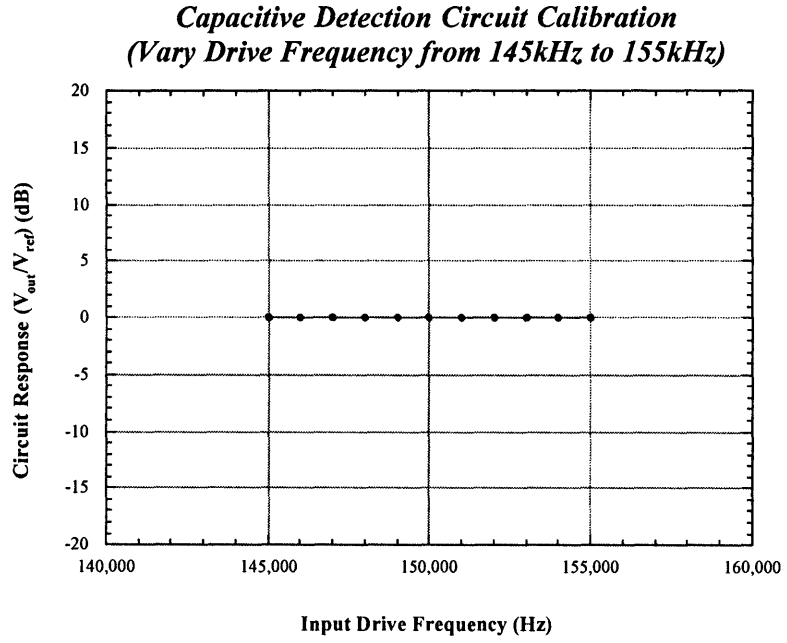


Figure 5–13(a): Capacitive detection circuit calibration: a fixed capacitor was placed in place of *Cs*, and the input drive frequency was scanned from 145kHz to 155kHz in 1kHz interval to obtain the frequency response.

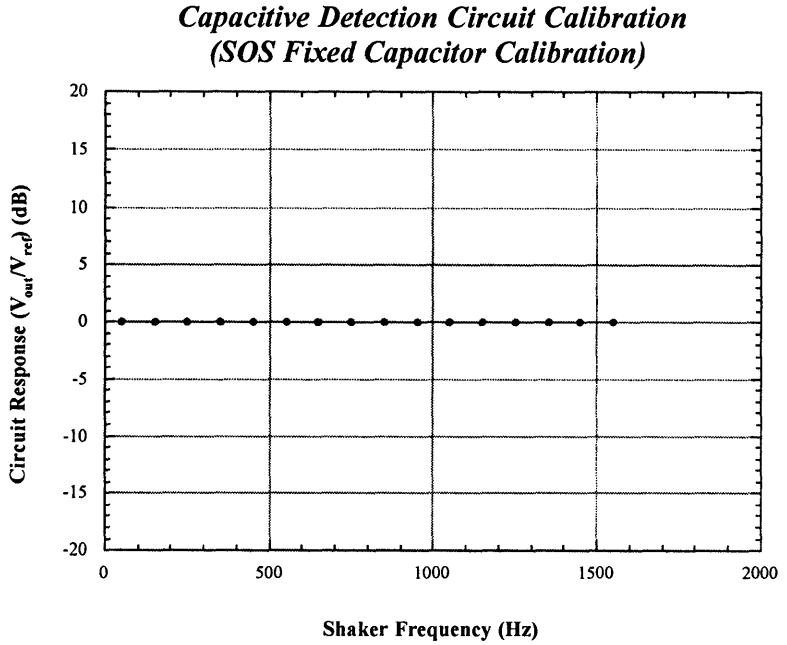


Figure 5–13(b): Capacitive detection circuit calibration: a fixed SOS capacitor was placed in the circuit as *Cs*. The SOS capacitor was then mounted on the accelerometer testing platform. The response of the SOS capacitor to sinusoidal accelerations was recorded.

5.4.3 Dynamic Device Testing

Device Sensitivity

The response of the microaccelerometers to sinusoidal accelerations was measured on the shaker at accelerations of 1g to 5g's for the 5g microaccelerometers (Type Accel #1 and Accel #2) and of 1g to 30g's for the 50g microaccelerometers (Type Accel #3). Figure 5–14 is an oscilloscope trace showing the response of the silicon microaccelerometer (top trace) compared to the B&K reference accelerometer. Both devices are being shaken at 5g's at a frequency of 750Hz. The silicon microaccelerometer appears to track the B&K reference accelerometer very well. More extensive measurements of the accelerometers amplitude response at a given frequency were taken. Accelerometers were tested at 10 different frequencies range from 50Hz to 1.5kHz; however, only three representative curves are shown in Figure 5–15 for clarity.

The 5g Accelerometer #1 shows good response, but also has an obvious roll-off in sensitivity with frequency. In addition, the sensitivity at the highest measured frequency, 1.5kHz, was only 7.3mV/g, as compared to the sensitivity of 30.6mV/g at the lowest measured frequency, 50Hz. The linearity of the sensor can be expressed as:

$$\text{Linearity} = \frac{\text{maximum deviation from the "best - fit" line}}{\text{full - scale output voltage}}$$

Despite the decrease in sensitivity at higher frequencies, the accelerometer's amplitude response remains very linear over all measured frequencies with a linearity of $< \pm 1.5\%$.

Similarly, the 5g Accelerometer #2 has a sensitivity of 26.4mV/g at 50Hz and 4.7mV/g at 1.5kHz. The accelerometer's amplitude response remains very linear over all measured frequencies with a linearity of $< \pm 1.5\%$.

The 50g Accelerometer #3 has a much lower sensitivity of about 1.06-1.08mV/g at all measured frequencies. The accelerometer's amplitude response is very linear with a linearity of $< \pm 2\%$.

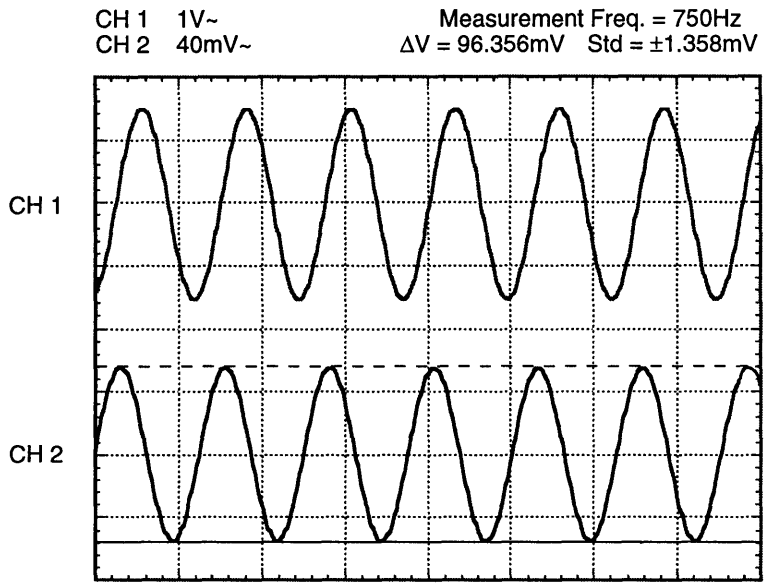


Figure 5–14: Oscilloscope trace of response of silicon microaccelerometer of a 5g sinusoidal input acceleration. Top trace (CH 1) is the output response of the reference accelerometer (B&K4379), bottom trace (CH 2) is the output response of the 5g accelerometer #1. Excitation frequency is 750Hz.

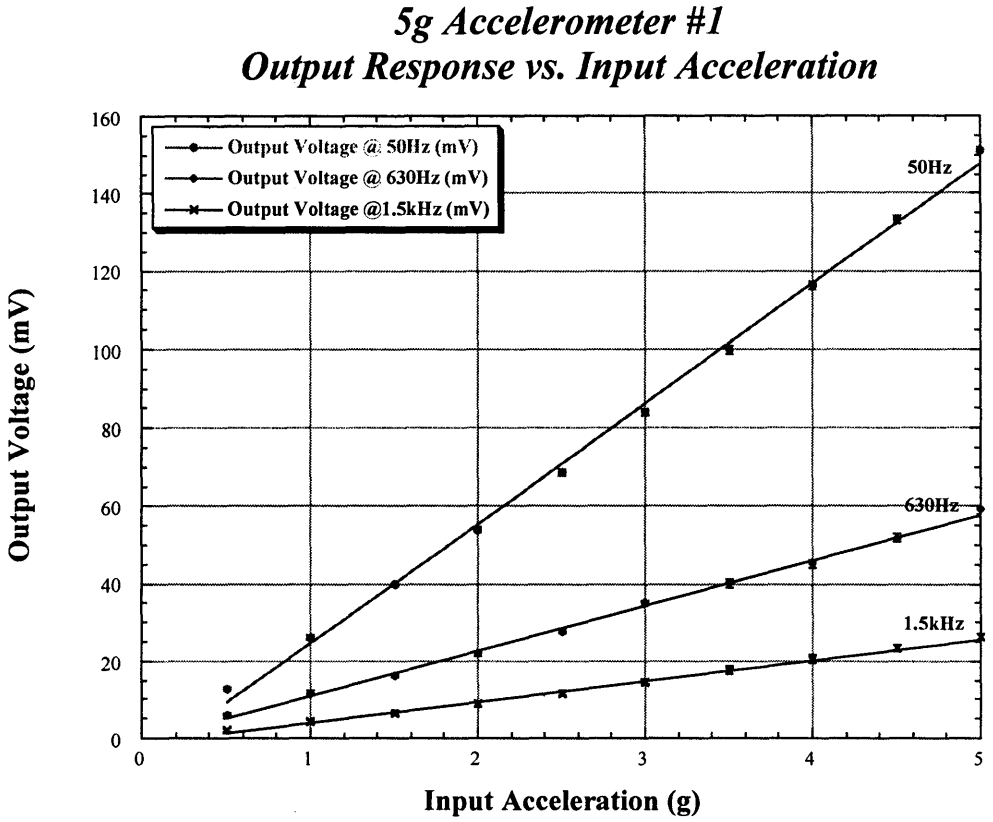


Figure 5–15(a): Output response of 5g Accelerometer #1 *vs.* input acceleration. Accelerometer's amplitude response is shown for 3 different frequencies.

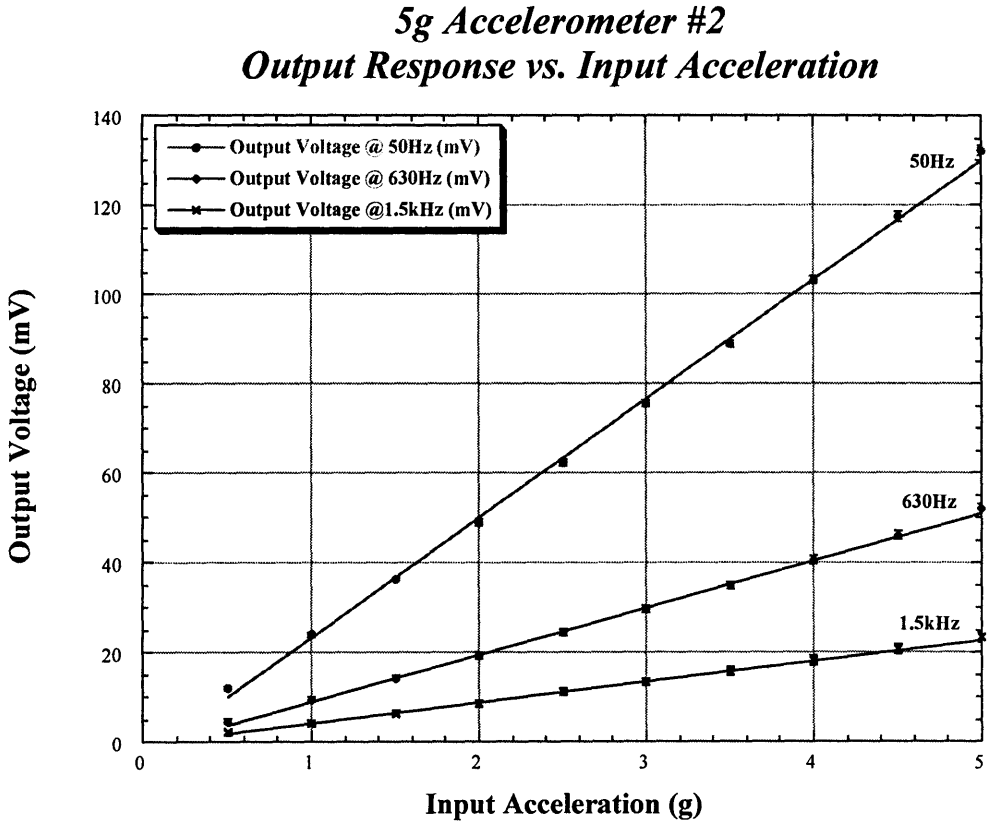


Figure 5–15(b): Output response of 5g Accelerometer #2 *vs.* input acceleration. Accelerometer's amplitude response is shown for 3 different frequencies.

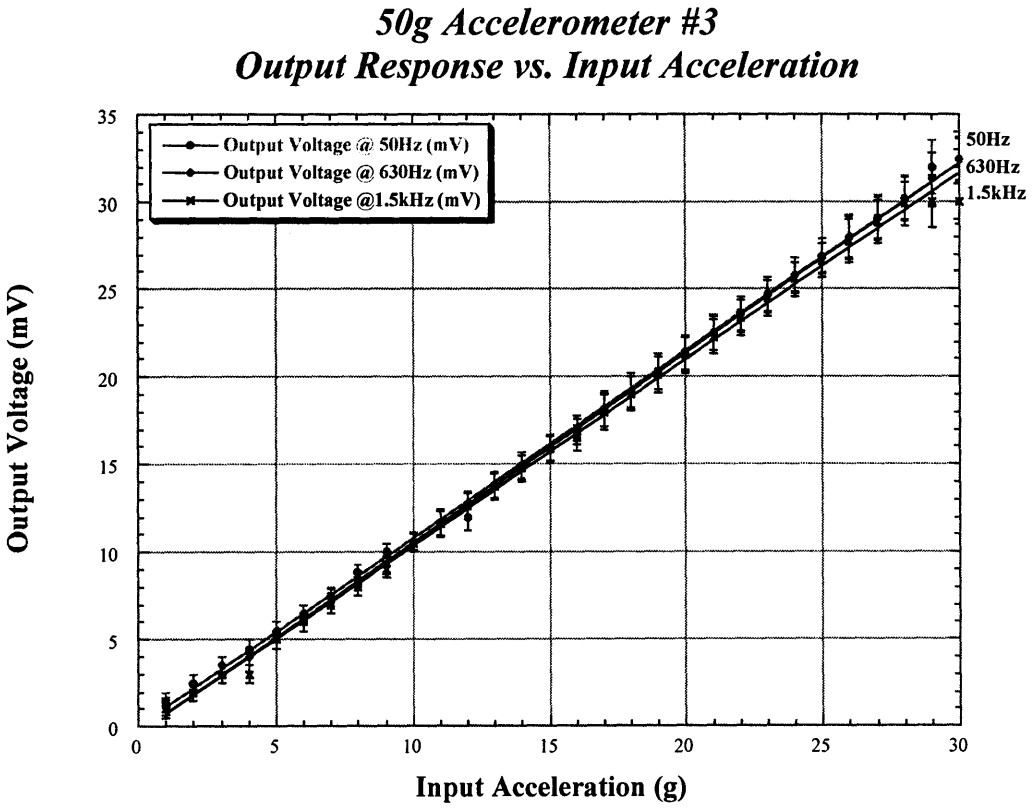


Figure 5–15(c): Output response of 5g Accelerometer #3 *vs.* input acceleration. Accelerometer's amplitude response is shown for 3 different frequencies.

Device Frequency Response

It is evident from Figures 5–15(a) and 5–15(b) that the frequency responses of the 5g accelerometers are not flat at lower frequencies. The designed damping ratios for these two types of accelerometers are 4.34 and 4.06 respectively (2-D damping model used). To illustrate this point more clearly, each accelerometer's output response is plotted as a function of frequency in Figure 5–16. In Figure 5–16(a) the measured 5g Accelerometer #1 data is plotted versus the theoretical response for the 2nd-order system. It appears that the accelerometer data makes a reasonable match to the response of the 2nd-order system with a damping ratio of 5.0 (compared to a designed value of 4.34). Clearly, the response of these devices is over-damped. However, the response of these devices is very linear, and the observed damping ratio is significantly improved over the worst-case damping for the structure (i.e., $\zeta \approx 1420$ with no damping apertures). Again, a damping ratio of 5.0 was also observed for the 5g Accelerometer #2 devices compared to a designed value of 4.06. Finally, a damping ratio of 1.0 could be fitted for the 50g Accelerometer #3 devices (compared to a designed value of 0.86). Since we only ran the vibration test to about 1.5kHz, we did not have enough data points (at higher frequency) to show the roll-off behavior modeled by the 2nd-order system illustrated in Figure 5–16(c).

The phase response plots (phase shift *vs.* frequency) for all three accelerometers are shown in Figure 5–17. It is evident in Figure 5–17(a) that the measured damping ratio for 5g Accel #1 is indeed 5.0 since the measured phase-shift data matches the $\zeta = 5.0$ curve quite well. For 5g Accel #2, the phase response plot suggests a damping ratio between 4.5 and 5.0 (shown in Figure 5–17(b)). For 50g Accel #3, as shown in Figure 5–17(c), measured phase shift data matches the $\zeta = 1.0$ curve quite well despite lack of data points beyond 1.5kHz. These phase-shift plots confirm our findings presented in Figure 5–16.

The measured damping ratio is consistently higher than that predicted by the 2-dimensional model in Chapter 2. We would expect that this difference might be attributed to 3-dimensional effects such as the flow resistance of the damping holes.

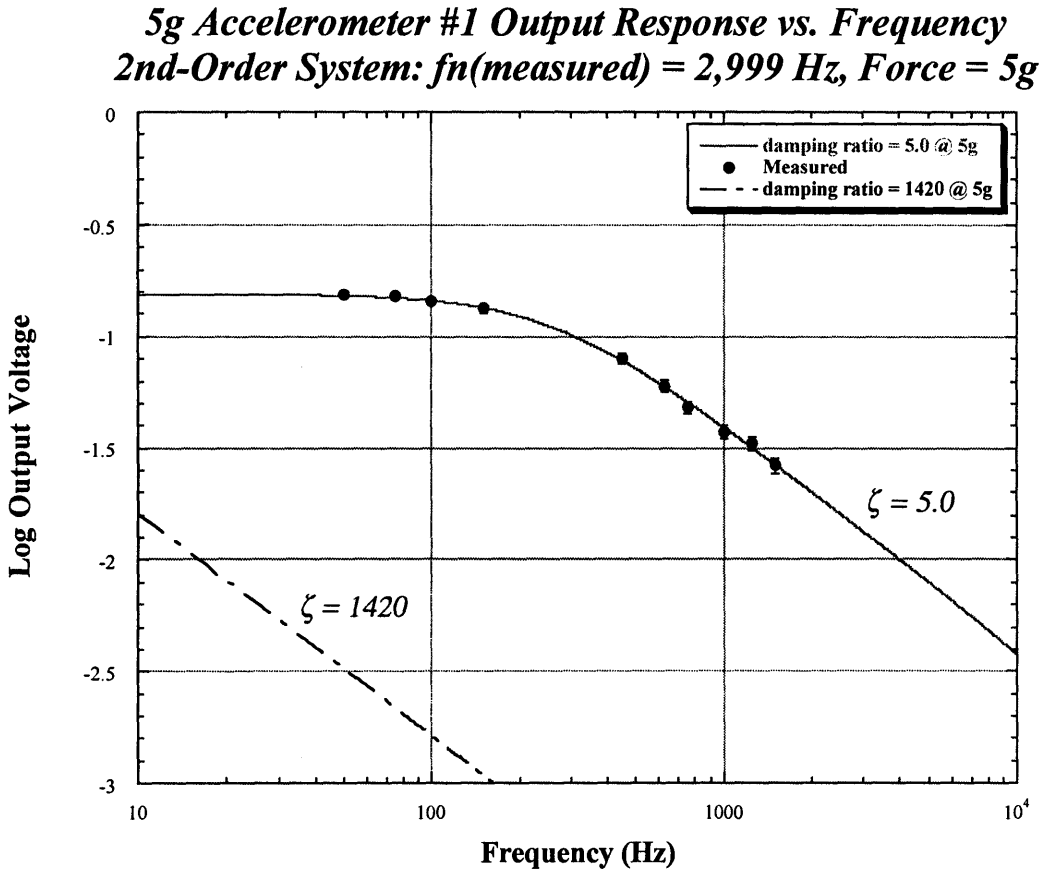


Figure 5–16(a): Log-log plot of accelerometer frequency response data fitted to theoretical magnitude *vs.* frequency response for a 2nd-order system. Damping ratio of $\zeta = 1420$ corresponds to the calculated damping ratio for this accelerometer structure in the absence of damping control apertures.

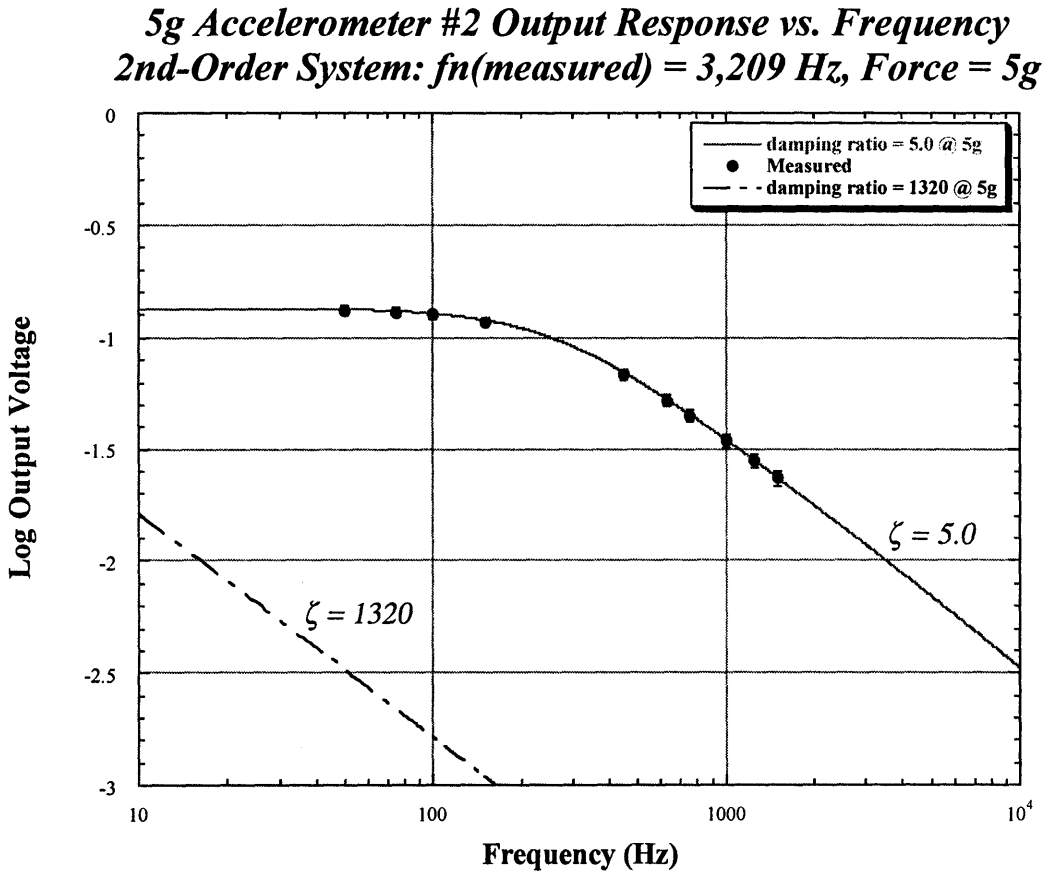


Figure 5–16(b): Log-log plot of accelerometer frequency response data fitted to theoretical magnitude *vs.* frequency response for a 2nd-order system. Damping ratio of $\zeta = 1320$ corresponds to the calculated damping ratio for this accelerometer structure in the absence of damping control apertures.

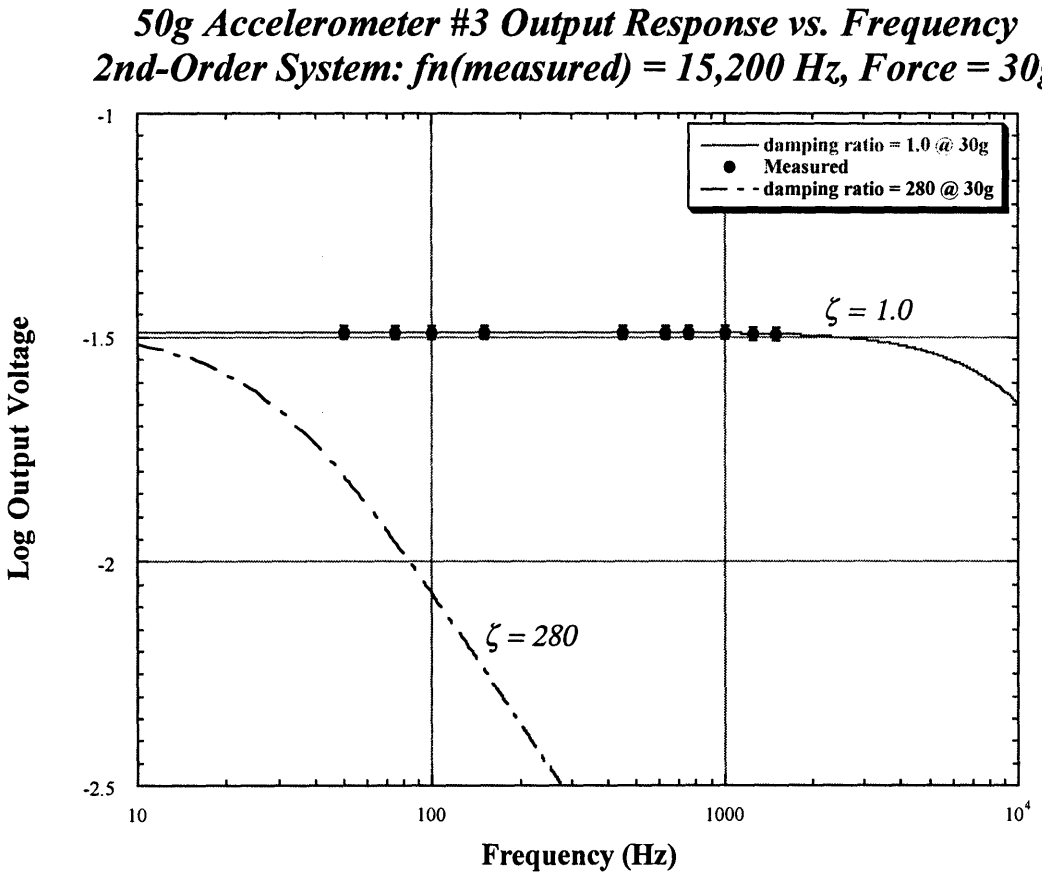


Figure 5–16(c): Log-log plot of accelerometer frequency response data fitted to theoretical magnitude *vs.* frequency response for a 2nd-order system. Damping ratio of $\zeta = 280$ corresponds to the calculated damping ratio for this accelerometer structure in the absence of damping control apertures.

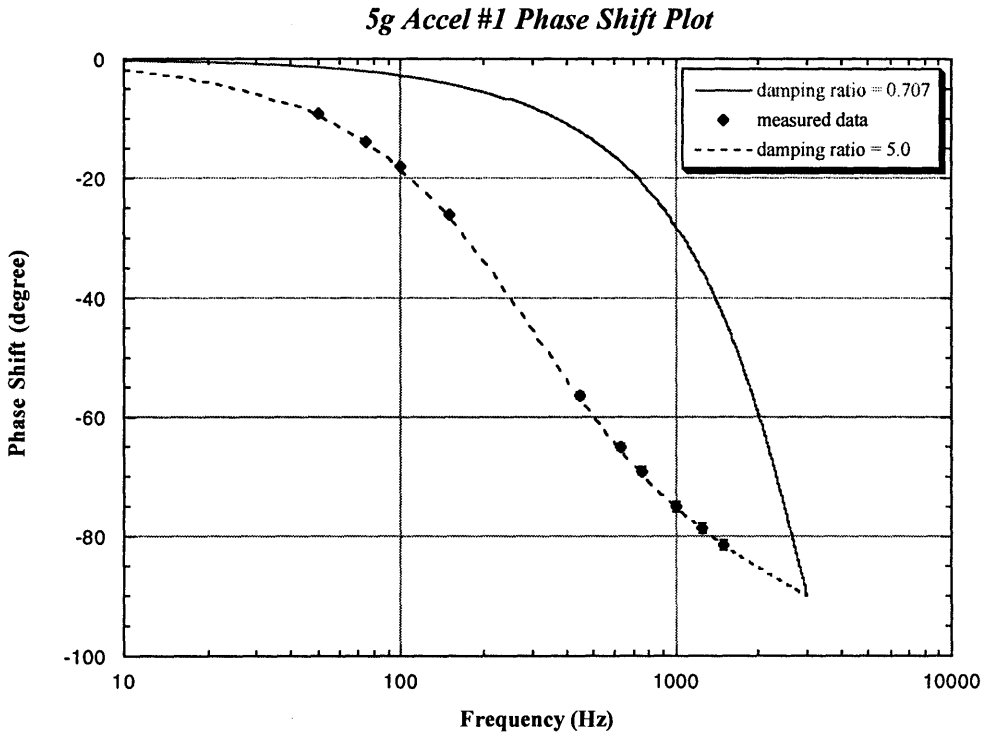


Figure 5–17(a): Phase-shift plot of 5g Accelerometer #1 frequency response data fitted to theoretical phase-shift *vs.* frequency response for a 2nd-order system.

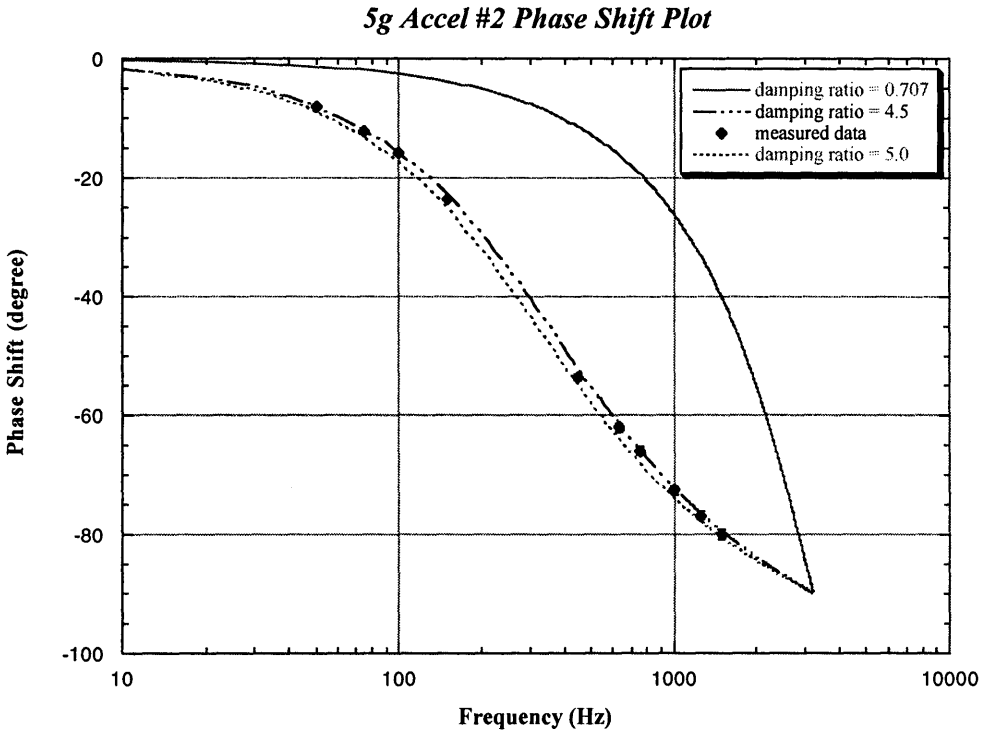


Figure 5–17(b): Phase-shift plot of 5g Accelerometer #2 frequency response data fitted to theoretical phase-shift *vs.* frequency response for a 2nd-order system.

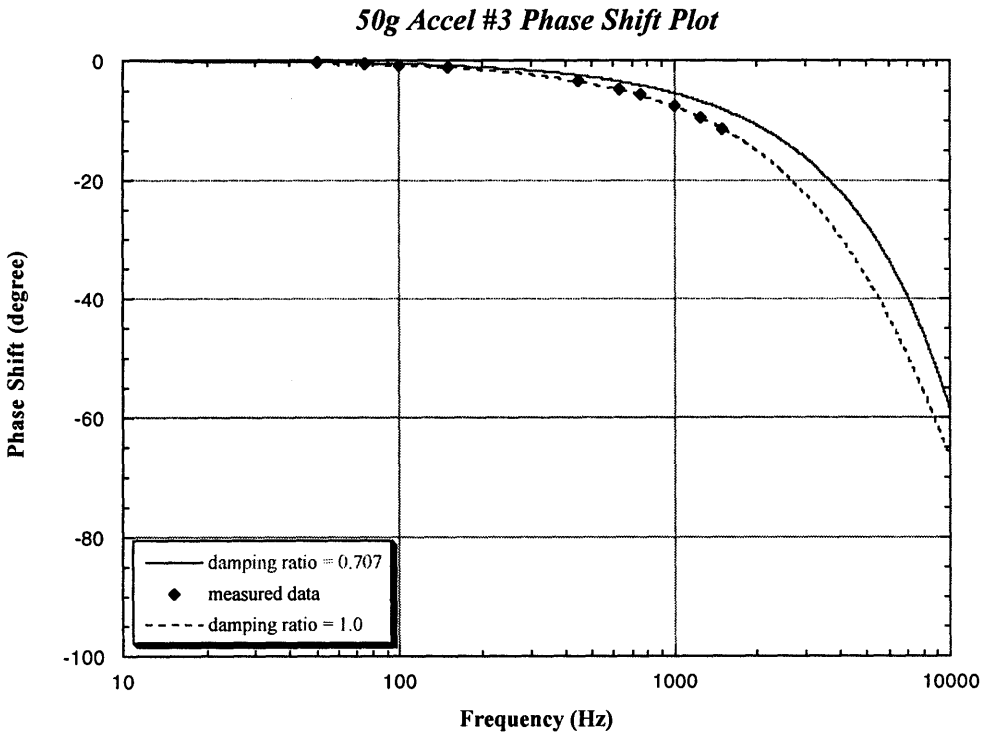


Figure 5–17(c): Phase-shift plot of 50g Accelerometer #3 frequency response data fitted to theoretical phase-shift *vs.* frequency response for a 2nd-order system.

It is important to know the accelerometer natural frequencies accurately so that the extracted damping ratios are also accurate. The accelerometer natural frequencies were measured prior to the frequency response test shown above. The accelerometer being tested was placed in a vacuum chamber, and the vacuum chamber was pumped down to approximately 100mTorr. A simple circuit shown in Figure 5–18 was used to detect the natural frequencies of the three accelerometers. The proof mass of the accelerometer was connected to the negative terminal of the first-stage AD745 op-amp while the bottom electrode was connected to V_{in}. The accelerometer was excited to resonance via an external pulse generator, and a small d.c. voltage (10-20mV) was used as V_{in}. After the current-to-voltage conversion stage, the signal went through an integrator, and finally a sinusoidal output signal with a frequency at the accelerometer natural frequency was measured. LabVIEW 4.0 was used to perform a spectrum analysis of V_{out} so the natural frequency of the accelerometer could be found. As an example, the resultant output signal from the detection circuit and the spectrum analyzer output (for 5g Accelerometer #1) are shown in Figure 5–19.

The amplitude gain of this circuit can be calculated as follows:

$$\begin{aligned} \text{Assume} \quad C &= C_0 + \tilde{C} \\ &= \frac{\varepsilon_0 A}{g_0 + g_1 \sin \omega t} \\ &\approx \frac{\varepsilon_0 A}{g_0} + \frac{\varepsilon_0 A}{g_0^2} g_1 \sin \omega t \end{aligned} \tag{5.17}$$

where A is the proof mass area, g_0 is the intial gap spacing, g_1 is the small displacement of the proof mass caused by the applied pulse, and ω is the natural frequency of the accelerometer. The voltage output at V_1 is given by:

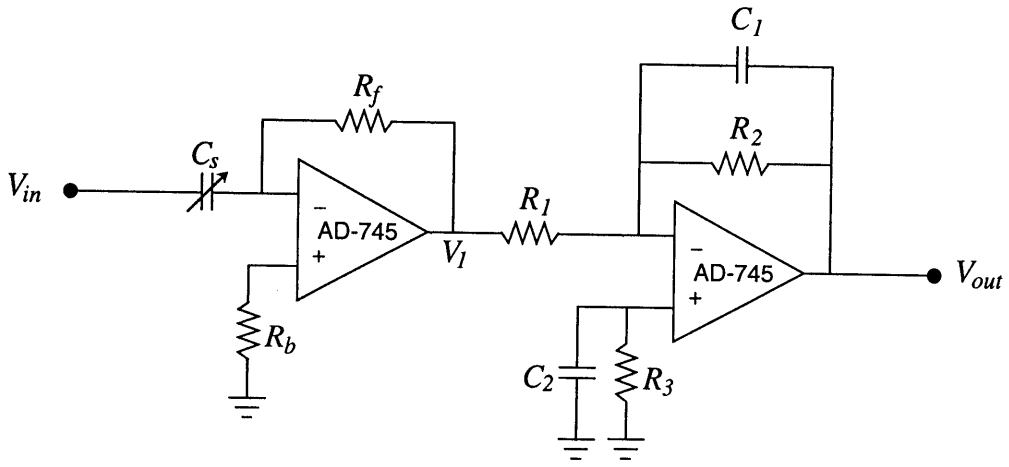
$$V_1 = -V_{in} R_f \frac{dC}{dt} = -V_{in} R_f \frac{d\tilde{C}}{dt} \tag{5.18}$$

and V_{out} is given by:

$$V_{out} = \frac{R_f \tilde{C}}{R_1 C_1} V_{in} \tag{5.19}$$

Finally, the amplitude gain of this circuit is given by:

$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{R_f}{R_1 C_1} \left(\frac{\varepsilon_0 A g_1}{g_0^2} \right) \sin \omega t \tag{5.20}$$



$R_f = R_b = 200\text{k}\Omega$

$C_1 = C_2 = 47\text{pF}$

$R_1 = 100\Omega \qquad R_2 = R_3 = 500\text{M}\Omega$

Figure 5–18: Detailed schematic of the natural frequency detection circuit.

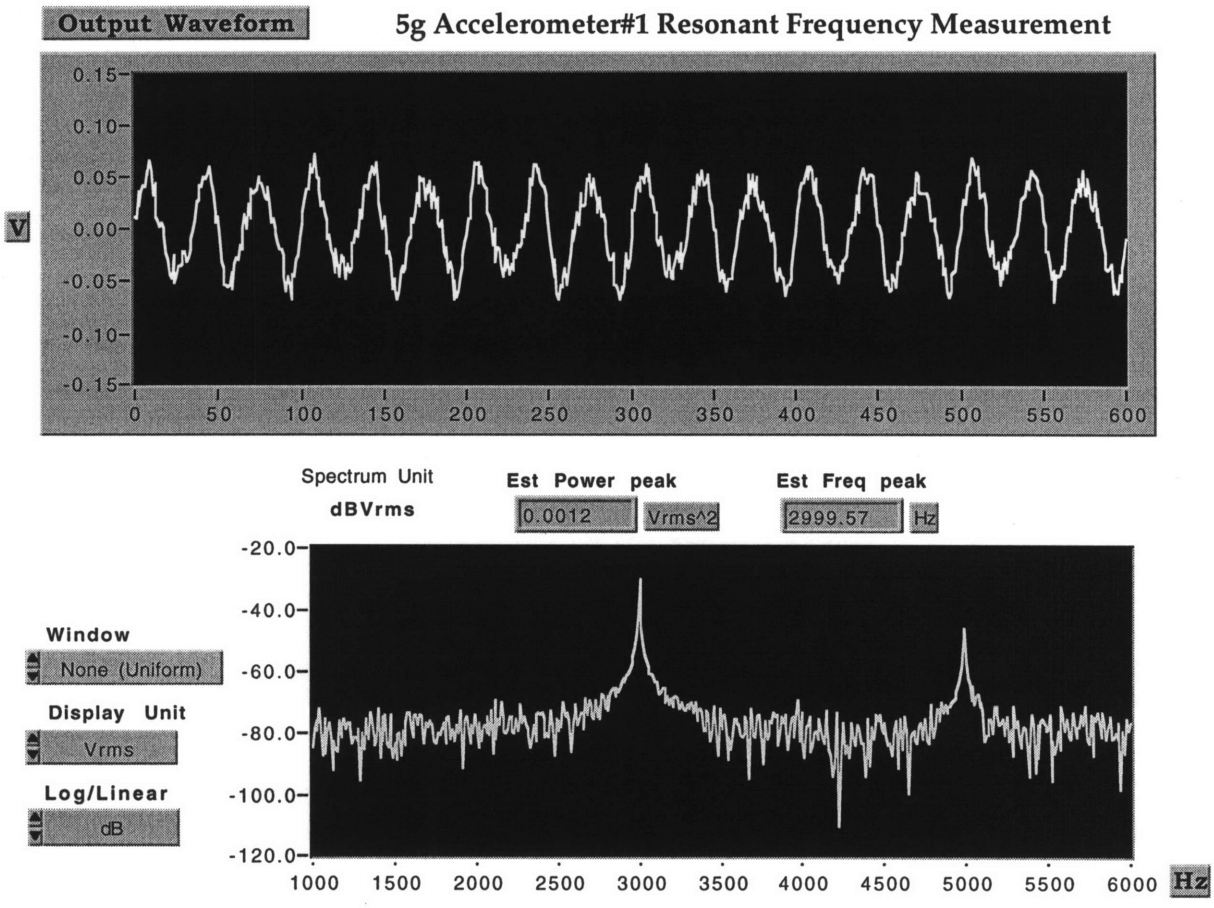


Figure 5–19: Output waveform and the corresponding spectrum analyzer output from the natural frequency detection circuit for 5g Accelerometer #1. The estimated natural frequency is 2,999Hz for this accelerometer.

5.5 Drift and Long-Term Stability

One of the characteristics of silicon microaccelerometers that makes them an attractive alternative to the traditional piezoelectric accelerometer is their ability to measure acceleration down to true DC. In particular, designers of navigational instrumentation are interested in seeing if silicon accelerometers can be produced with performance characteristics good enough to be used in their systems. An important device characteristic for such an application is the drift and stability of the silicon accelerometer. For instance, if the sensor were to be applied to measurements in a low-g environment, it would not only have to resolve accelerations in the 0.1μg range, but its output in a constant acceleration field must be stable in terms of drift over the same scale.

An attempt was made to measure the drift in DC output of one of the 5g Accel #1 microaccelerometers. The microaccelerometer was placed in a +1g field and a nominally 0g field (by rotating the device so its sensitive axis is 90° with respect to Earth's gravity) and its output was monitored over the course of 72 hours. The accelerometer's output was measured with the custom-built capacitive detection circuit. In order to make sure that only DC shifts in the accelerometer's output were being measured, the output of the detection circuit was additionally filtered with a 3-pole Butterworth low-pass filter with a 0.1Hz cutoff frequency.

Before initiating each measurement run, the circuit was turned on and allowed to equilibrate for at least 30 minutes. The temperature near the setup was monitored with a digital thermometer, and was always 24±1.2°C during the course of all runs. The inherent drift of the capacitive detection circuit was measured by connecting a fixed 5.0pF high-precision ceramic capacitor (in place of the accelerometer) to the input of the circuit.

The inherent drift of the detection circuit was measured, and then the DC output drift on an accelerometer was measured. Figure 5–20 plots the drift of the accelerometer in two different orientation and the inherent drift of the circuit with a 5.0pf fixed capacitor.

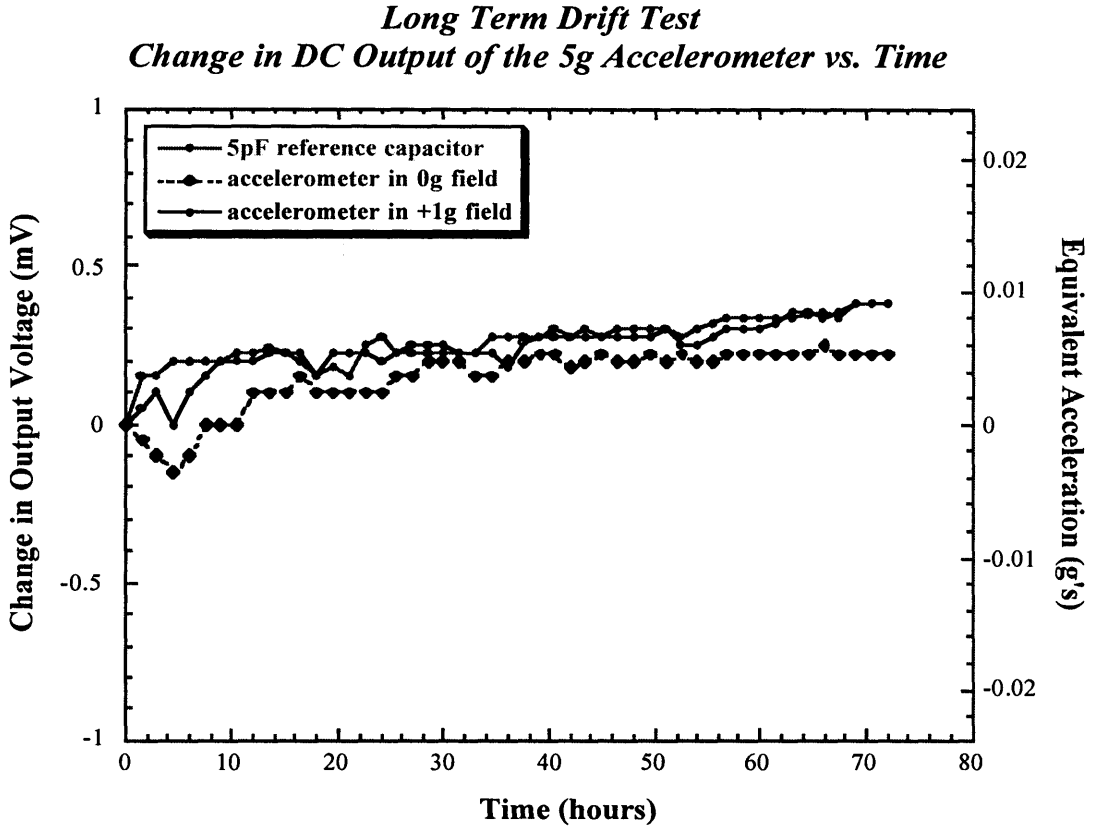


Figure 5–20: A 72-hour drift experiment was performed to measure the DC stability of the accelerometer (5g Accelerometer #1). The inherent DC drift of thedetection circuit was measured by connecting a fixed 5.0pF capacitor to the input of the circuit.

The inherent drift of the detection circuit is relatively small, with a maximum value of 0.38mV. The DC output of the accelerometer was also very stable. Measurements on the accelerometer in the +1g orientation showed a similar trend as the fixed 5.0pF capacitor data. The output of the accelerometer in the 0g configuration exhibited a drift which was even slightly smaller than the measured drift of the detection circuit. The equivalent acceleration change for both runs was less than 0.01g. This represents a variation of approximately 0.2% of its full-scale (5g) input range. It is clear from Figure 5–20 that we did not successfully measure the drift of the accelerometer under test since the inherent drift of the detection circuit seemed to dominate the measurement results. Thus, we conclude that the drift and the stability of the accelerometer under test were no worse than what were exhibited from the off-chip detection circuit.

The fundamental sensing limit for these microaccelerometers is determined by the mechanical noise resulting from molecular agitation of the proof mass. This Brownian noise limit can be found by using the Nyquist relationship and calculating an equivalent mechanical resistance to get an expression similar to the Johnson noise equation for electrical systems as described in [11, 50]. We use the following equation to calculate the Brownian noise limit in our accelerometers,

$$\bar{a}_n = \sqrt{\frac{4k_B T\omega_n}{MQ}} = \sqrt{\frac{8k_B T\omega_n \zeta}{M}} \tag{5.21}$$

where k_B is Boltzman's constant, T is temperature in degrees Kelvin, ω_n the natural frequency of the device, M the mass of the proof mass, Q the quality factor and ζ is the damping ratio. For our accelerometers, we assume room-temperature conditions (300°K) and that the devices are over-damped in air with ζ = 5.0. Using the extracted devices parameters we calculate that the Brownian noise for the 5g Accel #1 accelerometer measured in the drift experiment is 654.3 $\mu g/\sqrt{Hz}$. Obviously, this puts the noise for such devices in the milli-g (mg) range for frequency bandwidths greater than 100Hz. As

pointed out by Gabrielson [50], this noise limit can be improved by increasing Q, reducing the natural frequency, or increasing mass M.

These initial drift results are encouraging, but further tests on a larger number of devices would be required to confirm these results. If such tests were positive, it may be possible that carefully selected silicon accelerometers might find application in special areas requiring high precision, stable DC acceleration measurements. In addition, careful consideration of the Brownian noise limit will have to be taken into consideration.

5.6 Hybrid-Accelerometer Testing

This section describes the incorporation of the accelerometer controller IC [45] with the micromechanical structure on the same pin grid array (PGA) package. Some processing problems with the mechanical structure which had not been resolved at the time of testing (October 1995) will be discussed as well.

Mechanical Sensor

A die photo of the unbonded micromechanical structure which was used for testing is shown in Figure 5–21. Note the structure has a straight tether design (*simple* pinwheel design). This was done to help separate the secondary resonance modes from the desired fundamental resonance mode. Simulations predicted just less than a factor of two separation of the fundamental resonant frequency from the secondary resonance mode using the folded pinwheel structure. The straight tether design yielded a 2.55× separation of fundamental and secondary resonances during simulation. Though not a large improvement, it could mean the difference between a high resolution accelerometer and a useless piece of silicon.

Long silicon tethers are used to provide high linearity for the mechanical spring force. The side-by-side fabrication of the proof mass and reference structure ensure good matching even with process variation. Note the short silicon beams which hold the reference mass rigidly in place. The bonding pads spread evenly along the lower bound of the die photo are used to stitch-bond the mechanical structure and accelerometer controller.

Problems

Some problems were encountered during the fabrication of the mechanical structure which severely degraded its yield and viability. As discussed in Chapter 4, one problem was

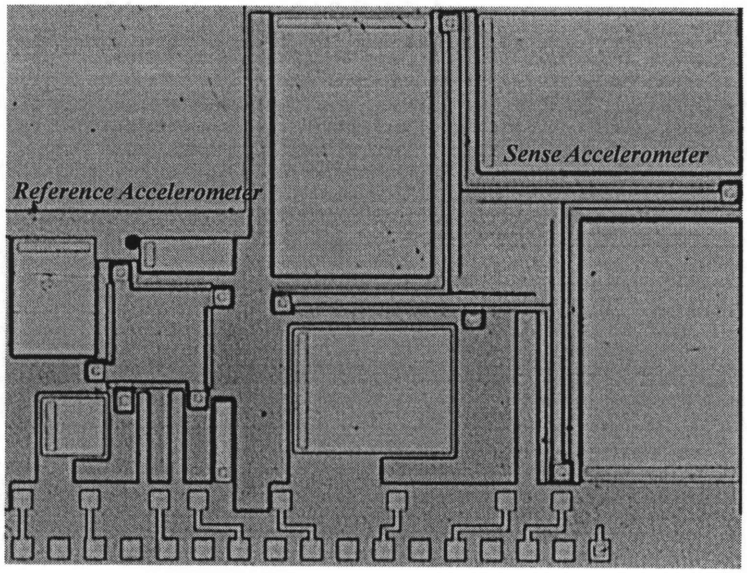


Figure 5–21: Die photo of the mechanical sensor for the hybrid-accelerometer projcet. The sense accelerometer (with long silicon tethers) is on the right-hand side and the reference accelerometer is on the left-hand side.

non-uniformity in the plasma etch which is used to release the proof mass and silicon tethers. A 25% non-uniformity was measured across the 4" wafer. Due to the gross non-uniformity of the etch, the yield was only about 30%. Another problem was associated with the thermocompression bonding process, again was described in Chapter 4. The yield dropped further to about only 10% when the fabrication process was completed.

For future fabrication of the accelerometers, a high density plasma etch (STS deep silicon etch) will be used to free the mechanical structure. The high density plasma etcher will reduce non-uniformity to less than 3% across the wafer. Also, the etcher has more than a 100:1 selectivity of Si:Oxide. A passivation layer can thus be used to prevent the plasma etch from compromising the lower electrode.

Stitch-bonding

A die photo of the stitch-bonded hybrid sensor is shown in Figure 5–22. To minimize parasitics at the sensitive nodes, no ESD protection or guard rings were placed on the sixteen bondpads which connect to the mechanical structure. As a result, ESD problems were encountered several times during the hybridization of the sensor.

Due to time restrictions and the low yield of the mechanical sensor, only six hybrid sensors were bonded for testing. Of these, the first five hybrid sensors had problems with electrostatic discharge blowing out gate dielectrics of MOS transistors. These devices multiplex voltages to the fixed electrodes above and below the proof mass and reference structures. It was not until the very last hybrid sensor was bonded that a viable accelerometer was available for testing.

Testing Results

The operation of the accelerometer controller was first tested open loop (without the micromechanical structure), then together with the micromechanical structure as a hybrid closed loop system. 10 bonded test chips were packaged at the MOSIS foundry for open-loop testing. 65-pin PGA packages were used to house the test ICs. 82 unbonded die

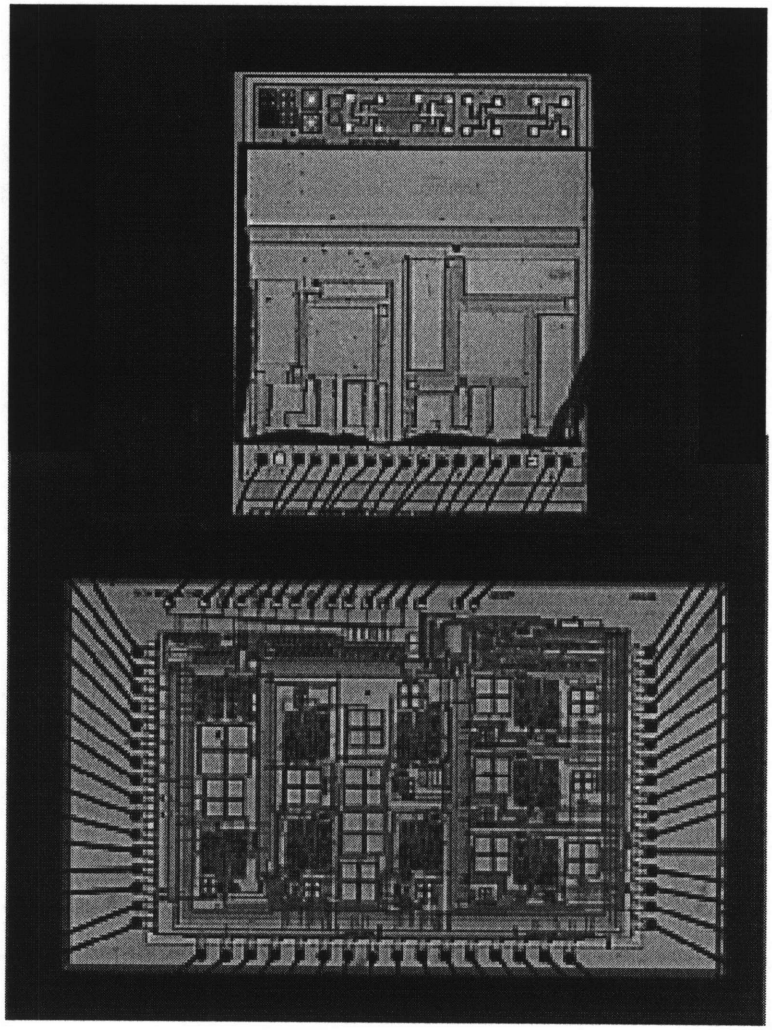


Figure 5–22: Hybrid-accelerometer packaged in a 64-pin PGA package. The mechanical sensor is shown on the top, and the controller IC is on the bottom.

were received and available for stitch-bonding with the micromechanical structure. A 68-pin PGA package was used to hold the hybrid accelerometers. The results of the open loop testing of the accelerometer controller are given in [45] and will not be repeated here. The results from the closed loop testing are presented in the following.

As previously discussed, an ESD problem was encountered when the hybrid accelerometer circuit was stitch-bonded together which destroyed all but one of the hybrid sensors. More mechanical structures were not available for bonding due to the low yield (10%) of the micromechanical structure which was caused by the nonuniform etch and thermocompression bond problem.

The accelerometer was first tested in second order reset mode. The hybrid structure assumed stable operation in an open air environment with a 1.0g DC input acceleration (gravity). The output spectrum from the second order operation is shown in Figure 5–23. Note the large amount of "white" noise which is present in the output spectrum. This is as a result of the Brownian noise from the heavily over-damped system. Also note the small signal "spike" at 120Hz. This is as a result of a microscope light which should have been powered off.

While the spectrum of Figure 5–23 verifies the function of the second order reset loop, operation of the higher order modes was never tested. Unfortunately, while the data was being analyzed for the output spectrum shown in Figure 5–21, the proof mass was pulled-in to the upper fixed electrode where it fused. Because this was the only viable hybrid accelerometer, the testing of higher order operation as well as testing in a vacuum will have to be the focus of later research. Ongoing research is currently investigating the possibility of placing mechanical stops on the upper electrode to prevent fusion of the proof mass as occurred here.

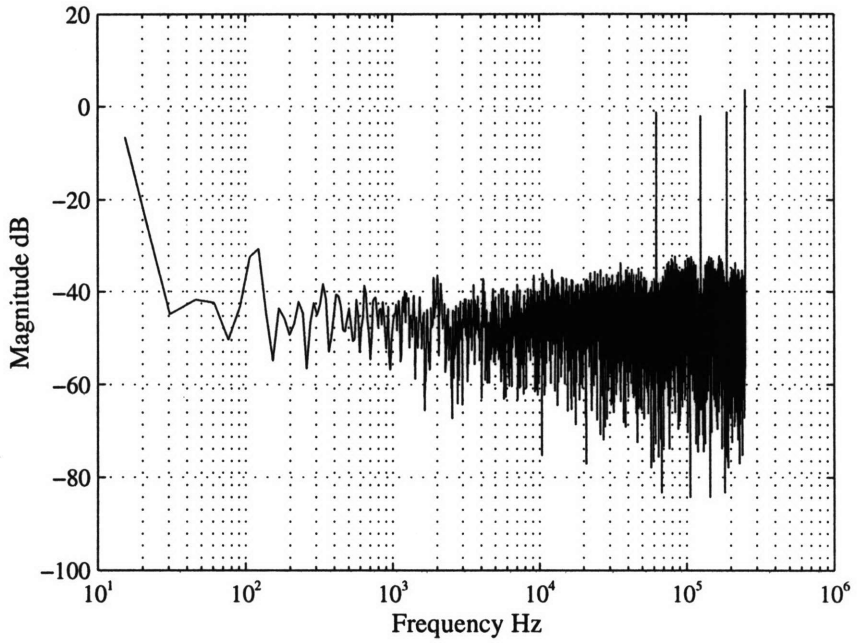


Figure 5–23: Output spectrum of second order accelerometer with 1.0g DC input.

5.7 Summary

We have successfully demonstrated the functionality of our wafer-bonded sealed cavity microaccelerometers. Electrostatic pull-in tests and ±1g flip test showed that the DC sensitivity of the accelerometer was very close to expected values. Dynamic vibration tests on the devices showed that the accelerometers had good linearity (< ±2% FSO), but were still over-damped. From fitting the device frequency response to the expected response for a 2nd-order system, we estimate that the damping ratio (ζ) was about 5 for both 5g accelerometers and could be fitted to 1 for the 50g accelerometer. While this value is higher than the desired value of 0.707, it is lower, by more than two orders of magnitude, than the expected damping ratio for such an accelerometer structure *without* damping control apertures. This data clearly indicates that the damping control design was successful in significantly reducing damping. Limited testing results were presented in this chapter regarding the hybrid-accelerometer, much more work is needed to verify the successful implementation of this type of hybrid approach. A few design and fabrication suggestions are presented in the Conclusion chapter next.

Further tests on the device's cross-axis sensitivity, performance over temperature, and insensitivity to packaging stress well help explore the efficacy of the other design features implemented in these structures.

Chapter 6
Conclusions

The goals of this thesis were: first, the development of *"surface-micromachining-like"* structures such as tuning fork gyroscopes and accelerometers fabricated from single-crystal silicon using silicon wafer bonding, and second, the development of the MEMS-CMOS integrated sensor technology based on the wafer-bonded sealed cavity process. The process was designed to take advantage of the beneficial properties of silicon as a good quality mechanical as well as electrical material, and also featured ease of integration into existing silicon foundries, thereby enabling separate optimization of all parts of the sensor-circuit system. The integrated MEMS-CMOS process incorporated silicon wafer bonding with a sealed cavity, buried etchstop layers for formation of backside pressure ports, and both front and backside release etches [7]. A thermocompression bond was used to form a capacitive electrode. In addition, this process was demonstrated by fabricating capacitive microaccelerometers whose structures were implemented using design features intended to reduce overall die size, improve output linearity, improve

insensitivity to external stresses, and control the effects of squeeze-film damping in small gap microstructures.

These accelerometers were successfully implemented and tested during the course of this research. We only had six hybrid-accelerometers successfully fabricated and ready for stitch-bonding to the IC chips. Only one stitch-bonded hybrid-accelerometer was finally tested, and limited testing results were presented. Approximately forty dielectrically isolated, single-electrode, discrete microaccelerometers were tested during the course of this research. While the response of the accelerometers tested was over-damped, the incorporation of damping control apertures in the proof mass reduced the observed damping by more than two orders of magnitude from the expected worst-case conditions. The increased damping (compared to the design damping ratio) is thought to be mainly attributable to an underestimate of the damping ratio from the 2-D FEA model [31–32] employed during the design phase of the accelerometers. However, The observed damping was about 3.3× larger than predicted by the 2-D FEA model. Despite the large damping, the accelerometer devices displayed good static sensitivity and dynamic response linearity. Though limited testing results for the hybrid-accelerometer were presented in this thesis, significant work is needed to achieve the full monolithic integration of the micromechanical sensor and control circuitry for the integrated accelerometer. Along with full integration, there are several other possible steps which could be taken which may improve the performance of the accelerometer (especially the mechanical sensor). Section 6.2 discusses the possible improvements.

6.1 Contributions of this Thesis

This thesis has produced a number of significant contributions. First, as demonstrated from the testing results in Chapter 5, we were successful in creating functional capacitive wafer-bonded silicon microaccelerometers. The accelerometers exhibit good static sensitivity, dynamic sensitivity, and linearity. The microaccelerometer structure itself is unique. It is fabricated with the wafer-bonded sealed cavity process, made completely from single-crystal silicon, and can easily incorporate mechanical layers thicknesses which may vary by as much as two orders of magnitude (i.e., few micrometers to hundreds of micrometers in device thickness). In addition, the mechanical design features used to implement these silicon accelerometers, particularly the damping control apertures, have proven to be effective. More extensive and detailed experiments on these devices will help determine the efficacy of these design features, and whether or not they might be applied to the design of other microelectromechanical structures.

The successful implementation of the accelerometer fabrication process relied heavily on developments in the integrated MEMS-CMOS process. The main element of the integrated MEMS-CMOS process is a sealed cavity formed by silicon wafer bonding, and one of the key contributions of the thesis was the process enhancement added to the wafer-bonded sealed cavity process co-developed with Parameswaran [7]. Two specific process enhancements, electrical isolation of mechanical structure from the substrate, and dry release of the mechanical structure, were discussed in this thesis. For electrical isolation of mechanical structure from the substrate, detailed discussions on both junction isolation scheme and dielectric isolation scheme were presented. Full characterization of these two isolation schemes was reported along with the p-n-p electrochemical etch process and the SOI-wafer-based process technology. The dry release method serves as an important "back-end micromachining" process in order to functionalize the surface-micromachining-like microstructures. Detail of this plasma dry release etch was also shown in this thesis. Furthermore, junction isolation and dry release facilitate the

successful fabrication of lateral comb-drive resonators, which in turn provide material property study opportunity. In addition, diodes formed with junction isolation and dry release process help to understand the electrical property of the bonded interface. Combination of dielectric isolation and dry release ensures successful fabrication of M-Test structures which in turn complete the integrated MEMS-CMOS process verification presented in Parameswaran's thesis [7].

6.2 Future Work

Future concerns in process development include two areas: the implementation of anti-stiction stubs both on the top and the bottom electrodes, and the extension of the thermocompression bond to a wafer level and its possible use for packaging and hermetic sealing. The development of the model and process, along with the availability of equipment for controlled ambient and thermocompression bonding has brought the sealed cavity MEMS-CMOS technology to a level that it can be transferred to industrial fabrication lines. With the addition of the above mentioned modifications to the process, it can be exercised in making a wide variety of integrated microelectronic transducers.

Regarding the wafer-bonded accelerometer as one of the demonstration vehicles for the integrated MEMS-CMOS process technology, understanding and modeling of fluid dynamics and device damping behavior are required. The accelerometer devices tested in this thesis exhibited over-damped dynamic response. It is believed that damping was larger than expected, mainly due to an underestimate in damping ratio when Novack's simple 2-D model [32] was employed during the design phase. In the original damping control simulation carried out by Novack, we did not have ready access to an actual 2- or 3-dimensional fluids simulation package to use with the finite element analysis software

system we had in place. Instead, by making an exact mathematical analogy between the equations for heat transfer and the Reynold's flow equations, the heat transfer package in ABAQUS (and later I-DEAS package) was used to create a simple 2-dimensional model of the squeeze-film damping problem and design the accelerometers [31–32]. It would be very desirable to use an actual 3-dimensional fluid dynamics simulation package to reinvestigate the damping control approach. In particular, it would be interesting to address whether or not the vertical fluid resistance for gas that must flow through the full thickness of the proof mass is insignificant and can be ignored, as was done in Novack's simple 2-D model.

Results in Chapter 5 indicate that there is reasonable correlation between experimental results and the expected performance of the accelerometer based on analytical calculations and finite element simulations. More careful experiments on a larger number of devices could yield better statistics for comparing design and experimental results. A natural progression to this work would seem to be to use the MEMCAD software tools being developed here at MIT to complete a fully self-consistent electromechanical simulation of the accelerometer device under a variety of test conditions (this work is currently underway with MIT's MEMCAD group and a commercial company, Microcosm Technologies, Inc. in Cambridge, MA). Such an exercise could compare experimental results, analytical calculations, and simple finite element modeling results against self-consistent electromechanical simulations to see how accurate the other methods are and when simpler approaches, such as an analytical calculation versus a finite element simulation, can be used to reduce both time and cost during the sensor design phase.

Appendix A

Mask Design

This section describes the mask designs used in the junction-isolated hybrid-accelerometer and the dielectrically isolated discrete accelerometer projects presented in this thesis.

Figure A–1 illustrates the mask layout for the hybrid-accelerometer. This is a 8-layer mask design for the sealed cavity *silicon wafer* process. Figure A–2 illustrates the 9th layer mask design for the Pyrex 7740 *glass wafer* process described in Chapter 4. The chip size is 1cm×1cm, and there are four hybrid-accelerometer devices per chip. We normally fabricate 60 dies per wafer, thus we have 240 devices per wafer.

Figure A–3 is the mask layout for the dielectrically isolated discrete accelerometer with the anti-stiction oxide bumps. Figure A–3 illustrates the mask design for the *silicon wafer* process while Figure A–4 illustrates the *glass wafer* process. The chip size is also 1cm×1cm. There are three discrete accelerometers per chip, and we fabricate 60 dies per wafer, thus we have total of 180 discrete accelerometers per wafer.

Figure A–5 illustrates detailed lateral dimensions for the first dielectrically isolated discrete accelerometer (Accelerometer #1) while Figures A–6 and A–7 clearly illustrate those dimensions for Accelerometer #2 and Accelerometer #3. It is important to note that damping control apertures are present in Accelerometer #1's and Accelerometer #3's tethers, and the hole dimension and spacing are clearly shown in Figures A–5 and A–7.

Two damping control aperture designs are shown in Figures A–8 and A–9 respectively. The main difference between these two designs is the "spacing" between the damping holes. Design *version 1* has damping holes equally spaced at 17μm apart while the second design has damping holes equally spaced at 12μm apart on the proof mass plate.

Please note that all layout files are available through the author upon email request (chsu@mtl.mit.edu).

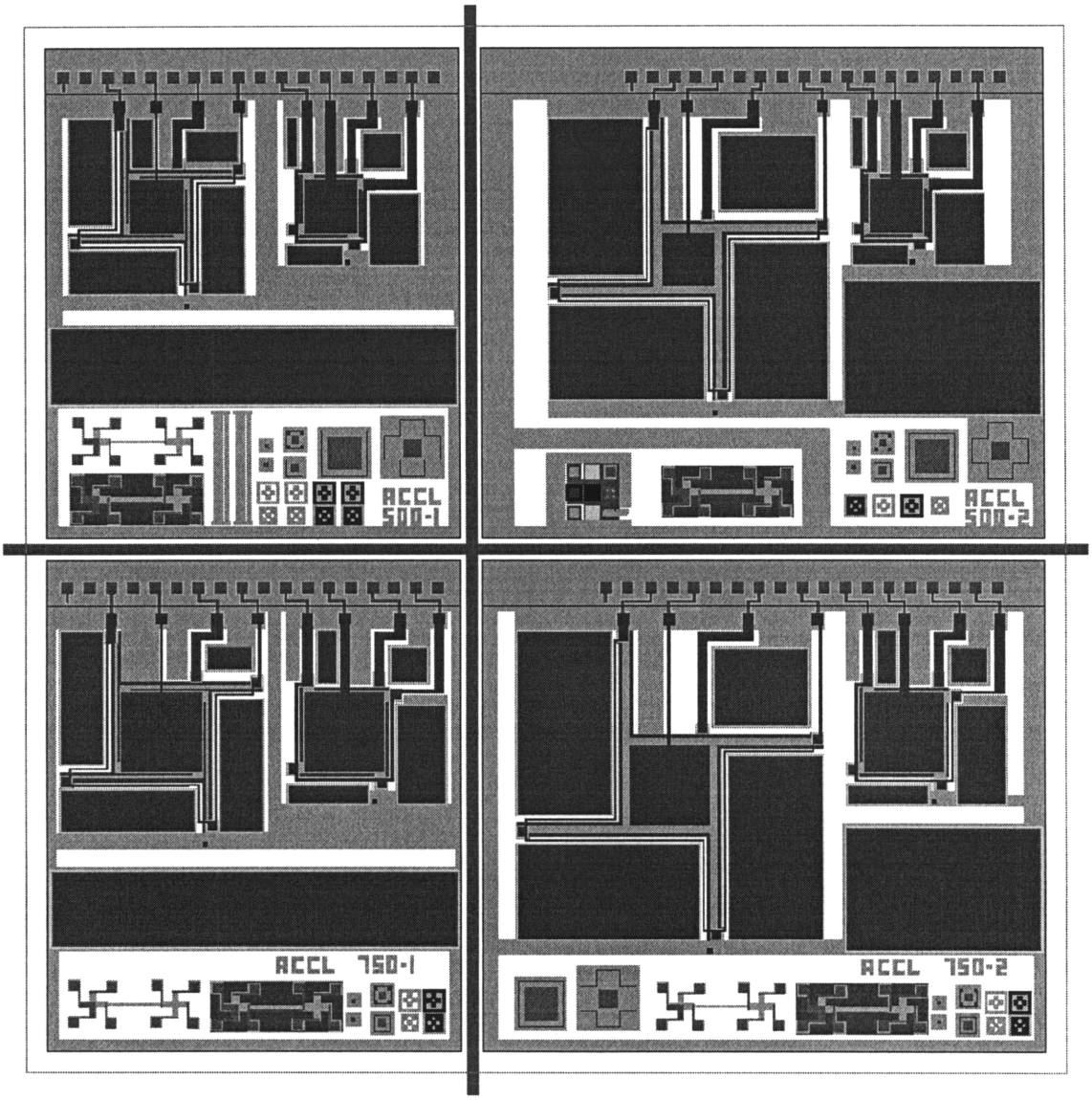


Figure A–1: 8-layer mask layout for the junction-ioslated hybrid-accelerometer (*silicon wafer* process).

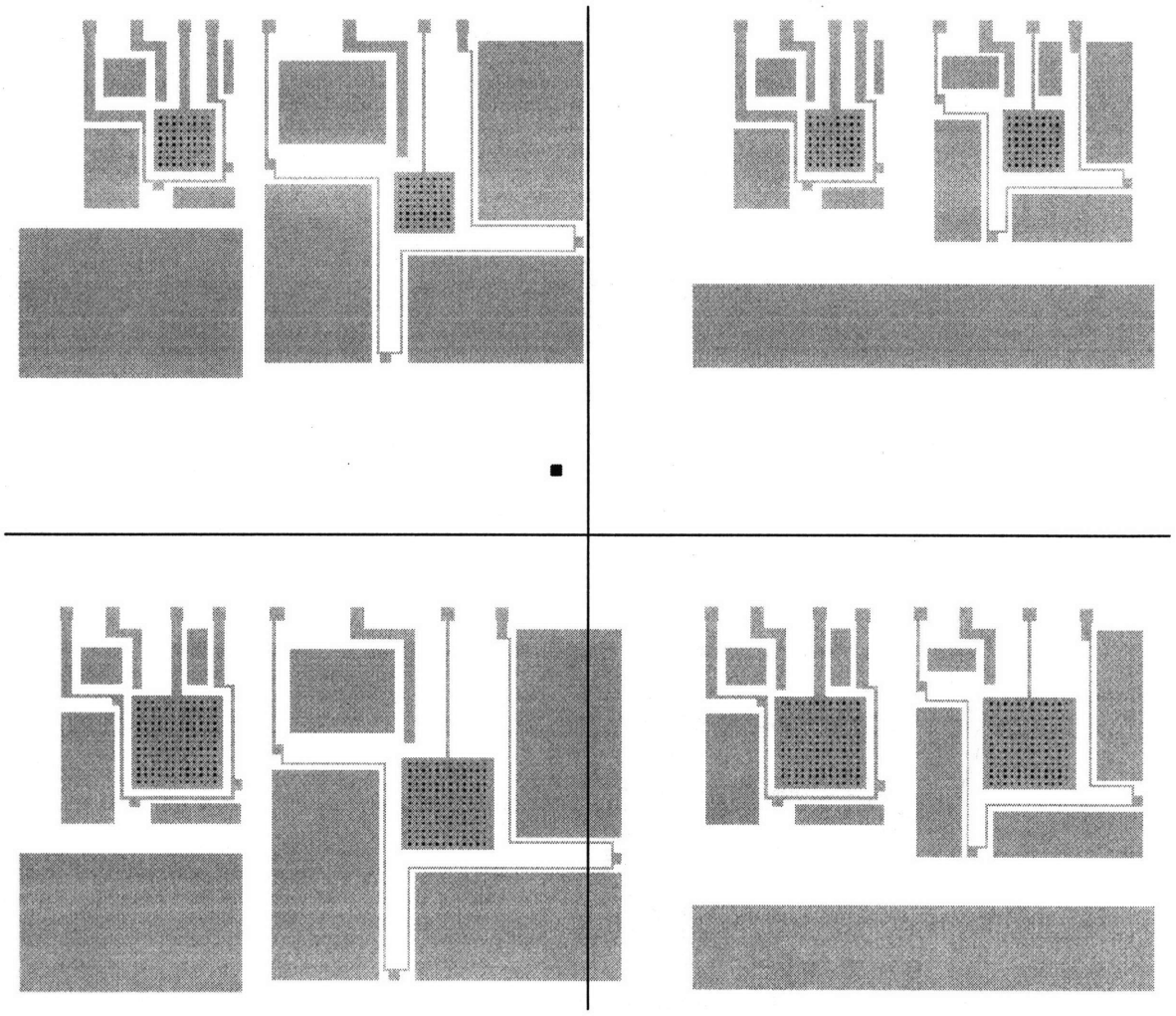


Figure A–2: Glass-layer mask layout for the junction-ioslated hybrid-accelerometer (*glass wafer* process).

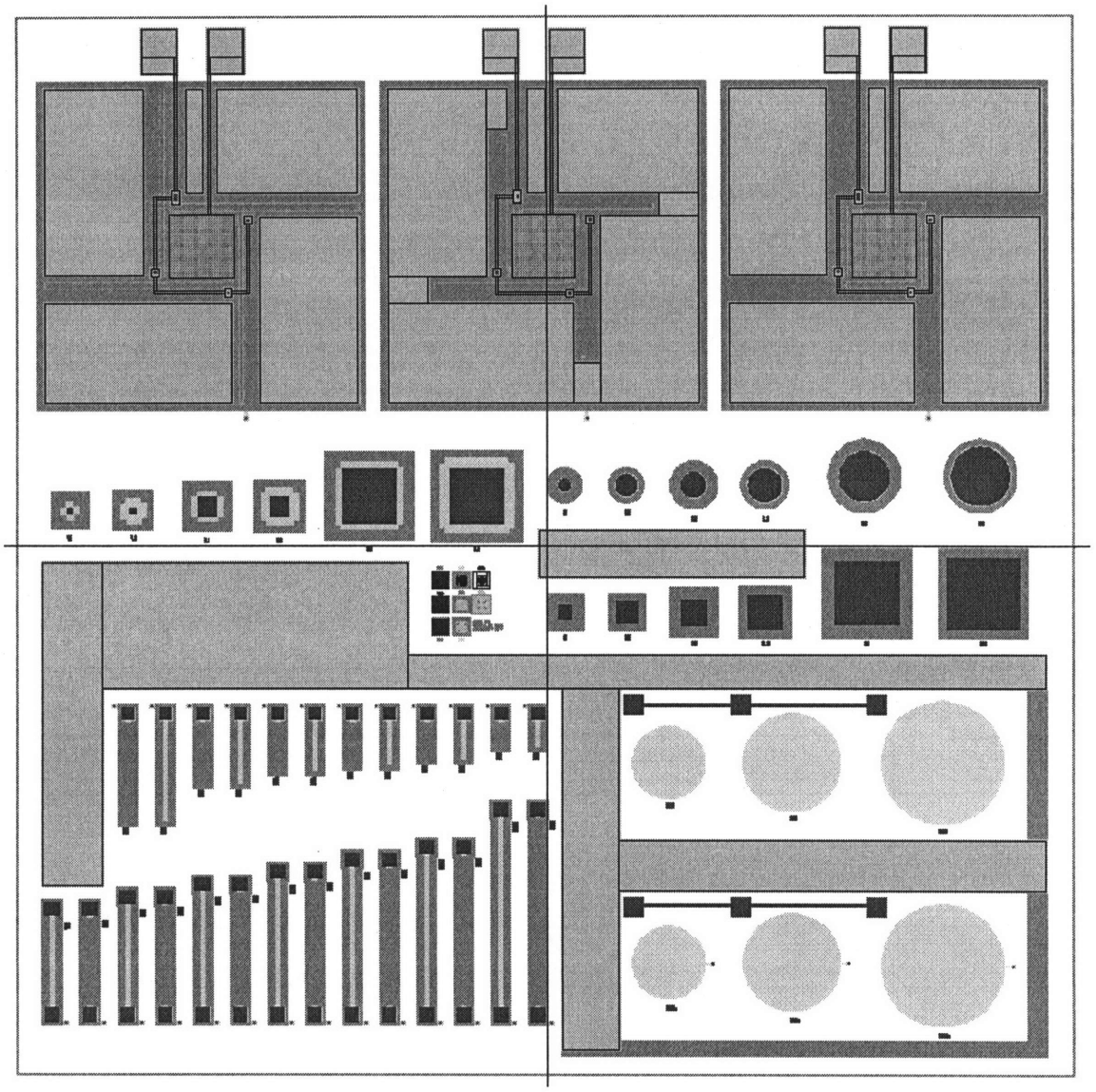


Figure A–3: 5-layer mask layout for the dielectrically isolated discrete accelerometer (*silicon wafer* process).

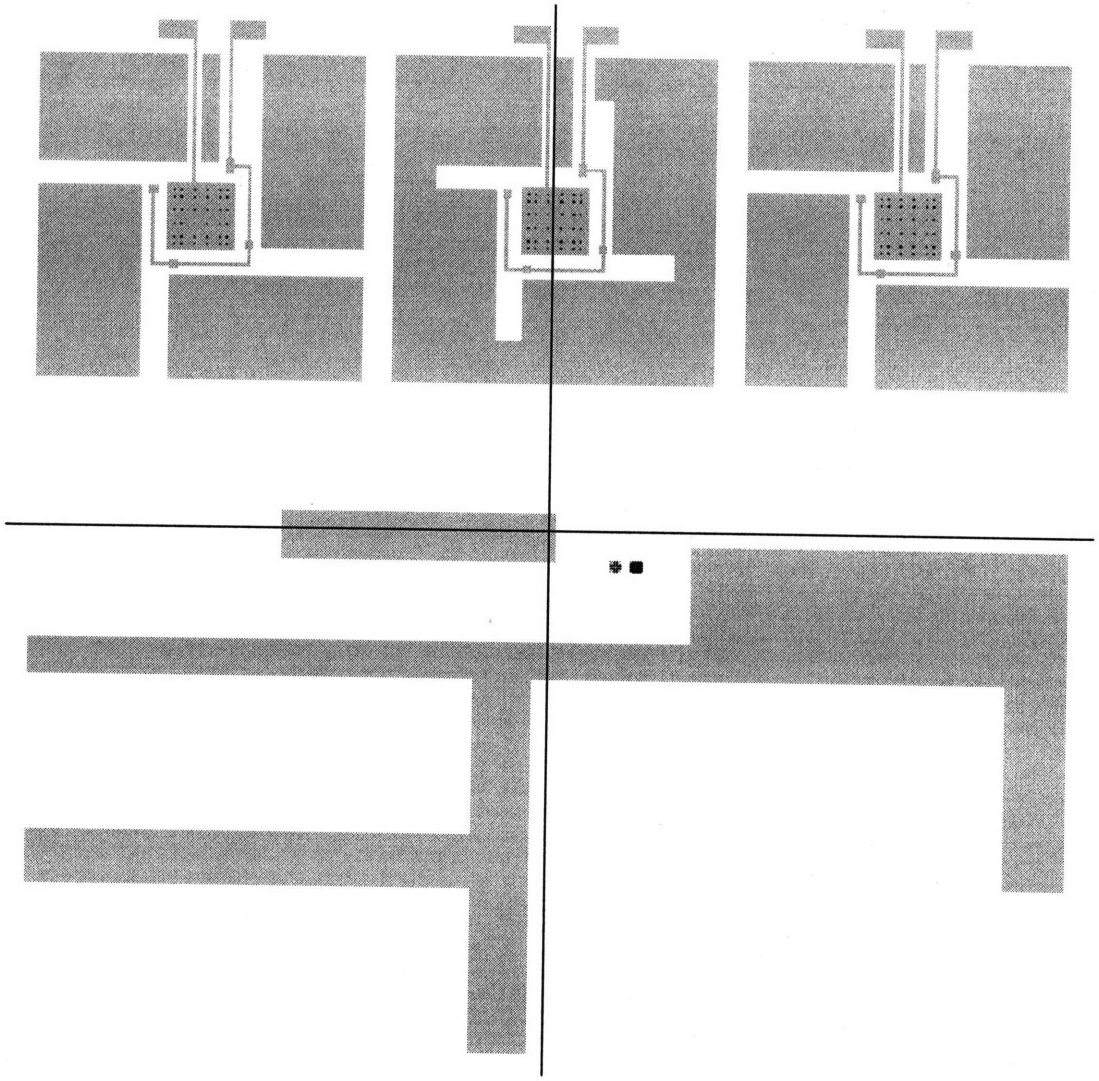


Figure A–4: Glass-layer mask layout for the dielectrically isolated discrete accelerometer (*glass wafer* process).

Accelerometer #1 Lateral Dimensions

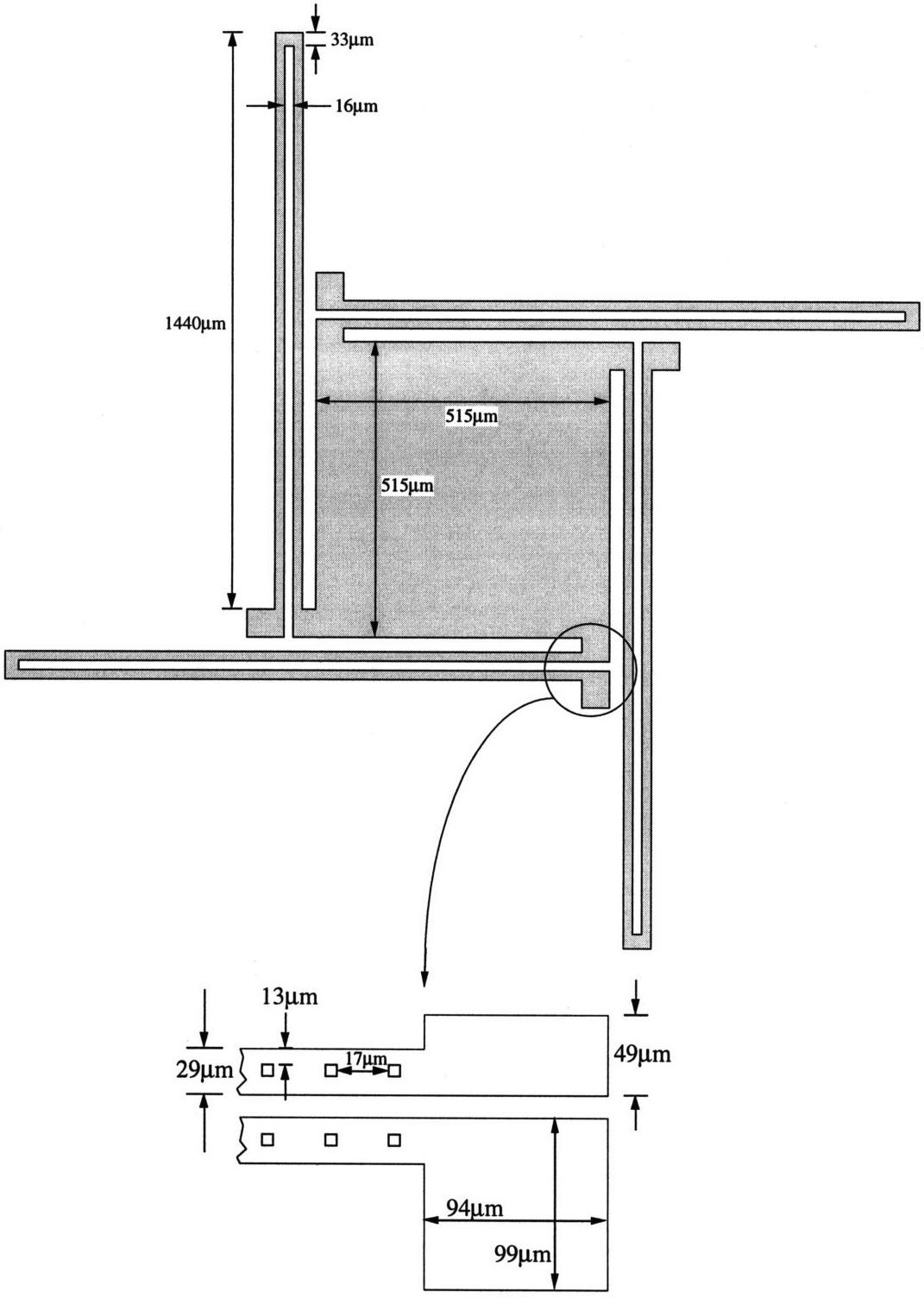


Figure A–5: Dielectrically isolated accelerometer #1 lateral dimensions.

Accelerometer #2 Lateral Dimensions

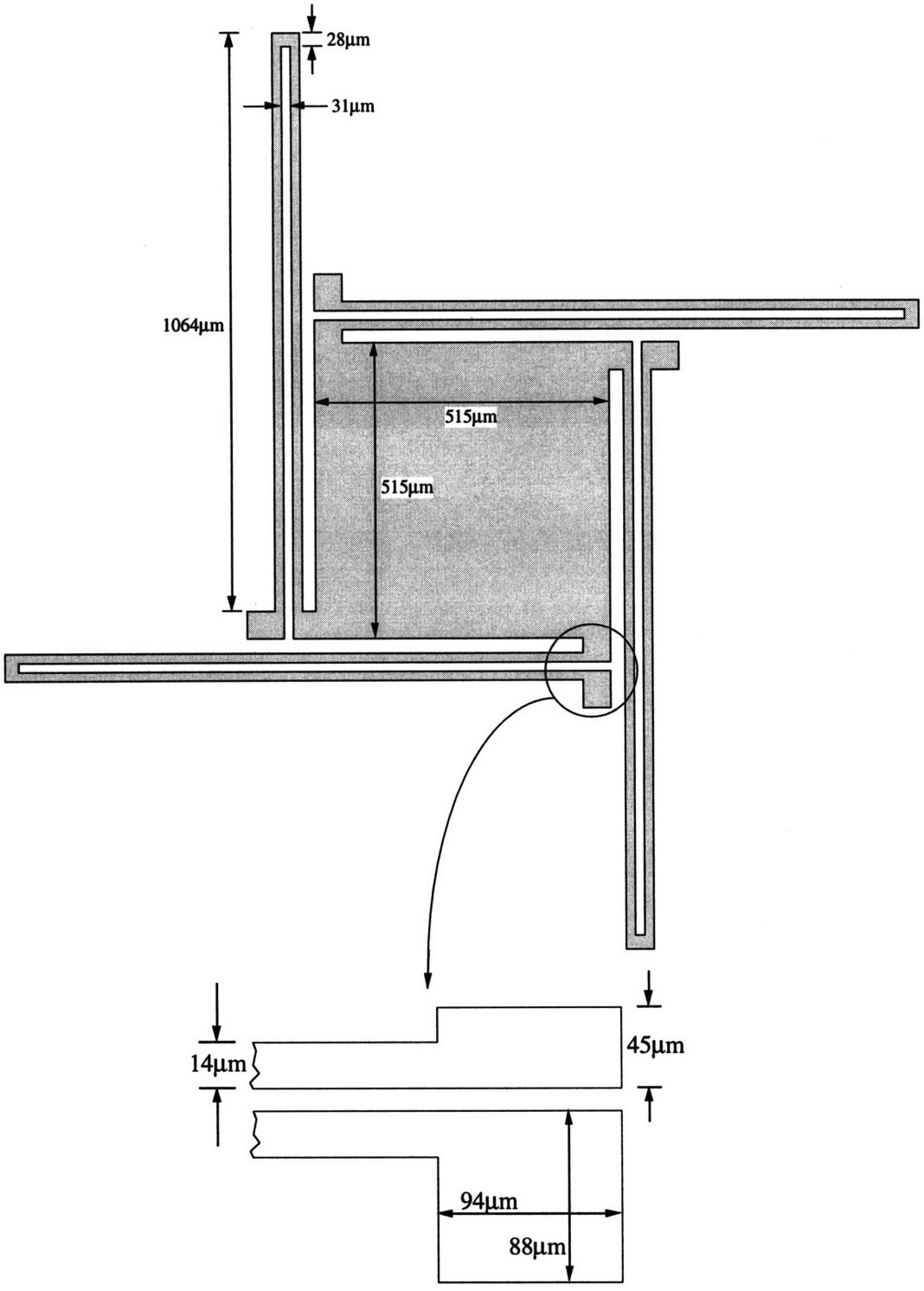


Figure A–6: Dielectrically isolated accelerometer #2 lateral dimensions.

Accelerometer #3 Lateral Dimensions

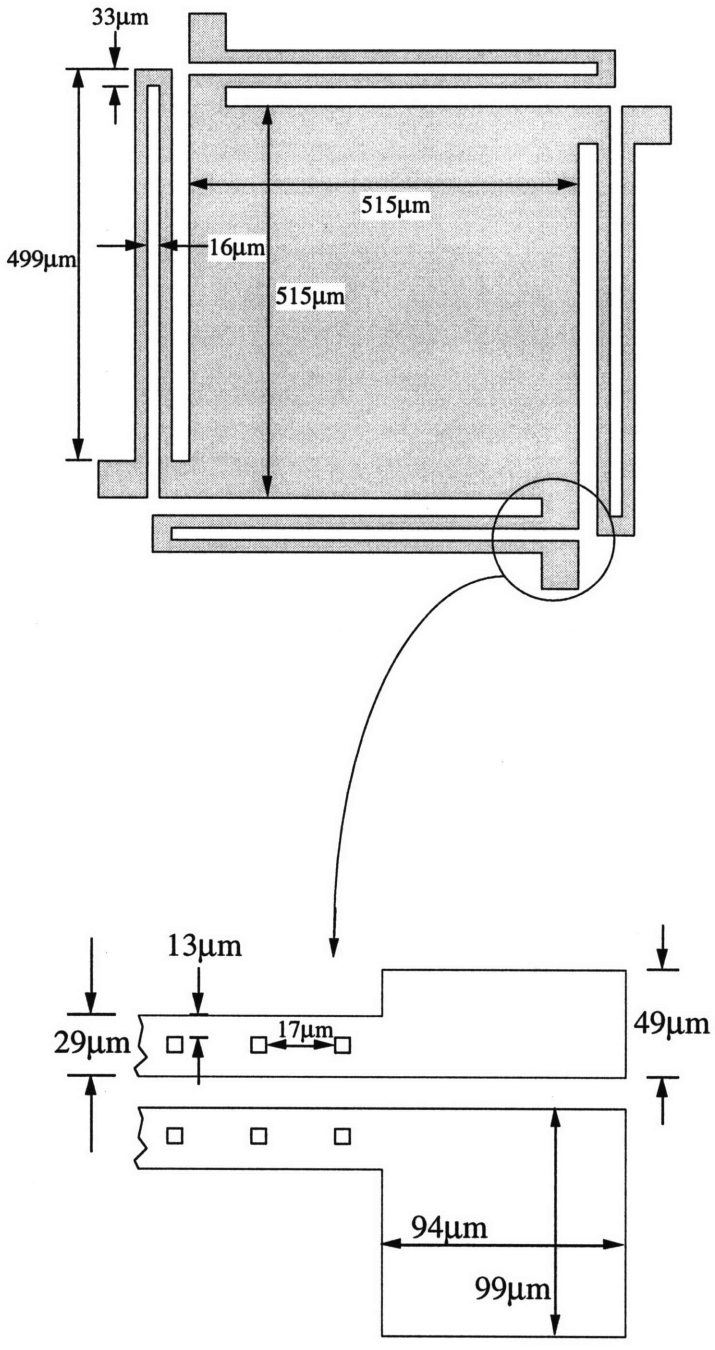
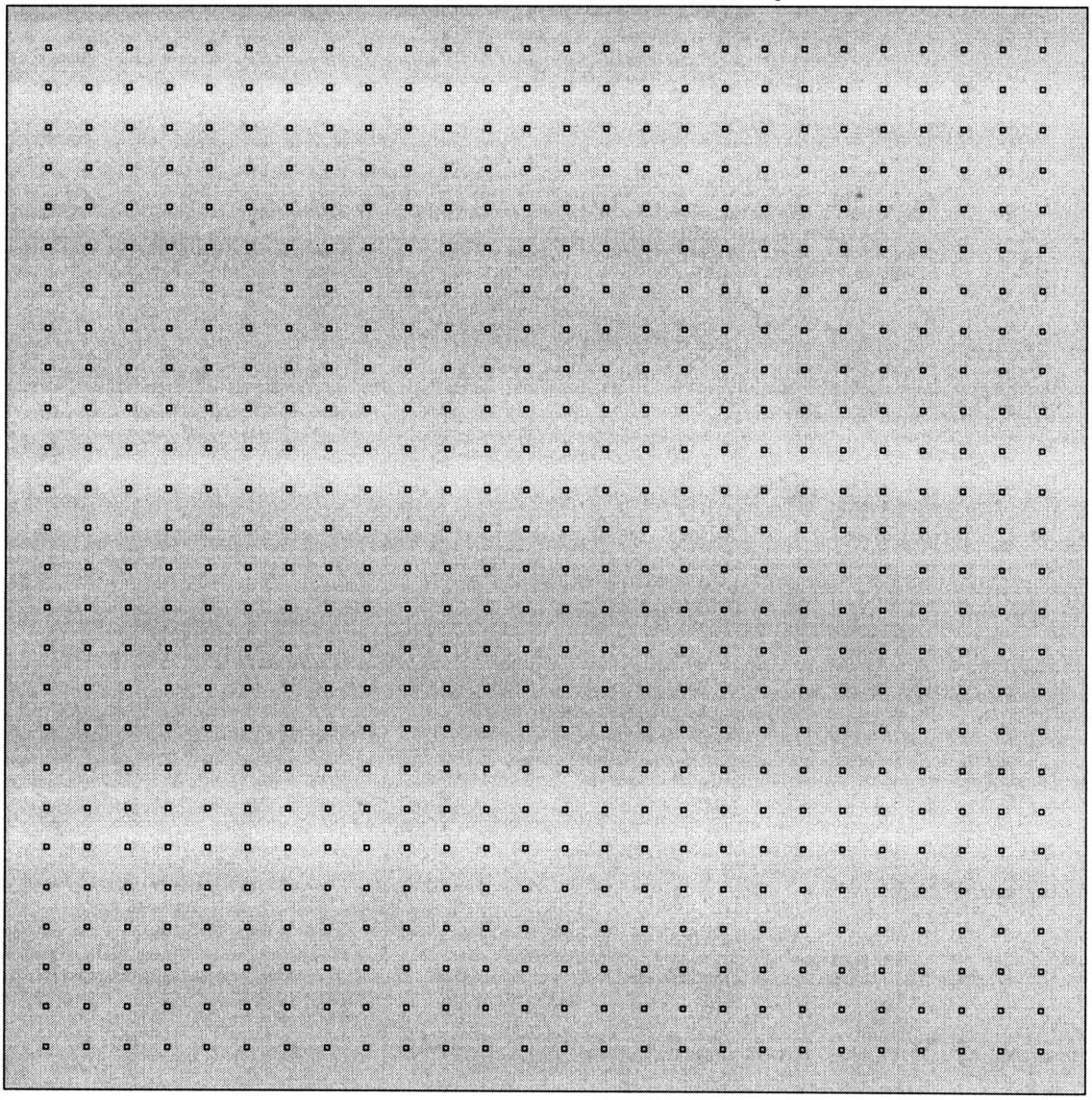
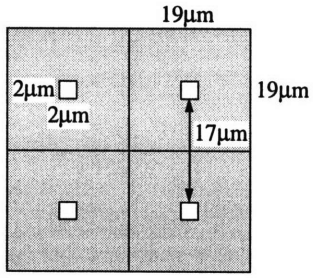


Figure A–7: Dielectrically isolated accelerometer #3 lateral dimensions.

Accelerometer Proof Mass Layout (1)





26 × 26 unit cells
515μm × 515μm

Figure A–8: Damping control aperture design (version one).

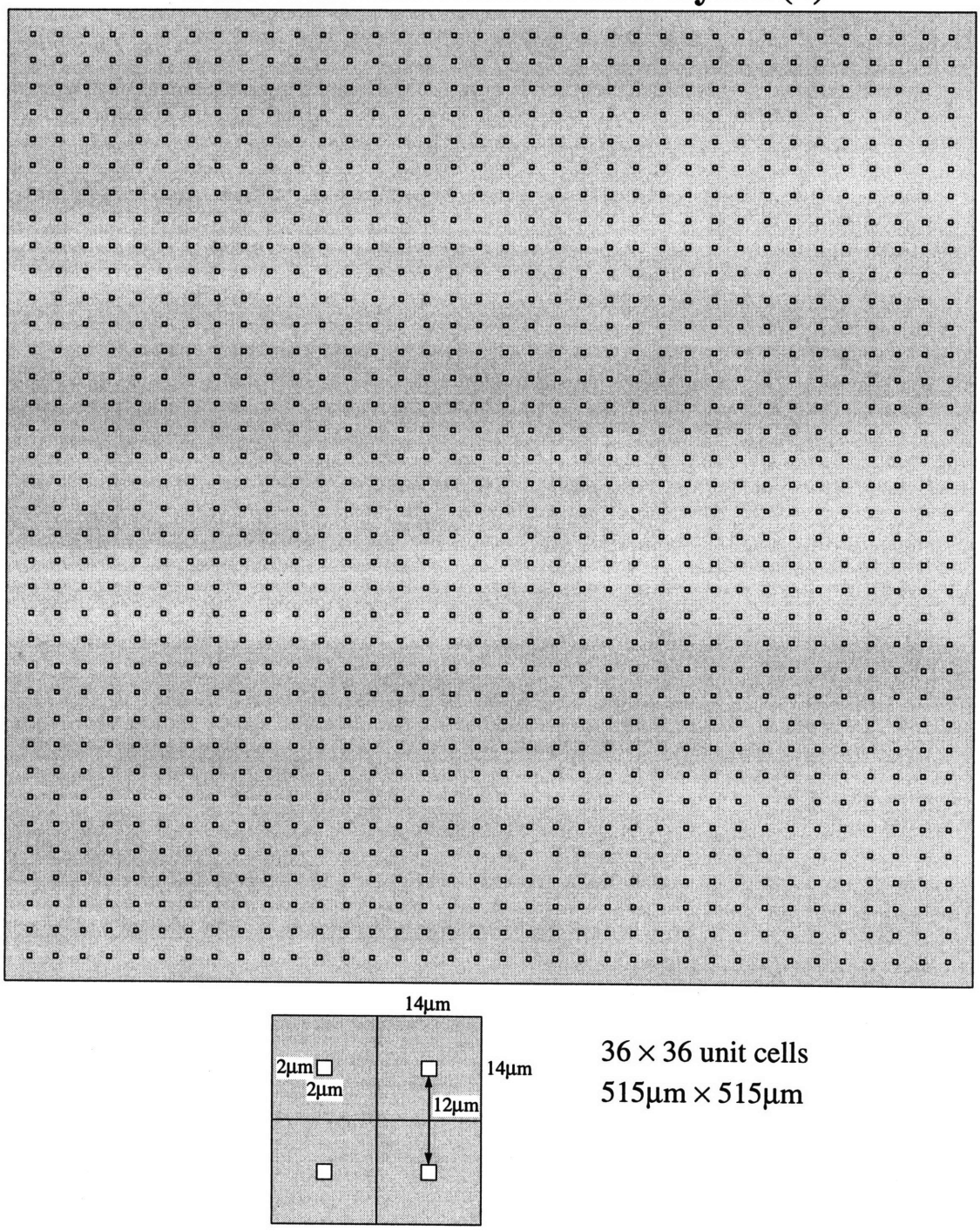


Figure A–9: Damping control aperture design (version two).

Appendix B

B.1 Process Travelers

PROCESS TRAVELER Revision 1
04/11/95

Silicon Hybrid-Accelerometer Process Flow

LOT NAME: accel_chsu
LOT OWNER: Charles Hsu

STEP #	STEP DESCRIPTION	STATUS

HANDLE WAFERS PREPARATION:

Starting material: 5 wafers p-prime 10-20Ω-cm.
DOUBLE SIDE POLISHED BY SILNET. Silnet polish to rear.

[TRL]

0.1	piranha clean	Number wafers: Date:
0.2	RCA	Number wafers: Date:

[ICL]

1.1	RCA	Number wafers: Date:

1.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:
2	ion implant (backside only) dopant: boron energy: 100keV dose : 5E15	Number wafers: Date:
3	drive-in (in N_2) recipe #253, tubeB1 or B2 (modify recipe #253 to do a 2-hour drive-in in N_2 at 1150°C)	Number wafers: Date:
4	strip SRO (7:1 BOE)	Number wafers: Date:
[TRL]		
5	pattern "HYBRID CAVITY" (mask #1) ch_photo.set	Number wafers: Date:
[ICL]		
6	plasma etch Si (1um etch) recipe #19, LAM-1	Number wafers: Date:
7	piranha strip resist	Number wafers: Date:
8.1	RCA	Number wafers: Date:
8.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:
9	ion implant (process side) dopant: boron energy: 70keV dose : 8E11	Number wafers: Date:

[TRL]

10	pattern "HYBRID DIFFUSION" (mask #2) ch_photo.set	Number wafers: Date:

[ICL]

11	ion implant (process side) dopant: phosphorus energy: 90keV dose : 7E15	Number wafers: Date:
12	piranha strip resist	Number wafers: Date:

[TRL]

13	pattern "HYBRID SRO" (mask #3) ch_photo.set	Number wafers: Date:

[ICL]

14	wet etch SRO (7:1 BOE)	Number wafers: Date:
15	piranha strip resist	Number wafers: Date:

DEVICE WAFERS PREPARATION:

Starting material: 5 device wafers (description shown in Section 4.3.2)

[ICL]

16.1	RCA	Number wafers: Date:

16.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:
17	ion implant (process side) dopant: phosphorus energy: 160keV dose : 5E15	Number wafers: Date:
18	drive-in (in N2) recipe #253, tubeB1 or B2 (modify recipe #253 to get a 15-hour drive-in run in N_2 at 1150°C)	Number wafers: Date:
19	strip SRO (7:1 BOE)	Number wafers: Date:

HANDLE AND DEVICE WAFERS READY FOR BONDING:

[TRL]

20.1	RCA	Number wafers: Date:
20.2	wafer bonding bond wafers in the single-wafer bonder (controlled ambient)	Number wafers: Date:
21	bonding anneal 1100°C bonding anneal in dry O_2 or N_2 ambient	Number wafers: Date:

SEALED CAVITY WAFER PROCESSING:

[AT&T or Lincoln Lab]

22	grinding and chemomechanical polishing (CMP)	Number wafers: Date:

[RGL]

23	electrochemical etch (20% by wt. KOH solution)	Number wafers: Date:

[RGL/TRL]

24	post-KOH clean	Number wafers: Date:

[TRL]

25	pattern "HYBRID STRUCTURE" (mask #4) ch_photo.set ** KSaligner in IR mode **	Number wafers: Date:

[ICL]

26	plasma etch 0.5μm Si recipe #19, LAM-1	Number wafers: Date:
27	piranha strip resist	Number wafers: Date:

[TRL]

28	pattern "HYBRID SCRIBE" (backside) (mask #5) ch_photo.set ** Ksaligner in IR mode **	Number wafers: Date:

[ICL]

29	plasma etch 2μm silicon scribe line recipe #19, LAM-1	Number wafers: Date:
30	piranha strip resist	Number wafers: Date:
31.1	RCA	Number wafers: Date:

31.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:
32	ion implant (process side) dopant: phosphorus energy: 90keV dose : 7E15	Number wafers: Date:
33	deposit 0.5μm LTO recipe #430, tubeA7 dLTO5k.set	Number wafers: Date:
34	densify LTO recipe #322, tubeA3 1000°C anneal in N_2 ambient	Number wafers: Date:
[TRL]		
35	pattern "HYBRID LTO" (mask #6) ch_photo.set	Number wafers: Date:
[ICL]		
36	wet etch LTO (7:1 BOE)	Number wafers: Date:
37	piranha strip resist	Number wafers: Date:
38	pre-metal HF dip (50:1 HF)	Number wafers: Date:
39	e-beam evaporation 1μm Al	Number wafers: Date:
[TRL]		
40	sinter Al tube A3, 15-min forming gas at 450°C	Number wafers: Date:

41	pattern "HYBRID SI_AU" (mask #7), on silicon wafer pattern "HYBRID GLASS_AU" (mask #8), on Pyrex 7740 glass wafer ch_photo.set (with AZ 5214-E resist)	Number wafers: Date:
42	descum ash for 2min	Number wafers: Date:
43	pre-metal HF dip (50:1 HF)	Number wafers: Date:
44	e-beam evaporation 100Å Cr + 0.5μm Au	Number wafers: Date:
45	acetone lift-off	Number wafers: Date:
46	nanostrip clean for 5min	Number wafers: Date:
47	coat 5μm AZ 4620 resist (process side)	Number wafers: Date:
[ICL]		
48	partial dicing (backside) diesaw, 150 μm-deep cut	Number wafers: Date:
[TRL]		
49	acetone strip resist	Number wafers: Date:
50	nanostrip clean for 2min	Number wafers: Date:
51	coat 5μm AZ 4620 resist (glass wafer)	Number wafers: Date:

[ICL]

52	dice glass wafer	Number wafers: Date:

[TRL]

53	acetone strip resist	Number wafers: Date:
54	nanostrip clean for 2min	Number wafers: Date:
55	pattern "HYBRID VENT" (mask #9) ch_photo.set (2.2 μm-thick resist)	Number wafers: Date:
56	descum ash for 2min	Number wafers: Date:
57	reactive ion etch PECVD/RIE 5μm silicon etch ** STS etch can be used here **	Number wafers: Date:
58	O_2 plasma ash resist RIE	Number wafers: Date:
59	nanostrip clean for 2min	Number wafers: Date:
60	pattern "HYBRID STRUCTURE" (mask #4) ch_photo.set (2.2 μm-thick resist)	Number wafers: Date:
61	descum ash for 2min	Number wafers: Date:
62	reactive ion etch PECVD/RIE 10μm silicon etch ** STS etch can be used here **	Number wafers: Date:
63	O_2 plasma ash resist RIE	Number wafers: Date:

64	manually break silicon and glass dies	Number wafers: Date:
65	UV ozone clean (Si and glass dies) 3-min clean	Number wafers: Date:
66	thermocompression bonding 350°C, 20psi, 2min	Number wafers: Date:
67	end process	

PROCESS TRAVELER

Revision 3
05/28/96

Silicon Discrete Accelerometer Process Flow

LOT NAME: accel_chsu
LOT OWNER: Charles Hsu

STEP #	STEP DESCRIPTION	STATUS
HANDLE WAFERS PREPARATION:		
Starting material: 5 wafers p-prime 10-20Ω-cm. DOUBLE SIDE POLISHED BY SILNET. Silnet polish to rear.		
[TRL]		
0.1	piranha clean	Number wafers: Date:
0.2	RCA	Number wafers: Date:
[ICL]		
1.1	RCA	Number wafers: Date:
1.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:
2	ion implant (backside only) dopant: boron energy: 100keV dose : 5E15	Number wafers: Date:

3	drive-in (in N_2) recipe #253, tubeB1 or B2 (modify recipe #253 to do a 2-hour drive-in in N_2 at 1150°C)	Number wafers: Date:
4	strip SRO (7:1 BOE)	Number wafers: Date:
5.1	RCA	Number wafers: Date:
5.2	grow 1μm thermal oxide recipe #223, tubeB1 or B2 1100°C, 2hr 15min	Number wafers: Date:
[TRL]		
6	pattern "ACCEL CAVITY" (mask #1) ch_photo.set	Number wafers: Date:
[ICL]		
7	wet etch oxide (7:1 BOE)	Number wafers: Date:
8	piranha strip resist	Number wafers: Date:
9.1	RCA	Number wafers: Date:
9.2	grow 0.1μm thermal oxide recipe #122, tubeA1 800°C, 47min 12sec	Number wafers: Date:
[TRL]		
10	pattern "ACCEL BUMPS" (mask #2) ch_photo.set	Number wafers: Date:

[ICL]

11	wet etch oxide (7:1 BOE)	Number wafers: Date:
12	piranha strip resist	Number wafers: Date:

DEVICE WAFERS PREPARATION:

Starting material: 5 device wafers (description shown in Section 4.4.2)

HANDLE AND DEVICE WAFERS READY FOR BONDING:

[TRL]

13.1	RCA	Number wafers: Date:
13.2	wafer bonding bond wafers in the single-wafer bonder (controlled ambient)	Number wafers: Date:
14	bonding anneal 1100°C bonding anneal in dry O_2 ambient	Number wafers: Date:

SEALED CAVITY WAFER PROCESSING:

[ICL]

15.1	RCA	Number wafers: Date:

15.2	deposit LPCVD silicon nitride recipe #410, tubeA5 1500Å	Number wafers: Date:
16	etch nitride (backside only) recipe #15, LAM-1	Number wafers: Date:
[RGL]		
17	chemical etch (20% by wt. KOH solution)	Number wafers: Date:
[RGL/TRL]		
18	post-KOH clean	Number wafers: Date:
[TRL]		
19	pattern "ACCEL STRUCTURE" (mask #3) ch_photo.set ** KSaligner in IR mode **	Number wafers: Date:
[ICL]		
20	plasma etch 0.5μm Si recipe #19, LAM-1	Number wafers: Date:
21	piranha strip resist	Number wafers: Date:
[ICL]		
22.1	RCA	Number wafers: Date:
22.2	grow SRO recipe #210, tubeA1 dsro430.set	Number wafers: Date:

23	ion implant (process side) dopant: phosphorus energy: 90keV dose : 7E15	Number wafers: Date:
24	implant drive-in tubeA3, idle condition 800°C, 4 hr, in N_2 ambient	Number wafers: Date:
25	strip SRO (7:1 BOE)	Number wafers: Date:
[TRL]		
26	pattern "ACCEL METAL" (mask #4) ch_photo.set (with AZ 5214-E resist)	Number wafers: Date:
[ICL]		
27	descum ash for 2min	Number wafers: Date:
28	pre-metal HF dip (50:1 HF)	Number wafers: Date:
29	e-beam evaporation (both sides) 1μm Al	Number wafers: Date:
[TRL]		
30	acetone lift-off	Number wafers: Date:
31	nanostrip clean for 5min	Number wafers: Date:
32	pattern "ACCEL VENT" (mask #5) ch_photo.set	Number wafers: Date:

[ICL]

33	descum ash for 2min	Number wafers: Date:
34	plasma etch 5μm Si recipe #19, LAM-1 ** STS etch can be used here **	Number wafers: Date:
35	O_2 plasma ash resist	Number wafers: Date:
36	nanostrip clean for 2min	Number wafers: Date:

[TRL]

37	pattern "ACCEL STRUCTURE" (mask #3) ch_photo.set (2.2 μm-thick resist)	Number wafers: Date:

[ICL]

38	descum ash for 2min	Number wafers: Date:
39	plasma etch 10um Si recipe #19, LAM-1 ** STS etch can be used here **	Number wafers: Date:
40	O_2 plasma ash resist	Number wafers: Date:

[TRL]

41	sinter Al tube A3, 15-min forming gas at 450°C	Number wafers: Date:
42	end process	

PHOTOLITH **ch_photo.set**
LOT # DATE (YYMMDD)

Operation	Parameter	DATA ENTRY	Time Required
dehydration	dehydration oven (200°C)		
HMDS	HMDS oven		
PR coating	coater (3000RPM)		
pre-bake	pre-bake oven (90°C)		
patterning	KS aligner		
developing	photo-wet station		
post-bake	post-bake oven (120°C)		

B.2 SUPREM Process Simulations

Hybrid-Accelerometer Process SUPREM Simulation Results

Handle Wafer Backside Contact Formation

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**********************************************************************

                              SUPREM-III
          Stanford Electronics Laboratories  Version 1B  Rev. 8507
             DEC/MIT  Version 2.04  SEG/CAD Release: 11-SEP-87
           Contact: Duane Boning   boning@caf.mit.edu   253-0450


                        Wed Apr  5 08:44:42 1995

**********************************************************************

     Simulation commands input from handle_back.in

   1... TITLE p-prime handle wafer backside preparation for the HYBRID_ACCEL project

   2... COMMENT initial wafer p-type <100> 15 ohm-cm (p-prime 10-20 ohm-cm)
   3... init silicon <100> boron conc=1e15 thickness=20 dx=0.01 spaces=200

   4... COMMENT grow SRO
   5... diffusion time=100 temp=950 dryo2
   6... diffusion time=30 temp=950 nitrogen

   7... COMMENT implant boron and drive-in
   8... implant boron dose=5e15 energy=100
   9... diffusion time=120 temp=1150 nitrogen

  10... COMMENT strip SRO
  11... etch oxide

  12... COMMENT regrow SRO
  13... diffusion time=100 temp=950 dryo2
  14... diffusion time=30 temp=950 nitrogen

  15... COMMENT implant boron one more time to assure a high surface concentration
  16... implant boron dose=5e15 energy=70

  17... COMMENT strip SRO
  18... etch oxide

  19... COMMENT bonding anneal at 1100C in N2
  20... diffusion time=70 temp=1100 nitrogen

  21... COMMENT get sheet resistance for the backside contact
  22... electrical extent=10
  23... end.electrical
```

```
 24... print active boron layers
 25... plot active net xmax=5
 26... stop


p-prime handle wafer backside preparation for the HYBRID_ACCEL project

initial wafer p-type <100> 15 ohm-cm (p-prime 10-20 ohm-cm)


grow SRO


implant boron and drive-in


strip SRO


regrow SRO


implant boron one more time to assure a high surface concentration


strip SRO


bonding anneal at 1100C in N2


get sheet resistance for the backside contact


Required Iterations =   2

                Electron       Electron       Electron
layer region     Charge     Sheet Conduct   Sheet Resist
  1      1    0.0000E+00     0.0000E+00     0.0000E+00

                  Hole           Hole           Hole          Sheet
layer region     Charge     Sheet Conduct   Sheet Resist    Resistance
  1      1    6.1689E+15     6.1259E-02     1.6324E+01     1.6324E+01

layer    material type      thickness   dx    dxmin top  bottom  orientation
 no.                        (microns)   (microns)   node  node  or grain size
  1    SILICON               19.9635 0.0100 0.0010  303   500      <100>

                      Integrated Dopant
layer            Net                        Total
 no.      active      chemical      active      chemical
  1    -6.1679E+15  -6.1731E+15   6.1679E+15   6.1731E+15
 sum   -6.1679E+15  -6.1731E+15   6.1679E+15   6.1731E+15

                      Integrated Dopant
layer           BORON
 no.      active      chemical
  1     6.1679E+15   6.1731E+15
```

sum	6.1679E+15	6.1731E+15

Junction Depths and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	junction depth (microns)	net active Qd	total chemical Qd
1	1	p	0.0000	6.1679E+15	6.1731E+15

Bottom Feedback Electrode Formation

```
******************************************************************************

                                SUPREM-III
          Stanford Electronics Laboratories  Version 1B  Rev. 8507
             DEC/MIT  Version 2.04  SEG/CAD Release: 11-SEP-87
           Contact: Duane Boning   boning@caf.mit.edu   253-0450


                        Thu Mar 30 12:31:13 1995

******************************************************************************

     Simulation commands input from bottom_electrode.in

   1... COMMENT simulate underlying feedback electrode process

   2... COMMENT initial wafer p-type <100> 15 ohm-cm
   3... init silicon <100> boron conc=1e15 thickness=20 dx=0.01 spaces=200

   4... COMMENT grow SRO
   5... diffusion time=100 temp=950 dryo2
   6... diffusion time=30 temp=950 nitrogen

   7... COMMENT blanket implant boron
   8... implant boron dose=8e11 energy=70

   9... COMMENT patterned implant phosphorus to form feedback electodes
  10... implant phosphorus dose=7e15 energy=90

  11... COMMENT bonding anneal thermal cycle
  12... diffusion temp=1100 time=70 nitrogen

  13... COMMENT cap gap 5000A LTO densification thermal cycle
  14... diffusion temp=1000 time=70 nitrogen

  15... COMMENT get sheet resistance
  16... electrical extent=10
  17... end.electrical

  18... print layers
  19... plot active boron phosphorus net xmax=5
  20... stop

 simulate underlying feedback electrode process

 initial wafer p-type <100> 15 ohm-cm


 grow SRO


 blanket implant boron


 patterned implant phosphorus to form feedback electodes
```

bonding anneal thermal cycle

cap gap 5000A LTO densification thermal cycle

get sheet resistance

Required Iterations = 6

layer	region	Electron Charge	Electron Sheet Conduct	Electron Sheet Resist
1	2	6.9355E+15	9.3811E-02	1.0660E+01
1	1	1.0324E+07	2.2637E-09	4.4175E+08

layer	region	Hole Charge	Hole Sheet Conduct	Hole Sheet Resist	Sheet Resistance
1	2	5.5492E+01	4.0643E-15	2.4604E+14	1.0660E+01
1	1	2.6982E+12	2.1531E-04	4.6445E+03	4.6445E+03

layer no.	material type	thickness (microns)	dx (microns)	dxmin	top node	bottom node	orientation or grain size
2	OXIDE	0.0419	0.0100	0.0010	298	300	
1	SILICON	19.9816	0.0100	0.0010	301	500	<100>

Integrated Dopant

layer no.	Net active	Net chemical	Total active	Total chemical
2	1.2391E+13	1.2391E+13	1.2541E+13	1.2541E+13
1	6.9338E+15	6.9464E+15	6.9393E+15	6.9518E+15
sum	6.9462E+15	6.9588E+15	6.9518E+15	6.9644E+15

Integrated Dopant

layer no.	BORON active	BORON chemical	PHOSPHORUS active	PHOSPHORUS chemical
2	7.5031E+10	7.5031E+10	1.2466E+13	1.2466E+13
1	2.7223E+12	2.7223E+12	6.9365E+15	6.9491E+15
sum	2.7973E+12	2.7973E+12	6.9490E+15	6.9616E+15

Junction Depths and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	junction depth (microns)	net active Qd	total chemical Qd
2	1	n	0.0000	1.2541E+13	1.2541E+13
1	2	n	0.0000	6.9375E+15	6.9501E+15
1	1	p	2.3465	1.7690E+12	1.7690E+12

Device Wafer Etch-Stop Formation

```
******************************************************************************

                                SUPREM-III
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               DEC/MIT  Version 2.04  SEG/CAD Release: 11-SEP-87
             Contact: Duane Boning   boning@caf.mit.edu   253-0450


                          Tue Aug 25 07:16:19 1994

******************************************************************************

     Simulation commands input from 10um.in

   1... COMMENT simulate device wafer with ECE etchstop

   2... COMMENT 10um wafer thickness after ECE

   3... COMMENT initial wafer p-type <100> 15 ohm-cm
   4... init silicon <100> boron conc=1e15 thickness=20 dx=0.01 spaces=200

   5... COMMENT grow SRO
   6... diffusion time=100 temp=950 dryo2
   7... diffusion time=30 temp=950 nitrogen

   8... COMMENT implant phosphorus and drive-in
   9... implant phosphorus dose=1e14 energy=160
  10... diffusion time=1380 temp=1150 nitrogen

  11... COMMENT strip SRO
  12... etch oxide

  13... COMMENT bond device wafer to handle with cavities

  14... COMMENT bonding anneal
  15... diffusion time=60 temp=1000 nitrogen

  16... COMMENT electrochemical etch until etchstop is reached

  17... print layers
  18... plot active net xmax=10


 simulate device wafer with ECE etchstop

 10um wafer thickness after ECE

 initial wafer p-type <100> 15 ohm-cm


 grow SRO


 implant phosphorus and drive-in
```

strip SRO

bond device wafer to handle with cavities

bonding anneal

electrochemical etch until etchstop is reached

layer no.	material type	thickness (microns)	dx (microns)	dxmin	top node	bottom node	orientation or grain size
1	SILICON	19.9816	0.0100	0.0010	301	500	<100>

Integrated Dopant

layer	Net		Total	
no.	active	chemical	active	chemical
1	9.4837E+13	9.4837E+13	9.8808E+13	9.8808E+13
sum	9.4837E+13	9.4837E+13	9.8808E+13	9.8808E+13

Integrated Dopant

layer	BORON		PHOSPHORUS	
no.	active	chemical	active	chemical
1	1.9857E+12	1.9857E+12	9.6822E+13	9.6822E+13
sum	1.9857E+12	1.9857E+12	9.6822E+13	9.6822E+13

Junction Depths and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	junction depth (microns)	net active Qd	total chemical Qd
1	2	n	0.0000	9.7666E+13	9.7666E+13
1	1	p	9.4781	1.1173E+12	1.1173E+12

Discrete Accelerometer Process SUPREM Simulation Results

Thermal Oxide Spacer Formation

```
*******************************************************************************

                                SUPREM-III
          Stanford Electronics Laboratories  Version 1B  Rev. 8507
             DEC/MIT  Version 2.04  SEG/CAD Release: 11-SEP-87
           Contact: Duane Boning   boning@caf.mit.edu   253-0450


                         Tue Sep 27 08:21:52 1994

*******************************************************************************

     Simulation commands input from 1um_oxide.in

   1... TITLE p-type handle wafer preparation for ACCELEROMETER project

   2... COMMENT initial wafer p-type <100> 15 ohm-cm (p-prime 10-20 ohm-cm)
   3... init silicon <100> boron conc=1e15 thickness=20 dx=0.01 spaces=200

   4... COMMENT grow 1um thermal oxide on the handle wafer

   5... COMMENT TubeA3, recipe#323

   6... COMMENT grow SRO
   7... diffusion time=100 temp=950 dryo2
   8... diffusion time=30 temp=950 nitrogen

   9... COMMENT implant boron and drive-in
  10... implant boron dose=5e15 energy=100
  11... diffusion time=120 temp=1150 nitrogen

  12... COMMENT strip SRO
  13... etch oxide

  14... COMMENT grow 1um thermal oxide in ICL
  15... diffusion time=135 temp=1100 weto2
  16... diffusion time=20 temp=1100 dryo2

  17... COMMENT bonding anneal at 1100C in N2
  18... diffusion time=70 temp=1100 nitrogen

  19... print active boron layers
  20... plot active net xmax=5
  21... stop


 p-type handle wafer preparation for ACCELEROMETER project

 initial wafer p-type <100> 15 ohm-cm (p-prime 10-20 ohm-cm)


 grow 1um thermal oxide on the handle wafer
```

TubeA3, recipe#323

grow SRO

implant boron and drive-in

strip SRO

grow 1um thermal oxide in ICL

bonding anneal at 1100C in N2

layer no.	material type	thickness (microns)	dx (microns)	dxmin	top node	bottom node	orientation or grain size
2	OXIDE	0.9910	0.0100	0.0010	299	317	
1	SILICON	19.5455	0.0100	0.0010	318	500	<100>

Integrated Dopant

layer	Net		Total	
no.	active	chemical	active	chemical
2	-2.0174E+15	-2.0174E+15	2.0174E+15	2.0174E+15
1	-2.8736E+15	-2.8737E+15	2.8736E+15	2.8737E+15
sum	-4.8910E+15	-4.8911E+15	4.8910E+15	4.8911E+15

Integrated Dopant

layer	BORON	
no.	active	chemical
2	2.0174E+15	2.0174E+15
1	2.8736E+15	2.8737E+15
sum	4.8910E+15	4.8911E+15

Junction Depths and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	junction depth (microns)	net active Qd	total chemical Qd
2	1	p	0.0000	2.0174E+15	2.0174E+15
1	1	p	0.0000	2.8736E+15	2.8737E+15

B.3 Process Modules

RCA Clean

The RCA clean is a standard wet chemical clean designed to remove organic and ionic contamihants fiorn the wafer surface before entering a high temperature (> 350°C) diffusion or oxidation step.

The organic clean consists of a 5:1:1 mixture of H_2O:NH_4OH:H_2O_2.The solution is heated to 80°C before the wafers are immersed in it. Following the organic clean (10mins), the wafers are immersed in deionized water (DI H_2O). The next step is to dip the wafers in a 50:1 H_2O:HF for 15secs, to remove any oxide which may have formed during the organic clean. The wafers are rinsed in DI H_2O again. The final step involves the ionic clean of the wafers in a solution of 6:1:1 of H_2O:HCl:H_2O_2. The solution is heated to 80°C before the wafers are immersed in it (for 15mins). Subsequent to the ionic clean, the wafers are again rinsed in DI H_2O and then they are spin-rinsed and dried.

Piranha Etch

Piranha is 3:1 solution of H_2SO_4:H_2O_2. This etch is often used to strip photoresist from the wafers (before metallization), to remove any organic contaminants from the wafer or to hydrate (create surface OH^- groups) the wafer surface before the wafer bonding step.

7:1 BOE Etch of Oxide

The buffered oxide etch (BOE) is a 7:1 solution of DI H_2O:HF buffered in NH_4F, which is used for etching oxides. The NH_4F is used to buffer the pH of the solution so that the photoresist layer will not delaminate from the wafer surface during the oxide etch. At room temperature the typical etch rate of thermal oxide in 7:1 BOE is 950Å/min.

Plasma Etch

All the "in-house" plasrna etches described in this thesis were carried out in a LAM Research model 480 etcher. The LAM etchers are cassette-to-cassette, load-locked, parallel etchers. The following table describes the parameters and the gas flow used in Recipe #19.

Process Parameters	**#01**	**#02**	**#03**	**#04**	**#05**	**#06**	**#07**
Chamber Pressure (rnTorr)	500	500	200	200	500	500	500
Top electrode Power (W)	0	300	0	300	0	0	50
Electrode gap spacing (cm)	1.5	1.5	1.5	1.5	1.5	1.5	1.5
CCl_4 flow rate (sccm)	0	0	130	130	0	3	3
O2 Flow rate (sccrn)	200	200	20	20	0	0	0
He flow rate (sccm)	100	100	70	70	120	120	120
Cl_2 flow rate (sccm)	0	0	0	0	0	0	0
SF_6 flow rate (sccm)	0	0	0	0	0	95	95
Process time	stable	6s	stable	10s	90s	stable	actual time

Photolithography

All the photolitbographic steps were performed in TRL using Solitec Inc., Model 5110 manual spinner with Blue M Model DDC-146C convection ovens for softbake and hardbake steps. A KarlSuss Model MA4 contact aligner with infrared (IR) alignment capability was used for all the patterning steps.

Photoresist

The positive photoresist used in all the photolithographic steps was OCG 825-35 CTS resist. The photoresist was developed using KTI 934 alkali-ion-free developer. The wafers were coated using a GCA model 1006 Wafertrac. The wafenrac is a cassette-to-

cassette process which uses an air-track wafer transport system and hot plate baking modules. Before the coating step, the wafers are primed in a HMDS (hexamethyldisilazane) vapor prime oven (Yield Engineering Systems, Inc., Model 3/10). The standard coating recipe (recipe #11) results in a photoresist layer thickness of 11,500Å (1.15μm). For some of the photolitbographic steps we also used a "thick-photoresist" process (recipe #7) which provides a photoresist thickness of 22,000Å (2.2μm). Also, both the recipes could be programmed to incorporate the edge bead removal (EBR) step.

For the metal lift-off step we used an image-reversal photoresist (AZ 5214-E). This photoresist was developed in AZ 422 MIF developer.

B.4 Freeze-Drying Procedure

Standard Frontside Dicing

There was a need to obtain "individual" accelerometers for packaging and testing purpose after the dielectrically isolated microaccelerometers have been successfully fabricated. Since the accelerometer chip, including electrical and mechanical test structures, is approximately 1cm×1cm, die separation was done either by manual cleaving or by "backside partial dicing" technique discussed in Chapter 4 with great success. However, individual microaccelerometers are only about 3mm×3mm or smaller, neither manual cleaving nor backside partical dicing worked to our satisfaction. A standard frontside dicing was then performed on the dies to obtain individual microaccelerometers. In order to protect the "free-standing" accelerometers during the dicing operation, a layer of 10 μm-thick resist (AZ 4620) was coated on the frontside of the wafer prior to dicing. The wafer was then diced to separate individual microaccelerometers.

Sticking and Freeze Drying

After removing the photoresist (with acetone) from the accelerometers, a freeze-drying method was employed to minimize *stiction.* As described previously regarding surface micromachining process, after etching the sacrificial layers in an undiluted (49%) HF solution, a specific drying procedure is required to prevent sticking of the free structural members to the substrate. Standard drying procedures such as drying spinning or air drying produce surface-tension forces that cause "pull-down" of the thin-film structures. Once contact has been made, other forces like van der Waals forces, electrostatic forces, chemical reactions, and hydrogen bridging come into play, resulting in permanet attachment of the structures to the substrate [79–81]. The so-called freeze-drying method was developed to solve this stiction problem. Guckel *et al.* [80] and later Takeshima *et al.*

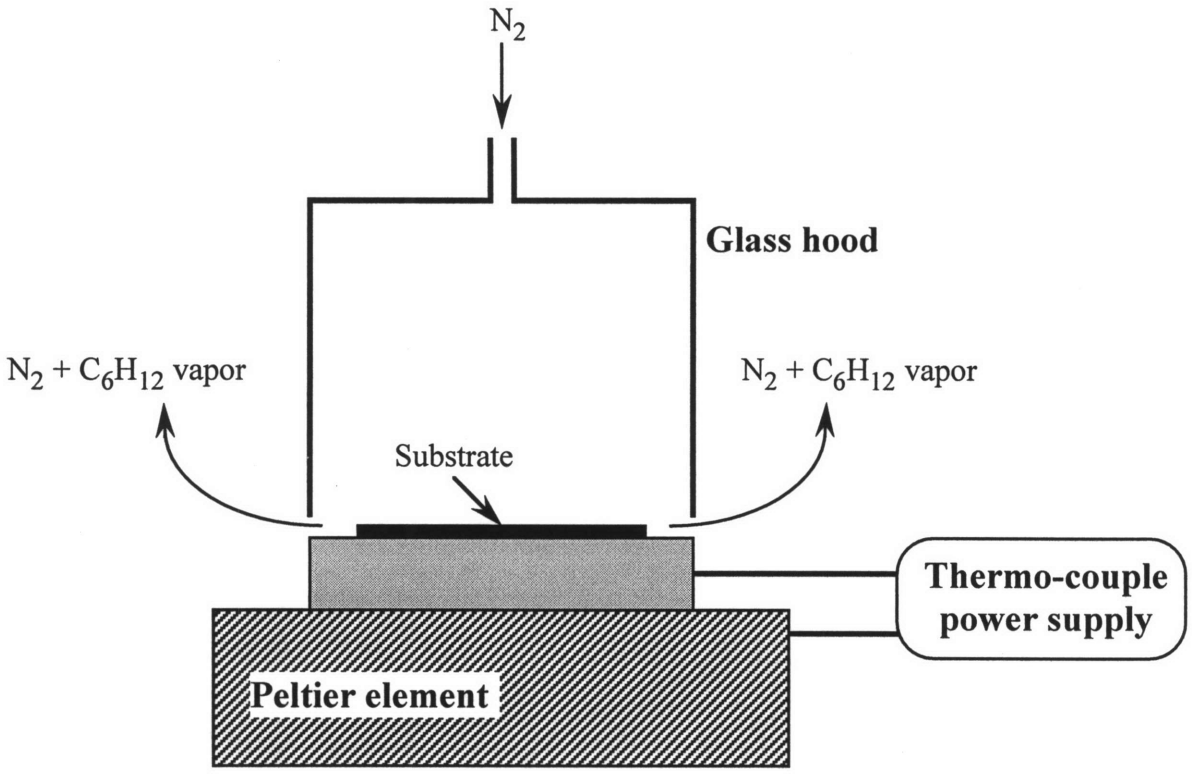


Figure B–1: Schematic of the experimental freeze-drying setup.

[82] implemented this technique for sacrificial-layer etching of surface-micromachined structures. They described a process whereby a final rinsing agent is frozen and subsequently sublimated in a few hours under vacuum conditions.

A new freeze-drying technique was presented by Legtenberg *et al.* [83] which does not require any vacuum equipment but instead can be performed under atmospheric conditions. Cyclohexane, which freezes at about 7°C, is used as the final rinsing agent. Freezing and subsequent sublimation are readily accomplished by placing the substrate under nitrogen flow on a regular Peltier element with a temperature below the freezing point (see Figure B–1). The total time for the freeze-sublimation process depends on the geometry of the sample and is typically 5-10mins for the structures described in this thesis.

Details of the rinse-freeze-sublimation procedure are described here: after the acetone strip of photoresist, the dies were placed in a beaker containing methanol to rinse off the acetone along with any resist residue. The dies were then placed in a beaker containing isopropyl alcohol for a thorough rinse. The dies were finally placed in cyclohexane, the final rinsing agent. After rinsing the dies in cyclohexane, they were placed upon a Peltier element that has already been cooled to 3°C. A nitrogen flow aided the sublimation process by removing cyclohexane vapors and preventing condensation of water. After sublimation was complete, the Peltier element was raised to room temperature, which completed the process. No residues were observed after the freeze-drying process. Microaccelerometers with aspect ratios (length/thickness) as high as 500, at gap spacing of 1μm, were obtained by this freeze-drying procedure.

Appendix C

Brüel & Kjær Reference Accelerometer

This section describes the B&K reference accelerometer used in this thesis. Figure C–1 illustrates the Delta Shear design of the B&K piezoelectric accelerometer . Figures C–2, C–3, and C–4 are the calibration report for our B&K 4379 reference accelerometer.

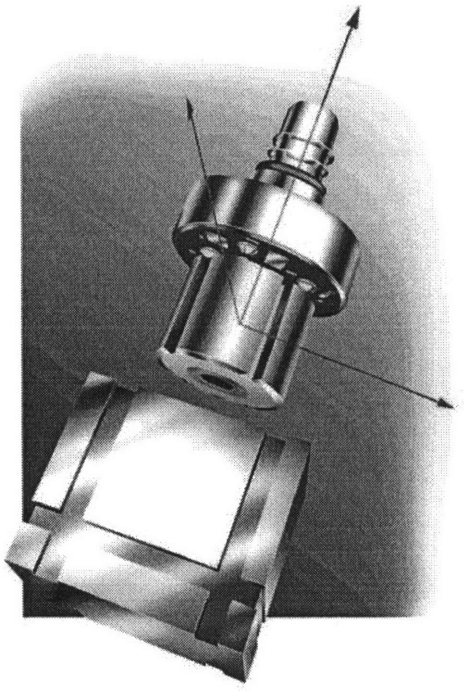


Figure C–1: A schematic view of the Delta Shear™ piezoelectric accelerometer.

Page 1 of 3.
Certificate Number 5591
Acello 4.96 Rev

Brüel & Kjær
CERTIFICATE OF CALIBRATION

REFERENCE STANDARD
This calibration is performed by comparison with Accelerometer Calibration Set Type 3506 Serial Number 680758

Calibrated by JSp Due Date 26 March 1998

CALIBRATION UNCERTAINTY
Reference Sensitivity At 160 Hertz:
a) Estimated uncertainty of Comparison:
± 1.1 % at 99% Confidence Level
b) Estimated uncertainty of Accelerometer Calibration Set Type 3506:
± 0.6% at 99% Confidence Level
c) Absolute Uncertainty:
$\sqrt{a^2 + b^2}$ = 1.3 % at 99% Confidence Level

MOUNTED RESONANCE
See Page 2 for Mounted Resonance Frequency and for frequency response relative to the reference sensitivity.

The mounted resonance response is obtained with the accelerometer mounted on a 180 gram stainless steel fixture as described in ANSI S2.61-1989.

Calibration Exciter Type 4290
Serial Number 1001293

Accuracy: 200 Hertz to 30% of the accelerometer mounted resonance frequency +/- 1 dB

Accelerometer Type 4379
Serial Number 1352556
Submitted by Massachusetts Institute of Technology

FINAL DATA
Reference Sensitivity at 160 Hertz, 31.6 ms^{-2} peak

Charge Sensitivity 303 pC/g, or 30.9 pC/ms^{-2}

Voltage Sensitivity 245 mV/g, or 24.9 mV/ms^{-2}

Capacitance (Including Cable) 1231 pF

Input Capacitance of Preamplifier C_i = 9.0 pF

This calibration is traceable to the National Institute of Standards and Technology Test Number 254888

The calibration of this accelerometer was accomplished using a test system which conforms with the requirements of MIL-STD-45662A.

This certificate, shall not be reproduced, except in full, without the written approval of the Brüel and Kjær Calibration Laboratory-Decatur, GA.

CONDITIONS OF TEST
Procedure Number 4379 1.90
Ambient Pressure 982 mbar
Temperature 22 °C
Relative Humidity 46 %
Date of Calibration 10 September 1996

Calibration Performed By Jana A. Smith
Date Certificate Issued 10 September 1996
Approved By

Brüel and Kjær Calibration Laboratory
2364 Park Central Boulevard
Decatur, Georgia 30035-3987
Phone 770/981-3831
FAX 770/981-8370

Figure C–2: Page 1 of B&K 4379 accelerometer calibartion certificate.

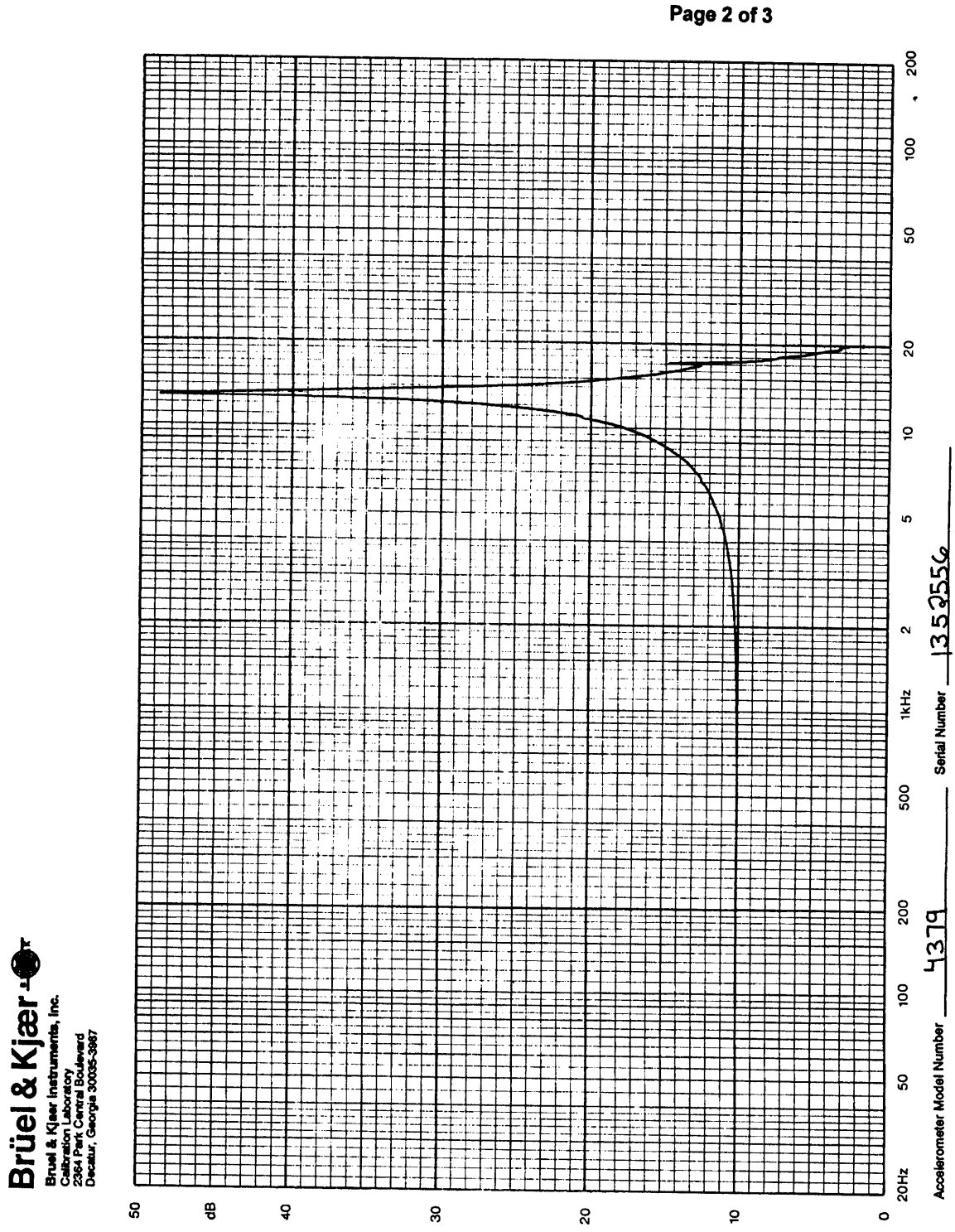
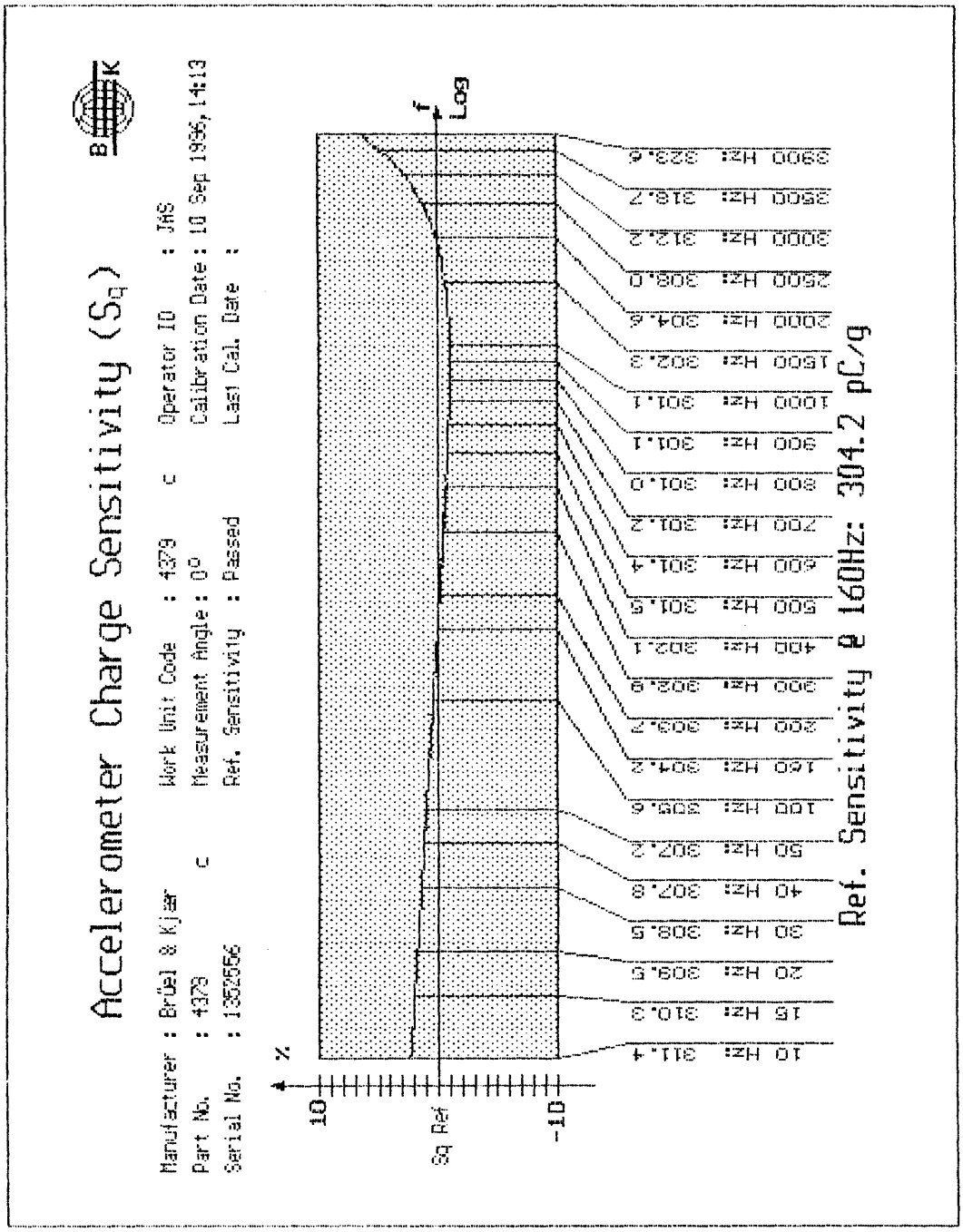


Figure C–3: Page 2 of B&K 4379 accelerometer calibartion certificate.

Page 3 of 3



This data is being provided by the Bruel and Kjaer Calibration Laboratory as a final Quality Check and verification of the data given on the cover of this calibration report.

Figure C–4: Page 3 of B&K 4379 accelerometer calibartion certificate.

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