

Micro-cleaved Ridge Lasers for Optoelectronic Integration on Silicon

by

Joseph J. Rumpler II

Submitted to the Department of Electrical Engineering and Computer
Science

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical Engineering

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

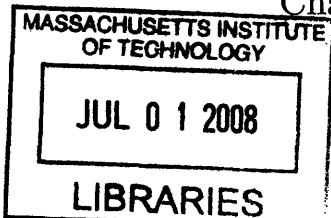
June 2008

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Abstract

This thesis addresses one of the last hurdles to optoelectronic integration on silicon, namely the incorporation of room-temperature, electrically-pumped edge-emitting laser diodes. To this end, thin ($\sim 6 \mu\text{m}$) InP-based multiple quantum well (MQW) ridge laser platelets emitting at a wavelength of 1550 nm have been manufactured and integrated by metal-to-metal bonding onto silicon substrates.

These laser platelets can be thought of as freestanding optoelectronic building blocks that can be integrated as desired on diverse substrates. These blocks are fully processed lasers, with both top side and bottom side electrical contacts. The thinness of these optoelectronic building blocks and the precision with which their dimensions are defined are conducive to assembling them in dielectric recesses on a substrate, such as silicon, as part of an end-fire coupled, coaxial alignment optoelectronic integration strategy. They are assembled by a micro-scale pick and place technique that allows the blocks to be picked up individually and placed as desired on any substrate. Integration is accomplished by metal-to-metal solder bonding.

To enable the manufacture of these laser blocks, a novel micro-cleaving process technology has been developed. This novel micro-cleaving process is used to simultaneously obtain both smooth end laser facets and precisely defined laser cavity lengths. As a proof of concept, this process has been shown to achieve nominal cavity lengths of $300 \mu\text{m} \pm 1.25 \mu\text{m}$. It is believed that this micro-cleaving process could be used in the future to make thin platelet lasers having much shorter cavity lengths and with better than $1.25 \mu\text{m}$ length precision.

For the $300 \mu\text{m}$ long, $6 \mu\text{m}$ thin, micro-cleaved ridge platelet lasers integrated onto silicon substrates, continuous-wave lasing at temperatures as high as 55°C and pulsed lasing at temperatures to at least 80°C have been achieved. These lasers have output powers as high as 26.8 mW (at $T = 10.3^\circ\text{C}$), differential efficiencies as high as 81% (at $T = 10.3^\circ\text{C}$), and threshold currents as low as 18 mA (at $T = 10.3^\circ\text{C}$). The characteristic temperatures, T_0 and T_1 , of the lasers on silicon were measured to be 43 K and 85 K, respectively.

To put the performance of these integrated micro-cleaved ridge lasers on silicon

in perspective, conventionally cleaved multiple quantum well (MQW) ridge lasers on their native InP substrate were also fabricated and tested. The thin micro-cleaved ridge platelet lasers integrated onto silicon outperformed the conventional lasers on InP in terms of thermal characteristics (maximum operating temperature, T_0 , and T_1), output power, and differential efficiency.

The structure of this thesis is as follows. First, the motivation for this work and the historical evolution of the optoelectronics field are briefly described. Next, the various optoelectronic integration techniques that have been pursued over the years and their limits are presented. The novel fabrication processes developed to manufacture these platelet lasers is then described in detail. Specifics on the characterization methods and measurement results of both the micro-cleaved ridge lasers on silicon and the conventionally cleaved ridge lasers on native InP substrates are presented. A technique, Magnetically Assisted Statistical Assembly, that could be potentially used to scale the integration technology to ultra-high densities of optoelectronic components is then theoretically described. Finally, the thesis concludes with a comparison with other state of the art results in the literature and proposes further directions for this research effort.

Thesis Supervisor: Clifton G. Fonstad, Jr.

Title: Professor

Acknowledgments

As I complete this chapter of my life, there are a great number of people I would like to thank. First, I would like to thank Professor Fonstad whose interesting projects on the topic of Optoelectronic Integration lured me here about seven years ago as a new graduate student.

I want to thank everyone in Professor Fonstad's research group. Not only have I enjoyed working with you all, I have enjoyed hanging out with you. To James Perkins and Ed Barkley, thanks for the great times. From our nearly daily social meetings in the office to our long hours spent in the lab to our sometimes even longer hours spent in the gym, I have had a truly awesome time spending time with you guys. There are a ridiculous number of inside jokes I will carry with me the rest of my life. Thanks to Diana Cheng for being so patient and understanding during this last term here when I was really swamped with trying to wrap up the thesis and passing off a lot of my experience with MASA to her. Thanks to Shaya Famenini, Mindy Teo, and Vivian Lei for always being friendly faces around Building 13. I want to thank Professor Sheila Prasad for making building 13 an enjoyable place to work. I will miss stopping by your office and catching up. I want to thank Henry Choy for showing me the ropes my first few years here.

I want to thank the members of my thesis committee, Professor Rajeev Ram and Professor Tayo Akinwande. I really appreciated the comments and insight you provided on my work.

I want to thank the folks out at Lincoln Lab, especially Jason Plant, Reuel Swint, and Paul Juodawlkis. Jason's willingness to help me with the ICP semiconductor etching was awesome. This was a huge enabler for the project.

I want to thank the folks over at MTL, namely Kurt Broderick, and Dennis Ward, who seemed to always go way out of their way to get the equipment back up and running when I really needed it. Thank you so much. I want to thank Bob Bicchieri, Eric Lim, and Dave Terry for their help over the years.

I want to thank the CMSE, especially Tim McClure, who always was there to

answer my questions on the P10 and Carl Zeiss Axioskop tools that I made use of so much in my work.

To all the people I've borrowed equipment from over the years, such as Professor Kolodziejcki and Dr. Gale Petrich, who let me use part of their laser testing setup. I want to thank Professor Ram again for letting me borrow equipment, such as the all-important TEC controller, that made all of the temperature analysis of my laser diodes possible.

I want to thank the folks associated with the 6.152J course. Over the years, I became a veteran TA of this course. Along the way I met some great people, namely Professor Tayo Akinwande, Professor Marty Schmidt, Professor Caroline Ross, Dr. Bob O'Handley, Li-Wen Wang, and Scott Poesse. I have had a blast and really thank you for the opportunity you gave me.

There are lots of friends around campus who have made my stay at MIT truly outstanding. As I am running against the clock to finish the thesis, I am reluctant to name everyone for fear of leaving off someone who has played an important role. One person I really have to mention by name is David Berns whose friendship gained during classes and working on "The Fund" is something I will remember the rest of my life.

Last but certainly not least I want to thank my family (my parents, Joe and JoAnn, my sisters, Jan and Jill and their families, and my brothers, Jim and Jason, and Kaiser) for all of their love and support. I also want to thank my Grandma Loretta and my Aunts and Uncles for their support. I want to thank my girlfriend Vivian Lei, who has been fundamental in me getting all this done. I also want to thank Cindy Ho, Vivian's Mom, for her well wishes and support. Getting a Ph.D., as I have learned, is a long journey with many ups and many downs. It helps so much when you have such great people in your life, making sure you keep the right perspective. Thank you so much for your support. I love you very much.

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Chapter 1

Motivation for Optoelectronic Integration

1.1 Introduction - Examples of Optoelectronic Products and their Impact

From the ways in which we communicate, to the ways our health is monitored, to the ways we are entertained, optoelectronic devices are becoming more pervasive in society. To provide the reader with some detail on the growing impact of optoelectronics on society, a couple of applications in the medical field and the field of communications strongly impacted by optoelectronic products will now be discussed.

In the medical field, doctors can now non-invasively monitor the oxygen level in a patient's bloodstream by using an optoelectronic instrument, known as a pulse oximeter. Operationally, when this device is placed on a patient's finger, toe, or ear lobe, light emitting diodes (LEDs) shine light that is either transmitted through or is absorbed by the blood. On the opposite end of the emitter array, a photodetector array measures the light that is transmitted. The amount of light transmitted depends on the amount of oxygen present in the blood.¹ Taking only a matter of seconds, this

¹In its simplest form, the measurement utilizes two wavelengths of light, red (i.e., wavelength around 650 nm) and infrared (i.e., wavelength around 900 nm). Hemoglobin with significant oxygen content absorbs more at infrared wavelengths than at red wavelengths as is shown in Figure 1-1.

non-invasive measurement allows medical professionals to continuously monitor the oxygen level in a patient's bloodstream. This fast accurate measurement is vital to the health of the patient since oxygen deprivation can result in brain damage within a few minutes. Before the commercialization of these devices, detecting the amount of oxygen in the bloodstream was a time consuming (i.e., tens of minutes) and painfully invasive process.

Non-invasive blood glucose monitoring for diabetics is another application in the medical field in which researchers are working to commercialize optoelectronic products.² The impact that such a device could have is far reaching as several hundred million people suffering from diabetes are at present resigned to drawing blood several times a day to measure their blood glucose level[62].

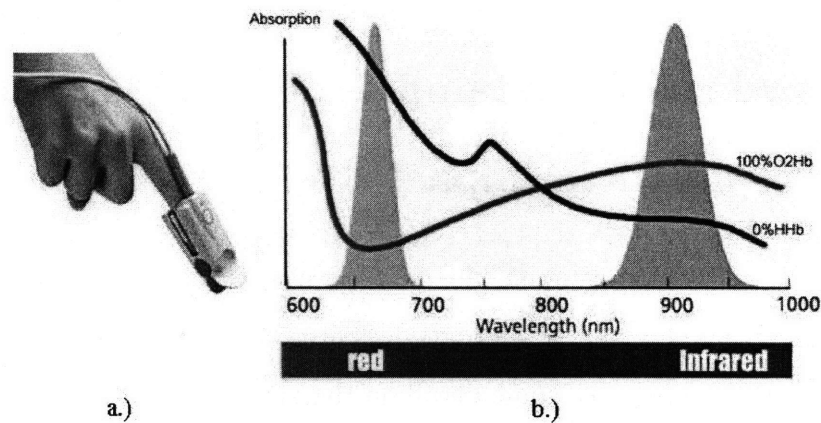


Figure 1-1: a.) A typical pulse oximeter [53] b.) Absorption spectrum of fully oxygenated hemoglobin and non-oxygenated hemoglobin[32].

Although the impact of optoelectronic devices on the medical field is impressive, it is arguable that optoelectronics has had its most significant impact in the field of communications, especially in long distance communications. In particular, the long distance undersea telecommunications network, which includes the link between Europe and North America, demonstrates how the development of several optoelectronic devices can revolutionize a field.

²Several companies, including VeraLight, Inc., are working to create non-invasive blood glucose monitors using optoelectronic devices.

There was a time when the undersea communication networks consisted of long spans of electrical coaxial cable with intermittently spaced electrical signal regenerators. However, near the end of the 1970s, the practical capacity (i.e., bits of information transmitted per second) limits of the the electrical network began to be approached. The problem with the electrical undersea network, as is the potential problem with all electrical interconnect networks, was that electrical interconnects have several frequency dependent parasitic impedances (i.e., resistances, capacitances, and inductances) which can degrade the transmitted signal. Specifically, the transmission capability for an electrical interconnect is limited by either skin effect³ loss as the signal transmission frequency is increased or resistive loss as the interconnect gets too long [67].

According to Miller et al., the transmission capacity of an electrical interconnect is directly proportional to the cross-sectional area of the interconnect and inversely proportional to the interconnect length squared:

$$Capacity \propto \frac{A}{l^2} [67] \tag{1.1}$$

Thus, for an electrically interconnected network, capacity increases can only be made by enlarging the coaxial core diameter, reducing the spacing between signal regenerators, or by utilizing more complicated modulation schemes. By the late 1970s, the capacity limit for coaxial undersea networks had been reached for all intents and purposes[10].

Optical signals, on the other hand, do not suffer from this signal distortion as the length of transmission or the signal transmission frequency is increased. Thus, in the 1980s, with the tremendous quality improvements (i.e., lower loss) having been made in optical fibers combined with the development of semiconductor lasers and corresponding photodetectors, undersea electrical networks began to be replaced with optoelectronic networks consisting of long spans of optical fiber with intermittently

³The skin effect is the phenomena that as the frequency of a signal is increased, the electromagnetic waves and thus the current density associated with this signal penetrate less and less into a conductor. As the current density is constrained to a thinner and thinner thickness of the conductor, the effective resistance increases substantially.

spaced optical-to-electrical-to-optical signal regenerators. This resulted in significant capacity increases as is shown in Figure 1-2.

In the 1990s, the optical-to-electrical-to-optical signal regenerators were replaced with newly commercialized Erbium Doped Fiber Amplifiers. This invention along with the development of large channel count wavelength division multiplexers enabled the capacity of the undersea network to increase even more substantially as is shown in Figure 1-2.

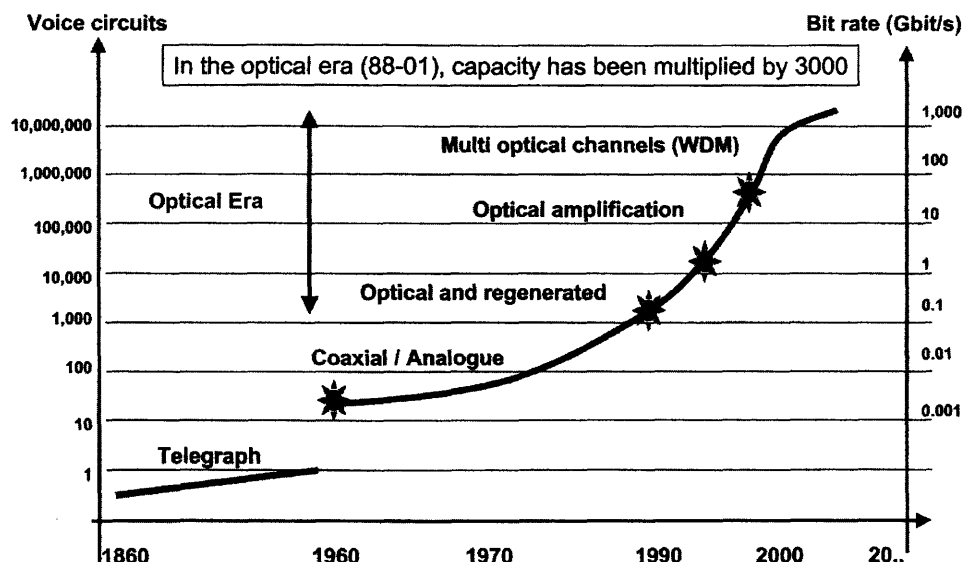


Figure 1-2: Historical transatlantic undersea network capacity [20].

The optoelectronics industry has recently entered a new phase in its development. This phase is aimed at integrating many of the powerful optoelectronic devices that have revolutionized the communications field onto a single chip, a process referred to as optoelectronic integration.

Using the communications field as a vehicle, the historical evolution of the optoelectronic integration research effort will now be detailed.

1.2 Historical Evolution of the Optoelectronic Integration Effort

The research topic of optoelectronic integration is not a new one. The concept of optoelectronic integration dates back to the late 1960s when Stewart Miller of Bell Labs published the paper "Integrated Optics: An Introduction" in the Bell System Technical Journal [68]. In this paper, Miller presented the idea of "miniature optical circuitry" that could transport optical signals much like newly developed microelectronic circuits that carried electrical signals.

To provide some context, less than a decade earlier, the first semiconductor laser had been demonstrated [35]. In the microelectronics industry, companies such as Intel (1968), Advanced Micro Devices (1969), and Fairchild Semiconductor (1957) had just been formed and were pioneering semiconductor microfabrication techniques to make miniature electronic circuits. It was an exciting proposition to extend the use of these techniques to manufacture integrated optoelectronic devices. Optical communications, however, was still at its infancy stage. The best optical fibers at this time had transmission losses in the tens of dB/kilometer [36]. The best semiconductor lasers could not yet run continuous wave at room temperature. Then, there was the significant issue of coupling light from the devices into the micron size diameter fiber cores. Unfortunately, the device technology was not yet at a mature enough level to seriously consider optoelectronic integration.

With the idea of optoelectronic integration planted way back in the late 1960s, the quality and diversity of photonic devices increased significantly over the next few decades. By the 1970s, low loss silica fiber was manufactured on a large scale. By the 1990s, highly reliable low threshold single mode semiconductor lasers were being manufactured. There are a great number of accounts detailing the optical communications technology development during this time [88, 36, 87]

With these device improvements, optoelectronic integration began to be considered more actively in the research community. In the 1990s, the optoelectronic integration research effort really took off when new devices, most notably the Erbium

Doped Fiber Amplifier (EDFA) and the Arrayed Waveguide Grating (AWG) were commercialized. These devices enabled the implementation of Wave Division Multiplexing (WDM).⁴ A simple WDM system where four different signals are wavelength multiplexed onto a single fiber is shown schematically in Figure 1-3.

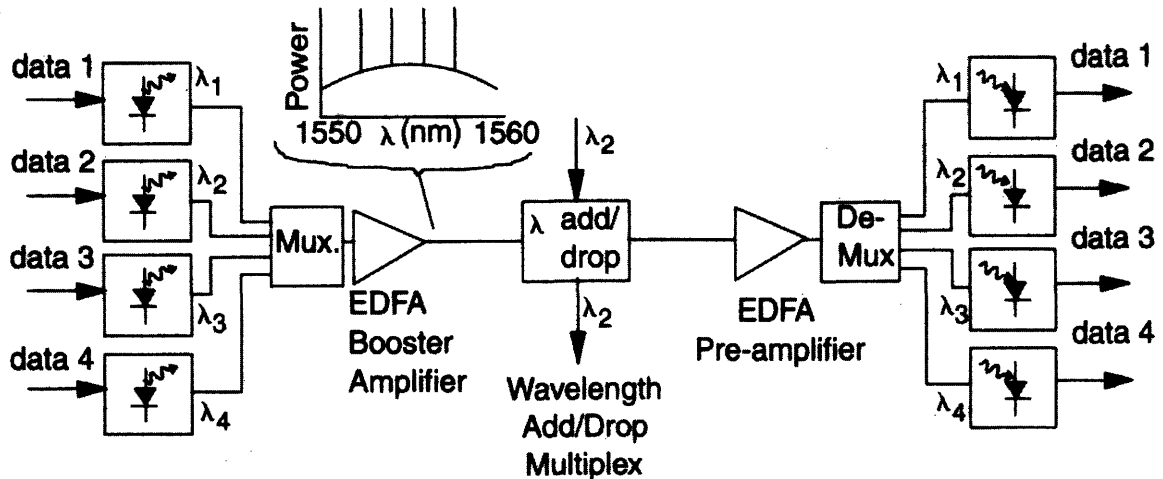


Figure 1-3: Functional schematic of a basic WDM network where four wavelengths are multiplexed on a single fiber, travel a long distance and then are demultiplexed[28].

With the increased transmission capacity provided by WDM, there was now a need for a large number of narrow linewidth lasers as well as many other complementary devices such as variable optical attenuators, channel equalization filters, optical modulators, and photodetectors. In response to the burgeoning market demand for these devices in the late 1990s, companies rushed in trying to profit. With the confluence of these major device breakthroughs along with the hypercompetition in the optoelectronic components industry, combining many of these high quality devices on a single substrate to produce cost-effective solutions was the logical next step. Thus, the optoelectronic integration research and development effort grew substantially.

A number of integrated products were introduced in the market during this time. For example, several companies manufactured distributed feedback (DFB) lasers in-

⁴Theorized in the 1970s, WDM involves simultaneously transmitting multiple optical signals, each at a different wavelength, on a single fiber. This enables the network capacity to be increased significantly without laying new fiber.

tegrated with electro-absorption (EA) modulators[60, 3]. Bookham, Inc. introduced an AWG multiplexer with integrated variable optical attenuators (VOAs)[2]. NTT integrated optical amplifiers and photodetectors with AWGs (see Figure 1-4).

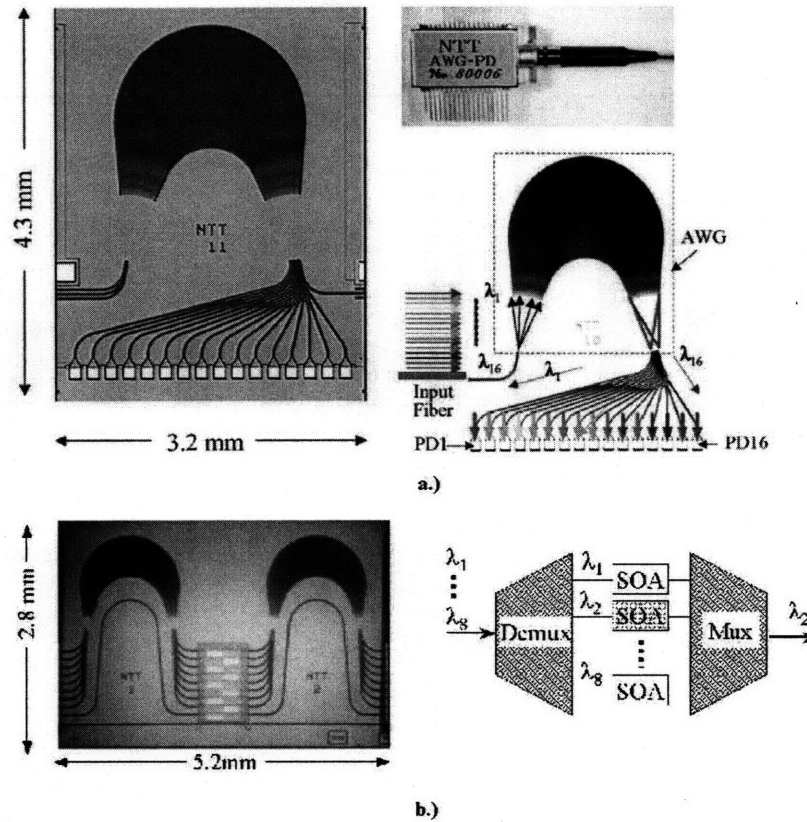


Figure 1-4: a.) Schematics and picture of a 16 channel AWG integrated with 16 photodetectors, b.) Schematic and picture of a monolithically integrated AWG mux, demux, and semiconductor optical amplifier (SOA) array[59].

Although significant progress was made in terms of integration capability, the optoelectronics market growth seen in the late 1990s up through 2001 could not be maintained. The demand projections for optoelectronic components turned out to be gross overestimations as so many working in the photonics industry during this time, including the author of this thesis, disappointedly found out. From 2000 to 2001, the total market for laser-diodes was cut in half (Figure 1-5) and the photonic integrated circuit market performed nearly as poorly (Figure 1-6).

Undoubtedly, this optoelectronic product demand collapse (i.e., "the busting of

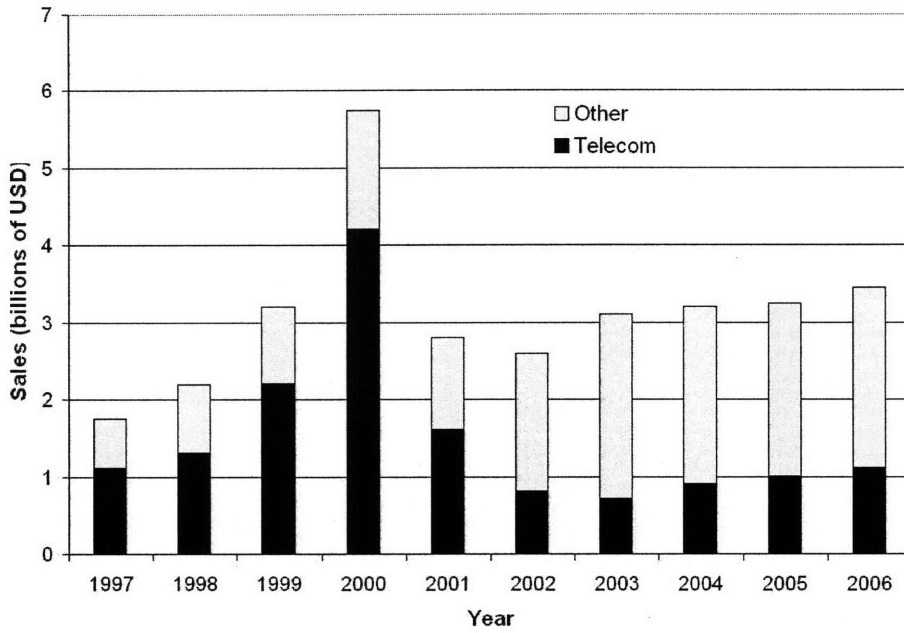


Figure 1-5: Historical laser-diode and telecom laser-diode market from 1997 up through 2006[79].

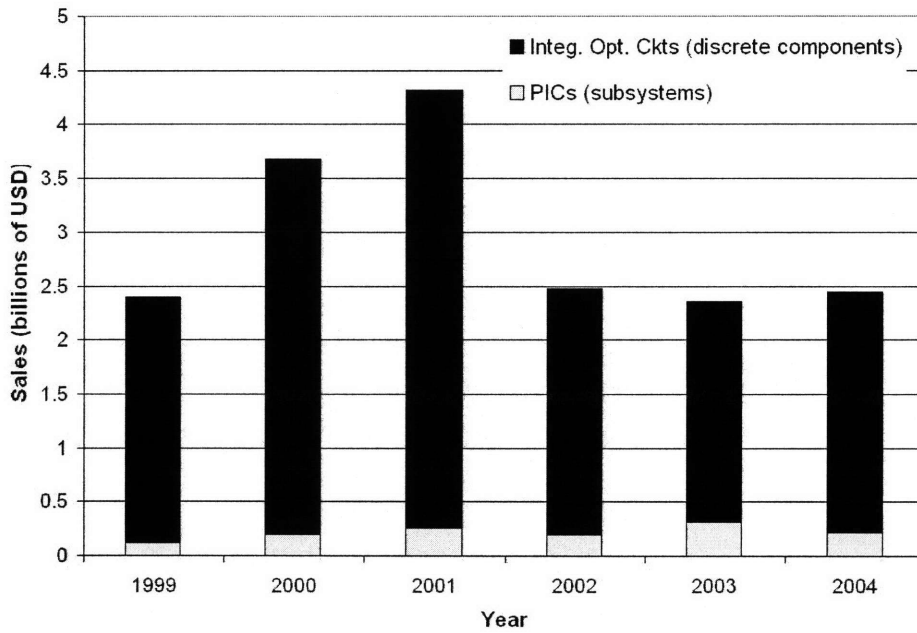


Figure 1-6: Historical photonic integrated circuit subsystem and discrete components markets from 1999 up through 2006 [4, 5].

the telecom bubble”) impeded the integration effort. From 2001 to 2004, 655 telecommunications companies with aggregate assets of 749 billion USD filed for bankruptcy [11].

Almost a decade after the telecom boom years, the telecommunications market is growing again. These gains are primarily due to the surging demand for broadband resulting from the ever increasing preponderance of video online.⁵ Moreover, by the beginning of 2007, the percentage of adults in the United States with home broadband access had risen to near 50% compared to only 10% back in 2002[11]. Equipment spending in the telecommunications sector is growing substantially (Figure 1-7). This bodes well for the funding of optoelectronic integration research in the near future.

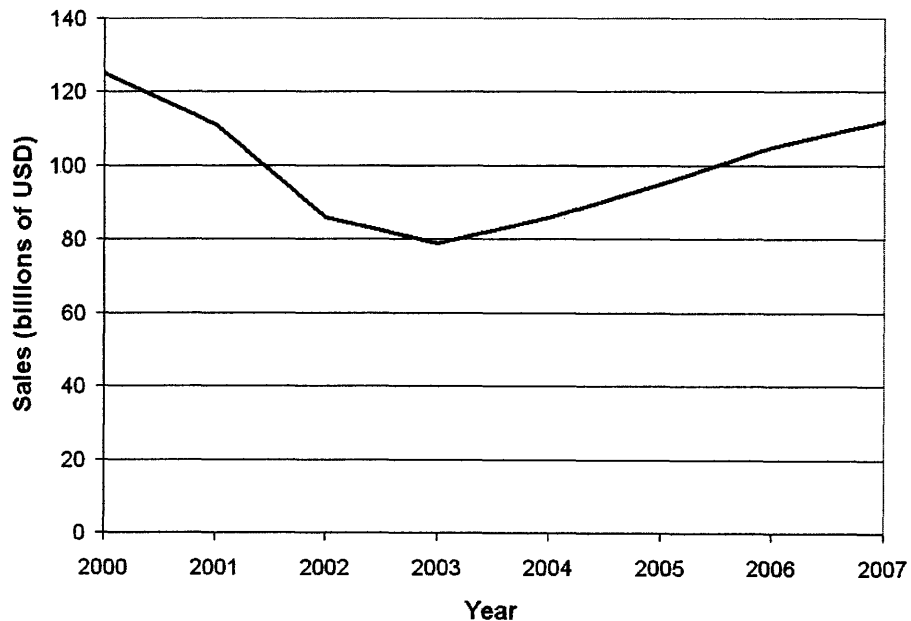


Figure 1-7: Historical telecommunication equipment sales [11].

⁵Back in the bust years, the main bandwidth consuming application was online music which consumes roughly a factor of one thousand times less bandwidth than video[11].

1.3 Modern Optoelectronic Integration Effort

With all the progress made in the communications industry in the late 1990s, it is not surprising that the primary area today which could be profoundly impacted by increased optoelectronic integration is still the field of communications. Differentiating between the two eras, the development in the late 1990s seemed to be focused on the long-haul telephony or wide-area network markets; whereas, today, the effort has shifted to shorter distance communications, including the last mile of the optical network, as well as chip-to-chip and on-chip interconnection.

1.3.1 Last Mile of the Optical Network

Fiber-to-the-home (FTTH) / Fiber-to-the-premises (FTTP) are synonymous technologies that address the last mile of the optical network. As their names imply, FTTH/FTTP refer to extending the optical network by the installation of optical fiber directly to homes. Presently, the last mile of the communications network, by and large, consists of twisted pair wire electrical interconnects.

In terms of performance, FTTH offers orders of magnitude bandwidth improvements over competing electrical interconnect technologies such as digital subscriber lines (DSL) and cable modem systems as is shown in Figure 1-8.

The use of FTTH technology has expanded considerably in the past several years as service providers in Asian nations like Korea, Japan, and European nations like Denmark and Sweden have made significant installments [24]. In North America, the largest potential market for FTTH equipment in the world, installations have risen significantly in the past couple years (Figure 1-9), but still lag behind the aforementioned countries in terms of percent market penetration.

A powerful role optoelectronic integration could play in FTTH is by enabling the manufacture of high data-rate, low cost optoelectronic transceiver products that convert the signals from the optical network to electrical signals that a computer can understand as well as convert electrical signals from a computer to optical signals that can be used to communicate with the optical network.

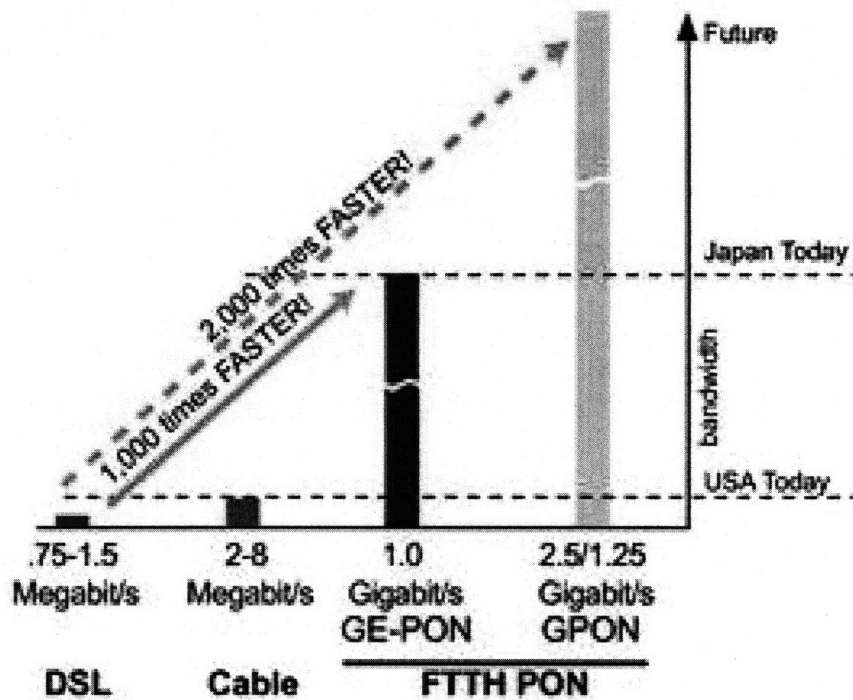


Figure 1-8: Bandwidth comparison between DSL, cable modem, and FTTH technologies. Note DSL, cable, and FTTH GE-PON (Passive Optical Network) are in volume deployment; whereas, the FTTH GPON is still in development[74].

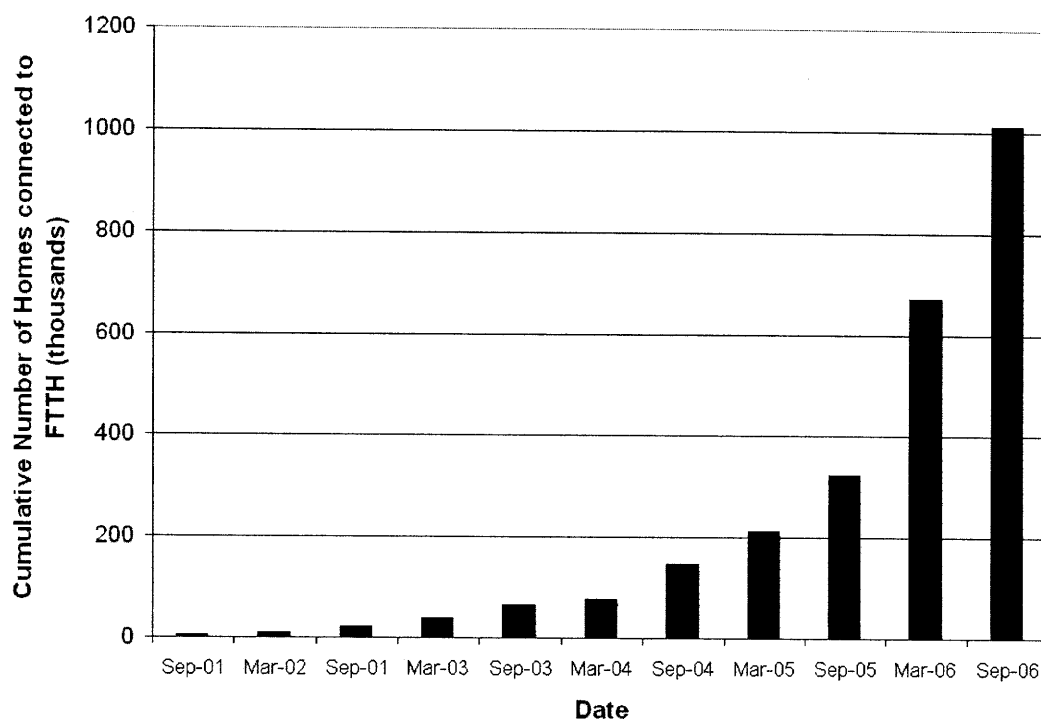


Figure 1-9: Cumulative number of homes in North America connected to FTTH [57].

Specific products in the FTTH market that could be impacted by increased integration capability are triplexers and diplexers [75]. A triplexer (Figure 1-10a) is essentially an optical transceiver which receives optical signals at wavelengths of 1490 nm and 1550 nm, converts them to electrical signals and transmits a optical signal back at 1310 nm. Utilizing such a product, the electrical signals can then be interpreted by a personal computer or set-top box in one's home.

A diplexer (Figure 1-10b) operates in a very similar manner to the triplexer, but instead of receiving two input wavelengths, it only is prepared to receive one.

If the 1310 nm laser, photodetectors and electronics could be integrated together on a single chip, the costs of the diplexer and triplexer products could be reduced dramatically. These reduced component costs could help accelerate the growth of the extremely price sensitive FTTH market.

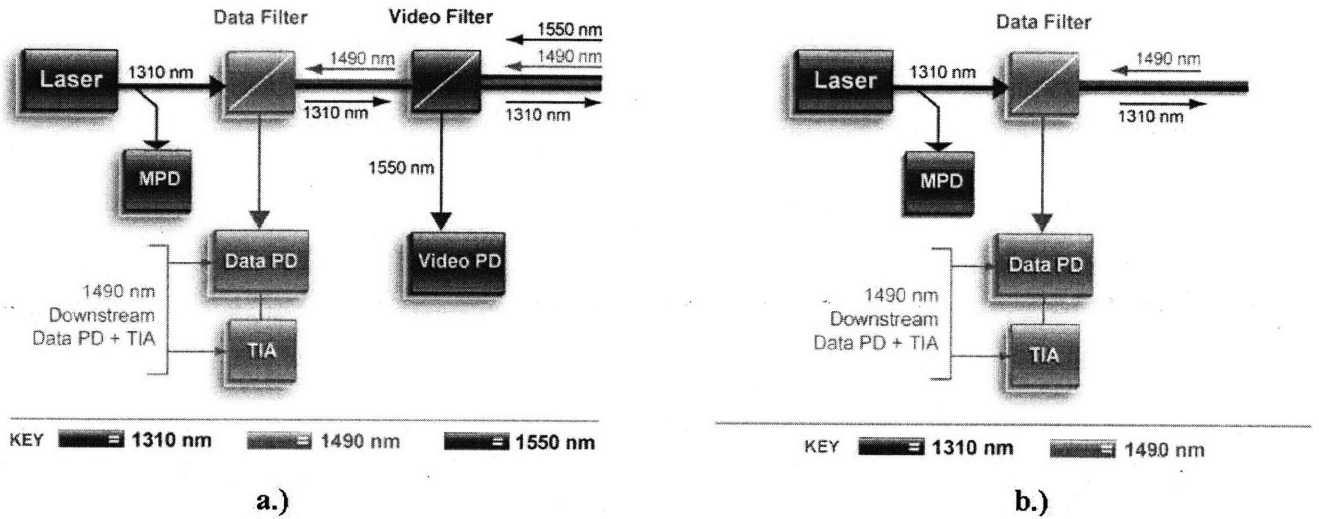


Figure 1-10: Schematic of a.) FTTH triplexer, b.) FTTH diplexer. Note, PD = photodetector, MPD = monitor photodetector, and TIA = transimpedance amplifier[91].

1.3.2 Chip-to-Chip and On-chip Optical Interconnects

Of great interest now in the research community is the role optoelectronics can play in ultra-short distance communications; in other words, communicating between chips or between devices on a single microchip. Chip-to-chip interconnection, as its name implies, refers to an optical link between two or more separate chips. In this case, the optical signal is typically transmitted over a distance of about 5 to 100 mm. On-chip interconnection, involves interconnecting different devices on a single chip. In this application, optical signals are usually transmitted over a distance of no more than 20 mm. Not as commercially developed as the FTTH/FTTP market, the work on chip-to-chip and on-chip optical interconnects is primarily a research effort now.

As was the case for longer distance communications networks, the allure of an optical solution for short distance applications is an increase in bandwidth. Moreover, the same problems which limited the capacity of the longer distance electrical networks, namely, interconnect parasitics and related signal degrading phenomena such as the skin effect, are the same issues that will likely limit the bandwidth of these shorter distance electrical interconnects.

Chip-to-chip Interconnects

Applied to chip-to-chip interconnection, optoelectronic integration could enable a significant bandwidth improvement between a microprocessor and other chips on a motherboard such as other microprocessors, memory, or chipsets. The standard electrical interconnect medium used today, copper traces, will likely be limited to data transfer rates of 15 to 20 gigabits per second due to the parasitic effects described earlier [95].

In anticipation of reaching these bandwidth limits, several research groups are pursuing optoelectronic solutions [48, 95]. Specifically, researchers at Intel Corp. have demonstrated a chip-to-chip twelve channel optical link consisting of GaAs Vertical Cavity Surface Emitting Lasers (VCSELs), Si p-i-n photodiode arrays, polymer waveguide arrays, and a Complementary Metal Oxide Silicon (CMOS) transceiver chip (Figure 1-11) that reached speeds of greater than eight giga-transfers per second. This chip-to-chip optical interconnect prototype is shown in Figure 1-11.

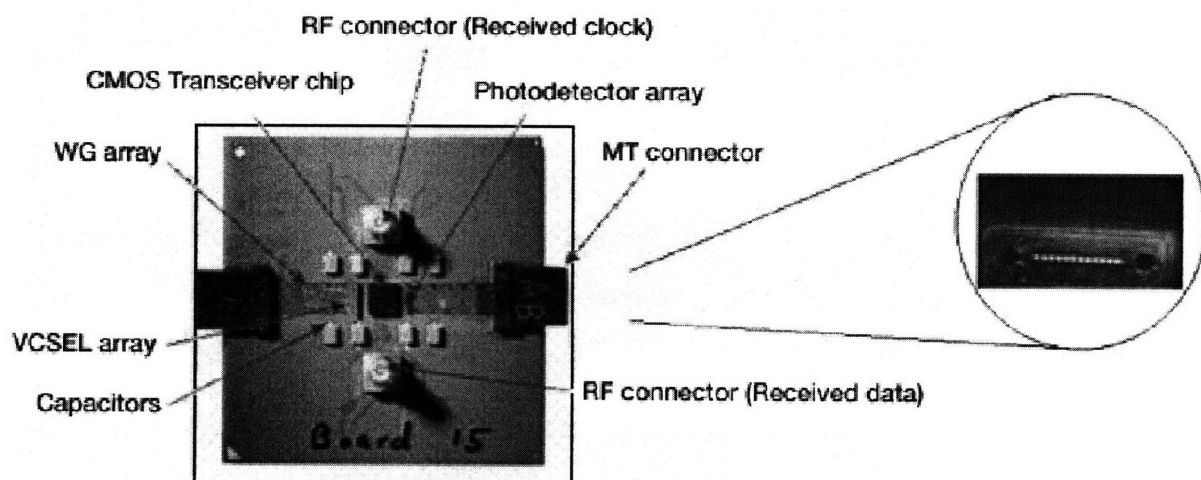


Figure 1-11: Intel chip-to-chip optical interconnect prototype [95].

On-chip Interconnects

On-chip interconnection is even more ambitious than the chip-to-chip integration effort; whereby, the ultimate goal is to replace the metal wiring, that has been the defacto industry standard since the birth of the microelectronics industry, with light carrying optical waveguides.

One of the significant accomplishments of the microelectronics industry has been the tremendous scaling of device dimensions that has been achieved. With this device geometry scaling, the number of devices that can be integrated on a single chip has increased considerably and the costs per component on an integrated circuit have gone down appreciably as is shown in Figure 1-12.⁶

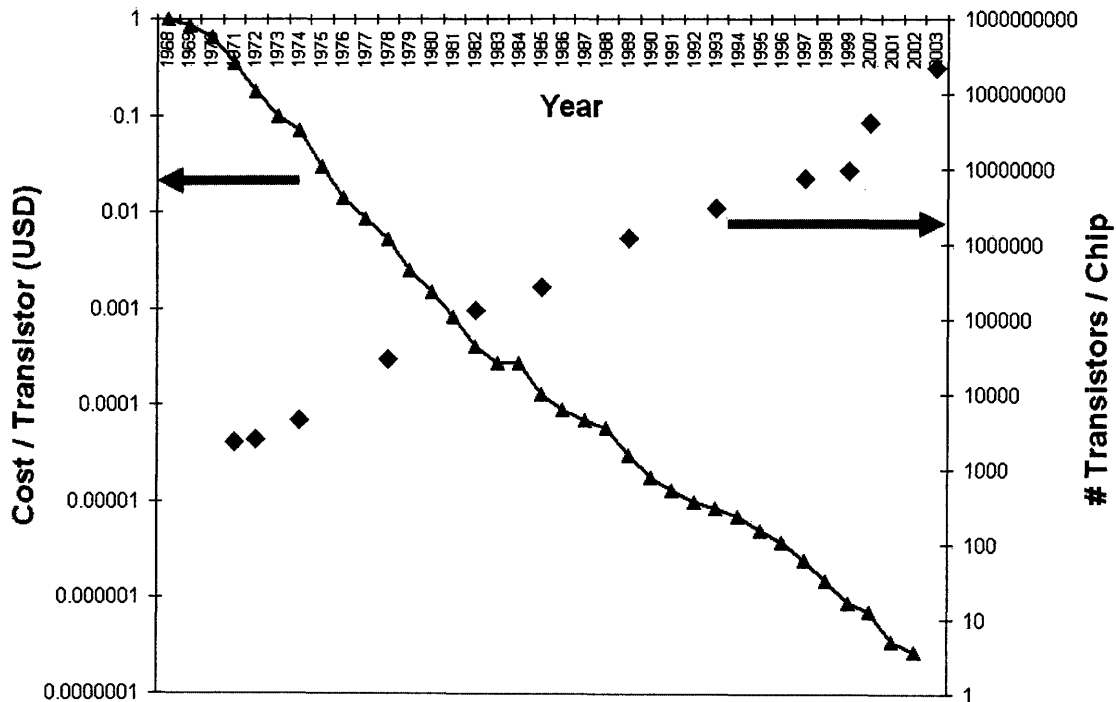


Figure 1-12: Number of transistors integrated on a single chip and the related cost per transistor[31].

⁶The prediction of the rate at which the number of transistors per microchip would increase and the associated cost savings due to this scaling was proposed by Intel founder, Dr. Gordon Moore, in 1965, and is referred to as Moore's law [70].

This tremendous shrinking of device dimensions coupled with the steady increase in signal clock frequencies has made the parasitics associated with transmitting signals on the metal interconnect lines more problematic.⁷ Specifically, as the transistor dimensions have been scaled to smaller and smaller dimensions, so too have the electrical pipes carrying the information from device to device. As the cross-sectional area of the individual pipes is made smaller, the transmission capacity decreases due to resistive losses. Similarly, as the signal frequency increases, parasitics such as the skin effect degrade the signal. In addition, as interconnects are scaled to smaller dimensions, so too are the dielectrics separating the metal interconnects. With this narrower spacing between metal lines, the parasitic capacitance between adjacent lines increases, resulting in what is called cross-talk noise. A further complication of scaling the interconnect cross-sectional area smaller is the phenomena of electromigration⁸ [52].

In the microelectronics industry, there have been several approaches to combat the aforementioned parasitic effects. First, instead of scaling the interconnect so aggressively, more metal interconnect levels are often utilized. While this has proven to be a useful approach, ultimately, it is likely that the addition of more and more metal interconnect layers will negatively impact the yield due to technical challenges related to planarization and photolithographic patterning. Second, electrical signal repeaters are sometimes inserted intermittently along a long interconnect line to reduce signal degradation. Unfortunately, these repeaters do not come without a cost as they consume power, and take up chip real estate. Third, to reduce the parasitic capacitances of the interconnect lines, low dielectric constant materials are being used as the insulation material between metal interconnects. Fourth, the industry has largely made the switch from aluminum to copper metal interconnects in order to reduce interconnect resistivity and electromigration issues. All of these improvements have enabled electrical interconnects to remain the technology of choice for ultra-short distance

⁷It should be noted that clock speeds have recently hovered in the range of 3 to 4 GHz due to the issue of power dissipation.

⁸Electromigration is the phenomena seen with electrical conductors in which high current densities cause electrons to impact atoms of the conductor so strongly that a void in the metal forms.

on-chip interconnects for the foreseeable future.

Optical interconnects are also not without problems and many of these issues become glaring when they are considered for short distance applications. The capability of manufacturing extremely low loss planar dielectric waveguides already exists; however, moving to ultra-short interconnect lengths, the quality of the optical link begins to be overwhelmed by the quality of the laser, modulator, and photodetector as well as the coupling between these devices and the dielectric waveguides. Techniques that efficiently integrate these optical devices with CMOS compatible electronics are still being researched and developed.

Researchers at Intel have investigated when it may be advantageous to move from electrical interconnects to optical interconnects. They concluded that on-chip optical interconnects do not appear to be worth the trouble in the near term (i.e., for technology nodes down to 22 nm L_{min}) for either clock or signal distribution applications[69].

Ultimately, the feasibility of implementing on-chip optical interconnects will be a great deal clearer after robust processes for manufacturing highly integrable optical active devices are developed. The goal of this thesis is to invent a new approach for manufacturing highly integrable active optical devices, such as lasers and amplifiers, that will get us closer to achieving optoelectronic integration for applications such as on-chip interconnection on silicon.

1.4 Overview of Thesis

This thesis describes the development of a novel process for creating highly integrable active optical devices and their integration on silicon. Structurally, this thesis consists of seven chapters with three appendices of supplemental details. Chapter 2 provides an overview of the different optoelectronic integration approaches that have been used both in academia and in industry. Chapter 3 introduces the goal of this thesis, a process technology for highly integrable active optical devices. Moreover, the requirements for the process technology are described and alternative approaches

are presented. Chapter 4 details the process technology developed to create highly integrable edge-emitting semiconductor lasers. The results, including the characterization of the process technology and the device are presented in Chapter 5. Chapter 6 presents a novel technique, known as magnetically assisted statistical assembly, to integrate these optoelectronic devices using a high-volume batch process. Chapter 7 concludes the thesis and proposes future work. Appendices A and B contain the process flows developed for the conventionally cleaved edge-emitting lasers and the highly-integrable edge-emitting laser platelets, respectively. Appendix C contains details on the specific metal deposition, photolithography, etching, and various other process steps. Appendix D contains detailed expressions for the magnetic scalar potential and associated constants for the magnetically assisted statistical assembly theory.

1.5 Lab Facilities

Most of the fabrication described in this thesis was carried out in the Exploratory Materials Laboratory (EML), which is part of the Microsystems Technology Laboratories (MTL). The semiconductor dry etching was performed at MIT Lincoln Laboratory with the assistance of Jason Plant. Many of the wet chemical etching steps, as well as the electrical characterization was carried out in Professor Fonstad's group laboratories. The vibrating sample magnetometer characterization of the magnetic samples was carried out in the laboratory of Dr. R.C. O'Handley. The profilometer, scanning electron microscope, and micro-cleaving precision characterization work was carried out in the Shared Experimental Facilities (SEF), which is part of the Center for Materials Science and Engineering (CMSE).

Chapter 2

Approaches aimed at Optoelectronic Integration

2.1 Key Deliverables of an Integration Strategy

The ultimate goal of the optoelectronic integration research effort is to provide a solution for combining both active optical devices that emit, detect, and modulate light, passive optical devices that direct and transport light, and electronic devices that perform information processing and optical device controlling operations.¹

There are several questions one may ask when evaluating optoelectronic integration techniques. First, does the specific technique enable products or applications that would otherwise be impossible to produce? Second, for products or applications where other technologies (i.e., purely electrical solutions) exist, does the integrated optoelectronic solution offer a significant performance advantage? Third, does the optoelectronic solution allow for a sizable cost savings over competing technologies? Fourth, does the optoelectronic integration process allow for flexibility in terms of the heterogeneity of devices that can be combined? Fifth, does the throughput of the integration technique scale to VLSI-size integrations?

¹There is sometimes a distinction made in the literature between devices (i.e., photonic integrated circuits) that integrate strictly optical functionality, and devices (i.e., optoelectronic devices) that integrate both optical and electrical functionality. Note that in this chapter, the use of the term optoelectronic is used to refer to either of these two integrated devices.

In terms of the commercial adoption of optoelectronic integration methods, techniques used include the hybrid technique of flip-chip bonding as well as full monolithic integration. Unfortunately, there are limitations associated with both of these techniques which have restrained their widespread adoption and have motivated a significant research effort in optoelectronic integration today. These research efforts range from strategies aimed at full-monolithic integration to hybrid integration strategies such as wafer bonding, fluidic assembly and flip-chip bonding. These techniques and their advantages and disadvantages will be discussed in this chapter.

2.2 Monolithic Integration Strategies

The holy grail of the optoelectronics field is a material system from which one could fabricate a dense arrangement of seamlessly interconnected high quality electrically pumped active and passive optical devices, of varying size and shape, along with associated electronics on a single substrate. Some monolithically integrated optoelectronic products have in fact been brought to market. For example, commercial devices such as telecom edge-emitting lasers with integrated electro-absorption modulators have been commonly fabricated for several years using monolithic techniques. Infinera has taken this level of integration further by developing a monolithic photonic integrated circuit technology (PIC) that has combined sixty optical components, including ten different wavelength lasers on an Indium Phosphide (InP) substrate[86]. Aside from this effort of Infinera, the flexibility and scale of monolithic integration techniques in industry has been limited. As a result, most commercial monolithic products integrate only a small number of different devices. In addition to InP, semiconductors such as silicon and gallium arsenide have been used for monolithic optoelectronic integration development. A brief overview of the integration work using these three material systems will now be presented.

2.2.1 Monolithic Optoelectronic Integration in Silicon

Silicon is the material of choice for high density electronic circuits because of its ability to implement low static power complementary metal oxide semiconductor (CMOS) technology. Silicon has been the dominant semiconductor material in the electronics industry for over forty years.² Because of this success and the gained maturity of the silicon material system in microelectronics, much investigation has occurred with the silicon system in the field of optoelectronics. A silicon containing compound, silicon dioxide (SiO_2) is the most commonly used material to make optical fibers. Not surprisingly, high quality, low loss planar waveguides composed of silicon dioxide, silicon oxynitride, silicon nitride, and silicon are the dominant optical planar waveguide technology in the market today. Furthermore, high density optical multiplexers (i.e., Arrayed Waveguide Gratings (AWG)) are also most often fabricated on a silicon wafer.

However, the development of active optical devices in the silicon material system has proved most challenging. The problem centers on the fact that silicon is an inefficient light emitting material due to its indirect energy bandgap. The implementation of monolithic optoelectronic devices in silicon has been stifled by this poor material property. Nonetheless, a significant research effort has been focused on trying to find ways to overcome these material problems. Specifically, researchers investigating porous silicon have achieved visible wavelength light emission through optical pumping with an emission efficiency of up to approximately 23%[13]. Electrically pumped devices have been realized as well, but offer extremely poor emission efficiencies of approximately 1%[54]. Similarly, researchers have demonstrated optical amplifiers fabricated on silicon wafers. These waveguide amplifiers typically consist of rare earth ion (i.e., Erbium ions) doped dielectric waveguides deposited on silicon. While a gain medium is achieved in this Erbium Doped Waveguide Amplifier

²Low static power consumption electronics are vital for applications such as SRAM memory where most transistors remain in a certain state for an extended period of time. Silicon CMOS technology is used in memory applications due to the fact that it operates with no static power dissipation. Thus, if a CMOS circuit is not being switched from on to off or vice versa, a CMOS circuit will not dissipate power. By keeping the static power to a minimum, it is possible to prevent the circuit from overheating.

(EDWA) structure, these devices require another laser, such as a 980 nm or 1480 nm, laser to induce optical amplification of the incoming 1550 nm signal [93, 92].

Recently, the world's first continuous-wave optically pumped silicon laser has been achieved by a team at Intel Corp[34]. The laser structure is a standard silicon-on-insulator rib waveguide with multi-layer dielectric mirrors on the waveguide facets.³ Utilizing the Raman effect to achieve lasing, the device is pumped with a several hundred milliwatt 1550 nm laser to achieve continuous-wave lasing at a wavelength of around 1690 nm. Another notable result in silicon laser research has been the demonstration of optical gain in silicon nanocrystals by Pavesi et al.[55] In addition, Kimerling et al. have measured optical gain from strained germanium grown on silicon substrates[45]. Although these demonstrations represent tremendous breakthroughs, it is apparent that to make silicon the material of choice for monolithic optoelectronic integration, the development of an efficient electrically pumped light emitting device is required. To date, this has yet to be accomplished.

2.2.2 Monolithic Optoelectronic Integration in Gallium Arsenide and Indium Phosphide

Given the difficulty with manufacturing efficient silicon optical emitters, a significant research effort has pursued monolithic optoelectronic integration using the Indium Phosphide and Gallium Arsenide semiconductor systems. This is not unwarranted as III-V semiconductors, such as GaAs and InP, are the industry standard for radio frequency (RF) communication electronics (Figure 2-1) and are the most commonly used semiconductor materials in the production of lasers. Taking advantage of these semiconductors orders of magnitude electron mobility advantage over silicon, commercial RF designs utilizing high electron mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs) are common. Moreover, high quality detectors, waveguides, and modulators can all be fabricated from these semiconductor systems.

³The waveguide forms the intrinsic (i) region of a reversed biased p-i-n diode that was implemented to reduce a free-carrier absorption problem that had earlier prevented continuous-wave operation.

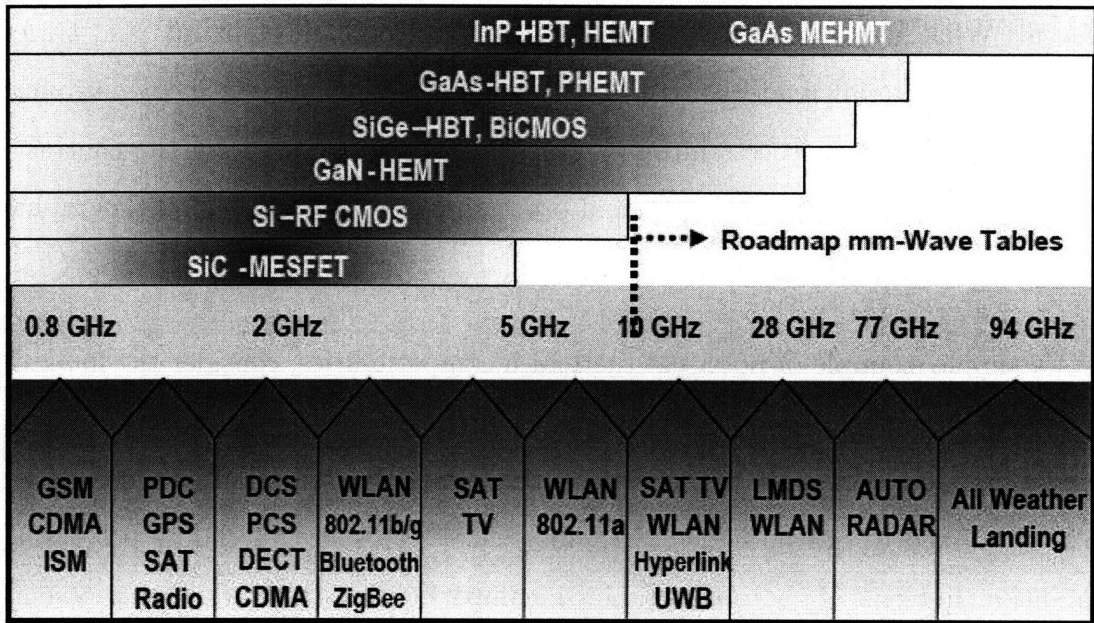


Figure 2-1: 2006 International technology roadmap for semiconductors, radio frequency and analog/mixed-signal technologies for wireless communications working group[6].

The primary area where compound semiconductors performance is inferior to silicon is large scale memory intensive electronics. Compound semiconductors are not optimal for this application because of issues such as electron and hole carrier mobility mismatch and gate dielectric leakage which make implementation of a CMOS style technology difficult. It is possible to create complementary III-V circuits; however, the technology is not as well developed as it is for silicon. Moreover, the smaller III-V substrate sizes put III-V semiconductors at a huge disadvantage compared to silicon.

However, there are many products on the market today that make use of monolithic integrations in these compound semiconductor material systems. For example, in the field of telecommunications, 1550 nm edge-emitting lasers and associated electro-absorption modulators are typically manufactured monolithically in the InP system. In addition, full monolithic integration of strictly passive devices is not uncommon in these material systems.

While monolithic integration in these semiconductor materials is in industry production, there are limitations on the scale and complexity that can ultimately be

achieved. What has limited the monolithic optoelectronic effort in InP and GaAs has not been material inadequacy, but instead fabrication process incompatibility and costs. In terms of process incompatibility, issues can result from the contrasting dry and wet etch chemistries, thermal processing budgets, and photolithographic specifications required for the different devices.

As a simple example of potential thermal incompatibilities, consider the integration of any device with metal connections. Once this device is fully processed, if there is a desire to integrate other devices, the subsequent processing temperatures would be allowed to rise no higher than 450 °C[58]. This severely limits processing capabilities. In terms of photolithographic incompatibilities, there are often problems due to the discrepancies in thickness between different optical devices and electrical devices. Typically, optical devices are much thicker than electronic devices (orders of magnitude thickness differences). If these topographic features persist and the surface of the semiconductor cannot be kept planar, photolithographic patterning of the devices can be very problematic.

In terms of cost, compound semiconductor substrates are over an order of magnitude more expensive than silicon. Figure 2-2 shows the volume leading substrate sizes of the three semiconductor systems. Epi-ready silicon wafers having an 8 inch diameter typically cost slightly less than \$50 a wafer; whereas, the 4 inch InP and 6 inch GaAs are roughly an order of magnitude more expensive than the larger silicon wafer.⁴ A much more significant cost in manufacturing is the value-added or additional processing that is undertaken. This is also a negative aspect for III-V devices because more processing needs to be performed to create the same number of devices as can be made from silicon wafers. This follows from the significant substrate size advantage silicon offers over III-V semiconductors.

⁴Presently, the largest substrate sizes commercially available in InP and GaAs (i.e., 6 inch diameter) are half the diameter of the largest available silicon wafer (i.e., 12 inch diameter)

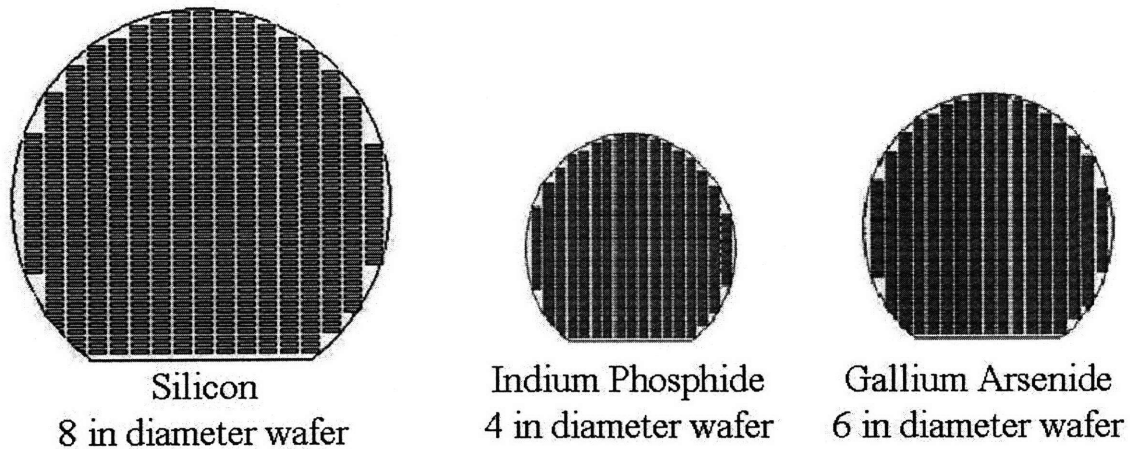


Figure 2-2: Typical substrate sizes used in industry for silicon, indium phosphide and gallium arsenide.

2.3 Hybrid Integration Strategies

Because of these problems with pure monolithic optoelectronic integration, the commercial manufacture of optoelectronic devices typically involves a hybrid technique where heterogeneous devices are optimally processed separately prior to integration. Then integration consists of either wire bonding or flip-chip bonding the devices to a target substrate or package (Figure 2-3).

Flip-chip is an acceptable solution at the moment since integration has primarily involved only small numbers of light sources, waveguide devices, and photodetectors. To implement large-scale optoelectronic integration for high bandwidth systems, then a technique offering less assembly time with less parasitics must be developed. Furthermore, it would be ideal to have a technology where further processing could be undertaken after the devices have been integrated.

Research of hybrid integration of compound semiconductors with silicon has been investigated for over two decades. For large-scale optoelectronic integration, the two techniques that have garnered considerable attention during this time period are direct epitaxy and wafer bonding. These methods attempt to integrate entire wafers of devices at once, and thus offer an improvement in scale over wire bonding and

flip-chip bonding. Most recently, techniques involving fluidic assembly have gained popularity in the research community.

2.3.1 Flip-chip Bonding

Flip-chip, first commercialized in the 1960s, is the well-established integration technology used in the optoelectronics industry today. In practice, flip-chip bonding involves the deposition of solder bumps on a target substrate wafer and the alignment of a die to the substrate. Once aligned, pressure is applied and the temperature is increased in order to aid in the bonding. An underfill is often deposited between the die and the substrate to reduce the stress between the device and the substrate that results from the thermal expansion coefficient mismatch of the materials being integrated.

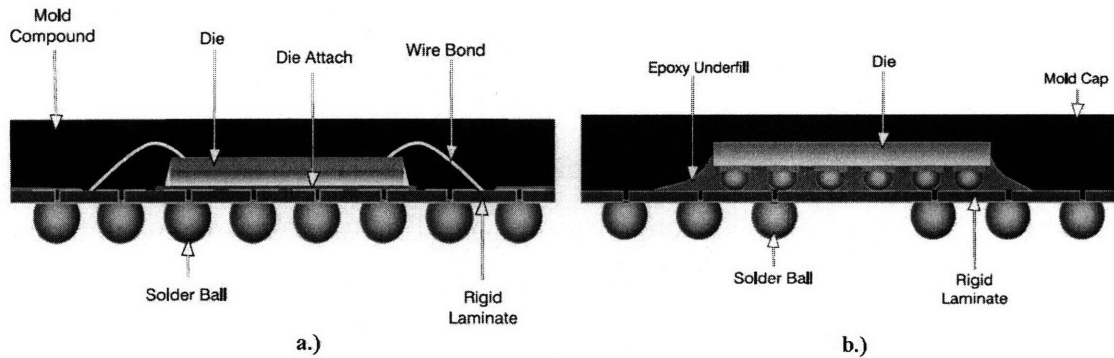


Figure 2-3: Hybrid integration techniques a.) Wire bonding b.) Flip-chip bonding[82].

Flip-chip bonding offers markedly better performance than wire bonding with regards to assembly time and parasitics. Unfortunately, issues with flip-chip bonding still remain. First, a significant issue with flip-chip bonding is the scalability of the technique in terms of the total number of devices that can be integrated. Consider the integration of a large array of small square devices on a target substrate (Figure 2-4a). Since the square devices are homogeneous, they could all be fabricated on their native substrate and a 2 cm x 2 cm piece of this substrate could be bonded to the target substrate in one flip-chip bonding step. There are two limiting factors regarding this scenario. First, the bonding precision with which the die can be aligned to the target substrate is typically limited to $\pm 10 \mu\text{m}$. Second, since the large array

of devices will be integrated (i.e., flip-chip bonded) at once, the square device yield must be perfect unless redundancy is included (which would add to the complexity).

As another instructive example, consider the integration of a number of devices, each with a different material structure, size and shape. Figure 2-4b). In this case, a flip-chip bonding step would be required for each type of device and in some instances for each device (where homogeneous devices are not situated side by side). In a situation where there are an inhomogeneous batch of thousands or more devices to be integrated, flip-chip would not be an acceptable solution.

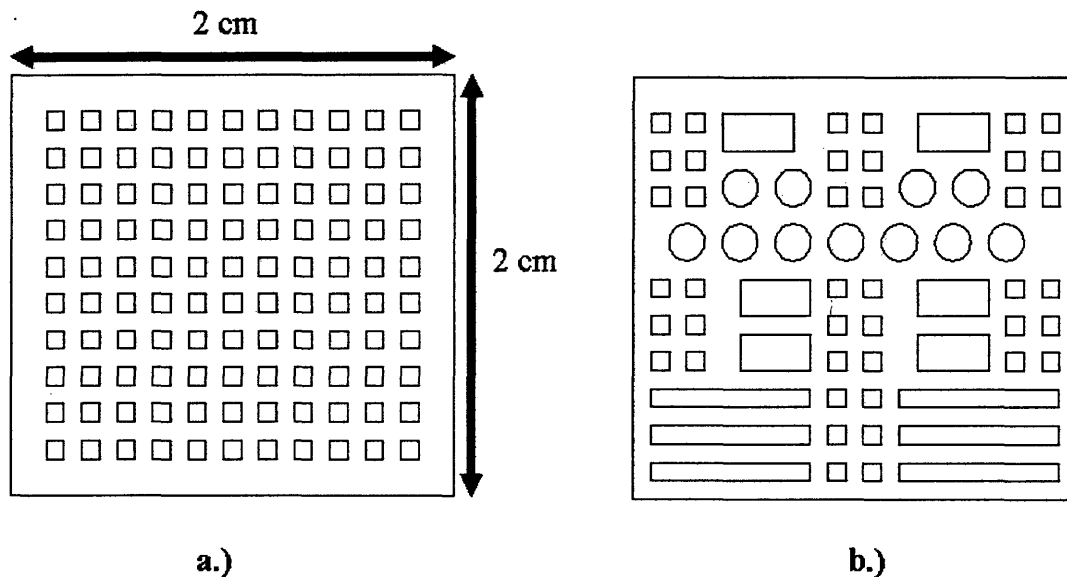


Figure 2-4: Demonstration of flip-chip bonding limits: a.) Homogeneous array of devices to be integrated. b.) Inhomogeneous array of devices to be integrated.

It should also be noted that there are upper and lower limits to the die sizes that can be reliably flip-chip bonded. Typically, acceptable die sizes vary from approximately $100 \mu\text{m} \times 100 \mu\text{m}$ up to a few cm^2 . This upper limit arises due to the requirement that as the bonded die size increases, the temperature and time required for bonding increase as well. Exposed to high temperatures for extended periods of time, the underfill between the die and substrate undergoes significant stresses. In addition, the larger size of the die, the more difficult it is to flow the underfill between the die and substrate without encountering air bubbles. For the communi-

cations industry, where reliability standards are stringent, flip-chip is an imperfect solution.

Flip-chip is an acceptable solution at the moment since integration has primarily involved only small numbers of light sources and detectors with associated electronics for low data rate systems. A commercial example of an optoelectronic product that makes use of flip-chip bonding techniques is the Fiber-to-the-home (FTTH) triplexer (Figure 2-5) manufactured by Enablence Technologies.

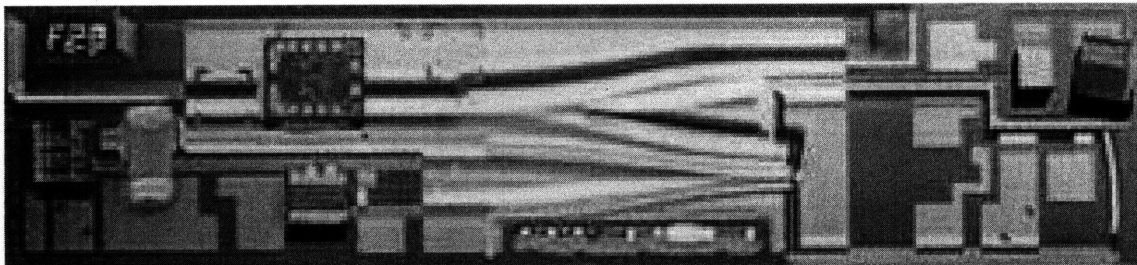


Figure 2-5: Top-down picture of a triplexer product manufactured by Enablence Technologies using flip-chip bonding techniques. A FTTH triplexer, as described in Chapter 1, has multiple photodetectors, one at 1490 nm and the other at 1550 nm, as well as a 1310 nm laser and electronics[85].

It is interesting to compare the requirements of flip-chip assembly in optoelectronic integrations versus those in system-on-a-board electronics integrations. Typically, the alignment tolerances in optoelectronic integrations are much tighter than in purely electrical integrations. Moreover, the bonding forces that can be used in flip-chip bonding optoelectronic components are less than can be used in flip-chip bonding of electrical components. This follows from the fact that many of the semiconductor substrates, like InP and GaAs, used for high speed optoelectronics are more fragile than silicon, the dominant semiconductor used in the electronics industry.

2.3.2 Direct Epitaxy

Direct epitaxy has been investigated with the goal that one day it could allow for a truly monolithic optoelectronic integration process. Using the integration of Si and GaAs as a reference, direct epitaxy is typically carried out by epitaxially growing a

thick layer of GaAs on Si. By growing a thick layer, the goal is to enable the lattice deep inside the GaAs to relax from its tensile strained state at the GaAs/Si interface that results from the 4% lattice constant mismatch. Unfortunately, if the devices are functional after processing, their lifetimes prove to be very short due to the lattice mismatch and the stress related to the mismatch of the materials' thermal expansion coefficients (CTE). Since GaAs has a CTE almost three times that of Si, the elevated temperature of the growth process often results in catastrophic stress related defects [51].

Parameters	Si	Ge	GaAs	InP
lattice constant (\AA)	5.43095	5.64613	5.6533	5.8686
CTE ($\times 10^{-6} \text{ } ^\circ\text{C}^{-1}$)	2.6	5.9	6.86	4.75

Table 2-1 Material parameters of Si, Ge, GaAs, and InP [51][80].

To alleviate the problems with the lattice mismatch, some research groups buffer the interface between Si and GaAs with intermediate lattice constant materials. One approach uses SiGe buffer layers to achieve three orders of magnitude reduction in the dislocation density from 10^9 cm^{-2} to 10^6 cm^{-2} from the direct epitaxy of GaAs on Si [66]. Typically, the process begins by growing layers of SiGe having a high Si content on a Si substrate. As more and more layers are grown, the content of the layers are given higher and higher Ge content. Finally, the GaAs layer is grown.

Still, even with the issue of the lattice constant mismatch essentially removed, further processing of the devices following growth, can cause catastrophic stresses due to the thermal expansion coefficient mismatch of the different semiconductor materials used in the implementation.

2.3.3 Wafer Bonding

Wafer bonding improves upon direct epitaxy by allowing for the optimum processing of devices prior to integration. While lattice constant mismatch is less of a problem for wafer bonding, the CTE mismatch remains a difficult obstacle to overcome[51].

The typical wafer bonding process involves the joining together of a semiconductor-to-semiconductor or a semiconductor-to-insulator interface. This differs from flip-chip bonding where a metal-to-metal contact is achieved. The wafer bonding process is performed at elevated temperatures though and the thermal changes the wafers undergo result in severe stresses due to the materials differing coefficients of thermal expansion[51]. The stress problem is magnified since the devices are all linked together and thus the stresses couple across the entire wafer.

Learning from the work in wafer bonding, Fonstad et al. developed the technique of Aligned Pillar Bonding (APB) to reduce the problems associated with the CTE mismatch[51]. The APB process involves optimally processing the devices to be integrated separately. For instance, silicon devices are optimally fabricated on a silicon wafer and GaAs-based devices are manufactured on a GaAs wafer. Then, the GaAs devices are patterned by a combination of photolithographic steps and etch steps, leaving behind arrays of device pillars with contact metals sticking up from the GaAs wafer. Similarly, dielectric recesses are formed on the silicon wafer, mirroring the protruding devices on the GaAs wafer. The two wafers are then aligned and metal-to-metal bonded. The GaAs substrate is then chemically removed, thus eliminating the link between the devices (through their native substrate). With this link removed, further elevated temperature processing can be undertaken without the extreme risks to device integrity seen with standard wafer bonding.

APB is not without its own issues, namely, that it is quite wasteful of semiconductor materials (like all other wafer bonding techniques), it requires a very challenging alignment procedure, and in many cases it does not allow for the testing of devices prior to integration.

2.3.4 Fluidic Assembly Techniques

Given the stress issues involved with wafer bonding and direct epitaxy, research is being performed involving the parallel integration of uncoupled pre-processed devices in solution. Like wafer bonding, these techniques involve the optimum processing of devices on their own device specific wafer prior to integration. In the fluidic assembly

technique's most basic form, one wafer will have large numbers of unconnected devices and the other target wafer will have interconnected components and recesses with dimensions corresponding to the devices on the device wafer. Improving on wafer bonding, the devices are etched free from their substrate, thus decoupling them from one another. The etched free devices are then drawn to and retained at the target wafer by some force mechanism. The main techniques in the literature are Fluidic Self-Assembly, Electric Field Directed Assembly, and DNA Assisted Assembly.

Fluidic Self-Assembly (FSA):

Fluidic Self-Assembly utilizes the force of gravity to direct trapezoidal shaped devices to a target wafer having correspondingly shaped recesses (Figure 2-6). Micromachining the devices and recesses into a particular shape ensures that the devices assemble with the proper orientation. Once etched free from their sacrificial substrate, the devices are flowed over the target wafer in a fluid and self-assemble in the recesses. Once properly in the recess, a device remains there by a combination of the Van der Waals force and the force of gravity[78, 94].

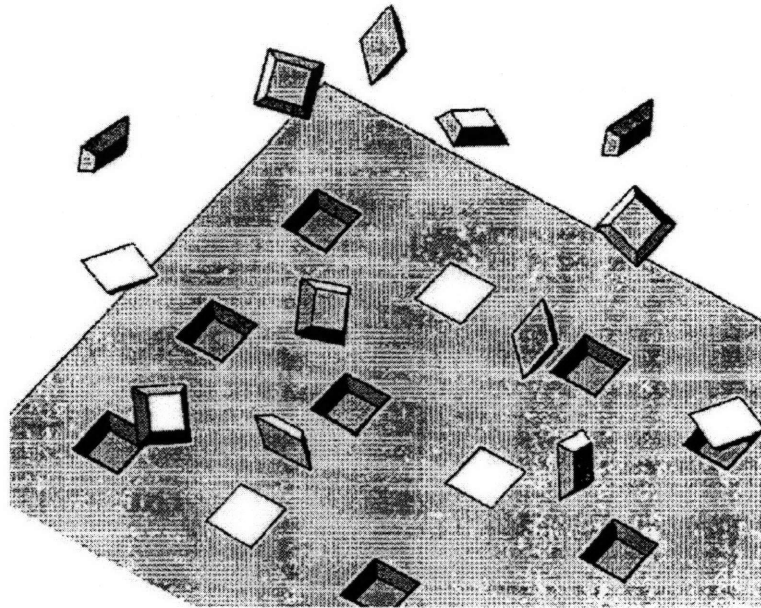


Figure 2-6: Fluidic self-assembly (FSA) schematic[94].

Fluidic Self-Assembly offers great potential in terms of scale and flexibility com-

pared to the previously mentioned integration techniques. For integrations of smaller scale though (i.e., less than ten devices), fluidic assembly is not worth the trouble. Another drawback of fluidic assembly is in cases where the orientation of the device is of significant importance. In these cases, using a fluidic assembly process requires devices to be micro-machined into complex shapes to ensure that they are assembled with the right orientation. Silicon based devices are often used in these orientation sensitive situations because of the existence of well developed anisotropic etches (like potassium hydroxide (KOH)) which can be used to pattern the devices. For complex device structures that incorporate a number of different materials, a suitable etchant that can be used is often hard to find. Another issue with Fluidic Self-Assembly is that devices are weakly retained on their target substrates after assembly and are prone to being knocked loose.

Electric-Field Directed Assembly (EFDA):

Whereas, FSA utilizes the force of gravity and the complementary geometries of the devices and recesses, Electric field directed assembly, as its name implies, uses electric fields to direct individual devices to a specific location on a target wafer (Figure 2-7). The principle by which this assembly technique operates is electrophoresis. Electrophoresis is the condition where attractive or repulsive forces act on particles due to an electric field. By making use of this concept, devices can be placed at specific locations on a target substrate. EFDA requires the fabrication of electrodes on the target wafer. When a voltage is applied to an electrode present on the host substrate, an electrophoretic force is created that moves the device toward the biased electrode [29, 18].

One drawback of EFDA is that it requires the incorporation of electrodes on the target wafer. This requirement limits the type and arrangement of devices on the target substrate upon which integration occurs. Moreover, once the devices are assembled and the bias on the electrodes is stopped, the assembled devices are not held strongly to the target substrate and thus could become misaligned or even fall off the target substrate.

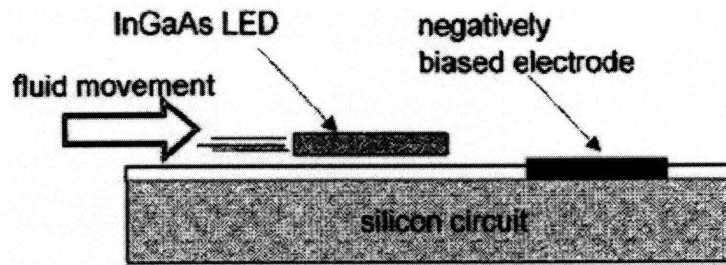


Figure 2-7: Electric field directed assembly (EFDA) schematic [29].

DNA Assisted Assembly:

As in EFDA, devices are directed toward specific locations on a target substrate by appropriately biasing electrodes on the target substrate. Retention is performed by coating the device and the specific target location with complementary DNA sequences (Figure 2-8)[27].

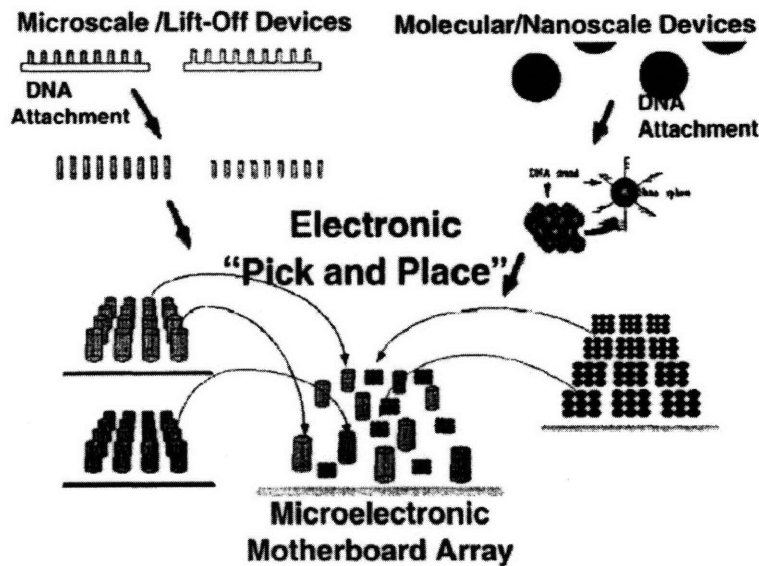


Figure 2-8: DNA assisted assembly schematic[27].

2.4 Our Approach and the Rationale Behind It

In this research and development, a hybrid integration approach is being pursued whereby each device can be manufactured on its own separate substrate, tested, and then assembled on an inexpensive target substrate (Figure 2-9). The main reason for choosing a hybrid technique is that it enables the use of optimal native substrates and ideal process chemistries, temperatures, and tools. Furthermore, the hybrid technique presented in this thesis offers the flexibility to integrate many different types of devices manufactured from many different material systems.

By allowing for the testing of devices prior to integration, our hybrid technique should enable a higher overall yield process than achievable with monolithic integration. By taking into account both performance and costs when choosing a substrate material, the total costs should be much reduced from those encountered when implementing a monolithic integration strategy in InP or GaAs. Since the expensive substrate is used to form large numbers of devices without having to worry about interconnection, the expensive compound semiconductor substrates can be jam packed with devices, enabling the cost effective use of material.

Assembly can be performed using a micro-scale pick and place technique when the number of devices to be integrated is small or a fluidic approach similar to those described earlier when the number of devices to be integrated is large.

The complexities in our process will be with regard to the individual processes required to manufacture the highly integrable devices. These must be considered on a device by device basis.

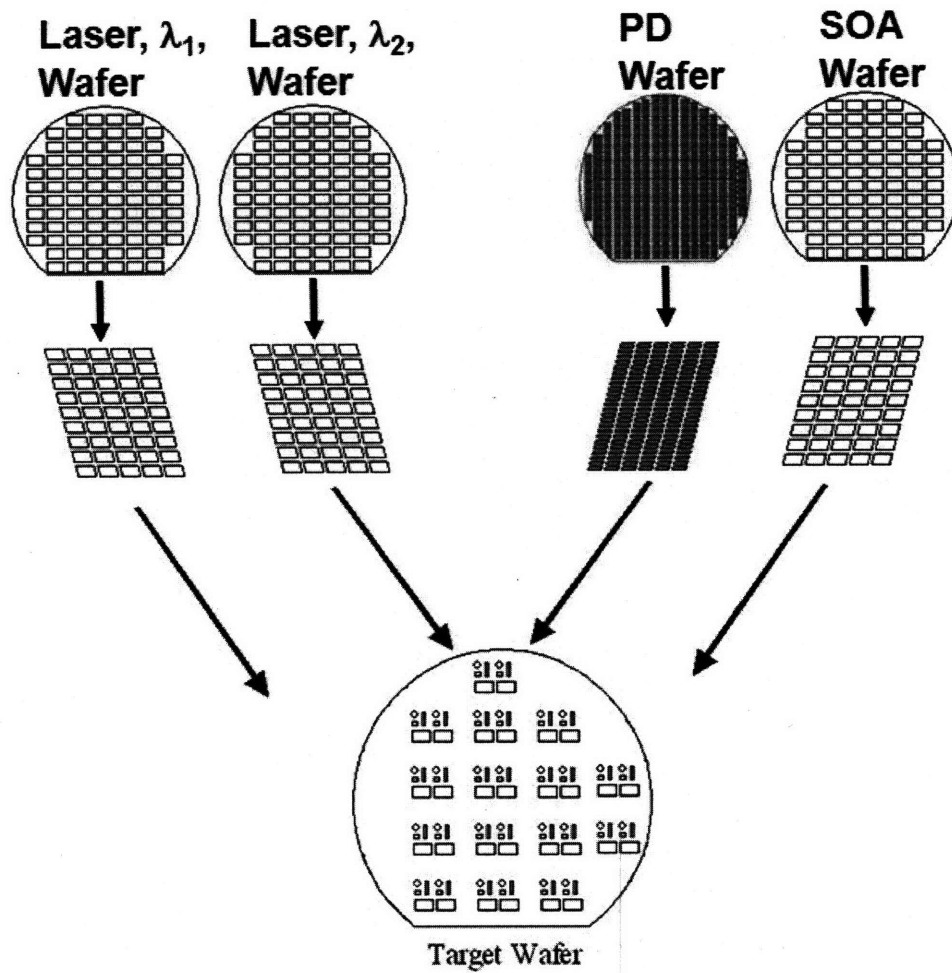


Figure 2-9: Schematic of our hybrid integration strategy whereby devices are optimally processed on their own substrates, tested, and removed from these substrates and assembled on a target substrate.

Chapter 3

Edge-Emitting Lasers for Integration with Low Loss Dielectric Waveguides

In the previous chapter, the many problems associated with a monolithic optoelectronic integration strategy were outlined, thus motivating the use of a hybrid integration approach. The focus of this thesis is to devise a strategy for creating in-plane active optical devices, such as edge-emitting lasers or semiconductor optical amplifiers, that can be integrated with passive optical components on a single substrate. Specifically, this thesis focusses on the fabrication of edge-emitting lasers that can be integrated with silicon based dielectric waveguides. To begin the discussion on this topic, the building blocks of an integrated optoelectronic system; namely, the integration platform upon which devices are integrated, the passive dielectric waveguides which interconnect active optical devices, and the focus of this thesis: the highly integrable edge-emitting lasers will be discussed.

3.1 Silicon, a Platform for Hybrid Optoelectronic Integration

A significant decision faced when developing an integration framework is what to use as the carrier substrate. Several substrate materials, such as silicon, gallium arsenide, indium phosphide, sapphire, and germanium, have been suggested or used as platforms for integrated optoelectronic systems. A number of concerns go into deciding which of these substrate materials will make the best integration platform for our purposes here. First, at a minimum, the platform must be amenable to fabricating high quality, low loss waveguides which could ultimately interconnect our active optical devices. Typical materials used to form low-loss waveguides, their typical propagation losses at 1550 nm, and the substrates on which they are easily fabricated are shown in Table 3-1.

Waveguide Material	SiO ₂	Si	SiO _x N _y	Polymers	GaAs	InP
Propagation Loss (dB/cm)	0.1	0.1	0.1	0.1	0.5	0.2
Substrate	Silicon	Silicon	Silicon	Any	GaAs	InP

Table 3-1 Typical propagation losses at 1550 nm for dielectric waveguides made of SiO₂, Si, SiO_xN_y, GaAs, and InP. [30]

As shown in Table 3-1, waveguides made from these different materials have very similar propagation losses. Thus, it should be no surprise that these materials are all used to some degree in optical interconnecting applications in the photonics industry today.

Since the devices being integrated (i.e., lasers or semiconductor optical amplifiers (SOAs)) can generate a lot of heat during operation, the integration platform should be a material which can effectively conduct heat away from the device. Thermal conductivity is the property which quantifies how well a material can disperse heat and is used here as an evaluation metric.

Before evaluating which substrate would be best at dispersing heat, let us first discuss why the active optical devices generate this heat in the first place and how

this heating negatively impacts device performance. There are a number of causes of this device heating. For example, active optical devices require a significant amount of current to operate (i.e., current densities in the hundreds of Amperes per cm^2 are typical). With this significant amount of current passing through even just a small amount of series resistance, a great deal of power can be dissipated, which can result in significant Joule heating of the devices. In addition, there is significant device heating due to non-radiative electron-hole recombination that can take place in the laser active region. Photon absorption in the semiconductor results in even further heating of the devices. If the materials surrounding the laser are poor thermal conductors, then this heat cannot be readily removed and the device temperature rises.

Heating has many deleterious effects on the performance of semiconductor lasers. Specifically, the laser threshold current, I_{th} , increases exponentially with increasing temperature. This temperature dependence is often modelled by the relation

$$I_{th} = I_{th0} e^{T/T_0} \quad (3.1)$$

where T_0 is a parameter referred to as the characteristic temperature [22]. Essentially, the lower the characteristic temperature of a device, the much more sensitive the device is to temperature excursions. The laser slope efficiency, η_d , which is related to the output laser power (mW) per unit of input current (mA)¹, decreases as the temperature is increased. For most InGaAsP quantum well lasers, characteristic temperatures are typically around 50 to 70 K, whereas for quantum well GaAs/AlGaAs lasers, T_0 values usually fall in the 150 to 180 K range[22].

The characteristic temperature, T_1 , used to evaluate how sensitive η_d is to temperature. In equation form,

$$\eta_d = \eta_{d,0} e^{-T/T_1} \quad (3.2)$$

The threshold current increases and the slope efficiency degradation as a function of increasing temperature is the result of several phenomena including increased car-

¹This parameter is calculated from this optical output power-current relationship when the device is biased above threshold.

rier leakage over heterojunction barriers and increased non-radiative recombination (i.e, defect recombination, interface recombination, and Auger recombination).

An additional negative effect that temperature has on a semiconductor laser is that the emitted lasing wavelength shifts to longer wavelengths as the temperature increases. The shifting of the emission wavelength can be qualitatively explained by semiconductor energy bandgap narrowing that occurs as the temperature is increased. The bandgap energy's dependence on temperature is often modeled by the Varshni equation

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T} \quad (3.3)$$

where $E_g(0)$ is the bandgap energy at $T = 0$ K, α is an empirical constant, and β is a constant associated with the Debye temperature [80]. Typical values for α , β , and $E_g(0)$ for a few semiconductors are given in Table 3-2.

Waveguide Material	Si	GaAs	InP
α (10^{-4} eV/K)	7.021	8.871	4.906
β (K)	1108	572	327
$E_g(0)$ (eV)	1.15	1.52	1.42

Table 3-2 Typical α , β , and $E_g(0)$ values for Si, GaAs, and InP. [38]

Ultimately, if there is not an efficient way to remove heat, the device will cease to operate. Specifically, as the temperature rises, the carriers will be given thermal energy which will result in smearing out of the Fermi-Dirac distribution. This causes a reduction in the gain. As the temperature rises more and more, the distribution smears out more and at a certain point the losses exceed the gain and the device ceases to lase.

Another thermal-related failure mechanism is the result of laser facet heating. Specifically, the mirrors at the end of an in-plane laser are not perfectly reflecting, and therefore, some light absorption occurs through the surface states at these mirror locations. This absorbed light results in heating (i.e, through phonon electron

interactions) of the regions near the mirrors and the semiconductor energy bandgap narrows in these mirror regions. Over time, this phenomena can result in thermal runaway; whereby, a positive feedback process occurs that catastrophically damages (i.e., melts) the mirror facets ².

Therefore, keeping the active device at a cool temperature is essential for maintaining device functionality. Cooling is an even more important issue when working with long-wavelength (i.e, 1300, 1550 nm) based lasers since these lasers typically have very low characteristic temperatures, as is shown in Table 3-2. ³

Emission Wavelength (nm)	T_0
900	120-200 K
1300	60-100 K
1550	40-70 K

Table 3-2 Typical characteristic temperature ranges of semiconductor lasers [44]

With an understanding of the potential sources of heat and the degrading effects that this heat can have on the active optical devices, let us now evaluate potential optoelectronic (OE) integration platform materials in terms of their effectiveness at dispersing heat. Table 3-3 shows the thermal conductivities of several substrate materials used in the optoelectronics industry. ⁴

Parameter	Si	Ge	Sapphire	GaAs	InP	SiO_2
thermal conductivity (W/(cm°C))	1.3	0.58	0.42	0.55	0.68	0.014

Table 3-3 Thermal conductivity of Si, Ge, Sapphire, GaAs, and InP. [41]

As shown in Table 3-3, silicon soundly outperforms the other substrate materials in terms of thermal conductivity.

²This failure mechanism is typically seen in very high power lasers and is referred to as Catastrophic Optical Damage (COD).

³It is possible to install a thermoelectric cooler on the platform that will ensure a cool device; however, installing this device reduces the cost-effectiveness that makes integration so attractive.

⁴A higher thermal conductivity value is desired for our integration platform because it allows for more heat to be dispersed away from the lasing device.

A third metric used to evaluate a proposed OE platform material is the cost effectiveness of the material. An integration strategy offering the same performance will never be adopted unless it offers a considerable costs savings. Today many devices are individually packaged and then interconnected by fibers and bulk lenses because integration is not yet a cost effective alternative. A significant cost in the manufacture of optoelectronic devices is the substrate cost. In Section 2.2, we emphasized that silicon substrates are an order of magnitude less expensive than InP and GaAs substrates.⁵

With the strong properties of silicon with regards to the formation of low-loss waveguides, thermal conductivity, and cost, silicon is a logical choice as the platform material for our hybrid integrated system. The basic parameters of our proposed edge-emitting laser / Si-based dielectric waveguide system will now be presented.

3.2 Introduction to our Proposed Edge-Emitting Laser - Dielectric Waveguide System

Our hybrid approach to large scale optoelectronic integration involves fabricating device building blocks, such as laser diodes or optical amplifiers, using their optimal material systems and processes, and assembling these blocks in dielectric recesses on a silicon platform. Optical signals can then be routed between device blocks using low loss dielectric waveguides that can be optimally fabricated on the silicon platform. Figure 3-1 schematically shows the integration of an in-plane laser with a dielectric waveguide with the typical dimensions labeled.

Aside from the fabrication challenges in manufacturing the dielectric waveguide and the in-plane laser device, the major challenge in achieving this integration is the efficient coupling of light between the in-plane laser and the dielectric waveguide.

⁵Another aspect of cost is the expense of fabricating the devices. With over forty years of silicon fabrication development in the microelectronics industry, silicon based device processing is the most mature of the possible substrate materials and there is significant infrastructure in place in terms of foundries. Many of the fabrication techniques developed for silicon are transferable to the other substrate materials, but silicon does still have an edge in terms of processing capability.

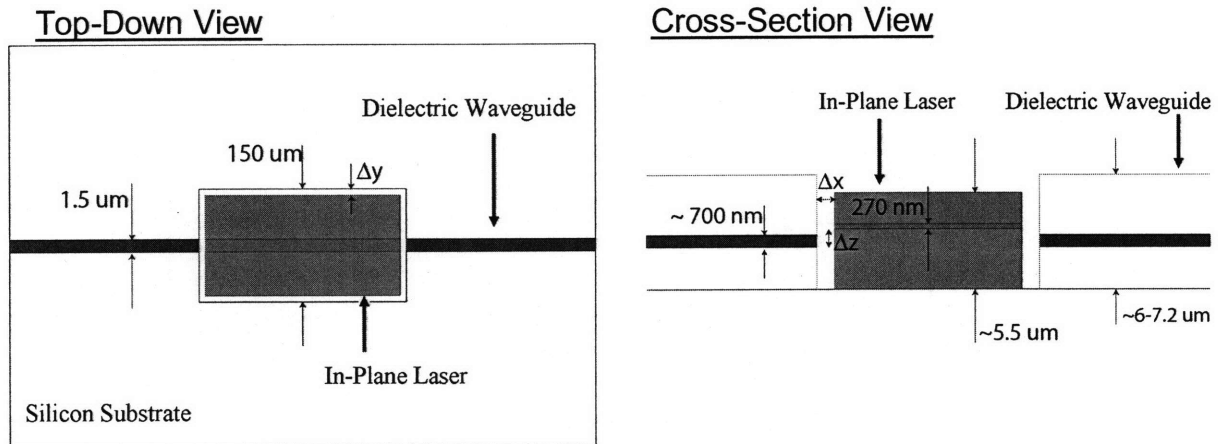


Figure 3-1: Top-down and cross-sectional schematics showing the integration of a edge-emitting laser with a dielectric waveguide on silicon.

The coupling scheme used in our approach is standard end-fire coupling. End-fire coupling involves the direct alignment of the laser and waveguide core regions in both the horizontal and vertical planes with little or no gap spacing between the laser and waveguide facets. How well the device can be aligned to the waveguide determines how lossy the coupling will be. Thus, the dimensions of the dielectric waveguide, the in-plane laser, and the dielectric recess formed on the silicon platform must all be precisely controlled. In Figure 3-1, there are three alignment tolerances which are labeled. Δx corresponds to the gap spacing between the in-plane laser and dielectric waveguide facets. Δy denotes the spacing between the non-facet plane of the in-plane laser and the dielectric recess wall. Δz represents the vertical offset between the in-plane laser and the dielectric waveguide core regions. Dr. Edward Barkley, did a thorough analysis of the coupling loss as a function of these alignment tolerances and the results are shown in Figure 3-2.

It is instructive to evaluate how difficult it is to keep the three alignment offsets to a minimum. The dielectric waveguide layers can be deposited with precise thickness using Plasma Enhanced Chemical Vapor Deposition (PECVD)⁶. The dimensions of

⁶Typical wafer-to-wafer thickness variation of state of the art deposition tools is on the order of 1% [65].

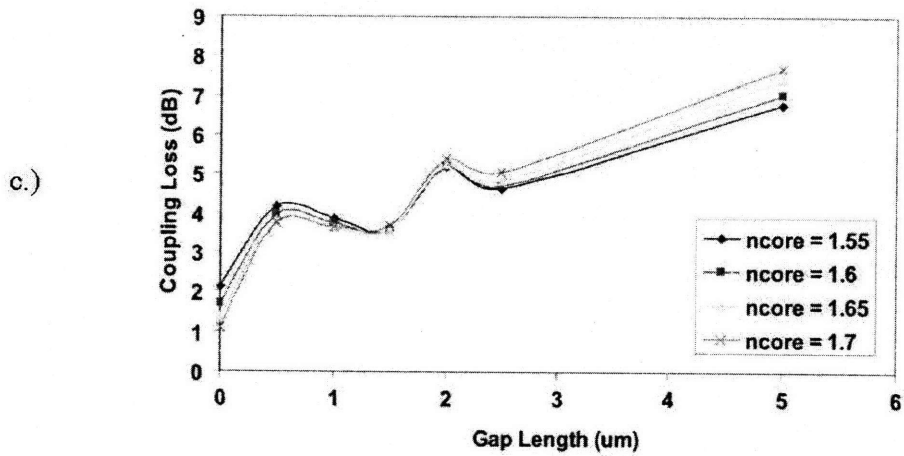
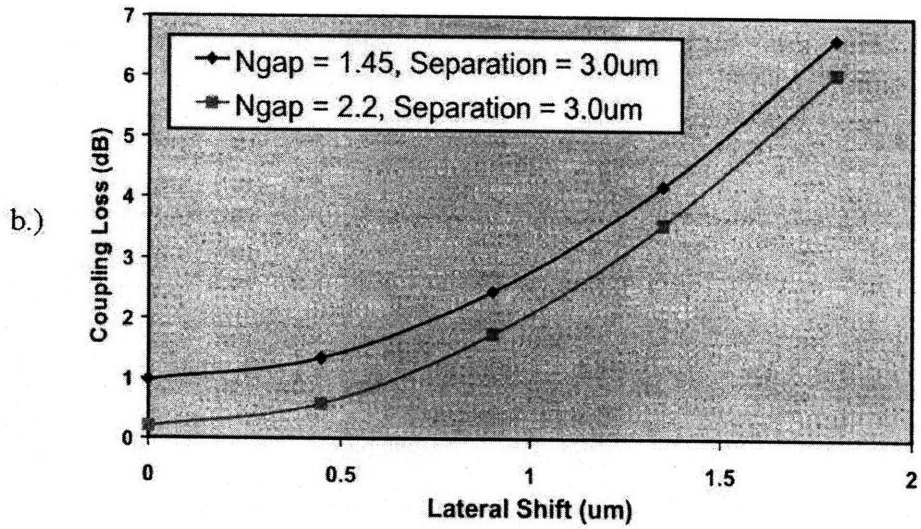
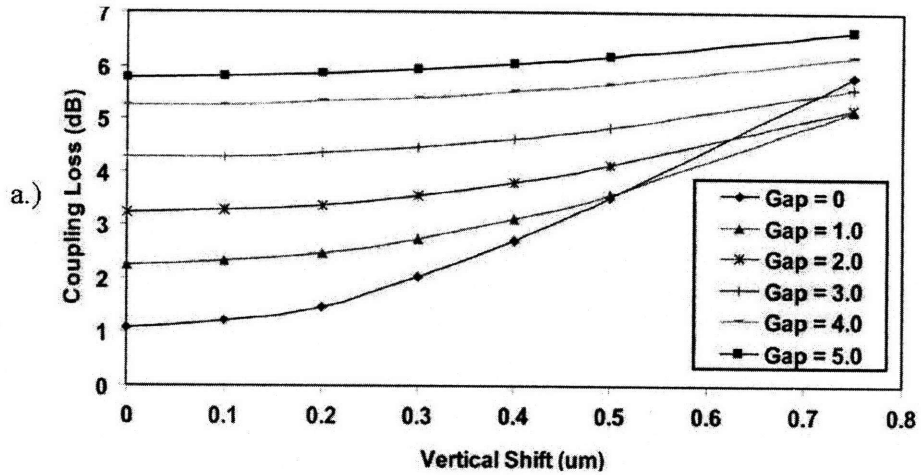


Figure 3-2: Simulation work carried out by Dr. Edward Barkley on the coupling loss as a function of a.) vertical offset, Δz , b.) lateral offset (related to Δy), and c.) gap spacing, Δx . [15]

the dielectric recesses can be controlled by state of the art photolithography⁷ and anisotropic dry etch processes.

The vertical location of the layers comprising the semiconductor laser can be accurately controlled by modern Metal Organic Chemical Vapor Deposition (MOCVD)⁸ or Molecular Beam Epitaxy (MBE) processes. The non-facet planes of the semiconductor laser can be dimensioned precisely using modern photolithography and anisotropic dry etch processes.

Thus, it has been argued that modern photolithography and standard dry etch processes can be used to keep Δy , the space between the recess wall and the non-facet side of the laser, small. The vertical offset between the devices, Δz , is kept small by proper device design and standard epitaxial laser device growths and waveguide CVD processes.

However, the complication is in accurately and consistently dimensioning the length of the laser and thus in keeping the gap, Δx , between the laser and waveguide facets small. This complication arises from the requirement that the precisely dimensioned device must also have smooth facets with sufficiently high reflectivity.

Poor reflectivity, in addition to resulting in higher threshold currents, can ultimately lead to the failure of laser diodes⁹. With the requirement that the facets be mirror smooth¹⁰, rudimentary wet and dry etching processes are ruled out as options for defining the laser length¹¹. The ideal laser facet is one that has been cleaved along the natural cleavage plane of the semiconductor crystal. Unfortunately, typical processes used to cleave semiconductors can position the location of the cleave to a precision of no better than $\pm 5 \mu\text{m}$ [64].

This lack of precision in defining the laser length coupled with the fact that the

⁷Resolutions down to smaller than $0.1 \mu\text{m}$ are achievable.

⁸typical thickness variation of state of the art deposition tools is better than 2.5% [23]

⁹Recall, the earlier description of the thermal runaway effect known as Catastrophic Optical Damage (COD).

¹⁰Laser facets are often coated with a thin film that further enhances the reflectivity of the facet.

¹¹There has been significant development over the last several years developing dry etch processes that have achieved highly reflective facets; however, these processes are not the industry standard. Furthermore, these novel processes and the requisite equipment to execute these processes were not at the disposal of the author of this thesis. The recent etched facet development will be discussed later in this chapter

dielectric recess, in which the laser will be assembled, has specific pre-defined dimensions, makes it very difficult to achieve small gap spacings between the laser and waveguide facets. Since the coupling loss increases significantly as this gap spacing increases, this integration strategy is unfeasible using industry standardized manual cleaving techniques. Therefore, the formation of highly reflective, precisely dimensioned edge-emitting laser diodes is a major obstacle in the implementation of this proposed end-fire coupled integration scheme. An approach to obtain edge-emitting lasers with precisely dimensioned lengths and smooth cleaved facets is a major focus of this thesis and will be introduced in this chapter.

3.2.1 Competing Approach in the Literature

Another approach in the pursuit of active optical device integration on silicon utilizes evanescent coupling between the III-V semiconductor laser and silicon-based waveguide. Evanescent coupling occurs by placing two waveguides in proximity with one another (Figure 3-3). By optimizing the spacing, dx , between and the offset, dy , along the lengths of the guides, it is possible to couple a signal from one waveguide to the other. To get the best evanescent coupling results, the waveguides are designed to have as similar an effective refractive index as possible.

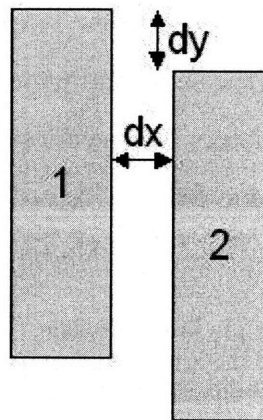


Figure 3-3: Arrangement of two evanescently coupled waveguides, labelled 1 and 2.

Using this evanescent coupling scheme, researchers at the University of California

at Santa-Barbara (UCSB) and Intel have achieved hybrid integration of a InP-based laser with an silicon-on-insulator waveguide (SOI) on a silicon substrate. To accomplish this, they utilized low temperature oxygen plasma assisted bonding of the as-grown laser substrate to a patterned SOI waveguide wafer. Once bonded, the InP laser substrate is wet etched and the laser structure is etch defined.

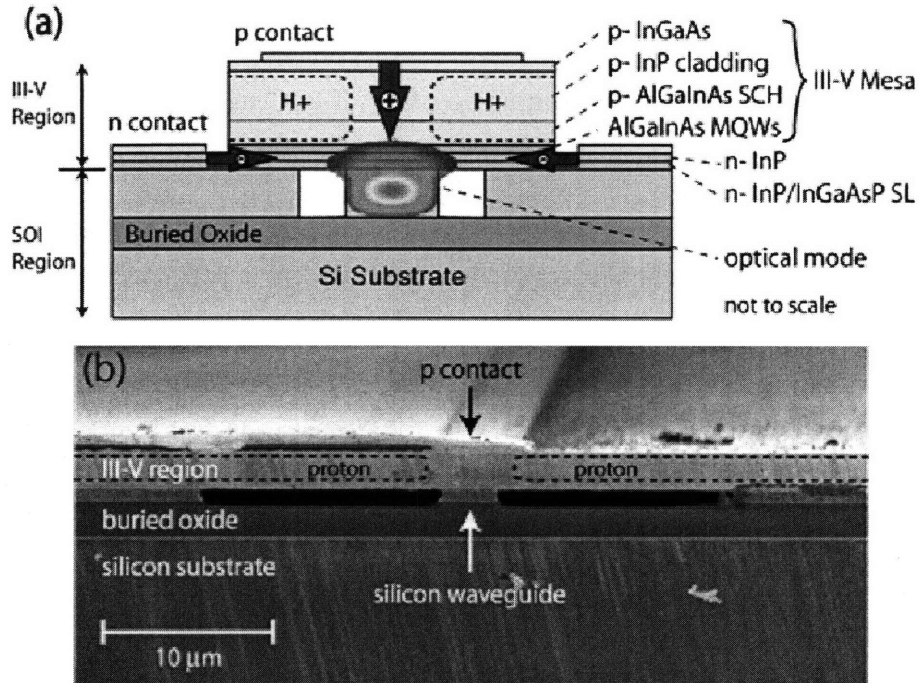


Figure 3-4: a.) Schematic and b.) SEM showing the Intel-UCSB approach of integrating an edge-emitting laser with a dielectric waveguide on silicon[33].

As seen in Figure 3-4, the laser is bonded directly above the SOI waveguide structure. With both the laser cavity and the SOI waveguide in close proximity, the evanescent field associated with the laser light output gives rise to propagating wave modes which couple to the silicon-based waveguide. One limit of the device is that the length of the laser cavity needs to be fairly long to compensate for the fact that the optical mode only partially overlaps the quantum well gain region [19]. The characteristics of this laser will be compared with the laser described in this thesis in the concluding chapter of this thesis.

Returning to the discussion of our scheme for active optical device integration

on a silicon platform, the dielectric waveguide and edge-emitting laser components of our integration strategy will now be briefly introduced. The analysis of dielectric waveguides was solely the work of Dr. Edward Barkley.

3.2.2 Dielectric Waveguides Basic Structure

Dielectric waveguides, consisting of a $0.7\ \mu\text{m}$ thick silicon oxynitride core layer, a $3\ \mu\text{m}$ thick silicon dioxide lower cladding layer, and a $3\ \mu\text{m}$ thick silicon dioxide upper cladding layer, were formed on a silicon substrate. Recesses, having sufficient depth and area to hold an integrable edge-emitting laser block, were etched through the dielectric layers. A simple schematic showing the basic structure is shown in Figure 3-5.

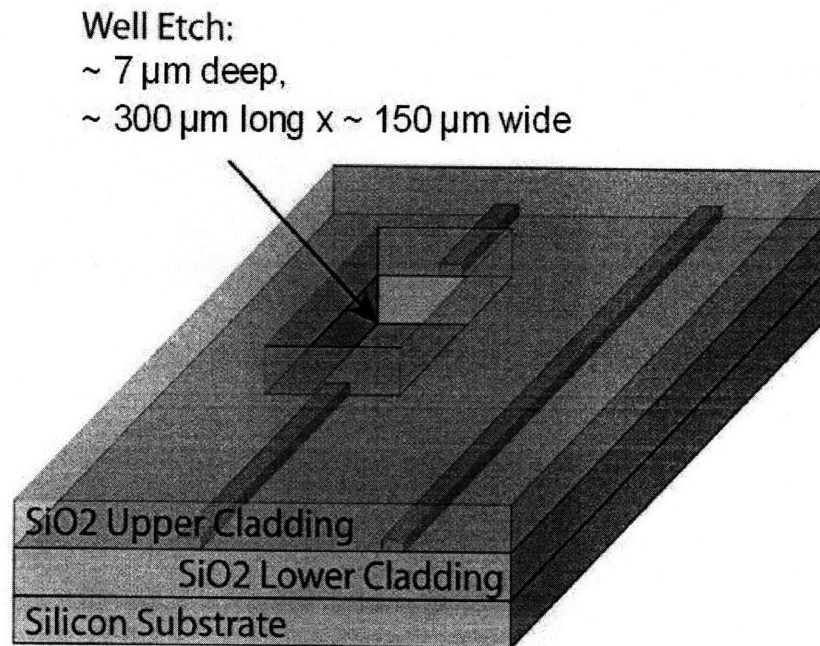


Figure 3-5: Schematic of the dielectric waveguide with SiO_xN_y core and SiO_2 cladding as well as the dielectric recess. [15]

Further details on the design and process development relating to these dielectric waveguides and recess formation on silicon can be found in the Ph.D. thesis of Edward Barkley [15].

3.2.3 Edge-Emitting Laser Basic Structure and Operation

An edge-emitting laser typically consists of a 500 or more micron long laser cavity that is bounded by two mirrors (i.e., reflective facets). In terms of the cross-sectional structure of this Fabry-Perot laser cavity, there is a thin (i.e., less than one μm) and narrow (i.e., a few μm) width active region sandwiched in between two lower refractive index cladding layers (Figure 3-6)

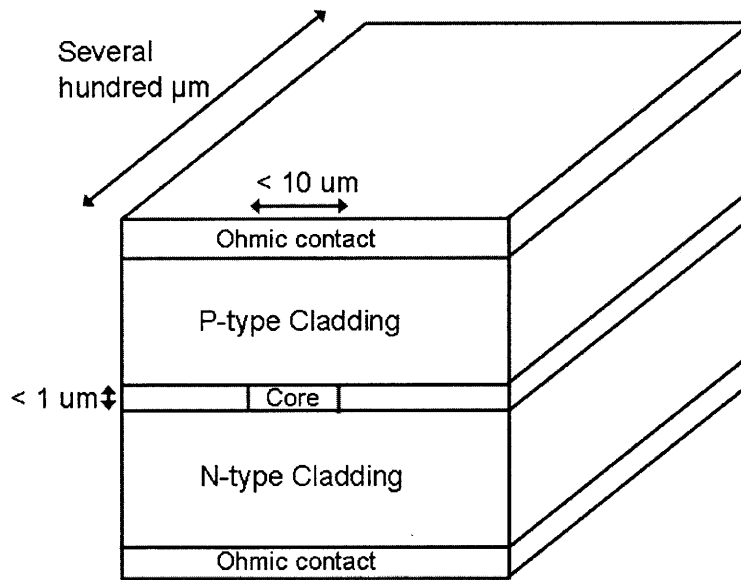


Figure 3-6: Simple schematic of an edge-emitting laser with five essential layers.

The ohmic contact layers allow electrical contact to be made to the device. The p-type and n-type cladding regions, are designed to inject a large density of electrical carriers (i.e., electrons and holes) into the active core region when the device is forward biased. The cladding layers have wider energy bandgaps and smaller refractive indices than the core region and thus help concentrate the optical wave in the active core region. The active core region is the region where electron and hole recombination occurs resulting in stimulated optical emission (i.e., lasing) ¹².

A specific type of edge-emitting laser used in this research effort is shown in Figure 3-7 and is known as a semiconductor ridge laser. In this realization, the cladding is made from doped n-type and p-type InP. The active core region consists of a multiple

¹²The active region is typically undoped to minimize losses from free-carrier absorption.

quantum well structure made from InGaAsP quaternary compounds.¹³

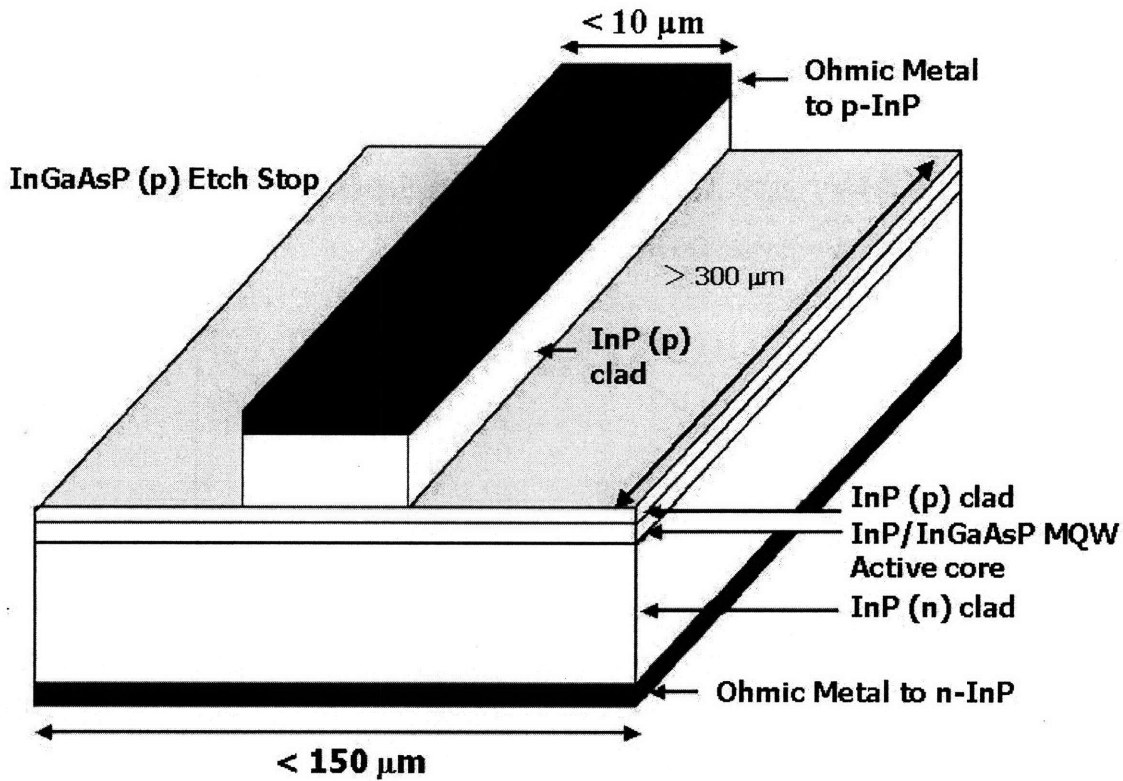


Figure 3-7: Schematic showing the basic structure of a edge-emitting laser.

The ridge laser is operated by adjusting the bias applied between the top and bottom contacts (i.e., n-type and p-type contact layers). To turn the laser on, a forward bias voltage is applied and results in the injection of carriers (i.e., electrons and holes) into the active region. Initially, when the bias is small (i.e., low tens of millivolts of forward bias), small numbers of carriers are injected resulting in weak carrier inversion. In this case, low levels of light, referred to as spontaneous emission, is output from the device. If the bias is increased, more carriers are injected and it is possible to achieve strong carrier inversion. A nontrivial amount of the generated light is not emitted from an end facet, but instead travels back and forth between the two end facets. This light has a wavelength determined by the length of the resonant cavity. In this case, the light travelling back and forth in the resonator stimulates

¹³The multiple quantum well (MQW) structure offers many benefits, most notably a lower threshold current than offered by conventional double heterostructure lasers. A detailed description of MQW laser structures and their benefits can be found in the literature [21, 22, 81].

carriers to recombine which results in light having the same wavelength and phase as the stimulating light to be emitted. This marks the onset of lasing and is visible as Fabry-Perot peaks in the output emission spectrum.

Reasonably low threshold currents are characteristic of ridge lasers due to the presence of lateral current confinement structures. Lateral current confinement is achieved by etching through the cladding region to a layer just above the active region. While this does a good job of concentrating the current above the active region, at and below the active region the current can spread laterally which can ultimately result in electron-hole recombination that does not contribute to lasing but does add to the heating of the device. Nonetheless, this approach was used in this work and results in reasonable, though not ultra-low, threshold currents.

There are a number of designs which could result in better current confinement. One approach is to ion implant the regions on both sides of the semiconductor ridge thus transforming them into either p-type or semi-insulating regions. This process can induce damage and increase non-radiative recombination at the stripe edges, but if controlled would result in lower threshold currents. Another approach to achieve better current confinement is to etch down completely through the active and lower cladding regions; however, this would negatively impact the laser by contributing to carrier scattering loss and nonradiative surface recombination.

Photon confinement is achieved by the formation of the ridge. The presence of the ridge lowers the effective refractive index of the regions beside the stripe and thus helps concentrate the optical mode in the active region under the ridge. As discussed earlier, vertical photon confinement is achieved by utilizing small energy bandgap (high refractive index) material for the active region and larger energy bandgap (lower refractive index) materials for the cladding regions.

As mentioned earlier, the key requirements of highly integrable edge-emitting lasers given priority in the present work were smooth facets with high facet reflectivity and precisely defined lengths. The various approaches that could be used to create edge-emitting lasers with these characteristics will now be presented.

3.3 Approaches to Create Accurately Dimensioned Lasers With Highly Reflective Optical Facets

3.3.1 Cleaved Facet Lasers

The ideal laser facet is formed by cleaving the semiconductor along a natural cleavage plane. When this technique is done properly, un-coated facet reflectivities around 30% are routinely achieved for semiconductor lasers. However, attempts to cut or break the wafer in directions even just a few degrees off axis of the cleavage plane, can result in poor facets [40].

Since the early 1970's, there has been automated commercial cleaving equipment produced by manufacturers such as Dynatex International and Loomis Industries [89]. This equipment characteristically treats cleaving as a manual two step process; whereby, the wafer is first diamond scribed along the cleavage plane and then a sufficient pressure is applied to propagate this scribe line cut through the semiconductor substrate. The first step in the process, the scribe procedure, results in a small cut made in the semiconductor that is typically from 3 to 5 μm wide [42, 39]. Figure 3-8 pictorially describes two techniques, referred to as the roller break method and the 3-point bending method, utilized by Loomis Industries in their commercial automated cleaving tools to propagate the break along the scribe line. Both of these techniques work by the application of tensile strain to the scribed wafer.

The precision of these automated cleaving processes is reported in the literature to be no better than $\pm 5 \mu\text{m}$ [64]. Looking at Figure 3-2c, this level of imprecision results in coupling losses in upwards of 6 dB/facet which makes our end-fire integration scheme impractical.

3.3.2 Etched Facet Lasers

It is quickly recognized that if one could etch low loss highly reflective facets, then the issue of creating well dimensioned lasers is fairly trivial. This would have important consequences for the present integration strategy as well as the whole laser

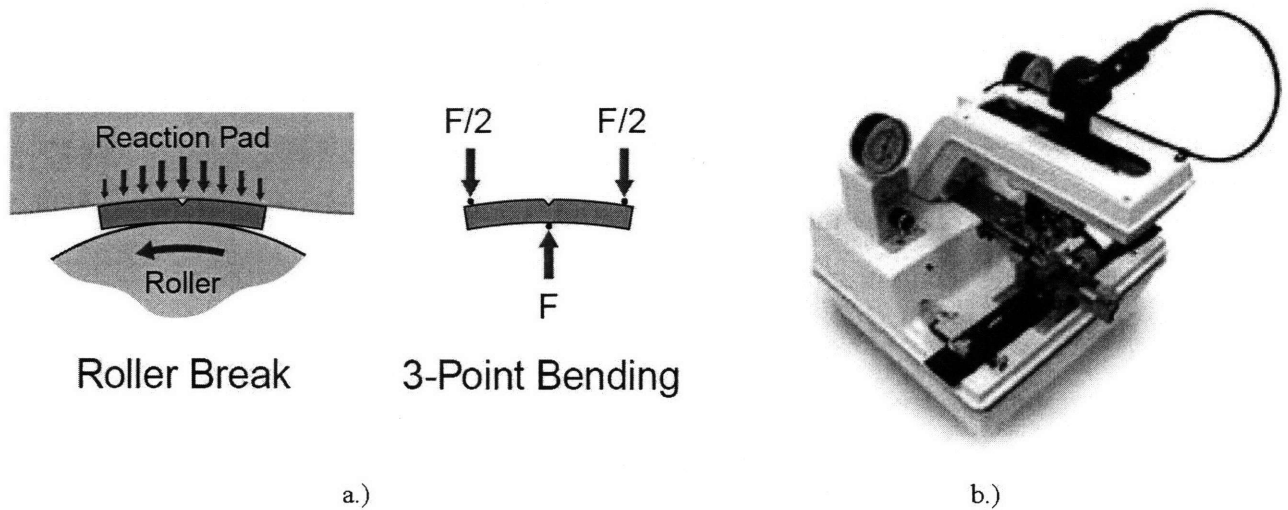


Figure 3-8: a.) Schematic showing the two general techniques, roller break and 3-point bending, used in the Loomis Industries automated cleaving process LSD-100 tool. b.) The LSD-100 tool. [39]

manufacturing industry in general. Unfortunately, over twenty five years of research has been done on laser facet etching, but today manual or mechanical cleaving is still the preferred manner of forming end facets[56]. The issue with etched facets is that the etching process seems to invariably impart roughness on the facets. This roughness arises either by the etching process in general or by roughness in the material used to mask the etch. Francis et al. studied the effect of etch roughness on laser performance[26].

A few companies have begun to implement etched facet technology in their production lines. BinOptics claims to have developed a chemically assisted ion-beam etching process that can be used to obtain mirror smooth facets in InP, GaAs, and GaN [16]. Similarly Xponent Photonics, Inc., reports that it etches the facets on its commercial Fabry-Perot and Distributed Feedback (DFB) lasers [7].

3.3.3 Micro-Cleaved Facet Lasers

Over the past two decades, several researchers have looked at controlled micro-cleaving of active devices. Most of these approaches involve etching deep grooves on the wafer backside to weaken the crystal so that application of force at these

locations results in cleaving.

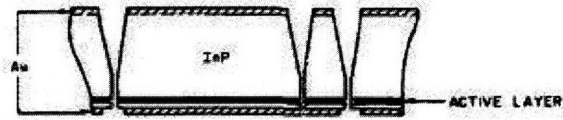
For instance, Bowers et al. used photoelectrochemical means to etch 80 μm deep, 20 μm narrow grooves on the backside of the InP substrate (Figure 3-9a). When the etched substrate was flexed, 65% of the devices cleaved in the deep groove areas and short lasers having cavity lengths of 38 \pm 4.2 μm were achieved [50].

Wada et al. utilized a cantilever structure (Figure 3-9b) to achieve micro-cleaved facets for AlGaAs/GaAs ridge lasers[71]. The general fabrication process associated with this micro-cleaving technique is shown in Figure 3-9b. Specifically, selective etching is used to obtain a cantilever device structure. When a force is applied to the two cantilever ends, micro-cleaving results. Other research efforts utilized a combination of deep groove etching, manual scribing and bending of the wafer to cause cleaving, while others focussed their work on cleaving epitaxially lifted-off GaAs/AlGaAs lasers by attaching the released epi-layer to a metal sheet and manual flexing the sheet [37]. Patterning of the deep groove had a precision of approximately 1 μm , but no mention was made of the precision of the resulting micro-cleave.

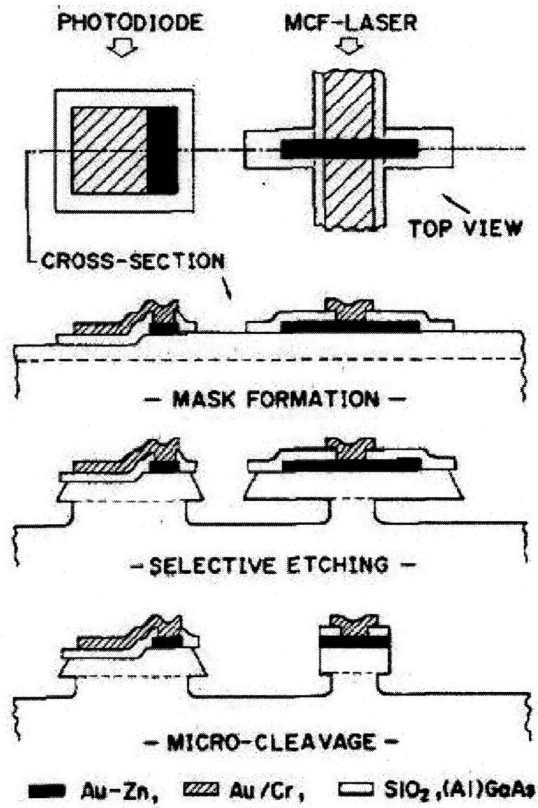
While these techniques achieved cleaved facets and fairly precise dimensional control, all of these techniques unfortunately relied on some manual component such as flexing of the substrate or scribing. Thus, they do not lend themselves to inexpensive, high-volume production. Even more importantly, none of these techniques used to produce ultrathin resulted in the continuous-wave laser operation on non-native substrates. Only pulsed laser operation was achieved.

3.4 Our Novel Micro-Cleaving Approach

Given the desire for an integration platform utilizing end-fire coupling between a recess mounted edge-emitting laser and a silicon-based dielectric waveguide, the need for an edge-emitting laser with both smooth facets and precisely defined dimensions has been motivated. It has been argued that the current techniques in industry used to obtain mirror smooth cleaved facets do not offer the precise control of laser di-



(a) Bowers et al. micro-cleaving approach. [50].



(b) Wada et al. micro-cleaving approach [71]

Figure 3-9: Micro-cleaving research approaches.

mensions that are required to keep the gap spacing between the laser and waveguide facets small and thus the coupling loss low. While etched-facet technologies are becoming commercialized more and more today, it is understood that an etched facet is not an ideal facet. Etched facets often have characteristic roughness which reduces facet reflectivity and compromises the device quality. While many groups have investigated micro-cleaving techniques, these techniques, by and large, rely on some manual component such as flexing of the substrate or diamond scribing. Moreover, these techniques have not resulted in CW lasing on non-native substrates. It would be ideal to develop a process devoid of any manual component while still achieving optical quality cleaved facets and CW lasing on non-native substrates.

Identifying the need for a fabrication process that results in both cleaved mirror smooth facets and precisely dimensioned laser cavity lengths, the approach taken was to develop a novel micro-cleaving process. A brief overview of the general micro-cleaving technique, which in theory could be applied to a multitude of in-plane optical devices requiring cleaved facets and precise dimensions, will now be given.

As is the case for the fabrication of all InP and GaAs semiconductor lasers, our process starts with a (100)-oriented compound semiconductor wafer upon which has been grown an in-plane laser or semiconductor optical amplifier epitaxial layer structure. This wafer crystal orientation is chosen since the cleavage planes of these materials lie along the (011) and (0 $\bar{1}$ 1) planes, or in other words, the orthogonal directions on a (100)-oriented wafer as is shown schematically in Figure 3-10.

Starting with this orientation, full front-side device processing is carried out. This front-side processing could involve, but is not limited to, top-side ohmic contact formation, current confinement implementation, photon confinement realization (i.e., such as the formation of a ridge in a semiconductor ridge laser), and device planarization. It should be emphasized that this micro-cleaving process aims to put no restrictions on the device front-side processing. After this device front-side processing is completed, the fabrication steps specific to the micro-cleaving process are undertaken. First, a pattern consisting of a large array of rectangular bars are aligned over the devices so that the short and long faces of the rectangular bars are aligned with

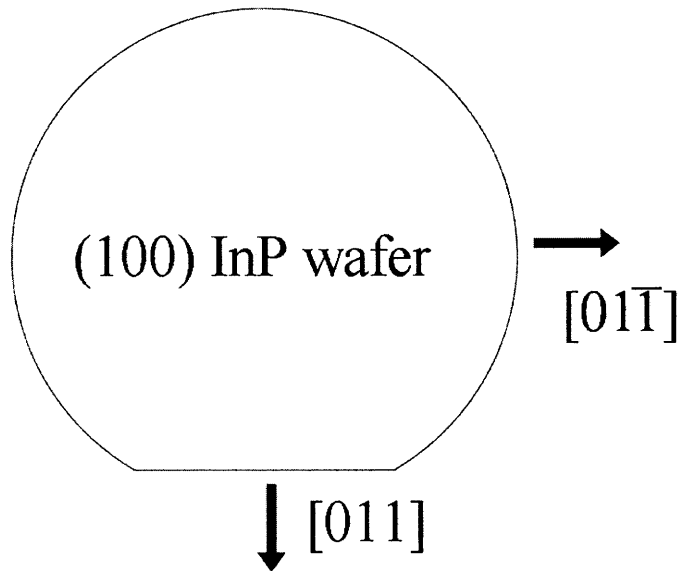


Figure 3-10: Schematic showing a (100) InP wafer and the associated cleavage planes

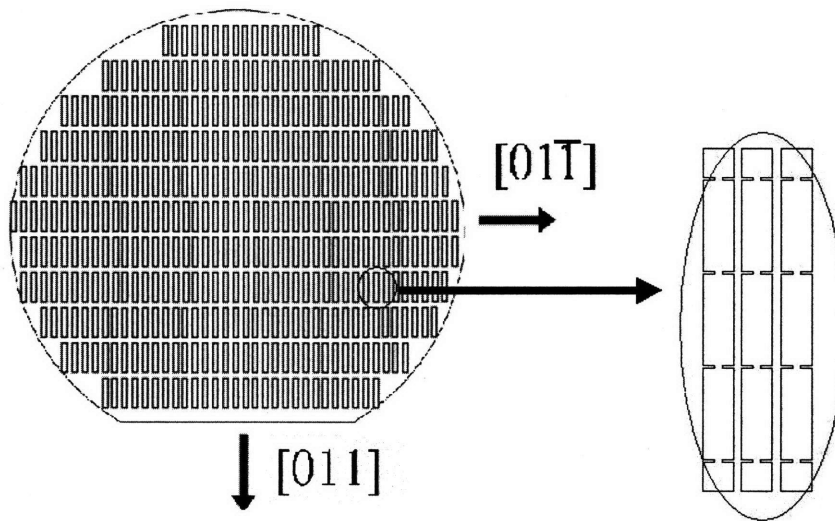
the two cleavage planes as is shown in Figure 3-11a.

Upon closer examination, these rectangular bars have notches in them which divide each long rectangular bar into three rectangular sub-bars in between two square sub-bars as is shown in Figure 3-11b. The rectangular sub-bars, labeled L1, L2, and L3, correspond to the desired active optical devices. The square sub-bars, labeled D1 and D2, denote the dummy devices.¹⁴ The distinguishing feature between the dummy devices and the desired active optical devices, is that after the micro-cleaving process is completed, the desired devices will have two micro-cleaved facets, while the dummy devices will have one micro-cleaved facet and one etched facet. An SEM of an array of bars patterned into a InP-based device wafer is shown in Figure 3-12.

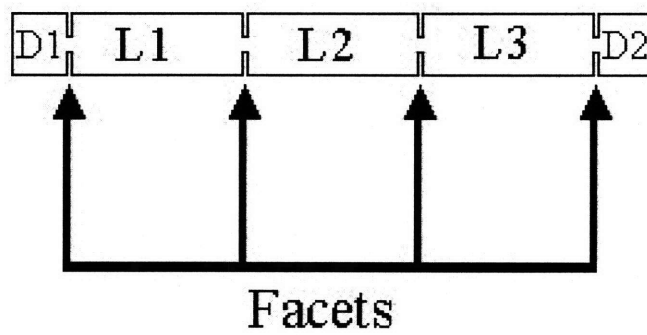
After this micro-cleave enabling bar pattern is etched into the device wafer, one of a multitude of techniques, such as selective substrate removal or epitaxial layer release, is utilized to etch these bars free from the substrate.

Once the bars are released from their native substrate, the task is to induce cleaving. To understand how this bar pattern will enable the cleaving, a few key

¹⁴To conserve real-estate on the expensive compound semiconductor wafer, the size of the dummy devices are kept small.



(a) Laser patterning schematic



(b) Micro-cleaving enabling element schematic,
D=Dummy, L=Laser

Figure 3-11: Micro-cleave enabling elements

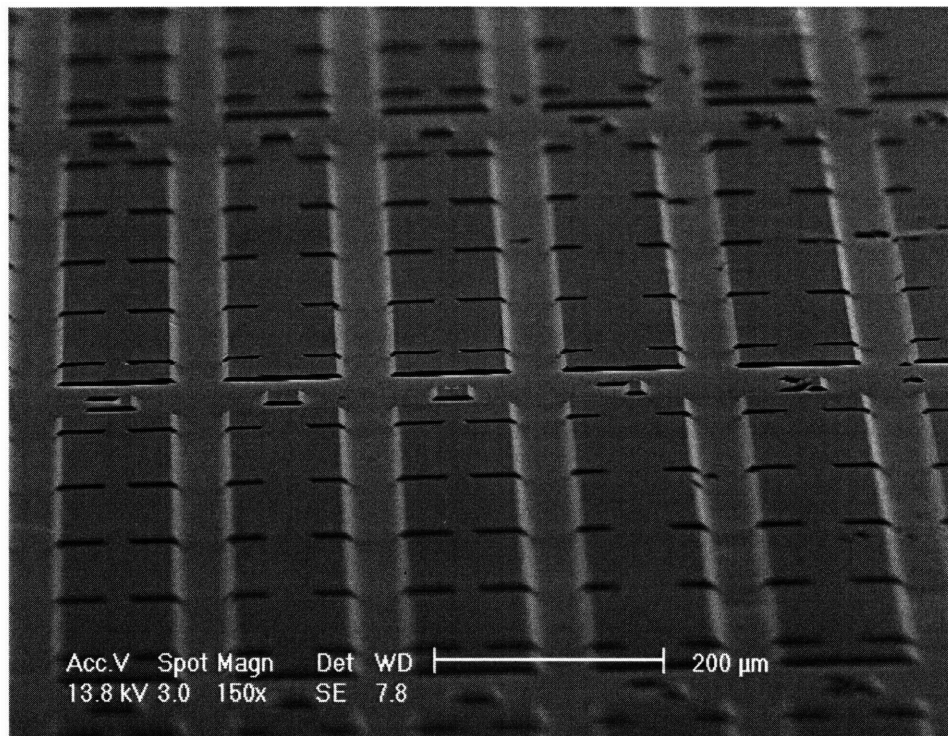


Figure 3-12: Array of bars formed on the front-side of a InP substrate upon which a InP/InGaAsP epitaxial structure has been grown.

concepts will first be described.

First, it is a well-known fact that crystalline materials will most easily break (i.e., cleave) along certain dimensions which are referred to as cleavage planes. The location of cleavage planes in semiconductors can be due to favorable atomic densities along certain planes (i.e., Silicon (111)) or electrical surface neutrality conditions (i.e., GaAs, InP). For compound semiconductors, like InP, cleavage planes lie along the non-polar crystal planes [14].

(100) InP and GaAs semiconductor wafers will most easily break (i.e., cleave) in two dimensions, one that is parallel to the plane of the wafer flat, and the other dimension which is perpendicular to the wafer flat. These cleavage plane locations are specifically why the bar pattern was aligned with the wafer flat.

With the bar pattern aligned with the cleavage plane, the notches are used to reduce the length over which the cleave must take place to achieve a cleaved facet. This reduction in the required cleavage length increases the likelihood that the cleave will occur in this region and that a good cleave, producing a smooth facet, will result.

The precision in terms of the location where the actual cleave takes place should be enhanced by making this notch as narrow and as long as possible. In other words, by making l_2 and w narrow, as is shown in Figure 3-13.

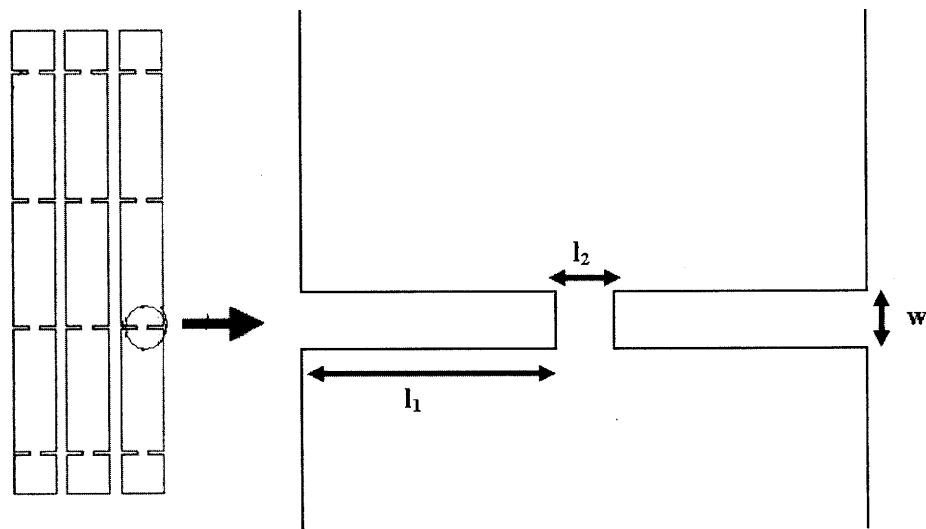


Figure 3-13: Schematic of the micro-cleave enabling bar pattern.

There are practical limits to how narrow the notch width and how long the notch, l_1 , can be. Theoretically, l_2 must be wider than the semiconductor ridge. This ridge is most typically narrower than $10 \mu\text{m}$ wide and for single mode operation, could be considerable narrower than this. The minimum size of the notch width, w , is limited by the device topography that is present when the bar patterning process step is reached. This topography will limit the achievable resolution of the photolithography process used to pattern the bar pattern. The minimum notch width is further limited by the process technique used to etch the bar pattern into the semiconductor. If wet etch techniques are used, the minimum width would be on the order of the thickness of the device structure. Dry etching could enable narrower notch widths, but phenomena such as aspect ratio dependent etching need to be addressed. Aspect ratio dependent etching (ARDE) is the term used to describe the phenomena where the etch rate of narrow openings proceeds at a slower rate than wide openings. ARDE encountered while etching a micro-cleave bar is shown in Figure 3-14 where the narrow notch region etched slower (and to a shallower depth) than the region outside the notch. More details on these dry etch phenomena are found in Ref.[46].

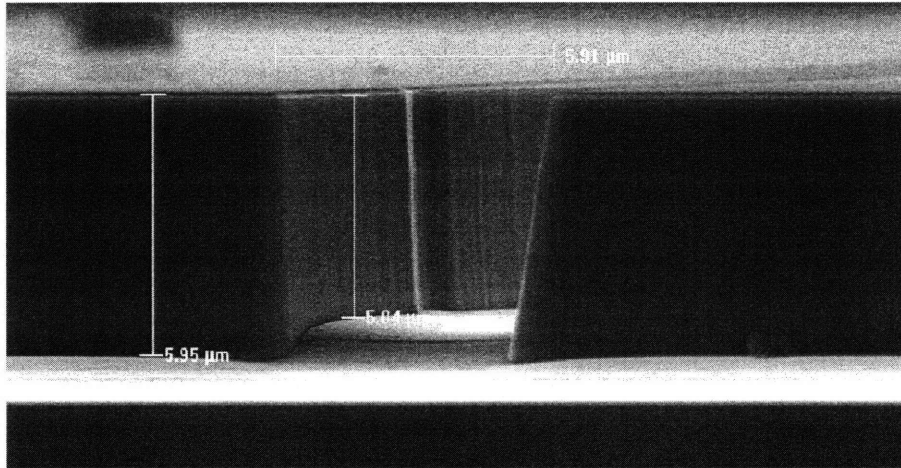


Figure 3-14: Aspect Ratio Dependent Etching in notch region

An intriguing way to increase the cleave precision even when w and l_2 reach their practical limits, is by incorporating other non-crystalline material as is shown in Figure 4-15. This Figure shows a situation where metal is deposited along a

semiconductor ridge except for a narrow region in the notch area.

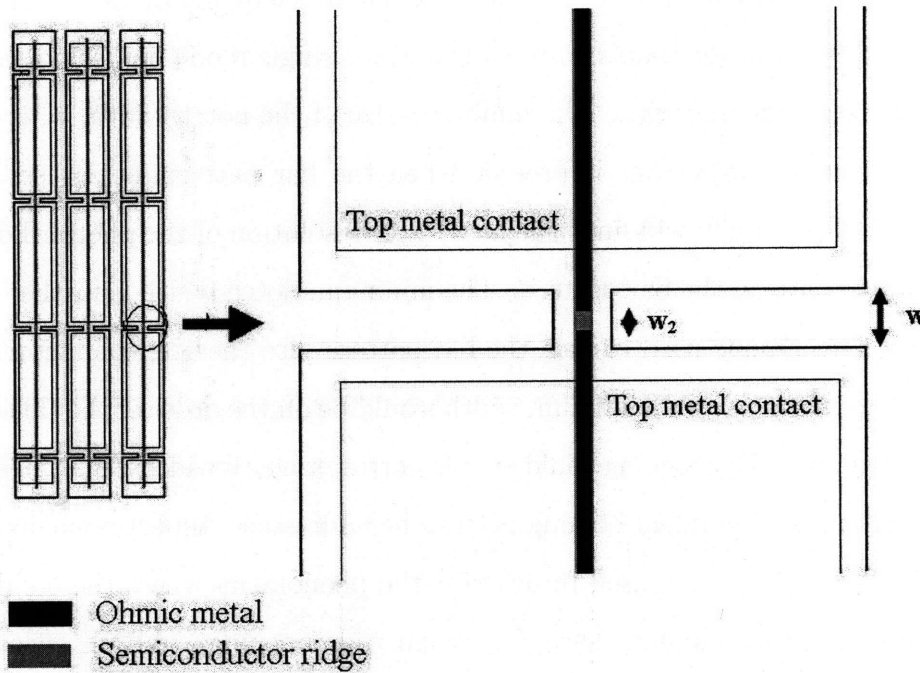


Figure 3-15: Schematic of the micro-cleave enabling bar pattern with detail of the semiconductor ridge and ridge metal ohmic contact.

In this example, a metal can be patterned to a resolution of w_2 which is narrower than the notch width, w . An opportunity like this could arise, for instance, if during the metal patterning step, the wafer is much more planar than during the bar patterning step. From our experience, micro-cleaving within the notch region is significantly enhanced by the presence of non-crystalline materials in regions outside the notch region.

The process technology used to manufacture the micro-cleaved ridge lasers will now be discussed in Chapter 4.

Chapter 4

Edge-Emitting Laser Process

Development

Semiconductor fabrication processes were developed for both a conventionally cleaved ridge laser and a highly integrable micro-cleaved ridge laser. Many of the same fabrication steps and techniques are used to manufacture both of these devices. In this chapter, the process used to fabricate the conventionally cleaved ridge laser will first be detailed. Then, the more innovative process for manufacturing the micro-cleaved ridge laser will be explained. In the course of describing these fabrication processes, the similarities and differences between the two processes will be clarified. Full process flows for both the conventionally cleaved ridge laser and the micro-cleaved ridge laser are included for the reader as a reference in Appendices A and B respectively.

4.1 Starting Semiconductor Material

For both the conventionally cleaved ridge laser and the micro-cleaved ridge laser, the process began with the procurement of a 1550 nm Fabry-Perot laser epitaxial InP wafer from Landmark Optoelectronics. The layer structure of the purchased epitaxial wafer is shown in Figure 4-1.

The substrate is a 350 μm thick n-type (i.e., highly doped with Sulfur to the level

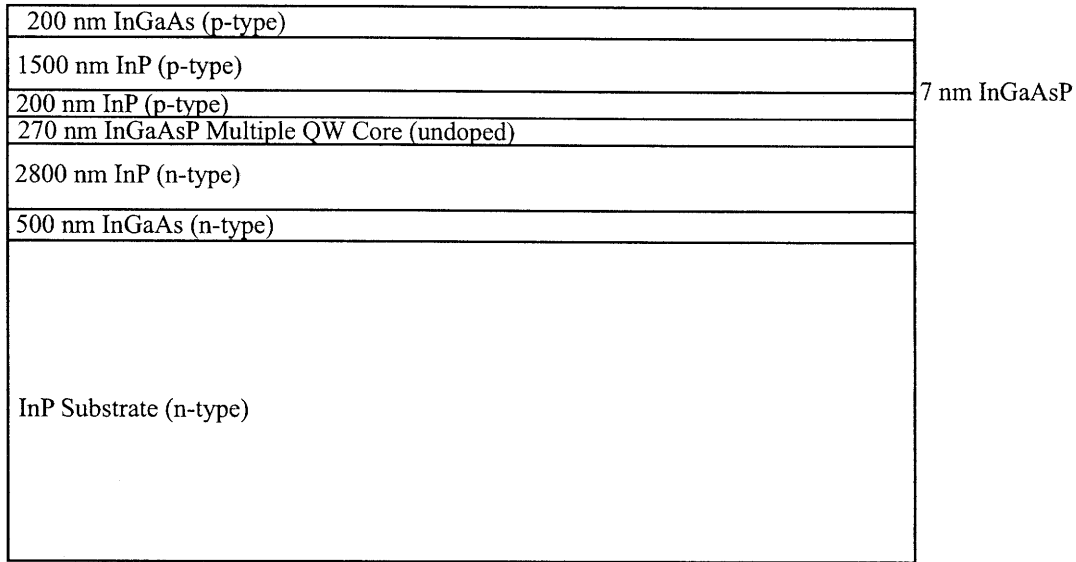


Figure 4-1: Cross-sectional schematic of the 1550 nm laser structure grown on InP.

$N_D = 2-8 \times 10^{18} \text{cm}^{-3}$) InP wafer. The epitaxial n-type InGaAs layer is included specifically for the micro-cleaved ridge laser process ¹. If only conventionally cleaved ridge lasers were being fabricated, this layer would not be included. For the micro-cleaved ridge laser, the n-type InGaAs layer serves a dual purpose. First, since it has a narrower energy bandgap than InP and is highly doped (i.e., $N_D = 2 \times 10^{18} \text{cm}^{-3}$), it is useful for forming a low resistance ohmic contact to the bottom of the device. Second, this layer acts as a reliable etch stop ².

The 2800 nm thick n-type InP layer serves multiple purposes as well. First, since it has a lower refractive index than the core region, it forms the lower cladding of the laser and guides the optical wave produced in the laser active region. Second, with its high n-type doping (i.e., $N_D = 5 \times 10^{17} \text{cm}^{-3}$), this InP layer enables a large density of electrons to be injected into the active region when the device is forward biased. This large injected carrier density is vital to the laser's operation. Third, this layer isolates the optical wave in the core region from the bottom n-type InGaAs contact layer, which has a characteristic high refractive index.

¹InGaAs is used as shorthand for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, the material which is lattice matched to InP.

²During subsequent front-side and back-side etch processes, it is useful to controllably stop the etch at a specific point. This layer will be used for this purpose.

The InGaAsP multiple quantum well core consists of four 6 nm wide InGaAsP ($\lambda_g = 1.71 \mu\text{m}$) quantum wells separated by three 9 nm wide InGaAsP ($\lambda_g = 1.25 \mu\text{m}$) barriers and bounded by two 110 nm thick InGaAsP ($\lambda_g = 1.25 \mu\text{m}$) layers. This 270 nm thick structure forms the active (i.e., gain) region of the laser device and is shown in Figure 4-2. Note that these layers are undoped to lessen the optical mode loss from free-carrier absorption.

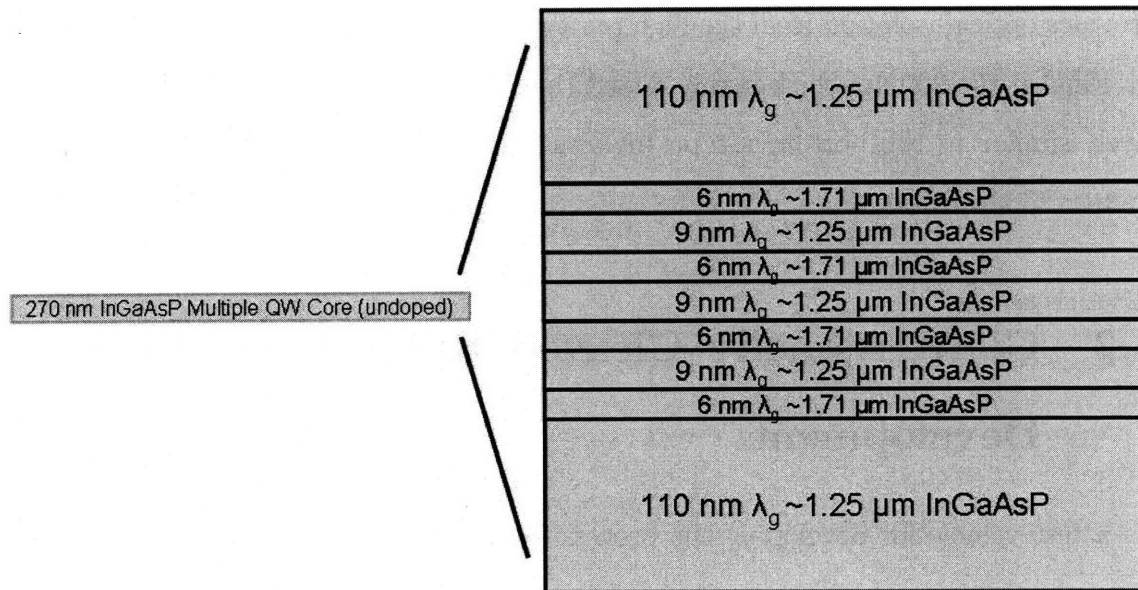


Figure 4-2: Cross-sectional schematic of the 270 nm thick active region of the 1550 nm laser epitaxial InP wafer.

The 200 nm thick p-type InP layer, with its low refractive index compared to the active core region, serves as part of the upper cladding layer. Moreover, this layer is a buffer layer between the active region and the ridge structure that is processed above this layer. If this buffer layer was left out of the device structure and instead the semiconductor ridge extended all the way down to where it just met the active layer, increased non-radiative recombination losses would likely result and the ridge would have to be considerably narrower to ensure single lateral mode operation.

The 7 nm thin InGaAsP layer serves as an etch stop that is useful for forming the ridge structure. In this case, hydrochloric acid has proven to be an extremely useful etchant in this process because it selectively etches InP at a high rate while it etches

InGaAsP a negligible amount.

The 1500 nm thick p-type InP layer serves many of the same purposes as the 2800 nm thick n-type InP layer. Specifically, this layer forms the upper waveguide cladding that guides the laser generated optical wave in the core region. Also, this layer with its large p-type doping (i.e., $N_A = 5 \times 10^{17} \text{cm}^{-3}$) enables a large density of holes to be injected into the active region when the device is forward biased. This layer also provides optical isolation from the high refractive index p-type InGaAs contact layer.

Finally, the 200 nm thick highly doped (i.e., $N_A = 2 \times 10^{18} \text{cm}^{-3}$) p-type InGaAs layer, similar to the bottom n-type InGaAs layer, aids the formation of an ohmic contact to the device.

4.2 Conventionally Cleaved Ridge Laser Process Development

As a test vehicle for developing the process for the highly integrable edge-emitting lasers, work was undertaken to produce conventionally cleaved ridge lasers starting with the structure shown in Figure 4-1. The front-side and back-side device processes will now be discussed.

4.2.1 Front-Side Device Processing

A schematic cross-sectional view of the basics of the conventionally cleaved edge-emitting laser process is shown in Figure 4-3.

Top Ohmic Contact Formation

The process begins with the deposition and lift-off of a Ti/Pt/Au ohmic metal stack on the top surface of the epitaxial wafer. To accomplish this, image reversal photolithography³ is performed. As is shown in Figure 4-4, care is taken to line up the

³Using an image reversal process is optimal in this case because it results in a sloped photoresist profile, that allows the metal to be easily lifted off in the areas where it is in contact with photoresist.

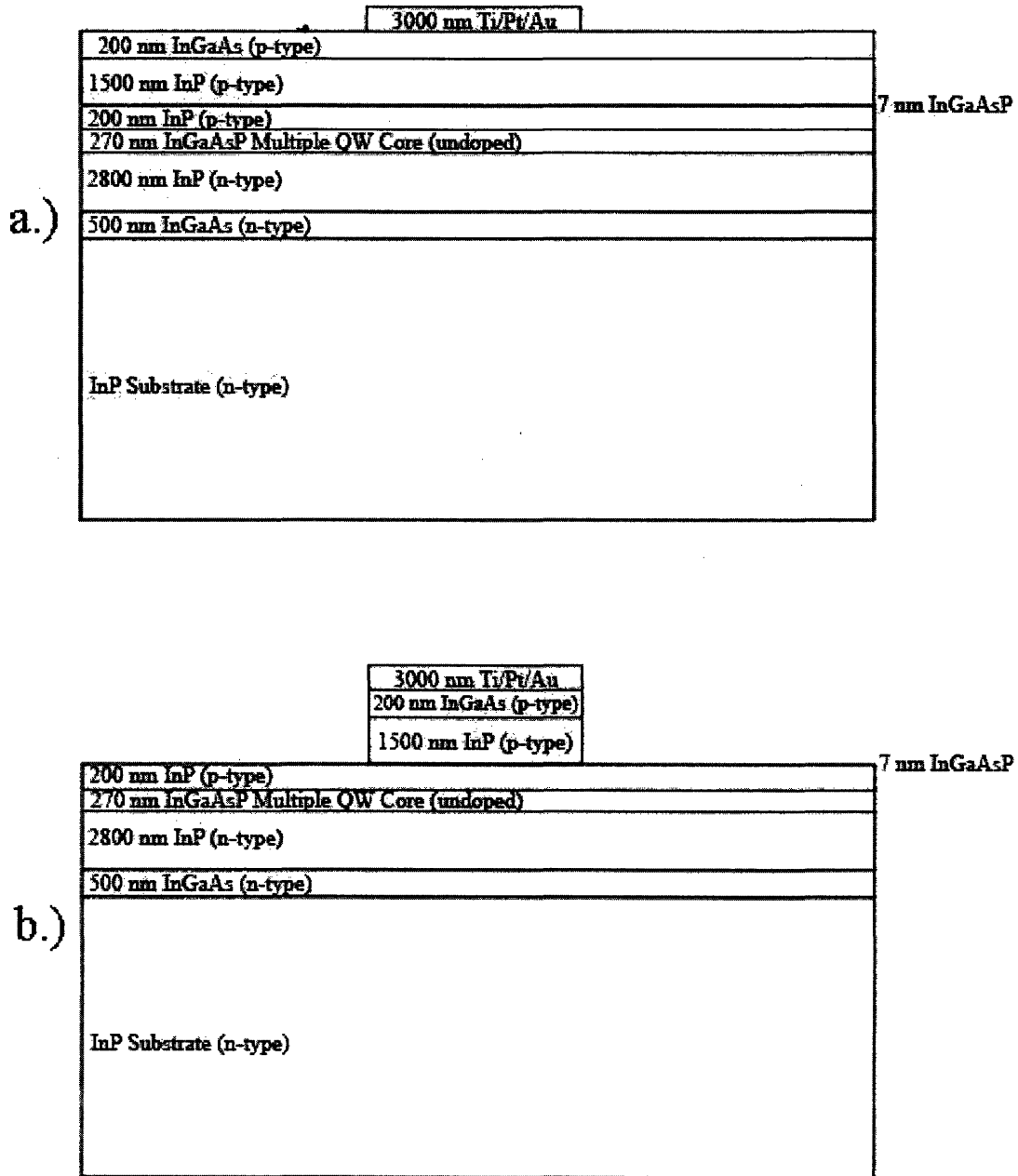


Figure 4-3: Conventionally cleaved ridge laser front-side process flow schematic: a.) Top ohmic contact formation through b.) Semiconductor ridge formation.

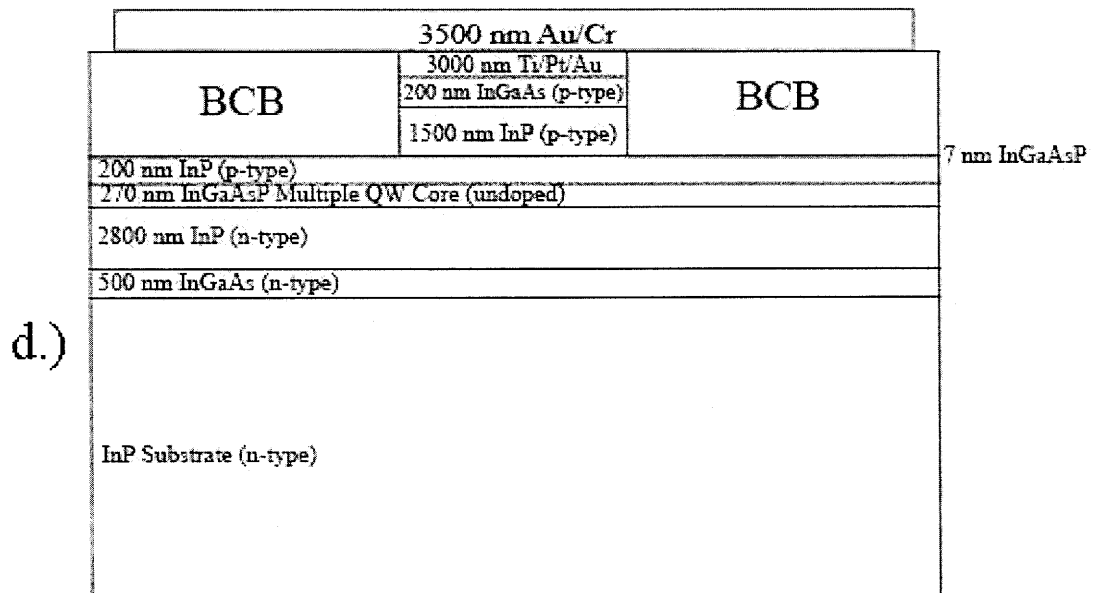
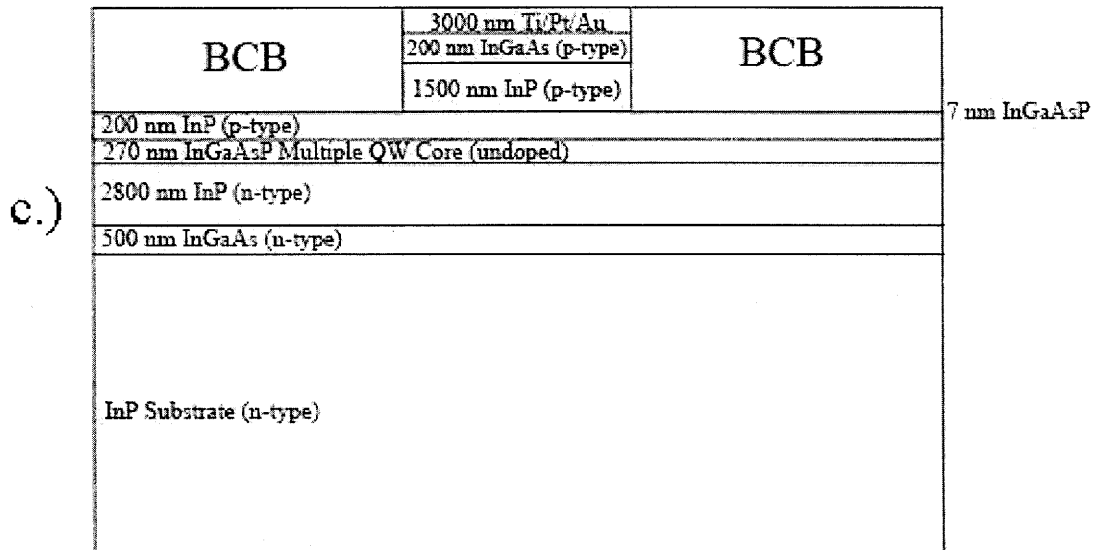


Figure 4-3: Conventionally cleaved ridge laser front-side process flow schematic continued: c.) Dielectric layer deposition and planarization through d.) Top large area contact formation.

ridge pattern with the cleavage plane of the (100) InP substrate. This alignment is critical for the cleaving process ultimately resulting in mirror smooth cleaved facets.

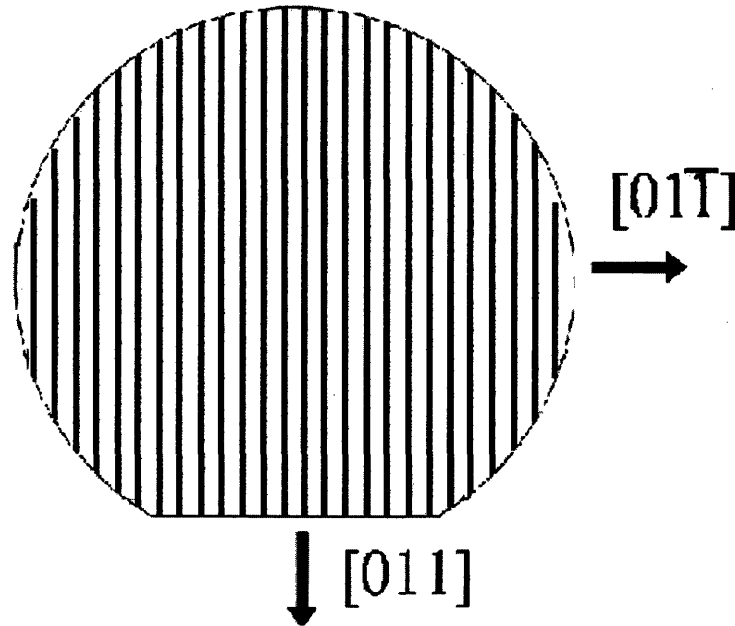


Figure 4-4: Schematic showing the alignment of the metal ohmic contact ridge pattern to the cleavage planes of the InP wafer.

Once photolithography is complete, the electron beam (e-beam) deposition of the Ti(300 Å)/Pt(200 Å)/Au(2500 Å) material is performed ⁴. Each of the metals deposited in this stack plays an important role in the ohmic contact formation. The titanium layer provides strong adhesion of the metal stack to the semiconductor. The platinum layer acts a barrier to prevent gold diffusion into the semiconductor substrate ⁵ as well as indium out-diffusion from the substrate [43]. The top gold layer is chosen for its low contact resistivity and high chemical inertness, which make it quite useful as a pad for probing the device [77, 8]. It should be noted that the electron beam currents and time duration of the application of these currents are controlled to ensure that the deposition process does not heat up the InP substrate

⁴This ohmic contact metallization is commonly used in the industry to obtain ohmic contacts on p-type InP and p-type InGaAs. The details of this process and other individual processes are found in Appendix C

⁵At elevated temperatures, gold can diffuse into the semiconductor which results in increased contact resistance

too much ⁶. If the substrate heats up too much, the photoresist can be rendered irremovable even by chemical (i.e., acetone or Microstrip remover) or ashing means.

Following this metal deposition, the sample is placed in a acetone (or Microstrip 2001, a proprietary solvent) bath and with the aid of slight ultrasonic agitation, the metal film is lifted off the substrate surface, remaining only where the film directly touched the semiconductor. After the lift-off process is complete and all of the photoresist has been removed from the sample, it is optimal to rapid thermal anneal (RTA) the sample for 385 °C for 30 seconds in a forming gas (95% N_2 , 5% H_2) ambient to lower the contact resistance ⁷. Another benefit of performing the annealing step is that it improves the adhesion of the metal contact to the semiconductor ridge. In some early trials of the conventionally cleaved laser process development, the sample did not undergo this annealing step and the ohmic metal peeled off following the semiconductor ridge wet etch (Figure 4-5).

Semiconductor Ridge Formation

Using the ohmic metal ridge contact as a self-aligned etch mask, the semiconductor is wet etched. First, the top p-type 200 nm thick InGaAs layer is etched in a room temperature solution of 20:1:1 deionized water (DI H_2O): hydrogen peroxide (H_2O_2 , 30%) : sulfuric acid (H_2SO_4 , 96%). This etchant selectively etches InGaAs at a rate of approximately 500 nm/minute and stops on the InP layer.

Then, concentrated hydrochloric acid (HCl, 37%) is used to selectively etch the 1.5 μm thick InP layer ⁸. Due to the strong selectivity of this etchant for InP over InGaAs and InGaAsP, this etch stops on the 7 nm InGaAsP etch-stop layer.

Concentrated hydrochloric acid is just one of several wet etch chemistries that offer good selectivity between InP and its InGaAs ternaries and InGaAsP quaternaries. Extensive characterization of these etch characteristics can be found in the literature [9].

⁶Significant heating of the substrate often occurs when depositing such high melting temperature materials like platinum ($T_{melt} = 1769$ °C.)

⁷Annealing of this ohmic contact leads to alloying at the Ti-InGaAs interface [77].

⁸HCl etches InP according to the reaction $\text{InP(s)} + \text{HCl(aq)} \rightarrow \text{InCl}_3 \text{(aq)} + \text{PH}_3 \text{(g)}$

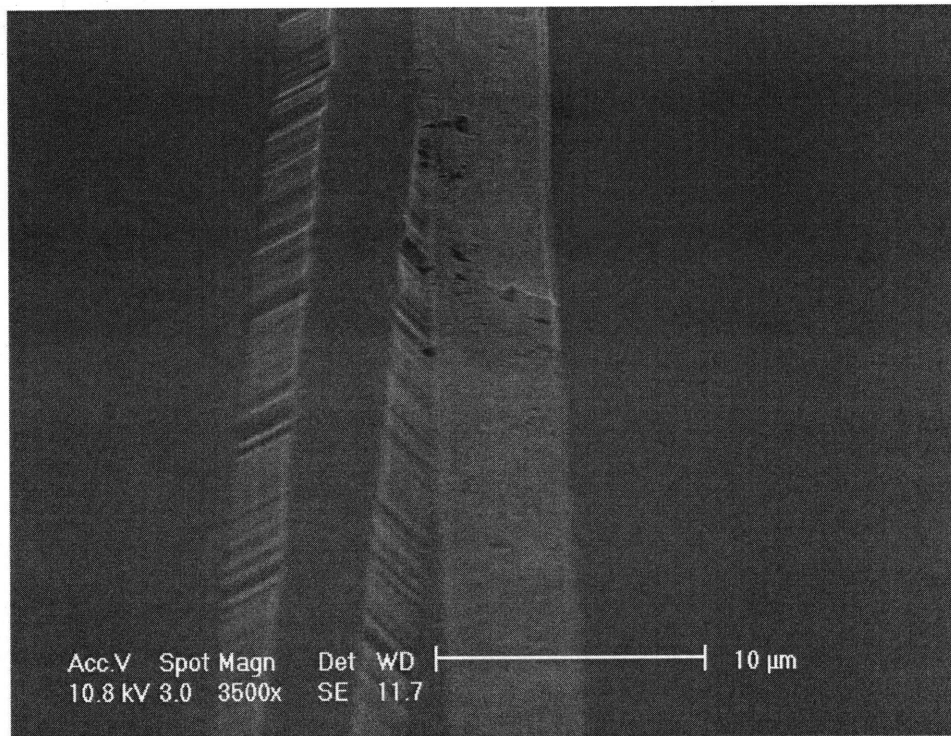


Figure 4-5: Scanning electron micrograph of an unannealed ohmic contact metal to semiconductor ridge after the semiconductor ridge etch.

Dielectric Layer Deposition and Device Planarization

With the semiconductor ridge formed and ohmic contacted, a large area electrical contact needs to be made to the ohmic ridge. However, at this stage of the process there is device topography of around $2\ \mu\text{m}$ around the ridge as is shown in Figure 4-6a. Therefore, the device must first be planarized. The material used to planarize the device is Cyclotene produced by DOW Chemical. Cyclotene, a material which is primarily composed of B-staged bisbenzocyclobutene-based (BCB) monomers, is a strong insulator with low dielectric constant (2.5 to 2.65) and large breakdown field ($5 \times 10^6\ \text{V/cm}$). The basic planarization process is shown in Figure 4-6.

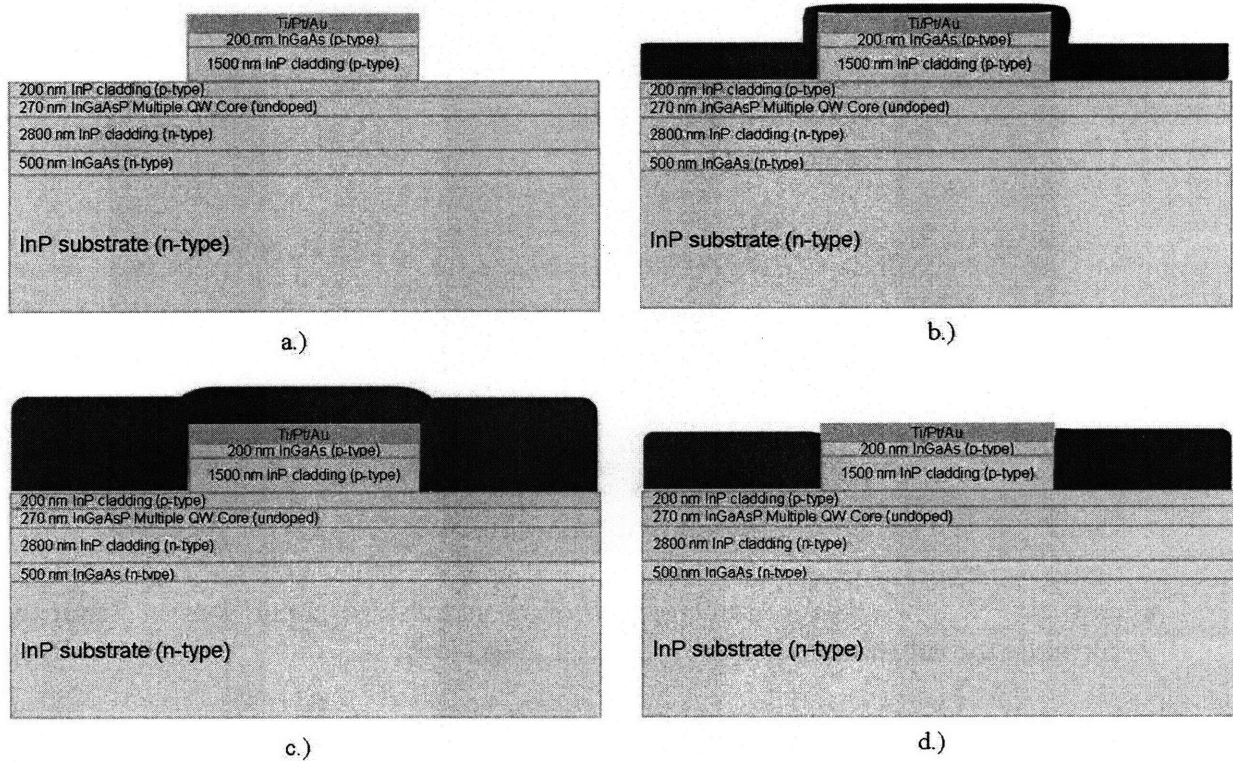


Figure 4-6: Schematic of the dielectric layer deposition and planarization procedure: a.) Starting sample, b.) First coat of Cyclotene and cure, c.) Second coat of Cyclotene and cure, d.) Cyclotene etch-back.

First, a layer of cyclotene is spun on the wafer. The wafer is then cured at a temperature of $210\ ^\circ\text{C}$ for 40 minutes in an annealing furnace. During this curing step, precautions are taken to prevent oxidation of the BCB film. Specifically, the

oxygen is flushed out of the furnace by sending a high flow of nitrogen into the furnace for thirty minutes prior to ramping up the furnace temperature. This flow of nitrogen continues as the furnace temperature is eventually raised and while the sample is curing. Next, a second coat of cyclotene is applied and the sample is cured at a temperature of 250 °C for 60 minutes.⁹

At this stage, the sample is quite planar according to profilometer measurements, having gone from 2 μm tall features to topography of around 50 nm. However, a thin layer of cyclotene is now covering the top of the ohmic metal ridge where electrical contact needs to be made. Thus, an etch-back process is used to uniformly etch-back the cyclotene until the metal ridge contact is exposed.

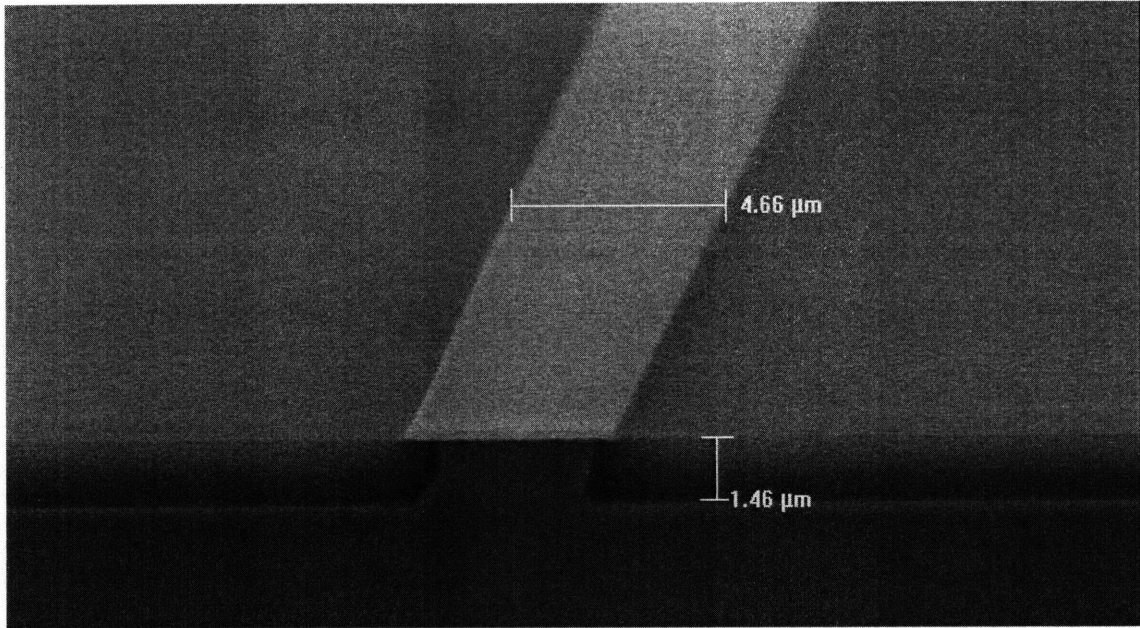
The specific etch-back process developed is a reactive ion etch (RIE) process performed in a Plasmatherm etch tool with a 6:1 oxygen (O_2): silicon hexafluoride (SF_6) chemistry at a relatively high pressure (200 mtorr) and low radio frequency (RF) power (150 W). Due to variations in both the cyclotene thickness as well as the cyclotene etch rate across a sample, a slight over-etch is used. With this over-etch, there will be times when the ions are directly bombarding some areas of the ridge metal ohmic contact. For this reason, low power is chosen to reduce the likelihood of metal sputtering of the ohmic contact metal. The pressure is kept high to obtain a reasonably high etch rate (i.e., approximately 70 nm/min) and nondirectional or isotropic etching. Endpoint detection was performed manually. That is to say every couple of minutes, the dry etching process was halted and the sample was removed from the machine and visually inspected under a microscope.

Scanning electron micrographs were taken of the laser after this dielectric layer deposition and device planarization process sequence and these images are shown in Figure 4-7.

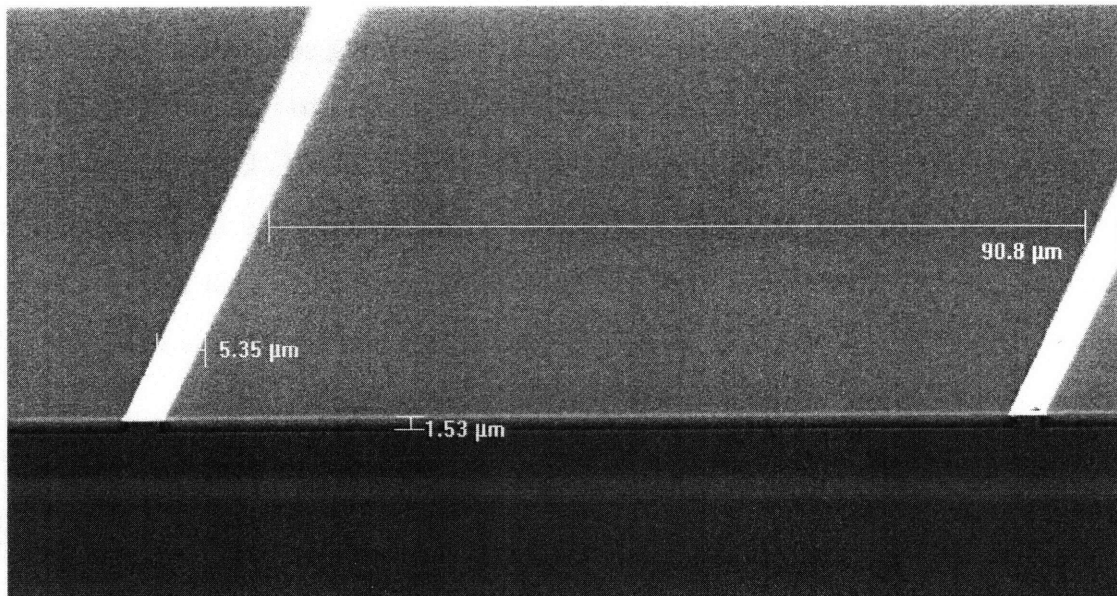
Top-Side Large Area Electrical Contact Formation

Once the planarization and etch-back processes are completed, a large area electrical contact is formed on top of the ridge. Specifically, image reversal lithography is used

⁹Further details on this process can be found in Appendix C.



(a) Cross-sectional view of a metallized ridge laser.



(b) Top-down view of a pair of metallized ridge lasers.

Figure 4-7: Scanning electron micrographs of ridge lasers after the BCB planarization and etch-back process.

to designate the deposition area and a thick (i.e., few hundred nm) layer of gold (with a few tens of nm chromium adhesion layer ¹⁰) is electron-beam deposited and a lift-off process is performed. SEMs of the cross-section of the resulting structure are shown in Figure 4-8.

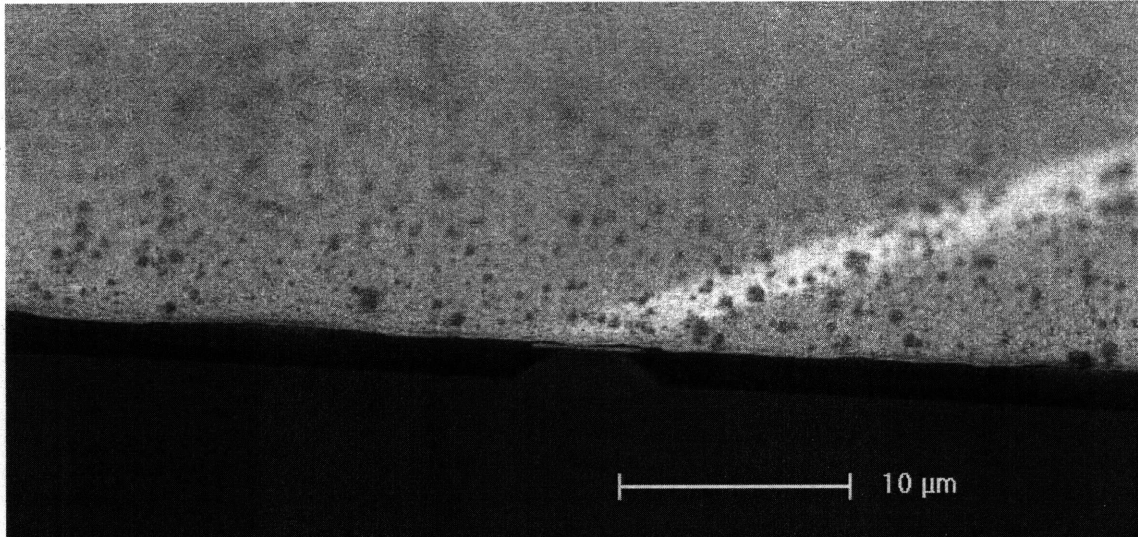
This large area electrical contact formation step is a critical step in the laser process. This can be understood if one thinks of the resistive nature of a metal layer. The resistance of a material can be defined by the following relation

$$Resistance = \frac{\rho L}{A} \quad (4.1)$$

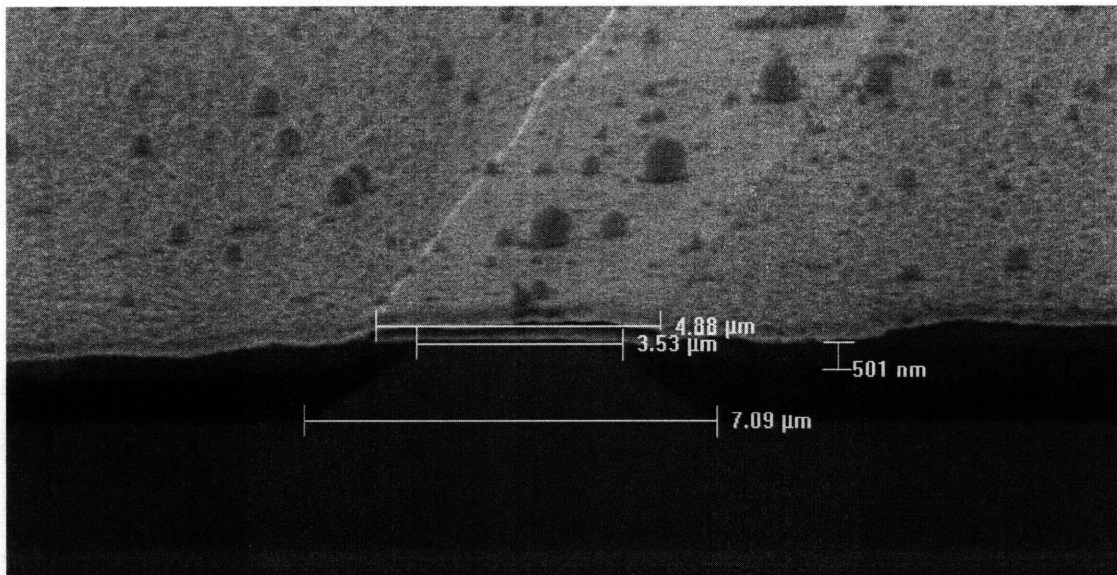
where ρ is the material resistivity, L is the length of the material between the electrical probes, and A is the cross-sectional area of the metal pattern. Metals in general, gold in particular, have very small resistivities, ρ . However, if the gold pattern is very long and/or if the gold pattern has a small cross-sectional area, the resistance associated with it can be appreciable. This is just the case for our ohmic metal ridge contact. This contact is nominally $0.25 \mu\text{m}$ thick, and less than $9 \mu\text{m}$ wide. This gives a unit resistance of roughly 50 Ohms/mm along the length of a ridge. For a typical device length of 0.2 to 1 mm , the voltage drop along the length of ridge would range from 0.5V to 2.5V assuming a 50 mA current driving the device. Since the device exhibits a diode electrical characteristic with a sharp turn-on around 0.6 V , this large voltage drop is problematic. Specifically, what happens is only regions near where the electrical probe contacts the ridge turn on and spontaneously emit light. This result is clearly shown in Figure 4-9 which displays the light output characteristic when the ridge laser was probed at two distinct locations along the length of the ohmic ridge contact; namely, one location near the facet closest to the photodetector and the other location several hundred μm down the length of the ridge away from the photodetector.

In both of these cases shown in Figure 4-9, lasing operation is not achieved. Instead, only spontaneous emission results. In essence, the voltage drop along the

¹⁰The chromium provides an extremely strong adhesion of the gold layer to the cyclotene planarization layer and to the top metal ridge.



(a) Zoomed-out cross-sectional view.



(b) Zoomed-in cross-sectional view.

Figure 4-8: Scanning electron micrographs of ridge lasers after the top large area electrical contact formation. Note that the nodules visible on the metal are likely a result of contamination that occurred due to the high pressure of several μ Torr during deposition.

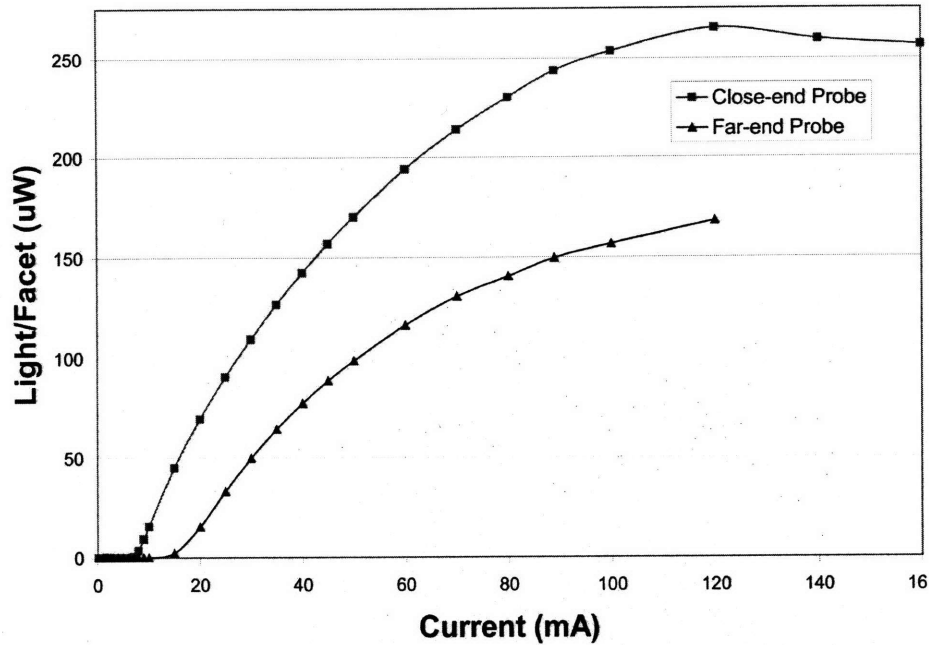


Figure 4-9: Experimental L-I characteristic of the edge-emitting laser, with $9 \mu\text{m}$ wide semiconductor ridge, probed at two distinct points on the ohmic ridge contact.

length of the ridge prevents the entire length of the device from being biased above threshold.

When a large area electrical contact is formed on top of ohmic ridge contact, the effective cross-sectional area of the metal line increases by about a factor of about thirty. With this factor of thirty reduction in the resistive drop along the length of the ridge ohmic contact, lasing operation can be achieved.

4.2.2 Back-Side Device Processing

Once the front-side device processing has been completed, the back-side processing is undertaken. The goals here are to first thin the substrate sufficiently in order that the device will cleave cleanly during the manual cleaving process. This is essential for mirror smooth facets. Then, once the substrate is thinned, the ohmic contact to the n-type bottom layer of the device will be formed. The basic back-side process flow is schematically shown in Figure 4-10.

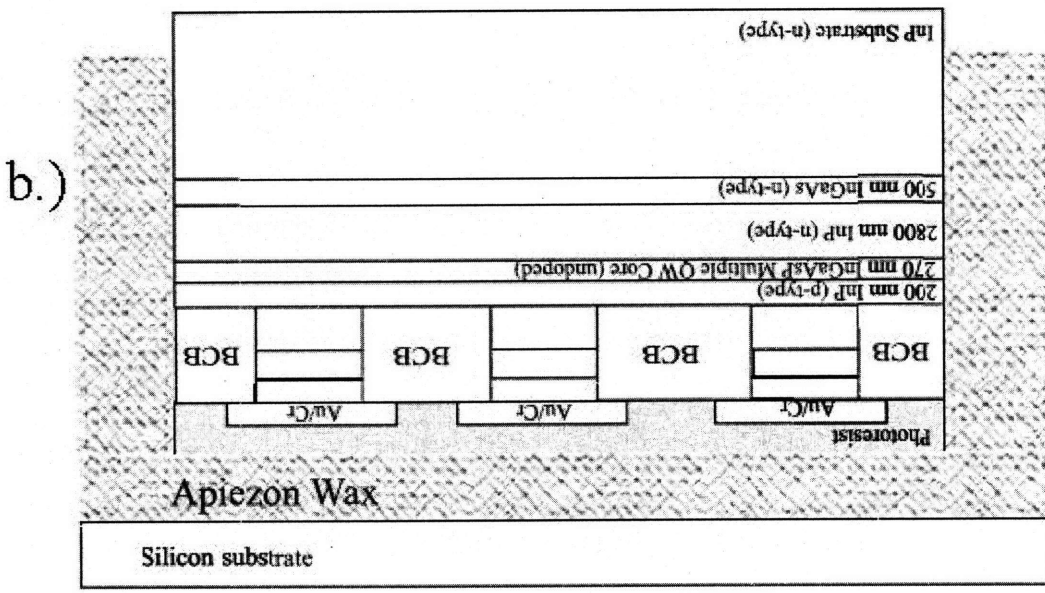
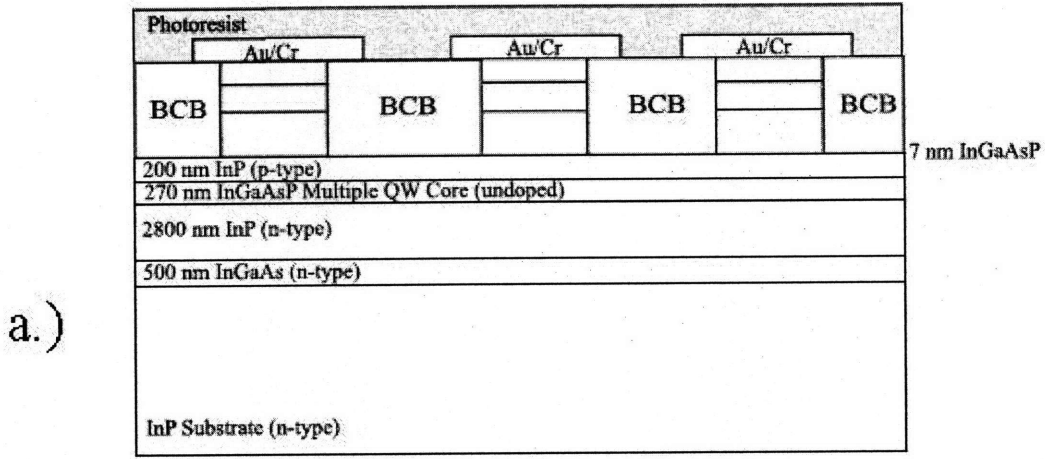


Figure 4-10: Conventionally cleaved edge-emitting laser back-side schematic process flow: a.) Front-side protective coat, b.) Substrate mounting. Continued on next page.

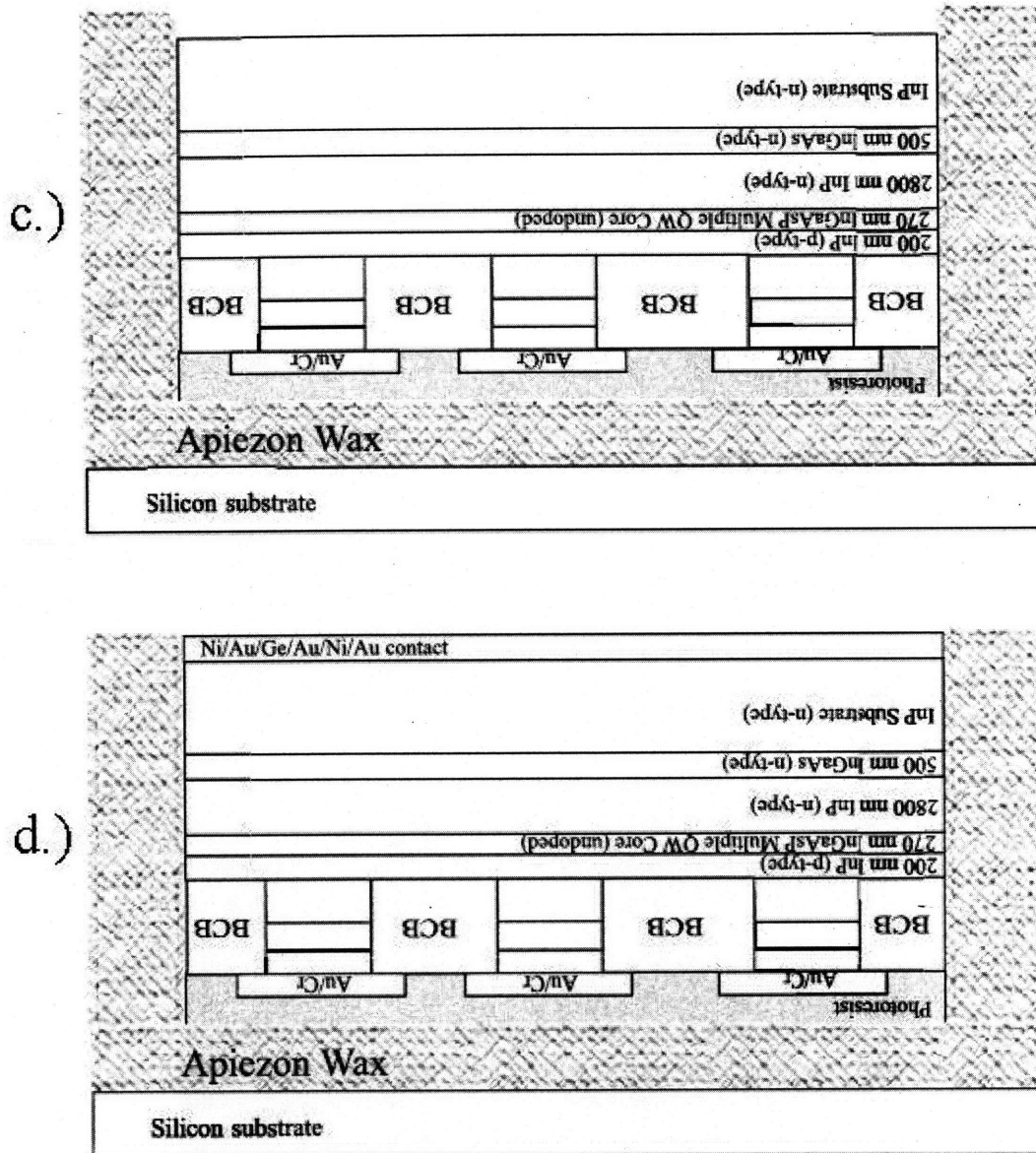


Figure 4-10: Conventionally cleaved edge-emitting laser backside schematic process flow continued: c.) Substrate thinning, d.) Backside ohmic contact formation. Continued on next page.

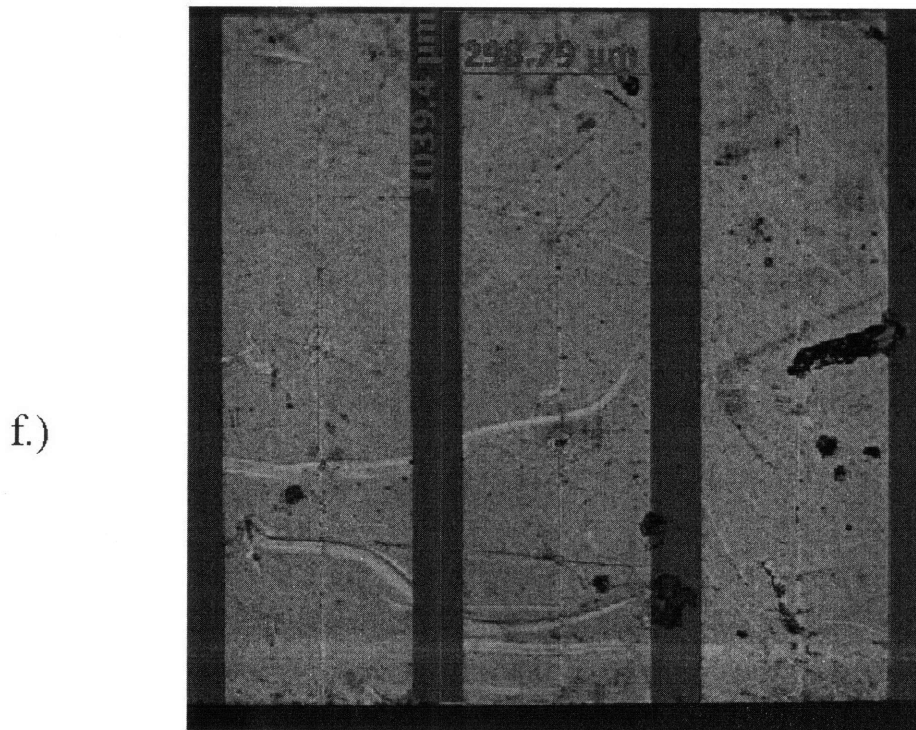
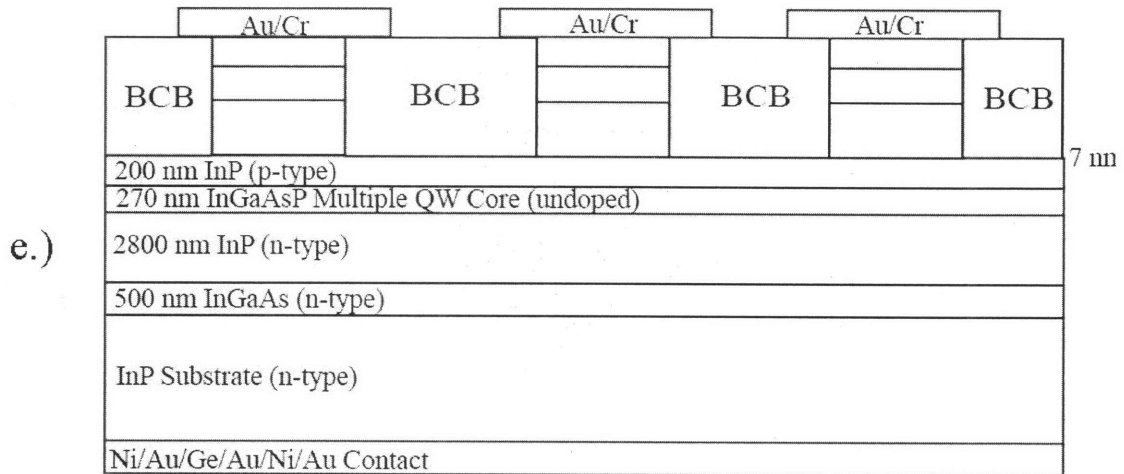


Figure 4-10: Conventionally cleaved edge-emitting laser backside schematic process flow continued: e.) Schematic cross-section of three finished devices, f.) Top-down photograph of three finished devices.

Substrate Thinning

At the start of this back-side process, the InP substrate is nominally 350 μm thick. The goal in this step is to remove approximately 100 to 150 μm of the substrate thickness. A number of approaches can be used to thin the substrate. Typically in industry and often reported in the literature, the substrate is chemo-mechanical polished on a flat mirror smooth chuck using fine grit. For the present process, though, it was decided to just wet etch the substrate using hydrochloric acid.

Before placing the wafer in the etch solution, it is imperative that the wafer front-side be protected from the etchant. To provide this protective layer, a thick photoresist (AZ 4620) is applied to the sample front-side. The sample is then mounted face down on a rigid silicon substrate using a Apiezon[®] wax adhesive. The sample backside is then wet etched at a nominal etch rate of 6 $\mu\text{m}/\text{minute}$.

Back-Side Ohmic Contact Formation

Once the substrate is thinned, the sample is placed in an e-beam evaporation chamber whereby an n-type ohmic metallization stack consisting of Ni(50 Å)/Au(100 Å)/Ge(600 Å)/Au(900 Å)/Ni(300 Å)/Au(1750 Å) is deposited. The nickel layers primarily act as adhesion layers. It is also suggested in the literature that the nickel layer enhances the diffusion of the Ge into the InP substrate [61]. Germanium is used to increase the doping in the n-type InGaAs layer, thus aiding ohmic contact formation. Specifically, during the subsequent annealing process, Ge will diffuse into the n-type InGaAs contact layer and increase the doping near the surface. Gold is used because of its extremely low contact resistance, which makes it an ideal material on which to electrically probe the device.

For the Ni/Au/Ge/Au/Ni/Au contact to a 350 μm thick n-type InP substrate, the results of the TLM measurements are shown in Figure 4-11. Both the as-deposited and annealed were found to be ohmic and had measured contact resistivities of approximately $2 \times 10^{-5} \Omega \text{ cm}^2$ and $1 \times 10^{-6} \Omega \text{ cm}^2$, respectively.

Once the ohmic metal deposition is complete, the sample is placed in a solvent

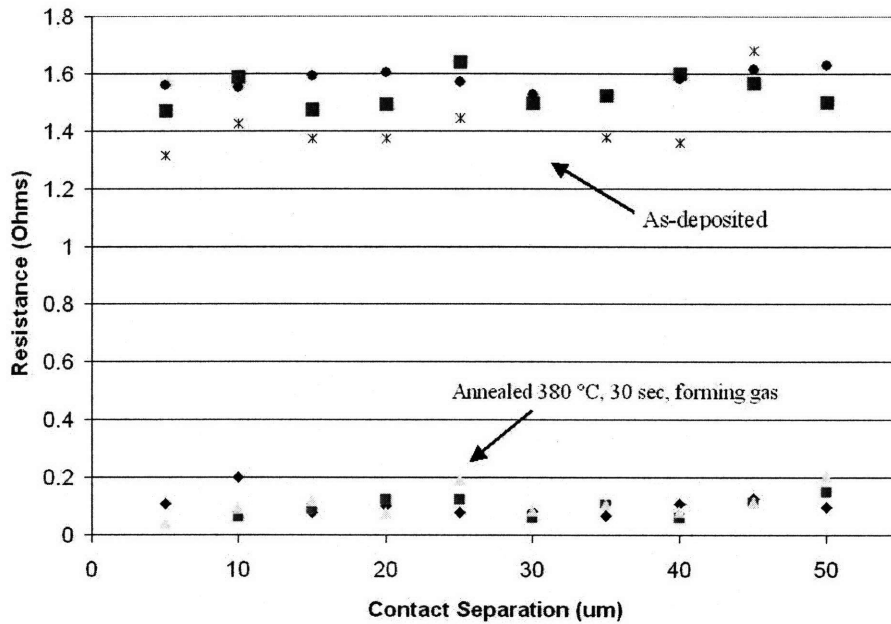


Figure 4-11: TLM of a Ni/Au/Ge/Au/Ni/Au contact to a 350 μ m thick n-type InP substrate

solution of trichloroethylene (TCE). This TCE solution quickly dissolves the black Apiezon[®] wax without affecting the device.

The laser is then manually cleaved, using a scribe, into shorter bars. These bars then undergo a short 30 second, rapid thermal anneal at 385 °C in a forming gas (95% N_2 , 5 % H_2) ambient. This anneal acts to lower the n-type ohmic contact resistance. At this point the laser is ready for testing. The results of this laser characterization are presented in Chapter 5.

4.3 Micro-Cleaved Ridge Laser Process Development

The micro-cleaved ridge laser process development builds on the processing knowledge gained from the conventionally cleaved ridge laser development. This process will now be detailed. In the course of describing this process, references will be frequently made to the the conventionally cleaved ridge laser process development.

4.3.1 Front-Side Processing

Top Ohmic Contact Formation

This ohmic contact process is similar to that of the conventionally cleaved ridge laser with one significant exception. Recall that for the conventionally cleaved laser, the Ti/Pt/Au contact to the semiconductor ridge was continuous along the length of the substrate. In this micro-cleaved ridge laser process, the Ti/Pt/Au ridge is discontinuous along the length of the substrate as is shown in Figure 4-12. Specifically, narrow regions where the metal is discontinuous correspond to notch regions in the micro-cleave enabling bar pattern (Figure 3-11) where the individual device facets will be formed by micro-cleaving.

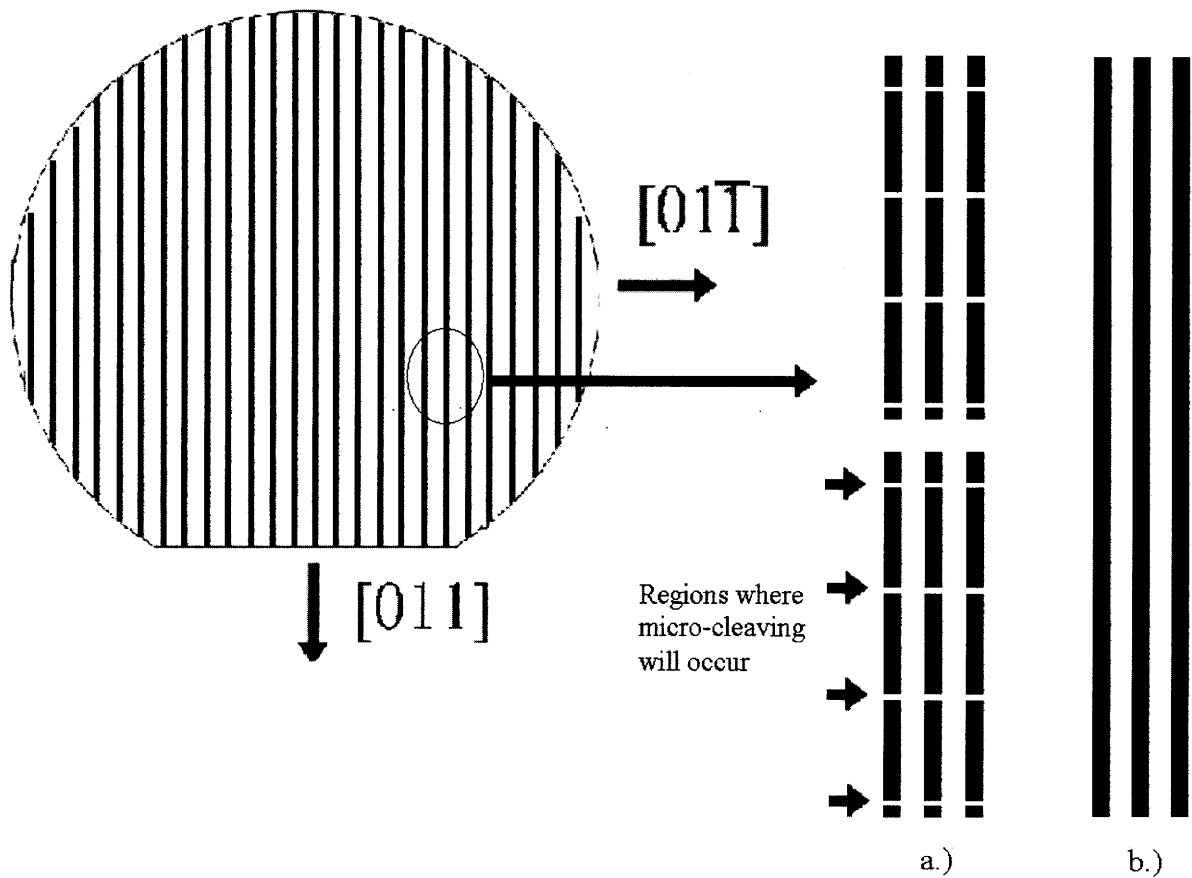


Figure 4-12: Schematic showing how the metal ohmic contact ridge pattern is aligned to the cleavage planes of the InP wafer: a.) Micro-cleaved ridge laser process, b.) Conventionally cleaved ridge laser process.

This discontinuity of the ridge metal is a key enabling element of the process since if a metal or any other non-crystalline material remains in the notch region between the individual devices, the devices will not easily micro-cleave. A typical micro-cleaved device where non-crystalline material was left in the notch region between devices is shown in Figure 4-13a.

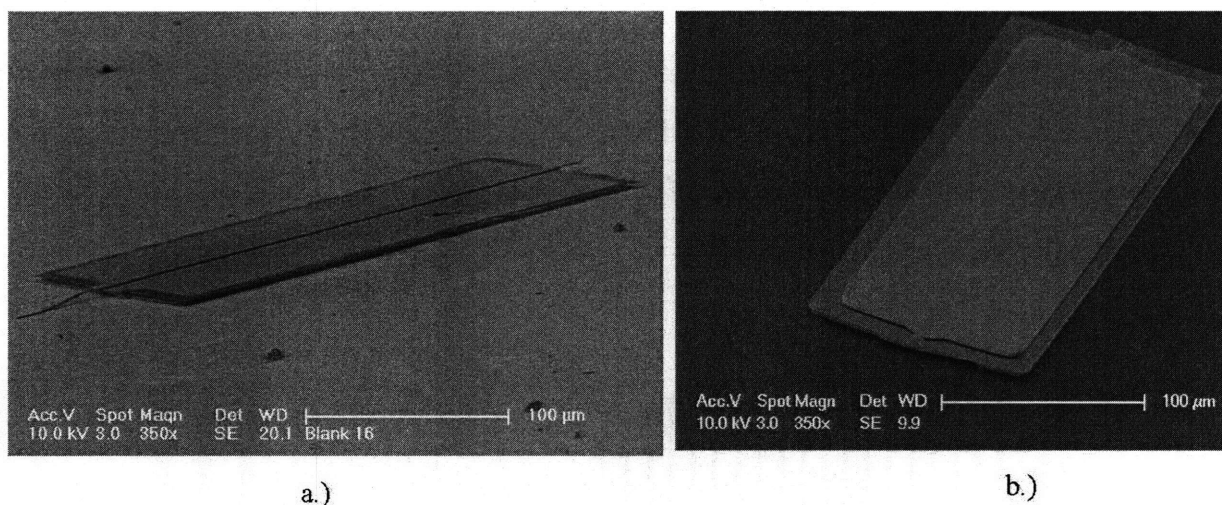


Figure 4-13: Scanning electron micrographs showing micro-cleaved devices where a.) the ohmic contact metal was continuous across multiple devices, b.) the ohmic contact metal was discontinuous in the notch regions between devices.

For characterizing the Ti/Pt/Au contacts to the 500 nm thick p-type InGaAs layer, the TLM measurement results are shown in Figure 4-14. Both the as-deposited and annealed (temperatures of 380 °C to 450 °C for 30 seconds) had a measured contact resistivity of approximately $6 \times 10^{-4} \Omega \text{ cm}^2$. In industry, p-type ohmic contacts often have an order of magnitude lower contact resistivity than achieved here. The lower quality contacts achieved here is likely a result of the rather high base and run pressures associated with the e-beam evaporation tool used. Typically, base pressures of no better than 10^{-6} torr are capable with this machine. Also, run pressures typically are no better than 2×10^{-6} torr. At these pressures, there can be quite a lot of particles incorporated in the deposited film. In industry, base pressures of 10^{-7} torr are standard.

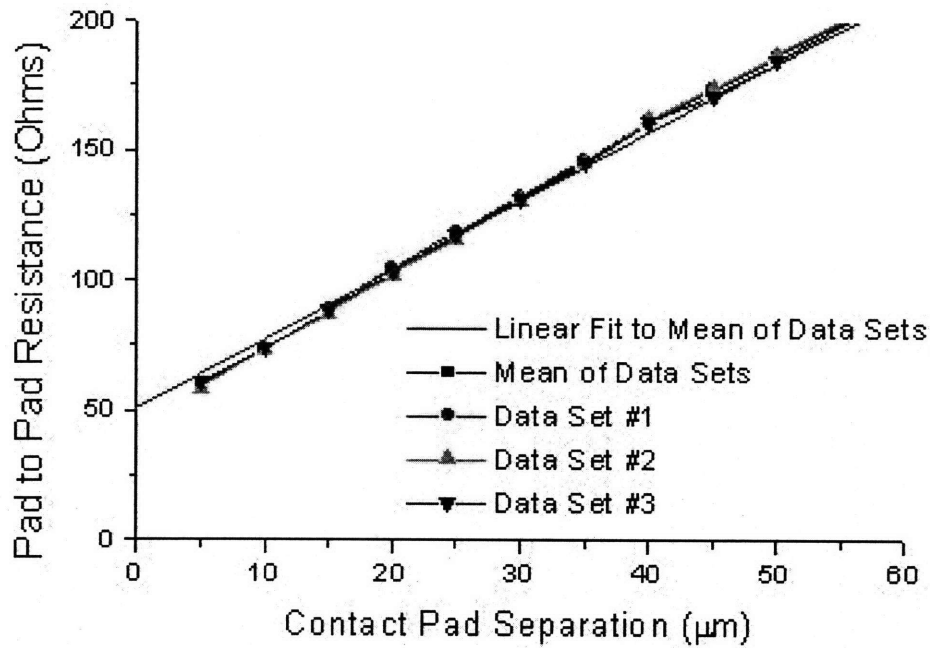


Figure 4-14: TLM of an annealed Ti/Pt/Au contact deposited on a 500 nm thick p-type InGaAs layer.

Semiconductor Ridge Etch

Since the ohmic contact layers are discontinuous in the notch regions between the devices, it is not possible to use the ohmic metal as a self-aligned mask for etching the semiconductor ridge. Therefore, a photoresist mask overlaying the ohmic metal and the notch region is patterned (Figure 4-15) and the semiconductor ridge is then etched using HCl.

Dielectric Layer Deposition Device Planarization

The Cyclotene spin coating and etch-back processes are identical to those explained for the conventionally cleaved ridge laser. It is important to note that for the micro-cleaved ridge laser process the Cyclotene is removed from the notch region between the devices. This follows from our experience that having non-crystalline material in the notch region seriously compromised the micro-cleaving process (Figure 4-13a).

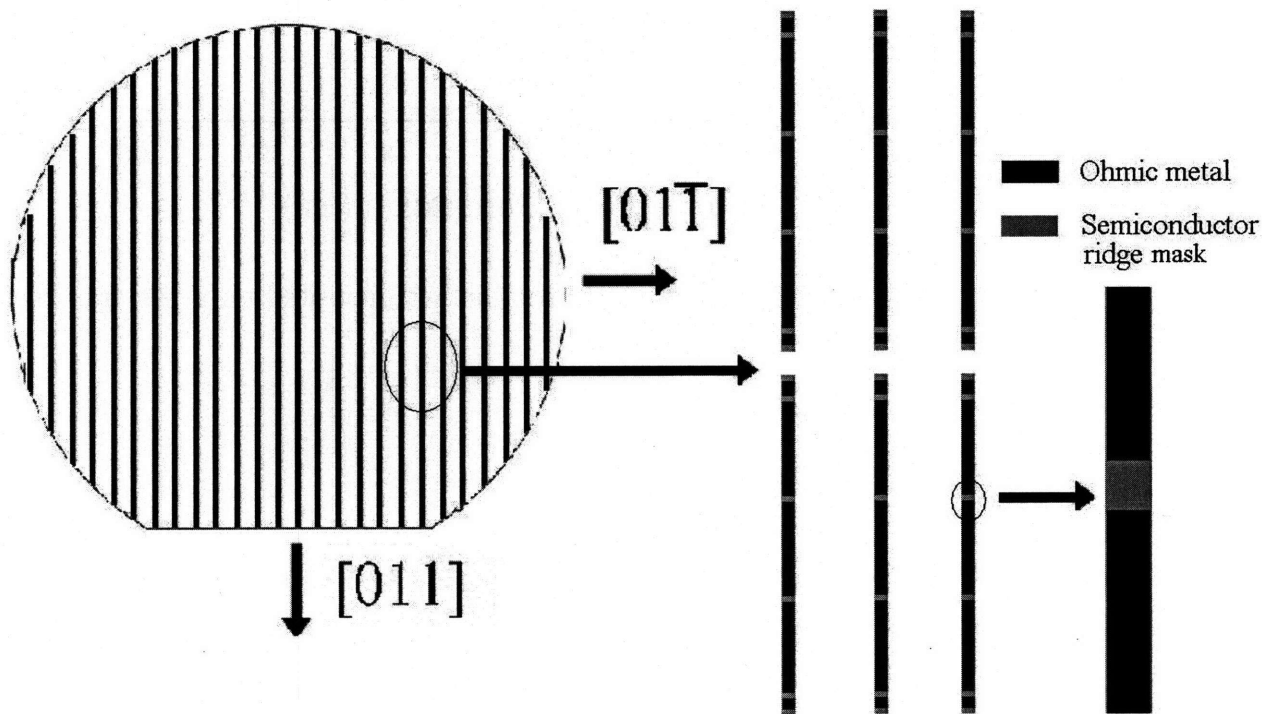


Figure 4-15: Schematic showing the semiconductor ridge pattern aligned over the ohmic contact.

Top-Side Large Area Electrical Contact Formation

Once the planarization and etch-back processes are completed, a large area electrical contact is formed on top of the ohmic ridge contact as was the case in the conventionally cleaved ridge laser process. The alignment of this large area electrical contact to the device structure is schematically shown in Figure 4-16.

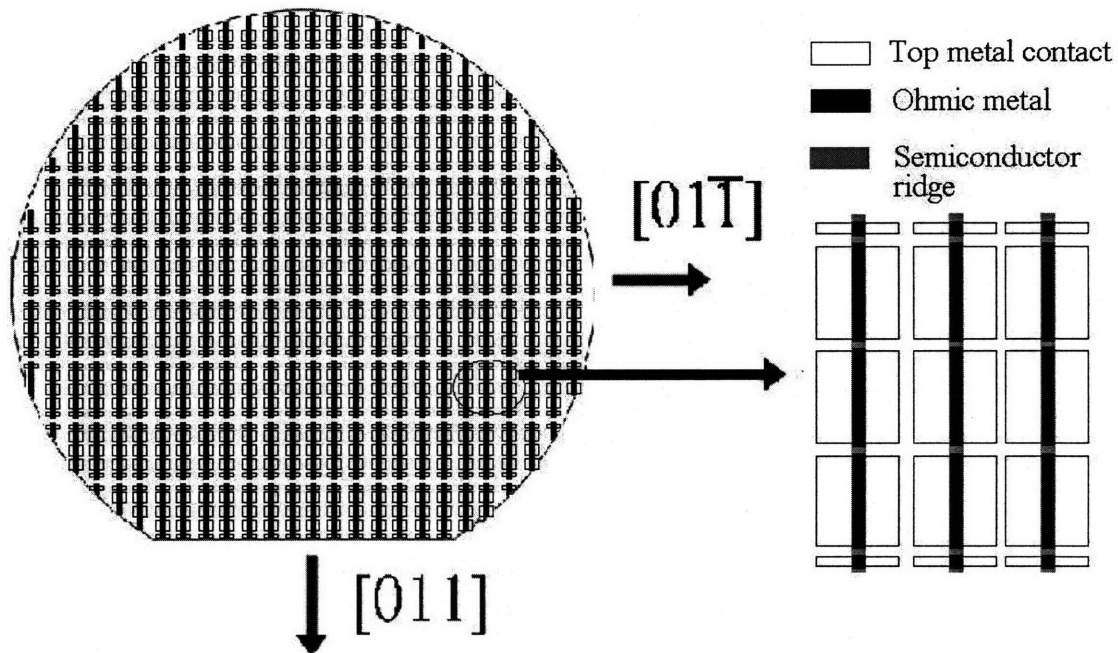


Figure 4-16: Schematic detailing how the top large area electrical contact is aligned over the ohmic ridge contact.

Micro-Cleave Pattern Transfer

With the semiconductor ridge formed, the device planarized, and the low resistance contacts formed to the top of the device, the next step is to pattern the device into the micro-cleaving enabling bar pattern (Figure 4-17). This process involves the anisotropic dry etching of the semiconductor. Specifically, the etching is carried out at Lincoln Laboratory with the assistance of Jason Plant using a SAMCO Inductively Coupled Plasma (ICP) Etching System (Model RIE 200).

This process first involves the sputter deposition of a thick (greater than 300 nm)

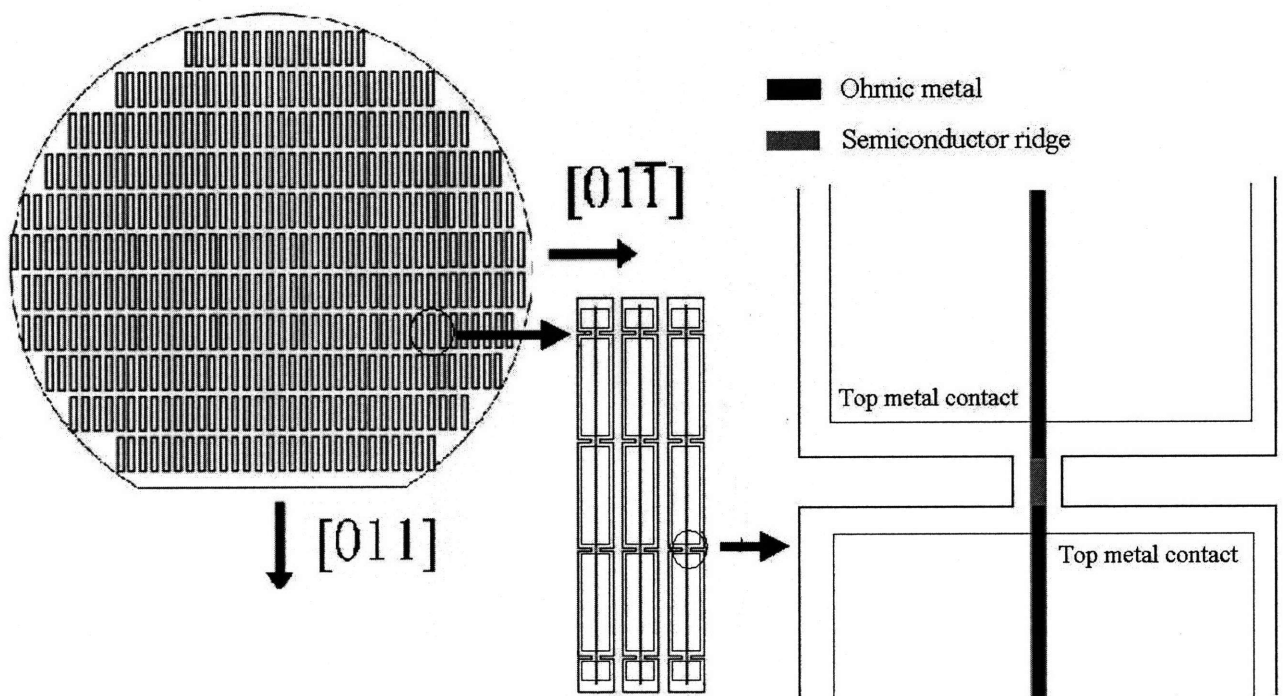


Figure 4-17: Schematic showing the alignment of the micro-cleave bar pattern to the semiconductor ridge, the ohmic metal ridge contact, and the top large area electrical contact.

film of SiO_2 . This SiO_2 hard-mask is then patterned by wet chemical etching (i.e., buffered hydrofluoric acid) into the micro-cleave bar pattern (Figure 4-18). As shown, care is taken to align this bar pattern over the semiconductor ridge, the ohmic ridge contact, and the large area electrical contact, which at this stage of the process are already formed on the wafer. It is also important to point out that these bars are also aligned with the semiconductor cleavage planes. This alignment is necessary for the micro-cleaving of the devices to ultimately be successful.

A schematic cross-section of the device structure both before and after the dry etch process are shown in Figure 4-18. As displayed, the semiconductor etch proceeds to a depth of roughly 3500 nm, and stops in the middle of this InGaAs layer. It should be noted that the dry etch chemistry is not selective over InGaAs¹¹.

The chemistry of the dry etch process is silicon tetrachloride ($SiCl_4$) /chlorine (Cl_2)/Argon (Ar) with flows of 0.5 sccm/0.5 sccm/10.0 sccm. The other operating parameters of this process include a plasma generating power of 250 W, a bias power of 250 W, and a substrate temperature of 220 °C. With these process parameters, the InGaAsP/InP semiconductor etch proceeds at a rate of approximately 180 to 250 nm/minute while etching the SiO_2 hardmask at a rate of roughly 30 nm/minute. SEMs of the etching results achieved are shown in Figure 4-19.

Once this etching sequence is complete, any remnants of the SiO_2 hard-mask are removed with buffered oxide etch.

In the development of this micro-cleaved bar pattern etch, a number of other etching techniques and chemistries were vigorously explored. For instance, wet etch solutions consisting of HCl/H_3PO_4 were attempted. However, they proved to not be as selective as required. Moreover, an etch used to selectively etch the InGaAs layers proved to be incompatible with the Cyclotene planarization layers.

Reactive ion etching using a methane (CH_4) / hydrogen (H_2) chemistry was attempted as well. With this chemistry, a nickel hard etch mask was chosen. Unfortunately, significant sputtering of the hardmask occurred which resulted in severe

¹¹The reason it is desirable to etch some of this bottom InGaAs layer is related to the back-side photolithography process. This is described later in this chapter in Section 4.3.2 Back-Side Processing, Sub-Section Back-Side Ohmic Contact Formation.

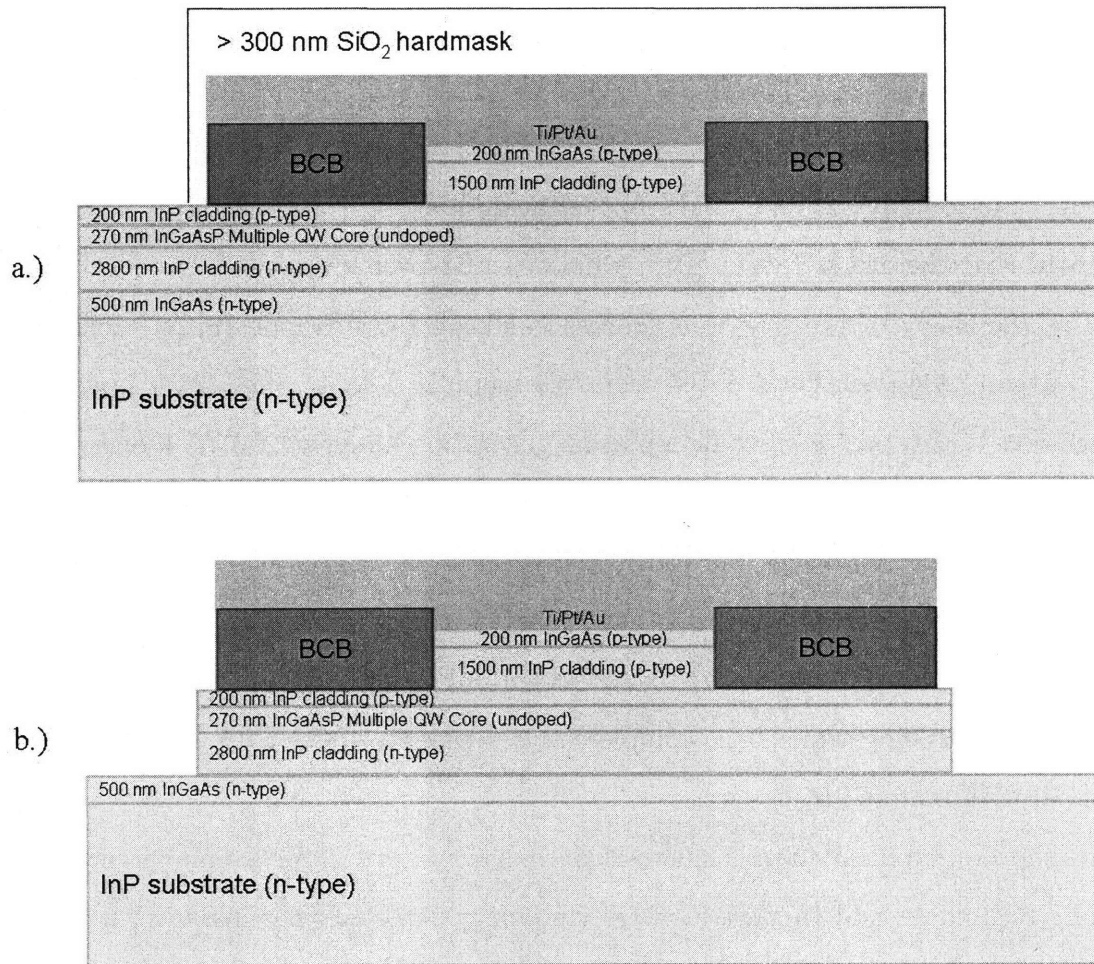


Figure 4-18: Schematic cross-section of the device a.) prior to dry etching, b.) after dry etching and SiO_2 hardmask removal.

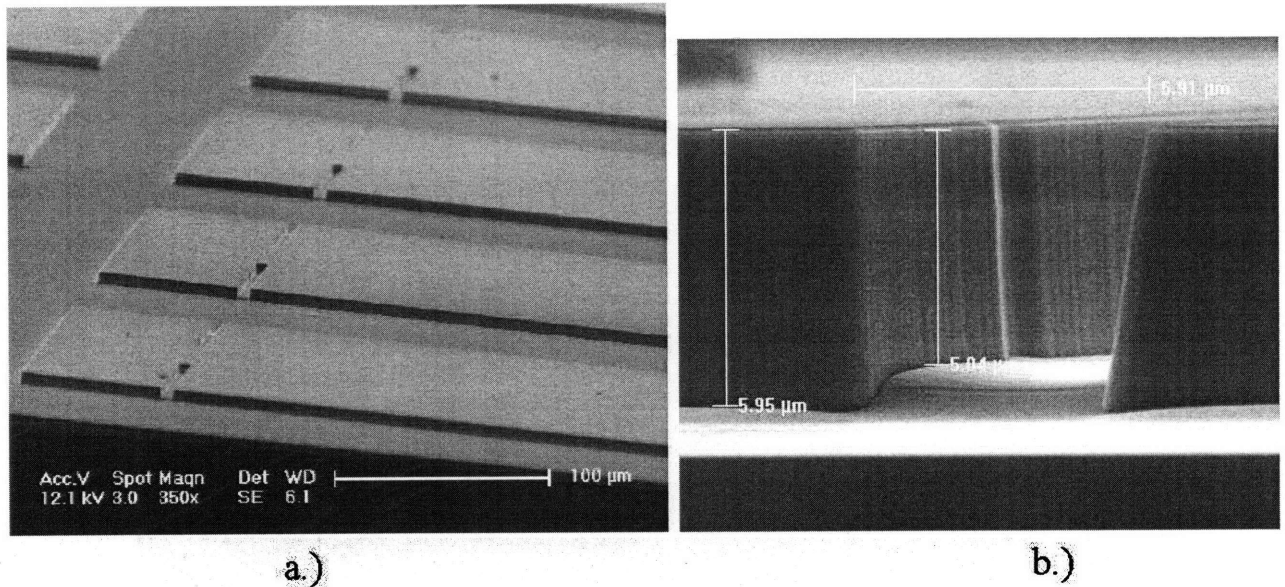


Figure 4-19: Scanning electron micrographs of: a.) An array of micro-cleave enabling bar patterns formed by ICP dry etching on the front-side of an InP substrate, and b.) Zoomed-in SEM of one notch. Note, these images are of etches on dummy InP material and not the actual laser epitaxial material.

micro-masking, as Figure 4-20 illustrates.

4.3.2 Back-Side Processing

With the front-side processing completed, the semiconductor substrate must be thinned and the back-side ohmic contacts need to be formed to every individual laser bar. This process development will now be detailed.

Substrate Thinning to Etch Stop Layer

The back-side process starts with the coating of the wafer front-side with a protective layer that will shield the devices from the harsh chemicals and processes used to remove the substrate. The sample is then mounted front-side down on a rigid substrate. The substrate is removed using a selective wet etch chemistry that stops in the middle of the 500 nm n-type InGaAs epilayer.

Whereas the conventionally cleaved ridge laser substrate thinning process was accomplished fairly straightforwardly using a thick photoresist protection layer and



Figure 4-20: Scanning electron micrograph of an array of circular InP-based diodes patterned by reactive ion etching using a methane/hydrogen chemistry.

Apiezon[®] wax adhesive layer to a rigid silicon substrate, the back-side process for the micro-cleaved ridge laser is significantly more challenging. For the micro-cleaved ridge laser process, the difficulty lies in the requirement that photolithography must be performed on the device back-side. Recall, that for the conventionally cleaved ridge laser a blanket ohmic contact deposition was performed over the entire wafer back-side. Thus, no photolithography was necessary and the process was simplified considerably.

Five different sets of materials were evaluated as protective/adhesive layers in our back-side process development. These materials are listed in Table 4-1 along with their performance in terms of four performance criteria; namely, are they resistant to hydrochloric acid etches, can they be easily removed, are they resistant to solvents such as acetone and methanol, and finally will they survive a metal lift-off process.

Material	Etch Resist.	Easily Removed	Solvent Resist.	Lift-off Compliant
Photoresist	Limited	Yes	No	No
Brewer ProTek™	Yes	No	Yes	N/A
Apiezon® Wax	Yes	No	Limited	No
Photoresist+Apiezon®	Yes	Yes	No	No
Brewer WaferBOND™	Yes	Yes	Yes	Yes

Table 4-1 Materials experimented with (listed in order of experimentation) in pursuit of a protective layer/adhesive layer for the micro-cleaved ridge laser back-side process.

Looking at Table 4-1, one begins to appreciate the issues at play in developing the micro-cleaved device back-side process. Photoresist was a crude choice of a back-side process protection layer because it does not hold up well to the harsh acids used to remove the InP substrate. The Brewer Science ProTek™ polymer, was much more resistant to the harsh semiconductor chemical etching; however, it was very challenging to ultimately remove the polymer from the devices as is shown in Figure 4-21.

As was the case with the ProTek™ polymer process, the Apiezon® wax holds up well to the semiconductor etch chemistry, but it is difficult to remove from the individual devices as is shown in Figure 4-22.

With the durability of the Apiezon® wax to the harsh chemicals, and the ease of removal of the photoresist, a process was developed that utilized both layers in the back-side process. This also became the workhorse process for the conventionally cleaved ridge laser process. This process looked as though it would also work very well for the micro-cleaved edge emitting laser process. It was possible to remove the semiconductor substrate completely without attacking the protective polymer or the wafer front-side. However, when it came to the back-side photolithography process¹², a sufficient amount of height variation was present on the sample backside making it difficult to pattern the desired features, as Figure 4-23 shows.

¹²The process was tweaked to utilize lower temperature bakes and the contact lithography process was performed as delicately as possible to minimize the likelihood of poor results.

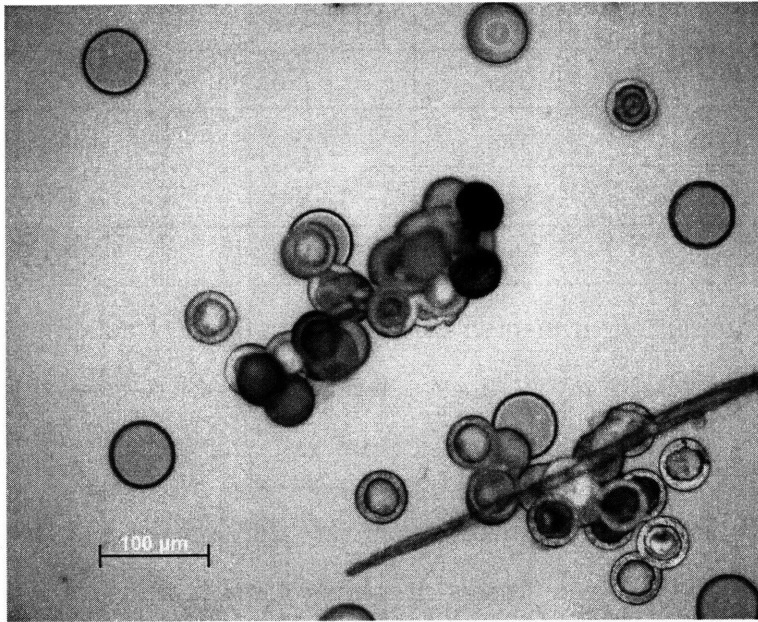


Figure 4-21: Pictorial results of the Brewer Science ProTek™ polymer process where arrays of heterostructure diode pills clumped together.

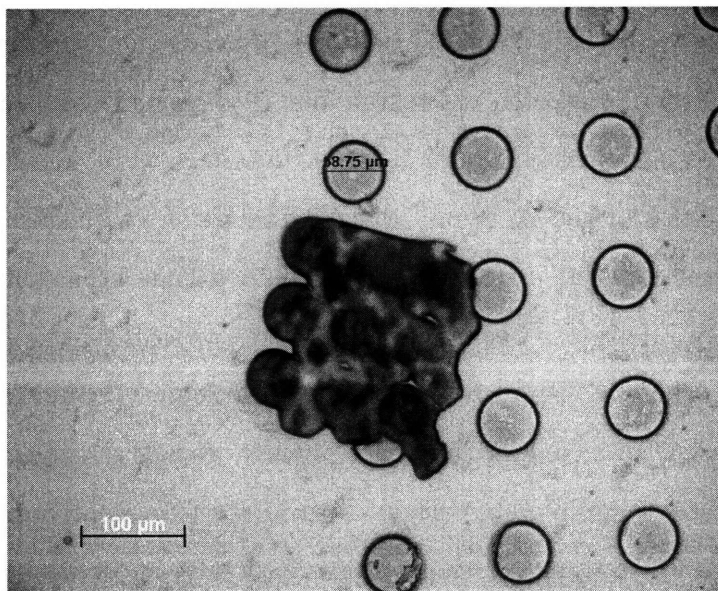


Figure 4-22: Pictorial results of Apiezon® wax process where arrays of heterostructure diode pills clumped together.

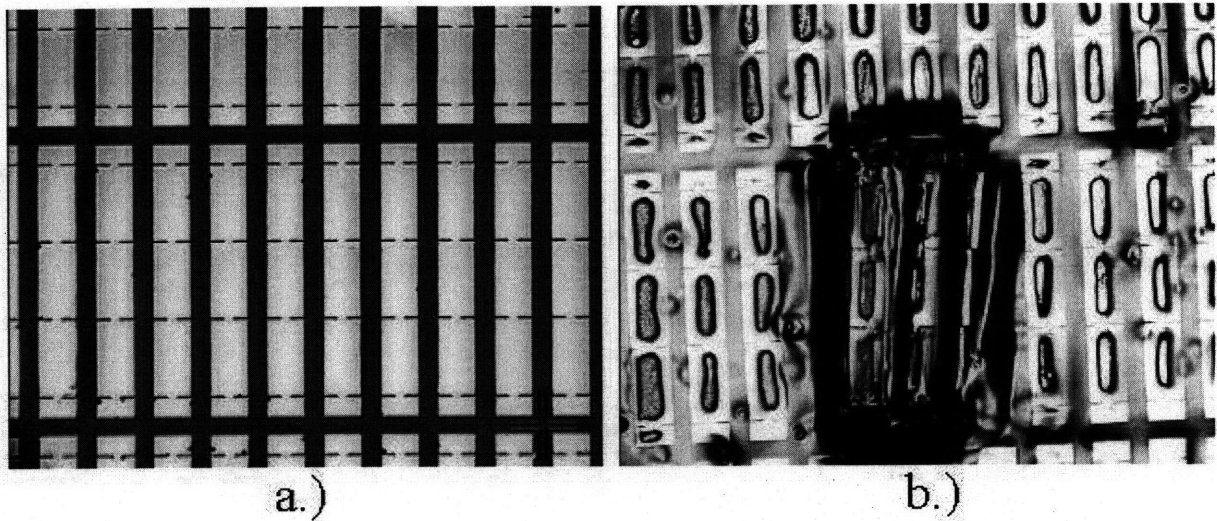


Figure 4-23: Pictorial results of the Apiezon[®] wax/photoresist process a.) Post-substrate removal, b.) Post back-side photolithography.

To recount the process travails, during the alignment phase of the photolithography process, the wafer was brought just out of contact with the mask. During the alignment of the substrate to the mask pattern, it became apparent that areas of the sample were at different heights. As the sample chuck was micro-positioned, the mask was still in contact with some unusually tall areas of the substrate. Thus, a number of bars mounted with the PR/wax began to move as they were pressed against the mask.

It is important to point out that even if it were possible to obtain an extremely flat wafer prior to the contact lithography process, this Apiezon[®] wax/photoresist process would still be imperfect. The imperfection is due to the fact that the wax/photoresist process is not impervious to solvents like acetone or processes like oxygen plasma ashing which are commonly used to strip photoresist. Basically, if a problem occurred during the lithography step, the photoresist could not be removed without completely releasing all of the ridge laser bars prematurely.

Finally, after much experimentation, a material was found that satisfied all the criteria listed in Table 4-1. This material, Brewer Science WaferBOND[™], is a proprietary polymer, that is extremely resistant to acids, bases, and most solvents. It

can be applied to a thickness of greater than $10\ \mu\text{m}$ in just one spin coat, and can withstand process temperatures as high as $180\ ^\circ\text{C}$.

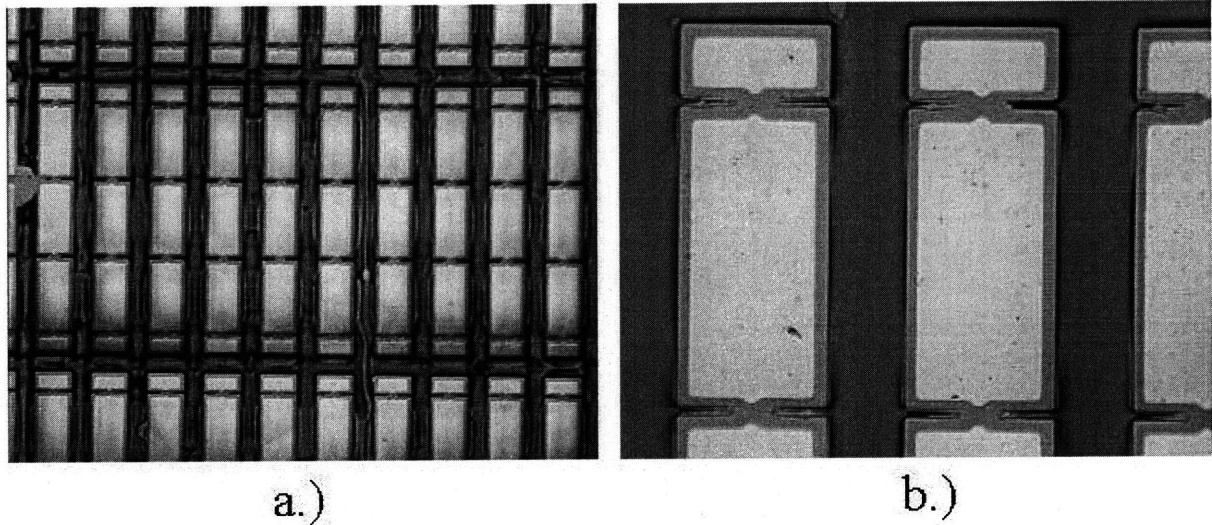
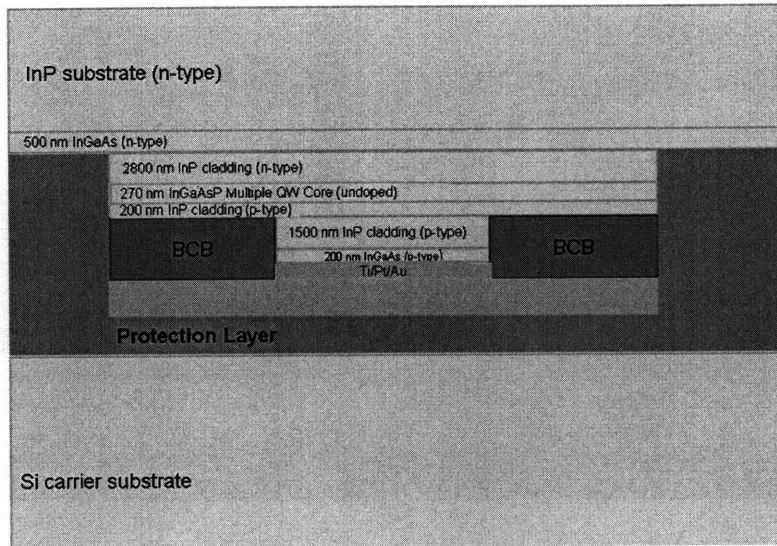


Figure 4-24: Pictorial results of the WaferBONDTM process post back-side metallization and lift-off processing, a.) Zoomed-out image, b.) Zoomed-in image. Note that there appears to be some residue in the notch regions. What looks like residue is, in fact, InGaAs. Since this thin InGaAs layer aids the ohmic contact formation, it is etched off only after the liftoff process is complete. This way the ohmic metallization is used as a self-aligned etch mask.

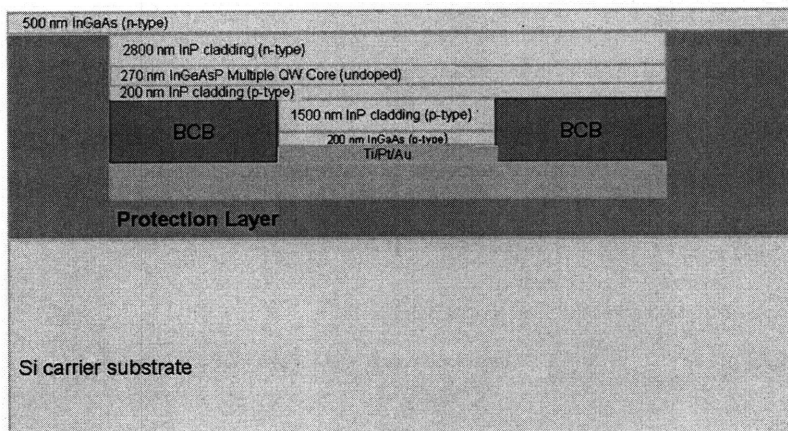
Back-Side Ohmic Contact Formation

Using the Brewer Science WaferBONDTM material as our protection layer/adhesive to a silicon wafer, back-side photolithography was a relatively straightforward process. Figure 4-25 schematically describes the process.

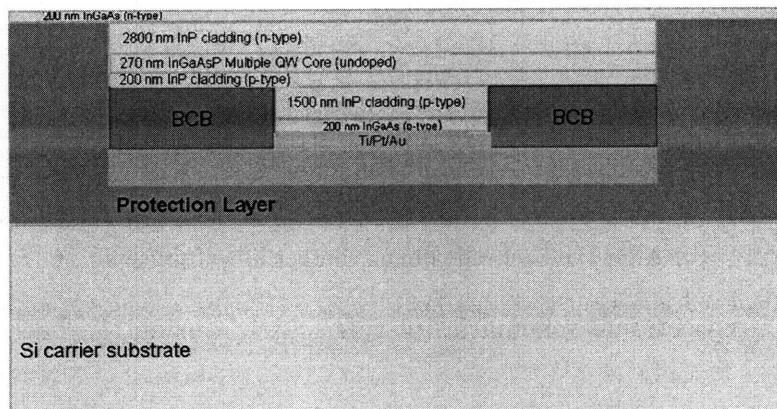
First, the sample is placed in a solution of the Brewer Science WaferBONDTM remover proprietary solvent for a quick twenty second dip. This step removes any WaferBONDTM from the edge or back-side of the substrate. Next, the substrate is chemically removed in concentrated HCl. Then, the n-type InGaAs layer is etched slightly, with roughly 300 nm removed. Note, care is taken to not completely remove the InGaAs layer. The development of this InGaAs etching procedure resulted from the need to align our photomask to the laser bars. If the InGaAs layer was etched



(a) After the front-side protection and wafer bonding steps.

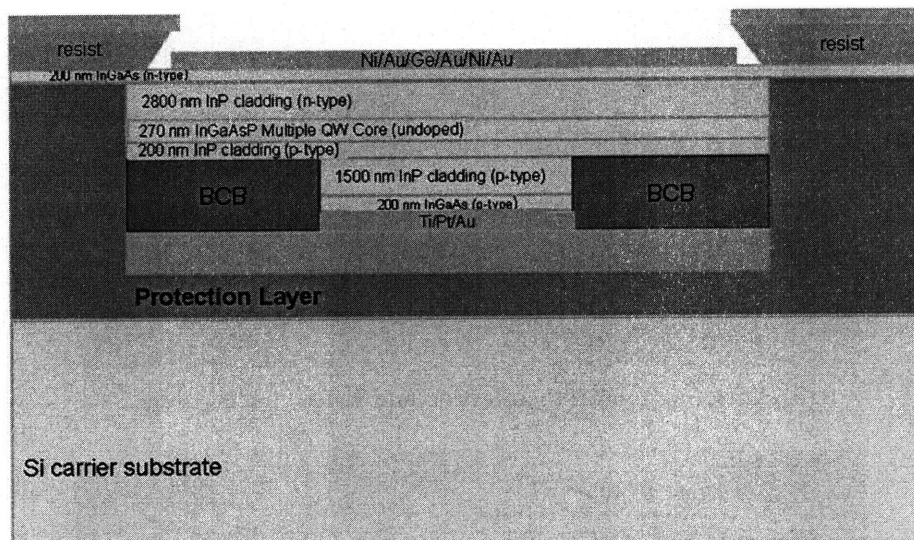


(b) After the InP substrate removal process.

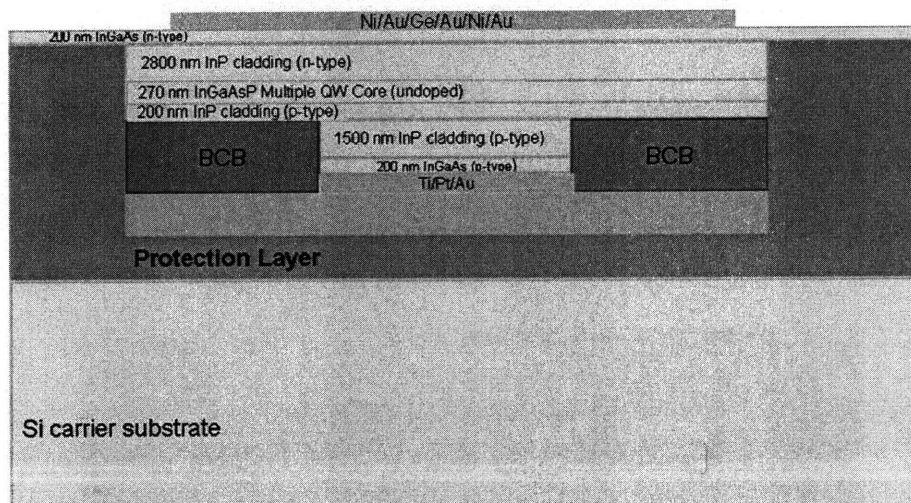


(c) After the InGaAs thinning step.

Figure 4-25: Cross-sectional schematics of ridge lasers during the back-side process.



(a) After the back-side photolithography step.



(b) After the back-side ohmic contact lift-off process.

Figure 4-26: Cross-sectional schematics of ridge lasers during the back-side process continued.

slightly, it was possible to punch through the InGaAs in the areas surrounding the bars, while still keeping a thin InGaAs layer on the bars themselves. The InGaAs around the bars is thinner than the InGaAs over the bars because during the front-side bar patterning process, the bottom InGaAs layer was etched halfway. This thin InGaAs layer on the bars should ultimately lead to lower contact resistances than if it was completely removed because of the properties of InGaAs mentioned earlier.

Now, negative photoresist (with sloped sidewalls to aid the lift-off process) is spun on the sample, the photomask is aligned, and the pattern is exposed and developed. At this time, the back-side ohmic metallization Ni(50 Å)/Au(100 Å)/Ge(600 Å)/Au(900 Å)/Ni(300 Å)/Au(1750 Å) is performed in an e-beam deposition system. The sample is then placed in an acetone or Microstrip 2001 solution; whereby, the metal is lifted off the sample, remaining only on the laser bar back-side as is shown in Figure 4-26.

The TLM results are shown in Figure 4-27 and 4-28 for the Ni/Au/Ge/Au/Ni/Au contact to the 500 nm thick n-type InGaAs layer. The as-deposited contacts had a measured contact resistivity of approximately $2 \times 10^{-5} \Omega \text{ cm}^2$, while the annealed contacts had a measured contact resistivity of approximately $x 10^{-5} \Omega \text{ cm}^2$.¹³

Platelet Release and Collection

With the back-side metallization process complete, the WaferBONDTM layer is then dissolved using the Brewer Science WaferBONDTM remover proprietary solvent. This process releases the long bars onto a teflon substrate as is shown in Figure 4-29¹⁴.

With care taken not to disturb the bars, the Brewer Science solvent is removed from the glassware containing the teflon substrate and bars. Next, the bars are rinsed off. This cleaning process involves filling the glassware with acetone, and the acetone

¹³Ohmic contacts to n-type InP are easier to form than ohmic contacts to p-type InP. Primarily this is due to the lower Schottky barrier height for a wide variety of metals on n-InP which arises because of Fermi level pinning[84]. One way to help form the p-type ohmic contact is to insert a lattice matched low energy bandgap p-type layer, InGaAs, on top of the p-type InP.

¹⁴Early experimentation was done collecting micro-cleaved devices on smooth silicon substrates instead of teflon. Unfortunately, when the fluid surrounding the micro-cleaved platelets evaporated, the platelets were strongly attached to the silicon substrate. The roughness of a teflon substrate prevents this strong bonding and allows for easy manipulation of the platelets.

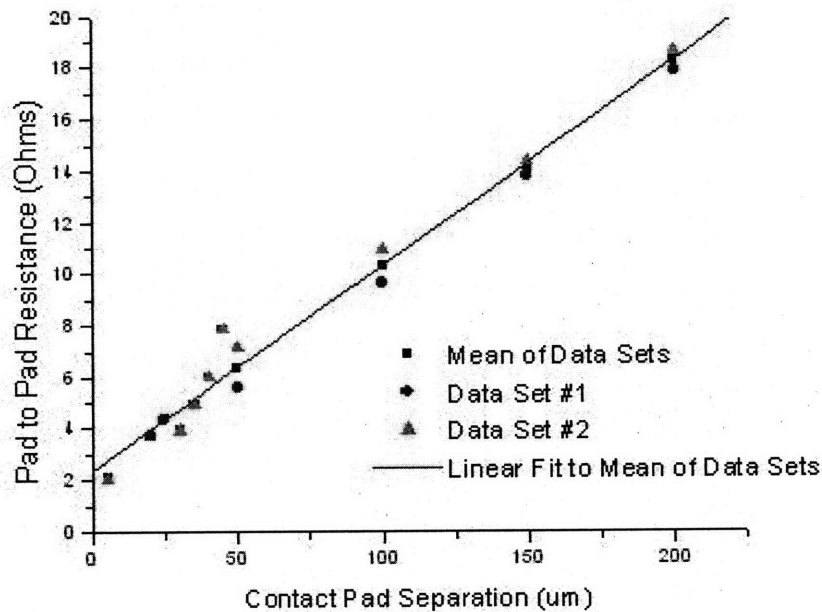


Figure 4-27: TLM of an as-deposited Ni/Au/Ge/Au/Ni/Au contact deposited on a 500 nm thick n-type InGaAs layer.

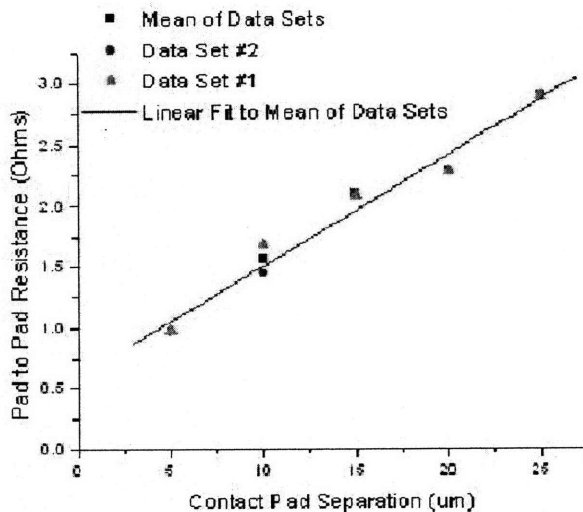
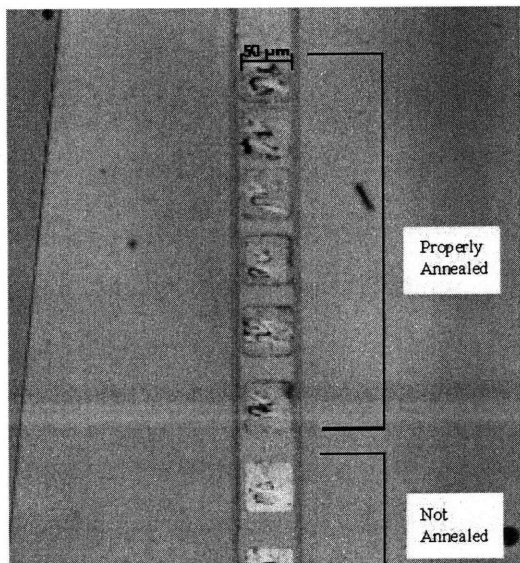


Figure 4-28: a.) Photo of contact pattern on InGaAs showing the importance of a flat surface when annealing or activating the contacts. b.) TLM of an annealed Ni/Au/Ge/Au/Ni/Au contact deposited on a 500 nm thick n-type InGaAs layer.

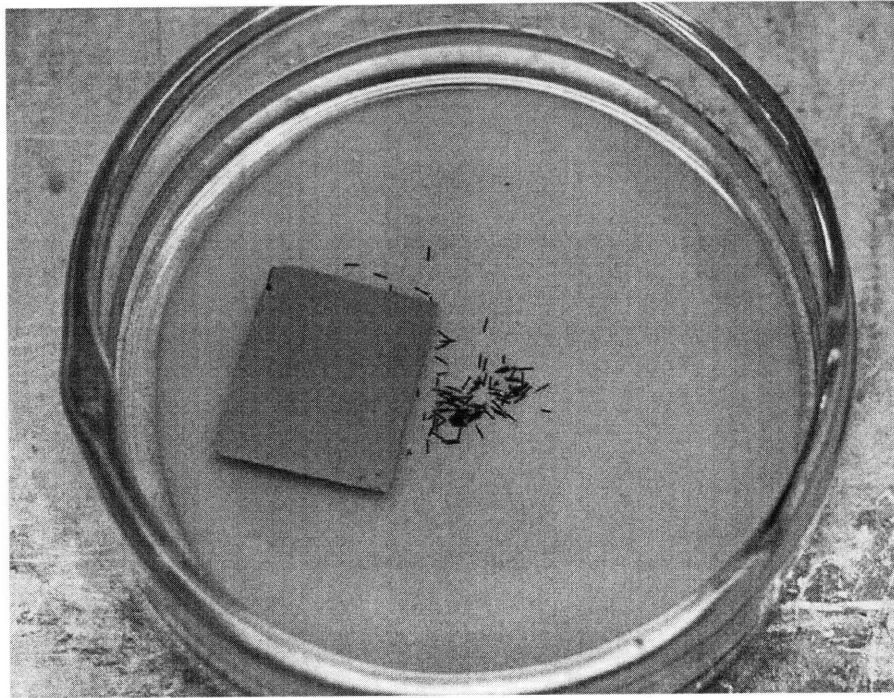


Figure 4-29: Pictorial results of the laser bars released in solution.

is decanted. This acetone rinse is done twice. Then, the glassware is filled with methanol, and the methanol is decanted. This methanol rinsing is repeated. Finally, the glassware is filled with isopropanol.

This cleaning procedure to remove the remnants of the Brewer Science WaferBond removing solvent is vital to the long-term quality of the devices. Figure 4-30 shows that if trace residues of the solvent are left on the device, the top large area metal contact is easily scratched off during electrical probing due to the weakened state of the underlying BCB.

In light of the dangers that the WaferBond solvent poses to the long-term device quality, great care is taken to flush the WaferBond removing solvent from the devices using treatments of acetone, methanol, and isopropanol. After cleaning, the micro-cleaved samples are baked out at a temperature of 115 °C for at least thirty minutes.

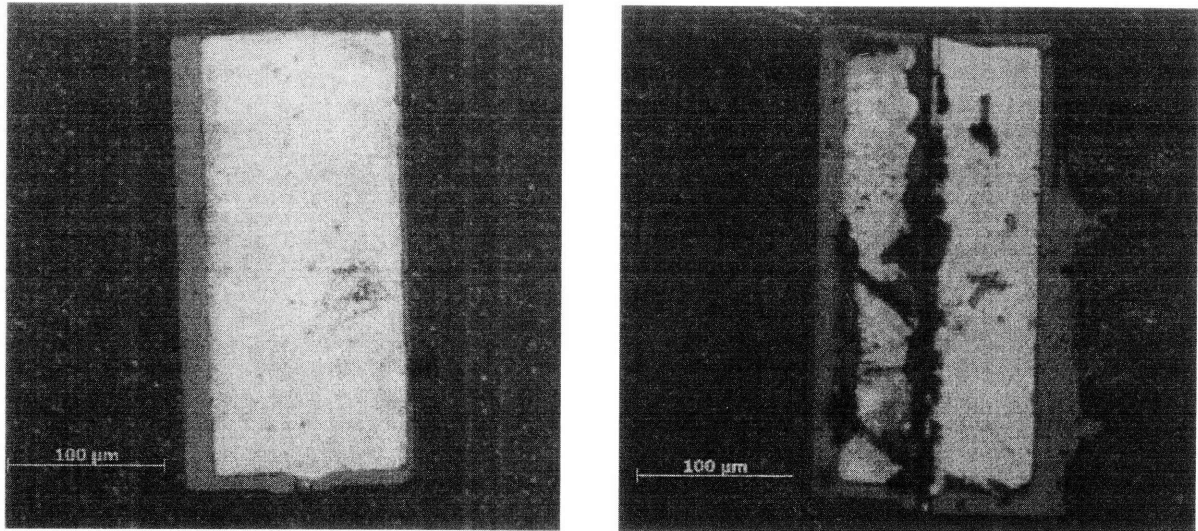


Figure 4-30: Top-down image of typical micro-cleaved ridge laser before and after electrical probing.

Micro-Cleaving

With the bars resting on a teflon substrate in a glass container filled with isopropanol, the bars are agitated ultrasonically causing them to preferentially cleave in the notch region. An SEM of a collection of micro-cleaved dummy and real devices, as well as long uncleaved bars is shown in Figure 4-31.

The micro-cleaved devices have characteristically smooth facets as is shown in Figure 4-32.

An SEM of a micro-cleaved facet showing the various layers of insulators and metals is shown in Figure 4-33.

It should be noted that the micro-cleaving process does not always work perfectly. Figure 4-34 shows some common failure mechanisms seen in the course of developing the process. The platelet in the lower half of the picture actually cleaved along the semiconductor ridge (with metal contact) in addition to cleaving in the notch region. It is evident from the large micro-cleaved platelet in the upper half of the picture that the quality of this sample was further compromised by non-crystalline material which was left in the notch region.

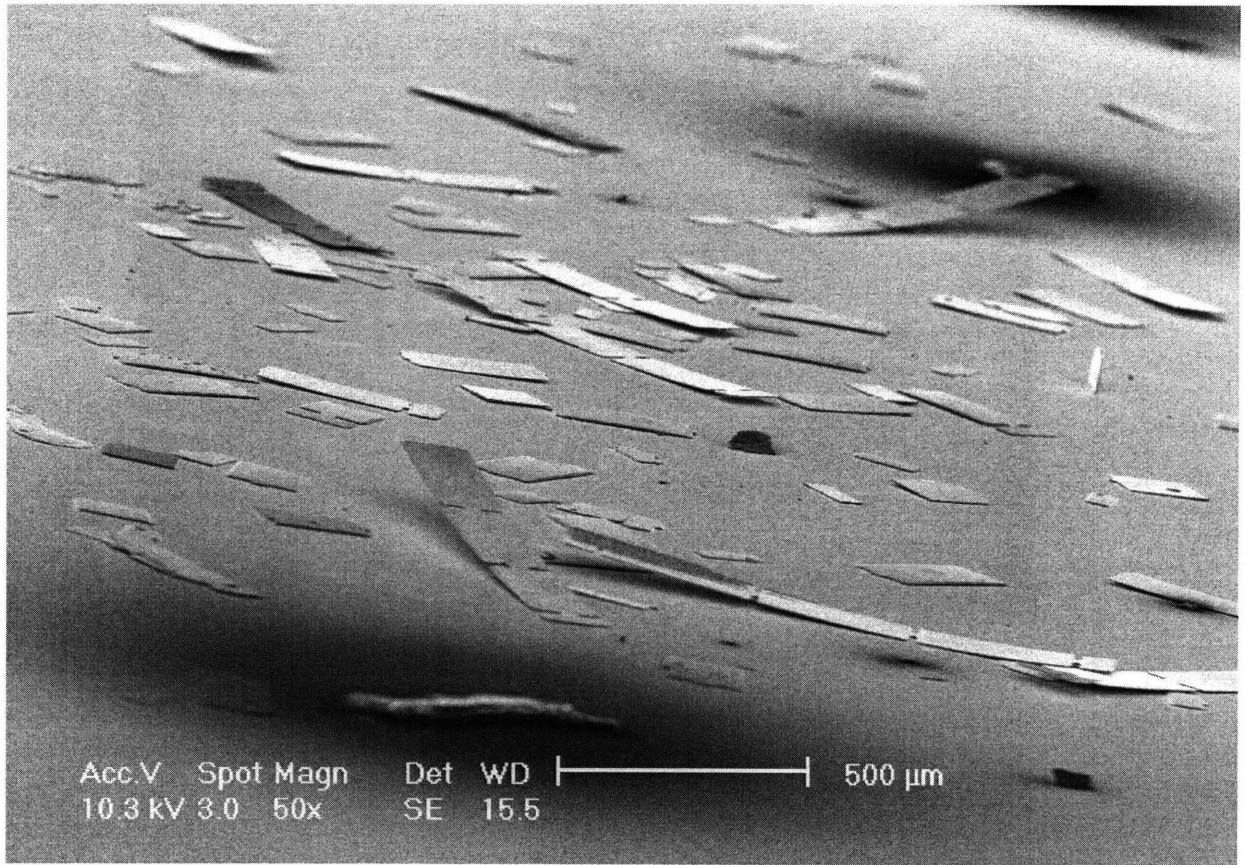


Figure 4-31: Scanning electron micrograph of a large quantity of micro-cleaved lasers, micro-cleaved dummy devices, as well as long uncles bars.

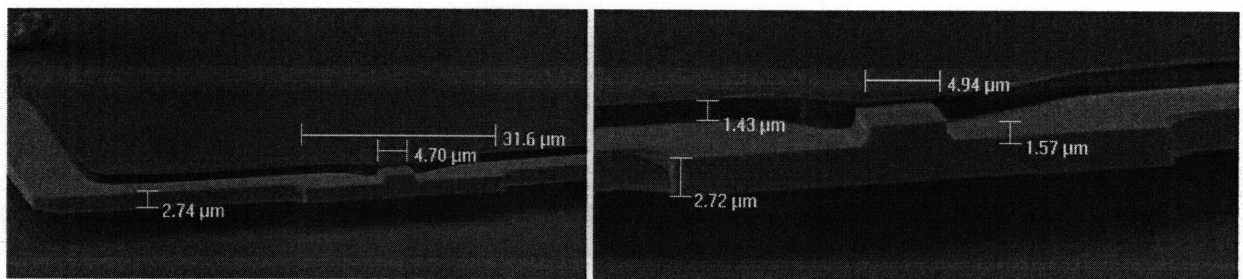


Figure 4-32: Scanning electron micrographs of a typical facet achieved with the micro-cleaving process, a.) zoomed-out image, b.) zoomed-in image.

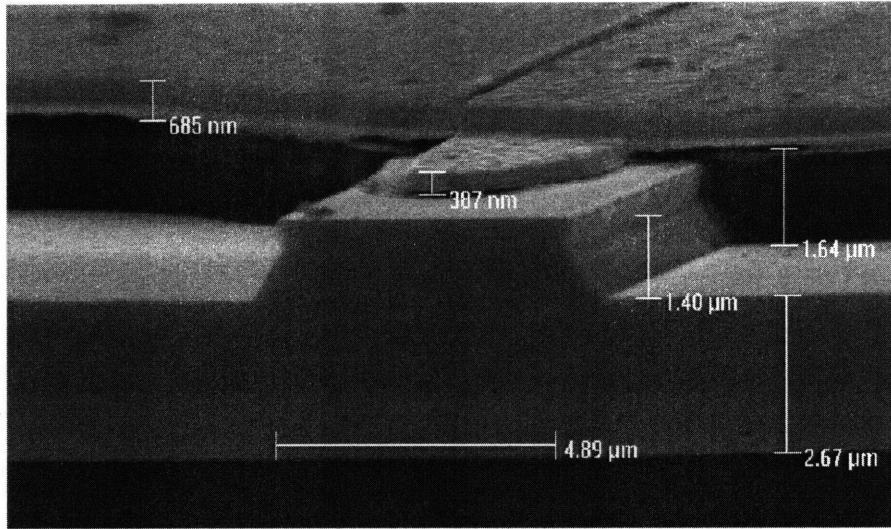


Figure 4-33: Scanning electron micrograph of a micro-cleaved platelet showing the various layers realized during the front-side processing of the device.

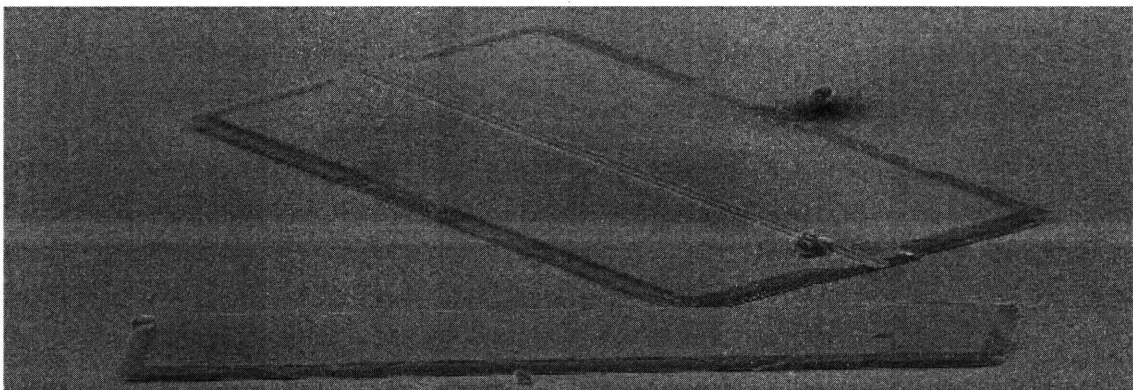


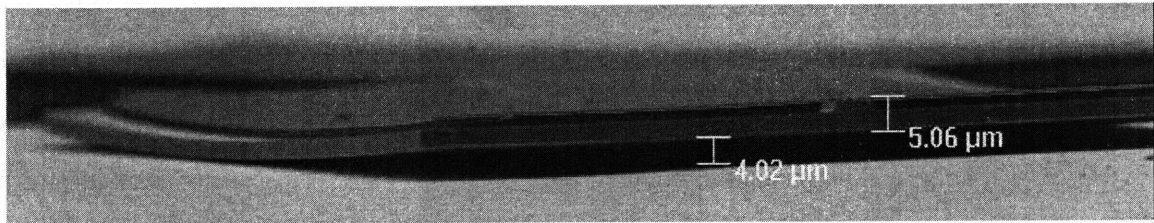
Figure 4-34: Scanning electron micrograph of a couple of poorly micro-cleaved platelets.

However, as the process has been gradually developed and refined, from micro-cleaving of platelets with no metal whatsoever, to micro-cleaving of platelets with just metal ridge contacts, to micro-cleaving of fully-metallized platelets with planarization layers and top large area metal contacts, the quality of the micro-cleaving process has improved. For instance, problems like those seen in Figure 4-34 have practically been eliminated. This is attributable to the incorporation of non-crystalline materials such as Cyclotene planarization layers, and metals. These materials, unlike single crystalline materials, like our InP semiconductor, do not break (i.e., cleave) easily. Thus, it is very difficult for a cleave in the device to propagate through these layers. Since the notch regions are the only areas devoid of these non-crystalline layers, the cleaving of these devices should only take place in these notch regions.

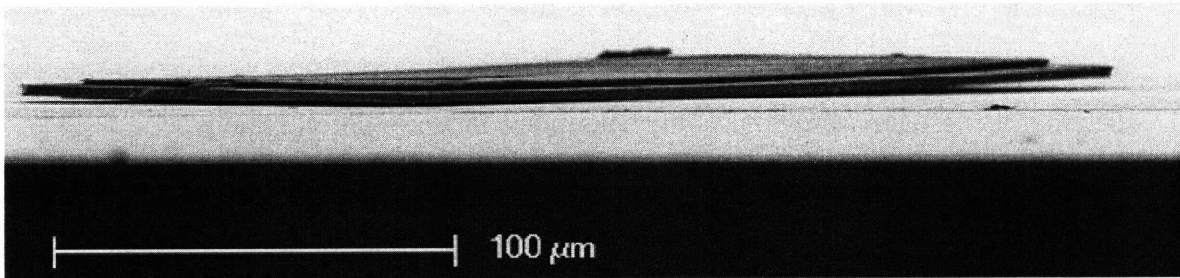
While the use of these non-crystalline layers really helps improve the micro-cleaving process, the presence of these layers on just one-side of these devices adds stress which can cause some warping in the platelet along its length. Figure 4-35 shows three micro-cleaved platelets, one with significant warping, one with less warping, and one without warping whatsoever. The first micro-cleaved platelet (Figure 4-35a) has front-side planarization layers and large area metal contacts, but no back-side metal contacts. The second micro-cleaved platelet (Figure 4-35b) has front-side planarization layers and large area metal contacts, as well as back-side metal contacts. The third micro-cleaved platelet (Figure 4-35c) has no metal whatsoever on the front-side or the back-side. This figure clearly shows the great deal of stress that these planarization and metal layers can place on a device.

Warping seems to be a significant concern for our integration approach of end-fire coupling. However, experiments were conducted that involved the thermal bonding of these warped platelets under pressure on a silicon substrate. Figure 4-36 shows that the warping of the device is removed from the bonding process and an extremely flat device results.

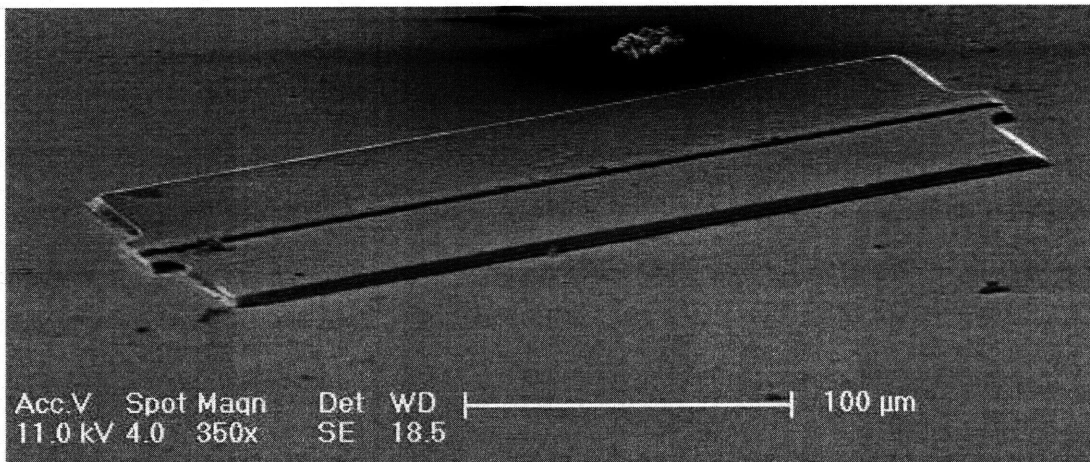
With the process of fabricating both the conventionally cleaved and micro-cleaved ridge lasers described in detail, the tools used to manipulate the devices will now be discussed.



a.)

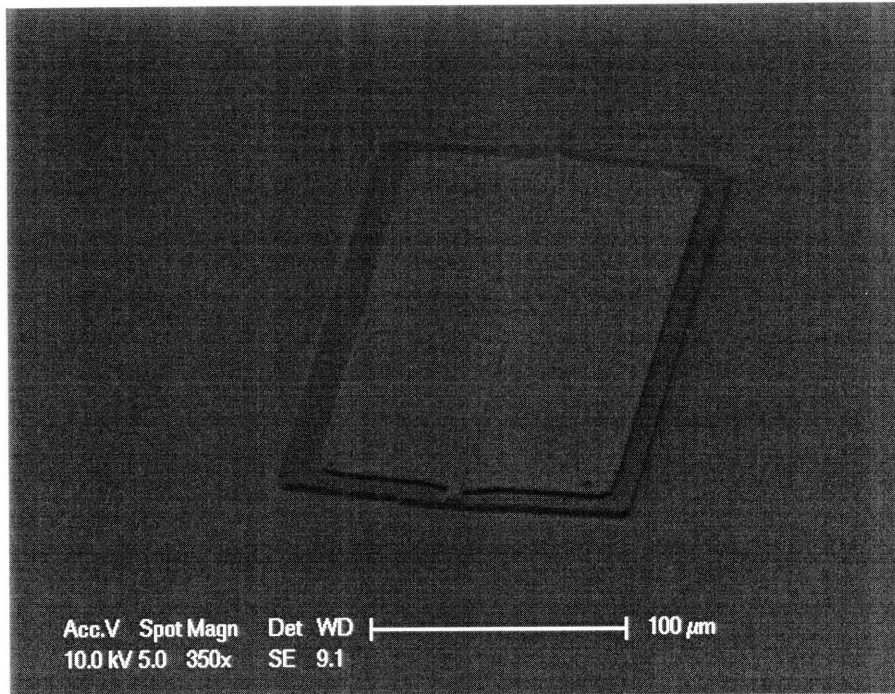


b.)

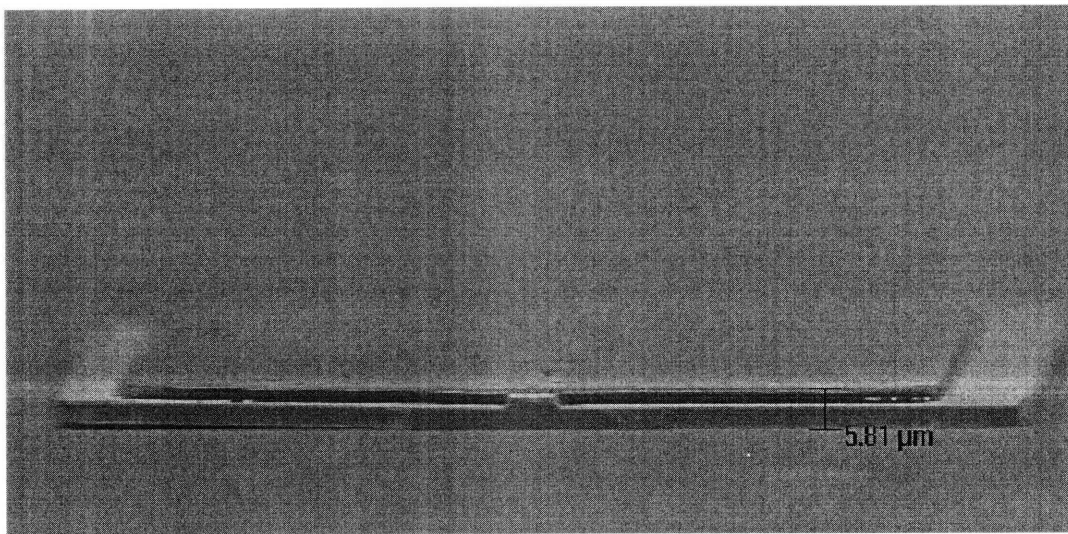


c.)

Figure 4-35: Scanning electron micrographs of: a.) A micro-cleaved platelet with front-side planarization and large area metal layers, but no back-side metal, b.) A micro-cleaved platelet with front-side planarization and large area metal layers, and back-side metal layers, c.) A micro-cleaved platelet with no front-side planarization and large area metal layers, and no back-side metal layers either.



(a) Laser bonded on silicon substrate



(b) Up-close SEM of bonded laser

Figure 4-36: Scanning electron micrograph of a laser bars indium bonded down on a silicon substrate.

4.4 Manipulation and Bonding of Micro-Cleaved Platelets

In order to characterize these small (i.e., nominally 300 μm long, 150 μm wide, < 10 μm wide semiconductor ridge) ridge laser platelets, there must first be a way to manipulate the platelets. Recall, that after the micro-cleaving process, a large batch of platelets rests in an unordered state on a teflon sheet. The transformation of these platelets into a state where the relevant electrical and optical properties of the device can be measured involves a combination of micro-scale pick and place assembly and thermo-compression bonding.

First, individual platelets are transported from the teflon sheet to a location of our choosing using micro-scale pick and place assembly. The specific tool used to perform this assembly operation was designed by Professor Clif Fonstad and former graduate student Mindy Teo and is shown in Figure 4-37.

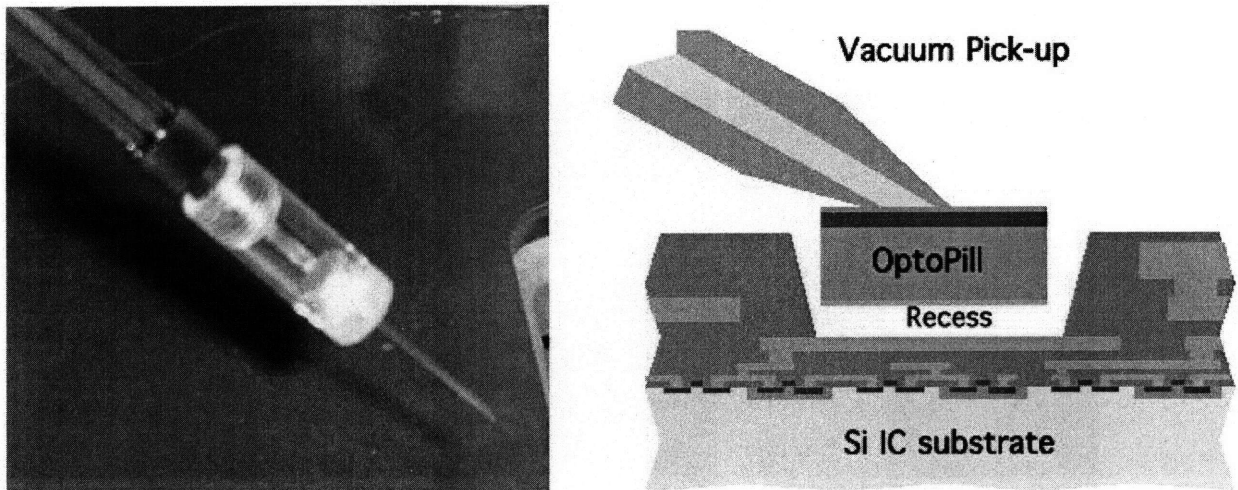


Figure 4-37: Picture and schematic of the micro-pipette tool used to pick up and move individual platelets.

The tool consists of a microscope and a narrow (i.e., 20 μm) opening glass micro-pipette that is connected to a three-axis micro-positioning stage. A vacuum is connected to the micro-pipette which creates a suction force on platelets when the pipette

approaches them. The end of the micro-pipette is beveled so that its tip is flush with the platelet.

Although this technique allows for the manipulation of the platelets, it is a rather cumbersome and slow process (i.e., greater than ten minutes per device assembly). If large numbers of platelets are required to be assembled, this pick-and-place technique, as it stands now, is impractical. Therefore, a new technique, referred to as Magnetically Assisted Statistical Assembly, aimed at large-scale micro-device integration, is being considered. The theory underlying this assembly technique will be introduced in Chapter 6. It is suggested that the combination of this technique with the platelet manufacturing processes described earlier in this thesis, large scale optoelectronic integration will be more ably pursued.

However, for our purposes here, where only small numbers of platelets are to be assembled, the micro-scale pick and place assembly process performs very well. This process has been used to assemble InP-based ridge waveguide platelets in dielectric recesses on a silicon substrate and InP-based ridge laser platelets on metallized silicon wafers. These assembly results and the post-assembly thermo-compression bonding process that is performed on the InP-based ridge laser platelets will now be presented.

4.4.1 Assembling InP-based Ridge Waveguide Platelets in Dielectric Recesses on a Silicon Substrate

Micro-cleaved InP-based ridge waveguide platelets were fabricated using many of the same processes described for the micro-cleaved ridge laser platelets. A top-down picture and cross-sectional schematic of a completely fabricated ridge waveguide platelet is shown in Figure 4-38.

Using the micro-scale pick and place assembly tool, many micro-cleaved ridge waveguide platelets were assembled in dielectric recesses on a silicon substrate as is shown in Figure 4-39. Emanating from two ends of the recess is the SiO_xN_y waveguide. The assembled ridge waveguide platelets just rest at the bottom of these recesses as no bonding operation is performed. Care must be taken when handling this integration

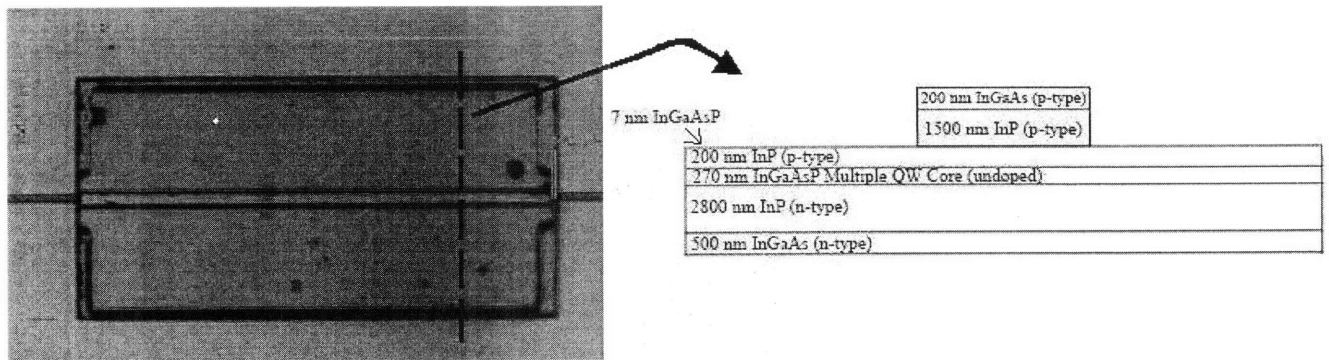


Figure 4-38: Picture and cross-sectional schematic of an InP-based micro-cleaved ridge waveguide platelet.

substrate to prevent platelets from being dislodged from the recesses. A thin (i.e., couple hundred nm thick) coating of silicon dioxide was sputter deposited over this substrate with hopes that it would help retain the platelets. Unfortunately, it was not successful and most platelets came out of the recess.

As can be seen from Figure 4-40, it is possible to assemble these platelets in tightfitting recesses, thus allowing for narrow gaps between the platelet facets and the SiON waveguide facets.

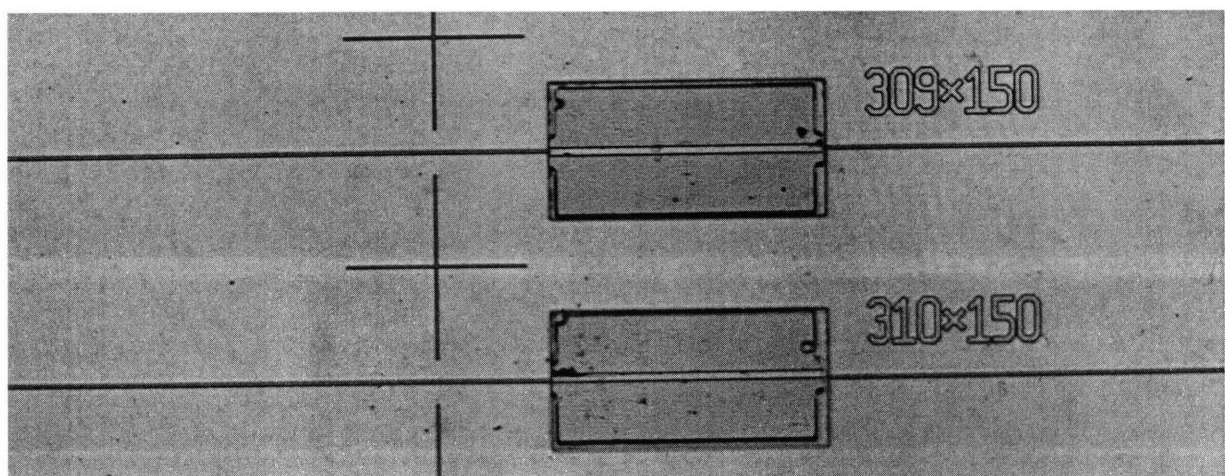
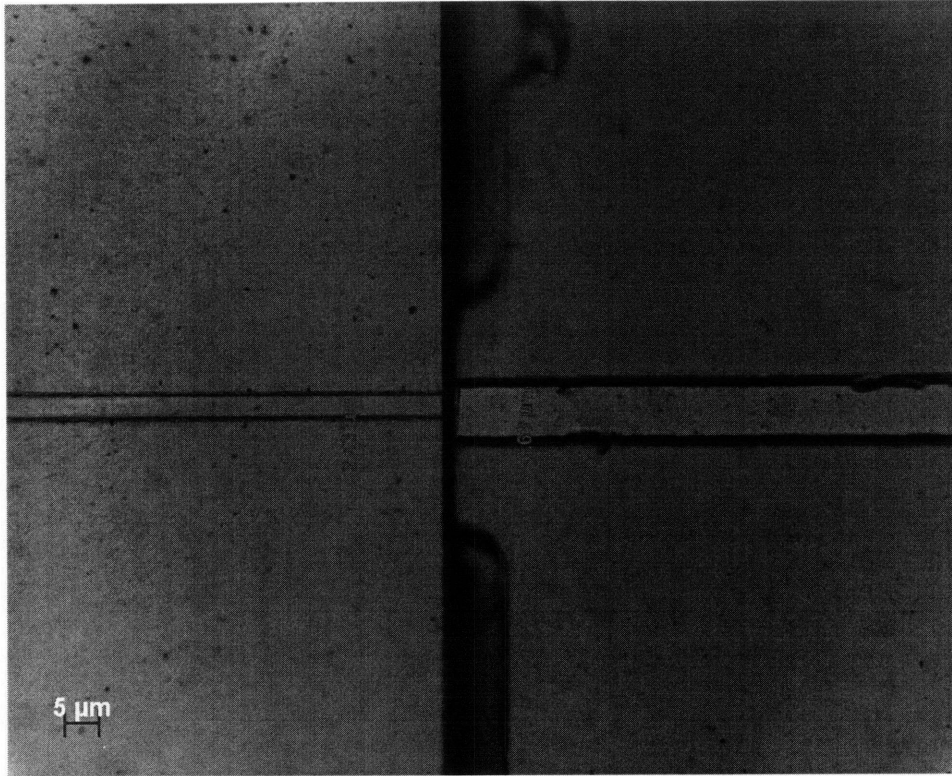
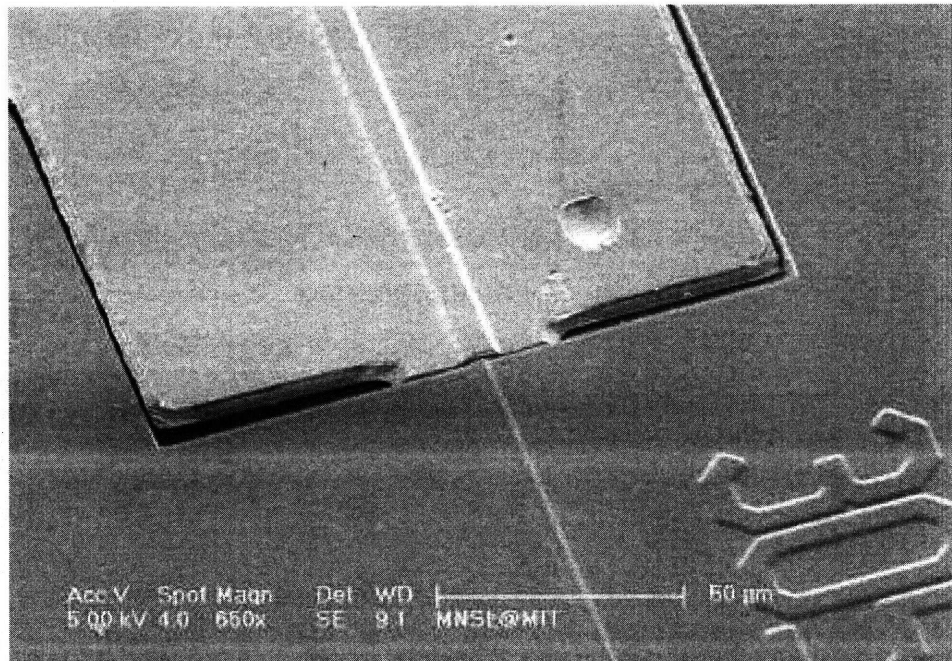


Figure 4-39: Picture of two InP-based micro-cleaved ridge waveguides assembled in dielectric recesses on a silicon substrate.



(a) Zoomed-in image showing the end-fire coupled arrangement of the micro-cleaved ridge waveguide with the silicon oxynitride waveguide on silicon.



(b) Scanning electron micrograph of a micro-cleaved ridge waveguide platelet assembled in a dielectric recess and end-fire coupled to a silicon oxynitride dielectric waveguide on silicon.

Figure 4-40: Images of micro-cleaved ridge waveguides assembled in dielectric recesses on a silicon substrate.

4.4.2 Assembling InP-based Ridge Laser Platelets on Metallized Silicon Substrates for Device Characterization

To facilitate their characterization, ridge laser platelets were picked up using the micro-scale pick and place tool and positioned on a silicon substrate that had been coated with a metal stack of gold and indium. Care was taken to position the platelets with the ridge side up. This orientation is desired to allow for the optimal bonding of the platelet to the silicon substrate and the resulting heat sinking effectiveness that is characteristic of well-bonded platelet/substrate system. The ridge side of the device can have upwards of a couple hundred nanometer topography which can compromise bonding and associated heat sinking if this side is bonded to the silicon substrate.

Once the device was placed on the carrier substrate, a thermo-compressive bonding process was undertaken. To accomplish this, a bonding chamber, designed and built by Professor Cliff Fonstad and former graduate student Mindy Teo, was utilized. A schematic of this bonding chamber is shown in Figure 4-41.

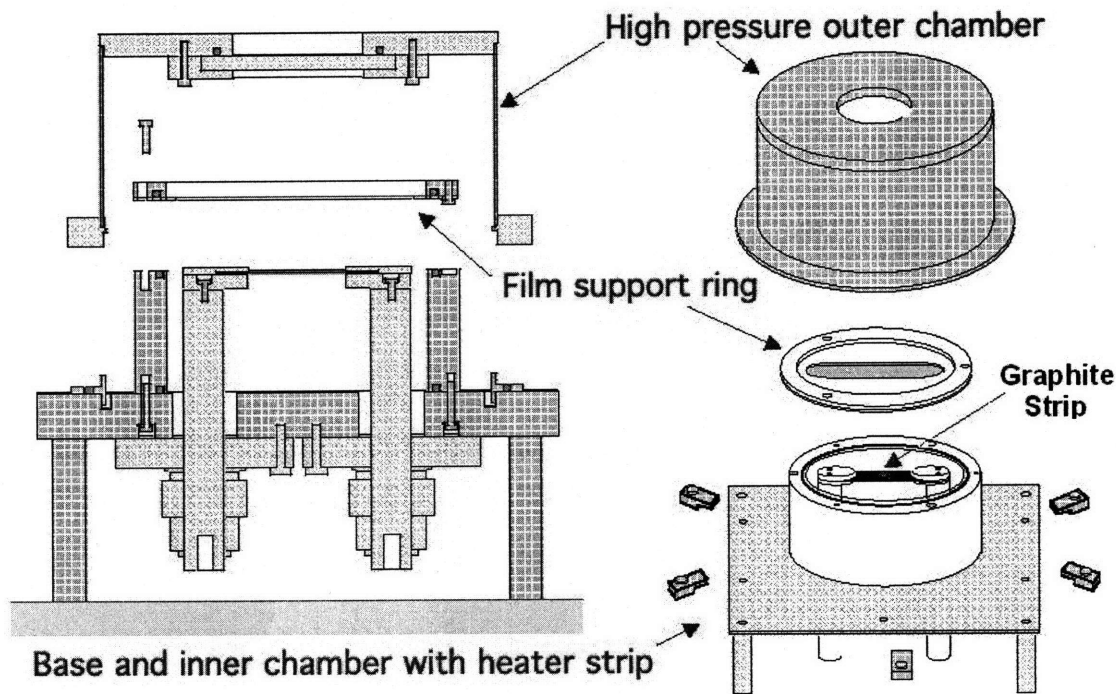


Figure 4-41: Schematic of the bonding chamber used.

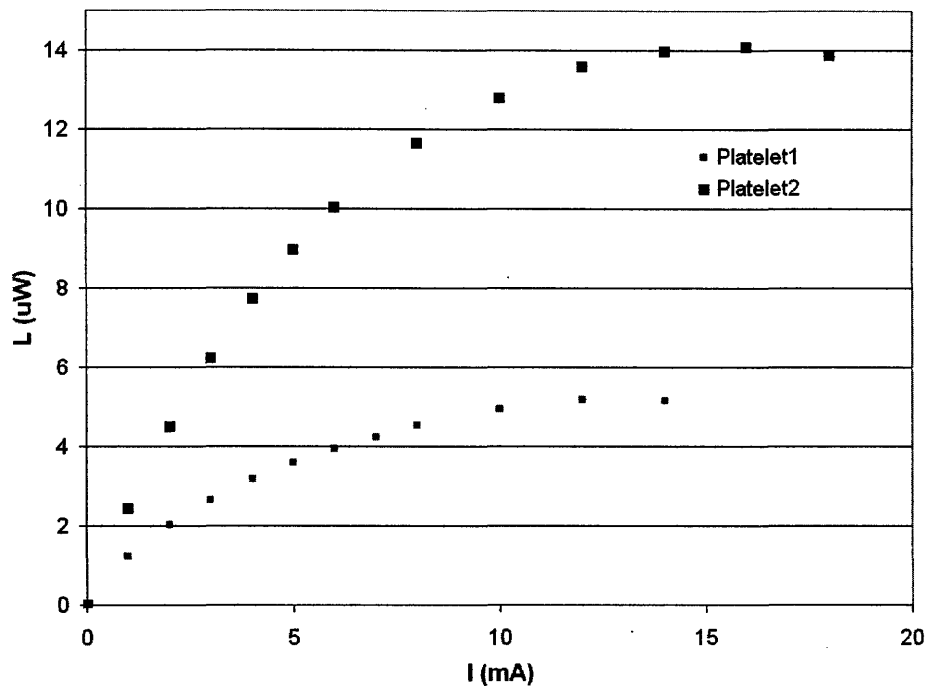
The metallized silicon substrate on which the micro-cleaved ridge laser platelet

rests, is first placed on a thin glass slide on the graphite heating strip¹⁵. The film support ring is then screwed tightly down on top of the sample. The high pressure outer chamber is then clamped down in place surrounding the inner chamber. Nitrogen is flowed into the outer chamber and this action causes the polymer film to be pressed downward onto the substrate to be bonded. Forming gas is flowed into the inner chamber to prevent oxidation of the sample as the temperature of the heating strip is increased. Entire control of the bonding temperature is provided through a Lindberg power controller. Temperature feedback is provided via a thermocouple which is mounted underneath the graphite heating strip. Successful platelet bonding was carried out for six minutes at a temperature of 210 °C and a pressure of 40 to 45 PSI.

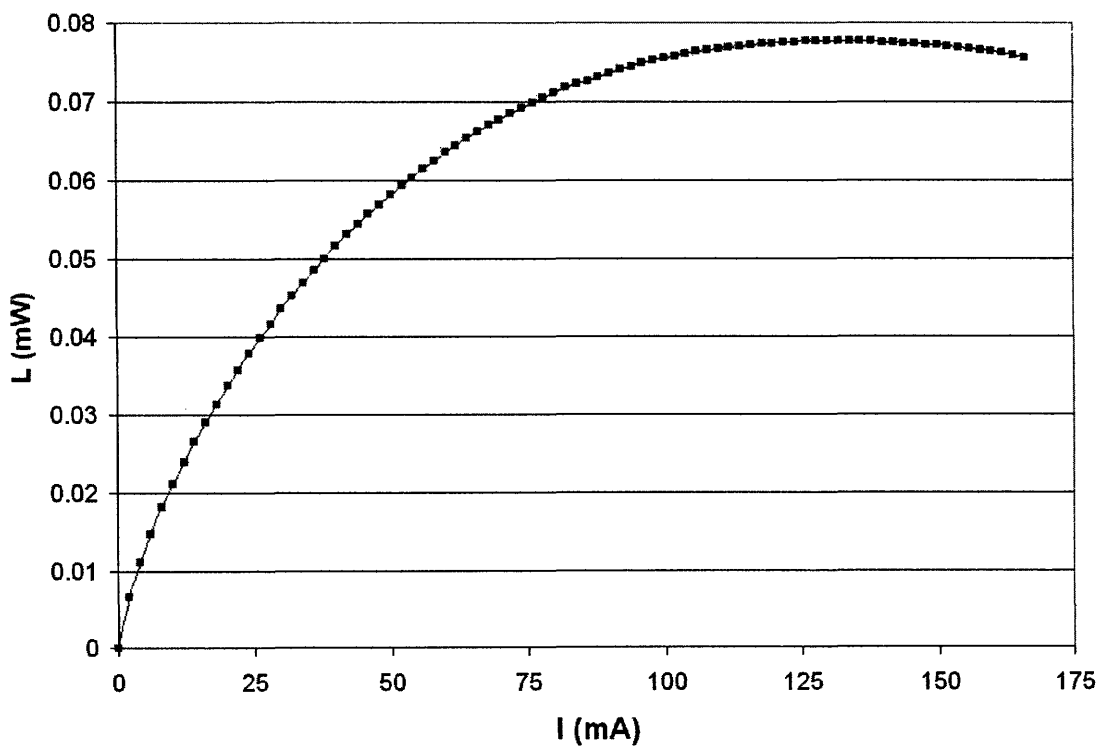
Bonding proved to be a critical step in getting the micro-cleaved devices to lase on silicon. Figure 4-42 shows the light output characteristics of two micro-cleaved devices. Figure 4-42a shows the characteristics of two devices that just rested (i.e., was not bonded) on a silicon substrate. In this case, just low levels of spontaneous emission were detected. Figure 4-42b shows the characteristic of a micro-cleaved device which was poorly bonded to a metallized silicon wafer. This device did not lase, but a significantly greater level of spontaneous emission was detected. When probing this device, it was apparent that the bonding process was substandard as the device came loose from the silicon substrate. Problems with the bonding process centered on the application of a pressure that was too low (i.e., 20 PSI) and the use of an indium film that was too thin (i.e., 100 nm).

By increasing the bonding pressure to greater than 40 PSI and using indium thicknesses of 500 nm, solid bonding was achieved and continuous-wave lasing operation of the micro-cleaved devices on silicon was achieved. The characterization of these devices as well as the conventionally cleaved devices will now be presented in Chapter 5.

¹⁵The glass slide is used to create an insulating barrier between the graphite strip and the bonding sample. Without this barrier, current that flows through the graphite strip during the bonding step would likely also travel through the substrate being bonded. This could cause serious damage to the platelet device.



(a) L-I characteristic of unbonded micro-cleaved device on silicon.



(b) L-I characteristic of poorly bonded micro-cleaved device on silicon.

Figure 4-42: Light output characteristics of unbonded and poorly bonded micro-cleaved ridge platelets on silicon.

Chapter 5

Micro-Cleaved Ridge Laser

Characterization

With the novel process technology to manufacture highly integrable micro-cleaved ridge lasers described, the measurements performed on these devices will now be presented in this chapter. First, the characterization experiments used to determine the precision with which the micro-cleaving process defines laser cavity lengths is detailed.

The optical and electrical characterization of the lasers is then presented. First, the analysis of several conventionally cleaved ridge lasers on native InP substrates is presented. Continuous-wave light output characteristics (L-I curves) are shown and parameters such as threshold current, $I_t h$, differential efficiency, η_d , characteristic temperatures, T_0 and T_1 , are extracted. Values for internal quantum efficiency and intrinsic loss, are reported for the laser epitaxial material. The output emission spectrum measured at three different drive currents is presented with the observed Fabry-Perot mode peak spacing agreeing with theory. The electrical characteristics of the conventionally cleaved lasers are detailed and values for the laser diode series resistance and diode ideality factor are extracted.

Electrical and light output characteristics of micro-cleaved ridge lasers integrated on a silicon substrate are then presented. Continuous-wave L-I curves measured at a number of different stage temperatures are shown. Peak output powers, differential

efficiencies, and threshold currents are presented. Characteristic temperatures, T_0 and T_1 , measured for the micro-cleaved ridge laser on silicon are shown. In addition, the results of pulse measurements are detailed.

An analysis of all six tested micro-cleaved devices lasing on silicon concludes this chapter. The values of threshold currents, differential efficiencies, T_0 , R_{series} , and $V_{turn-on}$ for these micro-cleaved lasers on silicon are compared and contrasted and reasons for their parameter value differences are suggested.

5.1 Micro-Cleave Precision Characterization

Given the end-fire coupling scheme for optoelectronic integration proposed in Chapter 2, it is extremely important that the active optical devices that are to be integrated have very precise dimensions. As was argued in Chapter 3, the most difficult dimension to precisely control for edge-emitting active devices is the cavity length. To produce edge-emitting lasers with both well-controlled cavity lengths and mirror smooth facets, a precision micro-cleaving technique was developed. Details on the micro-cleaving technique were presented in Chapter 3 and the specific process to realize micro-cleaved laser platelets was outlined in Chapter 4.

In Chapter 3, it was suggested that as the micro-cleave notch is narrowed, the precision with which the laser cavity lengths are dimensioned will increase. To investigate this hypothesis, several samples, each with a different micro-cleave bar pattern notch width, were fabricated and the notch widths were measured for completeness. Then, the micro-cleaving operation was performed and the cavity lengths of these micro-cleaved platelets were measured. These notch width and cavity length measurements were made using a Carl Zeiss AxioSkop microscope system outfitted with an AxioCam MRc digital camera and the AxioVision digital imaging software. This method produces an overall measurement reproducibility of better than $0.21 \mu\text{m}$.¹

Other methods were first considered for performing this characterization study.

¹Ten independent measurements of the cavity length of one specific platelet were carried out and the standard deviation of these measurements was used as an estimate for the measurement reproducibility.

For example, for measuring the notch widths, a profilometer² was first tried. However, it was quickly realized that there was an inherent error in these measurements due to the size and shape of the profilometer stylus. The stylus has a conical shape with radius, R, as is shown in Figure 5-1. When measuring notches, the measurement always suggests that the notch is narrower than it actually is. This phenomena is labelled "groove loss" by the profilometer manufacturer. The accompanying table in Figure 5-1 shows the groove loss as a function of stylus radius and groove depth.

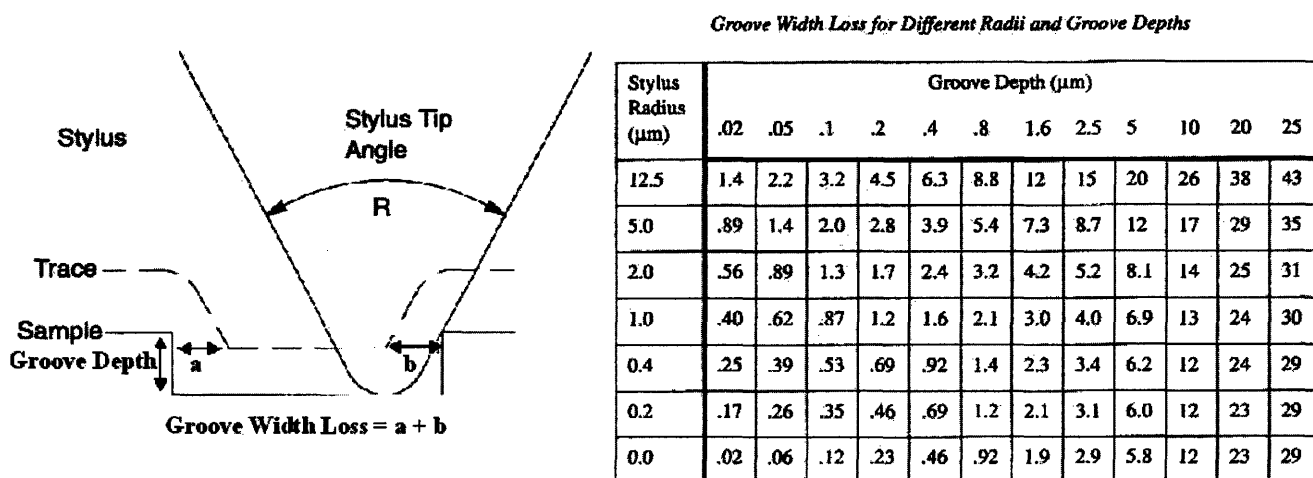


Figure 5-1: Schematic and table detailing the effect of profilometer stylus radius on the lateral measurement accuracy[83].

For the Tencor P-10 profilometer available on campus at the MIT Center for Materials Science and Engineering (CMSE), the smallest stylus available has a radius of 2 μm. From Figure 5-1, profiling 5 μm groove depths, using this stylus, would result in groove width losses of roughly 8 μm. This groove width loss varies as a function of stylus radius and groove depth and thus adds another uncertainty in the measurement of the notch width. Moreover, if the sidewalls of the notch are sloped, the actual notch width is even more difficult to determine using a profilometer. Due to these issues with using a profilometer, the Carl Zeiss AxioSkop system was used.

The specific experimental protocol followed for each sample involved first measuring the realized notch widths of fifteen different bars from the same sample process

²Two widely used commercial profilometers are the DekTak and the KLA Tencor P-10 instrument.

run. Sample notch width measurements are shown in Figure 5-2. Averaging these fifteen notch widths, an estimate is determined for the notch width of that sample. The average notch width variation across a given sample is typically $0.45 \mu\text{m}$ for dry etched samples and upwards of $0.8 \mu\text{m}$ for wet etched samples.³ With the notch width of a given sample estimated, the cavity lengths of ten different micro-cleaved platelets from that same sample were measured as is shown in Figure 5-3. The standard deviation of these ten measurements gives an estimate of the laser cavity length precision for a specific notch width.

Combining these notch width and cavity length standard deviation measurements, a plot of the estimated laser cavity length precision as a function of notch width is shown in Figure 5-4. Horizontal error bars are present to account for notch width variation specific to each sample. Vertical error bars corresponding to the measurement repeatability of $0.21 \mu\text{m}$ are also included.

This experimental study confirms the hypothesis that as the micro-cleave bar pattern notch width is narrowed, the precision with which the laser cavity lengths are defined increases. The lowest device length standard deviation obtained was $1.16 \mu\text{m}$ and the narrowest notch patterned was $5.5 \mu\text{m}$. The benefits of patterning narrower notches seem to be diminishing as we pattern the notches narrower than $7.5 \mu\text{m}$. Notches having widths in the $5.5 \mu\text{m}$ to $7.5 \mu\text{m}$ range all had similar device length standard deviations. It is believed that by significantly narrowing the notch width to values closer to $1 \mu\text{m}$ that the device length standard deviation could be further reduced. A number of experiments were carried out in attempts to pattern narrower notches. These experiments relied on both reactive ion etching of the SiO_2 etch mask and the InP/InGaAsP semiconductor. Notches as narrow as $3 \mu\text{m}$ were patterned in photoresist using contact lithography. The notches typically widened to between 4 and $5 \mu\text{m}$ during the reactive ion etching of the $1 \mu\text{m}$ thick SiO_2 hardmask. The InP/InGaAsP high density plasma dry etch widened the notches slightly to near $5.5 \mu\text{m}$ because of sloped features on the SiO_2 hardmask. It is believed that with higher

³The standard deviation of the notch width measurements on a given sample provides an estimate for this.

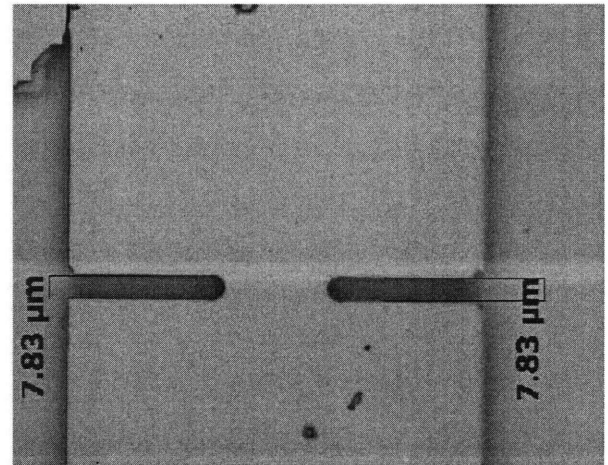
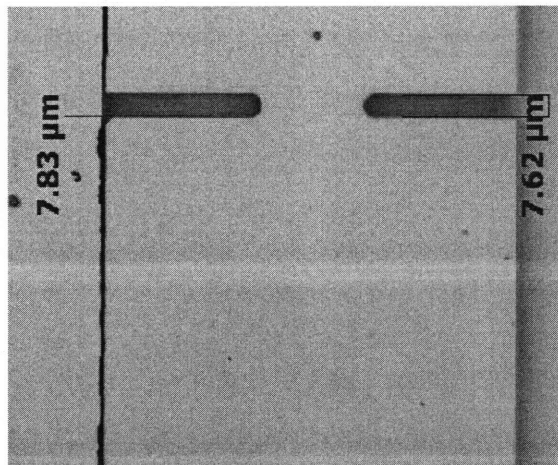
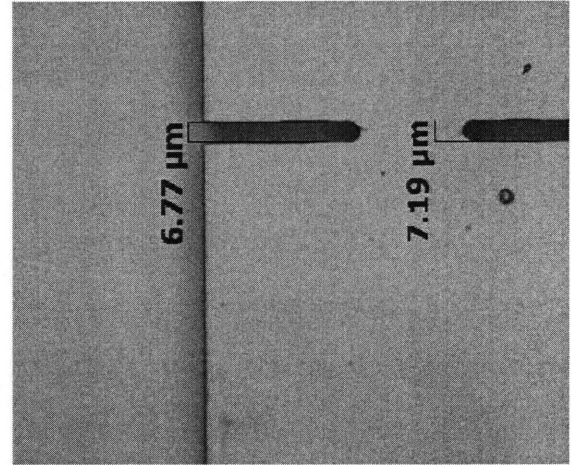
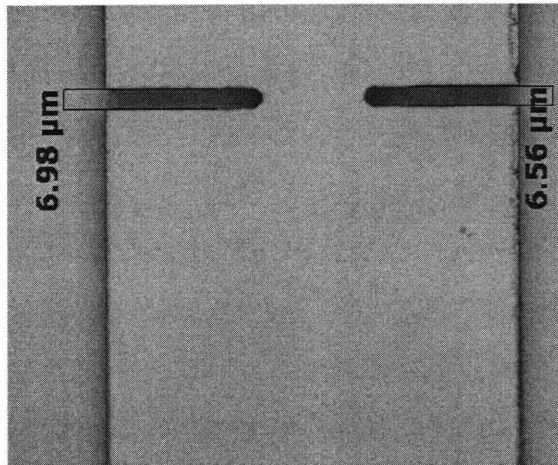
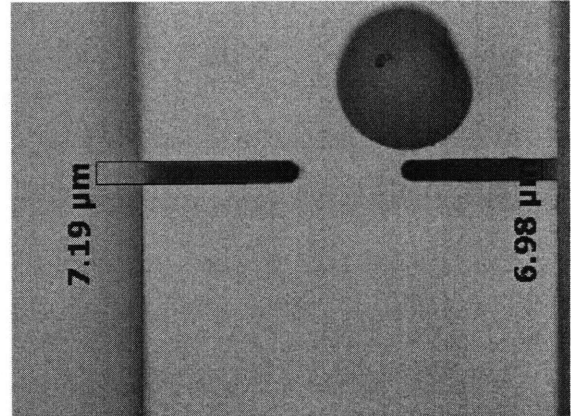
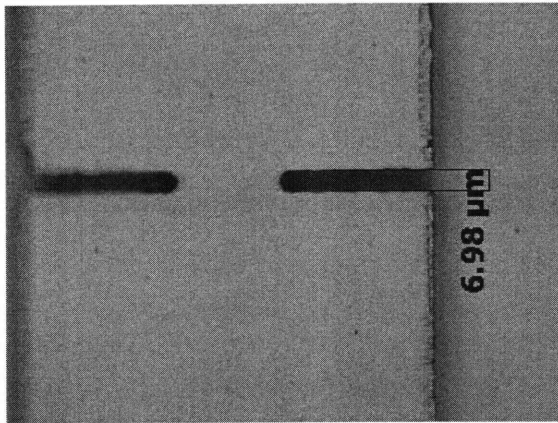


Figure 5-2: Pictures taken with the Carl Zeiss Axioskop microscope system of a number of notches from one given sample.

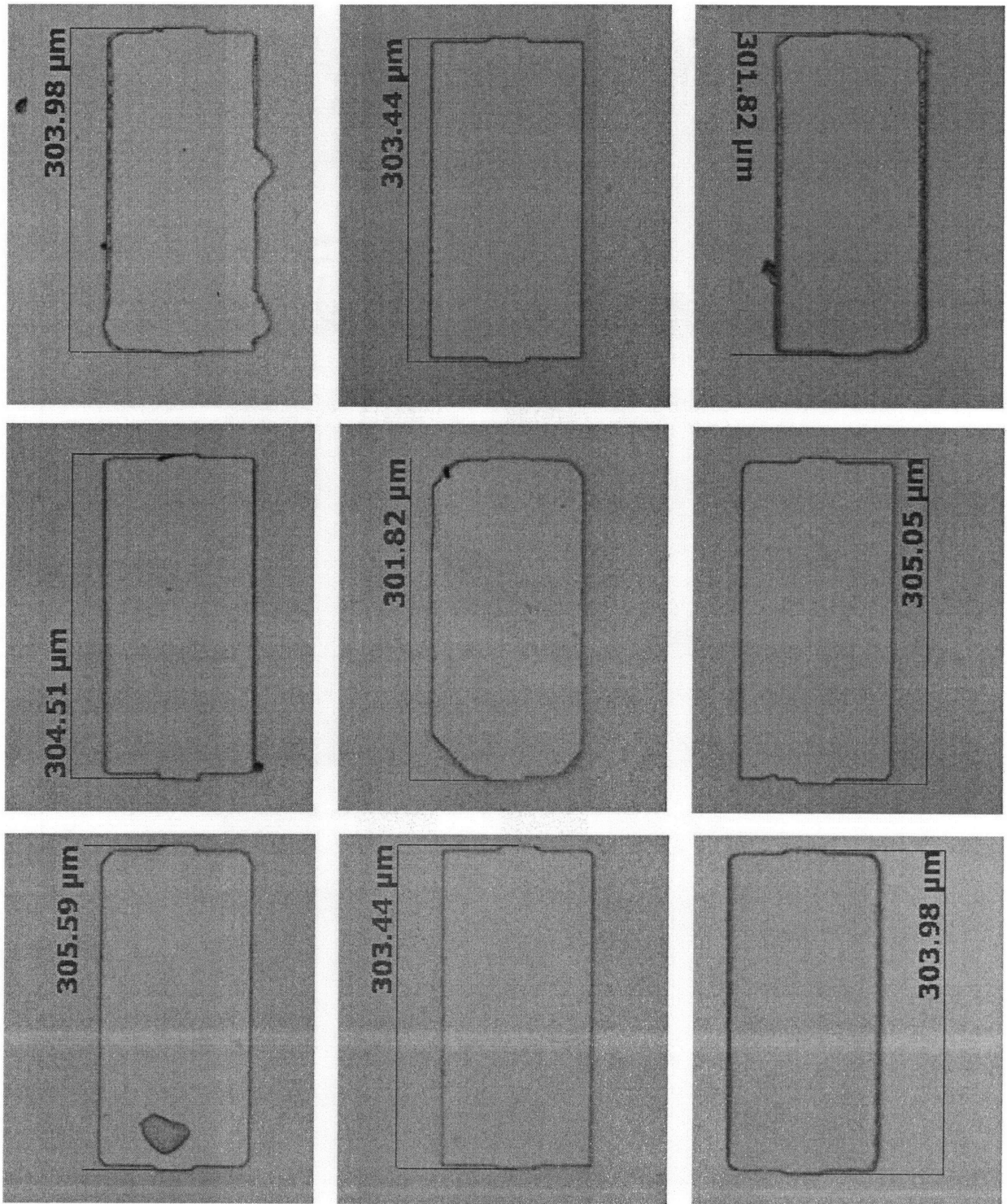


Figure 5-3: Pictures taken with the Carl Zeiss Axioscope microscope system of a number of micro-cleaved platelets from one given sample.

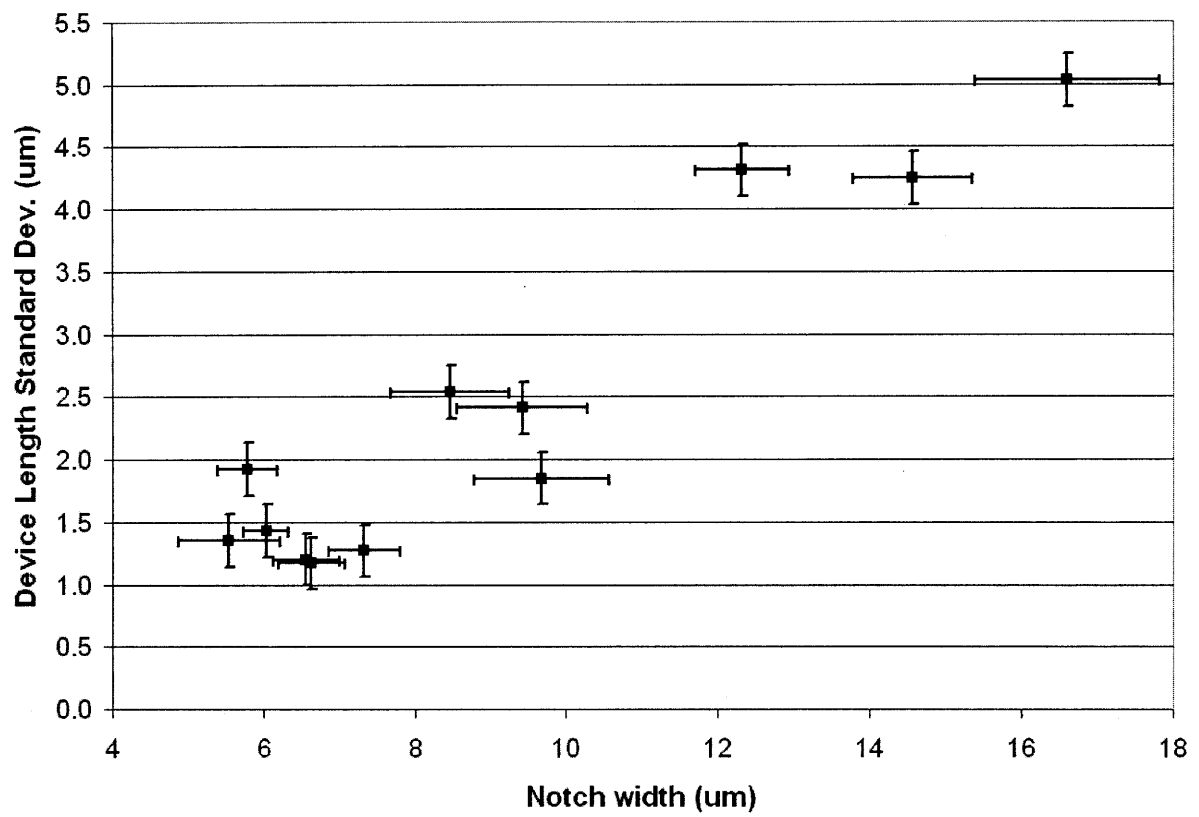


Figure 5-4: Experimental results of the micro-cleave process device length variability as a function of notch width.

resolution lithography tools and a dedicated high density plasma dry etch tool for dielectrics, significantly narrower notches could be achieved.

Ultimately, the notch width will be limited by the planarity of the device structures just before the bar pattern photolithography process step. The micro-cleaving precision characterization experiments discussed here were carried out on flat InGaAsP/InP laser wafers and thus should reflect the best possible results achievable with the processing equipment used in this work. Real micro-cleaved ridge lasers are non-planar when they reach the bar pattern photolithography step. In fact due to the ridge pattern and metal contacts, there is around $2\ \mu\text{m}$ of topography. So, instead of $5.5\ \mu\text{m}$ notch widths, the notch widths on actual realized devices were a few microns wider. Even with this topography, notches narrower than $7.5\ \mu\text{m}$ should be easily achieved with the use of modern photolithography and etching tools. This process capability would allow device standard deviations better than $1.25\ \mu\text{m}$ to be attained. Tight control like this of the micro-cleaved length dimension should make the end-fire coupling integration strategy feasible. For integrating devices which need to be end-fire coupled at both facets (i.e., SOAs), the average gap spacing on the input and output facets should be less than $1.25\ \mu\text{m}$. Coupling losses to SiO_xN_y dielectric waveguides, assuming no gap fill, are estimated to be only a few dB per facet for gaps of this length[15]. For integrating devices which only need to be end-fired coupled at one facet (i.e., laser), it should be possible to minimize the gap spacing by assembling the device right up to the dielectric waveguide facet. In this case the coupling loss should be even lower.

5.2 Ridge Laser Optical and Electrical Characterization

Continuous-wave (CW) characterization of both conventionally cleaved (CC) and micro-cleaved (MC) ridge lasers was carried out using the setup schematically shown in Figure 5-5. During testing, the devices rest on a stage at the end of which is

situated a large area long wavelength photodetector. A Wavelength Electronics Model LFI-3751 Thermoelectric Temperature Controller was used to control and read the stage temperature. The lasers were electrically driven with a Newport Laser Diode Driver Model 5005 and the laser light emission was detected using an ILX Lightwave OMH-6708B InGaAs Power head detector which was connected to an ILX Lightwave OMM-6810B Optical Multimeter.

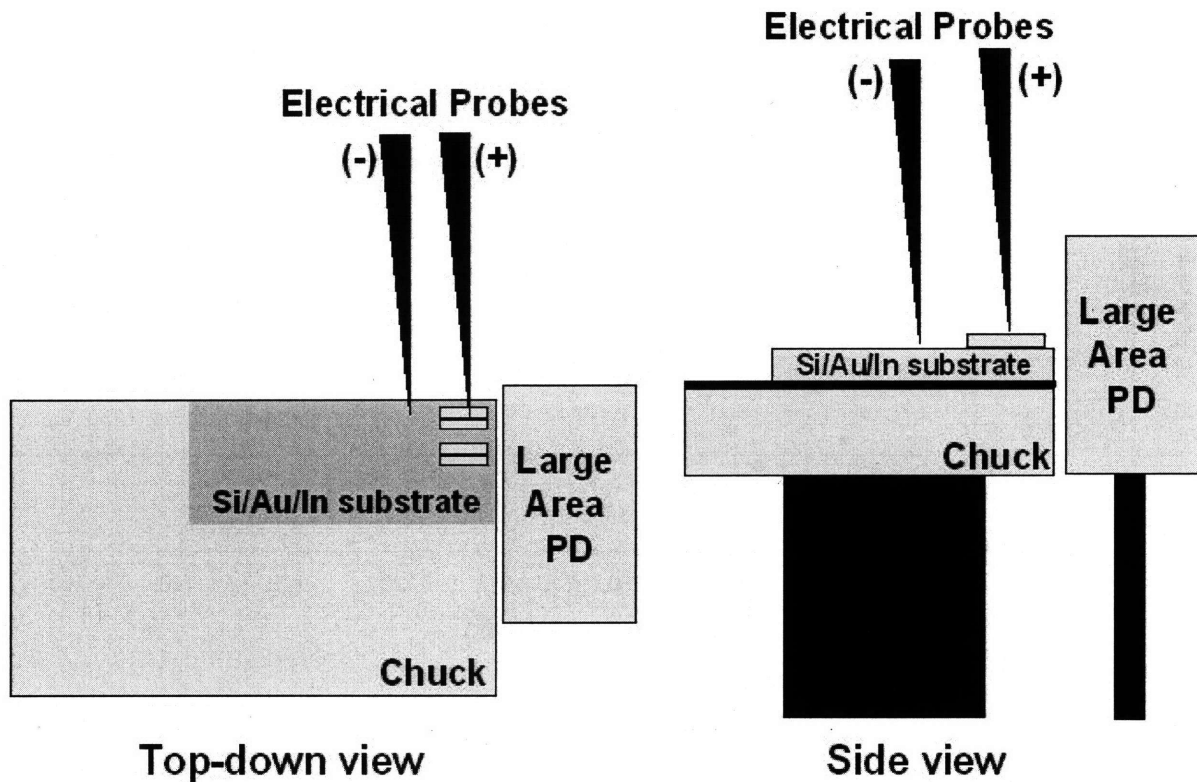


Figure 5-5: Test setup for the ridge laser light output characterization.

5.2.1 Conventionally Cleaved Ridge Laser

Conventionally cleaved ridge lasers were first fabricated and tested to ensure that the semiconductor epitaxial material was capable of lasing and to provide a reference for comparing the micro-cleaved ridge laser results to. A top-down photograph of a typical conventionally cleaved ridge laser is shown in Figure 4-10. Both optical and electrical characteristics of these ridge lasers were measured and these results will now

be presented.

Light Output Characteristics

Room temperature CW light output characteristics of several CC ridge lasers having different lengths were measured and these characteristics are shown in Figure 5-6.

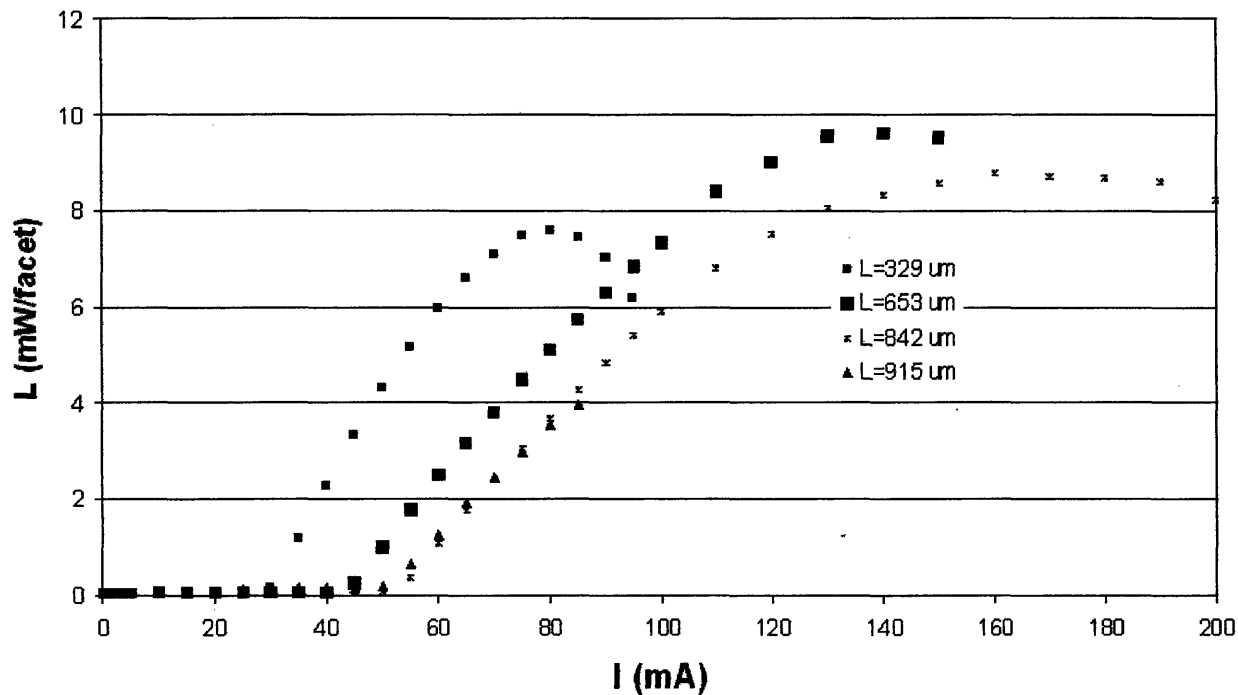


Figure 5-6: Experimental light output characteristics of CC ridge lasers ($6.8 \mu\text{m}$ wide ridge) of various cavity lengths measured at room temperature and under continuous-wave conditions.

Threshold current values were extracted from light output characteristics of CC lasers and are plotted as a function of laser cavity length in Figure 5-7. The linear

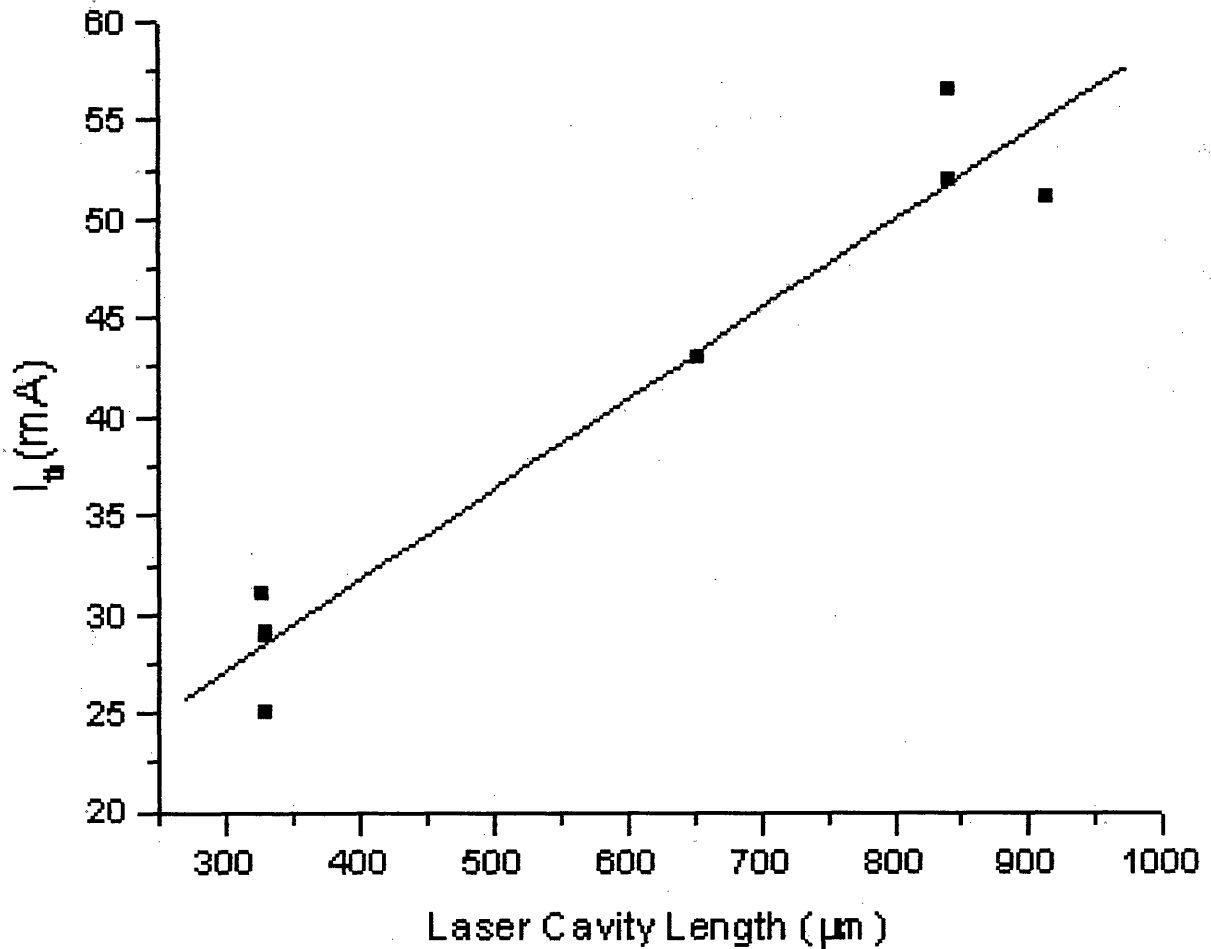


Figure 5-7: Threshold current as a function of laser cavity length for CC ridge lasers (6.8 μm wide ridge) measured at room temperature and under continuous-wave conditions.

relation between these lasers' threshold currents and their cavity lengths obtained from the linear fit is

$$I_{th}(mA) = 0.045L(\mu m) + 13.6 \quad (5.1)$$

If a 300 μm long conventionally cleaved ridge laser was produced from this epitaxial material, this laser would likely have a room temperature threshold current of approximately 27 mA. Since the micro-cleaved lasers that will be discussed later in this

chapter have nominal lengths of $300 \mu\text{m}$, this extracted CC threshold current value will be useful for comparison.

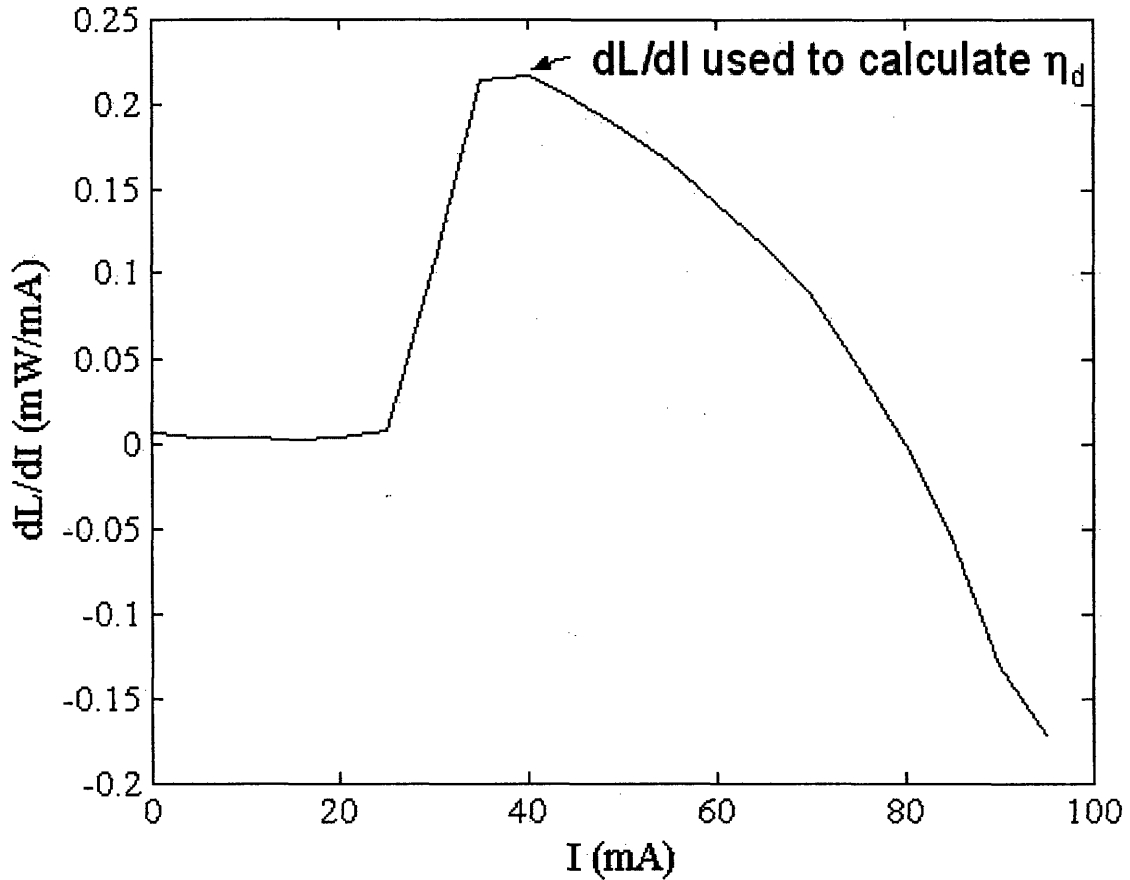


Figure 5-8: dL/dI vs. I characteristic for a CC ridge laser ($6.8 \mu\text{m}$ wide ridge, $328.5 \mu\text{m}$ long device) measured at room temperature and under continuous-wave conditions.

A plot of the derivative of the light output power with respect to input current for one output facet is shown in Figure 5-8. Taking note of the dL/dI value just beyond threshold at the point of operation just before the dL/dI starts to decrease as I is increased, a value of η_d was calculated using the following equation

$$\eta_d = \left(\frac{q}{h\nu}\right) \frac{dL_{tot}}{dI} \quad (5.2)$$

where L_{tot} is the total light power emitted from both facets. Note that if only one facet is measured then the total dL/dI is usually assumed to be equal to twice this

dL/dI value measured for one facet. The inverse of the differential efficiency can be expressed by

$$\frac{1}{\eta_d} = \left(\frac{\alpha_i}{\eta_i \ln(1/R)} \right) L + \frac{1}{\eta_i} \quad (5.3)$$

where α_i is the net internal optical loss, η_i is the internal quantum efficiency, and R is the mirror reflectivity. Values of the differential efficiency, η_d , were extracted for several CC ridge lasers. By fitting a line to a plot of the inverse of the differential efficiency as a function of cavity length, several device properties can be extracted. For the CC ridge lasers, this plot is shown in Figure 5-9. A value of 87.6% is extracted for η_i and 19.4 cm^{-1} for $\alpha_i/\ln(1/R)$.

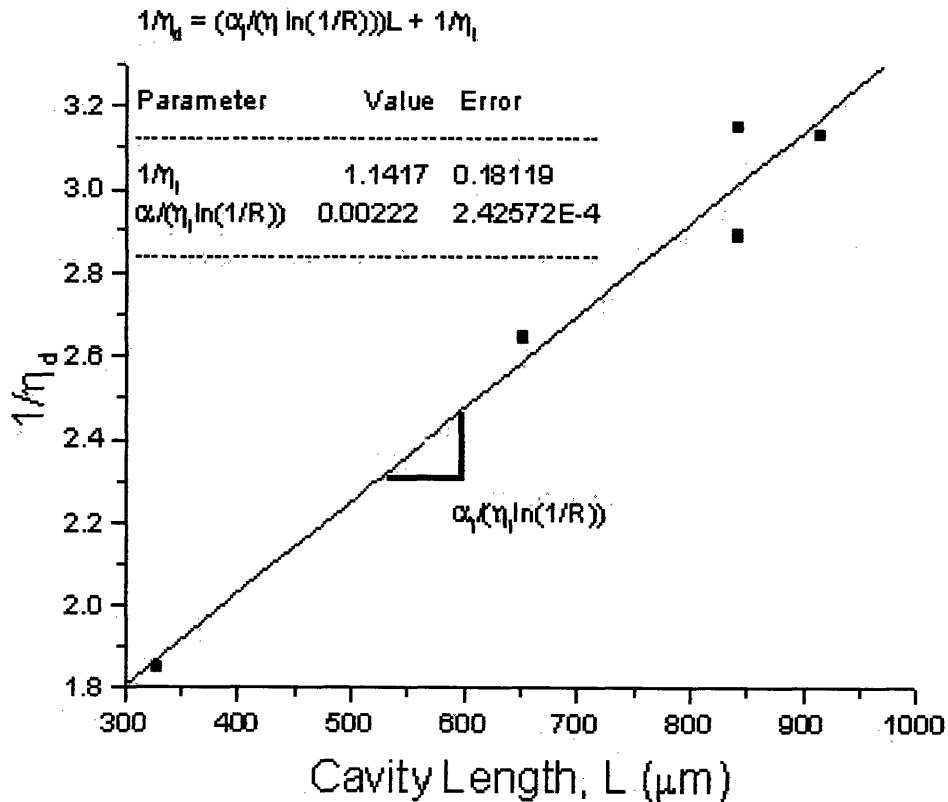


Figure 5-9: Inverse of the maximum differential efficiency as a function of laser cavity length for CC ridge lasers ($6.8 \mu\text{m}$ wide ridge) measured at room temperature and under continuous-wave conditions. Extracted parameters are $\eta_i = 87.6\%$, and $\alpha_i/\ln(1/R) = 19.4 \text{ cm}^{-1}$.

To determine α_i , the mirror reflectivity, R , must be known. Assuming normal

incidence of the optical wave at the laser facet between air and the semiconductor, R is given by the relation

$$R = \frac{(n_{eff} - 1)^2}{(n_{eff} + 1)^2} \quad (5.4)$$

where n_{eff} is the effective refractive index of the ridge laser. From theoretical calculations, the fundamental TE mode of the ridge laser structure used in this work was found to have an effective refractive index of approximately 3.2[15]. It is possible to experimentally verify this effective refractive index. Since the CC ridge laser is a Fabry Perot laser, there are several longitudinal modes visible as narrowly spaced peaks in the output spectrum. These peaks are spaced according to the relation

$$\delta\lambda = \lambda \left(\frac{2Ln_g}{2Ln_g - \lambda} - 1 \right) \quad (5.5)$$

Thus, if one knows the emission wavelength, λ , the cavity length, L , and the mode spacing, $\delta\lambda$, then the group index, n_g , can be estimated using the following relation.

$$n_g = \frac{\lambda}{2L} \left[1 + \frac{\lambda}{\delta\lambda} \right] \quad (5.6)$$

The output spectrum and corresponding light output characteristic of a 328.5 μm long CC laser are shown in Figure 5-10 and Figure 5-11 respectively. The output spectrum has $\delta\lambda = 1.0$ nm. Given this observed mode spacing of 1.0 ± 0.08 nm,⁴ $n_g = 3.6 \pm 0.3$. This extracted value of the group index, as expected is slightly higher than the value of the effective refractive index. With $n_{eff} = 3.2$, R is approximately 27.4% and α_i is 25.1 cm^{-1} .

To gain a perspective of the thermal performance of the laser, light output characteristics were measured at a number of different stage temperatures. A typical set of L-I curves measured for a 1170 μm long, 6.8 μm wide CC ridge laser (CC1) is

⁴The resolution bandwidth of the ANDO Optical Spectrum Analyzer is 0.08 nm.

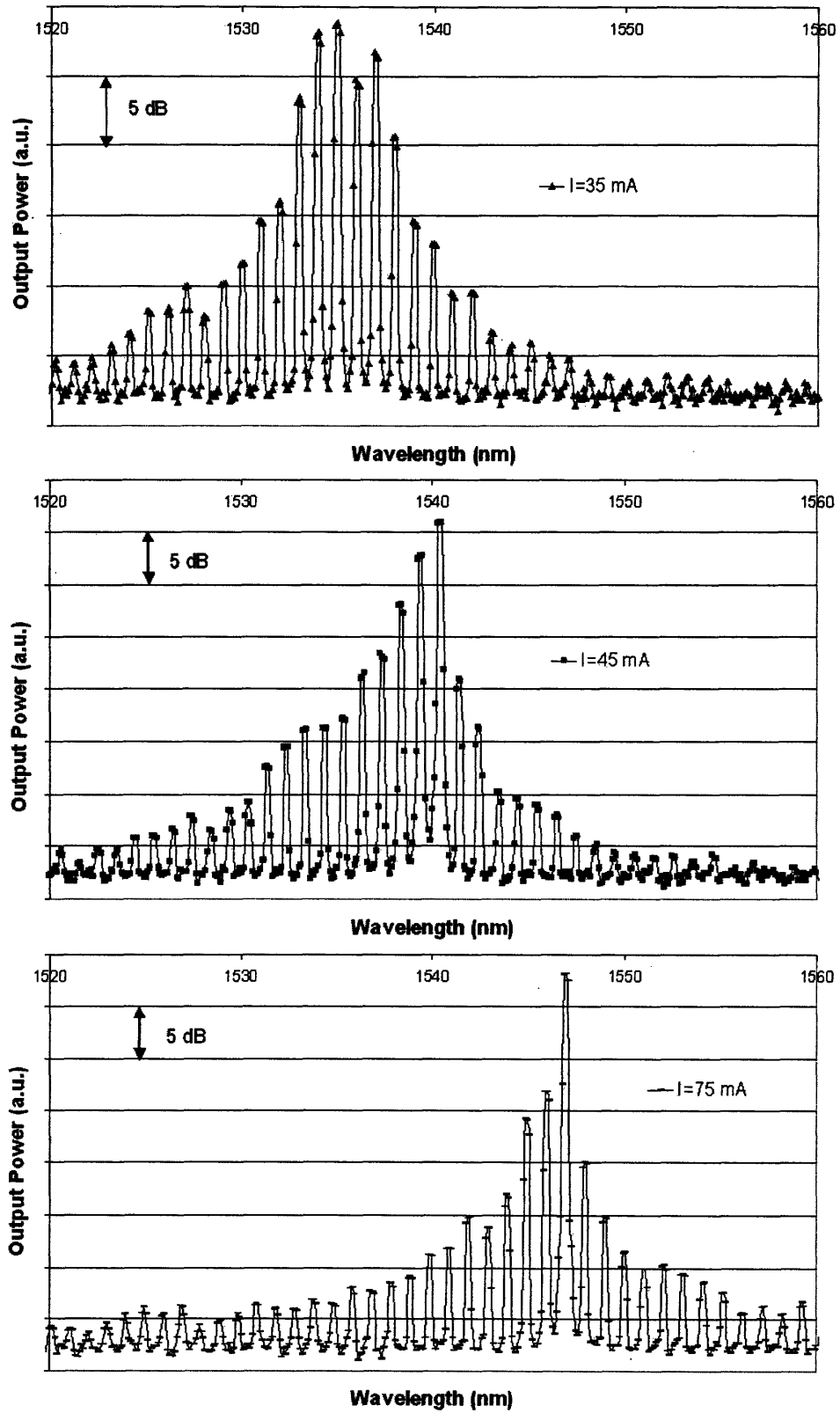


Figure 5-10: Optical output spectrum of a CC ridge laser with length = $328.5 \mu\text{m}$ and ridge width of $6.8 \mu\text{m}$ measured at room temperature and under continuous-wave conditions.

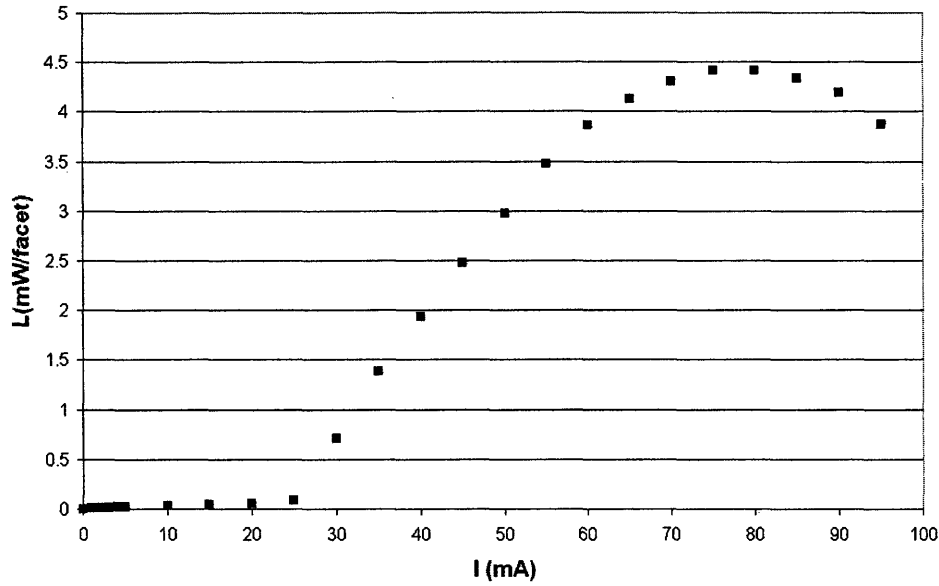


Figure 5-11: Light output characteristic of a CC ridge laser with length = 328.5 μm and ridge width of 6.8 μm measured at room temperature and under continuous-wave conditions. This output spectrum corresponding to this laser is shown in Figure 5-

shown in Figure 5-12 for reference. From this plot, it is possible to extract the characteristic temperatures, T_0 and T_1 , for the devices. T_0 , as was described in Chapter 3, relates the dependence of the threshold current on the temperature. T_1 relates the dependence of the differential efficiency on temperature. The higher the characteristic temperatures the less sensitive the devices are to temperature. The threshold current, I_{th} , is related to the characteristic temperature, T_0 , through the expression

$$\ln(I_{th}) = \ln(I_{th,0}) + \frac{T}{T_0} \quad (5.7)$$

By fitting a line to a plot of the natural logarithm of the threshold currents vs. stage temperature, estimates for T_0 and $I_{th,0}$ were found (Figure 5-13). This analysis was carried out on four CC lasers and the results are shown in Figure 5-14. The dimensions of these four CC lasers are shown in Table 5-1.

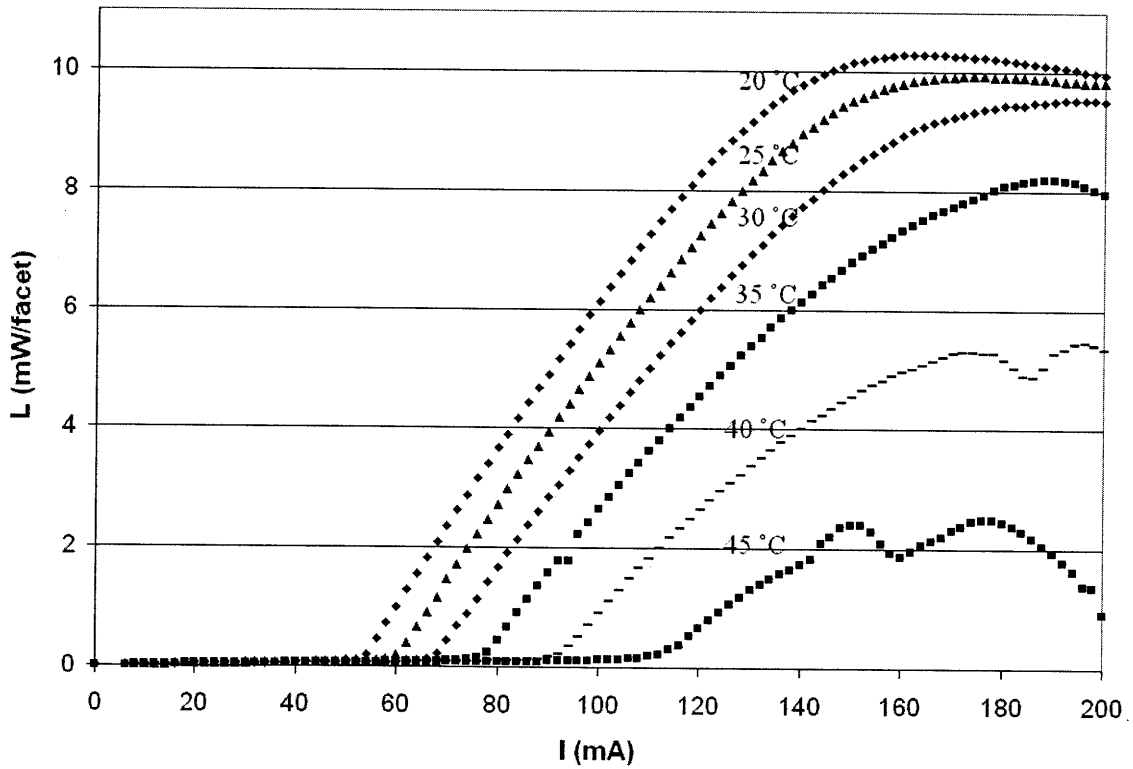


Figure 5-12: Light output characteristic as a function of stage temperature for an 1170 μm long, 6.8 μm wide CC ridge laser (CC1) measured under continuous-wave conditions.

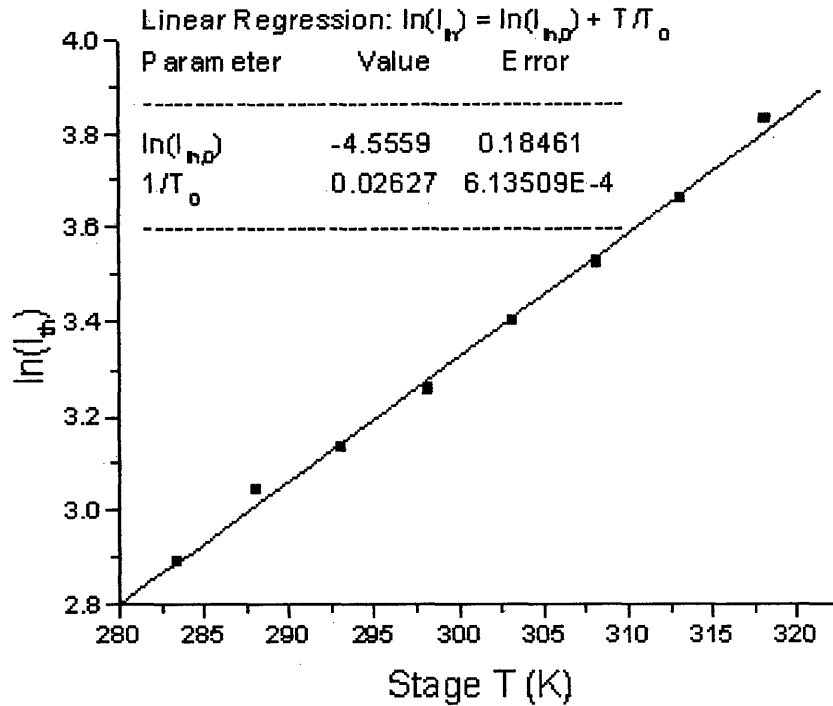


Figure 5-13: $\ln(\text{Threshold current})$ as a function of stage temperature for a continuous-wave tested conventionally-cleaved ridge laser (CC1).

Laser	Ridge Width(μm)	Length(μm)
CC1	6.8	842.3
CC2	6.8	1169.7
CC3	6.8	1169.7
CC4	6.8	842.3

Table 5-1 Dimensions of CC lasers that underwent characterization at different stage temperatures.

The characteristic temperatures of these CC lasers are rather low. For state of the art InP-based MQW ridge laser designs with facet coatings, T_0 s of greater than 50 K are commonly achieved. There are several improvements which could be made to the laser to improve T_0 . One way to increase T_0 would be to implement a current confinement structure to reduce current spreading.⁵ For instance, by making the

⁵It should be noted that this thesis work was focussed on demonstrating the proof of concept of

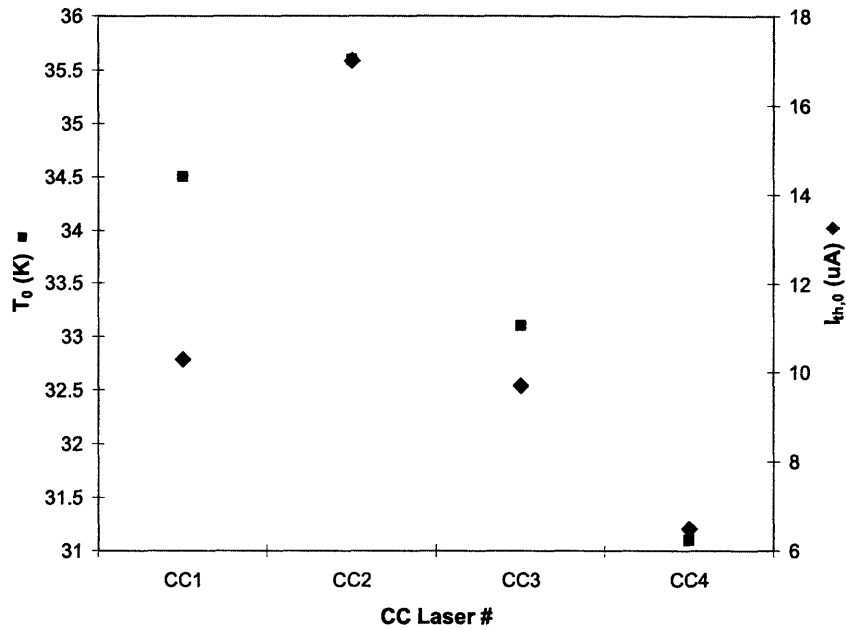


Figure 5-14: Characteristic temperatures, T_0 , and the 0 K threshold currents, $I_{th,0}$, of four conventionally cleaved ridge lasers tested under continuous-wave conditions.

semiconductor regions below the BCB layers resistive (Figure 4-10e) (i.e., by ion or proton implant), would direct the current to the active region of the device under the ridge where carrier recombination translates into lasing. This type of current confinement structure is typically incorporated in commercial laser designs. Another improvement that could be made to achieve better thermal performance is by lowering the laser diode series resistance. With the characterization of the ohmic contacts (Figure 4-11, 4-14) showing the contact resistivity roughly an order of magnitude higher than is typically seen in commercial ohmic contacts, this presents one logical area for device improvement and a potential increase of T_0 .⁶

The differential efficiency, η_d , is related to the characteristic temperature, T_1 , through the expression

a laser on silicon. Thus, the laser design used was simple and a number of improvements could be made to achieve lower threshold currents and higher temperature operation.

⁶As current passes through a resistive region, power is dissipated causing the region to heat up. This heating up could cause a lower T_0 reading when using continuous-wave measurements to extract T_0 .

$$\ln(\eta_d) = \ln(\eta_{d,0}) - \frac{T}{T_1} \quad (5.8)$$

A line was fit to a plot of $\ln(\eta_d)$ vs. T , and values of 38.5 K (CC3) and 46.9 K (CC1) (Figure 5-15) were obtained for the characteristic temperature, T_1 .

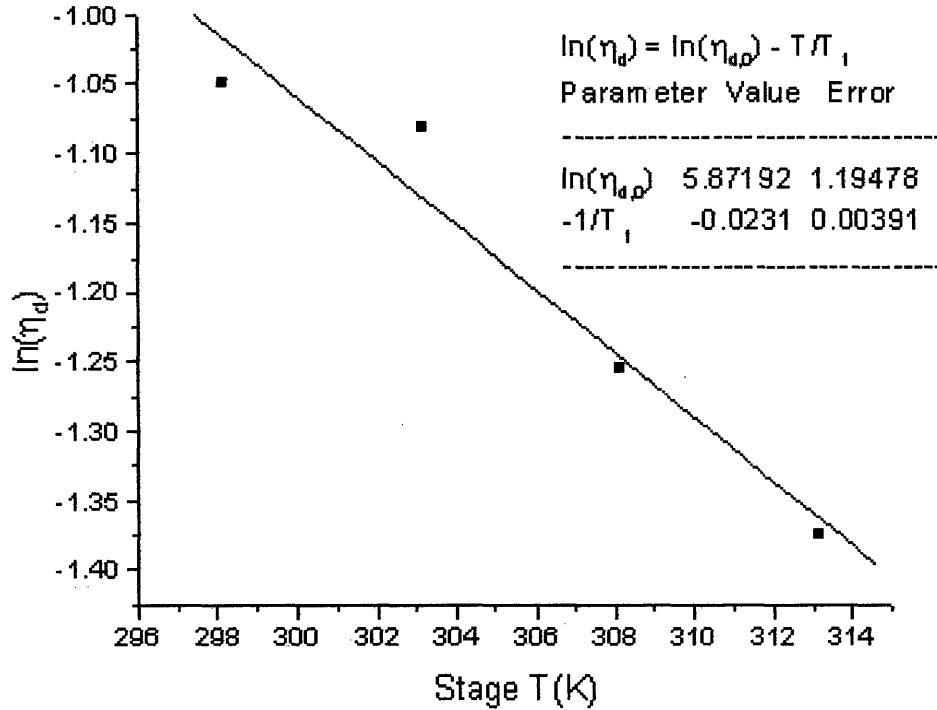


Figure 5-15: $\ln(\text{differential efficiency})$ as a function of stage temperature for a conventionally-cleaved ridge laser (CC1) tested under continuous-wave conditions.

Electrical Characterization

Current(I)-Voltage(V) characteristics were measured and analyzed for several CC ridge lasers. Figure 5-16 shows the I-V with corresponding L-I characteristic for CC1 ridge laser. The diode has an observed turn-on voltage of approximately 0.8 V.

From the I-V characteristics, it is possible to extract electrical device parameters such as the diode's ideality factor, n , and the electrical series resistance, R_{series} . To accomplish this, the diode is modelled with the simple relation

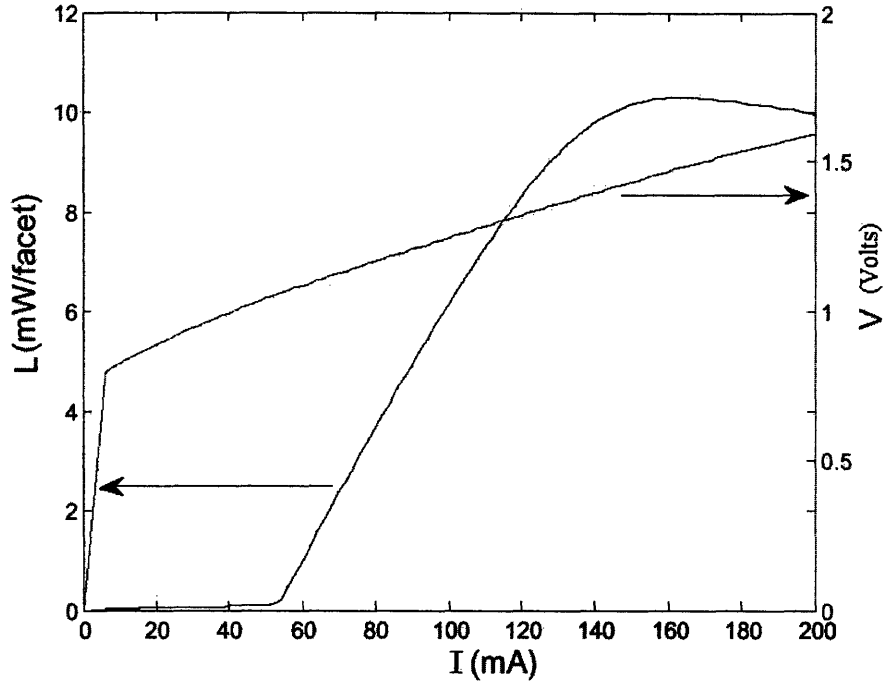


Figure 5-16: Light output and current-voltage characteristics for a ridge laser (CC1) measured at a stage temperature of 20 °C and under continuous-wave conditions.

$$I = I_0 \left(e^{\frac{qV_d}{nkT}} - 1 \right) \quad (5.9)$$

where V_d is the voltage across the diode, and I_0 is the diode's saturation current. The voltage applied to the contact of a diode is given by the relation

$$V = V_d + IR_{series} \quad (5.10)$$

where a voltage drop occurring between the contact probes and the diode is accounted for. To perform this device parameter extraction, it is useful to analyze a plot of IdV/dI vs. I . If the laser diode is operated below threshold and I is still much larger than I_0 , then the following relation holds

$$I \frac{dV}{dI} = \frac{nkT}{q} + IR_{series} \quad (5.11)$$

If the laser diode is biased above threshold where I is much larger than I_0 , then the following relation applies[22]

$$I \frac{dV}{dI} = IR_{series} \quad (5.12)$$

The IdV/dI vs. I characteristic for the CC1 ridge laser is shown in Figure 5-17. The series resistance is approximately 4 Ohms and the ideality factor is 1.2. Similar

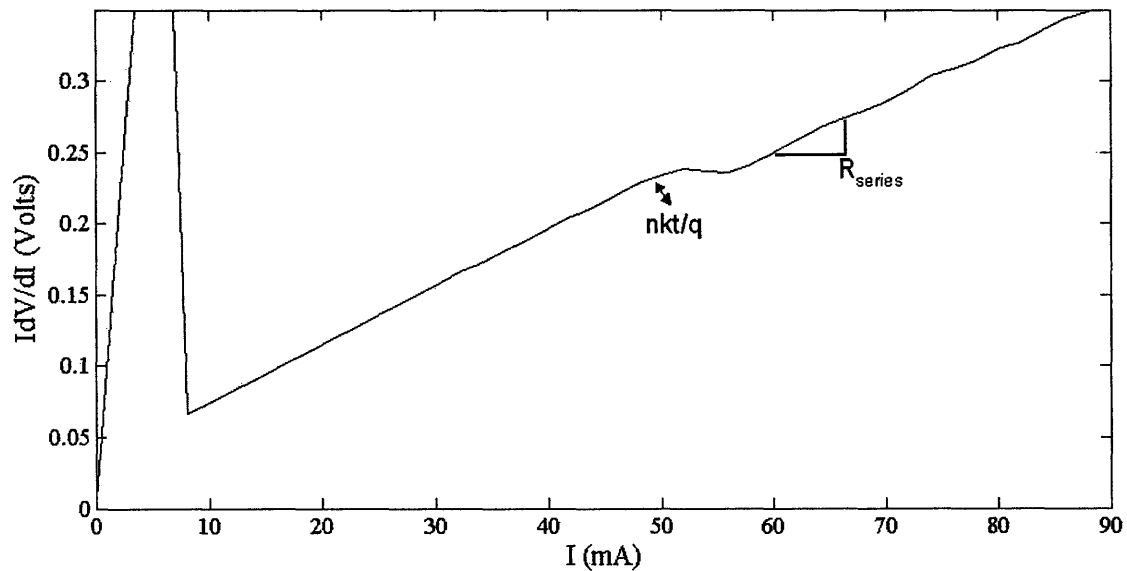


Figure 5-17: IdV/dI vs. I for a CC ridge laser (CC1) measured at room temperature and under continuous-wave conditions.

analysis was done for the other CC lasers and they were found to have series resistance values near 4 Ohms as can be seen in Figure 5-18.

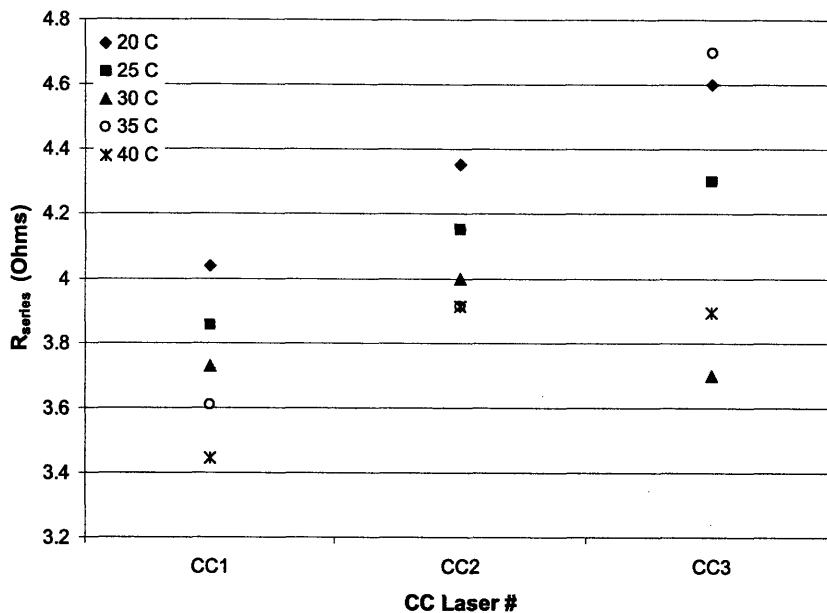


Figure 5-18: Diode forward series resistance as a function of stage temperature for three different conventionally cleaved ridge lasers, CC1, CC2, and CC3.

5.2.2 Micro-Cleaved Ridge Laser

When all the processes used to manufacture the micro-cleaved ridge laser work as designed, the quality of the ridge laser integrated onto a silicon substrate can be quite high. The analysis performed on the MC ridge laser, which had the most optimal processing, will first be described in detail. A top-down photograph of this micro-cleaved ridge laser is shown in Figure 5-19. After presenting the characterization results for this micro-cleaved ridge laser on silicon, other micro-cleaved ridge laser characteristics will be presented and the variation among them will be addressed.

Light Output Characteristics

Figure 5-20 shows the continuous-wave light output characteristics of micro-cleaved laser, MC6, on silicon at several stage temperatures. For this device, output powers as high as 26.8 mW (at $T = 10.3\text{ }^{\circ}\text{C}$) have been detected (from one facet) and the device lases at stage temperatures as high as $55\text{ }^{\circ}\text{C}$. By plotting dL/dI vs. I (Figure 5-21) for the output of one laser facet, and taking note of the dL/dI value just beyond

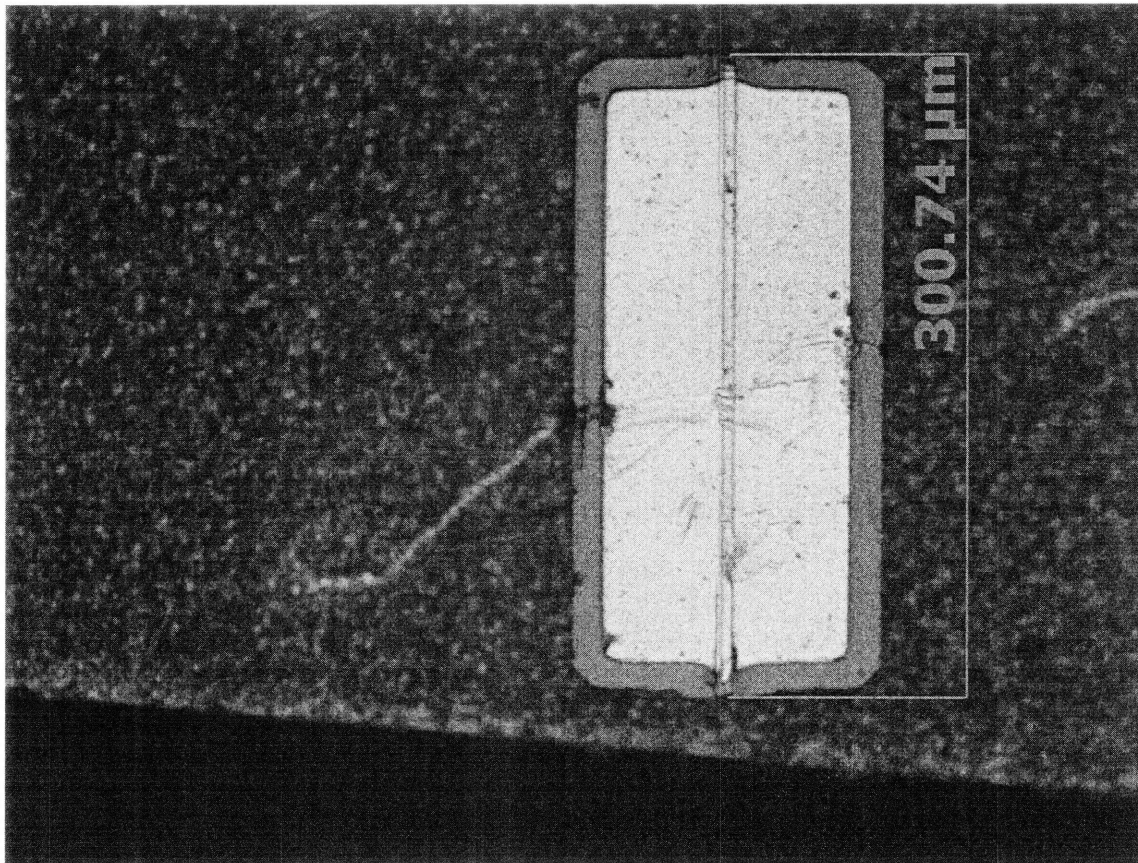


Figure 5-19: Top-down photograph of micro-cleaved ridge laser (MC6) bonded on silicon.

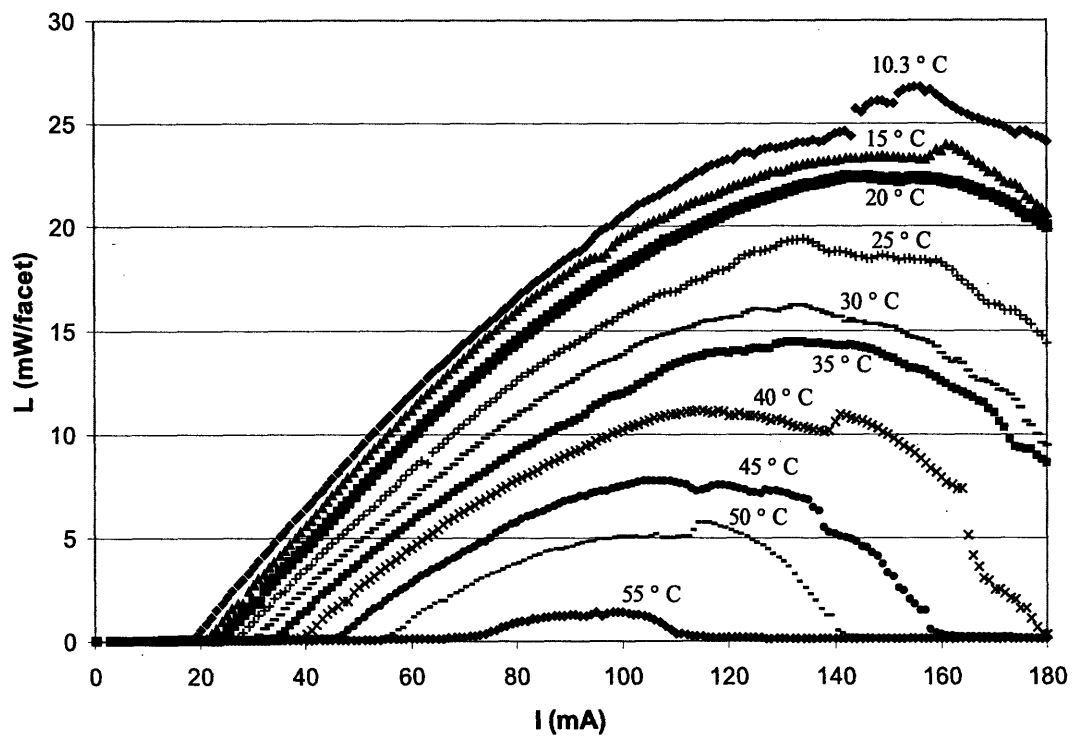


Figure 5-20: Light output characteristic for micro-cleaved ridge laser (MC6) on silicon as a function of stage temperature and under continuous-wave conditions.

threshold before the dL/dI starts to decrease as I is increased, a value of η_d was calculated using equation (5.2). Note that this dL/dI extracted from Figure 5-21 needs to be multiplied by two to account for the power output from both facets. At a stage temperature of 20 °C, η_d is 73%. At 10.3 °C, $\eta_d = 81\%$.

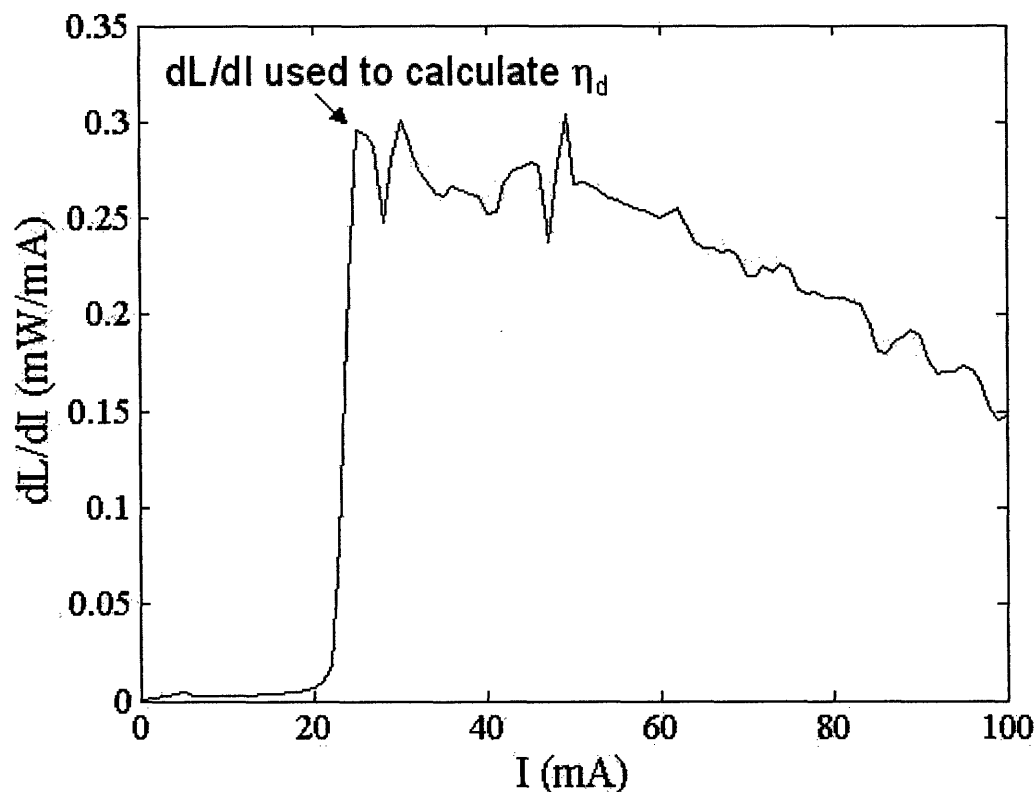


Figure 5-21: dL/dI vs. I characteristic for a micro-cleaved ridge laser (MC6) measured at a stage temperature of 20 °C and under continuous-wave conditions.

A T_0 of 38.1 K was extracted for MC6 by performing a linear fit to the $\ln(I_{th})$ vs. T plot (Figure 5-22) and using equation (5.7). From a linear fit to the $\ln(\eta_d)$ vs. T plot (Figure 5-23) and using relation (5.8), a T_1 value of 85 K was extracted for MC6. Both of these characteristic temperatures are higher than was measured for any of the CC ridge lasers. The improved thermal properties are believed to be due in part to the fact that silicon is a better thermal conductor than InP and that the metal bonding layers, namely gold, acts to spread heat from the laser active region. Gold has been shown by Tauber et al. to be an efficient heat spreader when used as an interface layer between an epitaxial laser structure and an InP substrate[25].

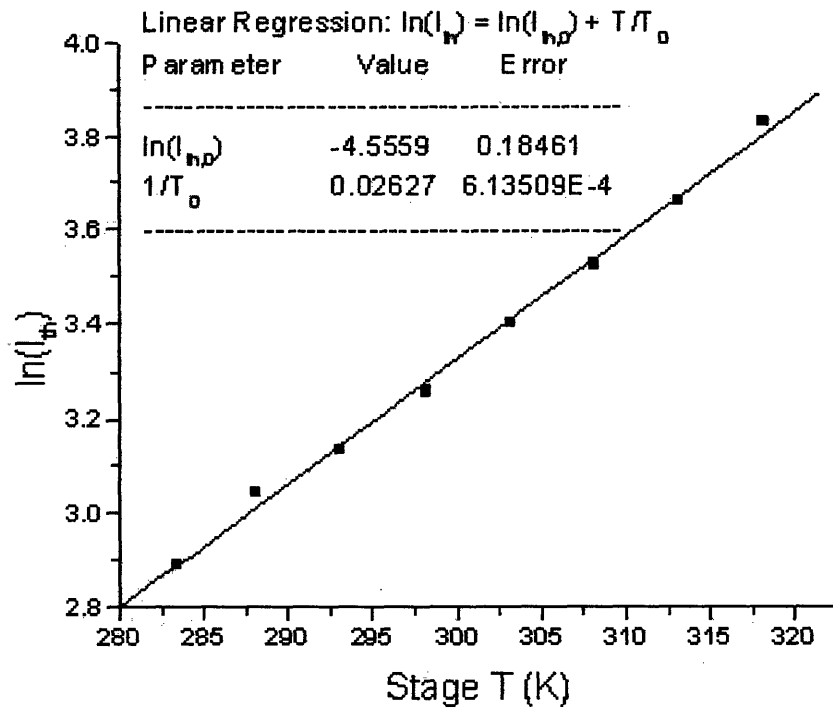


Figure 5-22: $\ln(\text{Threshold current})$ as a function of stage temperature for a continuous-wave tested micro-cleaved ridge laser (MC6).

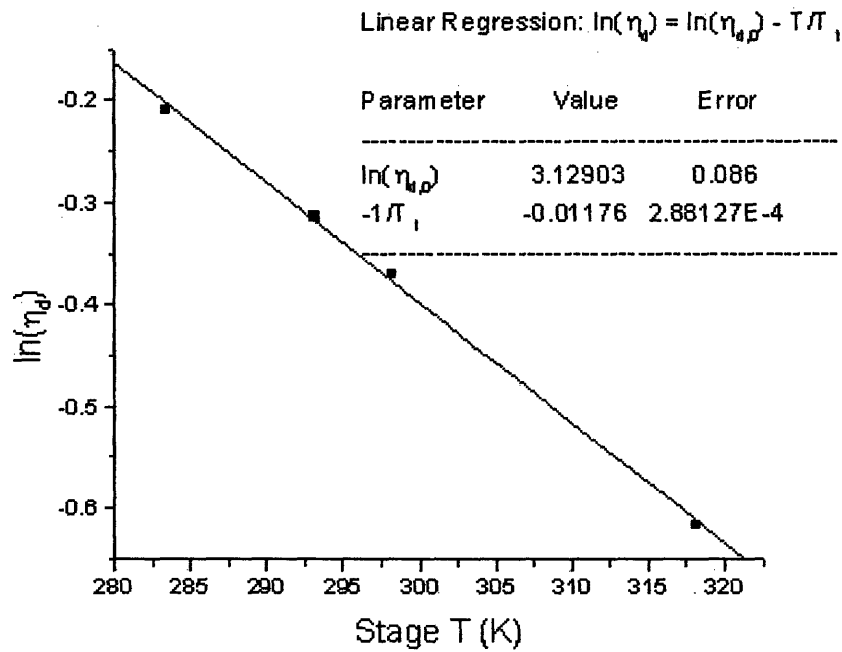


Figure 5-23: $\ln(\text{differential efficiency})$ as a function of stage temperature for a micro-cleaved ridge laser (MC6) tested under continuous-wave conditions.

Pulse measurements were made of the micro-cleaved ridge laser at a number of stage temperatures as is shown in Figure 5-24.

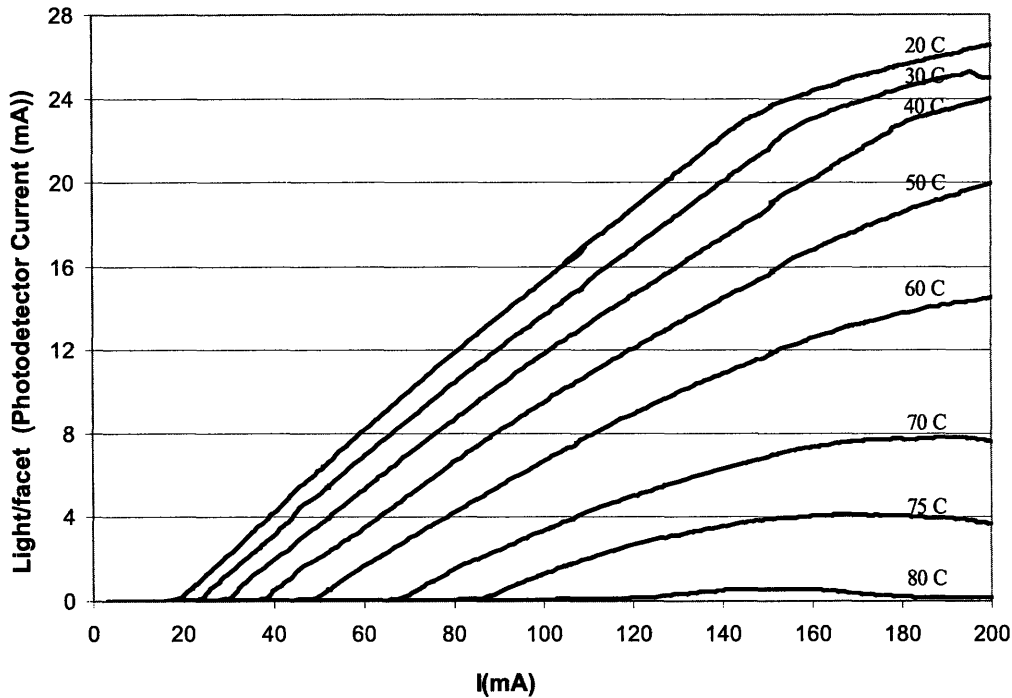


Figure 5-24: Light output characteristic for micro-cleaved ridge laser (MC6) on silicon as a function of stage temperature and under pulse conditions.

Pulsed lasing occurred to a temperature of at least 80 °C. Since 80 °C was the temperature limit for the stage thermoelectric cooler (TEC), testing was not carried out at higher temperatures. Taking note of the threshold current values at the various stage temperatures, a value of T_0 equal to 42.9 K was extracted. This measurement of T_0 is thought to be a more accurate estimate than that made under continuous-wave conditions. This follows from the fact that pulsed laser testing prevents the laser diode junction from heating up well-beyond the stage temperature as can happen when the diode is continuous-wave biased.

Electrical Characterization

The I-V and corresponding L-I characteristic for the MC6 ridge laser are shown in Figure 5-25. The I-V characteristic is very clean with the diode exhibiting a turn on

voltage of 0.8 V.

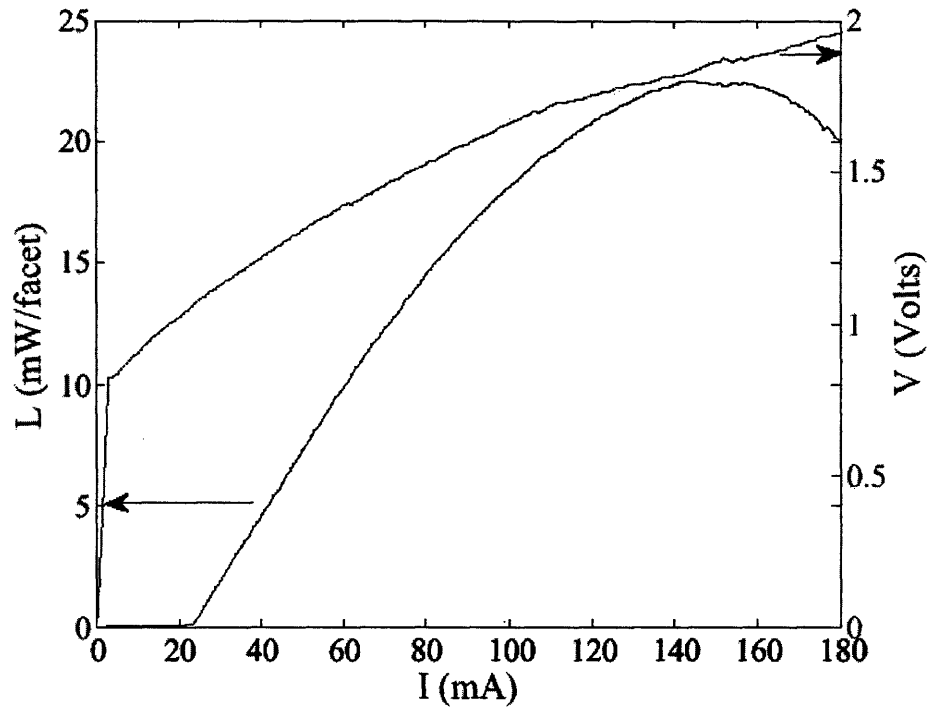


Figure 5-25: Light output and current-voltage characteristics for a micro-cleaved ridge laser (MC6) measured at a stage temperature of 20 °C and under continuous-wave conditions.

Performing the derivative analysis (Figure 5-26) of the electrical characteristics, a value of 8.8 Ohms is extracted for the diode series resistance and a value of 1.3 for the diode ideality factor.

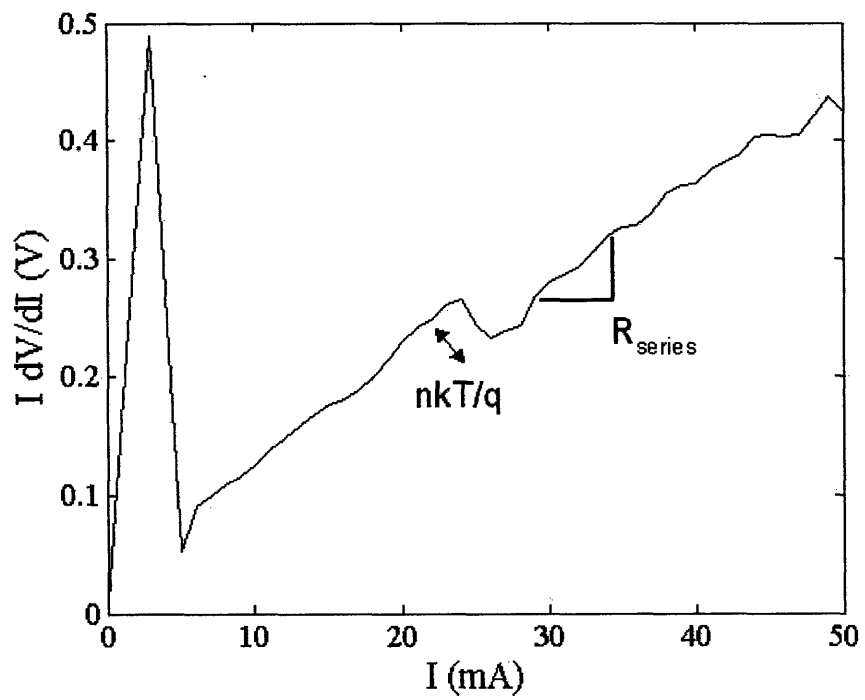


Figure 5-26: $I \frac{dV}{dI}$ vs. I for a micro-cleaved ridge laser (MC6) on silicon measured at a stage temperature of 20 °C and under continuous-wave conditions.

5.2.3 Comparison of the Micro-Cleaved Ridge Lasers

In total, nine micro-cleaved ridge lasers were assembled on silicon substrates. Of these nine lasers, six resulted in lasing. The dimensions of these six micro-cleaved lasers are shown in Table 5-2.

Laser	Ridge Width(μm)	Length(μm)
MC1	7.7	298.1
MC2	7.6	315.3
MC3	7.6	294.3
MC4	7.2	294.3
MC5	7.1	294.3
MC6	7.6	300.7

Table 5-2 Dimensions of the MC lasers that were characterized.

For comparison, the light output characteristics of all six micro-cleaved ridge lasers measured at several stage temperatures are shown in Figure 5-27. The threshold current values for the six MC ridge lasers are plotted as a function of stage temperature in Figure 5-28. To give the reader an idea of the spread in threshold currents, I_{th} measured at a stage temperature of 20 °C varies from 23 mA for MC1 and MC6, the two best MC lasers, to 43 mA for MC4. The differential efficiency values for the six MC ridge lasers are plotted in Figure 5-29. To give the reader an idea of the spread in differential efficiencies, η_d measured at a stage temperature of 20 °C varies from 73% for MC6, the best MC laser to 23% for MC5. The characteristic temperature (T_0) values for the lasers are plotted in Figure 5-30.

The variation in micro-cleaved laser characteristics, such as threshold current and peak output power, is believed to be tied to variation of the electrical contact properties among the devices. To help understand these variations, it is instructive to compare the micro-cleaved ridge laser I-V characteristics. Both the L-I and the I-V characteristics of all six tested micro-cleaved ridge lasers are shown in Figure 5-31. Note that all of these measurements were made at a stage temperature of 20 °C.

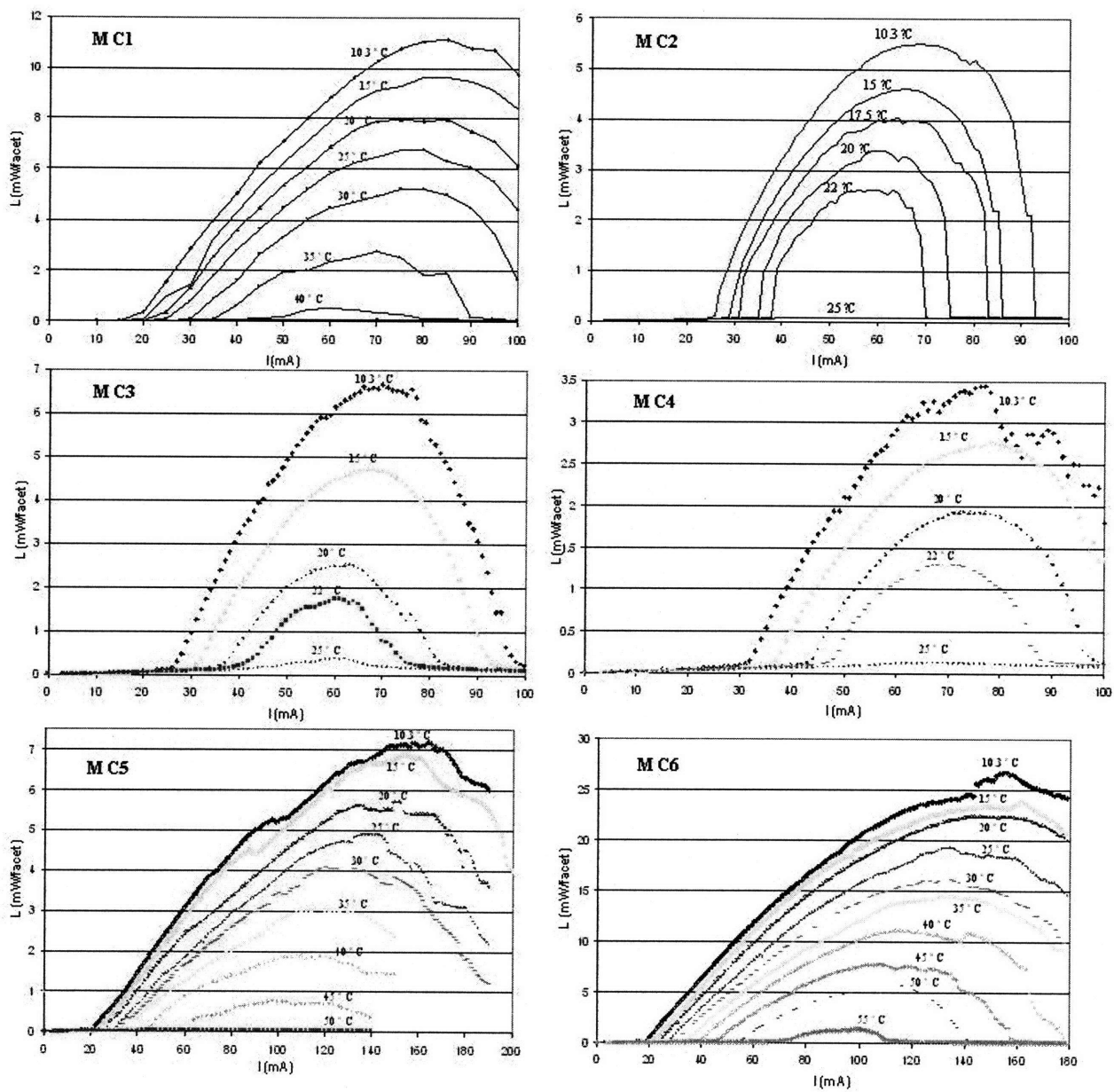


Figure 5-27: Light output characteristics for all tested micro-cleaved ridge lasers as a function of stage temperature measured under continuous-wave conditions.

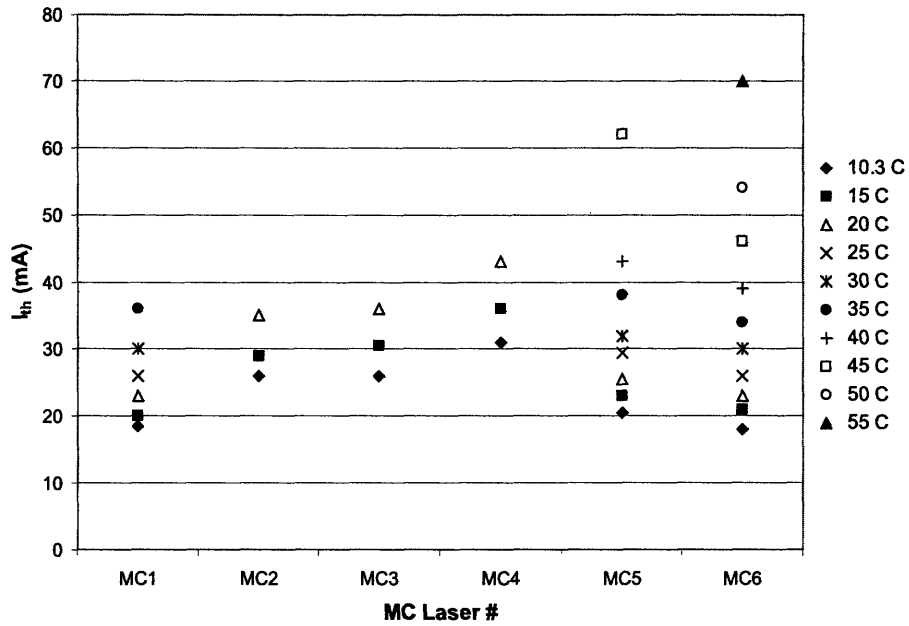


Figure 5-28: Threshold current, I_{th} , as a function of stage temperature extracted from continuous-wave measurements of six micro-cleaved ridge lasers on silicon.

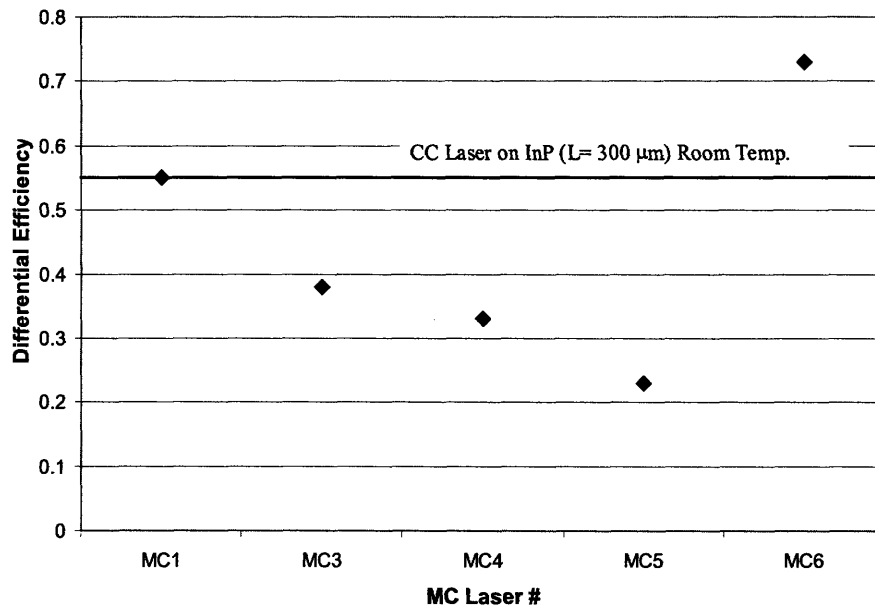


Figure 5-29: Differential efficiency, η_d , at a stage temperature of 20 °C extracted from continuous-wave measurements of micro-cleaved ridge lasers on silicon.

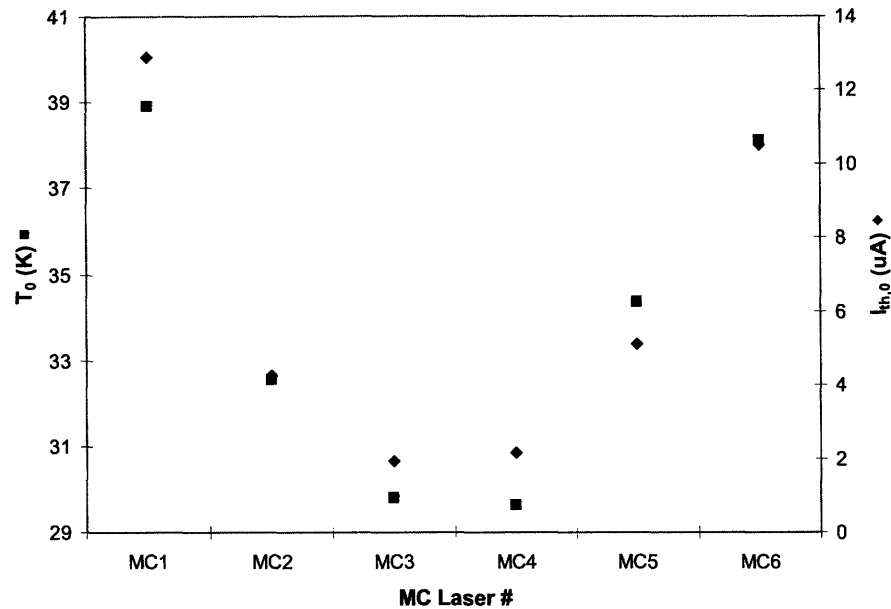


Figure 5-30: Characteristic temperatures, T_0 , and the 0 K threshold currents, $I_{th,0}$, extracted from continuous-wave measurements of six micro-cleaved ridge lasers on silicon.

The first parameter to evaluate with respect to the laser diode I-V characteristics is the diode turn-on voltage (Figure 5-32). The best performing MC laser in terms of output power and maximum temperature operation, MC6, has a sharp 0.8 V turn-on voltage. All of the other diodes have higher turn-on voltages. In some cases, such as for MC2 and MC5, the turn-on voltages are considerably higher. A higher diode turn-on voltage is one sign of poor electrical characteristics. Another sign of poor electrical characteristics is high diode series resistance. The series resistance for the six micro-cleaved ridge lasers are shown in Figure 5-33. Of note is the fact that MC4, which has the lowest T_0 and highest I_{th} , also has the highest diode series resistance.

Another characteristic to evaluate with respect to the I-V curve is how clean the curve is. Regarding this point, MC2 and MC5 have very noisy or unclean I-V characteristics. Noisy characteristics suggest issues with the electrical contact to the diode. They are problematic because they can result in resistive heating of the diodes, which ultimately leads to increased threshold currents and lower peak output powers. Although the stage temperature was kept constant during these measurements, it

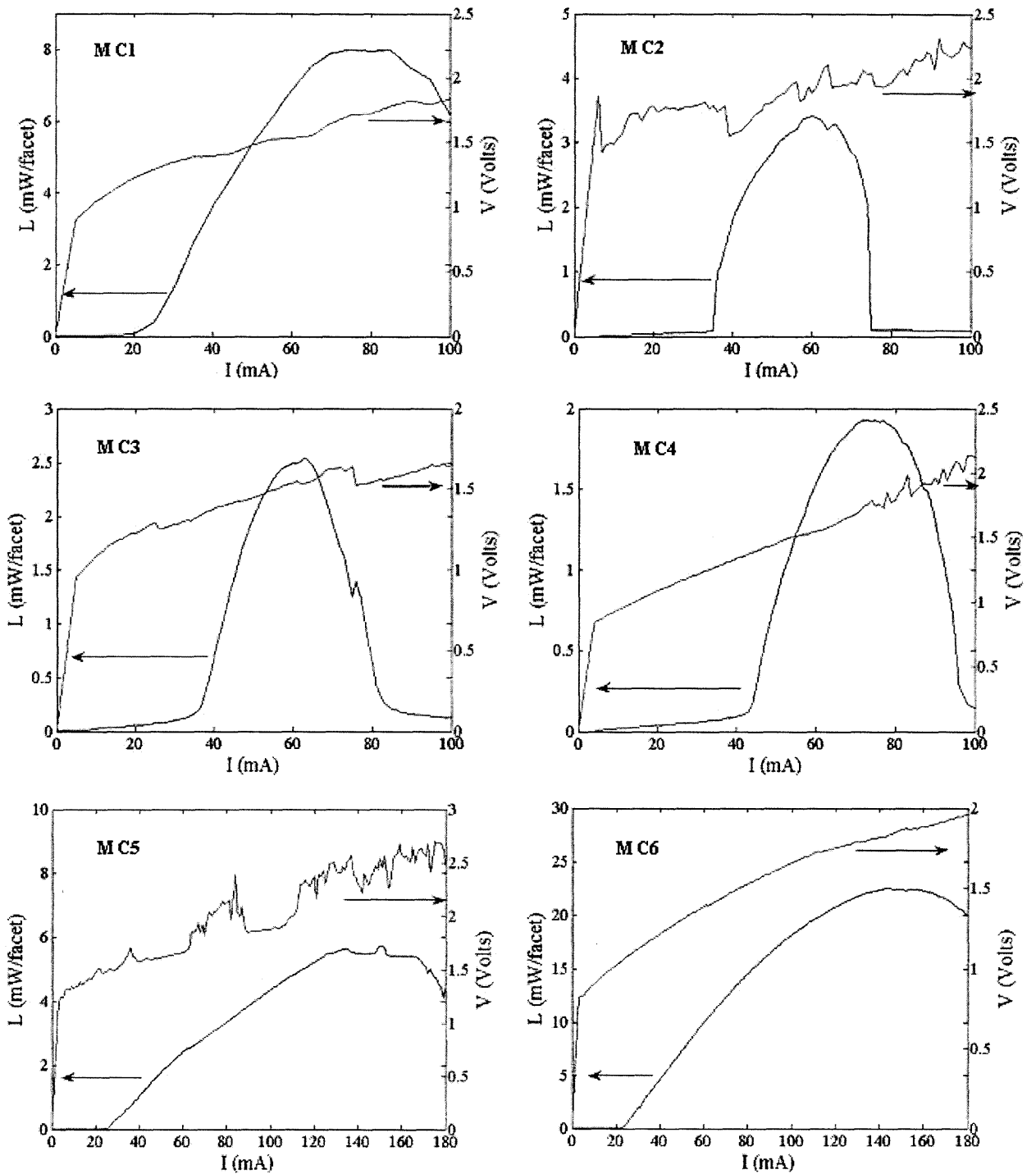


Figure 5-31: Light output and current-voltage characteristics for all micro-cleaved ridge lasers measured at a stage temperature of 20 °C and under continuous-wave conditions.

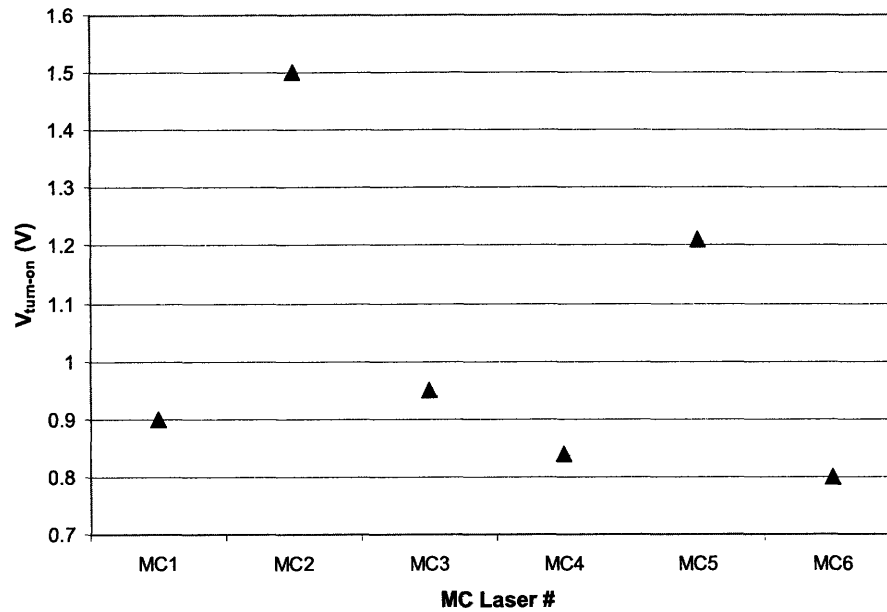


Figure 5-32: Turn-on voltages for for all micro-cleaved ridge lasers measured at a stage temperature of 20 °C and under continuous-wave conditions.

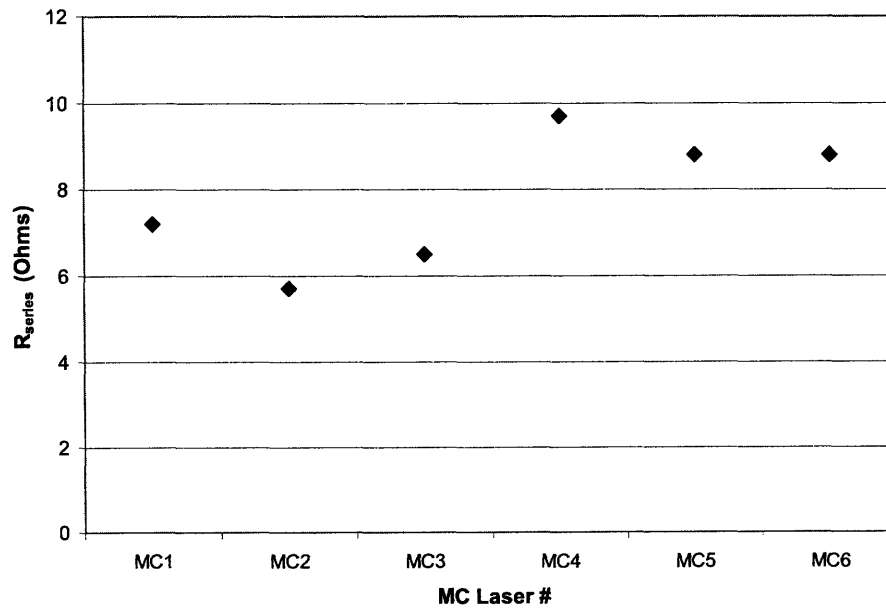


Figure 5-33: Laser diode series resistance for for all micro-cleaved ridge lasers measured at a stage temperature of 20 °C and under continuous-wave conditions.

is very likely that the junction temperature rose significantly due to these resistive heating effects.

Identifying the electrical contact as the discriminating characteristic between the realized micro-cleaved ridge lasers, it is useful to consider the possible mechanism resulting in poor contacts. One possible cause could be variation in the micro-cleaved laser to silicon bonding process. Poorly bonded lasers could have loose electrical connections and thus noisy I-V characteristics. They would be less well heat sunk and thus their maximum operating temperatures would be low. Their threshold currents would also be higher and their differential efficiencies lower due to poor heat sinking. Limitations with the BCB planarization process seems to be another possible root cause of the electrical contact quality variability. The main problem with the planarization process is that all of the development work was carried out on small area samples (i.e., areas less than or equal to 1 cm^2). Endemic to the BCB spin-coat process is the presence of an edge bead. Right from the beginning, regions along the die edges on the order of 100s of μm are unusable due to this edge bead (up to approximately $3000 \mu\text{m}$). In addition, the limited performance (i.e., repeatability and uniformity) of the Plasmatherm dry etching tool, resulted in large variation in the BCB thickness across the sample as is shown in Figure 5-34.

Due to the variation in the BCB thicknesses across the sample, there exists a situation where, after the BCB etchback process, many devices still have BCB covering some if not all of the metal ridge contact. Thus, when the top large area electrical contact is deposited, this contact does not make a good contact to the ohmic metal ridge. This failure mechanism is clearly shown in a cross-sectional SEM shown in Figure 5-35. If the large area metallization does not contact the entire length of the ohmic ridge contact, then there will be a voltage drop occurring along the length of the ridge. This voltage drop can prevent areas of the device from being biased above threshold and diode turn-on.

If the BCB is overetched to avoid this problem, the step height between the BCB and the ohmic metal ridge contact will be too high when depositing the large area contact and can result in lateral gaps between the ohmic metal ridge and the large

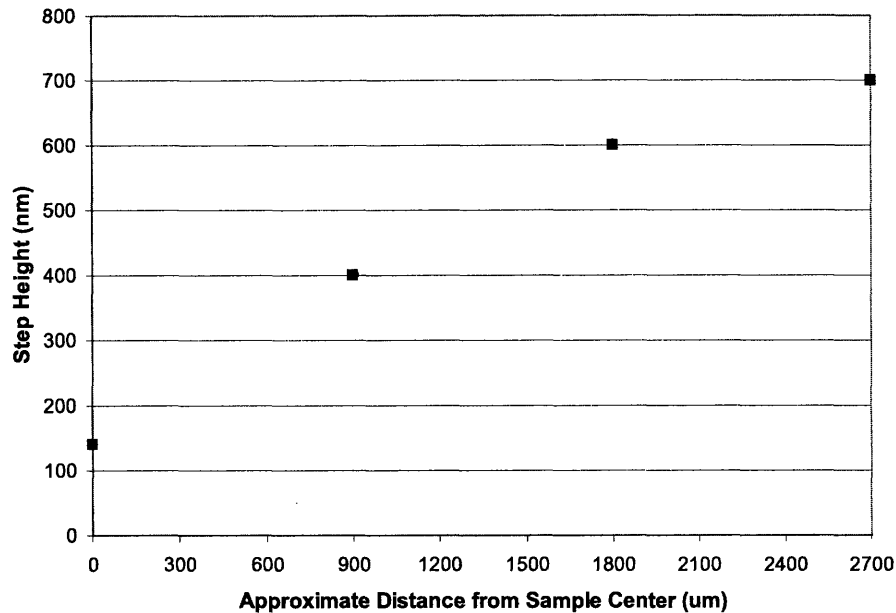


Figure 5-34: Step height of ridge to planarization layer following the BCB etch-back process. Note that the data point taken at 2700 μm from the sample center is 900 μm from the sample edge.

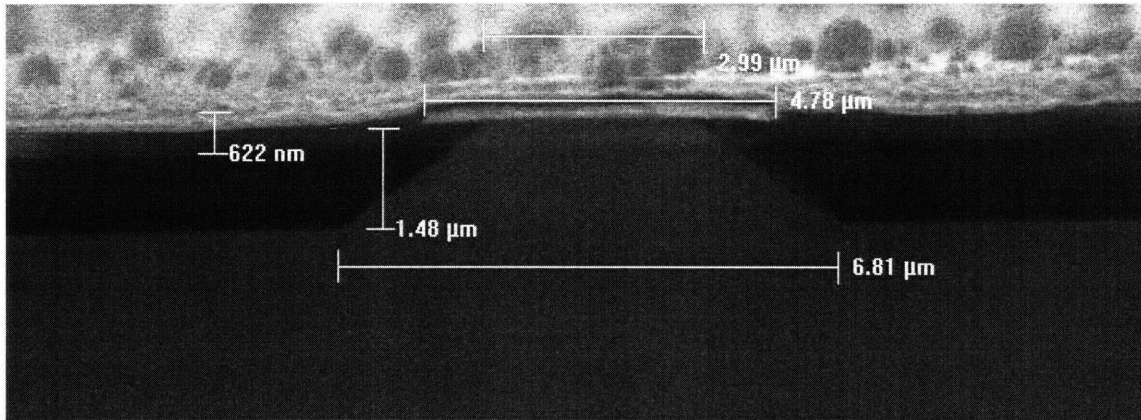
area contact.

For the micro-cleaved ridge lasers characterized here, care was taken to minimize this BCB to ohmic ridge contact step height. Therefore, it is not surprising that not all of the BCB was removed from the top of the ohmic metal ridge contact prior to the large area contact formation.

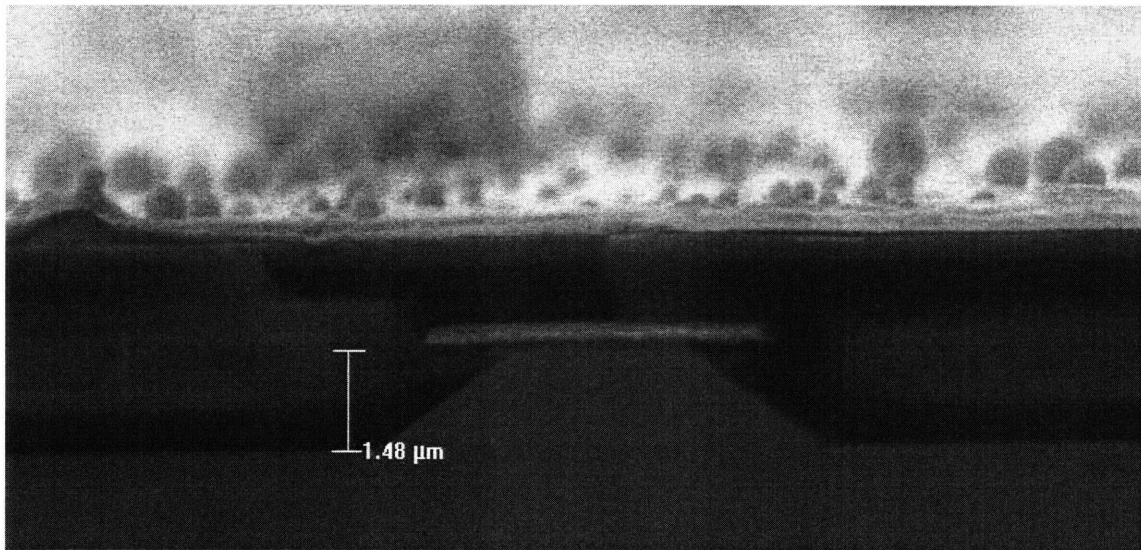
It is believed that by transferring this micro-cleaved ridge laser process to larger wafers (i.e., 2 inch diameter and greater) and by using higher quality, dedicated dry etch tools, significantly better planarization results would be achieved. Thus, the electrical characteristics across micro-cleaved lasers produced from a single wafer would also become more uniform.

With the less than ideal performance of MC2, MC4, and MC5 being attributed to contact properties,⁷ an explanation of the performance of the MC3 device needs to be made. MC3's I-V characteristics are not very noisy and MC3 has comparatively

⁷MC2 and MC5 have noisy I-V characteristics. MC4 has the highest series resistance and turn-on voltage of all the lasers.



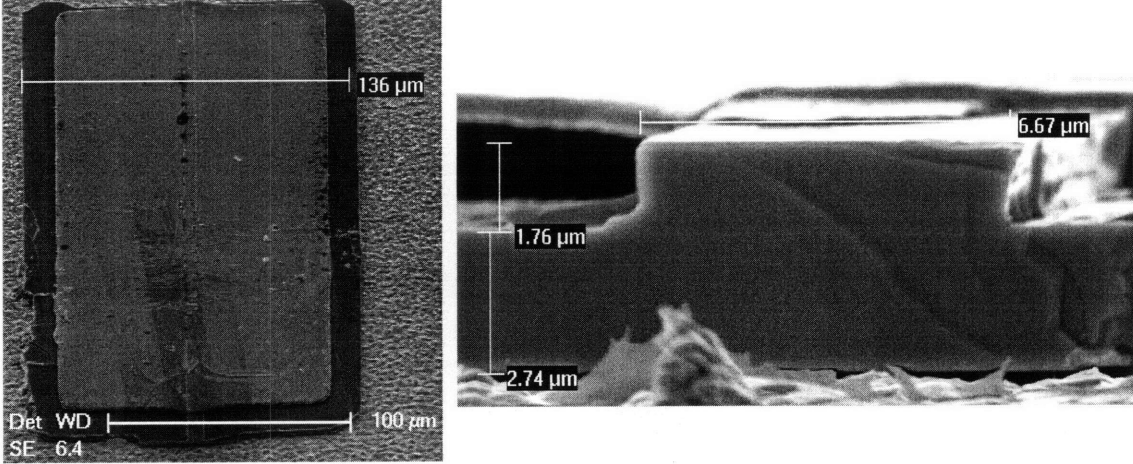
(a) Successful process.



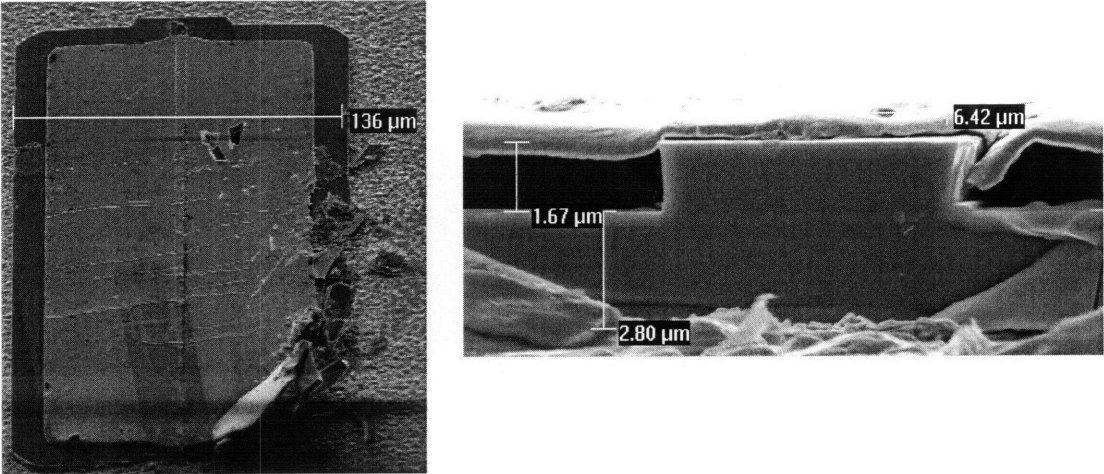
(b) Device process failure where BCB still covered the ohmic ridge contact.

Figure 5-35: Scanning electron micrographs (SEM) of the cross section of a ridge laser after the top large area contact formation process.

low R_{series} and $V_{turn-on}$, so problems with the electrical contact do not seem to be the issue. To investigate the devices further, SEMs were taken of the top-side as well as the output facets of MC3, MC4, MC5, and MC6 (Figure 5-36, 5-37). The facets of these devices look good with the exception of MC3 which has some significant roughness. The presence of this facet defect seems to explain MC3's poor thermal performance.

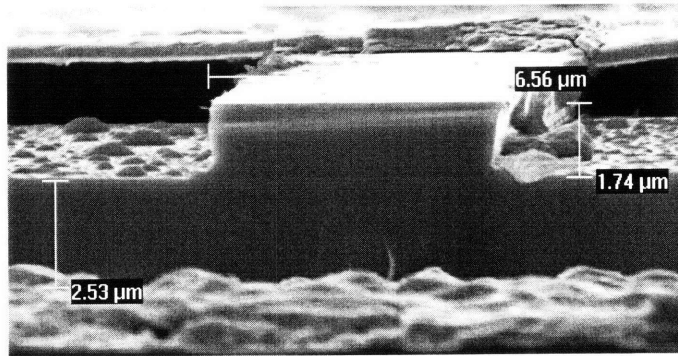
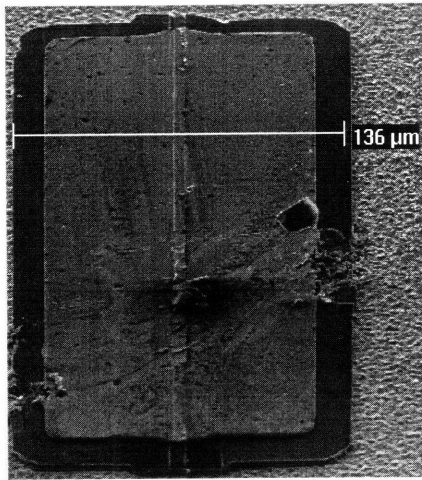


(a) MC3

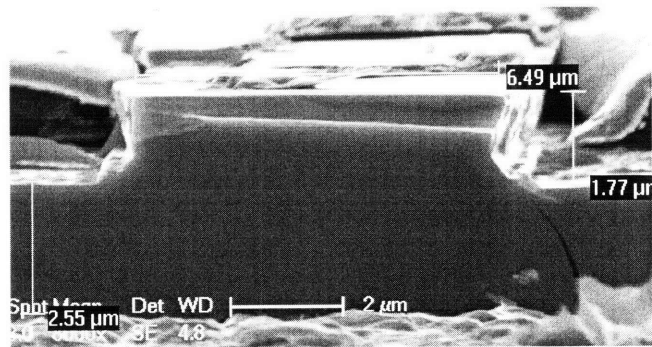
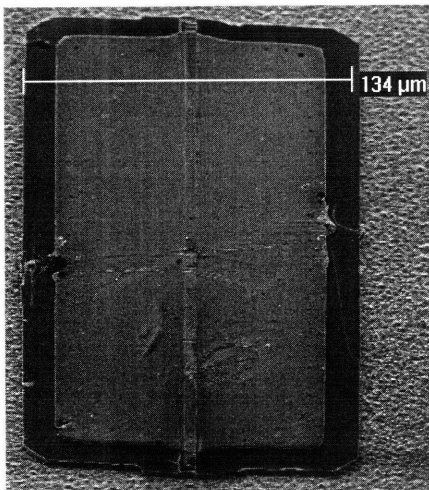


(b) MC4

Figure 5-36: SEMs of micro-cleaved ridge lasers on silicon (MC3, MC4).



(a) MC5



(b) MC6

Figure 5-37: SEMs of micro-cleaved ridge lasers on silicon (MC5, MC6).

Chapter 6

Enabling Higher Density

Integration - Magnetically Assisted Statistical Assembly

A hybrid approach for achieving optoelectronic integration has been proposed. The fundamental building blocks for this system have been realized, namely the highly integrable ridge laser platelets and the dielectric waveguides[15]. Up until this point, the manipulation of these platelets has involved a manual pick-and-place assembly technique. However, the question remains, is there a way to achieve large scale optoelectronic integration with our hybrid integration approach? A technique which we believe will enable this large scale integration is referred to as Magnetically Assisted Statistical Assembly.

6.1 Magnetically Assisted Statistical Assembly

Magnetically Assisted Statistical Assembly (MASA) is a fluidic assembly technique having many similarities with the fluidic assembly techniques described in Chapter 2. However, the mechanism in MASA by which a device is ultimately retained at the target substrate is novel. The MASA technique utilizes the inherent properties of ferromagnetic thin films to aid in the retention of devices on a target substrate.

Especially suited to our hybrid integration approach, the MASA technique, shown simplistically in Figure 6-1, begins by optimally processing two separate semiconductor wafers. On the device wafer, devices are fully processed with a soft ferromagnetic film deposited on one side of them. On the other wafer, referred to as the target wafer, dielectric recesses having geometries corresponding to the devices are formed. At the bottom of these dielectric recesses are located patterned hard ferromagnetic films.

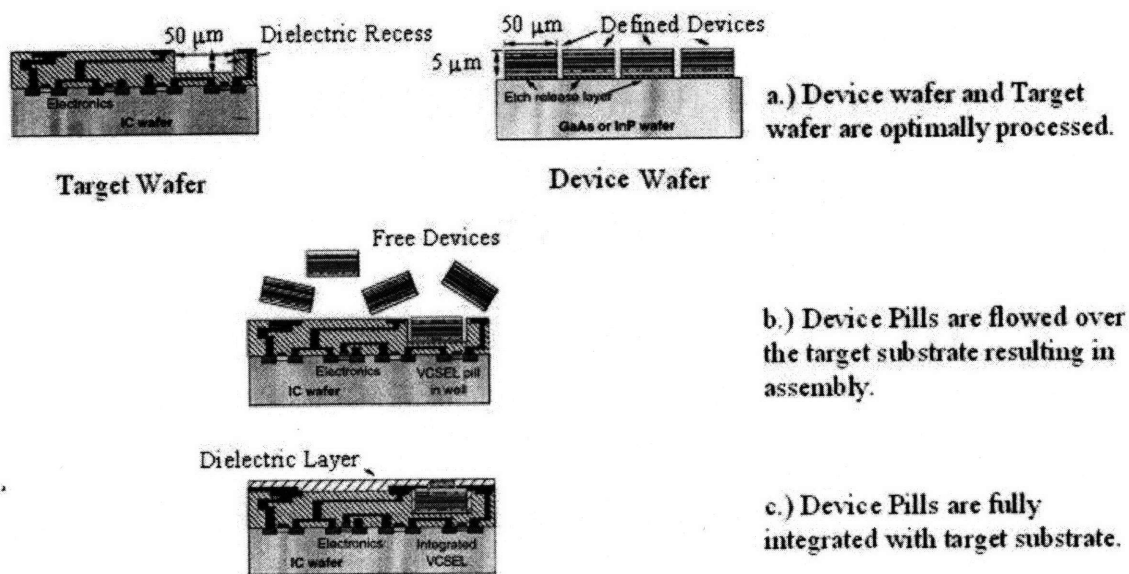


Figure 6-1: Magnetically assisted statistical assembly technique.

Once the devices are fully processed with an integrated magnetically permeable layer, they are etched free of their native substrate and collected in a solution. These freestanding devices are then flowed over the target wafer where they fall by gravity into recesses. Proper device orientation¹ and retention² in the recess is enabled by the magnetic force acting between the two aforementioned magnetic films.

¹In theory, pills are assembled and then the target substrate is turned upside down so that incorrectly oriented pills fall off the target wafer due to the force of gravity. Thus, for MASA to work the magnetic force density should be larger than the force density due to gravity only for separations less than the thickness of a typical pill.

²One can think of this retentive force as the same force encountered when a big bulk permanent magnet attracts a magnetically permeable material. The only difference is that the magnets used in MASA have dimensions on the order of microns.

6.1.1 Properties of the Ferromagnetic Films used in MASA

Two types of ferromagnetic films are utilized in MASA. The magnetic film on the target substrate acts as the permanent magnet in the system. Thus, it is desirable that this film have high remanent magnetization and reasonably high coercivity. On the device, a soft magnetic film is desired. The optimal magnetic properties for this film are low remanent magnetization, high permeability, and low coercivity. When considering these films, both the magnitude and the orientation of the magnetic properties of these films must be considered. In terms of the magnetization orientation in these films, there are two extremes. In-plane films define a class of magnetic films that are magnetized easily in a direction in the film plane.³ Perpendicular films label a class of magnetic films magnetized easily in a direction out of the plane of the film.⁴

The orientation of these films can depend on several factors such as the shape of the film, stresses between the magnetic film and the substrate upon which it was deposited, the crystalline nature of the film, as well as surface effects that occur when ultra-thin layers are used[72, 17]. For ferromagnetic thin films, the dominant factor in determining the orientation is usually the shape of the film. This dependence of the magnetic properties on the shape of the magnetic material is referred to as shape anisotropy. Shape anisotropy causes the magnetization to orient along the longest dimension of the magnetic material. Due to shape anisotropy, most magnetic thin films, especially homogeneous films have in-plane preferential characteristics. To create perpendicular magnetic films, effects such as surface anisotropy, magneto-crystalline anisotropy, or magneto-elastic anisotropy must be utilized to overcome the dominant in-plane shape anisotropy.⁵

A couple of different materials have been evaluated for use as the hard magnetic film in the MASA technique. The magnetic films considered are a Co/Pd multi-layer film which was produced by Prof. T.C. Chong at the Data Storage Institute at the

³In-plane hard magnetic films have higher remanence directed in the film plane.

⁴Perpendicularly oriented hard magnetic films can have high remanent magnetization directed out of the plane of the film and little or no remanence directed in the plane of the film.

⁵In general, in-plane oriented thin films are simpler to produce than perpendicularly oriented thin films.

National University of Singapore, and a SmCo film, which was produced by Prof. Cadieu of the Department of Physics at Queens College of the City University of New York (CUNY). Both films have been patterned, the former patterned into an array of stripes geometry⁶, and the latter film patterned into an array of squares⁷ geometry as is shown in Figure 6-2.

Vibrating sample magneto-meter (VSM) measurements have been performed on both samples and the results are shown in Figure 6-3. From these VSM measurements, the perpendicular anisotropy present in the Co/Pd multi-layer film and the in-plane anisotropy present in the SmCo film are obvious.

6.1.2 Theory Underlying the MASA Technique

The simple system used to analyze the magnetic retention force is shown in Figure 6-4. In short, a compound semiconductor device block having a soft magnetic film with permeability, μ_S , is situated at a height, g , above a target substrate having a hard magnetic film with magnetization, \vec{M} . The expression for the magnetic field resulting from the hard magnetic material has been modelled assuming this geometry.

Starting with Ampere's current law and applying the magneto-static approximation in every region of the system shown in Figure 6-2,

$$\nabla \times \vec{H} = \vec{J} + \frac{\partial \vec{D}}{\partial t} \quad (6.1)$$

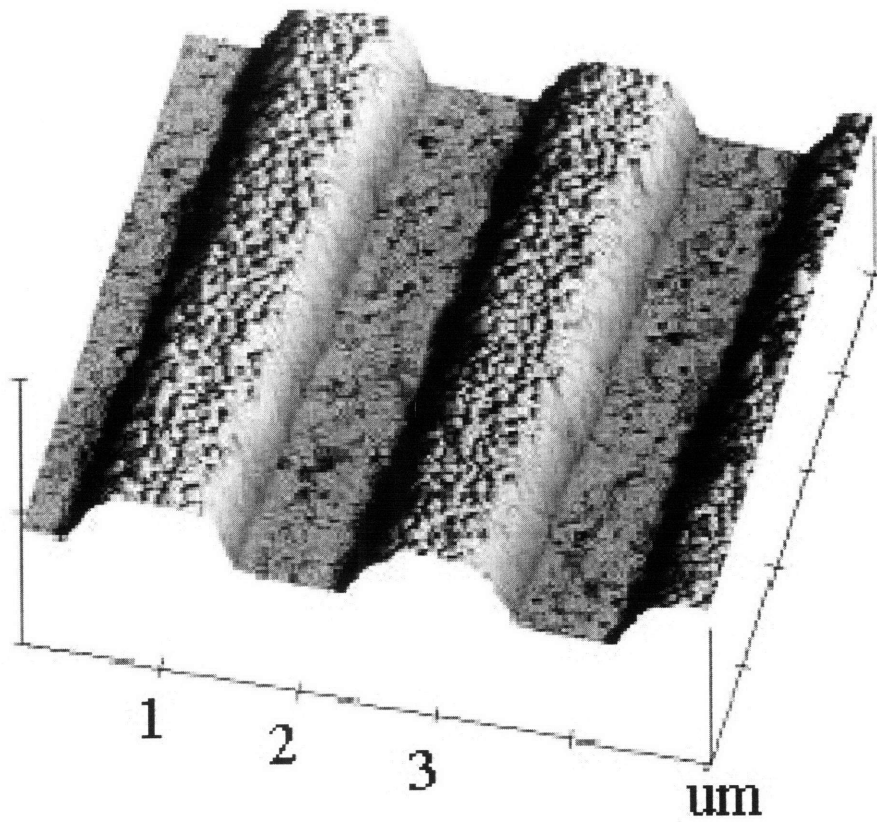
$$\nabla \times \vec{H} = \vec{J} \quad (6.2)$$

Since no free current is assumed, the magnetic field \vec{H} can then be written in terms of a quantity referred to as the magnetic scalar potential, ψ ,

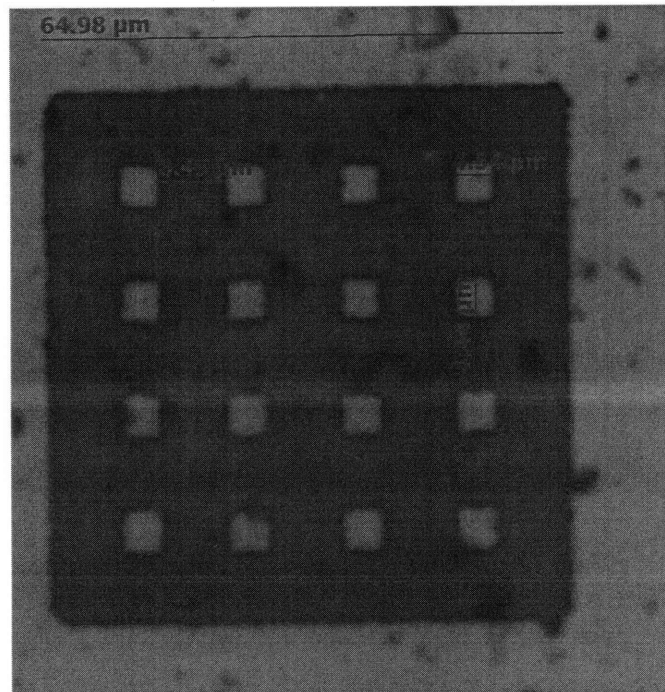
$$\vec{H} = \nabla \psi \quad (6.3)$$

⁶This film was patterned by ion milling at the National University of Singapore.

⁷Processing techniques have been developed to pattern the SmCo films by photolithography and wet etching. Details on these processes are included in Appendix C.

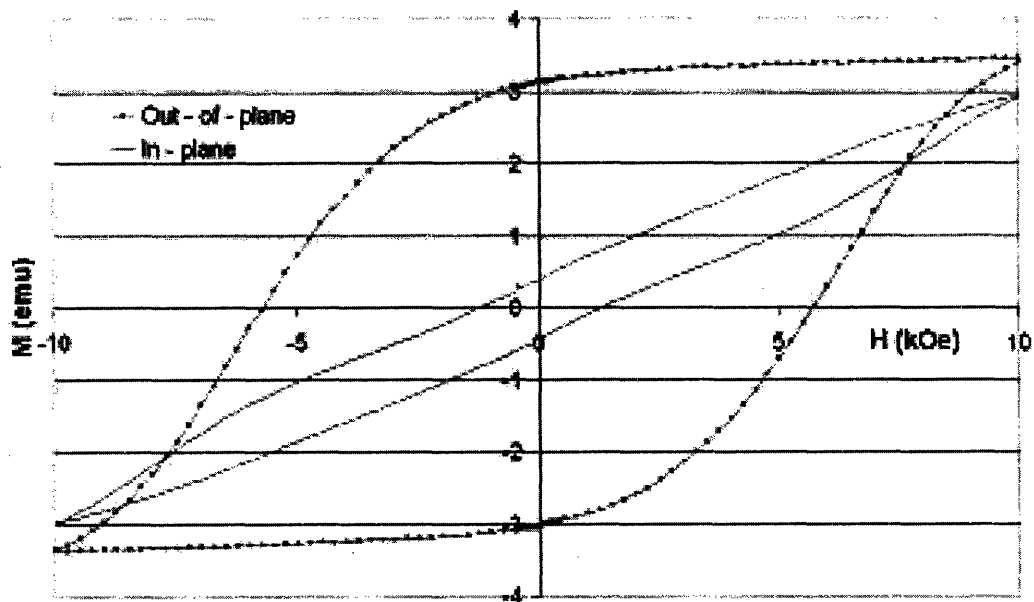


(a) Co/Pd film patterned into an array of stripes.

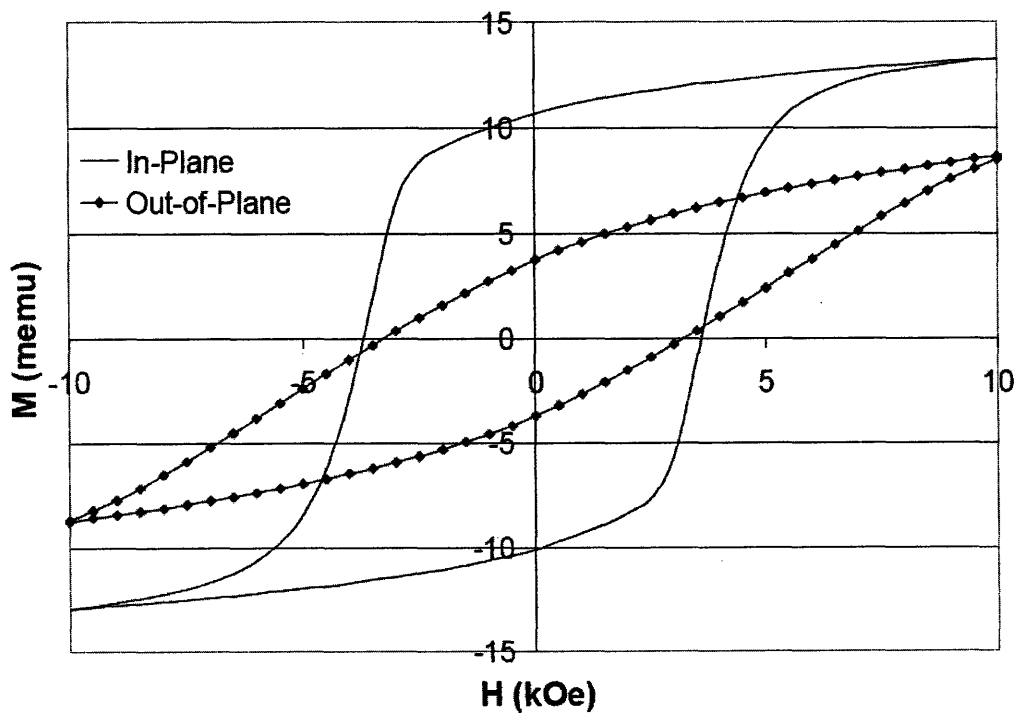


(b) SmCo film patterned into an array of squares.

Figure 6-2: Patterned hard magnetic films.



(a) Co/Pd film patterned into an array of stripes.



(b) SmCo film patterned into an array of squares.

Figure 6-3: Magnetization vs. Applied Magnetic Field for patterned hard magnetic films.

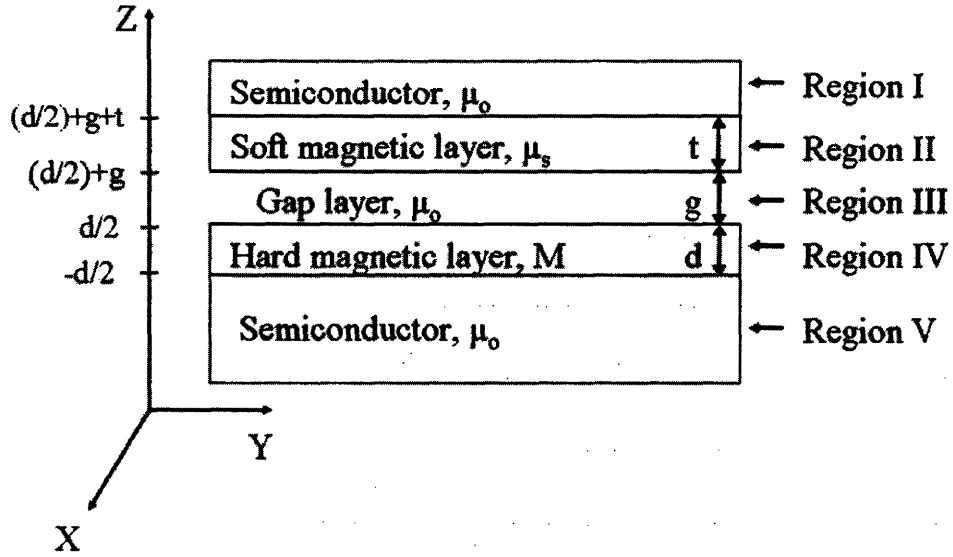


Figure 6-4: Schematic of the system under consideration for the magnetic force modeling[1].

Gauss' law for the magnetic field states

$$\nabla \cdot \vec{B} = 0 \quad (6.4)$$

The constitutive relation between the magnetic flux density, \vec{B} , and the magnetic field, \vec{H} , is

$$\vec{B} = \mu_0(\vec{H} + \vec{M}) \quad (6.5)$$

where \vec{M} is the magnetization and μ is the permeability of free space. Combining Gauss' law for the magnetic field and the constitutive relation

$$\nabla \cdot \vec{B} = \nabla \mu_0(\vec{H} + \vec{M}) = 0 \quad (6.6)$$

$$\mu_0(\nabla \cdot \vec{H} + \nabla \cdot \vec{M}) = 0 \quad (6.7)$$

$$\nabla \cdot \vec{H} = -\nabla \cdot \vec{M} \quad (6.8)$$

A relation between the magnetic scalar potential and the magnetization is deduced

$$\nabla \cdot (-\nabla \psi) = -\nabla \cdot \vec{M} \quad (6.9)$$

$$\nabla^2 \psi = \nabla \cdot \vec{M} \quad (6.10)$$

The magnetization, \vec{M} , depends on the properties of the magnetic material and its geometry. By assuming an expression for the magnetization, relations for the scalar magnetic potential, ψ , the magnetic field, \vec{H} , and the magnetic flux density, \vec{B} , are deduced. Given expressions for the magnetic field, the magnetic retention force can be modelled using the Maxwell Stress Tensor approach. In the treatment considered here, an expression for \vec{M}_{IV} , the magnetization in Region IV, is assumed to have a periodic distribution related to the geometry of the hard magnetic film pattern. It is also assumed that \vec{M}_I , \vec{M}_{II} , \vec{M}_{III} , and \vec{M}_V are all equal to zero due to the absence of hard magnetic material in these regions.

6.2 Derivation of Magnetic Field Expressions

In this theoretical treatment, the two \vec{M} orientation extremes, in-plane and perpendicular hard ferromagnetic films are considered. Expressions for the magnetic fields in the system shown in Figure 6-4 are derived assuming two hard magnetic pattern geometries, an array of squares and an array of stripes. These two hard magnetic film geometries are shown in Figure 6-5.

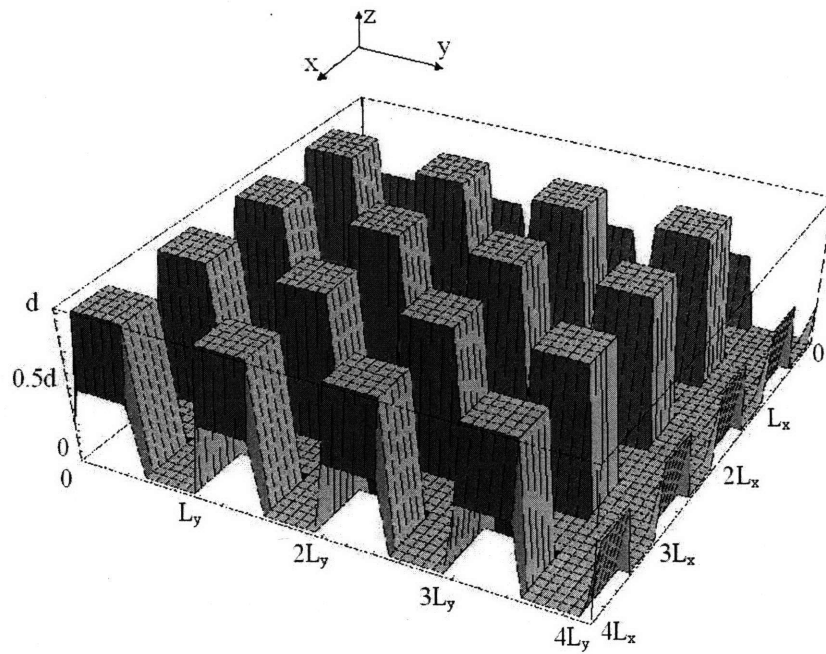
6.2.1 Hard Magnetic Film with Perpendicular Anisotropy

Assuming perpendicular anisotropy, the expressions for the magnetization vectors in the hard magnetic film (i.e., Region IV) are given by

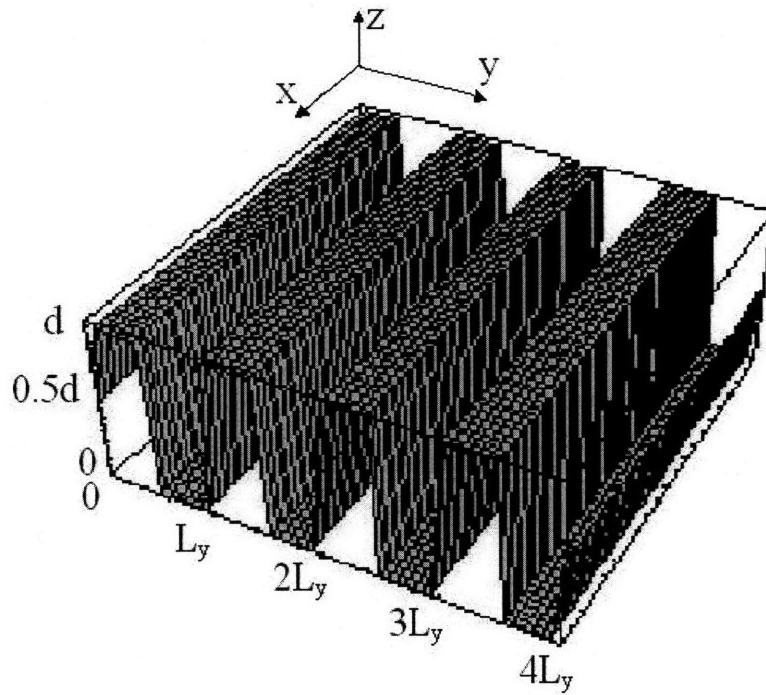
$$\vec{M}_{IV} = M_r \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left(\frac{4}{\pi^2 m n} \sin k_{x_m} x \sin k_{y_n} y + \frac{1}{\pi m} \sin k_{x_m} x + \frac{1}{\pi n} \sin k_{y_n} y + \frac{1}{4} \right) \hat{i}_z \quad (6.11)$$

for the array of squares geometry and

$$\vec{M}_{IV} = M_r \left(\frac{1}{2} + \frac{2}{\pi} \sum_{n, \text{odd}}^{\infty} \frac{1}{n} \sin k_{y_n} y \right) \hat{i}_z \quad (6.12)$$



(a) Hard magnetic film in an array of squares pattern.



(b) Hard magnetic film in an array of stripes pattern.

Figure 6-5: Graphical representations of the hard magnetic material patterns.

for the array of stripes geometry where $k_{x_m} = \frac{2\pi m}{L_x}$, $k_{y_n} = \frac{2\pi n}{L_y}$, L_x is the pattern period in the x direction, L_y is the pattern period in the y direction, and M_r is the remanent magnetization.

For hard magnetic films having these geometries and anisotropy, $\nabla \cdot \vec{M} = 0$. Thus in each region, Equation (6-10) simplifies to Laplace's equation

$$\nabla^2 \psi = 0. \quad (6.13)$$

Concerning the array of squares hard magnetic film geometry, expressions for the magnetic scalar potential in Regions I through V have been solved for and are given in Appendix D.

Expressions for the magnetic field, H , and the magnetic flux density, B , are derived using relations (6.3) and (6.5) respectively as well as the boundaries conditions that the tangential magnetic field is continuous

$$\hat{i}_n x (\vec{H}_1 - \vec{H}_2) = \vec{J}_s = 0 \quad (6.14)$$

and the normal magnetic flux density is continuous.

$$\hat{i}_n \cdot (\vec{B}_1 - \vec{B}_2) = 0 \quad (6.15)$$

The general expressions for the magnetic scalar potentials and magnetic fields for the array of stripes hard magnetic film geometry are obtained most easily by simplifying the expressions derived for the array of squares geometry in the limit $k_{x_m} = \frac{2\pi m}{L_x} \rightarrow 0$. Expressions for the magnetic scalar potentials, given this hard magnetic film geometry and magnetization orientation, are given in Appendix D.

6.2.2 Hard Magnetic Film with In-Plane Anisotropy

Assuming in-plane anisotropy, the expressions for the magnetization vector characteristics of a hard magnetic film patterned into an array of squares (Figure 6-5a) and an array of stripes (Figure 6-5b) are

$$\vec{M}_{IV} = M_r \sum_{m,\text{odd}}^{\infty} \sum_{n,\text{odd}}^{\infty} \left(\frac{4}{\pi^2 mn} \sin k_{x_m} x \sin k_{y_n} y + \frac{1}{\pi m} \sin k_{x_m} x + \frac{1}{\pi n} \sin k_{y_n} y + \frac{1}{4} \right) \hat{i}_x \quad (6.16)$$

and

$$\vec{M}_{IV} = M_r \left(\frac{1}{2} + \frac{2}{\pi} \sum_{m,\text{odd}}^{\infty} \frac{1}{m} \sin k_{x_m} x \right) \hat{i}_y \quad (6.17)$$

respectively. Since for the array of squares pattern, \vec{M}_{IV} varies in the direction in which it is directed, Laplace's equation in Region IV is not satisfied, but rather

$$\nabla \cdot \vec{M}_{IV} = \nabla^2 \psi = \frac{8M_r}{\pi L_x} \sum_{m,\text{odd}}^{\infty} \sum_{n,\text{odd}}^{\infty} \frac{1}{n} \cos k_{x_m} x \sin k_{y_n} y + \frac{2M_r}{L_x} \sum_{m,\text{odd}}^{\infty} \cos k_{x_m} x \quad (6.18)$$

Concerning this array of squares hard magnetic film geometry, expressions for the magnetic scalar potential in Regions I through V have been solved for, and are given in Appendix D.

For the case where the hard magnetic material is patterned into an array of stripes, Laplace's equation (6.13) is satisfied in each region. Assuming the infinite extent of the pattern and that the magnetization is aligned along the stripe due to shape anisotropy, the expressions for ψ , and \vec{H} evaluate to zero in all the regions.

6.3 Derivation of the Magnetic Retention Force Expression

An expression for the magnetic force acting between the patterned hard magnetic material on the target substrate and the soft magnetic film on the device block is derived using the Maxwell Stress Tensor. In this treatment, we will first consider the array of squares geometry. As is the case in solving for the magnetic field expressions, the force relation for the array of stripes is easily extractable from the array of squares analysis. Reference [90] provides a more in-depth description of Maxwell Stress Tensor

analysis.

For the case of the magnetic retentive force, we are interested in the force in the z direction. This is given by

$$f_z = \oint_S (T_{zx}n_x + T_{zy}n_y + T_{zz}n_z)dS \quad (6.19)$$

where the Stress Tensor components are given by

$$T_{zx} = \mu H_x H_z \quad (6.20)$$

$$T_{zy} = \mu H_y H_z \quad (6.21)$$

$$T_{zz} = \mu H_z H_z - \frac{\mu}{2} H_k H_k \quad (6.22)$$

where $k = x, y,$ and z .

With a general relation for the force, an appropriate surface needs to be chosen in order to evaluate this expression. The dashed line shown in Figure 6-6 outlines the surface over which the integration is performed.

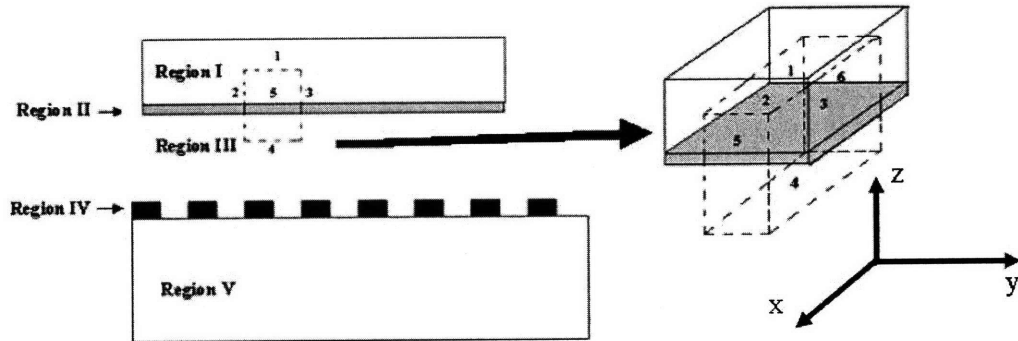


Figure 6-6: Schematic depicting the surface chosen to evaluate the force integral, where the six faces of this volume are labeled 1, 2, 3, 4, 5, and 6.

With the labelling in Figure 6-6, the magnetic force can be expressed as

$$f_z = \int_1 T_{zz}dS + \int_2 -T_{zy}dS + \int_3 T_{zy}dS + \int_4 -T_{zz}dS + \int_5 T_{zx}dS + \int_6 -T_{zx}dS \quad (6.23)$$

Considering the periodicity of the array of squares pattern in the x and y directions

$$\int_2 -T_{zy}dS + \int_3 T_{zy}dS = 0 \quad (6.24)$$

and

$$\int_5 T_{zx}dS - \int_6 T_{zx}dS = 0 \quad (6.25)$$

The Maxwell Stress Tensor force expression thus simplifies to

$$f_z = \int_1 T_{zz}dS + \int_4 -T_{zz}dS \quad (6.26)$$

Taking into account the exponential decrease of the magnetic field in the semiconductor (Region I), we approximate

$$\int_1 T_{zz}dS = 0 \quad (6.27)$$

The force expression is thus given by

$$f_z = \int_4 -T_{zz}dS = -\frac{\mu_0}{2} \int_4 [H_{IIIz}^2 - H_{IIIx}^2 - H_{IIIy}^2]dS \quad (6.28)$$

where H_{IIIx} , H_{IIIy} and H_{IIIz} are the magnetic fields along surface 4 in the gap region (Region III) in the x, y and z directions respectively.

Assuming a perpendicular magnetization orientation with this array of squares pattern, the expression for the magnetic force density can be expressed as

$$\begin{aligned} F_z = & -\frac{\mu_0 M_r^2}{\pi^2} \sum_{m, \text{odd}} \sum_{n, \text{odd}} \left[\frac{2}{\pi^2 m^2 n^2} [e^{-2k_{zm}g}] [(1 - e^{-k_{zm}d})^2] \left[\frac{(e^{2k_{zm}t} - 1)(\mu_s^2 - 1)}{e^{2k_{zm}t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \right. \\ & + \frac{1}{4m^2} [e^{-2k_{xm}g}] [(1 - e^{-k_{xm}d})^2] \left[\frac{(e^{2k_{xm}t} - 1)(\mu_s^2 - 1)}{e^{2k_{xm}t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \\ & \left. + \frac{1}{4n^2} [e^{-2k_{yn}g}] [(1 - e^{-k_{yn}d})^2] \left[\frac{(e^{2k_{yn}t} - 1)(\mu_s^2 - 1)}{e^{2k_{yn}t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \right] \quad (6.29) \end{aligned}$$

where $k_{z_{m,n}}^2 = k_{x_m}^2 + k_{y_n}^2$. Assuming an in-plane magnetization orientation with this array of squares pattern, the force density can be modelled by

$$F_z = -\frac{4\mu_0 M_r^2}{\pi^4} \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\frac{L_y^2}{n^2(m^2 L_y^2 + n^2 L_x^2)} [e^{-2k_{z_{m,n}} g}] [(1 - e^{-k_{z_{m,n}} d})^2] \left[\frac{(e^{2k_{z_{m,n}} t} - 1)(\mu_s^2 - 1)}{e^{2k_{z_{m,n}} t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \right. \\ \left. + \frac{2m^2 L_y^4}{n^2(m^4 L_y^4 + n^4 L_x^4 + 2m^2 L_y^2 n^2 L_x^2)} [e^{-2k_{x_m} g}] [(1 - e^{-k_{x_m} d})^2] \left[\frac{(e^{2k_{x_m} t} - 1)(\mu_s^2 - 1)}{e^{2k_{x_m} t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \right] \quad (6.30)$$

If we now apply Equation (6.23) to the array of stripes geometry, taking note of the assumed infinite extent in the x direction of the stripes pattern, the magnetic field in the x direction has evaluated to be zero for all regions. Thus for all surfaces, the stress component T_{zx} evaluates to zero.

Combining this with the results obtained for the array of squares case, the force expression simplifies to

$$f_z = \int_4 -T_{zz} dS = -\frac{\mu_0}{2} \int_4 [H_{IIIz}^2 - H_{IIIy}^2] dS \quad (6.31)$$

Given expressions for the magnetic field derived earlier, an expression for the magnetic retention force can be derived. As an example, the magnetic force density expression when the hard magnetic film is assumed to be an array of stripes with perpendicular anisotropy is given by

$$F_z = -\frac{\mu_0 M_r^2}{\pi^2} \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \frac{1}{n^2} [e^{-2k_{y_n} g}] [1 - e^{-k_{y_n} d}]^2 \left[\frac{(e^{2k_{y_n} t} - 1)(\mu_s^2 - 1)}{e^{2k_{y_n} t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right] \quad (6.32)$$

First order force density expressions for the square geometry with both in-plane and perpendicular magnetic anisotropy, are plotted alongside the stripe geometry with perpendicular magnetic anisotropy⁸ in Figure 6-9. These characteristics were

⁸For films with in-plane anisotropy, the stripe geometry will produce little force since the magnetization will align along the longest stripe dimension due to shape anisotropy.

generated assuming typical thicknesses and magnetic property values of the SmCo and Co/Pd hard magnetic films and soft magnetic materials such as nickel and permalloy.⁹

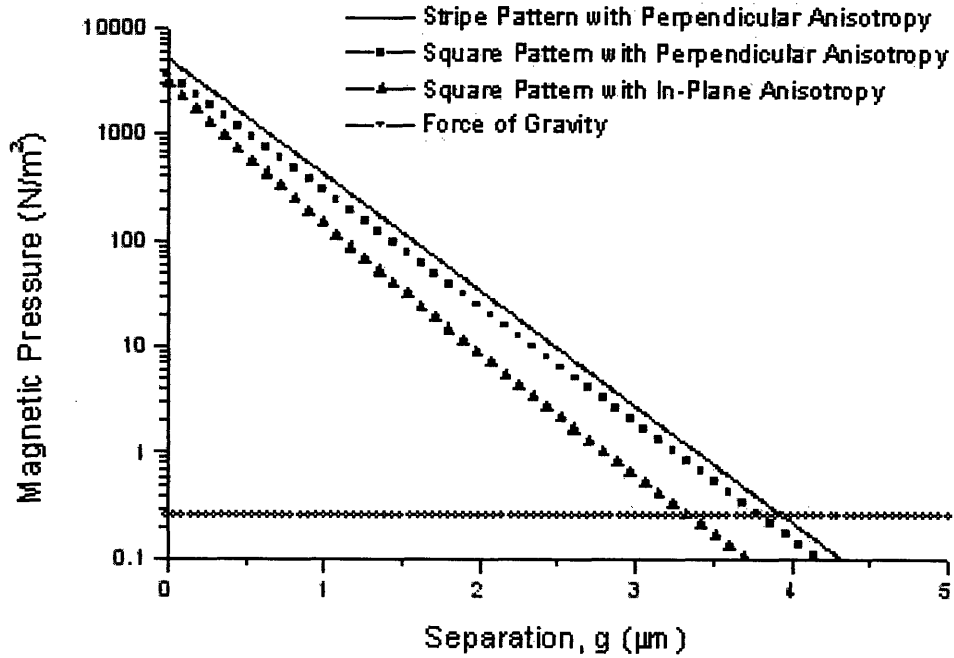


Figure 6-7: Magnetic retention forces for the various magnetization orientations and pattern geometries assuming $L_x = L_y = 5 \mu\text{m}$, $M_r = 1000 \text{ emu/cm}^3$, $\mu_s = 50$, $d = t = 0.25 \mu\text{m}$.

6.3.1 Magnetic Force Density Dependencies

The magnetic force density expressions can be analyzed as a product of four factors. These factors are given by

⁹The force density due to gravity is calculated assuming a cylindrical GaAs devices with thickness of $5 \mu\text{m}$, and radius $50 \mu\text{m}$.

$$f(M_r) = \frac{\mu_0 M_r^2}{\pi^2} \quad (6.33)$$

$$f(g, L) = e^{-\frac{4\pi g}{L}} \quad (6.34)$$

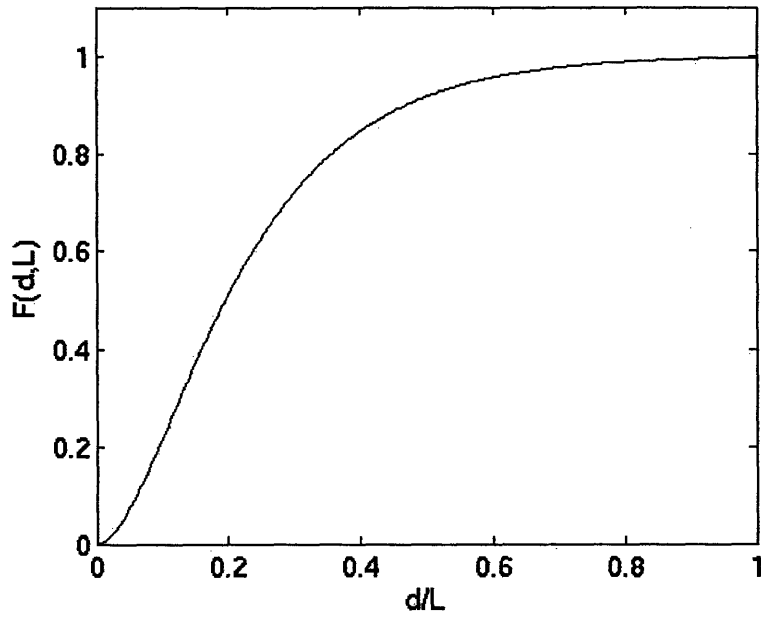
$$f(d, L) = (1 - e^{-\frac{2\pi d}{L}})^2 \quad (6.35)$$

$$f(\mu_s, t, L) = \frac{(e^{2kt} - 1)(\mu_s^2 - 1)}{e^{2kt}(\mu_s + 1)^2 - (\mu_s - 1)^2} \quad (6.36)$$

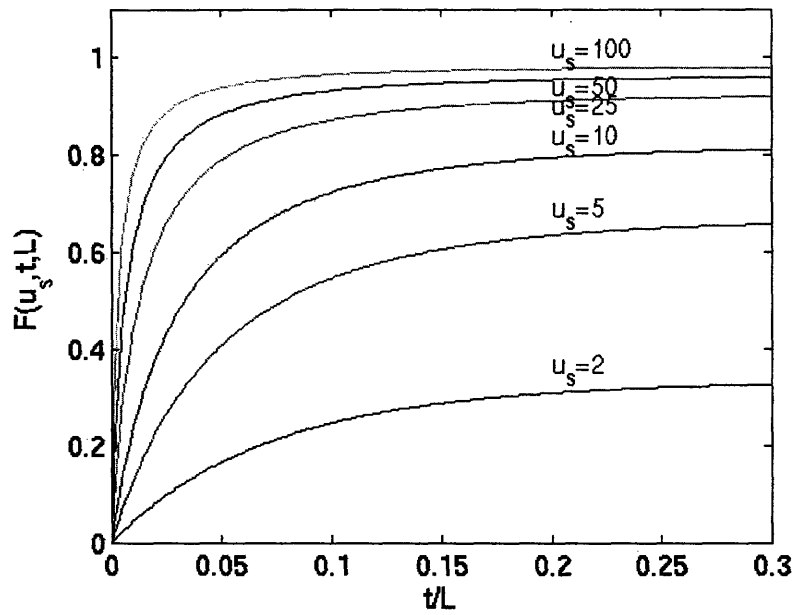
Three of these factors, $f(g, L)$, $f(d, L)$, and $f(\mu_s, t, L)$ have magnitudes less than one. The behaviors of the functions, $f(M_r)$ and $f(g, L)$, are straightforward with the former increasing quadratically with increasing remanent magnetization and the latter decreasing exponentially with increased gap separation, g . The function $f(d, L)$ increases with increasing thickness, d until it saturates at a value of one for larger values of d as is shown in Figure 6-8a. The function $f(\mu_s, t, L)$ is plotted in Figure 6-8b.

To make the technology viable for large-scale integration, we would like to keep the magnetic film thicknesses as thin as possible. However, from Figure 6-8, we see that if the magnetic films are too thin, the magnetic force density will be reduced significantly. If higher permeability magnetic films are used, reducing the soft magnetic film thickness has a less profound effect on the magnetic force density.

To obtain the highest retentive forces at approximately zero separation between the device block magnetic layer and the target substrate magnetic layer, it is advantageous to pattern the hard magnetic film into a very fine pattern. For instance, a pattern period of $2 \mu\text{m}$ offers approximately a factor of 4 larger magnetic force density than a pattern period of $5 \mu\text{m}$ and a factor of 16 larger magnetic force density than a pattern period of $10 \mu\text{m}$ when the separation narrows to near zero. A consequence of this fine pattern is that the magnetic force will decay at a faster rate than for more coarse patterns. This is shown in Figure 6-9.



(a) First order component of $f(d,L)$ plotted as a function of d/L .



(b) First order component of $f(\mu_s, t, L)$ plotted as a function of t/L for different values of the relative permeability

Figure 6-8: Dependence of the force expression on hard and soft magnetic film thickness.

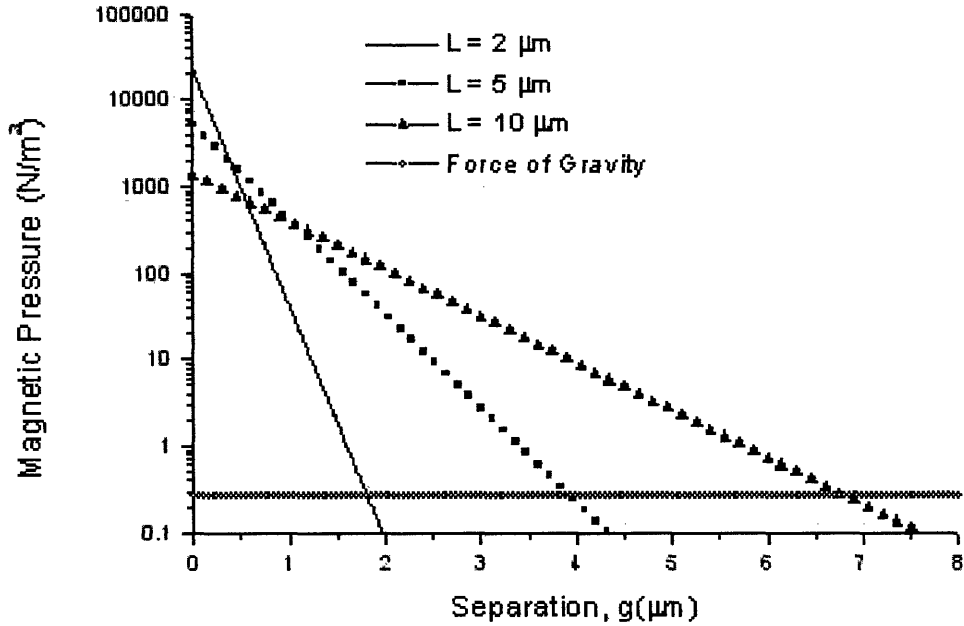


Figure 6-9: Magnetic retention force for the array of stripes pattern with perpendicular anisotropy as a function of pattern period.

6.3.2 Magnetic Force Verification

Dr. James Perkins developed a technique to measure the magnetic force between a permeable nickel film and a SmCo hard magnetic layer. Specifically, Dr. Perkins fabricated micro-cantilevers upon which he deposited a thin film of nickel. These micro-cantilevers were then brought in close proximity with the SmCo film, which was patterned into an array of squares. By measuring the deflection of the micro-cantilever as the two magnetic films were brought close together, a measurement of the magnetic force between the two films was attained. At a gap separation just less than $1 \mu\text{m}$, a force of approximately 300 to 400 N/m^2 was measured. This is on the order of what we expect from the theoretical model. More details on these measurements can be found in Reference [73].

Chapter 7

Concluding Remarks

With the key missing link in silicon optoelectronics, namely electrically pumped, continuous-wave edge-emitting lasers achieved with this thesis work, a significant step has been made towards the realization of a building block optoelectronic integration architecture. Having described the processes used to manufacture and integrate the micro-cleaved ridge platelet lasers and their performance on silicon, these results will now be put into perspective and possible future research directions will be outlined.

7.1 Alternative Approaches to Achieving III-V Lasers on Silicon

Prior to and simultaneous with the work described in this thesis, a number of groups have pursued the integration of III-V semiconductor lasers on silicon using epitaxial lift-off processes. Most notable among these are the efforts of Pollentier et al. and Seo et al. who achieved pulsed lasing of GaAs-AlGaAs GRIN-SCH SQW lasers on silicon and InP-InGaAsP MQW ridge lasers on silicon, respectively[37, 76].

Pollentier et al. indium bonded epitaxial 250 μm long GaAs-based thin film, graded-index, separate-confinement, single quantum well (SQW) lasers to silicon. The cleaved facets of the edge-emitting lasers were formed prior to integration by affixing the thin film laser to a flexible carrier substrate and bending. Pulsed (i.e.,

20 kHz repetition rate, 1 μ s wide pulses) laser operation was achieved; however, the device did not lase under continuous-wave conditions[37].

Seo et al. metal bonded epitaxial 200 μ m long InP-based thin film, MQW ridge (5 μ m wide) lasers to silicon substrates. As in the Pollentier et al. effort, the cleaved facets of the edge-emitting lasers were formed prior to integration by attaching the thin film laser to a flexible carrier substrate and bending. Biasing the devices with 0.5 μ s wide pulses at a 10% duty cycle, the devices lased at a threshold current of 25 mA and a peak output power of less than 1 mW (measured using an integrating sphere and a photodetector). The devices did not lase under continuous-wave biasing[76].

Since these aforementioned research efforts resulted in pulsed, not continuous-wave lasers on silicon, to put this thesis work in perspective, it is most useful to compare it with other work that has achieved electrically pumped, continuous-wave lasing on silicon. For example, Van Campenhout et al. integrated tiny (7.5 μ m diameter) thin film (1 μ m) InP-based microdisk lasers emitting at a wavelength of 1600 nm with silicon on insulator (SOI) waveguides on silicon substrates. These lasers utilize evanescent coupling from the laser to the SOI waveguide and have achieved continuous-wave lasing at ultra-low threshold currents of 0.5 mA and maximum output powers of 10 μ W at room temperature. This approach to integrating lasers on silicon has a great number of advantages, namely the devices have a very small footprint and they have extremely low threshold currents. Drawbacks of the device are that it sits on top of a poor thermal conductor (i.e., SOI waveguide) and it only has been shown to emit low levels of light[47].

Another interesting approach is the recent combined effort of Intel and UCSB which has received the most attention in the press[63]. This Intel/UCSB effort has, like this thesis work, resulted in electrically pumped CW 1.55 μ m wavelength cleaved facet lasers on silicon. Whereas this thesis work has resulted in a stand-alone laser integrated on silicon, the Intel/UCSB effort has achieved an integration with an SOI waveguide. Since this Intel/UCSB laser has received the most acclaim of all the competing lasers on silicon, it is interesting to compare the results of this thesis work with it. Several performance characteristics of the two lasers are listed in Table 7-1.

Parameter	MIT	Intel/UCSB
Wavelength (μm)	1.55	1.55
Length (μm)	300	860
Max Operating T ($^{\circ}\text{C}$)	55	40
J_{th} (kA/cm^2)	0.96	1.89
T_0 (K)	38.1	39
R_{series} (Ohms)	8.8	7.5

Table 7-1 Comparison between MIT edge-emitting laser on silicon and that of the Intel/UCSB discrete cleaved facet laser [49].

Comparing the properties of the two lasers, most striking is the distinction in temperature performance. The MIT device lased at temperatures as high as 55°C versus 40°C for the Intel/UCSB device.¹ The Intel/UCSB laser threshold current density, J_{th} , is also almost twice that of the MIT laser. The discrepancy in maximum operating temperatures and threshold current density between the MIT and Intel/UCSB lasers is glaring given that the Intel/UCSB laser utilized proton implanted current confinement structures to reduce current leakage, whereas the MIT approach did not[49]. The Intel/UCSB devices requires such a large threshold current because of the small overlap (3 %) the optical mode in the device has with the III-V quantum wells. Moreover, the thermal performance of the Intel/UCSB device is limited because the laser sits on an SOI layer which as we saw in Chapter 3 is a very poor thermal conductor. The characteristic temperatures, T_0 , measured under CW conditions for the two lasers are similar with the MIT device having a value of 38.1 K compared to 39 K for the Intel/UCSB device. The areas of the devices need to be taken into account when interpreting the diode series resistances. The MIT ridge is approximately 300 μm long and 7.6 μm wide whereas the Intel/UCSB device has a 2.5 μm wide ridge and a 860 μm long cavity. Normalizing for area, the MIT laser has resistance per unit area of $0.0038 \Omega/\mu\text{m}^2$ versus the Intel/UCSB laser which has a resistance per unit area of $0.0035 \Omega/\mu\text{m}^2$.

¹In fact, the MIT lasers integrated on silicon had better thermal performance than the MIT conventionally cleaved lasers tested on native indium phosphide substrates.

Comparing the peak output power is not appropriate since the Intel/UCSB max output power of 7.2 mW reported at 15 °C is the power emanating from an SOI waveguide which the InP laser is evanescently coupled to. The MIT device, which is not coupled to a waveguide, emits a peak output power of 23.96 mW at 15 °C. If the MIT laser was integrated with a waveguide, the integration could have as much as a 5.2 dB coupling loss for the MIT laser to have equivalent to or better performance with respect to peak output power than the Intel/UCSB laser. From theoretical calculations, the estimated end-fire coupling loss between an MIT laser and a SiO_xN_y dielectric waveguide is less than 5 dB for air gaps less than 2 μm between the two device facets. These results have been verified experimentally. Theoretical analysis has further shown that if higher refractive index gap fill materials are used in the regions between the laser facet and the dielectric waveguide facet, coupling losses as low as 1 or 2 dB are achievable. Furthermore, if the laser mode size is tailored for coupling to the dielectric waveguide, coupling losses of less than 1 dB should be reachable[15]. Gap spacings of this magnitude or better are feasible given the measured precision of the micro-cleaving process developed in this thesis work.

There are several comparative advantages of the MIT edge-emitting laser over the competing Intel/UCSB laser. First among these is with regards to heat sinking. The MIT laser is attached to the silicon substrate using metal-to-metal bonding; whereas, the Intel/UCSB laser is bonded to a silicon dioxide dielectric layer on a silicon substrate.² Since the MIT laser's bond to the silicon substrate is through a good thermal conductor, it should offer superior high temperature performance. Looking at the maximum operating temperature of the two devices, this advantage of the MIT laser is confirmed.

Another advantage of the MIT laser is in its process flexibility. Only a quick six minute, 200 °C bonding step is needed to attach the laser to a silicon chip; whereas, the Intel/UCSB laser requires a 12 hour long 300 °C oxygen assisted plasma bonding step[49].

²Due to the benefits in evanescent coupling of having the laser effective refractive index similar in value to the coupling waveguide refractive index, an SOI waveguide was likely chosen over other possible dielectric waveguides for the Intel/UCSB integration scheme.

The MIT building block integration approach could potentially offer higher yields than the Intel/UCSB approach. The reasoning behind this is that before bonding to the silicon substrate, the MIT laser is fully processed. Therefore, it may be possible to yield screen (i.e., pulse characterize) these lasers prior to integration, and assemble only the best performing devices. The Intel/UCSB laser, on the other hand, requires a significant amount of processing after bonding to the silicon wafer. For instance, all the backside processing, including InP substrate removal, device etch patterning, and n-type and p-type ohmic contact formation, still needs to be carried out. Thus, in the case of the Intel/UCSB laser, if problems occur with the InP processing, the entire silicon device will be wasted.

The MIT integration approach offers a smaller overall footprint than that of the Intel/UCSB approach. Therefore, the MIT laser allows for a very cost effective use of substrate materials like InP. To achieve integration on silicon, the Intel/UCSB effort utilizes a racetrack laser structure[12]. As its name implies, the device looks strikingly like a racetrack. It is an extremely large device with racetrack radius of 200 μm and total laser cavity length of 2656 μm . The dimensions need to be so large because of the weak optical confinement of the InP-based laser and Si-based waveguide evanescently coupled pair. Additionally, the cavity needs to be long to compensate for the fact that the optical mode only partially overlaps the quantum well gain region [19]. Due to its use of end-fire coupling, no long coupling regions, like those seen in evanescent approaches, are required for the MIT laser on silicon. Thus, the MIT integrable devices can be kept rather compact. Figure 7-1 shows the comparative footprints of the two integration structures.

The MIT integration approach is more flexible with regards to the variety of devices that can be integrated than is the Intel/UCSB approach. Since fully processed MIT devices are assembled like building blocks (by metal-to-metal bonding), it is not necessary to tailor the silicon based waveguide composition every time a new type of device is integrated. One could imagine, integrating lasers operating at a number of wavelengths, as well as photodetectors, and amplifiers with the MIT approach. Coupling to silicon-based waveguides could be tailored by making use of tapers and other

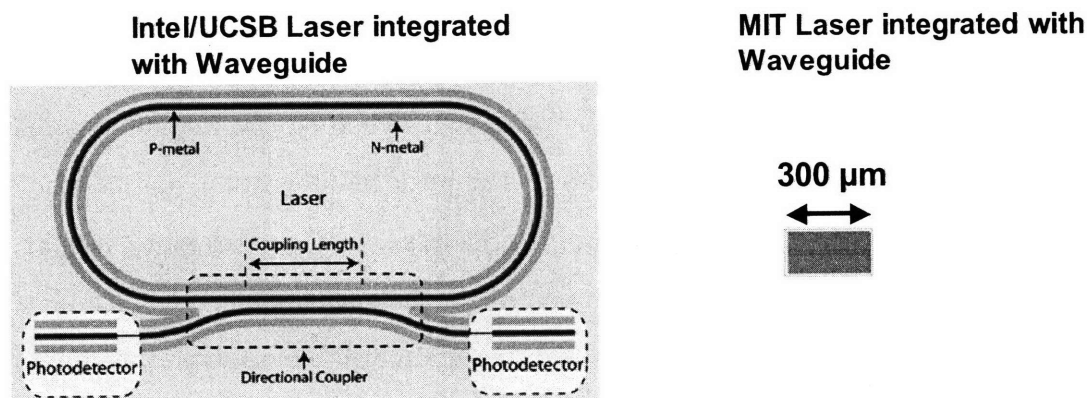


Figure 7-1: Schematic detailing the comparative size of the Intel/UCSB Racetrack laser and the MIT laser integrated with a dielectric waveguide[12].

coupling regions on the specific device being integrated without making adjustments to the silicon-based waveguides.

The MIT approach allows individual building blocks (i.e., individual lasers in this work) to be assembled. It is uncertain if it is practical for individual lasers to be integrated with the UCSB/Intel technique due to the requirements of the long oxygen assisted plasma bonding step.

The MIT approach allows the cavity length of the edge emitting lasers to be precisely controlled. The micro-cleaving process used to form the facets already has been used to create batches of 300 μm long edge-emitting lasers with a standard deviation in lengths of less than 1.25 μm. Strategies have been suggested in this thesis to improve this precision even more. For instance, by incorporating thin non-crystalline materials, like metals, on top of the semiconductor in the region between the micro-cleave bar pattern notches, cleaving can be prevented in areas where it is not desired. It is uncertain how well the Intel/UCSB cavity length can be controlled but it's assumed that a typical length variation of approximately +/- 10 μm is likely seen.

There are a number of qualities that both lasers share. First, both laser fabrication processes can be tailored to produce the highest quality laser diodes incorporating current confinement structures, for instance. Second, both lasers are extremely thin, approximately 5 μm thick in the case of the MIT laser, and thus common dielectric

layers routinely deposited in industry can be used to planarize the integrated chip and allow for post-integration processing of the devices.

7.2 Future Directions

This achievement of electrically pumped, continuous-wave lasing on silicon opens the doors for significant future work. This work could be divided into four main areas, device improvements, micro-cleaving improvements, integration with other optoelectronic components, and new integrable devices.

Device Improvements

The laser realized in this thesis was a simple ridge laser device and a rudimentary process technology was used to create the devices. Therefore, a large number of device improvements could likely be made. Along these lines, state of the art designs that incorporate current confinement structures, could be executed. These design improvements would likely result in lower threshold operation and extend continuous-wave laser operation to even higher temperatures than 55 °C.

Second, moving the process to a higher quality fabrication facility would likely result in significant performance improvement. As an example, the n-type and p-type laser ohmic contacts in this development work had contact resistivities on the order of $10^{-5} \Omega \text{ cm}^2$ and $10^{-4} \Omega \text{ cm}^2$, respectively. This is more than an order of magnitude worse than is readily achieved in industry. Another possible process improvement is the conversion of the ridge patterning process from a combination of contact lithography and wet etching³ to high resolution photolithography and anisotropic semiconductor dry etching. Doing this would enable narrower ridges and significantly lower threshold lasers. Incorporating high reflectivity facet coatings would also result in improved laser performance. Right now the facet reflectivity is less than 30%, so there is a significant amount of improvement that could be made here. Processing larger samples than the 1 cm^2 area samples used in this development work would

³Wet etching typically offers much worse dimensional control than dry etching.

lend itself to more uniform results and larger batches of devices to conduct integration experiments.

Micro-cleaving Improvements

Improvements to the micro-cleaved process could be made that allow for the realization of narrower micro-cleave bar notches. As was pointed out in Chapter 5, micro-cleaving bars with notches in the $5.5\ \mu\text{m}$ to $7.5\ \mu\text{m}$ width range result in micro-cleaved cavity length precision of nearly $1.25\ \mu\text{m}$. It remains to be seen whether narrowing these notches further would have beneficial consequences, but with better fabrication equipment at our disposal, a study of the effect of narrowing the notches could be carried out. Furthermore, a thorough analysis of the micro-cleaving could be carried out. This analysis would ideally include studies of the frequency of the ultrasonic agitation, the effect the liquid solution plays on the micro-cleaving process, and the intensity of the agitation process. Along these lines, it would be interesting to develop a theoretical model for the micro-cleaving process and use this model as a tool for improving the process. Possibly, one could model the micro-cleaving bar as a resonant system and tailor the length of the bar, and the location of the notches with the applied drive frequency and amplitude.

Moreover, studies on the geometries of the bar and notch geometry should be carried out to see not only how narrow the notches can be made, but also how deep they can penetrate in toward the ridge structure. It would also be very interesting to further investigate the use of patterned thin films of non-crystalline material, such as metals, and study if these materials can help precisely locate cleaving locations without the need for deep semiconductor etching in narrow notch regions.

The micro-cleaving process has been shown to be very capable of producing $300\ \mu\text{m}$ long devices. It would really be interesting to see how short devices could be made using this micro-cleaving technique. Allowing for an even more reduced footprint and more efficient use of material, this could have very significant implications in terms of integration. It would also be instructive to investigate how long a device can be made using this micro-cleaving process before effects like warping make it impractical.

Integration with other Optoelectronic Components

With regards to integration, work related to the design and optimization of the coupling between a ridge laser platelet on silicon and a dielectric waveguide is a logical next research effort. Integration work would be significantly aided by improvements in the ridge laser fabrication process. For instance, the ability to pattern very narrow semiconductor ridges, which enable single lateral mode operation, would be useful. Also, the investigation of gap fill materials between a ridge laser platelet facet and a dielectric waveguide facet should be undertaken.

In terms of assembly, a great deal of work could be done on the demonstration of magnetically assisted statistical assembly (MASA), the integration technique theoretically described in Chapter 6. Some basic experiments filling recesses and measuring the magnetic force have been done, but a thorough set of assembly experiments have yet to be carried out. Graduate student Diana Cheng is researching MASA now and will be carrying out the desired assembly experiments.

New Integrable Devices

Finally, the process technology developed in this thesis could be extended to other optoelectronic building blocks. For example, semiconductor optical amplifiers (SOA) would be a logical choice for the extension of this technology. The epitaxial layer structure for an integrable SOA should be much like that of the integrable laser and thus the process to make these SOAs should be very similar as well. The only foreseeable complications for the integrable SOA are with regards to the device length and facet requirements. The SOA would likely need to be significantly longer, at least two or three times the length of the ridge lasers described in this thesis, to provide the gain necessary to make its integration worthwhile. Recalling the device warpage which was seen with the ridge lasers, it is reasonable to expect worse warpage with the much longer SOAs. This warpage could be combatted by making the devices wider and slightly thicker to reduce the discrepancy in dimensions. It is understood that to make it most attractive for integration, the device should be kept relatively

thin, so the main dimension that could be adjusted to lessen the warpage is the width. Regarding the facet requirements of the SOA, it is acknowledged that the facet reflectivity must be kept sufficiently low so that light can be both coupled into and out of the device. However, the facet must also be smooth so as to minimize loss. Therefore, micro-cleaving would still be a good approach to define the facets, but instead of forming the facets orthogonal with the ridge, it would be optimal to form them at angle of approximately 7° off axis from the ridge. This requirement would therefore affect the alignment of the facet to the wafer flat and would likely mandate the use of a dry etch process to etch the semiconductor ridge.

Appendix A

Conventionally Cleaved Ridge Laser Process Flow

InP-based Laser (Conventionally Cleaved) Process Flow (Page 1/3)

Sample Number: _____
Date: _____

Done?	Step	Process Description	Notes:
	100	Start with InP wafer upon which InP-based laser structure has been grown	
	200	Cleave substrate, Solvent Clean, N ₂ Blow Dry	
		-- Starting with a (100) InP wafer, cleave rectangular bars so that the long side of the rectangular is perpendicular to the wafer flat	
	300	Stripe Photolithography	Scrape edge bead at or cleave at corners before exposure to enable high res litho
		-- AZ5214E (Image Reversal) Static dispense, 2k rpm, 35 sec total	
		-- Oven Bake 90 C, 30 minutes	
		-- Exposure 45sec (incl. 4 sec rampup, 2.8-3 mW/cm ²) - High Res Aligner w with long wavelength filter	
		-- Hotplate Bake 105 C, 52 sec	
		-- Flood Exposure 2.7 min Broadband Aligner	
	400	Native Oxide Strip	
		-- (7:1 Buffered Oxide Etch) No agitation 8-10 sec, DI H ₂ O rinse, N ₂ Blow Dry	
	500	P-type Ohmic Contact Metal Deposition	
		-- Base Pressure ~ 10 ⁻⁶ torr, Dep Pressure < 6x10 ⁻⁶ torr	
		-- Ebeam Evap. Ti(300A)/Pt(200A)/Au(2500A)	
	600	Metal Liftoff Process	
		-- Acetone, slight agitation	

Figure A-1:

InP-based Laser (Conventionally Cleaved) Process Flow (Page 2/3)

Sample Number: _____
 Date: _____

Done?	Step	Process Description	Notes:
	700	Ohmic Contact Anneal -- RTA, 15 min > 3 scfh forming gas (95% N ₂ , 5% H ₂) flow; 30 sec 385 C, forming gas flow	
	800	Verify Ohmic Contact Electrically -- HP Semiconductor Parameter Analyzer/Probe Station	
	900	Solvent Clean, N ₂ Blow Dry, 130 C Oven Bake	
	1000	Semiconductor Ridge Etch A.) 200 nm InGaAs etch Stir 6.5 min, Room Temperature, Etch Time < 20 sec -- Etchant 1:1:20 H ₂ SO ₄ : H ₂ O ₂ : H ₂ O --> Etch rate > 450 nm/min B.) Microscope Inspection C.) 1.5 um InP Etch HCl : During Etch No agitation, Etch Time < 15 sec -- Etchant Conc. HCl (37%) --> Etch rate > 5.8 um/min, Etch InP substrate ~ 6.8 um/min D.) Microscope Inspection	If InGaAs etch results look spotty, etch a few sec more, agitate slightly. If InP etch results look spotty, etch a few sec more, agitate slightly.
	1100	Profilometry (accurate measure of ridge height) -- CMSE Profilometer	
	1200	Solvent Clean, N ₂ Blow Dry, 130 C Oven Bake	
	1300	Planarization Layer 1 (BCB) Deposit -- AP3000 Static Dispense, 300 rpm (5 sec), 2-3k rpm (20 sec) -- Hotplate Bake 100 C, 5 min -- BCB Static Dispense, 500-750 rpm (5 sec), 3k rpm (25 sec) ~ 1.3 um thickness -- Hotplate Bake 100 C, 1 min	Make certain no BCB gets on the backside of the sample. Pour BCB only in center of sample, not at edges.
	1400	Planarization Layer 1 (BCB) Cure -- EML Furnace - Put Samples in at T < 100 C, Close end of furnace -- Flow N ₂ (>20 scfh) for 30 min -- Ramp Temp up to 210 C, Set N ₂ flow down to ~ 5-15 scfh -- 40 min at 210 C -- Ramp down temp	Rest sample on the backside of a Si wafer. to prevent sticking.
	1500	Planarization Layer 2 (BCB) Deposit -- BCB Static Dispense, 500-750 rpm (5 sec), 2k rpm (25 sec) -- Hotplate Bake 100 C, 1 min	Make certain no BCB gets on the backside of the sample.
	1600	Planarization Layer 2 (BCB) Cure -- EML Furnace - Put Samples in at T < 100 C, Close end of furnace -- Flow N ₂ (>20 scfh) for 30 min -- Ramp Temp up to 250 C, Set N ₂ flow down to ~ 5-15 scfh -- 60 min at 250 C -- Ramp down temp	Rest sample on the backside of a Si wafer. to prevent sticking.
	1700	Planarization Layer (BCB) Etch -- EML Plasmatherm Chamber Clean (30 sccm O ₂ , 45 mtorr, 250W, 35 min) -- no samples -- EML Plasmatherm Chamber Season (15 sccm SF ₆ , 90 sccm O ₂ , 150W, 15 min) -- EML Plasmatherm BCB Etch (15 sccm SF ₆ , 90 sccm O ₂ , 150W) - Short etches and inspection. -- CMSE Profilometer/Electrical Probe Station to determine etch endpoint	Include dummy Si with BCB samples around edge of EEL sample to minimize edge etch effects.
	1800	Electrically Verify BCB Removed from Metal -- HP Semiconductor Parameter Analyzer/Probe Station	
	1900	Solvent Clean, N ₂ Blow Dry, 100 C Hot Plate Bake	

Figure A-2:

InP-based Laser (Conventionally Cleaved) Process Flow (Page 3/3)

Sample Number: _____

Date: _____

Done?	Step	Process Description	Notes:
	2000	Top Large Area Contact Photolithography	
		-- NR1-3000P (Negative Resist) Static dispense, 2.5k rpm, 37 sec total	
		-- Hotplate Bake 150 C, 135 sec	
		-- Exposure 45 sec high res aligner	
		-- Hotplate Bake 100 C, 180 sec	
		-- Develop 40 sec (RD6)	
	2100	Top Large Area Contact Metal Deposition	
		-- EML Ebeam Evaporator -- Cr(250A)/Au(3250A)	
	2200	Metal Liffoff Process	
		-- Acetone, slight agitation	
	2300	BCB Etch	
		-- EML Plasmatherm Chamber Clean (30 sccm O ₂ , 45 mtorr, 250W, 35 min)	
		-- EML Plasmatherm Chamber Season (15 sccm SF ₆ , 90 sccm O ₂ , 150W, 15 min)	
		-- EML Plasmatherm BCB Etch (15 sccm SF ₆ , 90 sccm O ₂ , 150W) - Short etches and inspection. -- Etch until no BCB outside of metal contact area	
	2400	Protective Layers Deposited on Sample Frontside	
		-- AZ4620 Static Dispense, > 2 k rpm, 80 sec total	
		-- Oven Bake 90 C, 70 minutes	
	2500	Mount Laser piece on a silicon carrier substrate	
		-- Cleave a Silicon piece that will act as the carrier substrate	
		-- a.) Melt wax on silicon piece (hotplate T ~ 120 C). b.) Mount laser face down in melted wax.	
	2600	Scrape PR/Wax from the edge and backside of the laser substrate	
	2700	InP Substrate Thinning	
		-- Concentrated HCl (37%) ~ 8-10 um/min --> Thin substrate to around 150 um or so; Thus, etch 20-25 min	
	2800	Backside N-type Ohmic Contact Metallization	
		-- Base Pressure ~ 10 ⁻⁶ torr, Dep Pressure < 6x10 ⁻⁶ torr	
		-- Ebeam Evap. Ni(50A)/Au(100A)/Ge(600A)/Au(900A)/Ni(300A)/Au(1750A)	
	2900	Metal Liffoff Process	
		-- Acetone room temperature (or Microstrip 2001, 85 C) slight agitation	
	3000	Detach Laser from Carrier Silicon wafer	
		-- Trichloroethylene solution removes apixxon wax	
		-- Acetone, Methanol, Isopropanol rinse, N ₂ blowdry	

Figure A-3:

Appendix B

Micro-cleaved Ridge Laser Process Flow

InP-based Laser Microcleaving Process Flow (Page 1/4)

Sample Number: _____

Date: _____

Done?	Step	Process Description	Notes:
	100	Start with InP wafer upon which InP-based laser structure has been grown	
	200	Cleave substrate, Solvent Clean, N ₂ Blow Dry	
		-- Starting with a (100) InP wafer, cleave rectangular bars so that the long side of the rectangular is perpendicular to the wafer flat	
	300	Stripe Photolithography	Scrape edge bead at or cleave at corners before exposure to enable high res litho
		-- AZ5214E (Image Reversal) Static dispense, 2k rpm, 35 sec total	
		-- Oven Bake 90 C, 30 minutes	
		-- Exposure 45sec (incl. 4 sec rampup, 2.8-3 mW/cm ²) - High Res Aligner with long wavelength filter	
		-- Hotplate Bake 105 C, 52 sec	
		-- Flood Exposure 2.7 min Broadband Aligner	
		-- Develop 60 sec (AZ422)	
	400	Native Oxide Strip	
		-- (7:1 Buffered Oxide Etch) No agitation 8-10 sec, DI H ₂ O rinse, N ₂ Blow Dry	
	500	P-type Ohmic Contact Metal Deposition	
		-- Base Pressure ~ 10 ⁻⁶ torr, Dep Pressure < 6x10 ⁻⁶ torr	
		-- Ebeam Evap. Ti(300A)/Pt(200A)/Au(2500A)	
	600	Metal Liftoff Process	
		-- Acetone, slight agitation	
	700	Ohmic Contact Anneal	
		-- RTA, 15 min > 3 scfh forming gas (95% N ₂ , 5% H ₂) flow; 30 sec 385 C, forming gas flow	
	800	Verify Ohmic Contact Electrically	
		-- HP Semiconductor Parameter Analyzer/Probe Station	
	900	Solvent Clean, N ₂ Blow Dry, 130 C Oven Bake	
	1000	Stripe Positive Photolithography (Mask Set 3, Mask b)	
		-- HMDS Static Dispense, > 3k rpm, 45 sec total	
		-- Oven Bake 130 C, 10 minutes	
		-- OCG-825 20CS (Standard Positive Resist) Static dispense, 3k rpm, 40 sec total	
		-- Oven Bake 90 C, 30 min	
		-- Exposure 0.55 min (incl. 4sec rampup, 2.8-3 mW/cm ²) High Res Aligner with long wavelength filter	
		-- Develop 80 sec (934 1:1)	
		-- Post-exposure oven bake (130 C) 3.5 min	
	1100	Semiconductor Ridge Etch	If InGaAs etch results look spotty, etch a few sec more, agitate slightly. If InP etch results look spotty, etch a few sec more, agitate slightly.
		A.) 200 nm InGaAs etch Stir 6.5 min, Room Temperature, Etch Time < 20 sec	
		-- Etchant 1:1:20 H ₂ SO ₄ : H ₂ O ₂ : H ₂ O --> Etch rate > 450 nm/min	
		B.) Microscope Inspection	
		C.) 1.5 um InP Etch HCl : During Etch No agitation, Etch Time < 15 sec	
		-- Etchant Conc. HCl (37%) --> Etch rate > 5.8 um/min, Etch InP substrate ~ 6.8 um/min	
		D.) Microscope Inspection	
	1200	Photoresist Strip	
		-- Microstrip 2001, 85 C, 15 min	
	1300	Profilometry (accurate measure of ridge height)	
		-- CMSE Profilometer	
	1400	Solvent Clean, N ₂ Blow Dry, 130 C Oven Bake	
	1500	Planarization Layer 1 (BCB) Deposit	Make certain no BCB gets on the backside of the sample. Pour BCB only in center of sample, not at edges.
		-- AP3000 Static Dispense, 300 rpm (5 sec), 2-3k rpm (20 sec)	
		-- Hotplate Bake 100 C, 5 min	
		-- BCB Static Dispense, 500-750 rpm (5 sec), 3k rpm (25 sec) ~ 1.3 um thickness	
		-- Hotplate Bake 100 C, 1 min	

Figure B-1:

InP-based Laser Microcleaving Process Flow (Page 2/4)

Sample Number: _____

Date: _____

Done?	Step	Process Description	Notes:
	1600	Planarization Layer 1 (BCB) Cure	Rest sample on the backside of a Si wafer. to prevent sticking.
		-- EML Furnace - Put Samples in at T < 100 C, Close end of furnace	
		-- Flow N ₂ (>20 scfh) for 30 min	
		-- Ramp Temp up to 210 C, Set N ₂ flow down to ~ 5-15 scfh	
		-- 40 min at 210 C	
		-- Ramp down n temp	
	1700	Planarization Layer 2 (BCB) Deposit	Make certain no BCB gets on the backside of the sample.
		-- BCB Static Dispense, 500-750 rpm (5 sec), 2k rpm (25 sec)	
		-- Hotplate Bake 100 C, 1 min	
	1800	Planarization Layer 2 (BCB) Cure	Rest sample on the backside of a Si wafer. to prevent sticking.
		-- EML Furnace - Put Samples in at T < 100 C, Close end of furnace	
		-- Flow N ₂ (>20 scfh) for 30 min	
		-- Ramp Temp up to 250 C, Set N ₂ flow down to ~ 5-15 scfh	
		-- 60 min at 250 C	
		-- Ramp down n temp	
	1900	Planarization Layer (BCB) Etch	Include dummy Si with BCB samples around edge of EEL sample to minimize edge etch effects.
		-- EML Plasmatherm Chamber Clean (30 sccm O ₂ , 45 mtorr, 250W, 35 min) -- no samples	
		-- EML Plasmatherm Chamber Season (15 sccm SF ₆ , 90 sccm O ₂ , 150W, 15 min)	
		-- EML Plasmatherm BCB Etch (15 sccm SF ₆ , 90 sccm O ₂ , 150W) - Short etches and inspection.	
		-- CMSE Profilometer/Electrical Probe Station to determine etch endpoint	
	2000	Electrically Verify BCB Removed from Metal	
		-- HP Semiconductor Parameter Analyzer/Probe Station	
	2100	Solvent Clean, N ₂ Blow Dry, 100 C Hot Plate Bake	
	2200	Top Large Area Contact Photolithography	
		-- NR1-3000P (Negative Resist) Static dispense, 2.5k rpm, 37 sec total	
		-- Hotplate Bake 150 C, 135 sec	
		-- Exposure 45 sec high res aligner	
		-- Hotplate Bake 100 C, 180 sec	
		-- Develop 40 sec (RD6)	
	2300	Top Large Area Contact Metal Deposition	
		-- EML Ebeam Evaporator	
		-- Cr(250A)/Au(3250A)	
	2400	Metal Liftoff Process	
		-- Acetone, slight agitation	
	2500	BCB Etch	
		-- EML Plasmatherm Chamber Clean (30 sccm O ₂ , 45 mtorr, 250W, 35 min)	
		-- EML Plasmatherm Chamber Season (15 sccm SF ₆ , 90 sccm O ₂ , 150W, 15 min)	
		-- EML Plasmatherm BCB Etch (15 sccm SF ₆ , 90 sccm O ₂ , 150W) - Short etches and inspection.	
		-- Etch until no BCB outside of metal contact area	
	2600	Solvent Clean, N ₂ Blow Dry, 100 C Hot Plate Bake	
	2700	SiO ₂ Hardmask Deposited x 3 --> resulting in total SiO ₂ thickness > 500 nm	
		-- 30 min SiO ₂ dep dummy run to ensure target is ready to dep. SiO ₂ and chuck is encapsulated	
		-- SiO ₂ Sputter Deposited.	
		P _{base} < 2x10 ⁻⁸ torr, 60 sccm Ar, 300 W RF Power, 85 min (~ 2 nm/min)	
	2800	Filmetrics SiO ₂ thickness (thick of SiO ₂ on Si dummy)	
	2900	Solvent Clean, N ₂ Blow Dry, 100 C Hot Plate Bake	

Figure B-2:

InP-based Laser Microcleaving Process Flow (Page 3/4)

Sample Number: _____

Date: _____

Done?	Step	Process Description	Notes:
	3000	Microcleave Photolithography	
		-- HMDS Static Dispense, > 3k rpm, 45 sec total	
		-- Oven Bake 130 C, 10 minutes	
		-- OCG-825 Static dispense, 3k rpm, 35 sec total	
		-- Oven Bake 90 C, 30 minutes	
		-- Exposure 10sec (incl. 4 sec rampup, 2.8-3 mW/cm ²) Broadband OR 0.55 min High Res Aligner	
		-- Develop 55 sec (934 1:1)	
	3100	SiO ₂ Hardmask Etch x 3	
		-- (7:1 Buffered Oxide Etch), No agitation, > 6 min	
	3200	Photoresist Strip	
		-- Dimethyl Sulfoxide, 85 C, 15 min, 350 rpm magnetic stirrer agitation	
	3300	Profilometry (accurate measure of step height before etching)	
		-- CMSE Profilometer	
	3400	InP Microcleave Etch	Stop just short of the bottom etch stop layer
		-- Lincoln Lab ICP Etch (0.5 sccm Cl ₂ , 0.5 sccm SiCl ₄ , 10 sccm Ar)	
		-- Take out after short etches and P10 step heights	
		-- ~ 265 nm/min through the heterostructure device	
	3500	Profilometry to determine etch depth	
		-- CMSE P10	
	3600	InP Wet etch dip to bottom etch stop layer	
		-- HCl (37%) 5-10 sec	
	3700	Profilometry to determine etch depth	
		-- CMSE P10	
	3800	SiO ₂ Hardmask Strip	
		-- (7:1 Buffered Oxide Etch) No agitation 2 min	
	3900	Electrically Verify All Dielectric has been removed from metal surface	
		-- HP Semiconductor Parameter Analyzer/Probe Station	
	4000	Protective Layers Deposited on Sample Frontside	
		-- Waferbond Static Dispense, > 2 k rpm, 20 sec total	
		-- Hotplate Bake 110 C, 1.5 minutes	
	4100	Bond Laser piece to a silicon carrier substrate	
		-- Cleave a Silicon piece that will act as the carrier substrate	
		-- a.) Pump down chamber for ~ 1.5 min, b.) Turn off vacuum, c.) Open N ₂ to a pressure of ~22 psi	
		d.) Flow forming gas. e.) Ramp-up temp to 160 C for ~ 6 min	
	4200	Removal of WaferBond Polymer from the edge and backside of the laser substrate	
		-- Immersion in WaferBond removal solution, Room Temperature, time ~ 20 sec	
		-- Spray rinse in isopropanol to wash off removal solution	
	4300	InP Substrate Removal	
		-- Concentrated HCl (37%) ~ 8-10 um/min --> Around 46-52 min etch duration	
	4400	Partial Etch of InGaAs etch stop layer	
		A.) 200 nm InGaAs etch Stir 6.5 min, Room Temperature, Etch Time < 20 sec	
		-- Etchant 1:1:20 H ₂ SO ₄ : H ₂ O ₂ : H ₂ O --> Etch rate > 450 nm/min	
		B.) Microscope Inspection	

Figure B-3:

InP-based Laser Microcleaving Process Flow (Page 4/4)

Sample Number: _____
 Date: _____

Done?	Step	Process Description	Notes:
	4500	Backside Ohmic Photolithography	
		-- NR1-3000P Static Dispense, 3k rpm, 37 sec total	
		-- Hotplate Bake 100 C, 2 min	
		-- Exposure 45-52 sec high res aligner	
		-- Hotplate Bake 100 C, 3 min	
		-- Develop 60 sec (RD6)	
		-- Microscope Inspection	
	4600	Native Oxide Strip	
		-- (7:1 Buffered Oxide Etch) No agitation 8-10 sec, DI H ₂ O rinse	
	4700	Backside N-type Ohmic Contact Metallization	
		-- Base Pressure ~ 10 ⁻⁶ torr, Dep Pressure < 6x10 ⁻⁶ torr	
		-- Ebeam Evap. Ni(50A)/Au(100A)/Ge(600A)/Au(900A)/Ni(300A)/Au(1750A)	
	4800	Metal Liffoff Process	
		-- Microstrip 2001, 85 C, slight agitation	
	4900	Bars released from Carrier Substrate	
		-- Sample turned upside down and layed on a Teflon substrate that is immersed in	
		WaferBond removal solution, Room Temperature, time ~ 2.5 min no disturbance sec	
		-- Lift sample up slightly after this 2.5 min to see if the laser bars are coming loose. Allow sample	
		to remain in solution for another few minutes	
		-- Remove Carrier substrate, just leaving released bars. Pipette out Waferbond removing solution.	
		-- Pipette isopropanol into glassw are to allow pills to rinse	
	5000	Bars of Laser are microcleaved	
		-- Isopropanol solution containing bars of connected lasers is stimulated ultrasonically	
		-- Microscope Inspection of pills sitting in solution	
		-- Ultrasonically agitate more as needed	
		-- Pipette out isopropanol	
		-- Allow teflon piece upon w hich the micro-cleaved devices now rest to dry in the fume hood	

Figure B-4:

Appendix C

Process Recipes

C.1 Lithography Process Recipes

1.) Standard Positive Photoresist (OCG-825) Lithography

- i.) Solvent Clean (Acetone, Methanol, Isopropanol, N₂ blow dry)
- ii.) Pre-bake: Oven Temp = 200 °C, time = 10 min
- iii.) HMDS Coating: Static Dispense, 30 sec at 4000 rpm
- iv.) Bake: Oven Temp = 130 °C, 10 min
- v.) Photoresist Coating: Static Dispense, 5 sec at 750 rpm
then 30 sec at 3000 rpm
- vi.) Softbake: Oven Temp = 90 °C, 30 min
- vii.) Exposure: Karl Suss MJB3 Contact Aligner, 4.5 sec
- viii.) Develop: 934 1:1 solution, 105 sec

2.) Thick Positive Photoresist (AZ4620) Lithography

- i.) Solvent Clean (Acetone, Methanol, Isopropanol, N₂ blow dry)
- ii.) Pre-bake: Oven Temp = 200 °C, time = 10 min
- iii.) HMDS Coating: Static Dispense, 30 sec at 4000 rpm
- iv.) Bake: Oven Temp = 130 °C, 10 min
- v.) Photoresist Coating: Static Dispense, 10 sec at 1500 rpm,
then 60 sec at 3000 rpm, then 10 sec at 5000 rpm

- vi.) Softbake: Oven Temp = 90 °C, 60 min
- vii.) Exposure: Karl Suss MJB3 Contact Aligner, 24 sec
- viii.) Develop: AZ 440 solution, 150 sec
- ix.) Hardbake: Oven Temp = 90 °C, 30 min

3.) Image Reversal Photoresist (AZ5214E) Lithography

- i.) Solvent Clean (Acetone, Methanol, Isopropanol, N₂ blow dry)
- ii.) Pre-bake: Oven Temp = 200 °C, time = 10 min
- iii.) HMDS Coating: Static Dispense, 30 sec at 4000 rpm
- iv.) Bake: Oven Temp = 130 °C, 10 min
- v.) Photoresist Coating: Static Dispense, 30 sec at 2000 rpm,
- vi.) Softbake: Oven Temp = 90 °C, 30 min
- vii.) Exposure: Karl Suss MJB3 Contact Aligner, 14 sec
- viii.) Post Exposure Bake: Hotplate Temp = 105 °C, 52 sec
- ix.) Flood Exposure: Karl Suss MJB3 Contact Aligner, 2.7 min
- x.) Develop: AZ 422 solution, 60 sec

4.) Thick Negative Photoresist (NR7-3000P) Lithography

- i.) Solvent Clean (Acetone, Methanol, Isopropanol, N₂ blow dry)
- ii.) Pre-bake: Oven Temp = 200 °C, time = 10 min
- v.) Photoresist Coating: Static Dispense, 10 sec at 1500 rpm,
then 60 sec at 3000 rpm, then 10 sec at 5000 rpm
- vi.) Softbake: Oven Temp = 90 °C, 60 min
- vii.) Exposure: Karl Suss MJB3 Contact Aligner, 24 sec
- viii.) Develop: AZ 440 solution, 150 sec
- ix.) Hardbake: Oven Temp = 90 °C, 30 min

5.) Thin Negative Photoresist (NR1-1000P) Lithography

- i.) Solvent Clean (Acetone, Methanol, Isopropanol, N₂ blow dry)

- ii.) Pre-bake: Oven Temp = 200 °C, time = 10 min
- v.) Photoresist Coating: Static Dispense, 10 sec at 1500 rpm,
then 60 sec at 3000 rpm, then 10 sec at 5000 rpm
- vi.) Softbake: Oven Temp = 90 °C, 60 min
- vii.) Exposure: Karl Suss MJB3 Contact Aligner, 24 sec
- viii.) Develop: AZ 440 solution, 150 sec
- ix.) Hardbake: Oven Temp = 90 °C, 30 min

C.2 Etching Process Recipes

C.2.1 Reactive Ion Etching

Tool: EML Plasmatherm Waf'r Batch 700D

1.) Material: GaAs/AlGaAs

a.) Recipe 1

Gas Flows: 12 sccm BCl_3 , 30 sccm Ar, 5 sccm

Ar Pressure: 15 mtorr

Power: 200 W

Etch Rate: 320 - 375 nm/min

Comments: Very fast etch results in some lateral etching. Lateral etching should be able to be decreased by reducing BCl_3 flow.

b.) Recipe 2

Gas Flows: 12 sccm BCl_3

Pressure: 10 mtorr

Power: 250 W

Etch Rate: 80-100 nm/min

Comments: For deep etches (i.e., deeper than a couple of microns), problems are encountered with the etch products building up, the etch rate

slowing down, and further etching being ultimately prevented.

2.) Material: SiO_2

a.) Recipe 1

Gas Flows: 25 sccm HC23

Pressure: 20 mtorr

Power: 250 W

Etch Rate: 20 nm/min

Comments: Etch rate is for the PECVD SiO_2 with a refractive index of 1.41.

b.) Recipe 2

Gas Flows: 20 sccm HC14 (CF_4)

Pressure: 25 mtorr

Power: 300 W Etch

Rate: 35 nm/min

Comments: Etch rate is for the silicon rich PECVD deposited SiO_2 .

3.) Material: Cyclotene Benzocyclobutane (BCB)

Gas Flows: 15 sccm SF_6 , 90 sccm O_2

Pressure: mtorr

Power: 150 W

Etch Rate: 35 nm/min

Comments: BCB was fully cured at 250 °C for 60 minutes.

Tool: Lincoln Lab SAMCO ICP

1.) Material: InP/InGaAs/InGaAsP

Gas Flows: 0.5 sccm $SiCl_4$, 0.5 sccm Cl_2 , 10 sccm Ar

Pressure: 0.5 Pa

Temperature: 220 °C

Bias Power: 250 W

ICP Power: 250 W

Etch Rate: 180-250 nm/min

Comments: Sputter deposited SiO_2 hardmask etches at approximately 30 nm/min.

C.2.2 Sputter Etching

Tool: EML Materials Research Corp. 8620 Sputtering system

1.) Material: Gold

Base Pressure: $< 2 \times 10^{-6}$ torr

Gas Flows: 50 sccm Ar

Power: 150 W

Etch Rate: Sputter etches faster than nickel.

2.) Material: Nickel

Base Pressure: $< 2 \times 10^{-6}$ torr

Gas Flows: 50 sccm Ar

Power: 150 W

Etch Rate: > 12.5 nm/min

3.) Material: Chromium

Base Pressure: $< 2 \times 10^{-6}$ torr

Gas Flows: Argon, 50 sccm

Power: 150 W

Etch Rate: N/A

C.2.3 Wet Etching

1.) Material: GaAs

a.) Recipe 1

Chemistry: 10:1:1 DI H₂O : H₂O₂ (30%) : H₃PO₄ (85%)

Temperature: Room Temperature

Agitation: Yes, 400 rpm, magnetic stirrer

Etch Rate: 400 nm/min

Comments: Not AlGaAs/GaAs material selective.

b.) Recipe 2

Chemistry: 1:1 H₂O₂(30%) : NH₄OH (30%)

Temperature: Room Temperature

Agitation: Yes, magnetic stirrer

Etch Rate: 5 μm/min

Comments: Not AlGaAs/GaAs material selective.

c.) Recipe 3

Chemistry: 30:1 H₂O₂(30%) : NH₄OH (30%)

Temperature: Room Temperature

Agitation: Yes, magnetic stirrer

Etch Rate: 4 μm/min

Comments: Etches GaAs preferentially over AlAs with a selectivity of greater than 100.

2.) Material: Gold

Chemistry: Transene Gold Etchant GE-8148

Temperature: Room Temperature

Agitation: No

Etch Rate: 300 nm/min

Comments: This etchant does not attack nickel.

3.) Material: Nickel

Chemistry: Transene Nickel Etchant Type TFB

Temperature: Room Temperature

Agitation: Yes, 400 rpm, magnetic stirrer

Etch Rate: 180 nm/min

Comments: Lateral etching tends to be very significant and the degree of lateral etching varied considerably over a small sized sample.

This etchant does not attack gold films.

4.) Material: InP

Chemistry: Hydrochloric Acid

Temperature: Room Temperature

Agitation: No

Etch Rate: 6 $\mu\text{m}/\text{min}$

Comments: This etchant does not attack InGaAs.

5.) Material: InGaAs

Chemistry: 20:1:1 H₂O : H₂SO₄ (%) : H₂O₂(30%)

Temperature: Room Temperature

Agitation: No

Etch Rate: 450 nm/min

Comments: This etchant does not attack InP.

5.) Material: Sputter Deposited SiO₂

Chemistry: 7:1 Buffered Oxide Etchant

Temperature: Room Temperature

Agitation: No

Etch Rate: 100 nm/min

Comments: This etchant does not attack photoresist. Be

sure to bake the photoresist prior to BOE etching as it will

help prevent lifting off of the photoresist.

5.) Material: SmCo

Chemistry: 500:15 H_2O : HNO_3

Temperature: Room Temperature

Agitation: No

Etch Rate: 1 $\mu\text{m}/\text{min}$

Comments: This etchant does not attack photoresist.

C.3 Deposition Processes

C.3.1 Plasma Enhanced Chemical Vapor Deposition (PECVD)

Tool: EML Plasmatherm Waf'r Batch 700D

1.) Material: SiO_2 (refractive index, $n = 1.4$)

Base Pressure: $< 4 \times 10^{-4}$ torr

Gas Flows: 600 sccm SiH_4 , 300 sccm N_2O

Temperature: 250 °C

Dep. Pressure 500 mtorr

Power: 25 W

Deposition Rate: 2 $\mu\text{m}/\text{hr}$

C.3.2 Sputter Deposition

Tool: EML Materials Research Corp. 8620 Sputtering system

1.) Material: Chromium

Base Pressure: 1×10^{-6} torr

Gas Flows: 50 sccm

Ar Power: 300 W

Deposition Rate: N/A

Comments: Clean target for 15 minutes prior to deposition.

2.) Material: Nickel

Base Pressure: 1×10^{-6} torr

Gas Flows: 50 sccm Ar

Power: 350 W

Deposition Rate: 14 nm/min

Comments: Target clean before deposition needed to make sure native oxide and other contaminants are removed.

3.) Material: Gold

Base Pressure: $< 2 \times 10^{-6}$ torr

Gas Flows: 50 sccm Ar

Power: 200 W

Deposition Rate: 25 nm/min

Comments: Short target clean prior to deposition needed to clean target of contaminants.

4.) Material: SiO₂

Base Pressure: $< 2 \times 10^{-6}$ torr

Gas Flows: 60 sccm Ar

Power: 200 W

Deposition Rate: 2.25 nm/min

Comments: Short target clean prior to deposition needed to clean target of contaminants.

C.3.3 Electron-Beam Deposition

Tool: EML E-beam Deposition System

1.) Material: Chromium

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 50 mA

Deposition Rate: 1-2 Å/s

2.)Material: Nickel

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 100 mA

Deposition Rate: 1-2 Å/s

3.) Material: Gold

Base Pressure: $< 2 \times 10^{-6}$ torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 120 mA

Deposition Rate: 2-3.5 Å/s

4.)Material: Titanium

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 50 mA

Deposition Rate: 1-2 Å/s

5.)Material: Platinum

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 225 mA

Deposition Rate: 1.5-2.5 Å/s

6.)Material: Germanium

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 80 mA

Deposition Rate: 1.5-2.5 Å/s

6.)Material: Indium

Base Pressure: 1×10^{-6} torr

Run Pressure: $< 3.5 \times 10^{-6}$ torr

Current: 25 mA

Deposition Rate: 1.5-3.5 Å/s

C.3.4 Electrodeposition

1.) Material: Nickel

Solution: Technic Inc. Nickel "S" solution

Anode: Nickel

Current Density: 74 mA/cm²

Temperature: 38 °C

Deposition Rate: 0.342 J nm/s where J is the current density in mA/cm²

2.) Material: Cobalt

Solution: 375 g/l $\text{CoCl}_2 \cdot 6\text{H}_2\text{O}$, 37.5 g/l H_3BO_3 , pH 3.6

Anode: Cobalt

Current Density: 20 mA/cm²

Temperature: Room Temperature

Deposition Rate: 7.02 nm/s

2.) Material: Gold

Solution: Technic Inc. Techni-Gold 25E

Anode: Platinum Clad

Current Density: 19.4 mA/cm²

Temperature: 60 °C

Deposition Rate: 20.5 nm/s

C.4 Photomask Making Process

i.) Develop: MIF 915 or MIF 917 solution, 80 sec

ii.) DI H₂O Rinse and N₂ Dry

iii.) Chrome Etch CR7, 80 sec

iv.) DI H₂O Rinse and N₂ Dry

v.) Visual Inspection

vi.) Chrome Etch CR7, 20 sec or more until complete

vii.) DI H₂O Rinse and N₂ Dry

viii.) Photoresist Strip: Nanostrip (Sulfuric Acid, Hydrogen Peroxide solution), 10 min

Appendix D

Magnetic Retention Force

Theoretical Model

D.1 Hard Magnetic Film with Perpendicularly Oriented Magnetization

D.1.1 Array of Squares Pattern

$$\psi_I = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\sin k_x x \sin k_y y A_1 e^{-k_z(z-\frac{d}{2}-g-t)} + \sin k_x x A_2 e^{-k_x(z-\frac{d}{2}-g-t)} + \sin k_y y A_3 e^{-k_y(z-\frac{d}{2}-g-t)} \right] \quad (\text{D.1})$$

$$\begin{aligned} \psi_{II} = & \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\sin k_x x \sin k_y y \left(B_1 e^{-k_z(z-\frac{d}{2}-g-t)} + C_1 e^{k_z(z-\frac{d}{2}-g-t)} \right) \right. \\ & \left. + \sin k_x x \left(B_2 e^{-k_x(z-\frac{d}{2}-g-t)} + C_2 e^{k_x(z-\frac{d}{2}-g-t)} \right) + \sin k_y y \left(B_3 e^{-k_y(z-\frac{d}{2}-g-t)} + C_3 e^{k_y(z-\frac{d}{2}-g-t)} \right) \right] \end{aligned} \quad (\text{D.2})$$

$$\begin{aligned} \psi_{III} = & \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\sin k_x x \sin k_y y \left(D_1 e^{-k_z(z-\frac{d}{2})} + E_1 e^{k_z(z-\frac{d}{2})} \right) + \sin k_x x \left(D_2 e^{-k_x(z-\frac{d}{2})} + E_2 e^{k_x(z-\frac{d}{2})} \right) \right. \\ & \left. + \sin k_y y \left(D_3 e^{-k_y(z-\frac{d}{2})} + E_3 e^{k_y(z-\frac{d}{2})} \right) \right] \end{aligned} \quad (\text{D.3})$$

$$\psi_{IV} = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\sin k_x x \sin k_y y \left(F_1 e^{-k_z z} + G_1 e^{k_z z} \right) \right. \\ \left. + \sin k_x x \left(F_2 e^{-k_x z} + G_2 e^{k_x z} \right) + \sin k_y y \left(F_3 e^{-k_y z} + G_3 e^{k_y z} \right) + Kz \right] \quad (\text{D.4})$$

$$\psi_V = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\sin k_x x \sin k_y y H_1 e^{k_z(z+\frac{d}{2})} + \sin k_x x H_2 e^{k_x(z+\frac{d}{2})} + \sin k_y y H_3 e^{k_y(z+\frac{d}{2})} \right] \quad (\text{D.5})$$

where $k_z^2 = k_x^2 + k_y^2$ and $A_i, B_i, D_i, E_i, F_i, G_i, H_i$, and K for $i=1$ to 3 are constants and given in the Derived Parameters subsection.

Derived Parameters

$$A_1 = \frac{8\mu_s M_r}{\pi^2 m n k_z} \left(e^{-k_z g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.6})$$

$$B_1 = \frac{4(\mu_s + 1) M_r}{\pi^2 m n k_z} \left(e^{-k_z g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.7})$$

$$C_1 = \frac{4(\mu_s - 1) M_r}{\pi^2 m n k_z} \left(e^{-k_z g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.8})$$

$$D_1 = \frac{2M_r}{\pi^2 m n k_z} \left(1 - e^{-k_x d} \right) \quad (\text{D.9})$$

$$E_1 = \frac{-2(\mu_s^2 - 1) M_r}{\pi^2 m n k_z} \left(e^{-2k_z g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.10})$$

$$F_1 = \frac{-2M_r}{\pi^2 m n k_z} \left(e^{-\frac{k_z d}{2}} \right) \quad (\text{D.11})$$

$$G_1 = \frac{2M_r}{\pi^2 m n k_z} \left(\frac{e^{-2k_z g}}{e^{\frac{3k_z d}{2}}} \right) \\ \left(\frac{-\mu_s^2 - e^{k_z(d+2g)} (\mu_s - 1)^2 + e^{k_z(d+2g+2t)} (\mu_s + 1)^2 + (e^{k_z d} + e^{2k_z t} - e^{k_z(d+2t)}) (\mu_s^2 - 1) + 1}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.12})$$

$$H_1 = \frac{2M_r}{\pi^2 m n k_z} \left(\frac{1}{e^{2k_z g}} \right) \quad (\text{D.13})$$

$$A_2 = \frac{2\mu_s M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.14})$$

$$B_2 = \frac{(\mu_s + 1) M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.15})$$

$$C_2 = \frac{(\mu_s - 1) M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.16})$$

$$D_2 = \frac{M_r}{2\pi m k_x} \left(1 - e^{-k_x d} \right) \quad (\text{D.17})$$

$$E_2 = \frac{-(\mu_s^2 - 1)M_r}{2\pi m k_x} \left(e^{-2k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.18)$$

$$F_2 = \frac{-M_r}{2\pi m k_x} \left(e^{-\frac{k_x d}{2}} \right) \quad (D.19)$$

$$G_2 = \frac{M_r}{2\pi m k_x} \left(\frac{e^{-2k_x g}}{e^{\frac{3k_x d}{2}}} \right) \left(\frac{-\mu_s^2 - e^{k_x(d+2g)}(\mu_s - 1)^2 + e^{k_x(d+2g+2t)}(\mu_s + 1)^2 + (e^{k_x d} + e^{2k_x t} - e^{k_x(d+2t)})(\mu_s^2 - 1) + 1}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.20)$$

$$H_2 = \frac{M_r}{2\pi m k_x} \left(\frac{1}{e^{2k_x g}} \right) \quad (D.21)$$

$$A_3 = \frac{2\mu_s M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.22)$$

$$B_3 = \frac{(\mu_s + 1)M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.23)$$

$$C_3 = \frac{(\mu_s - 1)M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.24)$$

$$D_3 = \frac{M_r}{2\pi n k_y} \left(1 - e^{-k_y d} \right) \quad (D.25)$$

$$E_3 = \frac{-(\mu_s^2 - 1)M_r}{2\pi n k_y} \left(e^{-2k_y g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.26)$$

$$F_3 = \frac{-M_r}{2\pi n k_y} \left(e^{-\frac{k_y d}{2}} \right) \quad (D.27)$$

$$G_3 = \frac{M_r}{2\pi n k_y} \left(\frac{e^{-2k_y g}}{e^{\frac{3k_y d}{2}}} \right) \left(\frac{-\mu_s^2 - e^{k_y(d+2g)}(\mu_s - 1)^2 + e^{k_y(d+2g+2t)}(\mu_s + 1)^2 + (e^{k_y d} + e^{2k_y t} - e^{k_y(d+2t)})(\mu_s^2 - 1) + 1}{e^{2k_y t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (D.28)$$

$$H_3 = \frac{M_r}{2\pi n k_y} \left(e^{-2k_y g} \right) \quad (D.29)$$

$$F_{const} = \frac{M_r}{4} \quad (D.30)$$

D.1.2 Array of Stripes Pattern

$$\psi_I = \sum_{n, \text{odd}}^{\infty} \sin k_y y A_3 e^{-k_y(z - \frac{d}{2} - g - t)} \quad (\text{D.31})$$

$$\psi_{II} = \sum_{n, \text{odd}}^{\infty} \sin k_y y \left(B_3 e^{-k_y(z - \frac{d}{2} - g - t)} + C_3 e^{k_y(z - \frac{d}{2} - g - t)} \right) \quad (\text{D.32})$$

$$\psi_{III} = \sum_{n, \text{odd}}^{\infty} \sin k_y y \left(D_3 e^{-k_y(z - \frac{d}{2})} + E_3 e^{k_y(z - \frac{d}{2})} \right) \quad (\text{D.33})$$

$$\psi_{IV} = \sum_{n, \text{odd}}^{\infty} \sin k_y y \left(F_3 e^{-k_y z} + G_3 e^{k_y z} \right) + F_{\text{const}} z \quad (\text{D.34})$$

$$\psi_V = \sum_{n, \text{odd}}^{\infty} \sin k_y y H_3 e^{k_y(z + \frac{d}{2})} \quad (\text{D.35})$$

Derived Parameters

$$A_3 = \frac{4\mu_s M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_y d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.36})$$

$$B_3 = \frac{2(\mu_s + 1) M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_y d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.37})$$

$$C_3 = \frac{2(\mu_s - 1) M_r}{\pi n k_y} \left(e^{-k_y g} \right) \left(1 - e^{-k_y d} \right) \left(\frac{e^{k_y t}}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.38})$$

$$D_3 = \frac{M_r}{\pi n k_y} \left(1 - e^{-k_y d} \right) \quad (\text{D.39})$$

$$E_3 = \frac{-(\mu_s^2 - 1) M_r}{\pi n k_y} \left(e^{-2k_y g} \right) \left(1 - e^{-k_y d} \right) \left(\frac{e^{2k_y t} - 1}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.40})$$

$$F_3 = \frac{-M_r}{\pi n k_y} \left(e^{-\frac{k_y d}{2}} \right) \quad (\text{D.41})$$

$$G_3 = \frac{M_r}{\pi n k_y} \left(\frac{e^{-2k_y g}}{e^{\frac{3k_y d}{2}}} \right) \left(\frac{1 - \mu_s^2 - e^{k_y(d+2g)} (\mu_s - 1)^2 + e^{k_y(d+2g)} e^{2k_y t} (\mu_s + 1)^2 + (\mu_s^2 - 1) (e^{k_y d} + e^{2k_y t} - e^{k_y(d+2t)})}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.42})$$

$$H_3 = \frac{M_r}{\pi n k_y} \left(e^{-2k_y g} \right) e^{-k_y d} \left(1 - e^{-k_y d} \right) \left(\frac{-1 + \mu_s^2 + e^{k_y(d+2g)} (\mu_s - 1)^2 - e^{k_y(d+2g+2t)} (\mu_s + 1)^2 - e^{k_y t} (\mu_s^2 - 1)}{e^{2k_y t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.43})$$

$$K = \frac{M_r}{2} \quad (\text{D.44})$$

D.2 Hard Magnetic Film with In-Plane Oriented Magnetization

D.2.1 Array of Squares Pattern

$$\psi_I = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\cos k_x x \sin k_y y A_1 e^{-k_z(z-\frac{d}{2}-g-t)} + \cos k_x x A_2 e^{-k_x(z-\frac{d}{2}-g-t)} \right] \quad (\text{D.45})$$

$$\begin{aligned} \psi_{II} = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\cos k_x x \sin k_y y \left(B_1 e^{-k_z(z-\frac{d}{2}-g-t)} + C_1 e^{k_z(z-\frac{d}{2}-g-t)} \right) \right. \\ \left. + \cos k_x x \left(B_2 e^{-k_x(z-\frac{d}{2}-g-t)} + C_2 e^{k_x(z-\frac{d}{2}-g-t)} \right) \right] \end{aligned} \quad (\text{D.46})$$

$$\psi_{III} = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\cos k_x x \sin k_y y \left(D_1 e^{-k_z(z-\frac{d}{2})} + E_1 e^{k_z(z-\frac{d}{2})} \right) + \cos k_x x \left(D_2 e^{-k_x(z-\frac{d}{2})} + E_2 e^{k_x(z-\frac{d}{2})} \right) \right] \quad (\text{D.47})$$

$$\begin{aligned} \psi_{IV} = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\cos k_x x \sin k_y y \left(\frac{-4k_x M_r}{\pi^2 m n (k_x^2 + k_y^2)} + F_1 e^{-k_z z} + G_1 e^{k_z z} \right) \right. \\ \left. + \cos k_x x \left(\frac{-M_r}{\pi m k_x} + F_2 e^{-k_x z} + G_2 e^{k_x z} \right) \right] \end{aligned} \quad (\text{D.48})$$

$$\psi_V = \sum_{m, \text{odd}}^{\infty} \sum_{n, \text{odd}}^{\infty} \left[\cos k_x x \sin k_y y H_1 e^{k_z(z+\frac{d}{2})} + \cos k_x x H_2 e^{k_x(z+\frac{d}{2})} \right] \quad (\text{D.49})$$

where $A_i, B_i, D_i, E_i, F_i, G_i, H_i$, and K for $i=1$ to 2 are constants and are given in the Derived Parameters subsection.

Derived Parameters

$$A_1 = -\frac{8k_x \mu_s M_r}{\pi^2 m n k_z^2} \left(e^{-k_z g} \right) \left(1 - e^{-k_z d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.50})$$

$$B_1 = -\frac{4k_x (\mu_s + 1) M_r}{\pi^2 m n k_z^2} \left(e^{-k_z g} \right) \left(1 - e^{-k_z d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.51})$$

$$C_1 = -\frac{4k_x (\mu_s - 1) M_r}{\pi^2 m n k_z^2} \left(e^{-k_z g} \right) \left(1 - e^{-k_z d} \right) \left(\frac{e^{k_z t}}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.52})$$

$$D_1 = -\frac{2k_x M_r}{\pi^2 m n k_z^2} \left(1 - e^{-k_z d} \right) \quad (\text{D.53})$$

$$E_1 = \frac{2k_x (\mu_s^2 - 1) M_r}{\pi^2 m n k_z^2} \left(e^{-2k_z g} \right) \left(1 - e^{-k_z d} \right) \left(\frac{e^{2k_z t} - 1}{e^{2k_z t} (\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.54})$$

$$F_1 = \frac{2k_x M_r}{\pi^2 m n k_z^2} \left(e^{-\frac{k_z d}{2}} \right) \quad (\text{D.55})$$

$$G_1 = \frac{2k_x M_r}{\pi^2 m n k_z^2} \left(\frac{e^{-2k_z g}}{e^{\frac{3k_z d}{2}}} \right) \left(\frac{-\mu_s^2 - e^{k_z(d+2g)}(\mu_s - 1)^2 + e^{k_z(d+2g+2t)}(\mu_s + 1)^2 + (e^{k_z d} + e^{2k_z t} - e^{k_z(d+2t)})(\mu_s^2 - 1) + 1}{e^{2k_z t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.56})$$

$$H_1 = \frac{2k_x M_r}{\pi^2 m n k_z^2} e^{-2k_z g} e^{-k_z d} \left(1 - e^{-k_z d} \right) \left(\frac{1 - \mu_s^2 + (\mu_s - 1)^2 e^{k_z(d+2g)} - (\mu_s + 1) e^{k_z(d+2g+2t)} + (\mu_s^2 - 1) e^{2k_z t}}{e^{2k_z t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.57})$$

$$A_2 = -\frac{2\mu_s M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.58})$$

$$B_2 = -\frac{(\mu_s + 1) M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.59})$$

$$C_2 = -\frac{(\mu_s - 1) M_r}{\pi m k_x} \left(e^{-k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{k_x t}}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.60})$$

$$D_2 = -\frac{M_r}{2\pi m k_x} \left(1 - e^{-k_x d} \right) \quad (\text{D.61})$$

$$E_2 = \frac{(\mu_s^2 - 1) M_r}{2\pi m k_x} \left(e^{-2k_x g} \right) \left(1 - e^{-k_x d} \right) \left(\frac{e^{2k_x t} - 1}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.62})$$

$$F_2 = \frac{M_r}{2\pi m k_x} \left(e^{-\frac{k_x d}{2}} \right) \quad (\text{D.63})$$

$$G_2 = \frac{M_r}{2\pi m k_x} \left(\frac{e^{-2k_x g}}{e^{\frac{3k_x d}{2}}} \right) \left(\frac{\mu_s^2 - e^{k_x(d+2g)}(\mu_s - 1)^2 + e^{k_x(d+2g+2t)}(\mu_s + 1)^2 + (-e^{k_x d} - e^{2k_x t} + e^{k_x(d+2t)})(\mu_s^2 - 1) - 1}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.64})$$

$$H_2 = \frac{M_r}{2\pi m k_x} \left(e^{-2k_x g} \right) \left(e^{-k_x d} \right) \left(1 - e^{-k_x d} \right) \left(\frac{-\mu_s^2 + e^{k_x(d+2g)}(\mu_s - 1)^2 - e^{k_x(d+2g+2t)}(\mu_s + 1)^2 + e^{k_x t}(\mu_s^2 - 1) + 1}{e^{2k_x t}(\mu_s + 1)^2 - (\mu_s - 1)^2} \right) \quad (\text{D.65})$$

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