

Technology and Market Evaluation for Semiconductor Nanowire Transistors

By

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Submitted to the Department of Materials Science and Engineering in Partial Fulfillment of the Requirements for the Degree of Master of Engineering in Materials Science and Engineering

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ABSTRACT

Information processing systems have been getting more powerful over the course of the past three decades due to the scaling of transistor dimensions. Scaling of transistor dimension causes a plethora of technological problems if pursued in the current fashion. Gate-All-Around architecture for transistors has been shown to alleviate many of the problems posed by scaling. Silicon being the material of choice of the semiconductor industry, it is highly desirable to have silicon one dimensional channel in the Gate-All-Around transistor. Silicon nanowires have been fabricated using various methods, in this work Self-Limiting-Oxidation was analyzed for its technological feasibility and found to be satisfactory. Possible value propositions and IP landscape analysis show that this methodology is very much feasible. As the new architecture essentially solves the problems that arise due to aggressive scaling, it becomes vital to look at the relevance of scaling beyond 45 nm technology node. Careful analysis of the semiconductor industry breakdown and top semiconductor foundries' financials reveal that scaling might not be pursued as aggressively as expected. The relevance of Moore's law in the current scheme of things could be that of a *Self-fulfilling prophecy*. Given this climate, Self Limiting Oxidation based Silicon nanowires have better commercial potential in the field of sensors. Monolithic integration and superior spatial precision makes this methodology ideally suited to the needs of applications which include many different kinds of sensors on the same Lab-on-Chip.

Thesis Supervisor: Eugene Fitzgerald

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CONTENTS

1	Introduction	7
2	Scaling and Problems	8
2.1	Power Leakage	9
2.2	Short Channel effect	10
3	Potential Solutions	10
4	Nanowire fabrication	11
4.1	VLS growth	12
4.2	Self-Limiting-Oxidation	15
5	Unique Advantages of GAA transistors using SLO	17
6	Alternate Approaches	18
6.1	Improvements to be made	21
7	Estimated Timeline	21
8	Feasibility	22
9	IP landscape	22
9.1	Patents	23
10	Value realization	24
11	Cost Evaluation	25
12	Value Proposition	26
13	Market Breakdown	27
13.1	End-Use Market Segmentation	29
14	Semiconductor Foundry Evaluation	30
14.1	TSMC	32
14.2	UMC	34
14.3	Chartered Semiconductor	36
14.4	SMIC	37
14.5	Consolidated Analysis	39
15	Industry Outlook	40
16	Profitability Vs Investment	40
17	SLO Si nanowire sensors	42

18	Conclusion	44
19	References.....	46

LIST OF FIGURES

Figure 1: Moore's Law [2]	7
Figure 2: Transistor and interconnects.....	9
Figure 3: Power Consumption [5].....	9
Figure 4: Transistor Architectures	11
Figure 5: VLS nanowire growth [10].....	12
Figure 6: VLS nanowire diameter [11].....	13
Figure 7: Templated Au clusters [11].....	13
Figure 8: LIL VLS growth template [12]	14
Figure 9: Transistor characteristics of VLS nanowire [13]	14
Figure 10: Schematic of SLO technique.....	15
Figure 11: Cross sectional TEM of Si nanowire with gate dielectric [8]	16
Figure 12: Transistor Characteristics of GAA transistor [16]	16
Figure 13: Inverter switching [17].....	17
Figure 14: Inverter - SLO nanowire GAA transistors [17].....	17
Figure 15: Low Temperature transistor characteristics [18].....	18
Figure 16: Evaluation of Alternate technologies [19].....	19
Figure 17: CNT GAA transistor and characteristics [20].....	20
Figure 18: GNR top-back-gate transistor (Schematic and SEM image) [21].....	20
Figure 19: Key areas of concern	22
Figure 20: Cost evaluation	25
Figure 21: Electronics Industry Revenue [3].....	26
Figure 22: Worldwide Semiconductor Market Product breakdown (2006) [23].....	27
Figure 23: Semiconductor product revenue plot.....	28
Figure 24: Percentage increase in revenue (Year-on-year).....	29
Figure 25: End-Use Market Breakdown	30
Figure 26: Semiconductor foundry revenue split [25].....	31

Figure 27: TSMC Revenue w.r.t Technology Node and Gross Margin %.....	33
Figure 28: TSMC Technology Node - Revenue Share.....	34
Figure 29: TSMC - 65 nm Sales (Billion NT\$).....	34
Figure 30: UMC Revenue w.r.t Technology Node and Gross Margin %.....	35
Figure 31: UMC - Technology Node - Revenue Share	35
Figure 32: Chartered Revenue w.r.t Technology Node and Growth Margin %.....	36
Figure 33: Chartered - Technology Node revenue share	37
Figure 34: 65 nm revenue of Chartered (US \$ Millions).....	37
Figure 35: SMIC revenue w.r.t Technology Node and Gross Margin %	38
Figure 36: SMIC - Technology Node Percentage Revenue Share	38
Figure 37: Consolidate Revenue w.r.t important technology nodes.....	39
Figure 38: Gross Margin % - Semiconductor Manufacturers.....	40
Figure 39: Intel's Profitability Vs Investment [30]	41
Figure 40: (a) SiNW with pads (b) Adhered species on SiNW causing conductivity to change	1
Figure 41: (a) Optical image of 200 μm long nanowire array showing 100 wires; zoom-in SEM image shows nanowires spaced at 2 μm with metal lines and passivation layer. (b) TEM image of nanowire showing rectangular cross-section [32].....	43
Figure 42: Temperature–conductance ($\sigma(T)$) plot for the resistor type poly-silicon nanowires [32]	44

LIST OF TABLES

Table 1: Gate length scaling	22
Table 2: Patent Summary.....	24
Table 3: Major Foundry revenue split up across segments.....	32

1 Introduction

Silicon CMOS has been the technology of choice of the microelectronics industry for the past three decades. Intel Corp. alone makes approximately US \$ 10 Billion in quarterly revenue; this goes to show the size of the industry and its importance [1]. The most important concern of the industry has been to manufacture smaller and more powerful microprocessors with every passing year. This has been flaunted as the Moore's law, which summaries the trend that number of transistors in a given area doubles every two years. Figure 1 shows the historical trend in the increase of number of transistors and it is quite an astonishing fact that the industry has kept up with this trend for over three decades.

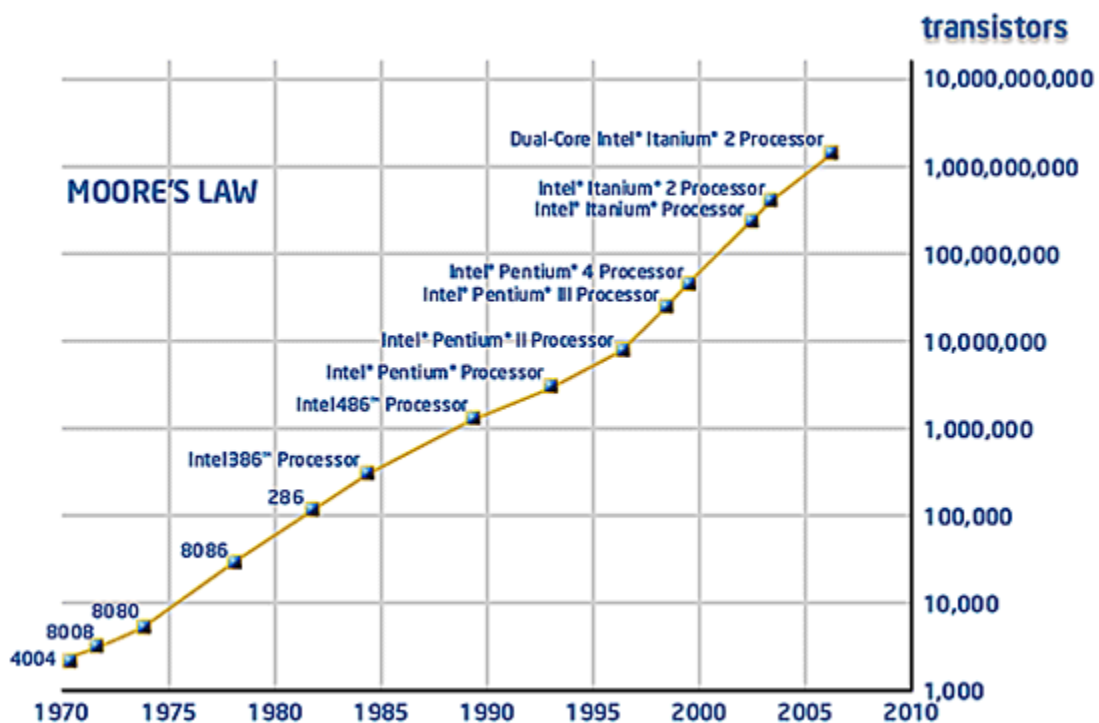


Figure 1: Moore's Law [2]

It should be noted that scaling of transistors is not the only alternative to making more functional and efficient information processing systems (microprocessors). Multi core architecture, distributed programming and application specific information processing systems are making processors more efficient and functional. Nonetheless, putting more

transistors into the processor is still considered the *Mantra* for the industry [3] and is valid in the sense that consumers wouldn't opt to buy new processors if the processors are not faster than what they already possess. Having more transistors on a microprocessor has many associated problems and possible solutions. In this thesis, semiconductor (specifically Si) nanowire transistors grown using specific methods will be analyzed for technological feasibility and market impact.

The initial sections of this thesis will cover the problems associated with scaling and potential solutions. Self-Limiting Oxidation will be critically analyzed to prove technological feasibility. After looking at various alternate technologies, a rough financial model for this line of research to be further pursued will be presented along with a discussion of the patent/IP landscape. This will be followed by a hard look at major semiconductor industry establishments to ascertain the role of Moore's law and scaling in the future of semiconductors. Based on the analysis it will be shown that Moore's law is becoming more of a Self fulfilling Prophecy and not a model where customer demand increases proportionally.

2 Scaling and Problems

Microprocessor is system of interconnected active devices called the transistors. Figure 2 shows the transistor in the left and interconnects on the right. Scaling generally refers to the reduction in transistor device dimensions to accommodate more transistors. The gate length is the distance between the source and drain; which is controlled by the gate voltage. This is gate length is currently at 45 nm. As the gate length reduces, there are various issues at the device and interconnect level. For the purpose of this report, we will go through the salient issues at the device level. Due to a variety of factors, it can be concluded that conventional CMOS scaling can't provide the solution for sub-22 nm generation [4].

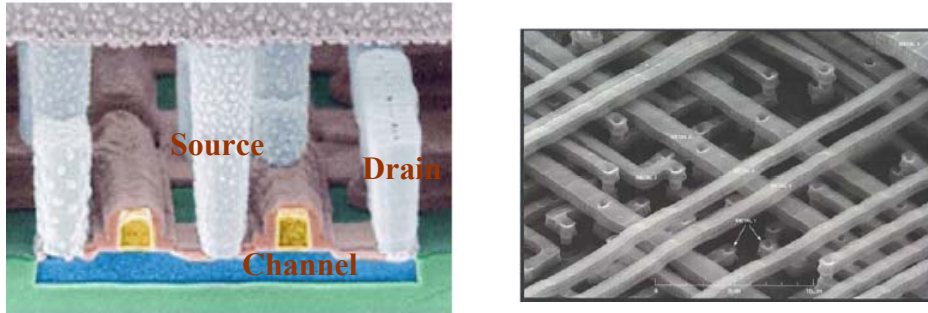


Figure 2: Transistor and interconnects

2.1 Power Leakage

As the channel length keeps shrinking, the gate dielectric thickness is reduced to have high drain current (which translates into faster switching devices). When the gate dielectric is extremely thin (2 nm currently), the electrons start to tunnel through the gate dielectric towards the gate electrode. This increases the OFF state power consumption (Passive power consumption). From the beginning of extreme scaling, leakage power has been increasing steadily as shown in Figure 3. With increase in mobile computing devices, reduction of power consumption is of at most importance and this is a major stumbling block along the path of continual scaling.

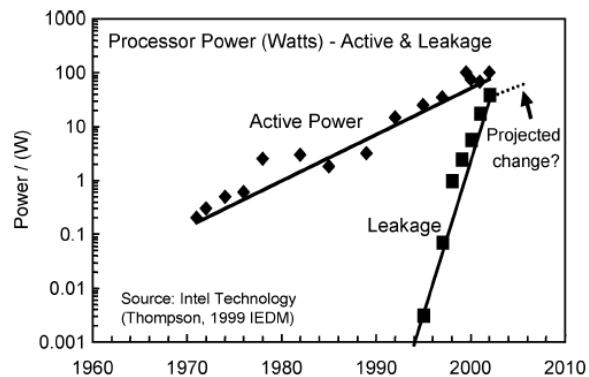


Figure 3: Power Consumption [5]

2.2 Short Channel effect

Short channel effect is phenomena where electrons start tunneling between source and drain. The means gate loses it control over the transport of carriers. This severely affects the switching device's integrity and also adds to the power loss during the OFF state. In extreme cases this leads to degradation in switching behavior leaving the device completely useless [4]. Thus short channel effect is a very predominant issue in nanoscale transistors that severely affects the threshold gate voltage. Apart from power and short channel issues, fluctuation of device parameters due to process variation is exaggerated at nano dimensions [3].

3 Potential Solutions

As we can see, there is a realistic issue with conventional CMOS scaling and the industry has taken many innovative steps to counter these problems. Strained Si grown on SiGe has been extremely important to increasing the speed of devices (drive current) without changing gate dielectric thickness (thereby reducing gate leakage current) [6]. Use of alternate gate dielectric oxides has been another route towards countering the gate leakage problem. High-K dielectric like HfO is being used in the current 45 nm processors that Intel Corp. is manufacturing. Apart from these, implementation of different transistor architecture is believed to solve many of the problems associated with scaling. Figure 4 (cross-sectional view) shows the conventional CMOS architecture on the left and Gate-All-Around (GAA) architecture on the right. In the case of GAA transistors the gate wraps around a cylindrical semiconductor channel and the gate controls the channel from all directions.

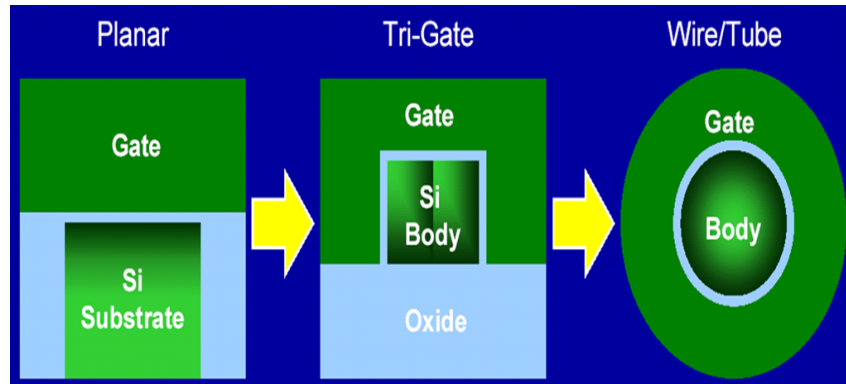


Figure 4: Transistor Architectures

GAA transistors have been shown to have much better electrostatic control in simulations when compared to tri-gate and conventional architecture [7]. The control of the gate is greatly enhanced when the diameter of the semiconductor channel is less than 10 nm. This calls for the fabrication of GAA transistors with semiconductor nanowire as the channel in between. It has also been shown experimentally that nanowire based GAA transistors have very low Drain-Induces-Barrier-Lowering (DIBL) and Sub-threshold gradient [8] [9].

The problem of scaling can be effectively solved using GAA transistors and given the current hunger for more powerful processing systems, there is a healthy demand for technology that will make GAA transistors compatible with the current CMOS technology. To evaluate further, the best possible methodology for growing nanowires and fabrication of transistor needs to be picked.

4 Nanowire fabrication

For the purpose of GAA transistors, single crystalline nanowire is needed. Smaller diameter is better for the application of GAA transistor, but the variation of diameter should be minimal since the operating characteristics of the transistor are highly dependant on the nanowire diameter. High degree of geometric versatility and reliable placement is highly desired during the back-end (to connect the transistors using interconnects) phase. Vapor-Liquid-Solid (VLS) and Self-Limiting-Oxidation (SLO) methodologies for growing nanowire will be analyzed to find the most feasible route.

4.1 VLS growth

VLS nanowire growth is the most popular route to grow nanowires and has been around since 1964 [10]. In this case, metal nano-clusters are embedded on the substrate followed by initiation of SiH_4 flow. Si preferentially melts in the vicinity of metal clusters due to decrease in melting point. This leads to super-saturation of Si in the Si-metal solution and Si solid is deposited on the surface. As the growth proceeds, the metal nano-cluster is pushed to the top and more Si is deposited at the Si / metal interface. Figure 5 illustrates the VLS technique schematically.

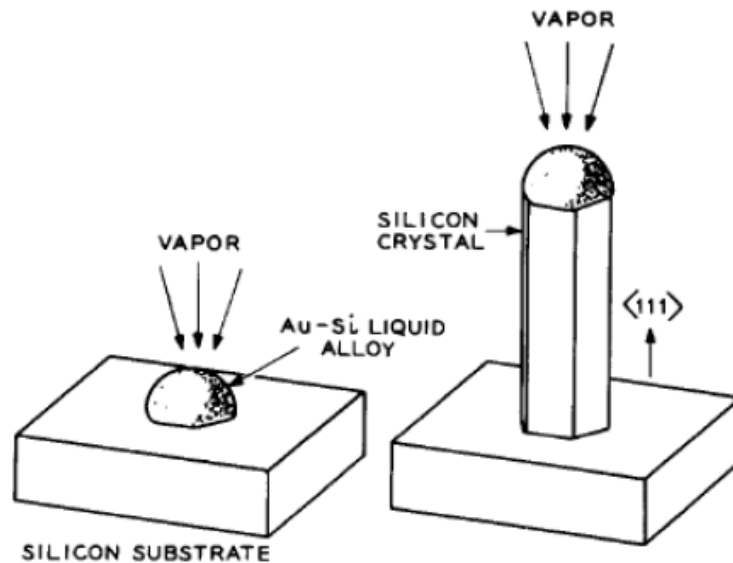


Figure 5: VLS nanowire growth [10]

Being a Bottom-Up technique, high throughput can be achieved. VLS growth can be performed in atmospheric pressure CVD chamber and thus is relatively cheap. Good control of nanowire diameter can be achieved as shown in Figure 6.

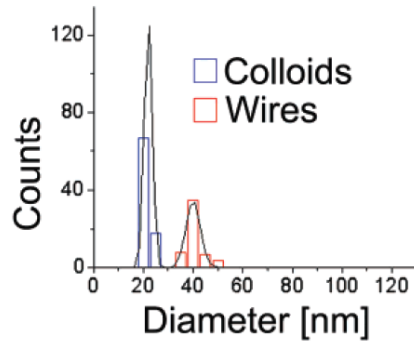


Figure 6: VLS nanowire diameter [11]

Growing nanowires precisely at a given location is very difficult in this technique. To obtain geometric precision, the metal clusters need to be placed with high degree of precision. This has been a problem with most bottom-up techniques and this potentially inhibits this technique to be used for making GAA transistors. Top-Down techniques have been used to provide the nano-clusters a template and thereby define the location of nanowires. A. I. Hochbaum et al. used polymer stamping to define the location of metal clusters and thereby the location of nanowires [11] as shown in Figure 7. This technique still doesn't grow single nanowires at specific locations. Like mentioned earlier GAA transistors need single nanowires to be grown at specific locations.

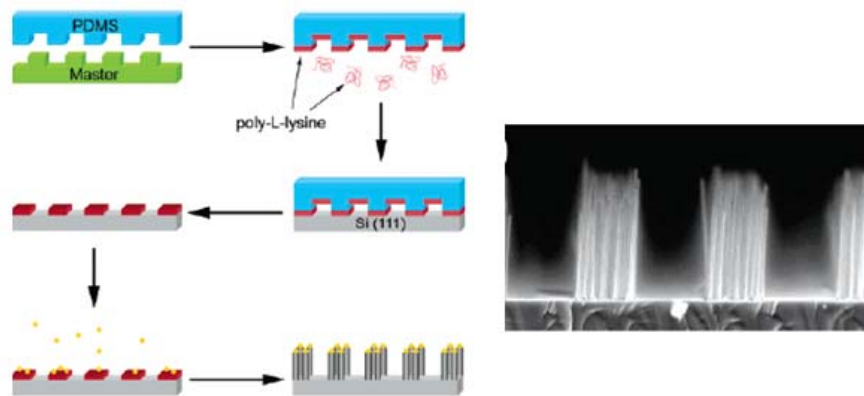


Figure 7: Templated Au clusters [11]

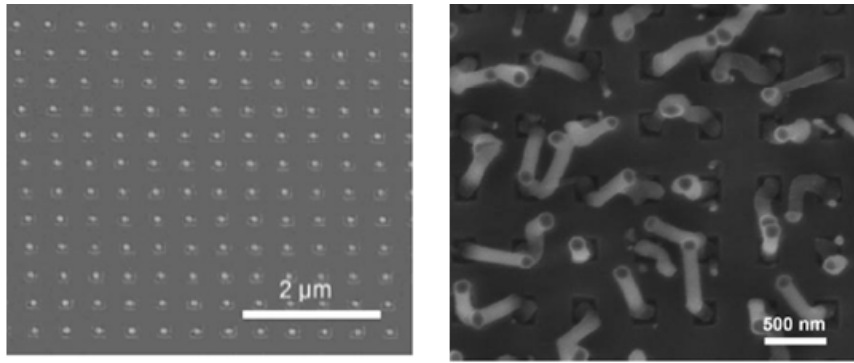


Figure 8: LIL VLS growth template [12]

W. K Choi et al. have effectively used Laser-Interference-Lithography (LIL) to template Au clusters to grow Si nanowires. This technique still doesn't guarantee crystalline nanowires. This limits this techniques use in GAA transistors.

In spite of the above restrictions, GAA transistors have been demonstrated using VLS growth. Vertical transistors are not preferred generally owing to the difficulty in inter-device connection and restrictions on films that can be deposited on top of the device. Fluidic flow of nanowires across micro-channels has been used to fabricate top-back-gate transistors [13] [14] and transistors with good witching characteristics have been demonstrated as shown in Figure 9 .

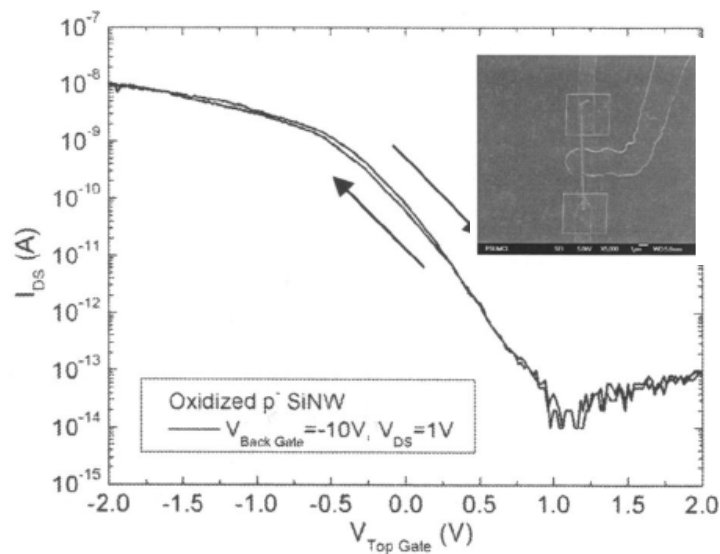


Figure 9: Transistor characteristics of VLS nanowire [13]

From the above reasoning, VLS growth has many short comings when it comes to GAA transistors. Au is the metal cluster of choice and it is well know that Au is totally incompatible with CMOS fabrication lines. Lack of precision and geometric versatility limits its use in transistor fabrication methodology. VLS is better suited for lighting applications in photonics, but is not meant for fabricating GAA transistors.

4.2 Self-Limiting-Oxidation

J. Kedzierski et al. demonstrated a decade back that oxidation can be used to fabricate nanowires with high level of crystalline structure [15]. Figure 10 shows the schematic of growing nanowires using SLO technique. A Si fin (40 – 50 nm) is oxidized and the core is left with Si nanowires (4 – 5 nm). The stress developed due the oxidation of Si limits further oxidation of the Si core. Thus this process is not time limited making it more robust. Very small nanowires can be grown with good control over the diameter. SLO technique is a CMOS compatible process and high throughput can be achieved by using DUV optical steppers. For industrial production, DUV with Alternating-Phase-Shift-Masks can be used to define the fin and in research setting, EBL can be used. The Si fin can be defined as per geometric requirements, which translates into high degree of geometric versatility of the process. N. Singh et al. demonstrated the use of SLO technique and top wire removal to fabricated GAA transistors [8]. Figure 11 shows the cross sectional image of the GAA transistor confirming the 4 nm nanowire diameter.

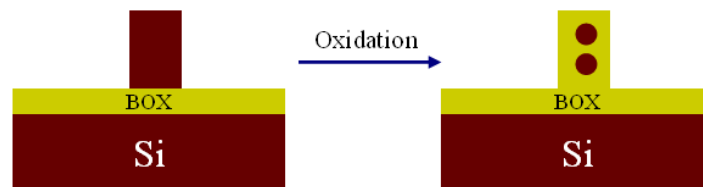


Figure 10: Schematic of SLO technique

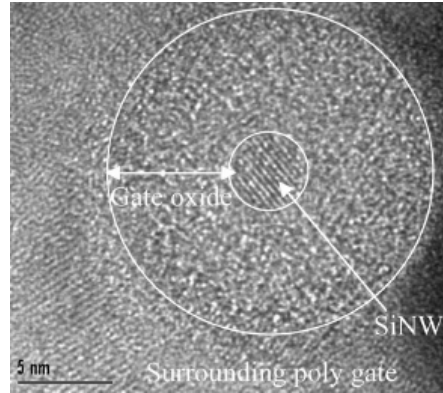


Figure 11: Cross sectional TEM of Si nanowire with gate dielectric [8]

These transistors have been shown to have excellent switching characteristics and effectively counter short channel effect and gate leakage as shown in Figure 12. Both the highest DIBL and sub-threshold gradient are less than 50 mV/V and 60 mV/dec. respectively.

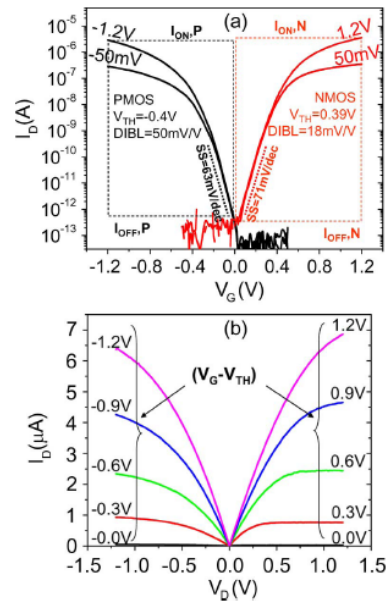


Figure 12: Transistor Characteristics of GAA transistor [16]

Inverters are the most basic logic unit that can be built with transistors and demonstration of one with a particular technology is regarded as a proof of concept for that particular technique. Figure 14 shows the GAA transistor based inverter build using SLO and

Figure 13 shows the inversion characteristics of the inverter. The inversion is stable up to 50 MHz and different number of P and N channels was used to match drain currents [17].

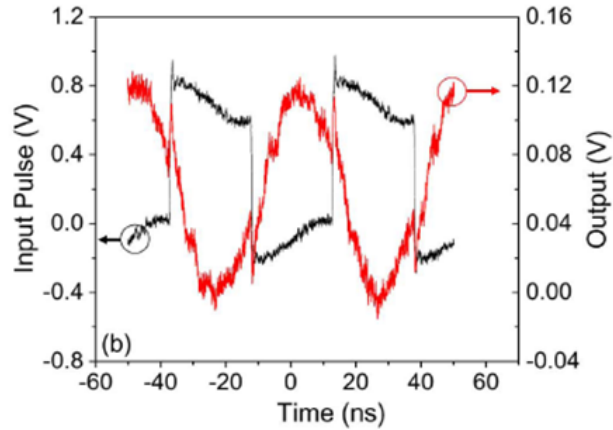


Figure 13: Inverter switching [17]

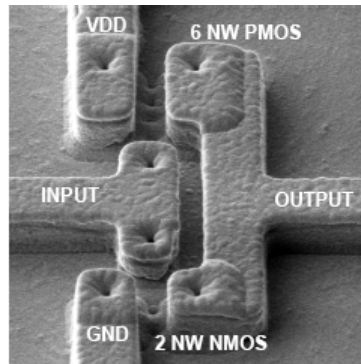


Figure 14: Inverter - SLO nanowire GAA transistors [17]

Successful fabrication of inverter makes SLO the leader among various methodologies to replace conventional CMOS in the years to come. At this stage it can be ascertained that Self-limiting-oxidation is technologically viable to construct GAA transistors with 1-Dimensional channel.

5 Unique Advantages of GAA transistors using SLO

In a nutshell, the advantages of GAA transistors fabricated using SLO are:

- CMOS compatible process
- Geometric versatility and spatial precision due to top-down patterning of Si fin

- Low DIBL
- Low Sub-threshold gradient
- Reduced Gate leakage
- High I_{on}/I_{off}

Apart from the above mentioned advantages, quantum confinement on two dimensions hold the potential for novel applications in the future.

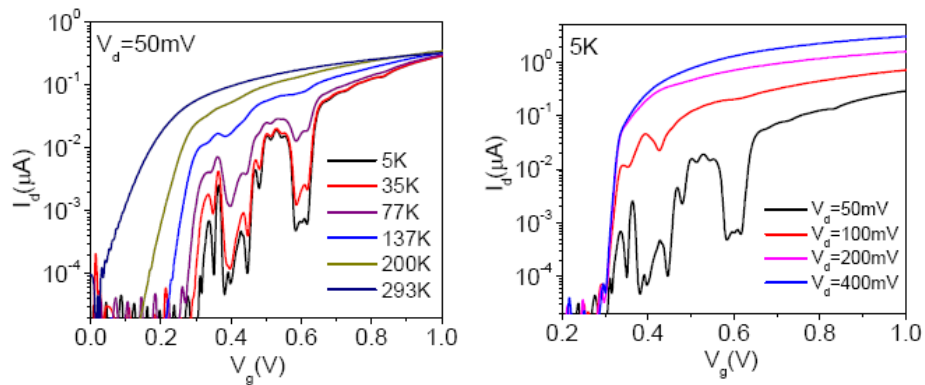


Figure 15: Low Temperature transistor characteristics [18]

Figure 15 shows the quantum oscillations found in GAA transistors at low temperature and low drain voltage.

6 Alternate Approaches

	Scalability	Performance	Energy Efficiency	Gain	Operational Reliability	Operational Temperature***	CMOS Technological Compatibility**	CMOS Architectural Compatibility*
1D Structures	2.4	2.2	2.5	2.3	2.0	2.5	1.8	2.3
3								
2								
1								
Channel Replacement Materials	2.0	2.9	2.3	2.4	1.9	2.3	1.8	2.5
3								
2								
1								
Single Electron Transistors	2.4	1.1	2.3	1.2	1.3	1.4	1.6	1.5
3								
2								
1								
Molecular Devices	2.5	1.5	2.2	1.5	1.3	1.8	1.6	1.7
3								
2								
1								
Ferromagnetic Devices	1.2	1.3	1.7	1.5	2.0	2.1	1.2	1.3
3								
2								
1								
Spin Transistors	1.7	1.4	2.3	1.7	1.4	1.3	1.3	1.3
3								
2								
1								

Figure 16: Evaluation of Alternate technologies [19]

Apart from GAA transistors there are many other possible transistors to better performance of information processing systems. The important ones are:

- Channel Material replacement
- Molecular Devices
- Single Electron Transistors
- Ferromagnetic Devices
- Spin transistors
- Other 1-D channel based transistors

Figure 16 shows an evaluation of these different approaches with respect to different factors (3: Very good, 2: As good as current technology and 1: Bad). It can be seen that on a relative scale 1D channel based transistors are much better than their alternates.

Among 1D channel approaches, GAA transistor using SLO based Si nanowire is the most ideally suited to current CMOS and hence high degree of compatibility. Carbon Nano-Tube (CNT) based transistors have been demonstrated (see Figure 17) and very high carrier mobility has been observed [20]. This would mean much faster devices and scaling might not be as important. Graphene Nano Ribbon (GNR) has also been used to demonstrate transistors [21] (see Figure 18) and very high carrier mobility is observed in GNR as well [22].

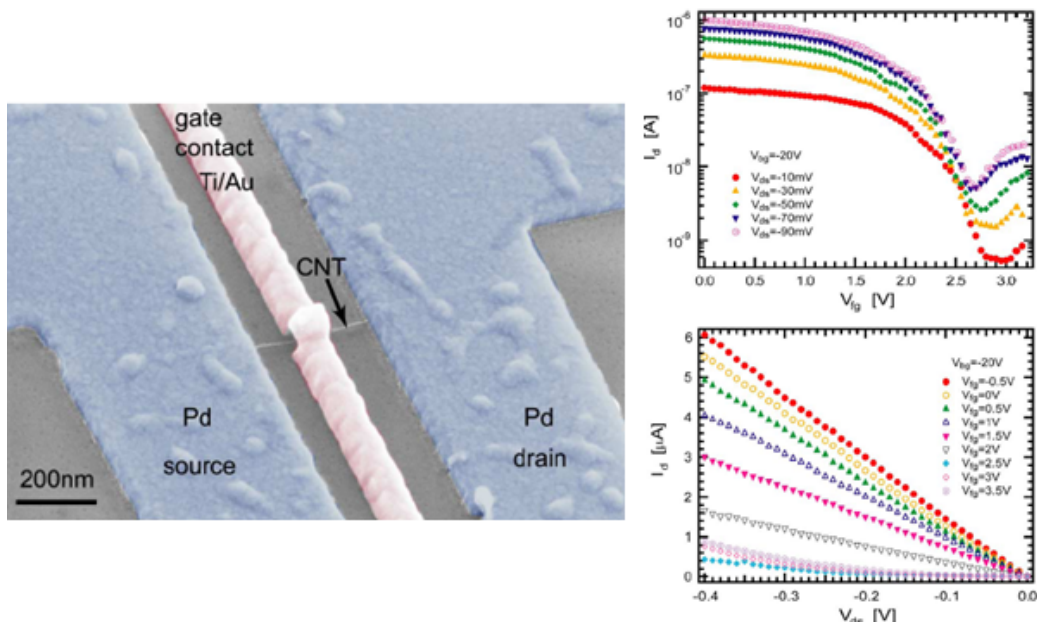


Figure 17: CNT GAA transistor and characteristics [20]

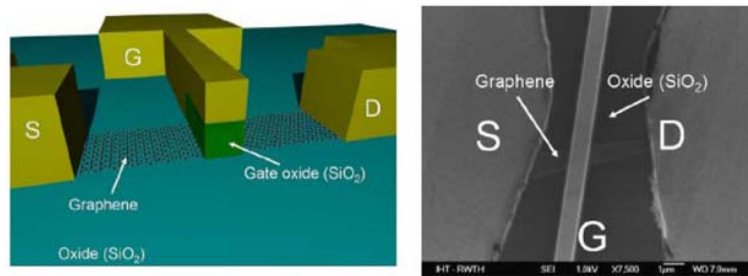


Figure 18: GNR top-back-gate transistor (Schematic and SEM image) [21]

In spite of the high carrier mobility, placement of CNT is done by dielectrophoresis [20] or templated Ni clusters. Both these approaches don't offer the sort of geometric versatility needed to make millions of transistors per die. Graphene is typically isolated by micromechanical cleaving [22], which is a time consuming and unreliable process. Though it feasible at research level, it is impossible to scale this processing technique to industry fabrication processes.

6.1 Improvements to be made

In light of the alternate technologies, the following improvements needed to be made to SLO based GAA transistors:

- Institute of Microelectronics, Singapore has demonstrated channel lengths down to 250 nm. There is a pressing need to demonstrate devices with smaller channel lengths to prove that channel length scaling doesn't degrade device functioning.
- Only 60-70% of the individual transistors build function reliably. The yield will further reduce when higher device density is needed. Device yield needs to be further studied.
- Channel mobility should be improved to better compete with CNT and GNR channel transistors.
- Drive current matching is currently achieved by using different number of P and N channels. This is not a scalable method and hence better methods should be employed to match drive currents.
- More functional and complex logic units need to be demonstrated using GAA transistors using SLO technique.

7 Estimated Timeline

Table 1 shows the predicted channel length in the years to come. Strained Si, newer gate dielectric material and SOI are supposed to propel till 13 nm (2013). From 14 nm (2012) onwards, newer device architecture will be introduced [4]. With this estimate, it can be concluded that the spot light will be on GAA transistors by the year 2012. This gives the researchers, four years to perfect the technology of growing nanowires using SLO and fabricating GAA transistors.

Year of Production	2009	2010	2011	2012	2013	2014	2015
Gate Length (nm)	20	18	16	14	13	11	10

Table 1: Gate length scaling

8 Feasibility

Figure 19 shows a summary of the areas where the technology lacks behind and where it performs better than other 1-D channel technologies. As mentioned earlier operational reliability at this point for this technology is significantly worse than what it should be. Performance wise CNT and GNR are much better, but GAA transistors perform on par with conventional CMOS devices. Compatibility with respect to CMOS processes is very good and this is an important differentiating factor. If this technology needs to be adopted by the industry CMOS compatibility is a very important factor.

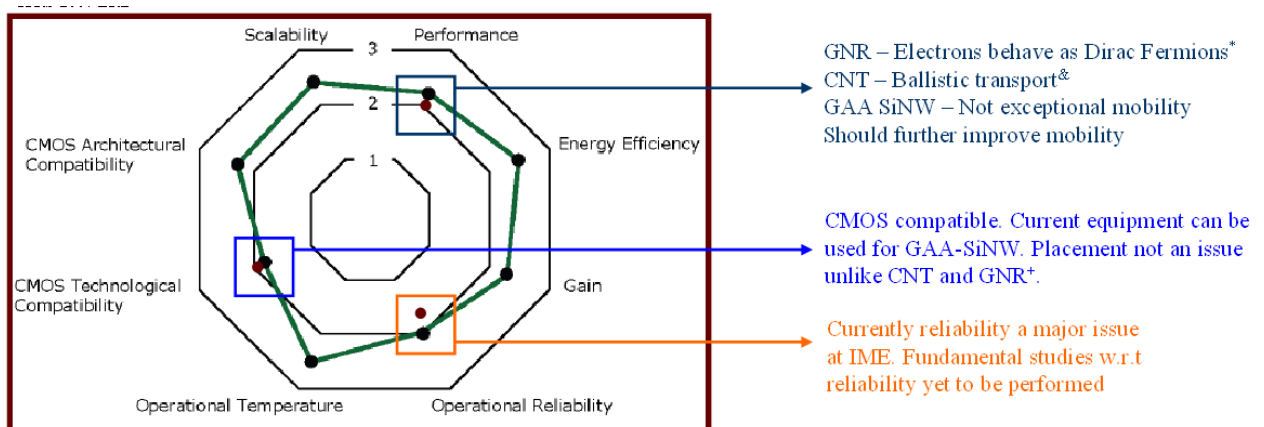


Figure 19: Key areas of concern

9 IP landscape

A total of 379 journals regarding 1-D channel transistors are there in Science Citation Index. This proves the gravity of the research and the need for it. VLS wire growth has been the choice of nanowire growth generally. But as we have seen so far, SLO nanowires are highly suited for the purpose of GAA transistors. GAA transistors according to simulations and experimental evidence perform really well and counter short channel effect effectively. Samsung Electronics and Institute of Microelectronics,

Singapore are the major research centers where GAA transistors are studied. It should be noted that Samsung is trying to build efficient twin/multi Si nanowire FETs. The processing method is significantly different from the one outlined in this report. Though SLO has been around since 1997, it is not too popular for applications other than GAA transistors.

9.1 Patents

Table 2 (grey cells -> Samsung) shows the most relevant patents with respect to nanowire GAA transistors. As mentioned earlier Samsung is a major player in the field of nano GAA transistors. After reviewing the claims of their patents, Samsung is fabricated multi nanowire FETs and they use Shallow trench isolation technique to fabricate the GAA channel. All of Samsung's patents clearly protect their fabrication technology and GAA transistors themselves haven't been patented. Enforcement of such a patent belongs to the grey area as GAA can be argued to be an idea or a concept which can't be patented.

ST-Microelectronics holds one patent for GAA transistors, but their fabrication methodology is purely dependant on lithography and doesn't encompass any novel method of fabricating the nano channel for GAA transistor. Thus, it can be inferred from the patent search that the technology for building transistor around Si nanowire grown using SLO hasn't been patented. SLO-GAA transistor based inverters been demonstrated is of significant importance and makes this technology readily patentable. To gain foothold in the IP landscape early patenting of this technology is of foremost importance and delaying this process might prove to be a fatal mistake.

Patent / Application Number	Title	Held by
US 7274051 B2	FET having wire channels and method of fabricating the same	Samsung Electronics

Application No. 11/259473	Multi Bridge Channel Field effect transistors with nano-wire channels and methods of manufacturing the same	Samsung Electronics
US 7253060 B2	GAA type of semiconductor device and method of fabricating the same	Samsung Electronics
US 6495403 B1	GAA semiconductor device and process for fabricating the same	ST Microelectronics

Table 2: Patent Summary

10 Value realization

Transistor is the most fundamental of all devices in any information processing systems. As explained earlier, scaling has brought the need and resources that are needed for any valuable technology. GAA transistor fabrication using SLO is a viable technology. There are two directions to realize the value of this research and technology. One being, setting up a company that manufactures GAA transistors and the other being licensing this technology to other established players in the industry. The issues with starting a company to solely manufacture GAA transistors are:

- Can't sell only transistors.
- Huge amount of technology needs to be licensed in order to manufacture microprocessors.
- Already established players of the industry essentially make these very transistors. Competing with them would be a great uphill task.
- Can't sell transistors also because wafers need to go through back-end processes right after the transistors are fabricated.

Given the issues with starting up a company, licensing the technology is the only other viable option. In order to do this, this technology needs to be patented and cover this whole spectrum of fabrication processes. To strengthen the patent portfolio, more complex logic units need to be demonstrated using GAA transistors and patented. As mentioned in the *Timeline* section, around 2012 when the industry is ripe enough for this technology licensing will fetch returns for this research effort.

11 Cost Evaluation

Figure 20 shows the rough estimation of the research cost that will be incurred to further mature this technology. For the purpose of cost evaluation, it has been assumed that all semiconductor manufacturing equipments required will be bought fresh. It should be noted that most of these equipments will be present in a research facility that can be rented. In the scenario that all the equipments are bought, they can be rented out, offsetting the cost by a considerable margin.

Optical Stepper (i-line)	\$4000000	Total Cost: S\$ 6.5 Million (US\$4.6 Million)
Deposition unit (Sputter)	\$300000	
Plasma etching	\$200000	
SEM	\$400000	
Wet Bench	\$30000	
Oxidation furnace	\$100000	
Clean Room (5000 sq. ft.)	\$200000	
Professor / Research Fellow (1)	\$120000/year	Fixed Cost → S\$ 5.23Million Bulk of the fixed cost will be experienced in setting up any semiconductor research institute
Research Students (4)	\$96000/year	
Wafer + Misc. Materials	\$50000/year	
Space rent	\$60000/year	
		Operation Cost → S\$ 326000/year 2008 – 2012 → S\$1.304 Million

Figure 20: Cost evaluation

With the simple cost model, US \$ 4.6 Million is the research funding needed for the period of four years (2012 when the industry will be ready for the technology).

12 Value Proposition

For a minimum ROI of 40% after 4 years, the licensing will have to fetch close to US\$ 6.5 Million. Figure 21 shows the increase in semiconductor revenue over the years and the estimated semiconductor revenue is projected to be around US \$ 1000 Billion which is a mammoth number. If GAA transistors made using SLO technique is technologically feasible and the industry needs it badly, US\$6.5 Million is an extremely modest estimate of what could be earned by licensing the technology. As mentioned throughout the report, industry will need alternate architectures in half decade from now and SLO technique is an excellent contender given it CMOS compatibly and the present state of the technology.

In conclusion, GAA transistor using semiconductor nanowire using SLO is an excellent research opportunity with the likelihood of making it big. This technology is not about riding the hype wave or based on unreasonable expectations. There is (or will be) a need for this technology in an industry that is going to be making close to a trillion dollars in revenue in a few years. Thus it makes technological and business sense to embark on this research opportunity.

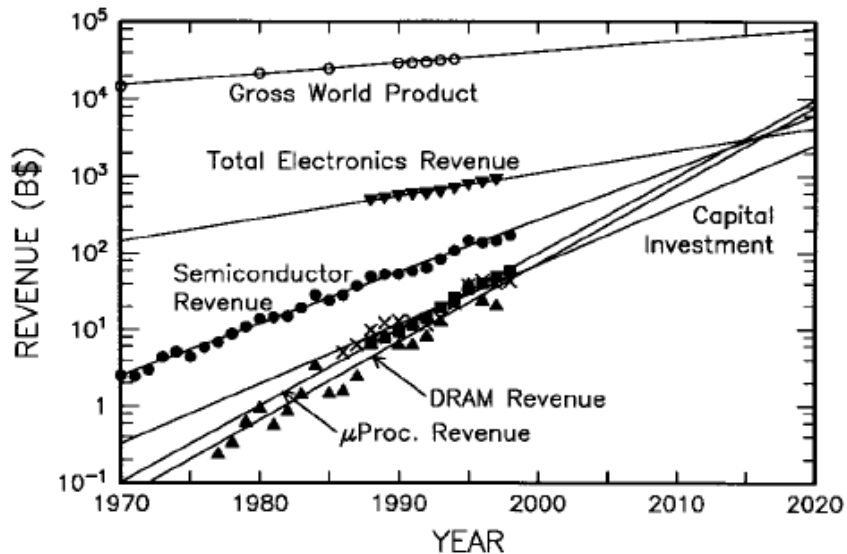


Figure 21: Electronics Industry Revenue [3]

13 Market Breakdown

In spite of the relatively rosy picture presented so far about the technology and the demand for it, it is very important to take a hard look at the importance of transistors and scaling across major semiconductor product segments.

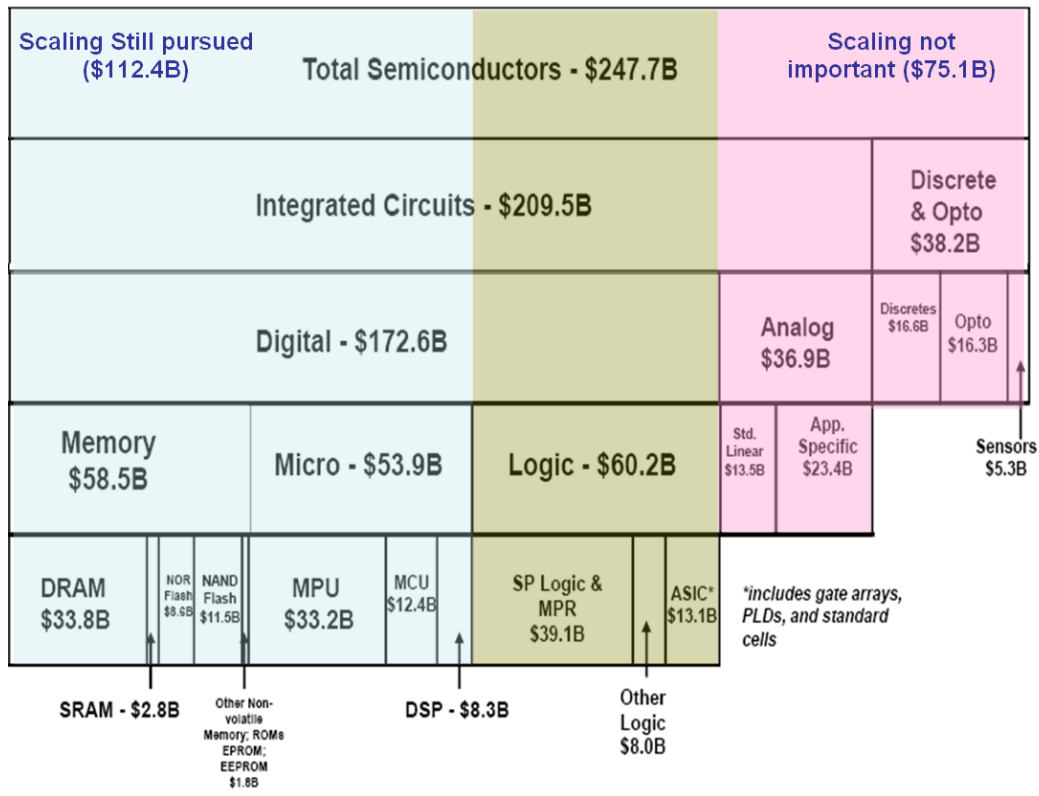


Figure 22: Worldwide Semiconductor Market Product breakdown (2006) [23]

Figure 22 shows the breakdown of the world semiconductor market. It should be noted that of the total market revenue of US \$ 247.7 Billion in 2006, ICs took a whopping US \$ 209.5 Billion. When it comes to memory and Microprocessors based information storage/processing systems, transistors are still very much important. This segment also happens to be taking the huge pie of the semiconductor market. Thus the role of this segment can't be overlooked. The right hand section of the market as shown in Figure 22 includes Discrete, Optoelectronics and analog devices based products. This part of the market doesn't view scaling as the ultimate quest of the semiconductor industry owing to the need for more functionality over speed/density. The segment in between that consists

of the rest of logic based devices views scaling with equal amount of interest and indifference. In the case of Application Specific ICs (ASIC) scaling is not too relevant, but Field Programmable gate arrays (FPGA) stand to gain a lot from scaling. Thus it can be concluded that majority of the semiconductor industry does feel the relevance of transistor dimension scaling. To further evaluate this claim Figure 23 shows the revenue of the various segments. It can be observed that though MOS devices have a huge share of the revenue, they have reached plateau exhibiting no further growth.

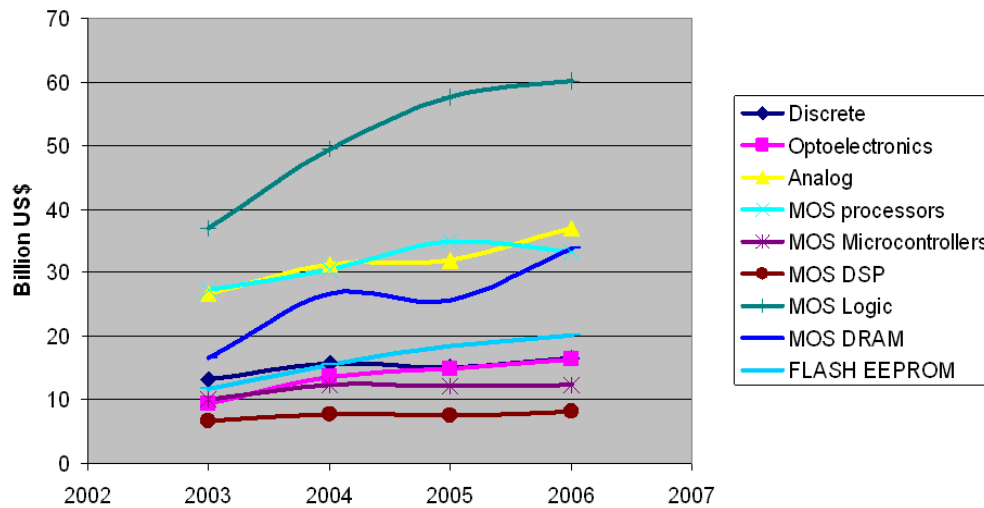


Figure 23: Semiconductor product revenue plot

This becomes more obvious when the percentage increase in revenue for each segment is considered as shown in Figure 24. This comparison provides valuable insights and shows that the revenue increase is on a steady decline for segments where scaling is relevant. Analog devices, discrete and optoelectronics have been growing at a steady rate. This provides a unique opportunity even though the market share is not too high, as more capital is available for commercialization of new technologies with novel functionalities. On the other hand for MOS devices, the growth is not as pronounced causing skepticism when it comes to capital investment outside the corporations. In the case of SLO nanowires, this means looking at applications for the technology that is essential out of the domain of MOS devices and looking at the faster growing piece of the market pie. Alternate uses for SLO nanowires will be discussed in the later sections, but the

important observation from this market evaluation is that bigger market segment doesn't necessarily guarantee value for innovation, whereas smaller segments with high Year-on-Year growth are brighter segments. The revenue figures for each segment were obtained from World Semiconductor Trade Statistics (Reference [23]).

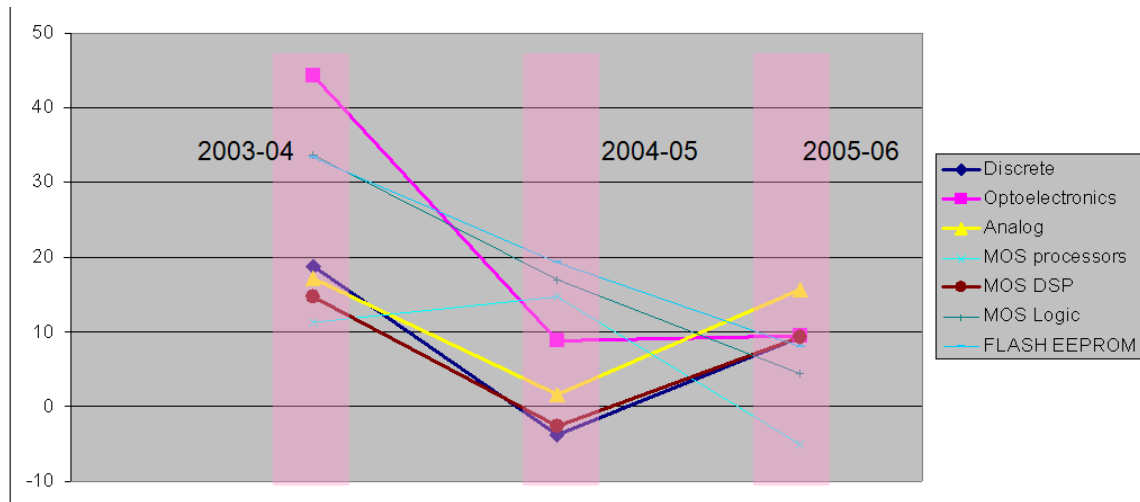


Figure 24: Percentage increase in revenue (Year-on-year)

13.1 End-Use Market Segmentation

Apart from industry segment breakdown, it is important to evaluate the end-use market segments. Observations made pertaining to end-use help in understanding the sort of functionalities end-consumers demand from manufacturers.

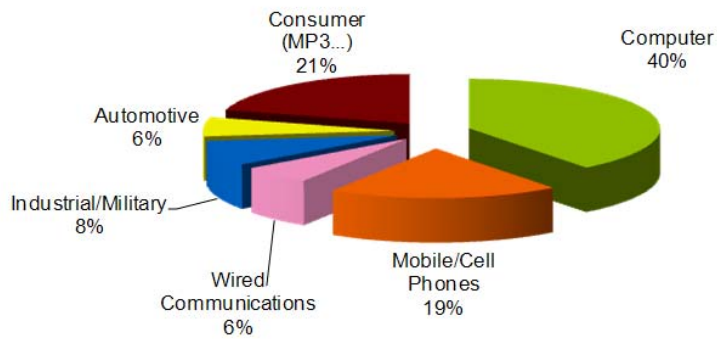


Figure 25: End-Use Market Breakdown

According to Semiconductor Industry Association (SIA) [24] computers is still the major stream of revenue for semiconductor products as seen in Figure 25. Computer segment is not much bigger when compared against mobile phone and consumer electronics products. With the introduction of MP3 players, digital cameras and smart phones these two sections have been steadily increasing. The share of computer is on a steady decline according to SIA. This is vital, as one can make the conclusion that shrinking computer market implies the rate of increase of demand for power and data hungry systems is going to be sluggish. Even though mobile devices need more solid state memory and faster power efficient processors, novel functionalities are the ones providing corporations with an edge with respect to others. An ideal example is the introduction of the new IPHONE by Apple Inc. Though it packs a lot processing power and solid state memory, it has been a huge success due to its touch interface, motion detection unit (Accelerometers) and light detector. To have a strong end-user base, it becomes very important to pack more functionality that mere processing power. Thus the relevance of scaling and hence Moore’s law is severely challenged. This again points to the direction away from transistors for SLO nanowires potential applications.

14 Semiconductor Foundry Evaluation

Semiconductor foundries provide an array of information as to the relevance of each semiconductor technology node. Analyzing important foundry’s financial returns and

revenues is an effective way to feel the pulse of each technology node. In this section four major foundries will be analyzed and the major players in this field are comprehensively shown in Figure 26. Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) takes a huge chunk of the pie followed by UMC. Chartered Semiconductors and SMIC are significant players as well.

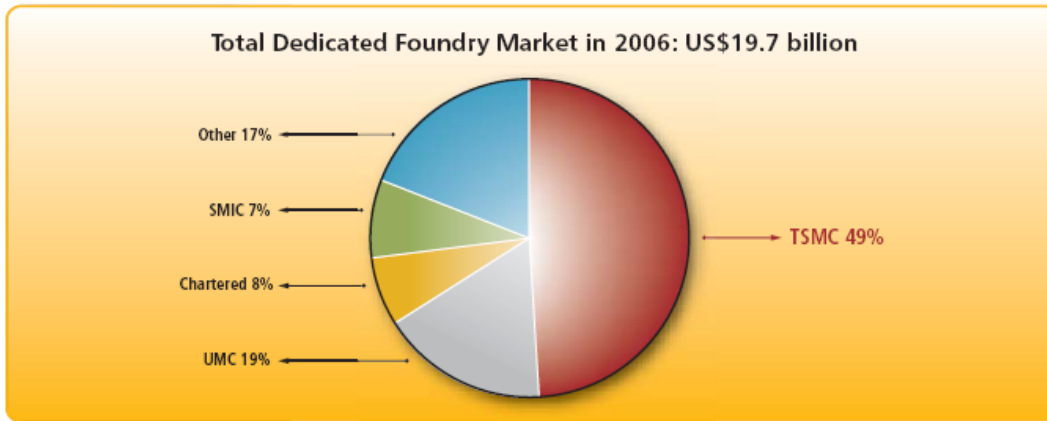


Figure 26: Semiconductor foundry revenue split [25]

Table 3 shows the revenue split of the four top semiconductor foundries. As we can see memory constitutes a small part of the earnings. This implies we are looking at information processing systems and not memory systems when looking at the earnings of these major foundries. This is desirable as information systems are far more diverse and it is difficult to look at it without noise from memory applications when it comes to effect of difference technology nodes.

	TSMC	UMC	Chartered	SMIC
Consumer	17%	21%	24%	26%
Communications	42%	56%	43%	54%
Computer	34%	21%	30%	13%
Industrial/Others	5%	1%	3%	7%
Memory	2%	1%	-	-

Table 3: Major Foundry revenue split up across segments

14.1 TSMC

The financial data of TSMC has been gathered from reference [25]. The evaluation of a technology node's relevance in each foundry begins with a look at the revenue earned by each node over the course of years of operation. Figure 27 shows the plot of node based revenue for TSMC and their gross margin percentage from 2002 to 2007. It is obvious that the gross margin percentage reflects the revenue from .15/.18 um technology. Though .15/.18 um is a relatively mature technology node, it is still the biggest revenue stream and affects gross margin percentage very closely. This goes a long way to show that in the case of TSMC .15/.18 um node is very relevant. Technology node - .11/.13 um is earning lesser revenue due to the increase in .09 um node's revenue. Unlike .15/.18 um node, .11/.13 um node had to wane for newer technology nodes to grow in prominence. It should also be noted that really old nodes (>.5 um) still earn considerable revenues. This shows how every application doesn't need aggressive scaling.

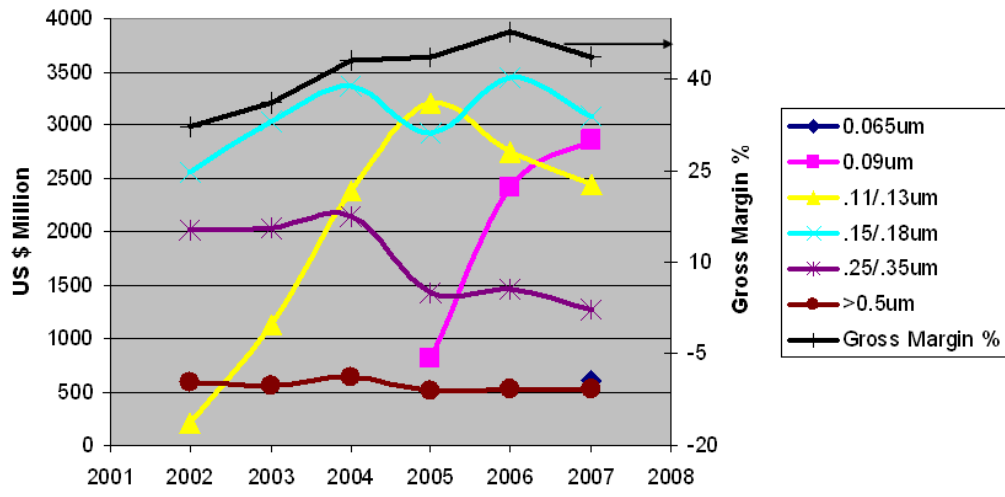


Figure 27: TSMC Revenue w.r.t Technology Node and Gross Margin %

Figure 28 shows the revenue share in percentage for different technology nodes. The observations made earlier hold good here as well. The decline in percent share of .11/.13 um node is very important as this means newer technology nodes have less than six years to pay back the investment made. This doesn't mean newer nodes are not growing. The most recent .065 um node has earned considerable revenue for TSMC over the past four quarters as shown in Figure 29. Increasing .065 um revenue would mean waning of .09 um node much faster than 0.13 um node. This goes to say that newer nodes have a shorter period to return the investments made for their development. This observation along with the prominence of mature nodes could mean that the beginning of the end for Moore's is here.

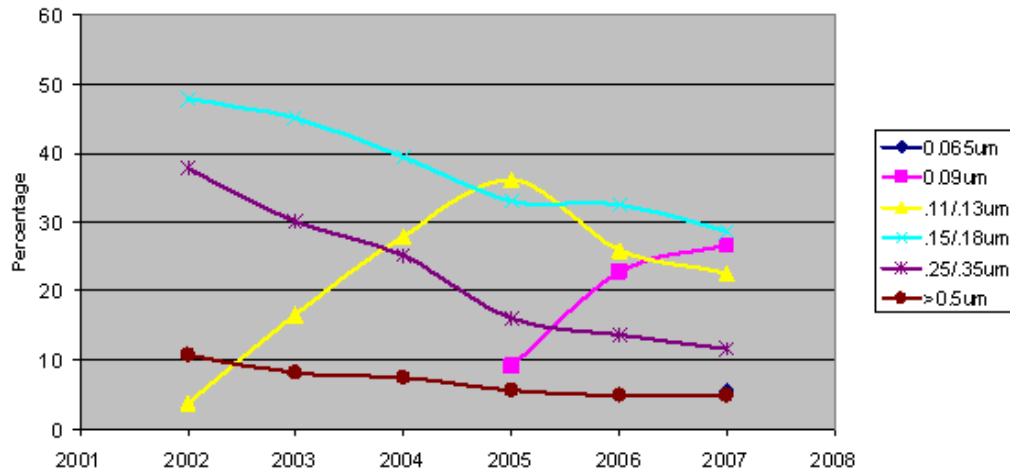


Figure 28: TSMC Technology Node - Revenue Share

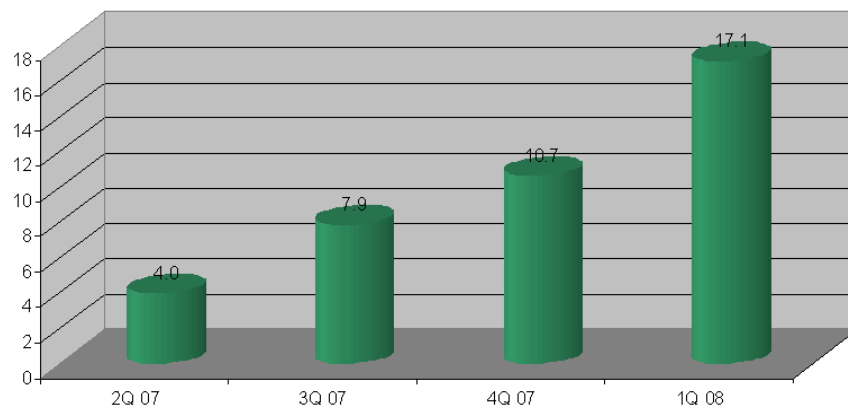


Figure 29: TSMC - 65 nm Sales (Billion NT\$)

14.2 UMC

The financial data of UMC has been gathered from reference [26]. UMC is the second biggest semiconductor foundry with meager revenue coming from memory manufacturing. The revenue split in Table 3 shows that UMC is very similar to TSMC in where its end product reaches. The similarity doesn't end there, Figure 30 shows that like in the case of TSMC, UMC also has great degree of correlation between gross margin percentage and the revenue from mature technology node (.15/.18 um). Though .13 um hasn't had a drop in revenues (except for 2005), the rate of growth has been very sluggish, giving way to .09 um. Figure 31 shows the revenue share on a percentage basis

and interesting point to note is that .09 um, .13 um and .35um all have the same contribution towards revenue in the year 2007. This provides additional fuel to the argument that scaling is not essential for everything within the information processing domain.

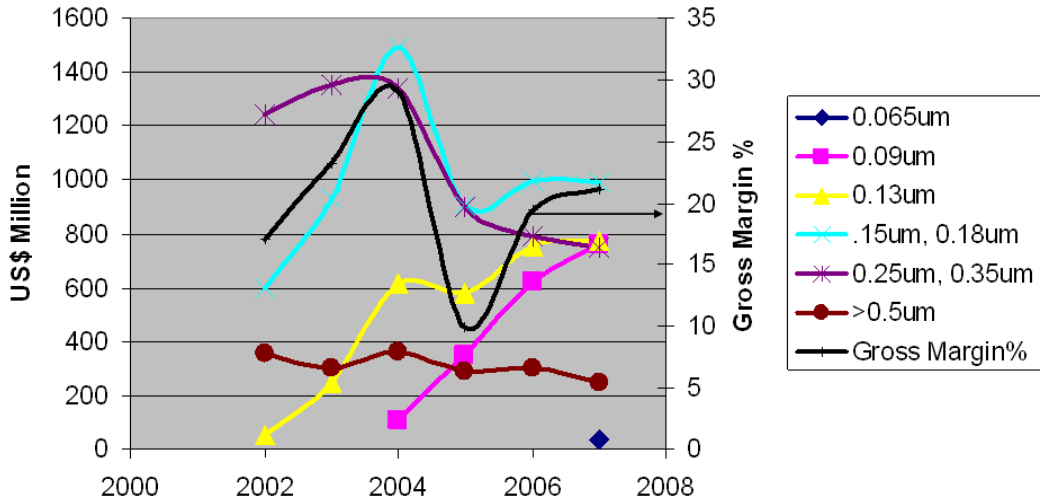


Figure 30: UMC Revenue w.r.t Technology Node and Gross Margin %

UMC -Technology Node - Revenue Share

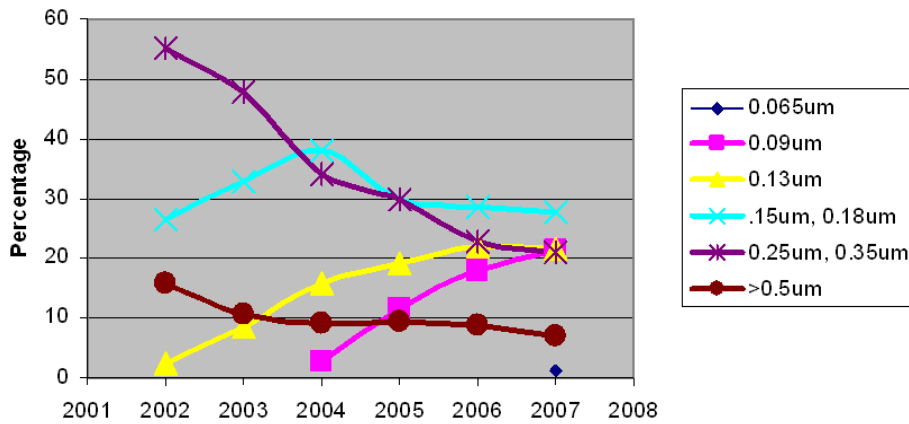


Figure 31: UMC - Technology Node - Revenue Share

14.3 Chartered Semiconductor

The financial data of Chartered has been gathered from reference [27]. The gross margin percentage of Chartered is no indicator as it has been negative for a good a part of half a decade as seen in Figure 32. In the case of Chartered, .13 um is the biggest earner. And the reduction in .09 um node's relevance can be clearly seen. Unlike TSMC and UMC, .18 is not the most prominent node, but its relevance has been steady over the past three years. Large revenues are still derived from relatively older nodes like .35 um and this indicates to the same conclusion as the previous cases. The period of relevance for the .09um is extremely small (three years) as illustrated in Figure 33. This is worrying as Chartered spent billions of dollars on its new FABS to manufacture .09 um technology node products [27]. Like in the case of TSMC the decline of .09 um node's relevance can be attributed to the steady inroads made by .065 um node as illustrated by Figure 34. The beginning to .065 um node's descent could be faster than .09 um node. But still the company is actively investing in newer nodes (down to 45 nm) [28]. Chartered also recently announced its roadmap to ramp down to 22 nm. Given the short longevity of each node, Chartered is forced to go further smaller dimensions due to the Self-fulfilling-prophecy character of Moore's law.

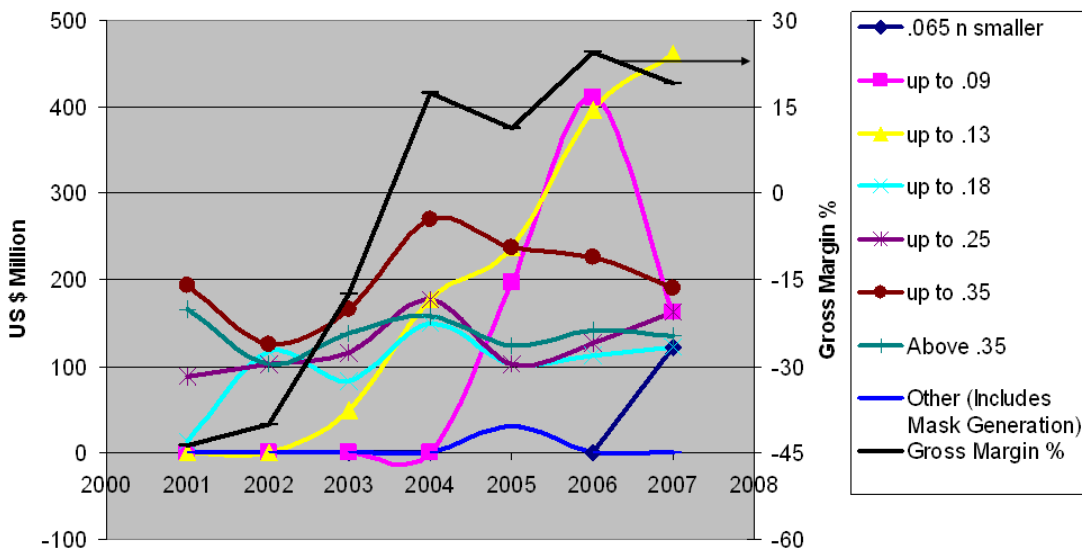


Figure 32: Chartered Revenue w.r.t Technology Node and Growth Margin %

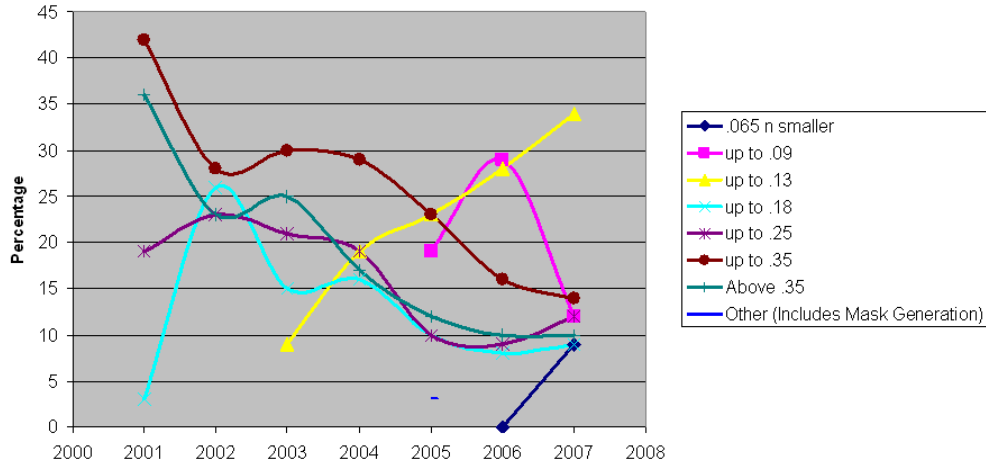


Figure 33: Chartered - Technology Node revenue share

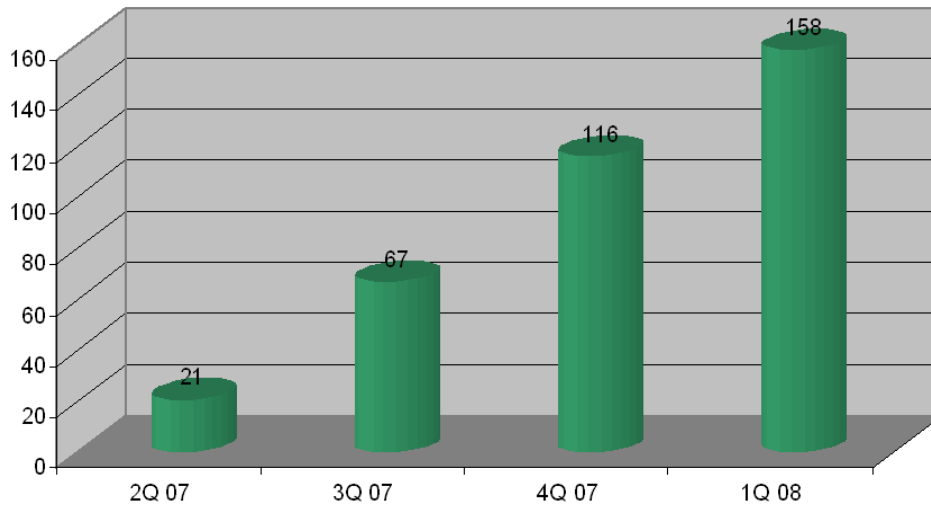


Figure 34: 65 nm revenue of Chartered (US \$ Millions)

14.4 SMIC

The financial data of Semiconductor Manufacturing International Corporation (SMIC) has been gathered from reference [29]. .18 um node is still very much relevant in SMIC as seen from Figure 35 and Figure 36. The descent of .13 um is very similar to TSMC and UMC as seen earlier. The gross margin percentage (without considering 2004's) seems to reflect more mature technology nodes like .15 um and .35 um. Like Chartered, .35 um is very much relevant. This could be attributed to the absence of memory products at Chartered and SMIC. This provides more credibility to the argument that memory

products push scaling faster than information processing units. This argument should be taken with a pinch of salt as TSMC and UMC have only a small percentage of revenue coming from memory products.

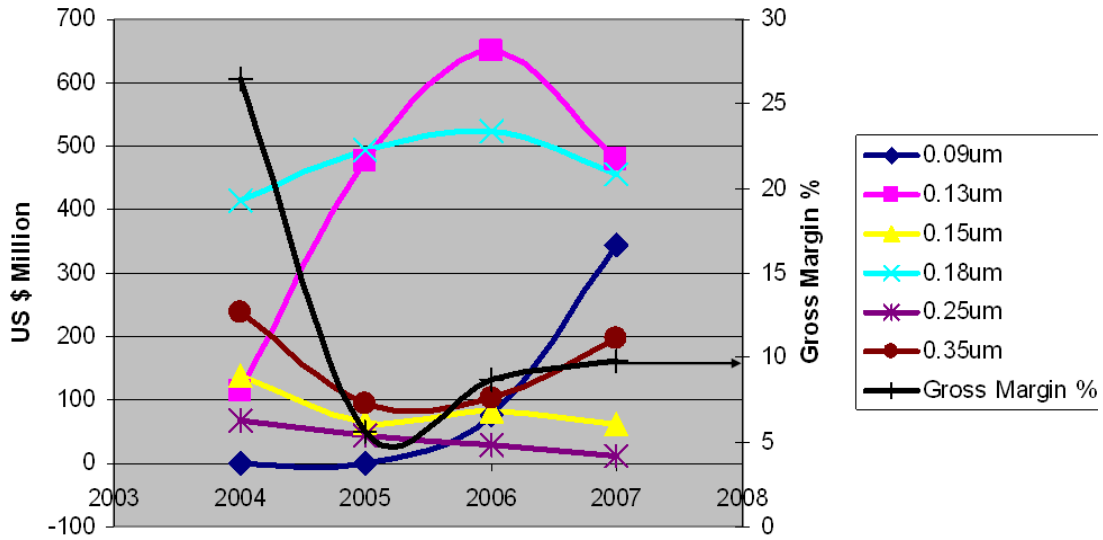


Figure 35: SMIC revenue w.r.t Technology Node and Gross Margin %

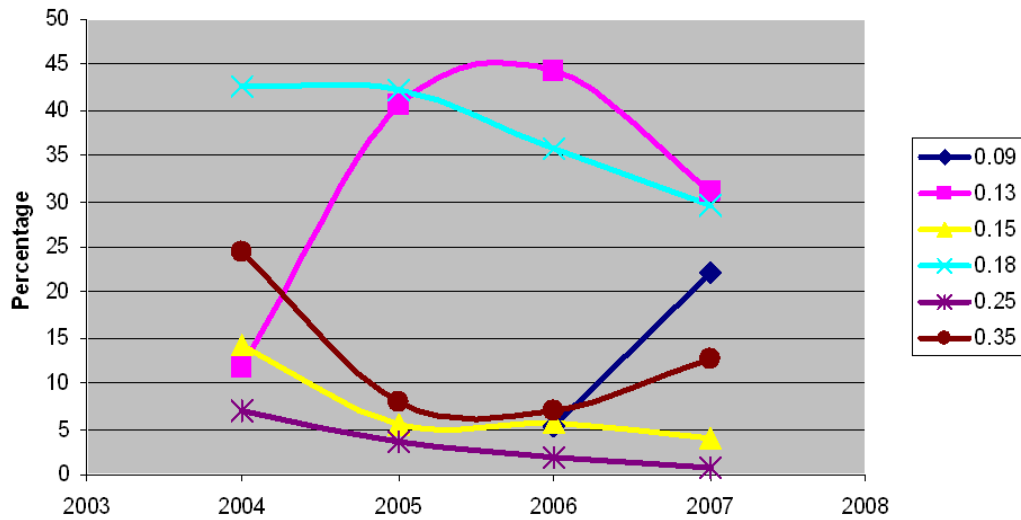


Figure 36: SMIC - Technology Node Percentage Revenue Share

14.5 Consolidated Analysis

To obtain a complete picture of the analysis performed for the top four foundries, the revenue from all four companies is plotted in Figure 37. On observation, it can be clearly seen that for the industry itself .15 / .18 um node is the biggest earner. Even more mature nodes like .35 um still gross close to US \$ 2.5 Billion. 0.13 um a relatively younger node has started to fade in relevance (not too obvious due to Chartered). On the other hand, .09um has been growing steadily from 2004, but the rate of growth reduced greatly in between 2006 and 2007.



Figure 37: Consolidate Revenue w.r.t important technology nodes

To conclude this section the following observations will be reiterated:

- Mature technology nodes are still very much relevant. Scaling doesn't have to be as aggressive as professed by the likes of Intel or ITRS.
- Gross margin percentage is linked to .15 / .18 um due to high capital investment for newer nodes.
- There is no preferred technology node for any year. If scaling is happening as ferociously, the peaks of revenue should be passed on to the next technology node.
- Relevance of Moore's law clearly is exaggerated and commercialization potential for SLO nanowires transistor is too optimistic.

15 Industry Outlook

Figure 38 shows the gross margin percentage from 2004 to 2007 of various top semiconductor manufacturers along with the top foundries. It is obvious that the companies that invest heavily in scaling like SMIC, UMC, Chartered and Micron have the least gross margins in the industry. Intel and AMD perform very well on this scale, even though they invest heavily on scaling. This could be attributed to their near monopoly in the microprocessor sector and thus can be considered an exception rather than an example. TI has been steadily increasing its margins by outsourcing digital manufacturing and developing analog manufacturing capabilities. This goes to show the amount of investment needed to keep scaling going. If this trend continues, foundries and memory manufacturers will have to eventually stop proceeding to the next technology node. It should be noted that TSMC has unusually large margins, which is suspected to be due to its high market share in the foundry segment.

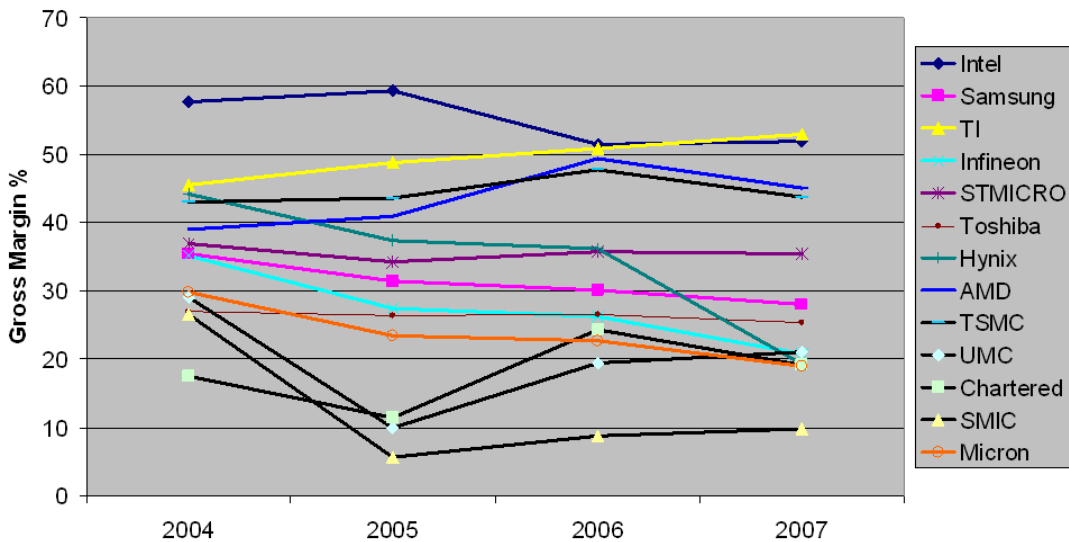


Figure 38: Gross Margin % - Semiconductor Manufacturers

16 Profitability Vs Investment

G. D Hutcheson and J. D Hutcheson at VLSI Research Inc. performed an in-depth study of Intel's profitability and investment [30]. The study tracked Intel from 1971 to 1996.

Figure 39 shows the investment Vs profitability over the years for Intel. The standard model of Return on Investment (ROI) can't be used for the semiconductor industry due to the steep capital expenditure on a regular basis. Thus in this work the ratio of new cash generated to equipment and R&D investment was used to quantify profitability. Ratio of plant and equipment investment to R&D expenditure was used to quantify investment. As years passed by the loops of profitability vs investment got lower. This means the investments weren't generated as much cash when compared against older technology nodes. This is a major indication as to why Moore's law might hit an economic barrier way before hitting a technological one. In the context of nanowires transistors, there might not be a need to solve the problems due to scaling because an economic barrier might be hit well before that.

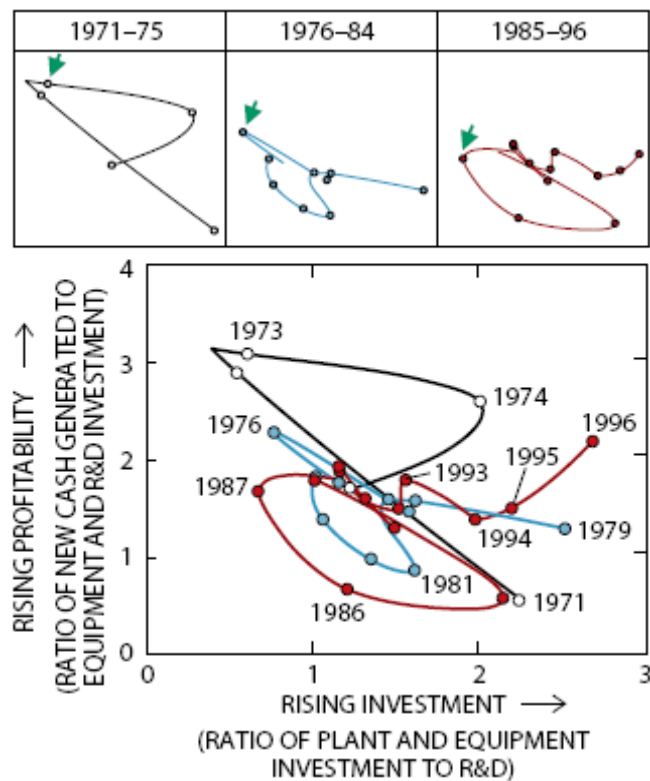


Figure 39: Intel's Profitability Vs Investment [30]

17 SLO Si nanowire sensors

As seen in the market breakdown section and in Figure 24 discrete devices which include sensors are growing at a steady rate. This translates to easier availability of capital to create newer functionalities. Chemical sensors depend on high surface area to volume ratio so that specific chemical when adsorbed on the surface will cause significant and measurable difference in the sensor material's electrical/electronic properties. This is schematically illustrated in Figure 40. Silicon nanowires based biological and chemical sensors have been shown to work very well [31]. A recent work at Institute of Microelectronics focuses on using SLO to make nanowire arrays for the purpose of chemical and temperature sensors [32]. The unique advantage offered by using SLO to make nanowires for sensory applications is that of monolithic integration. Horizontal wires are better suited to make sensors an integral part of a lab on chip system with electronic circuitry. SLO methodology being a CMOS compatible system makes this route more lucrative.

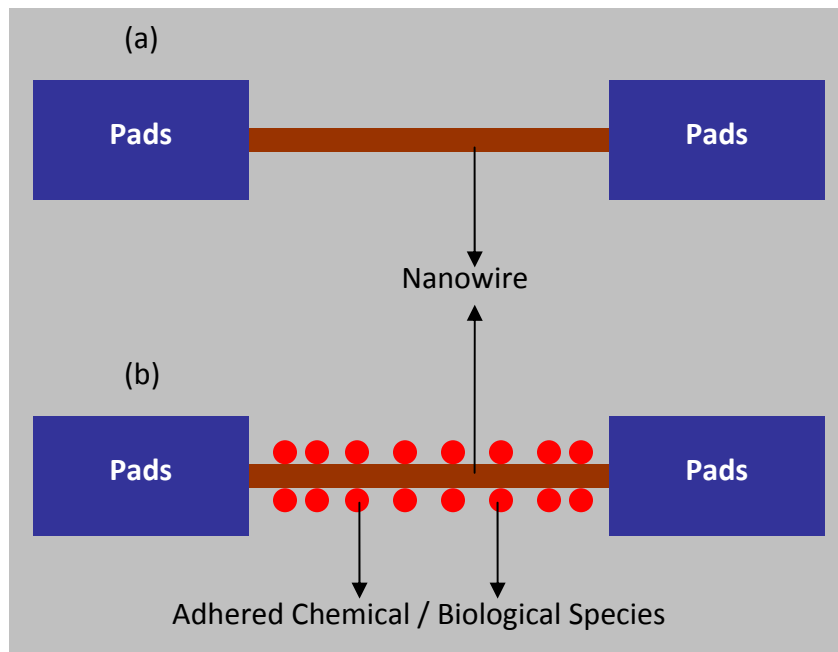


Figure 40: (a) SiNW with pads (b) Adhered species on SiNW causing conductivity to change

Figure 40 shows the electron microscopy of the nanowire array fabricated using SLO. It clearly shows the uniform nature, superior spatial control and reliability of the process which makes it ideal to be implemented in a lab-on-chip system. This would be better functionality without any reliability / yield trade off.

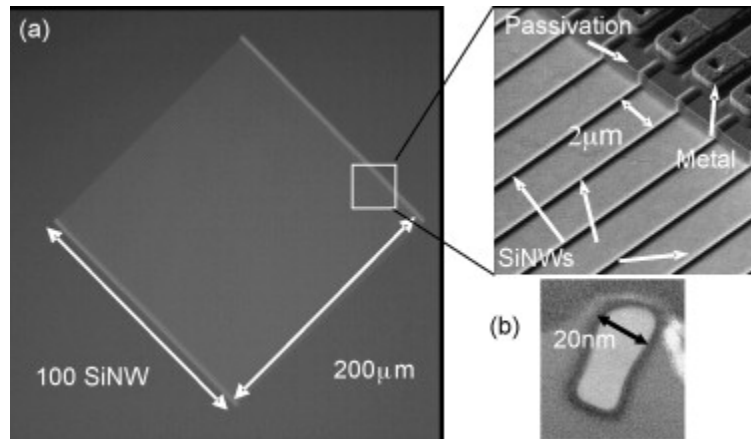


Figure 41: (a) Optical image of 200 μm long nanowire array showing 100 wires; zoom-in SEM image shows nanowires spaced at 2 μm with metal lines and passivation layer. (b) TEM image of nanowire showing rectangular cross-section [32]

Figure 42 shows the Temperature–conductance ($\sigma(T)$) plot for the resistor type polysilicon nanowires plotted with a standard deviation over 10 wires. Data shows good linear fit making it ideal to be used as temperature sensors. Added to chemical sensory ability as explained in [32] makes SLO a preferred method to make sensors of different kinds on the same substrate (same level) to pack a lot of functionality in one chip. When produced in large number economy of scales would imply that the chip would be very cheap. As the coating the wire with gate dielectric and electrode in the case of GAA transistors makes the process flow inherent low yield, avoidance of it would greatly improve the yield and drive cost of production lower.

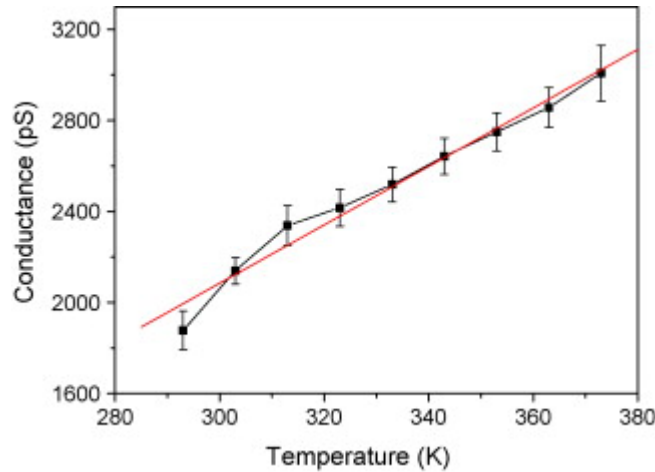


Figure 42: Temperature-conductance ($\sigma(T)$) plot for the resistor type poly-silicon nanowires [32]

Thus, SLO is better suited to be used in the fabrication of SiNW for sensors than transistors. In this case, the product can be commercialized in many forms and there is not need to wait for an opportune moment as in the case of GAA transistors as illustrated in Table 1. Further technological feasibility evaluation needs to be done in the case of SLO nanowires for sensors as the proof-of-concept for this methodology has only been recently reported (July-August 2008). Nonetheless SLO bases SiNW seem to be ideally suited to the demands of the sensor market and seems technologically feasible at a cursory level.

18 Conclusion

Self Limiting Oxidation is an excellent method to fabricate crystalline Silicon nanowires. The unique advantages include superior spatial precision, geometric flexibility, CMOS compatibility and the ability to fabricate horizontal nanowires. Gate All Around transistors abate most of the problems raised due to scaling below 22 nm. SLO based Si nanowire GAA transistors have been shown to work reliably and even basic logic units like inverters have been built using these transistors. They indicate superior performance and good CMOS compatibility. The research funding needed to continue this endeavor is not too expensive and the IP landscape is relatively sparsely populated. Other than Institute of Microelectronics, Samsung Electronics is the only organization looking at

GAA transistors seriously. But they use a completely different approach. Other competing 1D channel transistors have poor spatial precision and are hence unfit for information processing systems. In the case of realizing the value of the innovation, licensing of technology is preferred over starting up a company to commercialize SLO based GAA SiNW transistors.

GAA transistors solve almost all the problems posed by scaling. Thus it becomes very important to evaluate the relevance of scaling and Moore's law. After looking at the performance of various technology nodes in the industry, it is obvious that scaling is as aggressive as it used to be. Scaling could very well hit an economic obstacle much before facing a technological one. Given the low margins and high cost of technology node porting, most foundries are not likely to go aggressively behind scaling. This means SLO GAA transistors might never get a chance to get commercialized given the retardation of the scaling rate. This prompts the use of the methodology in other faster growing semiconductor segments that don't depend on transistors and hence scaling. The recent work at Institute of Microelectronics shows SLO nanowires perform efficiently as chemical, biological and temperature sensors. Given the advantages of monolithic integration and the rapid growth in discrete electronics segment, SLO might have brighter future as a methodology for fabricating nanowires for sensory applications.

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