Technological Assessment of Silicon on Lattice Engineered Substrate (SOLES) for Optical Applications

by

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Abstract

Over the past decade, much effort had been placed to integrate optoelectronic and electronic devices. Silicon on lattice engineered substrate (SOLES) had been developed for such purpose. As SOLES technology mature, a technological analysis is important so as to evaluate its potentials. In this report, a technological assessment will be done on the SOLES technology. This technology will be evaluated technologically and economically. The IP landscape in which SOLES would be applied is also looked into so as to ensure that there would be no infringement of intellectual properties. It has been concluded in this report that LED printer market would be a good introduction application for SOLES. A fabless company model is suggested as the start-up approach. A simple cost model had been done in this report. Cost of fabrication is expected to be reduced by 13% by changing current fabrication process to SOLES process. On the final note, if SOLES could capture a market share in the world market of 0.1% to 1% , the expected profit was projected to be about USD$1.32 M over the next five years, with an expected sales of about 210 thousand unit, averaging about USD$264K per annum.

Thesis Supervisor: Eugene A. Fitzgerald

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Contents

Introduction

Since the era of microelectronics, the ever on-going downscaling of electronic devices had continued just like what Moore's law had predicted. Roadmap had been painted on the unceasing miniaturization of integrated circuits. However, it now meets a bottleneck in the development of downscaling. According to the roadmap, there are many unachievable targets with current technology. [1] Hence, the quest for solution to continuously downscale had become more pressing than ever.

In the recent decades, circuit integration had become the trend of research. Much effort had been placed into research for new methods to put systems on chip[2]. This is one of the most promising methods to pack more functions in a single chip. Further, by integrating devices in the 3D manner, the need for interconnect is reduced. This leads to lower crosstalk and faster data transfer rate between different components[3].

Though the advantages of integration are great, there exist some challenges in bringing the idea into reality. Over the decades, people had been working to integrate circuits together. From packaging technique such as wire bonding to the monolithic integration, each technique involves its pros and cons. Some of these techniques will be looked into in the next chapter.

The main issue with packaging technique is that it incurred extra cost in the connection between devices. On the other hand, monolithic integration of devices has an issue of lattice mismatch between different materials. The lattice mismatch can be detrimental when devices are subsequently built on the lattice mismatched substrate.

Thus, silicon on lattice engineered substrate (SOLES) was developed. This technology solves the issue of lattice mismatch between different materials substrate and at the same time allows different types of devices to be built on the same substrate. Hence, the cost of packaging is also eliminated.

In this project, current technologies for devices integration and SOLES has been looked into. SOLES will be evaluated on how it can solve some of the problems faced by current technologies. An application point in which SOLES could enter the market is projected. IP landscape in the application area is also being studied. A simple cost model is built at the end of the report so as to project the estimated cost of switching from current fabrication method to SOLES fabrication process. The cost difference is analyzed and evaluated.

Literature Review

Silicon and its development

In electronics application, silicon is one of the most important semiconductors. The element was found by Antoine Lavoisier in 1787. Since then, it has received much attention from different industries. By the 19th century, silicon was successfully isolated and its development took off at great speed.

Silicon is the second most abundant element found in earth's crust, making up 25.7% of the crust by mass. Due to its availability, silicon is the principal component of most semiconductor devices till this day. In most integrated circuits, silicon is widely used. Most component devices are built on silicon surface.

Another reason for its popularity is its possibility. Pure silicon can be used to produce silicon wafers. By doping different levels of boron or porous, charge carries in silicon can be controlled. This allows silicon to become an important platform for many devices such as transistors, solar cells and semiconductor detectors. These component devices are the basic building blocks for many consumer electronic products. This is one of the main driving forces for the development of silicon fabrication plants around the world. The leading semiconductor firms include Intel and TSMC [4]. Billions of sales had been generated by each of these companies in 2006 and 2007 alone[4].

As technology developed, there is a pressing need for speed in electronic integrated circuits. According to Moore, the size of transistors is to decrease their sizes by half every 18 months[5], implying requirement for speed in each of these transistors. This has posed a great deal of challenges in integrated circuit design and manufacturing.

Different solutions had been proposed by different research group around the world to increase transistor speed. One such approach is by introducing strain within the silicon substrate[6]. By

introducing strain within the silicon substrate, mobility of charge carries can be increased, in turn increase the speed of transistors. Since then, different semiconducting devices had been built on strained substrates. Many renowned companies such as Intel had started using strained silicon for electronic devices processing.

In the recent decades, as optical photonics is also developed, silicon received even more attention. Due to its indirect bandgap[7, 8], light emittion is difficult within these material[9]. The presence of indirect bandgap had greatly reduced the probability for an excited electron- hole pair to recombine and emit a photon. Although, some efforts had been made to achieve light emission from Si, either by modifying the Si on nanoscale or by exploiting its nonlinear optical properties[9], these techniques were not as effective as III-V optoelectronic devices. This leads to the development of other semiconducting materials such as GaAs and other III-V materials.

III-V materials

Due to continued development and commercialization of optoelectronics devices such as light emitting diode and lasers III-V materials had received much research attention.

One of the key advantages in III-V materials is that most of these materials are of direct bandgap making light emittion to be achieved much more easily. These materials have the desired direct band-gap range for emission of photons and can provide electrical- carrier and optical spatial-mode confinement[10]. Another reason for choosing III-V materials is that most of these materials are of wider bandgap compared to silicon making them a better candidate for high-power and high temperature devices[11].

The key III-V materials include GaAs, GaP, GaN, GaN, GaAlAs, InP and InSb[12]. These materials exist superior noise characteristics and high efficiency, thus, are also used in many electronic applications such as tunable photodetectors[13]. Such unique properties of III-V materials make them very important materials in the fabrication of opelectronics materials.

GaAs, being the most commonly used of the III-V materials is now frequently used as the starting platform in most opelectronic devices. GaAs exhibits bulk negative resistance at high fields and a high electron mobility[10]. Negative resistance is important in the fabrication of Gunn diodes as it is useful for forming short triggered electrical pulses and the for the generation of microwave oscillations[10]. Also, the high electron mobility of GaAs is useful in MESFET application.

Since electronic and optoelectronic devices are build on different substrates, it is important to integrate these devices so as to be used to produced into useful consumer products.

Methods to integrate III-V into Silicon circuitry

When GaAs is grown on Si substrate, antiphase domains are generated[14]. These antiphase domains happened due to the polar on nonpolar nature of GaAs on Si substrate. Antiphase domains are formed when the GaAs and Si structure doest not remain the same in the entire crystal. At the boundaries across these domains, the like atoms are connected thus resulting in a higher energy than usual. This in turn affects the performance of the III-V devices. Thus, methods have to be invented to effectively integrate III-V devices and the silicon devices.

Many different methods had been used to introduce III-V into silicon circuitry. Different methods include wire-bond packaging, flip-chip packaging, die- to-wafer bonding, epitaxial liftoff (ELO), assembly and also monolithic integration. Most of these methods involved the fabrication of the III-V device, transfer of the device to Si circuitry, bonding of the device to the circuitry, and removal of the III-V substrate[1].

In most techniques, the hybrid method is used whereby the III-V devices are first fabricated before transferring onto the Silicon substrate and packaging them together[1]. This often leads to expensive manufacture cost such as interconnects and large number of mask levels in building the devices.

Wire bonding

Wire bonding is one of the most common techniques in connecting III-V devices to silicon. This technique was first introduced in the 1950s by Bell Laboratories. Gold or aluminum was used to provide electrical connection from the chip to the device leads. The diameter of these bonding wire are usually of micron scale[15]. At the end of the wire, the wires are bonded to the by either wedge bond or ball bond.

The ball- bonding technique requires the gold wire tip to be melted with a small electrical spark. At the connection pad, the wire is pulled back and broken closed to the bonding area. Following which, the capillary is lifted and a few microns of wire is fed in, forming the ball bond, consequently the next ball- bonding cycle begins.

In the wedge bonding, the wire is pressed into the semiconductor pad horizontally and attaches in that position. The wedge tip is then lifted up and moved to the connection pad position, where identically, the wire is attached horizontally. The wire is then pulled and broken, and the next bonding cycle begins.

Today, close to 90% of wire bonding are done by the ball- bonding technique. However, as devices continue to decrease in size, the wedge-bonding is expected to become more common, since wedge-bonding require a smaller bonding area[16].

It cost about 1 cent per wire-bonding. Thus, for a 400- pin chip, the chip would cost about $400 per wafer [16]. However, such interconnects usually cause a time lag and power loss during data transfer[17]. Thus, integration became the solution to fast data transfer and low power loss devices.

Flip-chip

Flip chip is another common technique used in connecting III-V chip and silicon chip.
In the flip chip technique, solder- bump are deposited over the area of the silicon wafer where it will be diced into individual die on which the III-V chip is attached. This method allows solder bumps to be placed over the entire area of the chip thus allowing the chip to have a comparative number of connections compared to the wire bonding. The cost of solder bonding is about $400 per 200 mm wafer [16].

Flip-chip integration is often referred to as slow and costly process, packing of individual dies are limited by the pitch of bumps. This makes integration density low[9].

Flip-chip solder- bump bonding and wire bonding are two most common method of connecting the III-V devices to the silicon[1]. These methods tend to incur high interconnect cost[15].

Monolithic integration

In order to eliminate the interconnect cost; some research groups had tried to grow III-V devices directly onto silicon substrate. By monolithically integrating the devices could potentially solve the problems of bottleneck in data transfer by providing optical chip to chip communication. This could also lower the cost of production for many chips[14].

As described in the previous section, the presence of antiphase domains could greatly affect the performance of the devices, monolithic process had to be considered very carefully[14]. In order to avoid antiphase domain, the starting silicon wafer had to be [100] substrate with a misorientation toward [011] by three degrees[18]. GaAs was directly deposited using MBE and the device could be fabricated directly on top of the deposited material. This method had been successful in 1μm gate length technology. However, as gate lengths continued to downscale; this

technique could no longer accommodate the technology requirement due to defect density within the material[19].

Thus, growing dislocation-free layer on top of silicon substrate became the next research interest. Since then, relaxed Ge had been successfully grown on silicon substrate using Ge_x-$Si_{(1-x)}$ buffer layer[20]. This technique has successfully allowed III-V device and silicon device to be fabricated on the same chip. However, such a technique introduced a height difference of about 10μm between the Ge and the Si relaxed layer. This difference in height posed fabrication challenges in integration of III-V and silicon devices chip[21].

Die-to-wafer bonding

Another technique that was used involved integrating III-V die onto Silicon substrate. The die-to- wafer bonding involves bonding unprocessed III-V material dies epitaxially to the processed SOI wafer. Such technique reduces III-V materials usage thus lowering the cost and time requirement of manufacture[9]. Following which, III-V devices are then fabricated using wafer-scale processing and lithographically aligned to the underlying SOI features. This technique also carries another advantage over other packaging methods. Since III-V devices are only fabricated after the transfer, the total number of mask level required for the overall device fabrication could be lowered.

This approach, however, did not allow thermal interface to be directly established as compared to the flip-chip method[9], thus, creating extra steps in manufacture. Also, in a die-to-wafer bonding processing, the III-V devices had to be fabricated with high precision as the die areas are small on the silicon wafer, this may result in alignment problem. Thus, throughput via die-to-wafer bonding is often lower than that of wafer-to-wafer bonding.

Wafer-to-wafer bonding

As an effort to resolve this alignment issue, wafer-to-wafer bonding had been developed. This technique is important in building system on chip. In 2002, Motorola and IQE agreed to invest a total of $24 million over the next five years in an effort to put gallium arsenide on silicon[22].

Their technique involves the use of high dielectric-constant oxide- interlayers, such as strontium titanate (STO). This oxide- interlayer act as a barrier and prevent reaction between silicon and the gallium arsenide layer. STO was first deposited onto silicon substrate to take stress out of the surface silicon layer and allows the growth of a low stress hetero epitaxial layer on the surface. Following that, a GaAs seed layer of about 2000Å is then deposited forming the pseudo substrate[22]. III-V device can then be build on this GaAs layer while silicon device can be fabricated on the bottom Si substrate. In order to prevent semi-insulating effect, conductivity of the STO layer can be controlled by doping aluminum[22].

Another method used in wafer-to-wafer bonding is by bonding silicon on GaAs wafers. This technique involves depositing a layer of silicon on top of GaAs which has a layer oxide grown on top of it. This wafers had show to be able to withstand temperature cycles to over 700°C[23]. Devices can be fabricated on these wafers through wafer process. However, GaAs wafers are usually of 100mm diameter. These wafers are usually small. Since Si devices are fabricated on these wafers, GaAs spaces are often wasted. This makes mass production of integrated circuits on these wafers non efficient.

Silicon on Lattice- engineered substrate (SOLES)

Since each of the described technologies has its draw back, there exists a driving force to develop even newer technologies to overcome the drawbacks. SOLES was one of such a development.

In involves the used of a Ge buffer layer grown on top of regular silicon wafer and also a wafer-to-wafer bonding technique which bonds another layer of silicon wafer on top of the grown Ge layer. Devices can then be built on the top silicon layer and the Ge layer.

Since the height difference between the top silicon layer and the Ge is relatively thin, the issue of huge height difference had been addressed. Also, as Ge buffer layer could be grown on 300mm wafer, much larger wafers can be process at any one time. This makes fabrication process much more efficient.

Furthermore, the top and bottom most layers of the SOLES are mad of silicon. It is expected that current fabrication infrastructure would be able to support the SOLES wafer. This implies that SOLES is able to enter the commercialized world with minimum change to fabrication infrastructures that are currently available.

Although SOLES is observed to be able to solve some of the issues of devices integration, it is yet to be commercialized. In this project, both the technical as well as commercial risks of SOLES will be explored and evaluated. A reasonable approach to commercialized SOLES will also be proposed.

Description of technology

SOLES is a wafer that consist of a relaxed layer of Ge built on silicon wafer, on top of which laid a layer of silicon oxide and a topmost layer of silicon[21].

The figure below shows a SOLES.

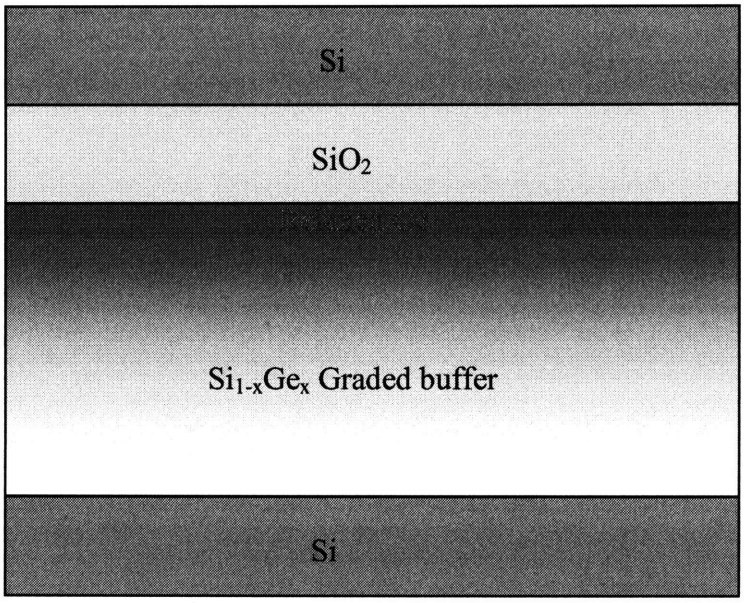

Fig 1: sturcture of SOLES

The graded Si(1-x) Gex buffers were grown from pure Si to a Ge-rich alloy ($0.96<x_{Ge}<1$) by UHVCVD[21]. This resulting Ge at the end of buffer layer was measured to be relaxed with dislocation density of $\sim 10^6$ cm^{-2}.

The SiGe buffered layer is first grown on top of a silicon substrate. However, a thin layer of silicon oxide is deposited on top of the pure Ge followed by a layer of pure silicon. The silicon-on insulator (SOI) structure on top of the Ge layer is built by layer transfer of Si layer.

After the SiGe is being grown on Silicon wafer, a SiO_2 layer of about 1μm is deposited on the Ge by low pressure chemical deposition. Following that, a donor Si wafer is prepared by growing a thin (~20nm) dry thermal SiO_2 layer, followed by H_2+ implantation of 5 x$10^{16}$$cm^{-2}$ with an energy of 80keV[21].

After the above preparation steps, both the donor wafer and the handle wafers are cleaned and bonded and annealed at 250C for 1 to 12 hour to strengthen the bond and then at 45C for 0.5-1h to drive hydrogen platelet nucleation and exfoliation of the donor wafer from the handle. This leave behind a layer of damaged Si surface, which will be removed using a chemical mechanical polishing process[21].

Figure 2 shows the process steps of how SOLES is fabricated.

The introduction of this technique had brought great promise to electronic and optical devices integration. According to Dohrman, this technology had had successfully integrated CMOS and III-V LED on the SOLES substrate[24].

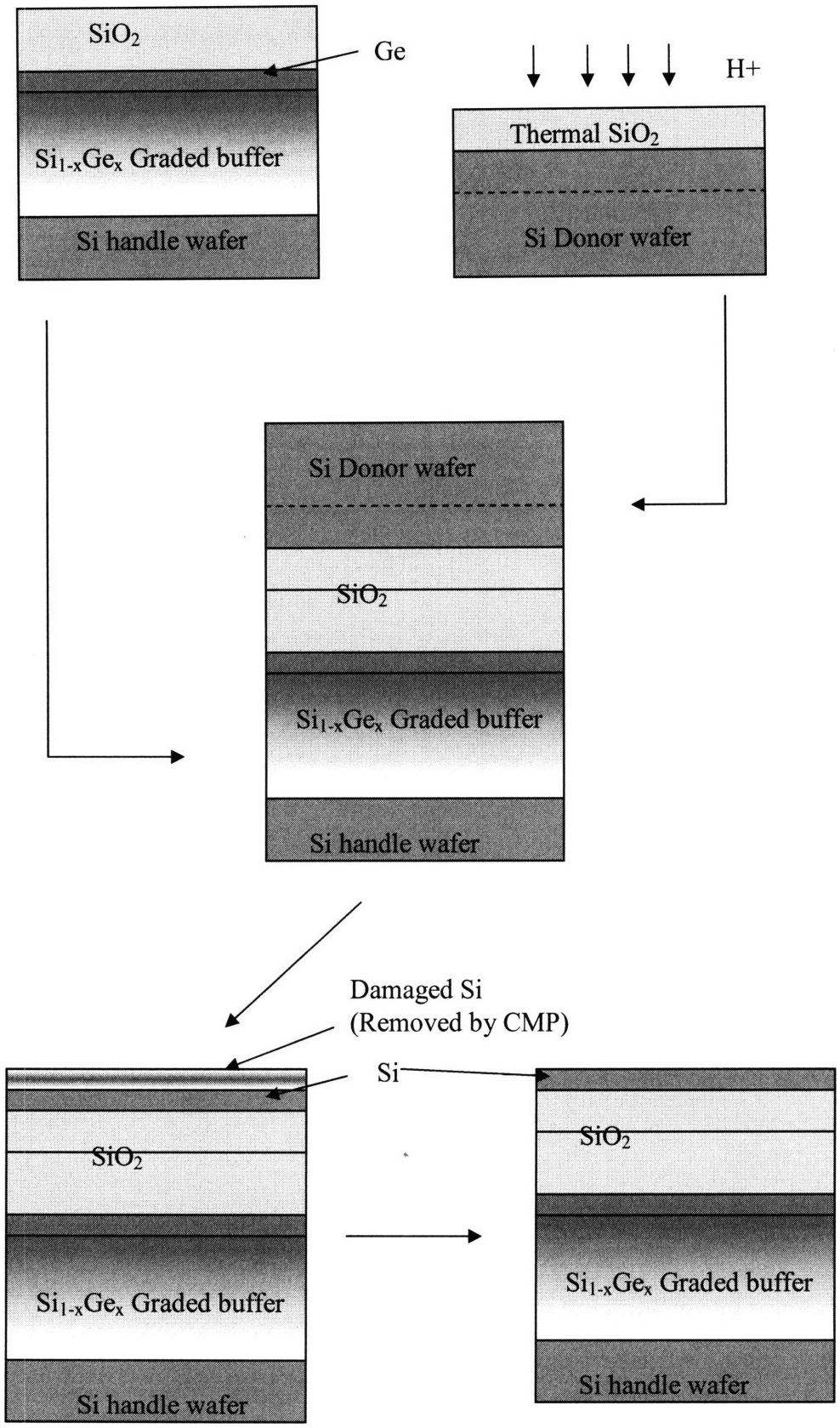

Fig 2: Process steps of SOLES fabrication

Potential Target markets

Since SOLES can be used for fabrication of any circuits that require optoelectronic device and electronic devices, the potential market of SOLES is enormous.

Even though application space is large, it is important to focus on a specific market space as an introduction point. Thus, the application landscape has to be evaluated.

One of the major markets of optoelectronic devices is in consumer products[25]. It has been estimated that most revenue comes from optoelectronic enabled products rather than optoelectronic components. Hence, it will be good if SOLES could find an application in the consumer product market[25].

The main form of optoelectronic devices are light-emitting diode (LED) and lasers. In LED, light is emitted by radiative recombination of electrons and holes in a material. The color of the LED would depend on the recombination wavelength. The mechanisms of laser is also base on stimulated emission process, however, in order to achieve lasers, the emission of energy has to come from a very specific wavelength. This suggested that the condition requirement of lasers is more stringent compared to condition requirement of achieving an LED light emission. GaAs is often deposited on Ge before fabrication of devices on SOLES. Since the cleaved angle between Si, Ge and GaAs are different, there exist a hindrance to achieve laser using SOLES at the present moment.

Thus, it will be technologically easier for the LED market to be reached first. The laser market can be reached at a later stage. Also, it has also been shown in the lab that arrays of LED could be built on SOLES connecting them to a CMOS circuitry[24].

At present, LEDs are used in many consumer products. Some examples are in the displays modules, image sensing and LED printers.

LED has been looked into as a backlight source in many display application. One example includes being the backlight source in LCD displays. This application of LED is expected to carry a potential growth of 50% over the next six years[26]. In many large screen LCD displays, light source is place at the back of the screen. These light sources are often as big as the screen. Many had tried to replace this light source with LED lightings. However, this would imply a large number of LED required. This may not be an efficient way to solve the issues. Some designers had come out with edge-light method to light up the LCD displays[26]. This method had demonstrated its ability in smaller screen displays. This is an advantage over current back light design as the edge-light design will require less LED resulting in lower power consumption and lower material cost. However, the edge-light design is unable to light up the large display set.

From this point of view, SOLES may be able to find its application point by going into the LCD backlight industry since one benefit of SOLES application includes closer packing of LED on the edge-light array.

Even though, this appeared to be a good introduction point of application, this market may not be a good commercialization point for SOLES. The reason is because this market involves fierce competition from other new technologies. One example is the organic LED (OLED), which tends to be much smaller and more flexible compared to conventional LED. The cost of production is also much lower. OLED has found its application in LCD display as the backlight. Thus, SOLES may need to face fierce competitors from the backlight design in this sector.

Another potential application of SOLES would be in sector of LED printers. This technology was introduced as an competitor to the laser printer market. The key advantages of LED printer over laser printer include less revolving parts in the printer, which implies lower hardware component cost [27]. The LED printer make use of an array of LED which produce a line by line scan compared to a point by point scan in an laser printer, this also implies higher print speed[27]. Currently, one drawback of the LED printer comparing to the laser printer is the print quality. Laser printers are able to produce quality of up to 1200dpi while LED printer could only produce about 600dpi[28].

Since SOLES is able to give a higher packing density, SOLES should be able to improve the current performance of the LED printing technology. Also, with SOLES, the packaging cost could also be reduced. Currently, most of the printer chips are manufactured using a 200mm silicon wafer as the substrate, since SOLES is able to be produced as a 300mm wafer, the production rate could also be increased and lowering the production cost at the same time. OKI had continued to improve LED printers performance by die-to-wafer bonding process. On the other hand, SOLES would be able to give a wafer-to-wafer integration in this case, thus giving a better enhancement.

Hence, the LED printer market would be a good commercialization point for SOLES to enter into the market.

Patent literature

Processing aspect

SOLES is built on two main prior art. This is generally, the smart-cut process and the growth of germanium on silicon wafer process. The following is a list of patents related to the processing of SOLES.

Looking at buffer layer growth of Ge on silicon substrate, MIT is rather well covered in this intellectual property. Following is a list of patents that has been filed on graded structure.

- 7,041,170 Method of producing high quality relaxed silicon germanium layers (2006)
- 6,927,147 Coplanar integration of lattice-mismatched semiconductor with silicon via wafer bonding virtual substrates (2005)
- 6,921,914 Process for producing semiconductor article using graded epitaxial growth (2003)
- 6,876,010 Controlling threading dislocation densities in Ge on Si using graded GeSi layers and planarization (2000)
- 6,864,115 Low threading dislocation density relaxed mismatched epilayers without high temperature growth (2003)
- 6,039, 803 Utilization of miscut substrates to improve relaxed graded silicon-germanium and germanium layers on silicon (2000)

All the listed patents belong to MIT except for patent number 7,041,170 and 6,864,115. This implies that MIT is rather well covered in the graded structure technology. It is noted that the two patents that does not belong to MIT belong to IP that are filed to improve the quality of Ge grown on silicon. It is possible to get around these IP by controlling the growth condition carefully. Thus, there does not exist much of an IP issue in the aspect of graded structure.

Another process that is important in the process of making SOLES is the smart- cut technique. Following is a list of patent filed in regards to this technique.

- 5,882,987 Smart cut process for the production of thin semiconductor materials films (1999)
- 6,326,285 Simultaneous multiple silicon on insulator (SOI) wafer production
- 6,191,007 Method for manufacturing a semiconductor substrate (2001)
- 6,251,754 Semiconductor substrate manufacturing method (2001)

The main patent that describe smart-cut is the first patent on the list. This patent belongs to International Business Machines Corporation. The claim describes bonding between a silicon surface and an oxide surface. In the case of SOLES, however, the "smart-cut" is carried out between two oxide surfaces. This gives SOLES some rooms of getting around the patent. Thus, the patent issue in this case is not major either.

Finally, since III-V devices has to be deposited on top of Ge layer most of the time. It is also important that we look into the IP landscape of deposition on III-V on Ge substrate.

- 5,308,444 Method of making semiconductor heterostructures of GaAs on Ge (1994)
- 4,835,116 Annealing method for III-V deposition(1989)

This list of patents above describes some techniques used to deposit III-V materials on Ge. Many claims had been filed in regards to put III-V materials on Ge. Although this list is non-exhaustive, there are a large number of alternatives to deposite III-V on Ge. Thus, it is believed that the deposition method of III-V on Ge will not cause any IP issue.

There also exist many patents on putting Ge onto silicon substrate. The following is a list of such IP.

- 6,537,370 Process for obtaining a layer of single- crystal germanium on a substrate of single crystal silicon, and products obtained (2003)
- 6,429,098 Process for obtaining a layer of single- crystal germanium or silicon on a substrate single- crystal silicon or germanium, respectively and multilayer products obtained (2002)
- 5,397,736 Liquid epitaxial process for producing three- dimensional semiconductor structures (1995)

- 5,326,716 Liquid phase epitaxial process for producing three- dimensional semiconductor structures by liquid phase epitaxial (1994)

None of the above patents relied on the graded structure. Thus, none of the above patents will cause an issue to our technology. However, it is important the for SOLES to claim enough area so that other inventors with other technology of growing Ge on silicon will not be able to modify their inventions to make it similar to SOLES and get around the patents that is currently claimed by MIT.

Technology aspect

Standing from the technology point of view, many IP had been filed base on the monolithic integration of optoelectronics and electronics devices. The following is a list of IP on this area.

- 4,847,665 Monolithic integration of optoelectronic and electronic devices (1989)
- US 5108947 Integration of GaAs on Si substrates (1992)
- US 2008/0035939 A1 Method of fabricating semiconductor devices on a group IV substrate (2007)
- US 2008/0029756 A1 Semiconductor buffer architecture for III-V devices on Si substrates (2008)

This list is non-exhaustive. However, none of these technologies are similar to the technology of SOLES, hence there exist not infringement issue for SOLES.

Application area- LED printing technology

Looking at current patents on LED printers, many patents had been filed on the idea of LED printing. The following is a list of patents that had been filed in the area of LED printer head by different companies.

Xerox:

- 4,587,717 LED printing array fabrication method (1985)
- 4,707,716 High resolution, high efficiency I.R. LED printing array fabrication method (1987)
- 5,510,633 Method of fabrication of porous silicon light emitting diode arrays (1996)

OKI:

- 4,916,464 Light emitting diode array print head having no bonding wire connections (1990)
- 5,067,809 Opto-semiconductor device and method of fabrication of the same (1991)
- 5,869,221 Method of fabricating an LED array (1999)
- 6,064,418 Led array, print head, and electrophotographic printer (2000)
- 6,211,537 LED array (2001)
- 6,388,696 Led array, and led printer head (2002)
- 6,515,309 LED array chip (2003)
- 6,165,824 Method of manufacturing a semiconductor device (2005)
- 7,061,113 Semiconductor apparatus, led head, and image forming apparatus (2006)

Xerox was the initial inventor of LED printing technology. They had filed in a few IP in the 1980s. From the list above, it could be observed that these IP are already over 20 years. This implies that the technology is no longer guarded by the patent. Thus, there should be no infringement when putting application into the LED printing technology.

OKI is the company that had been keeping LED printing technology alive until today. They had filed in a large number of patents on fabrication of LED printing technology. Most of this technology involved fabrication of LED and requires connection to the IC diver via wire bonding. Only 4,916,464 and 7,061,113 mentioned about connection without wire bonding. The first IP involves bonding with solder bump while the other involves a technology called "Epi-film bonding". The "Epi-film bonding" technique involved putting LED dies onto a silicon substrate. Again, these two technologies are different from that used in SOLES. Thus, no major issue in IP is observed.

Worldwide market

The printer market is of large potential. Base on analysis, it is estimated that the global market for printer is about 7.5 million globally[29], and it is growing at a rate of 12% annually. According to market research analysis in 2005, the color printer market is expected to growth at a annual compound rate of 30% [30]..

Printer is also one of the major exports in China. I has generated a large amount of revenue for the country[31]. The export sector had generated US$2606 million in the year 2002, US$4317 million in 2003 and US$6144.98 million in 2004. Thus, it can be concluded that the printer market industry is of great potential[31].

Major players

HP is currently the leader in the overall printer market. Base on analysis in 2007, it is taking a market share of 45% in the global market[29, 32]. This is their 20th consecutive quarters holding the first position in the market. In the laser printer market alone, they are currently holding 53% of the market share[29]. In the first quarter of 2008 it had already sold about 1 million units[29]. Over the years, HP had targeted its audience at small to medium businesses. The price range of their printers is about $100 to up to a few thousands. One of their product series includes HP Color LaserJet CP1215 printer series. This series of printer are priced about $250[32, 33]. This series of printers is able to do full color printing at 8ppm and black/white printing at 12ppm, giving a resolution of 600dpi by 600dpi. HP had explained that this series printers is among one of the cheapest to give color laser printing.

Another player in the market that is worth mentioning is the OKI. They are the leader in LED printing technology in today's market. Their sales is divided throughout the world with a distribution of 50% in EMEA, 24% in Americas, 17% in Asia and Oceania and 9% in the rest of

the world. Today they are the leader in A3 color printing in 10 countries in the EMEA, namely, Austria, Germany, Israel, Poland, Portugal, Slovakia, Slovenia, Spain, Switzerland, Ukraine[34]. It can be observed that their main target sector is business-used printers.

Their newest product is based on LED printing technology. Their unique technique of making LED printer head had been the spotlight in their annual report in 2007. They had make used of "Epi-film bonding" technique to fabricate LED print head. Figure 3 is a schematic of how their LED print head is made.

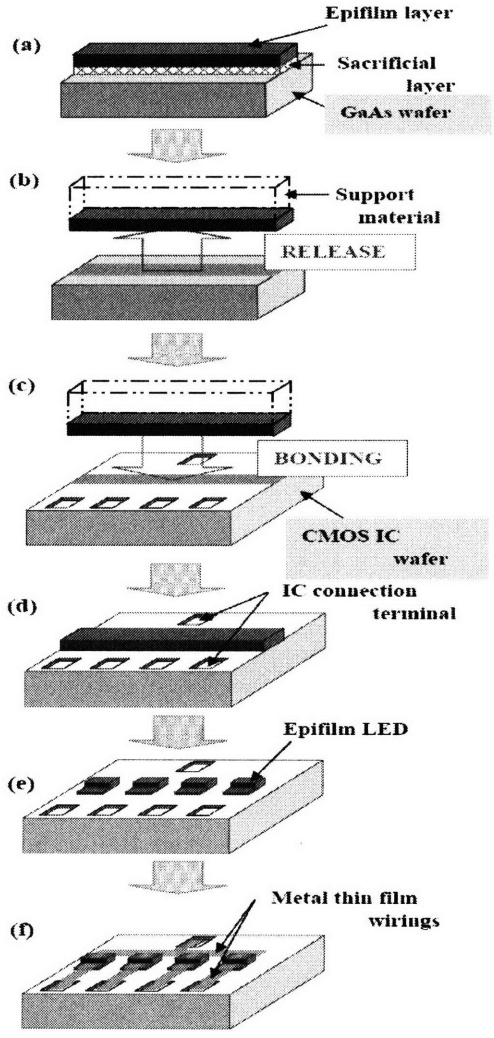

Fig 3: Schematic of LED print head fabrication[35]

This technique is a modification of die- to –wafer bonding technique. The C3400 series is build based on this technique. The printer is able to give full- color printing up to 16ppm and 20ppm for black/white printing. The resolution is 1200dpi x 600dpi and is priced about $300 [33].

Performance and cost analysis

In current commercialized market, laser printer typically prints at a resolution of 1200dpi. Such laser printer usually print using a laser diode array connected to silicon driver. The array of laser diode first sends out laser signal onto the optical system that is present in the printer. The signal is then focused and reflected by the optical lens and mirrors within the printer after which the laser signal finally hit the printer drum. This in turn allows toner to be picked up by the drum which eventually prints. The laser printer relies on a step and scan method in order to position the laser signal on to the drum. Figure 4 below shows a schematic of components within a laser printer.

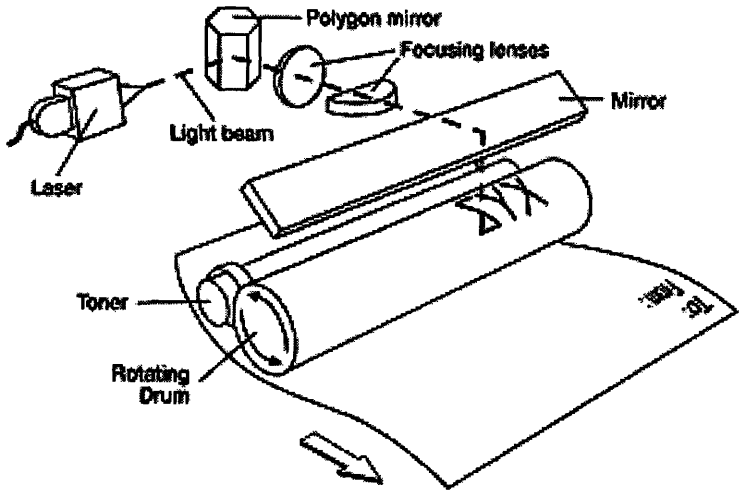

Figure 4: components within a laser printer [36]

The laser diode array and the silicon driver are usually connected to each other using wire bonding method. Figure 5 shows a laser diode array in a conventional printer. The laser diode array is connected to the external circuit via 32 pin wire bond. This implies that wire bonding is an essential cost origin in the fabrication of such printer chip.

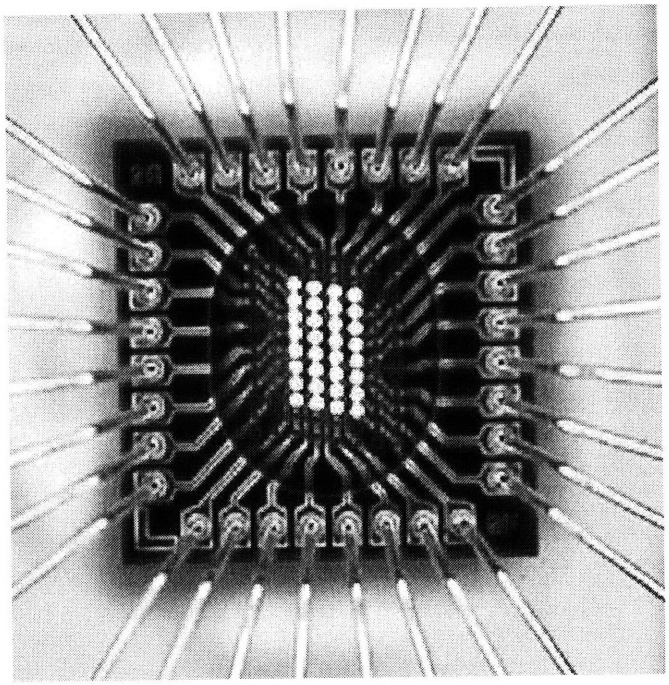

Fig 5: laser diode array with wire bonding[37]

On the other hand, current LED printer involves a large array of LED on the printer head. Signal is send out from individual LED on the printer head onto the printer drum. Toner is then directly collected and the printer prints. The LEDs are of fixed in position. This is the main reason for LED printers to be of a lower resolution compared to laser printer. However, the LED printer had eliminated the optical system in the printer, giving the LED printer a much higher print speed. Figure 6 below shows a schematic of how LED printer works. The LED printer head are fabricated using the die-to-wafer bonding technology.

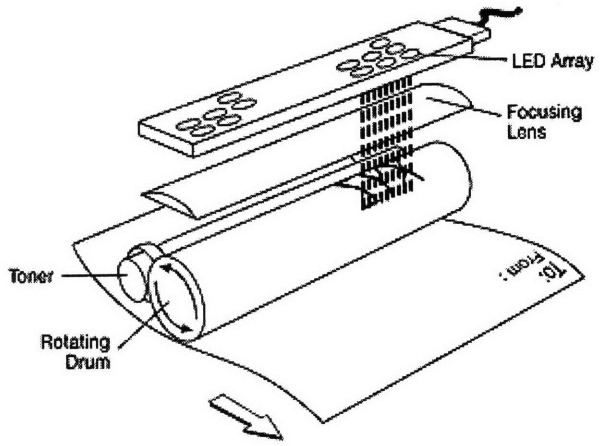

Fig 6: components within a LED printer [36]

Base on current technology, for a 6000 dpi printer head, there exist 192 LED, each of size 900μm, on each printer chip. The centre to centre spacing is measured to be 42.3μm between the LEDs. Thus, each chip is estimated to be 8.486mm^2[28]. Subsequently, 26 of such printer chips are connected to produce the whole printer head.

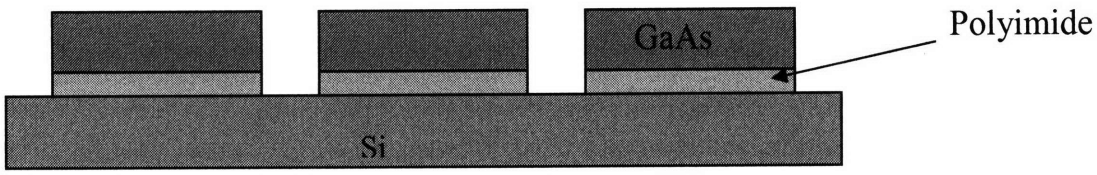

Fig 7: schematic of a conventional LED printer chip

Cost modeling

In order to properly analysis the cost for building a printer head, a cost model had been made for a laser printer chip, a conventional LED printer head and also LED printer head with SOLES.

Each of the building components in each device had to be considered. In most laser printer chip, there usually involves a laser diode array and the spatial light modulator array and a variety cylindrical micro-optics. Process steps of each of these components can be looked into.

One of the most simplified ways to estimate the cost of producing a chip would be to estimate the number of mask level required and the cost per mask level. The numbers of mask levels required are characterized by the device technology. Mask level is defined via a set of non- overlapping polygons. Each mask level incorporates a number of steps such as resist coating, exposure, development, alignment check and also several clean- up steps such as resist strip and megasonic cleaning[38]. In a conventional CMOS transistor formation, 30 to 40 mask levels are required. Several mask levels were required for formation of isolation, threshold adjust implants, gate dielectric and polysilicon gate material deposition. Following that one or a few more masking levels may be need to separately dope the NMOS and PMOS polysilicon regions. Then, another masking level is required to pattern and etch these polysilicon. After which, MDD/LDD PMOS and NMOS masking levels were implanted from each other. Subsequently, several masking levels are needed for the metallization and interconnect. [38]

In 2007, Intel is currently producing 45nm technology, it is estimated that about 31 wafer levels is required for such CMOS production. This process starts out with Epi wafer, consist of single gate oxide thickness, embedded silicon germanium and a tensile stress layer for strain engineering and about 8 layers of copper[39]. On the other hand, AMD is working on 45nm to 65nm technology. AMD starts with a SOI wafer, includes dual gate oxides, has embedded silicon germanium, dual stress liners and stress memorization for strain engineering and 10 layers of copper metallization for interconnect. The AMD process was estimated to be consisting of 42 mask levels [39].

In order to estimate the cost per mask level, different cost factors has to be taken into account. These include the cost of machine, footprint of the machines, labor cost, cost of making the mask and cost of consumables. Taking into account of these factors, the cost of each mask level can be estimated. The cost of producing a 300mm wafer in AMD is about $4320, while it cost about $2500 per wafer in Intel [39]. By averaging the cost, it cost about $103 per mask level for AMD and about $81 per mask lever for Intel.

Another cost contributing cost factor is the packaging and assembly of the chips. Wire bonding is one of the most common methods used to package chips together. Currently, it cost about 1 cent per wire bond and most chip contain about 300 pins[16]. On the other hand, flip chip can also be used, in connecting chips to other chips. Currently, it cost about $300 per 200-mm wafer [16].

Laser printer

In the making of a laser diodes, about 6 mask level is required[40]. Another silicon chip is required to control the signal going in to each of the laser diode. The laser diode chip is first mounted onto a LCC ceramic package, followed by wire bonding and encapsulation processes.

Both the cost of producing laser diode array and the silicon chip are estimated separately and then bonded via wire bonding.

Based calculation on a producing a laser diode array as 6 mask levels with abut 5 mask levels of metallization and silicon chip and its metallization production as 30 mask levels. Assume wire bonding cost to be about one cent per wire bond and it contains 32 pin in both the laser diode array[37] and the silicon chip. The wire bonding cost is estimated to be $0.64 per package. The assembly cost is estimated to be close to 20% of the fabrication cost [41].

Currently, the yields of III-V devices are low compared to silicon devices[16]. Since yield of III-V was about 60% in 1991[42], yield of current III-V devices can be assumed to be 70%. Assuming yield of silicon device to be 95%[42]. Cost of the printer chip package can be estimated.

Table 1: estimated cost of laser printer chip package based fabricated on 200mm silicon wafer

Silicon Chip	20	mm^2
Silicon wafer (200mm)	$20	
number of chip per wafer	1432	
cost per mask level	$60	
number of mask level	30	
fabrication cost		***$1800***
Estimate yield	0.95	
Laser diode array	10	mm^2
GaAs wafer (100mm)	$125	
number of chip per wafer	688	
cost per mask level	$60	
number of mask level	11	
fabrication cost		***$660***
Estimate yield	0.7	
packaging and assembly-wire bonding	$1.193	
Cost per unit	**$4.16**	

The calculation is based on 200mm silicon wafer, where it is still a common wafer facility in producing printer chips. The cost price was estimated to be about $4.16. This estimated price is close to production price of printer chips commercially available today, which is about $3 to $4[43, 44].

By changing the 200mm silicon wafer to 300mm silicon wafer, the cost price per unit can be reduced. However, the starting cost of changing the fabrication facilities would have to be considered. Table 2 illustrates the cost of producing a printer chip unit using 300mm silicon wafer in place of 200mm wafer.

Table 2: estimated cost of laser printer chip package based fabricated on 300mm silicon wafer

Silicon chip	20	mm^2
Silicon wafer (200mm)	$90	
number of chip per wafer	3325	
cost per mask level	$80	
number of mask level	30	
fabrication cost		***$2400***
Estimate yield	0.95	
Laser diode	4	mm^2
GaAs wafer (100mm)	$125	
number of chip per wafer	1808	
cost per mask level	$60	
number of mask level	11	
fabrication cost		***$660***
Estimate yield	0.7	
packaging and assembly-wire bonding	$0.882	
Cost per unit	**$2.29**	

From the estimation above, the cost could be lowered to $2.29 per unit by replacing 200mm wafer with 300mm wafer. Above the printer chip, the optical lens involved in the printer had to be considered. The optical system in a laser printer typically cost about $20[45].

Non-integrated LED printer head

OKI is currently the leading player in LED printers. LED printers prints by making used of an array of LEDs that were packaged at the print head. Currently, most LED printer prints with a resolution of 600 dpi. These LEDs are then connected to silicon IC drivers which control voltage across each LED. There consist of 26 print LED arrays across the width of the page. Each LED array consists of 192 LEDs and these LEDs are controlled by one silicon chip. This sums to a

total of 4992 LEDs across width of the page and these LEDs are in turn controlled by 26 silicon chips[28].

Each print chip is manufactured using die-to-wafer bonding. A four-inch GaAs substrate was used as the starting wafer. An epitaxial thin-film (EF) layer was then deposited on the substrate. This layer was measured to be about 2μm in thickness. With the help of a sacrificial layer, the EF layer and the GaAs substrate where separated. These dies are then transferred onto silicon substrate. The EF layer is attached onto silicon substrate using polyimide as adhesive. Finally, LEDs would be fabricated on the EF layer while the silicon chip would be fabricated on the silicon substrate[28]. The overall size of each of the printer chip is about 8.486mm^2. As the length of each of the chip is about 8mm across in length, a total of 26 print chips would be required to be placed across so as to provide signal across the whole page. Figure 8 shows a sketch of unprocessed GaAs dies on silicon substrate.

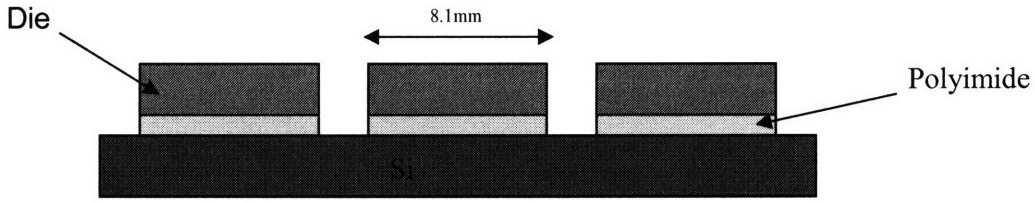

Fig 8: Unprocessed die on silicon wafer

In commercially available LED array drum chip, the price are in the range of USD$30 to USD$40[43, 44]. Table 3 shows breakdown of fabrication cost using the die-to-wafer on a 200mm wafer.

Table3: breakdown cost of LED printer head fabricated on 200mm wafer

Silicon chip	8.486	mm^2
Silicon wafer (200mm)	$20	
Die-to-wafer bonding	$300	
number of chip per wafer	3487	
cost per mask level	$60	
number of mask level	30	

fabrication cost		***$1800***
Estimate yield	0.95	
	100	mm
LED array	0.486	mm^2
GaAs wafer (100mm)	$125	
number of chip per wafer	15704.99	
cost per mask level	$60	
number of mask level	12	
fabrication cost		***$720***
Estimate yield	0.7	
packaging and assembly-wire bonding	$0.72	
Cost per unit	$1.37	
Cost per printer head (26 printer chips)	**$35.63**	

The cost of production is very much dependent on the cost per mask level of both the LED array fabrication process and the silicon chip process. As LED array are relatively simpler in terms of fabrication steps, less number of mask levels were required to fabricate the LED array compared to the silicon chip, making fabrication cost of the LED array to be relatively low. However, the yields of III-V devices are low compared to silicon devices fabrication[16]. The typical yield of III-V devices are about 60%[42] in 1991. Currently, the yield of III-V devices should be much higher. As a conservative estimate, the yield of LED array is assumed to be 70% in this cost model. Taking assembly cost of the whole printer head to be 20% of the fabrication cost of the silicon chip and LED array, the total cost of a printer head would cost about $35.63.

Looking at 300mm wafer fabrication, the cost per mask level is expected to be more expensive compared to 200mm wafer fabrication process. In the current cost model, the cost per mask level is calculated based on Intel wafer process which who are currently working at 45nm technology[39]. Cost model for 300mm wafer process is shown in table 4. The cost of the print head is expected to be about $30.62. This is a 13.5% decrease in cost price by using the larger wafers.

Table 4: breakdown cost of LED printer head fabricated on 300mm wafer

Die-to-wafer bonding	$300	
IC driver	8.486	mm^2
Silicon wafer (300mm)	$90	
number of chip per wafer	8005.248	
cost per mask level	$90	
number of mask level	30	
fabrication cost		***$2700***
Estimate yield	0.95	
LED array	0.486	mm^2
GaAs wafer (100mm)	$125	
number of chip per wafer	15704.99	
cost per mask level	$80	
number of mask level	12	
fabrication cost		***$960***
Estimate yield	0.7	
packaging and assembly-wire bonding	$0.69	
Cost per printer chip	$1.17	
Cost per printer head (26 printer chips)	**$30.62**	

Comparing laser printer chip and LED printer bar, there exists a huge cost difference. Even though LED printer printing system can eliminate some of the hardware component cost, the bulk difference in fabrication cost can come from printer chip fabrication. Typically selling price of a laser printer is about USD$200 per unit while that of LED printer is about USD$300[33].

This may be one of the reasons for LED printers not being able to penetrate into the market at the present moment.

However, the LED printer does carry an advantage of being able to give a much faster print rate. The advantage in performance may be able to account for the difference in price currently. However, there exists a need to lower the cost of production for LED printer so as to allow LED printer to further penetrate into the printer market.

LED printer head on SOLES

Exploring into the possibilities of SOLES, the cost of production could be further adjusted by bringing the fabrication process on SOLES. Since most fabrication infrastructures are switching to 300mm wafer process, the cost model of LED print head on SOLES will be based on 300mm wafer process. Table 5 shows the estimated cost of a LED print head. The overall cost of production is estimated to be about $26.66.

Table 5: breakdown cost of LED printer head using SOLES process on 300mm wafer

size of printer chip	8.486	mm2	
Silicon wafer (300mm)	$180		
number of chip per wafer	8005		
CVD	$300		
wafer bonding	$200		
IC chip			
cost per mask level	$90		
number of mask level	30		
fabrication cost			***$2700***
LED array			
cost per mask level	$90		
number of mask level	14		
fabrication cost			***$1260***
Estimate yield	0.65		
assembly	$0.134		
Cost per unit	$1.025		

Cost per printer head (26 printer chips)	**$26.66**

Comparing the cost price of SOLES printer head fabrication process to that of the conventional process, it can be observed that the reduction of cost came from the elimination of GaAs substrate, and die-to-wafer bonding process. It should be noted that there is a slight increase in number of mask levels in fabricating the LED array due to a need to deposit GaAs on Ge. Although, extra steps such as CVD and wafer bonding process are incurred into the fabrication process, it still results in an overall reduction of cost price. The reduction in cost is about 13%. This cost per mask level is expected to remain unchanged from the conventional method to SOLES method. This is because both fabrication techniques are of normal wafer process [39]. From this simplified model, it can be shown that cost reduction is possible with the introduction of SOLES. Even though this cost is still about slightly higher than that of a laser printer head system, it is expected that LED printer will give a higher print rate thus giving a performance advantage.

Further, it is projected that, by using SOLES, the number of LEDs that can be fabricated per unit area can be higher due to the integration process[10]. With the increased number of LEDs fabricated, the performance of the printer head can be further improved.

Comparing both techniques, the number of mask level required in the process are expected to greatly affect the cost of fabrication. Even though SOLES had proved to be of a lower fabrication cost in the case of LED array printer head, SOLES is not an ultimate cost saving fabrication technique at all times. Looking closely at both fabrication techniques, if the number of mask level in III-V devices fabrication is increased, the increase in cost per increase of III-V mask level using SOLES is expected to be higher than the increase in cost per increased of III-V mask level using die-to-wafer bonding technique.

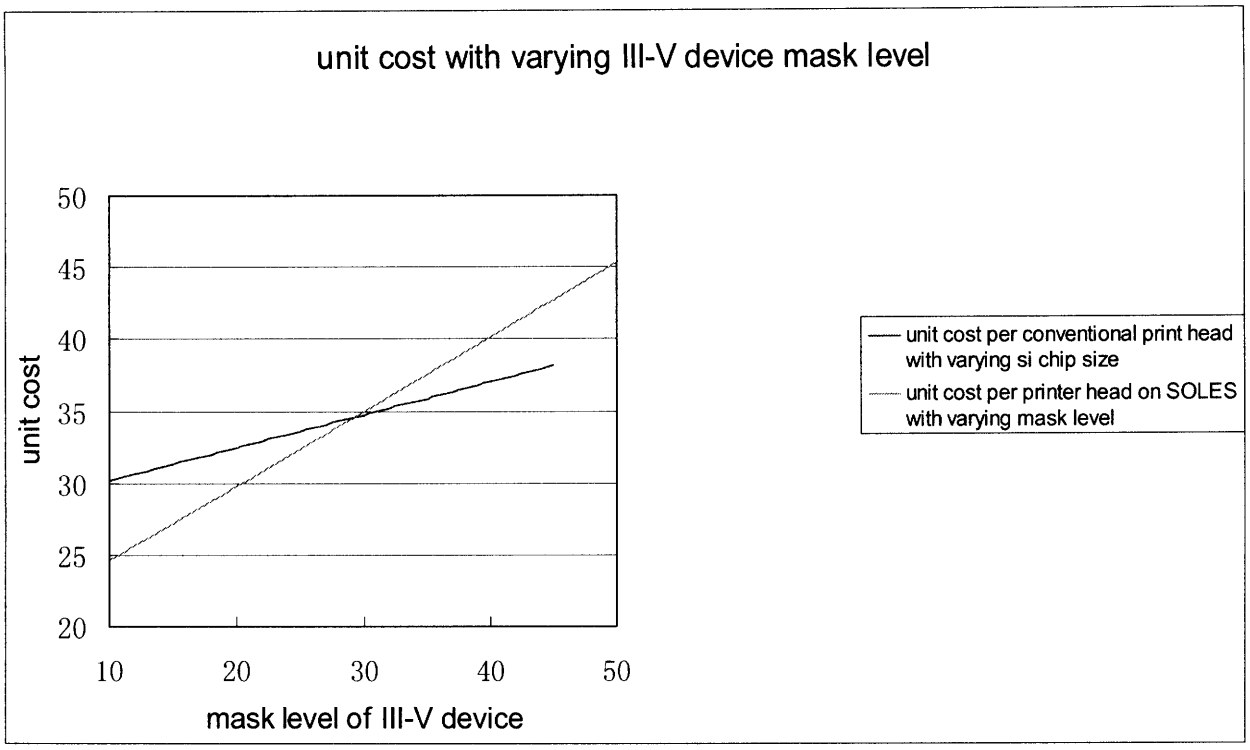

Fig 9: Unit cost per printer head with varying III-V device mask level

Figure 9 shows the unit price of integrated devices versus number of III-V process mask levels. It is observed that as the number of mask level required for III-V devices increases to more that 30 mask levels, SOLES process would incurred even higher cost compared to die-to-wafer bonding. This would imply that SOLES is suitable for III-V devices that are of moderate complexity fabrication method compared to the silicon devices.

On the other hand, SOLES process is observed to be able to support rather complicated silicon device processes. As shown in figure 10, SOLES process is projected to be cheaper than the conventional die-to-wafer fabrication process up to a 64 mask level process.

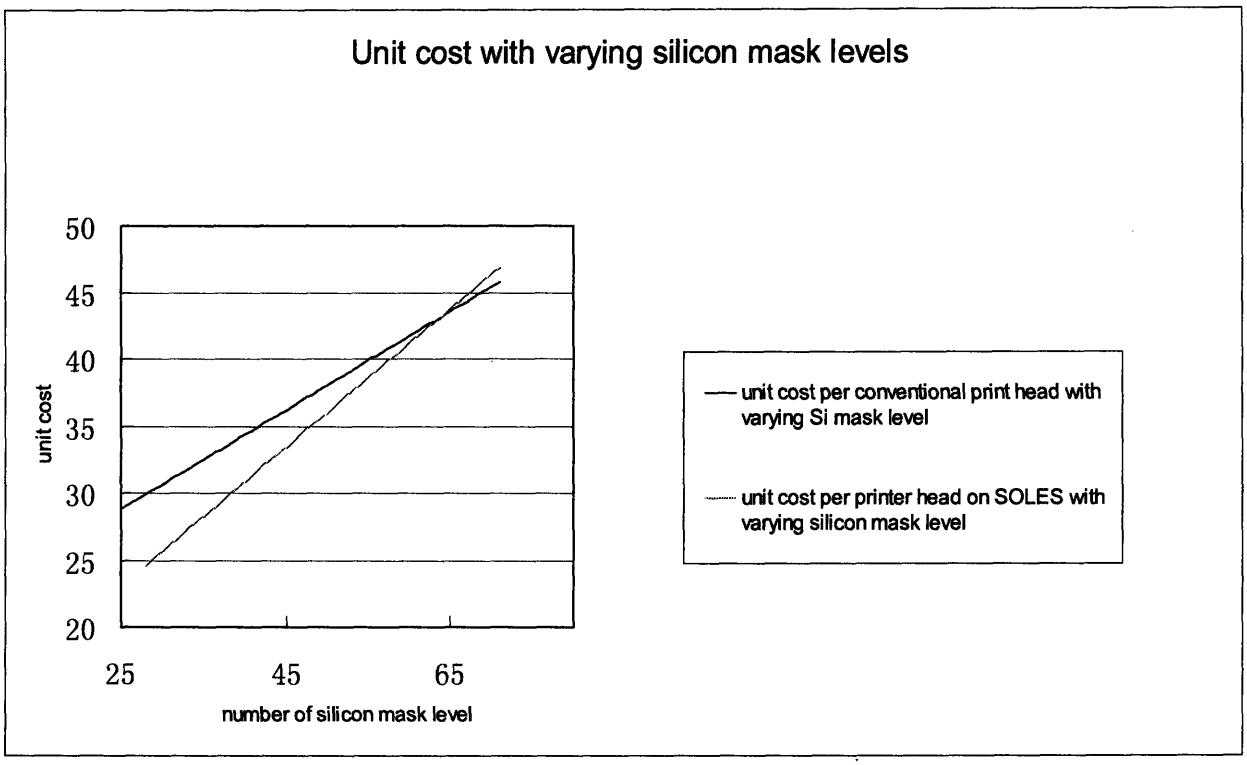

Fig 10: unit cost per printer head with varying silicon mask levels

From the analysis above, it can be concluded that SOLES process is able to support any complicated silicon devices fabrication process and it is able to support rather complicated III-V devices process of up to 30 mask levels at the same time.

The cost per unit mask level is also a factor that affects fabrication cost. Figure 11 shows a comparison of how cost per unit mask level of III-V device fabrication will affect cost price of a print head.

If it cost $50 per III-V mask level, the SOLES fabrication process cost about 44% less than the conventional fabrication process. However, the increase in cost per increment of silicon mask level is much higher in SOLES fabrication process compared to conventional process. The fabrication cost via SOLES process would overtake conventional technique if cost per III-V mask level is more than $110. Hence, it is important that cost per III-V mask level is kept low in the SOLES process.

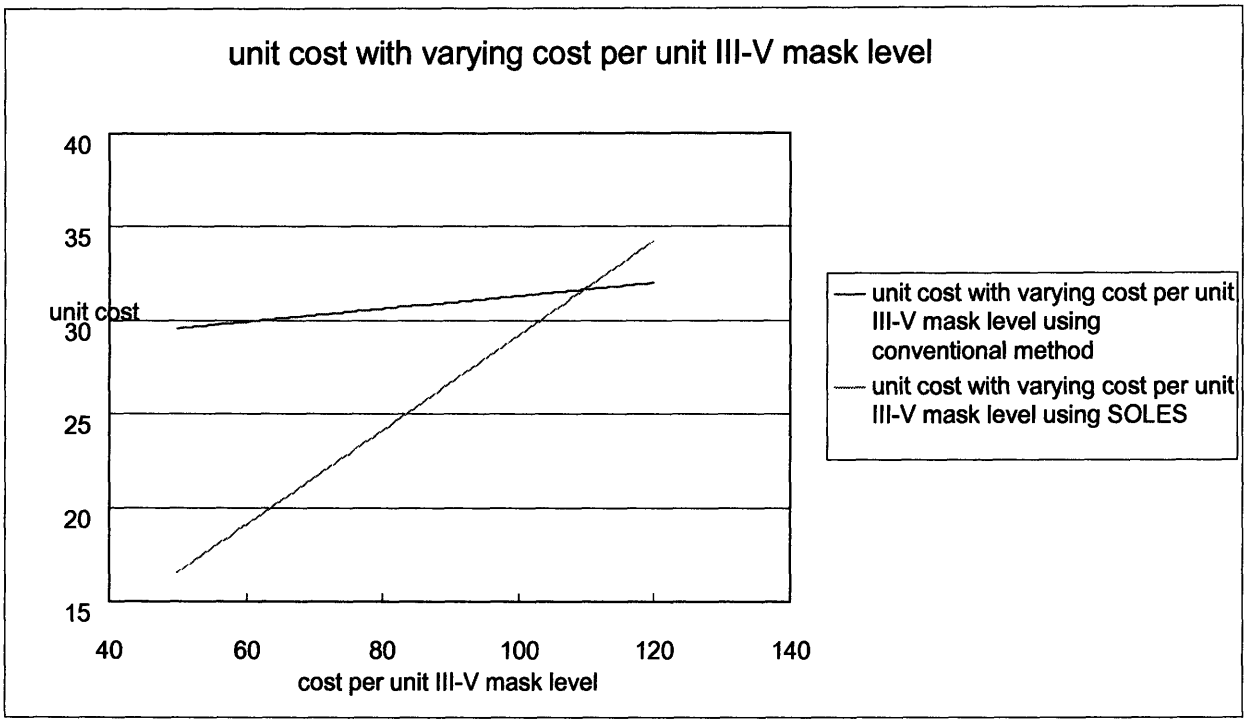

Fig 11: Unit cost with varying cost per unit III-V mask level

Figure 12 shows a comparison of how cost per unit mask level of silicon device fabrication will affect cost price of a print head. It can be observed that SOLES process would become more expensive than conventional process if cost per silicon mask level becomes more than $120. Since most silicon devices require an average cost of less than $140 per mask level[46], it can be concluded that SOLES process would be useful in most fabrication process.

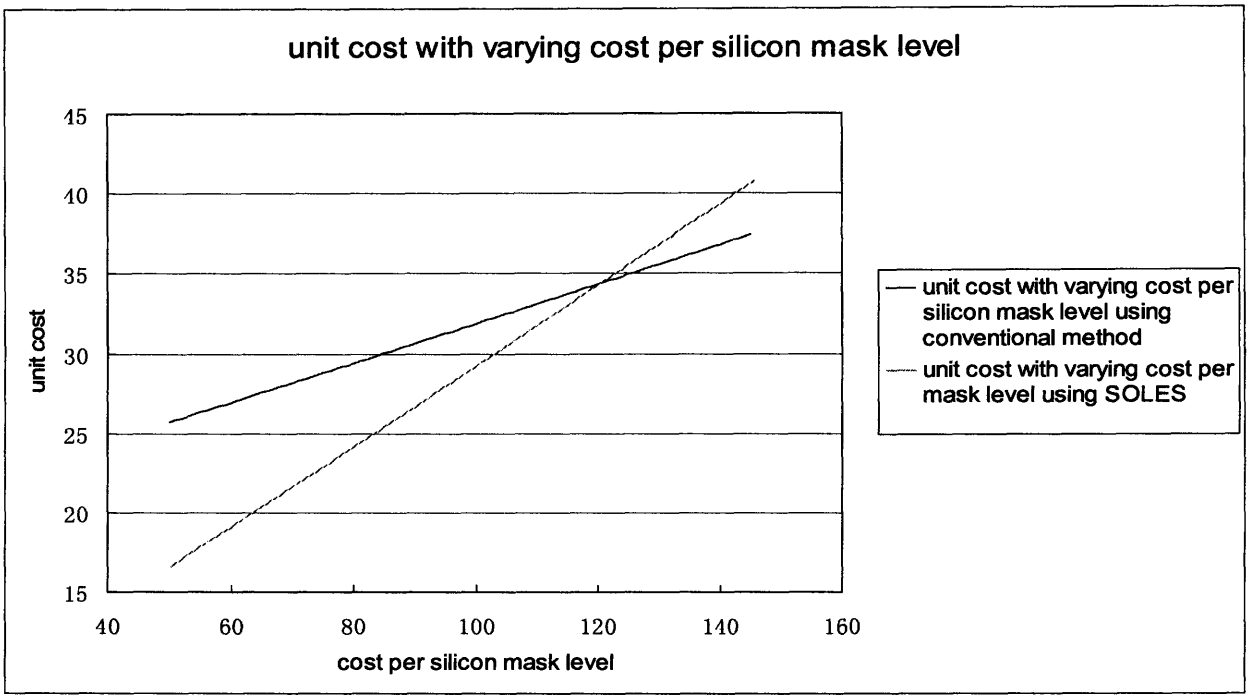

Fig 12: unit cost with varying cost per silicon mask level

From another point of view, cost of SOLES process is greatly affected by its yield. Figure 13 shows unit cost vs varying yield of production. It can be seen that the decrease in cost per unit increase in yield is rather high in the range of 60% to 85% yield. Thus, yield of SOLES process should be carefully considered when placing SOLES process into production.

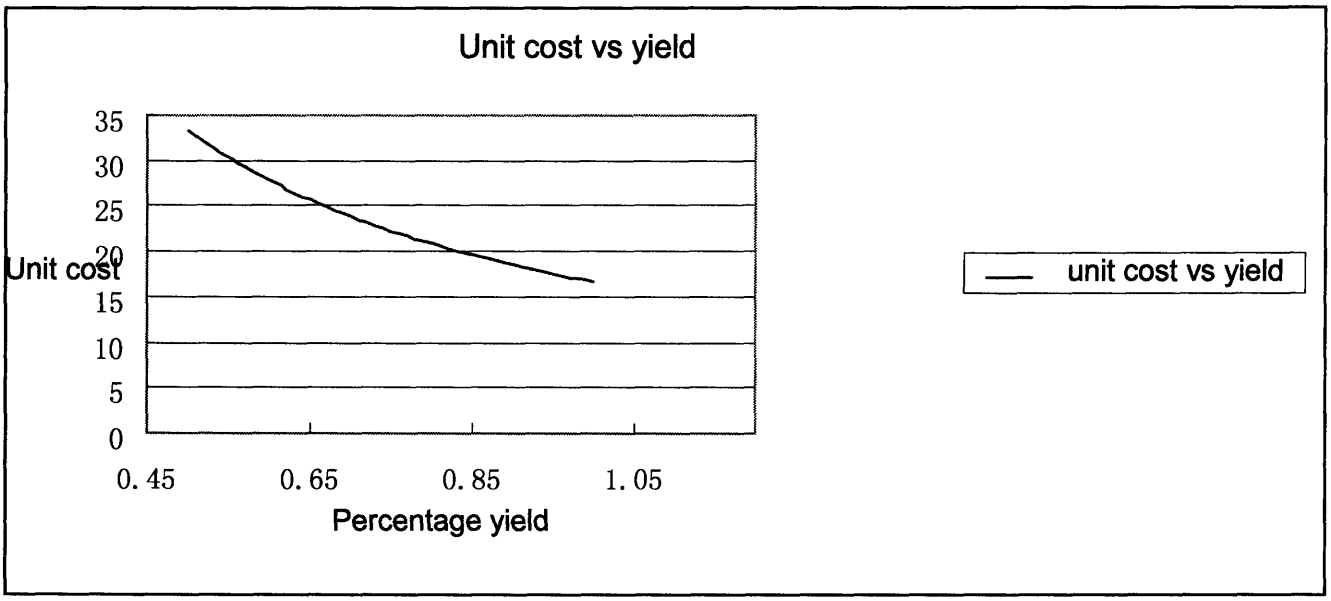

Fig 13: unit cost vs yield

From the comparison above, a general conclusion could be drawn. SOLES would be suitable of most silicon devices to be built onto. However, SOLES is only suitable for moderately complex III-V devices to be built on. Base on current technology, most III-V device can be fabricated below 30 mask level at a cost less than $110. Further, this suggest that LED printer head would be one of the possible application introduction point for SOLES to penetrate into the market since LED printer head only involves little mask levels in the III-V device process. Also, as LED printer head are rather simple in terms of design and fabrication process, little time would be required for production development before actual commercialization. Thus, allowing SOLES to be able to enter the market within the shortest time possible.

Business strategy

Looking at the conventional supply chain of optoelectronic enabled products. Optoelectronic devices and electronic devices are fabricated separately and then assembled together during packaging. It is estimated that packaging cost can be close to 20% of the cost price of a chip [41]. SOLES is a wafer that would be going to the bottom of the supply chain. It can be forecasted that SOLES would reduce many of the packaging steps as well as changing the fabrication process. This may prose a challenge in changing the supply chain.

As an effort to overcome such challenges, the business strategy has to be carefully evaluated. There are different approaches to commercialization of SOLES, one approach would be to set up an IP company and licensing the technology to wafer companies. This approach would allow simple management and royalties can be collected with each wafer sold. However, by licensing the technology to other companies, the start-up would lose its control over the application field of the technology. This may not be a good starting point as SOLES had demonstrated to be of high application potential in many areas. Furthermore, many companies would try to reverse engineer the technology with slight modification and go around the IP that is protecting it. Thus, IP Company is not taken as the approach in this case.

Another approach would be to build a fabless company. A fabless company would outsource most of its processes to production facilities. This approach is taken because this is of the low start-up cost by virtually integrating itself into the current supply chain in the field. Such a start-up would also give the company the flexibility to change its production plan within short time scale. Also, such a company would be a virtual vertical integration into the current supply chain. There are many companies that are producing both electronic device and optoelectronic devices; thus, it will be easier for SOLES to be introduced into these companies as a start. Figure 14 shows a simple supply chain of how optoelectronic products are usually fabricated.

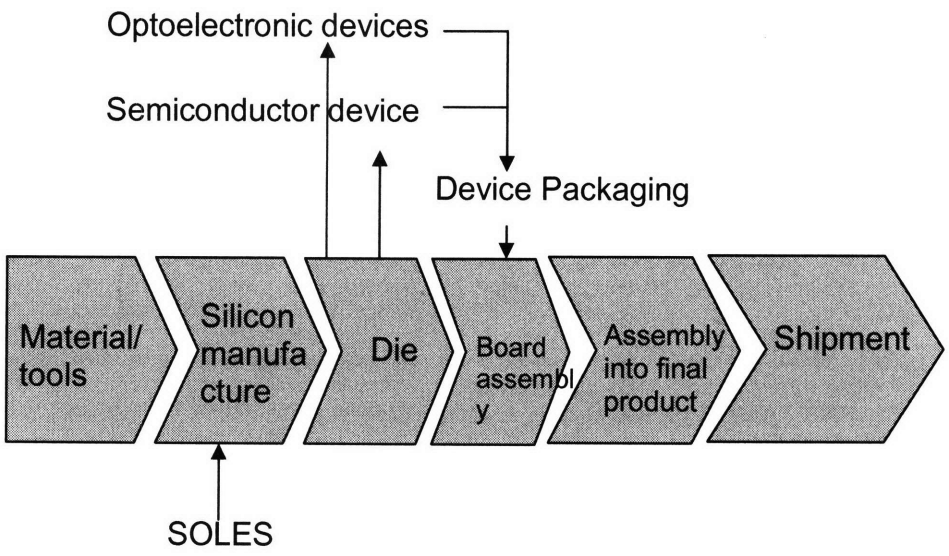

Fig 14: Conventional supply chain of optoelectronic enabled products

As a start, the start- up would consist of a small team of design engineers who would be responsible in designing the new SOLES printer chip. The production process would then be sub-contracted to fabrication facilities.

The estimated cost of a SOLES is about USD$26.66 per unit base on the cost analysis from the last section. This cost has not account for the cost of hiring design engineers. Assuming two design engineers are hired, an extra cost of $60K would be incurred annually.

A simple market projection model can then be built base on these values. Base on the 7.5 million printer unit global market.

The target market is expected to be 0.1% to 1%. Taking probability of 40% chance getting a market share of 0.1%, 30% chance of getting a market share of 0.5% and a 30% chance of getting a market share of 1%. The production volume is assumed to be either 8,500 or 40,000 or 100,000 per year. With all this chance values and expected outcome, the most profitable outcome would be to produce a volume of 100,000 per annual.

Assuming a selling price of USD$35 per printer chip, the expected profit would be USD$1.32M over the next five years ,with an expected sales of 210 thousand units, averaging to be about USD$264K per annum.

Conclusion

Over the years, much effort had been placed to integrate optoelectronic and electronic devices monolithically. Many had tried die to wafer bonding while others had tried wafer to wafer bond. SOLES is one of the more promising technologies in the area of wafer to wafer bonding technique. SOLES has already overcome most of its technological barriers in the path to commercialization. What lies ahead of it are mostly commercialization barriers which require in-depth market analysis and careful investment. The important steps ahead would to form ties with different printer manufacturers as well as wafer fabrication facilities. The author believed that SOLES is already at a mature stage that is ready for commercialization. Thus far, there are no pressing IP issues and arrays of LED connected to COMS circuitry had been fabricated successfully in the laboratory. The application of SOLES is wide; LED printer chip is only one of the many potential applications that are possible in SOLES. Base on the simple cost model that was built, LED printer head is expected to cost more than current laser printer chip. However, high speed printing of LED printer may be able to account for the cost difference. Comparing current fabrication technique of LED printer head and projected SOLES fabrication technique, fabrication cost is expected to decrease by about 13%. Since SOLES can be processed in most current fabrication infrastructures, little starting cost is expected by switching from current fabrication technique to SOLES process. Hence, SOLES is expected to bring in an extra profit compared to current fabrication technique.

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Appendix

Application potential: Substrate to support edge-light lighting in LCD display module

LCD display module backlighting can be mainly divided into to classes, back-lit and edge-lit. In LCD display module larger than 1 meter, the backlight is done by back-lighting. This is mainly because; edge-lit technology is unable to give enough brightness across the entire screen[47].

Regardless of the non-uniformity in brightness in edge-lit backlight, edge-lit is preferred when ever possible due to its less power consumption.

In edge-lit technology, the brightness is non-uniform across the screen[48]. Most of the time, a wedge guide is involved so as to compensate the non-uniformity across the screen[49]. The wedge guide used mainly to distribute light from a source placed beside the LCD display. Thus, the edge-lit display usually involve lower power consumption and thinner package[49].

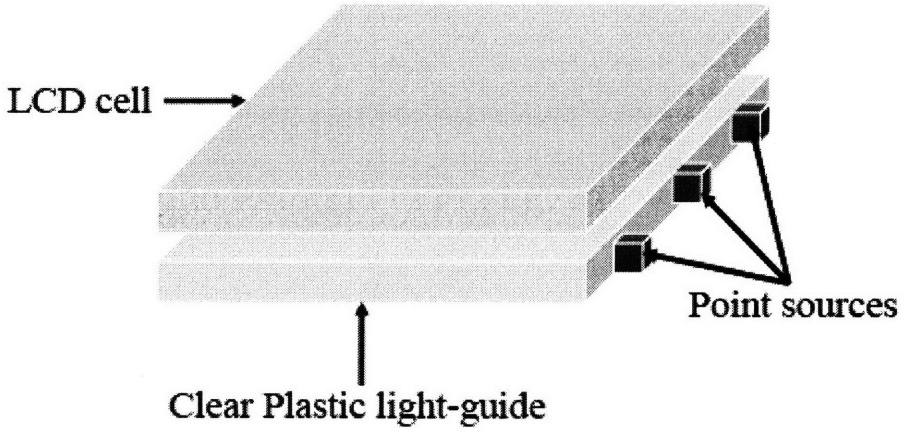

Fig A1: Edge-lit LCD display[49]

The light sources are usually a row of LED. A reflector is placed behind the source so as to increase the efficiency of the system. The wedge light guide will then exploits total internal reflection (TIR) so as to distribute light more evenly across the display area. Mirrored surfaces are also used so as to further increase the efficiency of the brightness across the screen. Most of the time, a patterned array film is used to control the luminous intensity and polarization of the emitted light.

Thus, the spacing of LED light source had to be carefully modeled so as to give enough brightness across the screen.

Many companies had ventured into the LCD display. Players such as Hitachi, Samsung, had tried to come out with different techniques so as to gain a larger portion in the LCD display market. Samsung is venturing mainly into OLED technology which ultimately relied on back-lit technology. In October 2007, Samsung had rolled out its plan to make 42in OLED display before 2010[50] and would be producing 14in OLED display by 2008[51]. Although Samsung's LCD display does not work on edge-lit technology, they are able to produce thin panel using OLED. This had also claimed that OLED processing cost can be lower than current back-lit technology [52]. This makes OLED a strong competitor in the LCD display market. Besides Samsung, Toshiba and Sony are other companies that have ventured into the OLED LCD display technology[53]. Toshiba had announced that 30in OLED display will be marketed in 2009.

Although, OLED is expected to be of lower cost than current back-lit technology, OLED displays are priced rather expensively currently. Sony had priced its 11in OLED display at $1,740 while Samsung is expected to price about $3,000 for its 14in display.

All these three companies had announced that OLED will be their focus in the near future[51]. Especially in the case of Sony, which had announce to phase out projection TV and focus on OLED[51].

Even though OLED is a technology that would be consuming less power compared to currently back-lit technology, it is still expected to consume more energy compared to edge-lit technology. Furthermore, the performance of OLED back-lit and LED edge-lit had yet to be looked into and compared. Thus, LED edge-lit display may still carry some advantage over the OLED back-lit technology.

Hitachi had been looking into LED edge-lit technology over the past few years. Also, Global Lighting Technologies (GLT) and Luminus Devices, Inc had announced that they would be partnering together to produce large LED edge-lit display[54]. Their edge-lit technology is expected to be able to produce 20in display module[54] as an introduction point of the technology.

From the above analysis, it can be observed that LCD display backlight is a rather large market ventured by many. Since OLED had not been penetrate totally into the market, SOLES may still be able to find its application point in the LED edge-lit display technology. Thus, SOLES can also consider venturing into the backlight display market.

Most edge-lit backlight source involves mounting the LED onto a PCB board; packaging is the most common technique of connection between the LED and the silicon circuitry[55]. Thus, if SOLES is to venture into this market, careful cost analysis may be necessary to ensure cost reduction compared to conventional fabrication method.

Relevant Patent

Processing aspect

Method of producing high quality relaxed silicon germanium layers

Abstract

A method for minimizing particle generation during deposition of a graded Si1-xGex layer on a semiconductor material includes providing a substrate in an atmosphere including a Si precursor and a Ge precursor, wherein the Ge precursor has a decomposition temperature greater than germane, and depositing the graded Si1-xGex layer having a final Ge content of greater than about 0.15 and a particle density of less than about 0.3 particles/cm2 on the substrate.

Patent number: 7041170
Filing date: Mar 19, 2003
Issue date: May 9, 2006

Inventors: Eugene A. Fitzgerald, Richard Westhoff, Matthew T. Currie, Christopher J. Vineis, Thomas A. Langdo
Assignee: AmberWave Systems Corporation
Primary Examiner: Robert Kunemund
Attorney: Goodwin Procter LLP

Application number: 10/392,338

U.S. Classification

117/89; 117/102; 117/105; 117/939

Coplanar integration of lattice-mismatched semiconductor with silicon via wafer bonding virtual substrates

Abstract

A method of bonding lattice-mismatched semiconductors is provided. The method includes forming a Ge-based virtual substrate and depositing on the virtual substrate a CMP layer that forms a planarized virtual substrate. Also, the method includes bonding a Si substrate to the planarized virtual substrate and performing layer exfoliation on selective layers of the planarized virtual substrate producing a damaged layer of Ge. Furthermore, the method includes removing the damaged layer of Ge.

Patent number: 6927147
Filing date: Jun 25, 2003
Issue date: Aug 9, 2005

Inventors: Eugene A. Fitzgerald, Arthuer J. Pitera

Assignee: Massachusetts Institute of Technology
Primary Examiner: Olik Chaudhuri
Secondary Examiner: Belur Keshavan
Attorney: Gauthier & Connors LLP
Application number: 10/603,850

U.S. Classification
438/458; 438/459

International Classification
H01L021/30

Process for producing semiconductor article using graded epitaxial growth

Abstract
A process for producing monocrystalline semiconductor layers. In an exemplary embodiment, a graded Si1-xGex (x increases from 0 to y) is deposited on a first silicon substrate, followed by deposition of a relaxed Si1-yGey layer, a thin strained Si1-zGez layer and another relaxed Si1-yGey layer. Hydrogen ions are then introduced into the strained SizGez layer. The relaxed Si1-yGey layer is bonded to a second oxidized substrate. An annealing treatment splits the bonded pair at the strained Si layer, such that the second relaxed Si1-yGey layer remains on the second substrate. In another exemplary embodiment, a graded Si1-xGex is deposited on a first silicon substrate, where the Ge concentration x is increased from 0 to 1. Then a relaxed GaAs layer is deposited on the relaxed Ge buffer. As the lattice constant of GaAs is close to that of Ge, GaAs has high quality with limited dislocation defects. Hydrogen ions are introduced into the relaxed GaAs layer at the selected depth.

Patent number: 6921914
Filing date: Mar 17, 2004
Issue date: Jul 26, 2005
Inventors: Zhi-Yuan Cheng, Eugene A. Fitzgerald, Dimitri A. Antoniadis, Judy L. Hoyt
Assignee: Massachusetts Institute of Technology
Primary Examiner: Craig A. Thompson
Attorney: Goodwin Procter LLP
Application number: 10/802,185

U.S. Classification
257/19; 257/55; 257/63; 257/65; 257/200; 257/616

International Classification
H01L029/06; H01L031/0328; H01L031/0336; H01L031/072; H01L031/109

Controlling threading dislocation densities in Ge on Si using graded GeSi layers and planarization

Abstract

A semiconductor structure including a semiconductor substrate, at least one first crystalline epitaxial layer on the substrate, the first layer having a surface which is planarized, and at least one second crystalline epitaxial layer on the at least one first layer. In another embodiment of the invention there is provided a semiconductor structure including a silicon substrate, and a GeSi graded region grown on the silicon substrate, compressive strain being incorporated in the graded region to offset the tensile strain that is incorporated during thermal processing. In yet another embodiment of the invention there is provided a semiconductor structure including a semiconductor substrate, a first layer having a graded region grown on the substrate, compressive strain being incorporated in the graded region to offset the tensile strain that is incorporated during thermal processing, the first layer having a surface which is planarized, and a second layer provided on the first layer.

Patent number: 7081410
Filing date: Apr 16, 2004
Issue date: Jul 25, 2006
Inventor: Eugene A. Fitzgerald
Assignee: Massachusetts Institute of Technology
Primary Examiner: Minh-Loan Tran
Attorney: Goodwin Procter LLP
Application number: 10/826,156

U.S. Classification
438/692; 438/697; 438/718; 438/933; 257E21125

Low threading dislocation density relaxed mismatched epilayers without high temperature growth

Abstract

A semiconductor structure and method of processing same including a substrate, a lattice-mismatched first layer deposited on the substrate and annealed at a temperature greater than 100° C. above the deposition temperature, and a second layer deposited on the first layer with a greater lattice mismatch to the substrate than the first semiconductor layer. In another embodiment there is provided a semiconductor graded composition layer structure on a semiconductor substrate and a method of processing same including a semiconductor substrate, a first semiconductor layer having a series of lattice-mismatched semiconductor layers deposited on the substrate and annealed at a temperature greater than 100° C. above the deposition temperature, a second semiconductor layer deposited on the first semiconductor layer with a greater lattice

mismatch to the substrate than the first semiconductor layer, and annealed at a temperature greater than 100° C. above the deposition temperature of the second semiconductor layer.

Patent number: 6864115
Filing date: Oct 9, 2002
Issue date: Mar 8, 2005
Inventor: Eugene A. Fitzgerald
Assignee: AmberWave Systems Corporation
Primary Examiner: David Nelms
Secondary Examiner: Thinh T Nguyen
Attorneys: Testa, Hurwitz & Thibeault LLP
Application number: 10/268,025

U.S. Classification
438/37; 438/37; 438/87

International Classification
H01L021/00

Utilization of miscut substrates to improve relaxed graded silicon-germanium and germanium layers on silicon

Abstract
A method of processing semiconductor materials, including providing a monocrystalline silicon substrate having a (001) crystallographic surface orientation; off-cutting the substrate to an orientation from about 2.degree. to about 6.degree. offset towards the [110] direction; and epitaxially growing a relaxed graded layer of a crystalline GeSi on the substrate. A semiconductor structure including a monocrystalline silicon substrate having a (001) crystallographic surface orientation, the substrate being off-cut to an orientation from about 2.degree. to about 6.degree. offset towards the [110] direction; and a relaxed graded layer of a crystalline GeSi which is epitaxially grown on the substrate.

Patent number: 6039803
Filing date: Feb 27, 1997
Issue date: Mar 21, 2000
Inventors: Eugene A. Fitzgerald, Srikanth B. Samavedam
Assignee: Massachusetts Institute of Technology

U.S. Classification
117/89; 117/101; 117/102; 117/902; 117/939

International Classification
C30B 2518

Smart cut process for the production of thin semiconductor materials films

Abstract
A process applicable to the production of monocrystalline films improves on the Smart-Cut.RTM. process by using an etch stop layer in conjunction with the Smart-Cut.RTM. process. Because of the etch stop layer, no chemical-mechanical polishing (CMP) is required after fabrication. Thus, the thickness and smoothness of the device layer in the fabricated silicon on insulator (SOI) substrate is determined by the uniformity and smoothness of the deposited layers and wet etch selectivity, as opposed to the CMP parameters. Therefore, the smoothness and uniformity of the device layer are improved.

Patent number: 5882987
Filing date: Aug 26, 1997
Issue date: Mar 16, 1999

Inventor: Kris V. Srikrishnan
Assignee: International Business Machines Corporation

U.S. Classification
438/458; 438/455; 438/406; 438/407; 438/977; 438/528; 148DIG50

International Classification
H01L 2130

Simultaneous multiple silicon on insulator (SOI) wafer production

Abstract
A method of forming multiple SOI wafers from a plurality of individual wafers each having a first side and a second side. The method includes forming an oxide surface on the first side on each of the plurality of individual wafers and forming a hydrogen rich region at a preselected depth on the second side on each of the plurality of individual wafers. The wafers are then bonded into a stacked configuration and heat treated to fracture the wafers at the hydrogen rich regions. This fracture forms at least two SOI wafers.

Patent number: 6326285
Filing date: Feb 24, 2000
Issue date: Dec 4, 2001

Inventors: Alex A. Behfar, Kris V. Srikrishnan
Assignee: International Business Machines Corporation

U.S. Classification
438/455; 438/458; 438/406

International Classification
H01L 2130

Method for manufacturing a semiconductor substrate

Abstract
Methods for manufacturing semiconductor substrates in which a semiconductor layer for forming semiconductor device therein is formed on a supporting substrate with an insulating film interposed between, with which in forming the semiconductor layer on a substrate on which a buried pattern structure has been formed it is possible to greatly increase the film thickness uniformity of the semiconductor layer and the film thickness controllability, particularly when the semiconductor layer is being formed as an extremely thin film. As a result, it is possible to achieve improved quality and characteristics of the semiconductor substrates and make possible the deployment of such semiconductor substrates to various uses.

Patent number: 6191007
Filing date: Apr 28, 1998
Issue date: Feb 20, 2001
Inventors: Masaki Matsui, Shoichi Yamauchi, Hisayoshi Ohshima, Kunihiro Onoda, Akiyoshi Asai, Takanari Sasaya, Takeshi Enya, Jun Sakakibara
Assignee: Denso Corporation
Primary Examiner: Christopher Lattin

U.S. Classification
438/459; 438/455; 438/458

International Classification
H01L 21331

Semiconductor substrate manufacturing method

Abstract
The invention provides a number of semiconductor substrate manufacturing methods with which, in manufacturing a semiconductor substrate having a semiconductor layer in an insulated state on a supporting substrate, it is possible to obtain a thick semiconductor

layer with a simple process and cheaply while reducing impurity contamination of the semiconductor layer to a minimum. One of these methods includes a defective layer forming step of carrying out ion implantation to a predetermined depth from the surface of a base substrate to partition off a monocrystalline thin film layer at the surface of the base substrate by a defective layer formed by implanted ions, a semiconductor film forming step of forming a monocrystalline semiconductor film of a predetermined thickness on the monocrystalline thin film layer, a laminating step of laminating the base substrate by the surface of the monocrystalline semiconductor film to the supporting substrate, and a detaching step of detaching...

Patent number: 6251754
Filing date: May 8, 1998
Issue date: Jun 26, 2001
Inventors: Hisayoshi Ohshima, Masaki Matsui, Kunihiro Onoda, Shoichi Yamauchi
Assignee: Denso Corporation
Primary Examiner: Granvill Lee

U.S. Classification
438/506; 438/506; 438/406; 438/458

International Classification
H01L 2120

Method of making semiconductor heterostructures of GaAs on Ge

Abstract
The invention is predicated upon the discovery by applicants that exposure of a Ge surface to arsenic produces a drastic change in the step structure of the Ge surface. Subsequent exposure to Ga and growth of GaAs produces three-dimensional growth and a high threading dislocation density at the GaAs/Ge interface. However exposure of the Ge surface to Ga does not substantially change the Ge step structure, and subsequent growth of GaAs is two-dimensional with little increase in threading dislocation density. Thus a high quality semiconductor heterostructure of gallium arsenide on germanium can be made by exposing a germanium surface in an environment substantially free of arsenic, depositing a layer of gallium on the surface and then growing a layer of gallium arsenide. The improved method can be employed to make a variety of optoelectronic devices such as light-emitting diodes.

Patent number: 5308444
Filing date: May 28, 1993
Issue date: May 3, 1994
Inventors: Eugene A. Fitzgerald, Jr., Jenn-Ming Kuo, Paul J. Silverman, Ya-Hong Xie
Assignee: AT&T Bell Laboratories
Primary Examiner: Ramamohan Rao Paladugu

U.S. Classification
117/90; 148DIG169; 117/95; 117/105; 117/106; 117/954

International Classification
H01L 2120

Annealing method for III-V deposition

Abstract
A method for producing wafers having deposited layers of III-V materials on Si or Ge/Si substrates is disclosed. The method involves the use of multiple in situ and ex situ annealing steps and the formation of a thermal strain layer to produce wafers having a decreased incidence of defects and a balanced thermal strain. The wafers produced thereby are also disclosed.

Patent number: 4835116
Filing date: Nov 13, 1987
Issue date: May 30, 1989
Inventors: Jhang W. Lee, Richard E. McCullough
Assignee: Kopin Corporation
Primary Examiner: William Bunch

U.S. Classification
437/111; 148DIG25; 148DIG48; 148DIG65; 148DIG94; 148DIG97; 148DIG110; 156/613; 437/126; 437/132; 437/247; 437/936; 437/939; 437/963; 437/973

International Classification
H01L 2120; H01L 21324

Process for obtaining a layer of single- crystal germanium on a substrate of single crystal silicon, and products obtained

Abstract
The invention concerns a method which consists in: (a) stabilization of the monocrystalline silicon substrate temperature at a first predetermined temperature T1 of 400 to 500 C.; (b) chemical vapour deposition (CVD) of germanium at said first predetermined temperature T1 until a base germanium layer is formed on the substrate, with a predetermined thickness less than the desired final thickness; (c) increasing the CVD temperature from said first predetermined temperature T1 up to a second predetermined temperature T2 of 750 to 850 C.; and (d) carrying on with CVD of germanium at said second predetermined temperature T2 until the desired final thickness

for the monocrystalline germanium final layer is obtained. The invention is useful for making semiconductor devices.

Patent number: 6537370
Filing date: Mar 9, 2001
Issue date: Mar 25, 2003
Inventors: Caroline Hernandez, Yves Campidelli, Daniel Bensahel
Assignee: France Tlcom
Primary Examiner: Felisa Hiteshew
Attorneys: Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C., Eric B. Meyertons
Application number: 9/786,996

U.S. Classification
117/88; 117/89; 117/97; 117/102; 117/105

International Classification
C30B 2504

Process for obtaining a layer of single- crystal germanium or silicon on a substrate single- crystal silicon or germanium, respectively and multilayer products obtained

Abstract
The process consists in depositing, by chemical vapour deposition using a mixture of silicon and germanium precursor gases, a single-crystal layer of silicon or germanium on a germanium or silicon substrate by decreasing or increasing the temperature in the range 800-450 C. and at the same time by increasing the Si/Ge or Ge/Si weight ratio from 0 to 100% in the precursor gas mixture, respectively.

Patent number: 6429098
Filing date: Sep 11, 2000
Issue date: Aug 6, 2002
Inventors: Daniel Bensahel, Yves Campidelli, Caroline Hernandez, Maurice Rivoire
Assignee: France Tlcom
Primary Examiner: Keith Christianson
Attorneys: Eric B. Meyertons, Conley, Rose & Tayon, P.C.
Application number: 9/659,913

U.S. Classification
438/478; 148/334

International Classification
H01L 2120

Liquid epitaxial process for producing three- dimensional semiconductor structures

Abstract
By a liquid epitaxial process monocrystalline semiconductor layers are produced having a high degree of crystal perfection in a multi-layer arrangement on intermediate layers of an insulating material and/or carbone and/or metal, in order to produce three-dimensional semiconductor structures which offer low mechanical stresses and load-bearing densities of between 10.sup.14 and 10.sup.21 per cm.sup.3. Very low manufacturing temperatures can be used, for example between 300.degree. and 900.degree. C. The seeding for each epitaxial layer is performed in the openings of the intermediate layer where a monocrystalline material is located in a free state. From these openings, the lateral and monocrystalline growth of the intermediate layers takes place. The repeated application of the liquid epitaxial process described allows three-dimensional integration in monocrystalline multilayer structures which are extremely devoid of defects.

Patent number: 5397736
Filing date: Jun 20, 1994
Issue date: Mar 14, 1995

Inventors: Elisabeth Bauser, Horst Paul Strunk
Assignee: Max-Planck-Gesellschaft zur Foerderung der Wissenschaften

U.S. Classification
437/92; 437/130; 437/131; 437/128; 437/108; 437/111; 437/120; 437/915

International Classification
H01L 2120; H01L 21208; H01L 2182; C30B 1900

Liquid phase epitaxial process for producing three- dimensional semiconductor structures by liquid phase epitaxial

Abstract
The present invention relates to a new application of the liquid epitaxial method, especially the manufacturing of epitaxial monocrystalline semiconductor layers having high crystalline perfection in multi-layer arrangements on an intermediate layer of an insulating material and/or carbon and/or metal for the manufacturing of a three-dimensional semi-conductor structure, in which low mechanical stresses are present and the charge carrier capacity is available between 10.sup.14 and 10.sup.21

per cubic centimeter, wherein very low process temperatures can be used, namely between 300.degree. and 900.degree. C. The seeding for the epitaxial layer is performed in openings made in the intermediate layer, wherein the monocrystalline material is exposed. From the openings the intermediate layers become overgrown laterally and in a monocrystalline fashion. The repeated application of the liquid epitaxy in the described fashion will permit a three-dimensional integration in monocrystalline...

Patent number: 5326716
Filing date: Jul 15, 1991
Issue date: Jul 5, 1994
Inventors: Elisabeth Bauser, Horst P. Strunk
Assignee: Max Planck-Gesellschaft zur Foerderung der Wissenschaften e.V.

U.S. Classification
437/92; 437/130; 437/131; 437/128; 437/108; 437/111; 437/120; 437/915

International Classification
H01L 2120; H01L 21208; H01L 2182; C30B 1900

Technology aspect

Integration technique

Monolithic integration of optoelectronic and electronic devices

Patent number: 4847665
Filing date: Mar 31, 1988
Issue date: Jul 11, 1989
Inventor: Ranjit S. Mand
Assignee: Northern Telecom Limited
Primary Examiner: David Soltz

U.S. Classification
357/16; 357/19; 357/56; 357/55; 357/30; 372/50; 350/961.2

International Classification
H01L 3100

Abstract
In the monolithic integration of HFET and DOES devices, a wide band gap carrier

confining semiconductor layer is provided only at predetermined locations where DOES devices are desired. This layer is not provided at other predetermined locations where HFET devices are desired as it would constitute a shunt path which would degrade the high frequency operation of the HFET devices. The invention is particularly useful where monolithic integration of optical sources, optical detectors, and electronic amplifying or switching elements is desired.

Integration of GaAs on Si substrates

Patent number: 5108947
Filing date: Jan 25, 1990
Issue date: Apr 28, 1992
Inventors: Piet M. Demeester, Ann M. Ackaert, Peter P. Van Daele, Dirk U. Lootens
Assignee: Agfa-Gevaert N.V.
Primary Examiner: William D. Bunch

U.S. Classification
437/89; 148DIG26; 148DIG97; 156/613; 437/132; 437/939; 437/962

International Classification
H01L 2120

Abstract
A method of growing a GaAs crystalline layer on a Si substrate by means of which mechanical stresses causing microcracks in the materials when cooled due to the difference in their thermal coefficients are reduced and the location of the microcrack is controlled to predetermined sites. Microcracks are deliberately induced in the GaAs layer at locations where the operation of the ultimate electronic device created on the material is not affected by applying to the substrate a SiO.sub.2 mask providing a deposition opening or window for the GaAs layer, which masks defines along the opening boundary at least one vertex in the cleavage direction of the GaAs crystals. The vertices in the mask create notches in the periphery of the deposited layer which determines the location of any microcracks.

Method of fabricating semiconductor devices on a group IV substrate

Application number: 11/776,163
Publication number: US 2008/0035939 A1
Filing date: Jul 11, 2007
Inventors: Norbert PUETZ, Simon FAFARD, Bruno J. RIEL
Assignee: CYRIUM TECHNOLOGIES INCORPORATED

U.S. Classification
257/94; 257/184; 438/478; 257E21119; 257E33014; 257E31005

Abstract
Electronic and opto-electronic devices having epitaxially-deposited III/V compounds on vicinal group IV substrates and method for making same. The devices include an AlAs nucleating layer on a Ge substrate. The group IV substrate contains a p-n junction whose change of characteristics during epitaxial growth of As-containing layers is minimized by the AlAs nucleating layer. The AlAs nucleating layer provides improved morphology of the devices and a means to control the position of a p-n junction near the surface of the group IV substrate through diffusion of As and/or P and near the bottom of the III/V structure through minimized diffusion of the group IV element.

Semiconductor buffer architecture for III-V devices on Si substrates

Application number: 11/498,685
Publication number: US 2008/0029756 A1
Filing date: Aug 2, 2006
Inventors: Mantu K. Hudait, Mohamad A. Shaheen, Dmitri Loubychev, Amy W.K. Liu, Joel M. Fastenau

U.S. Classification
257/14; 257/615; 257/628; 438/483; 438/496

Abstract
A composite buffer architecture for forming a III-V device layer on a silicon substrate and the method of manufacture is described. Embodiments of the present invention enable III-V InSb device layers with defect densities below 1×108 cm−2 to be formed on silicon substrates. In an embodiment of the present invention, a dual buffer layer is positioned between a III-V device layer and a silicon substrate to glide dislocations and provide electrical isolation. In an embodiment of the present invention, the material of each buffer layer is selected on the basis of lattice constant, band gap, and melting point to prevent many lattice defects from propagating out of the buffer into the III-V device layer. In a specific embodiment, a GaSb/AlSb buffer is utilized to form an InSb-based quantum well transistor on a silicon substrate.

Application area- LED printing technology

Xerox:

LED printing array fabrication method

Abstract
The method of fabricating Light Emitting Diodes (LEDs) with supporting circuits on a silicon chip or wafer for a Full Width Array (FWA) in which the silicon substrate or chip is first coated with Silicon Dioxide to form a thin film layer, a plurality of holes corresponding in number and configuration to the desired array are next opened in the layer, Gallium

Phosphide LEDs together with p-n junctions and contact layers are then grown epitaxially in the holes, and finally attendant LED operating circuits are epitaxially formed on the silicon chip together with operative connections to the individual LEDs by Integrated Circuit techniques.

Patent number: 4587717
Filing date: May 2, 1985
Issue date: May 13, 1986
Inventors: Joseph J. Daniele, Mehdi N. Araghi
Assignee: Xerox Corporation

U.S. Classification
29569L; 29576B; 148/15; 148/175

International Classification
H01L 736

High resolution, high efficiency I.R. LED printing array fabrication method

Abstract
An IR LED array and method of fabrication having a GaAs wafer with one surface metallized to form a common LED contact. Epitaxially formed on this wafer is a GaAs/GaAlAs heterostructure with successive layers of Ga.sub.1-x Al.sub.x As-n, GaAs-p, and Ga.sub.1-y Al.sub.y As-p on the other surface, followed by an electrical contact layer of GaAs-p+ and an insulating layer of SiO.sub.2, discrete areas of the contact and insulating layers being removed by etching to form viewing windows for the individual LEDs, and with the area of the contact layer bordering the viewing windows being exposed and metallized to provide individual LED electrical contacts. In a second embodiment, the GaAs-p+ layer is dispensed with and the transparent electrically conducting coating is applied directly on both the insulating layer bordering the Ga.sub.1-y Al.sub.y As viewing windows and over the viewing windows. In a third embodiment, an edge emitting LED variant is provided and in a fourth embodiment,...

Patent number: 4707716
Filing date: Aug 14, 1986
Issue date: Nov 17, 1987
Inventor: Joseph J. Daniele
Assignee: Xerox Corporation

U.S. Classification
357/17

International Classification
H01L 3300

Method of fabrication of porous silicon light emitting diode arrays

Abstract

A porous silicon Light Emitting Diodes (LEDs) device and method for fabricating LEDs with supporting circuits on a silicon chip or wafer for a Full Width Array in which a switch diode structure is used to form the porous silicon LED element and later drives the LED after the LED is fabricated. The LED is formed by defining an area in the switch diode for placing an LED element. Epi silicon is deposited in the defined area; and the epi silicon is electrochemical etched to produce porous silicon. This procedure creates column-like Si structures of nanometer dimension which can efficiently emit visible to infrared light at room temperature. Next, the porous silicon LED chip can be cut and butted without excessive damage. In this way, the chips bearing both LEDs and drive circuitry are made of silicon and can be cut and accurately butted by known techniques to form a low cost, high resolution Full Width LED array.

Patent number:5510633
Filing date: Jun 8, 1994
Issue date: Apr 23, 1996

Inventors: Thomas E. Orlowski, Sophie V. Vandebroek
Assignee: Xerox Corporation
Primary Examiner: Courtney A. Bowers

U.S. Classification
257/93; 257/94; 257/103

International Classification
H01L 3300

OKI:

Light emitting diode array print head having no bonding wire connections

Abstract

An LED array print head for an electrophotographic printer includes: LED array device packages each being loaded with an array of LEDs individually connected to a first major surface of the LED package by first solder joints; LED driver packages each loaded with a driver circuit connected to a first major surface of the driver package by second solder joints; and an optically transparent insulative substrate with a first major surface carrying conductive leads adapted to electrically connect the LEDs and driver circuits. The LED and driver packages are mounted on the substrate in such an orientation that the first

major surfaces of the packages face the first major surface of the substrate and the first and second solder joints are connected to the conductive leads of the substrate.

Patent number: 4916464
Filing date: May 4, 1989
Issue date: Apr 10, 1990
Inventors: Katsuyuki Ito, Naoji Akutsu, Yuhei Itasaka
Assignees: Oki Electric Industry Co., Ltd.
Primary Examiner: Scott A. Rogers

U.S. Classification
346/107R; 346/160

International Classification
G01D 942; G01D 1506

Opto-semiconductor device and method of fabrication of the same

Abstract

In an opto-semiconductor device, a light-emitting part formed on a substrate, a transparent insulating monocrystalline layer is formed over the entire surface of the substrate covering the light-emitting part, a contact window is opened through the transparent insulating monocrystalline layer in the center of the light-emitting part, and an electrode is formed of a transparent conductive monocrystalline layer passing through the contact window and connected to the central part of the light-emitting part, the electrode being formed on the transparent insulating monocrystalline layer. A transparent insulating monocrystalline layer may additionally be formed on the device including the electrode formed of the transparent conductive monocrystalline layer, and a photo-sensitive device formed of a monocrystalline layer may be provided on the transparent insulating monocrystalline layer.

Patent number: 5067809
Filing date: Jun 4, 1990
Issue date: Nov 26, 1991
Inventor: Takashi Tsubota
Assignees: Oki Electric Industry Co., Ltd.

U.S. Classification
357/17; 357/15; 357/16; 357/2; 357/4; 357/65; 357/67

International Classification
H01L 3300

Method of fabricating an LED array

Abstract

A method of fabricating an LED array includes forming a first insulating film composed of aluminum oxide on a semiconductor substrate of a first conductive type; patterning the first insulating film by photolithography to form a plurality of first windows; diffusing an impurity of a second conductive type through the plurality of first windows into the first insulating film, thereby forming a plurality of diffusion regions of the second conductive type below the plurality of first windows; forming a second insulating film on the first insulating film and the plurality of first windows; patterning the second insulating film by photolithography to-remove the second insulating film from the plurality of first windows, using an etchant that does not etch the first insulating film; forming a metal film on the second insulating film and the plurality of first windows; and patterning the metal film by photolithography to form a plurality of electrodes which make electrical contact...

Patent number: 5869221
Filing date: Dec 24, 1997
Issue date: Feb 9, 1999
Inventors: Mitsuhiko Ogihara, Yukio Nakamura, Takatoku Shimizu, Masumi Taninaka
Assignees: Oki Electric Industry Co., Ltd.

U.S. Classification
430/311; 430/313; 257/88

International Classification
G03F 900

Led array, print head, and electrophotographic printer

Abstract

In an array of light-emitting diodes formed by diffusion of an impurity into a semiconductor substrate, the width of the diodes in the array direction is between four-tenths and five-tenths of the array pitch. The width of the windows above the diodes is between three-tenths and four-tenths of the array pitch. Between one-fourth and one-half of the surface area of each diode is covered by an electrode making contact with the diode through the window. The distance from the centers of the light-emitting diodes at the ends of the array to the edges of the substrate is between twenty-five and sixty-five hundredths of the array pitch.

Patent number: 6064418
Filing date: Apr 9, 1998
Issue date: May 16, 2000

Inventors: Takatoku Shimizu, Mitsuhiko Ogihara, Masumi Taninaka, Hiroshi Hamano
Assignee: Oki Data Corporation

U.S. Classification
347/238; 347/130

International Classification
B41J 245

LED array

Abstract
A 1200 dpi LED may be manufactured without highly accurate mask alignment and provide good light radiation efficiency. A first interlayer dielectric is formed on a semiconductor substrate and has a plurality of first windows formed therein and aligned in a row. A diffusion region is formed in the semiconductor substrate through each of the first windows. An electrode is formed to have an area in contact with the corresponding diffusion region. Another electrode is formed on the other side of the substrate. A second interlayer dielectric is formed on the first interlayer dielectric such that the second interlayer dielectric does not overlap the area of the electrode and does not extend to a first perimeter of the area.

Patent number: 6211537
Filing date: Mar 18, 1998
Issue date: Apr 3, 2001
Inventors: Takatoku Shimizu, Mitsuhiko Ogihara, Masumi Taninaka, Hiroshi Hamano
Assignees: Oki Electric Industry Co., Ltd.
Primary Examiner: Matthew E. Warren

U.S. Classification
257/88; 257/89; 257/90; 257/91; 257/92; 257/99; 257/100; 257/640; 257/651; 257/639

International Classification
H01L 3300

Led array, and led printer head

Abstract
According to the present invention, a plurality of p-type semiconductor layers 13 are formed in a single row and a first layer insulating film 12 having first opening portions 16a and an n-side opening portion 17 is formed on the layers in an n-type semiconductor block 11. On the first layer insulating film 12, p-side electrodes 14 to connect to the

p-type semiconductor layers 13 at the first opening portions 16a and an n-side electrode 55 (an n-side contact electrode 55a and an n-side pad electrode 55b) to connect with the n-type semiconductor block 11 at the n-side opening portion 17 are formed. Furthermore, p-side common wirings 4 to connect with specific p-side electrodes 14 are formed via a second layer insulating film 18. The p-side electrodes 14 and the n-side electrode 55 are formed using the same conductive film material through a single film formation and patterning process. An Au alloy film, for instance, may be used to form the conductive film that is to constitute...

Patent number: 6388696
Filing date: May 27, 1998
Issue date: May 14, 2002
Inventors: Masumi Taninaka, Mitsuhiko Ogihara, Hiroshi Hamano, Takatoku Shimizu
Assignees: Oki Electric Industry Co., LTD
Primary Examiner: N. Le
Secondary Examiner: Lamson D. Nguyen
Attorneys: Venable, Norman N. Kunitz
Application number: 9/084,324

U.S. Classification
347/238; 347/237; 257/88

International Classification
B41J 245

LED array chip

Abstract

An LED array chip comprises a semiconductor substrate having a front surface and a side surface. The first surface and the front surface come together at an end of the chip to define an end portion of said semiconductor substrate that has an acute angle between the first surface and the front surface. The end of the chip defines an outermost dimension of the chip. The first surface extends further away from the front surface than the diffuison depth of the light emitting elements. A method of manufacturing an LED array chip includes the steps of: forming grooves between adjacent LED arrays of the plurality of LED arrays, each of the grooves having opposing side walls each of which makes an acute angle with the front surface; and dicing the semiconductor wafer except for the opposing side walls of each of the grooves to separate the plurality of LED arrays into individual LED array chips.

Patent number: 6515309
Filing date: Dec 27, 1999
Issue date: Feb 4, 2003
Inventors: Hiroshi Tohyama, Susumu Ozawa, Yuko Kasamura, Satoru Yamada

Assignees: Oki Electric Industry Co., Ltd.
Primary Examiner: Olik Chaudhuri
Secondary Examiner: Timothy Sutton
Attorneys: Akin Gump Strauss Hauer & Feld, L.L.P.
Application number: 9/472,349

U.S. Classification
257/88; 438/33; 438/68; 438/462

International Classification
H01L 3300; H01L 2100; H01L 21301; H01L 2146; H01L 2178

Method of manufacturing a semiconductor device

Abstract
A crystal growth 301 is carried out by diffusing a metal element, and a nickel element is moved into regions 108 and 109 which has been doped with phosphorus. An axis coincident with the moving directions 302 and 303 of the nickel element at this time is made to coincide with an axis coincident with the direction of the crystal growth, and a TFT having the regions as channel forming regions is manufactured. In the path of the region where nickel moved, since high crystallinity is obtained in the moving direction, the TFT having high characteristics can be obtained by this way.

Patent number: 6165824
Filing date: Mar 3, 1998
Issue date: Dec 26, 2000
Inventors: Tamae Takano, Hideto Ohnuma, Hisashi Ohtani, Setsuo Nakajima, Shunpei Yamazaki
Assignees: Semiconductor Energy Laboratory Co., Ltd.
Primary Examiner: Michael S. Lebentritt

U.S. Classification
438/160; 438/166; 438/175; 438/486; 438/571

International Classification
H01L 2100; H01L 2120

Semiconductor apparatus, led head, and image forming apparatus

Abstract
A semiconductor apparatus has a substrate to which is attached a thin semiconductor film including at least one semiconductor device. A first interconnecting line formed on the thin semiconductor film makes electrical contact with the semiconductor device. A

second interconnecting line extends from the thin semiconductor film to the substrate, electrically coupling the first interconnecting line to an interconnection pattern on the substrate. At the point where the first and second interconnecting lines meet, one of the two interconnecting lines is widened to provide an increased positioning margin, thereby relaxing the requirement for precise positioning of the thin semiconductor film. The thin semiconductor film may include an array of light-emitting diodes and the substrate may include driving circuitry for driving them.

Patent number: 7061113
Filing date: Aug 26, 2004
Issue date: Jun 13, 2006
Inventors: Hiroyuki Fujiwara, Mitsuhiko Ogihara
Assignee: Oki Data Corporation
Primary Examiner: Mai-Huong Tran
Attorneys: Akin Gump Strauss Hauer & Feld, LLP
Application number: 10/926,890

U.S. Classification
257/758; 257/758; 257/761; 257/763; 257E2316

Performance

VCSEL array-based light exposure system for laser printing

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ABSTRACT
Improving the image quality and speed is an endless demand for printer applications. To meet the market requirements, we have launched the world first laser printer (DocuColor 1256 GA) introducing 780-nm single-mode 8×4 VCSEL arrays in the light exposure system in 2003. The DocuColor 1256 GA features 2400 dots per inch (dpi) resolution which is the highest in the industry and a speed of 50 pages per minute (ppm). A VCSEL array design has an advantage that it can increase the pixel density and also increase the printing speed by simultaneously scanning the 32-beam to the photoconductor in the exposure process. Adopting VCSELs as a light source also contributes to the reduction of the machine's power consumption. The VCSELs are industrially manufactured based on the original in-situ monitored oxidation process to control the oxide aperture size. As a result, uniform characteristics with a less than 5% variation in both output power and divergence angle are obtained. Special care is also taken in the assembly process to avoid additional degradation in performance and quality. This technology is currently extended to high-end tandem color machines (2400 dpi, 80 ppm) to grasp on-demand

publishing market. This paper will cover the key technologies of the VCSEL based light exposure system as well as its manufacturing process to assure its quality.

LED array integrated with Si driving circuits for LED printer printhead

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Oki Digital Imaging Corp., Tokyo, Japan;

Abstract
A 600 dots per inch LED array chip integrated with Si drivers using a three-dimensional epitaxial thin-film bonding has been developed. Performance tests showed high emitted light power (47 /spl mu/W at an LED current of 1 mA) with smaller variations (/spl plusmn/7%), and long lifetime. Test results provide good enough characteristics to use the LED array chip in a high-printing-speed LED printer printhead.

Business Strategy

Projected sales

Table A1: Projected sales of market penertration of 0.1%, 0.5% and 1%; total market size of 7.5 million

TOTAL MARKET FOR PART(/YR)= 7,500,000

Scenario	Year	Market Share Growth Rate	Market Share	Total Units Projected/yr
LOW	2008	N/A	0.1%	7,500
	2009	2%	0.1%	7,650
	2010	2%	0.1%	7,803
	2011	2%	0.1%	7,959
	2012	2%	0.1%	8,118
	TOTAL			39,030
MEDIUM	2008	N/A	0.5%	37,500
	2009	6%	0.5%	39,750
	2010	6%	0.6%	42,135
	2011	6%	0.6%	44,663
	2012	6%	0.6%	47,343
	TOTAL			211,391
HIGH	2008	N/A	1.0%	75,000

2009	8%	1.1%	81,000
2010	8%	1.2%	87,480
2011	8%	1.3%	94,478
2012	8%	1.4%	102,037
TOTAL			439,995

Table A2: probabilities of gaining different market share

Probabilities
probabilities for low, medium and high
market share in the next 5 years
for setting selling price at $35 and $40

	Prob $35	Prob $40
low	40.00%	70.00%
medium	30.00%	20.00%
high	30.00%	10.00%

Setting production size to be 8,500 or 40,000 or 100,000

Table A3: projected revenue and sales volume with a production size of 8,500 per annum

		8,500	UNIT production per annum
EARNINGS			
	PRICES:	$35.00	$40.00
	LOW	$259,146	$414,509
	MEDIUM	$283,043	$452,733
	HIGH	$283,043	$452,733
PRODUCTION AND COSTS			
	# OF UNITS	$/UNIT	TOTAL COST
2008	7,500	26.66	$199,950
2009	7,650	26.66	$203,949
2010	7,803	26.66	$208,028

2011	7,959	26.66	$212,189
2012	8,118	26.66	$216,432
TOTAL	39,030		$1,040,548
2008	8,500	26.66	$226,610
2009	8,500	26.66	$226,610
2010	8,500	26.66	$226,610
2011	8,500	26.66	$226,610
2012	8,500	26.66	$226,610
TOTAL	42,500		$1,133,050
2008	8,500	26.66	$226,610
2009	8,500	26.66	$226,610
2010	8,500	26.66	$226,610
2011	8,500	26.66	$226,610
2012	8,500	26.66	$226,610
TOTAL	42,500		$1,133,050

Table A4: projected revenue and sales volume with a production size of 40,000 per annum

		40,000	UNIT production per annum
EARNINGS			
	PRICES:	$35.00	$40.00
	LOW	$259,146	$414,509
	MEDIUM	$1,310,875	$2,096,771
	HIGH	$1,331,968	$2,130,510
PRODUCTION AND COSTS			
	# OF UNITS	$/UNIT	TOT. COST
2008	7,500	26.66	$199,950
2009	7,650	26.66	$203,949
2010	7,803	26.66	$208,028
2011	7,959	26.66	$212,189
2012	8,118	26.66	$216,432
TOTAL	39,030		$1,040,548
2008	37,500	26.66	$999,750

2009	39,750	26.66	$1,059,735
2010	40,000	26.66	$1,066,400
2011	40,000	26.66	$1,066,400
2012	40,000	26.66	$1,066,400
TOTAL	197,250		$5,258,685
2008	40,000	26.66	$1,066,400
2009	40,000	26.66	$1,066,400
2010	40,000	26.66	$1,066,400
2011	40,000	26.66	$1,066,400
2012	40,000	26.66	$1,066,400
TOTAL	200,000		$5,332,000

Table A5: projected revenue and sales volume with a production size of 100,000 per annum

			100,000	UNIT production per annum
EARNINGS potential selling price:		PRICES:	$35.00	$40.00
		LOW	$259,146	$414,509
		MEDIUM	$1,395,274	$2,231,769
		HIGH	$2,884,273	$4,613,454
PRODUCTION AND COSTS		# OF UNITS	$/UNIT	TOT. COST
	2008	7,500	26.66	$199,950
	2009	7,650	26.66	$203,949
	2010	7,803	26.66	$208,028
	2011	7,959	26.66	$212,189
	2012	8,118	26.66	$216,432
TOTAL		39,030		$1,040,548
	2008	37,500	26.66	$999,750
	2009	39,750	26.66	$1,059,735

	2010	42,135	26.66	$1,123,319
	2011	44,663	26.66	$1,190,718
	2012	47,343	26.66	$1,262,161
TOTAL		211,391		$5,635,684
	2008	75,000	26.66	$1,999,500
	2009	81,000	26.66	$2,159,460
	2010	87,480	26.66	$2,332,217
	2011	94,478	26.66	$2,518,794
	2012	100,000	26.66	$2,666,000
TOTAL		437,958		$11,675,971