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Tektronix™ Solid Ink Printer

Print Head Drive Board

Cost Reduction Project

By

Gary W. Gill

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degrees of

Bachelor of Science in Electrical Science and Engineering

and Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

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ABSTRACT

The Tektronix™ solid ink ink jet color printer dealt with in this project is designed for the office environment. The cost of the print head drive board, which supplies the high voltage print waveforms to the print head, was reduced by replacing the custom high voltage driver chips with standard NEC™ high voltage drivers, NEC™ uPD16306. Each NEC™ chip has twice the number of high voltage outputs of the original chips, thus only half the number of high voltage driver chips are required on the new board. In order to use the new board as a drop in replacement for the old board a PAL based control logic interface was designed. Level shifting circuits were designed in order to use the NEC™ chips with the high voltage print waveforms. At the time of this paper, the new print head drive board is being evaluated at Tektronix™ for robustness and cost savings.

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Title: Technical Instructor, 6.101 Analog Design Lab
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Overview

1.1 Introduction

The Tektronix solid ink ink jet printer dealt with in this project is designed for the office environment. Since the printer began production in 1995, most of the major manufacturing problems have been solved, and the emphasis of manufacturing engineering has switched from problem solving to cost reduction. The cost reduction effort was the main driving force behind this project.

The print head on the printer uses several hundred ink jets to distribute four colors (black, yellow, cyan, and magenta) onto the printed page. Driven by individual piezo-electric pumps, these jets must be connected to a very specific voltage waveform, which is generated by the power electronics of the printer and supplied to the print head drive board. This waveform determines how much ink is deposited with each firing of the ink jet. All jets being fired are connected to the print waveform while the unused jets remain at zero volts.

The current head drive board uses ASICs custom made by Motorola™ for Tektronix™ to control each of the ink jets. Each of these ASICs is capable of driving 33 ink jets, hence each head drive board requires the use of about ten of these chips.

The cost reduction project involved replacing these custom ASICs with a standardized chip currently produced by NEC™. This part, NEC™ uPD16306, has 64 high-voltage outputs thus only half chips are required per board. The per-chip price of this part is approximately equal to that of the Motorola™ part, but only half the number of parts are required. Since the high voltage driver chips comprise a major portion of the cost of the head drive board, the new head drive board will be considerably less expensive.

1.2 Background of Printer Control Electronics

A block diagram showing the organization of the printer as it pertains to the head drive board is shown in figure 1.1.

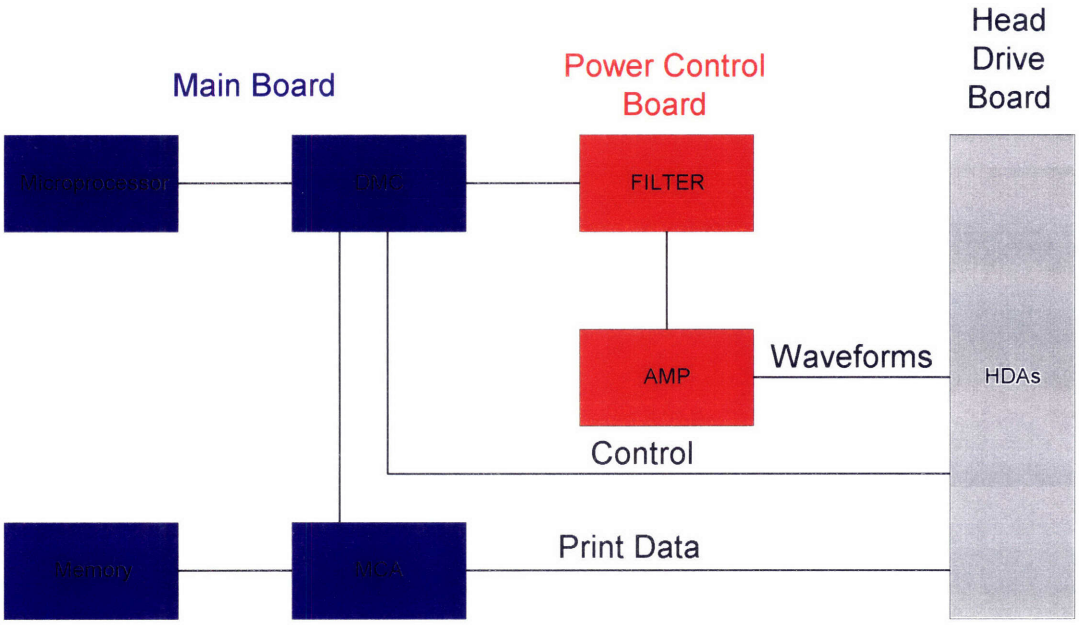


Figure 1.1

The DMC (Digital Motion Controller) is responsible for generating the print voltage waveform and providing the control signals for the head drive board. The MCA (Memory Control ASIC) supplies the actual print data to the head drive board where the data is routed through the HDAs (Head Drive ASICs). The HDAs directly drive the individual ink jets on the print head.

As mentioned, each ink jet must be driven by a very specific voltage signal in order to achieve the correct drop mass and velocity. The microprocessor uses information about the waveform and generates a digital version. The DMC then takes this information and sends it to an analog filter where the waveform is reconstructed. This waveform is amplified and sent to the head drive board. The high voltage waveform is repeated for each firing of the ink jets. A typical print waveform is shown in figure 1.2.

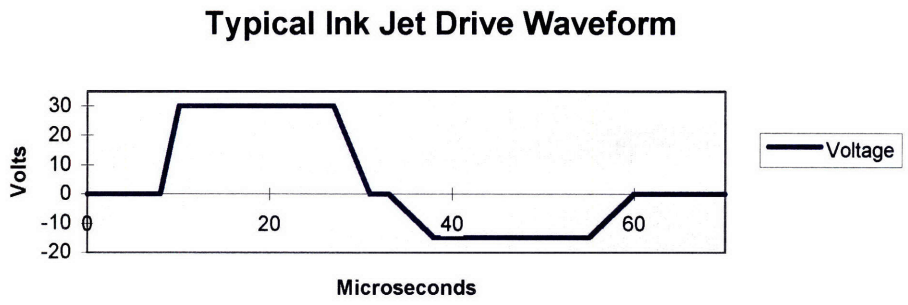


Figure 1.2

This waveform is divided into two independent signals. V_{pp}, the positive pulse, and V_{ss}, the negative pulse, are generated and amplified independently. When viewed separately, the waveforms appear as shown in figure 1.3.

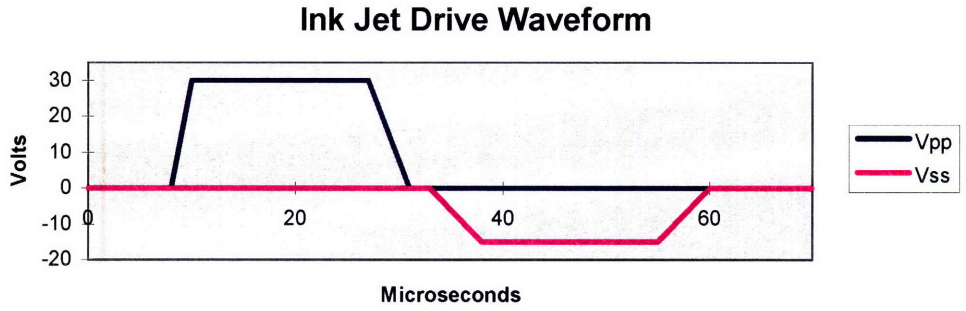


Figure 1.3

The original Head Drive ASIC (HDA) receives logic level (0 to 5.0 V)inputs to control the high voltage (0 to + or - 60 V) PZT drive outputs. The function of the HDA is to switch its outputs between the three states of V_{ss}, V_{pp}, and open (high impedance) at the appropriate times. The HDA receives data serially and outputs it in parallel to all 33 high voltage outputs.

The NEC™ uPD16306 is similar to the HDA with several important differences. This CMOS device is controlled by three logic level inputs to control the high voltage outputs. Where the HDA is capable of switching between V_{ss}, V_{pp}, and open, the NEC™ part can only switch its outputs between its high voltage source

and ground. As with the HDA, data is received serially and output in parallel to its high voltage outputs. However, each chip has 64 high voltage outputs to the 32 outputs of the HDA.

1.3 Difficulties and Main Areas of Design

There are two main issues that had to be addressed in order to adapt the head drive board to the uPD16306. First, the control signals for the HDA and the uPD16306 are different. In order to make a print head board that can be used as a drop in replacement for the current print head board, it was necessary to design an on-board interface that takes the control signals for the HDA as inputs and outputs the corresponding control signals for the uPD16306. Additionally, data shifting is run differently for each of the chips. The shift register in the HDA shifts at the positive edge of the clock signal and only when the SHIFT control line is high. The shift register in the uPD16306 shifts on every negative clock edge. Thus the uPD16306's shift register will shift data at times when the shift register in the HDA would not. Therefore the data should be latched as soon as it is in position. The selected solution to these problems was to use a PAL as an interface to translate the signals.

The second design issue was due to the lack of two high voltage inputs on the uPD16306. When printing it is necessary to connect the jets being fired to the V_{pp} waveform for the first half of the print cycle and then the V_{ss} waveform for the second half. During the first half, when the V_{pp} waveform pulses positive, ink is sucked into the jet from the ink reservoir. As the V_{pp} waveform returns to zero volts, the ink is pushed out of the jet. Then the jet is connected to the V_{ss} waveform which pulses negative at this time to push more ink out of the jet and on to the paper. The uPD16306's output voltage range is 0 to 80 volts with respect to ground. Since the outputs can only be switched between one positive high voltage output and ground, it is necessary to connect the V_{pp} waveform to the high voltage input and V_{ss} to the ground input. During the print cycle, when the V_{pp} waveform pulses, the V_{ss} waveform is at zero volts. The jets being driven are connect to V_{pp} during this period while the unused jets are connected to V_{ss}. After the V_{pp} pulse is complete, it remains at zero volts and the V_{ss} signal pulses negative. At this point the jets being

driven are connected to the V_{ss} waveform and the non-firing jets are connected to V_{pp}. This sequence results in the jets used during that print cycle being connected to the print voltage waveform and the unused jets remaining at zero volts throughout the print cycle. Because the voltage at the ground pin on the uPD16306 is always equal to or below that at the V_{pp} pin, the chip will function correctly. The difficulty with this idea lies with the CMOS level inputs. The digital voltage supply and the control signals cannot be more than six volts above the voltage at the ground pin. When V_{ss} pulses negative, the digital voltage supply and the control signals must follow this waveform negative in order to avoid burning out the chip by having more than six volts across the digital inputs. In order to accomplish this, V_{dd} and the control signals arelevel-shifted to ride above the V_{ss} waveform. V_{dd_s}, the level shifted version of V_{dd}, is connected to the digital voltage supply pin of all of the CMOS chips that have their ground pins connected to V_{ss}. The shifted V_{dd} waveform, V_{dd_s}, appears as shown in figure 1.5.

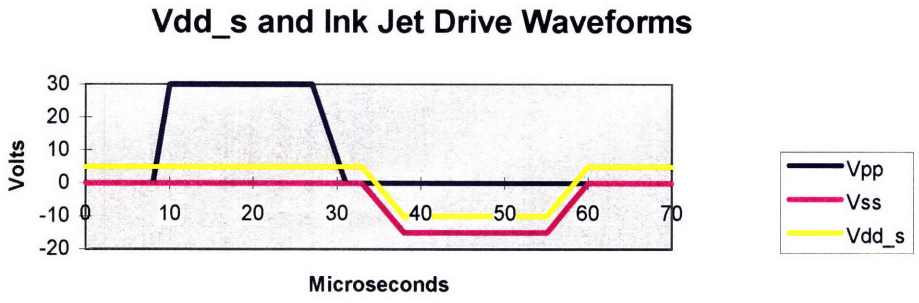


Figure 1.5

In addition to these two main design issues, a simple test fixture was designed to facilitate testing the head drive board's functionality.

Interface PAL

2.1 HDA

The HDA is controlled with four control signals (shift, cnten, polarity, select) and a clock. SHIFT is a positive true shift enable for the 33 bit long data shift register. Shifting starts one clock pulse after asserting SHIFT and stops one clock pulse after de-asserting SHIFT. One of the data or calibration latches may be loaded one clock after the de-assertion of SHIFT based on the levels of the three other control lines at the time that Shift is de-asserted. Table 2.1 shows the truth table for the HDA's control logic.

CNTEN	SELECT	POLARITY	LATCH LOADED
0	0	X	Data
0	1	X	None
1	0	0	Calibration Bit 0
1	0	1	Calibration Bit 1
1	1	0	Calibration Bit 2
1	1	1	Calibration Bit 3

Table 2.1

CNTEN, POLARITY, and SELECT along with the data latched at each output, control the high voltage outputs. Each output can be connected to either V_{pp}, V_{ss}, or ground. The truth table follows for the high voltage outputs is shown in table 1.2. "Open" after an output state indicates that it will be open after the calibration counter reaches the value stored in the calibration latch for that output. The rising edge triggered clock input is used for shifting serial data, incrementing the calibration counter, and synchronizing the other control input pins.

CNTEN	SELECT	POLARITY	DATA LATCH	OUTPUT
0	0	0	X	Vss
0	0	1	X	Vpp
0	1	0	0	Vss
0	1	0	1	Vpp
0	1	1	0	Vpp
0	1	1	1	Vss
1	0	0	0	Vss(open)
1	0	0	1	Vpp
1	0	1	0	Vpp(open)
1	0	1	1	Vss
1	1	0	0	Vss
1	1	0	1	Vpp(open)
1	1	1	0	Vpp
1	1	1	1	Vss(open)

Table 2.2

2.2 UPD16306

The uPD16306 is controlled with three control signals (/PC, /STB, BLK) and a clock. Data is shifted in on the falling edge of the clock signal. The three control lines are not registered at the inputs. Table 2.3 shows the truth table for the control logic of the uPD16306.

DATA	/STB	BLK	/PC	OUTPUT
X	X	1	1	All High
X	X	1	0	All Low
1	0	0	1	High
1	0	0	0	Low
0	0	0	1	Low
0	0	0	0	High
X	1	0	1	Latch's Data Output
X	1	0	0	Latch's Data Output (inv)

Table 1.3

2.3 Interface PAL Implementation

The interface PAL must accept the control signals intended for the HDA and translate them in order to correctly drive the uPD16306. Since the HDA shifts on the rising edge of the clock and the uPD16306 works on the falling edge of the clock. The control lines can be latched into the PAL on the rising edge of the shift clock and propagate through quickly enough to meet the setup times for the uPD16306. The control signals coming onto the board are latched into the PAL at the rising edge of the clock. Then there is a propagation delay before the output signals reach the uPD16306. If the uPD16306s are clocked with the same signal that clocks the PAL, then the set-up and hold times of the control signals to the inputs of the uPD16306 will not be symmetrical. The set-up times will be much smaller than the hold times. In order to alleviate this problem, the clock signal is routed through the PAL before it reaches the uPD16306. This delays the clock and makes the set-up and hold times more symmetrical. Since all of the inputs to the uPD16306 pass through the interface PAL, the speed of the PAL is not important. The PAL selected for the design, AMD™ PALCE16v8Q-15, was the best value based on the part's cost, power usage, and speed. This device costs less than one dollar each, uses 55mA when the clock is pulsed at 55 mA, and has a propagation delay of 15ns. The available parts with lower power usage and a slower propagation delay were considerably more expensive.

There are two main sections to the interface PAL. A state machine controls the shift register and combinational logic determines the high voltage output state. After the last data bit is shifted in the shift registers of the uPD16306s it needs to be latched into the outputs before the next clock cycle. Otherwise the data will be shifted too far. The HDA's shift register is enabled and disabled through the use of the SHIFT signal. Thus, when all of the data is shifted to the correct location, SHIFT goes low. Then on the next clock cycle, the data is latched. Further clock transitions do not affect the shift register, but are required because all of the control line inputs are registered. A simple state machine was designed that uses the clock and the SHIFT signal to determine when to latch the data from the shift register to the output latches. The uPD16306 cannot disable its shift register. The data is

shifted at every negative edge of the clock. Therefore, once the data is in the correct location, it must be strobed to the output. The output latches are data through when the /STB signal is low. To latch the correct data and not be affected by future clock edges. The /STB signal must be forced low to send the data to the output latches. Then it must go high before the shift register shifts again. Figure 2.1 shows a state diagram for this section of the interface PAL.

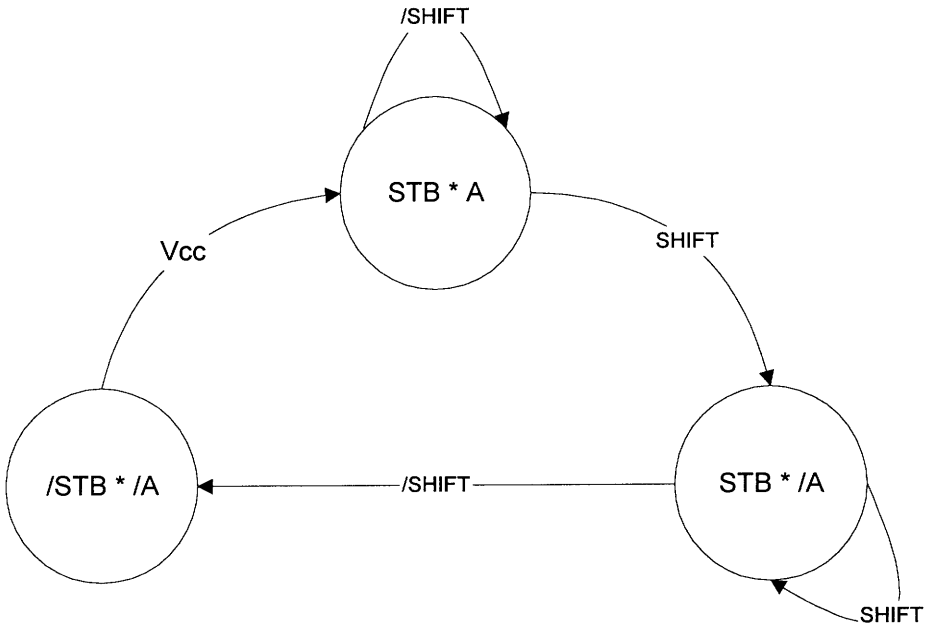


Figure 2.1

Table 2.4 shows how the remaining control signals were translated:

INPUTS				OUTPUTS	
SHIFT	CNTEN	SELECT	POLARITY	/PC	BLK
X	0	0	0	0	1
X	0	0	1	1	1
X	0	1	0	1	0
X	0	1	1	0	0
X	1	0	0	1	0
X	1	0	1	0	0
X	1	1	0	1	0
X	1	1	1	0	0
1	X	X	X	X	X

Table 2.4

Verilog Simulation of Interface PAL

3.1 System Module

In order to verify that all of the set-up and hold times for the uPD16306 would be met and that the correct data would be shifted in, a verilog simulation was completed that modeled the PAL, uPD16306, and the system inputs to these devices. Figure 3.1 shows a block diagram of the components of the verilog system module.

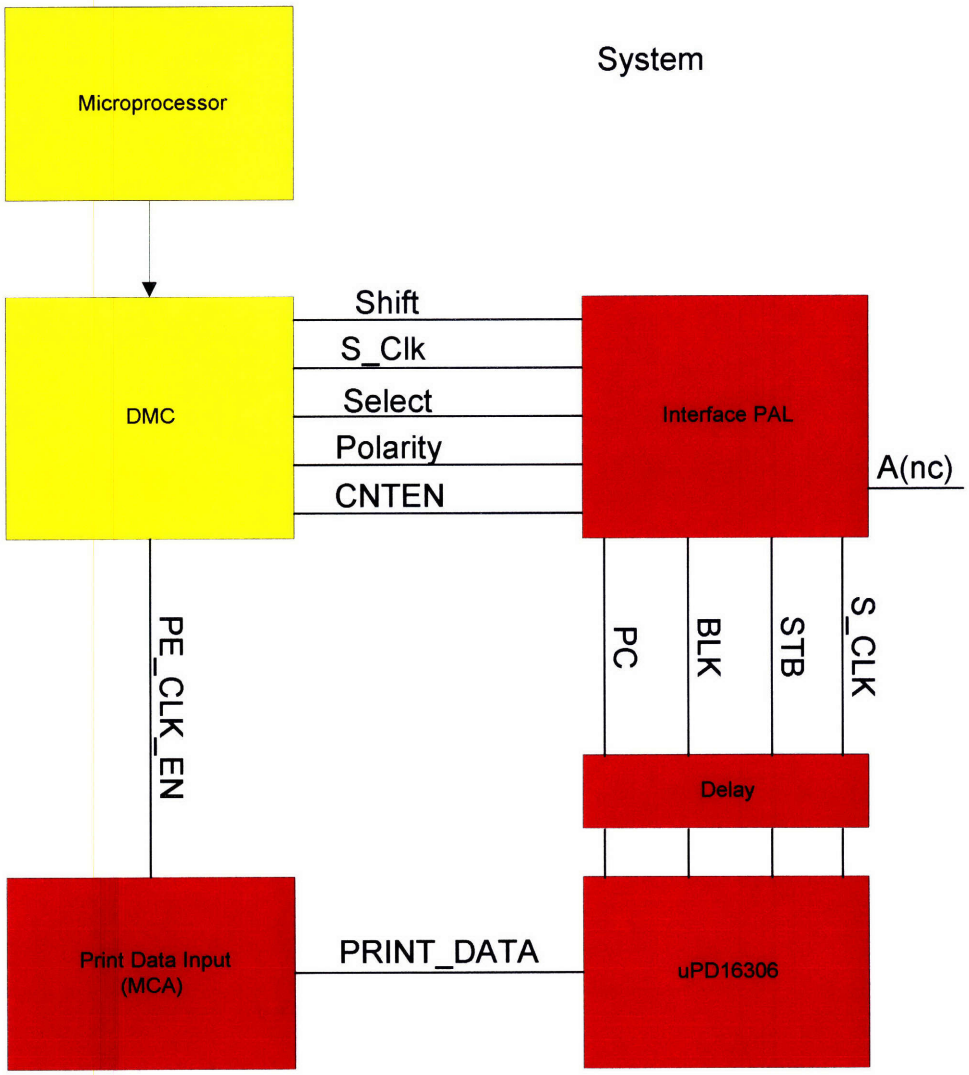


Figure 3.1

A model of the ASIC that sends the control signals to the board (DMC) and the printers main processor was already in existence and being used at Tektronix™. The microprocessor model involves the use of software that allows it to be programmed using PCL (Postscript Command Language) code. The model for the PAL was created automatically from the JEDEC code and a standardized model of a particular PAL device. The existing models were used along with the created models to simulate the system. The verilog code for the system module and the models for each of the subcomponents except the DMC and the microprocessor is included in the appendix.

3.2 Microprocessor and DMC

The print process in the Phaser 340 is controlled by a print engine microprocessor. The microprocessor controls the DMC (Digital Motion Control) which in turn controls the print head driver board. A complete model of the microprocessor is in general use at Tektronix. This model is programmed by creating PCL files. Files containing the microprocessor command code to model the print process of the printer were already in existence for another type of simulator. These simulations were converted into PCL code and then used to test the system for proper performance.

3.3 MCA

Although a verilog model for the MCA(Memory Control Asic) was also readily available, this simulation was only concerned with a small portion of the MCA's functionality. It was easier to create a simplified model of the MCA to simulate its communication with the head drive board than to set up the complete model. The MCA supplies the print data to the head drive board from the RAM in serial form. The DMC tells the MCA when to supply the next data bit with the pe_clk_en control

line. Thus a sequence of data bits can be simulated cycling a variable using pe_clk_en as the clock signal.

3.4 Interface PAL

The verilog simulation of the interface PAL was created using a standard model for the Intel I85C220 PAL. Verilog uses this standard model and the JEDEC command file used to program the PAL to model the device. The original development of the interface PAL was carried out using design software for an INTEL™ part. The actual PAL used in the design is the AMD™ PALCE16V8Q-15. Functionally, they are equivalent parts.

3.5 Delay

For the purposes of this simulation, the particular PAL used is not important. What is important is the propagation delay through the device. Instead of creating separate verilog models to try PALs with different propagation times, a delay block was created. The signals passing through the delay block are delayed to simulate different clock to Q times of various PALs.

3.6 UPD16306

The purpose of these simulations is to insure that all of the setup and hold times of the UPG16306 high voltage driver ICs are met. Thus, the model for this chip does not have to simulate the device's functionality. Instead the model must check the setup and hold times for all of the control signals and the data line.

3.7 System

The previously described modules are integrated at the top layer with the system verilog file. Each of the modules are instantiated in this file, and the timing format is set. When the system module is run, a plot file showing the activity of all of the signals is generated and the setup and hold times of the uPD16306 are verified. No timing violations were discovered when the simulation was run. The plots generated by the simulation were useful for debugging the design.

Digital Supply Level Shifting

The digital supply voltage of the CMOS chips with their ground pins connected to V_{ss} must be held at five volts above V_{ss} to prevent the chips from being damaged. This is accomplished by level shifting the supply voltage relative to V_{ss}. This shifted voltage supply is used to drive the uPD16306s and one CMOS octal buffer.

The frequency of the V_{ss} pulse during printing never rises above 11kHz. Although, the frequency components of the corners of the V_{ss} pulse are much higher than 11kHz, the design does not have to follow the corners of the pulse exactly to protect the CMOS parts. Since a voltage difference of greater than six volts is required to damage the chips, the corners of the shifted waveform can be rounded provided the shifted waveform does not reach more than six volts above the voltage at the ground pin of the chips (V_{ss}). There for the transistor chosen for this level shifting circuit does not need to be a high speed part.

Power dissipation is a major design factor. The digital supply level shifting circuit must be able to supply all of the uPD16306s and a CMOS octal buffer used in the signal level shifting circuit with current. This results in a current load of approximately 40mA. In order to save board space and minimize cost, surface mount components would be ideal. However, the SOT-23 packages common for most surface mount transistors can only dissipate .225W of continuous power. Since V_{ss} may drop as low as -30V . The amount of current that can be driven through a surface mount transistor used to accomplish the level shifting is very limited. Therefore a high voltage transistor capable of dissipating .5W of was chosen

The design of this level shifting circuit (Figure 4.1) involves the use of a pnp transistor as a current source driving a zener diode with a breakdown voltage of 5.1V This circuit is both simple and inexpensive. As long as the zener is constantly biased on, noise from the diode should not be an issue. Additionally, the zener is relatively insensitive to current variations. Thus different current loads will not effect the regulation of the zener as long as it remains biased. Since the only system parameter that changes is V_{ss}, the only speed limitation will be the rate at

which the collector voltage can change. This is limited by the output capacitance of the transistor. At this current level and transition speeds, the effect of this capacitance is minimal relative to the frequency of the V_{ss} signal.

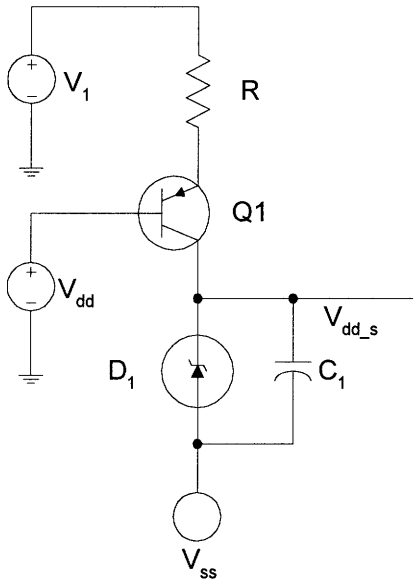


Figure 4.1

In order to keep Q_1 in the forward active region, V_1 must be greater than V_{dd} by at least .4V. When V_{ss} is at zero volts the emitter of Q_1 must be at least V_{sat} (collector to emitter saturation voltage) above the zener breakdown voltage of the diode for the transistor to function correctly as a current source. V_{sat} is the. Additionally, it is desirable to make V_1 high enough to minimize the changes in I_c caused by variations in the characteristic V_{be} of individual transistors.

A couple of factors preclude using this design for level shifting the digital voltage supply line to shift the logic control lines. First, when a zener's breakdown voltage is reached, the diode creates a significant amount of noise. This, plus their turn on time, makes zener diodes undesirable for high speed switching applications. Second, this design requires a dc to dc converter in order to supply V_1, which must be higher than V_{dd} as mentioned in the previous paragraph. Since V_{dd_s} is only driving a few CMOS parts and the zener does not require much current to remain biased on, the converter does not need to supply more than about 30mA.

However there are three control lines, a data line, and a clock signal to be level shifted. If the dc to dc converter were asked to supply current to five more level shifting circuits that use this transistor-zener design, then the current load would be greatly increased.

DC-DC Converter

5.1 Converter Design

Because V_{dd} is the highest DC voltage supplied to the head drive board by the printer, it is necessary to convert V_{dd} to a higher voltage on the board in to support the V_{dd} level shifting circuit. This was accomplished by using a monolithic DC-DC converter. The Motorola MC34063 was selected as an inexpensive and simple to use choice. Figure 5.1shows the schematic for the circuit used to convert 5VDC to 9VDC. The internal subsystems of the MC34063 are drawn inside the outline of the chip to give a clearer picture of how the circuit functions.

The converter works by dumping energy into the inductor when the driving transistor is on and then dumping this energy into the output capacitor in series with V_{in} when the driving transistor is turned off. Thus V_{out} can be any value greater than V_{in} as determined by the duty cycle of the transistor.

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right) + V_{in}$$

The manufacturer provides the following equations to determine the values of the external components based on the desired performance.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_e - V_{in}}{V_{in} - V_{sat}}$$

$$t_{on} + t_{off} = \frac{1}{f_{min}}$$

$$C_t = 4 * 10^{-5} t_{on}$$

$$I_{pk} = 2I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

$$L_{min} = \left(\frac{V_{in} - V_{sat}}{I_{pk}}\right) t_{on}$$

$$I'_{pk} = \left(\frac{V_{in} - V_{sat}}{L_{min}}\right) t_{on}$$

$$R_{sc} = \frac{.33}{I'_{pk}}$$

$$C_o \approx \frac{I_{out}}{V_{rp-p}} t_{on}$$

$$V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right)$$

$$I_b = \frac{I_{pk}}{B_f}$$

$$I_{170} = \frac{V_{be}}{170}$$

$$V_{rsc} = R_{sc} I_{pk}$$

$$R_{driver} = \frac{V_{in} - V_{sat} - V_{rsc}}{I_b + I_{170}}$$

5.2 Convertor component selection

The previous equations were entered into an Excel spreadsheet to determine the best values to use for the external components. After examining the current requirements for the components that would draw from the shifted Vdd signal, the converter was designed to supply 40mA at 9V. The results of these calculations are shown in table 5.1

R_1	2,200Ω
R_2	13,640Ω
C_t	222pF
L_{min}	173uH
R_{sc}	1.8Ω
R_{dr}	484Ω
C_o	15uF

Table 5.1

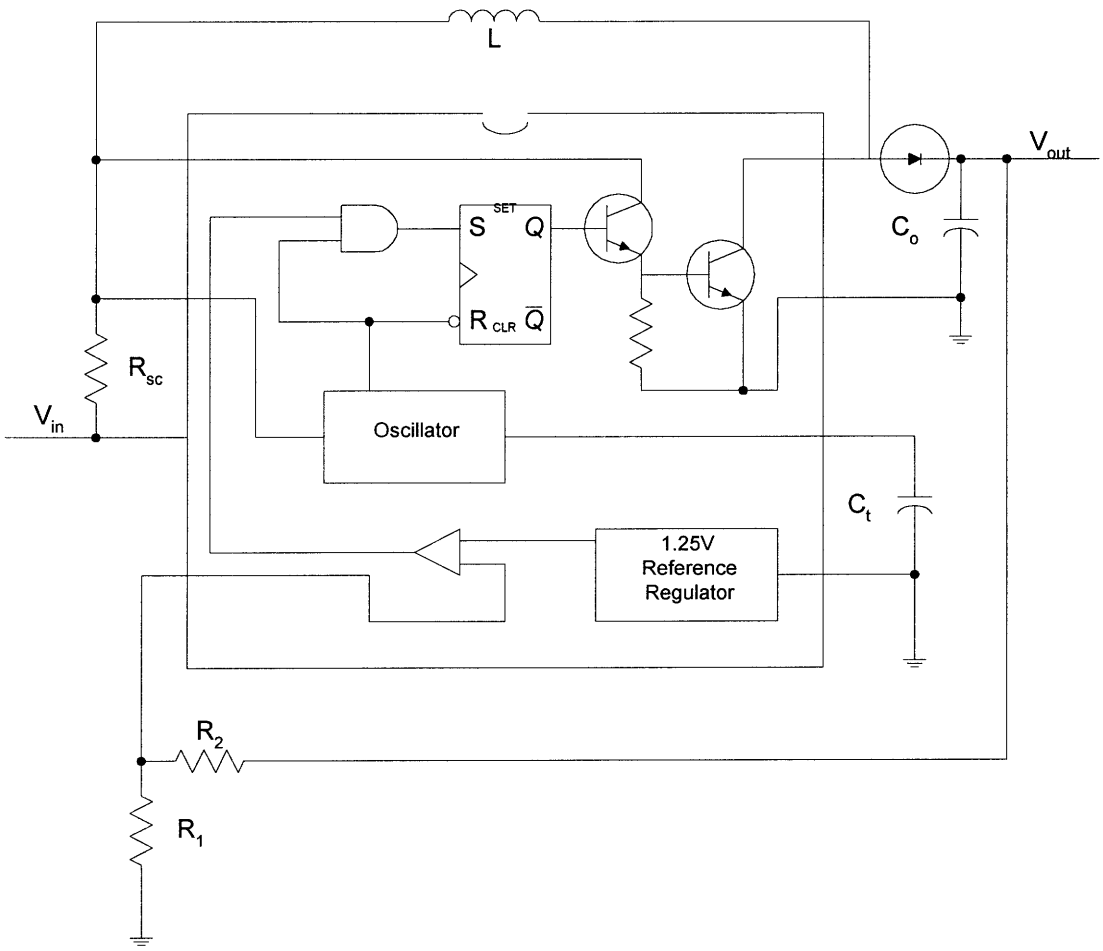

L
V_{out}
SET
S
Q
R CLR
$\overline{Q}$
C_o
R_{sc}
V_{in}
Oscillator
C_t
1.25V
Reference
Regulator
R_2
R_1

Figure 5.1

Signal Level-Translation

6.1 Introduction

The same design constraints exist for the signal level shifting that exist for the digital voltage supply level shifting. However speed is much more of an issue because these signals change states. Not only must the output ride above V_{ss}, but it must change quickly to follow the input. This need for speed is driven by two factors. First of all, the control signals to the uPD16306 are combinational while the control line inputs on the HDA are registered. The slower the rise and fall times are for the level shifting, then the more variation is to be expected. Currently, there is enough delay between different signal changes, that race conditions are not a concern. However, a problem may arise if one of the level shifter circuits is significantly faster than the others. Second, the shift register is driven at 8 MHz. Due to the nature of the proposed interface PAL (as will be described later) only 1/2 of this clock signal is available to make setup times. This leaves the system with only 60ns to work with. In order to insure a stable signal at the clock edge, the target rise time of the level shifting is 6ns (10% of 60ns). Due to the compounded effects of parasitics, the design should be as simple and use as few parts as possible. The circuit shown in figure 6.1 was selected because of its simplicity and inexpensive cost. The buffers used in this circuit are ACT devices. ACT logic chips have TTL level inputs and CMOS level outputs. By using output buffers with TTL level inputs, the collector of the pnp transistor only needs to be above 2V to make the output buffer (B_2) go high. To make the buffer's output go low, the collector of the pnp transistor only needs to go below .8V. This allows the signal level shifting circuit to use V_{dd} instead of requiring a higher voltage. The base voltage was chosen to be 3.3V in order to keep the transistor in the active region. The base voltage is created with the use of a 3.3V zener diode. The important voltages for this circuit during one print cycle with a high input are shown in figure 6.2.

This circuit cannot be used for the digital voltage supply level shifting because the output buffer, B2, must have a shifted digital voltage supply in order to use V_{ss} as ground and not be damaged.

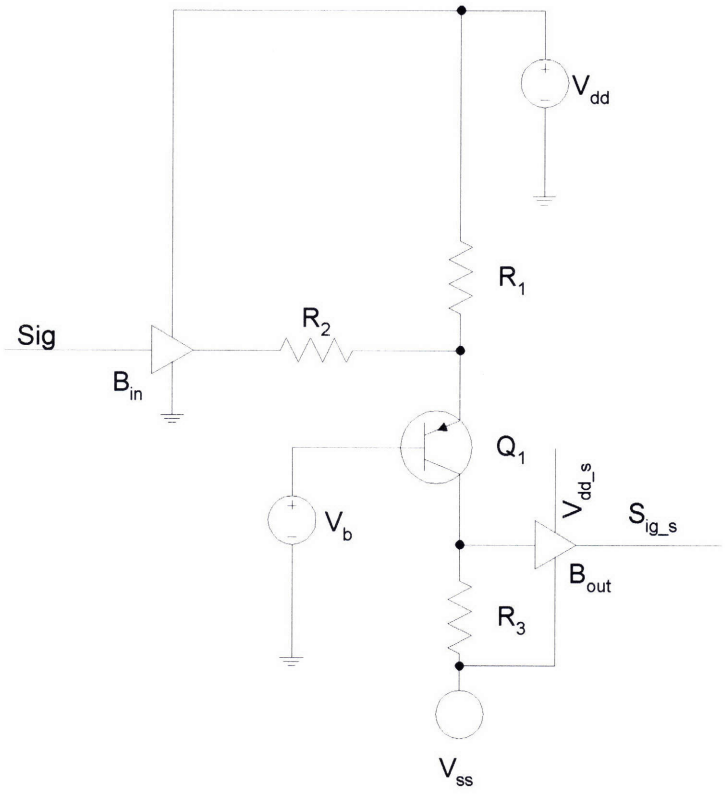


Figure 6.1

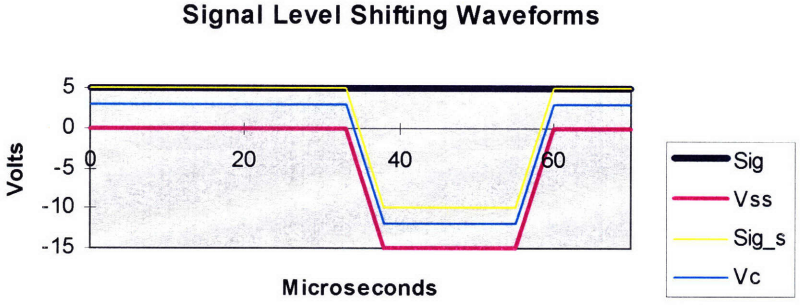


Figure 6.2

Not only do the input attributes of the buffer eliminate the need for a voltage greater than V_{dd}, the TTL input levels provide better noise immunity. Noise may cause a CMOS buffer to trigger several times as its input changes because CMOS logic triggers at 2.5V. However, provided the noise on the signal is smaller than about 1.2V the TTL inputs should protect from any instability problems.

The rise and fall times of the transistor are the speed limiting factors in this circuit. The buffers have rise and fall times on the order of 1 to 3 ns. The junction capacitances of the transistor make it necessary to use very small resistance values in order to achieve a transition time on the order of 6ns. This is particularly true of R_3. The base to collector capacitance, input capacitance of the buffer, and R_3 make up the largest portion of the time constant for the circuit. Small resistance values require larger currents in order to produce the required voltage. Thus the resistor size is limited by the power dissipated across the PNP transistor. This is the primary trade off to be made in this circuit.

6.2 Mathematical Analysis of Level Shifting Circuitry

A simple linear model was used to determine the large signal values of the circuit. Using iterative methods it is possible to incorporate nonlinearities caused by variations in V_{ce} and V_{be}; however, these variations are no greater than those caused by device variations. These variations will not cause more than a few tenths of a volt which will not greatly affect the attributes of the system. Using the basic linear model:

$$V_e = V_b + V_{be}$$

$$I_e = \frac{V_{dd} - V_e}{R_1} + \frac{V_{in} - V_e}{R_2}$$

$$I_c \approx I_e$$

$$V_{out} = I_c R_3 + V_s$$

6.3 Power Consumption

Since the input buffer to the level-shifting circuit will always be either high or low there are only two states to consider for power consumption. When V_{in} is low, the transistor will be near cutoff, and very little current will be flowing through the device. Thus our only concern is when V_{in} is high. When V_{in} is held high:

$$P = V_{ce} * I_c$$

The power dissipated across the transistor goes up linearly as V_{ss} decreases. Thus the worst case calculation for power dissipated in the transistor:

$$P_{max} = V_{cemax} * I_c$$

Since I_c is directly dependant on the value of R_3, the power dissipation of the Vdd level shifting circuit can be plotted verses the value of R_3 as in figure 6.3.

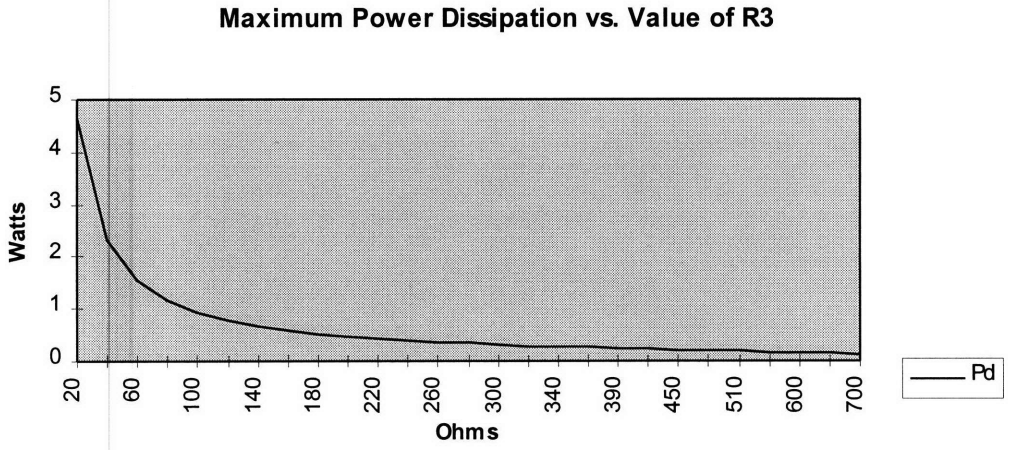


Figure 6.3

Fortunately V_{ss} does not spend most of its time at its minimum value. V_{ss} drops below 0V only during printing in the 300dpi print mode. When printing, this

waveform repeats periodically with a duty cycle of .22. Thus the actual amount of power dissipated in the transistor is approximately:

$P_{printing} = .22 V_{cemax} * I_c$

In order to use the sot-23 surface mount package for the transistor, which is the most inexpensive version, the power dissipated accross the device must be kept below .225W.

6.4 Small Signal Model

In order to calculate the rise and fall time of the signal level-shifting, the small signal model must be evaluated. C_u(the base to collector capacitance), C_π, (the base to emitter capacitance), and C_{bin}(the input capacitance of the output buffer are the three parasitic capacitances of concern.

Figure 6.4 shows the hybrid-pi model for the entire circuit

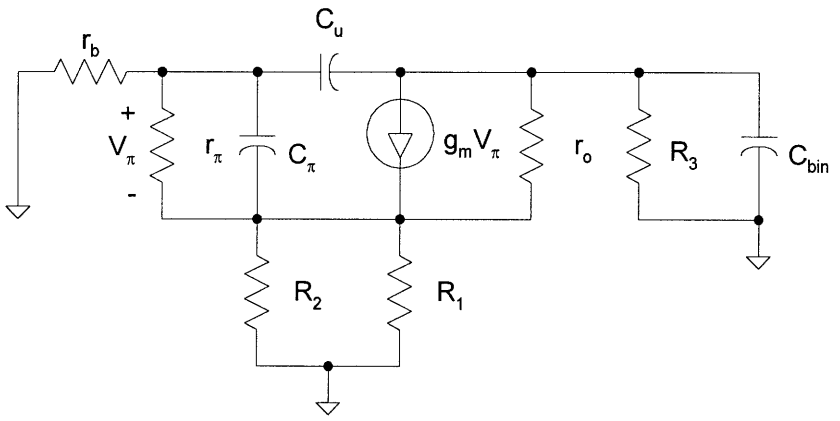
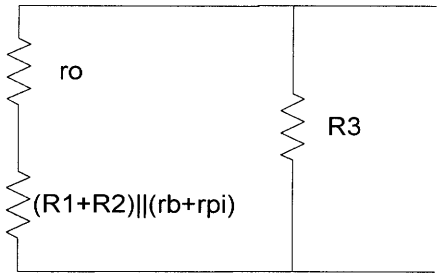


Figure 6.4

Due to the complexity of the circuit the method of open circuit time constants is used here. First the resistance seen by C_{bin} is determined. The hybrid-pi model reduces to:



$$R_{cbin} = R_3 \| (r_o + ((R_1 + R_2) \| (r_b + r_\pi))) \approx R_3$$

Next, the resistance seen by C_u is determined. The reduced hybrid-pi model is shown in figure 6.5.

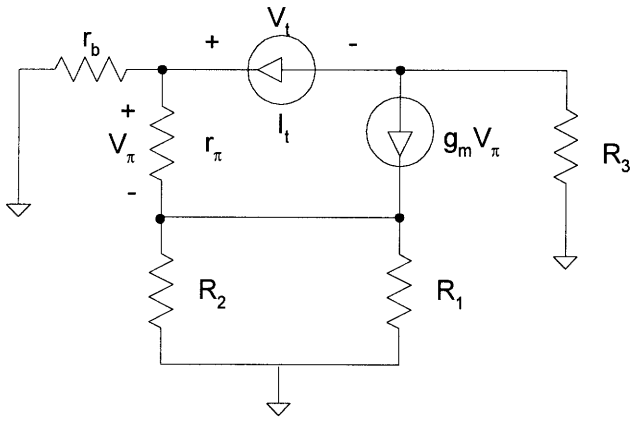


Figure 6.5

In order to simplify the calculations, the model can be redrawn as shown in figure 6.6 (Gray and Meyer 208).

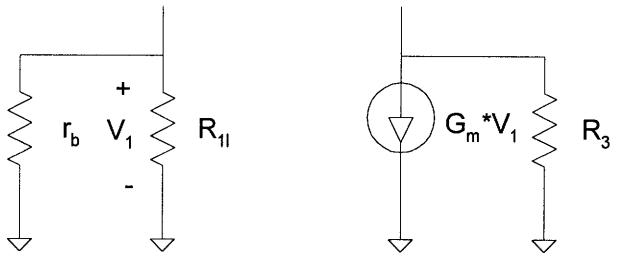


Figure 6.6

$$R_{il} = r_\pi(1 + g_m * R_3)$$

$$G_m = \frac{g_m}{1 + g_m * R_3}$$

$$R_{cu} = r_b \| R_{il} + R_3 + G_m * R_3 * r_b \| R_{il}$$

$$R_{cu} = r_b \| r_\pi(1 + g_m * r_3) + R_3 + \frac{R_3 * g_m * r_b \| r_\pi * (1 + g_m * R_3)}{1 + g_m * R_3}$$

Finally, the resistance seen by C_{pi} must be determined. The hybrid-pi model reduces figure 6.7.

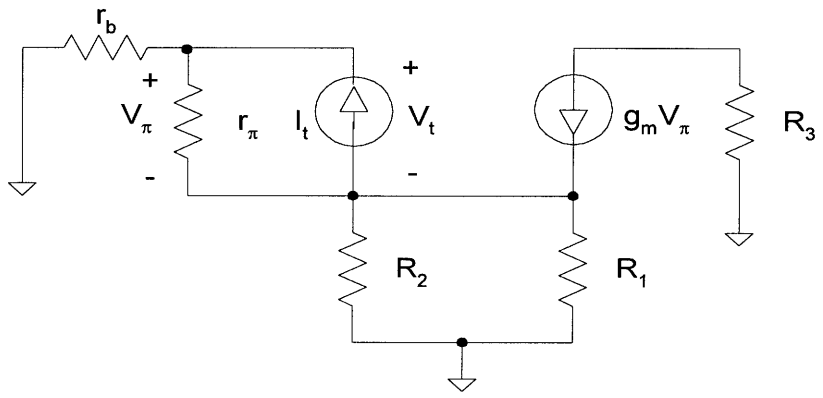


Figure 6.7

$$V_t = V_b - V_a$$

$$V_t = i_2 * r_\pi$$

$$V_a = -i_1 * R_1 \| R_2$$

$$V_b = i_3 * r_b$$

$$V_t = i_3 * r_b + i_1 * R_1 \| R_2$$

$$V_t = r_b * (i_t - i_2) + i_1 * R_1 \| R_2$$

$$V_t = r_b * \left(i_t - \frac{v_t}{r_\pi} \right) + i_1 * R_1 \| R_2$$

$$i_1 = \frac{V_t - r_b * \left(i_t - \frac{V_t}{r_\pi} \right)}{R_1 \| R_2}$$

$$I_t = i_3 + i_2$$

$$I_t = g_m * V_t + i_1 + i_2$$

$$I_t = g_m * V_t + i_1 + \frac{v_t}{r_{pi}}$$

$$I_t = V_t \left(g_m + \frac{1}{r_\pi} \right) + i_1$$

$$I_t = V_t * \left(g_m + \frac{1}{r_\pi} \right) + \frac{V_t - r_b * \left(I_t - \frac{V_t}{r_\pi} \right)}{R_1 \| R_2}$$

$$(R_1 \| R_2) * I_t = (R_1 \| R_2) * V_t * \left(g_m + \frac{1}{r_\pi} \right) + V_t - I_t * r_b + V_t * \frac{r_b}{r_\pi}$$

$$(R_1 \| R_2) * I_t + r_b * I_t = (R_1 \| R_2) * V_t * \left(g_m + \frac{1}{r_\pi} \right) + V_t + V_t * \frac{r_b}{r_\pi}$$

$$I_t (R_1 \| R_2 + r_b) = V_t * \left(R_1 \left\| R_2 * \left(g_m + \frac{1}{r_\pi} \right) + 1 + \frac{r_b}{r_\pi} \right. \right)$$

$$\frac{V_t}{I_t} = R_{th} = \frac{R_1 \| R_2 + r_b}{\left(R_1 \| R_2 * \left(g_m + \frac{1}{r_\pi} \right) + 1 + \frac{r_b}{r_\pi} \right)} = R_{c\pi}$$

$$R_{c\pi} = \frac{r_\pi * (R_1 \| R_2 + r_b)}{\left(r_\pi * R_1 \| R_2 * \left(g_m + \frac{1}{r_\pi} \right) + r_\pi + r_b \right)}$$

$$R_{c\pi} = \frac{r_\pi * (R_1 \| R_2 + r_b)}{r_\pi * R_1 \| R_2 * g_m + R_1 \| R_2 + r\pi + r_b}$$

$$R_{cpi} = r_\pi \left\| \frac{(R_1 \| R_2 + r_b)}{1 + g_m * R_1 \| R_2} \right.$$

These values can be used to approximate the -3dB point using the method of open circuit time constants. This methods approximates the system using a single pole that is equal to the sum of the R-C values calculated previously. Thus for this circuit:

$$f_{-3dB} \approx \frac{1}{2pi(R_{c\pi}C_{\pi} + R_{cu}C_m + R_{cb}C_b)}$$

It is possible to calculate the rise time on the circuit based upon the single pole assumption. A single pole system has the following transfer function:

$$H(s) = \frac{V}{1 - \frac{s}{RC}}$$

Where V is the low-frequency gain and RC is the approximated single pole. Solving for Vo:

$$Vo(s) = V * V_i\left(\frac{1}{s} - \frac{1}{s - RC}\right)$$

The circuit response to a small voltage step:

$$Vo(t) = V * V_i\left(1 - e^{-RCt}\right)$$

This previous calculation assumes that the voltage step is small enough that the system can be considered linear. Since this circuit will go from cutoff to well into the linear region, this assumption is not strictly true. However, since the transistor does not go into saturation, and we are interested in the 10%-90% rise and fall times, this approximation should still result in a value that can be used to design the circuit. Next we determine the relative time values:

$$.1V * V_i = V * V_i(1 - e^{-RCt_1})$$
$$.9V * V_i = V * V_i(1 - e^{-RCt_2})$$

6.4 Nodal Analysis

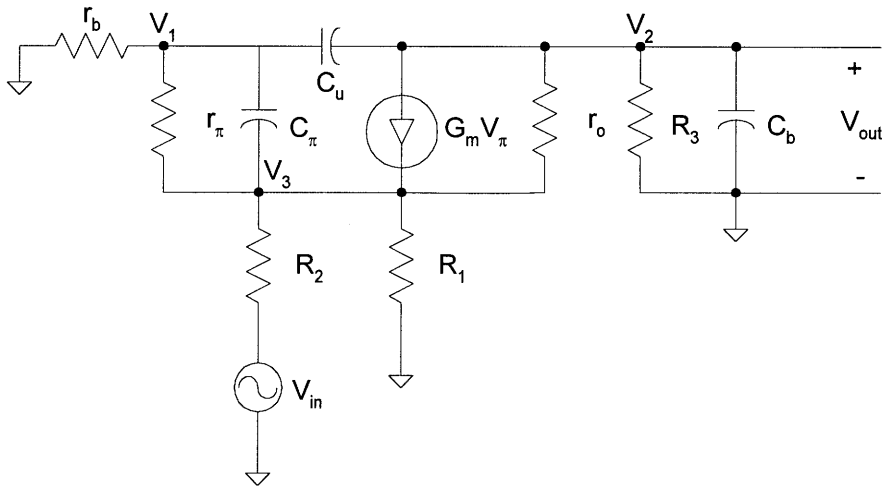


Figure 6.9

Further insight can be gained about the level shifting circuit by using nodal analysis. By performing KCL at each of the labeled voltage nodes on the small signal model in figure 6.9, we can determine the components of the following matrix equation:

$$(\mathbf{G} + s\mathbf{C})U = \mathbf{V}$$

$$\mathbf{G} = \begin{bmatrix} G_b + G_\pi & 0 & -G_\pi \\ G_m & G_o + G_3 & -G_m - G_o \\ -G_\pi - G_m & -G_o & G_2 + G_\pi + G_1 + G_m + G_o \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} C_\pi + C_u & -C_u & -C_\pi \\ -C_u & C_u + C_b & 0 \\ -C_\pi & 0 & C_\pi \end{bmatrix}$$

$$\mathbf{C}^{-1} = \begin{bmatrix} \frac{C_u + C_b}{C_u C_b} & \frac{1}{C_b} & \frac{C_u + C_b}{C_u C_b} \\ \frac{1}{C_b} & \frac{1}{C_b} & \frac{1}{C_b} \\ \frac{C_u + C_b}{C_u C_b} & \frac{1}{C_b} & \frac{C_u C_\pi + C_\pi C_b + C_u C_b}{C_u C_b C_\pi} \end{bmatrix}$$

$$\mathbf{V} = \begin{bmatrix} V_1 & V_2 & V_3 \end{bmatrix}$$

$$\mathbf{U} = \begin{bmatrix} 0 & 0 & V_{in}G_2 \end{bmatrix}$$

Using Cramer's rule, we can determine the transfer function for V_{in} and V_{out}.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{V_2(s)}{V_{in}(s)} = \frac{\begin{vmatrix} G_b + G_\pi + s(C_{pi} + C_u) & 0 & -G_\pi - sC_\pi \\ -G_m - sC_u & 0 & -G_m - G_o \\ -G_{pi} - G_m - sC_\pi & V_{in}(s)G_2 & G_2 + G_\pi + G_1 + G_m + G_o + sC_\pi \end{vmatrix}}{|(\mathbf{G} + s\mathbf{C})|V_{in}(s)}$$

The results of this nodal analysis can be transformed to a state-space form which simplifies further analysis of the circuit.

$s\mathbf{X} = \mathbf{AX} + \mathbf{BU}$

Where $\mathbf{X}=\mathbf{V}$, $\mathbf{I}=\mathbf{U}$, $\mathbf{A}=-\mathbf{C}^{-1}\mathbf{G}$, and $\mathbf{B}=\mathbf{C}^{-1}$.

These values can then be used to determine the natural frequencies of the circuit. In the nodal equation formulation the natural frequencies are the values of s that make $\mathbf{G}+s\mathbf{C}=0$. This equation can be rewritten as:

$-\mathbf{A}+s=0$

The natural frequencies are the eigenvalues of **A**. The results from evaluating this equation are too complex to list here. However, all of the poles turn out to be in the left half plane. Thus the system is stable.

Once the models were completed, they were entered into an Excel® spreadsheet. Potential values for R_1, R_2, and R_3 were then examined for their effects on the performance of the circuit. By setting the required bias points for V_{out}, only the value of one of the resistors is independent. The values of the other two resistors follow from the equations.

The following equations result from solving for R_1 and R_2 in terms of R_3, V_{out} in the high state, and V_{out} in the low state:

$$R_1 = \frac{R_3}{V_{oh} - \frac{(V_{oh} - V_{ol})}{5}}$$

$$R_2 = \frac{5R_3}{V_{oh} - V_{ol}}$$

With $V_{oh} \approx 3V$ and $V_{ol} \approx 0V$ and $R_3=150\Omega$, $R_2=250\Omega$, and $R_3=62.5\Omega$. Since the value of R_3 has the greatest effect on the rise time of the circuit, it was selected first in order to achieve a predicted rise time of about 6ns. The values for R_1 and R_2 followed.

The transistor selection was based on its maximum collector to emitter voltage and the values of its parasitic capacitances. In general, these two values are inversely proportional. Based on these considerations, the Motorola BC856ALT1 was selected. According to the manufacture, it has a maximum collector to emitter voltage is 60V. The maximum value for the output capacitance of the transistor is given as 4.5pF.

With these resistor values the transistor's bias current is approximately 18mA. When Vss is at -30V, the power dissipated accross the transistor is .56W. However, since the duty cycle of the Vss pulse is .22, the time averaged power dissipated accross the transistor is about .12W. The estimate rise time using the method of open circuit time constants is 6.2ns.

By plugging these values into the results of the nodal analysis, we can generate a bode plot for the V_{out} in terms of V_{in} as shown in figure 6.10.

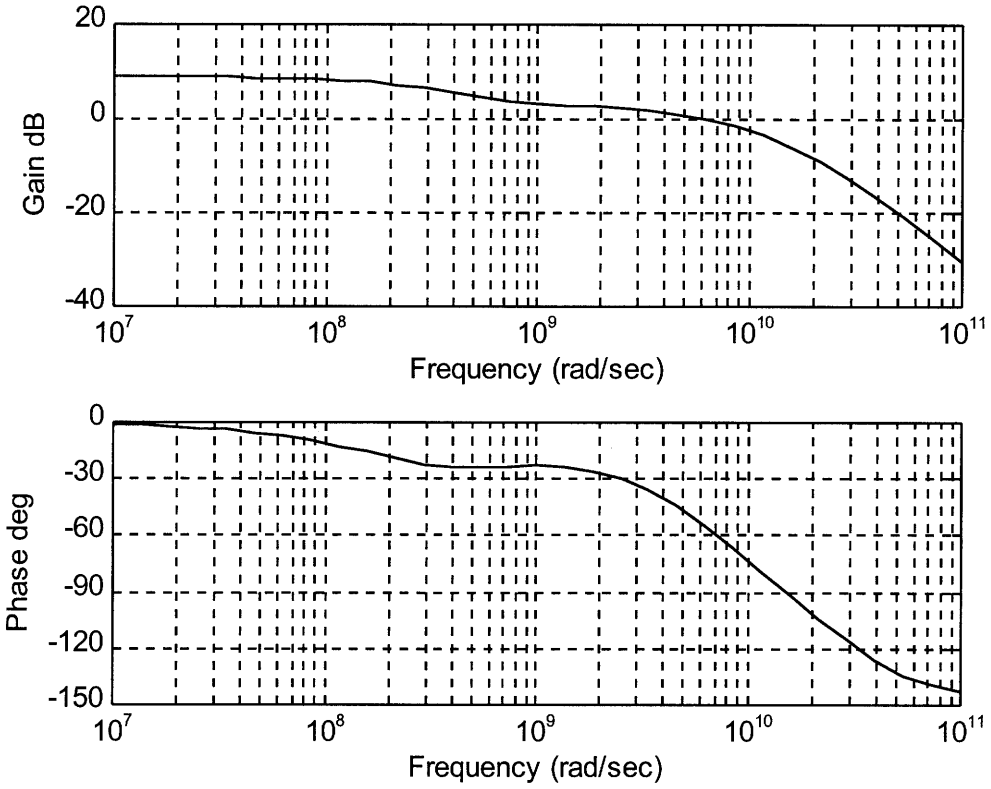


Figure 6.10

Thus the nodal analysis predicts a rise time of approximately 5ns.

6.5 Prototyping

Once the models were completed, several prototype circuits were constructed using different transistors in order to test the validity of the calculations. The first prototypes were constructed using a breadboard and then tested. The following component values were selected because they were readily available: R_1=50Ω, R_2=180Ω, R_3=110Ω. The measured circuit parameters for these prototypes are shown in table 6.1.

	t_r(ns) measured	t_r(ns) calculated	C_{cb}(pf)	V_{oh} measured	V_{oh} calculated
2N5087	20	3.7	4	2.7	2.7
MPS6523	20	3.3	3.5	2.6	2.7
2N5401	17	8	10	2.6	2.7
2N3906	19	4	4.5	2.6	2.7
MPSH69	20	1	0.3	2.7	2.7

Table 6.1

In order to minimize parasitic capacitances caused by using a bread board, the first prototypes were built directly on to a copper plate that acted as the ground plane. The circuit parameters measured for these prototypes are shown in table 6.2.

	t_r(ns) measured	t_r(ns) calculated	C_{cb}(pf)	V_{oh} measured	V_{oh} calculated
2N5401	11	8	10	2.6	2.7
2N3906	8	4	4.5	2.6	2.7
MPSH69	3	1	0.3	2.7	2.7

Table 6.2

These results were much closer to the predicted value.

Finally, to accurately model the use of surface mount parts, several prototypes were built using different surface mount parts. The parts were glued directly to a piece of fr-5. Copper tape was used to create a ground plane. A photograph of one of these prototypes is included. Table 6.3 shows the results of these experiments.

	t_r(ns) measured	t_r(ns) calculated	C_{cb}(pf)	V_{oh} measured	V_{oh} calculated
MMBT3906	4	4	4.5	2.7	2.7
BC856ALT1	6	4	4.5	2.7	2.7

Table 6.3

These results matched the calculations well. In general C_{cb} was provided as a graph verses V_{ce} in the manufacturer's specification. The worst case value for C_{cb} was used in these calculations.

Test Fixture

A simple test fixture was built to facilitate the testing of the head drive board (Figure 8.1). The fixture has a switch for each of the logic inputs and a DPDT spring back switch for manual clock pulses. The clock switch uses a debounce circuit to prevent multiple clock pulses from resulting from pressing the button once. The fixture uses a self contained 9V AC to DC converter. The 9V is then lowered to 5V with a National Semiconductor 7805 three terminal voltage regulator. The outputs are connected to a connector with holes were wires from the board can be placed. The wires are held in place with individual set screws.

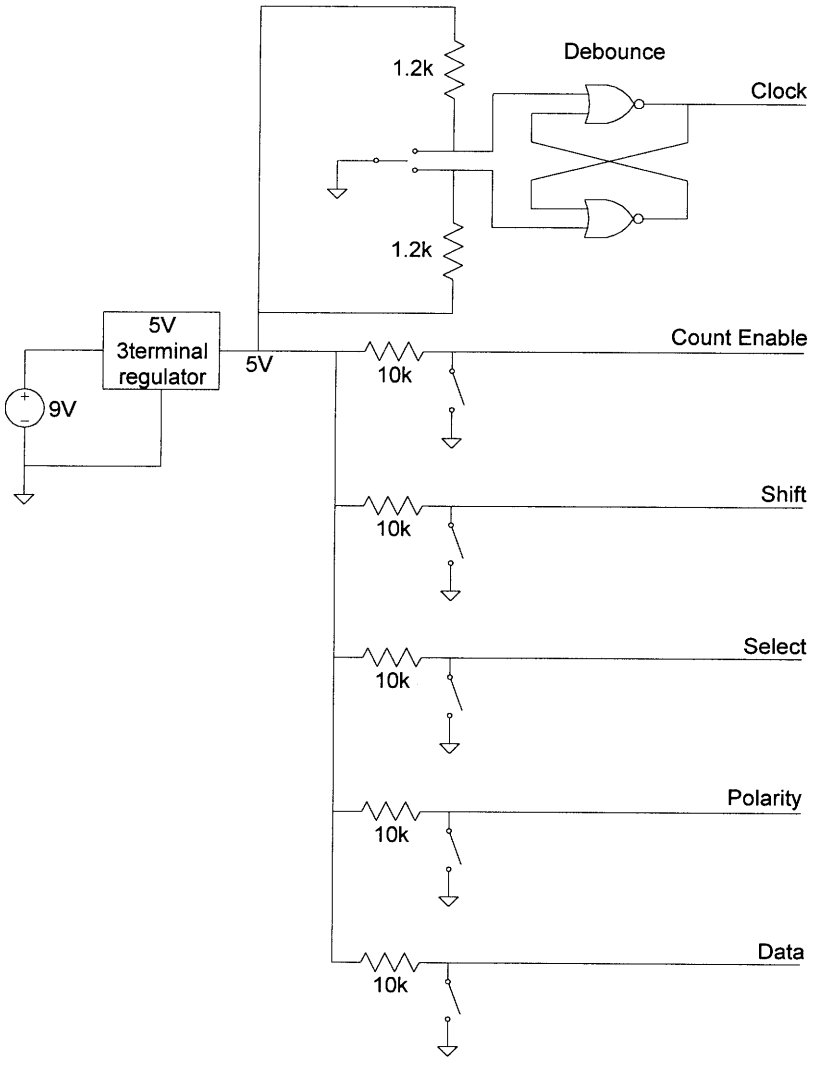


Figure 8.1

Schematic Capture and Board Layout

Once the initial design was completed, the circuit schematics were entered into the Cadence™ design package using schematic capture. The schematics followed the form of the original schematics as much as possible. Figure 9.1 shows the components of the head drive board.

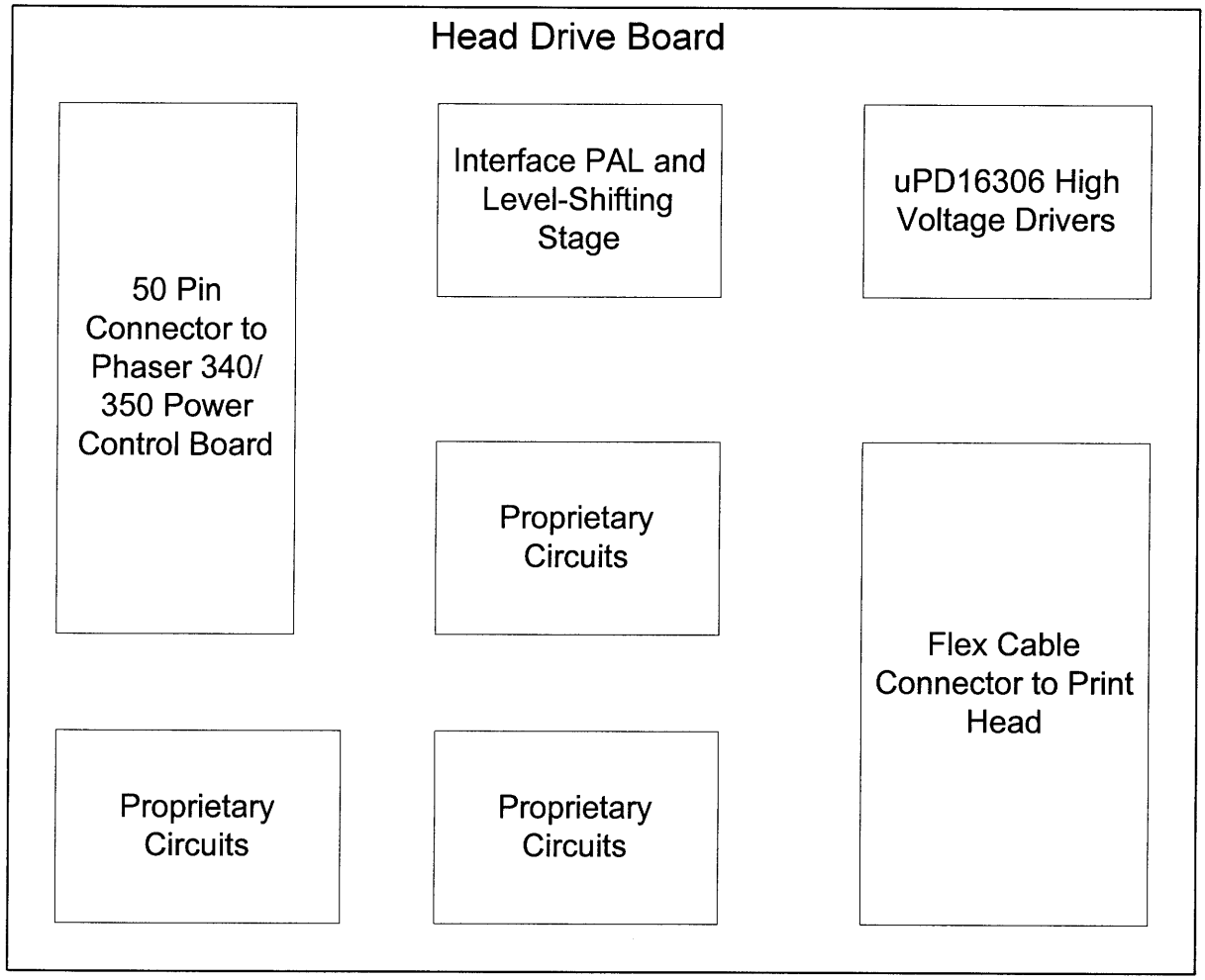


Figure 9.1

The head drive board is connected directly the power control board with a 50 pin connector. All of the control signals from the main controller board pass through the power control board on their way to the head drive board. Also, the high voltage

print waveforms are amplified in the power control board.

The interface PAL and level shifting stage encompass most of the design for this project. The control, clock, and data signals are translated and level shifted in this stage. The digital supply voltage going to the high voltage drivers, V_{dd_s} is also level shifted here.

The flex connector connects the high voltage output pins on the head drive board to the ink jets on the print head.

After drawing the schematic using the Cadence design tools several diagnostic checks were run through the software package to check for errors. The software runs several checks to insure that all ground and power nodes are connected properly, all part attributes are specified, and no signal lines are shorted.

Once the design passed this stage a netlist was generated. This netlist was used by a circuit board layout engineer to complete the board design. In order to insure that the new head drive board is an exact replacement for the old board, the original layout design was used as a basis for this design. The old parts were deleted and the new parts were added automatically by the software using the netlist. Due to the large number of connections, the layout software was unable to route the connections automatically. Instead the layout engineer hand routed all of the connections.

The level shifting and dc to dc converter circuitry required special attention during the layout process. In order to minimize the affects of parasitics, the components of each of the five signal level shifting circuits were placed close together. The external components of the dc to dc converter circuit were kept close to the MC34063 in order to minimize noise problems and to keep the high current connections very short to minimize emf noise. Most signal lines are 12 mils in width, all high current signals, power, and ground lines are 24 mils in width. The only signal lines 24 mils wide are the connections to the inductor used in the dc to dc conversion circuit.

In order to have room for all of the signal paths, the both versions of the head drive board are composed of four layers. There are three signal layers and one ground plane layer. A picture of each of the layers is included in the appendix.

Before outsourcing the board designs for prototype production, a buildability

meeting was held with several manufacturing engineers to ensure that the design did not have the potential for any manufacturing problems. Because the new board is very similar to the old head drive board, the design was passed easily. The only changes suggested by the manufacturing engineers involved the addition of test points.

Once each of the current head drive boards are stuffed, they are tested using a custom test fixture. The fixture uses a bed of nails to probe the outputs of the board during the test. The functionality of every portion of the board is tested. Since the fixture only deals with the inputs and outputs of the head drive board, this same test fixture will be used to test the new boards. If a board fails, the incorporation of test points connected to internal signals on the board makes it easier to determine the location of the problem.

The board design files were outsourced to a board manufacture who produced fourteen boards. The empty boards were then returned to Tektronix, where all the parts were mounted to the board using high speed machinery.

Results

10.1 Print Head Drive Board Debugging and Test Fixture Evaluation

The prototype boards were examined for visible flaws, and then the power connections were checked for voltage shorts before powering up the board. Next the board was powered up and the interface PAL was checked by manually changing the control signals. Once a modification wire connecting the PAL's output enable pin to ground was added, the PAL functioned properly.

The work up to this point was completed at Tektronix' printer manufacturing site in Wilsonville, Oregon. The remaining characterization was completed at MIT. Only one board was available for testing.

The test fixture previously mentioned was used to supply V_{dd} and the control signals to the board. The manual clock was used to check that the design worked correctly.

The test fixture's V_{dd} was measured at 4.98V DC. 40mV of noise was measured on the V_{dd} line. When the high frequency noise was blocked out, the waveform shown in figure 10.1 was evident on top of the digital voltage supply.

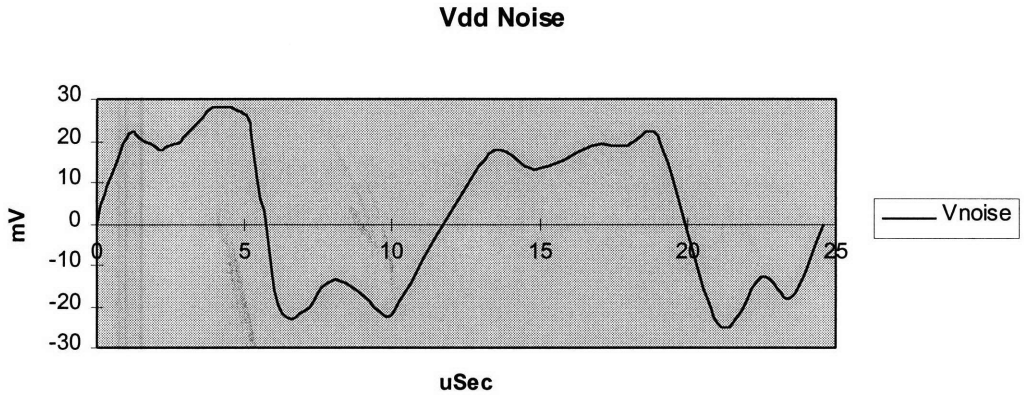


Figure 10.1

This noise signal propagated through much of the head drive board.

10.2 Dc to Dc Conversion

The voltage step-up converter circuit was designed to provide 9V at 37mA. The output voltage was measured to be 8.9V. This slight difference could be the result of variation of several circuit paramaters such as switching frequency and inductance value. The switching speed was measured by measuring the voltage across the timing capacitor and the schottky diode. The voltage waveform shown in figure 10.2 appeared accross the timing capacitor:

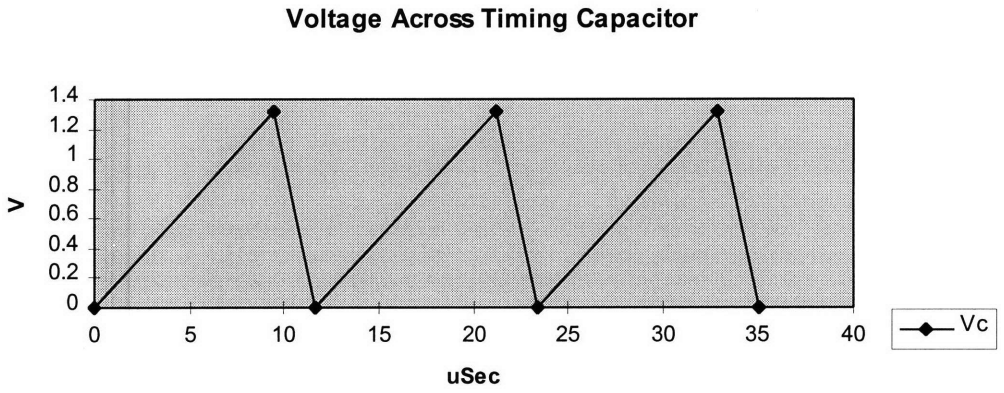


Figure 10.2

The switching frequency was designed to be 90KHz during the design with the duty cycle equal to .5. The measured frequency was 85KHz. This difference is most likely caused by the timing capacitor's 10% tolerance and a slightly higher output current than expected. Figure 10.3 shows the waveform measured at pin 1 of the MC34063.The duty cycle was .5 as designed. The ripple on the output voltage was designed to be 50mV. It was measured at 45mV.

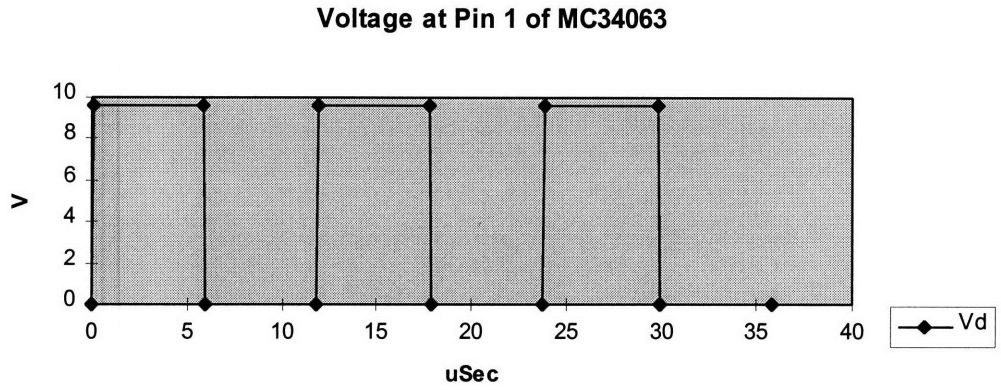


Figure 10.3

10.3 Digital Supply Level Shift

The digital supply level shifting circuit was designed to provide a voltage 5.1V above V_{ss}. The output voltage was measured at 5.17V. This variation is solely due to the diode's zener breakdown voltage and is well within the specifications provided by Motorola™. The base-emitter voltage of the level shifting transistor was measured to be .8V. The noise signal measured from the V_{dd} supply was present on $V_{dd\text{-}s}$ signal; however, the noise signal did not cause any problems for this circuit.

10.4 Signal Level Shift

The bias points of the signal level shift circuit are highly dependent on transistor characteristics. This variation is inconsequential as long as V_{ol}<.8V and V_{oh}>2V. The circuit was designed to provide at least a 50% margin of error for both of these requirements. V_{ol} was designed to be near 0V and V_{oh} was designed to equal 3V. Not only does this provide margin of error to compensate for part tolerances, the rise and fall times between the transition voltages is decreased if the circuit is designed to go beyond these transition voltages. Assuming that the base to emitter voltage equals .7V, the circuit values were selected so that V_{ol}=0V and V_{oh}=3V. The values measured are shown in table 10.1.

	Measured	Designed
V_b	3.27	3.3
V_{eh}	3.98	4
V_{el}	3.91	4
V_{inh}	4.91	5
V_{inl}	0.15	0
V_{oh}	2.97	3.1
V_{ol}	0.26	0.01

Table 10.1

With the exception of the low state output voltage all of the values are within .1 volts of the designed values. The errors can be easily explained. One source of error is the output voltage of the CMOS buffers, which serves as the input for the level shifting circuit. The buffers are not able to drive their output completely to the supply rails. Thus the measured high value of the buffers was 4.91V and the low value was .15V. This is within the specification provided by Motorola™. The other source of error comes from the base to emitter voltage of the transistor used to accomplish the level shifting. This value was assumed to equal .7V. However, depending on the collector current, this value is specified by Motorola™ to range from .6V to .9V. Often the relationship between the base to emitter voltage and the collector current of a transistor is modeled with a logarithmic relationship. The following equation is used:

$$I_c = I_s\left(e^{\frac{Vbe}{Vt}} - 1\right)$$

Where I_s is the reverse saturation current and V_t is equal to .026V at 25°C. Instead of providing I_s, Motorola™ supplies a chart showing V_{be} vs. I_c. This plot shows that the relationship is almost logarithmic.

If the values of the model are changed to reflect the measured values of Vb, Vin, and Vbe more accurate values result as shown in table 10.2

	Measured	Designed
Vb	3.27	3.27
Veh	3.98	3.98
Vel	3.91	3.91
Vinh	4.91	4.91
Vinl	0.15	0.15
Voh	2.97	3
Vol	0.26	0.3

Table 10.2

10.5 Noise

The noise waveform present on V_{dd} is also present at the input to the level shifting circuit. The circuit amplifies the noise at the output. The noise measured on V_{oh} was equal to 158mV. Thus the noise signal was amplified approximately by a factor of three. This amplification was predicted by the Bode plot included in the description of the signal level shifting design. This noise signal did not affect the circuit's performance. Because the head drive board was not tested while being used on an actual printer, the board's noise immunity may not be as good as measured. The 158mV of noise that was generated as a result of the noise signal present on the Vdd supplied by the test fixture did not cause any problems; however, if the noise signal had been a factor of three larger, the circuit may not have performed correctly. Further testing in conjunction with actual printers is underway at Tektronix™.

10.6 Rise Times

A 1MHz clock pulse was used to examine the rise times of each of the elements of the level shifting circuit. 1MHz was chosen because it was the highest frequency square wave that could be produced by the available signal generator. Table 10.3 shows the measurements taken.

	T_{rise}(ns)	V10%	V90%	Overshoot
PAL	3.5	0.38	3.38	none
Input Buffer	2.62	0.49	4.41	0.75
Level shift	7.24	0.55	2.67	0.1
Output Buffer	3.4	0.51	4.6	0.45

Table 10.3

The predicted rise time for the PAL was 6.15ns. This calculation did not take into account the capacitance of the scope probe or the rise time of the oscilloscope. If 15pF is added to the input capacitance of the output buffer to compensate for the capacitance of the oscilloscope probe, then the predicted rise time changes to 11.1ns. This value is almost twice the measured value. The accuracy of the prediction is seen to be even worse if the rise time of the oscilliscope is used to adjust the measured rise time.

$$t_{r\text{ - scope}} = \frac{.35}{150\text{MHz}} = 2.33\text{ns}$$

$$t_{r\text{ - measured}} = \sqrt{(t_{r\text{ - scope}})^2 + (t_{r\text{ - actual}})^2}$$

$$7.24\text{ns} = \sqrt{5.43\text{ns}^2 + (t_{r\text{ - actual}})^2}$$

$$t_{r\text{ - actual}} = 6.9\text{ns}$$

Thus the calculated value for the rise time of the level shifting circuit is off by a factor
of 2. This is to be expected due to the linear approximations used by the transistor models and the values used. The transistor small signal model was designed to be used as a linear small signal approximation. As the input signals leave the small signal region, the nonlinear nature of the system becomes more evident. Additionally, the parasitic values used in the model were worst case values provided by the manufacturer. It is likely that these values are actually smaller than the worst case. In any case, the transistor models did provide a rise time figure of merit that

was important to the design process.

10.7 Conclusion

The head drive board tested met the design requirements established for the board. It correctly functions as a drop in replacement for the original head drive board and costs considerably less. However, further testing is necessary with a larger sample of boards tested in printers. Although the noise present in the board tested, it is unknown if noise will be a problem when the board is used in the printer because a printer was not available when this board was tested. At the time of this paper, engineers at Tektronix™ are evaluating this print head drive board design for its reliability.

APPENDIX A
PALASM Code and Simulation

```
TITLE          INTERFACE PAL
REVISION         2
AUTHOR           GARY GILL
COMPANY           TEKTRONIX
DATE           9/4/96

OPTIONS  TURBO=ON
      SECURITY=OFF

CHIP   HEAD_INTERFACE  I85C220

PIN        CLK
PIN        SHIFT
PIN        CNTEN
PIN        SELECT
PIN        POLARITY
PIN        PC
PIN        BLK
PIN        STB
PIN        A
PIN        DATA_IN
PIN        DATA_OUT
PIN        CLK_DELAY_OUT
; State Machine Controlling STB

STATE
MOORE_MACHINE
DEFAULT_BRANCH S1

; State Assignments
S1 = /STB * /A ;mod 10-16
S2 = STB * A
S3 = STB * /A
S4 = /STB * A

; State Transitions
S1 := VCC -> S2
S2 := SHIFT -> S3
  + /SHIFT -> S2
S3 := /SHIFT -> S4
  + SHIFT -> S3
S4 := VCC -> S1
```

```
EQUATIONS
CLK_DELAY_OUT = CLk
PC.CLKF      = CLK
BLK.CLKF     = CLK
STB.CLKF     = CLK
A.CLKF       = CLK
DATA_OUT.CLKF = CLK

T_TAB(SHIFT CNTEN SELECT POLARITY :>> PC.D BLK.D)

X 0 0 0 : 0 1
X 0 0 1 : 1 1
X 0 1 0 : 1 0
X 0 1 1 : 0 0
X 1 0 0 : 1 0
X 1 0 1 : 0 0
X 1 1 0 : 1 0
X 1 1 1 : 0 0
1 X X X : X X

T_TAB(DATA_IN :>> DATA_OUT)

0 : 0
1 : 1


SIMULATION
SETF /CLK /SHIFT /POLARITY /CNTEN /SELECT /DATA_IN
PRLDF /STB /A /BLK /PC /DATA_OUT
TRACE_ON CLK CNTEN SELECT POLARITY SHIFT STB BLK A PC DATA_IN
DATA_OUT CLK_DELAY_OUT

; First a simple check of the combinational logic

CLOCKF CLK
CLOCKF CLK

SETF /CNTEN /SELECT /POLARITY
CLOCKF CLK

SETF /CNTEN /SELECT POLARITY DATA_IN
CLOCKF CLK

SETF /CNTEN SELECT /POLARITY /DATA_IN
```

```
CLOCKF CLK

SETF /CNTEN SELECT POLARITY
CLOCKF CLK

SETF CNTEN /SELECT /POLARITY DATA_IN
CLOCKF CLK

SETF CNTEN /SELECT POLARITY /DATA_IN
CLOCKF CLK

SETF CNTEN SELECT /POLARITY
CLOCKF CLK

SETF CNTEN SELECT POLARITY DATA_IN
CLOCKF CLK

SETF SHIFT /DATA_IN
CLOCKF CLK

SETF /SHIFT
CLOCKF CLK
CLOCKF CLK
TRACE_OFF
```

APPENDIX B
Verilog Simulation Code

System.v

```
`timescale 1 ns / 10 ps

//      define clock period
`define PERIOD  30
`define UNITDELAYLIB

`define PALMODEL
file=/tools/complibData/lmc_r40b/special/cds/verilog/historic/i85c220.v
`uselib file=mc68330.v file=dmc_asic.v file=mca.v file=upd16306.v file=delay2.v
`PALMODEL

module sys ;

        tri1 pulled_high ;
        tri0 pulled_low ;
        wire buf_cpu68_clk;
        buf #2(buf_cpu68_clk, p_clk16);

        wire [15:0] pin_data ;
        wire [15:8] pin_dat ;
        wire [19:0] pin_addr ;
        reg  [15:0] dead_reg ;
        reg  sys_clk ;
        reg  cpu_clk ;
        wire pin_sys_clk_in = sys_clk;
        reg  sys_rst_n ;
        wire pin_trst = sys_rst_n;
        wire reset_68k_n;
        buf ( reset_68k_n, sys_rst_n );
        wire lwe_n ;
        wire uwe_n ;
        wire as_n ;
        wire modck; pulldown ( modck );
        wire bram_enable_n; pulldown (bram_enable_n );
        wire avec; pullup ( avec );
        wire berr; pullup ( berr );
        wire halt; pullup ( halt );
        wire irq1; pullup ( irq1 );
        wire irq2; pullup ( irq2 );
        wire irq3; pullup ( irq3 );
        wire irq4; pullup ( irq4 );
        wire irq5; pullup ( irq5 );
        wire irq7; pullup ( irq7 );

        wire pin_y_sin; pullup ( pin_y_sin );
```

```
        wire pin_y_cos; pullup ( pin_y_cos );
        wire pin_y_cl_n; pullup ( pin_y_cl_n );
        wire pin_spare_sin; pullup ( pin_spare_sin );
        wire pin_spare_cos; pullup ( pin_spare_cos );
        wire pin_spare_cl_n; pullup ( pin_spare_cl_n );
        wire pin_proc_sin; pullup ( pin_proc_sin );
        wire pin_proc_cos; pullup ( pin_proc_cos );
        wire pin_proc_cl_n; pullup ( pin_proc_cl_n );
        wire pin_misc_cl_n; pullup ( pin_misc_cl_n );
        wire pin_x_sin; pullup ( pin_x_sin );
        wire pin_x_cos; pullup ( pin_x_cos );
        wire pin_xa_in1; pullup ( pin_xa_in1 );
        wire pin_xa_in2; pullup ( pin_xa_in2 );
        wire pin_xb_in1; pullup ( pin_xb_in1 );
        wire pin_xb_in2; pullup ( pin_xb_in2 );
        wire pin_mca_data_in; pullup ( pin_mca_data_in );
        wire pin_ext_ac_sdin; pullup ( pin_ext_ac_sdin );
        wire pin_auxt_type1; pullup ( pin_auxt_type1 );
        wire pin_auxt_type2; pullup ( pin_auxt_type2 );
        wire pin_auxt_option; pullup ( pin_auxt_option );
        wire pin_auxt_paper_out; pullup ( pin_auxt_paper_out );
        wire pin_auxt_cl_n; pullup ( pin_auxt_cl_n );
        wire pin_spare_flagin1; pullup ( pin_spare_flagin1 );
        wire pin_spare_flagin2; pullup ( pin_spare_flagin2 );

    wire pin_tck; pullup ( pin_tck );
    wire pin_tms; pullup ( pin_tms );
    wire pin_tdi; pullup ( pin_tdi );
      wire pin_bram_cs_n; pullup( pin_bram_cs_n );

// Pullups added 10 Oct
        wire p_ac_in1; pullup (p_ac_in1);
        wire p_ac_in2; pullup (p_ac_in2);
        wire p_ac_in3; pullup (p_ac_in3);
        wire p_ac_in4; pullup (p_ac_in4);
        wire p_ac_in5; pullup (p_ac_in5);
        wire p_ac_in6; pullup (p_ac_in6);
        wire p_ac_in7; pullup (p_ac_in7);
        wire p_ac_in8; pullup (p_ac_in8);
        wire p_ac_in9; pullup (p_ac_in9);
        wire p_aux_climit; pullup (p_aux_climit);
        wire pin_auxt_opt; pullup (pin_auxt_opt);
        wire p_fbcm; pullup (p_fbcm);
        wire p_fbyk; pullup (p_fbyk);
        wire p_l_sense; pullup (p_l_sense);
        wire p_xa_in2; pullup (p_xa_in2);
        wire p_xa_in1; pullup (p_xa_in1);
        wire p_xb_in1; pullup (p_xb_in1);
        wire p_xb_in2; pullup (p_xb_in2);
```

```
 wire chucks_68k_rst; pullup ( chucks_68k_rst );

wire p_ack0_68_n; pullup ( p_ack0_68_n );
wire p_ack1_68_n; pullup ( p_ack1_68_n );

// DMC Instantiation
dmc_asic dmc (
        .p_ac_out1(p_ac_out1),
        .p_ac_out2(p_ac_out2),
        .p_ac_out3(p_ac_out3),
        .p_ac_out4(p_ac_out4),
        .p_ac_out5(p_ac_out5),
        .p_ac_out6(p_ac_out6),
        .p_ac_out7(p_ac_out7),
        .p_ac_out8(p_ac_out8),
        .p_ac_out9(p_ac_out9),
        .p_ack0_68_n(p_ack0_68_n),
        .p_ack1_68_n(p_ack1_68_n),
        .p_adc_mux0(p_adc_mux0),
        .p_adc_mux1(p_adc_mux1),
        .p_adc_mux2(p_adc_mux2),
        .p_adc_muxen_n(p_adc_muxen_n),
        .p_auxt_dir(p_auxt_dir),
        .p_auxt_pwm(p_auxt_pwm),
        .p_bram_cs_n(pin_bram_cs_n),
        .p_cap_heat_n(p_cap_heat_n),
        .p_cink_heat_n(p_cink_heat_n),
        .p_clk16(p_clk16),
        .p_dfan_en(p_dfan_en),
        .p_drum_heat_n(p_drum_heat_n),
        .p_efan_en_n(p_efan_en_n),
        .p_hda_cnten(p_hda_cnten),
        .p_hda_pol(p_hda_pol),
        .p_hda_sel(p_hda_sel),
        .p_hda_shf_clk(p_hda_shf_clk),
        .p_hda_shift(p_hda_shift),
        .p_head_heat_n(p_head_heat_n),
        .p_iic_nv_clk(p_iic_nv_clk),
        .p_irq_n(p_irq_n),
        .p_kink_heat_n(p_kink_heat_n),
        .p_media_heat_n(p_media_heat_n),
        .p_mink_heat_n(p_mink_heat_n),
        .p_pe_clk_en(p_pe_clk_en),
        .p_phase(p_phase),
        .p_proc_clst(p_proc_clst),
        .p_proc_dir(p_proc_dir),
        .p_proc_pwm(p_proc_pwm),
```

```
.p_pwm_p(p_pwm_p),
.p_pwm_s(p_pwm_s),
.p_pwr_lmt(p_pwr_lmt),
.p_pwr_waste_en(p_pwr_waste_en),
.p_ra_heat_n(p_ra_heat_n),
.p_ref(p_ref),
.p_resv_heat_n(p_resv_heat_n),
.p_sclk(p_sclk),
.p_spare_out1(p_spare_out1),
.p_sram_oe_n(p_sram_oe_n),
.p_tdo(p_tdo),
.p_wave_vpp(p_wave_vpp),
.p_wave_vss(p_wave_vss),
.p_wipeaot1(p_wipeaot1),
.p_wipeaot2(p_wipeaot2),
.p_wipebot1(p_wipebot1),
.p_wipebot2(p_wipebot2),
.p_xaout1(p_xaout1),
.p_xaout2(p_xaout2),
.p_xapwm(p_xapwm),
.p_xbout1(p_xbout1),
.p_xbout2(p_xbout2),
.p_xbpwm(p_xbpwm),
.p_xslopeco(p_xslopeco),
.p_ydir(p_ydir),
.p_yink_heat_n(p_yink_heat_n),
.p_ypwm(p_ypwm),
.p_d_68_15(pin_data[15]),
.p_d_68_14(pin_data[14]),
.p_d_68_13(pin_data[13]),
.p_d_68_12(pin_data[12]),
.p_d_68_11(pin_data[11]),
.p_d_68_10(pin_data[10]),
.p_d_68_9(pin_data[9]),
.p_d_68_8(pin_data[8]),
.p_d_68_7(pin_data[7]),
.p_d_68_6(pin_data[6]),
.p_d_68_5(pin_data[5]),
.p_d_68_4(pin_data[4]),
.p_d_68_3(pin_data[3]),
.p_d_68_2(pin_data[2]),
.p_d_68_1(pin_data[1]),
.p_d_68_0(pin_data[0]),
.p_iic_nv_dio(p_iic_nv_dio),
.p_sda(p_sda),
.aw_13(pin_addr[13]),
.aw_12(pin_addr[12]),
.aw_11(pin_addr[11]),
.aw_10(pin_addr[10]),
```

```
.aw_9(pin_addr[9]),
.aw_8(pin_addr[8]),
.aw_7(pin_addr[7]),
.aw_6(pin_addr[6]),
.aw_5(pin_addr[5]),
.aw_4(pin_addr[4]),
.aw_3(pin_addr[3]),
.aw_2(pin_addr[2]),
.aw_1(pin_addr[1]),
.p_ac_in1(p_ac_in1),
.p_ac_in2(p_ac_in2),
.p_ac_in3(p_ac_in3),
.p_ac_in4(p_ac_in4),
.p_ac_in5(p_ac_in5),
.p_ac_in6(p_ac_in6),
.p_ac_in7(p_ac_in7),
.p_ac_in8(p_ac_in8),
.p_ac_in9(p_ac_in9),
.p_aux_climit(p_aux_climit),
.p_aux_opt(pin_auxt_opt),
.p_aux_pout(pin_auxt_paper_out),
.p_auxttyp1(pin_auxt_type1),
.p_auxttyp2(pin_auxt_type2),
.p_cl_misc(pin_misc_cl_n),
.p_clk32(pin_sys_clk_in),
.p_cs_68_n(p_cs_68_n),
.p_fbcm(p_fbcm),
.p_fbyk(p_fbyk),
.p_l_sense(p_l_sense),
.p_proc_cl_n(pin_proc_cl_n),
.p_proc_cos(pin_proc_cos),
.p_proc_sin(pin_proc_sin),
.p_rst_in_n(pin_trst),
.p_spare_flagin1(pin_spare_flagin1),
.p_spare_flagin2(pin_spare_flagin2),
.p_sz0_68(p_sz0_68),
.p_sz1_68(p_sz1_68),
.p_tck(pin_tck),
.p_tdi(pin_tdi),
.p_tms(pin_tms),
.p_trst(pin_trst),
.p_wr_68_n(p_wr_68_n),
.p_xain1(p_xa_in1),
.p_xain2(p_xa_in2),
.p_xbin1(p_xb_in1),
.p_xbin2(p_xb_in2),
.p_ycl_n(pin_y_cl_n),
.p_ycos(pin_y_cos),
.p_ysin(pin_y_sin)
```

```
);


bufif0 ( pin_data[7], 1'b0, chucks_68k_rst );

microprocessor mot(
        .clkout(),
        .w_(p_wr_68_n),
        .uwe_(uwe_n),
        .lwe_(lwe_n),
        .cs1_(),
        .cs2_(p_cs_68_n),
        .data(pin_data),
        .addr(pin_addr),
        .halt_(),
        .irq6_(p_irq_n),
        .reset_(reset_68k_n),
        .modclk(modck),
        .siz0(p_sz0_68),
        .siz1(p_sz1_68),
        .dsack1_(p_ack1_68_n),
        .dsack0_(p_ack0_68_n),
        .extal(buf_cpu68_clk),
        .berr_()
);

I85C220 pal (
        .INP1 (p_hda_shf_clk),  // clk
        .INP2 (p_hda_shf_clk), // clk combinatorial
        .INP3 (pal_din),  // data from MCA
        .INP4 (p_hda_pol),  // polarity
        .INP5 (p_hda_sel),  // select
        .INP6 (p_hda_cnten),  // cnten
        .INP7 (p_hda_shift),  // shift
        .INP7 (),
        .INP8 (),
        .INP9 (),
        .INP10 (),
        .IO1 (),
        .IO2 (),
        .IO3 (clk_delay_pal),
        .IO4 (pal_dout),
        .IO5 (pc_pal),
        .IO6 (blk_pal),
        .IO7 (stb_pal),
        .IO8 (a)
);
/* parameters for the pal model */
defparam pal.COMPONENT = "I85C220-7"; // timing version of part
```

```
defparam pal.JEDECFILE = "head.jed";  // name of jedec file

reg print_data;

delay2 delay1 (
        .clk_in (clk_delay_pal),
        .stb_in (stb_pal),
        .blk_in (blk_pal),
        .pc_in (pc_pal),
        .print_data_in (pal_dout),
        .stb_out (stb),
        .blk_out (blk),
        .pc_out (pc),
        .print_data_out (pal_dout),
        .clk_out (shift_clk)
);


upd16306 necpart (
        .stb (stb),
        .blk (blk),
        .pc (pc),
        .s_clk (shift_clk),
        .print_data (pal_dout)
);

mca mca (
        .pe_clk_en (p_pe_clk_en),
        .mca_dout (pal_din)
);




        initial begin
                sys_clk = 0 ;
                forever #(`PERIOD/2) sys_clk = ~sys_clk ;
        end

initial
  begin
        force sys.dmc.cpu_io.reset_cntr_tmp_0   = 1'b0 ;
      #100
        release sys.dmc.cpu_io.reset_cntr_tmp_0 ;
  end
*/

        /* set the format for timing data in the simulator */
        initial $timeformat( -9, 1, " ns", 9 );
```

```
        initial begin
    sys_rst_n = 0 ;
    #(`PERIOD*5) sys_rst_n = 1'b1;
    #(`PERIOD*5) sys_rst_n = 1'b0;
    #(`PERIOD*10) sys_rst_n = 1'b1;
  end

        always @(sys_rst_n or pin_addr[19:12] or p_wr_68_n) begin
                @(posedge buf_cpu68_clk) if (~sys_rst_n)
                        dead_reg = 16'h0 ;
                else if ((pin_addr[19:12] == 8'hab) & (p_wr_68_n == 1'b0))
                        @(posedge buf_cpu68_clk) dead_reg = pin_data ;
        end

        always @(dead_reg) begin
                @(posedge sys_clk) if (dead_reg == 16'hdead) begin
                        $display ( "Processor halted by dead_reg == dead" );
                        $stop ;
                end
        end

        /* watchdog, to stop simulator from running forever */
        initial #1000000 $stop;



endmodule
```

Plot.v

```
module plotfilegen;

        initial begin
                $dumpfile ( "verilog.vcd" );
                $vtDump;
                $dumpvars ( 1, sys );
                $dumpvars ( 1, sys.dmc );
                $dumpvars ( 0, sys.mot );
                $dumpvars ( 1, sys.mca);
                $dumpvars ( 1, sys.necpart);
                $dumpvars ( 1, sys.pal);
                $dumpvars ( 1, sys.delay1);
        end

endmodule
```

uPD16306

```
module upd16306 ( stb, blk, pc, s_clk, print_data );
input stb, blk, pc, s_clk, print_data;
```

```
reg flag;
specify
        specparam tSU=10, tHLD=10, tCLK_STB=50, clkw=20, stbw=20, blkw=200,
                pcw=200;
        $setup(print_data, negedge s_clk, tSU, flag);
        $hold(print_data, negedge s_clk, tHLD, flag);
        $setup(negedge s_clk, posedge stb, tCLK_STB, flag);
        $width(negedge s_clk, clkw, 0, flag);
        $width(negedge stb, stbw, 0, flag);
        $width(negedge blk, blkw, 0, flag);
        $width(negedge pc, pcw, 0, flag);
endspecify

/* dummy module for the NEC part */

endmodule
```

MCA.v

```
module mca (pe_clk_en, mca_dout);
        input pe_clk_en;
        output mca_dout;

        wire pe_clk_en;
        reg mca_dout;

        initial begin
                mca_dout = 0;
        end

        always @(posedge pe_clk_en)
                mca_dout = ~mca_dout;

endmodule
```

Delay.v

```
module delay2 (stb_in, blk_in, pc_in, print_data_in, clk_in, stb_out, blk_out,
                pc_out, print_data_out, clk_out);
 input  stb_in, blk_in, pc_in, print_data_in, clk_in;
 output stb_out, blk_out, pc_out, print_data_out, clk_out;


 buf #18 b1 (stb_out, stb_in),
        b2 (blk_out, blk_in),
        b3 (pc_out, pc_in),
        b4 (print_data_out, print_data_in),
        b5 (clk_out, clk_in);

endmodule
```

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD16306

HIGH VOLTAGE CMOS DRIVER FOR PDP,EL,VFD

DESCRIPTION

μPD16306 is high voltage driver for PDP, EL or VFD graphic panel structured by CMOS process. Logic power supply is 5 V connecting direct to control logic. Maximum output voltage is 80 V and maximum current is 50 mA.

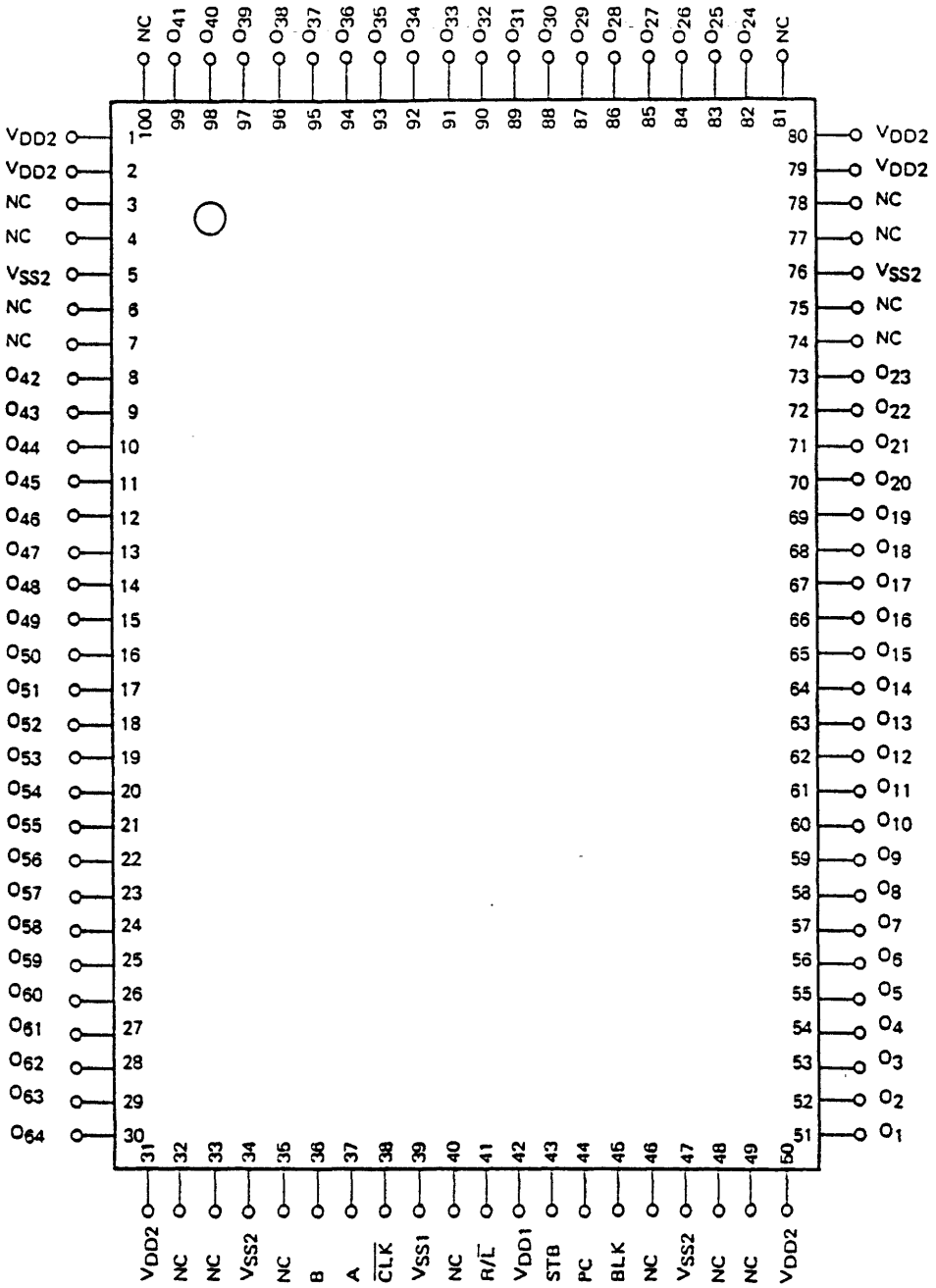
FEATURES

- 80 V Output Voltage Swing Capability
- 50 mA Output Sink and Source Current Capability
- 64 bit Shift-register and Latch
- High Speed Serial DATA Transferring (f_{max} = 20 MHz
- Low Standby Current 100 μA

ORDERING INFORMATION

PART No.	Package
μPD16306GF-3BA	100 pin Plastic QFP (14 x 20)

PIN CONNECTION DIAGRAM (Top View)



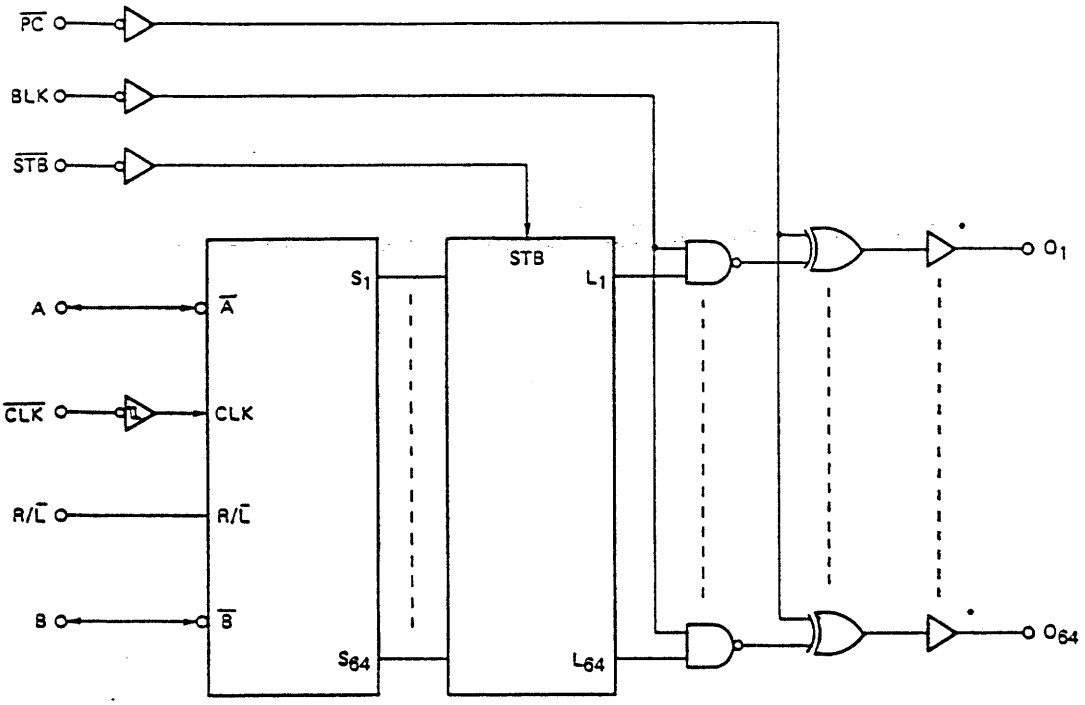
Note:

The 40 pin (NC) should be open.

All the power supply terminals should be used.

V_{SS1} and V_{SS2} should be respectively connected with themselves outside.

BLOCK DIAGRAM



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PIN CONFIGURATION

SYMBOL	PIN NAME	PIN No.	FUNCTION
$\overline{PC}$	Polarity Change input	44	All driver outputs' level are inverted while PC is L.
BLK	Plank input	45	All driver outputs are H while BLK is H and PC is H.
$\overline{STB}$	Latch Strobe input	43	Latch's status is data through while STB is L.
A	Right Data input/output	37	R/L = H : A = IN, B = OUT R/L = L : A = OUT, B = IN
B	Left Data input/output	36	
$\overline{CLK}$	Clock input	38	Data of shift-register is shifted while CLK is going H to L. (Negative edge is active.)
R/$\overline{L}$	Shift Direction Control input	41	H : Right Shift Mode A → O_1 --O_{64} → B L : Left Shift Mode B → O_{64} --O_1 → A
O_1–O_{64}	Driver Outputs	8–30, 51–73 82–99	High voltage output 80 V, 50 mA
V_{DD1}	Logic Power Supply	42	5 V ± 10 %
V_{DD2}	Driver Power Supply	1, 2, 31, 50, 79, 80	10 – 70 V
V_{SS1}	Ground (for Logic)	39	
V_{SS2}	Ground (for Driver)	5, 34, 47, 76	
NC	No Connect	3, 4, 6, 7, 32, 33, 35, 40, 46, 48, 49, 74, 75, 77, 78, 81, 100	No. 40 pin should be open.

TRUTH TABLE 1 (Shift-Register part)

INPUT		IN/OUT		SHIFT-REGISTER
R/$\overline{L}$	CLK	A	B	
H	↓	IN	OUT	DATA is shifted.
H	H or L	IN	OUT	No Change
L	↓	OUT	IN	DATA is shifted.
L	H or L	OUT	IN	No Change

TRUTH TABLE 2 (Latch, Driver part)

DATA	$\overline{STB}$	BLK	$\overline{PC}$	DRIVER OUTPUT
X	X	H	H	ALL H
X	X	H	L	ALL L
H	L	L	H	H
H	L	L	L	L
L	L	L	H	L
L	L	L	L	H
X	H	L	H	Latch's data output
X	H	L	L	Latch's data output (inverting)

DATA are contents of shift register. (S_1-S_{64})

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ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C, V_{SS} = 0 V)

Logic Power Supply	V_{DD1}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to V_{DD1} +0.5	V
Logic Output Voltage	V_{O1}	−0.5 to V_{DD1} +0.5	V
Driver Power Supply	V_{DD2}	−0.5 to 80	V
Driver Output Voltage	V_{O2}	−0.5 to V_{DD2} +0.5	V
Driver Maximum Current	I_{O2}	±50	mA
Power Dissipation/Package	P_D	1000	mW
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = 25 °C, V_{SS} = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Logic Power Supply	V_{DD1}	4.5	5	5.5	V
High Level Input Voltage	V_{IH}	0.7 · V_{DD1}		V_{DD1}	V
Low Level Input Voltage	V_{IL}	0		0.2 · V_{DD1}	V
Driver Power Supply	V_{DD2}	10		70	V
Driver Output Current	I_{OL2}			+40	mA
	I_{OH2}			−40	mA

DC CHARACTERISTICS

(T_a = 25 °C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 70 V, V_{SS} = 0 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
High Level Output Voltage	V_{OH1}	0.9·V_{DD1}			V	Logic, I_{OH1}=−1 mA
Low Level Output Voltage	V_{OL1}			0.1·V_{DD1}	V	Logic, I_{OL1}=1 mA
High Level Output Voltage	V_{OH21}	69			V	O_1–O_{64}, I_{OH2}=−1 mA
	V_{OH22}	65			V	O_1–O_{64}, I_{OH2}=−10 mA
Low Level Output Voltage	V_{OL21}			1	V	O_1–O_{64}, I_{OL2}=5 mA
	V_{OL22}			10	V	O_1–O_{64}, I_{OL2}=40 mA
High Level Input Current	I_{IH}			1	μA	V_I=V_{DD1}
Low Level Input Current	I_{IL}			−1	μA	V_I=0 V
High Level Input Voltage	V_{IH}	0.7·V_{DD1}			V	
Low Level Input Voltage	V_{IL}			0.2·V_{DD1}	V	
Stand by Current	I_{DD1}			1.0	mA	for V_{DD1}, T_a=−40 to +85 °C
	I_{DD1}			10	μA	for V_{DD1}, T_a=25 °C
	I_{DD2}			1.0	mA	for V_{DD2}, T_a=−40 to +85 °C
	I_{DD2}			100	μA	for V_{DD2}, T_a=25 °C

AC CHARACTERISTICS

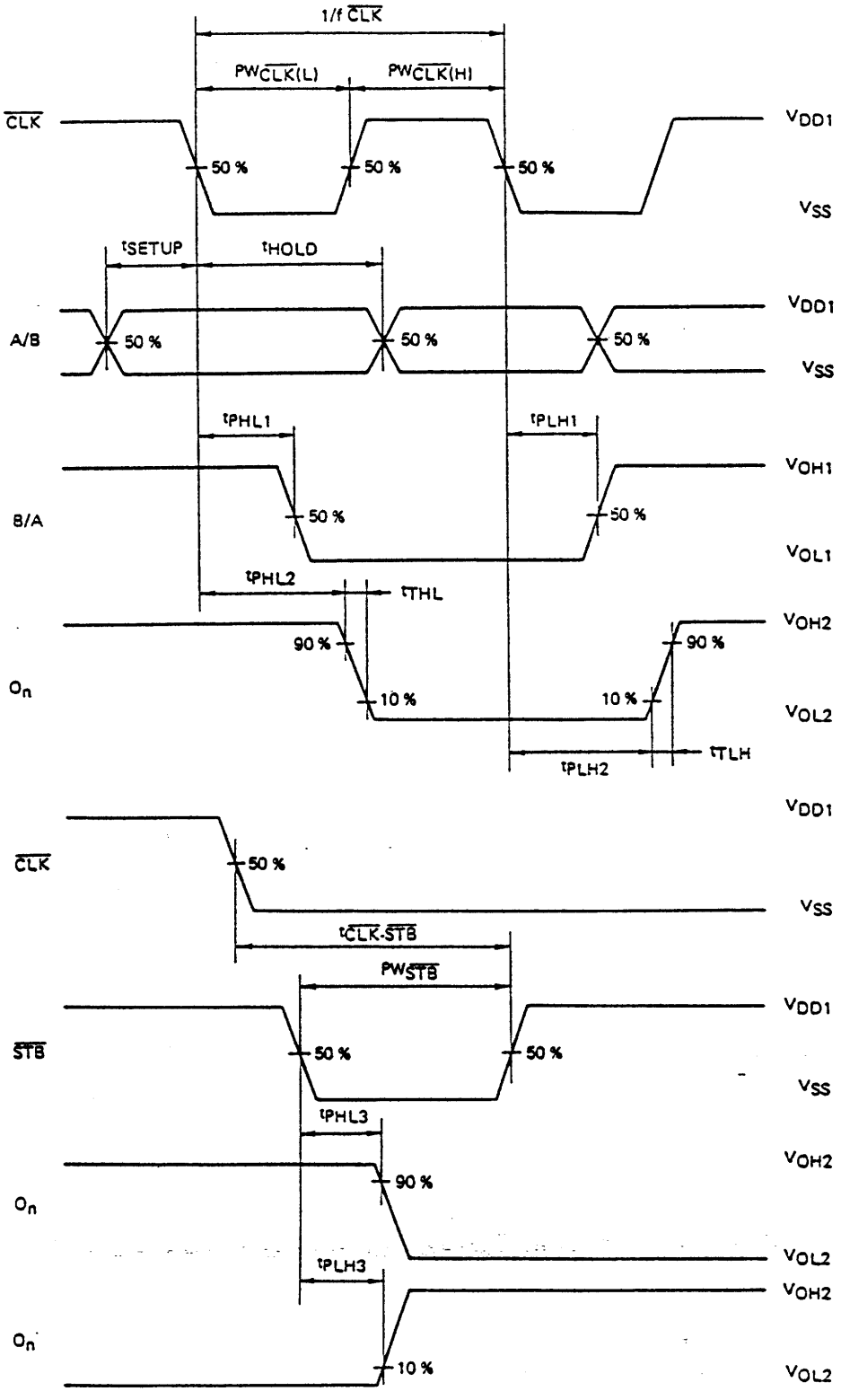
(T_a = 25 °C, V_{DD1} = 5 V, V_{DD2} = 70 V, Logic C_L = 15 pF
Driver C_L = 50 pF)

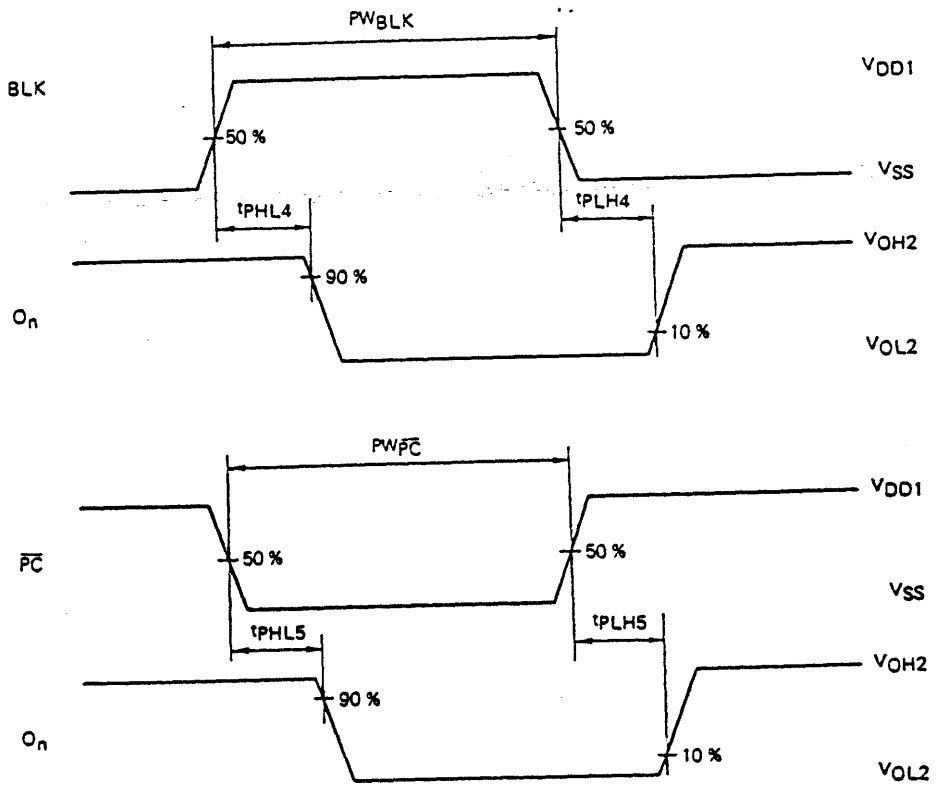
ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Delay Time	t_{PHL1}			50	ns	$\overline{CLK}$ → A/B
	t_{PLH1}			50	ns	
	t_{PHL2}			160	ns	$\overline{CLK}$ → O_1–O_{64}
	t_{PLH2}			160	ns	
	t_{PHL3}			150	ns	$\overline{STB}$ → O_1–O_{64}
	t_{PLH3}			150	ns	
	t_{PHL4}			145	ns	BLK → O_1–O_{64}
	t_{PLH4}			145	ns	
	t_{PHL5}			140	ns	$\overline{PC}$ → O_1–O_{64}
	t_{PLH5}			140	ns	
Rise Time	t_{TLH}			70	ns	O_1–O_{64}
Fall Time	t_{THL}			70	ns	O_1–O_{64}
Maximum Frequency	f_{max}	20	30		MHz	Duty=50 %, for CLK
Input Capacitance	C_I		10	15	pF	

AC TIMING REQUIREMENT (T_a = −40 to 80 °C, V_{DD1} = 4.5 to 5.5 V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Clock Pulse Width	$PW_{\overline{CLK}}$	20			ns	
Strobe Pulse Width	$PW_{\overline{STB}}$	20			ns	
Blank Pulse Width	PW_{BLK}	200			ns	
Polarity Change Pulse Width	$PW_{\overline{PC}}$	200			ns	
Data Setup Time	t_{SETUP}	10			ns	
Data Hold Time	t_{HOLD}	10			ns	
Setup Time	$t_{\overline{CLK}\text{-}\overline{STB}}$	50			ns	for CLK ↓ to $\overline{STB}$ ↑

AC CHARACTERISTICS WAVEFORM




PWBLK
BLK
VDD1
50 %
50 %
VSS
tPHL4
tPLH4
VOH2
90 %
On
10 %
VOL2
PWPC
PC
VDD1
50 %
50 %
VSS
tPHL5
tPLH5
VOH2
90 %
On
10 %
VOL2

10

NOTES

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

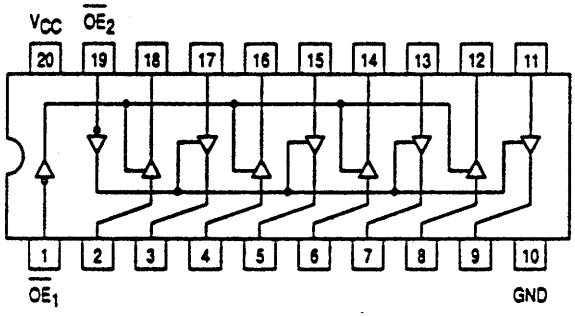
MC74AC244
MC74ACT244

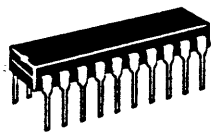
Octal Buffer/Line Driver with 3-State Outputs

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

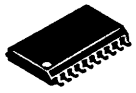
The MC74AC244/74ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT244 Has TTL Compatible Inputs





N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-04
PLASTIC

TRUTH TABLE

Inputs		Outputs
OE_1	D	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

TRUTH TABLE

Inputs		Outputs
OE_2	D	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Ref. to GND)		0		V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V		150		ns/V
		V_{CC} @ 4.5 V		40		
		V_{CC} @ 5.5 V		25		
t_r, t_f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V		10		ns/V
		V_{CC} @ 5.5 V		8.0		
T_J	Junction Temperature (PDIP)				140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current — High				−24	mA
I_{OL}	Output Current — Low				24	mA

1. V_{in} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{in} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	74AC T_A = −40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76		I_{OH} −12 mA
		5.5		4.86	4.76		I_{OH} −24 mA
							I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44		I_{OL} 12 mA
		5.5		0.36	0.44		I_{OL} 24 mA
							I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.
Note: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	1.5 1.0	10.0 7.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	6.5 5.0	9.0 7.0	2.0 1.0	10.0 7.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	2.0 1.5	6.0 5.0	10.5 7.0	1.5 1.5	11.0 8.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	2.5 1.5	7.5 5.5	10.0 8.0	2.0 1.5	11.0 8.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	3.0 2.5	7.0 6.5	10.0 9.0	1.5 1.0	10.5 9.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	2.5 2.0	7.5 6.5	10.5 9.0	2.5 2.0	11.5 9.5	ns	3-8

* Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	74ACT T_A = −40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5			75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μA	V_{IN} = V_{CC} or GND

* All outputs loaded; thresholds on input associated with output under test.
† Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	2.0	6.5	9.0	1.5	10.0	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	2.0	7.0	9.0	1.5	10.0	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.5	6.0	8.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	2.0	7.0	9.5	1.5	10.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	2.5	7.5	10.0	2.0	10.5	ns	3-8

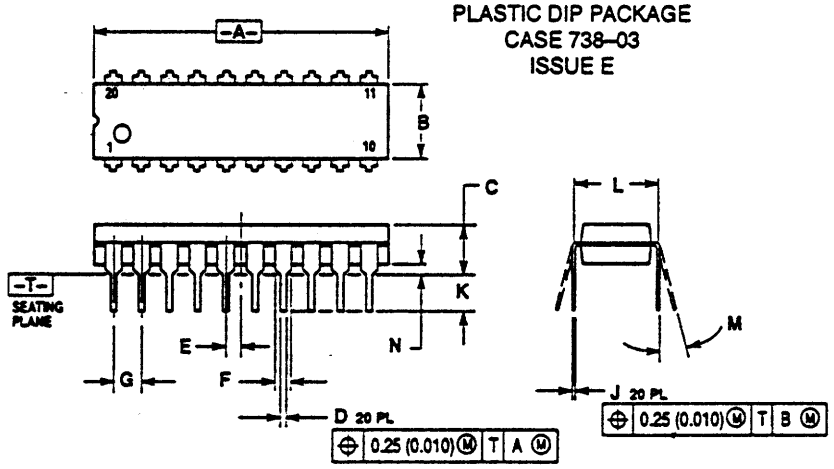
* Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

OUTLINE DIMENSIONS

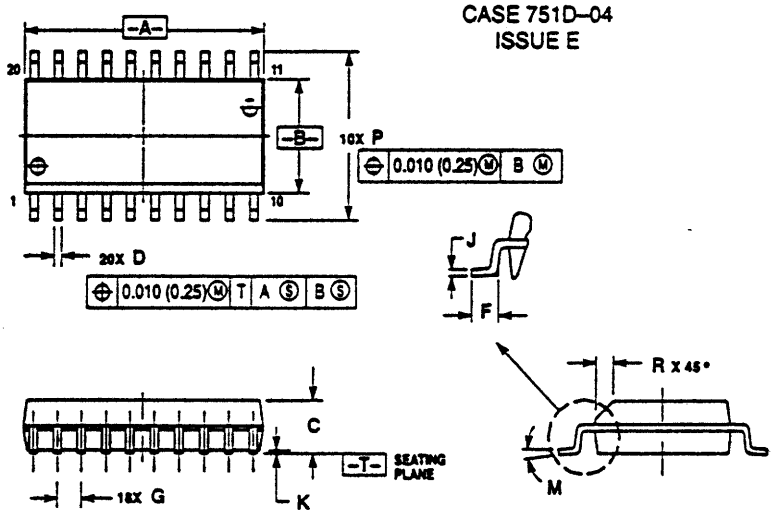
N SUFFIX
PLASTIC DIP PACKAGE
CASE 738–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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MFAX: RMFAX0@email.sps.mot.com –TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

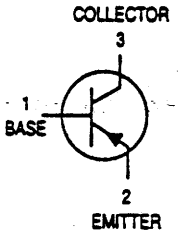
JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

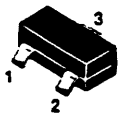
HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

General Purpose Transistors
PNP Silicon

BC856ALT1,BLT1
BC857ALT1,
BLT1,CLT1
BC858ALT1,BLT1,
CLT1

Motorola Preferred Devices





CASE 318–08, STYLE 6
SOT–23 (TO–236AB)

MAXIMUM RATINGS

Rating	Symbol	BC856	BC857	BC858	Unit
Collector–Emitter Voltage	V_{CEO}	–65	–45	–30	V
Collector–Base Voltage	V_{CBO}	–80	–50	–30	V
Emitter–Base Voltage	V_{EBO}	–5.0	–5.0	–5.0	V
Collector Current — Continuous	I_C	–100	–100	–100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board, (1) T_A = 25°C Derate above 25°C	P_D	 225 1.8	 mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (2) T_A = 25°C Derate above 25°C	P_D	 300 2.4	 mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	°C

DEVICE MARKING

BC856ALT1 = 3A; BC856BLT1 = 3B; BC857ALT1 = 3E; BC857BLT1 = 3F;
BC857CLT1 = 3G; BC858ALT1 = 3J; BC858BLT1 = 3K; BC858CLT1 = 3L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–Emitter Breakdown Voltage (I_C = –10 mA)	BC856 Series BC857 Series BC858 Series	$V_{(BR)CEO}$	–65 –45 –30	— — —	— — —	V
Collector–Emitter Breakdown Voltage (I_C = –10 μA, V_{EB} = 0)	BC856 Series BC857 Series BC858 Series	$V_{(BR)CES}$	–80 –50 –30	— — —	— — —	V
Collector–Base Breakdown Voltage (I_C = –10 μA)	BC856 Series BC857 Series BC858 Series	$V_{(BR)CBO}$	–80 –50 –30	— — —	— — —	V
Emitter–Base Breakdown Voltage (I_E = –1.0 μA)	BC856 Series BC857 Series BC858 Series	$V_{(BR)EBO}$	–5.0 –5.0 –5.0	— — —	— — —	V
Collector Cutoff Current (V_{CB} = –30 V) (V_{CB} = –30 V, T_A = 150°C)		I_{CBO}	— —	— —	–15 –4.0	nA μA

1. FR–5 = 1.0 x 0.75 x 0.062 in 2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

Thermal Clad is a registered trademark of the Bergquist Company.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
DC Current Gain	BC856A, BC857A, BC585A	h_{FE}	—	90	—	—
(I_C = −10 μA, V_{CE} = −5.0 V)	BC856A, BC857A, BC858A		—	150	—	
	BC857C, BC858C		—	270	—	
(I_C = −2.0 mA, V_{CE} = −5.0 V)	BC856A, BC857A, BC858A		125	180	250	
	BC856B, BC857B, BC858B		220	290	475	
	BC857C, BC858C		420	520	800	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = −10 mA, I_B = −0.5 mA)			—	—	−0.3	
(I_C = −100 mA, I_B = −5.0 mA)			—	—	−0.65	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$				V
(I_C = −10 mA, I_B = −0.5 mA)			—	−0.7	—	
(I_C = −100 mA, I_B = −5.0 mA)			—	−0.9	—	
Base–Emitter On Voltage		$V_{BE(on)}$				V
(I_C = −2.0 mA, V_{CE} = −5.0 V)			−0.6	—	−0.75	
(I_C = −10 mA, V_{CE} = −5.0 V)			—	—	−0.82	
SMALL–SIGNAL CHARACTERISTICS						
Current–Gain — Bandwidth Product (I_C = −10 mA, V_{CE} = −5.0 Vdc, f = 100 MHz)		f_T	100	—	—	MHz
Output Capacitance (V_{CB} = −10 V, f = 1.0 MHz)		C_{ob}	—	—	4.5	pF
Noise Figure (I_C = −0.2 mA, V_{CE} = −5.0 Vdc, R_S = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)		NF	—	—	10	dB

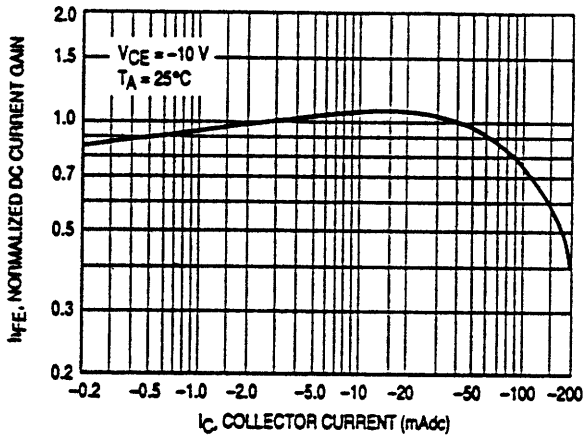


Figure 1. Normalized DC Current Gain

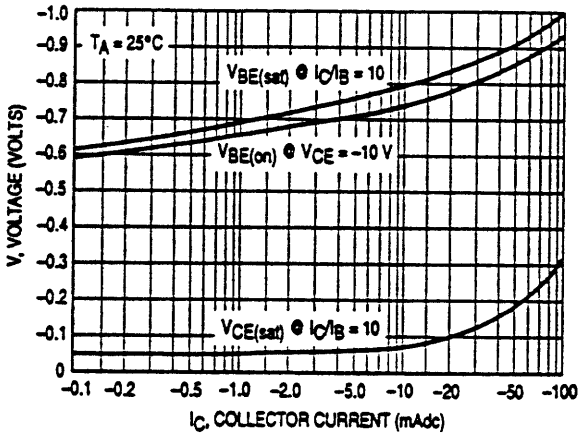


Figure 2. "Saturation" and "On" Voltages

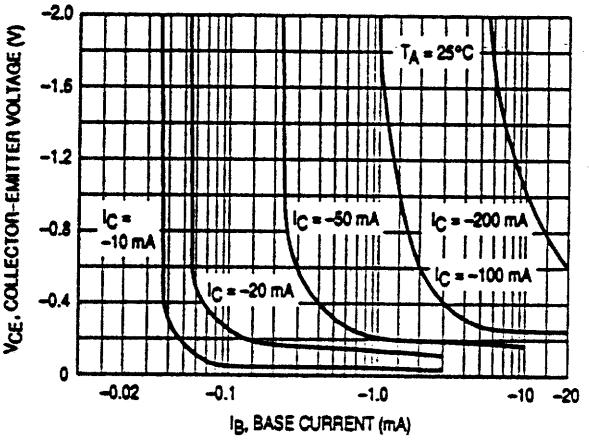


Figure 3. Collector Saturation Region

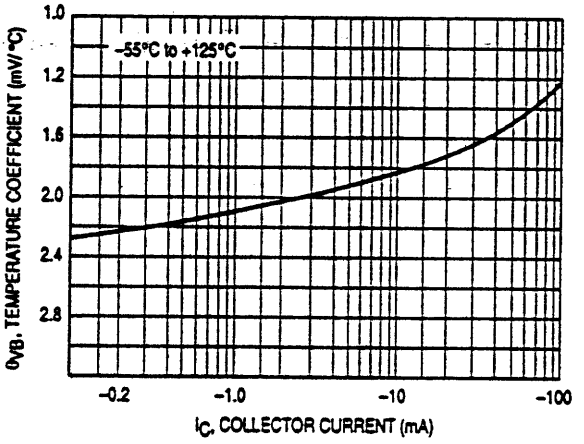


Figure 4. Base–Emitter Temperature Coefficient

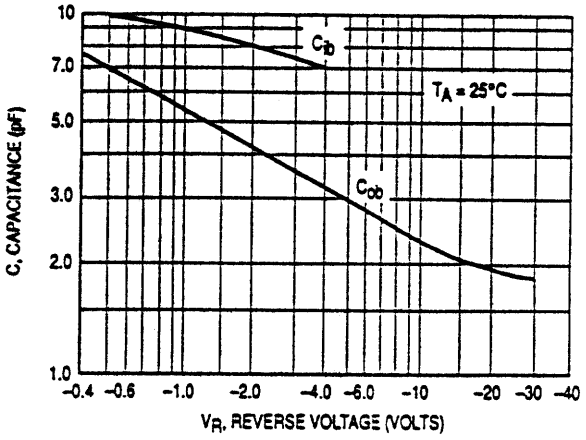


Figure 5. Capacitances

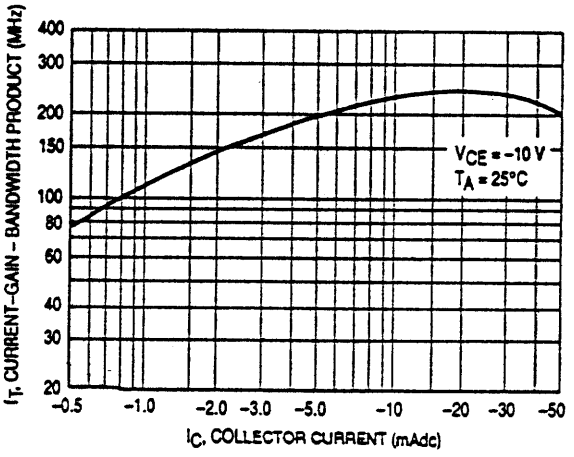


Figure 6. Current–Gain – Bandwidth Product

BC856

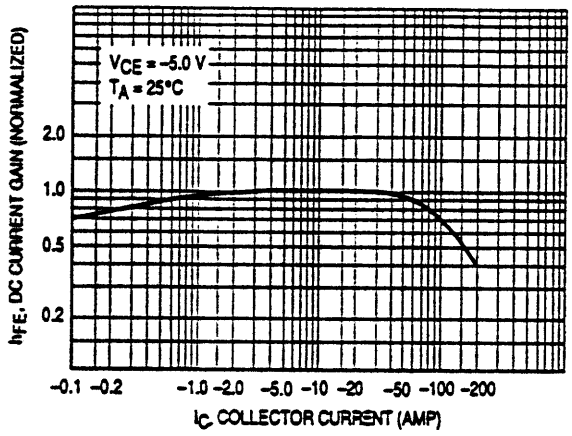


Figure 7. DC Current Gain

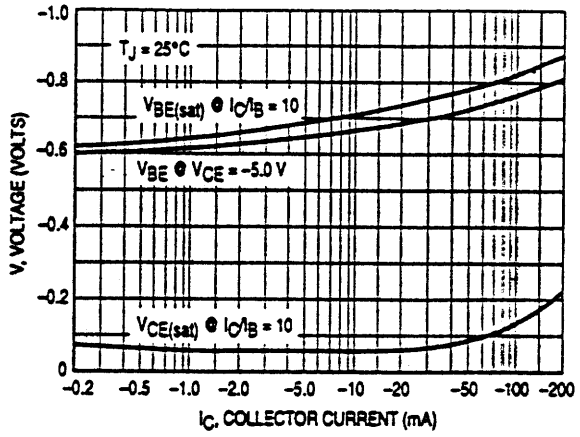


Figure 8. "On" Voltage

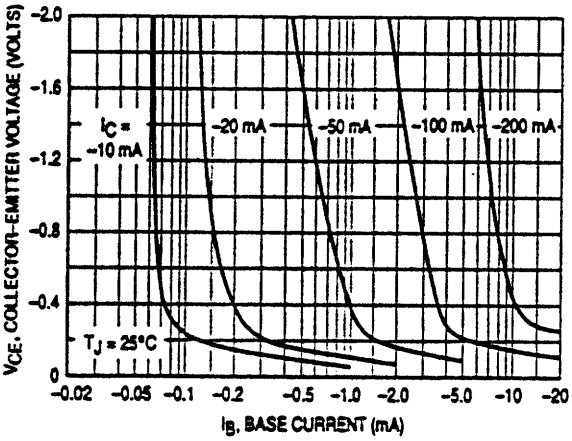


Figure 9. Collector Saturation Region

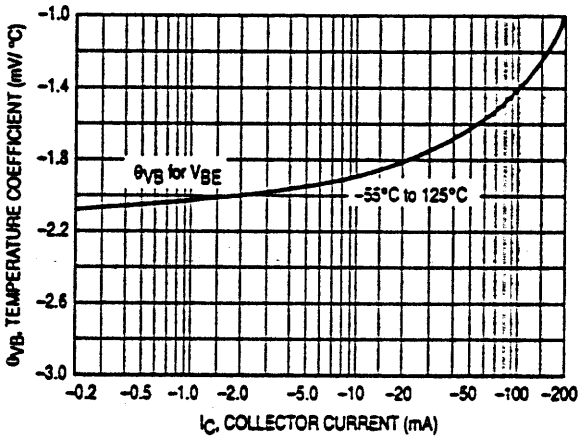


Figure 10. Base–Emitter Temperature Coefficient

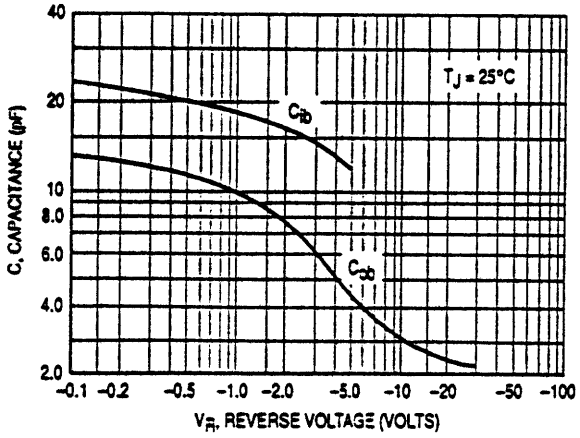


Figure 11. Capacitance

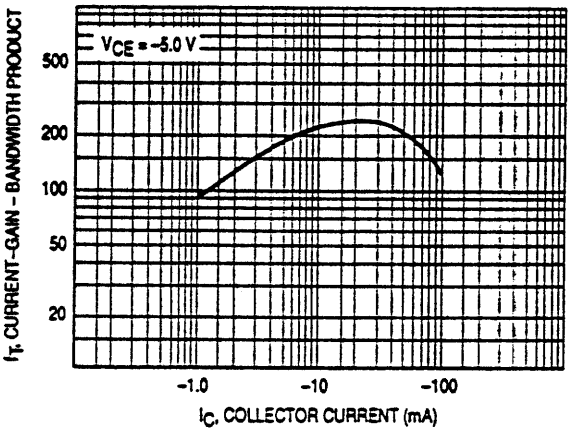


Figure 12. Current–Gain – Bandwidth Product

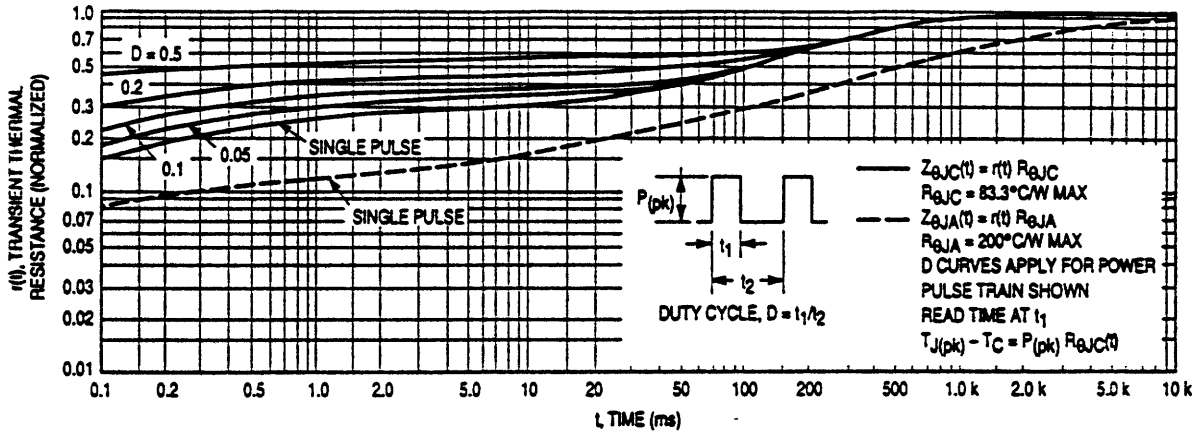


Figure 13. Thermal Response

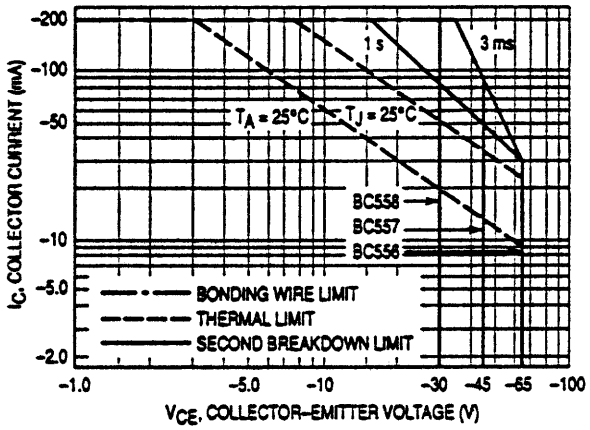


Figure 14. Active Region Safe Operating Area

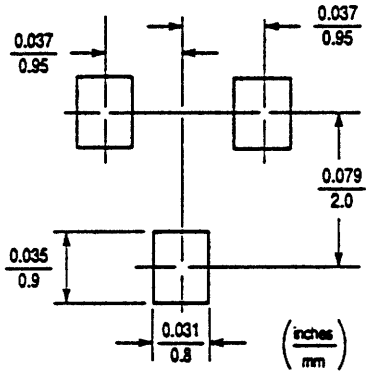
The safe operating area curves indicate I_C–V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 14 is based upon $T_{J(pk)}$ = 150°C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 13. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by the secondary breakdown.

INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT–23

SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–23 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

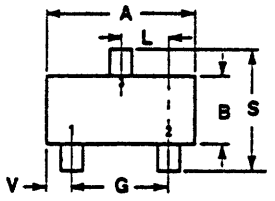
SOLDERING PRECAUTIONS

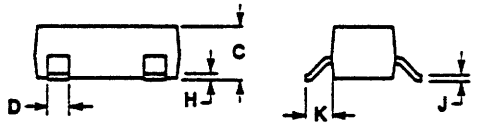
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0180	0.0236	0.45	0.60
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.0984	2.10	2.50
V	0.0177	0.0236	0.45	0.60

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

CASE 318–08
ISSUE AE
SOT–23 (TO–236AB)

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INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

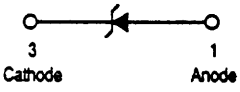
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

225 mW SOT-23
Zener Voltage Regulator Diodes

GENERAL DATA APPLICABLE TO ALL SERIES IN THIS GROUP

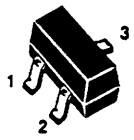
Zener Voltage Regulator Diodes

GENERAL DATA
225 mW
SOT-23



Manufacturing Locations:

WAFER FAB: Phoenix, Arizona
ASSEMBLY: Seremban, Malaysia
TEST: Seremban, Malaysia
MAXIMUM CASE TEMPERATURE FOR SOLDERING PURPOSES: 260°C for 10 seconds



CASE 318-07, STYLE 8
SOT-23 (TO-236AB)
PLASTIC

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board,* T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate,** T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temeprature	T_J, T_{stg}	150	°C

*FR-5 = 1.0 x 0.75 x 0.62 in.
**Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.

TYPICAL CHARACTERISTICS

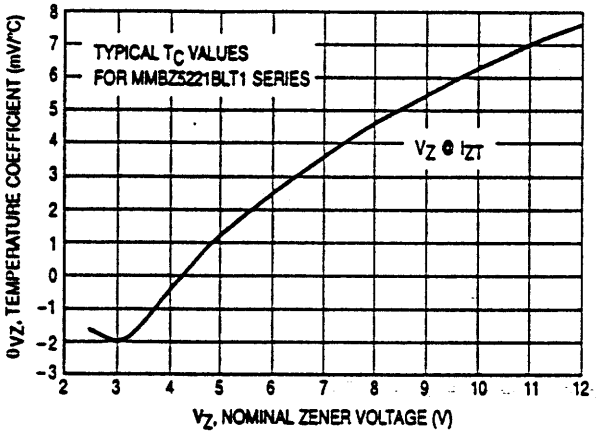


Figure 1. Temperature Coefficients (Temperature Range −55°C to +150°C)

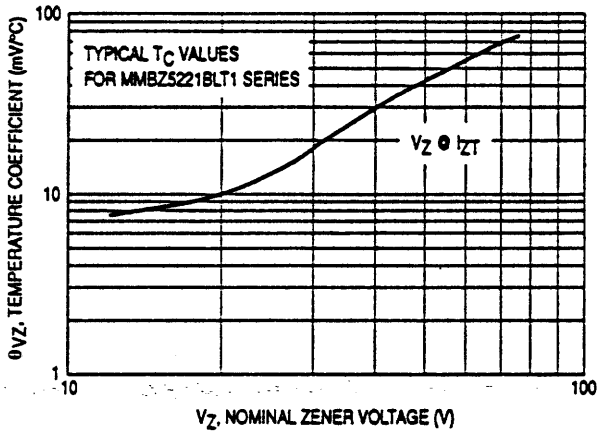


Figure 2. Temperature Coefficients (Temperature Range −55°C to +150°C)

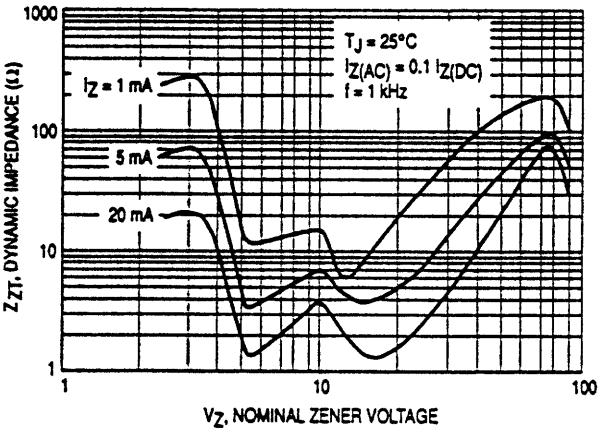


Figure 3. Effect of Zener Voltage on Zener Impedance

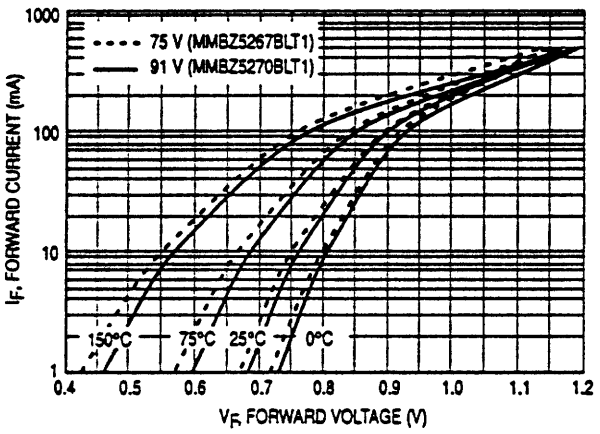


Figure 4. Typical Forward Voltage

TYPICAL CHARACTERISTICS

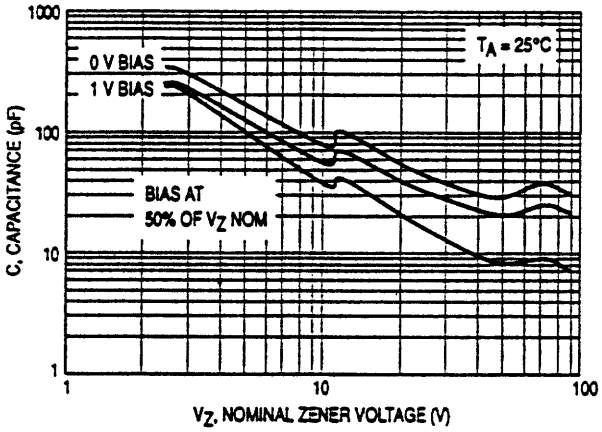


Figure 5. Typical Capacitance

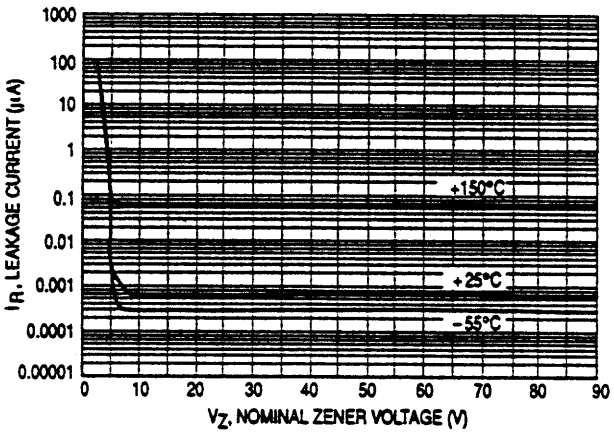


Figure 6. Typical Leakage Current

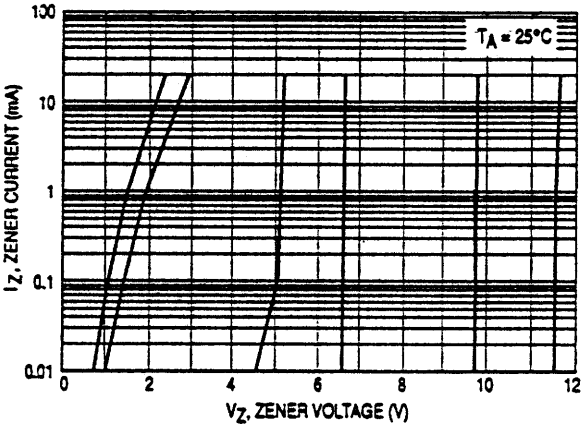


Figure 7. Zener Voltage versus Zener Current
(V_Z Up to 12 V)

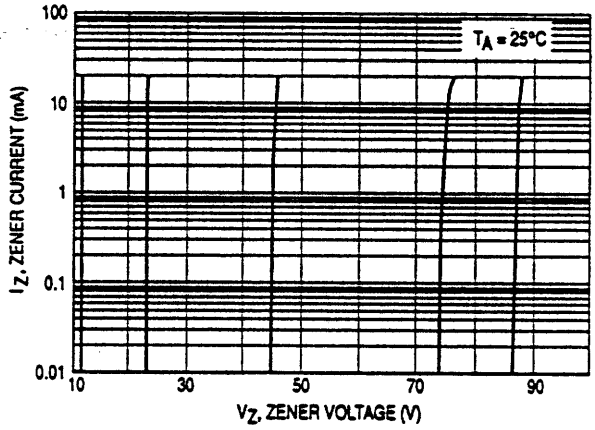


Figure 8. Zener Voltage versus Zener Current
(12 V to 91 V)

GENERAL DATA — 225 mW SOT-23

ELECTRICAL CHARACTERISTICS (Pinout: 1-Anode, 2-NC, 3-Cathode) (V_F = 0.9 V Max @ I_F = 10 mA for all types)

Type Number	Marking	Zener Voltage V_{Z1} (Volts) @ I_{ZT1} = 5 mA (Note 1)			Max Zener Impedance Z_{ZT1} (Ohms)	Max Reverse Leakage Current		Zener Voltage V_{Z2} (Volts) @ I_{ZT2} = 1 mA (Note 1)		Max Zener Impedance Z_{ZT2} (Ohms)	Zener Voltage V_{Z3} (Volts) @ I_{ZT3} = 20 mA (Note 1)		Max Zener Impedance Z_{ZT3} (Ohms)	d_{VZ}/dt (mV/k) @ I_{ZT1} = 5 mA		C pF Max
		Nom	Min	Max	@ I_{ZT1} = 5 mA	I_R µA	@ V_R Volts	Min	Max	@ I_{ZT2} = 1 mA	Min	Max	@ I_{ZT3} = 20 mA	Min	Max	@ V_R = 0 f = 1 MHz
BZX84C2V4LT1	Z11	2.4	2.2	2.6	100	50	1	1.7	2.1	600	2.6	3.2	50	-3.5	0	450
BZX84C2V7LT1	Z12	2.7	2.5	2.9	100	20	1	1.9	2.4	600	3	3.6	50	-3.5	0	450
BZX84C3V0LT1	Z13	3	2.8	3.2	95	10	1	2.1	2.7	600	3.3	3.9	50	-3.5	0	450
BZX84C3V3LT1	Z14	3.3	3.1	3.5	95	5	1	2.3	2.9	600	3.6	4.2	40	-3.5	0	450
BZX84C3V6LT1	Z15	3.6	3.4	3.8	90	5	1	2.7	3.3	600	3.9	4.5	40	-3.5	0	450
BZX84C3V9LT1	Z16	3.9	3.7	4.1	90	3	1	2.9	3.5	600	4.1	4.7	30	-3.5	-2.5	450
BZX84C4V3LT1	W9	4.3	4	4.6	90	3	1	3.3	4	600	4.4	5.1	30	-3.5	0	450
BZX84C4V7LT1	*Z1*	*4.7*	*4.4*	*5*	*80*	*3*	*2*	*3.7*	*4.7*	*500*	*4.5*	*5.4*	*15*	*-3.5*	*0.2*	*260*
BZX84C5V1LT1	*Z2*	*5.1*	*4.8*	*5.4*	*60*	*2*	*2*	*4.2*	*5.3*	*480*	*5*	*5.9*	*15*	*-2.7*	*1.2*	*225*
BZX84C5V6LT1	*Z3*	*5.6*	*5.2*	*6*	*40*	*1*	*2*	*4.8*	*6*	*400*	*5.2*	*6.3*	*10*	*-2.0*	*2.5*	*200*
BZX84C6V2LT1	*Z4*	*6.2*	*5.8*	*6.6*	*10*	*3*	*4*	*5.6*	*6.6*	*150*	*5.8*	*6.8*	*6*	*0.4*	*3.7*	*185*
BZX84C6V8LT1	Z5	6.8	6.4	7.2	15	2	4	6.3	7.2	80	6.4	7.4	6	1.2	4.5	155
BZX84C7V5LT1	Z6	7.5	7	7.9	15	1	5	6.9	7.9	80	7	8	6	2.5	5.3	140
BZX84C8V2LT1	Z7	8.2	7.7	8.7	15	0.7	5	7.6	8.7	80	7.7	8.8	6	3.2	6.2	135
BZX84C9V1LT1	Z8	9.1	8.5	9.6	15	0.5	6	8.4	9.6	100	8.5	9.7	8	3.8	7.0	130
BZX84C10LT1	Z9	10	9.4	10.6	20	0.2	7	9.3	10.6	150	9.4	10.7	10	4.5	8.0	130
BZX84C11LT1	Y1	11	10.4	11.6	20	0.1	8	10.2	11.6	150	10.4	11.8	10	5.4	9.0	130
BZX84C12LT1	*Y2*	*12*	*11.4*	*12.7*	*25*	*0.1*	*8*	*11.2*	*12.7*	*150*	*11.4*	*12.9*	*10*	*6.0*	*10.0*	*130*
BZX84C13LT1	Y3	13	12.4	14.1	30	0.1	8	12.3	14	170	12.5	14.2	15	7.0	11.0	120
BZX84C15LT1	Y4	15	13.8	15.6	30	0.05	10.5	13.7	15.5	200	13.9	15.7	20	9.2	13.0	110
BZX84C16LT1	Y5	16	15.3	17.1	40	0.05	11.2	15.2	17	200	15.4	17.2	20	10.4	14.0	105
BZX84C18LT1	*Y6*	*18*	*16.8*	*19.1*	*45*	*0.05*	*12.6*	*16.7*	*19*	*225*	*16.9*	*19.2*	*20*	*12.4*	*16.0*	*100*
BZX84C20LT1	Y7	20	18.8	21.2	55	0.05	14	18.7	21.1	225	18.9	21.4	20	14.4	18.0	85
BZX84C22LT1	Y8	22	20.8	23.3	55	0.05	15.4	20.7	23.2	250	20.9	23.4	25	16.4	20.0	85
BZX84C24LT1	Y9	24	22.8	25.6	70	0.05	16.8	22.7	25.5	250	22.9	25.7	25	18.4	22.0	80
		V_{Z1} Below @ I_{ZT1} = 2 mA			Z_{ZT1} Below @ I_{ZT1} = 2 mA			V_{Z2} Below @ I_{ZT2} = 0.1 mA		Z_{ZT2} Below @ I_{ZT4} = 0.5 mA (Note 2)	V_{Z3} Below @ I_{ZT3} = 10 mA		Z_{ZT3} Below @ I_{ZT3} = 10 mA	d_{VZ}/dt (mV/k) Below @ I_{ZT1} = 2 mA		
BZX84C27LT1	Y10	27	25.1	28.9	80	0.05	18.9	25	28.9	300	25.2	29.3	45	21.4	25.3	70
BZX84C30LT1	Y11	30	28	32	80	0.05	21	27.8	32	300	28.1	32.4	50	24.4	29.4	70
BZX84C33LT1	Y12	33	31	35	80	0.05	23.1	30.8	35	325	31.1	35.4	55	27.4	33.4	70
BZX84C36LT1	Y13	36	34	38	90	0.05	25.2	33.8	38	350	34.1	38.4	60	30.4	37.4	70
BZX84C39LT1	Y14	39	37	41	130	0.05	27.3	36.7	41	350	37.1	41.5	70	33.4	41.2	45
BZX84C43LT1	Y15	43	40	46	150	0.05	30.1	39.7	46	375	40.1	46.5	80	37.6	46.6	40
BZX84C47LT1	Y16	47	44	50	170	0.05	32.9	43.7	50	375	44.1	50.5	90	42.0	51.8	40
BZX84C51LT1	Y17	51	48	54	180	0.05	35.7	47.6	54	400	48.1	54.6	100	46.6	57.2	40
BZX84C56LT1	Y18	56	52	60	200	0.05	39.2	51.5	60	425	52.1	60.8	110	52.2	63.8	40
BZX84C62LT1	Y19	62	58	66	215	0.05	43.4	57.4	66	450	58.2	67	120	58.8	71.6	35
BZX84C68LT1	Y20	68	64	72	240	0.05	47.6	63.4	72	475	64.2	73.2	130	65.6	79.8	35
BZX84C75LT1	Y21	75	70	79	255	0.05	52.5	69.4	79	500	70.3	80.2	140	73.4	88.6	35

NOTES: 1. Zener voltage is measured with a pulse test current (I_Z) applied at an ambient temperature of 25°C.

2. The zener impedance, Z_{ZT2}, for the 27 through 75 volt types is tested at 0.5 mA rather than the test current of 0.1 mA used for V_{Z2}.

GENERAL DATA — 225 mW SOT-23

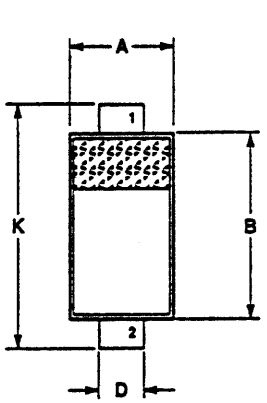
ELECTRICAL CHARACTERISTICS (Pinout: 1-Anode, 2-NC, 3-Cathode) (V_F = 0.9 V Max @ I_F = 10 mA for all types.)

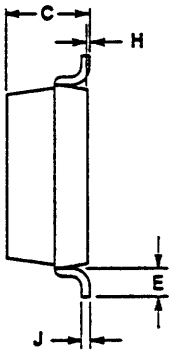
Device	Marking	Test Current I_{ZT} mA	Zener Voltage V_Z (±5%) Nominal (Note 1)	Z_{ZK} I_Z = 0.25 mA Ω Max	Z_{ZT} $I_Z = I_{ZT}$ @ 10% Mod Ω Max	Max I_R @ µA	V_R V
MMBZ5221BLT1	18A	20	2.4	1200	30	100	1
MMBZ5222BLT1	18B	20	2.5	1250	30	100	1
MMBZ5223BLT1	18C	20	2.7	1300	30	75	1
MMBZ5224BLT1	18D	20	2.8	1400	30	75	1
MMBZ5225BLT1	18E	20	3	1600	29	50	1
MMBZ5226BLT1	8A	20	3.3	1600	28	25	1
MMBZ5227BLT1	8B	20	3.6	1700	24	15	1
MMBZ5228BLT1	8C	20	3.9	1900	23	10	1
MMBZ5229BLT1	8D	20	4.3	2000	22	5	1
MMBZ5230BLT1	8E	20	4.7	1900	19	5	2
MMBZ5231BLT1	***8F***	***20***	***5.1***	***1600***	***17***	***5***	***2***
MMBZ5232BLT1	***8G***	***20***	***5.6***	***1600***	***11***	***5***	***3***
MMBZ5233BLT1	8H	20	6	1600	7	5	3.5
MMBZ5234BLT1	***8J***	***20***	***6.2***	***1000***	***7***	***5***	***4***
MMBZ5235BLT1	***8K***	***20***	***6.8***	***750***	***5***	***3***	***5***
MMBZ5236BLT1	8L	20	7.5	500	6	3	6
MMBZ5237BLT1	8M	20	8.2	500	8	3	6.5
MMBZ5238BLT1	8N	20	8.7	600	8	3	6.5
MMBZ5239BLT1	8P	20	9.1	600	10	3	7
MMBZ5240BLT1	***8Q***	***20***	***10***	***600***	***17***	***3***	***8***
MMBZ5241BLT1	8R	20	11	600	22	2	8.4
MMBZ5242BLT1	***8S***	***20***	***12***	***600***	***30***	***1***	***9.1***
MMBZ5243BLT1	8T	9.5	13	600	13	0.5	9.9
MMBZ5244BLT1	8U	9	14	600	15	0.1	10
MMBZ5245BLT1	***8V***	***8.5***	***15***	***600***	***16***	***0.1***	***11***
MMBZ5246BLT1	8W	7.8	16	600	17	0.1	12
MMBZ5247BLT1	8X	7.4	17	600	19	0.1	13
MMBZ5248BLT1	***8Y***	***7***	***18***	***600***	***21***	***0.1***	***14***
MMBZ5249BLT1	8Z	6.6	19	600	23	0.1	14
MMBZ5250BLT1	81A	6.2	20	600	25	0.1	15
MMBZ5251BLT1	81B	5.6	22	600	29	0.1	17
MMBZ5252BLT1	81C	5.2	24	600	33	0.1	18
MMBZ5253BLT1	81D	5	25	600	35	0.1	19
MMBZ5254BLT1	***81E***	***4.6***	***27***	***600***	***41***	***0.1***	***21***
MMBZ5255BLT1	81F	4.5	28	600	44	0.1	21
MMBZ5256BLT1	81G	4.2	30	600	49	0.1	23
MMBZ5257BLT1	***81H***	***3.8***	***33***	***700***	***58***	***0.1***	***25***
MMBZ5258BLT1	81J	3.4	36	700	70	0.1	27
MMBZ5259BLT1	81K	3.2	39	800	80	0.1	30
MMBZ5260BLT1	18F	3	43	900	93	0.1	33
MMBZ5261BLT1	81M	2.7	47	1000	105	0.1	36
MMBZ5262BLT1	81N	2.5	51	1100	125	0.1	39
MMBZ5263BLT1	81P	2.2	56	1300	150	0.1	43
MMBZ5264BLT1	81Q	2.1	60	1400	170	0.1	46
MMBZ5265BLT1	81R	2	62	1400	185	0.1	47
MMBZ5266BLT1	81S	1.8	68	1600	230	0.1	52
MMBZ5267BLT1	81T	1.7	75	1700	270	0.1	56
MMBZ5268BLT1	81U	1.5	82	2000	330	0.1	62
MMBZ5269BLT1	81V	1.4	87	2200	370	0.1	68
MMBZ5270BLT1	81W	1.4	91	2300	400	0.1	69

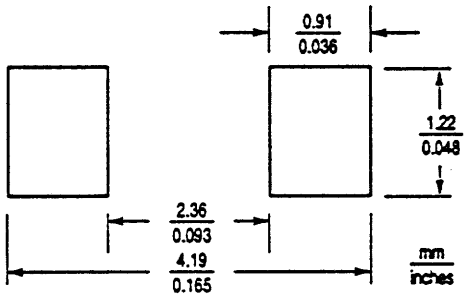
NOTE 1. Zener voltage is measured with a pulse test current (I_{ZT}) applied at an ambient temperature of 25°C.

Zener Voltage Regulator Diodes — Surface Mounted

500 mW SOD-123







SOD-123 Footprint

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 425-01 THRU -03 OBSOLETE, NEW STANDARD 425-04.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	1.40	1.80	0.055	0.071
B	2.55	2.85	0.100	0.112
C	0.95	1.35	0.037	0.053
D	0.50	0.70	0.020	0.028
E	0.25	—	0.010	—
H	0.00	0.10	0.000	0.004
J	—	0.15	—	0.006
K	3.55	3.85	0.140	0.152

CASE 425
PLASTIC

STYLE 1:
PIN 1. CATHODE
2. ANODE

(Refer to Section 10 for Surface Mount, Thermal Data and Footprint Information.)

MULTIPLE PACKAGE QUANTITY (MPQ) REQUIREMENTS

Package Option	Type No. Suffix	MPQ (Units)
Tape and Reel	T1(1)	3K
Tape and Reel	T3(2)	10K

NOTE: 1. The numbers on the suffixes indicate the following:
1. 7" Reel. Cathode lead toward sprocket hole.
2. 13" Reel. Cathode lead toward sprocket hole.

(Refer to Section 10 for more information on Packaging Specifications.)

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

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MOTOROLA

MC34063A
MC33063A

DC-to-DC Converter Control Circuits

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

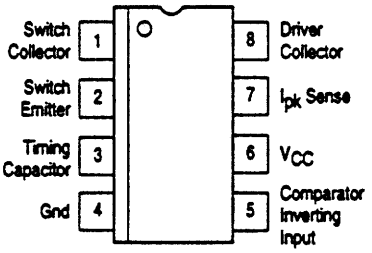
DC–to–DC CONVERTER CONTROL CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626

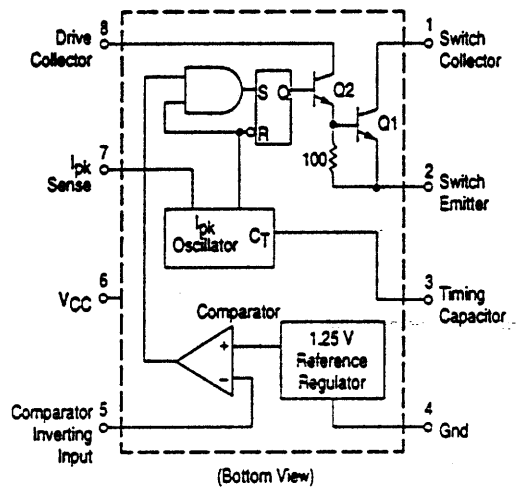
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



(Bottom View)

This device contains 51 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33063AD	T_A = – 40° to +85°C	SO–8
MC33063AP1		Plastic DIP
MC33063AVD	T_A = –40° to +125°C	SO–8
MC33063AVP		Plastic DIP
MC34063AD	T_A = 0° to +70°C	SO–8
MC34063AP1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	−0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics Plastic Package, P, P1 Suffix T_A = 25°C Thermal Resistance SOIC Package, D Suffix T_A = 25°C Thermal Resistance	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1.25 100 625 160	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range MC34063A MC33063AV MC33063A	T_A	 0 to +70 −40 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	35	42	µA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	220	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage (I_{chg} = I_{dischg}, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced β = 20)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	75	–	–
Collector Off–State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.01	100	µA

NOTES: 3. T_{low} = 0°C for MC34063A, −40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver} - 7.0\ mA^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage T_A = 25°C T_A = T_{low} to T_{high}	V_{th}	 1.225 1.21	 1.25 –	 1.275 1.29	V
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V) MC33063A, MC34063A MC33363AV	Regline	 – –	 1.4 1.4	 5.0 6.0	mV
Input Bias Current (V_{in} = 0 V)	I_{IB}	–	–20	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES: 3. T_{low} = 0°C for MC34063A, –40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
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Forced β of output switch : $\frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}^*} \geq 10$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

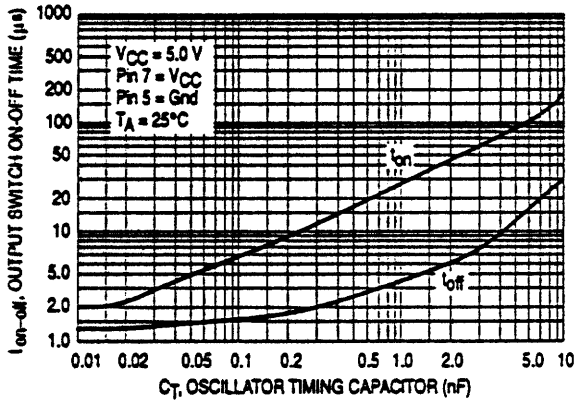


Figure 2. Timing Capacitor Waveform

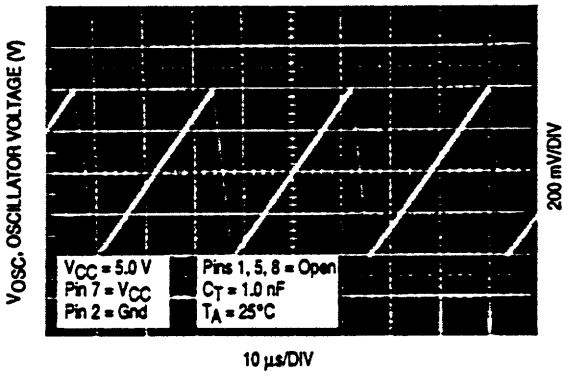


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

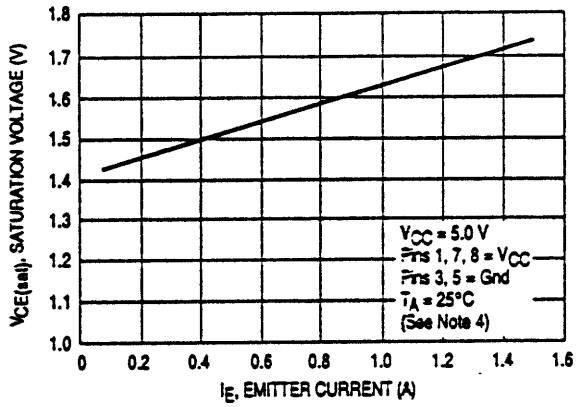


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

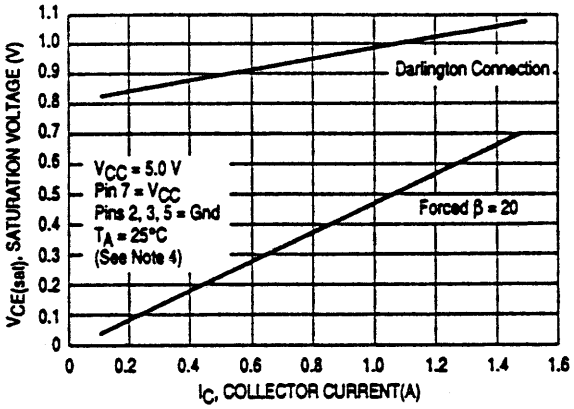


Figure 5. Current Limit Sense Voltage versus Temperature

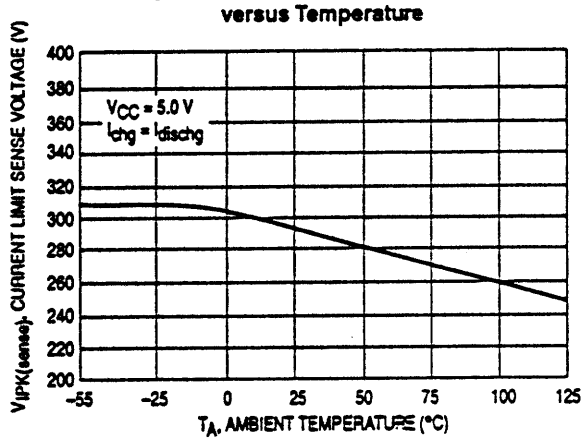
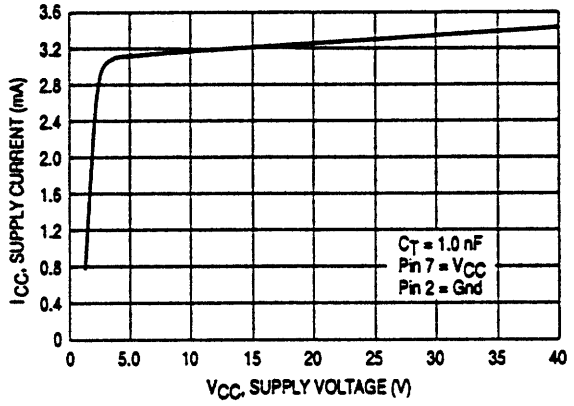
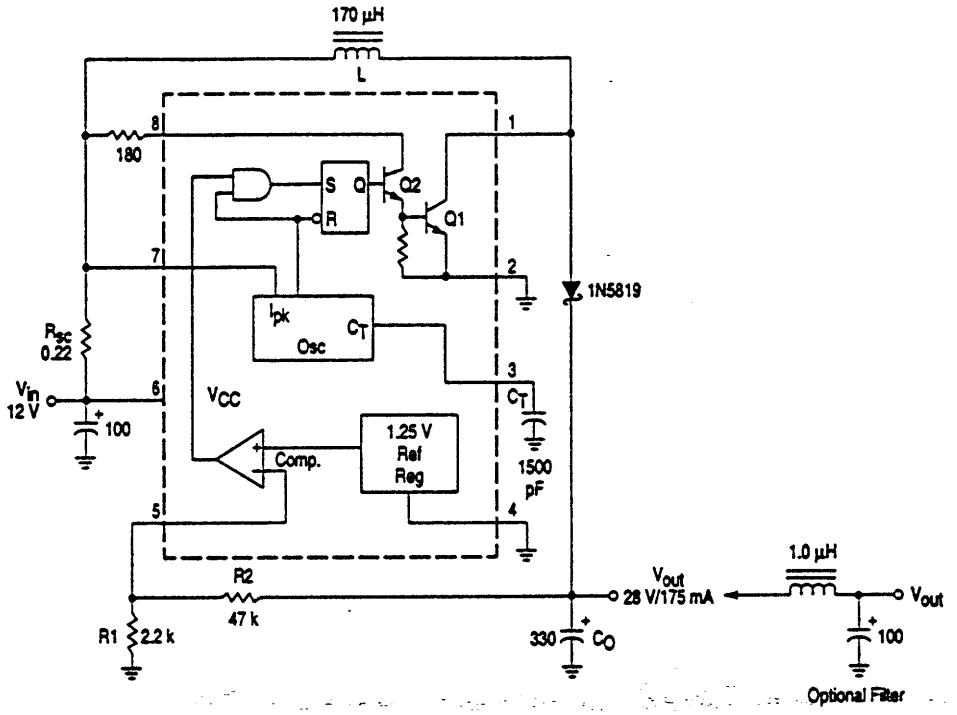


Figure 6. Standby Supply Current versus Supply Voltage



NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

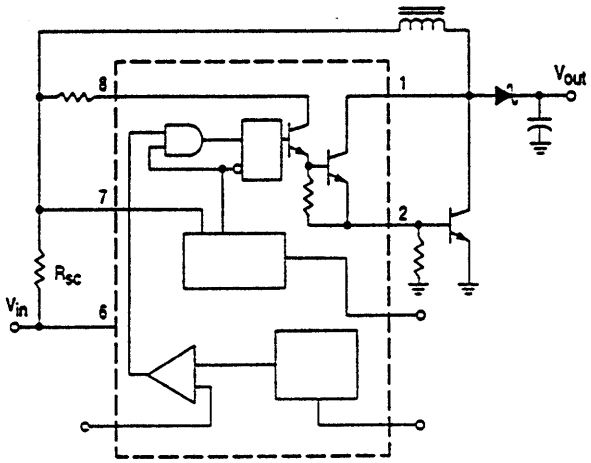
Figure 7. Step–Up Converter



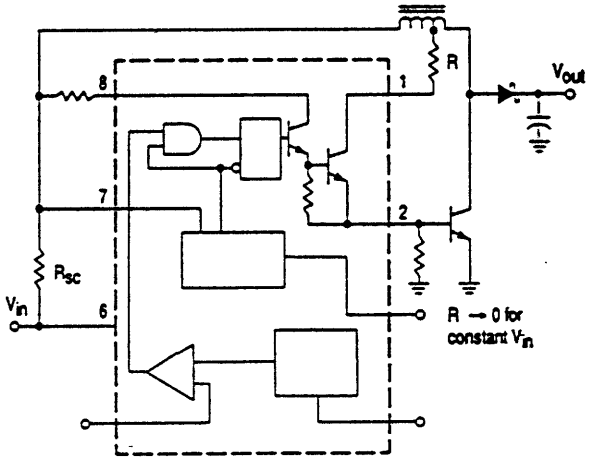
Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

Figure 8. External Current Boost Connections for I_C Peak Greater than 1.5 A

8a. External NPN Switch

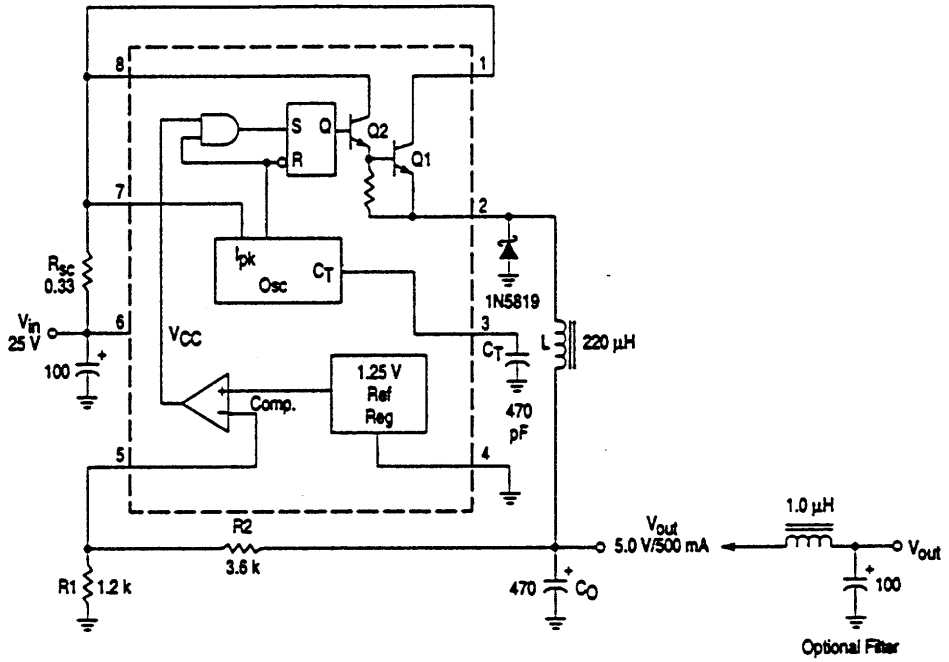


8b. External NPN Saturated Switch
(See Note 5)



NOTE: 5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

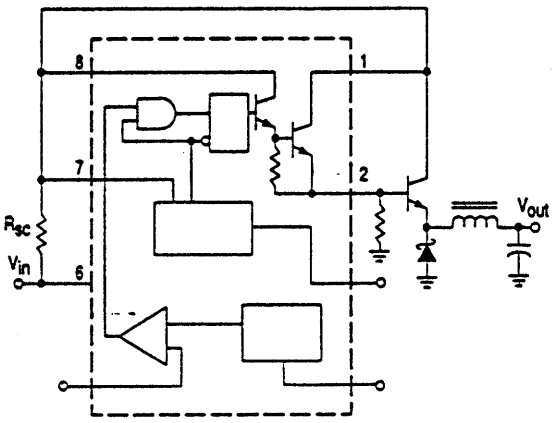
Figure 9. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A

10a. External NPN Switch



10b. External PNP Saturated Switch

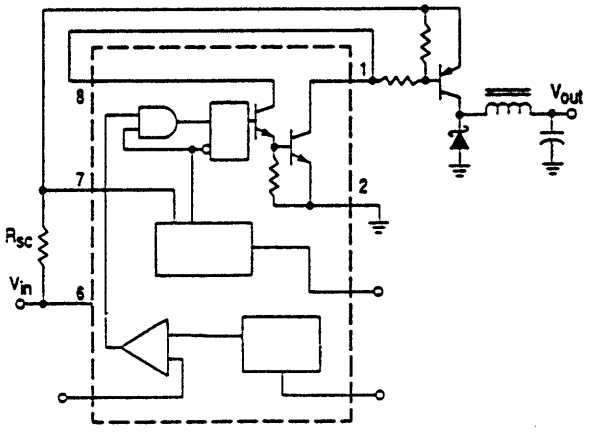
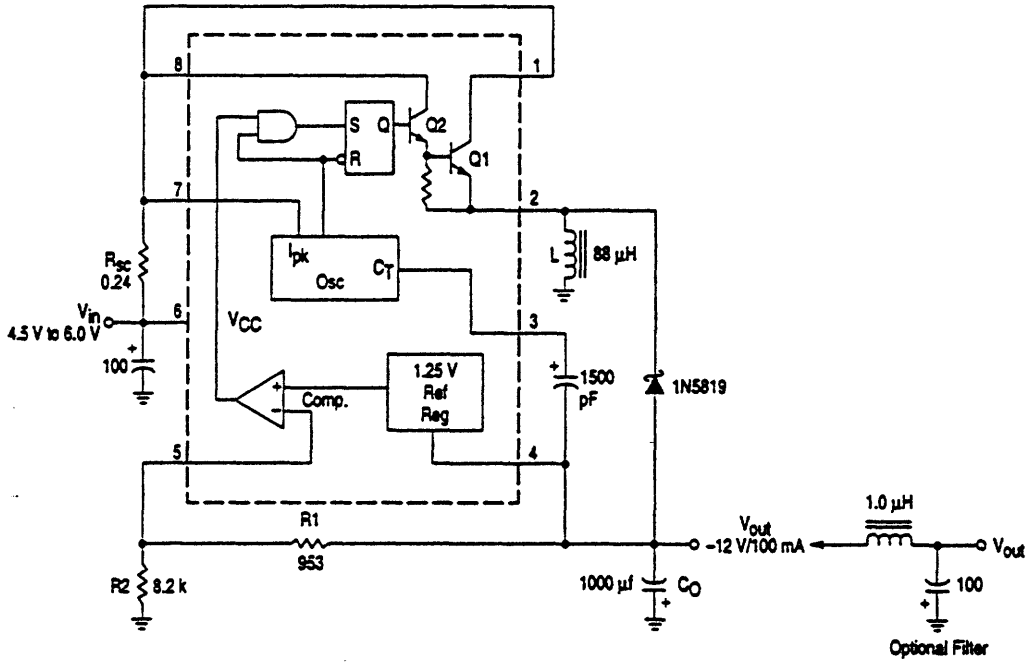


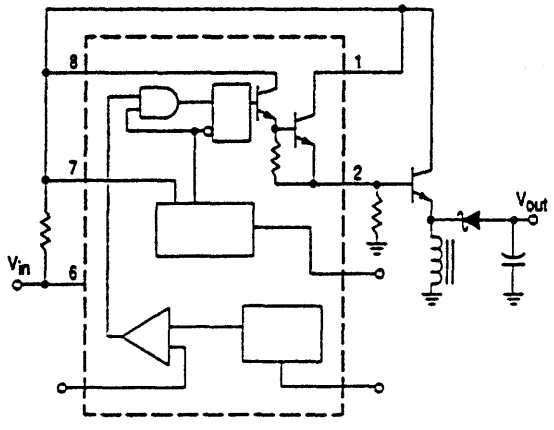
Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

Figure 12. External Current Boost Connections for I_C Peak Greater than 1.5 A

12a. External NPN Switch



12b. External PNP Saturated Switch

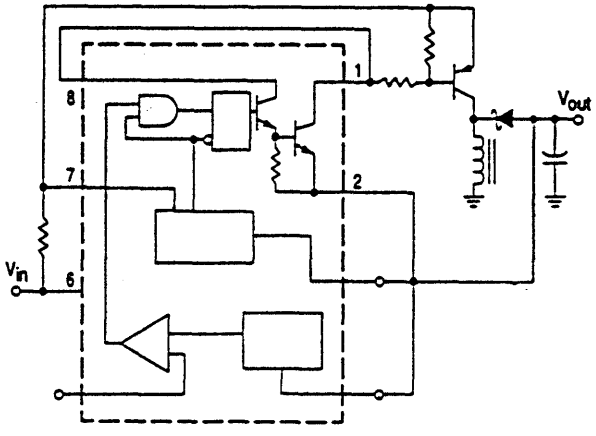
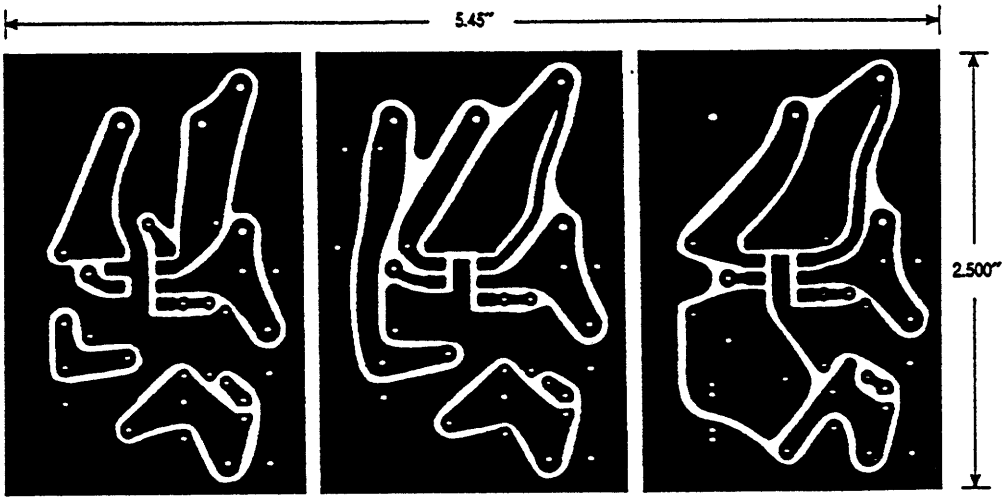
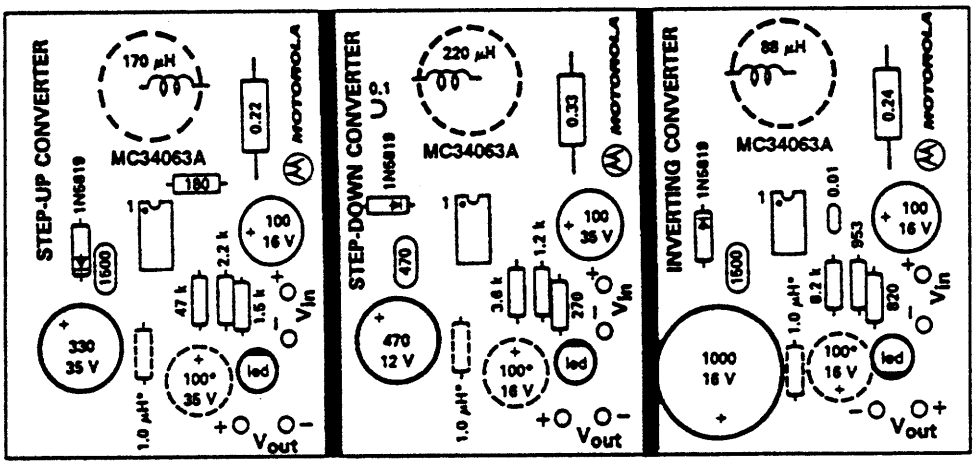


Figure 13. Printed Circuit Board and Component Layout
(Circuits of Figures 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



(Top View, Component Side)

*Optional Filter.

INDUCTOR DATA

Converter	Inductance (µH)	Turns/Wire
Step–Up	170	38 Turns of #22 AWG
Step–Down	220	48 Turns of #22 AWG
Voltage–Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

Figure 14. Design Formula Table

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

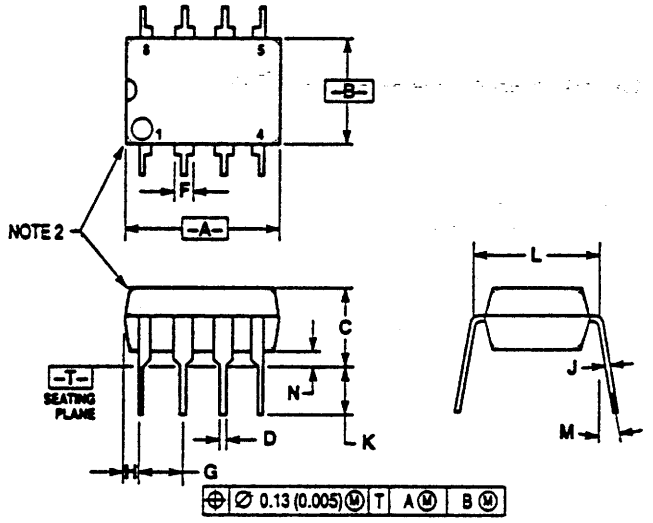
The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $|V_{out}| = 1.25\left(1 + \frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

OUTLINE DIMENSIONS

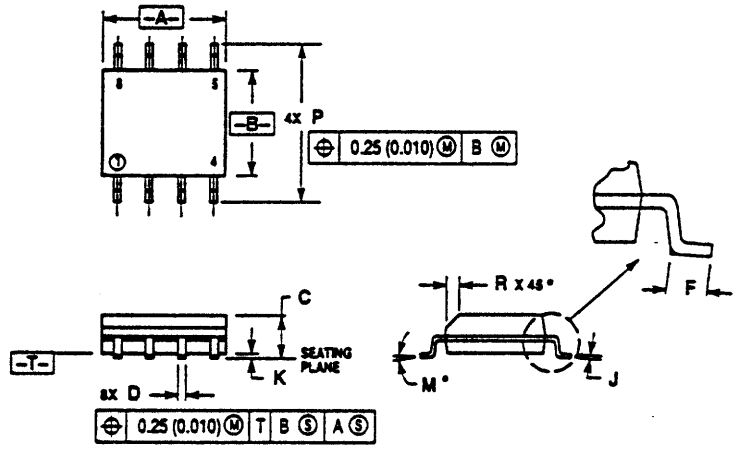
P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE P



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Works Cited

Gray, Paul, and Robert Meyer. Analysis and Design of Integrated Circuits. New York: John Wiley & Sons, Inc., 1993.

Hill, Winfield, and Paul Horowitz. The Art of Electronics. Cambridge University Press, 1995.

Thornton, Richard D. Electronic Circuits: Models, Analysis, Simulation; Intuition and Design. Unpublished.