RF Breakdown Effects in Microwave Power Amplifiers

by

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S.B., Massachusetts Institute of Technology (2006)
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Abstract

Electrical stresses in the transistors of high-efficiency switching power amplifiers can lead to hot-electron-induced "breakdown" in these devices. This thesis explores issues related to breakdown in the Transcom TC2571 PHEMT, and the effects this has on the Draper Laboratory 2.3 GHz microwave power amplifier in which the transistor is used. Characterization of breakdown was performed under DC and RF drive conditions, and shows the surprising role of impact ionization at low temperatures in DC off-state breakdown, as well as the apparent prevalence of on-state breakdown under RF drive. DC characterization shows that breakdown walkout and recovery both proceed more quickly at higher temperatures, and also shows that breakdown stress might lead to the permanent creation of traps that degrade breakdown voltage. Walkout under RF drive decreases amplifier gain at lower levels of RF input drive, but appears to have no negative effect on amplifier saturated output power. The use of temperature-compensated input drive and a diode to clamp negative gate voltage swing are also explored as circuit design techniques that can mitigate device degradation due to breakdown stress.

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There are several other people at Draper I need to thank as well: Jim Keith, for creating the automated measurement setup that was used for characterization of breakdown walkout under RF drive, and for sticking around and debugging the setup during what was an extremely frustrating time; Steve Scoppettuolo and Steve Finberg for their valuable assistance in procuring necessary parts and equipment; and my office-mates Kevin Boyle, Russell Sargent, and Tim Wells for the solidarity and entertainment that they provided.

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Gautham Venkat Arumilli

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Chapter 1

Introduction

1.1 Motivation

A major driving force in the design of portable electronic devices is increasing device energy efficiency. Cellular phones, laptop computers, and portable music players have all been made more energy efficient in recent years due to advances in design and fabrication. As portable communications devices, like cellular phones, become more energy efficient, the power consumed by a device's radio frequency (RF) power amplifier constitutes an increasing portion of a device's energy budget. Within these devices, the RF power amplifier serves to amplify an input signal for transmission. The RF power amplifier does so by converting DC power from a battery to an output RF waveform which drives a device's antenna. Increasing the efficiency of the RF power amplifier in a device can improve the device in many possible ways, including increasing its battery life, increasing its output transmission power, decreasing the amount of heat it produces, and decreasing the size of the device by reducing the size of its battery. The reduction in heat production can also allow the device to be fabricated in a more compact package without negatively affecting its reliability and lifetime.

As RF power amplifier efficiency increases, the electrical stresses on the power transistor in the amplifier tend to increase as well. Specifically, in order to avoid dissipating power in the transistor in high efficiency power amplifiers, the amplifiers

are designed and biased such that the transistor operates like an ideal switch and never conducts a significant amount of current while a large voltage exists across it. Ideally, when the transistor is "on", it conducts current with almost no voltage across it, and when the transistor is "off", it conducts almost no current while there is a voltage across it. As the power amplifier is required to amplify a larger amount of RF power, the bias voltage at the drain of the transistor increases, and the transistor generally has a larger voltage across it in the off state. Similarly, in high-efficiency switching power amplifier topologies like the Class E and Class F topologies, a large drain voltage swing tends to occur in the off state. Additionally, under these high power or high efficiency conditions, larger input drive waveforms are required to switch the transistor, and in the off state, this leads to a large negative voltage at the gate of the transistor. These factors contribute to increased device electrical stress, and can lead to the creation of "hot electrons" in the transistor, which in turn can cause the phenomenon of "breakdown". Breakdown stress can reduce the reliability and performance of the RF power amplifier as transistor performance degrades [1, 2]. Therefore, by mitigating breakdown stress in high efficiency RF power amplifiers, device reliability can be maintained while amplifiers are made more highly efficient at larger levels of RF output power.

This thesis explores issues related to breakdown in a microwave power amplifier designed and fabricated at Draper Laboratory. The amplifier utilizes a pseudomorphic high electron mobility transistor (PHEMT) as its active device. During initial characterization, the amplifier demonstrated significant breakdown effects that have the potential to negatively affect reliability, including breakdown "walkout". The first part of this thesis focuses on characterizing breakdown in this amplifier under DC and RF conditions, including reliability issues related to device walkout and recovery. The second part covers circuit design techniques that might be used to mitigate device degradation caused by breakdown stress, and suggests models that might be used to simulate breakdown.

1.2 Background and Previous Work

1.2.1 High Efficiency RF Power Amplifiers

As mentioned before, RF power amplifiers are used to convert DC power to RF power in order to amplify an input signal to an appropriate level for driving a device's antenna. The basic topology of an RF power amplifier is given in Figure 1-1. The circuit uses a single transistor, although certain RF power amplifier topologies do use more than one. A large inductor, or RF choke, is used to couple the DC power supply to the drain of the transistor for biasing. The choke is used to present an effective open circuit to the drain of the transistor at high frequency. Passive input and output impedance networks are used to connect the drive signal and load, respectively, to the transistor. These networks provide the ability to match impedances at the drive frequency as well as the ability to set impedance characteristics for harmonic components and "shape" the current and voltage waveforms of the transistor.

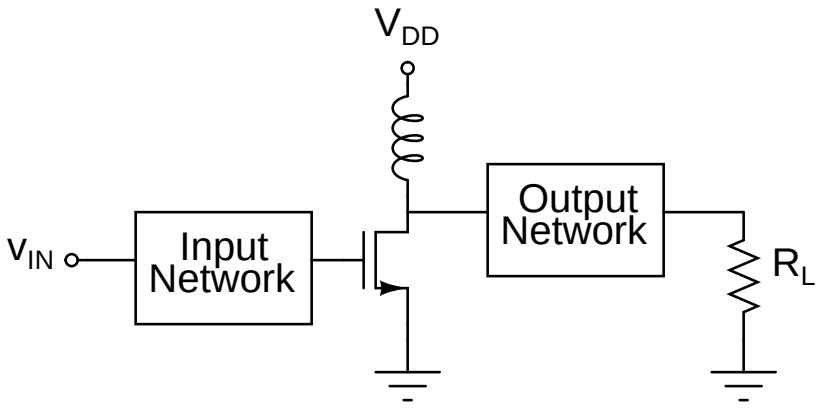

Figure 1-1: A diagram of the basic topology of an RF power amplifier.

Most RF power amplifiers are divided into one of eight classes (lettered "A" through "H") based on their specific network topologies and biasing conditions. Each class of amplifiers has specific benefits and drawbacks related to achievable gain, linearity/distortion, and efficiency. For the purposes of this introduction, it is sufficient to focus on the specific class of RF power amplifiers known as Class E power amplifiers. General principles of operation and design equations for this class of power

amplifiers can be found in [3] and [4]. Class E amplifiers belong to a more general class of RF power amplifiers called switching power amplifiers. Switching power amplifiers operate on the principle that high efficiency can be achieved by driving the transistor in a power amplifier such that it behaves like a switch. In this fashion, the transistor is either conducting a large current (on state) or has a large voltage across it (off state), but never both at the same time, and thus ideally does not dissipate significant power. Due to transistor nonidealities, however, it is inevitable that a transistor will simultaneously have a voltage across it and conduct current during switching transition periods. If these switching transition periods are significant fractions of the RF signal period, then significant power dissipation can occur. The Class E amplifier minimizes this dissipation by using the output network of the amplifier to shape the drain voltage and current waveforms to minimize overlap, thus reducing power dissipation. The Class E amplifier also has the additional feature of achieving zero slope in the drain voltage waveform at transistor turn-on, which guarantees low power dissipation even if the switching transition period is significant and the drain voltage and current waveforms overlap.

Ignoring device non-idealities, an ideal Class E power amplifier would display 100% drain efficiency as no overlap of the drain voltage and current waveforms would occur, and thus no power should be dissipated in the transistor. Typical Class E power amplifier designs have shown drain efficiencies of between 80% and 95%, which is a dramatic improvement on more traditional RF power amplifier topologies [3]. However, a drawback of the Class E topology is the large drain voltage swing that occurs during the off-state, which can lead to increased electrical stress on the device. Like all switching amplifiers, the Class E amplifier is highly non-linear, which can limit its uses for certain applications that require linearity.

A diagram of a lumped element topology (without the input network) for a Class E power amplifier is given in Figure 1-2. Use of a transmission line topology for the input and output networks is also possible, and one such topology is described in [5]. While a transmission line topology provides a relatively simple means of matching impedance at the drive frequency and setting impedance characteristics for harmonics,

it also requires a large amount of area for fabrication. In applications where achieving small size and high density is an ultimate concern, use of a lumped element topology is necessary.

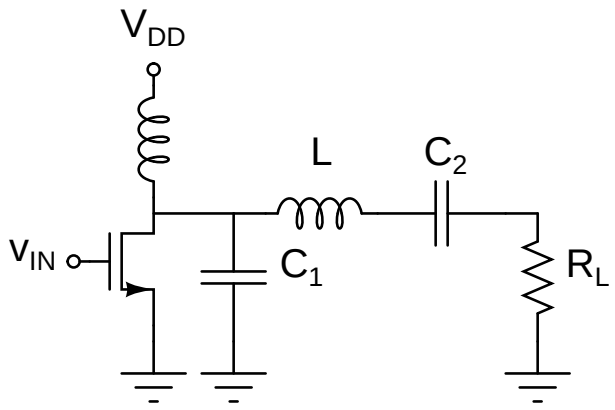

Figure 1-2: A diagram of a lumped element topology for a Class E power amplifier.

1.2.2 Breakdown in GaAs PHEMTs

Several types of transistors are commonly used in high efficiency RF/microwave power amplifier applications, as described in [6]. One of these devices is the GaAs metal semiconductor field-effect transistor (MESFET). The MESFET is a variation on traditional JFET devices where the p–n gate junction is replaced by a metal–GaAs Schottky junction. The GaAs MESFET has higher mobility and lower input capacitance than traditional silicon devices, which allows for operation at much higher frequencies. The high electron mobility transistor (HEMT) is a variation on the MESFET which uses an AlGaAs–GaAs heterojunction for the gate–channel interface to help improve electron mobility, which increases the device's high-frequency response. The pseudomorphic HEMT (PHEMT) is an improvement on the HEMT which uses a very thin layer of InGaAs in between the AlGaAs and GaAs layers of the heterojunction to further increase mobility and the device's high-frequency response. Due to their excellent high-frequency performance, PHEMTs are used in RF/microwave power amplifier applications at frequencies as high as 80 GHz [6].

Like a JFET, a PHEMT has three primary terminals — gate, source, and drain. When the gate–source voltage is sufficiently high, the device is "on", and a current flows in the channel from the drain to the source when a drain–source voltage is applied. In ordinary operation, the gate–source and gate–drain junctions are reverse-biased, and there is a negligible amount of gate leakage current in the device.

Two factors can lead to gate leakage current in a PHEMT device in an RF power amplifier. First, since the gate–source junction behaves like a Schottky junction, when the gate voltage rises and the junction is forward-biased, current can flow from the gate to the source of the device. Second, when a sufficiently large drain–gate voltage is present (typically when the power amplifier is conducting almost no current in its off state), then a large electric field can form across the reverse-biased gate–drain junction, and so-called "hot electron" effects can lead to breakdown of the gate–drain junction and reverse gate leakage current. While forward gate leakage current due to a forward-biased gate–source junction is generally not a damaging effect, the reverse gate leakage current due to breakdown of the gate–drain junction can damage the device.

There are three primary hot-electron mechanisms that are potentially responsible for breakdown in PHEMT devices: tunneling, thermionic field emission, and impact ionization [7, 8]. While the magnitude of the reverse gate current due to each of these mechanisms tends to go up with increasing drain–gate voltage, each of the three mechanisms has different dependences on temperature. Tunneling current does not depend on temperature, thermionic field emission current has a positive temperature coefficient, and, in PHEMT devices, impact ionization current has a negative temperature coefficient. Therefore, by observing the behavior of reverse gate current with respect to temperature, it is possible to determine which mechanism is dominant in a device for a given range of temperature and current [7, 8]. Using this technique, it has been demonstrated in the literature that the dominant mechanisms involved in off-state breakdown in PHEMTs are tunneling (especially at lower temperatures) and thermionic field emission (especially at higher temperatures) [7, 9, 10]. As will be shown later, though, this does not seem to be the case for the device studied in

this thesis.

Breakdown stress leads to the trapping of hot electrons at the extrinsic drain surface, which in turn leads to a reduction of peak electric field for a given drain–gate voltage [10]. As a result, drain–gate off-state breakdown voltage for a given reverse gate leakage current increases with breakdown stress, which in itself is a positive effect. However, the trapping of hot electrons also leads to degradation of device characteristics like small-signal transconductance g_m and RF power gain [10, 11], which can significantly affect the performance of an RF power amplifier. The phenomenon of device degradation during prolonged breakdown stress is known as "breakdown walkout", and is stated by some sources to be a permanent effect [10, 11]. However, once again, as will be discussed later, this does not appear to be the complete case for the device studied in this thesis.

Characterization of off-state breakdown in PHEMTs has generally been performed using two-terminal tests where the source of a device is left floating as the drain–gate voltage is measured for a fixed current injected into the device [10]. This approach is understandable since the drain–gate voltage is the primary factor in off-state breakdown. However, since the transistor is a three-terminal device, it would be ideal to use three-terminal measurements to determine off-state breakdown characteristics. Using the drain-current injection technique described in [12], it was shown in [7] that a gate–source bias voltage can have an impact on the drain–gate breakdown characteristics. In addition to providing drain–gate breakdown voltage, the drain-current injection technique has the advantage of providing a measure of off-state drain–source breakdown voltage, which can provide a more useful figure for design considerations. It has also been shown in [11] that three-terminal stress conditions result in significantly larger breakdown walkout when compared with two-terminal stress conditions.

Breakdown in PHEMTs does not necessarily have to occur when the device is in the off state. On-state breakdown, where a large drain–gate voltage exists while there is a significant drain–source current, can also lead to reverse gate current in PHEMT devices. While not as well documented in the literature as off-state breakdown, there has been work performed on characterizing on-state breakdown in PHEMTs [13].

In general, it has been demonstrated that impact ionization is the dominant factor involved in on-state breakdown [13]. While high-efficiency switching power amplifiers are designed to operate with minimal periods of high drain voltage and high drain current, it is possible that transition between the on state and the off state (and vice versa) may lead to brief periods of operation where on-state breakdown occurs.

1.3 Thesis Overview

As mentioned previously, this thesis focuses on a microwave power amplifier designed and fabricated at Draper Laboratory that demonstrated significant breakdown effects under RF drive in initial characterization. The amplifier is a high-efficiency switching power amplifier designed for use at 2.3 GHz with an output power of 30 dBm[1], and uses a Transcom TC2571 PHEMT as its active device. Transcom declined to provide specific information about the structure of the device, citing the need to protect proprietary information. However, a datasheet is available for the device [14], and figures given for the device include a gate width of 2.4 mm, a gate length of 0.35 μm, and a drain–gate breakdown voltage greater than 15 V for a reverse gate current of 1.2 mA, which corresponds to a current density of 0.5 $^{\mathrm{mA}}/_{\mathrm{mm}}$.

This thesis is organized into six chapters, including this introduction. The five remaining chapters can be roughly organized into three parts. The first part of the thesis covers characterization of breakdown in the amplifier under DC and RF conditions. Chapter 2 covers two-terminal and three-terminal DC characterization across temperature of off-state breakdown in the TC2571. Chapter 3 describes characterization of reverse gate current under RF drive at different bias conditions and temperatures for the complete amplifier. Chapter 4 finishes the first part by looking at breakdown walkout and recovery at different temperatures under DC and RF conditions.

The second part of the thesis covers circuit design techniques that might be used to mitigate device degradation, and modeling. Chapter 5 covers circuit design techniques that might be used to mitigate device degradation and increase reliability by

[1] dBm is a measure of power where p dBm is equivalent to $10^{(p/10)}$ milliwatts.

decreasing breakdown stress in a device. Appendix A suggests models that might be used to describe breakdown for circuit simulation.

The final part of the thesis is the conclusion, contained in Chapter 6. This chapter summarizes the results of the thesis, and provides suggestions for possible future research.

Chapter 2

DC Device Characterization

Since the transistors used in microwave power amplifiers are stressed under RF drive conditions, RF breakdown characterization would be the most meaningful way of determining the relevant device characteristics. However, for a variety of reasons, such measurements tend to be significantly more cumbersome to perform than DC measurements. Additionally, RF measurements tend to yield less meaningful direct data about the device since such measurements often must be performed using observations of a complete power amplifier instead of just the transistor itself. Therefore, it makes sense to characterize the device under DC conditions first, and then to apply the insight gained from these measurements to guide RF characterization.

This chapter represents the first part of this approach and focuses on characterization of off-state breakdown in the Transcom TC2571 PHEMT under DC conditions. The first two sections of this chapter focus on two-terminal (drain–gate) and three-terminal DC characterization of off-state breakdown across a range of currents and temperature. The final section summarizes the results of this chapter.

2.1 Two-Terminal Characterization

Two-terminal DC characterization of the TC2571 involved measurement of the device's drain–gate characteristics while the source was left floating. Each of these tests involved injecting a fixed forward drain current (or reverse gate current) into the de-

vice while measuring the drain–gate voltage V_{DG}. Three separate two-terminal tests were performed, and will be detailed in the following subsections.

2.1.1 Temperature Sweep with Long Sampling Time

The first type of two-terminal characterization performed on the TC2571 involved measurement of drain–gate voltages at reverse gate currents from 230 μA to 1000 μA at temperatures from −32 °C to 71 °C. Since the TC2571 has a gate width of 2.4 mm, this range of currents corresponds to current densities from 0.096 $^{\mathrm{mA}}/_{\mathrm{mm}}$ to 0.417 $^{\mathrm{mA}}/_{\mathrm{mm}}$. Sampling time for these measurements was roughly three seconds, but varied depending on the amount of time required for the voltmeter readings to stabilize. Results of these measurements for two different transistors are shown in Figures 2-1 and 2-2.

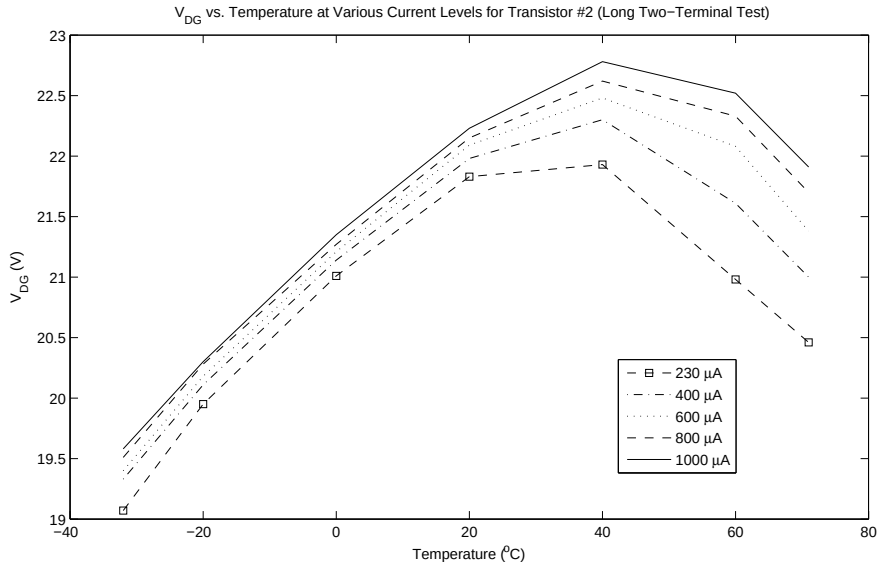

Figure 2-1: Transistor #2 drain–gate voltage V_{DG} versus temperature at various current levels for long sampling time two-terminal test.

Some general trends can be seen in the transistors tested by this method, including those transistors whose characteristics are displayed in the figures. First, for both transistors at the higher current levels, the drain–gate voltage generally has a positive temperature coefficient from −32 °C to 40 °C, and a negative temperature coefficient

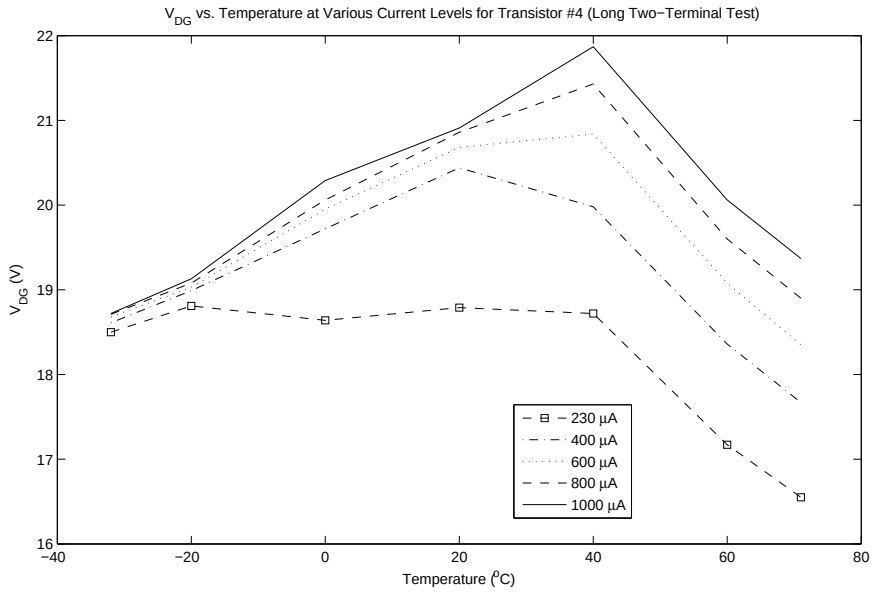

Figure 2-2: Transistor #4 drain–gate voltage V_{DG} versus temperature at various current levels for long sampling time two-terminal test.

from 40 °C to 71 °C. As described in Chapter 1, this gives an indication of which breakdown mechanisms may be responsible for the reverse gate current in the device in a particular range of current and temperature. Reverse gate current due to impact ionization in a PHEMT has a negative temperature coefficient at a fixed drain–gate voltage. Similarly, reverse gate current due to thermionic field emission has a positive temperature coefficient for a fixed drain–gate voltage, and reverse gate current due to tunneling has no temperature coefficient. Thus, for a fixed drain–gate current, we would expect the drain–gate voltage to have a positive temperature coefficient if impact ionization were the dominant mechanism, a negative temperature coefficient if thermionic field emission were the dominant mechanism, and no temperature coefficient if tunneling were the dominant mechanism. For the TC2571 at the higher current levels tested in this two-terminal setup, it would therefore appear that impact ionization is the dominant breakdown mechanism from −32 °C to 40 °C, and that thermionic field emission is the dominant breakdown mechanism from 40 °C to 71 °C.

The second thing that is significant about the device characteristics shown in the figures is that impact ionization appears to be less dominant at the lower current

levels tested than it is at the higher levels. This is especially noticeable in Figure 2-2, where at 400 μA, the negative slope of V_{DG} begins at a lower temperature, and at 200 μA, there appears to be no temperature coefficient between -32 °C to 40 °C (indicating that tunneling is the dominant breakdown mechanism for this current level and temperature range). In general, basic impact ionization theory indicates that impact ionization is proportional to drain current [13], which may provide an explanation for this behavior. This observation about the role of impact ionization at lower current levels will be expanded upon in the results of the two other two-terminal tests.

A final thing to notice about the device characteristics is that while V_{DG} shows the same general behavior with respect to temperature in both devices, there is significant variation in the magnitude of V_{DG} between specific transistors. This is shown for three transistors at a drain–gate current of 1000 μA in Figure 2-3. This device variation is a fundamental consequence of variations in manufacturing the devices, and will be present in all tests performed in this thesis.

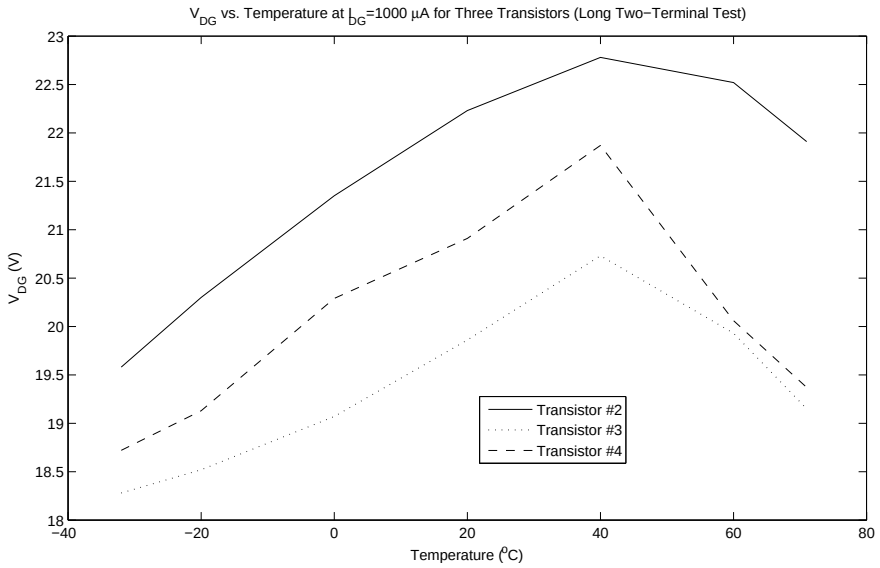

Figure 2-3: drain–gate voltage V_{DG} versus temperature at various current levels for three transistors in the long sampling time two-terminal test.

2.1.2 Temperature Sweep with Short Sampling Time

The second two-terminal test performed on the TC2571 is similar to the first test, but uses a shorter sampling time. Measurements were performed between −32 °C and 71 °C at currents between 230 μA (0.096 $^{\mathrm{mA}}/_{\mathrm{mm}}$) and 1200 μA (0.500 $^{\mathrm{mA}}/_{\mathrm{mm}}$) using a sampling time of 25 ms. A shorter sampling time was used to determine if the longer sampling time in the first test had affected device characteristics. A plot of drain–gate voltage vs. temperature at different current levels for one of the transistors tested is given in Figure 2-4.

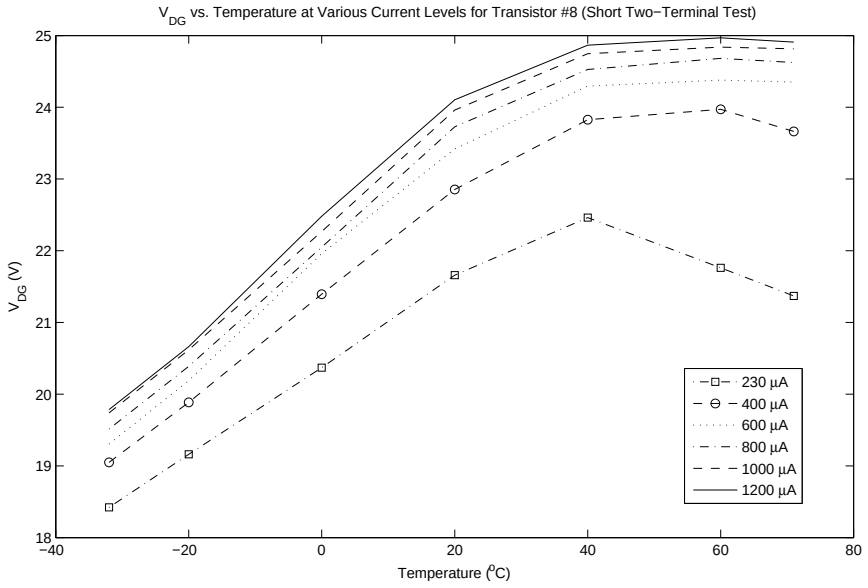

Figure 2-4: Transistor #8 drain–gate voltage V_{DG} versus temperature at various current levels for short sampling time two-terminal test.

The most notable thing about Figure 2-4 when compared to the transistors in the first test is the fact that V_{DG} no longer has a negative slope at higher temperatures for the higher current levels. Impact ionization still appears to be prevalent at lower temperature for these current levels, as indicated by the positive slope of V_{DG}, but the traces of V_{DG} flatten out from 40 °C to 71 °C, indicating that tunneling is the dominant breakdown mechanism in this temperature range. For the test with shorter sampling time, it now appears that thermionic field emission is no longer the dominant

factor in reverse gate current for the higher current levels at higher temperature. A reason for this behavior will be given in Chapter 4, where a degradation in drain–gate breakdown voltage under prolonged stress will be shown at higher temperatures.

A second notable feature about Figure 2-4 is the behavior of V_{DG} at the lower current levels. As with the first test, it appears that impact ionization may be less dominant at lower current levels as V_{DG} has a smaller positive slope at lower temperatures at the lower current levels. Second, at 200 μA and 400 μA, V_{DG} shows a negative slope at higher temperatures, although less noticeably than in the first test. This indicates that for higher temperatures, thermionic field emission is the dominant breakdown mechanism at lower current levels (while tunneling is dominant at higher current levels). This two-terminal behavior for PHEMTs, where tunneling is the dominant breakdown mechanism for higher current levels while thermionic field emission is dominant at lower current levels, is also demonstrated in [7] and [8].

2.1.3 Broad Current Sweep at Different Temperatures

The final two-terminal DC test performed on the TC2571 is derived from the methodology presented by Somerville and del Alamo in [8]. The test involves measuring the device's drain–gate voltage across a broad range of current to obtain the device's drain–gate "diode characteristics", and then comparing diode characteristics at different temperatures to determine which mechanisms are responsible for breakdown in a given range of temperature and current. In this test, diode characteristics were measured for reverse gate currents between 240 pA (100 $^{\mathrm{pA}}/_{\mathrm{mm}}$) and 24 mA (10 $^{\mathrm{mA}}/_{\mathrm{mm}}$) and at temperatures between -32 °C and 70 °C.

Figure 2-5 shows drain–gate diode characteristics at 60 °C and 70 °C for the transistor used in this test. As indicated in [8], this plot is characteristic for a range of temperature and current where reverse gate current is dominated by tunneling/thermionic field emission. For a given drain–gate voltage, the drain–gate current is always larger at the higher temperature. Furthermore, for higher drain–gate voltages, the ratio of current at the higher temperature to current at the lower temperature gets closer to 1 as tunneling current becomes a larger component of reverse gate current. This

is consistent with the observation of device behavior in the previous two-terminal tests, where reverse gate current appeared to be dominated by thermionic field emission or tunneling at higher temperatures. It matches especially well with the second test, where reverse gate current at higher temperatures appeared to be dominated by tunneling at the higher current levels and thermionic field emission at the lower ones.

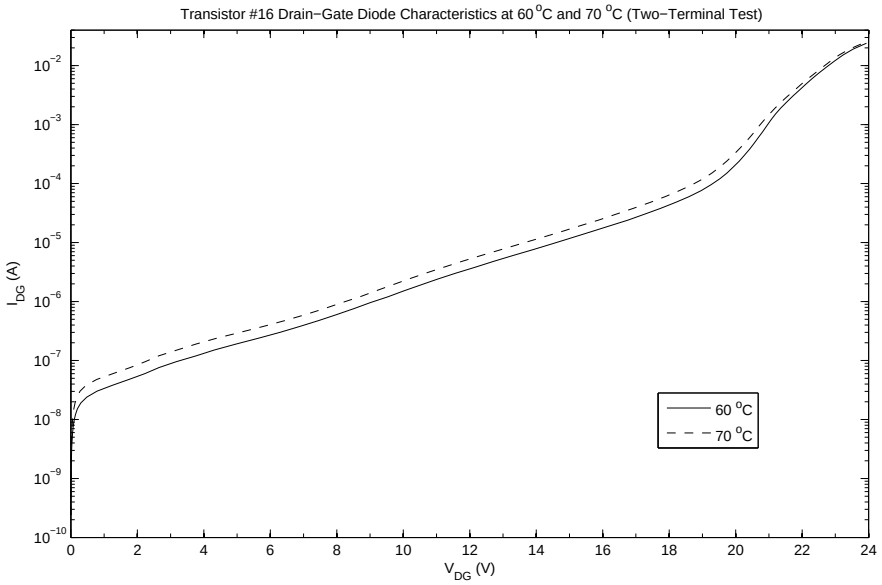

Figure 2-5: Transistor #16 drain–gate diode characteristics at 60 °C and 70 °C.

Figure 2-6 shows drain–gate diode characteristics of the same transistor at −32 °C, −20 °C, and 0 °C. As with Figure 2-5, at lower voltages, the current is always larger at higher temperature. However, unlike Figure 2-6, at higher voltages, the traces "cross over": for a given drain–gate voltage, the current is now smaller at higher temperature. According to [8], this cross-over behavior for PHEMTs is characteristic of a range of temperature and current where impact ionization is dominant. Thus, for low temperatures, it appears that tunneling/thermionic field emission is dominant for reverse gate currents less than about 1 μA (and drain–gate voltages less than 15 V), and that impact ionization is dominant at these temperatures for higher currents. This is consistent with observations in the previous two-terminal tests which indicated that impact ionization was dominant at lower temperatures for reverse gate currents

between 230 μA and 1200 μA.

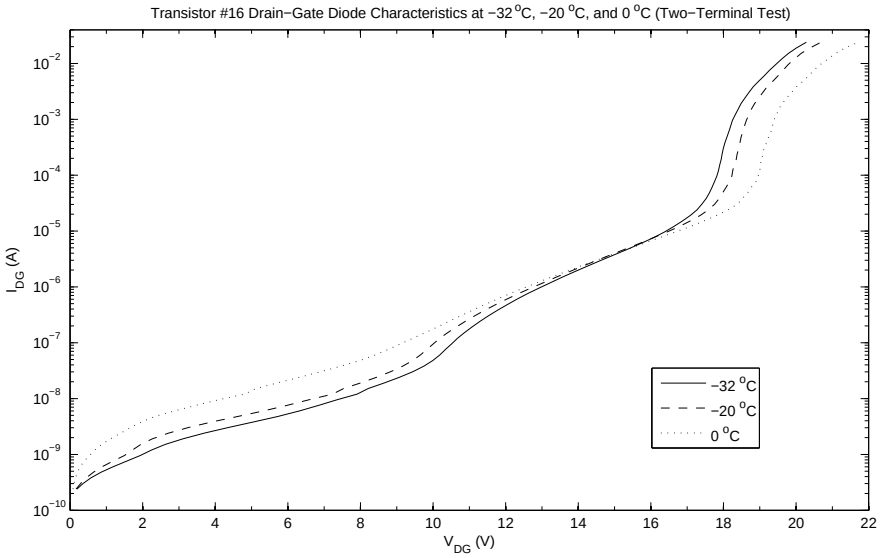

Figure 2-6: Transistor #16 drain–gate diode characteristics at −32 °C, −20 °C, and 0 °C.

2.1.4 Summary of Two-Terminal Characterization

All three two-terminal DC off-state breakdown tests on the TC2571 show some common results. At low temperature and sufficiently high reverse gate current, the dominant breakdown mechanism is impact ionization. This can be seen in the positive temperature coefficient of drain–gate voltage for a fixed reverse gate current in this region. At lower currents or higher temperatures, the dominant component of reverse gate current is tunneling/thermionic field emission. Furthermore, as the reverse gate current is decreased, the transition between the range where impact ionization dominates and the range where tunneling/thermionic field emission dominates occurs at a lower temperature. Finally, when tunneling/thermionic field emission dominates reverse gate current, tunneling tends to play a larger role at higher current levels while thermionic field emission plays a larger role at lower current levels.

The fact that impact ionization appears to be the dominant breakdown mechanism for lower temperatures and higher currents in the two-terminal tests is surprising. As

mentioned in Chapter 1, the literature suggests that tunneling and thermionic field emission are the dominant mechanisms involved in off-state breakdown in PHEMTs, and that drain–gate voltage should monotonically decrease with increasing temperature for a fixed reverse gate current. The experiments in the literature that demonstrate this cover temperatures between −50 °C and 50 °C and reverse gate current densities up to 1 $^{\mathrm{mA}}/_{\mathrm{mm}}$ [9], which easily covers the range of temperatures and currents where we see the effect of impact ionization in the two-terminal tests of the TC2571.

Aside from the literature, the fact that impact ionization appears to be a dominant breakdown mechanism in the two-terminal tests of the TC2571 is also surprising because impact ionization is fundamentally a three-terminal mechanism. Impact ionization in a PHEMT occurs when a hot electron loses energy in the channel and creates a new pair of charge carriers, an electron and a hole. A fraction of these holes leave the channel through the gate, which leads to reverse gate current [13]. Thus, impact ionization requires hot electrons to be conducting in the channel between the drain and the source, which would not appear to be the case in the two-terminal tests here where the source is left floating. A possible mechanism for how this impact ionization current arises is described in Appendix A.

2.2 Three-Terminal Characterization

Three-terminal DC characterization of off-state breakdown in the TC2571 is based on the drain-current injection technique developed by Bahl and del Alamo and described in [12]. The drain-current injection technique, which was touched upon briefly in Chapter 1, involves injecting a fixed current into the drain of the device while sweeping the gate–source voltage from above threshold to below it. The drain–gate voltage when the drain current equals the reverse gate current (that is, where the source current is zero) is termed the drain–gate breakdown voltage ($\mathrm{BV_{DG}}$). The maximum drain–source voltage achieved is termed the drain–source breakdown voltage ($\mathrm{BV_{DS}}$).

Three-terminal DC testing on RF power transistors is notoriously difficult for a

number of reasons. Most significantly, since RF power transistors tend to have high gain when in the on state, they tend to oscillate when there is a sufficiently high gate–source voltage unless a sophisticated and difficult impedance-matching setup is used to stabilize them. This was observed for PHEMTs in [7], and was also observed for the TC2571 devices tested in this thesis. This oscillatory behavior would not be troublesome if it were not destructive since the relevant measurements are made with the device in the off state. Unfortunately, the oscillatory behavior has a tendency to eventually burn out the device being tested, which renders the device useless. This was the case for essentially all of the TC2571 devices tested, and as a result, it was possible to only get data across the full range of temperature and current for one device. The characterization of this specific device will be presented in the rest of this section.

A plot of BV_{DG} versus temperature for drain currents between 200 μA (0.083 $^{mA}/_{mm}$) and 1200 μA (0.500 $^{mA}/_{mm}$) is given in Figure 2-7. This plot resembles the plots of V_{DG} derived from the first two-terminal characterization test where impact ionization appears to dominate reverse gate current in this range of currents for temperatures between -32 °C and 40 °C and thermionic field emission appears to dominate for temperatures between 40 °C and 70 °C.

A plot of BV_{DS} for the same temperatures and currents is given in Figure 2-8. At high temperatures, the plot of BV_{DS} appears similar to the plot of BV_{DG} where BV_{DS} increases with increasing drain current. However, this is inverted at low temperatures, where BV_{DS} actually decreases with increasing drain current. The reason for this can be seen in Figures 2-9 and 2-10. Figure 2-9 shows drain–source voltage versus gate–source voltage for the values of drain current tested at -32 °C. For a higher drain current, the device leaves the on state (and the region of oscillatory behavior) at a lower V_{GS}, and since V_{DS} is so closely "spaced" together for the different drain currents at this temperature, the maximum value of V_{DS} is actually smaller for a higher drain current. Figure 2-10 is similar to 2-9, but at 70 °C. In this case, even though the device still leaves the on state at a lower V_{GS} for a higher drain current, V_{DS} is "spaced" far enough apart at the different current levels such that the maximum value of V_{DS} is

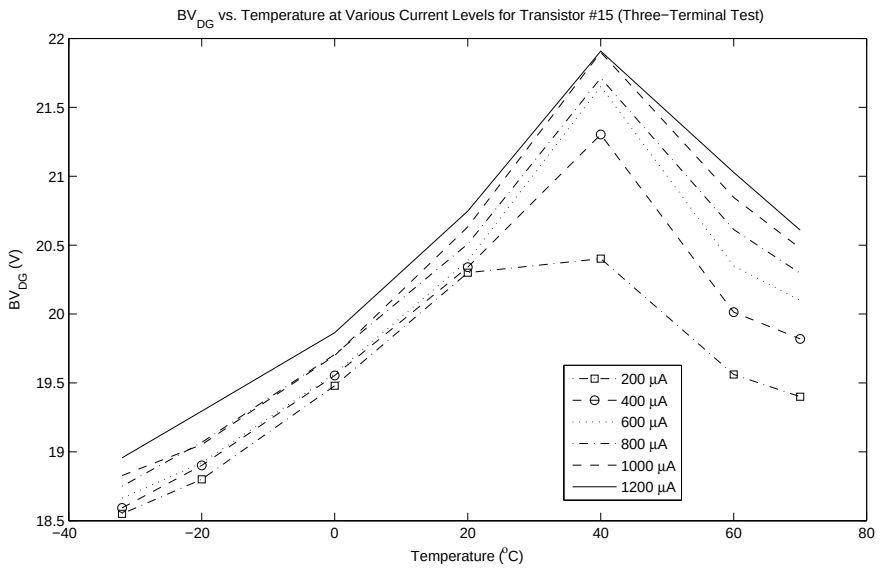

Figure 2-7: Transistor #15 drain–gate breakdown voltage BV_{DG} versus temperature at various drain current levels for three-terminal test.

greater for a higher drain current. Regardless of this behavior though, at each fixed value of drain current, the plot of BV_{DS} shows a positive temperature coefficient at lower temperatures and a negative temperature coefficient at higher temperatures, which once again indicates that impact ionization is dominant at lower temperatures while thermionic field emission is dominant at higher temperatures. Furthermore, the plots of BV_{DS} and BV_{DG} appear to again show that impact ionization is less dominant at lower current levels.

Figure 2-11 shows a plot of V_{DG} versus V_{GS} for a drain current of 1200 μA at -32 °C and 70 °C. A noticeable difference between the traces at the two temperatures is the noisiness of V_{DG} at -32 °C when compared to the trace at 70 °C. This noisiness was noticed in three-terminal characterization of the transistor at lower temperatures, and may be characteristic of the fact that impact ionization appears to be the dominant breakdown mechanism at lower temperatures while thermionic field emission appears to be dominant at higher temperatures.

Another key feature of Figure 2-11 is that V_{DG} is essentially constant with respect to V_{GS} at both temperatures once the transistor enters the off state. In general, this

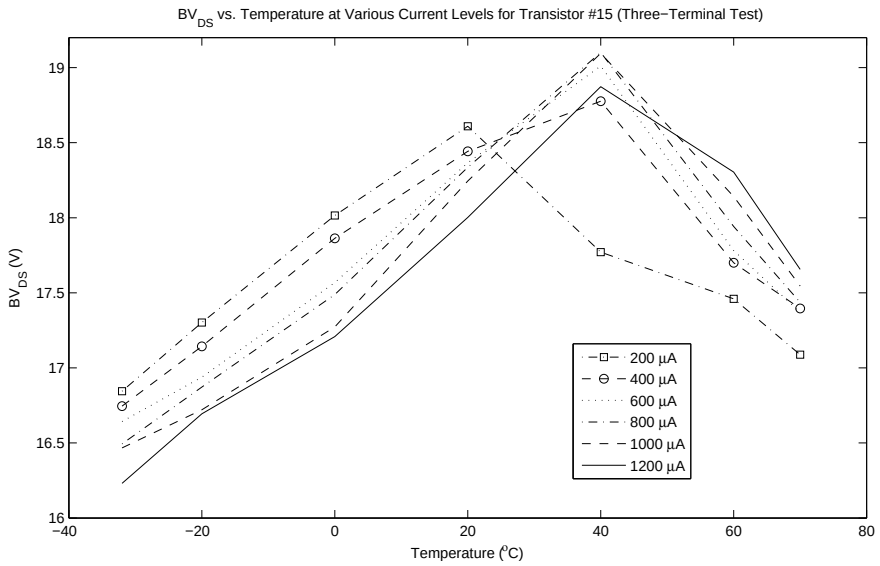

Figure 2-8: Transistor #15 drain–source breakdown voltage $\mathrm{BV_{DS}}$ versus temperature at various drain current levels for three-terminal test.

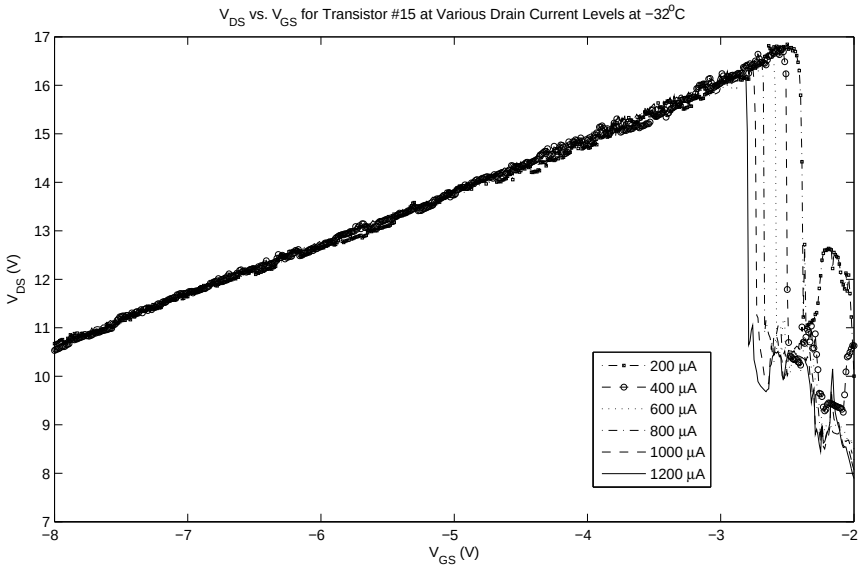

Figure 2-9: Transistor #15 drain–source voltage $\mathrm{V_{DS}}$ versus gate–source voltage $\mathrm{V_{GS}}$ at -32 °C for various drain current levels in the three-terminal test.

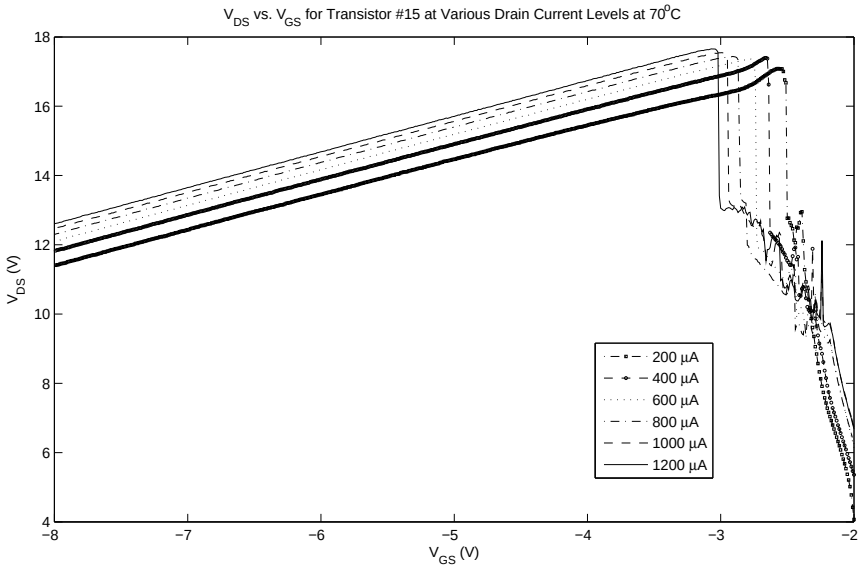

Figure 2-10: Transistor #15 drain–source voltage V_{DS} versus gate–source voltage V_{GS} at 70 °C for various drain current levels in the three-terminal test.

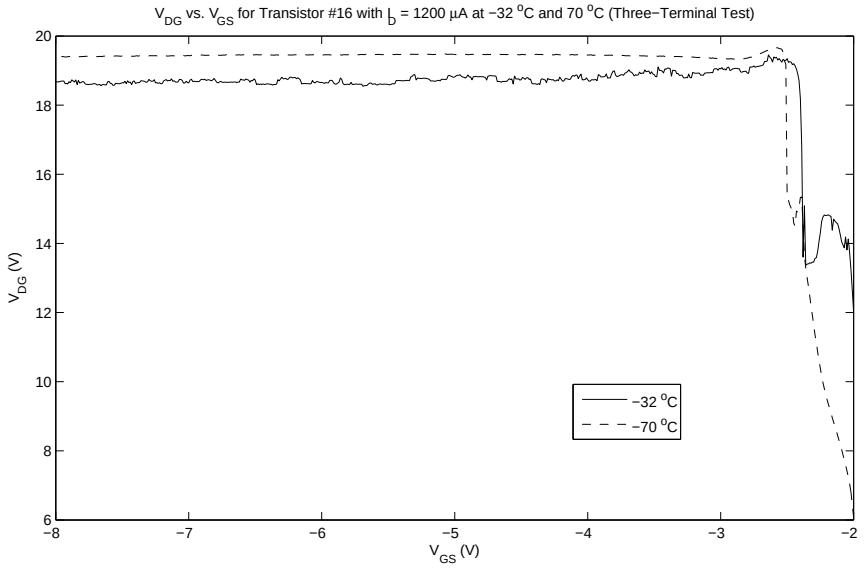

Figure 2-11: Transistor #15 drain–source voltage V_{DG} versus gate–source voltage V_{GS} at -32 °C and 70 °C for a drain current of 1200 μA in the three-terminal test.

was found to be true for the transistor at all currents and temperatures tested. This is notable because a significant effect on V_{DG} by V_{GS} in the off state for PHEMTs was demonstrated by [7] in the range of drain current considered in this thesis. The paper concludes that the ratio of gate length to depletion region extension is the major factor in determining whether V_{GS} has an impact on V_{DG}. Shorter gate length devices tend to show more of the "source effect" where decreasing V_{GS} causes the value of V_{DG} to decrease for a fixed drain current. The PHEMT device considered in [7] has a gate length of 0.25 μm while the TC2571 PHEMT considered in this thesis has a gate length of 0.35 μm [14], which may contribute to the lack of source effect. Without more specific information from the manufacturer about the device's structure and composition, though, it is difficult to determine exactly why the source effect is not demonstrated in this transistor.

2.3 Summary

This chapter presented results from the two-terminal and three-terminal DC tests that were used to characterize off-state breakdown in the TC2571 PHEMT. Results from all of these tests suggest that impact ionization is the dominant mechanism responsible for off-state breakdown at lower temperatures, especially at higher levels of reverse gate current. At higher temperatures, the dominant breakdown mechanism appears to be tunneling/thermionic field emission. In this case, tunneling appears to play a larger role at higher levels of reverse gate current, while thermionic field emission appears to be more dominant at lower levels of reverse gate current. The three-terminal test also appeared to show little of the "source effect" that was documented for some PHEMTs in the literature.

The fact that impact ionization appears to be dominant in off-state breakdown at lower temperatures for the TC2571 is surprising since this contradicts much of the existing literature on off-state breakdown in PHEMTs. It is also surprising because impact ionization is fundamentally a three-terminal mechanism that requires hot electrons traveling from the drain to the source. A possible explanation and model

for this behavior is given in Appendix A.

Chapter 3

RF Device Characterization

This chapter represents the second part of the approach outlined at the beginning of Chapter 2, and focuses on characterization of breakdown in the TC2571 PHEMT under RF drive. Specifically, this chapter describes measurements made of average reverse gate current in the Draper 2.3 GHz microwave power amplifier across a range of RF input drive levels, temperatures, and biasing conditions. This chapter consists of five sections. The first section covers measurements made under nominal bias conditions, while the second and third sections describe the effects of varying the drain bias voltage and the gate bias voltage, respectively. The fourth section describes the role that on-state breakdown may play in operation of the amplifier under RF drive based on the measurements made in the first three sections. The final section summarizes the results of the chapter.

3.1 Measurements With Nominal Bias

The Draper 2.3 GHz amplifier was designed for use under nominal bias conditions where the gate of the TC2571 is biased at -1.70 V and the drain is biased at 7.00 V. During characterization of breakdown under RF drive in the amplifier, measurements of average reverse gate current in the TC2571 were made by measuring the current supplied from the gate DC power supply at temperatures between -32 °C and 71 °C and RF input drive between 12.50 dBm and 16.00 dBm. For nominal bias conditions,

plots of average reverse gate current with respect to temperature at RF input drive levels of 13.00 dBm, 14.00 dBm, 15.00 dBm, and 16.00 dBm are given in Figure 3-1 for one amplifier and in Figure 3-2 for a second amplifier.

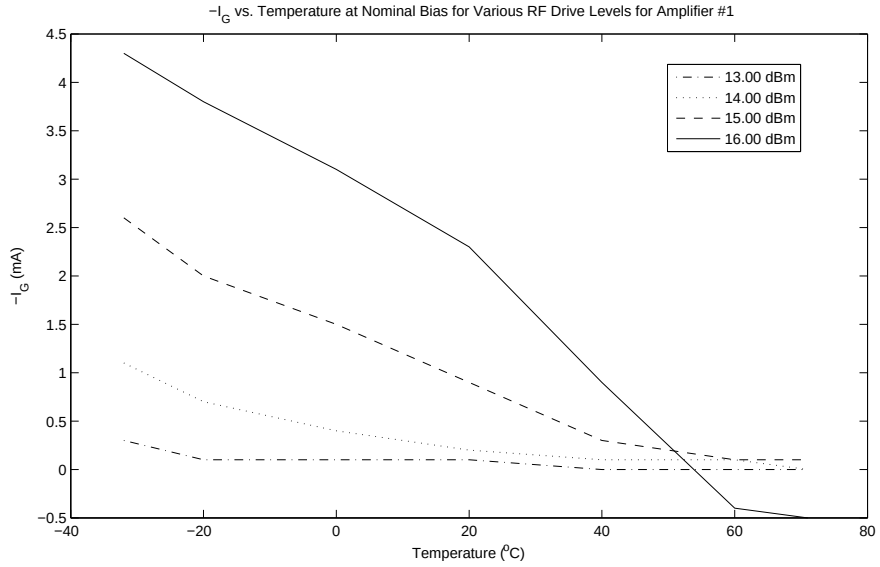

Figure 3-1: Amplifier #1 average reverse gate current $-I_G$ versus temperature at various levels of RF input drive with nominal bias conditions.

For both amplifiers and at all levels of RF input drive, reverse gate current decreases monotonically as temperature increases. This behavior is characteristic of impact ionization being the dominant breakdown mechanism in this region of operation. This is similar to the results seen in Chapter 2 for the DC characterization of off-state breakdown, where impact ionization was the dominant breakdown mechanism at lower temperature in the TC2571 PHEMT. In this case, though, it appears that under nominal bias conditions, impact ionization is dominant in breakdown under RF drive at all temperatures. This observation will be expanded upon in Section 3.4, where the possible role of on-state breakdown will be discussed.

A complication involved in using measurements of average reverse gate current to characterize breakdown in the TC2571 under RF drive is the forward gate current that arises due to forward biasing of the gate–source junction during positive swings of the gate voltage. The presence of forward gate current in this amplifier can be clearly

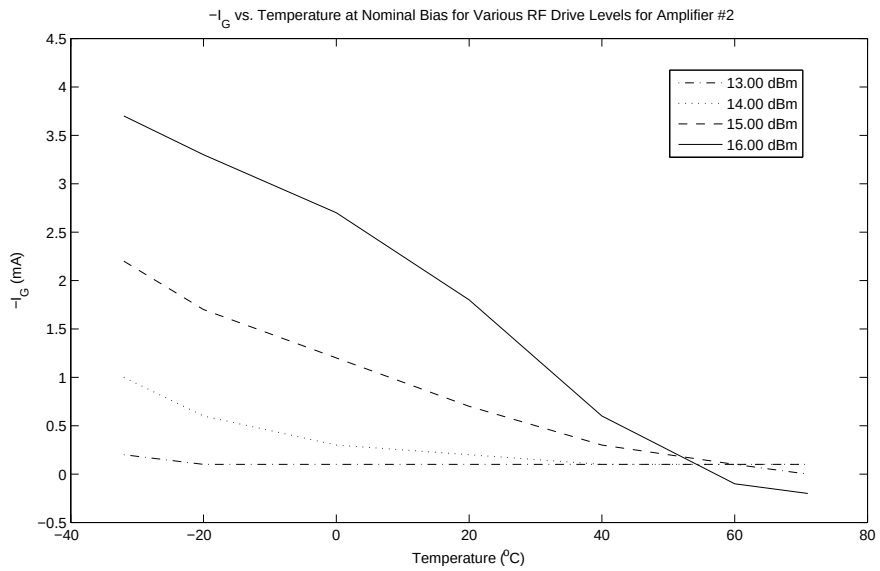

Figure 3-2: Amplifier #2 average reverse gate current $-I_G$ versus temperature at various levels of RF input drive with nominal bias conditions.

seen in both Figures 3-1 and 3-2, where the average reverse gate current becomes negative for an input RF drive of 16.00 dBm at higher temperature, indicating that the average gate current in this region of operation is positive. This forward diode current increases with increasing temperature, which would make it more difficult to determine whether a decrease in reverse gate current with increasing temperature is primarily the result of impact ionization being dominant in breakdown under RF drive, or if it is primarily the result of increasing forward gate–source diode current. However, since we would expect both the reverse impact ionization current and the forward diode current to increase with increasing input RF drive, it is possible to separate the regions of operation where each is the dominant component of gate current by looking at the change in reverse gate current across RF input drive at fixed temperature. A plot of reverse gate current versus RF input drive at temperatures of -32 °C, 0 °C, 40 °C, and 71 °C for nominal bias is given in Figure 3-3.

At all temperatures except 71 °C, reverse gate current increases with drive level, which indicates that the reverse impact ionization current dominates at these temperatures for the range of input RF drive considered. Even at 71 °C, reverse gate

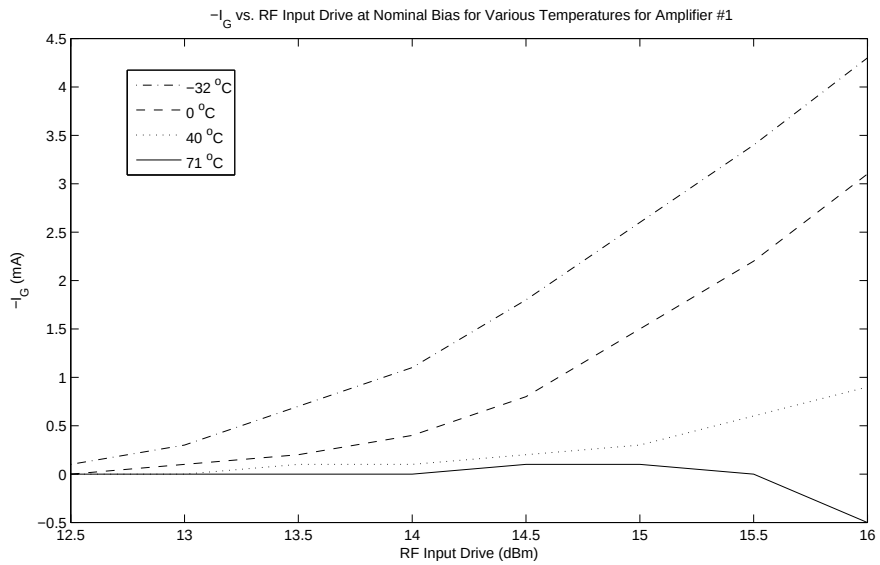

Figure 3-3: Amplifier #1 average reverse gate current $-\mathrm{I_G}$ versus RF input drive at various temperatures with nominal bias conditions.

current does not begin to decrease until the higher levels of RF input drive. Thus, in general, it appears that forward gate–source diode current is not a major factor in overall average gate current except in regions of operation with high temperature and high levels of RF input drive. In general, this was observed to be true of all measurements of reverse gate current under RF drive described in this chapter.

Finally, the TC2571 transistors selected for use in the two amplifiers were closely matched under two-terminal DC off-state breakdown characterization at 20 °C for reverse gate current levels between 600 μA and 1200 μA. The characteristics shown in Figures 3-1 and 3-2 are similar, and show the same general trends, but are not quite identical. This presence of device variation is similar to what was noted in Chapter 2 about DC device characterization with multiple transistors. All of the tests in this chapter were performed on both amplifiers, and show the same general trends for both amplifiers.

3.2 Measurements With Varied Drain Bias

In order to determine the effects of drain bias on breakdown under RF drive, measurements were made of amplifier reverse gate current using drain bias voltages of 6.50 V and 7.50 V. Plots of reverse gate current across temperature at drain bias voltages of 6.50 V, 7.00 V, and 7.50 V are given in Figure 3-4 for 14.00 dBm RF input drive and in Figure 3-5 for 15.00 dBm RF input drive.

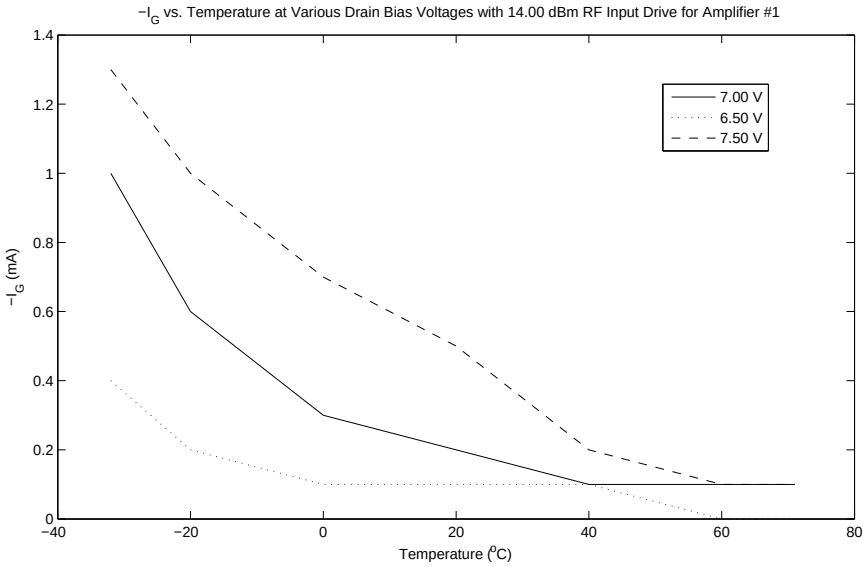

Figure 3-4: Amplifier #1 average reverse gate current $-I_G$ versus temperature at various drain bias voltages with 14.00 dBm RF input drive.

Both plots show increased reverse gate current with increasing drain bias voltage, which is as expected. Increasing the drain bias voltage of the amplifier causes the output power of the amplifier to increase and also increases the voltage swing at the drain of the transistor. This in turn increases drain–gate voltage stress in the transistor, which leads to increased reverse gate current. Furthermore, both plots show that the negative temperature coefficient of reverse gate current is present for each bias voltage tested, which once again indicates that impact ionization is dominant in breakdown under RF drive in the region of operation tested.

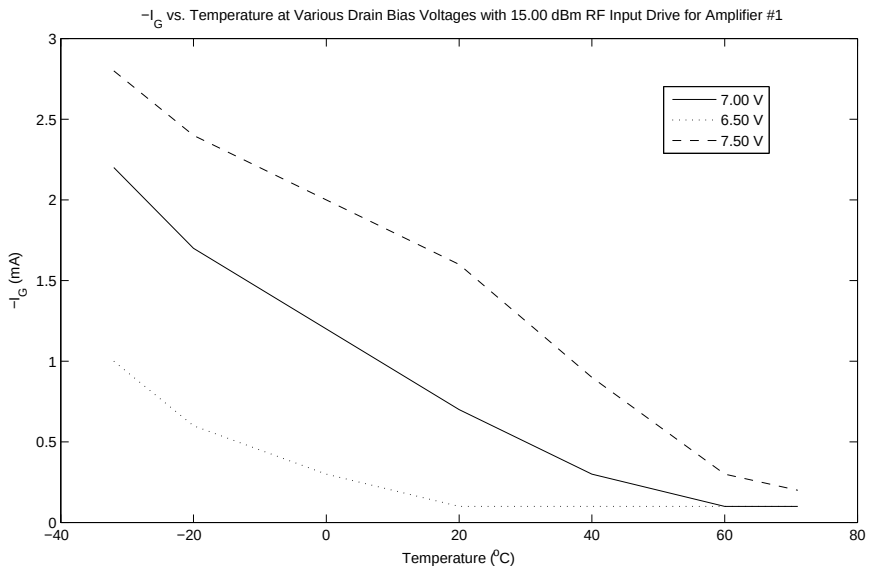

Figure 3-5: Amplifier #1 average reverse gate current $-I_G$ versus temperature for various drain bias voltages with 15.00 dBm RF input drive.

3.3 Measurements With Varied Gate Bias

Measurements were also made to determine the effects of gate bias on breakdown under RF drive. Gate bias voltages of −1.65 V, −1.70 V, and −1.75 V were used. A plot of reverse gate current across temperature for these gate bias voltages and 15.00 dBm RF input drive is given in Figure 3-6.

The plot in Figure 3-6 shows no consistent effect of gate bias voltage on reverse gate current. We might expect that decreasing the gate bias voltage would increase drain–gate voltage stress and that higher levels of reverse gate current would therefore be present for a more negative gate bias. This is not the case, and at high temperature, the opposite effect is present where decreasing the gate bias actually decreases the reverse gate current. At lower temperature, the reverse gate current at a gate bias voltage of 1.70 V is greater than the reverse gate current at either of the other bias voltages.

The reason for these effects is that changing the gate bias voltage dramatically affects the output power of the amplifier for a given level of RF input drive. Increasing the gate bias voltage tends to increase the gain of the amplifier at higher temperature,

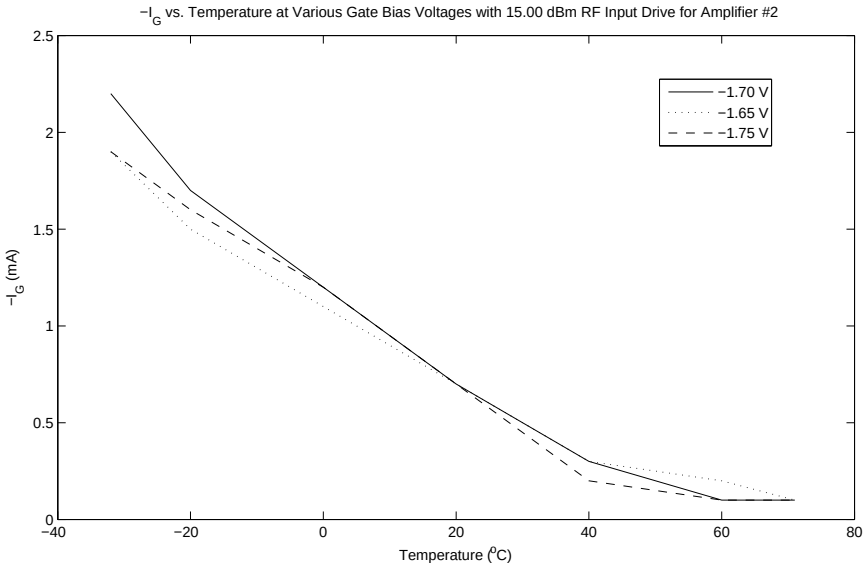

Figure 3-6: Amplifier #2 average reverse gate current $-I_G$ versus temperature for various gate bias voltages with 15.00 dBm RF input drive.

which in turn tends to increase the voltage swing at the drain of the amplifier and causes drain–gate voltage stress to increase at higher gate bias voltage. At lower temperatures, the effect of gate bias voltage seems more complex, and the maximum amount of amplifier gain is found at the nominal gate bias voltage of −1.70 V. Plots of reverse gate current with respect to RF output power at the different gate bias voltages are given in Figure 3-7 for −32 °C and Figure 3-8 for 20 °C.

In general, the plots show that for a given level of RF output power, reverse gate current is higher for a more negative gate bias. This effect now makes sense when we consider that a given level of RF output power generally corresponds to a similar level of drain voltage swing, regardless of of gate bias. Therefore, for a given level of RF output power, drain–gate voltage stress will be higher at more negative gate bias voltages, and there will be more reverse gate current for a given level of RF output power at more negative gate bias voltages.

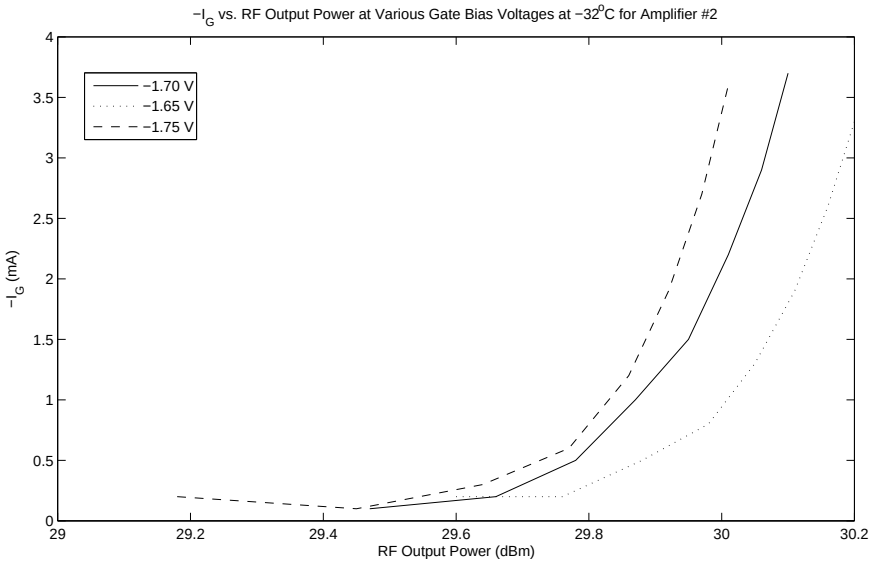

Figure 3-7: Amplifier #2 average reverse gate current $-I_G$ versus RF output power for various gate bias voltages at −32 °C.

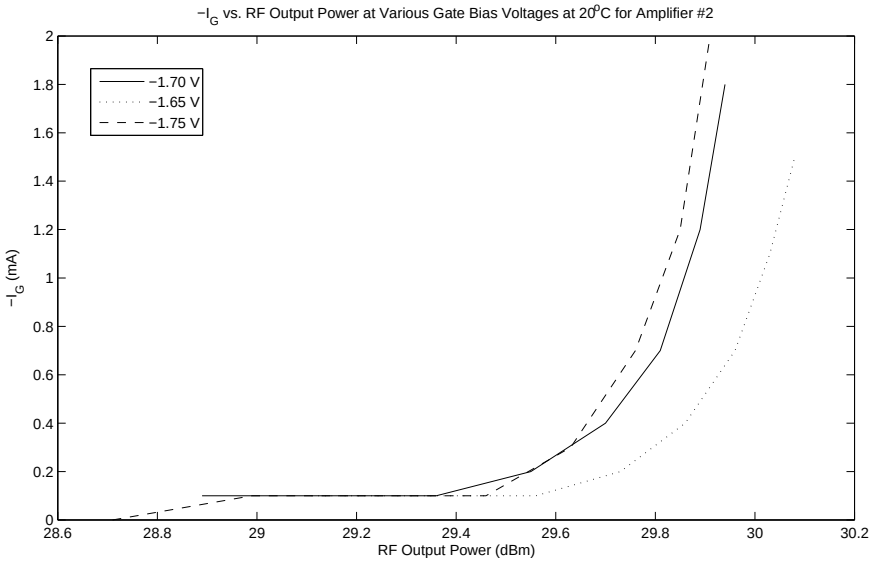

Figure 3-8: Amplifier #2 average reverse gate current $-I_G$ versus RF output power for various gate bias voltages at 20 °C.

3.4 Role of On-State Breakdown

The levels of average reverse gate current seen in experiments in this chapter are surprising if off-state breakdown is the only mechanism responsible for reverse gate current in the amplifier. Under nominal bias conditions, average reverse gate current of up to 2.3 mA was seen at 20 °C at an RF input drive level of 16.00 dBm. Simulation of the amplifier circuit indicates that peak drain–gate voltage during operation under these conditions should not exceed 17.5 V. Furthermore, before the transistors were used in fabrication of the microwave power amplifiers, they were characterized under two-terminal DC conditions, and showed a drain–gate breakdown voltage of about 21 V for a reverse gate current of 1.2 mA. The broad current sweep characterization of Chapter 2 also suggests that for a peak drain–gate voltage of 17.5 V, peak reverse gate current due to off-state breakdown would be expected to not exceed 20 μA, and therefore average reverse gate current should be less than this. Therefore, there would appear to be another effect that is leading to increased reverse gate current under RF drive in the amplifier.

The most likely explanation for the magnitude of reverse gate current under RF drive is the presence of on-state breakdown. As explained in Chapter 1, on-state breakdown occurs in a PHEMT when there exists a large drain–source voltage and the device is in its on-state with a significant amount of drain–source current. Impact ionization is generally held to be the mechanism dominant in on-state breakdown in PHEMTs [13], which matches the observations made in this chapter where reverse gate current decreased with temperature in the entire range of operation.

On-state breakdown was not initially considered as a possible mechanism for reverse gate current in the Draper 2.3 GHz amplifier due to the fact that the amplifier is a high-efficiency switching amplifier, and therefore has minimal periods of operation where the device is on and a large drain voltage exists. However, it is possible that there is enough overlap between regions of high drain voltage and high drain current during transitions between the on state and off state (and vice versa) for on-state breakdown to be dominant in the creation of reverse gate current. Although on-state

breakdown was not considered in the DC characterization performed in Chapter 2, it should still be possible to create a model that accounts for on-state breakdown based on these measurements due to the presence of impact ionization in DC off-state breakdown characterization at low temperature. This idea is expanded upon in Appendix A.

3.5 Summary

This chapter described the results of characterization of average reverse gate current in the Draper 2.3 GHz microwave power amplifier under RF drive conditions. The tests in this chapter were performed across a range of RF input drive levels, temperature, and biasing conditions. Forward gate current that arises due to forward biasing of the gate–source junction did not appear to be a major factor except for high temperatures and large levels of input drive. The results show that an increase in drain bias voltage leads to increase in average reverse gate current for a fixed level of RF input drive. Additionally, for a fixed level of RF output power, an increase in gate bias voltage leads to a decrease in average reverse gate current. Tests under all conditions showed a decrease in average reverse gate current with temperature, which indicates that impact ionization current is the dominant component of breakdown reverse gate current in the amplifier under RF drive.

The relatively large magnitude of average reverse gate current in the tests in this chapter when compared to data from DC characterization of off-state breakdown in Chapter 2 suggests that off-state breakdown is not the dominant mechanism responsible for reverse gate current in the amplifier under RF drive. This, along with the prevalence of impact ionization, suggests that on-state breakdown is dominant in the amplifier under RF drive. While on-state breakdown was not originally considered as a possible mechanism for reverse gate current in the amplifier, it is possible that enough overlap exists between regions of high drain voltage and high drain current during amplifier transitions for on-state breakdown to be dominant.

Chapter 4

Device Walkout and Recovery Characterization

Reliability is crucial to most circuit applications, including those that use microwave power amplifiers. By degrading device characteristics, hot electron stress during breakdown has the potential to negatively affect the performance of microwave power amplifiers. As mentioned in Chapter 1, the trapping of hot electrons during breakdown stress leads to a phenomenon called "breakdown walkout". Walkout leads to an increase in off-state breakdown voltage, but also negatively affects device characteristics like RF power gain, which can degrade the performance of a device. With the removal of breakdown stress, detrapping of electrons can lead to device recovery, but this recovery may only be partial.

This chapter focuses on characterization of breakdown walkout and recovery in the TC2571 PHEMT, and is divided into three sections. The first section covers two-terminal DC characterization of walkout and recovery, while the second section covers walkout characterization under typical RF drive stress conditions. The final sections summarizes the results of the chapter.

4.1 DC Walkout and Recovery Characterization

The first type of walkout and recovery characterization performed on the TC2571 involved DC characterization at different temperatures. For this test, it was decided to only perform characterization using two-terminal stress and measurement conditions. This decision was made due to the difficulty of stabilizing the device in a three-terminal setup that had been evidenced in the three-terminal characterization of the device described in Chapter 2. The first part of this section describes results of the two-terminal walkout characterization under stress, and the second part covers characterization of recovery of the device.

4.1.1 Walkout Characterization

Two-terminal DC characterization of walkout in the TC2571 was performed with the source of the device left floating and a fixed current of 1.2 mA ($0.5\ ^{\mathrm{mA}}/_{\mathrm{mm}}$) injected into the drain of the device for the duration of the stress. During the stress, V_{DG} was monitored, and stress was stopped when V_{DG} increased 10% from the lowest value recorded during the period of stress. Characterization was performed at −32 °C, 20 °C, and 70 °C. Before the application of stress, a pulsed measurement of V_{DG} was made to determine an initial value for V_{DG}. Figure 4-1 shows evolution of V_{DG} with respect to time since the application of stress for the transistor at 70 °C. A summary of the results from the characterization at all three temperatures is given in Table 4.1.

Temperature	**Initial V_{DG}**	**Minimum V_{DG}**	**Time to Walkout 10%**
−32 °C	18.44 V	18.40 V	99m:30s
20 °C	21.95 V	21.68 V	23m:40s
70 °C	22.77 V	20.74 V	12m:20s

Table 4.1: Table summarizing key results from breakdown walkout characterization on transistors at −32 °C, 20 °C, and 70 °C. The results listed are the initial value of V_{DG} before application of stress, the minimum value of V_{DG} recorded during stress, and the amount of time from the minimum recorded value of V_{DG} to when V_{DG} reached a value 10% larger.

A notable feature of the evolution of V_{DG} shown in Figure 4-1 is that the minimum V_{DG} achieved during stress is below the initial value. This is notable because it is

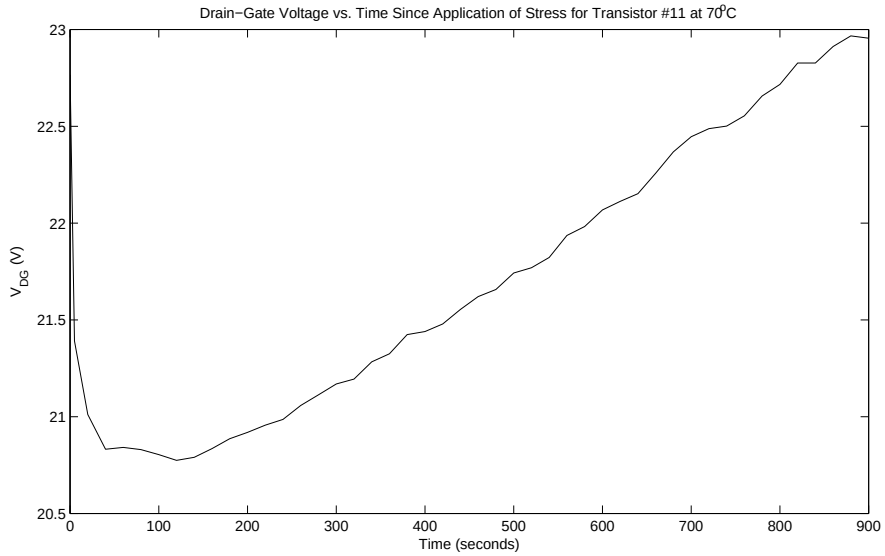

Figure 4-1: Transistor #11 drain–gate voltage V_{DG} versus time since application of stress at 70 °C.

believed that breakdown stress in PHEMTs leads to the trapping of hot electrons at the extrinsic drain surface, which should lead to an increase in V_{DG} for a fixed reverse gate current [10]. The decrease in V_{DG} is most evident at 70 °C, but is present at the other temperatures as well, as shown in Table 4.1. At the two other temperatures, V_{DG} shows a drop of 1.2% or less, and the minimum value was recorded within five seconds of the beginning of stress, at which point V_{DG} steadily increased until stress was removed. At 70 °C, the minimum value of V_{DG} is 8.9% smaller than the initial value, and is achieved 2 minutes after the application of stress. At all temperatures, after the minimum V_{DG} is achieved, V_{DG} increases steadily until stress is removed.

The reason for the decrease in V_{DG} immediately after the application of stress at all temperatures might be explained if we make a distinction between trap *creation* and trap *occupation* in PHEMTs. Hot electrons during breakdown stress might lead to the *creation* of traps in the drain access region [15, 16], which in itself leads to a decrease in drain–gate voltage for a fixed reverse gate current. The subsequent *occupation* of these traps might be what leads to breakdown walkout and the increase in drain–gate voltage for a fixed reverse gate current. From the results presented here,

it appears that trap creation and the subsequent decrease in drain–gate voltage are most prevalent at higher temperatures. This also helps to explain the difference at high temperature between the two-terminal DC tests with short and long sampling times in Chapter 2. In the test with long sampling time, a decrease in V_{DG} at high temperatures was shown when compared to the test with short sampling time. This decrease can now be seen as possible evidence of trap creation at higher temperature due to the longer sampling time used.

The other notable feature about the results in Table 4.1 is the amount of time it takes from the minimum recorded value of V_{DG} to the point when V_{DG} reaches a value 10% higher than this. At −32 °C, this took almost 100 minutes, but at 20 °C, it only took about 24 minutes. At 70 °C, it was even faster, and only took about 12 minutes. The fact that walkout occurs faster at higher temperatures seems to indicate that trap occupation occurs more rapidly at higher temperatures. This is actually in contrast to results that are reported for PHEMTs in the literature which indicate that device degradation induced by hot-electron effects should be smaller at higher temperatures due to the role of increased phonon scattering [11].

4.1.2 Recovery Characterization

DC characterization of recovery from breakdown stress in the TC2571 was performed on the same transistors that were stressed during DC walkout characterization. After the removal of stress, the devices were kept at the same temperature, and a pulsed measurement of V_{DG} using a fixed drain–gate current of 1.2 mA and a sampling time of 25 ms was made every 20 seconds. Figure 4-2 shows measurements of V_{DG} with respect to time since the beginning of recovery for the transistor at 70 °C. Table 4.2 summarizes some of the results from this part of the characterization.

A notable feature about the plot in Figure 4-2 is the rapid drop in V_{DG} immediately after the removal of stress. The results given in Table 4.2 show that this drop occurs at all temperatures almost immediately after stress is removed. After 20 seconds of recovery, the transistors showed a drop in V_{DG} from the final value recorded during stress of 1.89%, 8.36%, and 13.71% at −32 °C, 20 °C, and 70 °C, respectively. This

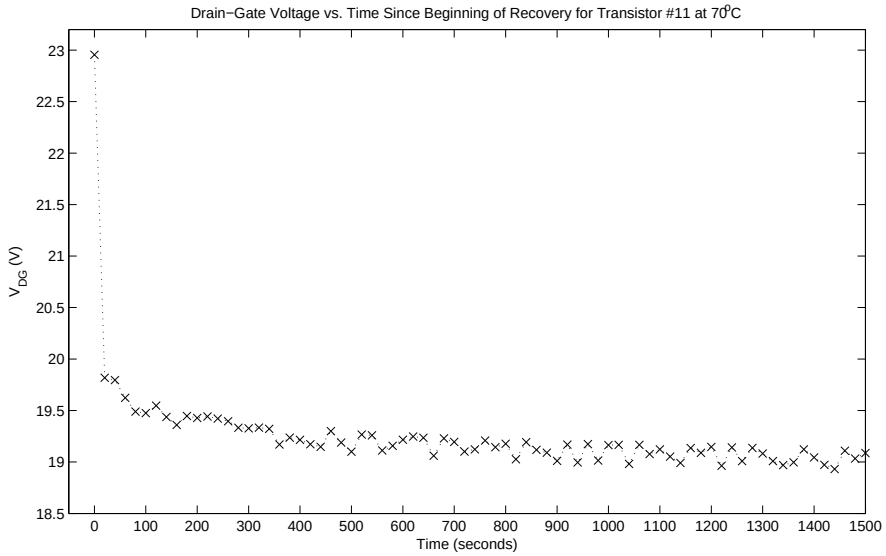

Figure 4-2: Transistor #11 drain–gate voltage V_{DG} versus time since beginning of recovery at 70 °C.

Temperature	V_{DG} **Before Stress**	V_{DG} **After Stress**	V_{DG} **at 20s Recovery**	V_{DG} **at 5m Recovery**	V_{DG} **at 30m Recovery**
−32 °C	18.44 V	19.64 V	19.27 V	19.08 V	18.94 V
20 °C	21.95 V	23.92 V	21.92 V	21.60 V	21.44 V
70 °C	22.77 V	22.97 V	19.82 V	19.33 V	18.84 V

Table 4.2: Table summarizing key results from walkout recovery characterization on transistors at −32 °C, 20 °C, and 70 °C. The results listed are the initial value of V_{DG} before application of stress, the final value of V_{DG} after application of stress, the value of V_{DG} after 20 seconds of recovery, the value of V_{DG} after 5 minutes of recovery, and the value of V_{DG} after 30 minutes of recovery.

drop in V_{DG} appears to show that detrapping of electrons occurs most quickly after the removal of stress, and also occurs more rapidly at higher temperature.

This observation about the speed of recovery and electron detrapping at different temperatures can be seen in the measurements made at 5 minutes and 30 minutes as well. The relatively slow recovery of the device at −32 °C when compared to the devices at 20 °C and 70 °C is especially notable. V_{DG} measured after 5 minutes and 30 minutes of recovery for the devices at 20 °C and 70 °C is actually below the minimum value of V_{DG} recorded during stress for these devices, while the value of V_{DG} for the device −32 °C at each of these times is still well above the minimum

value recorded during stress. Furthermore, 24 hours after the removal of stress for the device at −32 °C, V_{DG} was measured to be 18.63 V, which is a drop of 5.16% from the final stress value of V_{DG}. For comparison, a drop of this relative magnitude in V_{DG} was observed within 20 seconds of the removal of stress for the devices at 20 °C and 70 °C. Similar observations of increased electron detrapping at higher temperature are described in [17].

After the final recovery measurements were made, the devices were stored at room temperature (roughly 21 °C) for a week. The devices were then removed from storage, and brought back to the temperatures at which they were originally stressed. V_{DG} for these devices was then measured using the same pulsed measurement technique used during the initial recovery measurements. Table 4.3 summarizes the results of characterization after one week of recovery, and includes key results from the previous walkout and recovery characterization. V_{DG} measured for each of these devices was well below the minimum V_{DG} recorded during stress of the device. This probably reflects the fact that traps continued to be created (and occupied) during stress of the device beyond the point where V_{DG} reached a minimum. Once the electrons were detrapped during recovery, the minimum value of V_{DG} was therefore lower than the minimum value recorded during stress.

Temperature	**Initial** V_{DG}	**Minimum** V_{DG} **During Stress**	V_{DG} **at 30m Recovery**	V_{DG} **After Week Storage**
−32 °C	18.44 V	18.40 V	18.94 V	17.59 V
20 °C	21.95 V	21.68 V	21.44 V	20.09 V
70 °C	22.77 V	20.74 V	18.84 V	17.51 V

Table 4.3: Table summarizing key results from walkout recovery characterization after one week of storage at room temperature on transistors initially stressed at −32 °C, 20 °C, and 70 °C. The results listed are the initial value of V_{DG} before application of stress, the minimum value of V_{DG} recorded during stress, the value of V_{DG} after 30 minutes of recovery, and the value of V_{DG} after one week of storage at room temperature.

Another observation made about the devices after a week of recovery at room temperature was the relatively fast rise in V_{DG} after a quick sequence of 25 ms pulsed measurements was applied. Five pulsed measurements within five seconds caused V_{DG}

for the device at −32 °C to rise to 18.44 V (from 17.59 V), at which point successive pulses appeared to show approximately the same V_{DG} of 18.4 V. A similar observation was made for the device at 20 °C, which showed a rise to 21.32 V from 20.09 V. Successive pulses also showed V_{DG} to be stable at about 21.3 V. This behavior may indicate that trap occupation occurs relatively rapidly after the beginning of application of stress, and that drain–gate breakdown voltage for PHEMTs that have been stressed may actually be higher in practice than what a pulsed measurement reveals.

As mentioned in Chapter 1, breakdown walkout is stated by some sources in the literature to be a permanent effect [10, 11] in PHEMTs. After observing the results of DC walkout and recovery characterization for the TC2571, it would appear that this is true, at least in a sense. The creation of traps caused by hot electron stress during breakdown walkout appears to be a permanent effect that leads to an initial decrease in V_{DG} for a fixed reverse gate current. The occupation of these traps by electrons, however, does not appear to be a permanent effect. The increase in V_{DG} caused by occupation of traps by electrons begins to disappear once breakdown stress is removed as electron detrapping occurs. This detrapping appears to proceed more quickly at higher temperatures.

4.2 RF Walkout Characterization

Characterization of breakdown walkout and recovery of the TC2571 PHEMT under RF drive was performed using tests of the 2.3 GHz Draper amplifier under conditions that were designed to simulate the stress that the amplifier would be expected to undergo during its target operating conditions. The amplifier was stressed using a cycle where it was turned on with drain bias voltage of 7.00 V and gate bias voltage of −1.70 V and stressed with RF input drive of about 16.25 dBm for about 30 seconds, and then turned off for about 240 seconds before the stress cycle was repeated. The level of RF input drive was chosen to ensure that the amplifier was driven well into saturation. A sweep of RF input power from 13.00 dBm to 16.25 dBm was performed

at the beginning and end of each amplifier "on" cycle, and halfway through each "off" cycle. During each sweep, measurements of RF output power and reverse gate current were made at each input power level tested. Two amplifiers were stressed under these conditions. The transistors used in each amplifier were initially screened for threshold voltages between -1.8 V and -1.6 V, and were then matched under two-terminal DC test conditions. One amplifier was tested using the RF stress cycle at 20 °C, and the other was tested at -32 °C.

The amplifier tested at 20 °C was left under stress for about 66 hours. Figure 4-3 shows a plot of average reverse gate current versus RF input drive before and after the operation period. A couple of interesting features are worth mentioning about this plot. As mentioned earlier in Chapter 3, the average gate current is the sum of forward (gate–source diode) and reverse (gate–drain breakdown) components. Given the results of characterization in Chapter 3 for temperatures below 60 °C, the reverse gate current component due to breakdown appears to be dominant. Second, for the amplifier "on" cycles, the input drive level is 16.25 dBm, which corresponds over the course of this test to an average reverse gate current level that decreased from 2.8 mA (1.17 $^{\mathrm{mA}}/_{\mathrm{mm}}$) to 2.3 mA (0.96 $^{\mathrm{mA}}/_{\mathrm{mm}}$). This level of average reverse gate current is about twice as high as that used in the DC two-terminal test of walkout and recovery. Finally, at all input drive levels tested, there is a decrease in average reverse gate current over time. This is a clear indication that breakdown walkout has occurred in the device over the course of the test.

Since walkout tends to degrade PHEMT device characteristics [10, 11], it might be expected then that the stress period would reduce amplifier output power at all drive levels. However, as shown in Figure 4-4, output power does decrease noticeably at lower input drive levels, but at higher input drive levels where output power is more saturated, there appears to be little change in output power after stress. This can also be seen in Figure 4-5, where the change in amplifier output power is plotted with respect to time since the beginning of stress for input drive levels of 13.00 dBm, 14.84 dBm, and 16.25 dBm. At the lowest drive level of 13.00 dBm, amplifier output power drops by 0.15 dBm during the stress period, and at 14.84 dBm, amplifier

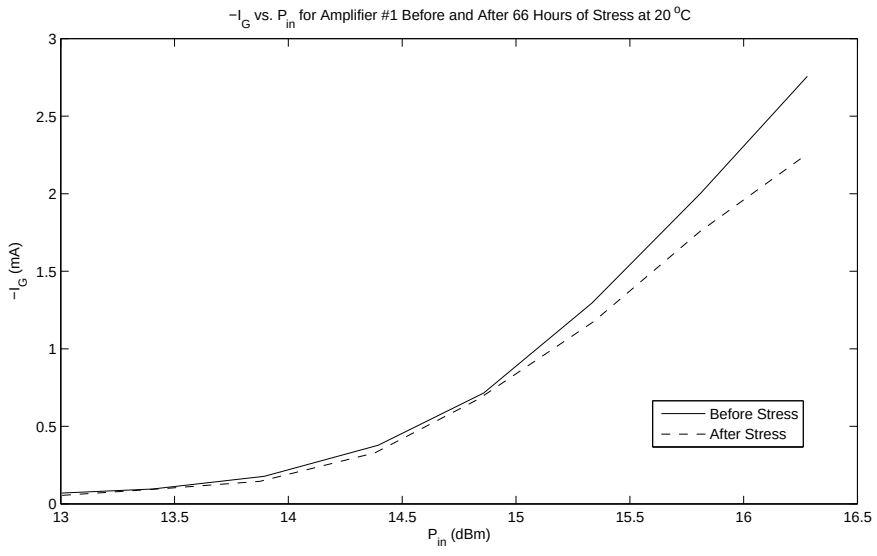

Figure 4-3: Amplifier #1 average reverse gate current $-I_G$ versus RF input drive P_{in} before and after 66 hours of stress at 20 °C.

output power drops by about 0.04 dBm. However, for input drive of 16.25 dBm, the output power actually appears to increase slightly by 0.02 dBm. This increase seems somewhat remarkable, and cannot be readily explained. Calibration drift in the measurement equipment was negligible, and there was a decrease in average drain current at all input drive levels tested over the course of the test. Regardless, it seems clear that while breakdown walkout in the amplifier PHEMT at 20 °C led to a decrease in amplifier gain at lower levels of input drive, it did not have a major effect on the saturated output power of the amplifier, which is an important consideration in determining the effect of breakdown walkout on device reliability.

The amplifier stressed at −32 °C showed similar trends under stress to the amplifier stressed at 20 °C. Figure 4-6 shows average reverse gate current versus RF input drive for the amplifier before and after 66 hours of stress, and a reduction in average reverse gate current at all levels of input drive is apparent. For this amplifier, during the "on" cycles where the amplifier had an input drive of 16.25 dBm, average reverse gate current over the course of the test decreased from 4.2 mA (1.75 $^{\mathrm{mA}}/_{\mathrm{mm}}$) to 3.5 mA (1.46 $^{\mathrm{mA}}/_{\mathrm{mm}}$). This range of current is roughly between three to four times as high as the current level used in the two-terminal DC characterization of breakdown walkout,

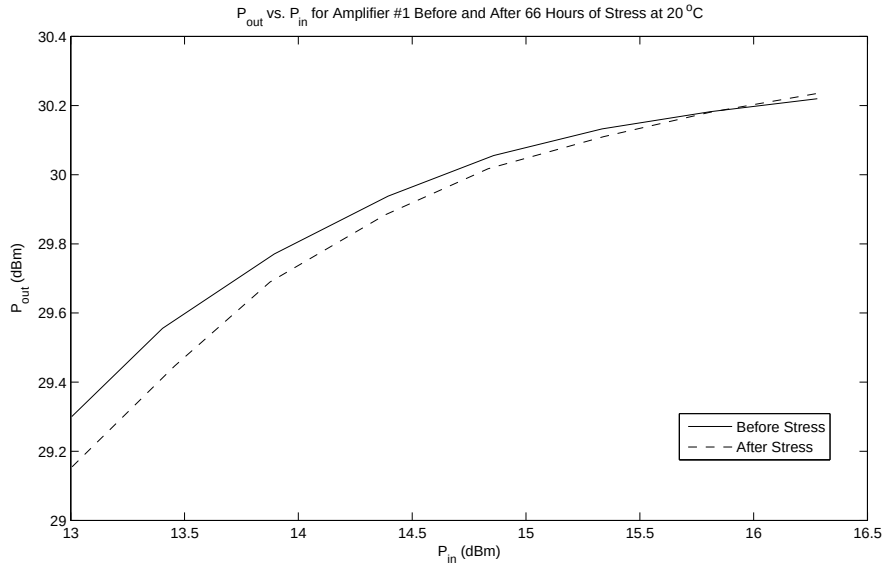

Figure 4-4: Amplifier #1 RF output power P_{out} versus RF input drive P_{in} before and after 66 hours of stress at 20 °C.

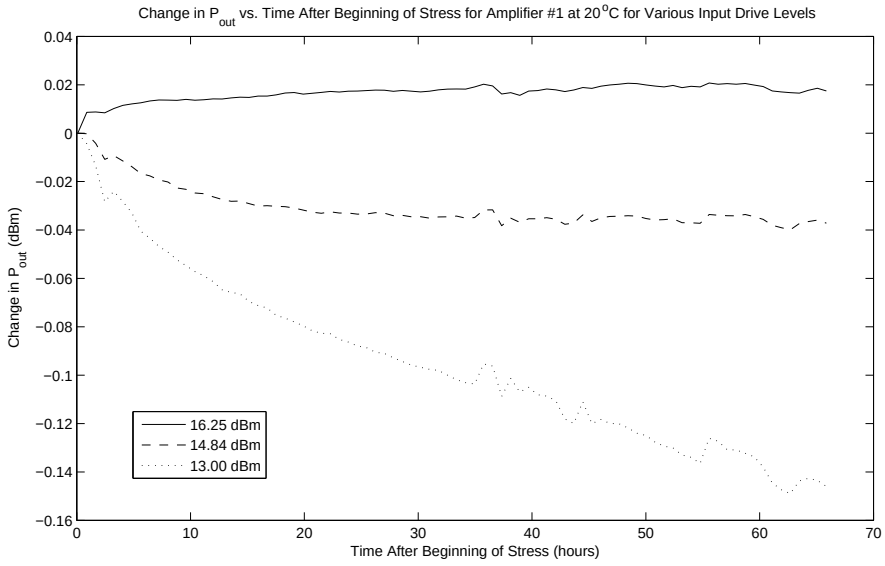

Figure 4-5: Amplifier #1 change in RF output power P_{out} versus time since beginning of stress at 20 °C for various input drive levels.

and is about 50% higher than the level of average reverse gate current in the test at 20 °C. Figure 4-7 shows a plot of RF output power versus RF input drive before and after 66 hours of stress, and once again, there is a noticeable decrease in RF output power at lower drive levels, and an apparent slight increase in saturated RF output power at higher drive levels. Figure 4-8 shows the change in amplifier output power with respect to time since the beginning of stress at input drive levels of 13.00 dBm, 14.34 dBm, and 16.25 dBm. This plot shows the change in output power over 145 hours, which is more than twice as long as the plots previously considered, but the trends shown seem to be continuations of those that would be observed at 66 hours. As with the test at 20 °C, there is a noticeable drop in amplifier gain at lower input drive levels, but there is also an increase in saturated amplifier output power at higher drive levels. The reason for the increase in amplifier saturated output power is still unclear. Once again, there was no calibration drift in the measurement setup, and there was a decrease in average drain current at all input drive levels over the course of the test.

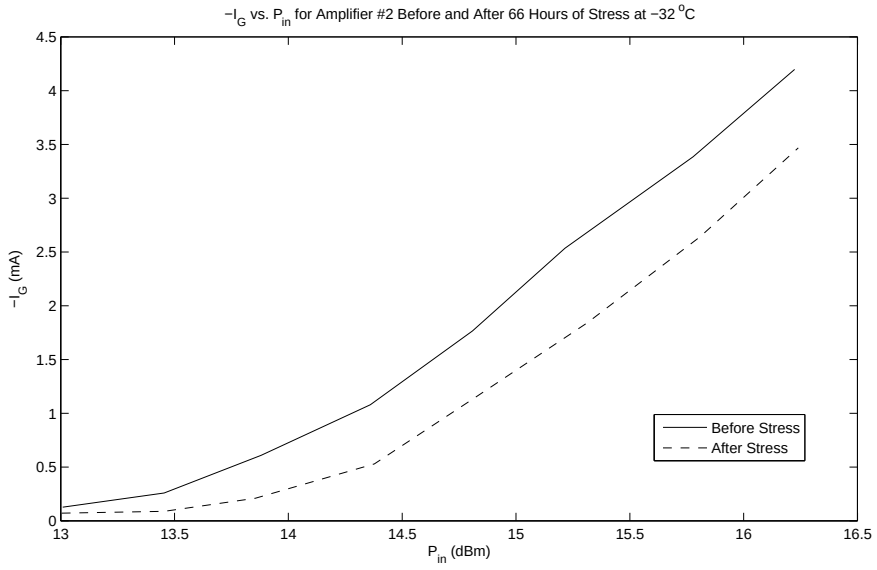

Figure 4-6: Amplifier #2 average reverse gate current $-I_G$ versus RF input drive P_{in} before and after 66 hours of stress at −32 °C.

While the general trends in the change of average reverse gate current and output

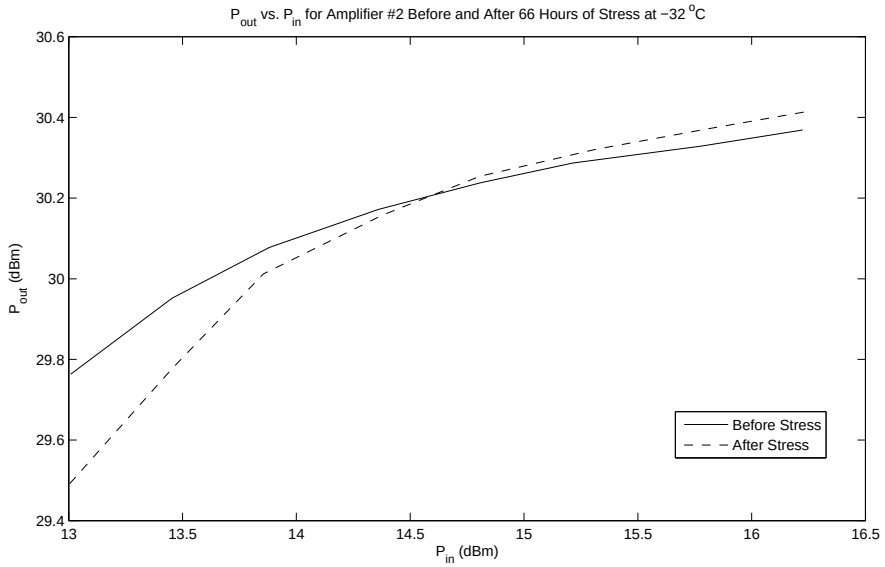

Figure 4-7: Amplifier #2 RF output power P_{out} versus RF input drive P_{in} before and after 66 hours of stress at −32 °C.

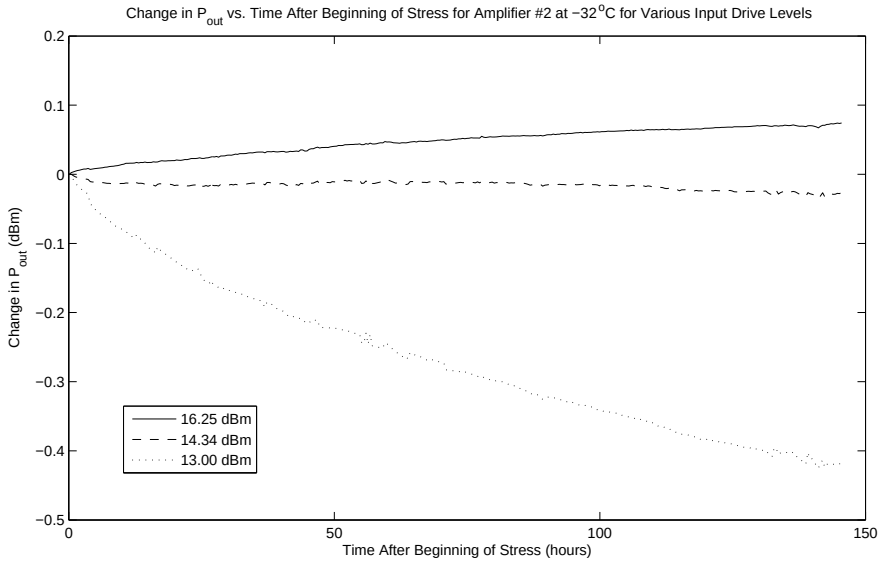

Figure 4-8: Amplifier #2 change in RF output power P_{out} versus time since beginning of stress at −32 °C for various input drive levels.

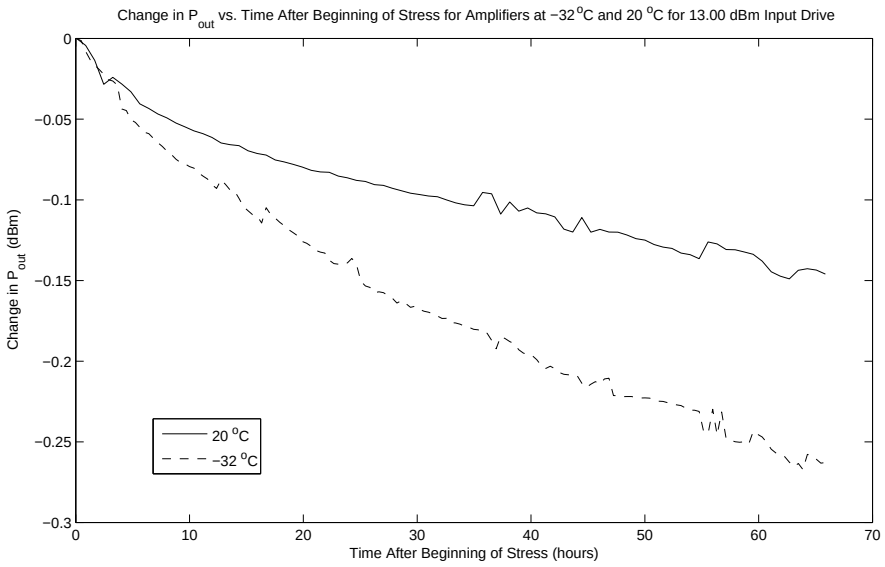

Figure 4-9: Comparison of change in RF output power P_{out} versus time since beginning of stress for Amplifier #1 (at 20 °C) and Amplifier #2 (at −32 °C) for 13.00 dBm RF input drive.

power in Figures 4-6 and 4-7 are the same as for the amplifier at 20 °C, the drops in both output power at lower drive levels and average reverse gate current are of larger magnitude in the amplifier at −32 °C. The increased speed and magnitude of breakdown walkout at lower temperature can also be seen in Figure 4-9, which shows the change in RF output power versus time since the beginning of stress for the amplifiers at 20 °C and −32 °C for 13.00 dBm RF input drive. The increased prevalence of walkout at lower temperatures is a marked change from the DC two-terminal characterization of walkout, where walkout proceeded far more slowly at −32 °C than it did at 20 °C. This is likely due to the increase magnitude of average reverse gate current at lower temperatures, which is believed to be a symptom of the prevalence of on-state breakdown induced by impact ionization (as stated in Chapter 3).

In the plots in this section that show changes in RF output power over time (like Figures 4-5 and 4-8), perturbations from the general trend can be noticed in the traces of output power. These perturbations are relatively small in magnitude, and occur

at the same time across all input drive levels in each test. It is believed that these perturbations have to do with the effect of poorly controlled ambient temperature on the measurement setup that was used to determine the value of RF input drive and output power. Such perturbations did not appear to affect the conditions that the device was stressed under, and therefore the general trends seen in output power in this section are still valid.

The results presented in this section present an interesting amplifier design dilemma related to continuous operation conditions. In order to have a steady level of output power during continuous operation for a fixed level of RF input drive, it seems that the power amplifier must be stressed in a region where amplifier output power is saturated. However, it is under these conditions where the amplifier will show the greatest walkout and degradation over time as the device undergoes high levels of breakdown stress. Further long term testing of walkout in the amplifier across a range of RF drive conditions and temperatures may help to provide a solution for this dilemma, and identify areas of operation where a certain amount of output power can be traded for increased reliability.

4.3 Summary

This chapter focused on characterization of breakdown walkout and recovery in the TC2571 PHEMT. The first section of the chapter described two-terminal DC characterization of walkout and recovery in the device. Testing was performed at three temperatures, and shows that walkout appears to proceed more quickly at higher temperatures as V_{DG} rose more rapidly for a fixed level of reverse gate current under these conditions. Walkout is believed to be the result of electrons occupying traps in the device, and as a result, it appears that trap occupation occurs more rapidly at higher temperatures, which is in contrast with existing research on PHEMTs in the literature. The device also shows faster recovery at higher temperatures as breakdown voltage decreases more rapidly after the removal of stress under these conditions, which is believed to be due to an increase in the rate of electron detrapping at these

temperatures. Tests after the devices had been stored for a week show that the final value of breakdown voltage after recovery degraded significantly from its initial value, which indicates that the creation of traps may occur during breakdown stress in the device. This possible trap creation may also be the reason why there is a rapid initial drop in V_{DG} after the application of stress. The trapping and detrapping of electrons does not appear to be a permanent effect in the device, but the creation of traps does appear to be permanent.

The second section of the chapter focused on characterization of walkout in the Draper 2.3 GHz amplifier under RF drive. Testing was performed using a stress cycle that is designed to replicate operational conditions for the amplifier. Observations of average reverse gate current show that significant walkout occurs after use of the stress cycle. While walkout leads to a noticeable decrease in amplifier gain at lower levels of RF input drive, it had no negative effect on amplifier saturated output power, which appears to increase slightly after walkout. Walkout under RF drive also proceeds more quickly at lower temperatures, which is likely due to the increased levels of reverse gate current seen under these conditions. The results of walkout characterization of the amplifier present a dilemma about continuous operation since the amplifier must be driven into saturation in order to maintain a steady level of output power over time, but it is under these conditions where the amplifier is most likely to show walkout and degradation.

Chapter 5

Circuit Design Techniques to Mitigate Degradation

As described in Chapter 4, breakdown stress in PHEMTs can lead to degradation of device characteristics. This has the potential to negatively affect the reliability of circuits that use PHEMTs, especially microwave power amplifiers. By mitigating device degradation due to breakdown stress, circuit reliability can be increased. Furthermore, as mentioned in Chapter 1, mitigating device degradation due to breakdown stress can also lead to power amplifiers with higher efficiency and/or higher output power while maintaining device reliability.

This chapter describes two circuit design techniques that might be used to mitigate device degradation due to breakdown stress in microwave amplifiers. The first section describes using temperature-compensated attenuation of input drive to reduce reverse gate current due to breakdown, particularly at lower temperatures. The second section describes the use of a diode to clamp the negative swing of voltage at the gate of the device. The final section summarizes the results of the chapter.

5.1 Temperature-Compensated Input Drive

As seen in Chapter 3, for the 2.3 GHz amplifier studied in this thesis, reverse gate current for a fixed level of RF input drive was markedly higher at lower temperatures.

However, the amplifier's RF power gain is also higher at low temperature. Thus, since a fixed amount of output power is usually desired regardless of temperature, input drive can be attenuated at low temperatures to take advantage of the higher gain and reduce breakdown stress.

An example of the effect of using temperature-compensated input drive is shown for one amplifier in Figure 5-1. If at least 30.00 dBm of output power is required between −32 °C and 60 °C for the amplifier, and a constant RF input drive level is used, then the input RF drive must be at least 16.00 dBm. However, if temperature-compensated input drive for an output power of 30.00 dBm is used, then reverse gate current (and breakdown stress) can be significantly reduced, as shown in the plot. At −32 °C, only about 13.18 dBm of input drive would be required, and at 20 °C, only about 14.75 dBm of input drive would be required. The figures for input drive and reverse gate current are derived from interpolation using RF characterization data from Chapter 3, and are thus approximate. However, the general effect of temperatured-compensated input drive is still clear.

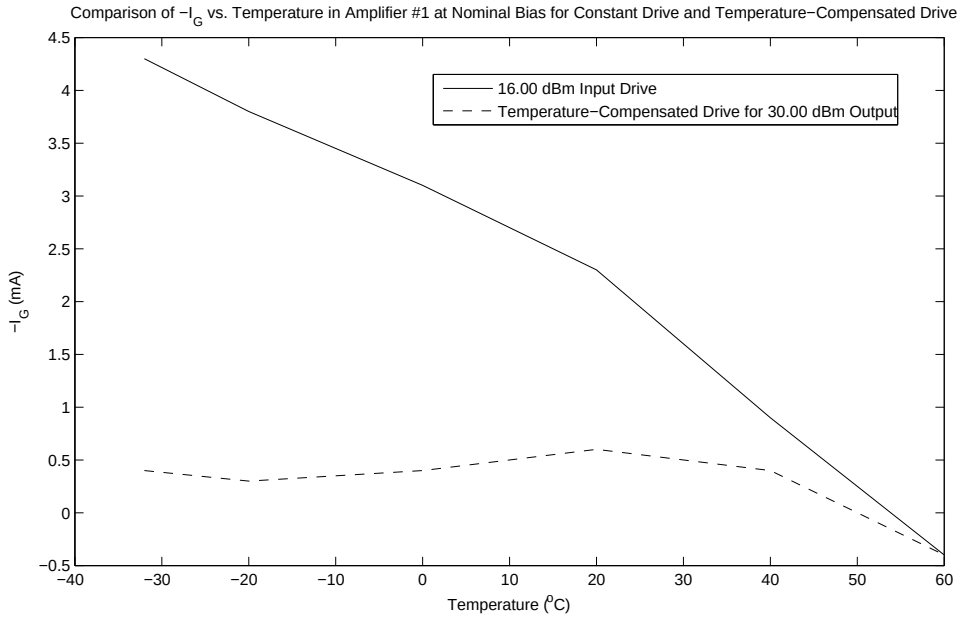

Figure 5-1: Comparison of amplifier #1 average reverse gate current $-I_G$ versus temperature at nominal bias conditions for 16.00 dBm constant input drive and temperature-compensated input drive for 30.00 dBm output.

Figure 5-2 shows a similar plot for a second amplifier, but between −32 °C and 71 °C for 29.50 dBm of output power (since the second amplifier has slightly less gain than the first). In this case, 15.50 dBm of input drive is required in order to have at least 29.50 dBm of output power across the full range of temperature for constant RF input drive. Once again, the plot shows that a significant reduction in reverse gate current (and the corresponding breakdown stress) can occur by using temperature-compensated input drive.

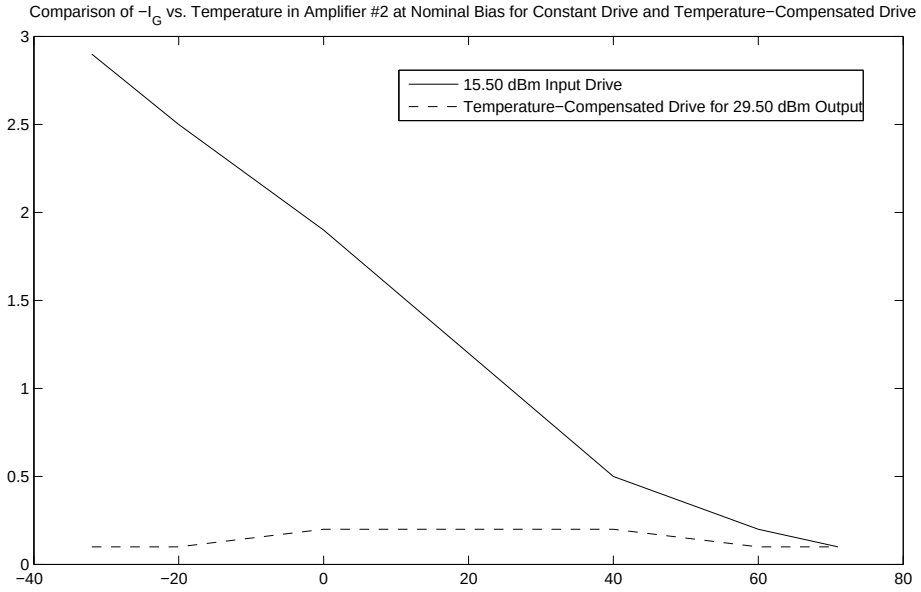

Figure 5-2: Comparison of amplifier #2 average reverse gate current $-I_G$ versus temperature at nominal bias conditions for 15.50 dBm constant input drive and temperature-compensated input drive for 29.50 dBm output.

Implementation of temperature-compensated input drive for a microwave power amplifier generally requires attenuating the output of the driver amplifier stage that precedes a microwave power amplifier. A method for implementing temperature-compensated input drive will not be covered, since it is beyond the scope of this thesis, but such methods are well covered in the literature. These techniques include placing a passive network of diodes and resistors at the gate of amplifier transistors [18], using a ROM to store appropriate input drive levels at various temperatures [19], and the use of a temperature-controlled variable gain amplifier to drive the power amplifier

[20]. Additionally, passive temperature compensation attenuators are sold as stand-alone products by some companies [21], and are perhaps the simplest solution for implementing temperature-compensated input drive. These passive attenuators also have the benefit of providing some impedance mismatch isolation between the driver and power amplifier stages.

5.2 Gate Voltage-Clamp Diode

High peak drain–gate voltage is the primary factor that leads to off-state breakdown stress in PHEMT microwave power amplifiers, and can also contribute to on-state breakdown stress. By reducing drain–gate voltage swing in microwave power amplifiers for a given amount of output power, gain, and/or efficiency, it should be possible to increase device performance while avoiding degradation due to breakdown stress, and thus maintain reliability. One possible method for reducing peak drain–gate voltage is to clamp the negative swing of gate voltage during the amplifier's off state by using a diode that is connected between the gate of the transistor and a bias voltage V_{CLAMP}, which should be set near the gate bias voltage. The gate bias voltage in a switching power amplifier is generally near the device's threshold voltage, and since negative gate voltage swing well below the threshold voltage of the device does not "turn off" the transistor significantly more than leaving the gate voltage just below threshold, such clamping, at first glance, would be expected to reduce peak drain–gate voltage while not significantly affecting amplifier performance. A schematic of a power amplifier circuit that uses a clamping diode to limit negative gate voltage swing is shown in Figure 5-3.

In order to determine the effects of using a diode to clamp negative gate voltage swing, it was decided to compare simulations in Agilent's Advanced Design System of designs of the Draper 2.3 GHz microwave power amplifier with and without a clamping diode. Since the diode has the potential to change input impedance characteristics of the amplifier, the input network of the amplifier was optimized separately for each circuit. A parameterized diagram for the input network of the amplifier

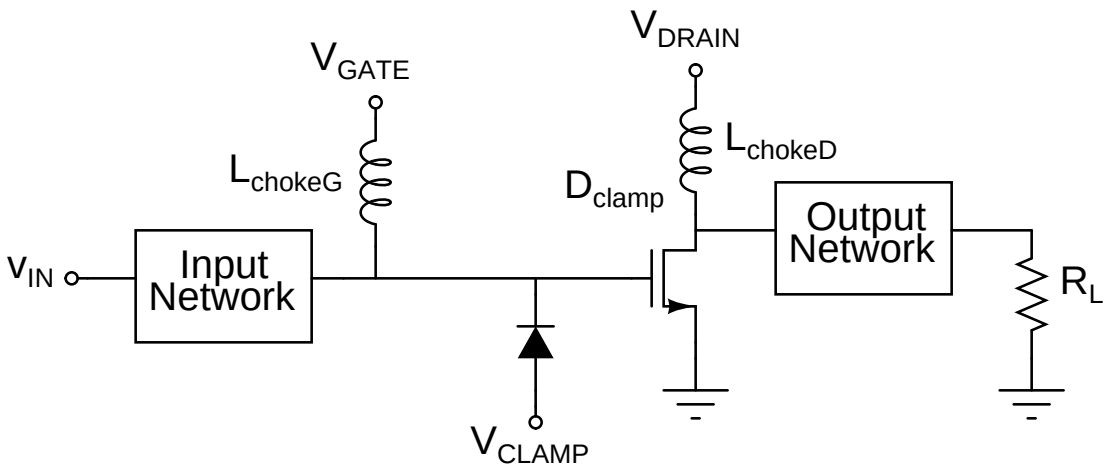

Figure 5-3: A schematic of a power amplifier circuit that uses a diode to clamp negative gate voltage swing.

is given in Figure 5-4. The input network contains a microstrip transmission line structure with a stub that is primarily used to control impedance characteristics at the second harmonic. All parameters of the input network were used in optimization except the value of the choke inductance, which was fixed at 2.55 nH. The drain bias and gate bias voltages were set at 7.00 V and −1.80 V, respectively. Optimization of the input network for each version of the amplifier was performed to provide the maximum power-added efficiency[1] with at least 30.50 dBm output power for 15.00 dBm input drive and a maximum drain–gate voltage of 17.50 V. For reasons that will be explained later, the diode used in the clamping diode amplifier design was biased at −3.10 V and was an ideal diode with no capacitance, ohmic resistance, or reverse current effects and a forward voltage of about 0.3 V[2].

Table 5.1 shows the optimized parameters for the amplifier input network for both amplifier designs. The parameters for both amplifiers are fairly similar with the exception of L_{main1}, which is significantly smaller for the design with the clamping diode. Comparison of simulated performance for the two amplifiers with 15.00 dBm input drive is given in Table 5.2. Output power is slightly higher and power-added

[1]Power-added efficiency (or PAE) for a power amplifier is defined as $\frac{P_{out}-P_{in}}{P_{DC}}$, where P_{out} is the RF output power, P_{in} is the RF input power, and P_{DC} is the power consumed by the amplifier from the DC drain and gate bias supplies.

[2]This is similar to a typical Schottky diode forward voltage drop.

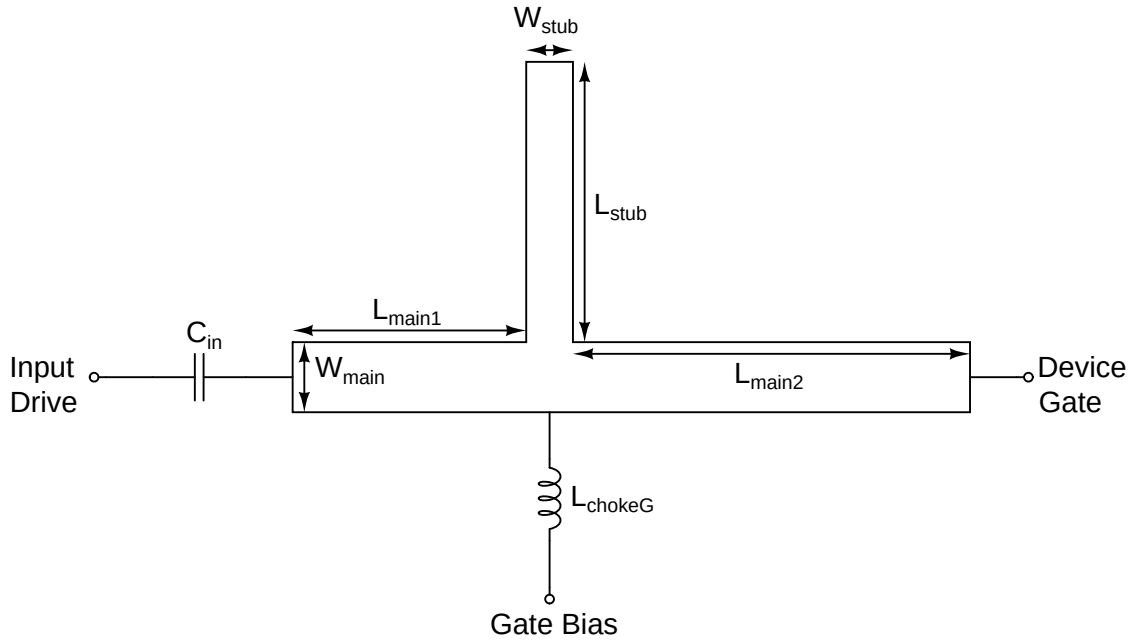

Figure 5-4: A diagram of the input network for the Draper 2.3 GHz microwave power amplifier. The input network contains a microstrip transmission line structure with a stub that is primarily used to control impedance characteristics at the second harmonic.

Parameter	**Original Amplifier**	**Clamping Diode Amplifier**
C_{in}	1.59 pF	1.60 pF
W_{main}	75.6 mil	52.4 mil
L_{main1}	139.3 mil	29.2 mil
L_{main2}	241.1 mil	291.9 mil
W_{stub}	25.1 mil	26.8 mil
L_{stub}	214.0 mil	212.0 mil

Table 5.1: Table of parameters for the amplifier input networks of the Draper 2.3 GHz power amplifier designs with and without a clamping diode.

Performance at 15.00 dBm Input	**Original Amplifier**	**Clamping Diode Amplifier**
Output Power	30.50 dBm	30.51 dBm
Power-Added Efficiency	80.18%	78.05%
Peak Drain–Gate Voltage	17.50 V	16.79 V

Table 5.2: Table of simulated performance values for the Draper 2.3 GHz power amplifier designs with and without a clamping diode for 15.00 dBm input power.

efficiency is slightly lower for the amplifier with the clamping diode. The most notable difference, though, is the fact that peak drain–gate voltage is reduced by 0.71 V in the amplifier with the clamping diode. This reduction may seem relatively small, but as was seen in Chapter 2 for DC characterization, even a small change in drain–gate voltage can lead to significant change in reverse gate current due to breakdown[3]. As Figure 5-5 shows, the diode helps to keep the negative gate voltage swing in the clamping diode amplifier about 1.2 V smaller than that in the original amplifier for 15.00 dBm input drive, which contributes to reduced peak V_{DG} in Figure 5-6. Indeed, the optimization constraint on keeping maximum drain–gate voltage to 17.50 V or below is not actually needed in the amplifier with the clamping diode, and the fact that this amplifier design is still able to meet the output power specification and come close in power-added efficiency to the original amplifier helps demonstrate the utility of using a clamping diode to limit negative gate voltage swing.

While the use of a diode to clamp negative gate voltage swing is promising, there are potential problems that were discovered with the technique during the course of evaluating its use. The first is the problem introduced by transistor package parasitics. Such parasitics behave like LC networks that are present between the input network and the intrinsic device gate, and the impedance characteristics of these networks can alter the characteristics of the gate drive before it reaches the device. This is demonstrated for the original Draper amplifier design at 15.00 dBm input drive in Figure 5-7, where the voltage at the intrinsic device gate shows a significant increase when compared to voltage at the gate lead of the transistor package due to resonance in the package parasitics. Thus, if the clamp diode is connected to the gate lead of a packaged transistor, as might be the case for a standard printed circuit board amplifier, then the diode can be ineffective in clamping the negative swing of voltage at the intrinsic gate of the transistor. This might not be as much of an issue in multi-

[3]A rather rough method of determining the reduction in reverse gate current can be used if a combination of simulation and RF characterization data from Chapter 3 is referenced. Simulation of the original Draper amplifier shows that a drop of peak drain–gate voltage from 17.50 V to 16.79 V corresponds to a drop in input drive from 15.00 dBm to 12.00 dBm. Such a reduction in input drive, from the characterization of Amplifier #1 under nominal bias conditions, would correspond to a reduction of average reverse gate current from 2.6 mA to less than 0.1 mA at −32 °C, from 0.9 mA to less than 0.1 mA at 20 °C, and from 0.1 mA to less than 0.1 mA at 71 °C.

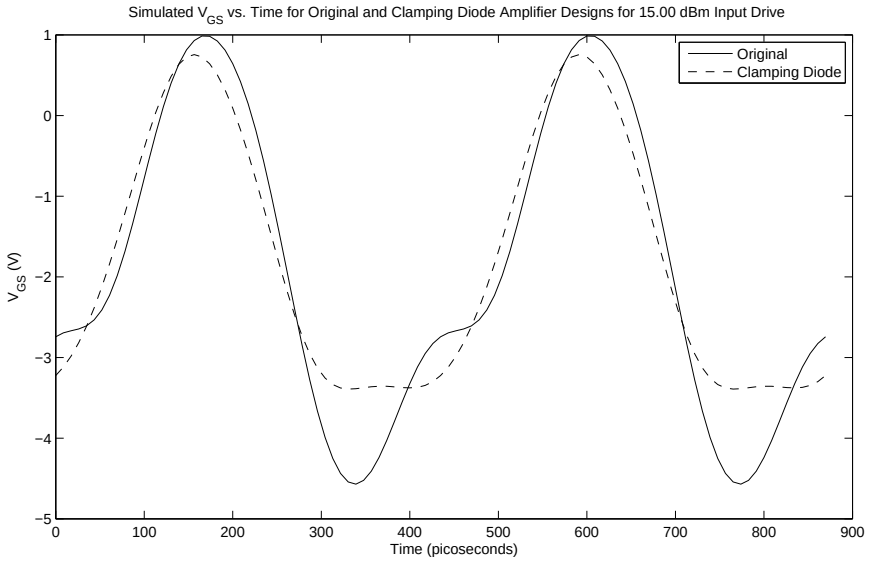

Figure 5-5: Comparison of simulated V_{GS} versus time for the Draper 2.3 GHz power amplifier designs with and without a clamping diode for 15.00 dBm input drive.

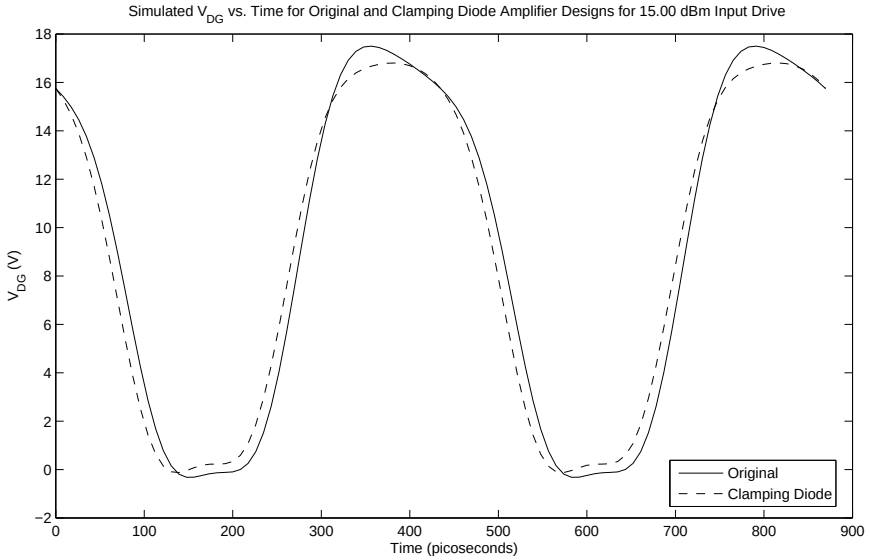

Figure 5-6: Comparison of simulated V_{DG} versus time for the Draper 2.3 GHz power amplifier designs with and without a clamping diode for 15.00 dBm input drive.

chip module (MCM) amplifiers [22] or in monolithic microwave integrated circuits (MMICs). In both of these types of circuits, components are much more tightly integrated, and therefore parasitics generally tend to play a smaller role. Since the Draper 2.3 GHz amplifier will eventually be fabricated in an MCM process, for the simulations in this thesis, it was decided to place the clamping diode "after" the package parasitics and put it directly at the intrinsic gate of the device.

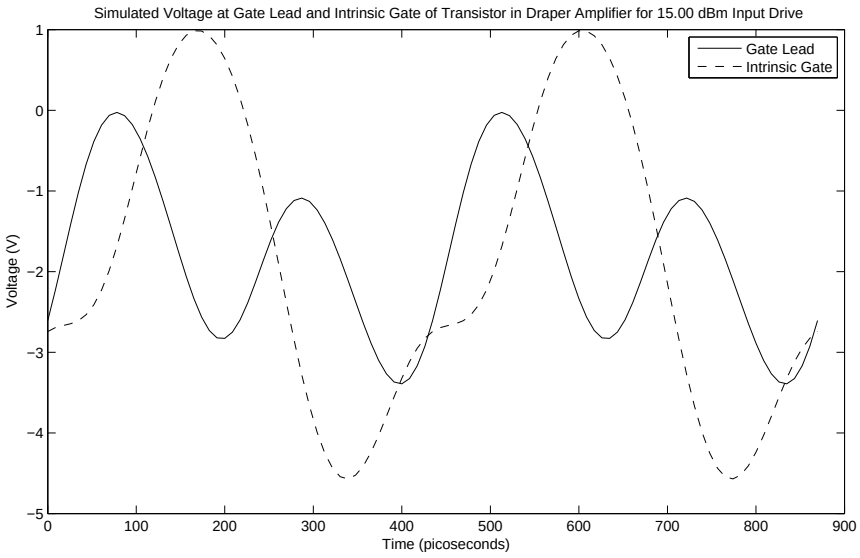

Figure 5-7: Comparison of simulated voltages at the gate lead and intrinsic gate of the transistor versus time for the Draper 2.3 GHz power amplifier for 15.00 dBm input drive.

Another potential problem with the use of a gate voltage-clamp diode is the presence of diode nonidealities like depletion and diffusion capacitances and ohmic resistance. The presence of diode capacitance can generally be dealt with by changing input network parameters to compensate for the added capacitance. However, ohmic resistance is a more serious problem as it degrades switching performance of the diode, which is critical for applications like a microwave amplifier where switching time needs to be in the picosecond range in order for clamping to be effective. Fast-switching Schottky diodes that are designed for use in RF clamping/transient-suppression applications would therefore probably be the best choice for gate voltage-clamp diodes.

A final potential problem discovered in simulation of the Draper 2.3 GHz amplifier with a negative voltage-clamp diode is the limitation of positive gate voltage swing by the diode. This effect was surprising, and it was discovered that as negative gate voltage swing became more clamped, the positive gate voltage swing decreased as well, which dramatically affected the gain of the power amplifier. To demonstrate this effect, the amplifier circuit with a clamp diode was simulated with different diode bias voltages. Figure 5-8 shows simulated gate–source voltage for the amplifier at 15.00 dBm input drive for the various diode bias voltages. As the diode bias voltage is increased, the negative voltage swing at the gate is clamped further, which is expected. However, the positive voltage swing decreases as well. A possible reason for this decrease in positive voltage swing can be seen in Figure 5-9, which shows simulated diode current under the same conditions. Due to inductance in the network connected to the gate of the device, the clamping diode cannot instantaneously "turn off" when the amplifier enters its "on" state, and the reactive current that flows through the inductance keeps the diode "on" and limits the positive swing of gate voltage. At higher bias voltages, this effect becomes more pronounced as the diode has a larger peak current in it during the amplifier "off" state and therefore takes longer to turn off as the amplifier enters its "on" state. In effect, by more strongly clamping the negative swing of gate voltage, the positive swing of gate voltage is also more strongly clamped.

As mentioned before, a diode with a 0.3 V forward voltage drop and a bias voltage V_{CLAMP} of -3.10 V was used in the simulation to determine the effects of clamping negative gate voltage swing. The large 1.30 V difference between the gate bias voltage and the diode bias voltage was required to achieve sufficient output power as higher diode bias voltages tended to restrain the positive swing of gate voltage too much. However, creating the additional negative DC voltage is usually not a trivial task, and requires additional circuit complexity, area, and power consumption. Another possible solution may be to keep the diode bias voltage at the gate bias voltage, but to use multiple diodes in series to increase the effective forward voltage drop. This poses a problem of increased effective series resistance, though. A change in the structure

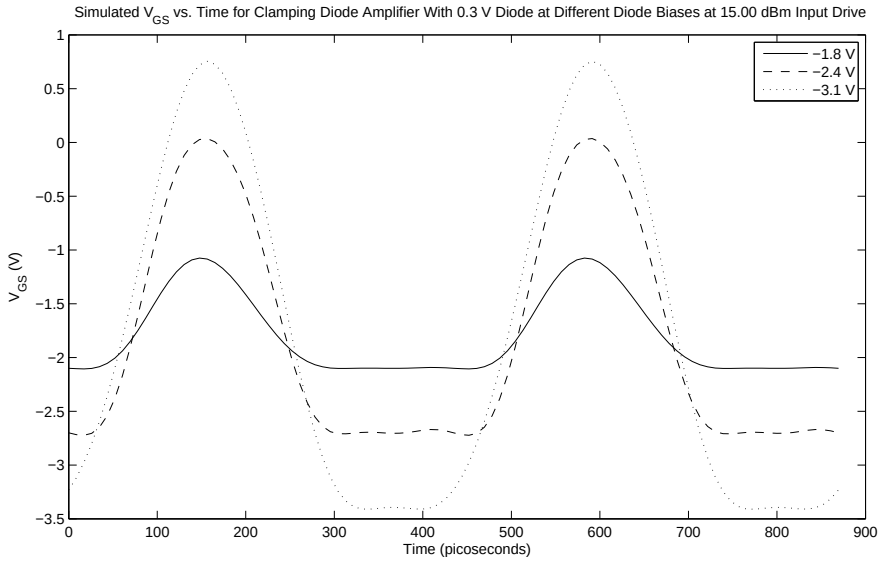

Figure 5-8: Comparison of simulated V_{GS} for the clamping diode amplifier with a 0.3 V diode at various diode bias voltages and 15.00 dBm input drive.

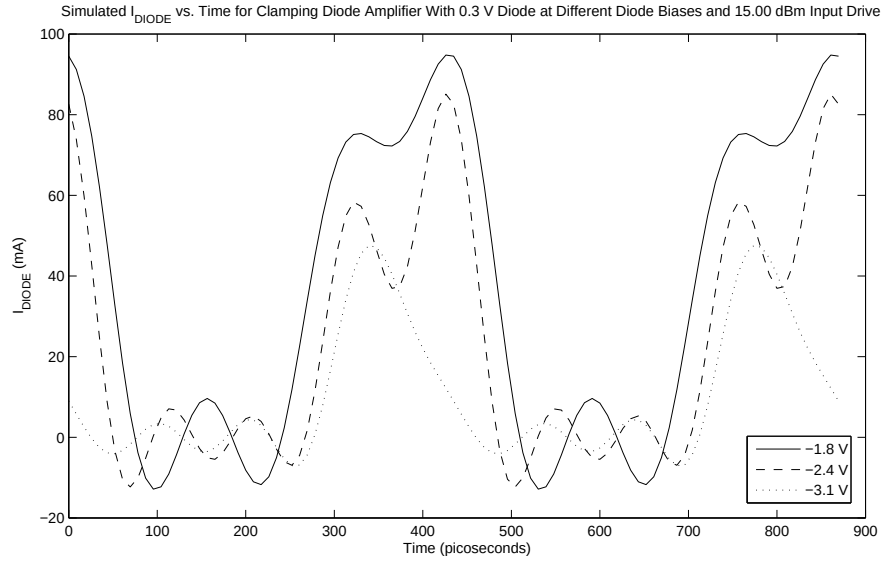

Figure 5-9: Comparison of simulated I_{DIODE} for the clamping diode amplifier with a 0.3 V diode at various diode bias voltages and 15.00 dBm input drive.

of the network connected to the gate of the device[4] could also prevent inductance from keeping the diode on when the amplifier enters the on state, and thus allow for negative gate voltage swing to be more strongly clamped without affecting amplifier gain. Even without this change, the effect of inductance will be less pronounced at lower frequencies, and therefore the use of a gate voltage-clamp diode will likely be more effective for amplifiers operating below 1 GHz.

5.3 Summary

This chapter described two circuit techniques that might be used to mitigate device degradation due to breakdown stress in microwave power amplifiers. Temperature-compensated input drive, the first technique, involves the attenuation of input drive at lower temperatures, where average reverse gate current is higher, in order to reduce breakdown stress. Since gain is higher at lower temperatures as well, the reduction of input drive at these temperatures can be performed without a loss of output power. Data from characterization of the Draper 2.3 GHz amplifier under RF drive demonstrates the potential value of using temperature-compensated input drive instead of a fixed level of input drive at all temperatures. A specific method of implementing temperature-compensated input drive was not described in this chapter, but possible techniques were suggested.

The second technique considered in this chapter involves the use of a diode to clamp the negative swing of voltage at the gate of the power amplifier transistor, and thus reduce drain–gate voltage stress. Effects of using the technique were determined through simulation of a reoptimized version of the Draper 2.3 GHz amplifier with a gate voltage-clamp diode. The simulation shows the promise of the technique as peak drain–gate voltage was noticeably reduced without significant negative effects on output power or efficiency. Limitations on the effectiveness of the technique were discovered though, including transistor package parasitics, diode nonidealities, and inductive current preventing the diode from turning "off", which restrains positive

[4]Such a change, for example, could be the inclusion of a "snubber" circuit.

voltage swing at the gate of the transistor and thus reduces amplifier gain. These limitations can likely be mitigated by more tightly integrating components to reduce parasitics, carefully selecting clamp diodes to minimize nonidealities, and changing gate network circuitry to prevent inductive current from keeping the diode on.

Chapter 6

Conclusion

This chapter concludes the thesis. The first section summarizes the work presented in previous chapters, while the second section provides some guidance for future research that might stem from the work done here.

6.1 Summary of Thesis

This thesis has explored issues related to breakdown in microwave power amplifiers. Specifically, this thesis has focused on breakdown in the Transcom TC2571 PHEMT, and the effects this has on the Draper Laboratory 2.3 GHz microwave power amplifier in which the transistor is used. Characterization of breakdown, including the effects of walkout and recovery, was performed under DC and RF conditions. Circuit design techniques to mitigate device degradation due to breakdown were also described.

Chapter 2 focused on DC characterization of off-state breakdown in the TC2571 under two-terminal and three-terminal conditions across a range of currents and temperature. As expected, at higher temperatures, the dominant mechanism involved in off-state breakdown appeared to be tunneling/thermionic field emission. However, surprisingly, the dominant mechanism involved in off-state breakdown at lower temperatures appeared to be impact ionization, particularly at higher levels of current.

Chapter 3 described RF characterization of average reverse gate current in the Draper 2.3 GHz power amplifier across a range of RF input drive levels, tempera-

ture, and biasing conditions. An increase in drain bias voltage led to an increase in average reverse gate current for a fixed level of RF input drive. Additionally, for a fixed level of RF output power, an increase in gate bias voltage led to a decrease in average reverse gate current. Tests under all conditions showed a decrease in average reverse gate current with temperature, which indicates that impact ionization is dominant in breakdown under RF drive for the amplifier. Based on the prevalence of impact ionization and the relatively large levels of average reverse gate current seen, it was suggested that on-state breakdown was dominant in the creation of reverse gate current in the amplifier.

Chapter 4 covered characterization of breakdown walkout and recovery in the TC2571. The first section of the chapter focused on DC characterization of walkout and recovery. Characterization of walkout was performed at three temperatures using two-terminal stress of the TC2571, and showed that walkout appeared to proceed more quickly at higher temperatures as the drain–gate breakdown voltage rose more rapidly for a fixed level of reverse gate current under these conditions. This was believed to be the result of electrons occupying traps faster at higher temperatures. The device also showed faster recovery and electron detrapping at higher temperatures as breakdown voltage decreased more rapidly after the removal of stress under these conditions. Long term tests showed that the final value of breakdown voltage after recovery degraded significantly from its initial value, which indicated that the creation of traps may occur during breakdown stress in the device. This possible trap creation also manifested itself as a rapid initial drop in drain–gate breakdown voltage immediately after the application of stress. While the trapping and detrapping of electrons may not be a permanent effect in the device, the creation of traps does appear to be permanent.

The second section of Chapter 4 focused on RF characterization of walkout in the Draper 2.3 GHz amplifier. Testing was performed using a stress cycle that was designed to replicate operational conditions for the amplifier. Observations of average reverse gate current showed that significant walkout occurred after use of the stress cycle. While walkout led to a noticeable decrease in amplifier gain at lower levels of

RF input drive, it had no negative effect on amplifier saturated output power, which actually appeared to increase slightly after walkout. Walkout under RF conditions also proceeded more quickly at lower temperatures, which is likely due to the increased levels of reverse gate current seen under these conditions. The results of walkout characterization of the amplifier present a dilemma about continuous operation since the amplifier must be driven into saturation in order to maintain a steady level of output power over time, but it is under these conditions where the amplifier is likely to show the most walkout and degradation.

Chapter 5 described two circuit design techniques that might be used to mitigate device degradation due to breakdown stress in microwave power amplifiers. The first technique was temperature-compensated input drive, and involved the use of attenuated input drive at lower temperatures to take advantage of higher amplifier gain and reduce reverse gate current. The second technique was the use of a diode to clamp negative voltage swing at the gate of the transistor, and thus reduce drain–gate voltage stress. The use of a clamping diode showed great promise, but was limited by the presence of several factors, including transistor package parasitics, diode nonidealities, and inductive current preventing the diode from turning "off", which in turn restrained positive voltage swing at the gate. Methods for dealing with these limitations were suggested.

6.2 Suggestions for Future Research

This thesis has explored several areas of interest related to breakdown in microwave power amplifiers and PHEMTs, and has only scratched the surface of many of them. There are many ways to build upon the research presented here, and investigate the research possibilities that were not explored. This section describes a few potentially useful avenues for future research.

As mentioned at the end of Chapter 3, on-state breakdown was not initially considered in this thesis as a possible mechanism for reverse gate current since the amplifier is a high-efficiency switching power amplifier, and therefore has minimal periods of

operation where the transistor is on and there is a large drain voltage. However, the characterization of Chapter 3 does indicate that on-state breakdown is dominant in the creation of reverse gate current in the amplifier under RF drive. Therefore, it would be useful to investigate on-state breakdown under DC conditions in the TC2571 PHEMT since this was not considered in Chapter 2, where DC characterization of only off-state breakdown was performed. A method of DC characterization of on-state breakdown, called the gate current extraction technique, is described in [23].

Characterization of breakdown in the TC2571 PHEMT showed several interesting features that appear to conflict with existing research described in the literature. The prevalence of impact ionization in off-state breakdown in the TC2571 at low temperatures is one such direct contradiction of the literature, which states that tunneling and thermionic field emission should be dominant at all temperatures [7, 9, 10]. Additionally, the device showed faster walkout under DC two-terminal conditions at higher temperatures, which is contrary to research that indicates that increased phonon scattering at higher temperature should reduce device degradation due to hot-electron stress [11]. Finally, while the gain of the Draper 2.3 GHz amplifier decreased after walkout for lower levels of input drive, the saturated output power of the amplifier actually increased, which contradicts research that device characteristics like output power should degrade during walkout [10, 11]. Investigation of each of these interesting features of the TC2571 PHEMT may be difficult without more specific information from Transcom about the device's design, but valuable information may still be gained from further characterization of the device.

As seen at low levels of RF input drive in Figures 4-5 and 4-8, characterization of walkout in the Draper 2.3 GHz amplifier under RF drive did not show the amplifier reaching a "steady state" where output power leveled off and was stable with continued stress. Indeed, if the trends at lower levels of input drive are extrapolated, it would appear that amplifier gain would continue to degrade indefinitely with continued stress. Therefore, further long term testing of walkout in the amplifier under RF drive would be useful. Such testing could also help determine if the increase in saturated output power seen after walkout in the amplifier is a temporary effect, or

if it continues indefinitely.

The three-terminal model of breakdown current presented in Appendix A could not be tested due to the lack of a model that accounted for the temperature dependence of other device characteristics. If such a temperature-dependent model existed, then it would be possible to test the usefulness and accuracy of the three-terminal model in replicating breakdown effects in the TC2571, which would be incredibly valuable. Data from DC characterization of on-state breakdown in the TC2571 would also be useful for testing of the three-terminal model. If the three-terminal model were found to be useful and accurate, it could then be applied in circuit simulation to optimize amplifier designs for minimal reverse gate current under RF drive, which could decrease device degradation due to breakdown stress.

Temperature-compensated input drive was described in Chapter 5 as a potentially useful technique for reducing device degradation due to breakdown stress. However, the technique was not actually implemented in this thesis, and only data from characterization of the amplifier under RF drive was used to defend the usefulness of the technique. Implementation of temperature-compensated attenuation in the driver stage for the Draper 2.3 GHz amplifier would help to confirm the value of the technique, and could be as simple as using a passive temperature-compensated attenuator between the driver and power amplifier stages [21].

The use of a diode to clamp negative gate voltage swing in Chapter 5 also showed great promise to reduce device degradation due to breakdown stress. However, several limitations were imposed on the technique due to nonidealities and parasitics, and these will need to be overcome for the technique to be a viable method of reducing device degradation. The mitigation of transistor package parasitics is necessary to remove resonance effects from gate drive, and could be accomplished by fabricating the amplifier in a multi-chip module (MCM) process where components are more tightly integrated. The mitigation of package parasitics could also help in reducing the effect that inductance has on keeping the diode in conduction when the amplifier enters its "on" state, which limits the positive swing of voltage at the gate of the device and decreases amplifier gain. However, it may also be necessary to add additional

circuitry to deal with the problem of inductance, like a "snubber" circuit. Diode nonidealities like diffusion and depletion capacitance and ohmic resistance also need to be dealt with, but these can probably be taken care of through careful device selection and reoptimization of input network parameters.

Additional circuit design techniques may also be discovered to have useful effects in mitigating device degradation in microwave power amplifiers. One such technique might be the use of differently "shaped" input drive waveforms to the power amplifier. In this thesis, only standard sine wave input drive waveforms were used with the Draper 2.3 GHz power amplifier. With a more carefully chosen input drive waveform shape, it may be possible to effectively "predistort" the input drive such that the drive waveform at the gate of the transistor minimizes drain–gate voltage stress while maintaining output power and efficiency. Such a change in input drive waveform would also likely remove the need for a diode to clamp negative gate voltage swing. However, the technique will likely be limited by the same issue of transistor package parasitics that limits the use of a gate voltage-clamp diode. Furthermore, implementation of the technique will likely require additional driver amplifier circuitry, which may pose a drawback in terms of additional circuit area, complexity, and power consumption.

Appendix A

Breakdown Modeling for Circuit Simulation

Circuit simulation is a valuable tool that aids the design process by allowing for accurate and rapid evaluation of circuit designs. In order for circuit simulation to be useful, though, accurate models of circuit components are required. For PHEMT microwave power amplifiers where breakdown stress is a factor, this means having an accurate model of reverse gate current due to breakdown can be incredibly valuable. Unfortunately, existing models of reverse gate current due to breakdown are often overly precise and complex physics-based models that require extensive information about the device's design and are not suited for use in circuit simulation software like SPICE [9]. Other models that are designed for use specifically in circuit simulation software tend to be overly simplistic, and often neglect aspects of breakdown like impact ionization current [24]. Therefore, creating a simple, yet accurate, model that is suitable for use in circuit simulation software could be extremely valuable.

This appendix consists of two sections, each of which covers a different model that might be used to simulate breakdown. The first section covers a simple two-terminal model that describes reverse gate current as solely dependent on the drain–gate voltage V_{DG}, and is perhaps most applicable to off-state breakdown in certain regions of operation. The second section covers a more complex three-terminal model that should be able to accurately model both on-state and off-state breakdown effects.

A.1 Simple Two-Terminal Model

As described in Chapter 2, three-terminal DC characterization of the TC2571 PHEMT showed relatively little effect on drain–gate voltage V_{DG} by gate–source voltage V_{GS} in the off-state. Therefore, it might be practical to create a two-terminal model of off-state breakdown current from the drain to the gate that depends only on V_{DG}. A schematic of this model is given in Figure A-1. As indicated by the schematic, the two-terminal model of I_{DG} can be added to an existing model for the transistor that does not account for breakdown current.

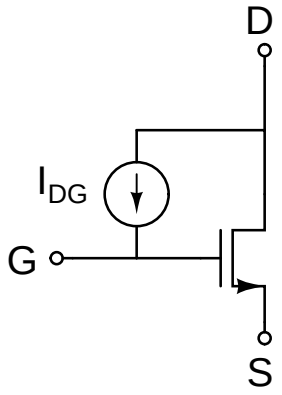

Figure A-1: A schematic of the simple two-terminal model of reverse gate current due to off-state breakdown.

As an initial guess, a rough possible model for the drain–gate current was suggested as:

$$I_{DG} = I_T + I_{TFE} + I_{II}$$

where the total drain–gate current I_{DG} is represented as the sum of tunneling current (I_T), thermionic field emission current (I_{TFE}), and impact ionization current (I_{II}). Possible equations for each of these components, based on temperature dependence, were suggested as:

$$I_T = I_{S1} \cdot e^{V_{DG}/B_1}$$

$$I_{TFE} = I_{S2} \cdot e^{(A_2 T + V_{DG})/B_2}$$

$$I_{II} = I_{S3} \cdot e^{(-A_3 T + V_{DG})/B_3}$$

where I_{Sn}, A_n, and B_n are positive constants, T is the temperature in kelvin, and V_{DG} is the drain–gate voltage. Each component has an exponential dependence on V_{DG}, and the role of A_n is to provide a positive temperature coefficient for I_{TFE} and a negative temperature coefficient for I_{II}.

After this model was created, the parameters I_{Sn}, A_n, and B_n were optimized to match the two-terminal off-state breakdown characteristics shown in Figure 2-1. Surprisingly, as shown in Figure A-2, given the roughness of the model, the model appears to fit the measured data fairly well. In particular, the transition between the region where impact ionization current dominates and the region where thermionic field emission current dominates appears to match well for this transistor. The model also seems to accurately replicate the observation made in Chapter 2 that the transition between these regions occurs at lower temperature for lower currents.

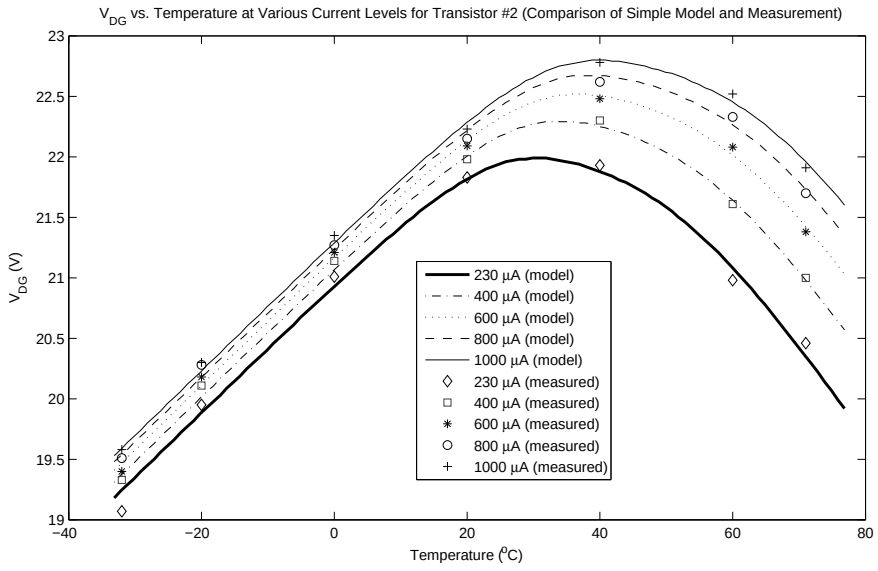

Figure A-2: Comparison of simple model and measurement values for Transistor #2 drain–gate voltage V_{DG} versus temperature at various current levels.

This simple two-terminal model has several limitations though. The first is its application over a broad range of current and temperature. The simple model's rough approximations for total thermionic field emission current and tunneling current are far simpler than the current density equations that are given in the literature [9]. The

approximation for impact ionization current is also far simpler than the equation given in the literature [13], which relies on a three-terminal description. The approximations are likely to limit the model's utility over a wide range of temperature and current.

Since the simple model is also a two-terminal model, it has limited usefulness in applications that involve on-state breakdown, which is a three-terminal effect. Specifically, it has the potential to significantly underestimate reverse gate current in simulation for a power amplifier where on-state breakdown is dominant under RF drive. This dominance of on-state breakdown appeared to be present in Chapter 3 for the amplifier studied in this thesis.

Even given the simple two-terminal model's limits, it might still have useful applications. In circuits where off-state breakdown is dominant and there is a small range of interest in reverse gate current and/or temperature, the two-terminal model may be a sufficient, simple model that can be usefully applied to characterizing circuit behavior. As mentioned in Chapter 3, though, for the amplifier studied in this thesis, two-terminal off-state breakdown effects cannot account for the amount of average reverse gate current seen in the amplifier under RF drive. Therefore a different model that accounts for three-terminal on-state breakdown effects is necessary for accurate simulation of this particular circuit.

A.2 Full Three-Terminal Model

A full three-terminal model of the TC2571 PHEMT is required in order to simulate the possible on-state breakdown effects under RF drive that were described in Chapter 3. Such a model would need to be able to simulate two-terminal breakdown effects due to tunneling and thermionic field emission, as well as three-terminal breakdown effects due to impact ionization. A schematic for this type of model is given in Figure A-3. The model consists of two diodes (a gate–drain diode and a gate–source diode) and two impact ionization current sources (drain–gate I_{IIg} and drain–source I_{IIs}) that have been added to an existing model of other PHEMT device characteristics.

The gate–drain and gate–source diodes are used for two purposes: to model the

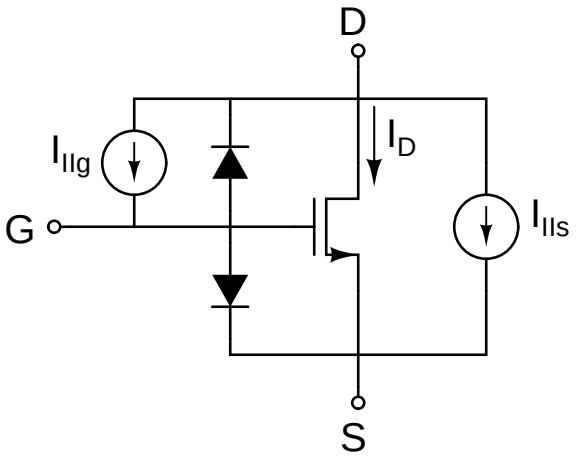

Figure A-3: A schematic of the three-terminal model of reverse gate current due to breakdown.

forward gate current created by forward-biasing either Schottky junction, and to model the reverse gate current due to tunneling and thermionic field emission in both junctions. For typical power amplifier operation, it is most important to model forward gate current for the gate–source diode, and reverse gate current for the gate–drain diode, although the forward and reverse components should be modeled for both diodes for the best accuracy. The forward gate current for both diodes can be modeled by the "standard" diode current equation, which is generally given as:

$$\mathrm{I_{DIODE}} = \mathrm{I_S(T)} \cdot (e^{\mathrm{v_{DIODE}}/(\mathrm{nv_{TH}})} - 1)$$

where $\mathrm{v_{DIODE}}$ is the (forward) voltage across the diode, $\mathrm{v_{TH}}$ is the thermal voltage[1], n is a constant, and $\mathrm{I_S}$ is the "saturation current" and is a function of temperature[2]. Since this equation is valid only for forward diode current, it is only applicable when $\mathrm{v_{DIODE}}$ is greater than zero.

A variety of equations exist for modeling the reverse gate current in the junction diodes [24]. These equations vary greatly in their complexity and general structure, and some may be more appropriate for particular devices than others. A relatively

[1]The thermal voltage is equal to $\frac{\mathrm{kT}}{\mathrm{q}}$, where k is Boltzmann's constant, T is the temperature in kelvin, and q is the elementary charge.

[2]Equations for the temperature dependence of $\mathrm{I_S}$ can be found in [24].

simple equation that is used to model the reverse gate current, and which is very similar to the standard equation for forward diode current, is:

$$I_{DIODE} = -I_{Sr}(T) \cdot (e^{-(v_{BR}+v_{DIODE})/(n_r v_{TH})} - 1)$$

where the parameters are generally similar to those for the forward diode current equation, but with the addition of a new parameter v_{BR} that represents a "reverse breakdown voltage". The temperature dependence of I_{Sr} is often modeled in the same way as the temperature dependence of I_S in the forward diode current equation. This dependence generally gives reverse gate current magnitude a positive temperature coefficient, which thus makes it suitable for modeling current that is due to a combination of tunneling and thermionic field emission. Furthemore, this model is only suitable for negative diode voltages where $v_{DIODE} < v_{BR}$. For negative diode voltages where $v_{DIODE} > v_{BR}$, the reverse diode current can be modeled as zero.

The drain–gate current source I_{IIg} and drain–source current source I_{IIs} in the three-terminal model represent current created by impact ionization in the device's channel. In effect, the current sources model the fact that a fraction of impact ionization leaves the channel through the gate, while the remaining amount leaves through the source. The equation for the reverse gate current due to holes leaving the channel through the gate is give in the literature [13, 25, 26] as[3]:

$$I_{IIg} = A_g I_D e^{-TE_i/(V_{DG}-V_T)}$$

where V_{DG} is the drain–gate voltage, V_T is the device's threshold voltage, T is the temperature in kelvin, I_D is the drain current (as shown in Figure A-3), E_i is the ionization energy, and A_g is a constant. The equation for impact ionization current that leaves through the source is then:

$$I_{IIs} = A_s I_D e^{-TE_i/(V_{DG}-V_T)}$$

[3]The $(V_{DG} - V_T)$ in the denominator of the exponential may need to be changed to $(V_{DG} + V_T)$ since there may exist confusion about the sign of V_T in the literature.

where the parameter A_s replaces A_g. Both equations demonstrate the negative temperature coefficient of impact ionization in PHEMT devices, as well as the increase in impact ionization current with an increase in V_{DG}. Impact ionization current is also proportional to drain current I_D since the creation of holes by impact ionization is proportional to the number of hot electrons in the channel of the device. For any level of impact ionization current, a constant fraction is modeled as leaving the channel through the gate, while the rest is modeled as leaving via the source.

This three-terminal model has the potential to accurately replicate the full set of breakdown effects seen in the TC2571 PHEMT. The gate–source and gate–drain diodes are able to model the two-terminal effects of tunneling and thermionic field emission reverse gate current, and the impact ionization current sources are able to model the three-terminal, on-state impact ionization current. Unlike the simple two-terminal model, the three-terminal model makes a distinction between on-state and off-state breakdown effects, which allows for accurate three-terminal simulation. The model also allows for the use of equations for each component of reverse gate current that provide accuracy over a wide range of temperature and current.

The three-terminal model also helps provide a possible explanation for the two-terminal impact ionization current seen at low temperature in the TC2571 in the DC tests of Chapter 2. Since impact ionization is a three-terminal effect that requires hot carriers in the channel, it would seem to be impossible for impact ionization reverse gate current to be present in a test where the source is left floating. However, since the TC2571 has a negative threshold voltage, the device can be "on" with a negative gate–source voltage. This, in turn, means that it is possible for the device to be on and have drain–source current flow in the reverse-biased gate–source diode instead of leaving via the source. Thus, a drain–source current can be present even when the source is left floating, which can lead to impact ionization current in a two-terminal test. At low temperature, it is therefore possible that the impact ionization current dominates in the two-terminal test when compared to tunneling and thermionic field emission current in the gate–drain diode.

Although it is believed that this model should be able to accurately simulate

reverse gate current due to breakdown in the TC2571 PHEMT, it was not possible to test the model during the research for this thesis. A model across temperature of the remaining device characteristics is not available, and therefore no suitable model exists to which to add the three-terminal model of breakdown current. If a model that accounted for the effects of temperature on other device characteristics did exist, though, it would be possible to test the usefulness and accuracy of the model.

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