Design and Fabrication of Quantum-Dot Lasers

by

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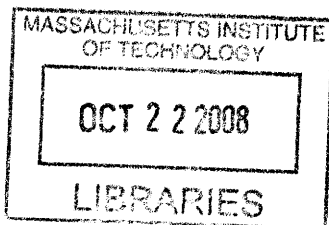August 15, 2008

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Abstract

Semiconductor lasers using quantum-dots in their active regions have been reported to exhibit significant performance advantages over their bulk semiconductor and quantum-well counterparts namely: low threshold current, high differential gain and highly temperature stable light-current characteristics. This thesis investigates the lasing characteristics of a ridge-waveguide laser containing seven layers of quantum dots as the active region.

A summary of the electrical and optical performance data of the heterostructure quantum dot lasers, as well as previously fabricated quantum well lasers, is presented. The motivation of using InAs quantum dots in the active region is to produce near infrared emission for telecommunication applications.

Thesis Supervisor: Leslie A. Kolodziejski
Title: Professor of Electrical Engineering and Computer Science

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Chapter 1

Introduction

1.1 Motivation

The roadmap of microelectronics processing has had silicon as its platform since its inception. Over the years, fabrication technologies have been developed and vastly improved, allowing for large scale production and integration of low cost electronic chips. However, further advancement of silicon microelectronics, especially in the fabrication of transistors in the submicron regime, is currently faced with problems that include inescapable material, technological and physical limitations [4]. The fundamental physical limitations include those based on the nature of the interconnects in transistors. The exponential growth of Moore's law has allowed chip designers to scale down transistors so as to integrate tens of millions of transistors onto a single chip, enhancing the overall chip performance in terms of gigaflops[1]. However, the interconnects on these chips are intrinsically resistive metal wires, whose electrical resistance increases as the cross-sectional areas are scaled down. Associated with this increase in resistance is heat generation and the negative thermodynamic effects on the other chip components. Furthermore, as the separation of these wires decreases, the wires start to exhibit antenna-like cross-talk behaviour with unwanted signals being transmitted between the interconnects. Lastly, as the critical dimensions decrease to tens of nanometers, circuit theory, in which spatial dimensions play no part, must

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[1]A giga flop is a measure for computing speed equal to 10^9 floating-point operations per second.

be replaced with transmission line theory. With the use of transmission line theory comes the importance of capacitance per unit length, a quantity that has an inverse relationship with the speeds at which signals can be transmitted.

The emerging field of integrated photonics proposes to solve some of the limitations with electrical interconnects. The elements in such a photonic chip are connected through waveguides, where light is confined by total internal reflection. The integrated optical components are fabricated using planar fabrication techniques, as for electrical interconnects. The individual optical components are integrated in a single substrate, resulting in a compact and robust photonic circuit, which can be optically connected through optical fibers. Although wires will always be used for short-range interconnection, optical communication attempts to alleviate many of the inherent problems associated with metal wire interconnects. Extensive optical data transmission via complex coast-to-coast fiber networks exists today because of low loss optical fibers and the photons' immunity to noise that is created by electromagnetic interference. The current goals in the integrated optics field are to determine how to integrate the various optical components onto single substrates as well as efficiently couple individual components [5].

The goal is that photonic Integrated Circuits (PICs) will complement the well established Silicon Integrated Circuits (Si-ICs). The state-of-the-art of integrated optics still lags far behind its electronic counterpart with only a few basic functions that are commercially feasible. This work addresses a key optical component of a PIC, the laser. The quantum-dot heterostructure laser presented in this work is not the kind that would ultimately be integrated in a PIC. Instead, it is a less complicated, relatively easily fabricated laser whose opto-electronic characteristics demonstrate the efficiency of the novel active region for application in a more complicated PIC laser.

1.2 Quantum Dots

Quantum Dots (QDs) are semiconductor structures in which the charge carriers are spatially confined in all three dimensions. Due to the strong three-dimensional

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(3D) carrier confinement, devices that employ quantum dots have unique capabilities that are otherwise practically unachievable with bulk semi-conductors, or even two-dimensionally (2D) confined quantum wells. QDs are nanocrystals of narrow band-gap material that are embedded in a wider band-gap material and can be grown a number of ways and the choice of fabrication depends on the application.

One of the fabrication methods is by Molecular Beam Epitaxy (MBE) in which, under certain growth conditions, self-assembled quantum dots nucleate due to the lattice-mismatch strain with the two-dimensional wetting layer on which they are grown. If grown under the right conditions, the QDs should be coherently strained with narrow inhomogeneous broadening. This growth method is known as the Stranski-Krastanov (SK) growth mode; the QDs in this work were SK-grown. Some of the limitations of SK growth include the cost of fabrication and the lack of control over the position of the dots but more importantly, the lack of precise control over the size of the dots, which determines the emission wavelength.

1.3   Overview

By exploiting the 3D quantum confinement of carriers within QDs, lasers with superior electrical and optical properties can be developed. The index-guided QD heterostructure lasers that were fabricated in this work investigate the quality of the epitaxially-grown active region. This thesis presents the various steps involved in the design, fabrication and characterization of these lasers. Optical simulations enabled the optimum design of these lasers, which were then fabricated by standard fabrication techniques, and then upon completion, were characterized.

Chapter 2 discusses the basics of lasers with special emphasis on QD heterostructure lasers.

Chapter 3 discusses the design and simulation of these lasers.

Chapter 4 discusses the fabrication of the lasers, using the various fabrication techniques and results are discussed.

Chapter 5 examines the characteristics of the lasers.

Finally, Chapter 6 summarizes this work and presents future directions of investigation.

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Chapter 2

Laser Basics

2.1 Background

The advancement of microelectronic fabrication techniques have enabled the development of semiconductor lasers. These lasers have gained special importance in the microelectronics arena due to their compactness, the possibility of fabricating many individual lasers on a single substrate as well as their ability to be integrated onto a chip. This section presents an overview of laser technology and the history and development of quantum dot heterostructure lasers.

2.2 Semiconductor Lasers

Semiconductor lasers emitting at telecommunication wavelengths $(1.3 - 1.6\mu m)$ have been developed from compounds of Column III elements such as: Gallium (Ga), Aluminium (Al), Indium (In), and Column V elements such as: Arsenic (As) and Phosphorus (P). Long wavelength $(2 - 3\mu m)$ Antimony-based emitters have also recently been developed [6]. The opto-electronic properties of semiconductor lasers are determined by the band structure of the semiconductor materials therein. Consider the band structures of two of the most prevalent semiconductors: Gallium Arsenide (GaAs) and Silicon (Si). The lowest energy level in the conduction band in GaAs lies directly above the highest energy level in the valence band, making GaAs a direct

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band-gap material. The consequence is that an electron located at the bottom of the conduction band can recombine with a hole at the top of the valence band simply by the emission of a photon, making GaAs an efficient light-emitting material. Si, on the other hand, is an indirect band-gap semiconductor in which in order to conserve momentum, electron-hole recombination must be accompanied by the emission or absorption of a phonon. This two-step process makes indirect gap materials less optically efficient than direct gap materials. This explains why III-V materials, most of which are direct band-gap, are widely used in opto-electronic devices.

A laser accomplishes light amplification via the radiative recombination of excited charge carriers in the presence of positive optical feedback that reinforces the radiation field. A medium can either be optically-pumped or electrically-activated and may emit light through spontaneous or stimulated processes. The medium can also absorb light via stimulated absorption as shown in Figure 2-1.
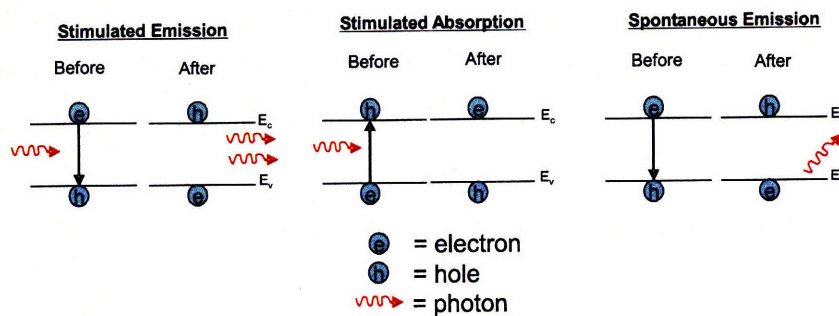
Figure 2-1: Light-Matter Interaction Processes.

Excited carriers will normally release their excess energy in the form of incoherent radiation and, in so doing, revert back to a stable state in a process called spontaneous emission. Alternatively, in the presence of radiation, a photon can possibly interact with an excited carrier while that carrier is still in its high-energy state. The carrier may then release its excess energy in the form of a photon that is in phase with, has the polarization of, and propagating in the same direction, as the stimulating photon in a process called stimulated emission. These emitted in-phase photons bounce back and forth inside the resonator cavity that includes the active medium and thus amplify

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the radiation with every pass. This optical feedback is usually achieved by placing high reflective coatings or having well-cleaved mirror-like facets at both ends of the cavity.

In accordance to Fermi-Dirac statistics, most carriers are ordinarily in their lowest energy state. In order to achieve lasing, the number of electrons in the conduction band must exceed a threshold value so that the probability of emission is higher than absorption. A population inversion [1] in which most carriers are excited to higher energy states, must be created and maintained so that stimulated emission, and not absorption, dominates. Pumping by electrical or optical means leads to a band structure depicted in Figure 2-2 in which more energy is required for absorption than for emission so that the material exhibits a net gain of radiation.
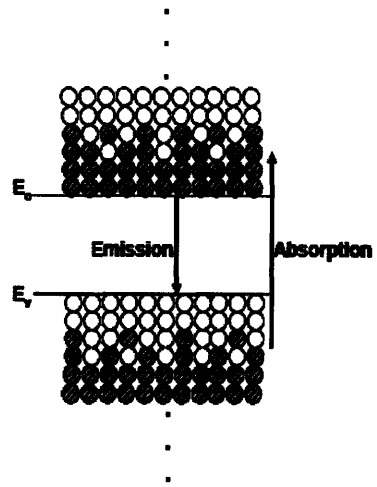
Figure 2-2: A simplified depiction of the active region due to excitation. Shaded circles represent electrons or filled states while unshaded circles represent holes or empty states [1].

2.3 Diode Lasers

The first semiconductor lasers date back to 1962 [7]. They were homojunction lasers in which a radiative interface was formed between differently doped semiconductor materials of the same band gap as shown below in Figure 2-3.
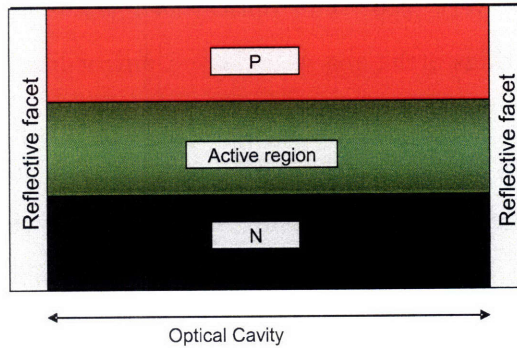
Figure 2-3: Simple schematic of an edge-emitting p-n junction laser with the reflective facets providing feedback.

At the time, this was the most realistic way of obtaining large concentrations of electrons and holes in close proximity to each other so that radiative recombination would occur. These lasers had enormous threshold current densities, on the order of $10^4 A/cm^2$, and were operated under Continuous Wave (CW) mode at cryogenic temperatures ($T \leq 77K$). At the end of the decade, amid skepticism over the idea of making a heterostructure with sufficiently different band gap while maintaining lattice matching, the concept of double heterostructures was proposed and developed, yielding lasers with better electrical and optical confinement than their homojunction predecessors [8].

The development of growth technologies such as Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) has resulted in the realization of novel separate confinement heterostructures (SCH) upon which most modern lasers are now built. A SCH is formed by surrounding a low band gap material with a higher band gap material. Materials with a small energy band gap typically have higher indices of refraction than larger band gap materials and therefore the optical mode is vertically confined in the small band gap material. Lateral confinement can be achieved in many ways including placing a lower index cladding material on either side of the active medium. A quantum well laser is the simplest SCH in which electrons and holes are confined within the dimension of the quantum well so that recombination only occurs at the site of the well. The small size of the gain region

means that fewer net carriers are required to reach a given threshold current density.

2.4 Quantum Dot Heterostructure Lasers

The novel idea to "exploit quantum effects in heterostructure semiconductor lasers to produce wavelength tunability and to achieve lower threshold current densities by reducing the number of translational degrees of freedom of the carriers and thus changing the density of states at the band edges" was first proposed by Dingle and Henry in 1976 [9]. However, it was not until the turn of the 21st century that lasers using confinement in two directions (Quantum wires) and all three directions (Quantum dots) gained physical realization. Quantum wells had become widely explored by the late 70s, but carrier confinement existed in only one direction and so the need for improvement was clear.

2.4.1 Development

The road toward the development of Quantum-dot QD heterostructure lasers has been long. The major breakthrough occurred in 1963 when Alferov et. al implemented the use of a double heterostructure in order to realize electrical confinement [12, 13]. Shortly after in 1966, the idea of using a waveguide to achieve optical confinement was theorized [14]. Today molecular beam epitaxy (MBE) and metal organic chemical vapour deposition (MOCVD) continue to dominate over other fabrication techniques in the growth of QD heterostructures under the Stanski-Krastanow (SK) method of growing self-assembled QDs. Under typical growth conditions [10], and with increasing strain energy in the strained layer (such as InAs in this work), the would-be planar layer gradually transitions into small energetically favourable islands - QDs. The dimension of the islands is inversely proportional to the emission wavelength due to the resulting modification in carrier confinement. QD dimensions can be adjusted by varying the substrate temperature and the amount of material deposited. Size can be also be adjusted by varying the composition of the material that defines the lattice mismatch.

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Both methods, MBE and MOCVD have their benefits and challenges. Specifically with MOCVD, the fabrication of QDs is difficult because of the high density of relaxed defect clusters that form as a result of increased strain and the complicated environment in which these layers are grown [15, 16]. Among the most important benefits of the SK method of epitaxial self-assembly includes the ability of growing a vast number of nanostructures in just one growth step. The resulting dense array of QD is necessary in order to provide modal gain sufficient for ground state emission [10, 3, 17]. The SK growth mode can yield QDs that are highly uniform in dimension and composition. However, self-assembled QDs still exhibit broad photo-luminescence (PL) spectral linewidths due to nano-scale variations in QD size, a feature that has adverse effects on laser performance [18]. Notwithstanding this shortcoming, SK growth still remains a prominent fabrication technique.

2.4.2   Performance Benefits

QD heterostructure lasers are a type of semiconductor laser that use quantum dots as their active media. Quantum dots are semiconductor nanocrystals of narrow band-gap material that are embedded in a wider band-gap material. Due to the strong 3D carrier confinement, devices that employ quantum dots have unique capabilities that are otherwise practically unachievable with bulk semi-conductors or even with 2D-confined quantum wells. These advantages have to do with the fact that with additional restriction of electron motion comes the discretisation of the allowed wave-functions with distinct indices along the confining direction(s). These previously unavailable wave functions result in a modification of the energy spectrum, which in turn changes the nature of the density of states, as illustrated in Figure 2-4.

In particular, in a QD, with dimensions on the order of an exciton Bohr radius, the density of energy states takes on the form of delta functions with peaks centered at atomic-like energy levels. This delta function density of states modifies the carrier distribution in such a manner as to enhance the concentration of charge carriers at the ground state at the expense of higher energy parasitic levels.

In theory, when QDs are used as the active region of electrically-activated semicon-
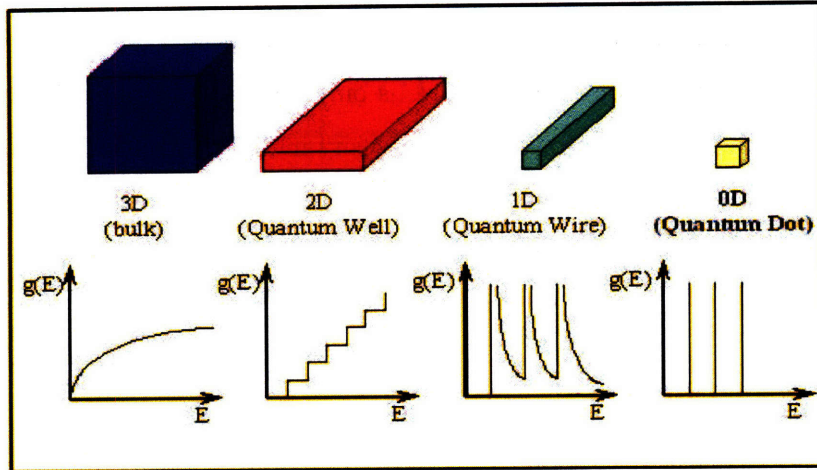
Figure 2-4: Density of states for charge carriers in structures with different dimensionalities [2].

ductor lasers, the vast majority of the injected non-equilibrium carriers are expected to relax into a narrow energy range near the bottom the conduction band in the case of electrons and near the top of the valence band, in the case of holes. The fact that the majority of the electrons and holes are located in the ground state energy levels of the conduction and valence bands respectively facilitates ground-state recombination, thus enhancing material gain for ground state emission. In reality however, this ideal situation is limited by a finite carrier capture time. There is a probability that non-radiative recombination within the quantum well may occur before the carriers have the chance to thermally relax into the ground state the quantum dot. Electronic transitions of carriers from the quantum well to the quantum dot occur at a finite rate. This finite rate dampens the radiative recombination current through the active region, ultimately limiting the output power from the laser [10].

As mentioned before, one of the direct results of the reduction in the carriers' translational degrees of freedom is in achieving lower threshold current densities, the injection current density above which light emission by stimulated emission dominates.

Another important functional benefit for the discretisation of energy states is that it reduces the influence of temperature on device performance. The spacing of the

energy subbands in QDs is on the order of 100s of meV while the average thermal energy of carriers at room temperature is only 10s of meVs, an order of magnitude smaller. As such, the threshold current density in QD lasers should be unaffected by temperature up to about 300K [11] since the carriers can only be thermally excited to a very limited range within these well-spaced energy levels. Carriers in excited levels would introduce loss in the device.

QD lasers are being developed to meet longer wavelength and higher power requirements. Herman et. al [19] have shown that the gain from a single layer of QDs is sometimes insufficient in overcoming internal optical mode losses in the cavity. This is especially true for short cavity lengths in which depositing high reflectivity coatings on the facets is not an option. Therefore, the growth of multi-stack QD layers has been developed in an effort to enhance modal gain [20]. In order for the formation of identical stacked structures, a smooth spacer layer surface between each QD layer is crucial so as to form QDs with uniform characteristics because even the slightest departure from uniformity would cause inhomogeneous broadening due to strain alteration.

Despite all these developments however, results published had, so far, indicated no significant speed performance over planar QW lasers until the idea of doping the QDs with holes was proposed and implemented. Deppe et. al have shown that for deep confinement potentials as in GaAs-based 1300nm lasers, p-type doping in conjunction with the intrinsically high carrier density associated with QDs is very effective in enhancing the gain characteristics so as to produce modulation response speed in excess of 30 GHz [3]. Figure 2-5 illustrates the relevance of the energy spacings of electron and hole energy levels [3].

Whereas the energy spacing for electrons is ~70meV, meaning that the electrons have a high probability of being confined to the ground state, the spacing for holes is ~10meV, which causes a thermal smearing of hole population among hole states. Thermal hole broadening has been shown to suppress gain performance [17]. Figure 2-5 illustrates that in the undoped QD layer case, charge neutrality requires an increase in the number of electrons that must be injected so as to achieve population inversion.
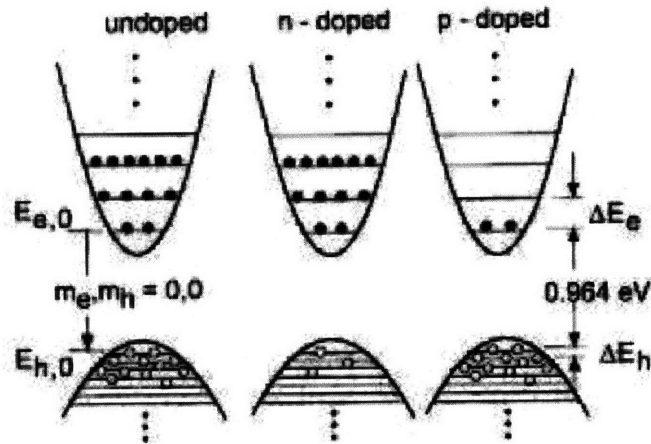
Figure 2-5: A schematic of QD energy levels with different built-in carrier distributions. The thermal smearing of the closely spaced hole energy levels requires that an excess of holes via p-type doping be built in so as to facilitate ground state recombination [3].

As a result, the injected radiative current must be increased and hence the differential gain is decreased [3]. If an excess of electrons is built in, as in the n-type doped case, the problem is made even worse because the injected holes that are thermally smeared among excited states recombine with the excess electrons in the higher energy states. If instead the hole density is increased as in the p-type doping case, the large built-in hole concentration ensures that there will be enough holes in the ground level of the valence band with which injected ground state electrons can radiatively recombine. As a result of p-type doping, room temperature ground state optical gain, as well as differential gain, can be increased.

2.4.3 Carrier injection and threshold condition

In order to understand the operational characteristics of lasers, one has to understand the fundamental principles. The following subsections, adapted from Chuang [21], present a semi-detailed discussion of the physical principles that govern basic heterostructure lasers.

When a forward bias is applied to a laser diode, the injection current density is assumed to be

$$J = \frac{I}{wL} \tag{2.1}$$

where I is the injection current, w is the width of the active region in the lateral direction and L is the length of the laser cavity.
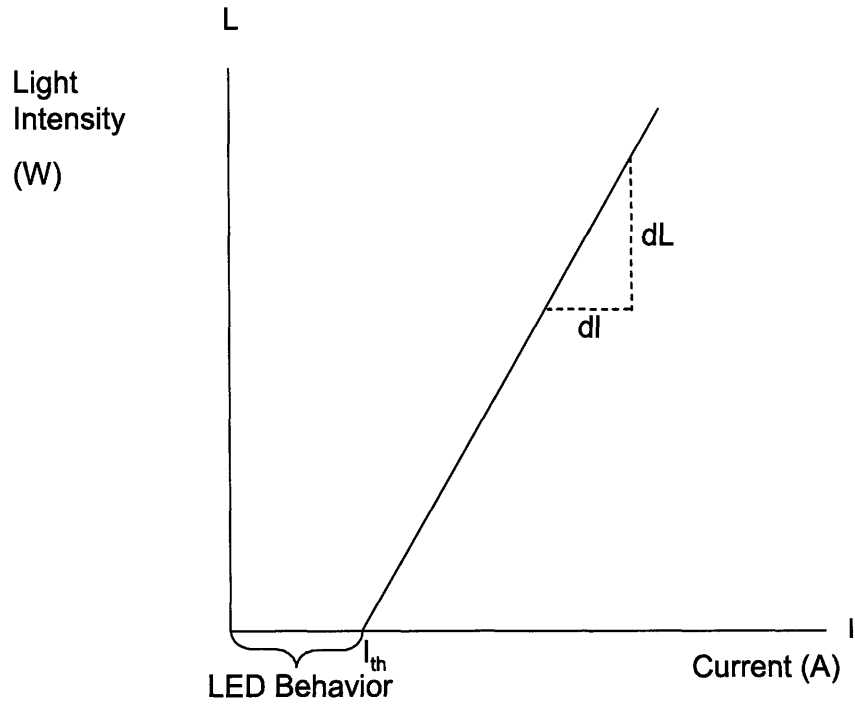
Figure 2-6: Light-Current (LI) relationship of a laser where I_{th} is the threshold current.

In an effort to understand charge carrier dynamics, which are at the heart of the emission processes, the nature of the carriers needs to be analysed. The concentration of the injected charge carriers n in the active region is determined by the second order differential equation:

$$\frac{\delta n}{\delta t} = D\Delta n + \frac{J}{qd} - R(n) \tag{2.2}$$

where the first term on the right hand side of Equation 2.2 is due to carrier diffusion,

the second term accounts for carrier injection into the active region of thickness d and the third term represents carrier recombination due to radiative and non-radiative processes.

For index-guided lasers[1], lateral carrier diffusion is negligible so that at steady state, carrier recombination can be simply expressed as

$$R(n) = \frac{J}{qd} \qquad (2.3)$$

In its more general form, the recombination rate is given by

$$R(n) = A_{nr}n + Bn^2 + Cn^3 + R_{st}N_{ph} \qquad (2.4)$$

where the first and second terms account for non-radiative and radiative processes respectively. The third term is due to non-radiative Auger recombination, a useful parameter to know for long wavelength lasers, and the fourth term is due to stimulated radiative recombination and is proportional to the density of impinging photons, N_{ph}.

Recombination occurs all the time, using the various processes depicted in Figure 2-1. Of particular interest in this work is what happens when the threshold current density has been reached. Below but near threshold, stimulated emission is still low so that Equation 2.4 can be simplified and written in the form

$$R(n) = n\left(A_{nr} + Bn + Cn^2\right) = \frac{n}{\tau_e(n)} \qquad (2.5)$$

where τ_e is the carrier lifetime, which is a function of carrier concentration.

Given J, q and d (recall Equation 2.3), if the coefficients A_{nr}, B and C are known, the carrier concentration, n, can be determined. In this analysis, low doping levels in the active region are assumed, hence electron-hole concentrations are equal, $n = p$. From the carrier concentration, the optical gain coefficient, g, which is one true measure of light amplification in a laser, can be extracted. The gain coefficient, g, as a function of carrier concentration is expressed in the form

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[1]The lasers that were fabricated in this work were all index-guided.

$$g(n) = a(n - n_{tr}) \tag{2.6}$$

where a is the differential gain and n_{tr} is the transparency point where gain, $g = 0$. This relationship should make intuitive sense since the injected carrier density is essentially the current flow through the active region. As shown in Figure 2-7 below, at carrier densities less than the transparency point, optical gain is negative, meaning that absorption dominates emission.
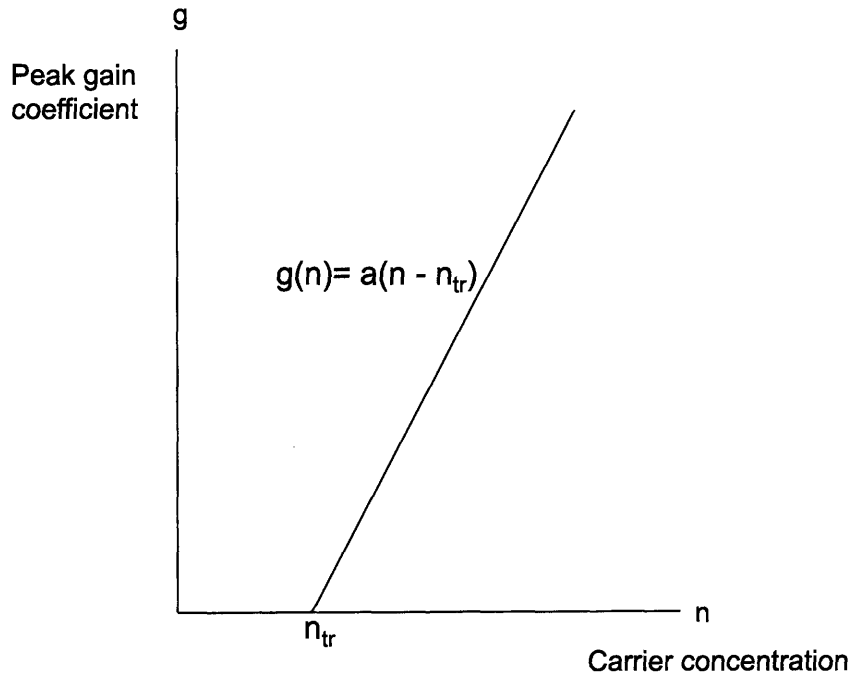
Figure 2-7: Peak optical gain coefficient g as a function of carrier concentration n.

The threshold material gain condition for a given mode is determined by

$$g_{th} = \alpha_i + \alpha_m \tag{2.7}$$

$$\alpha_i = \alpha_o(1 - \gamma) + \alpha_g \gamma \tag{2.8}$$

$$\alpha_m = \frac{1}{2L} \ln \frac{1}{R_1 R_2} \tag{2.9}$$

where g_{th} is the threshold material gain, an intrinsic property of the active region that is independent of the nature of optical confinement. γ is the optical confinement factor which determines α_i, the intrinsic loss due to absorption inside the waveguide α_g and outside the waveguide α_o. α_m accounts for the loss through the two end facets where the R_1 and R_2 are the reflectivities of the facets. Equations 2.3 and 2.4 suggest that an increase in injection current density will increase the carrier concentration, which will in turn lead to an increase in gain according to Equation 2.6. When the threshold current density J_{th} is reached, the carrier density n becomes clamped at the threshold value n_{th} and as will the gain according to Equation 2.7. Hence, the threshold current density in terms of carrier concentration can be expressed as

$$J_{th} = \frac{qd}{\tau_e\,(n_{th})} \tag{2.10}$$

2.4.4 Output power and quantum efficiency

The output power P_{out} of an edge-emitting laser with mirrors on both ends of the cavity can be expressed as

$$P_{out} = \frac{1}{2}\,[\hbar\omega]\,[N_{ph}]\,[Lwd_{op}]\,[v_g\alpha_m]\,[\eta_i] \tag{2.11}$$

where $\hbar\omega$ is the energy of a photon, N_{ph} is the photon density, $v_g\alpha_m$ is the photon escape rate, w is the width of the mode, L is the cavity length and $d_{op} = d/\gamma$ is the effective thickness of the optical mode. η_i is the internal quantum efficiency, the number of injected carriers that contribute to radiative recombination. Generally, $\eta_i < 1$. The output power can also be expressed in terms of the threshold current as

$$P_{out} = \frac{\hbar\omega}{q}\frac{\alpha_m}{\alpha_m + \alpha_i}\,(I - I_{th})\,\eta_i \tag{2.12}$$

An important measure of laser performance is the external differential quantum efficiency η_i, which is determined by

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$$\eta_e = \frac{dP_{out}/dI}{\hbar\omega/q} = \frac{\alpha_m}{\alpha_m + \alpha_i}\eta_i \qquad (2.13)$$

The inverse of the external differential efficiency is often of interest and can be expressed in terms of the laser cavity parameters as

$$\eta_e^{-1} = \eta_i^{-1}\left[1 + \frac{2\alpha_i L}{\ln(1/R)}\right] \qquad (2.14)$$

where $R = R_1 R_2$, the product of the facet reflectivities. A plot of the linear relationship between η_e^{-1} as a function of cavity length L is plotted in Figure 2-8.
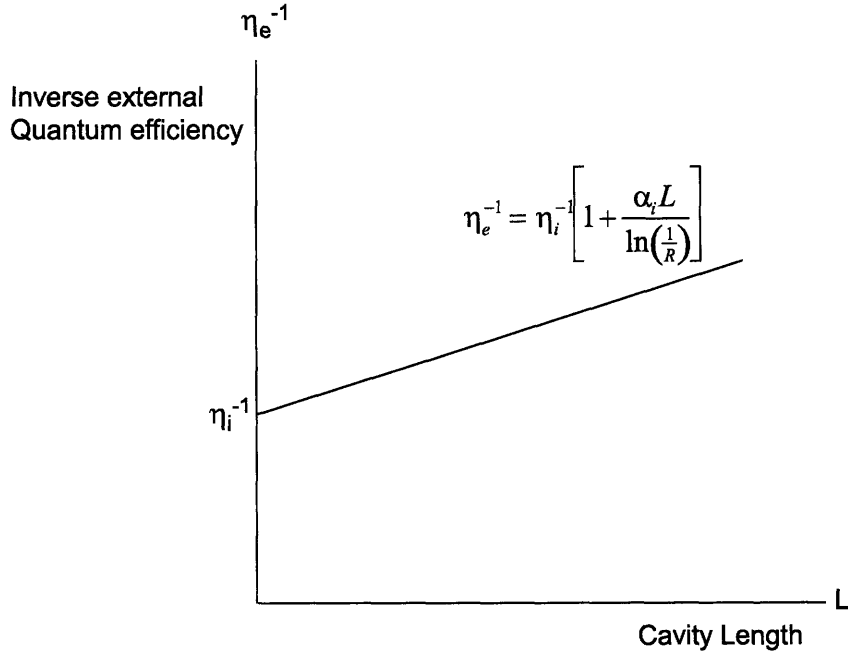
Figure 2-8: Inverse external quantum efficiency versus cavity length. The intercept with the vertical axis is the inverse intrinsic quantum efficiency.

Throughout this theoretical analysis, leakage current, which exists in real devices, has been neglected.

$$I = I_A + I_L = JwL + I_L \qquad (2.15)$$

In Equation 2.15 I is the total injected current, I_A is the current injected into the

active region and I_L is the leakage current. Equation 2.12 must be modified to reflect leakage current.

$$P_{out} = \frac{\hbar\omega}{q} \frac{\alpha_m}{\alpha_m + \alpha_i} (I - I_{th} - \delta I_L) \eta_i \qquad (2.16)$$

A typical relationship between output power and injection current in a diode laser is depicted in the Figure 2-9. Below threshold, where spontaneous emission dominates, little to no power is observed. Above threshold, stimulated emission begins to increase with the output power increasing linearly with current until saturation begins to manifest. Saturation occurs for many reasons including the fact that leakage current increases with injection current. In addition, increases in temperature due to junction heating may reduce the recombination lifetime τ_e resulting in a net decrease in emission.
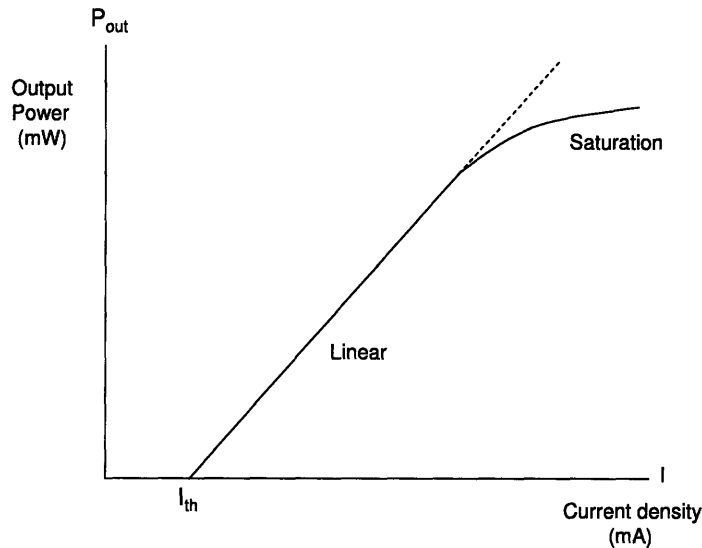
Figure 2-9: A typical LI curve of a laser diode.

Chapter 3

Design and Simulations

3.1   Design Concepts

There is a wide range of literature on the design of quantum dot heterostructure lasers. The central theme in considering laser design is how electrical and optical confinement are to be achieved. The most commonly fabricated semiconductor lasers are either gain-guided or index-guided whereby the difference between the two lasers is in the lateral confinement of the injected carriers and consequently, the optical mode in the active region.

In stripe-geometry, gain-guided lasers, the top metal contact is defined by fabrication processes. Injected carriers spread along the lateral direction due to lateral carrier diffusion and current spreading and as a result, the effective width of the carrier distribution, n, and the optical gain profile end up being wider than the actual metal contact width. The gain distribution is the mechanism behind the confinement of the optical mode in the lateral direction. Lateral carrier spreading also degrades the laser performance by increasing the threshold current and therefore reducing the quantum efficiency. In contrast, for index-guided lasers, such as the ridge waveguides lasers in this work, the lateral confinement of injected carriers and consequently the optical mode, are achieved by the use of a low-index dielectric. The low-index dielectric enhances the contrast in the lateral effective index profile, thereby confining the mode in the high-index region.

A schematic of the epitaxial structure of sample VA55 that was grown in this work is shown in Figure 3-1. The use of a separate confinement heterostructure enables electrical confinement while optical confinement is achieved by means of ridge waveguides.
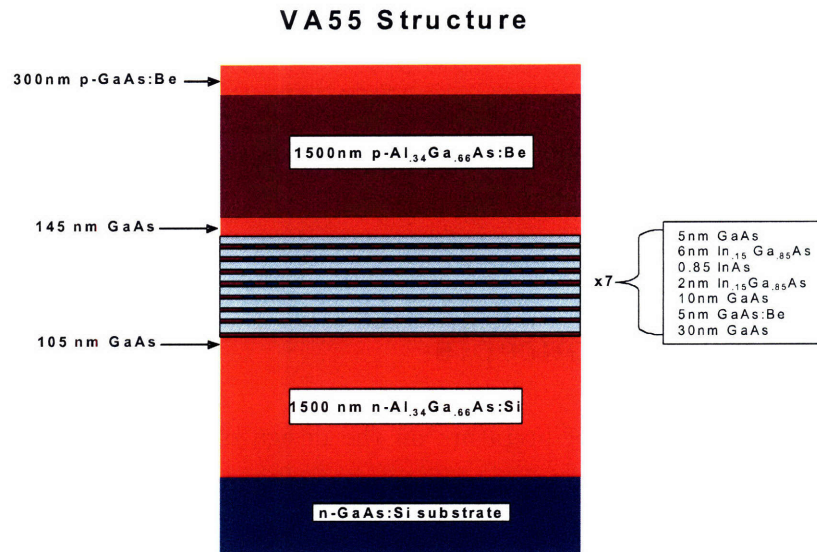
VA55 Structure

Figure 3-1: Structure of VA55 semiconductor laser with epitaxial semiconductor layers and the seven layers of quantum dots as the active region.

The active area of the VA55 epitaxial structure that is shown in Figure 3-1 comprises of seven InAs QD layers each lying within an InGaAs quantum well and are separated by high temperature GaAs spacers. The active region is sandwiched by undoped GaAs inner cladding layers followed by AlGaAs outer cladding layers that are lightly doped with Be and Si for the p-type and n-type regions respectively. Holes are injected into the laser through the top p-type GaAs:Be layer while electrons are injected through the bottom n-type GaAs:Si substrate.

Self-assembled quantum dots reside in the quantum well in what is called the "dots-in-a-well" (DWELL) design [22] in which InAs quantum dots are deposited in an InGaAs quantum well that is in turn placed in a wider band-gap GaAs/AlGaAs matrix. The dots in this device have been p-doped with two holes per dot in order to enhance the gain characteristics as mentioned in the previous chapter. The size

of the QDs determines the energy band-gap and consequently the emission wave-length. Precise emission wavelength tuning is unachievable because the nature of self-assembled growth creates a distribution in the size of the dots thereby leading to a smearing of energy levels and consequently a broadening of the emission spectral width. The photoluminescence spectrum (PL) of the VA55 structures shown in Figure 3-2 exhibits this linewidth broadening about ~880nm, even though the material composition of the QD lasers was designed for 1300nm emission. The PL spectrum is measured by exciting a sample with photons that are at an energy that is above the sample's band-gap energy and then observing the emitted light from the sample. The VA55 sample was excited with 500nm Ar-ion light, whose absorption depth was found to be only $\approx$ 19nm. Thus, it is highly likely that the excitation, and therefore emission, occurs at the contact GaAs layer and not in the QD region because the light is significantly attenuated before it even gets to the dots.
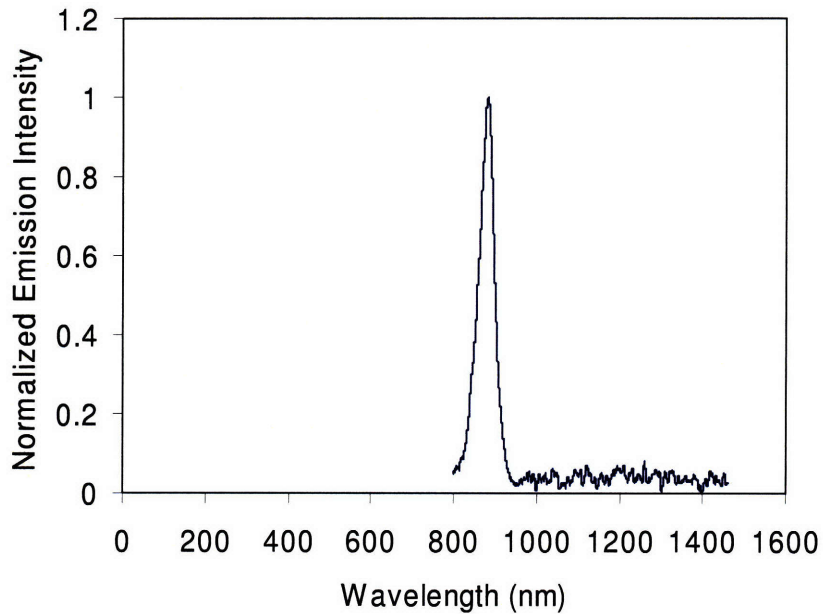
Figure 3-2: Room temperature photoluminescence spectrum for grown VA55 epilayers showing a possible GaAs peak at 880nm.

3.2 Optical Simulations

Commercial design software from Optiwave® was used to simulate the optical modes for ridge depths ranging from $0.1\mu m$ to $1.5\mu m$. Based on the Beam Propagation Method (BPM), the program calculates the propagation of electromagnetic field by computing an effective index of refraction. Since a guided optical mode is centered at the region with the highest refractive index, the highest index region in these devices was designed to be the QD region. Using the cross-section of the heterostructure laser, the transverse (TE) electric field distribution of the guided mode(s) as a function of ridge dimension was calculated. A more comprehensive description of this software can be found at [23].

The index of refraction for most of the materials in the VA55 device was taken from [24] while the code that was used to calculate the index of refraction of the doped outer cladding AlGaAs layers can be found in Appendix A. For simplicity, the indices of refraction are assumed to change negligibly with injection current and temperature. The ridges, as defined by photolithography, range from $1.5\mu m$ to $30\mu m$ in width. For each stripe width, the ridge depth was varied from $0.05\mu m$ to $1.45\mu m$ in order to determine ridge depths that support a single optical mode. According to the simulations, $0.5\mu m$ - $0.55\mu m$ and $0.7\mu m$ - $0.8\mu m$ ridge depth ranges supported the most single modes for most ridge widths. Figure 3-3 shows the results of the simulations for ridges that are $30\mu m$, $15\mu m$ and $1.5\mu m$ wide.

The output facets are formed by cleaving, making use of the semiconductor-to-air reflection coefficient to provide optical feedback. Emission is supported in both axial directions since no reflective coatings were applied.

30 μm ridges
1.4 μm 0.9 μm 0.4 μm

15 μm ridges
1.4 μm 0.9 μm 0.4 μm

1.5 μm ridges
1.4 μm 0.9 μm 0.4 μm
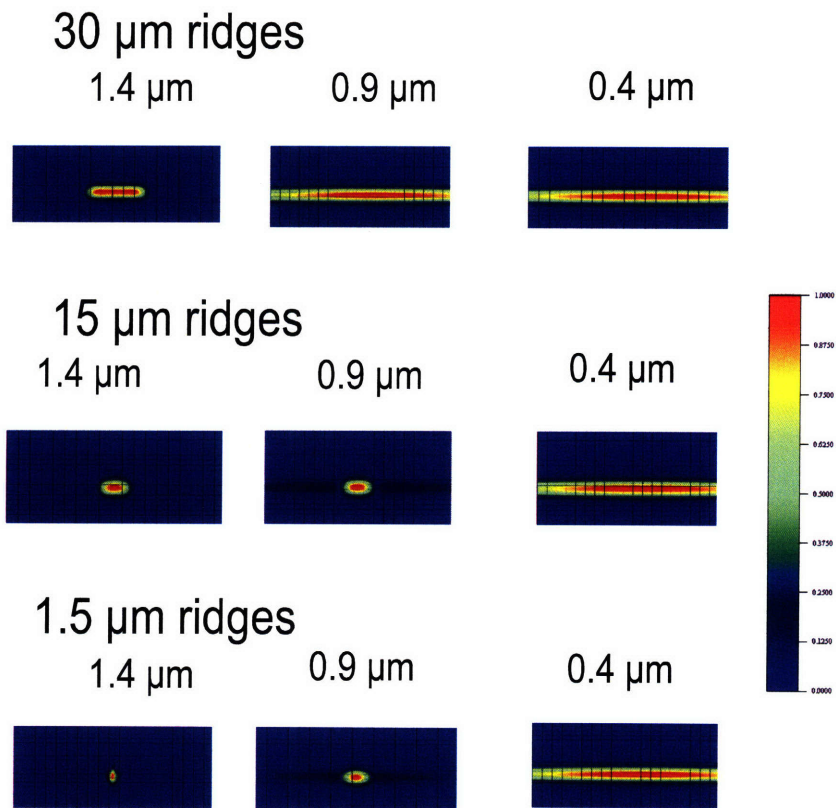
Figure 3-3: Optiwave BPM simulations showing transverse mode confinement for $30\mu m$, $15\mu m$ and $1.5\mu m$-wide ridges at $1.4\mu m$, $0.9\mu m$ and $0.4\mu m$ etch depths. Lateral confinement decreases as the ridges become more shallow.

Chapter 4

Fabrication

4.1 Epitaxial Growth

The fabrication process begins with the epitaxial growth of semiconductor layers by Solid Source Molecular Beam Epitaxy (SSMBE). The MBE growth technique offers excellent control in material composition, doping concentration and layer thickness. MBE allows for the ultra-pure growth of a wide array of III-V semiconductor material systems on single or multiple wafers within a single growth chamber. By epitaxially growing binary, ternary, quaternary and even quintinary semiconductor materials of different bandgaps, the electrical and optoelectronic properties of the lasers can be tailored to meet design specifications.

The basic principle of MBE is that when elements are heated, they evaporate or sublime to form linear molecular beams that diverge in a cone-shaped fashion. The geometry of the growth chamber is such that the beams overlap when they reach the target substrate. The substrate is heated so that upon arrival, the adatoms have sufficient thermal mobility to migrate along the substrate surface until an energetically favourable location to incorporate is found. Ideally, the grown epitaxial layers should be duplicates of the underlying substrate's crystal structure. The quality of the resulting epilayer is analyzed using techniques such as X-ray diffraction in which the x-rays diffracted off atoms in the crystalline structure offer a fingerprint of the structure. The MBE that was used is a Veeco Gen 200 solid-source MBE, whose basic

setup resembles that illustrated in Figure 4-1.
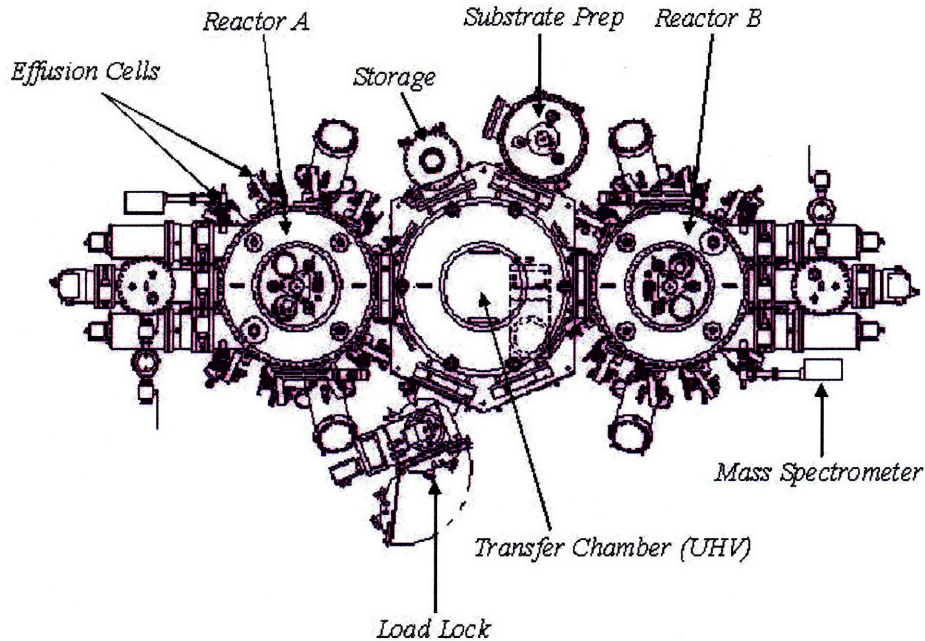
Figure 4-1: A simplified schematic of the Veeco GEN200 MBE chamber that was used for the epitaxial growth in this work.

Material sources, or effusion cells are independently heated and precisely monitored until the desired flux is reached. Fractional changes in temperature can lead to significant flux changes, which in turn cause unwanted variations in growth rate and thus film thickness. Therefore, the effusion cell temperature is closely monitored with highly stable PID (proportional -integral- derivative) controllers, that are based on a control-loop feed back mechanism. Computer-controlled shutters, which open and close in a fraction of a second allow for atomically abrupt transitions from layer to layer. The material sources are extremely pure and the material growth is carried out in an ultra high vacuum (UHV) environment with chamber base pressures ranging from 10^{-10} to 10^{-12} Torr. This high vacuum condition is achieved using standard roughing and UHV pumping configuration. Prior to growth, the substrate is baked at low temperature $\approx 300°C$ under vacuum in order to evaporate any moisture and other compounds that may be present on the surface of the substrate. Following this, a GaAs substrate undergoes another even higher temperature step $> 600°C$ to allow

for the desorption of the native oxide from the surface. However, at this temperature, arsenic preferentially desorbs from the GaAs surface and so an arsenic overpressure is required to prevent the surface from becoming Gallium-rich. Having established an UHV environment and after reaching the desired temperatures for the substrate and effusion cells, epitaxial growth is ready to begin.

4.2   Fabrication Techniques

Semiconductor lasers can be fabricated by a number of standard fabrication techniques, the most enabling of which is photolithography. Photolithography allows for the fabrication and incorporation of multiple lasers on a single wafer and/or chip. The very first step in all photolithographic techniques is to perform a surface clean. A solvent clean, a sequential acetone/methanol/isopropanol rinse followed by drying with nitrogen, is typically performed with III-V semiconductor materials. The solvent clean removes particles and any organic materials, which would adversely affect the pattern transfer.

The clean wafers are then spin-coated with photoresist using a vacuum chuck spin-coater. As photoresist by nature is made of solvents, the next step is a soft-bake, which would evaporate the solvents in the photoresist. The wafer is then exposed to ultraviolet (UV) light through a chrome-patterned quartz mask that is placed in intimate contact with the resist-coated surface of the wafer. The chrome selectively blocks the UV light from reaching the photoresist. During exposure, a photo-activated chemical reaction occurs within the resist that changes the resist's solubility in a particular chemical solution known as the developer, whereby exposed areas may becoming soluble (positive resist) or insoluble (negative resist). During the development, the soluble portions of the resist are washed off leaving behind a replica of the mask pattern on the wafer. The final resist pattern is then used for subsequent patterning of the wafer. The somewhat archaic photolithographic process that has been described above is known as contact lithography and continues to be widely used for academic/research purposes while industry has moved on to use more

complicated tools such as steppers in which instead of making contact to the wafer surface, the mask pattern is projected onto the wafer.

The patterned photoresist may be used as a "soft" mask for the etching of underlying layers. Alternatively, hard masks may be used instead as they are more robust to the etching process. One example of a commonly used hard mask is Silicon dioxide (SiO_2) deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD). In PECVD, reactive gases such as SiH_4, O_2, N_2O are introduced into a vacuum environment in which a plasma is then generated by radio-frequency (RF) electric fields. The ionized gases undergo a series of chemical reactions, eventually forming a film on the surface of the substrate. By controlling the gas chemistries and flows of the various gases, uniform and relatively defect-free films can be grown. The SiO_2 films in this work were deposited using a Surface Technology Systems Multiplex PECVD system.

Following a successful patterning of either "soft" or "hard" masks, the process of etching ridge waveguides into the semiconductor may follow. In some cases, the optical mode is entirely contained within the ridge waveguide. In such a situation, the sidewalls of the ridge must be smooth and vertical, as any deviations would lead to significant scattering of the optical mode. However, if shallow ridges are to be patterned, sidewall smoothness is not critical because the mode may not "feel" much of the roughness as the optical mode is not entirely confined in the ridge waveguide. In such cases a simple wet etch may usually suffice. Wet etches are typically isotropic and do not exhibit great etch uniformity. Due to the isotropic nature of wet etching, small features are typically completely undercut. The larger features also get undercut but remain relatively intact.

In cases where deep, vertical ridges are desired, reactive ion etching (RIE) would make a much better etching option. Similar to PECVD, except that during the RIE process, material is being removed not deposited; a chemically reactive plasma removes material from the substrate. The etching process is both chemical and physical in nature such that the reactive gas atoms (e.g. Chlourine) etch the unmasked areas of the sample and form volatile species, whose removal is enhanced by high-

energy ions bombardment, which remove the atoms from the surface by means of a kinetic energy exchange. The byproducts are then transported away by the vacuum. The high anisotropy, which is a characteristic feature of RIE etch profiles, is achieved by the vertical delivery of the bombarding ions. By changing the parameters such as the gas flows, DC bias voltage and RF power, the etch rates and profiles may be systematically adjusted. At low DC biases and high pressures, chemical etching of the sample dominates while at high DC biases and low pressures, the physical etching dominates. The latter produces more damage but better anisotropy compared to the former.

Finally, active devices require a means of current injection. To facilitate this, ohmic contact pads are incorporated onto the surface of the device. Metallization is typically done by evaporating metal onto the substrate surface. The metal contacts are typically defined by a procedure known as lift-off in which metal is evaporated onto a photoresist patterned surface of a wafer. The photoresist is eventually removed, along with the metal above it, leaving behind areas that have metal on the bare semiconductor surface. A rapid thermal anneal (RTA) may be used to facilitate alloying in the case of multi-layer contacts.

The methods presented above are the most standard techniques used in photonic devices fabrication. The following sections give an in-depth look into the sequence of fabrication steps that were used to produce the QD index-guided lasers in this work. Scanning Electron Micrographs (SEMs) of the control samples as they went through the various fabrication processes are also included.

4.3 Fabrication Overview

The fabrication of QD ridge waveguide lasers may not be as easy as gain-guided stripe lasers, but it is relatively simple compared to non-planar waveguide schemes. For this work, two fabrication routes were taken; a wet etch and a dry etch route, both of which are presented here. As shown in Figures 4-2 and 4-3, the two process flows differ up to the semiconductor etch step, after which the samples go through the

exact same planarization, metal evaporation and backend processing steps. Please refer to Appendix B for a complete summary of the processing recipes.

4.3.1 Wet Etch Process

The wet etch process flow is illustrated in Figure 4-2. The first step in this fabrication sequence is depositing a 100nm film of PEVCD SiO_2. The patterned oxide film will act as a hard mask for the wet etch step. A positive photoresist AZ 5214 is then spun, baked, exposed and developed, transferring the pattern from the quartz mask onto the wafer surface. The resist acts a soft mask during the SiO_2 RIE etch. A fluorine-based RIE step is used to etch through the oxide, transferring the pattern from the photoresist mask into the underlying oxide. The photoresist, having served its purpose is then removed using an organic solvent N-MethylPyrrolidone (NMP) that is heated at about 80°C, followed by a short He/O_2 ashing step to remove any organic residue. The oxide, which now defines the ridges of the lasers, is then used to transfer the pattern to the underlying semiconductor via a $H_2SO_4/H_2O_2/H_2O$ etch, forming approximately 0.5 μm deep ridges of the various widths that were defined by the mask pattern.

Following the ridge formation, a stable planar surface must be formed in order to enable successful patterning of the metal contacts on top of the ridge. This flat surface is commonly referred to as the planarization layer. As the name suggests, a planarization layer serves to planarize the underlying topography for subsequent layer fabrication. For this reason, a planarization layer plays an important role in the fabrication of non-planar structures such as ridge waveguides. Being a dielectric material, the planarization layer is also used for electrical isolation of components that should not be electronically linked. In particular, a p-n junction device requires that the charge carriers uniquely flow through the designated active region. The planarization layer that is used in this work restricted the path of injected charge carriers to the ridge (p-type) through the active region and then to the underlying n-type substrate.

The planarization layer must be mechanically sound so as to withstand subsequent

Wet Etch Process Flow

SIDE

TOP

1. Epitaxial layers grown on GaAs.

2. Plasma Enhanced Chemical Vapor Deposition (PECVD) of 100nm SiO_2.

3. Spin coating of 1500nm of AZ5214 positive photoresist.
4. Contact lithography with OAI aligner.
5. Develop in AZ422 to produce stripes of photoresist.

6. Reactive Ion Etch (RIE) SiO_2 in CF_4.

7. Wet etch GaAs and AlGaAs layers in 1:1:40 H_2SO_4:H_2O_2:H_2O solution at 19 °C.

8. Spin coating BCB 3022-35 polymer
9. RIE BCB in CF_4/O_2.
10. Remove SiO_2 with Buffered HF.

11. Spin and Pattern 1000nm of NR9 negative photoresist with OAI aligner.

12. Electron Beam (e-beam) evaporation of 30/20/200nm of Ti/Pt/Au.

13. Back-side lap and e-beam evaporation of 30/60/30/200nm of Ge/Au/Ni/Au

Key:
- P-type GaAs
- P-type AlGaAs
- GaAs
- DWELL InGaAs/GaAs layer
- N-type AlGaAs
- N-type GaAs substrate
- AZ 5214 photoresist
- PECVD SiO_2 etch mask
- NR9 photoresist
- Top side P-type metal contact
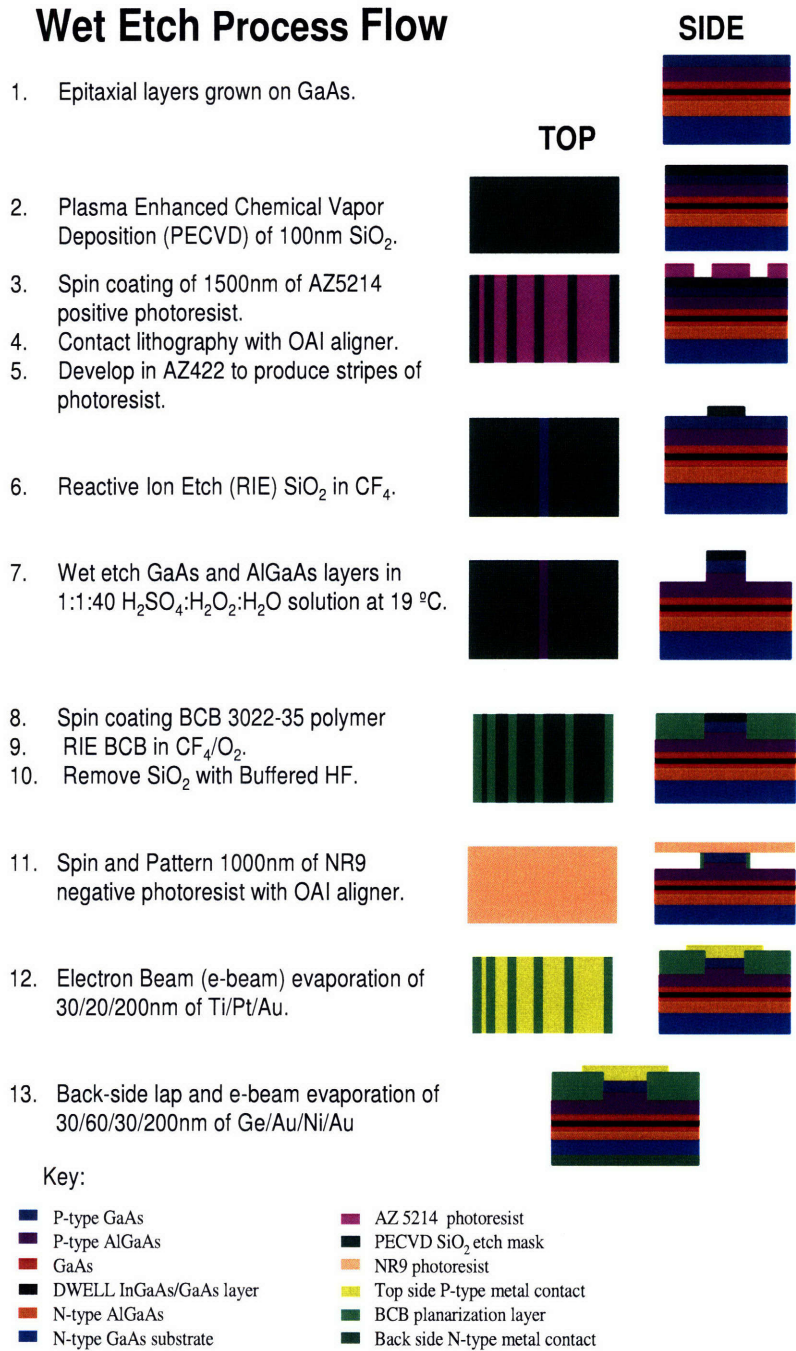- BCB planarization layer
- Back side N-type metal contact

Figure 4-2: Fabrication process using chemical etching of the semiconductor.

processing and packaging. The demonstration of thermal stability so as to endure the significant heating that can occur during characterisation and operation is also critical for a planarization layer.

There are a few commonly used planarization materials such as hydrogen silsesquioxane (HSQ) and benzocyclobutene (BCB), both of which are spin-on insulators. BCB was the resin of choice in this work. Following the spin-on application, the BCB layer undergoes a thermal cure in order to reach full polymerization. The BCB is then uniformly etched back until the top of the ridge is just exposed. The plasma used must be oxygen and fluoride-based since silicon and carbon are at the heart of the BCB polymer. A CF_4/O_2 etch chemistry was used. The oxide mask, also having served its purpose as a mask for the semiconductor etch as well as protecting the ohmic contact of the semiconductor from ion bombardment-induced damage during the BCB RIE etch, must then be removed. A quick Hydroflouric (HF) acid dip removes the oxide, leaving behind ridges of bare semiconductor that are ready for the ohmic contact patterning.

The final step in the front end processing is to deposit 30nm/20nm/200nm of Ti/Pt/Au contact metal. A negative resist NR9-1000PY is carefully patterned whereby the chrome features on the quart mask are well aligned with the underlying ridges onto which the contacts are to be patterned. Following evaporation of the metal contact, a liftoff procedure with RR5 resist remover removes the photoresist along with the superfluous metal.

4.3.2   Reactive Ion Etch (RIE) Process

The dry etch fabrication sequence, as illustrated in Figure 4-3, begins with the deposition of a Ti/Pt/Ni base metal, which would later act as a metal hard mask during the RIE semiconductor etch. Specifically, nickel is used as the hard mask while the Ti/Pt is just part of the p-type metal contact, the rest of which is evaporated at the end of the front-end fabricating process. A negative resist NR9-1000PY is spun, exposed and developed, leaving behind a negative photoresist profile on the wafer. 30nm of Ti, 20nm of Pt and 50 nm of Ni is evaporated onto the resist and following

RIE Etch Process Flow

SIDE

1. Epitaxial layers grown on GaAs.

2. Spin coating of 1000nm of NR9 negative photoresist.
3. Contact lithography with OAI aligner
4. Develop in RD-6 to produce bare stripes embedded in photoresist.

TOP

5. E-beam evaporation of 20nm/20nm/50nm of Ti/Pt/Ni

6. Perform lift-off in RR5 resist remover for 15mins.

7. Reactive Ion Etch (RIE) GaAs and AlGaAs layers in HBr.
8. Remove Ni mask.

9. Spin coating BCB 3022-35 polymer.
10. RIE BCB in CF_4/O_2.

11. Pattern 1000nm of NR9 negative photoresist with OAI aligner.
12. E-Beam evaporation of 30nm/20nm/200nm of Ti/Pt/Au.

13. Back-side lap and e-beam evaporation of 30/60/30/200nm of Ge/Au/Ni/Au
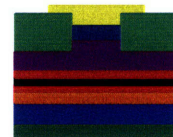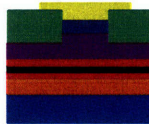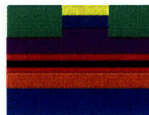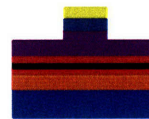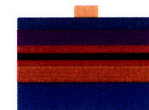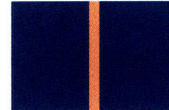
Key:

■ P-type GaAs	■ NR9 photoresist
■ P-type AlGaAs	■ Nickel etch mask
■ GaAs	■ Top side P-type metal contact
■ DWELL InGaAs/GaAs layer	■ BCB planarization layer
■ N-type AlGaAs	■ Back side N-type metal contact
■ N-type GaAs substrate	

Figure 4-3: Fabrication process using reactive-ion etching (RIE) of the semiconductor.

49

liftoff in RD6 resist remover, stripes of metal are left on the wafer surface. The metal hard mask is then used to transfer the pattern into the semiconductor using an HBr etch, forming ridges that are approximately 0.8 μm deep.

Having served its purpose as an etch mask, the nickel is removed using a transene nickel etchant TFG. This etchant is III-V compatible and negligibly etches Ti and Pt, making TFG a good choice for this application.

The same BCB planarization step as in the wet etch process sequence is then performed thereafter. Following the same BCB etch back procedure, the final 200nm of Au in the trilayer Ti/Pt/Au contact is evaporated using the same procedure as the initial metal deposition that is described above.

4.4 Sidewall Roughness-Photoresist

Sidewall roughness of the etch mask is a direct result of the roughness of the patterning resist. Sidewall roughness can easily render a waveguide prohibitively lossy and so sidewall smoothness must be optimized. The resist used for the initial photolithography step in the wet etch process was AZ 5214, a positive resist spun to a thickness of roughly 1.45 μm. This resist was then patterned and that same pattern was transfered to the underlying oxide during the RIE oxide etch. In the dry etch process, NR9-1000PY, an acid-catalyzed negative resist with a thickness of about 1 μm was used to pattern the nickel, which would act as an etch mask for the subsequent semiconductor etch. As stated earlier, the sidewalls must be smooth from the very beginning, as this determines the quality of all subsequent etches.

Optimizing the resist profiles began with adjusting the ultraviolet (UV) exposure dosage. Photoresists require a certain amount of UV exposure energy (typically on the order of mJ/cm^2) in order to activate the photo-active compound (PAC) that is at the heart of pattern formation. Depending on the mode of operation of the UV exposure tool, the exposure dosage can either be changed by adjusting the intensity of the UV lamp, while keeping the exposure time constant (Constant power mode), or by keeping the intensity constant and varying the exposure time (Constant intensity

mode). The exposure tool used in this work operated under neither mode as this tool did not have a Power-Intensity feedback loop. Instead, prior to resist exposure, the UV bulb intensity was measured using a UV meter and the exposure times were then calculated based on the manufacture-recommended resist exposure dosage. The exposure times were adjusted until satisfactory sidewalls were produced.

The optimum exposure time for the positive resist was determined to be 14 sec, corresponding to an exposure dosage of 302 mJ/cm^2, while for the negative resist the optimum exposure time was 47 sec corresponding to a dosage of approximately 1015 mJ/cm^2. Following exposure, the negative resist went through a post exposure bake (PEB), which completed the crosslinking reaction that the UV exposure had initiated. An insufficient PEB led to incomplete crosslinking and therefore huge undercuts of the negative resist as shown in Figure 4-4.
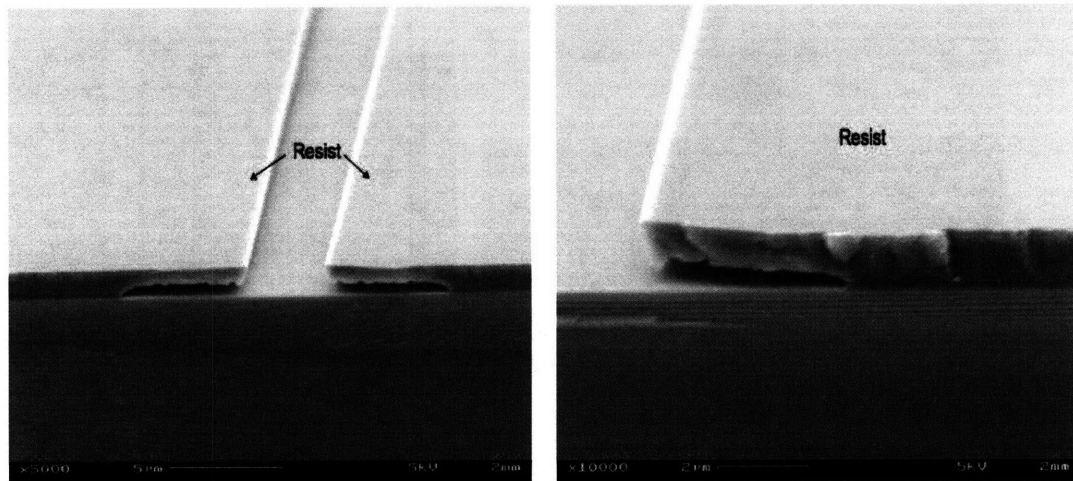
Figure 4-4: SEM micrographs showing a deep undercut of the negative resist caused by insufficient crosslinking.

Resist development is also important, as it is easy to overdevelop the resist, which would also result in a poor resist profile. Smaller features develop first, making it hard to gauge when to stop development so experimentation is necessary in determining the endpoint. The developer that was used with the positive AZ 5214 photoresist was a tetramethylammmonium hydroxide (TMAH)-based metal ion solution. The developer for the NR9 resist, RD6, was also TMAH-based. As a final sidewall im-

provement, the resist may be exposed to a short He/O_2 descum step. During a descum, any residual surface resist as well as the little resist bumps along the resist sidewall, which are areas of slightly increased electric field strength get etched away first, leaving behind a smoother sidewall. The descum step that was used was a 10sec, 5scccm/10sccm He/O_2, 20mTorr, 150W etch. Figures 4-5 and 4-6 show the optimised positive and negative resist profiles. The exposure tool used was the OAI HybraAlign 400 series.
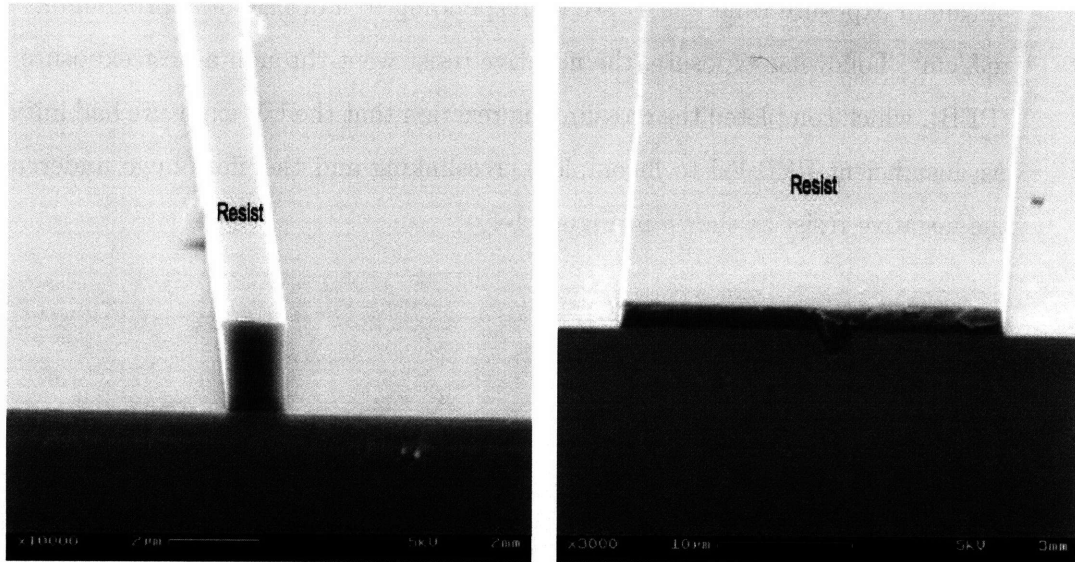
Figure 4-5: SEM micrographs showing smooth sidewalls of the AZ 5214 positive resist sidewalls on a control GaAs wafer. Left and right images show 1μm and 24μm stripes respectively.

4.5   Sidewall Roughness- Oxide RIE Etch

Following positive resist patterning, the pattern is then transferred into the underlying oxide via a fluorine-based etch process. The etch used 15 sccm of CF_4 at 10 mTorr with 148 W of RF power, which yielded an etch rate of about 30nm/min. The CF_4 molecules dissociate into ions, which by virtue of the oscillating RF electric field, continuously bombard the target material, etching it. In addition to the kinetics, the fluorine radicals react with the SiO_2 to form unstable species SiF_4 and O_2, which then
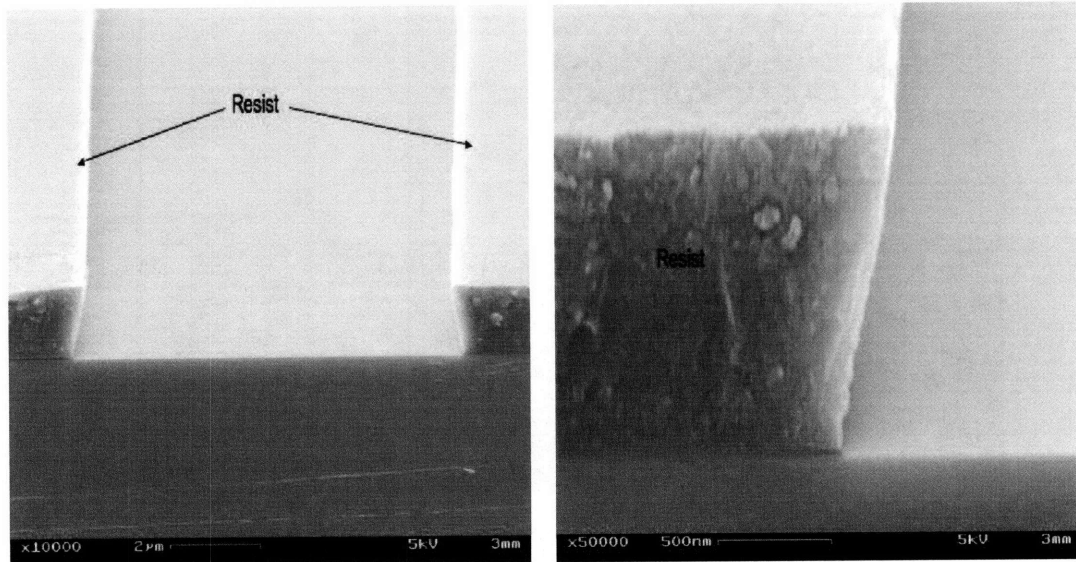
Figure 4-6: SEM micrographs of the NR9 negative resist profile with a slight undercut that facilitates lift-off.

get pumped away by the vacuum. When designing an etch process, the vulnerability of the etch mask to the etch parameters must be kept in mind. For example, high voltage etches may lead to unwanted heating of the resist etch mask, causing residual photo-polymer to outgas and in effect ruin the resist profile. A poor mask profile would then be reflected in a rugged pattern transfer into the oxide. Figure 4-7 illustrates an optimized oxide etch with the resist etch mask still present. The RIE tool used was a Plasmatherm Model 790.

Following a successful oxide patterning, the positive photoresist is stripped by soaking the samples in hot (80°C) N-Methylpyrrolidone (NMP) for a few minutes followed by a short He/O$_2$ descum.

4.6 Sidewall Roughness-Semiconductor Etch

The next step is to transfer the metal/oxide pattern into the semiconductor so as to form the ridges. The ridges should have smooth sidewalls, even though the mode will not actually reside in the ridge. As mentioned before, RIE and wet etches were both carried out and are individually discussed below.
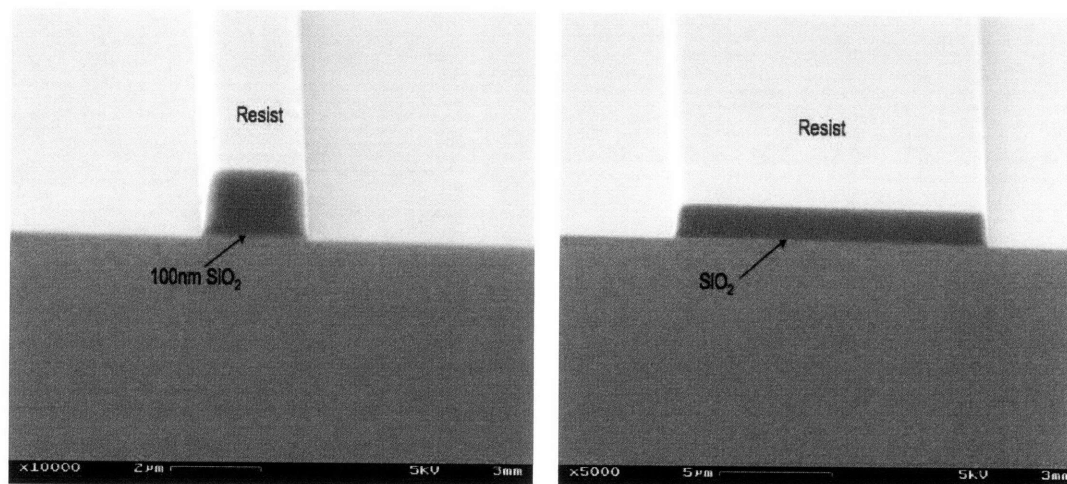
Figure 4-7: SEM micrographs showing smooth, nearly vertical resist sidewalls following a CF_4/O_2 SiO_2 etch. Left and right images show 2μm and 15μm stripes respectively.

4.6.1 RIE Etch

The RIE etch process used a low pressure 2m Torr, 118 W RF power, 20sccm Hydrogen Bromide (HBr) etch. The wafers were kept at a temperature of approximately 75°C to aid the removal of volatile etch species from the sample surface. The GaAs etch rate was found to be approximately 212 nm/min while the $Al_{.34}Ga_{.66}As$ etch rate was approximately 150 nm/min. As dictated by the simulations, 743 nm -deep ridges of GaAs/AlGaAs were formed as shown in Figure 4-8 below. The sidewalls were nearly vertical by virtue of the anisotropical nature of RIE etches. In addition, the nickel etch mask withstood the etch with minimal erosion.

4.6.2 Wet Etch

The basic principle of the chemical etch is the oxidation of the semiconductor surface and then the removal of the soluble reaction product. Most of the solutions that are used for GaAs/AlGaAs etching include hydrogen peroxide, which dissolves the oxidized products that are created by the acid in the solution.

The chemical etch that was used was a solution of H_2SO_4:H_2O_2:H_2O in a 1:1:40 ratio at 19°C giving a GaAs/AlGaAs etch rate of $\approx$15.8 A/sec and 20.44 A/sec
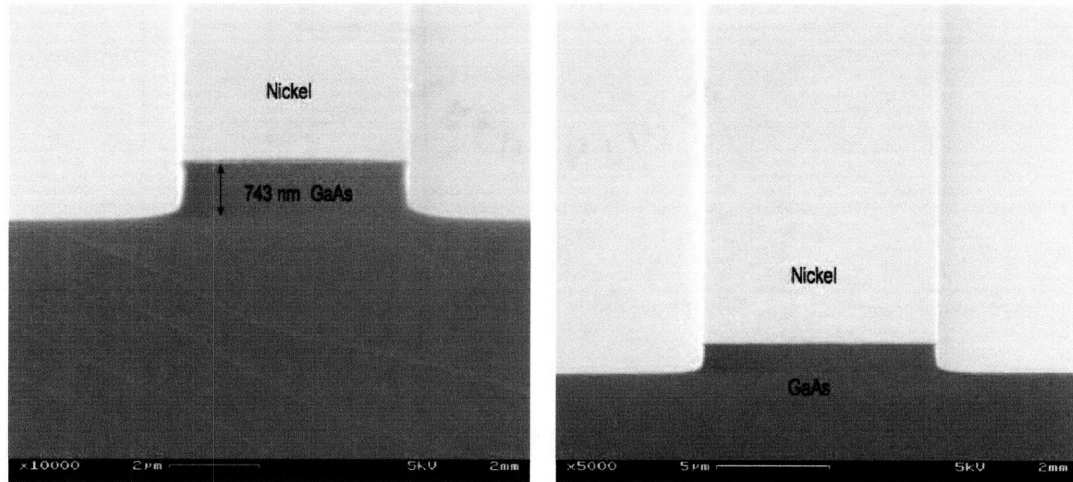
Figure 4-8: SEM micrographs of the GaAs/AlGaAs RIE etch with the nickel etch mask still present. The etch chemistry was 20sccm HBr, 2mTorr discharge with 375V DC bias.

respectively. A reaction-limited etch such as the solution used is generally insensitive to agitation, but exhibits a marked temperature dependence. For this reason, the solution was placed in a water bath to keep the temperature constant and therefore maintain the etch rates.

Initially, a nickel etch mask was used but the etchant attacked the metal, leading to uncontrollable etching of the formerly protected semiconductor top surface. The lesson from using a nickel mask was that metal was a poor etchmask for the chemical etch. Figure 4-9 shows that in some areas, all the metal was etched away, leaving an exposed rugged semiconductor surface.

These poor results motivated the use of an oxide mask instead, which held up well to the acid/base etch mixture. Based on the results from the optcal simulations, the goal was to perform a shallow etch that would 500-550nm semiconductor ridges. The shallow ridges are shown in Figure 4-10. Figure 4-10 also shows that the etch mixture does not attack the oxide mask. The vertical etch depth was right on target at approximately 541nm while the horizontal etch depth due to the isotropy was about 500nm. This undercut of the oxide mask meant that the 1 μm features got completely undercut, as was expected. The bigger features, 2 μm and higher were also undercut, but present.
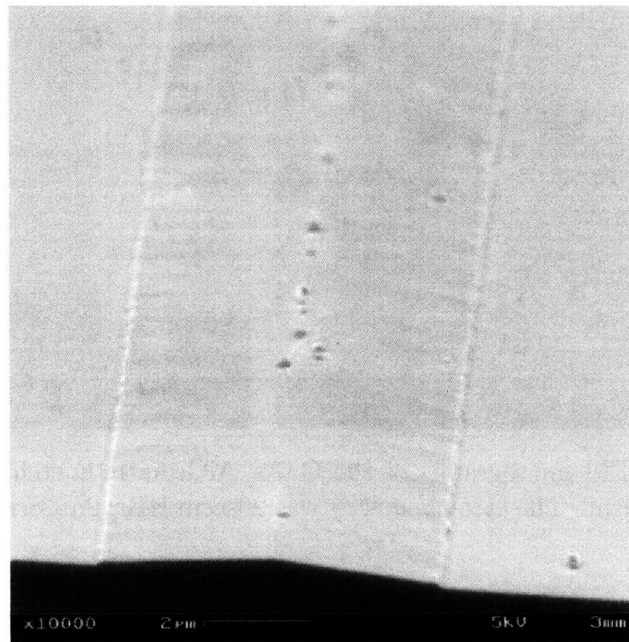
Figure 4-9: SEM micrograph showing that total removal of the nickel etch mask by the 1:1:40 H_2SO_4:H_2O_2:H_2O etching solution.
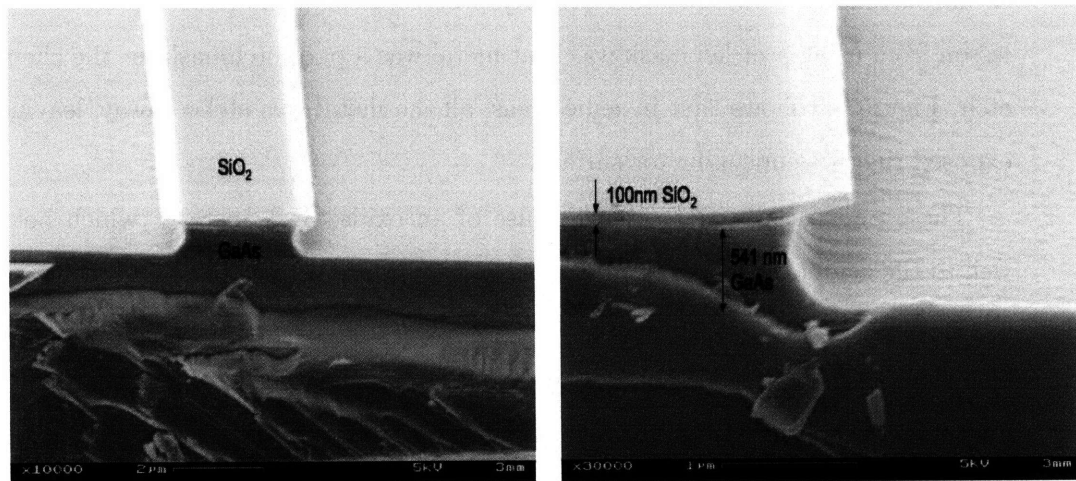
Figure 4-10: SEM micrograph showing an undercutting of the oxide masked GaAs/AlGaAs layers by a 1:1:40 H_2SO_4:H_2O_2:H_2O etching solution. The vertical etch depth of semiconductor is ~541nm.
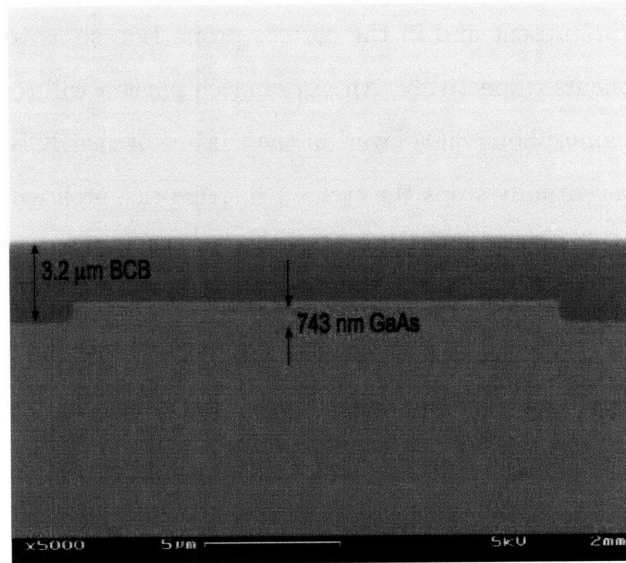
Figure 4-11: SEM micrograph showing BCB (cyclobezene) offering full planarization of etched GaAs/AlGaAs ridge waveguides.

4.7 Planarization

A cyclotene spin-on dielectric derived from bisbenzocyclotene (BCB) monomers, BCB 3000-26, was used as the planarization layer in this work. The characteristic low dielectric constant, low moisture absorption, and negligible out-gassing of BCB during the subsequent dry etch made BCB a good choice.

The wafer is cleaned with a quick solvent rinse and then dehydrated in a convection oven at 130°C for 30 min to drive off moisture, which could impair adhesion. An adhesion promoter AP3000 is then spun on and baked at 100°C. BCB is then spun at 3000rpm to yield a thickness of about 3.2μm. The BCB is then soft-baked on a hot plate at 100°C to evaporate some of the solvent. Finally, the BCB undergoes a full polymerisation via a 60 min 250°C thermal cure in a nitrogen environment. Profilometry measurements of the cured BCB showed negligible variation in surface uniformity even over the deepest 0.8 μm ridges suggesting adequate global planarisation, as illustrated in Figure 4-11.

BCB is composed of silicon and carbon. Therefore, in order to etch BCB, CF_4

and O_2 must be present and in the correct proportion so as to etch the silicon and carbon components respectively. An oxygen-rich plasma will remove the carbon, but will create an amorphous SiO_2 layer on the surface of the BCB, which decreases the etch rate and eventually stops the etch. A flourine-rich etch will etch the silicon, but also forms an amorphous silicon layer, impairing the etch as well. Initially, a plasma containing 15% CF_4 was used to etch back the BCB. However, even after sufficient chamber conditioning, the initial etchback produced a "grassy" surface, which seemed to suggest that the silicon component, which is the harder material to etch, was not being etched fast enough, thus creating unwanted etch masks in the shape of rods for the carbon component. These grassy features are illustrated in Figure 4-12.
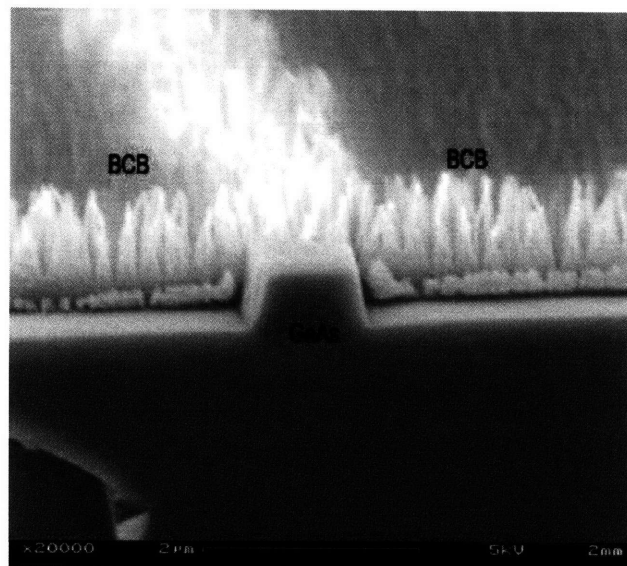
Figure 4-12: SEM micrograph showing that a low concentration of CF_4 caused insufficient etching of the silicon component of BCB. This led to micromasking of the carbon component by the unetched silicon and produced many tiny rods, also known as "grass".

The etch was then modified to a 33% CF_4, 67% O_2 chemistry at 15mTorr and 148W of RF power to etch back the BCB layer until the underlying ridges were just revealed. Even though the BCB etch rate had been calibrated and found to be ≈ 0.1375 μm/min, frequent inspections of the sample under a microscope in between short etches was necessary in order to make sure the end point had been reached,

removing all of the BCB above the ridge. The results of the etch back of BCB revealing underlying Ti/Pt and SiO_2 ridge surfaces are shown in Figures 4-13 and 4-14 respectively.
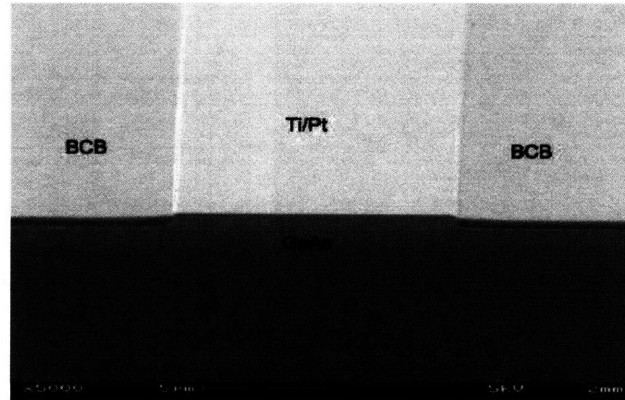
Figure 4-13: BCB etch back using a 33% CF_4, 67% O_2 etch chemistry at a 15 mTorr discharge and a power of 148 W. Following short etches that were accompanied by SEM inspections, the underlying Ti/Pt base metal is revealed.

The oxide was left on top of the ridges so as to protect the top surface of the semiconductor during the BCB etch back, after which the SiO_2 was removed by a quick buffered Hydroflouric (HF) acid dip. The SiO_2 overhang that resulted from the wet etch undercut protected the underlying BCB from being etched, thus creating the BCB step that is seen in Figure 4-14. The HF dip was kept as short as possible because an unnecessarily long etch would have started to attack the aluminium in the AlGaAs layer.

Following planarization, the top Ti/Pt/Au ohmic contacts are patterned using the negative NR9 photoresist. In the case of the samples that went through the RIE etch, the final metallization was preceded by the removal of the Ni etch mask using a Transene nickel etchant-TFG. The remaining Au contact was then evaporated on top the base Ti/Pt layer. Figure 4-15 illustrates a fully front-end-fabricated wafer.

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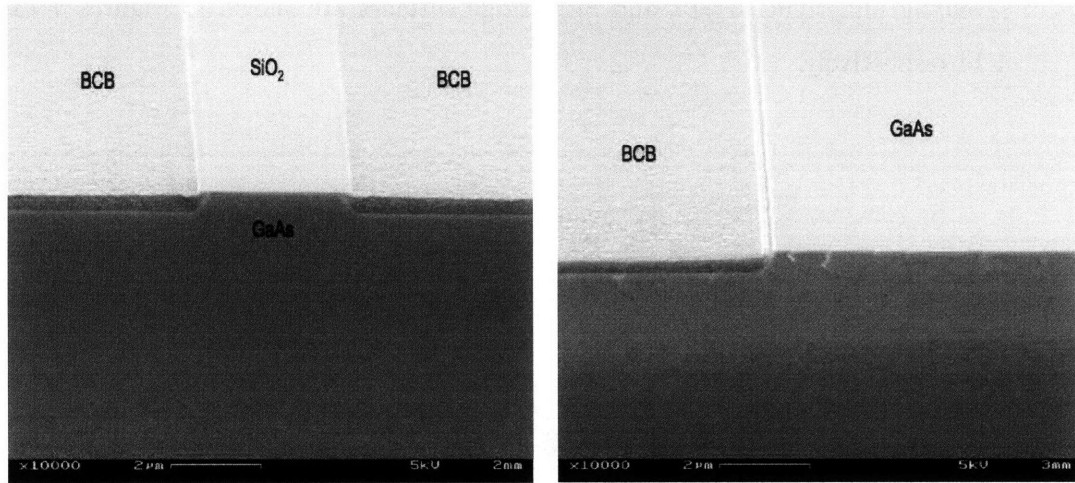
Figure 4-14: Left image shows BCB etch back using a 33% CF_4, 67% O_2 etch chemistry at 15 mTorr and a power of 148 W. Following short etches that were accompanied by SEM inspections, the underlying oxide is revealed. Right image shows the underlying GaAs/AlGaAs ridge after a short buffered HF dip to remove the oxide.
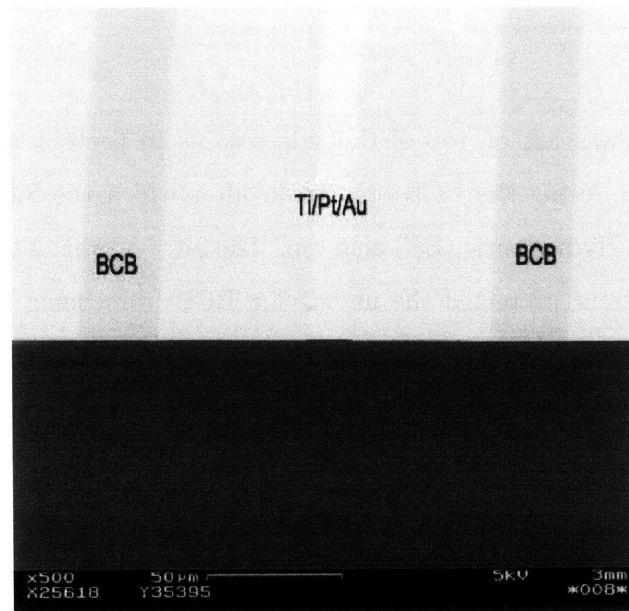
Figure 4-15: SEM micrograph showing the fully-front-end fabricated VA55 sample.

4.8 Back-end Processing

Back-end processing is the very last step in the fabrication sequence. Often regarded as a simple process, back-end processing is critical and can damage or adversely affect device operation if not done correctly. This processing includes wafer thinning, evaporation of back-side metal and then mounting the sample in preparation for characterization. During front-end processing, the wafers have a considerable thickness ($\sim$360 μm) to minimize breaking from tweezer handling and the numerous processing steps that the wafers must undergo. However, when all the front-end processing is complete, there is no longer a use for this excess material. In the particular case of heterojunctions, a thick wafer substrate behaves like a thermal and electrical resistor in series with the p-n diode that is fabricated on top of it. Thus, the wafer must be thinned down to reduce these resistances.

Secondly, thinning a wafer improves the quality of the cleaved surfaces. The thinner the wafer, the easier it is to cleave along the preferential cleave plane, forming mirror-like facets, which provide the feed back in the laser cavity. Figure 4-16 illustrates the improvement of fact quality as a result of lapping.
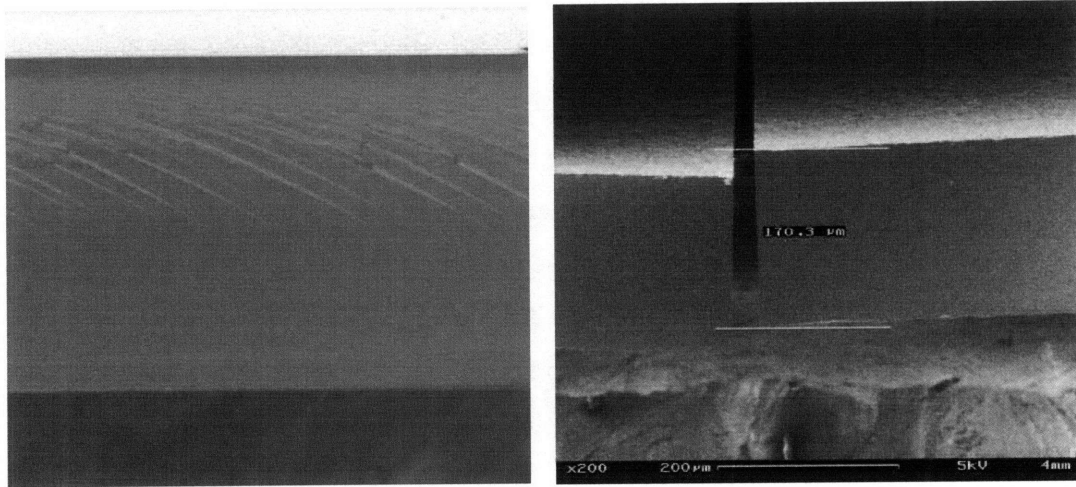
Figure 4-16: SEM micrographs showing cleaved facet quality before lapping (left) and after lapping (right). Before lapping, "scallops" are seen on the facets, which form due to strain during the cleaving process and ultimately lead to optical loss. After lapping to $\sim$ 170 μm, the wafers cleave easier to form smooth mirror-like surfaces.

Wafers were thinned by a combination of lapping and polishing processes. Lapping was done to thin down the wafers from about 360 μm to 150 μm-180 μm. In the lapping procedure, a wafer is mounted, back-end up, onto a stainless steel mounting block using a wax that is soluble in trichloroethylene (TCE). The block and wax are heated above the melting point of the wax (165°C) and the wax is spread out in a thin layer. The substrate is then placed back-end up in the wax puddle, applying pressure to make sure that the front end is sufficiently wetted and that the wafer is sitting as flat as possible. The assembly is allowed to slow cool after which any excess wax is scrapped off the block and the substrate. The samples are then lapped using a South Bay Technology-Model 910 Lapping machine. The mounting block is mounted onto a micrometer-controlled lapping fixture, which allows the operator to set the amount of material that is to be removed.

Material removal begins with a gentle lap using silicon carbide abrasive paper followed by a polish using a 3 μm alumina oxide suspension and a polishing cloth. This step smoothens out the uneven surface that the lapping created. When the desired thickness and polish are reached, the sample and block are rinsed thoroughly in DI water to remove all the material debris. The next step is the coating of Ni/Au/Ge/Au (300/600/300/2000A) n-type ohmic contact by e-beam evaporation. The tool that was used was the Temescal FCE-2500. So as to minimize the handling of fragile lapped wafer pieces, it was only after the final metal evaporation that the samples were dismounted from the mounting blocks. The blocks are heated to melt the wax and the samples are gently removed and allowed to sit in hot (90°C) TCE to remove all the remaining wax from the front-end of the wafer. Finally, the wafers go through a 30 second rapid-thermal anneal (RTA) at 380°C. This RTA step alloys both the top and bottom contacts. Using a sharp scalpel, the devices are then manually cleaved into chips, ready to be mounted for characterization.

Chapter 5

Characterization of Devices

5.1 Device Mounting

In preparation for characterization, the sample must be carefully mounted to a heat sink. During operation, active devices generate significant amounts of heat therefore it is important that there is good thermal contact to the heat sink in order to achieve optimal performance and device longevity. In choosing the materials to use to mount, careful matching of the thermal coefficients of expansion (TCE) between the device substrate and the sample mount is paramount. The mounting scheme that was used in this study uses materials that are TCE-matched to GaAs substrate and is illustrated in Figure 5-1.
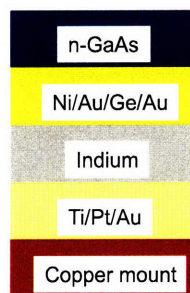

Figure 5-1: Structure of the metals used to solder the GaAs substrate to a copper mount.

The copper mounts were coated with 500nm/700nm/500nm of Ti/Pt/Au, similar

to the back side n-type ohmic contact of the sample. Immediately before mounting, the Ti/Pt/Au face of the copper mount is given a quick clean with a fluorine-based flux to remove any oxide that may have formed between the Ti/Pt/Au evaporation step and the actual mounting. A freshly cleaved sample is then mounted on the copper mount using indium solder. Indium was selected since it has a coefficient of thermal expansion (CTE) that closely matches that of copper. The assembly is gently pressed down using a fine probe tip so as not to damage the metal stripes. After the mounted sample has cooled, the mount is placed on a gold-coated thermo-electric (TE) cooler, ready for testing.

5.2   Testing Scheme

5.2.1   Electrical Testing Design

Previously fabricated quantum well devices and the quantum dot devices that have been fabricated in this work were tested under Continuous Wave (CW) operation as well as pulsed operation. In the CW mode of operation, the laser output is relatively constant with respect to time and population inversion is achieved by a steady injection of current from the laser driver. Current is fed to the stripes through a probe and an optical multimeter measures the output optical power. The optical multimeter is a broad-area detector, which measures the optical power with an InGaAs photodetector. The InGaAs photodetector in sensitive up to 1600nm, well above the 1300nm emission wavelength of the QD lasers. The CW driver that was used had a compliance voltage of 7V and a maximum input current of 500mA. Figure 5-2 is a block diagram of the CW setup.

For currents above 500mA, the pulsed driver had to be used instead. In the pulsed mode, the output of the laser varies with respect to time in an on-off manner in the form of a square wave on an oscilloscope. An InGaAs photodiode linked to a lock-in amplifier was the detector of choice for pulsed operation measurements instead of the optical multimeter that was used in CW mode. This was because the multimeter was

Using an optical spectrum analyzer (OSA) the electroluminescence spectrum can be observed. However, due to the low power from the fabricated lasers and the significant loss of that little power through the measurement optics, no emission peaks were observed.

The first attempt at free space coupling of the output light from the devices to a large core multi-mode fiber (MMF) failed, as there was significant insertion losses. Thus, the setup was upgraded to include a collimating aspheric lens and a focusing objective lens. This two-lens system (Figure 5-4) was supposed to collimate the slightly divergent laser beam with the aspheric lens and then focus it down to a fine point with the objective lens so as to couple into the fiber.
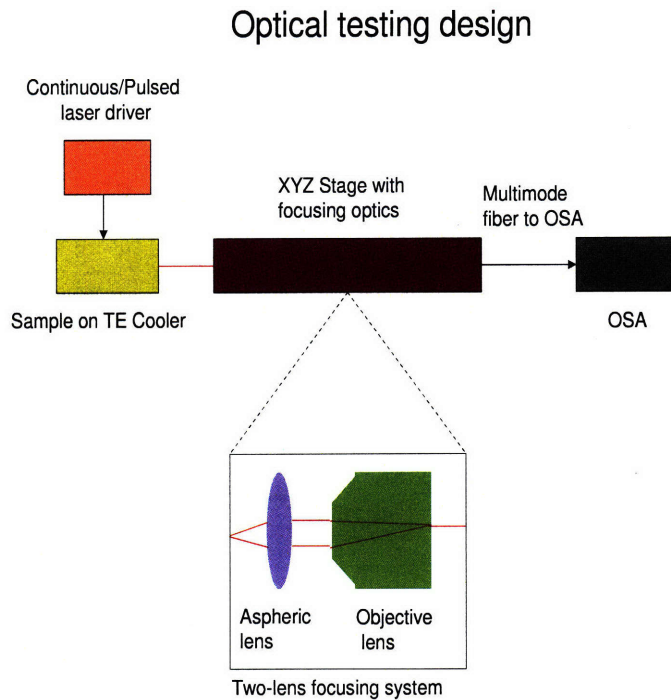
Figure 5-4: A block schematic of the optical testing design. The two-lens system first collimates and then focuses the output signal onto the fiber tip. A multimode fiber with a 60 μm core was used.

A precision translation stage is used to move the lens, fiber, and device with respect
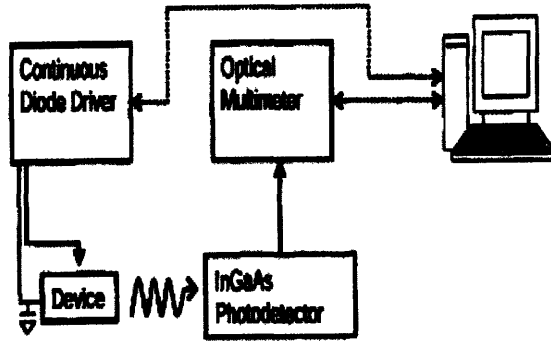
Figure 5-2: Schematic of the continuous wave (CW) operation using an InGaAs detector.

unable to resolve the 10% duty cycle signal from the devices. The pulsed driver had a compliance voltage of 10V and a maximum current of 1000mA. The basic setup of pulsed operation is depicted in Figure 5-3.
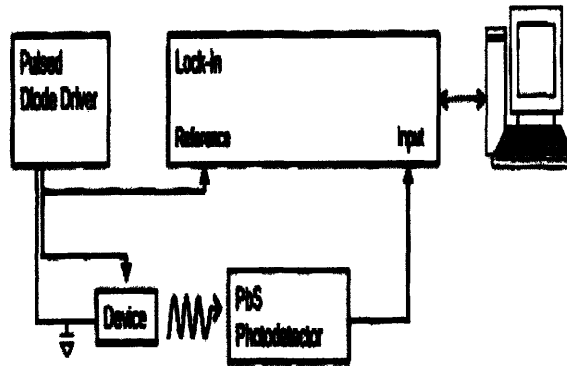
Figure 5-3: Schematic of the pulsed operation using an InGaAs photodiode. The purpose of the photodiode was to provide a DC signal, which would then be amplified by the lock-in amplifer.

5.2.2 Optical Testing Design

In addition to investigating the Light-Current (L-I) and Current-Voltage (I-V) characteristics of these devices, the optical spectrum of the lasers was also of interest.

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to each other in order to allow optimal coupling efficiency. To facilitate the optical alignment process, commercial high power laser chips in the mW range from Axcel Photonics were used. An emission peak from these commercial lasers was observed on the OSA but unfortunately no peaks were observed from lasers that were fabricated in this work.

5.3   Characterization Results

Lasing was observed from the VA36 quantum well (QW) samples only under pulsed operation. This was because the bias voltage across the lasers reached the 7V compliance voltage of the CW driver before the threshold condition had been met. Therefore, the pulsed driver with a higher compliance voltage had to be used. Figure 5-5 shows room temperature (Light-current) LI characteristics of as-cleaved 4mm-long quantum well lasers of widths ranging from 4-30 μm.

There was no noticeable relationship between output power and cavity width. As was shown by the simulations in Section 3.2, but not in the results presented here, increasing the cavity width causes the optical mode to broaden in the lateral direction. However, the total detected output intensity remained the same because the broad area of detection of the detector. Even though the optical modes were less laterally confined in the wider laser cavities, the total output power was still collected by the detector.

Room temperature CW lasing from the VA55 QD sample was also achieved. Figure 5-6 shows the room temperature LI characteristics from as cleaved 4mm-long lasers of widths ranging from 1-30 μm. As with the QW lasers, there was no observable relationship between cavity width and output power or voltage. However, the threshold condition was met at lower currents and bias voltages in the QD lasers compared to the QW lasers. This is in agreement with the superior opto-electronic performance that is expected from QD lasers compared to the QW lasers.

Of particular interest was the temperature dependence of the threshold current. Thermal coupling to higher energy levels for the QD lasers can have a significant

Figure 5-5: Light versus current room temperature characteristics of VA36 2-QW lasers of lateral cavity widths ranging from 4-30 μm. 4mm-long as cleaved lasers operating under pulsed operation at 10% duty cycle.

impact on the temperature dependence of the threshold current. In particular, as expected from the discussion in Section 2.4.2, the threshold current should increase as temperature increases. Given a large increase in temperature, the lasers can effectively be turned off if the threshold current is no longer reached. Saturation is also expected to occur at lower currents. This temperature behavior would be caused by the thermo-enabled current leakage across the junction as well as Auger or non-radiative recombination.

The L-I characteristics of the QW and QD lasers were investigated at the temperatures ranging from 15°C to 58°C, the highest temperature possible for the chracterization system. This was a very small temperature range. In order to obtain a good understanding of the L-I temperature characteristics of lasers, the temperature
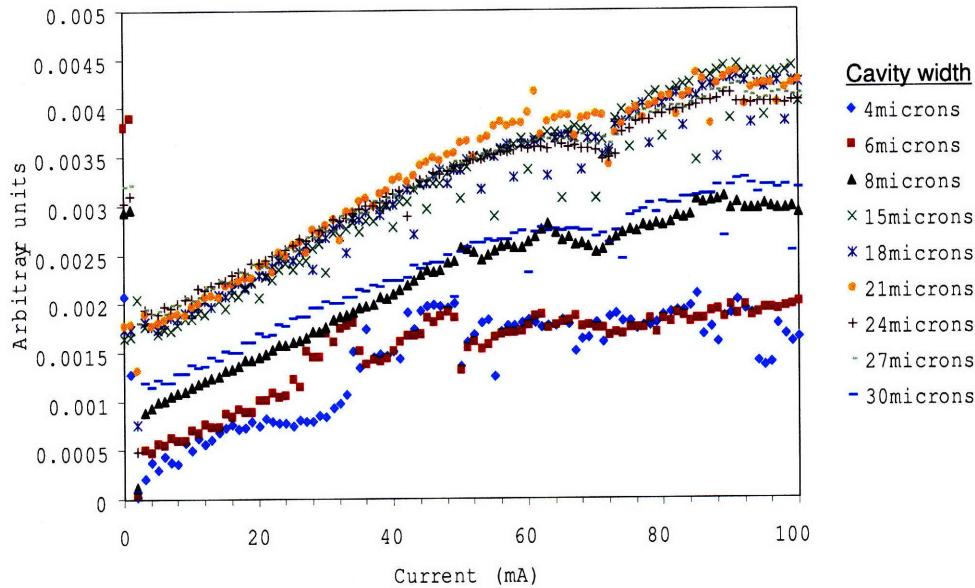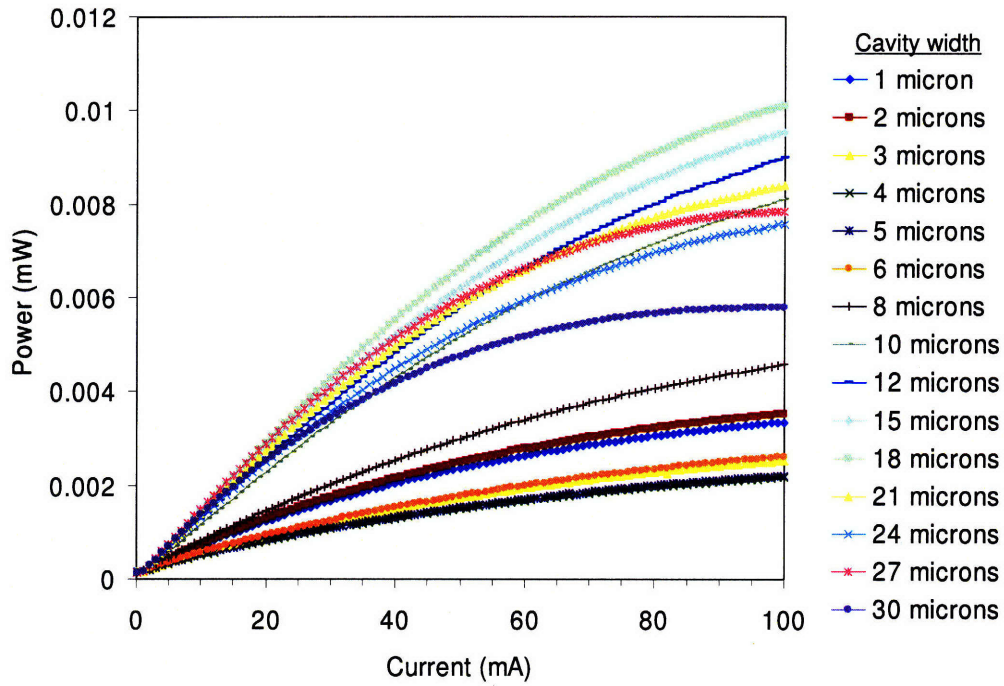
Figure 5-6: Light versus current room temperature characteristics of VA55 7-stack QD lasers of lateral cavity widths ranging from 1-30 μm. 4mm-long as cleaved lasers operating under CW operation.

range should stretch from cryogenic temperatures to temperatures above 60°C. Unfortunately, the measuring system used in this work does not have that capability at this time. The L-I temperature dependence was investigated none-the-less and the characteristics from the VA36 and VA55 lasers are shown in Figures 5-7 and 5-8 respectively.

The V-I plots in Figures 5-7 and 5-9 show no dependence of threshold current on temperature for both QW and QD lasers as was expected from the limited temperature range used in these measurements. However, Figure 5-8, which shows the L-I characteristics of the VA55 lasers showed a dependence of output power on temperature. As is shown in the figure, the output power had a marked inverse relationship with temperature. This L-I temperature dependence can be explained by the in-

Figure 5-7: Temperature dependence of the LI characteristics of the VA 36 30 μm-wide QW lasers. 4mm-long as cleaved lasers operating under 10% duty cycle pulsed operation at temperatures ranging from 15°C to 53°C.

creased Auger recombination, inwhich the energy released during the electron-hole recombination is given up to an electron, instead of being released in the form of a photon. In addition, the thermally energized carriers may also be leaking into the quantum well where they may or may not radiatively recombine because the energy band-gap is larger in the quantum well than in the quantum dots.

Finally, the relationship between the output power and cavity length was investigated. This was done by varying the lengths of three stripe widths and examining the L-I, V-I behaviour as the cavity length was changed. These measurements were all carried out at room temperature under pulsed and CW operation for the VA36 and VA55 samples respectively. VA36 samples were cleaved at 1mm, 2mm and 4mm while the VA55 samples were cleaved longer at 4mm, 5 mm and 8mm. The expectation

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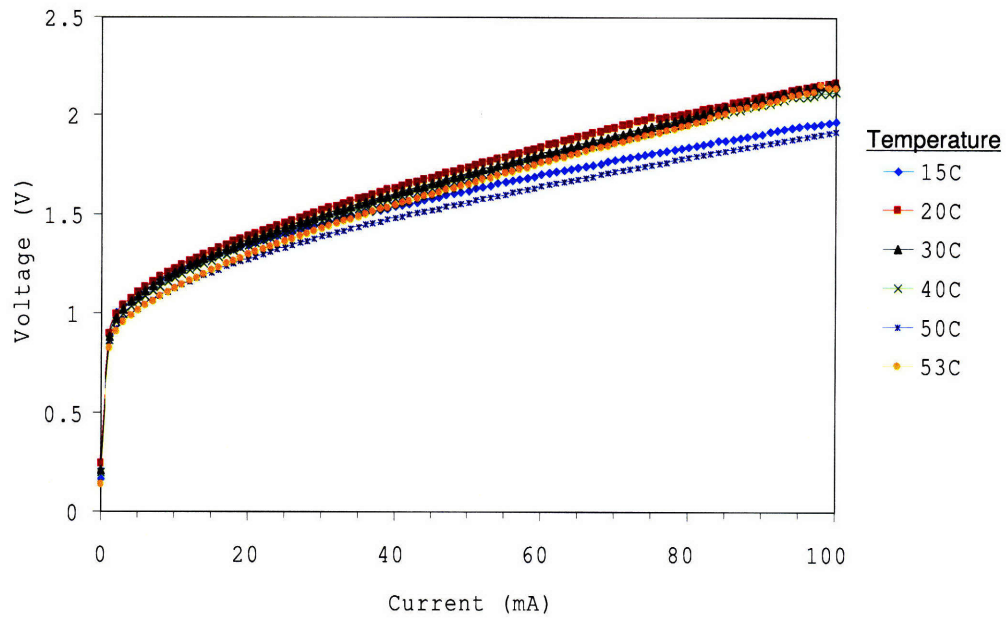
Figure 5-8: Temperature dependence of the VI characteristics of the VA55 30 μm-wide QD lasers. 4mm-long as cleaved lasers operating under CW operation at temperatures ranging from 15°C to 58°C. An inverse relationship between temperature and bas voltage across the lasers is observed.

was that given a fixed facet loss (minimized due to lapping), creating longer cavities would not only increase the modal gain, but would also provide more material to heat sink the device. Lasing would therefore be maintained and the overall external quantum efficiency would be augmented. However, the results shown in Figures 5-10 and 5-11 show no dependence of output power on the chosen cavity lengths.
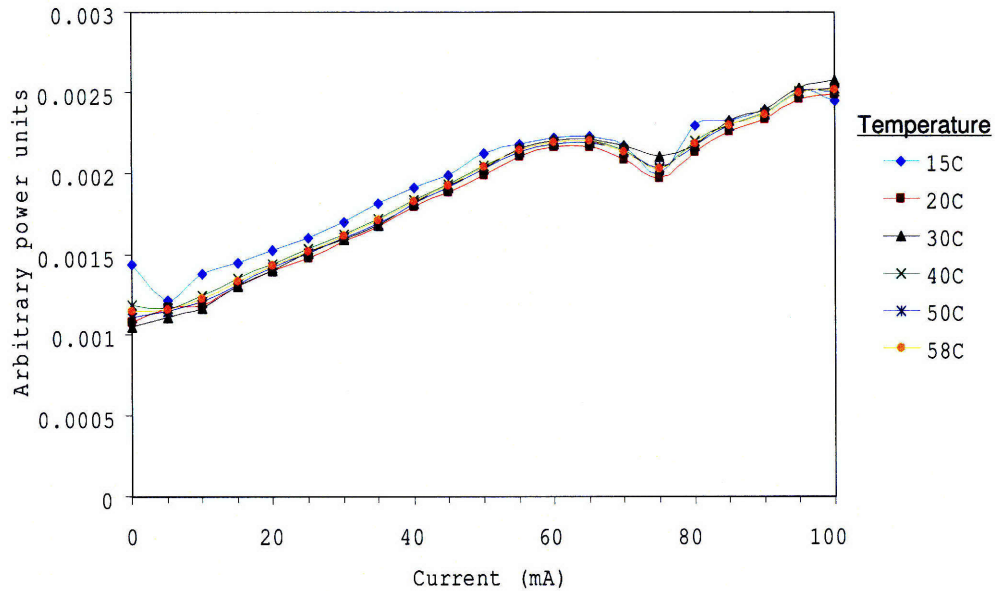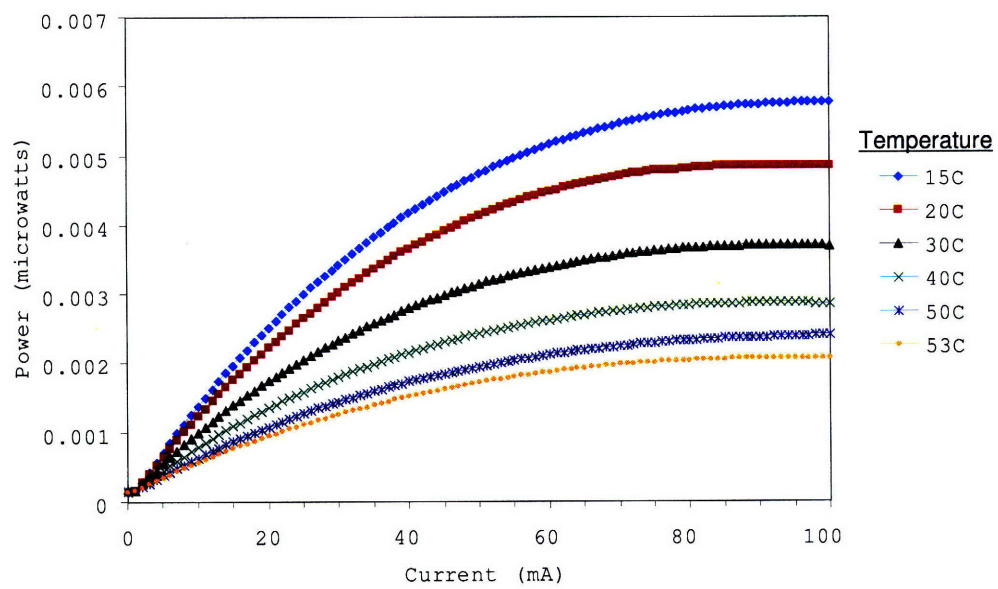
Figure 5-9: Temperature dependence of the LI characteristics of the VA55 30 μm-wide QD lasers. 4mm-long as cleaved lasers operating under CW operation at temperatures ranging from 15°C to 58°C.
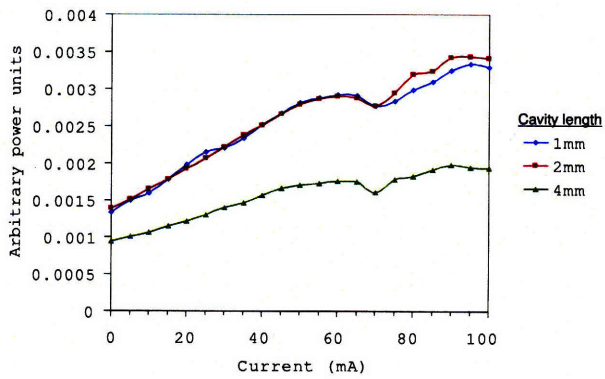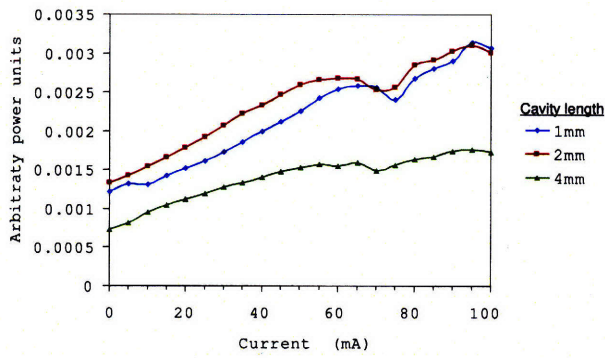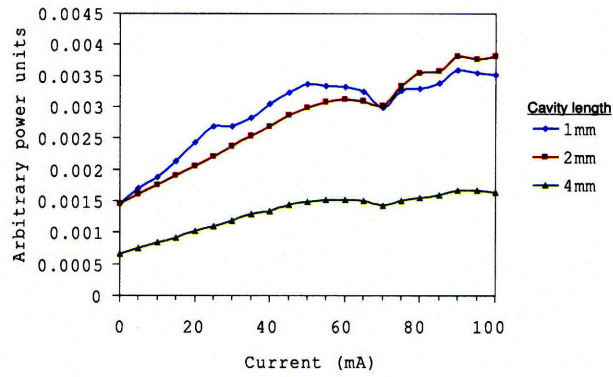
Figure 5-10: LI dependence on cavity length of the VA 36 QW lasers. 6 μm (top), 15 μm (middle) and 30 μm-wide (bottom) cavities each at 1mm, 2mm and 4mm length. As-cleaved lasers operating under 10% duty cycle pulsed operation at room temperature.
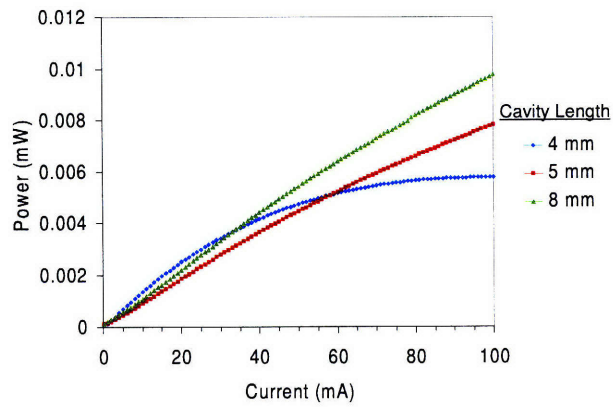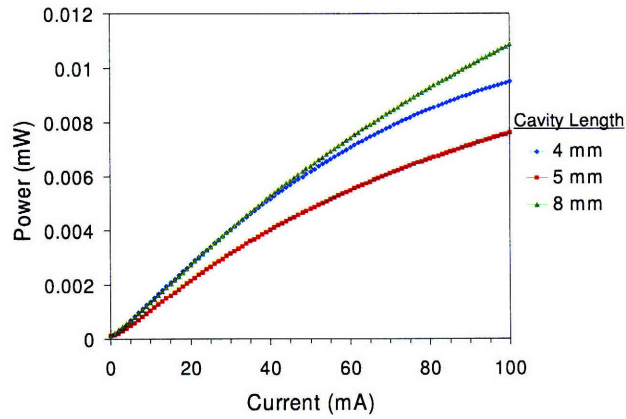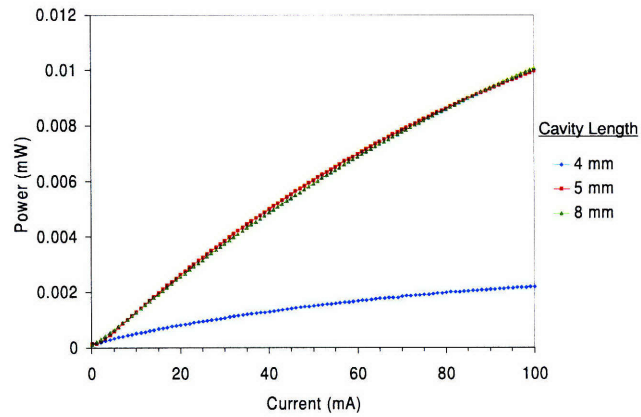
Figure 5-11: LI dependence on cavity length of the VA 55 QD lasers. 5 μm (top), 15 μm (middle) and 30 μm-wide (bottom) cavities each at 4mm, 5mm and 8mm length. As-cleaved lasers operating under CW operation at room temperature.

Chapter 6

Conclusion

The work presented in this thesis included the design, fabrication and characterization of quantum dot heterostructure ridge lasers. The transverse optical mode profiles for the ridge waveguides were simulated during the design process. Two different fabrication processes; wet etching and RIE were designed and implemented. The QD lasers were fabricated, and the fabrication methods and tools were analyzed, optimized and the end results were compared. Characterization of the QD lasers showed electrical and optical performance that was superior to the QW lasers that were also fabricated and characterized.

6.1 Applications and future work

In Chapter 5, the output power of the QD lasers was shown to be on the order of microwatts. This small output power, in conjunction with insertion loss associated with the quality of the alignment of the lens system and the fiber tip made it difficult to couple the output light from the device into a fiber so as to measure the electroluminescence spectrum. Without the EL spectrum the wavelength of the emission peak of these lasers remains unknown. The EL spectrum would have confirmed the wavelength of ground-state emission at the QDs. Therefore, the output optics remain to be improved in order to makespectral measurements. In addition, there is room for improvement as far as the laser structure. A revision of the structure may be

performed in order to increase the power from the lasers.

The short-term goal of this project is to incorporate the well-understood QD active region in the microcavity photonic crystal lasers (Figure 6-1).
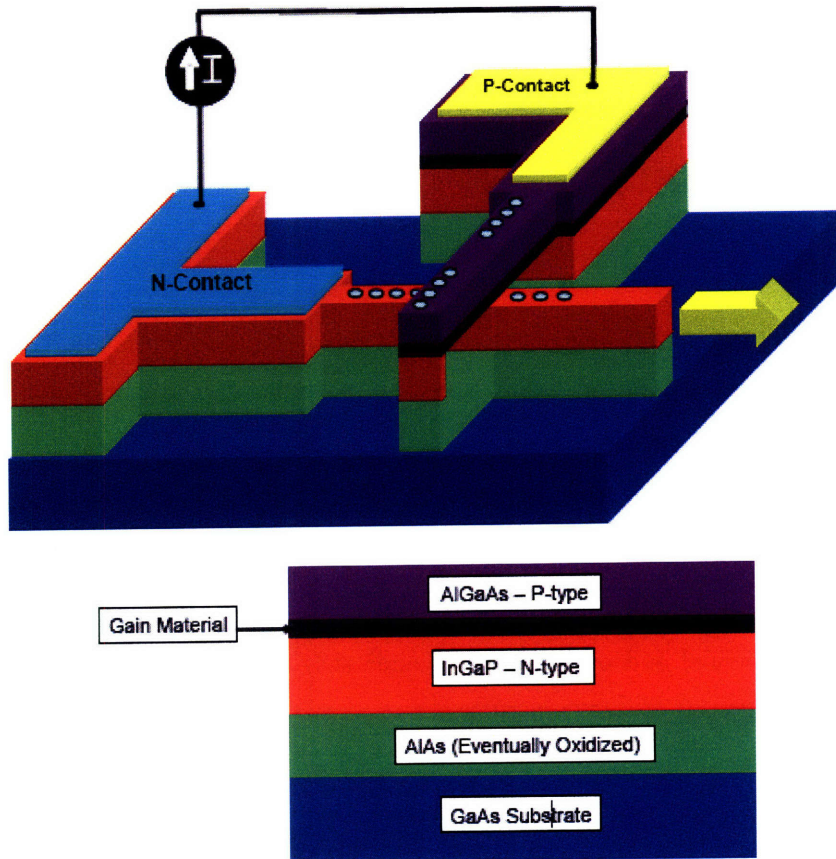
Figure 6-1: Schematic of Photonic Crystal laser and epilayers

The laser in Figure 6-1 is well suited for integrated optics for several reasons, which include in-plane emission and electrical activation. This laser conserves chip-real estate and would couple directly into an output waveguide. Most of the fabrication and characterization techniques developed in this work could also be applied to the processing and testing of these lasers.

Appendix A

Index of Refraction for Al_xGa_{1-x}.

% Function calculates the refractive index of Al_xGa_{1-x}. User inputs x and the wavelength in meters. All formulae was taken from [25].

$h = 6.63e - 34$; % Planks constant

$h_{bar} = h/(2 * pi)$;

$c = 3e + 8$; % speed of light

$c_{cm} = 3e10$; % Speed of light in centimeters

$h_{cm} = 4.14e - 12$; % Plank constant in microelectronic units;(charge of an electron)

$hbar_{cm} = h_{cm}/(2 * pi)$;

$mo = 9.11e - 31$; % mass electron in mks units

$mo_{cm} = 5.69e - 16$; % mass of electron in microelectronic units

$me_{GaAs} = .067 * mo$; % mass of electron in GaAs QWELL

$mh_{GaAs} = .34 * mo$; % mass of hole in GaAs QWELL

$me_{AlGaAs} = .091 * mo$; % mass of electron in AlGaAs barrier

$mh_{AlGaAs} = .38 * mo$; % mass of hole in AlGaAs barrier

$Eg_{AlGaAs} = 1.6734$; % Bandgap for AlGaAs

$kt = .0259$; % Thermal voltage in eV

$Nc = 2.74e + 18$;

$Nv = 1.0477e + 19$; % Density of states for AlGaAs

$epsilon0 = 8.85e - 12$; % Value in meters

$epsilonGaAs = 13 * epsilon0$; % The permittivity of GaAs

$q = 1.6e - 19;$ % Charge of electron

****

$lambda = 1.25e - 6;$ % INPUT WAVELENGTH IN METERS

****

$w = c * 2 * pi/lambda;$

$Ep = h * c/(q * lambda);$ % Photon energy in eV

****

$x = .34;$ % INPUT PROPORTION OF ALUMINUM

****

$Eg = 1.424 + 1.266 * x + .26 * (x)^2;$ % Bandgap of AlGaAs in eV

$delta = .34 - .5 * x;$

$A = 6.64 + 16.92 * x;$

$B = 9.2 - 9.22 * x;$

$yso = Ep/(Eg + delta);$

$y = Ep/Eg;$

$fy = 1/y^2 * (2 - (1 + y)^{.5} - (1 - y)^{.5});$

$fyso = 1/yso^2 * (2 - (1 + yso)^{.5} - (1 - yso)^{.5});$

$EpsilonFactor = (A * (fy + .5 * (Eg/(Eg + delta))^{(1.5)} * fyso)) + B;$

$n_AlGaAs = EpsilonFactor^{.5}$

$Energy = h * c/(q * lambda)$

$3.51 * .85/(8 + .85) + 3.45 * 8/(8 + .85)$

Appendix B

Fabrication Recipes

Times in (min:sec) format

B.1 Wet Process

Oxide Deposition: PECVD SiO_2 is deposited for later use as a hard mask.

1. Clean samples: Acetone/Methanol/Isopropanol/N_2 Dry

2. Deposit 100nm, PECVD SiO_2

   13.56 MHz, 550mTorr, 300°C platen, 250°C shower head, 30W, N_2O 1420 sccm,

   N_2 392 sccm, SiH_4 12 sccm

3. Clean samples: Acetone/ Methanol/ Isopropanol/N_2 Dry

Photolithography: Patterning the photoresist soft mask.

1. Solvent clean, dehydrake bake on hot plate at 100°C

2. HMDS Primer: Spin for 36sec, 4000 rpm

3. Spin resist: AZ 5214-positive resist

   Dispense: static

   Spread: 6 sec, 750 rpm

   Spin: 36 sec, 4000 rpm

4. Bake: 95°C, 35min in a convection oven

5. Contact Aligner- OAI HybraAlign 400 Series (MASK 1-narrow stripes) Expose 14.4 sec

6. Develop: AZ 422; 90 sec with gentle swirl

Oxide Reactive Ion Etch: Transfers the phtoresist pattern to the underlying oxide to form a hard mask.

1. Clean chamber: CF_4 4 sccm, O_2 20 sccm, 20m Torr, 300V

2. Descum: He 5 sccm, O_2 10 sccm, 20 mTorr, 150 W, 5 min

3. Oxide etch in Plasmatherm 790 RIE: CF_4 15 sccm, 10 mTorr, 50W
   Total time = 4:03 @ 30nm/min

4. Remove resist: Soak in 80°C N-MethylPyrrolidinone (NMP) for 15 mins
   Ash: He/O_2 200W, 0.350 mTorr for 2 mins

GaAs/AlGaAs Wet Etch: Etch stripes into the semiconductor.

1. Make 1:1:40 H_2SO_4:H_2O_2:H_2O etch solution and place it in a water bath.

2. Etch semiconductor in solution at 19°C for $\approx$ 6:42

3. Rinse thoroughly in DI water and N_2 dry

Planarization: Planarize the front-side ridged topography.

1. Solvent clean, dehydrake bake in oven at 130°C, 30 min

2. Adhesion Layer AP3000
   Dispense: static
   Spread: 300 rpm, 5 sec
   Spin: 2-3K rpm, 20 sec

3. Hot plate bake at 100°C, 5 mins

4. Planarization Layer BCB 3022-46

   Dispense: static

   Spread: 500-750 rpm, 5 sec

   Spin: 3000 rpm, 25 sec

5. Hot plate bake at 100°C, 1 min

6. BCB thermal cure: Anneal furnace

   Load wafer, flow N_2 (> 20scfh) for 30 mins

   Slowly ramp up to 250°C, set N_2 flow to $\approx$ 5 scfh

   Anneal at 250°C for 60 mins

   Ramp down to room temperature, flow N_2 (> 20scfh) for 60 mins

BCB Etchback: Etch back planarization layer to reveal ridges.

1. Clean chamber: CF_4 4 sccm, O_2 20 sccm, 20m Torr, 300V

2. Condition chamber: CF_4 6.60 sccm, O_2 13.4 sccm, 15m Torr, 150W, 16mins

3. Etch BCB in Plasmatherm 790 RIE

   CF_4 6.60 sccm, O_2 13.4 sccm, 15m Torr, 150W, Total time = 21:44 at 0.1375 μm/min

Oxide Etch: Remove oxide hard mask.

1. Buffered Oxide Etch (BOE)

   57A/sec at 19°C for 21 sec.

Photolithography: Negative resist pattern defines the metal coontact pads for liftoff.

1. Solvent clean, dehydrake bake on hot plate at 150°C, 1 min

2. Spin resist: NR9-1000PY-negative resist

   Dispense: static

   Spin: 3000rpm, 40sec

3. Hot plate bake: 150°C, 1 min

4. Contact Aligner- OAI HybraAlign 400 Series (MASK 3-wide stripes) Expose 14.4 sec

5. Post-Exposure Bake (PEB): 105°C, 1 min

6. Develop: RD6; 12 sec with a gentle swirl

Metal Deposition and Liftoff: Ti/Pt/Au is evaporated for the top p-type ohmic contact.

1. Electron beam evaporation using the Temescal FCE-2500
   Evaporate 30/20/200nm of Ti/Pt/Au

2. Liftoff at room temperature in resist remover RR5, 15 mins, gently swirling

3. Solvent rinse to remove excess resist, N_2 dry

Backside Processing: Thinnng the wafer and backside metal evaporation.

1. Lap backside of the wafer
   Mount sample on stainless steel chuck using LogiTech bonding wax
   Remove all the excess wax with (Tricholoroethylene) TCE and isopropanol.
   Lap wafer using South Bay Technology 910 Grinder/Polisher to a final thickness of$\approx$ 160μm with 600-grit silicon carbide film
   Polish wafer backside with a rayon-fine polishing cloth and 1μm alumina suspension
   Rinse sample thoroughly with DI water

2. Electron beam evaporation of n-type metal contact on backside surface using the Temescal FCE-2500
   Evaporate 30/60/30/250nm of Ge/Au/Ni/Au

3. Dismount sample from stainless steel chuck and remove wax by heating/dissolving in 90°C TCE

4. Rapid Thermal Anneal (RTA) metal contacts

   380°C, 30 sec

5. Manually cleave samples using a sharp scalpel

6. Prepare Cu mounts

   Evaporate 50/70/50nm of Ti/Pt/Au

7. Mount die on Cu mount using indium solder

B.2   RIE Process

Photolithography: Negative resist pattern defines the metal contact pads for liftoff..

1. Solvent clean, dehydrake bake on hot plate at 150°C, i min

2. Spin resist: NR9-1000PY-negative resist

   Dispense: static

   Spin: 3000 rpm, 40sec

3. Hot plate bake: 150°C, 1 min

4. Contact Aligner- OAI HybraAlign 400 Series (MASK 1-narrow stripes) Expose
   for 14.4 sec

5. Post-Exposure Bake (PEB): 105°C , 1 min

6. Develop: RD6; 12 sec with a gentle swirl

   Metal Deposition and Liftoff: Ti/Pt/Ni is evaporated as the top p-type ohmic
contact as well as hard etch mask for the subsequent semiconductor etch.

1. Electron beam evaporation using the Temescal FCE-2500

   20/20/50nm of Ti/Pt/Ni

2. Liftoff at room temperature in resist remover RR5, 15 mins, gently swirling

3. Solvent rinse to remove excess resist, N_2 dry

GaAs/AlGaAs RIE Etch: Etch stripes into the semiconductor.

1. Etch arsenide-based materials using Plasmatherm 770 RIE

   HBr 20sccm, 375V, 2mTorr, 120W, Total time = 4:12

Nickel Etch: Remove nickel etch mask.

1. Remove nickel using Transene TFG Ni etchant at 40°C for 2:30

Planarization: Planarize the front-side ridged topography.

1. Solvent clean, dehydrake bake in oven at 130°C, 30 min

2. Adhesion Layer AP3000

   Dispense: static

   Spread: 300 rpm, 5 sec

   Spin: 2-3K rpm, 20 sec

3. Hot plate bake at 100°C, 5 mins

4. Planarization Layer BCB 3022-46

   Dispense: static

   Spread: 500-750 rpm, 5 sec

   Spin: 3000 rpm, 25 sec

5. Hot plate bake at 100°C, 1 min

6. BCB thermal cure: Anneal furnace

   Load wafer, flow N_2 (> 20scfh) for 30 mins

   Slowly ramp up to 250°C, set N_2 flow to $\approx$ 5 scfh

   Anneal at 250°C for 60 mins

   Ramp down to room temperature, flow N_2 (> 20scfh) for 60 mins

BCB Etchback: Etch back planarization layer to reveal ridges.

1. Clean chamber: CF_4 4 sccm, O_2 20 sccm, 20m Torr, 300V

2. Condition chamber: CF_4=6.60 sccm, O_2 13.4 sccm, 15m Torr, 150W, 16mins

3. Etch BCB in Plasmatherm 790 RIE

CF_4 6.60 sccm, O_2 13.4 sccm, 15m Torr, 150W, Total time= 21:44 at 0.1375 μm/min

Photolithography: Negative resist pattern defines the metal coontact pads for liftoff.

1. Solvent clean, dehydrake bake on hot plate at 150°C, i min

2. Spin resist: NR9-1000PY-negative resist
   Dispense: static
   Spin: 3000 rpm, 40sec

3. Hot plate Bake: 150°C, 1 min

4. Contact Aligner- OAI HybraAlign 400 Series (MASK 3-wide stripes) Expose for 14.4 sec

5. Post-Exposure Bake (PEB): 105°C, 1 min

6. Develop: RD6; 10 sec with a gentle swirl

Metal Deposition and Liftoff: Au is evaporated for the top p-type ohmic contact.

1. Electron Beam Evaporation using the Temescal FCE-2500
   Evaporate 200nm of Au

2. Liftoff at room temperature in resist remover RR5, 15 mins, gently swirling

3. Solvent rinse to remove excess resist, N_2 dry

Backside Processing: Thinnng the wafer and backside metal evaporation.

1. Lap backside of the wafer
   Mount samples on stainless steel chuck using LogiTech bonding wax
   Remove all the excess wax with (Tricholoroethylene) TCE and isopropanol.

Lap wafer using South Bay Technology 910 Grinder/Polisher to $\approx 160\ \mu$m thickness with 600-grit silicon carbide film.

Polish wafer backside with a rayon-fine polishing cloth and 1 μm alumina suspension

Rinse sample thoroughly with DI water

2. Electron beam evaporation of n-type metal contact on backside surface using the Temescal FCE-2500

   Evaporate 30/60/30/250nm of Ge/Au/Ni/Au

3. Dismount sample from stainless steel chuck and remove wax by heating/dissolving in 90°C TCE

4. Rapid Thermal Anneal (RTA) metal contacts

   380°C, 30 sec

5. Manually cleave samples using a sharp scalpel

6. Prepare Cu mounts

   Evaporate 50/70/50nm of Ti/Pt/Au

7. Mount die on Cu mount using indium solder

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