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Monolithic Integration of Etched Facet Lasers with GaAs VLSI Circuits

by

Yakov Royter

S.B. Massachusetts Institute of Technology (1988)
S.M. Massachusetts Institute of Technology (1991)

Submitted to the Department of Electrical Engineering
and Computer Science in partial fulfillment of
the requirements for the degree of

Doctor of Philosophy

at the

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

January 31, 1998

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Author
Department of Electrical Engineering and Computer Science
January 31, 1998

Certified by
Clifton G. Fonstad, Jr.
Department of Electrical Engineering and Computer Science
Thesis Supervisor

Accepted by
Arthur C. Smith
Chair, Department Committee on Graduate Students
Department of Electrical Engineering and Computer Science

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Abstract

Monolithic optoelectronic integration has obvious advantages of lower power, higher speed, and lower cost than hybrid and flip-chip bonding integration approaches. Most attempts at monolithic optoelectronic integration suffer from the necessity to develop both the electronic VLSI and the optoelectronic device processes simultaneously. Epitaxy on Electronics (E-o-E) technology, in which optoelectronic devices are fabricated on commercially pre-fabricated VLSI chips, eliminates the need to develop the electronic VLSI process, and gives a short term solution to optoelectronic integration. Some integrated circuits with AlGaAs/GaAs LEDs, fabricated in this technology, have been demonstrated. However, further work in optimization of the material quality, substrate preparation for epitaxy, and device fabrication techniques is needed in order to obtain reliable and employable OEICs. Furthermore, expanding the assortment of optoelectronic devices that can be produced in this technology will increase the maturity of E-o-E integration, as well as make it more attractive to a wider array of users. Both integration technology development and specific device integration techniques were pursued in this work.

For this thesis, development of the E-o-E integration technology was continued, and the feasibility of In-Plane Surface Emitting Laser (IPSEL) optoelectronic integrated circuits in this technology was demonstrated. To make the IPSELS, dry etching must be used to form the laser facets and reflectors. These lasers are fabricated from aluminum free heterostructures, using InGaP lattice matched to GaAs as the wide band gap, low refractive index material, whose optimal growth temperature is much more compatible with the E-o-E process than AlGaAs. However, most of III-V compound semiconductor dry etch technology has been developed for either AlGaAs/GaAs or InGaAsP/InP heterostructures. In order to etch the facets and reflectors for the IPSELS in the InGaP/GaAs material system, a novel bromine ion beam assisted etch (IBAE) was developed. Etch characterization was performed on InP and GaAs. Etch optimization was performed on heterostructures. Etched facet lasers were fabricated and measured. In parallel other E-o-E technology steps were optimized. These were demonstrated by fabricating LED OEICs.

Thesis Supervisor: Clifton G. Fonstad
Title: Professor, EECS

Acknowledgments

I am indebted to many people in my very long stay at MIT, but without the slightest attempt to avoid a cliché, I would like to thank my parents, Zinaida, God bless her memory, and Boris, for everything that I am and have right now. Both of them dedicated most of their lives to me, yet because of their great personal example, I managed not to turn out too spoiled. They always provided all the support they could, without applying any pressure. I only wish my mother was still here to share my joy in finishing my thesis.

This thesis would not have been possible without the support and advice of Prof. Clifton Fonstad. I would also like to thank all the other people I collaborated with at MIT, Joseph Ahadian, Steve Patterson, Gale Petrich, Hao Wang, Prof. Leslie Kolodziejcki and Aitor Postigo. Praveen Vaidyanathan and Prof. Sheila Prasad, of Northeastern University, deserve equal gratitude. Working with Joe Ahadian, despite his occasional brusque manner, was particularly productive and enjoyable.

This thesis would also not be possible without the help of our collaborators at MIT Lincoln Laboratory. Prof. William Goodhue, of University of Massachusetts Lowell, was invaluable to the success of etching done in this thesis. His students, Jennifer Rossler and Samuel Choi helped me tremendously. Advice and steady tweezers helped me time and again in processing. Daniel Mull's training and IBAE maintenance are also appreciated. Finally, discussions with Joseph Donnelly and James Walpole taught me a great deal about semiconductor lasers and helped me understand my devices.

I would also like to thank Krishna Shenoy, Eric Braun, Woo-Young Choi, Rajni Aggarwal, Jurgen Smet, and Paul Martin for their example, training, and help in the past.

Special thanks to Janet Pan and Henry Choy for their support, discussions, and offers of hot beverages during the writing of my thesis.

In addition to research, the MIT Tae Kwon Do Club was the other part of my life at MIT. The members, my friends, helped me mature during my stay at MIT. I enjoyed teaching and learning from them.

Finally, very special thanks goes to my wife and best friend, Lori Ainbinder. Her support and help is immeasurable, and even from the other side of the globe, she inspired me to work harder and with more enjoyment.

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Chapter 1

Introduction

1.1 Motivation for OEICs

The persistent increase in speed of integrated circuits has created a demand for optical signal distribution and processing [1]. Optical signals have the potential to be wider in bandwidth, higher in speed, lower in power, and lacking in crosstalk under proper conditions. The first demand for optical signal distribution was in long haul communications, where the optical fiber advantages are truly apparent. In fact, they made fiber-optic links so cost effective, that the cost of the equipment at the transmitter and repeater stations was not a limitation. As the speed and storage capacity of computers increased, and computational tasks became more distributed, more information had to be transferred to more places at higher rates. As a consequence, shorter fiber optic links connecting more nodes have become desirable. Furthermore, the fiber is getting closer to the end user, and soon we can expect to see optical fiber plugged in directly into the personal computer. At this time, more switches, repeaters, amplifiers will be needed, and at a greatly reduced cost and increased functionality [52]. Monolithically integrated optoelectronic integrated circuits (OEICs) on GaAs or InP substrates would be the most likely choice for this purpose [1, 2, 3].

In addition to the above telecommunication applications, integrated OEICs also have a future for chip to chip and board to board interconnection in computers and other computational systems [4,5,6]. As the processor speeds increase, the power required to transfer the high frequency signals from and to these chips will surpass the power required for the electrical to optical signal conversion[6]. Once the signals are converted to light, other problems of signal skew, distributed signal effects, and crosstalk will be eliminated.

Finally, elimination of crosstalk will also benefit circuits required for mobile communications, where the cost reduction of monolithic integration will be important.

1.2 Types of Optoelectronic Circuits

Optoelectronic circuits can be divided into many categories [52], according to the type of devices connected together, the way they are connected together, and the function they provide. Each of these categorization methods can produce a spectrum of categories. This is due in part to the number of applications in which optoelectronic circuits can be used, in part due to the variety of optoelectronic and electronic devices, and mostly due to the immaturity of the technology. Since few low cost high performance circuits are commercially available, no standards or preferred technologies or architectures exist.

Numerous optoelectronic devices are candidates for optoelectronic circuits [53]. First on the list are detectors [11]. These could be photoconductors, p-n junction diodes, Schottky diodes, avalanche diodes, and quantum well intersubband detectors. Materials for these could vary as well. Silicon, germanium, III-V semiconductors, and narrow bandgap semiconductors are all used for photodetectors. Some of these can be operated in both waveguide propagation and surface incidence structures. Diode lasers [7, 8] are on the same priority level as detectors, and these can be in different material systems, emitting from blue to far infrared. The structures can also vary. Buried heterostructure or ridge waveguide, Fabry-Perot or DFB, in-plane emitting or surface emitting - these are just some of the options the designer has. Modulators [9, 10] are also high on this list. Lithium niobate and compound semiconductors have been the choice, but silicon and glass have also been used. Most of these are optical phase modulators, but compound semiconductor quantum well Stark-effect absorption modulators have demonstrated good performance. Of course, modulators can act in the waveguide or surface normal mode as well. Other devices, like LEDs and liquid crystal cells can also be used in optoelectronic circuits.

Functionality of optoelectronic circuits can vary greatly. They can be applied to optical signal processing, board-to-board to on-chip optical interconnects for electronic systems, massively parallel electronic computing, all-optical computing, displays, imaging arrays, and sensors. A very common optoelectronic circuit is an optical receiver [54], where photodetectors are interconnected with electronic amplifier circuits. Some further signal conditioning and processing could also be part of the electronics. Transmitters are also very common, where light sources, such as lasers and LEDs, are connected to electronic drivers [55]. Here, as well, signal processing electronics could be made side by side with the drivers. When all three, detectors, light sources, and electronics are assembled together, another common type of optoelectronics circuit, a transceiver, is achieved. Since using external modulation is often desirable, intensity modulators are also commonly made into an optoelectronic circuit when put together with their drivers [56]. Furthermore, optoelectronic switches [52], neural network circuits [57], and Self Electrooptic Effect Device (SEED) [58] computational circuits are all examples of optoelectronic circuits. The direction of light incidence in relation to the substrate also determines functionality of the circuit. Edge incidence and emitting devices allow only one dimensional arrays of optoelectronic devices. Access issues also restrict these devices to be in the periphery of the circuit. Surface incidence and emitting architectures, on the other hand, allow for two dimensional optoelectronic arrays, where the devices are free to be intermixed.

The ways of connecting the electronic and the optoelectronic devices involves another spectrum of approaches [1, 52]. This spectrum ranges from isolated components connected together on a printed circuit board to having all of the devices being part of the same crystal. When all of the devices are part of the same crystal, this approach is called monolithic integration. “Monolithic integration” does not always refer to all the devices being part of the same *perfect* crystal. There could be a layer of high defect material or a

noncrystalline interface between one type of substrate and the other. In one such approach, lattice mismatched material is epitaxially grown on another substrate [59, 60]. Special care is taken that all of the dislocations are formed and terminated in the lower part of the epitaxial layer, called the relaxed buffer, so that the top part that has the device layers has few defects. Relaxed buffer growth is used to grow GaAs on silicon, to take advantage of the mature Si electronic VLSI processing technology, InGaAsP on GaAs, to integrate longer wavelength devices with GaAs electronics, and InGaAs on Si, for longer wavelength devices integrated with Si LSI. Wafer bonding is another such approach where most of the dislocations are right at the interface [61]. In this technology, often the epitaxial layers form the interface, and then one of the substrates is etched away. Another such “monolithic integration” technique is epitaxial lift-off [1, 62]. In this approach, the bottom layer of an epitaxial heterostructure is etched away, separating small areas of device epitaxial layers from the substrate. These small thin pieces of crystal are then transplanted to preselected areas of another substrate. Usually devices on this substrate are already processed, and only the transplanted areas require further processing.

The word “integration” is used for a variety of other approaches, but perhaps most common labels in these cases are “hybrid integration” or “heterogeneous integration”. In these approaches, the crystals of the two substrates are not really in contact. All of these integration methods have the advantage of having all of the different devices fully grown and processed, before they are interconnected. Thus all the necessary epitaxial growth and microfabrication can be done under optimal condition. A further advantage is that as many different substrates and devices can be put together as desired. The most common hybrid integration approach is epoxying all the different devices together in a ceramic or plastic package, and connecting them together with bond wires. For example, to make a receiver, an IC chip with an array of drivers is mounted side-by-side with an array of photodetec-

tors, and then the two chips are wire bonded together, and a fiber ribbon is aligned with the detectors. This approach suffers from the parasitic capacitance, inductance, and resistance of the bond wires. Moreover, large two dimensional optoelectronic arrays cannot be built this way. More intricate hybrid integration approaches which greatly reduce the parasitic impedances are flip-chip bonding and multichip modules.

The phrase “multichip module (MCM)” [63] usually refers to a hybrid assembly where chips from different substrate are mounted on a common substrate, all face up. Usually, the common substrate has etched regions in which the chips are inserted, so that they are planarized with the surface of the common substrate. Then, interconnections between chips are defined photolithographically using standard processing techniques. The common substrate is often silicon or glass, though sometimes more heat conductive substrates are required. Sometimes optical interconnection in the form of waveguides is also performed in addition to electrical interconnections.

In the flip-chip bonding [64] scheme, one processed substrate, usually consisting of electronic ICs, is left intact, with specifically patterned contacts pads included. The substrate of the optoelectronic devices is then diced or cleaved into individual devices or arrays, each also having specific contact pads. Then, these chips are mounted face down onto the larger substrate, so that the contact pads on one are touching the contact pads on the other. For mechanical stability and electrical connectivity, microscopic drops of melted indium are used to solder the contacts together. Due to the requirement of mechanical alignment of the contact pads and the solder balls, the contacts pads have to be relatively large, and therefore they introduce extra parasitic capacitance in the circuits. Circuit density is also decreased due to these large contacts.

Though this is somewhat ambiguous, systems, which have an optoelectronic device integrated with other devices, are categorized into Photonic Integrated Circuit (PIC) and

Opto-Electronic Integrated Circuit (OEIC) categories [52]. Photonic Integrated circuits refer to systems where at least two optoelectronic devices are integrated together. This integration is accomplished by waveguiding of light, and therefore occurs in the plane of the substrate. Common examples of PICs are lasers integrated with a modulator, optical splitters, optical switches, and many combinations of different waveguiding active and passive devices. Even if electronics are also integrated, such systems are still often called PICs. Often, if an active device is integrated with another active device, the heterostructure required for these devices is different. Thus, regrowth is often a common technique used for PICs. Sometimes waveguide coupling from a waveguide formed by the top heterostructure layers to the one formed by the bottom one is used to bring light from one device to another. In other structures, where an active device has to be connected to a passive waveguide, the same epitaxial layers are used for both, but selective implantation disorders the quantum well structure in the passive device area, so that the material is transparent to the active device operating wavelength. Most of the PICs are monolithic, though, in theory, multichip modules can also be used with some success.

The label Optoelectronic Integrated Circuit is usually assigned to the cases where optoelectronic devices are integrated with electronic devices. Photoreceivers and transmitters described above are examples of such circuits. Two or more different optoelectronic devices integrated together, and with electronics, are still called OEICs if the only connection between the optoelectronic devices is electronic, and not optical. Both hybrid and monolithic integration schemes can be used for OEICs. Two dimensional arrays of surface emitting and incident devices would also be considered OEICs. The system for which the work in this thesis was done is also an OEIC. A monolithic integration approach is used for this purpose, so a brief review of monolithic integration efforts will be given in the next section.

1.3 Monolithic Integration Approaches

There have been numerous attempts at monolithic optoelectronic integration on GaAs and InP substrates. Laser diodes [7, 8], modulators [9, 10] or detectors [11] have been integrated with various types of transistors. Again, a spectrum of monolithic integration approaches can be found in the literature. Everyone of them suffers from some drawbacks, depending on the choices that are made. Almost all of the optoelectronic devices require epitaxial growth, though there are some electronic devices that do not require epitaxy. Therefore the first choice to make is how to arrange electronic layers with the optoelectronic layers. Electronic layers can be grown on top of the optoelectronic layers [65], which can be accessed by etching away the transistor layers in certain areas. An exactly opposite approach of growing optoelectronic layers on top of the electronics is also possible. An advantage could be gained if the same layers could be used for both types of devices [55], though neither structure would be optimal. Finally, two different heteroepitaxial layers can be placed side by side by first etching down one layer in selected locations, and then regrowing the second layer in these etched areas [66]. Of course, all four of these options apply if homoepitaxial, rather than heteroepitaxial electronic devices are used.

Each one of these options has advantages and disadvantages. Planarity of the surface during critical photolithography steps plays a big part in their success. If the surface is not planar, then both the nonuniform photoresist thickness and an increased requirement on the depth of focus of the aligners, make it difficult to define small features. For the current state of the art devices, electronic devices have smaller features than many of the optoelectronic ones. Therefore having electronic devices on top has an advantage over having them below the optical devices. Furthermore, the epitaxial layer thicknesses of the optical devices is usually on the order of 3-4 μm , whereas the electronic devices are less than 1

μm thick. Thus, having the electronics on top, and then etching these layers selectively to expose the optoelectronic layers produces a much more planar surface than when the top optoelectronic layers have to be etched down to the electronic layers. The decreased planarity of the electronics on the bottom approach makes it more difficult to define upper level metallization as well. However, the disadvantage of having the electronic layers on top is that the junctions and the conductive layers of the optoelectronics will cause back-gating and crosstalk effects in an electronics circuits. Solution to this problem could be achieved either by deep isolation mesa etching or by providing contact to a common highly conductive layer just below the electronics and tying it to a known potential. Both of these solutions require extra space and decrease circuit density.

Using the same layers for both electronics and optoelectronic devices has its disadvantages as well. The biggest one is that each type of device will have a far from optimal structure. In circuits where state of the art is often not good enough, this restriction will limit the practicality of this approach. Perhaps the side by side approach is the best in terms of planarity. However, though recent improvements have been shown, good quality epitaxial regrowth on etched surfaces is still a challenge. Furthermore, most of the time the material on the periphery of the regrown material is not of good quality, which decreases the circuit density.

Another choice that needs to be made in an integration technology is the exact order of the process steps. This order can alleviate or worsen the problems of each integration approach mentioned above. For example, some process steps can planarize the surface to some degree. Properly performed dielectric isolation film deposition is one example of a step that reduces step heights. Many other process steps, however, produce more surface structures. Therefore, processing the most critical layers first, such as the electronics, can be a definite advantage. The homoepitaxial electronic devices are defined by dopant

implantation, which usually requires subsequent high temperature annealing. This annealing will significantly degrade heteroepitaxial interfaces. Thus, for the side-by-side integration approach, implantation and annealing should be done before the regrowth.

Even when electronics are fabricated on a planar surface, very large scale integration (VLSI) is difficult to achieve in a research lab, which is part of the reason why no optoelectronic VLSI have been demonstrated. This is not due to a fundamental limitation, but rather to the cost and complexity of developing a VLSI process. A state of the art electronic VLSI process requires extensive development and dedicated production lines and staff. Process uniformity and defect density minimization are the key issues for VLSI. This can only be achieved in a dedicated commercial foundry.

To eliminate some of the disadvantages of the integration approaches described above and to use the commercial VLSI foundry capability to fabricate the electronics, an alternate integration approach called Epitaxy-on-Electronics (E-o-E) was proposed [12]. In this approach, the electronics are fabricated in a commercial GaAs VLSI foundry. The finished VLSI circuits are then further processed to clear selected areas, the dielectric growth windows (DGWs), down to the substrate. Once the substrate is opened, the next step is epitaxial growth. Finally, the optoelectronic devices are fabricated and interconnected with the electronic circuits [13, 14, 15]. This approach has the advantage of fabricating the electronic circuits first, doing all the implantation annealing before the optoelectronic layer growth, growing only once, having no extra crosstalk and backgating problems, using predefined and preconnected bottom contacts for the optoelectronics, and planarizing the surface by growing the epitaxial layers the same thickness as the interconnection stack.

1.4 Thesis Overview

In the previous sections, motivation for optoelectronic circuits was given. Advantages of monolithic integration, especially for high density OEICs, were also described. There is no mature technology available yet that can produce high density OEICs. One of the more likely candidates for this task is believed to be the Epitaxy-on-Electronics integration technology. Work on this topic was already started, and the general purpose of the work described in this thesis is to develop this technology further and to acquire all the necessary expertise to make it useful for a real OEIC system.

The improvements on the E-o-E technology that have been made are the more robust and mass-production compatible methods of pre-growth substrate preparation and post-growth planarization. All of the other work done for this thesis involves developing the design and processing capabilities to make two dimensional OEIC systems with emitters, detectors, all the drivers and amplifiers, and digital VLSI circuits monolithically integrated on one substrate. Although some work was done with LEDs as emitters, this thesis is mostly concerned with the effort to develop a technology with In-Plane Surface Emitting Lasers (IPSELS) as the emitters. The major obstacle to developing IPSEL fabrication compatible with E-o-E technology is its material system requirement. Due to lower growth temperature, the InGaP/GaAs material system is used for the emitters, instead of the usual AlGaAs/GaAs material system. For IPSELS, dry etching with straight sidewall profiles is extremely important. No dry etches that satisfy this condition for InGaP/GaAs material system have been developed previously. Neither have there been any reports of IPSELS in this material system. Thus the major thrust of this thesis work was to develop a suitable dry etch. For this purpose a bromine Ion Beam Assisted Etching (IBAE) system was assembled and employed. Since no bromine IBAE work has been reported, a study of the etching characteristics of this system on GaAs and InP was conducted. Etching studies of

InGaP and InGaP/GaAs heterostructures were also carried out. The proper etch mask material and patterning procedures were also dealt with in detail. To test the quality of the etch, InGaP/GaAs etched facet lasers were fabricated and measured. Most of the procedures and results of this work, as well as some background material will be described in the remainder of this thesis.

In Chapter 2, the basic concepts of E-o-E technology will be described. The challenges for this technology will be outlined to put this thesis in perspective. Issues such as circuit degradation and material choice will be briefly discussed. Detailed descriptions of the improvements made to pre-growth substrate preparation and post-growth planarization will be also described in Chapter 2. Chapter 3 will start with an introduction to different dry etching equipment and chemistries to provide the background for the choice of the bromine IBAE system. In the same chapter, IBAE principles of operation and system description will be given. Then, results of the GaAs, InP, and heterostructure etch studies will be given. Finally, the efforts of obtaining the best etch mask will be explained. In the next chapter, Chapter 4, etched facet laser results are given and interpreted. Finally, in Chapter 5, after some conclusions, suggestions for improvements in all aspects of this project will be given, since the efforts on this project will be continued by others. Also for the sake of the people continuing this project, Appendix A contains details of fabrication procedures, and Appendix B thoroughly describes IBAE operation and maintenance procedures.

Chapter 2

Epitaxy-on-Electronics Technology

2.1 Technology Description

As mentioned in the Introduction, Epitaxy-on-Electronics technology is a very promising way to produce optoelectronic VLSI in the near future. The primary reason for this is that the electronics are fabricated in a dedicated commercial foundry. Therefore all the electronic steps are thoroughly developed and tested, and the process reproducibility and uniformity is constantly checked and maintained. Furthermore, all of the devices and interconnections in this process are well characterized, and accurate simulation models are available, including parameter statistical variation data. This allows for much more straight forward and reliable design methodology. Additional design simplification is created by the necessary CAD tools development by the company that fabricates the electronics. For example, for the layout tool that was chosen for this thesis, the company provided the proper technology file, all the layout rules, as well as the files that are necessary for schematic extraction (generation, out of a layout schematic, of a model circuit consisting of correctly sized and typed transistors, resistors, diodes, capacitors, and wires). The VLSI circuits were obtained through the MOSIS service, which had them fabricated by the Vitesse Semiconductor Corporation. These VLSI circuits were fabricated on a GaAs substrate, which is another advantage, since good quality lattice matched optoelectronic device layers can be grown on this substrate. The circuits are based on metal-semiconductor field-effect transistors (MESFETs). Both depletion mode (DFET) and enhancement mode (EFET) MESFETs were available [68]. In the HGaAsIII technology used for this project, the minimum effective gate length is 0.6 μm . All parts of the transistor were defined by selective implantation. Only refractory metals were used for Schottky (WN)

and ohmic (NiGe) contacts. Four levels of WN encapsulated AlCu_x upper level interconnection is also used in this technology [17, 67, 68].

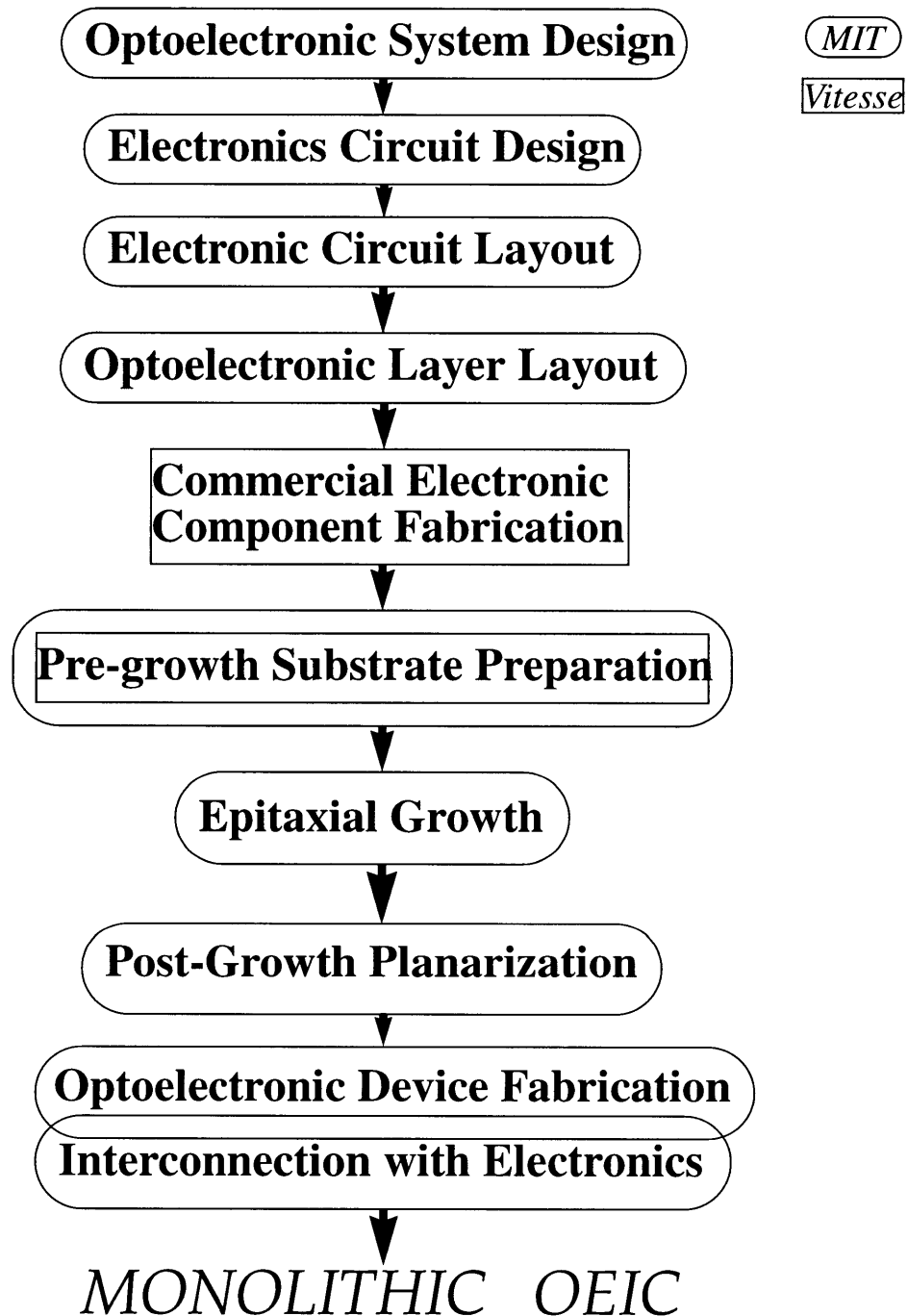


Figure 2.1: Design and process flow of the Epitaxy-on-Electronics Technology.

The Vitesse HGaAsIII technology is primarily designed for digital applications. Because of the full four level interconnection capability, complex VLSI circuits are possible. These digital circuits are also fast, with a 70 ps gate delay when used in direct coupled FET logic (DCFL) mode [68]. However, analog circuits, needed for driving optoelectronic devices, can also be designed using this technology. Usually a 2 V power supply is used, though power supplies as high as 4 V can be used reliably. In addition to MESFETs, two types of detectors can also be fabricated in this technology. One is an optical field-effect transistor (OPFET), which is an EFET with a floating gate. The other one is a metal semiconductor metal (MSM) photodetector, made up of interdigitated Schottky gate metal. An OPFET is slow, but has a large intrinsic gain and in combination with a properly sized active DFET load, it is sufficient to convert an optical digital signal into a DCFL signal. An MSM detector is much faster, but requires a transimpedance amplifier at the output. Both of these devices are used for surface normal incidence operation. Both of them use GaAs as the photogeneration layer, and are sensitive to radiation of about 850 nm wavelength.

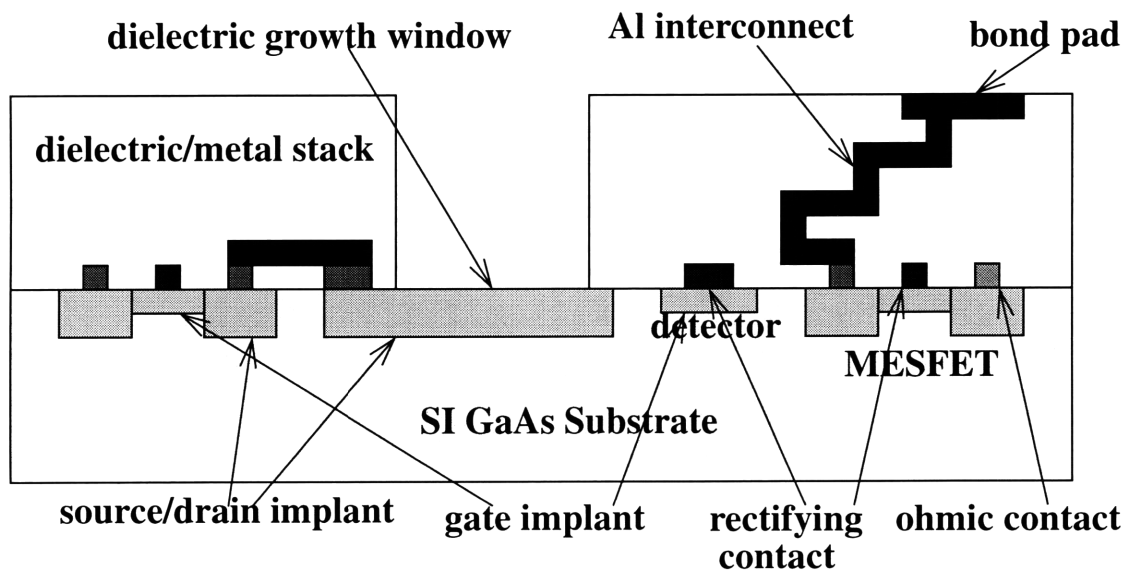
The flow of the design and process steps is shown in Figure 2.1 [13, 15]. The first step is the design of the system. Requirements, such as wavelength, speed, optical power, power dissipation, and power supply voltage, are taken into account. Next, the optoelectronic devices are designed to meet these requirements. Usually these devices are first fabricated on bulk substrates to ensure proper operation. The electronic circuits are designed next. Logic corresponding to the high level system description is first derived, and then the actual transistor circuits are designed. Analog circuits are also designed to drive optoelectronic devices or amplify optical signals; this is done with optoelectronic performance characteristics in mind. All these circuits are tested using device models provided by the foundry. Finally, these circuits are laid out, providing proper structures needed for the

optoelectronics. Bottom side contacts, openings in the dielectric stack, and metal lines and pads to which the top side contacts will be connected, are the main examples of such structures. After schematic circuit extraction, the circuit verification and resimulation can be performed. Finally, at this stage, the design can be sent to the foundry for fabrication. At this stage, the layout layers for the optoelectronic device fabrication and pre- and post-growth processing are also generated. These are not sent to the company, but are used to create photolithographic masks for use when the chips are received.

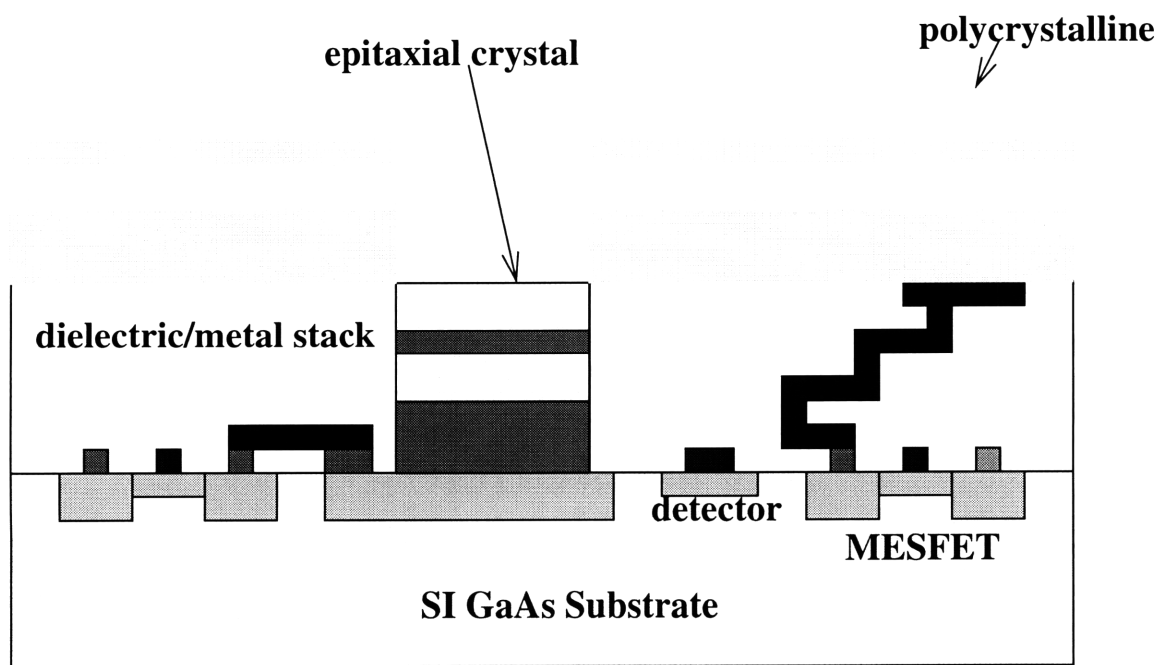
Multiple copies of the chips are sent back from the VLSI foundry. Usually, electronic testing is performed as the first step. Then the preselected areas in the dielectric stack are opened up to the substrate, creating dielectric growth windows (DGWs). At this point the chip looks like the schematic depiction in Figure 2.2a. Where the dielectric stack is opened to the substrate, there is a highly conductive n-type implant, which is used as the bottom side contact of the optoelectronic devices. This implant extends slightly outside the DGWs, and an ohmic contact is made to it there, which is further connected through top-level interconnection metal to the electronics. The electronics, including the detectors, are still protected by the dielectric stack. Some of the circuit nodes also have connection to the bond pads on surface of the stack. These pads are used either for probing or bonding to a package, or for the interconnection to the top side contact of the optoelectronic devices.

After the DGWs are opened and the substrate is fully prepared, the optoelectronic device heterostructure layers are grown. Inside the DGWs, crystalline material which is a continuation of the substrate is grown. Usually, it is grown the same thickness as the thickness of the dielectric stack. Outside of the DGWs, on top of the dielectric stack, polycrystalline material is deposited. This stage of the process is illustrated in Figure 2.2b. Next, the polycrystalline material is etched away to planarize the chip surface, as shown in Figure 2.2c. Finally, the optoelectronic layers are processed into devices. These devices, are

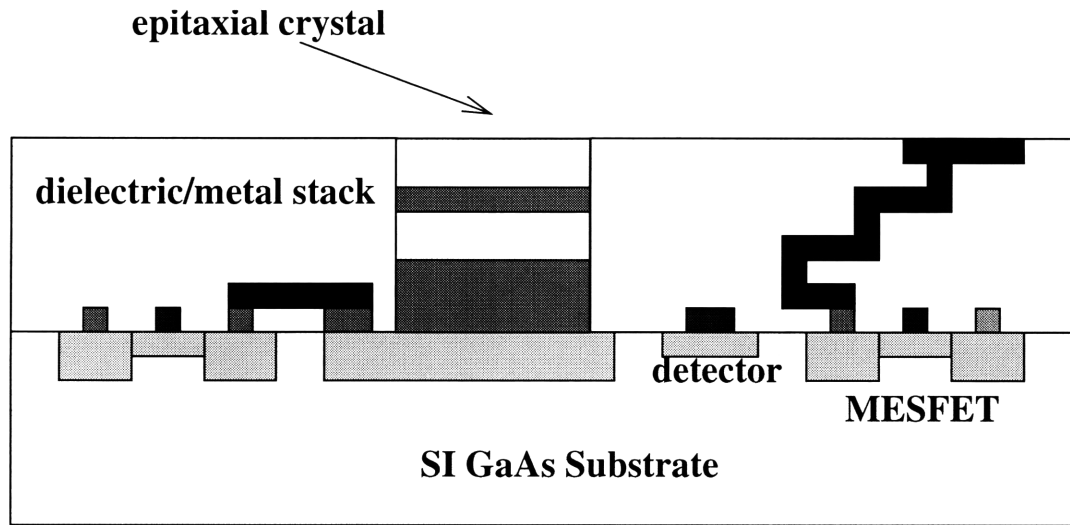
interconnected with another layer of metal to the surface pads of the electronic circuits (Figure 2.2d). This finished OE-VLSI circuit chip can then be packaged and measured.



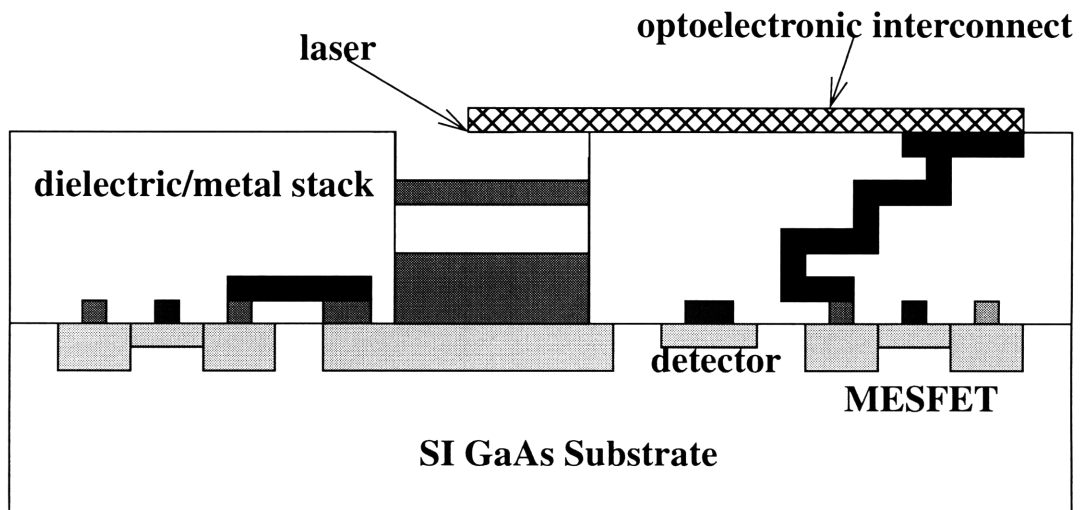
a) pre-growth view



b) post-growth view



c) post-planarization view



d) finished OEIC

Figure 2.2: Schematic illustration of the major stages of OEIC fabrication in the E-o-E technology: the commercially fabricated chip after a) DGW cleaning, b) epitaxial MBE growth, c) polycrystalline material removal from the dielectric stack, and d) optoelectronic device processing and interconnection with the transistor circuits.

Care is taken during the design to provide test structures for each step in the process. Thus a properly designed E-o-E OEIC will have test circuits for electronics performance comparison before and after growth and processing. Structures that allow to test etch depths, contact quality, and interconnection metal quality, among other processes should be included in the optoelectronic device lithography masks. Of course, the locations for these test structures is included as extra DGWs on the electronic circuit layout. Provisions are also made for alignment marks to be defined on the chips at the foundry, and during each step of the fabrication.

As mentioned before, this technology is currently designed so that the more densely integrated part of the OEIC, the electronics are fabricated in a dedicated state of the art commercial facility, and the optoelectronic components are fabricated in a general purpose university laboratory. Fabrication requirements for the optoelectronic devices can often approach the ones for VLSI circuits. Therefore, for this technology to become mature, efforts have to be made to bring each process step into the dedicated production line where state of the art equipment is used, and each process step is optimized and controlled for consistency. However, a dedicated commercial foundry is extremely expensive, and market demand justification has to exist for its implementation. Therefore, the laboratory approach is useful as a development and a demonstration tool. Demonstration of a working system is required to attract industrial interest.

An additional incentive for the commercial development of this technology would be its applicability to a broad range of optoelectronic systems, demonstrated by integrating various devices with the GaAs VLSI. Thus, once the steps specific to the E-o-E integration are far into their development, the types of optoelectronic devices that can be put on the chips can be considered for different applications. As already mentioned, as part of the VLSI process two types of optical detectors, OPFETs and MSM photodetectors are

already available. Both types of detectors are GaAs and are sensitive around 850 nm. The devices that need to be grown can be broken down into surface emitting/incident and in-plane devices. The most basic surface emitting device that can be grown on the chip is an LED. A much more elaborate extension of an LED process would be Vertical Cavity Surface Emitting Lasers (VCSELs). A reflection modulator, which can be used for SEED devices as well, is another option. Detectors which are sensitive at other wavelengths, especially 1.3 μm and 1.55 μm , would also be very useful for telecommunication purposes. These would have to be grown on lattice mismatched, relaxed buffers. Among the in-plane devices, laser diodes would be the first to come to mind. Waveguides, and waveguide modulators and detectors also have a potential usefulness for complex switching nodes. In-Plane Surface Emitting Lasers (IPSELs) are a cross between the in-plane and surface emitting devices, and have certain advantages over VCSELS, making them good choices for many applications [16].

2.2 Technology Challenges

Despite the many advantages, the Epitaxy-on-Electronics process has numerous challenges that need to be overcome. Some of them are intrinsic to the technology itself, and some stem from the limited access to the VLSI manufacturing process. The biggest challenge is preserving the performance of the electronics on the chips during the growth. In order not to degrade the electronics, the growth and the pre-growth native oxide removal temperatures needed to be decreased as low as possible without sacrificing material quality. The optoelectronic device processing steps also have to be designed to not degrade the electronics. Circuit protection from chemical exposure has to be considered. Also high temperature processes, such as implantation anneals, CVD, and mass transport have to be avoided. Other fabrication challenges also need to be solved. For example, for the final optoelectronic interconnection, a detrimental reaction between gold contacts, used for

optoelectronic devices, and aluminum, used to the upper level interconnection, has to be solved. Another problem that needs to be solved is the planarization of the epitaxial material with the surface of the chip. Preparing the chips for growth is also a very important challenge. The substrate that is opened for growth has to be totally cleaned of the dielectric deposited in the foundry, and yet be undamaged, and free of other residues. The dry etching process used to remove dielectric at the foundry damages the crystal and leaves a fluoro-carbon residue on its surface, so a separate process had to be developed.

While developing the processing techniques necessary for E-o-E integration, the difficulties are compounded by the fact that the substrate opening and post-growth processing has to be done outside the VLSI facility, on small chips, rather than on full wafers, and with limited numbers of these chips. When these chips are received, they are cut into as small as 5x5 mm chips. The limited quantities are as low as twenty samples per run. Furthermore, we have no control over the processing steps, and receive limited information about the process and any changes in it. We receive these chips at most twice a year, during which time the foundry process changes just enough to cause problems. Finally, the processing facility we work in is primitive, in comparison to the foundry, thus making it almost impossible to achieve the optimal density and yield for the optoelectronic devices. All these factors have to be considered when designing all the process steps for any of the E-o-E projects in which we are involved.

Perhaps, the biggest issue for the Epitaxy-on-Electronics technology is the degradation of the integrated circuits due to high temperature exposure during epitaxial growth. This degradation occurs because of the upper level metal deterioration. The problem is compounded, by the fact that more than 6 μ m of material have to be grown to planarize epitaxial films with the top of the metal/dielectric stack. This corresponds to 7 hours of high temperature exposure. For such a long duration, degradation seems to have a critical tem-

perature range between 475-500°C, with exposures above those temperatures rendering the circuits dysfunctional [17, 18]. This degradation is demonstrated in Figure 2.3, where the measured data of the interconnection metal sheet resistance after a five hour thermal exposure is plotted against the temperature during the exposure. In this plot, it is evident that 475°C is about the highest temperature where degradation does not occur. Thus, the optical devices have to be grown at the temperatures close to or below the 475°C, limiting the material choice to ones that can be optimally grown at that temperature. Another constraint for the material system is that it has to be lattice-matched to the GaAs substrate. For double heterostructure waveguides on a GaAs substrate, thick layers of lattice matched wide bandgap material for the upper and lower claddings are needed. With the material growth capability at MIT, this allows three options for this cladding material: AlGaAs, InGaP, and InGaAsP.

The most convenient choice of material system for the waveguide heterostructure would be the GaAs/AlGaAs system, where AlGaAs would be used as the cladding, and either lower mole fraction aluminum AlGaAs or GaAs as the guiding core. This material system is the one most commonly used for double heterostructures lattice matched to GaAs, and is regularly grown in the MIT's MBE machines. Since a range of Al mole fractions can be used for either the cladding or the core, with almost no lattice mismatch, a greater design flexibility is obtained. Even more importantly, the processing technology, that is the recipes for wet and dry etching and metal contacts, is well established. Unfortunately, the best AlGaAs is grown at 600-700°C range, with material quality degradation below that temperature [19, 20, 21]. Attempts at growth of lowered temperature (<530°C) AlGaAs with conventional MBE at MIT has had some, though with limited success [15]. Many lasers, made with lowered temperature AlGaAs do not perform nearly as well as the ones grown at regular temperatures [19, 21]. This could be a problem with oxygen incorpo-

ration and DX center formation, which contributes to shorter recombination lifetimes, leakage current, etc. The exact causes are not totally clear, but consistent poor laser performance indicates very little future in such material for lasers and LEDs (unless it is grown by a nonconventional techniques, such as migration enhanced epitaxy [22, 23, 24]).

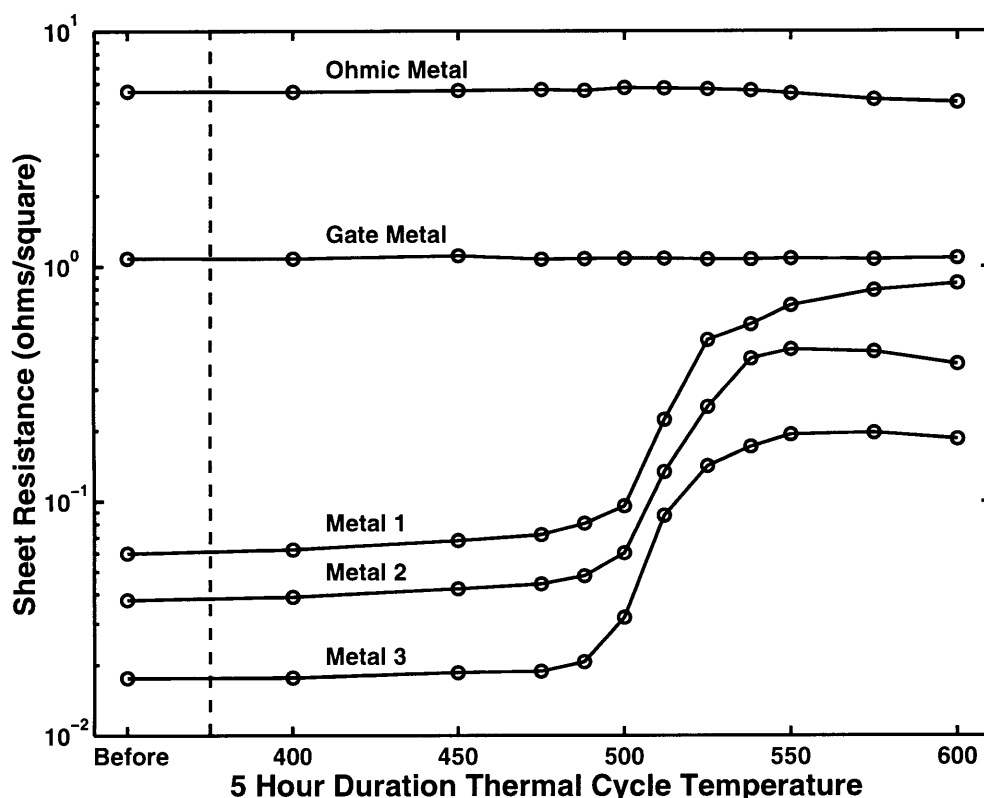


Figure 2.3: Interconnect Metal degradation after a five hour thermal exposure at various temperatures [17].

The choice of the alternative material system lattice matched to GaAs comes from the work done in the past decade on aluminum free lasers. These lasers use a ternary compound $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$ as the wide band gap material. Unlike AlGaAs which is closely lattice matched to GaAs for any aluminum to gallium ratio, InGaP is only lattice matched when the indium composition is 49%. For a continuous bandgap change, the quaternary

compound, InGaAsP, would have to be used. The greatest advantage of these materials for our project is that they can be grown at 475°C with good quality in an MBE system. (An MOCVD type of system cannot be used for this purpose because it requires substrate temperatures of about 700°C [25, 27].)

InGaAsP, though interesting and promising, would be a difficult material to work with, since reliable growth is more difficult than for the ternaries, and little work has been done on InGaAsP matched to GaAs at MIT. (So far, only quaternary material matched to InP has been studied.) Therefore, the possibility of using InGaAsP for the cladding or the core of waveguides could not be relied on for this thesis. However, material grown under conditions not compatible with E-o-E and containing quaternaries will be used for certain parts of this project [27]. Thus, the material system used for the E-o-E integration of IPSELS with GaAs VLSI will be InGaP/GaAs.

In the long run, however, the ability to grow InGaAsP lattice-matched to GaAs will be extremely important. Having this ability can both improve laser performance and greatly simplify OEIC system design. The reason for improved laser performance can be understood by looking at the typical band diagrams of modern semiconductor lasers in Figure 2.4. Almost all of the modern lasers are quantum well lasers. The quantum well material has the lowest bandgap in the heterostructure. It also has the highest refractive index, but it is too thin to provide well confined mode characteristics in a waveguide. For this purpose, a thicker higher bandgap and lower refractive index material is used around the well to act as the waveguide core. Of course, a third, even higher bandgap and lower refractive index material is used as the cladding on either side. Thus, the simplest quantum well laser structure, shown in Figure 2.4a, has three types of material used. However, the electrons traveling from outside to the inside of the well do not always have the time to thermalize with the rest of the electrons in the well, and for this reason not all of the electrons in the well

reach the subband energy of the well. To fix this situation of poor carrier confinement, the core material is graded in composition (and band gap) from the cladding to the well. Linearly graded confinement layer and parabolically graded confinement layer laser band structures are shown in Figure 2.4b and Figure 2.4c respectively. To achieve such structures for our purpose, InGaAsP growth capability is needed, which will improve laser performance.

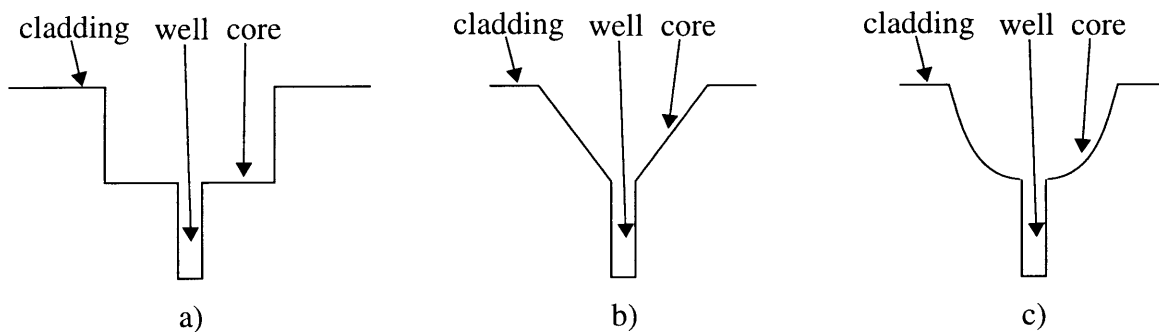


Figure 2.4: Quantum well laser band structures: a) simple structure, b) linearly graded carrier confinement structure, c) parabolically graded carrier confinement structure.

Perhaps even more important is the system design simplification that this capability can provide. Going back to the simple quantum well structure of Figure 2.4a, three materials are needed. The cladding and the core materials, since they are thick, have to be lattice matched. Thus using only the InGaP/GaAs material system, InGaP has to be the cladding and GaAs the core, thus making the well material (pseudomorphically strained InGaAs, for example) to have a bandgap smaller than GaAs. This laser, then, will emit light at a longer wavelength, which GaAs does not absorb. Therefore, the detectors which can be fabricated in the commercial VLSI process cannot be used, and separate detector layers or structures which can be used as both detectors and lasers will have to be grown. This

would greatly complicate the OEIC fabrication process. If, however, lattice matched InGaAsP can be grown, then InGaP would act as the cladding, InGaAsP as the core, and GaAs as the well material. Thus, the wavelength compatibility problem would be solved. (Using the wavelength that is absorbed by the substrate, however, can create problems of crosstalk between an optoelectronic device and other electronic or optoelectronic devices in the vicinity. This is another challenge for the E-o-E technology.)

For a successful epitaxial crystal growth, the high temperature is required not only during the deposition but also during the native oxide desorption from the growth substrate. For GaAs, the substrate temperature has to be increased above 580°C to desorb the oxide. This temperature, unfortunately, will destroy the electronics. Alternatives to thermal oxide desorption have been explored in the past. The use of hydrogen plasma or thermally cracked atomic hydrogen [13, 28] was proved to be successful for low temperature oxide desorption. For this project, atomic hydrogen oxide removal will be used. The substrate for this process is held at 300°C, which is well within acceptable limits.

2.3 Dielectric Growth Window Cleaning

The choice of the right material system and the optimization of the epitaxial growth conditions are not the only requirements for good material quality. In the E-o-E integration technology, the other requirement is a clean undamaged starting surface for growth in the Dielectric Growth Windows (DGWs). As in the case of growth, the cleaning procedures are constrained to processes which do not destroy the circuits on the chip. In this case, instead of thermal damage to the higher level metal interconnection, one has to take care that the whole dielectric stack, the bondpads, the ohmic contacts connecting to the DGW, and the crystal surface itself do not get damaged during the etching of the 6.5µm dielectric stack. This phase of the E-o-E process is affected by fact that different chip generations have somewhat different dielectric stack structures. Consequently, different chip genera-

tions present different problems during DGW cleaning.

The Vitesse HGaAsIII process has four levels of aluminum interconnect metallization [67, 68]. The top and bottom of each aluminum layer is protected by a thin tungsten nitride layer. PECVD oxide is deposited on top. Then, spin-on glass is used to planarize the structure. PECVD oxide is deposited again before WN and aluminum are deposited and patterned. The process has both depletion mode and enhancement mode MESFETs. The active area and the channel are implanted, with silicon nitride and oxide used for the mask. Though the process is described here in some detail, many of the aspects of the process are proprietary and are unknown. Furthermore, due to changes during the half to full year period between each generation of the chip, the dielectric stack structure changes somewhat, causing very noticeable differences in the etching. This situation provides unwelcome challenges to the E-o-E process.

The first attempt at the DGW cleaning (Figure 2.5a) was done on chips from a three level metal Vitesse process, HGaAsII. Passivation (usually used to open the bond pads) and the scribe line etches were used at the foundry to open up the windows all the way to the substrate. After an oxygen plasma clean, and a quick buffered hydrofluoric acid etch, the chips were put into an MBE for AlGaAs LED structure growth. The LEDs fabricated on the chips did emit light, but with very poor efficiency. The surface of the DGWs was not carefully investigated for surface roughness. More importantly, it became apparent later, that single crystal material grown on those chips was fortuitous, since later attempts to remove the fluorocarbon deposits from the substrate surface on chips from the same batch have failed.

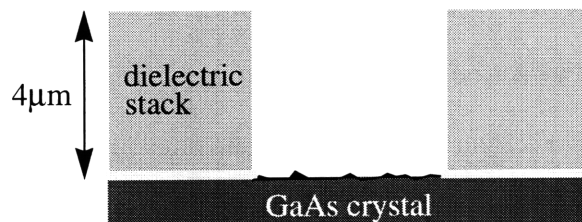
For the next generation chips (Figure 2.5b), the multiproject MIT-OEIC3 [15], only the scribe line etch was performed at the foundry in the DGWs in attempt to leave between half and one micron of the dielectric. However, this chip was fabricated in the HGaAsIII

process with four levels of interconnect metal, and the dielectric stack is more than $6\mu\text{m}$ thick. The scribe line etch was not as deep as expected, at least not for this run. Therefore the OEIC3 chips had $4.0\text{-}4.5\mu\text{m}$ of dielectric left in the dielectric growth windows. To remove this dielectric, a range of approaches were investigated. Using an CF_4/O_2 reactive ion etching (RIE) system, we cleaned the DGWs were cleaned down to the substrate. The oxygen level was kept in the 10% range to reduce the polymer deposits. However, even when no deposits were visible by Nomarski filter microscope, the surface had many dislocations, which were later traced to dry etching deposits. In addition to the deposits, surface damage from the ion bombardment in the RIE was also observed. For the overetch of 30 min, the surface roughness could be observed by Nomarski filter microscope. Even for 5 minute etch, the GaAs surface was clearly roughened, when examined in an atomic force microscope (AFM). The chips were routinely overetched by about 30 min, since the thickness of the dielectric stack varied from chip to chip, and even in different locations of the chip. Another problem with the dry etch was that the selectivity between photoresist and silicon oxide was so poor that the resist etched faster than the oxide. To compensate for this, both multiple remasking and metal mask approaches were used, both of which were cumbersome.

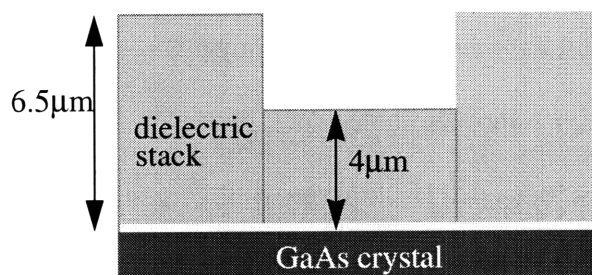
Wet etching the dielectric stack was also labor intensive due to the lateral etching at interfaces, which exceeded vertical etch rates by more than an order of magnitude. One of the interfaces that did not hold up to the etching was the photoresist-silicone oxide interface. The hydrofluoric acid seeped underneath the resist and etched outwards as far as $30\mu\text{m}$ in 10 minutes. One interface near the bottom of the dielectric stack was also causing problems, because the acid etched laterally along it. It is speculated that it was the silicon nitride to silicone oxide interface, but this could not be verified. Thus, multiple lithography steps were required for wet etching down to the substrate. Even when the oxide was

etched down to $0.5\mu\text{m}$ from the substrate with the RIE, the subsequent wet etch required at least two photolithography steps to complete it.

a) First Generation



b) Second Generation (OEIC3)



c) Third Generation (OEIC4 and OPTOCHIP)

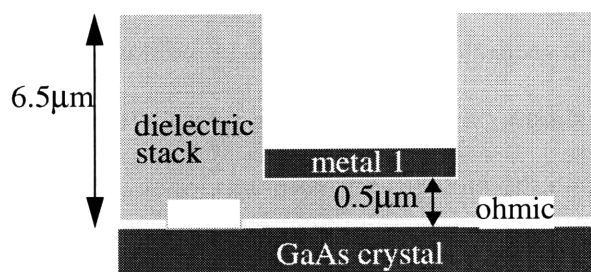


Figure 2.5: Dielectric growth window (DGW) design progression. Shown are the DGWs after the commercial VLSI fabrication, and before the pre-growth processing.

The dielectric growth window cleaning procedures described above were too cumbersome and labor intensive, and had a potential to drastically reduce the yield for good devices. The optimal process would consist of an etch at the foundry that comes close to, but stops short of the substrate uniformly across the wafer. Then, the rest of the DGW can be wet etched clean in the laboratory. A solution which comes close to this situation is to put first level interconnect metal over the DGW, and then have the foundry do both the passivation and the scribe line etches (Figure 2.5c). These etches will go through the whole dielectric stack, and stop on the metal, since aluminum is not attacked by the oxide etch. The aluminum, then can be wet etched away, leaving the dielectric underneath. The dielectric thickness under the metal is very uniform, since it is so close to the planar substrate. It is about $0.5\mu\text{m}$ thick, and a few more lithography steps are required to finish the cleaning. This approach was employed on OEIC4 and OPTOCHIP chips [13], and though not perfect, is a much more reliable process.

Unfortunately, the OEIC4 chips were delivered in very limited numbers, and have since been used up. The only chips available for laser and waveguide projects are the OEIC3 chips with the old DGWs with $4.5\mu\text{m}$ of dielectric left to remove. There is usually an additional $0.7\mu\text{m}$ of silicon oxide deposited on top to protect the bondpads during the post-growth planarization. Fortunately, the DGW for the experiments in this thesis is very large, $450\mu\text{m} \times 6\text{mm}$, and more room for lateral etching can be allowed. Some details of the chip layout and the dielectric growth window geometry used for this project are illustrated in Figure 2.6.

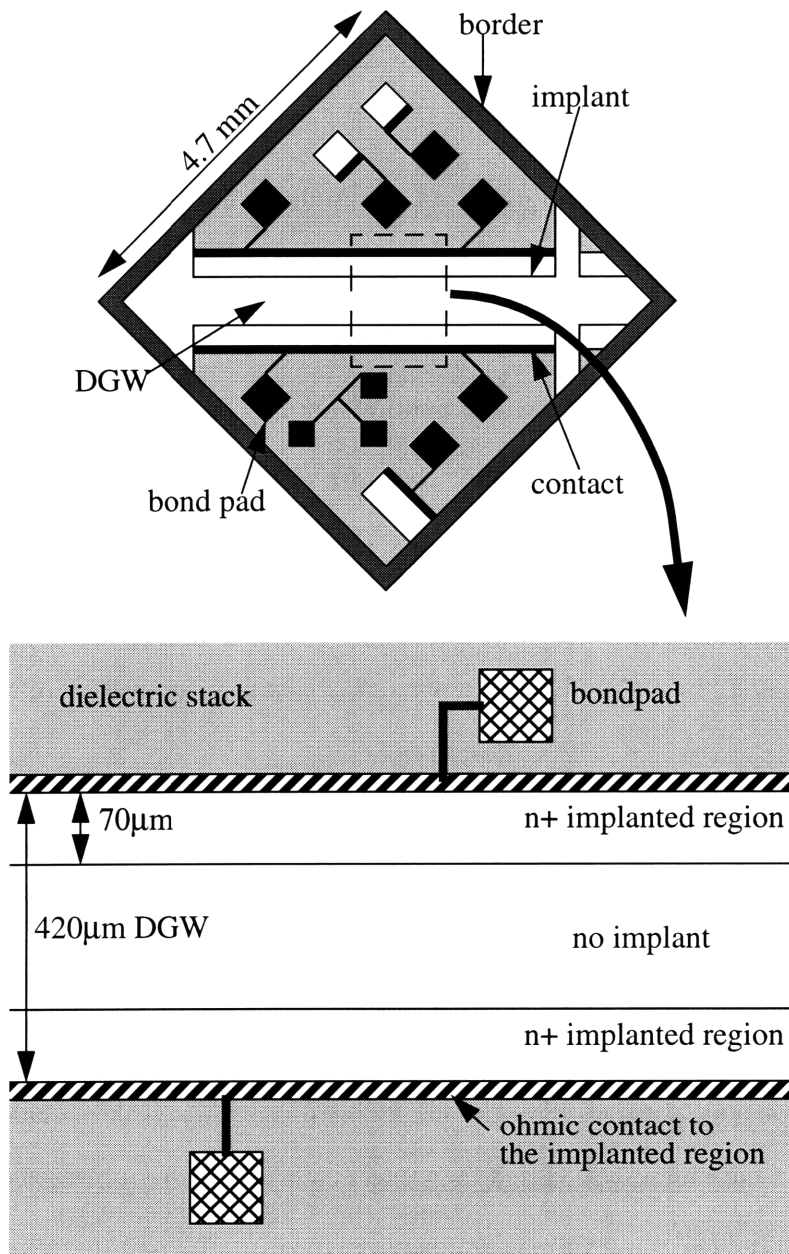


Figure 2.6: Schematic of the OEIC3 chip layout and of the stripe DGW geometry.

The substrate material in the window is not uniform, but consists of both implanted and unimplanted regions. The implanted region is vital to our process, because together with the ohmic (source/drain) contact, it provides the bottom (n-side) contact. The reason

the middle of the window is not implanted is that it was thought that the material quality grown in the implanted region would be inferior to the unimplanted one, and by partially implanting the periphery of the DGW, the device could be grown on the unimplanted region, while still having the bottom contact available. (Since then, no detectable quality difference between the material grown on the implant and outside the implant was found so in the OEIC4 and OPTOCHIP designs all of the DGW was implanted.) As a result of this, even if only the middle 50 μm is needed to be opened for a device, most of the stripe has to be opened in order to make the bottom contact. Thus when cleaning this window, the photoresist line was patterned about 20 μm from the contact, which leaves 50 μm of the implant cleaned. During the wet etch, the region of the DGW next to the contact is inspected for lateral etch spread, and when the damage gets close to the contact area, the photoresist is reapplied. An all-wet etch process requires about five lithography steps to complete.

To reduce the number of steps, and thus increase the yield and productivity, a different dry etch was attempted. CHF_3 gas was added to the RIE system, which when used similarly to the CF_4 etch produced an oxide-to-photoresist etch ratio of 1.2:1. Thus, with a 4.5 μm thick resist, the dielectric stack in the DGW can be etched down to the substrate without removing all of the resist first. The dry etch was used to get down to about 0.1-0.3 μm of dielectric in the thinnest spot, and then a wet etch is used (requiring two more masking steps) to clean the DGW down to the substrate. However, the RIE might not be acceptable for the etch, due to some evidence that the residue deposited during the etch on the oxide, somehow redeposits on the substrate after the oxide is wet etched away. This was demonstrated in a parallel plate oxygen plasma etcher, and has not been demonstrated on the particular RIE system used for the DGW opening. The morphology of the chip DGW crystal surface and the bulk wafer crystal surface after growth seemed identical under an optical

microscope with Nomarski filters. Photoluminescence of the chip and bulk material was also similar, with the chip material having a stronger peak. However, the quality of the growth was extremely poor, so any substrate quality effects might have been below the noise level. Whether the contaminants are permanently deposited will have to be determined in a more formal study in the future, by analyzing the substrate surface after DGW cleaning and the material quality after growth on chips prepared by the RIE and wet etch processes.

If the RIE process does not cause contamination, the new generation chips will be cleaned in the following manner: First, silicon oxide will be deposited to provide bondpad protection during subsequent processing steps. Then, the first lithography step will be performed, and the protective oxide in the DGWs will be removed with RIE. Using the same photoresist, the WN/Al/WN first level metal will be wet etched away using H_2O_2 to remove WN, and HCl to remove aluminum. Again, the same photoresist will be used to dry etch the dielectric underneath the metal until about $0.1\mu\text{m}$ remains, and without touching the substrate. This process should be more reproducible and controllable, since the dielectric underneath is uniform and relatively thin. One more photolithography step will be needed to wet etch the $0.5\mu\text{m}$ of SiO_2 , and one more to wet etch the 40nm Si_3N_4 layer on top of the substrate, finishing the DGW cleaning. If the RIE does cause contamination, all of the dielectric under the metal will have to be wet etched.

2.4 Post-Growth Planarization

Planarization of the optoelectronic device epitaxial layers with the top surface of the interconnect metal/dielectric stack is important for two reasons. First, a planar surface allows for much better control of the photolithographic patterning, enabling definition of smaller features. A non-planar surface does not allow close contact between the mask and photoresist, causing diffraction and rounded wavy features. It also causes photoresist thickness

variation on different parts of the wafer, not allowing for use of optimal process parameters for all the features on the chip. The ability to define smaller features enables an increase in circuit density, as well as improvement in device performance. Moreover, for such devices as waveguide switches and splitters, device performance is critically dependent on small feature patterning capability.

The second reason for having the epitaxial material top surface level with the dielectric stack, is the ease of interconnection it provides between the optoelectronic devices and the electronics. If there is a drop between the two surfaces, metal coverage over that drop becomes a problem. This is especially true if the drop is very straight, as would be for mostly dry etched features. However, even if the drop is slanted, the yield would be reduced. Furthermore, patterning metal over this drop is also a problem, especially for small features desirable for high density applications. Thus, having a planar structure before optoelectronic device processing is important.

To make the epitaxial layers planar with the dielectric stack, their thickness has to be equal to the thickness of the stack, and usually, a buffer is grown on the substrate, providing for the extra thickness. However, the material is not only deposited inside the DGWs, but also on the dielectric stack in a polycrystalline form. This polycrystalline material deposited during growth has to be removed to make the surface planar.

The removal can be done by covering the epitaxial material with masking material, and etching the polycrystalline material away. Most etching mixtures for compound semiconductor will not etch the silicon oxide containing materials, so the PECVD deposited oxide and spin-on glass on top of the dielectric stack will not be affected by the chemistry used to strip the polycrystalline material. However, the aluminum bondpads will be destroyed by most of these chemicals. To prevent the damage to the bondpads, therefore, a layer of silicon oxide is deposited on the chip surface prior to the DGW substrate cleaning

procedure. In the future, a layer of dielectric on the bondpads will not be etched away at the foundry and will be left intact, eliminating the need for the bondpad protection process step.

There are two options for the poly stripping: wet or dry etching. Wet etching is quicker and this was the original method. For the AlGaAs/GaAs material system, an $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2$ mixture in aqueous solution was used. For the InGaP/GaAs material system, alternating etches of $\text{HCl}/\text{H}_3\text{PO}_4$ aqueous solution for InGaP and $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2$ aqueous solution for GaAs was used. A single etch of $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ can also be used for this material. However, it is harder to control. Unpredictable undercutting is possible, creating a risk of the wet etch solution penetrating under the protective mask, and damaging the epitaxial layers in the DGWs. Furthermore, it has been noticed that for some versions of the HGaAsIII Vitesse VLSI chips, the dielectric underneath the poly cracks during the growth. These cracks then provide a path for the wet etching solution to seep under the top dielectric layers, destroying some of the aluminum interconnects and bondpads.

To avoid the hazard of wet etching, mainly due to the isotropic nature of the etch, dry etching was used for stripping the polycrystalline material. Room temperature dry etching of GaAs is usually done with chlorine containing compounds. However, these do not etch indium containing semiconductors due to low vapor pressure of indium chlorides at room temperature. Indium containing compound semiconductors are usually dry etched with methane and hydrogen mixture. However, this process does not etch GaAs very well. Due to availability, the initial dry etching of the poly stack etch was done with chlorine at elevated temperatures (150-225°C) on an Ion Beam Assisted Etching (IBAE) system, which uses extraction grids to extract an argon ion beam from an Electron Cyclotron Resonance (ECR) plasma source [13, 29]. At these temperatures, the etch rates of InGaP are fairly fast, and the etch is mostly anisotropic. GaAs has a much stronger isotropic etch rate, but

much smaller than the anisotropic component. More importantly, it is much smaller than with a wet etch, where all of the etching is isotropic. Because the temperatures are high, photoresist cannot be used, and silicon oxide will have to be the choice as a protective mask for this step. The LED OE-VLSI project used this processing step for post-growth planarization with the sample heated to 195°C. The etching characteristics of the InGaP/GaAs material system in the chlorine IBAE system will be discussed later in Section 3.3.

As another option for polycrystalline material stripping, a bromine IBAE was also used, since this system is already being developed as a laser facet etch. The advantage in using this system lies in the fact that the etch can be performed at temperatures as low as 50°C, so that photoresist instead of silicon oxide can be used to mask the DGWs. This eliminated the need for the oxide etching before the poly strip, and the patterning of resist after the poly strip to protect the dielectric stack during the oxide removal from the epitaxial material after the poly strip. This resist can then also be used for the dry etching of the oxide deposited on the bondpads. Perhaps using an IBAE system for this step is too costly for a manufacturing process, but a bromine based RIE etch for the InGaP/GaAs material system can very likely be developed.

2.5 E-o-E OEIC Examples

Most of the work described in this thesis was done for a project whose final goal was E-o-E integration of IPSELS and GaAs VLSI circuits. Due to the complexity of the IPSEL fabrication, the final IPSEL OEIC was not fabricated for this thesis, but rather the development of the IPSEL fabrication techniques and improvement of the E-o-E technology are its focus. However, a fully completed E-o-E OEIC with LEDs was completed with the author's participation. Therefore, as an example of the full E-o-E development, design, and fabrication process, this project will be briefly described in this section.

The project to be described here is called OPTOCHIP [69]. For this project, MIT acted as an optoelectronic integrated circuit foundry for eight other research groups. Each group had available to them 2 mm x 2 mm chip for their project. Including MIT, nine projects were placed together in a 3x3 array (see Figure 2.7). The total size on the chip, including the scribe lanes and borders, was slightly less than 1 cm on a side. The choice of devices for the OEICs included all the transistors and photodetectors available in the Vitesse HGaAsIII process, and LEDs. All the groups used a modified technology file for their circuit layout, which included layers used for the LED and pre- and post-growth processing. However, a standard LED cell was provided for them to instantiate into their design. This cell included all the layers, including the DGW, bottom contact, and top contact pad definition at Vitesse, and all the layers for the processing at MIT. Full control of the electronic and detector device cells was given to the individual groups, and cells for LED drivers were also provided for optional use. All of the electronic component models, schematic files extraction files, and rule checking tools were provided by Vitesse.

Before the designs for the groups were commenced, the details of the integration process and the LED structure were designed and tested. For the design, both the experience from previous E-o-E integration efforts and the results of new experiments and simulations were utilized. For the E-o-E technology experiments, a multiproject OEIC4 chip was used. (Since multiple copies of chips come from the foundry, a few projects can be put on the chip, with a few copies of the chip used for each project. This is the multiproject chip concept. In theory, only a portion of each copy of the chip is used, but often it is the case that the circuits and the DGWs on other projects can also be used.) OEIC4 chip was the first chips with the new generation DGWs. As described in Section 2.4, this new design has the level one metal protecting a thin dielectric layer and the crystal from the etch at the foundry, which removes the rest of the dielectric stack in the DGWs. The process steps

needed to clean out the rest of the material in the DGW were developed on these chips. Estimates for the proper size of the DGW were also obtained from these experiments. The wet etch chemistry for the post-growth polycrystalline material removal was also developed on this chip. As mentioned before, alternating GaAs etchant and InGaP etchant method was used. Problems, such as cracks in the upper dielectric layers after growth, which allow the penetration of the acids and destruction of the circuits underneath, were also noted. This prompted investigations into the dry etching technology necessary for poly stripping. Another issue, growth on the chips for this project, was also addressed using the OEIC4 chips.

LED design and process development was done on both bulk GaAs substrate and OEIC4 chips [13]. The major LED heterostructure design issue was the thickness of the active layer. After different structures were tested, the structure was chosen with a n-doped GaAs buffer layer, 700 nm n-type InGaP layer, 600 nm nominally undoped GaAs active layer, 700 nm p-type InGaP layer, and 200 nm p+ GaAs contact layer on top. Other issues for the LED design and processing were mesa depth for current isolation, top contact shape, size, and location, and the location and size of the contact pads. A structure with 30 μm wide mesa, 3 μm Ti/Au contact arranged in a 20 μm wide square on a side was chosen. Commercial software was used to model current spreading, and to assist in the contact design. Interconnection with the chip's electronics was also investigated. Aluminum, patterned by wet etching, was used for interconnection. It was discovered that aluminum reacts with the gold contact, causing high series resistance. This prompted a study of alternative LED contact structures. It was also realized that dry etching aluminum is a process much less susceptible to photolithographic misalignments, because of the minimal lateral etching.

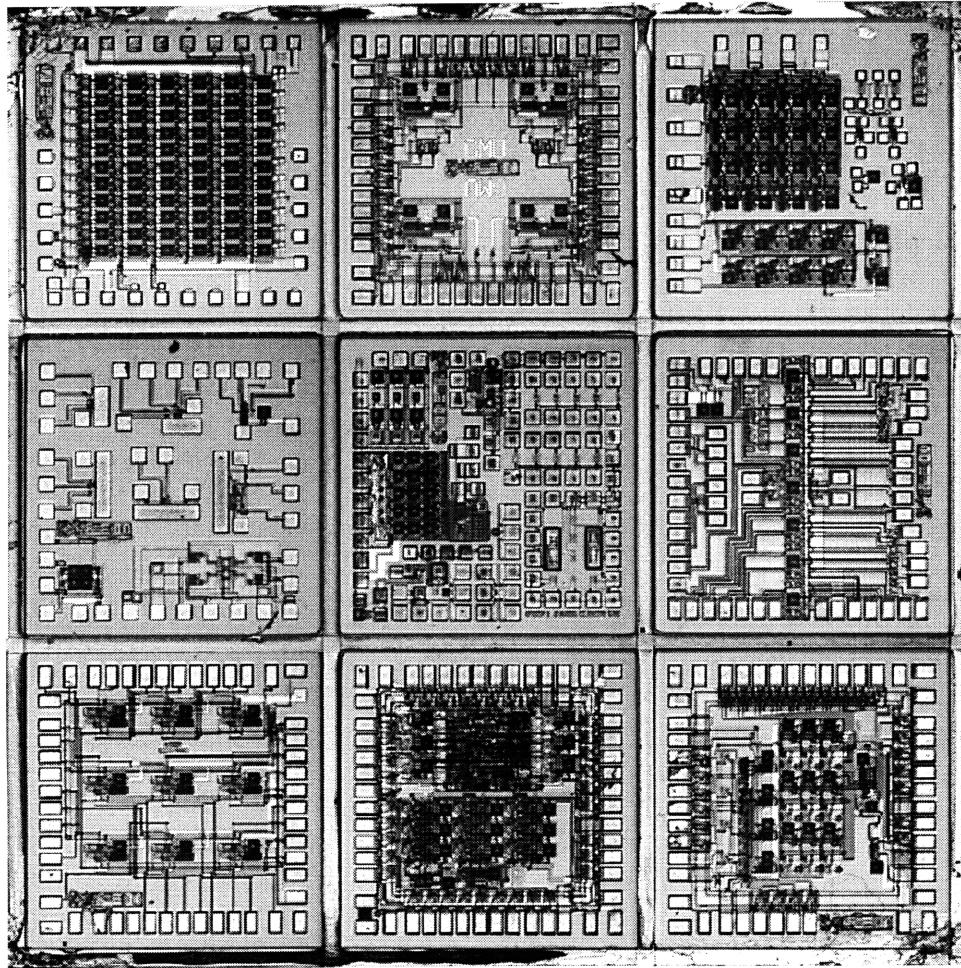


Figure 2.7: Photograph of the completed OPTOCHIP OEIC.

OEIC4 chip was also used to do some electronic circuit characterization. The transimpedance amplifier was tested. The LED driver was tested to make sure sufficient current is supplied to the LED in the “on” state, and that the LED is off in the “off” state. Circuit performance degradation after epitaxial growth and device processing was also studied. No significant degradation was found. Finally, the effect of optical crosstalk was also studied.

The design and testing of the E-o-E integration process, the LED structures, and the electronic circuits, provided us with enough information to decide on the final LED cell that the participating groups were using. Additional layout rules to those required by the

Vitesse line were also decided on. For example, a bondpad design, different from the one recommended by Vitesse, was requested in order to increase planarity of the chip surface. Also, all were requested to include alignment marks in their portion on the chip. Continuous communication between the eight groups and MIT was maintained to ensure proper understanding of the design rules, and to solve any unforeseen problems. Once the design of the chip was completed, the layout was assembled at MIT, rule checked, and sent out to Vitesse for fabrication through MOSIS.

Most of the eight groups used their chip area to fabricate a system. On the portion of the chip designed by MIT, mostly testing and demonstration circuits were included. Some area was left for E-o-E process characterization. Some special DGWs were included to study different size LED structures. Of course, electronic test circuits, such as a ring oscillator, from which the gate delay, a parameter very sensitive to the circuit degradation, can be easily obtained, were also put on the chip. A variety of detector structures were also included for future system optimization. Furthermore, different types of LED drivers, integrated with LEDs were put on the chip. Different types of OEICs were designed. One, was a simple structure with an OPFET/active load structure connected through a digital inverter, and then through a driver to an LED, to study crosstalk issues. As a demonstration project for integration of an LED array with complex digital electronics, a 5x3 array of individually addressable and drivable LEDs was connected to a combinational logic circuit, which converted a binary number input into a display. (The LEDs can be seen in a camera, which is sensitive to 850 nm light.) This circuit was called the “Number Array”. A high speed, high density circuit was also designed. In this circuit a 300x300 μm size “pixel” was made up of one LED, one detector, and 500 transistors (including the LED driver). The detectors and LED centers were 150 μm apart, so that if an array of these “pixels” was assembled, a standard fiber ribbon with 150 μm pitch can be used to bring in

and carry out the signals. The electronic circuits consist of a ring oscillator, and seven D flip-flops to divide the oscillator signal to measurable levels. It is designed such that if the light is shining on the detector, then the LED output is about 300 kHz, and if the detector is not illuminated, the LED output frequency is half, or about 150 kHz. This circuit, called the “Smart Pixel”, is shown in Figure 2.8.

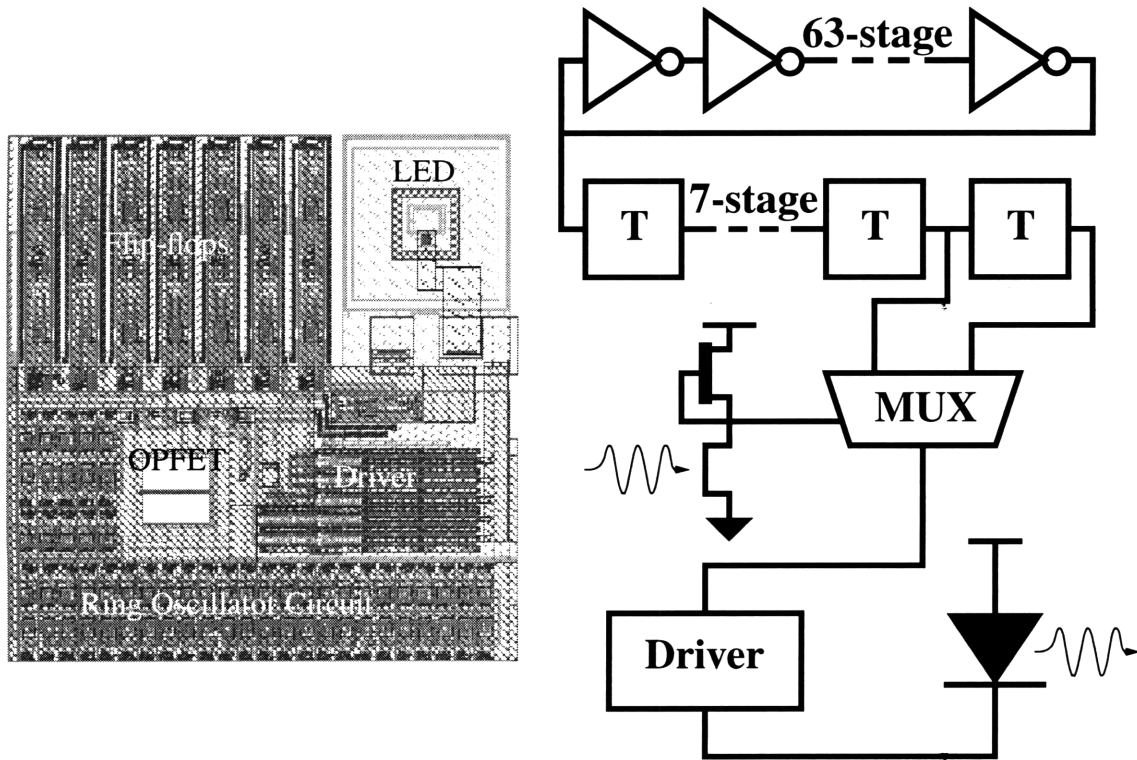


Figure 2.8: Smart Pixel circuit: layout schematic and functional block circuit diagram.

After the chips were received from Vitesse, the electronics were tested. For circuits that would be integrated with LEDs, the current provided by the driver was measured. All of the circuits performed as expected, though the Smart Pixel circuit frequencies were higher due to improper modeling of the gate capacitance.

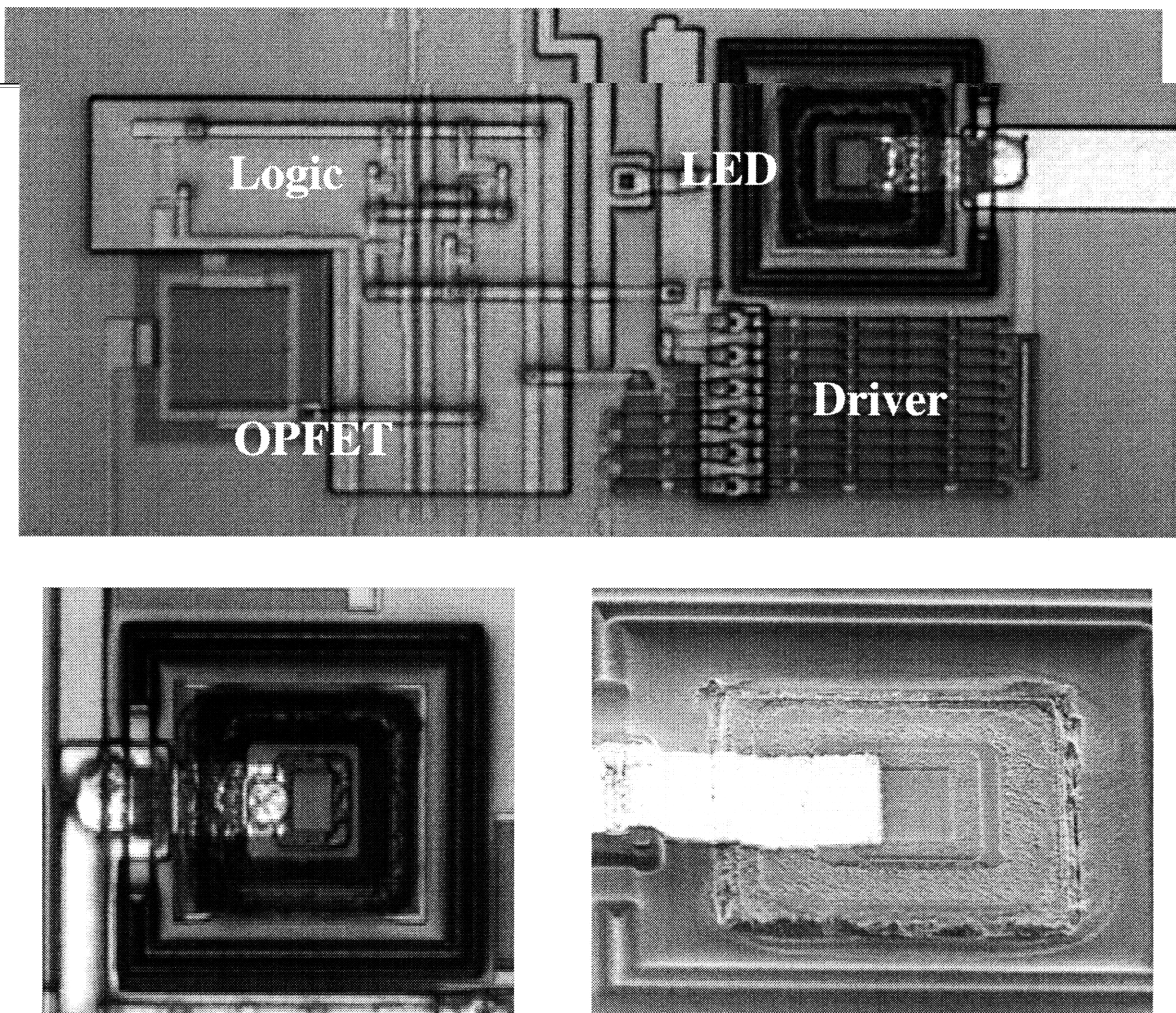


Figure 2.9: Optical microscope and SEM images of a fully processed and interconnected LED on OPTOCHIP.

First fabrication step was bondpad protection dielectric deposition. Next, DGW cleaning was performed. All wet etch processing was used. After the protective aluminum layer was removed, five photolithography steps were performed until the substrate was cleaned of the dielectric. Next, epitaxial growth was performed. After growth, the chip was remounted on a larger silicon piece with indium for ease of handling. Oxide was patterned to protect the crystal, and the chlorine IBAE was used to strip the polycrystalline material.

Using another lithography, the oxide on the crystal was removed. Next, the top contact was deposited using the lift-off technique. To avoid the detrimental effects of the aluminum and gold reaction in the subsequent interconnection, Ti/Pt and Ti/Au/Ni (where Ni forms a barrier) were successfully employed. After the contact patterning, the mesas were etched using wet chemistry. Isolation dielectric was laid down next. It was patterned to open vias to the LED contacts. Next the protective dielectric was removed selectively from the bondpads using dry etching, since wet HF etch will damage the bondpads. Once the pads and the contact vias are open, aluminum is deposited. The fabrication procedure was concluded by patterning it in a chlorine based RIE system. The completed OPTOCHIP is shown in Figure 2.7. A fully processed and interconnected LED is shown in Figure 2.9.

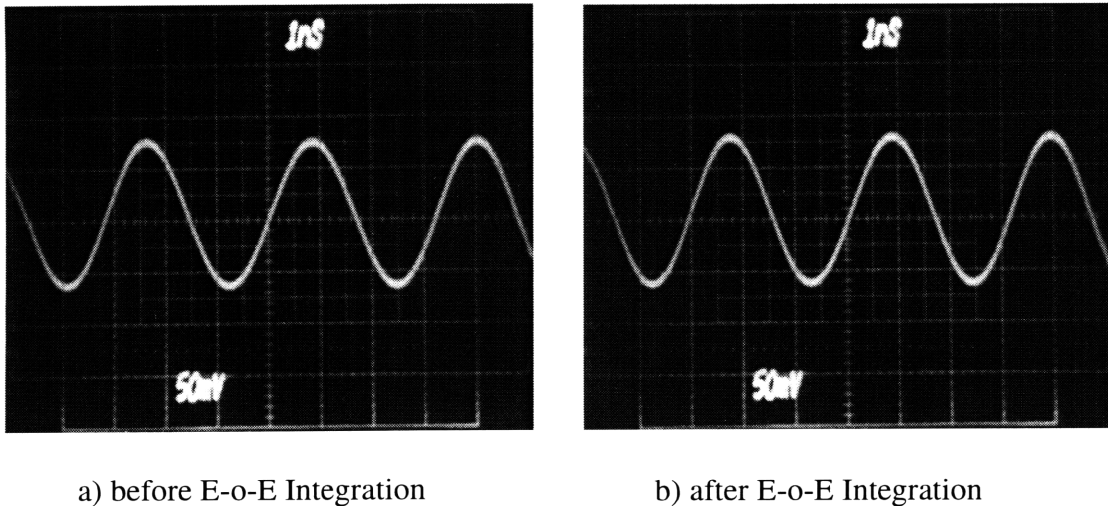


Figure 2.10: Output waveform of a 23 stage ring oscillator circuit a) before and b) after the E-o-E integration process. The gate propagation delay of 67 ps remained constant [70].

Some of the chips were tested to make sure the electronics and the LEDs were functional. For example, a 23 stage ring oscillator circuit frequency of five unprocessed chips was compared to the frequency of the same circuits on five chips after growth and processing. (Different chips were used for the pre- and post-integration measurements.) The aver-

age frequency for each group suggested the same 67ps gate delay for both pre- and post-integrated chips, as shown in Figure 2.10. A photograph of a functioning LED is shown in Figure 2.11. The major problem with the OEIC performance was LED performance uniformity. Finally, after the measurement, the nine project chips were diced using a diamond saw into the individual 2x2 mm chips, and shipped for testing to the groups.

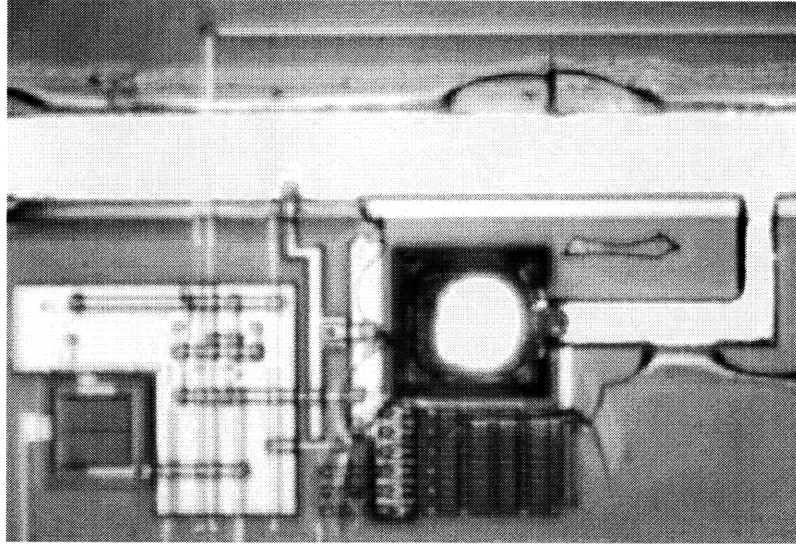


Figure 2.11: A functioning OEIC with an emitting LED.

Chapter 3

Laser Facet Etching

3.1 Facet Etch Requirements

As is true for any laser, semiconductor lasers require an optical cavity, defined by mirrors, in order to establish lasing. The mirrors provide feedback for photons associated with a select number of optical Fabry-Perot modes (preferably one for most applications), which in turn, through stimulated emission, generate more photons in these modes, creating coherent laser radiation. A typical semiconductor laser mirror is created by a crystallographic cleaved facet perpendicular to the laser cavity. Reflectivity of these cleaved facet mirrors is close to the reflectivity of a normal incidence plane wave on a semiconductor-to-air interface, approximately 30%. Because semiconductor lasers have the highest optical gain of any laser gain medium, such reflectivity is enough to provide sufficient feedback for lasing, even with sub-millimeter size cavities.

When discrete semiconductor lasers are fabricated commercially, most of a semiconductor wafer is patterned with laser cavities running along a major crystallographic direction. The wafer has to be thinned to $< 150 \mu\text{m}$ to maximize the chances of obtaining a good cleave. Then, it is cleaved perpendicular to the cavities into bars, tested, and cleaved or sawn again to separate individual devices.

The necessity of creating good cleaves for the laser mirrors complicates the laser process, introduces extra handling, and reduces yield. The first critical step in the process occurs during the alignment of the laser facet to the crystallographic axes. If there is any misalignment, mirror reflectivity will be effectively reduced. The necessity of thinning the wafer introduces problems in subsequent process steps, such as back-side metallization and testing, due to the wafer fragility. Finally, the impossibility of testing the devices on a

full wafer, and the need to handle small laser bars makes the mass fabrication process even more complicated and costly. Thus, an ability to fabricate laser mirrors without relying on the cleave would be an enhancement of the manufacturing process [1].

Another application for non-cleaved facets is for two dimensional arrays of lasers [16]. These lasers would be emitting normal to the surface of the laser, such as In-Plane Surface Emitting Lasers (IPSELS) described in Section 4.1, where a deflector redirects the light perpendicular to the wafer. As discussed in the introduction, these arrays are indispensable for certain OEICs, where the lasers would be intermixed with electronics and detectors. The research done for this thesis was conducted with exactly such a system in mind.

In addition to IPSELS, there are other devices that can only be built if vertical facets can be fabricated. Total Internal Reflection (TIR) mirrors at abrupt waveguide bends would allow compact photonic circuits [71, 72]. Losses at continuous bends can also be drastically reduced if the waveguide walls at the bends act like curved facets [73]. Semiconductor ring lasers, where the cavity is continuous, and only one facet is allowed to transmit, is another example [74]. A U-shaped laser, where both output facets are facing in the same direction, is another application [75]. Laser and modulator integration also requires such facets before regrowth [53].

One approach to forming a laser facet without cleaving the whole wafer is microcleaving [76]. In this approach, selective etching is used to etch away the substrate under the epitaxial laser layers, forming a cantilever from the laser layers. Then, the cantilevers are cleaved off. Published attempts at using ultrasonic vibration to microcleave devices across a full wafer produced poor yields, and each microcleave had to be done by hand. For this reason, microcleaving is an inefficient method to produce facets without cleaving the substrate. Furthermore, no sloped deflectors for IPSELS can be formed. Thus, the most attractive and common way to make non-cleaved facets is by etching.

From the description of different applications above, an ideal type of etch required for laser and waveguide mirrors and deflectors can be deduced. Such an ideal etch would etch all the device epitaxial layers and not effect the etch mask. It would be able to produce walls perfectly perpendicular to the wafer surface, regardless of the crystallographic direction of the etch feature or the crystal orientation of the substrate. (Sometimes wafers are cut as much as 10° away from a crystallographic plane to enhance epitaxial growth properties.) The walls would be perfectly straight vertically, regardless of types of materials included in the heterostructure. Furthermore, the wall should not recede back from the etch mask, reproducing mask profile perfectly. This is especially useful for structures employing separate facet and deflectors, or for TIR mirrors at waveguide turns, where alignment is critical. Moreover, the etch should not leave any roughness or damage on the facets. Rough facets would cause scattering losses at the mirrors, and any defects at the mirror could cause laser reliability problems during high power operations. Finally, the etch should be totally isotropic and crystal orientation independent, allowing for complex facet and deflector shapes.

Some other, less obvious requirements, would make device fabrication simpler and reliable. The first requirement would be etch rate reproducibility and uniformity. The etch rate should also not depend on the pattern feature size, depth, or orientation. For etching complicated deflector shapes, having the rate to be equal for all the heteroepitaxial materials would be a major advantage. Sometimes, having a material, a thin layer of which, when incorporated into the heterostructure, acts as an etch stop, is very advantageous for etch depth control. Process reliability is further enhanced by a etch which is relatively insensitive to small parameter variations. Finally, simplicity and safety of the equipment should also be considered.

In the case of the present project, an etch is required that will create smooth and straight walls in a heterostructure composed of lattice matched InGaP, InGaAsP, and GaAs. Since parabolic deflectors will be fabricated, the etch should optimally have the same rates for these materials. Finally, it should be possible to use a photoresist mask for this project, which is easy to apply and to remove.

All of the ideal etch characteristics described above are difficult to obtain simultaneously. Some of these requirements must be relaxed when developing real process steps. For the present application, retaining the requirement of verticality and smoothness of the facets is of utmost importance. Having the etch rate vary for different semiconductors in the heterostructure is not as important, as long as the rates are consistent. Simplicity of the etching system can also be compromised, as long as the possibility of full wafer processing is retained. The availability of an etch stop layer is also not as important. Finally, materials other than photoresist can be used as an etch mask without too much penalty. This material does not have to be totally resistant to the etch, as long as the integrity of the pattern remains throughout the etch.

3.2 Dry Etching Equipment and Processes [36]

The first attempts at making IPSEL structures were done with wet etching 45° intracavity deflectors [77]. Some lasers with wet etched vertical facets were also obtained [78]. However, constraints on the type of the heterostructure and the exact facet orientation make obtaining straight wall profiles with wet etching proved very difficult and not practical. Since the development of mature plasma processing technology, it became obvious that the most appropriate method for laser facet fabrication is dry etching.

Dry etching usually refers to etching with gaseous reactive species under kinetic energy assistance. Usually, the kinetic energy assistance is obtained by creating a plasma,

and then accelerating the ions out of the plasma towards the sample using a built-in or applied potential bias. The ions impinging on the sample are relatively normal to its surface, thus providing a relatively vertical etch profile. In addition to the kinetic assistance, plasma etching has another advantage of being able to generate new etching species during the electron-ion collisions. Because of these properties of plasma etching, it has become the technology of choice for etching in the semiconductor industry.

The relevant parameters of any plasma etch in the vicinity of the sample are the types of reactive species and their concentrations, energy of the impinging particles, their concentration, and their directionality, and the temperature of the substrate. The way these local parameters are related to the global parameters, such as gas flows, chamber pressure, incident electromagnetic power, and the bias voltage, is totally dependent on the type of system, and varies greatly even among similar system types. Usually only empirical knowledge of a particular etching apparatus is the only way to investigate its potential for a certain application. However, before choosing among the options available, the different types of equipment need to be reviewed and compared. When doing so, one can estimate, if only qualitatively, the relative range of the local etching parameters available. Just as important as the range of the parameters, the extent to which these parameters can be controlled independently also must be considered. Therefore before starting with the project, different types of dry etching equipment were evaluated with the above considerations in mind.

The simplest type of dry etching equipment is what is most often called a barrel etcher. In this apparatus, a low pressure gas mixture is introduced into a cylindrical quartz cavity. A coil is wrapped around this cylinder, and a Radio Frequency (RF) current is passed through this coil. The electromagnetic field set up by this coil interacts with the gas molecules, ionizing some of them, and thus creating a plasma. Some of the electrons, acceler-

ated by the field, collide with more molecules, ionizing them as well, creating a denser plasma. The field, electron to molecule collisions, and ion to ion collisions sometimes break bonds, creating unstable radicals. Since the pressure in the chamber is low, the chance of these radicals colliding and recombining back to the stable compounds is lowered. It is these unstable radicals with prolonged lifetimes that are responsible for most of the dry etching.

The electrical characteristics of the plasma are also important to many etching processes. The electrons are much faster than the positive ions in the plasma, and thus respond much more quickly to the field than the ions. Thus during each cycle of the RF field, the electrons are attracted to one or the other part of the coil, reaching the walls of the chamber closest to the coil. The ions are also attracted to the opposite parts of the coil, but since they move much more slowly, they do not have time to respond fully, so most of them do not reach the walls of the chamber. Thus, this discrepancy in the electron and ion speed, creates a space charge layer at the walls of the chamber. As this space charge builds, it creates a built-in DC field. This field grows as the space charge layer grows, until it prevents the electrons from reaching the walls, and in this way limits itself and the extent of the space charge region. Apart from the space charge region, the plasma itself is quasi-neutral, and being conductive, it is at an equipotential. If something, such as a sample, is inserted inside this plasma, however, the conductivity of the plasma is locally interrupted, and a space charge region forms around this object. The built in field associated with this space charge layer is only about 5-20 V. However, acceleration of ions even by this small field does enhance the etching characteristics.

The major drawback of the barrel etcher is the small ion energy available to assist the chemical etching. Furthermore, the field direction around the sample is not uniform, so the direction of the ion impingement is not uniform. These two facts are the reason that the

etch profiles in this equipment are not vertical, and some undercutting is also evident. Finally, none of the local etching parameters can be controlled independently. Each of them - ion energy, ion current density, and the radical types and densities - depends on each of the global system parameters, such as gas mixture and pressure, RF power, sample and sample holder location and geometry, and on the chamber configuration. Barrel etchers are useful though for very thin film etching, cleaning the bottoms of photoresist patterns, as well as stripping materials. This is the least expensive dry etching apparatus used in the industry.

Another inexpensive etching apparatus is a parallel plate plasma etcher. In this case, the RF field is applied between two equal size parallel plates, and the sample is placed on one of the plates. Just as in the barrel configuration, plasma and reactive species are generated by the field, and a space charge region is generated next to the electrodes. The difference lies in the fact that the sample is now on the electrode, and inside the DC bias field. This field is much larger and more uniform than the one created by placing the sample inside the plasma, and as a result, the energy and the directionality of the impinging ions is greatly increased. Thus the possibility of obtaining a more anisotropic etch is also increased. The lack of ability to independently control local etching parameters remains the same, however.

If the parallel plate etcher is altered by decreasing the size of the sample holding electrode relative to the other electrode, the bias voltage is divided unequally between the two electrodes, with a larger potential drop over the space charge region adjacent to the smaller electrode. In this way, the energy of the ions impinging on the sample is larger, and etches can be designed in which the etching by the reactive radicals occurs only in conjunction with the energetic ion impingements. Usually the voltage range for an unequal parallel plate etcher is 100-500 V, whereas for the equal plate case is only 50-100V. The unequal

plate parallel plate reactive plasma etcher has acquired the name Reactive Ion Etcher (RIE). (Other types of equipment are also called RIE, but people use additional descriptors with this acronym to specify the configuration.) The larger electrode in an RIE does not have to be flat, and is usually made to be the top cover of the chamber. If the ratio of the electrode areas is further increased, the gas inside the chamber is made to be inert, and the RF power is increased to about 1000W, the system is called a sputter etcher, where the material is removed only through the mechanical action of impinging energetic ions

. For the case of the RIE, the ability to independently control etching parameters is not improved over the regular parallel plate etcher. However, this type of equipment is the most widely used of any other dry etching equipment, and many good results for etching semiconductors, dielectrics, polymers, and metals have been achieved with it. Furthermore, when the project began, this was the only type of equipment available on the MIT campus.

As was mentioned earlier, the plasma is produced mostly by ionizing electron-molecule collisions. The pressures, however, are low, and the electron velocities are large, so that the chance of a collision is small before the electron reaches the chamber wall. To increase the effective path length of the electron, and thus increase its chances of collision, magnetic fields can be used. There are many varieties of configurations used for the magnetic field enhanced RIEs. All these provide higher, as well as more independently controlled, plasma densities. The most popular configuration recently is an Electron Cyclotron Resonance (ECR) RIE. Instead of an RF source, a microwave power source is used. The magnetic field strength and distribution is tuned so that a resonance between the linear motion due to the microwave excitation, and tangential motion due to the magnetic field is established. During that resonance, the motion of the electrons becomes circular,

effectively making their path length almost infinite. Thus a much denser plasma is established.

With the ability of obtaining dense plasmas, a downstream RIE configuration became possible. In this configuration, the plasma generation chamber and the sample chamber are separate. Usually, the plasma is generated in a separate chamber above the sample, which is in the etch chamber, and diffuses into the etch chamber. The sample is biased, most commonly with an RF source, so that the ions from the plasma are accelerated towards it. In this configuration, the ability to control the ion energy separately from radical and ion impingement rate is greatly improved. Directionality of the impinging ions is also slightly improved if the distance between the plasma chamber and the sample is increased. In most cases in use now, the plasma is generated by a microwave source. In fact, downstream RIE reactors with an ECR plasma source are becoming an industry standard.

The next logical improvement to the downstream reactor is to collimate the ions that are accelerated by the potential bias into a beam by placing two aligned grids at the output of the plasma chamber. This configuration is called Reactive Ion Beam Etching (RIBE) system. The amount of control over the parameters is about the same as for the downstream RIEs. However, in most of these systems a DC bias is used for the sample, and larger power supplies allow for larger voltages.

In order to separate the kinetic and the chemical components of a dry etch, the Ion Beam Assisted Etching (IBAE) systems have been employed. (These are sometimes called Chemically Assisted Ion Beam Etching (CAIBE) systems.) These are almost identical to RIBE systems, except that the plasma, and consequently the ion beam, is generated from inert molecules, usually argon. The chemically reactive gas is introduced next to the sample not in a plasma form. (If no chemical agent is introduced, the system is called Ion Beam Etching (IBE) system.) Thus the ion beam parameters are separate from the chemi-

cal species density, and ion beam voltage can for most situations be decoupled from the ion beam current. The only disadvantage is that these systems are limited to stable species for the chemical etch component, since they are not generated by plasma. A system that corrects this shortcoming is Reactive Beam/Ion Beam Etching (RBIBE) system, where the etchant gas is first made into a plasma before being introduced to the sample, which as in the IBAE case is being bombarded by an inert ion beam [1].

Regardless of the plasma etching system used, the processes that can determine etch rates and profiles are the same for all the systems. Perhaps the most basic process is the chemical reaction between the gas molecules and radicals, and the substrate. In the absence of any kinetic assistance, the etch rate depends on the reaction rate with, and the availability of, the reactive species. Usually, the reaction rate is sensitive to substrate temperature. The availability of the reactive species depends on the relative pressure of the species, the rate of their consumption, and the ability for them to diffuse. If the etch is reaction rate limited, then addition of extra radicals does not increase the etch rate. If the etch is limited by the reactive agent supply, then increasing their concentration increases the etch rate. Another sign of a supply limited etch is a dependence of the etch rate on the amount of material that is being etched; that is the issue of whether the rate is much higher when the sample is mostly covered by the mask, than when it is mostly open to the etch. Finally, diffusion limited etching happens when the reactive species are exhausted in a small deep hole before a fresh supply can diffuse from the surface. This is manifested in decreasing etch rates with time for small hole patterns. Pure chemical etching is often isotropic, and causes lateral as well as horizontal etching. Sometimes certain crystallographic directions are preferred.

The action of the ion bombardment can have an impact in three ways. The first way is simply sputtering, where atoms of the sample material is knocked away, and gets depos-

ited elsewhere in the chamber. The mask material can also sputter, and has to be chosen carefully, so that the integrity of the pattern remains throughout the etch, and so that the masking material does not get redeposited on the sample where etching is desired. The second action of the ion bombardment is to break the bonds on the sample material to enable or increase the rate of the chemical reactions. The last action that is possible is the removal of the reaction product, if the product is not sufficiently volatile. These reactants are sputtered away. Sometimes, a strong ion assistance is required in the initial stage of the etch to remove the native oxide on the sample. These actions greatly enhance the etch rates, and are responsible for the anisotropic etching since the ions require a line of sight. One exception to this happens when ions rebound off the floor of the etch site, and hit the sidewall, causing some enhanced lateral etching.

Since unstable radicals are formed in the plasma, they can recombine into new molecules. In some cases these new molecules are nonvolatile, and may coat the surfaces of the sample. (In fact, plasma enhanced deposition is a very common way to deposit thin films.) A coating rate begins to compete with the sputtering and etching rates. In many cases, the coating rate on the masking material could be greater than on the sample material, due to the fact that the radicals, instead of having the sample material to combine with and form a volatile product, combine with themselves into nonvolatile species. If the etch parameters are chosen such that the deposition rate is significant on the mask but not on the sample material, then the degradation of the mask is reduced. If the parameters are such that both the ion sputtering and the availability of the reactants (the sample material) for the etchant species are needed for the deposition not to occur (and the etch to continue), then the deposition occurs on the mask material, as well as on the walls of the etched features (glancing angle impact does not exchange much energy). This deposited layer provides

protection to the walls from any lateral etching due to isotropic etching or rebounding ions.

The existence of such a variety of interdependent processes in plasma etching hinders total understanding of a particular etch. The situation is even more complicated by the fact that for most etching systems, all of these processes depend on every etch parameter. For example, in an RIE, if the etching rate of the radicals, not assisted by the ions, is desired, there is no way to obtain it since the reactive species cannot be created without starting a plasma and causing ion bombardment. Some people perform complicated studies of these processes by using in situ time-resolved surface composition analysis or mass spectroscopy of the desorbed species to obtain concentrations of etchants and products. However, such studies require expensive and cumbersome equipment. When applying the results of these studies to another somewhat different etching equipment, they, at best, give just a qualitative understanding of the processes, and not the quantitative relationships between them and the system parameters. Thus extensive empirical studies are required to characterize any new system or any new etch.

3.3 Dry Etching Chemistries for GaAs, InGaP, and InGaAsP

As stated in Section 3.1, one of the goals of this project is to be able to etch smooth vertical walls in InGaAsP/InGaP/GaAs system in one etch. In other words, it was necessary to find an etch that is anisotropic for both InGaP and GaAs under the same conditions. This material system is not widely used, except for a small effort in aluminum-free lasers [25, 27] and for heterojunction bipolar transistor (HBT) development. For HBTs, most of the etches required are ones that etch one layer and stop on another with little damage (e.g., to make contact to the base and collector regions) [43, 79]. Therefore, the etches developed for these devices are not compatible with our goals. For the Al-free lasers, no reports have been published about etching cavity facets or deflectors, and most of the etching is done to

define ridges, which requires etching of only InGaP without emphasis on verticality. Thus, to the best of the author's knowledge, the work done for this thesis is the first attempt to obtain totally vertical deep etching in the InGaP/GaAs heterostructures for laser facets or any other purpose. Thus, in addition to the type of system that would satisfy our requirements, the proper etch chemistry had to be considered. The two most commonly used III-V compound semiconductor material systems are AlGaAs/GaAs and InGaAsP/InP. There have been many attempts to use many different chemistries for either of these material systems. In order to obtain a starting point for the etch chemistry, an investigation was conducted on the etching chemistries that etch GaAs and the chemistries that etch indium containing compounds, with the hope that an overlap could be found.

For the AlGaAs/GaAs material system, the most common etch chemistries are chlorine based. In many systems, especially early in the research effort, chlorine alone was used[37]. It etched GaAs, but for some systems problems were encountered etching AlGaAs, which were attributed to aluminum oxide formation with the residual oxygen and water in the system. This was especially the case for systems with poor vacuum pumps and chambers, and with relatively low ion bombardment energy and rate. Straight chlorine etching of AlGaAs/GaAs remains the state of the art for RIBE and IBAE systems, where together with more energetic ions capable of sputtering some of the aluminum oxides, UHV chambers, cryogenic pumps, and liquid nitrogen cooled traps are used.

For systems where such conditions could not be established, different chlorine based etches were developed. Some of the more successful ones are boron trichloride (BCl_3) [38] and silicon tetrachloride (SiCl_4) [39]. Sometimes these are used together, sometimes alone, and sometimes chlorine is added. These have proved successful in both regular RIE, downstream ECR RIE, and RIBE. Sometimes inert gasses are added to enhance the kinetic effect. Nitrogen and hydrogen are also added to harness their reactivity with oxides

[38]. Fluorine based gasses are also added [80], since aluminum reacts with fluorine radicals.

The most common etching chemistry for InGaAsP/InP is a mixture of methane and hydrogen [40]. For this chemistry, simultaneous etching of the semiconductor and deposition hydrocarbon polymer occur. As long as the methane presence is low, deposition occurs only on the mask material. However, if it is too high, the etch rate drastically decreases. In some cases, a small amount of oxygen is introduced, whose radicals react with hydrocarbons. Inert gases are also added to increase the ion bombardment to chemical reaction ratio [42, 81]. In some cases chlorine is also added [41]. This chemistry has been used in both RIE, ECR RIE, and RIBE systems.

There is some overlap in the etching chemistries for these material systems. There are some cases where the chlorine based chemistries were used to etch indium containing compounds. Both chlorine [45] and BCl_3 [82] were used for this purpose. However, these systems required elevated temperatures to efficiently remove indium chloride reaction products from the surface. In some cases etching was done at room temperature, but where large ion and radical densities were used, since an ECR RIE system was used at 1000 W of microwave power [82]. There are also reports of CH_4/H_2 RIE systems etching GaAs, though with low rates. However, for both cases of chlorine and methane, different conditions were used to etch InP than to etch GaAs. Furthermore, the sidewall profile was not mentioned in these reports. This does indicate that finding a single set of conditions that is optimized for both GaAs and InGaP would require a considerable effort. Initial attempts to etch GaAs with CH_4/H_2 in an RIE, and InP with Cl_2 in an ECR RIE produced very poor results. There are other less established chemistries, involving the other two halogens, bromine and iodine, that were reported to be successful [46]. The different gases used were HBr, HI, BrI_3 , and Br_2 .

Upon investigation of different systems and chemistries that are used for compound semiconductor etching, one conclusion was made: most of the recent success in etching optical mirrors was accomplished with either RIBE or IBAE systems. A chlorine ECR IBAE system at the MIT Lincoln Laboratory, which was very successful in AlGaAs/GaAs IPSEL fabrication [34], was available to us. Therefore, even though attempts at using a regular RIE were made (the campus ECR RIE system was not in place at the time), a more concentrated effort of developing an etch in this IBAE system was initiated.

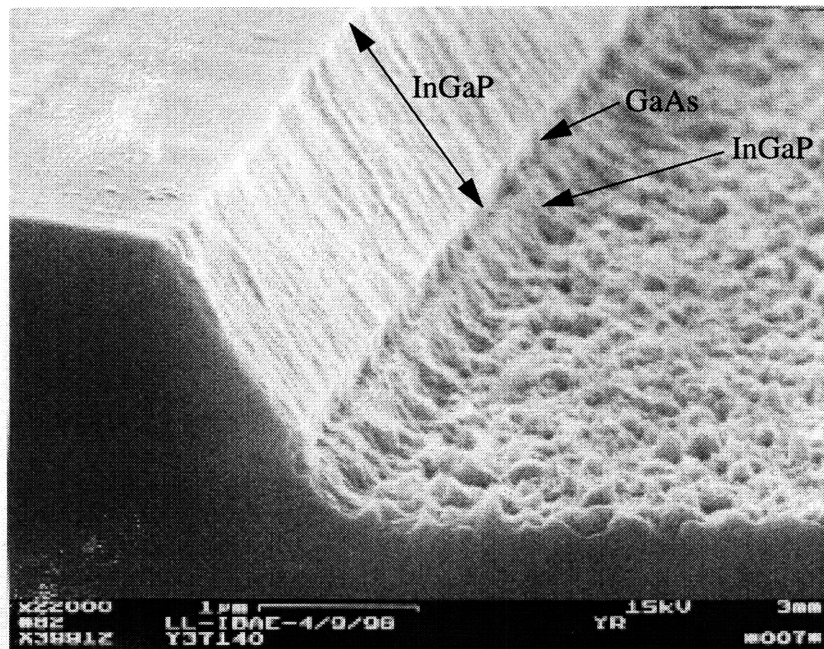


Figure 3.1: Non-optimal chlorine ECR IBAE etch of InGaP/GaAs heterostructure (MIT R417 - 500 V, 40 $\mu\text{A}/\text{cm}^2$, 175°C, 3 sccm Cl_2).

The chlorine IBAE system at Lincoln Laboratory is the same system used for some of the polycrystalline material stripping in the E-o-E process flow described in Chapter 2. It consists of mostly UHV chamber components, and is pumped by a cryogenic pump. It can achieve a background pressure of 3×10^{-8} Torr. To generate a plasma, 3 sccm of argon is

flowed through the plasma chamber. About 400W of 2.45 GHz microwave energy is introduced into the chamber via a waveguide connected to a magnetron microwave generator. Tuning of the waveguide is performed to minimize reflections and to ensure that all of the power is delivered into the plasma. Then the currents in the two electrostatic magnets around the plasma chamber are tuned to establish electron-cyclotron resonance inside the plasma chamber. The ion beam is established with a DC high voltage source and two grids. The ion beam voltage used was always 500 V. With proper tuning, a beam current density of $40 \mu\text{A}/\text{cm}^2$ was obtained, as measured by a Faraday cup. The beam was neutralized by a hollow cathode neutralizer. Chlorine was introduced to the system via a perforated stainless steel ring, which was about 3cm away from the sample. The sample was clipped to a heated stainless steel flat.

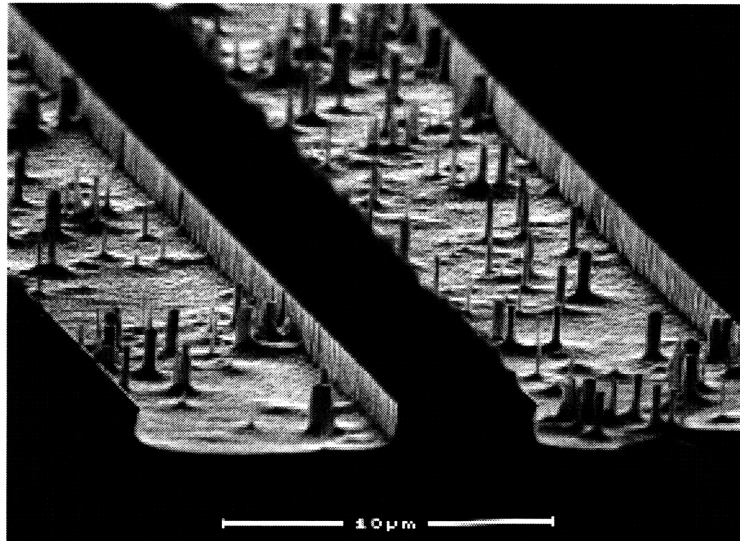


Figure 3.2: Optimal chlorine ECR IBAE etch of InGaP (500 V, $40 \mu\text{A}/\text{cm}^2$, 175°C , 9 sccm Cl_2).

Keeping the ion beam parameters as stated above the same (beam voltage 500 V and beam current $40 \mu\text{A}/\text{cm}^2$), the temperature and chlorine flow were changed to obtain a

good etch profile in $\text{In}_{0.49}\text{Ga}_{0.51}\text{P}$, masked by SiO_x patterned by wet etching. Up to 150°C , the etch was very rough, and the profiles were not straight. At low chlorine flows and higher temperatures, the profile was not straight, but rather followed a crystallographic plane. For example, in Figure 3.1, a slanting profile resulting from a low chlorine flow is shown. An etch with an optimized temperature, 175°C , and chlorine flow, 9 sccm, is shown in Figure 3.2. At these parameters, the roughness almost disappears, and the walls became straight, even to the point that micromasked (unintentional specks of residue acting as an etch mask) columns of less than $0.3\ \mu\text{m}$ in diameter, and about $4\ \mu\text{m}$ in height appeared straight. Then an InGaP/GaAs heterostructure, consisting of $0.7\ \mu\text{m}$ of InGaP, $0.6\ \mu\text{m}$ of GaAs, $0.7\ \mu\text{m}$ of InGaP, and $0.2\ \mu\text{m}$ of GaAs grown in that order on a GaAs substrate, was etched at 175°C . An SEM micrograph of the etch profile is shown in Figure 3.3. The masking material is mostly sputtered away in this sample, and some deterioration of the top GaAs has occurred. However, in the profile of the top layer of the heterostructure, it is visible that the InGaP etch is very straight and anisotropic. Gallium arsenide, on the other hand, has a very strong spontaneous isotropic etching component. Even at a much lower chlorine flow, there is considerable spontaneous etching of GaAs, as can be seen in Figure 3.1. Thus chlorine IBAE does not seem to be the right choice for facet etching in InGaP/GaAs lasers.

The reason for chlorine being a poor choice can be understood by looking at the vapor pressures of the reaction products on indium, gallium, arsenic, and phosphorus with chlorine. Since the chlorine flow rate and the ion beam current and voltage are high, the reaction rate is limited by the desorption rate of the reactant products, which is proportional to the vapor pressure of the compound. As can be seen from Figure 3.4a, the vapor pressures of indium chlorides (compared at the same temperature) are much lower than those of the chlorides of the other three elements. (In fact comparison of only the chlorides of the fam-

ily III elements is sufficient, since the vapor pressures of family V chlorides are high.) Thus, higher temperatures are need to increase the vapor pressure, and thus the desorption, of the indium chlorides in order to establish proper etching conditions for InGaP. At these temperatures, however, the vapor pressure of gallium chlorides is so high that the reaction is not limited by desorption, and the chlorine spontaneous etching rate, also high at these temperatures, creates the lateral etching. One thing to notice, however, is that the ion beam assisted etch rate is still at least more than an order of magnitude higher that the spontaneous rate, and thus this etch can be useful for applications without critical features and wall profiles, such as polycrystalline material stripping step in the E-o-E process (Section 2.4).

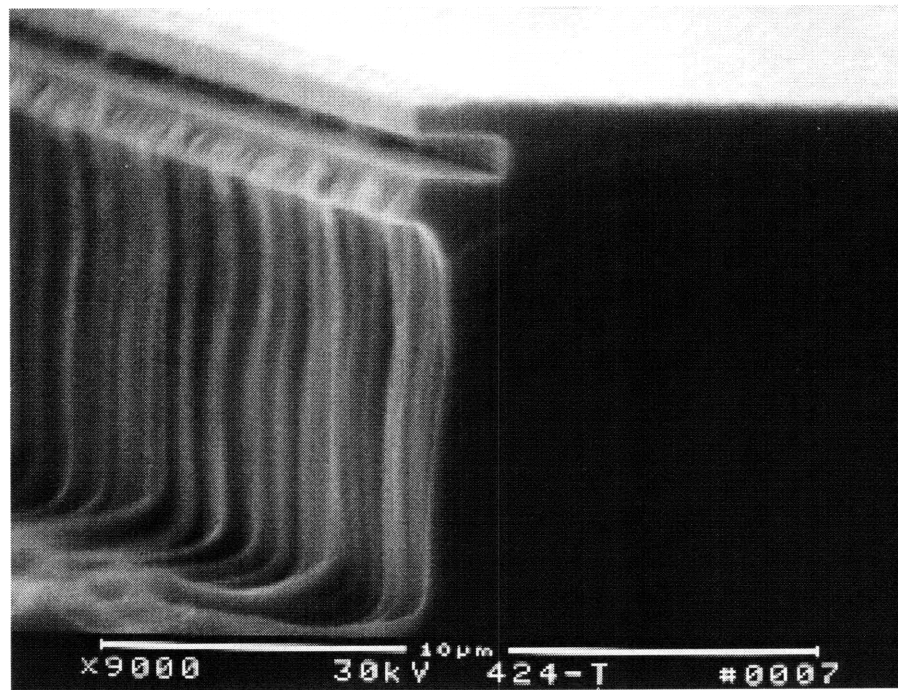


Figure 3.3: InGaP/GaAs heterostructure etched in a chlorine IBAE system at 175°C.

Upon examination of vapor pressure data for the bromides of indium, gallium, arsenic, and phosphorus, Figure 3.4b, it was discovered that they are much closer than those for the chlorides. This is especially so for the vapor pressure of InBr_3 , which is the dominant by-

product, and gallium bromides. For this reason, bromine based etching was chosen. Incidentally, as seen in Figure 3.4c, the vapor pressures of the iodides for gallium and indium are even farther apart than for chlorine, and bromine. Among the few options of simple bromine containing substances, pure bromine was chosen. Hydrogen bromide was not as attractive because of the poor hydrogen pumping ability of cryogenic pumps. The other choice, BrI_3 , was hard to obtain, and is not stable at room temperature. Bromine, however, is a liquid, and is readily available in electronic grade purity at most suppliers. Thus, even though no reports of this technique was reported in the literature, IBAE etching of III-V semiconductors with bromine was investigated.

3.4 Kaufman Source Ion Beam Assisted Etching System

For the reasons described in Section 3.3, a bromine ion beam assisted etching system was chosen for the development of InGaP/GaAs laser facet etching. Bromine could not be added to the ECR IBAE system that proved successful for chlorine etching of AlGaAs/GaAs lasers, due to fear of contamination. Therefore, another system was assembled, dedicated for bromine etching. In this section, this system will be described in detail. Principles of operation of such a system will also be described. Finally, inconsistencies in the mode of operation will be mentioned. Suggestions for possible improvements on the system to reduce the inconsistencies will be outlined in Section 5.3. The current standard operating procedures and maintenance routines developed for this system are detailed in Appendix B.

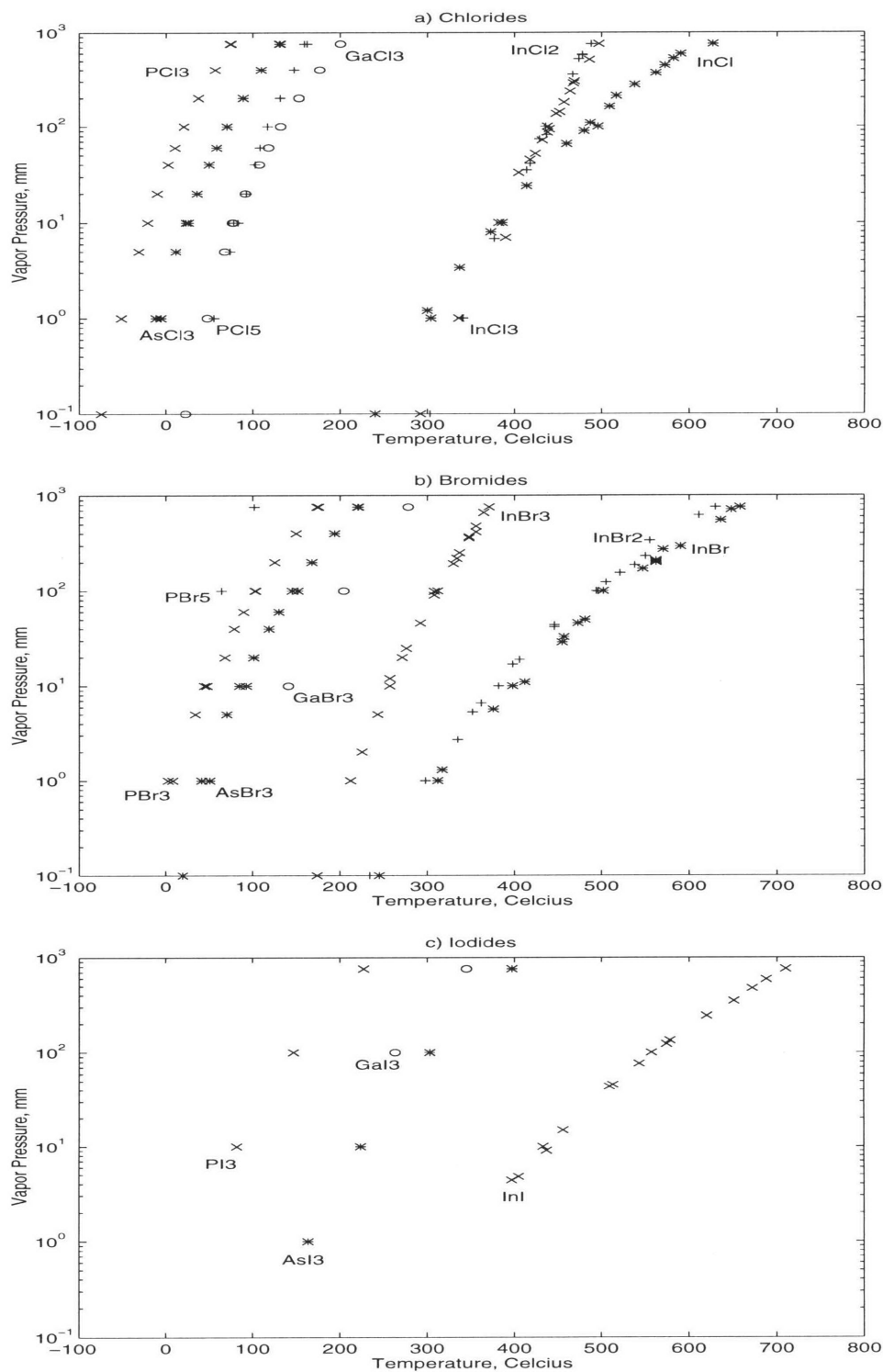


Figure 3.4: Vapor pressures at various temperatures for chlorides, bromides, and iodides of arsenic, indium, gallium, and phosphorous [47, 48, 49].

The whole system is shown in schematic form in Figure 3.5. The system chamber consists of standard Ultra High Vacuum (UHV) components made of welded stainless steel. Most of the ports to the chamber are sealed with copper gaskets and knife edged flanges. Most of the gas lines are made of stainless steel and are joined with VCR gaskets. However, some of the ports are sealed with Viton o-rings, and the argon gas line input is plastic, joined with a Swagelock connector, both of which are incompatible with UHV practice. The system is pumped by a cryogenic pump. The exhaust of the pump is fitted with a o-ring pop-out valve, which is also inconsistent with UHV practice. The chamber is equipped with coil shaped cold trap through which liquid nitrogen can flow to further enhance the pumping, but it was not used. The chamber background pressure before introduction of bromine was 1.4×10^{-8} Torr. After introduction of bromine to the system, pressures of $3-4 \times 10^{-8}$ Torr have been achieved consistently for almost a year.

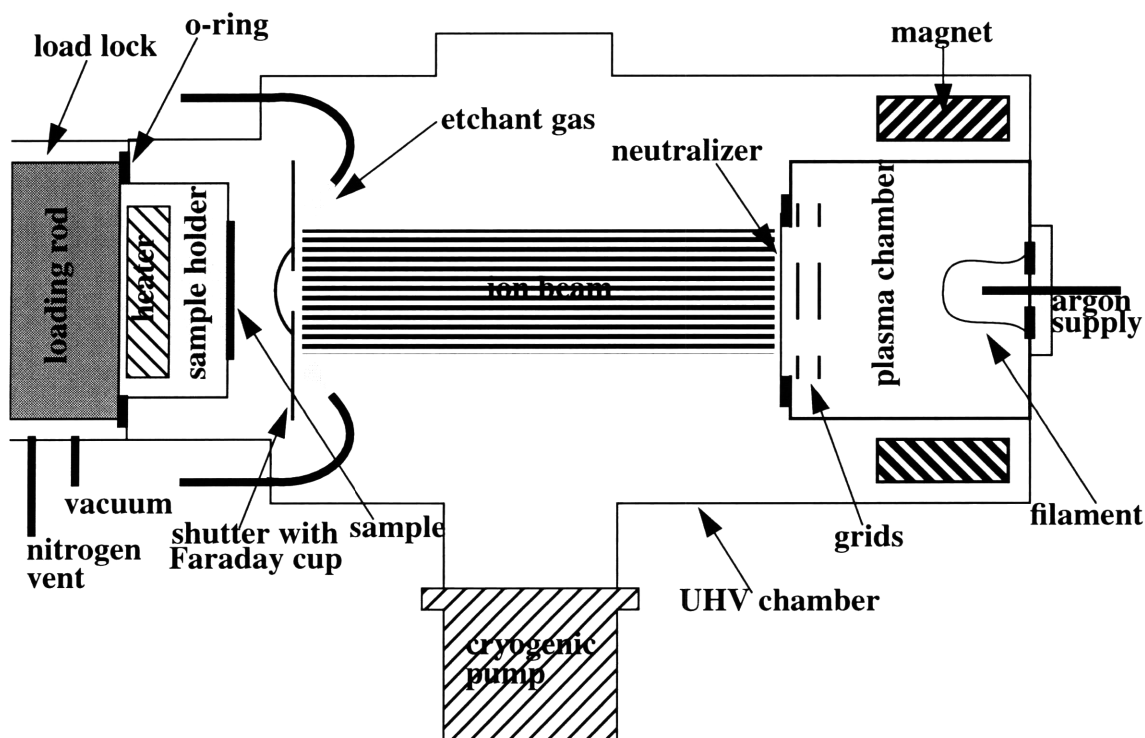


Figure 3.5: Kaufman gun ion-beam assisted etching (IBAE) system schematic.

The main part of the chamber is in the form of a cylinder. At one end of the cylinder is the gun assembly. At the other end is a flange with a 3" diameter tube, which acts as a loadlock. The flange is blocked off by a gate valve. Inside the tube grooves are cut, and square o-rings are fitted within the grooves. A substrate holder is attached to an anodized aluminum rod, which forms a vacuum seal with the square o-rings when inserted inside the tube. After the insertion, the volume of the tube is pumped out by a mechanical pump. Then the gate valve is opened and the tube is pushed further inside the chamber, until another o-ring, fitted on the lip on the rod, is pressed against another lip inside the chamber, thus forming a vacuum seal. Even with the loading mechanism in, the chamber can pump down to $3-4 \times 10^{-8}$ Torr. Just in front of the sample holder there is a shutter, which blocks it from the ion beam and the direct gas flow. Finally, the sample holder is fitted with a heater and two thermocouples, which are not on the vacuum side.

For this system, three different etchant gas channels are available. Each gas is introduced by two nozzles on two sides of the sample holder. Only bromine has been used on this machine. Since bromine is liquid at room temperature, it is stored in a glass bottle. The bottle is fitted with a stopper and a glass tube, which in turn is connected to stainless steel tubing. When the stopper of the bottle is open, the flow of the bromine is controlled by a leak valve, with a numeric dial. A mass flow controller was not used because it was expected that it would become clogged. The bromine reservoir, as well as the tubing it is connected to, are fitted with heaters, since bromine is liquid. However, the heaters were not used, since the flow was always more than sufficient without them, and no clogging of the lines was observed.

For a specific setting, the leak valve did not produce reproducible flows, so the flow has to be monitored before the run commences in order to obtain consistent flows from run to run. This is accomplished by putting another nozzle in front of one of the bromine out-

lets, so that it captures most of its flow. This nozzle was connected to an absolute pressure transducer (Baratron), in which a change in capacitance of a membrane due to its flexion resulting from a pressure change gives a relative indication of the flow. This approach allows us to make an indirect measurement of the bromine flow. During the etching, however, the Baratron nozzle is moved back from the gas outlets. Because there is no feedback control over the flow, it is checked a few times during an etch. This method of flow measurement produces inconsistencies, stemming primarily from the inconsistency of alignment of the bromine outlet and the Baratron inlet nozzles. Even with careful alignment 5% error can occur just from differences in alignment.

The ion beam source [50] is on the other side of the main part of the chamber from the sample, about 0.5 meters away. It consists of the plasma chamber, the extraction grids, and the neutralizer. In the plasma chamber, an inlet of argon is situated next to a 0.25 mm tungsten filament. An AC current is applied to the filament heating it. A DC discharge voltage is applied between the anode in the chamber and the filament, which acts as the cathode. The chamber walls themselves are left electrically floating. This voltage discharges electrons from the heated filament. The electrons discharged from the cathode filament are highly energetic, and can ionize the argon atoms in the chamber upon collision, creating positive ions and low-energy electrons, which constitute the plasma. The plasma is conductive, so there are very minor potential variations across it, and it is very close to the anode potential. The pressure in the chamber is fairly low, usually in the 10^{-4} Torr range, and the discharged electrons are so energetic, that most reach the chamber walls and the anode without colliding with the neutral atoms. In order to increase the effective path length of the electrons, a magnetic field is introduced by a permanent magnet, which prevents high velocity electrons from moving in a straight line. The low-energy electrons are

not greatly affected by the magnetic field, and their diffusion to the anode completes the cathode-anode current.

An ability to get a denser plasma is usually desirable. In order to achieve higher ion concentration, two things can be done: increasing the number of atoms in the chamber and increasing the number of high-energy electrons emitted from the filament. Thus increasing the flow or the pressure (a more fundamental parameter) increases the number of ions available. Eventually, the ion concentration saturates, and an optimal pressure occurs just before this saturation. In the present system, for all of the experiments, a 3 sccm flow of argon was used. This corresponded to 2.3×10^{-4} Torr in the main chamber, with a slightly higher value possible for the plasma chamber due to the proximity of the gas inlet. This is consistent with the 10^{-4} - 10^{-3} Torr range usually quoted in the literature. The ions generated in the plasma chamber are not just argon ions. Since the pressure is very low, there is very little probability that the etchant gas molecules collide with the argon molecules and ions when the etchant ions diffuse from the main chamber. Thus there is always some concentration of bromine ions in the plasma, and different combinations of low and high-energy, neutral and charged, diatomic and monoatomic bromine molecules reach the sample.

The most effective way to increase the number of electrons emitted from the cathode filament is to increase the heating current. Increasing the discharge voltage will also increase the emission. A limit to increasing the cathode current is the possibility of burning it out. Furthermore, a space charge layer of electrons can accumulate around the filament, preventing more electrons from escaping. This limit can be postponed, by increasing the discharge voltage and the chamber pressure. There is a danger in increasing the discharge voltage and the filament emission too much. As the discharge voltage between the cathode and the anode is increased, the electrons become more energetic. An

electron can acquire enough energy to doubly ionize an atom. Double ionization can occur also by consecutive collisions of an atom with two electrons, which become more probable with higher cathode emissions. Doubly ionized ions will have twice as much energy of impact on the sample, causing extra damage, without providing extra assistance to the etch. Additionally, they give a false reading of the ion emission rate, since it no longer has the same proportionality to the ion beam current.

The positive ions in the plasma chamber are extracted by applying a DC voltage, called the beam voltage, between the anode (which is very close to the plasma potential) and ground. The system body and the sample are at ground, and the ions are accelerated towards it. Thus, the beam voltage directly determines the ion energy and to some degree determines the number of ions extracted. For the present system, the maximum beam voltage is 1500 V, but voltages between 500 - 1000 V were used in this study, with 500V and 600 V being the most common. Like any plasma, the ions extracted have a fairly constant potential due to the mobility of the charged particles. And as with any plasma, the electrons that escape with it are much faster than the ions, and as a result a space charge is formed around the sample, so that the plasma is at a slightly more positive potential than ground. As the ions travel towards the sample, some of them exchange charge with low energy neutral atoms. In this way, high energy neutral particles are created, which could further generate misleading ion beam current readings. For this reason, the minimum acceptable pressure in the chamber should be used to minimize this effect.

Two closely spaced carbon grids, placed such that the holes are aligned, are responsible for collimating the ions extracted from the plasma into a beam. The first grid is electrically floating, and therefore is close to the anode and plasma potentials. The second grid, called the accelerator grid, is biased negative in respect to ground by an accelerator voltage supply, so that the ions inside see an accelerating potential, V_t , which is the sum of the

accelerator and the beam voltages. Therefore, the extraction of the ions from the chamber is related to this sum of voltages, and not only on the beam voltage. In fact the ion beam current is proportional to the $V_t^{3/2}$. The beam energy, however, remains being determined by the beam voltage, since the ions after going through the grid decelerate back to the beam voltage potential. Perhaps even more important than the enhanced ion extraction, the accelerator voltage provides a barrier for the electrons created by the neutralizer, keeping them from entering the plasma chamber. The accelerator voltage is usually chosen to be about 10-20% of the ion beam voltage, but in present work the accelerator voltage was held constant at 60 V, regardless of the beam voltage used. Excessive accelerator voltage will result in ion bombardment of the accelerator grid. This ion bombardment can be monitored by the current flow increase through the accelerator voltage supply, and should be avoided.

In addition to the effect of the grids, the divergence of the beam is also determined by the electrostatic repulsion of the ions in the beam. Thus, the denser the beam, the more the ions repel each other, and the more the spreading. This is particularly important when the ion energy is not large. In order to eliminate this cause of beam spreading, neutralization is necessary. In our system, neutralization is done by electron emission from a heated tungsten filament. The emitted electrons are very mobile, and spread themselves along the beam. Most of them do not recombine with the ions, however.

The beam current density is an important etching parameter, and it is important to be able to measure it accurately. There are two ways to get information about the beam current. One is to measure the current flowing through the beam voltage supply. Then, by estimating the area of the beam, the density can be calculated. Another method for measuring the beam current is by having a shielded probe in the path of the beam, with a known size aperture. The charge arriving at the probe surface generates a current under

closed circuit conditions, which can be measured. Since the area of the aperture is known, the current density can be obtained. Both of these methods have inherent inaccuracies in terms of estimating the rate of energetic particle arrival at the sample due to beam nonuniformity and doubly ionized ions. The probe method is also affected by the charge exchange phenomena, where energetic uncharged particles bombarding the surface are not measured. In our case, both methods were used to monitor the beam current density. The current measurement and display was included in the beam voltage power supply. A Faraday cup was used as the current probe, and was attached behind the sample shutter, with 1 cm² aperture opened in the shutter.

With the equipment and some of its physics described above, the method of the operation will be summarized. An etching run starts with the sample loaded in the chamber and the chamber pumped to mid 10⁻⁸ Torr range. A shutter is in place between the sample, and the soon to be established ion beam and bromine flow. First the argon flow is established. It is always 3 sccm, which produces 2.3x10⁻⁴ Torr in the main chamber. First, the plasma is established by supplying the discharge voltage between the cathode and anode, and supplying a heating current to the cathode filament. By applying the beam voltage between the anode and ground, and the accelerator voltage between the accelerator grid and ground, the ions in the plasma are extracted into a beam. A heating current is applied to the neutralizer filament, and the emitted electrons neutralize the beam. The beam current density is measured by the Faraday cup on the shutter. All the supplies are on the same Iontech power supply panel. There is a possibility of controlling the beam parameters automatically, but manual operation is generally used. Discharge and accelerator voltages are always kept constant at 60 V. Beam voltage is selected according to the run. The cathode filament current is then tuned to obtain the maximum reading of current density, as measured by the Faraday cup. The current through the beam voltage supply for this maxi-

imum is noted, and is kept constant during the etch, when the shutter is open, and the Faraday cup is outside the beam. The neutralizer current is turned up until the current reading through the Faraday cup is almost zero. By this time, the sample temperature is stable. At this point, a two minute ion beam clean is performed to remove any residue on the surface. After the clean, the shutter is closed again, and bromine flow is established. When bromine is flowing, the emission efficiency of the neutralizer filament is drastically reduced, and therefore the neutralizer current is increased at this point. Finally, the etch can commence by opening the shutter. During the etch, the bromine flow, the sample temperature, and the current through the beam voltage supply are monitored, and kept constant.

3.5 GaAs and InP Etching Study

As mentioned earlier in this chapter, dry etching is very complicated, with many different processes and parameters, all interdependent. It is very difficult to obtain a complete quantitative model for an etch, as it is difficult to make accurate measurements of physical parameters for such a model. Thus, most of dry etching fabrication steps are developed and optimized empirically. In the present case, since no other reports of bromine IBAE etching were published, it is even more important to thoroughly characterize the system. To accomplish this, a study of the etch rates and sidewall profiles in GaAs and InP as a function of temperature, ion beam current density, and bromine flow was carried out. Binary compounds are simpler to analyze with a qualitative model, more consistent in quality, less expensive, and readily available. For the laser facet etch optimization, the same study should also be carried out on InGaP, but this was not possible due to material unavailability. Consequently, the trends noted for InP are assumed to be similar for InGaP, though the exact numbers are expected to vary significantly.

The first set of studies was done to determine the etch rate dependence on the substrate temperature. This was done with an ion beam energy of 500 V, ion beam current density of

40 $\mu\text{A}/\text{cm}^2$, and relative bromine pressure of 5.5 mTorr. The temperature was varied from 20°C to 200°C. These etch rates were compared with the spontaneous etch rates without the ion beam. The results are shown in Figure 3.6. The spontaneous etch rate curve seems to resemble an Arrhenius equation, with the activation energy not varying more than a factor of two over the whole temperature range. The activation energy variation could be due to the etch rate being dependent on factors other than reaction rates, such as reactant diffusion. A more likely explanation would be the error in the etch depth measurement. Of course, the etch rate for both materials does not depend on a single chemical reaction, but rather on several. Throughout the whole temperature range, the GaAs spontaneous etch rate is higher than that of InP.

The ion beam assisted etch rate dependence on temperature does not follow a simple relation. There are regions in the curves for both GaAs and InP, where an increase in the temperature increases the rate, and there are saturation regions where the temperature has less of an effect. The saturation regions indicate that at some temperatures, the etch rate is not as dependent on the reaction rate, or even reaction product volatility, but rather on the ion current density and bromine concentration. The InP curve has the even more interesting feature of a sudden increase of the etch rate between 150°C and 180°C, indicating a change in the dominant reaction. At this point, the InP etch rate surpasses that of GaAs. This is promising for our purpose, since etch conditions where both InGaP and GaAs have equal rates is ideal. However, for these temperatures, the spontaneous etch rates are substantial enough to make this operating point not useful for the purpose of facet etching. In addition to ion beam assisted and pure chemical etch rates, the sputtering rates, with just the ion beam without bromine, were obtained. The sputtering rates are 6 nm/min and 3 nm/min for GaAs and InP, respectively. These rates were approximately the same at both 20°C and 200°C, as expected. It is worthwhile to note the classic characteristic of kineti-

cally assisted etching, where the sum of the sputtering and chemical rates is much smaller than the ion assisted etch rates.

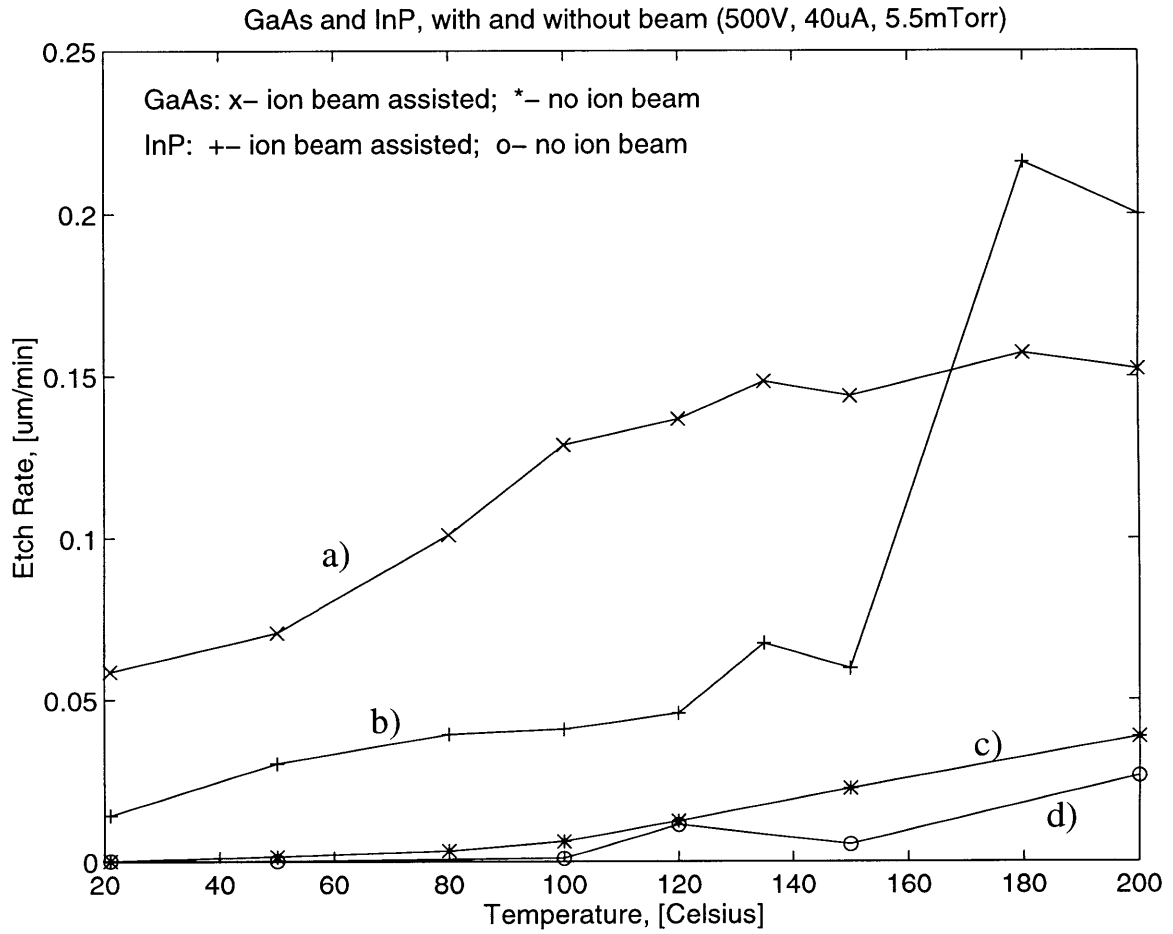


Figure 3.6: Etch rate dependence on temperature in the Br_2 IBAE system with 500 V, 40 $\mu\text{A}/\text{cm}^2$ ion beam and 5.5 mTorr Br_2 pressure for a) GaAs with ion beam, b) InP with ion beam, c) GaAs without beam, and d) InP without beam.

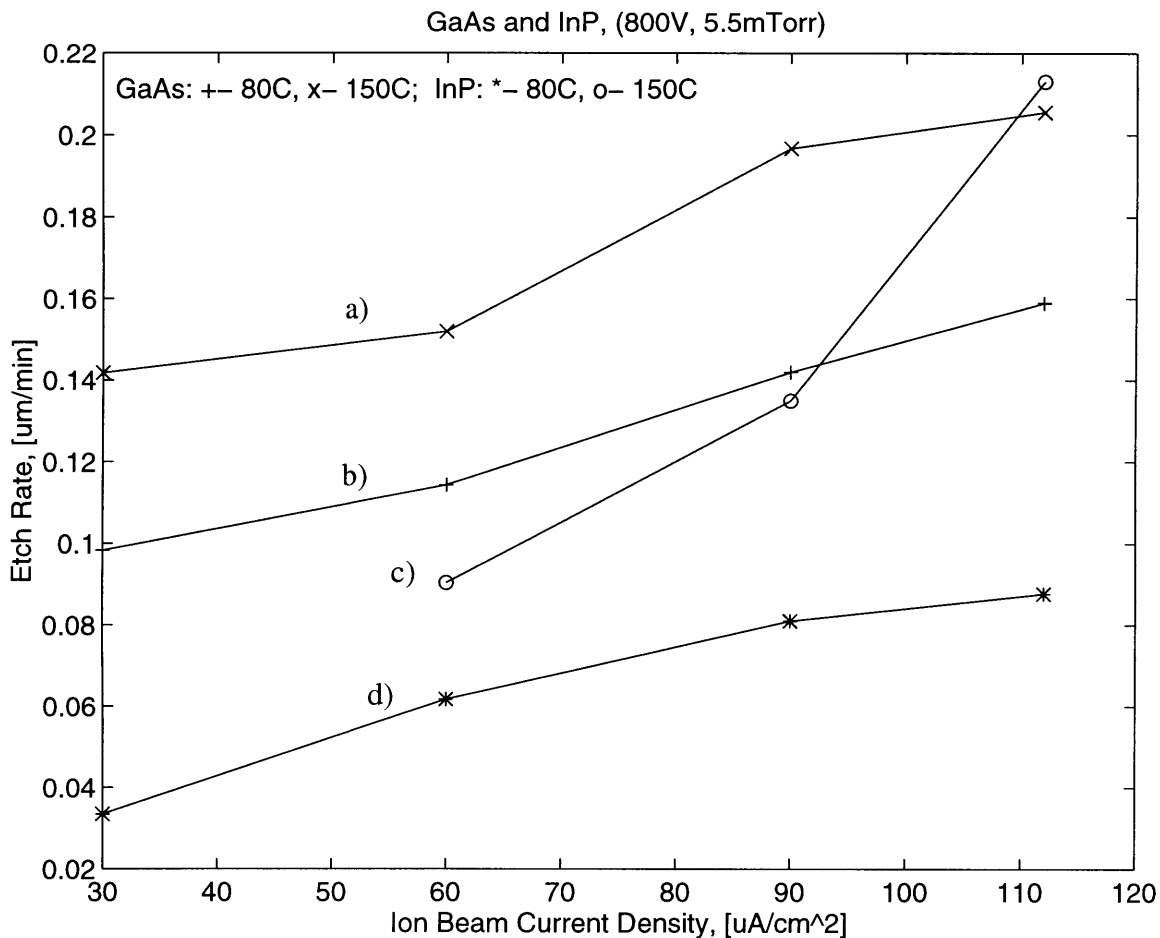


Figure 3.7: Etch rate dependence on ion beam current density in the Br_2 IBAE system with 800 V ion beam and 5.5 mTorr Br_2 pressure for a) GaAs at 150°C, b) GaAs at 80°C, c) InP at 150°C, and d) GaAs at 80°C.

The etch rate data as a function of ion beam current density is shown in Figure 3.7 for two substrate temperatures, 80°C and 150°C. The ion beam energy here is increased to 800 V to obtain a greater range of current densities, and the bromine pressure is kept constant at 5.5 mTorr. The current density is varied between 30 $\mu\text{A}/\text{cm}^2$ and 112 $\mu\text{A}/\text{cm}^2$. In all of the cases, the etch rate monotonically increases with the current density. However, except for high temperature InP, there is a relatively weak dependence on the beam density, where quadrupling the current density only doubles the etch rate. At 150°C, InP etch

rate increases sharply with the beam current. Perhaps, this could be due to the combined effect of the more efficient sputtering of the indium bromides and the enhancement of the InP etch rate around that temperature seen in Figure 3.6b.

The results of the bromine pressure on the etch rates are shown in Figure 3.8. For this study the substrate temperature was kept at 150°C, and the beam parameters at 800 V and 60 $\mu\text{A}/\text{cm}^2$. The etch rate is not effected significantly by the bromine pressure, and quadrupling the pressure only doubles the etch rate. The increase, however, implies that the etching done for the temperature and current density studies was probably somewhat bromine deficient. Bromine deficiency might be an explanation for the etch rate saturation effects as a function of temperature and beam density, seen in Figures 3.6a, 3.7a, and 3.7d, since then the etch rates would depend more on the bromine supply. No hypothesis exists for the decrease in the etch rate at higher bromine pressure. There is a possibility that the high bromine concentration affects the emissivity of the filaments in the ion beam source, reducing the ion beam current density. This decrease would not be noticed by the operator since the density is measured only before introduction of bromine into the system. The fact that the InP etch rate drops much faster than for GaAs would support this hypothesis,

since at this temperature, InP is much more sensitive to the beam current density than GaAs, as can be seen in Figures 3.7a and 3.7c.

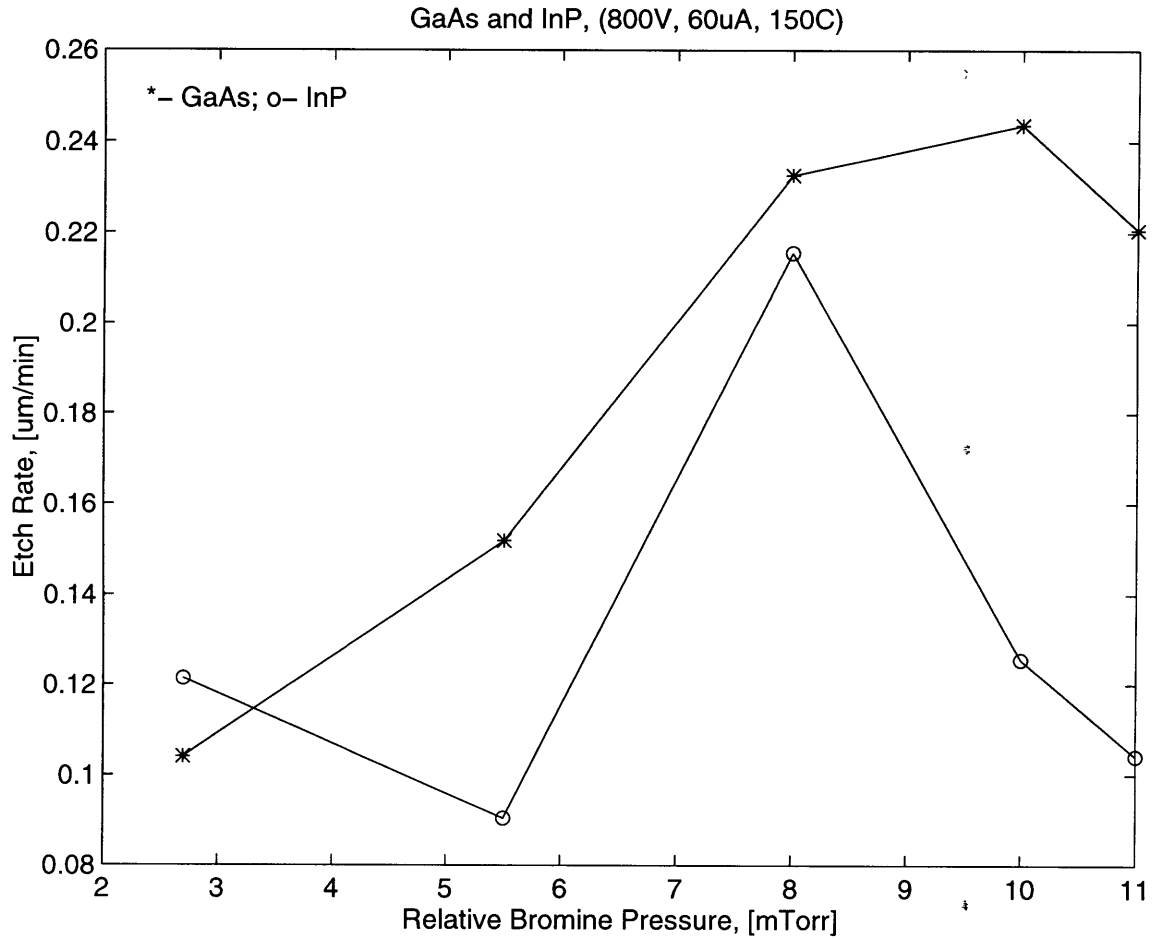
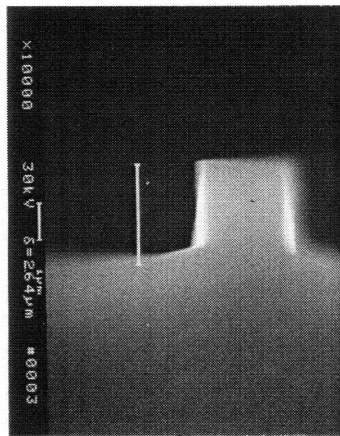
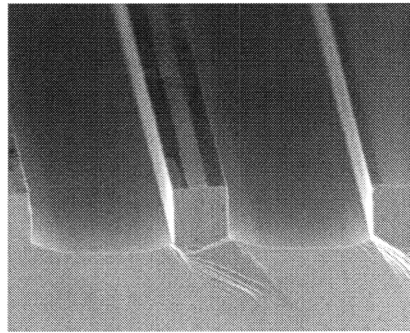


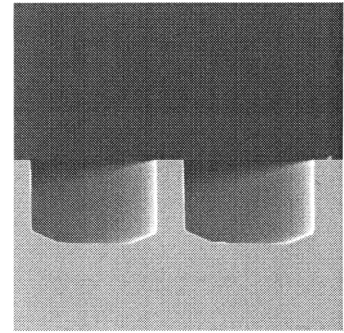
Figure 3.8: Etch rate dependence on bromine pressure in the Br_2 IBAE system with 800 V, $60 \mu\text{A}/\text{cm}^2$ ion beam and 150°C substrate temperature for a) GaAs and b) InP.



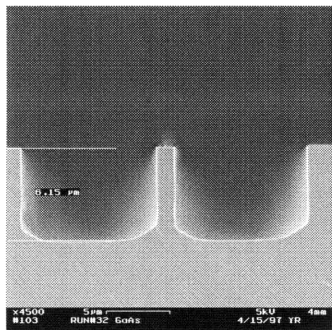
a) 20°C



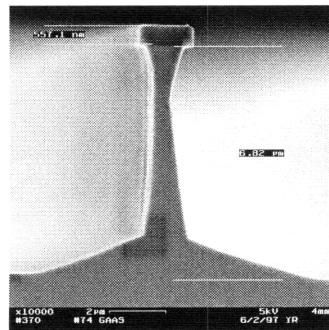
b) 80°C



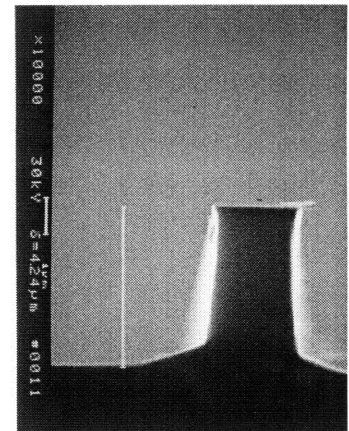
c) 100°C



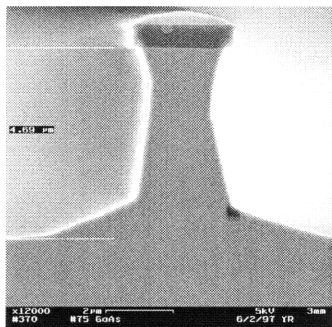
d) 120°C



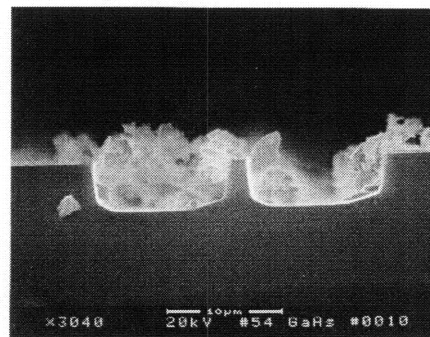
e) 135°C



f) 150°C



g) 180°C



h) 200°C

Figure 3.9: Sidewall profiles of GaAs etched in the Br₂ IBAE system with 500 V, 40 μA/cm² ion beam and 5.5 mTorr Br₂ pressure at different temperatures.

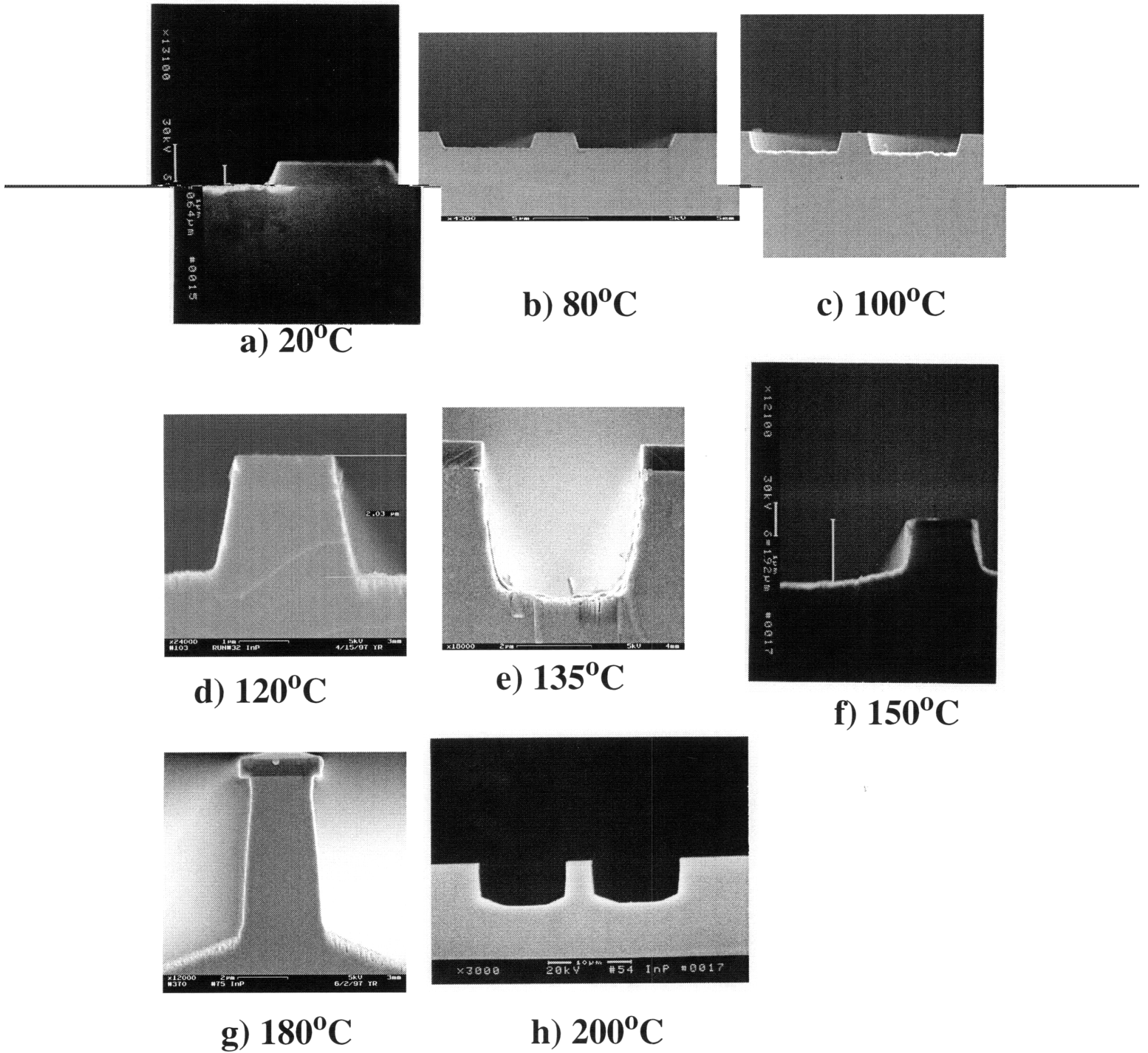


Figure 3.10: Sidewall profiles of InP etched in the Br₂ IBAE system with 500 V, 40 μA/cm² ion beam and 5.5 mTorr Br₂ pressure at different temperatures.

Even more important for our purpose than the etch rate dependence on the etch parameters, are the sidewall profiles. The etch profiles at temperatures between 20°C and 200°C are shown in Figure 3.9 for GaAs, and in Figure 3.10 for InP. The ion beam and bromine flow parameters were kept constant for all of the samples. Though at room temperature, the GaAs profile is slightly slanted, by 50°C, the walls are straight. Hardly noticeable undercutting begins somewhere between 100°C and 120°C. More noticeable undercutting starts to occur just under 135°C. Thus a substantial temperature window (i.e. 50-120°C) exists for purely vertical etching of GaAs. Even for the 200°C etch, the spontaneous etch component is not severe, as compared to the 175°C chlorine IBAE case in Figure 3.3. However, as indicated on the plot of Figure 3.6a, the etch rate does not increase past 135°C for these beam and bromine flow conditions. Thus, an optimal etch in terms of the sidewall profile and etch rate is possible somewhere between 100°C and 135°C.

For InP the sidewall profile is slanted until somewhere between 135°C and 150°C. Soon after that range, noticeable undercutting begins. Thus the optimal etch temperature window is much smaller than for GaAs. Just as for GaAs, however, the undercutting is not severe, since the spontaneous etch rate is at least an order of magnitude smaller than the ion beam assisted etch rate, as can be seen in Figure 3.6. Thus, this etch can be used for purposes where sidewall profile and pattern reproduction requirements are slightly reduced.

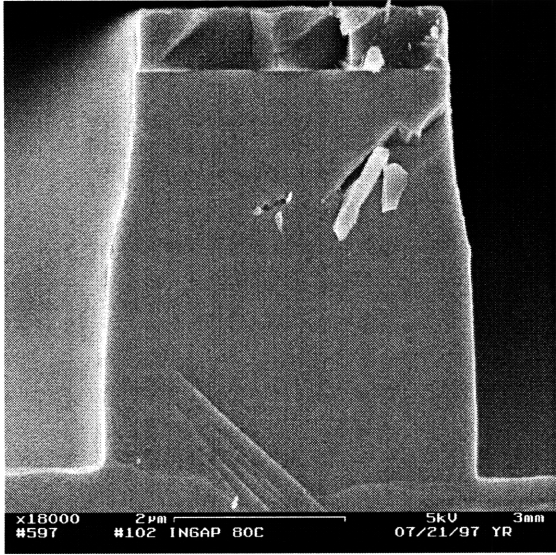
3.6 Heterojunction Etching Study

A full empirical etch study, as the one done for GaAs and InP, could not be done with InGaP or with more complicated heteroepitaxial layers due to the limited material availability. Nevertheless, etch optimization was done on heterostructures. First, a structure with just InGaP grown on top of GaAs substrate was used. The layer was originally grown for doping and lattice matching calibration, and consisted of 2 μm thick p-type InGaP.

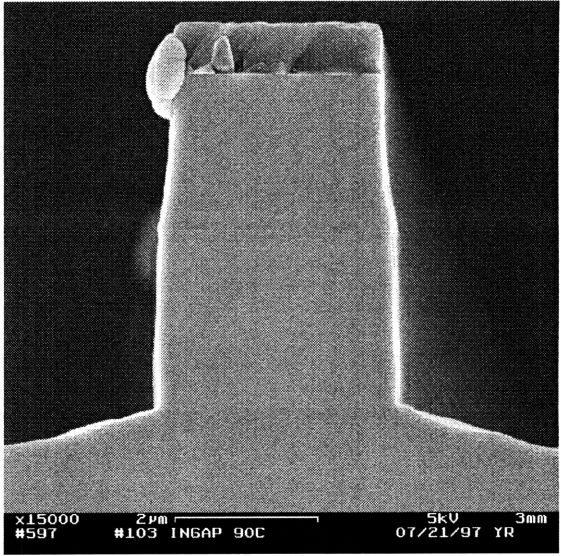
Examining the results of the GaAs/InP etch study, it was decided that temperature is the most critical parameter, so a few etches were done, where the temperature was changed, but the other parameters were held constant. It was decided that an increase in the beam current density would improve the etching, and $60 \mu\text{A}/\text{cm}^2$ was chosen. To minimize damage and the ion ricochet effect, the beam energy was kept to the minimum, so 600 V was chosen, which is just enough to obtain $60 \mu\text{A}/\text{cm}^2$. Finally, the bromine pressure was increased slightly to 6.0 mTorr. Further increase was not thought necessary since the temperatures would be lower than the 150°C used to obtain the data in Figure 3.8. Furthermore, an increase in the bromine concentration was thought to increase GaAs spontaneous etch rate and to reduce filament performance and life. An example of some of the InGaP etch profiles is shown in Figure 3.11. It can be seen that for 80°C , Figure 3.11a, and 90°C , Figure 3.11b, etches, InGaP has a tilted wall profile, while GaAs underneath has vertical walls. However, for 100°C etch, Figure 3.11c, both InGaP and GaAs walls are straight. Slight GaAs undercutting is visible. The bromine and ion beam currents were changed slightly for some of these runs, so that all of the etches done in Figure 3.11 were done at 5.5 mTorr bromine pressure, and the current density in the etch of Figure 3.11c was about $70 \mu\text{A}/\text{cm}^2$.

After the InGaP etching, multilayer InGaP/GaAs heterostructure etch optimization was done. Two types of heterostructures were used. Both are double heterostructures with an active layer sandwiched between p-type InGaP on top, and n-type InGaP on the bottom. The first, MIT R424, grown as an LED structure, has $0.6 \mu\text{m}$ thick GaAs core, with $0.7 \mu\text{m}$ InGaP layers. The second, LL OM661, has a quaternary InGaAsP layer active layer, $0.4 \mu\text{m}$ thick, and $1.3 \mu\text{m}$ top InGaP thickness, and $1.5 \mu\text{m}$ lower InGaP thickness. This structure also has a thin InGaAs quantum well in the middle of the active layer. Both structures have a GaAs cap layer, $0.2 \mu\text{m}$ thick for the former, and $0.4 \mu\text{m}$ for the latter. The

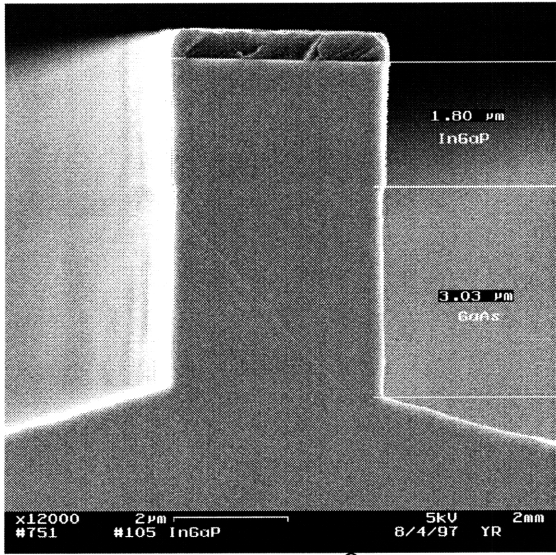
sidewall profiles are shown in Figure 3.12a for the GaAs core material etched at 90°C, and in Figure 3.12b for the InGaAsP core material etched at 115°C.



a) 80°C

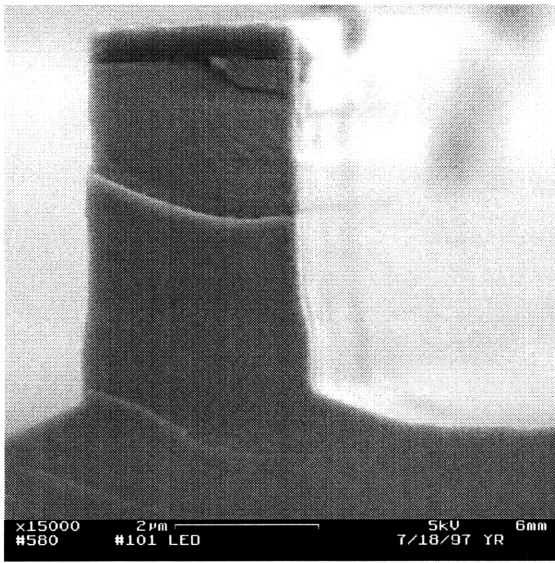


b) 90°C



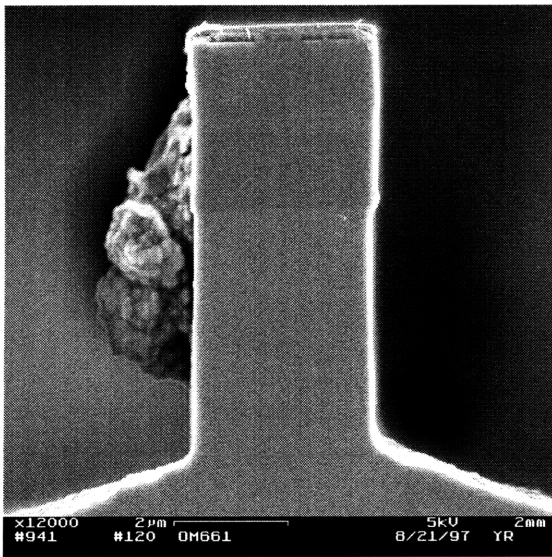
c) 100°C

Figure 3.11: Sidewall profiles of InGaP on GaAs substrate etched in Br₂ IBAE system at a) 80°C, b) 90°C, and c) 100°C.



a)

p+ GaAs 0.2μm
p InGaP 0.7μm
ud GaAs 0.6μm
n InGaP 0.7μm
 n+ GaAs



b)

p+ GaAs 0.4μm
p InGaP 1.3μm
ud InGaAsP 0.2μm
 - - - - - InGaAs-QW -
ud InGaAsP 0.2μm
n InGaP 1.5μm
 n+ GaAs

Figure 3.12: Optimized InGaP/GaAs multilayer heterostructure etch for a) an LED sample with GaAs core, and b) a laser sample with InGaAsP core.

Slight undercutting is visible in the GaAs core layer in Figure 3.12a, but the InGaP sidewalls are straight. The etch temperature of the quaternary material is somewhat higher,

since all of the structure contains indium. However, the quaternary spontaneous etch rate is larger than that of InGaP, and at higher temperature, undercutting in the core is visible. With the quaternary core material, steps for IPSEL deflector fabrications were also developed. The sample was mounted on a 45° slanted chuck to obtain the 45° deflector. Photoresist, which has sloped sidewall profile was used for the mask, since it more closely approximates a vertical profile when the mask is tilted. An example of the 45° etch is shown in Figure 3.13. The etch was performed at 110°C, with a 600 V, 60 $\mu\text{A}/\text{cm}^2$ beam and 6.0 mTorr of Br_2 pressure.

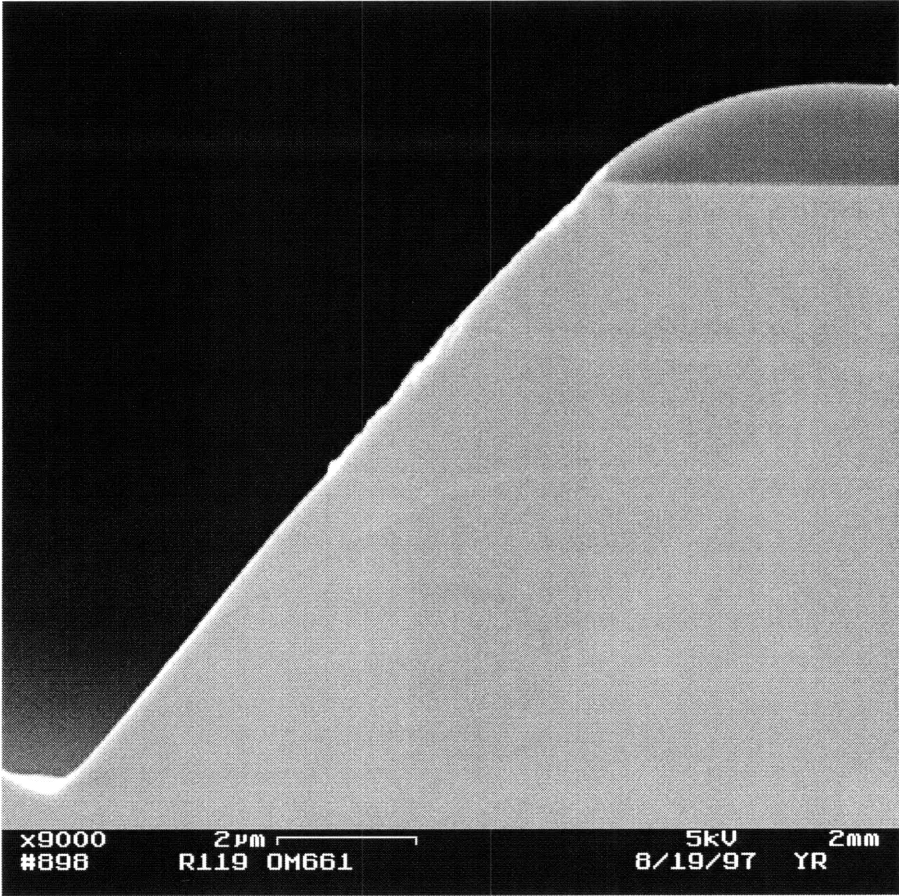


Figure 3.13: Profile of LL OM661 material etched in the Br_2 IBAE system on a 45° tilted stage at 110°C, 600 V, 60 $\mu\text{A}/\text{cm}^2$, and 6.0 mTorr of Br_2 , with a photoresist mask.

3.7 Etch Mask Development

After the proper etching equipment, chemistry, and parameters, the etch mask material and patterning is the most important issue for obtaining smooth straight facets. The type of etch system, chemistry, and parameters used, however, determine the type of masking material and its thickness that are necessary. The material that is being etched also puts constraints on the masking material. Finally, the methods available for patterning the masking materials are also important in deciding on the proper choice. In this section, the different requirements for the etch mask material will be described. Next, the competing materials will be compared. Finally, the best etch masks used in this project will be discussed. Future directions for improvement will also be mentioned.

An ideal mask is a mask that is not affected by the etch. It should also be very easy to pattern without affecting the sample material underneath. The quality of patterning of the mask material should not depend on the sidewall profile of the photoresist used. Finally, it should be easy to strip the mask without affecting the sample. If a mask does not get affected by the etch, then the sidewall profile of the etch mask is not important. In the case where the sidewall of the mask is not vertical, the farthest part of the mask's edge defines the etch pattern. The patterning process has to be developed to make this edge as straight as possible. A problem can arise if the farthest mask edge alternates between the top and bottom edges. Also, if there is any spontaneous etching of the sample and the mask profile is undercut, then the mask edge acts as the mask for the kinetically assisted etching, and the inside etch acts as the mask for the unassisted etch. However, for a mask that is not affected by the etch, the mask can be made so thin, that the relative position of its edges is made irrelevant.

If the mask does get affected by the etch, however, then the profile of the wall becomes important. One way its importance is manifested is through the transfer of the mask edge

slope into the etched sidewall profile of the sample. The transfer is not complete. If the etch is purely anisotropic, then the slope in the semiconductor is equal to the slope of the etch mask multiplied by the etch rate ratio of the semiconductor and the etch mask materials. Therefore, even if the mask material does etch in the system, the slower it does so, the better the verticality of the etch sidewalls in the semiconductor will be. If the profile is more complex, where there are two or more slopes in the mask at a single horizontal location (as in a concave or convex edge case), then these slopes add up to give an equivalent one.

Examples of the effects of the mask profile on the sidewall profile of the etched sample are shown in Figure 3.14. For all of these examples, it is assumed that the substrate etches four times faster than the mask material. In Figure 3.14a, a mask profile of slope $m=1$ is transferred into the substrate, which ends up with sidewalls of slope $m=4$. The bottom of the sidewall corresponds to the original edge of the mask. The top is under the edge of the post-etch mask. Correspondingly, if the slope of the mask is larger, then the substrate slope will be larger, as in Figure 3.14b, where the mask slope is $m=2$, and that of the substrate is $m=8$. If the mask has a negative slope, the situation is, in theory, exactly the same. Thus the resulting profile of the substrate is the same if the mask has $m=1$ (Figure 3.14a) or $m=-1$ (Figure 3.14c). Again, in the negative slope case, the bottom of the substrate sidewall is defined by the original mask edge, and the top, by the final outermost mask edge. In the case where both positive and negative slopes exist in the mask, as in Figure 3.14d, these two slopes effectively add up. Thus, the resultant profile for a mask with a “dovetail” profile with slopes 1 and -1 (Figure 3.14d) has the same substrate profile as in the case of $m=2$ slope mask of Figure 3.14b. This “concave” mask profile occurs when the mask is etched with a diffusion limited etch. The situation is the same in the case of a “convex”, rather than “concave”, mask profile.

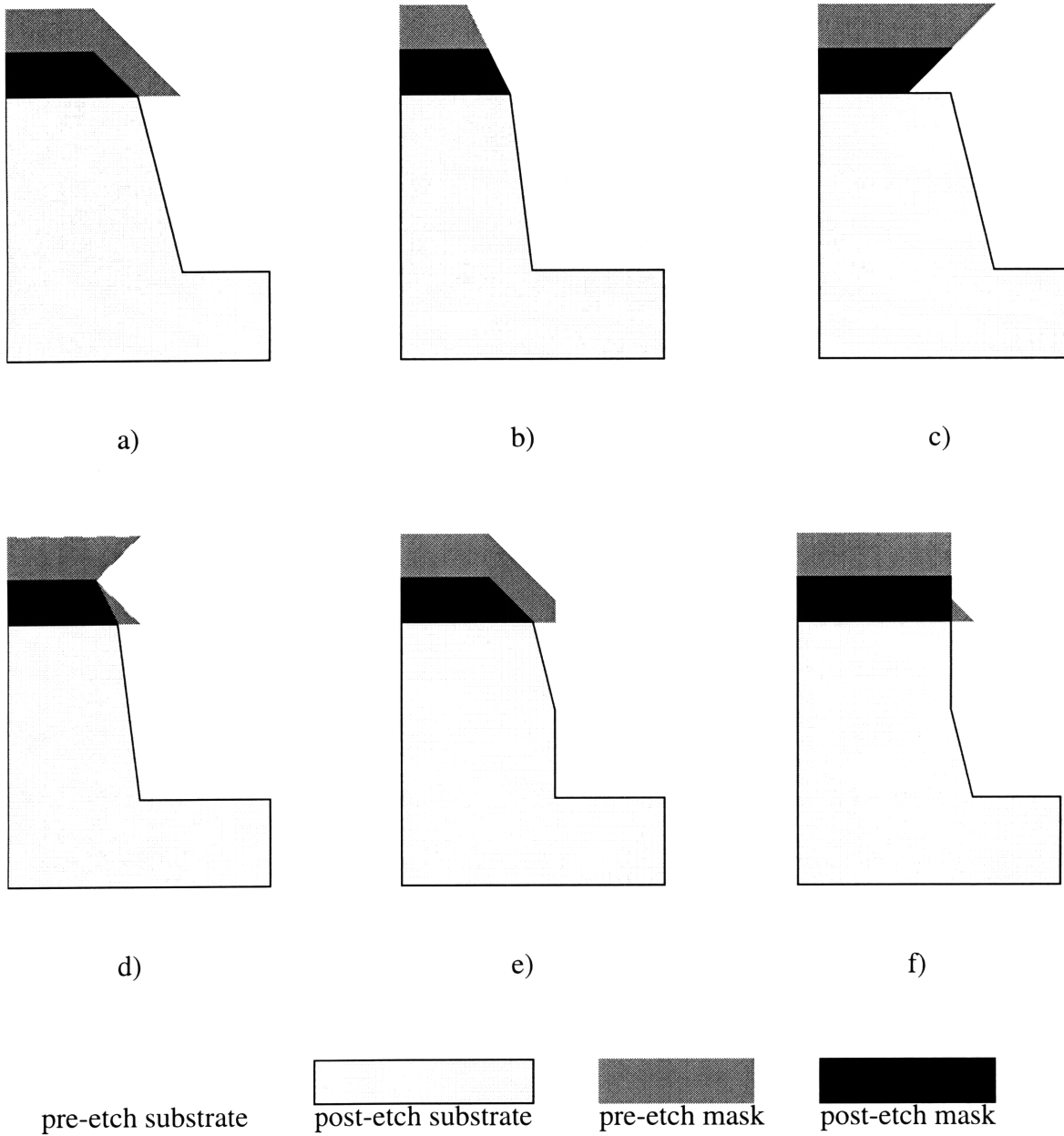


Figure 3.14: Effect of different mask profiles on the profile of the etched substrate.

Transformation of the mask profile for more complicated profiles is shown in Figure 3.14e and Figure 3.14f. The mask profile similar to the one in Figure 3.14e occurs in some

patterned photoresist, where the resist forms “dew drop” type of profile. The profile in Figure 3.14f occurs for dry etched features, which have been underetched. It should be reiterated here that the etch rate ratio of the mask to the substrate can be just as important as the sidewall profile, and for some mask materials that do not etch very fast, the slanted sidewall can be tolerated.

All of the descriptions of the etch profiles explained above assume totally anisotropic kinetically assisted etching. If there is some spontaneous etching, then undercutting under the mask edge will be visible. This effect is more pronounced in cases where the mask has a negative slope. Furthermore, an unassisted etch component can have a crystallographic plane preference. Thus, underneath the undercut mask the etch can assume slopes consistent with crystallographic planes. Sometimes these are not single slope profiles, but more complicated multiplane profiles.

If mask materials that etch during the substrate etch are used, then it is necessary to make them thick and straight. The mask etching in the case of bromine IBAE is not chemical, but is purely mechanical. The ion energy and density was large enough during the etches to produce sufficient sputtering rates for most materials. Thus, choosing a material which can be patterned vertically is important. Three different masking materials have been used for the IBAE etching. The most obvious one is photoresist. It can be deposited in a thick layer. Since patterning any other material requires photoresist patterning, using photoresist directly reduces the number of processing steps. Furthermore, photoresist is very easy to remove without degrading or contaminating the sample surface. However, it is not stable at higher temperatures, which are sometimes necessary for InGaP etching. It is also very difficult to pattern vertically in a contact aligner. (See Section 4.3, for example.) Another polymer film, ARC XL20, was also investigated. This polymer has a much

higher temperature stability (up to 190°C), and etches in photoresist developer. However, it cannot be deposited thicker than 200 nm, which limits its use to short etches only.

Using metal is another option. Metals have similar or smaller sputtering rates than photoresists and dielectrics. Many research groups use metals as dry etch mask materials. Some of the metals, however, are easily attacked by bromine. Aluminum and titanium are two such commonly used metals, which react chemically with bromine. This fact was confirmed in the bromine IBAE. Since the sputtering rate of the metals is appreciable, patterning them with vertical sidewalls is desirable. Metals can be patterned with wet etching, dry etching and lift-off. Wet etching produces sloped sidewall profiles characteristic of isotropic etches. Lift-off also produces sloped profiles. For example, the profile of a 400 nm thick titanium film patterned by lift-off is shown in Figure 3.15. Dry etching metal, especially without damaging the semiconductor underneath, is difficult. Titanium, which dry etches in fluorocarbon plasmas, is the only choice known. (Commonly used aluminum etches are chlorine based, which attack compound semiconductors.) Finally, to strip many metals, acids which react with semiconductors have to be used. However, in many of our etches, where the sidewall profile was not as important, we used nickel as masking material. Nickel has a lower sputtering rate than photoresist and silicon dioxide, and does not react with bromine. It also can be etched with a sulfuric acid based etch without attacking the semiconductors. (The etchant was a commercial product of Transene Co., and was verified in our laboratory not to noticeably react with GaAs and InP.) Thus Ni can be patterned and stripped easily. The lift off technique was also used to pattern the nickel.

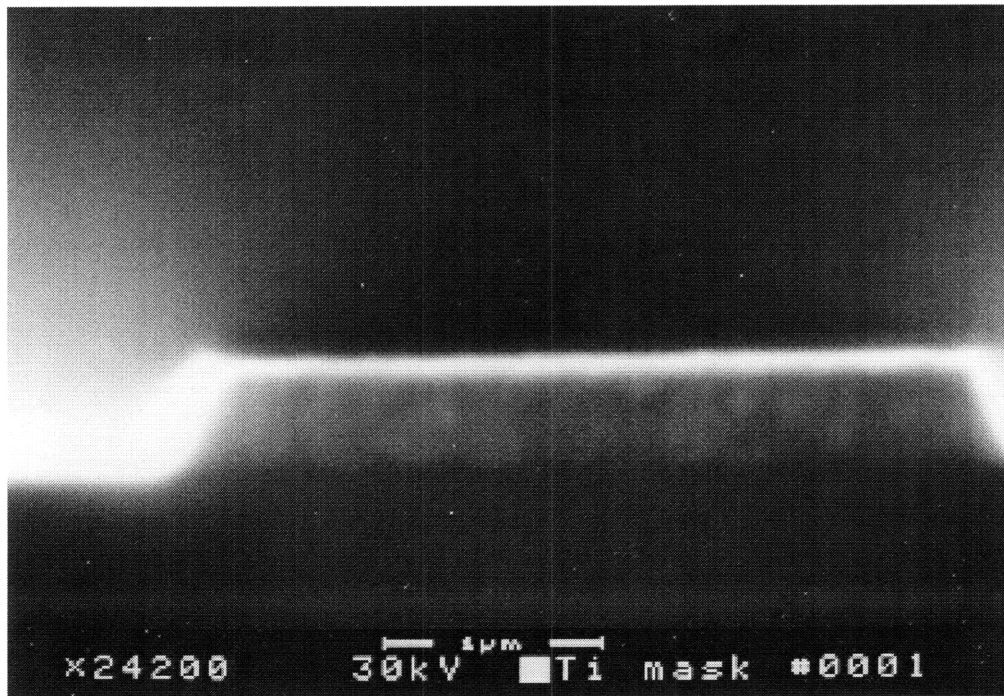


Figure 3.15: Metal (Ti, 400 nm) profile after lift-off patterning.

The mask material that has been used the most in this work was silicon oxide. It is easily patterned by wet hydrofluoric acid etching or dry etching using a fluorocarbon plasma. It can also be quickly stripped in HF solution, without damaging the underlying semiconductors. When sidewall profiles were not as critical, wet etched patterning was used. To obtain straight wall profiles the oxide films were dry etched. Both of the RIE systems available etched photoresist at least as fast as the dielectric. Addition of oxygen to the freon gases, which is necessary to remove fluorocarbon polymer deposits, was part of the cause. However, etching in pure CF_4 also produced 1:1 photoresist to silicon oxide etch rate ratios, perhaps due to reduced oxide etch rate. This etch and $\text{CHF}_3/\text{O}_2(5\%)$ were the best in terms of reducing photoresist etch rates, but nevertheless produced equal etch rate ratios. As discussed above, in the case were an etch mask etches at the same rate as the

material, the profile of the mask is reproduced. This is effect is demonstrated in Figure 3.16, where the profile of silicon oxide, patterned in $\text{CHF}_3/\text{O}_2(5\%)$ RIE with resist mask, is shown.

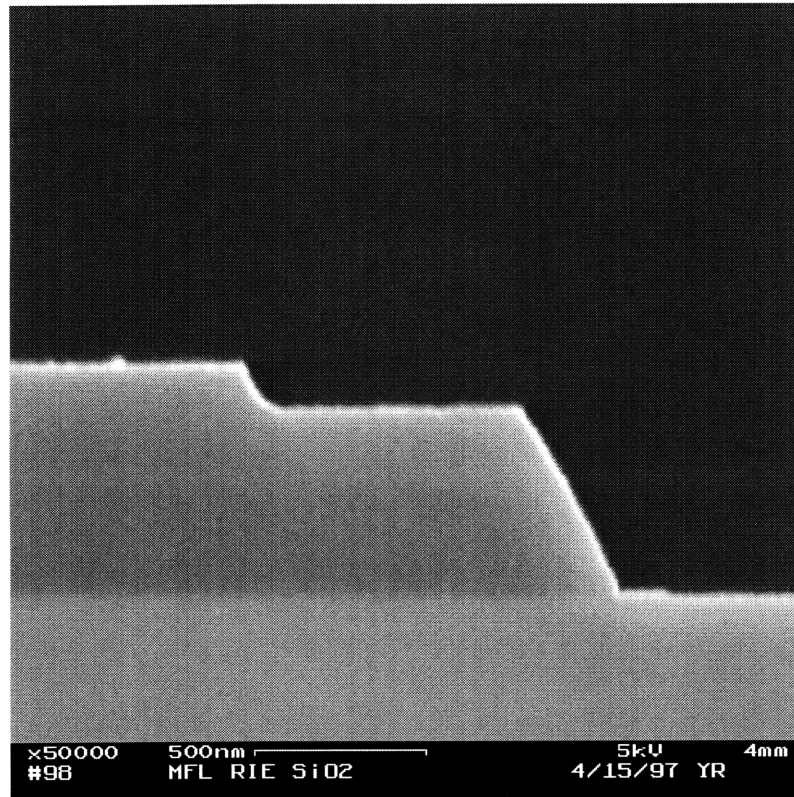


Figure 3.16: Profile of a 400 nm thick silicon oxide film patterned in $\text{CHF}_3/\text{O}_2(5\%)$ RIE with a photoresist mask.

The solution to obtaining a patterned silicon oxide etch mask with vertical sidewalls was to use a metal mask during the oxide RIE etch. In particular, nickel was used because it is not attacked in the freon RIE, and is easily stripped without damaging the semiconductor. A thin 60 nm Ni layer was used. Either wet etching or lift-off was used to pattern the nickel. Using nickel improved the oxide sidewall profile. However, the oxide dry etch had to be optimized to reduce the isotropic etch component. The full procedure of the mask definition is detailed in Appendix A. An example of the oxide mask profile is shown

in Figure 3.17. This figure shows a semiconductor etch profile with the oxide mask intact. The dark top layer of the ridge is the oxide, which has vertical profile. This method of oxide patterning described above was developed due to suboptimal RIE and photolithography capabilities. However, if straight wall resist profiles or a more selective RIE process are developed, these would be preferred due to fewer processing steps.

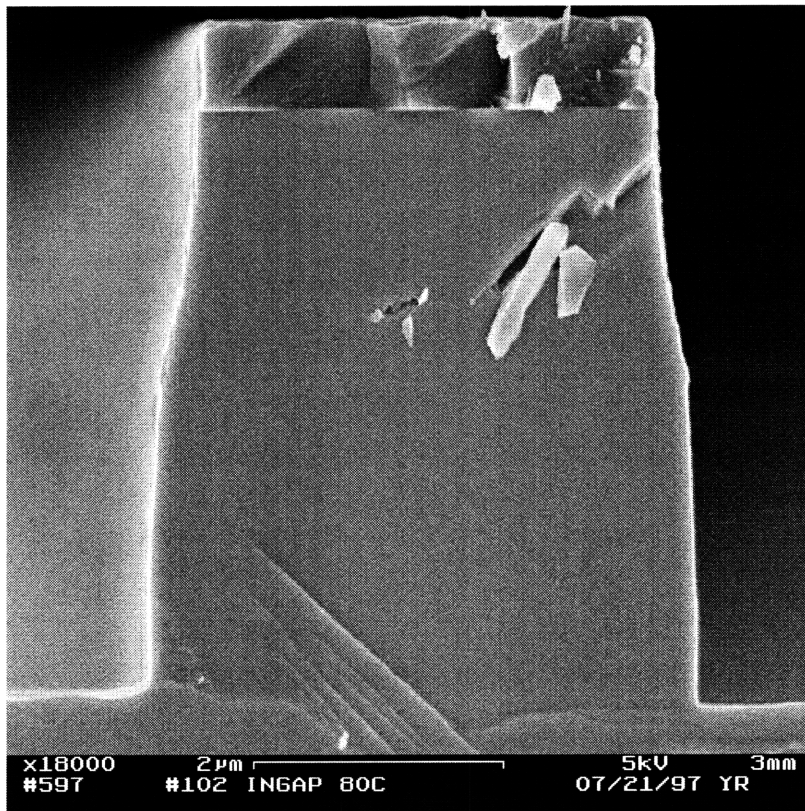


Figure 3.17: Vertical profile silicon oxide mask (dark layer) on top of an etched semiconductor ridge.

In addition to silicon oxide, the use of other dielectrics as etch masks was investigated. Figures of merit for an etch mask material is its resistance to the bromine IBAE etch, its patternability in an RIE system (straight wall profile), and ease of stripping. Since both silicon nitride and titanium oxide can be stripped in HF (though not as quickly as SiO_x) and can be patterned in the freon RIE, the etch rates of these materials in the IBAE were com-

pared to those of silicon oxide. It should be mentioned, before the results are reported, that the sputtering rate of these materials depends on the quality of the deposited dielectric, as well as the type of material. Thus the results could vary if a higher quality films can be deposited. Both silicon oxide and silicon nitride in this study were deposited in a PECVD system with the sample heated to 350°C. Titanium oxide was deposited in a e-beam evaporation system with a background oxygen concentration. The silicon nitride deposited in this manner etched 1.5 times as fast as the oxide, though its refractive index was measured by an ellipsometer to be 1.96 (indicating reasonable quality). This is contradictory to other reports that it should be more resistant to ion bombardment than the oxide. Titanium oxide, however, performed much better, with silicon oxide etching twice as fast as titanium oxide. Furthermore, consistent with other reports [83], dry etching of TiO_x in CF_4 RIE system was demonstrated in our laboratory with an etch rate of 8 nm/min. Thus, in the future, it is anticipated that this material will be used for masking, instead of silicon dioxide.

Chapter 4

Etched Facet Lasers

4.1 IPSEL Structures

As outlined in Chapter 1, the main thrust of this thesis is to develop the technology necessary for integrated In-Plane Surface Emitting Laser (IPSEL) VLSI circuits. In addition to the further development of the E-o-E technology described in Chapter 2, the dry etching for the mirrors and deflectors of IPSELS was investigated. This effort was described in Chapter 3. In this Chapter, application of the etching developments to etched facet lasers is described and the laser results are reported. Before proceeding to the etched facet lasers, however, the possible IPSEL structures themselves will be examined to understand the types and constraints of processes required for their fabrication.

For the most part, the structure of these lasers is similar to the conventional semiconductor laser structures [84]. The epitaxial layers needed for this device are a double heterostructure. This means that a relatively low bandgap, high refractive index active layer is sandwiched between two high bandgap, low refractive index cladding layers. The sandwich acts to confine the field in the direction normal to the wafer. It also serves the purpose of carrier confinement in the undoped active region, where the electrons entering from the n-type doped cladding layer and the holes entering from the p-type cladding layer, encounter a potential barrier to propagate further. Thus, they are encouraged to recombine and emit light. Usually, a thin layer of even lower bandgap material, called the quantum well, is inserted into the active region to enhance the gain, and often the active region around the well is compositionally graded to improve carrier confinement in the well. The lateral optical field confinement in the IPSEL is accomplished in the same way as in the

conventional diode laser by etching a ridge in the upper cladding, or by overgrowing the active region with cladding material, as in the buried heterostructure lasers.

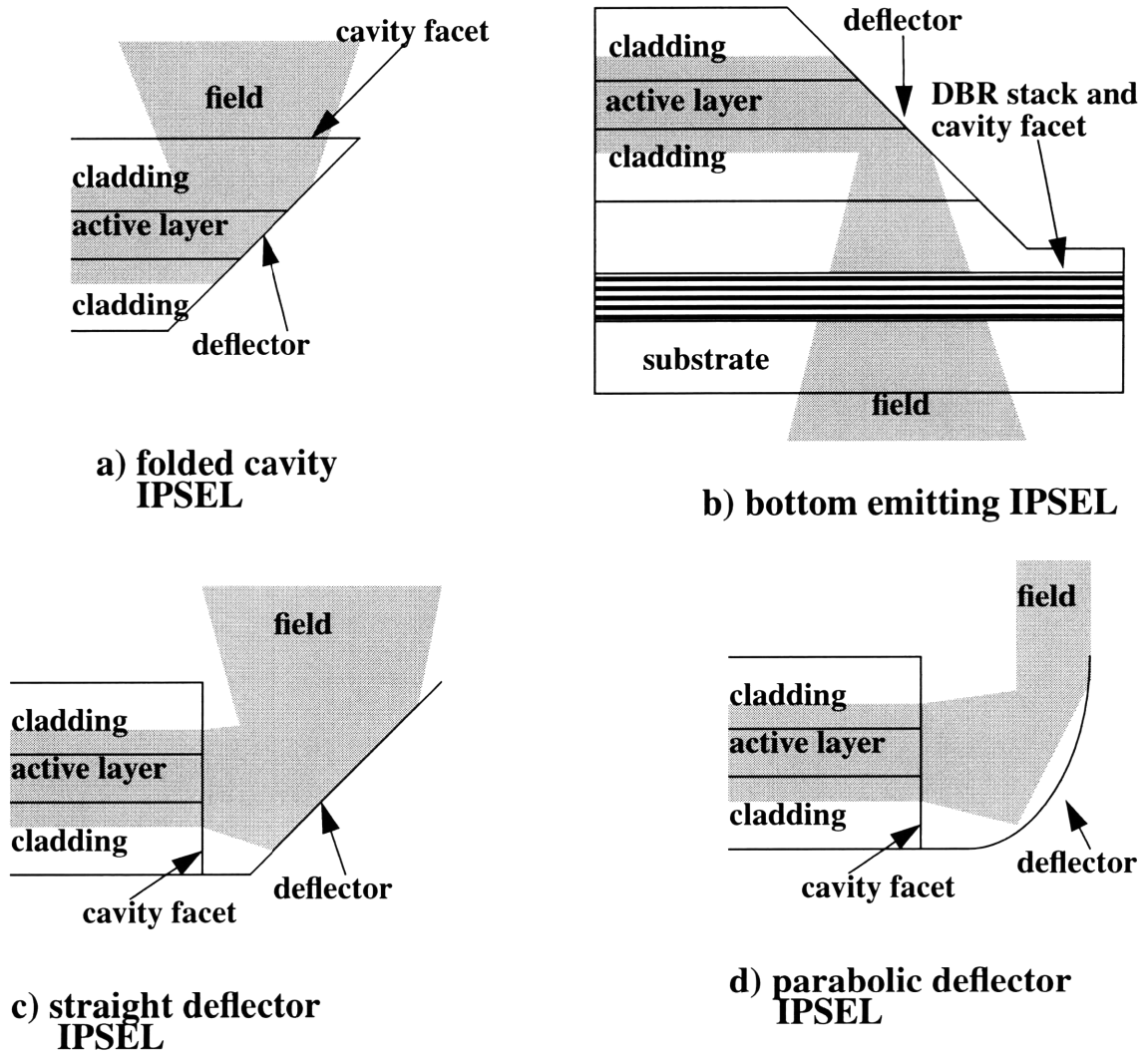


Figure 4.1: Schematic illustration of various IPSEL structures.

Though the structure of IPSELS and conventional lasers is similar in the vertical and lateral directions, the way the optical laser cavity is defined in the longitudinal direction is very different. Conventionally, the laser cavity in the longitudinal direction is defined by crystallographic cleaving. For IPSELS, the cavity is defined by either an etched vertical

“facet” or by a horizontal surface. Furthermore, all IPSELS have a deflector, which changes the light direction from in-plane to surface-normal. The following figure, Figure 4.1, is a cross-sectional illustration of some of the different types of IPSEL structures.

The IPSEL structures can be categorized as in-cavity deflector structures and external deflector structures [16]. In the in-cavity deflector case, the beam is deflected by a 45° etched semiconductor to air interface. At this angle, there is total internal reflection, so all of the light (which does not get scattered by the etch imperfections) is reflected. Next, the light encounters a partially reflecting interface parallel with the surface. In the case of the folded cavity IPSEL structure in Figure 4.1a [30, 31, 32], this reflecting interface is the wafer surface itself. The contact is recessed back from the edge of the laser far enough to allow the expanding beam to escape. Without any coatings, about 30% of the light is reflected from this interface. (A dielectric stack coating on the surface could increase or decrease this reflectivity.) However, because the beam continues to diverge away from the waveguide after the surface and the second deflector reflections, a much smaller percentage is coupled back into the in-plane laser waveguide. A similar situation occurs in the bottom emitting IPSEL with an in-cavity deflector, shown in Figure 4.1b [85]. In this case, if the light is reflected off the back of the wafer, which is relatively far away, very little would couple back into the waveguide. Therefore, a Bragg reflector dielectric stack is typically grown right below the waveguide structure to act as the partially reflecting mirror. The position of the top contact does not matter in this case, but an opening in the bottom contact is required. Moreover, the substrate must be transparent at the laser wavelength and the bottom surface would have to be anti-reflection coated to minimize multiple reflections. For both cases, the active layer should be kept as close to the cavity mirror as possible to maximize the light coupled back into the cavity. And for both cases, the beam

coming out of the laser is highly divergent and astigmatic, requiring expensive optics when these devices are used in a system.

An example of an external deflector IPSEL is shown in Figure 4.1c. As in the other examples discussed, the deflector is 45° to the surface, which redirects the light from the in-plane direction into surface normal direction [33]. However, in this structure, there is another vertical etched interface in the path of the light. This vertical etched facet defines the longitudinal cavity. As long as this etched facet is smooth and vertical, whatever light that does not get out of the cavity, is coupled back into the laser waveguide mode. For this reason, the external deflector IPSEL mirror losses should be smaller than for the in-cavity IPSELS. However, if the deflector is too far from the cavity facet, then the expanding field coming out of the facet does not fully fill the deflector, and not all of the light goes into the surface normal direction. Another cause of higher losses of the external deflector IPSELS over the in-cavity ones is that the light sees two etched mirrors in its path. If the mirrors are not perfect, then the mirror losses are incurred twice. However, if the fabrication and the etching is well developed, the external deflector devices should be better than the in-cavity deflector devices.

All three devices mentioned so far have a highly divergent and astigmatic beam at the output. Consequently, the cost improvements due to the monolithic system integration could be offset by expensive optics. To improve this, parabolic-external-deflector IPSELS, Figure 4.1d, have been fabricated [34]. The parabolic deflector collimates the output light in the direction that normally has the largest divergence. The issues involved with this type of device are the same as the ones for the 45° external deflector case. To etch such a deflector, a much better control of the etching parameters has to be obtained than for a straight deflector. Nevertheless, this is the final structure chosen for our project.

There are other ways of reducing beam divergence. The parabolic deflector can also be fabricated for the in-cavity deflector structures. This would be easiest for the bottom emitting structure. In this case, the coupling of reflected light would also be improved. However, any deviations of the deflector from the parabola would cause both beam spreading and losses due to coupling for the in-cavity structures, whereas for the external deflector structures only the beam quality suffers. Another way to reduce beam divergence, is to etch a lenslet [86] on the surface of the in-cavity deflector structures, which again would be the most convenient for the bottom emitting lasers. However, using the bottom emitting structure would probably prove a wrong choice in the long run, since the wavelength at which the Vitesse fabricated detectors operate (and thus the wavelength at which the lasers will have to emit), is absorbed by the substrate. For these reasons, the approach of Figure 4.1d is the most practical for our application. Past success of this structure for AlGaAs/GaAs lasers at the MIT Lincoln Laboratory further favors this choice.

The final issue to address for the IPSEL design is whether to make both facets or one facet surface emitting. This issue has as much to do with the system design as with the device design. Having both facets surface emitting allows for all of the light to be used. However, the system designer might find having two beams for one signal undesirable. Furthermore, there might be a possibility of high-reflection coating one of the facets, so that very little light escapes. This requires angled evaporation or sputtering of dielectrics with precise thickness control, but is nevertheless possible. In this way, the quality factor of the cavity would be higher, and the cavity size and threshold currents can be reduced, and external efficiencies increased.

Even with the best designed IPSEL structure, device performance is directly related to the quality of the etched facets and deflectors. The etch quality can be determined indirectly by observing it on a scanning electron microscope. However, when imperfections

are observed, it is difficult to compare relatively the quality of one facet versus another, since it is difficult to estimate the relative losses for different types of imperfections. For example, issues such as when does roughness introduce more loss than tilting of the facet, or how does an indentation effect the scattering losses are hard to resolve. Therefore, the quality of a facet is best measured by its bottom line: how does it effect the laser performance. Consequently, to test the quality of the etching done in this study, etched facet lasers (without deflectors) structures were used. These devices were measured under pulsed current conditions, and from the output light vs. current characteristics, information about facet quality was deduced. In the remainder of this chapter, the structure and the fabrication procedures of the etched facet lasers will be described, and the results from the tests of these lasers will be reported. A detailed list of procedures used for fabricating etched facet lasers in included in Appendix A.

4.2 Etched Facet Laser Structure

As mentioned before, the main reason for fabricating etched facet lasers is to ascertain the etch quality. Thus a structure and the experiments have to be chosen so that variations in all of the parameters, other than the facets, would not effect the laser structure. Furthermore, to tell how good the etched facets are, it would be best to compare them with cleaved facet lasers, where the mirror reflectivity is well known. It would be optimal to have the cleaved and the etched facet lasers side by side to eliminate any doubts about material quality variation over the sample. The bottom of the etch next to the etched facet will reflect and scatter some of the light away, so the experiment and the structure have to be designed so that as much as possible of this light can be collected from the facet. Finally, as will be discussed in the next section, much of the information can be deduced about the mirrors by examining certain laser characteristics as a function of cavity length.

The structure shown in Figure 4.2 was designed and fabricated specifically to satisfy all of above requirements. For this test, a broad area laser structure was chosen to eliminate sensitive fabrication steps. Broad area lasers do not require any ridge etching or intricate contact definition, to which laser properties are very sensitive. The broad area lasers are terminated on each side by a deeply etched area, the edges of which make up the facets. The etched facet lasers are fabricated in four different lengths, which should provide a sufficient number of points to determine the function of any length dependent laser characteristics. The length is determined by the distance between the etched facets and the length of the contacts themselves. The etch facets are interrupted by unetched areas. In these unetched areas, which extend over the length of the whole sample a continuous broad area laser contact is fabricated. This contact is designated for the cleaved facet lasers.

When following a line of etched facet lasers, each of the four sizes of contacts is interrupted by an etched area. Then the four contacts and etched area repeat again. These lines of lasers are grouped together side by side in sets of five. In between each set, runs a continuous contact. This pattern of five etched facet lasers and one continuous contact repeats itself. When the fabrication is finished, the sample is cleaved through the etched areas to separate the different length lasers. On one of the sides, the cleave is as close as possible to the etched facet to increase the light collected from that facet. The cleaves, in addition to separating the lasers and allowing a way to collect the light directly from the etched facets, forms the cavity mirrors for the cleaved facet lasers. The cavity length for the cleaved lasers thus is slightly different from the etched ones, but four different lengths are still obtained from each experiment. The four different etched facet laser lengths are 0.6 mm, 0.9 mm, 1.2 mm, and 1.5 mm. Actually, the contact is receded from the etched facets by 3 μm on each side to ensure that shorting of the diode does not occur in case of slight misalignments. The length of the etched area is 144 μm , so the length of the cleaved lasers

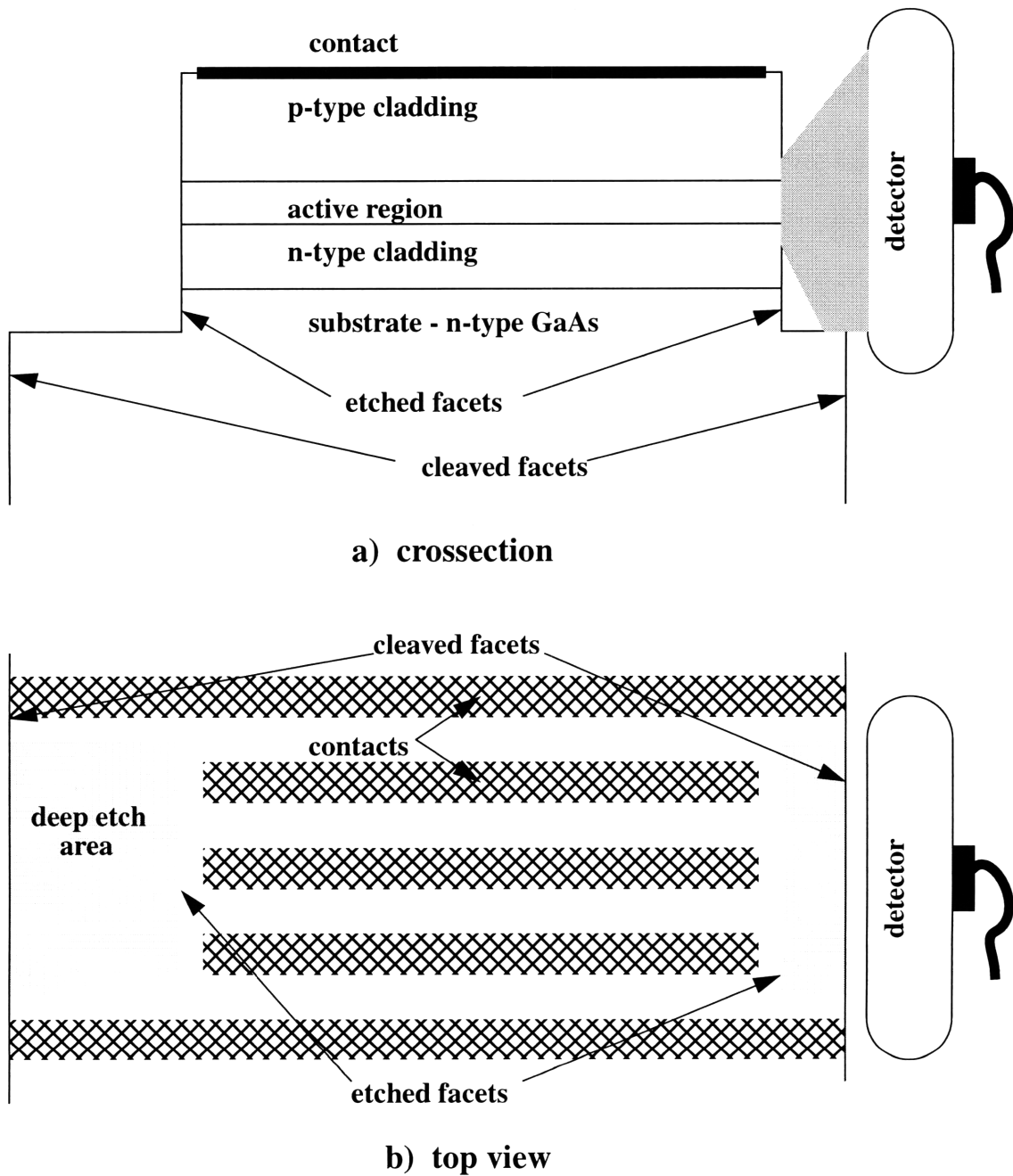


Figure 4.2: Schematic of the side-by-side etched and cleaved facet laser performance comparison experiment.

would be longer by about that amount. Two widths for the etched facet broad area laser contact were used: 50 and 100 μm . Because of a miscalculation during the layout the

cleaved facet laser contact widths are smaller, being 28 and 78 μm . The spacing between each contact is 50 μm .

For the broad area lasers, the laser is defined in the lateral dimension only by region of gain which closely corresponds to the region of current flow. In turn the current flow is primarily defined by the contact, but some current spreading also occurs. To control this current spreading, and to make it reproducible, the lasers were isolated by etching away the highly doped cap layer and some of the cladding layer. This isolation etch is between contacts, and starts 3 μm away from the contact. This etch extends along the whole length of the lasers, and etches partly into the etched area. The etched walls next to the contact are not etched, and for further protection, 12 μm are left unetched adjacent to the contacts in the neighborhood of the facets. The walls of the etched area perpendicular to the facet walls are also protected, so that they can be examined after the cleaving for the lasers is done.

Even though broad area lasers are used in this experiment, in the future index guided ridge lasers will be fabricated. Thus, in addition to the geometric structure design, the heterostructure design to provide optimal waveguiding was also done before epitaxial growth. Two important requirements were used for such a structure. One requirement is that for a selected ridge width, there is only a single transverse optical mode for this structure. The other requirement is for this single mode to have the largest possible fraction of its power in the active region. (This fraction is called the confinement factor, Γ .) An optical field profile for a structure that satisfies these requirements is shown in Figure 4.3. The simulation was done using the effective index method. The structure was grown in the MIT GSMBE, runs R625 and R626 [87]. A thin GaAs etch stop layer was placed in the upper InGaP cladding layer at the exact location where the ridge should be. The simulation was run also for cases where the etch stop layer cannot be used, and the ridge was overetched

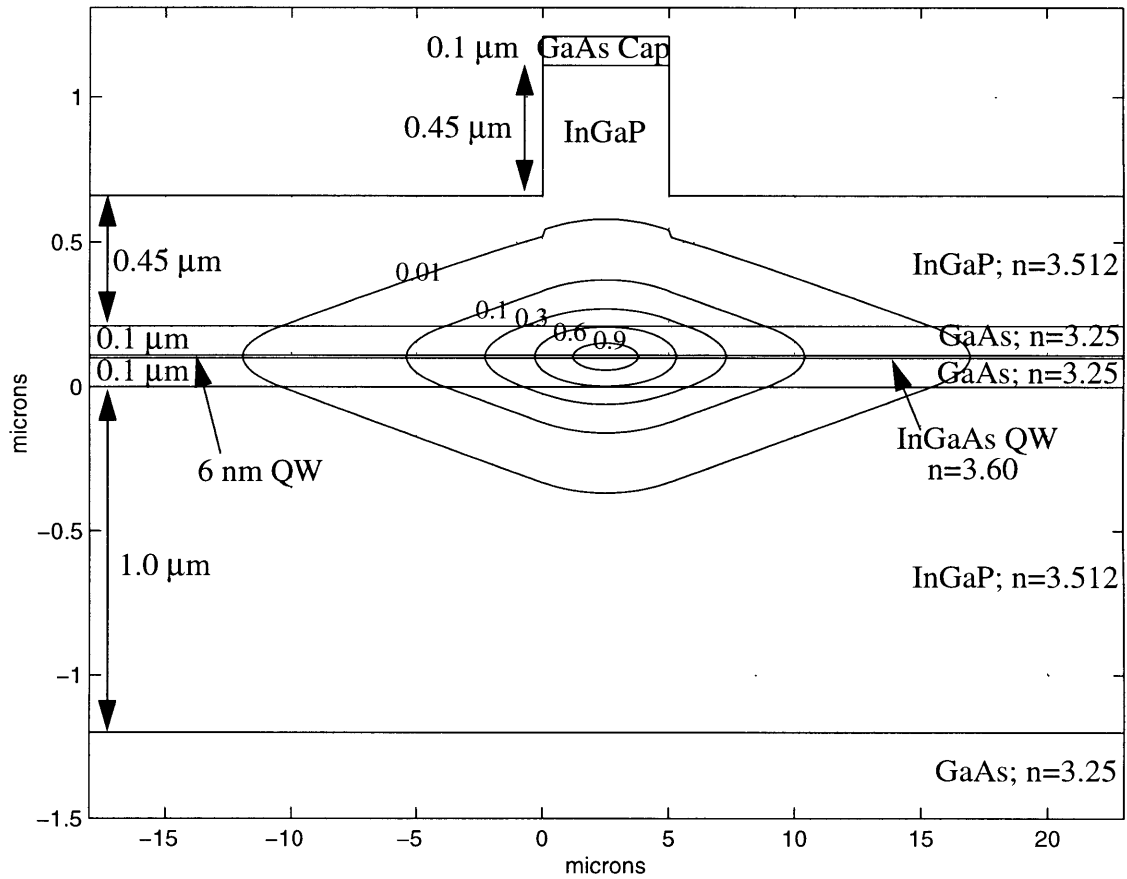


Figure 4.3: Simulated optical field contour profile for a 5 μm ridge laser for the heterostructure grown for this project.

or underetched by 0.1 μm. It was confirmed that both of these cases produced single mode waveguides. This structure was optimal for this experiment, where the upper cladding was kept to the minimum, so that the active region can be as close to the surface so that the more of the light can be collected. For the case of external-deflector IPSELs, as thick as possible upper cladding should be grown to reduce the stringency of the alignment between the etched facet and the deflector.

4.3 Laser Fabrication

Total fabrication of the etched facet lasers on bulk material requires three photolithographic masks. The first one is used for patterning the etched facets, the second one is for defining the contacts, and the last one is for the isolation etch. First, the mask used for the facet etch is patterned. Before commencement of fabrication, the sample is solvent cleaned. Then the sample is covered with about 0.6-0.8 μm of SiO_x , using either pyrolytic deposition or PECVD. Thickness uniformity over the sample is one of the problems of this step, especially using the pyrolytic system. Next, using photoresist patterning and electron-beam evaporation, about 60 nm of nickel is patterned using a lift-off technique. This nickel pattern is used as a mask to etch the oxide in the CF_4/O_2 RIE system. After the oxide is patterned, nickel is removed. The oxide is used as the mask for the facet etch in the bromine IBAE system. After the facet etch, the SiO_x mask is removed in buffered HF solution. Ti/Au film is then patterned using a lift-off technique to make contact to the top p-type GaAs layer. Five micron thick resist was used to ensure that it fills the etched areas and the facets are covered. Next a thick photoresist was patterned to protect everything, other than the areas between the contacts, during the isolation etch. The isolation etch was carried out in the Br_2 IBAE at 50°C. (The low temperature Br_2 IBAE was developed for the purpose of bottom side contact formation, since it forms sloped walls, which are easy to metallize. It was also used for post-growth polycrystalline material removal described in Section 2.4. It proved to be the perfect choice for the isolation etch as well, since photoresist can be used as a mask.) The sample then was lapped down to about 150 μm and polished on lens paper in bromine/methanol solution. Finally, as the last step before cleaving, the whole back side of the sample is covered with a Ge/Au/Ni/Au film, which is then annealed at 450°C for 30 seconds in a rapid thermal annealer. A much more detailed description of the process is available in A.

Most of the steps in the etched facet laser fabrication had to be developed to suit the requirements of the fabrication. Of course, the most critical step to the performance of the lasers is the facet etch itself, development of which was discussed in Section 3.6. The next most crucial steps have to do with the etch mask definition. Development of the oxide dry etch and the reasons for choosing Ni as the mask are described in Section 3.7. However, patterning nickel itself is just as important, since the edge of the nickel pattern has to be very straight, because any roughness or undulations will transfer into the facet and cause optical losses. The lift-off process for this step uses 0.5 μm positive resist. (Thin resist is used to enhance pattern reproducibility.) The top layer of the resist is hardened with chlorobenzene prior to development. This causes this layer to etch more slowly in the developer than the underlying resist, causing an undercut. Ideally, this hardened top portion of the photoresist will be the outermost part of the edge, and it will define the metal that gets deposited during the evaporation. Photoresist, however, treated or untreated does not develop vertically, unless extreme care is taken. This is due mostly to the light profile inside the resist during the exposure and the etching of unexposed resist during development. All the exposures done for this project were done on a contact aligner, where the mask comes into contact with the resist, and the parts of the resist not covered by the mask are exposed to uncollimated light. Angled light rays, diffraction around the features, standing wave patterns due to reflections from the air to resist and substrate to resist interfaces, and light absorption by the resist cause the sloped photoresist walls. These effects are exacerbated if the mask is not in good contact with the resist. Development time also plays an important part in the photoresist profile. The developer has greater than 10:1 selectivity of etching the exposed versus unexposed resist (depending on the total exposure energy), but if overdeveloped the resist pattern will start to wash away, contributing

further to the sloping of the walls. These effects caused the chlorobenzene lift-off process to be unreliable.

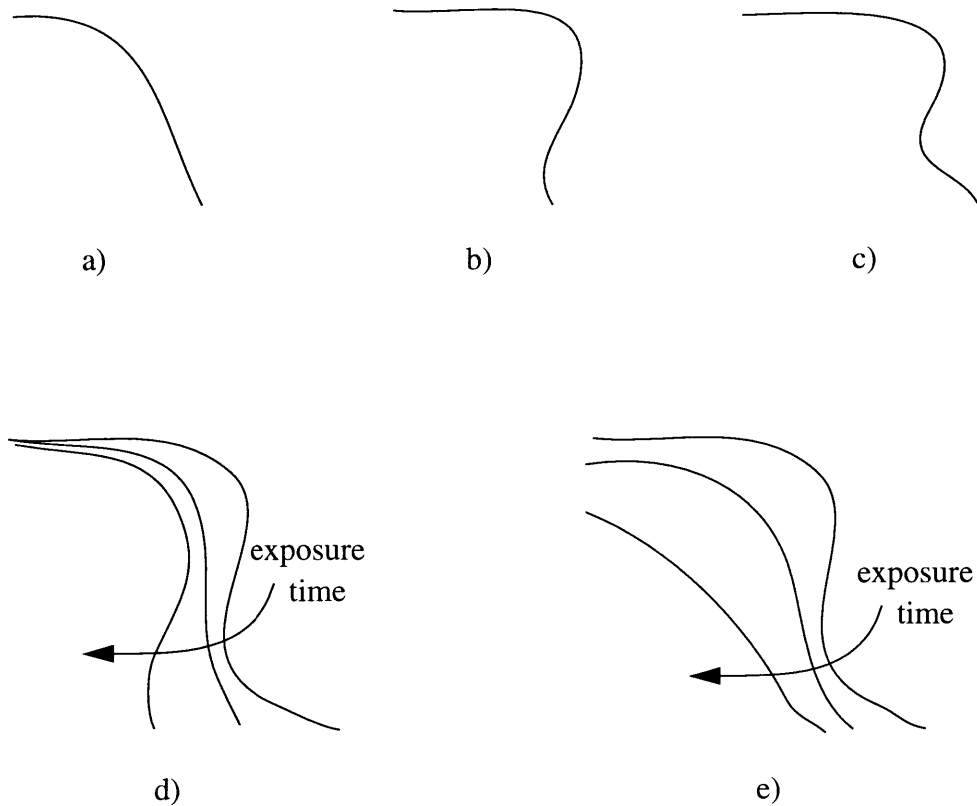


Figure 4.4: Chlorobenzene soaked photoresist profiles: a) no chlorobenzene treatment, b) properly exposed and developed, c) improperly exposed, d) exposure time effects with good mask contact, e) exposure time effects with poor mask contact.

The geometries involved in photolithography for lift-off metal processing using chlorobenzene treated positive photoresist are shown in Figure 4.4. The photoresist profile without the chlorobenzene soaking is shown in Figure 4.4a. The profile is sloped due to the light diffraction and standing wave effects. When evaporation is done on top of this resist, in some places there will be a continuous sheet of metal covering both the slope and the resist free region. During lift-off, tearing of the metal film will occur in these spots, causing uneven edges in the metal pattern. The ideal resist profile for lift-off metal pattern-

ing is shown in Figure 4.4b. When metal is evaporated on this structure, no link is formed between the metal on top of the resist and on the resist free area, and a clean metal edge is obtained. Unfortunately, if the resist is not exposed properly, then the bottom portion retains the shape it would have without the chlorobenzene soak, while the top is undercut as expected, as shown in Figure 4.4c. Since the bottom edge extends beyond the top edge, the undercut does not help in terms of metal pattern edge definition, and problems similar to the case of lift-off with resist untreated with chlorobenzene come up. These problems are further amplified, since the bottom edge in the case of Figure 4.4c is rougher than the top edge in the case of Figure 4.4a.

Exposure time of the chlorobenzene soaked positive photoresist is critical to obtain a proper profile. Part of the approach is to expose the bottom of the photoresist film enough, so that it develops faster. As shown in Figure 4.4d, as the exposure time is increased, the total optical energy increases and the whole thickness of the photoresist, except for the part affected by the chlorobenzene, acquires the same etch rate in the developer, so the undercutting can occur even at the bottom. If longer development times are used, the hardened top edge of the photoresist starts to degrade and roughen by the time the bottom portion is developed out. Thus for the type of photolithography where the top is hardened to produce undercutting, longer exposure times are needed than for regular photoresist patterning.

Too much exposure however, allows the total optical energy of diffracted and stray light in the top portion of the resist to build up. Consequently, even though this part is hardened, the developer etch rate there increases, and the top part is pulled back, counteracting the undercutting. This effect is particularly evident for the case where the lithography mask does not come into contact with the resist during the exposure. In this case, the amount of stray light exposing the sample is much larger, so that as the exposure is

increased, the energy in the top part below the mask accumulates faster than in the bottom portion of the resist. As shown in Figure 4.4e, this causes the resist profile to become even more slanted as the exposure time is increased. Poor contact during exposure is sometimes due to improperly maintained equipment, though most often it is caused by the photoresist buildup next to the edge of the sample (called edge bead). For small samples, this effect is much more severe, and for square samples, edge bead on the corners can be tens of microns high. For these reasons, much difficulty was encountered with obtaining straight edge etch masks for the facet etch.

Other challenges in the etched facet laser fabrication were also mainly concerned with the etch mask. The process of obtaining straight walls in the SiO_x mask using RIE was discussed in Section 3.7. In order to facilitate the optimization of the oxide RIE etching, uniform oxide deposition was important. After failing to obtain uniform films using a pyrolytic deposition system, it was necessary to switch to a more complicated PECVD system. This made it possible to have a thickness variation within $0.1 \mu\text{m}$, as opposed to $0.3 \mu\text{m}$ variation on the pyrolytic deposition system. Developing a cleaning procedure for both of these systems was also important to eliminate silica particle incorporation into the film. Finally, the thick photoresist lithography used for lift-off contact patterning also had to be developed. The edge bead on the thick resist is severe, and the situation in Figure 4.4e was encountered. Thus edge bead removal and low exposure times were used to obtain acceptable results. The rest of the processing steps did not require as much develop-

ment, and only slightly altered standard processing parameters were used for these processes.

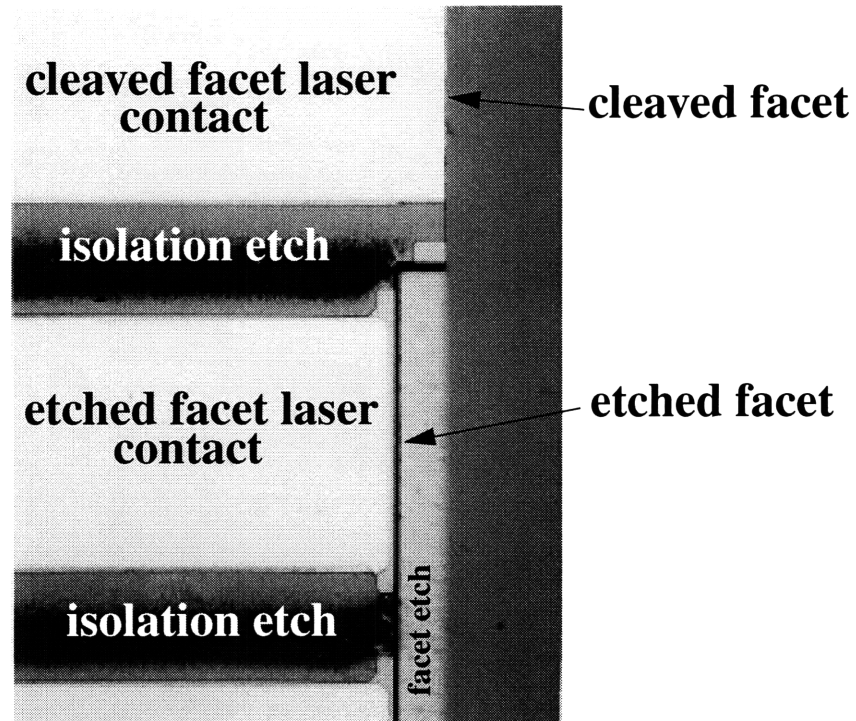


Figure 4.5: Photograph (top view) of completed etched facet laser structure.

Throughout the processing, alignment during the photolithography was very important. First alignment is done to the sample's crystallographic axes. A well-cleaved sample is very important for this. If the crystal axis and the etched facet are misaligned, then during the cleaving of the sample at the final stage to define the mirrors for the cleaved facet lasers, the cleave will propagate at an angle to the etched facet, and will eventually cut off some of the etched facets. In this case, the only way to prevent this would be to cleave farther from the etched facet, which would reduce the light collection from the etched facets. For the OMCVD-grown sample, keeping track of the particular crystallographic direction

was also important since the substrate wafer is cut 5° off axis in one direction [27]. Thus, a vertical cleaved facet can be obtained along one of the crystallographic directions, but not the other. The alignment for the other two photolithography steps was done with alignment marks. Misalignments during the contact patterning lithography could cause metal to deposit on the etched facets, electrically shorting the laser diode. Misalignments in the isolation etch step could cause destruction of parts of the etched facets.

4.4 Etched Facet Laser Results

The broad area structure was chosen for the etched facet laser experiment in order to minimize the dependence of the laser results on the contact and ridge definition. Thus, the laser results should primarily reflect the quality of the mirrors and the material. To obtain the information on the quality of the mirrors, it is sufficient to measure the light-current (LI) characteristics of the lasers under pulsed conditions (to prevent thermal effects from coming into play). The important parameters in this case are the threshold current density and the differential quantum efficiency of the lasers. The threshold current density is dependent on the total optical loss in the laser cavity. Some of this loss is due to absorption of the material, and some to the escape of the light at the mirrors. If the cavity is shorter, the light escape at the mirrors becomes more important, thus increasing the total loss due to the mirrors, and, consequently, increasing the threshold current. In fact, from basic principles of laser operation, a relationship between the threshold current density, the cavity length, and the mirror reflectivity (or scattering) can be written down [84]:

$$J_{th} = \frac{qd}{\tau_e} \left(n_0 + \frac{\alpha_m + \alpha_i}{a\Gamma} \right) \quad (4.1)$$

where d is the active region thickness, τ_e is the carrier lifetime, n_0 is the carrier density necessary for transparency, a is the linear gain coefficient, Γ is the confinement factor, and α_i is the internal material loss. α_m is the mirror loss defined as

$$\alpha_m = \frac{1}{L} \ln \frac{1}{R} \quad (4.2)$$

where L is the laser cavity length, and R is the mirror reflectivity. In this expression, identical mirrors on both ends of the cavity were assumed. If the reciprocal cavity length is defined by K , and the different terms in the threshold current expression are lumped together, Equations 4.1 and 4.2 can be combined to produce the following expression:

$$J_{th} = A + B \left(\ln \frac{1}{R} \right) K \quad (4.3)$$

Terms A and B are lumped parameters, and contain the information about the gain medium and not the mirrors.

As can be seen from Equation 4.3, if the threshold current densities are plotted against the reciprocal length of the cavities, the slope contains the information about the mirror reflectivity. Furthermore, if two types of lasers fabricated from the same material, but with different mirrors, are compared, then from the slopes of the $J_{th}(K)$ plots, relative mirror reflectivities can be obtained. This is particularly useful for our case, since we know the cleaved facet laser mirror reflectivity to be about 30%, $R_c=0.3$, and therefore from the slopes of the threshold current plots, m_c and m_e , for cleaved and etched facet lasers respectively, etched facet reflectivity, R_e , can be obtained. For this purpose, the expression in Equation 4.4 can be used.

$$\ln \frac{1}{R_e} = \frac{m_e}{m_c} \ln \frac{1}{R_c} \quad (4.4)$$

Thus, no material parameters are needed to obtain the mirror reflectivities.

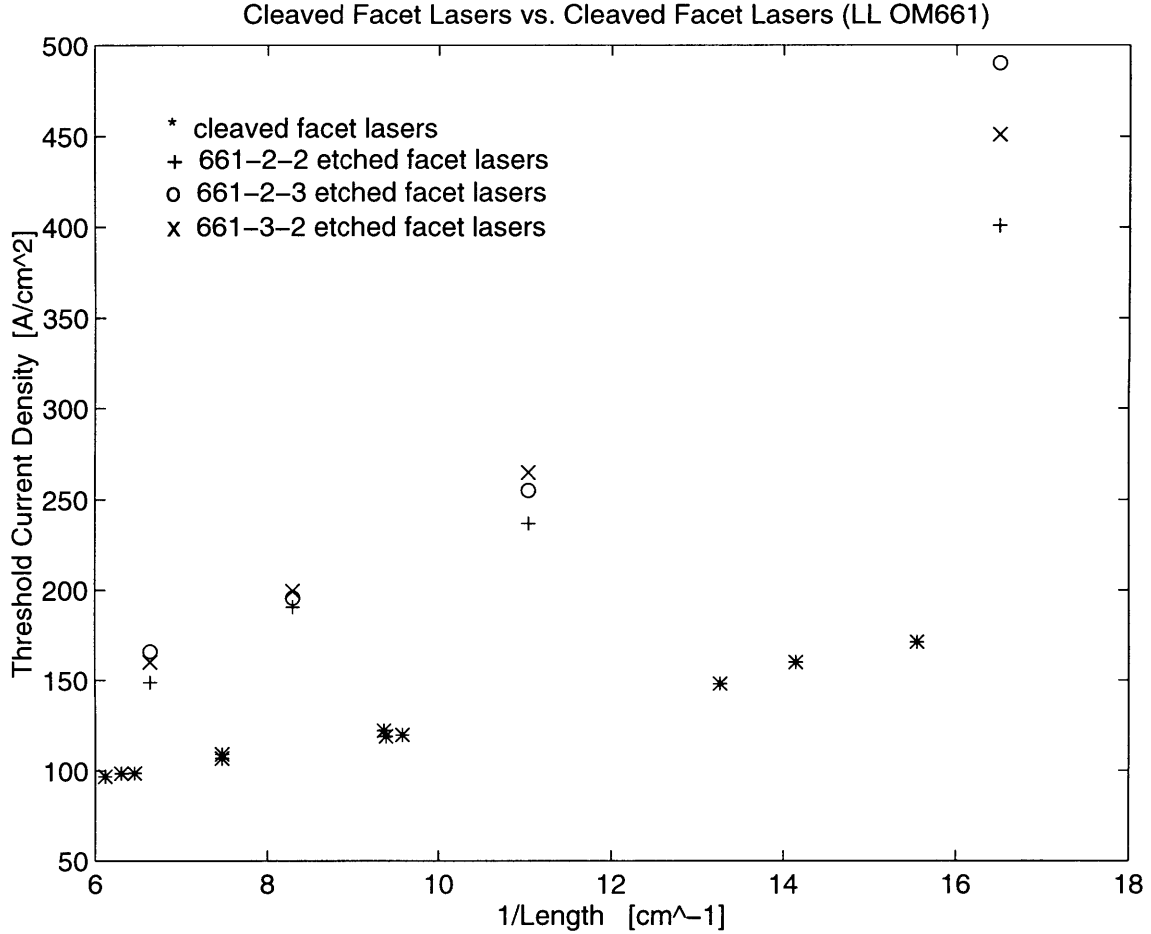
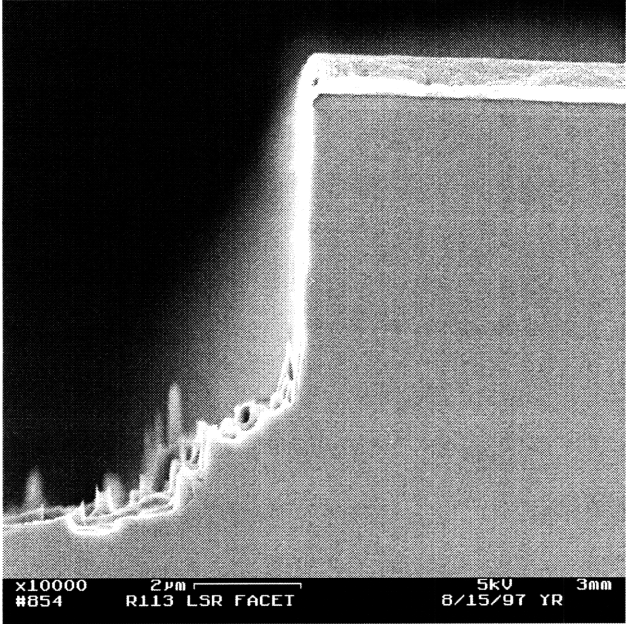


Figure 4.6: Threshold current density plot for cleaved and etched facet lasers fabricated from the Lincoln Laboratory OMCVD material.

The plots of the threshold current densities of the cleaved and etched facet lasers fabricated from the OMCVD material are shown in Figure 4.6. Since both the cleaved and the etched facet lasers have similar slopes for the different samples, the data from the samples is lumped together. Extracting the slopes from the graph and using Equation 4.4, etched facet mirror reflectivity $R_e=0.05$ is calculated. The difference between the cleaved and etched facet reflectivity, i.e. 0.3 and 0.05, respectively, is due to the light being scattered out of the cavity or into the lasing mode by the mirror imperfections. A micrograph of a

representative etched facet is shown in Figure 4.7. The scattering into other cavity modes is very evident in the L-I characteristics of the lasers, where for the etched facet lasers the lasing commencement is very smooth with L-I curve “knee” being rounded, whereas for the cleaved facet lasers it is abrupt, as shown in Figure 4.8.



p+ GaAs 0.4µm
p InGaP 1.3µm
ud InGaAsP 0.2µm
 - - - - - InGaAs-QW -
ud InGaAsP 0.2µm
n InGaP 1.5µm

 n+ GaAs

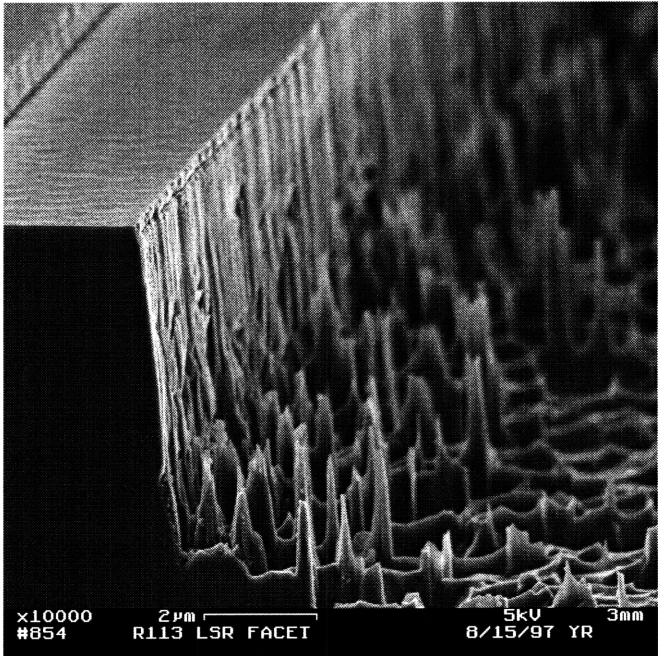


Figure 4.7: SEM micrographs of the etched facets in the OM661-2-2 laser sample.

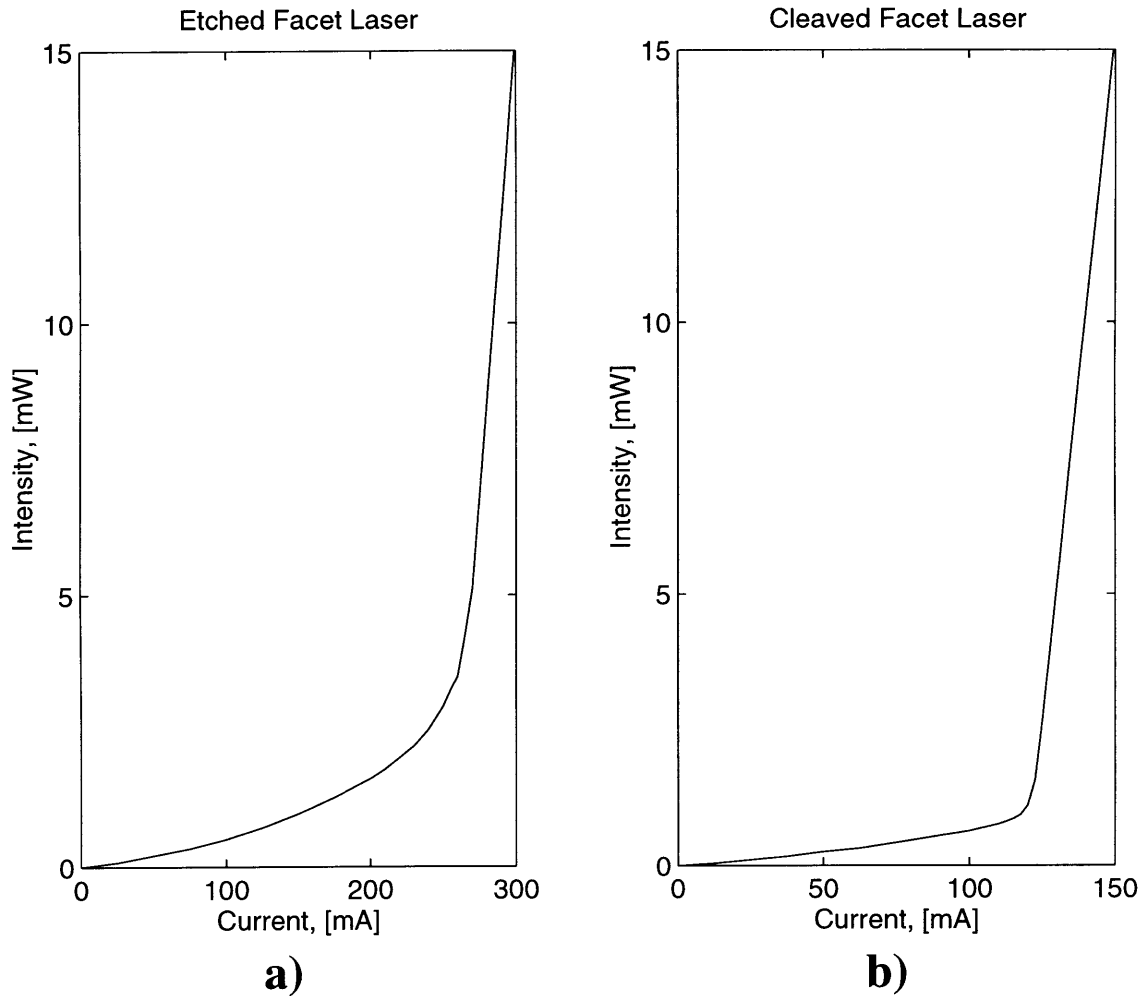


Figure 4.8: Light-Current plots of a) 1340 mm long cleaved facet lasers and b) 1200 mm long etched facets lasers made from LL OM661-3-2 sample.

The reflectivity obtained from the slopes of the $J_{th}(K)$ plot can be somewhat smaller than the actual value. The error comes in assuming that the linear gain coefficient, a , and the carrier lifetime, τ_e , of Equation 4.1 are constant. In actuality, these parameters themselves depend on the injected carrier concentration, and thus on the current density [84]. This effect is not negligible in the case of high carrier injection. In fact, this effect is visible in Figure 4.6, where the $J_{th}(K)$ function deviates from the straight line for the short

etched facet lasers, where high carrier densities are required to commence lasing. Therefore, a better estimate can be made if lasers of with the same threshold current density, but different lengths, are compared. There are some cases like this in the data of Figure 4.6, where an etched facet laser has almost exactly the same threshold current density as a cleaved facet laser, but a different length. To obtain the relation between the reflectivities of the two lasers the following expression can be used.

$$\ln \frac{1}{R_e} = \frac{K_c}{K_e} \ln \frac{1}{R_c} = \frac{L_e}{L_c} \ln \frac{1}{R_c} \quad (4.5)$$

Thus, for OM661-2-2 and OM661-3-2 samples, $R_e=0.09$ and $R_e=0.078$, respectively, were calculated.

The mirror reflectivities for the laser sample fabricated from the MIT GSMBE grown R170 material (GaAs core layer) were also calculated. The plot of the threshold current densities for cleaved and etched facet lasers are shown in Figure 4.9. This sample has had some macroscopic defects which tended to decrease the laser performance. This is the reason that the cleaved facet laser current plot is not straight. For the etched facet sample lasers, the statistical sample was much larger, so it was easier to find the lasers with no defects. To exclude the effect of these macroscopic defects, the two devices with best performance are used to obtain the slope of the plot. Thus, calculating the etched facet reflectivities from the $J_{th}(K)$ plot slopes using Equation 4.4 resulted in $R_e=0.1$. Using the method of choosing devices with equal threshold current density, but different lengths, and using Equation 4.5, the etched facet reflectivity $R_e=0.17$ was calculated. An example of these etched facets is shown in Figure 4.10.

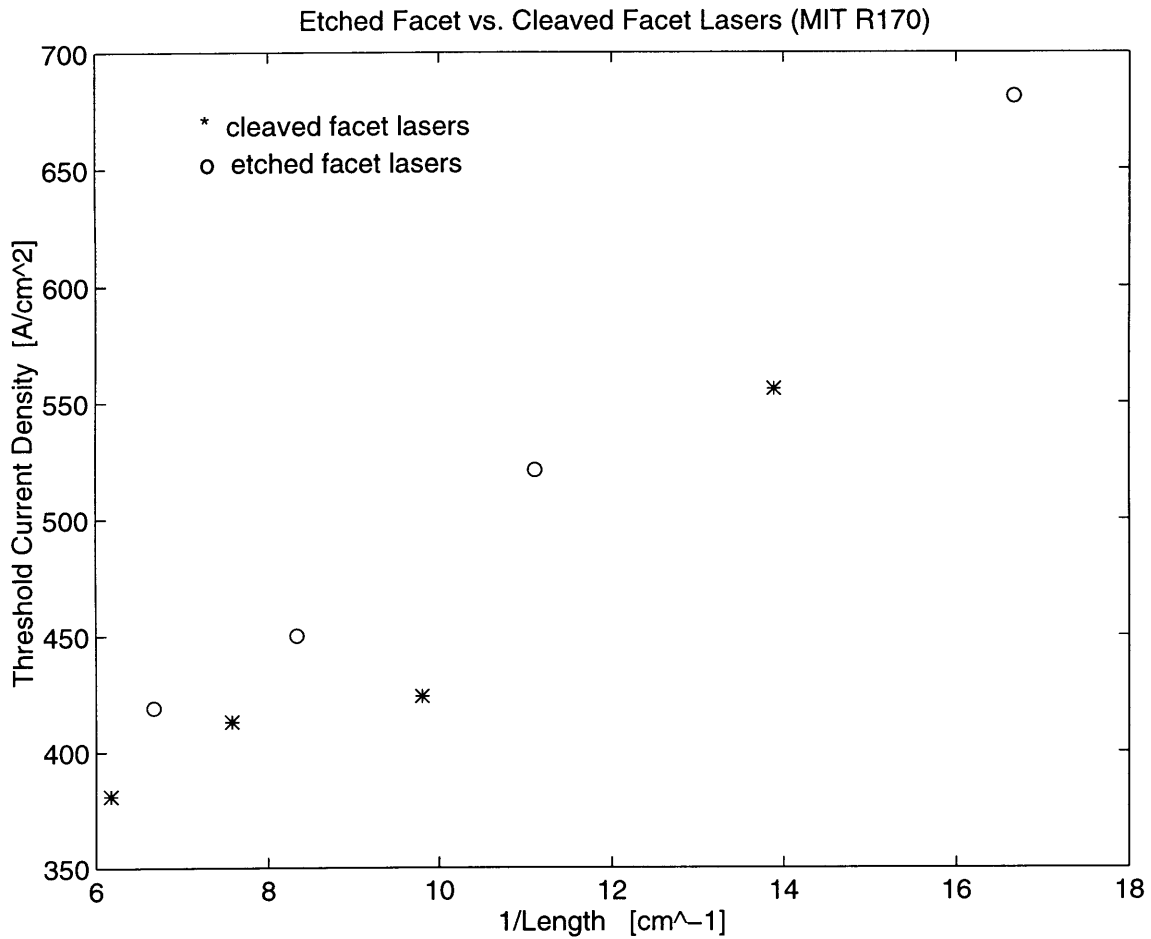
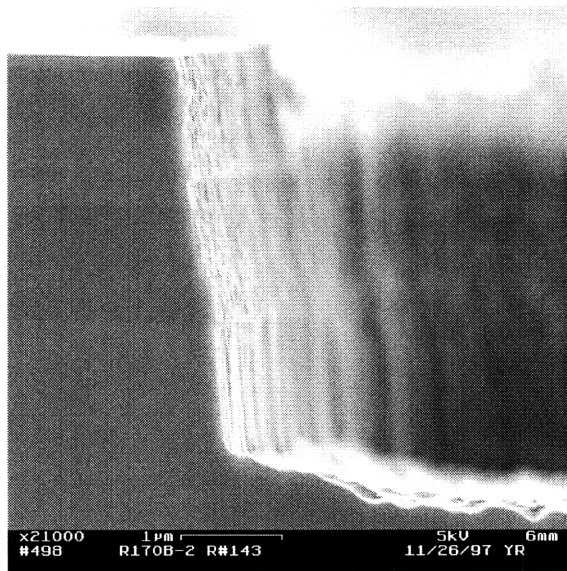


Figure 4.9: Threshold current density plot for cleaved and etched facet lasers fabricated from the MIT GSMBE material.

Representative L-I curves for the cleaved and etched facet lasers in this material are shown in Figure 4.11. Consistent with the mirror reflectivity results, the knee in the etched facet laser curve is more abrupt than in the case of the etched facet laser from LL OM661-3-2 sample (Figure 4.8a).



p+ GaAs 0.1 μ m
p InGaP 1.0 μ m
ud GaAs - 0.1 μ m
- - - - InGaAs-QW -
ud GaAs - 0.1 μ m
n InGaP 1.0 μ m
n+ GaAs

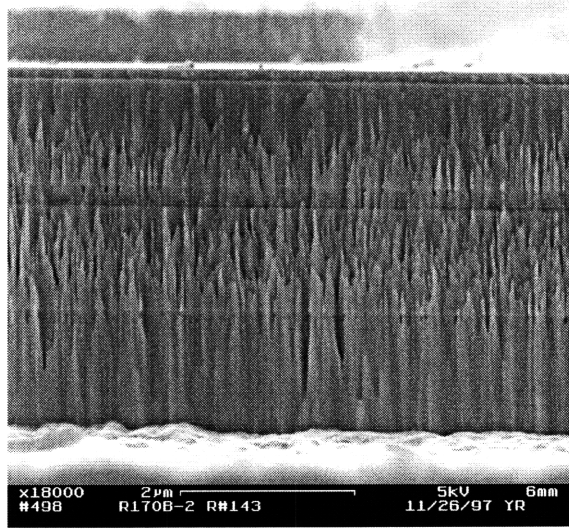


Figure 4.10: SEM micrographs of the etched facets in the R170 laser sample.

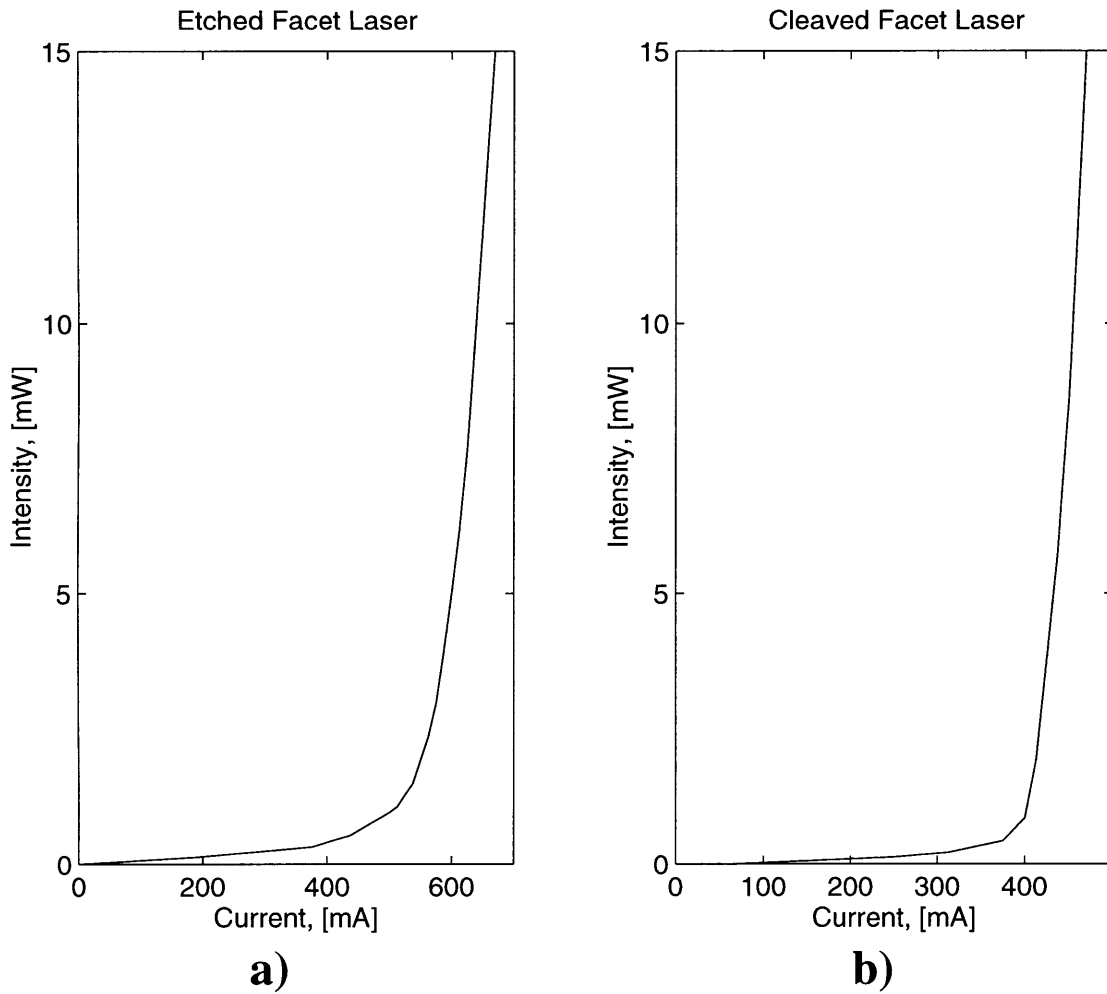


Figure 4.11: Light-Current plots of a) 1340 mm long cleaved facet lasers and b) 1200 mm long etched facets lasers made from MIT R170 sample.

In addition to the threshold current density, another parameter that can be obtained from the L-I plots which contains information about the mirror reflectivity, is the external differential quantum efficiency, η_d . Differential quantum efficiency is the slope of the L-I curve above threshold. A way to express this coefficient is in its reciprocal form, where it should be linear with the cavity length [84]:

$$\frac{1}{\eta_d} = \frac{1}{\eta_i} \left(1 + \frac{\alpha_i L}{\ln(1/R)} \right) \quad (4.6)$$

The above expression, where η_i is the internal quantum efficiency and α_i is the material optical loss, shows this relationship. The plots of the reciprocal external differential quantum efficiencies as a function of cavity length is shown in Figure 4.12 and Figure 4.13 for OM661 and R170 samples, respectively. However, in the present case, the differential quantum efficiency cannot be used to compare the cleaved and etched facet lasers because this parameter is dependent on the amount of light collected from the facet, and the collection of light from the etched facet lasers is not complete (as illustrated in Figure 4.2).

An attempt was made to adjust the efficiencies for etched facet lasers by estimating the amount of light that is incident on the etched region floor below the etched facet. The light impinging on the floor is assumed to be lost. The relative amount of light that is lost depends on the angle of the spread of the field as it exits the facet, on the distance between the etched facet and the cleave, and on the height of the active region from the etch floor. The height of the active region is obtained with a surface profilometer and the heterostructure parameters. The distance between the etched facet and the cleave is obtained using an optical microscope. The near-field profile of a cleaved facet laser was measured to obtain the angle of spread of the output beam from the full-width half-maximum (FWHM) points in the intensity profile. The FWHM spread is 41° in the vertical direction for the OM661 lasers [88]. As an example, with a 41° beam angle and $4 \mu\text{m}$ active region height, the differential quantum efficiency should be increased by 15%, 30%, and 64%, for $15 \mu\text{m}$, $20 \mu\text{m}$, and $50 \mu\text{m}$ facet to cleave distances, respectively. However, the differential efficiency data did not follow this model at all, and lower differential efficiencies were seen for lasers with the same active region height, and smaller facet to cleave distance, and smaller cavity length. It is suspected that not all of the light that impinges on the etch floor is totally lost,

and some of it is collected. If this is the case, then the measured etched facet laser efficiency dependence on the geometry is not as strong as assumed by the model above. Furthermore, since the measured differential quantum efficiency is dependent on the reflectivity and losses of the particular facet the measurement is taken from, facet nonuniformity further attributes to the inapplicability of the above model. Finally, the scattering of the data and its inconsistency with Equation 4.6 for the OM661 material (Figure 4.12), even for the cleaved facet lasers, cannot be presently explained and further complicates data analysis.

For the above reasons, the external differential quantum efficiency can only be used qualitatively to ascertain the etched facet laser quality. For the LL OM661 material, the best efficiency for a cleaved laser was 43.1% per facet. Some of the etched facet laser efficiencies were above 29%, which if imperfect light collection is taken into account, is surprisingly good in the light of the mirror losses calculated. For the MIT R170 lasers, the difference between cleaved and etched facet lasers is larger, with best efficiencies of 34% and 15%, respectively. However, in the case of this material, the facet etch was much shallower, so the smaller active layer height might explain this larger difference.

A final note about the accuracy of the etched facet reflectivity calculation should be made. Many of the parameters that go into the calculation are not precisely measured or known. Such parameters include the cleaved facet laser cavity lengths and the cleaved facet reflectivity. The assumption about the uniform material quality or uniform fabrication quality is also incorrect. To reduce the uncertainty, only the best devices were chosen for the calculation. However, some fluctuations are still present.

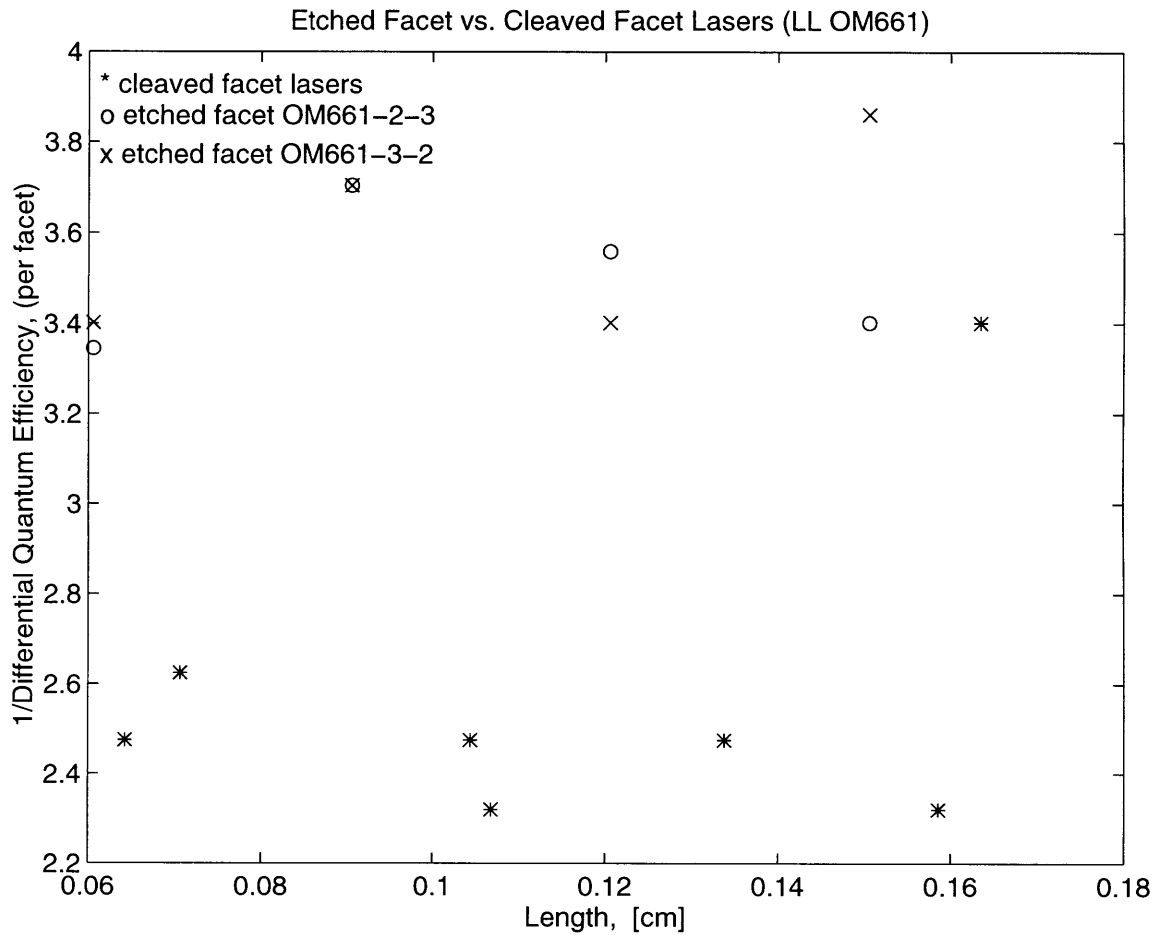


Figure 4.12: External differential quantum efficiencies of etched and cleaved facet laser fabricated from LL OMCVD material.

The conclusion that can be made from the etched facet laser results is that further improvement is necessary for the bromine IBAE process step. In particular, consistency of the etching needs to be improved. The facet etch quality in the lasers from both materials shown on the SEMs in Figure 4.7 and Figure 4.10 is inferior to those produced during the etch optimization, shown in Figure 3.12. Thus the optimized etch parameters need to be reproduced for the laser structures. Finally, even though the experiments are designed to

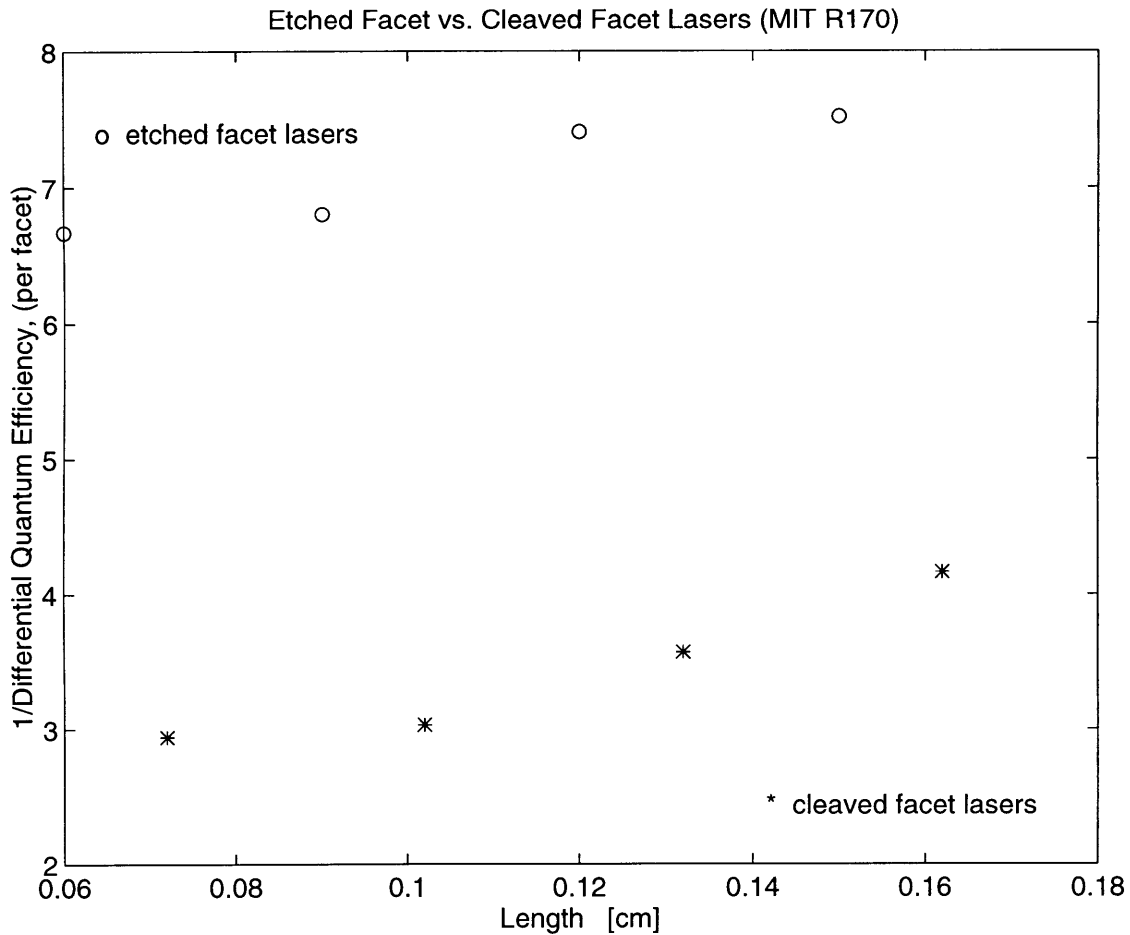


Figure 4.13: External differential quantum efficiencies of etched and cleaved facet laser fabricated from MIT GSMBE material.

isolate the effects of the facet quality from the material, good quality material is needed to carry out these experiments, since the effects of the facet losses can be overshadowed by the material losses. For example, through visual inspection the facet quality of the MIT R170 lasers seems to be worse than the ones from the LL OM661 material, the calculated mirror loss results make them appear to be better. This is partly due to the overshadowing of the mirror losses by the material losses. Extra material losses can also explain the rela-

tive sharpness of the threshold transition region in the L-I curve of MIT R170 etched facet lasers (Figure 4.8a) as compared to the ones from LL OM661 material (Figure 4.11a). Extra material losses in the MIT R170 sample dampen the oscillation in the side modes, so the scattering of the light by the mirror imperfections into these modes from the main lasing mode around threshold is not as apparent as in the case of LL OM661 low loss material. An even more serious effect than the material quality itself is the nonuniformity in the material quality. It is believed that for the MIT R170 sample, the material quality of the best etched facet lasers was much better than the material quality of the best cleaved facet lasers, due to the fact that five times as many etched facet lasers were measured. Therefore, the etched facet lasers must be compared to better cleaved facet laser to obtain more accurate (and probably lower) mirror reflectivities.

Regardless of the relatively high mirror losses and poor material quality (in the case of the MIT R170 sample), from both of these materials, functioning etched facet lasers with reasonable threshold densities and differential quantum efficiencies (especially if corrected for the uncollected light) were fabricated. These lasers can be easily used in experimental systems, even before the etch quality is improved and made more consistent.

Chapter 5

Conclusion

5.1 Thesis Contributions

The general purpose of the work described in this thesis was to develop the technology necessary to integrate in-plane surface-emitting lasers with GaAs electronics. As the base for this technology development, previous efforts in the epitaxy-on-electronics integration approach were used. These efforts were primarily accomplished by others [12, 13, 14, 15, 17, 18], but many were done with the author's involvement, including waveguide, modulator, and self-electrooptic effect device integration development. These were only briefly mentioned in Chapter 2. The developments described in this thesis are of two types. The first is the general E-o-E technology process improvements. The second type concerns the processing steps necessary for IPSEL fabrication.

There were numerous improvements made in the general E-o-E processing steps. Some of these include changing the p-type ohmic contact metal from Ti/Au to Ti/Pt or Ti/Au/Ni to improve the final Al interconnection reliability, introducing dry etching for the final aluminum interconnection, and designing optoelectronic circuits. The major accomplishments, however, were improvements in the pre-growth dielectric window preparation and post-growth polycrystalline material removal, described in Sections 2.3 and 2.4, respectively. A new configuration for the DGW was designed, which would allow for the removal of most of the dielectric stack at the commercial foundry without the risk of substrate damage, regardless of the foundry process variation. Subsequent steps for final window cleaning, which combine dry and wet processing, were also developed.

New processes had to be developed for the polycrystalline material removal because the epitaxial material was switched from AlGaAs/GaAs to the InGaP/GaAs system. Since

wet processing for this step was cumbersome and caused damage to the electronics, dry processes were developed. Both chlorine and bromine ion beam assisted etching was used for this purpose. The bromine based etch in particular has many advantages, since it occurs at lower temperatures, and photoresist can be used for the crystal protection. For this process, the unassisted spontaneous etch rate for GaAs is small, so if there are gaps in the protective photoresist or between the dielectric stack and the crystal, virtually no damage to the crystal will occur.

Most of the E-o-E technology improvements described in this thesis were done in as part of the InGaP/GaAs integration project, namely the OPTOCHIP [69]. The success of the OPTOCHIP project attests to the success of these improvements. (Multiple collaborators were involved in the OPTOCHIP project, and many improvements are credited to them as well.)

The major effort in the IPSEL process development was the development and optimization of a dry etch. Since the InGaP/GaAs material system was used instead of the more common AlGaAs/GaAs system, a new etch had to be found to be able to etch smooth vertical walls in both InGaP and GaAs. For this purpose, a novel bromine ion beam assisted etch was developed. The bromine IBAE system was assembled, and characterized on GaAs and InP substrates. Then the etch parameters were optimized using InGaP and InGaP/GaAs heterostructures. Slanted 45° etches were also performed in preparation for IPSEL deflector fabrication. Finally a method for obtain good quality etch masks was also developed. The etch parameters and mask were used to fabricate etched facet lasers (with both facets etched) in the InGaP/InGaAsP/GaAs and InGaP/GaAs materials (both with strained InGaAs quantum wells). These were measured side-by-side with cleaved facet lasers. From the threshold current density data the facet reflectivities were deduced to be 9% and 17% for the InGaP/InGaAsP/GaAs and InGaP/GaAs materials, respectively (as

compared to 30% cleaved facet reflectivity). Nevertheless, lasers with threshold current densities of less than $150 \mu\text{A}/\text{cm}^2$ and external differential quantum efficiencies of more than 29% per facet were achieved.

With the contributions of this thesis, the expertise and the equipment necessary for IPSEL OEVLSI fabrication has come into existence. This project will continue to reach the final goal of fabricating opto-electronic integrated circuits. The IPSEL structures and the optoelectronic circuits that will be used in these OEICs will be described in Section 5.4. Further improvements and characterization of the E-o-E technology processes and the dry etching used for IPSELS are needed in order to be able to fabricate high performance systems. Suggestions for further research for the E-o-E processing will be given in Section 5.2. Improvements for the IBAE system, its mode of employment, heterostructure etch optimization, and etch mask fabrication are suggested in Section 5.3.

5.2 E-o-E Technology Improvements

Most of the current problems that occur in OEIC fabrication using E-o-E technology are not intrinsic to the technology itself, but rather occur because of the specifics of the Vit-esse fabrication process, because of the lack of access to this process, and because of the lack of equipment access. When the E-o-E process is used commercially, the interaction between the electronic and optoelectronic fabrication facilities will be very close. Perhaps, slight changes will be needed in the details of the interconnection metal and the dielectric stack. Furthermore, any changes in the electronic process will have to be made with the effect on the whole E-o-E process in mind. Ideally, changes to the interconnection metal can be made to increase its thermal stability, without compromising performance, yield, and cost of the electronic process.

State-of-the-art dedicated equipment for photolithography and dry processing will be needed for the DGW opening, and the optoelectronic device fabrication. The photolithography processes are especially important. In order to take advantage of the modern photolithography techniques, full wafer processing will be required. Furthermore, better methods of surface planarization will need to be adopted. Methods, such as chemical mechanical polishing (CMP), will make the surface of the dielectric stack much more planar, and allow for submicron pattern definition. Introduction of CMP techniques into the electronics process represents a major change in the process, but will allow for high density, high yield, and high complexity OEICs produced by E-o-E integration technology.

Other developments in silicon IC fabrication technology will eventually be applied to the GaAs technology. Applicability of these developments will need to be evaluated for the E-o-E technology. In particular, using lower resistivity metals, such as copper, instead of aluminum will be of a particular advantage to GaAs ICs. Thus, an investigation of copper interconnect thermal stability will need to be conducted. It might even be the case that copper interconnects could be more thermally stable due to the better diffusion barrier technology they require, and thus will be advantageous to the E-o-E technology.

Finally, more complete DGW substrate quality studies still need to be conducted in order to assess the amount of contamination and damage various process steps introduce. The processes that should be investigated first would include the DGW preparation in the laboratory. Effects of dry etching of the dielectric stack need to be investigated. In particular, effects of gas composition, chamber cleaning procedures, and overetching need to be looked at. Wet etching and sample degreasing procedures should also be investigated. To conduct these investigations, both bulk and chip samples should be used. Primary surface investigations can be done using normal surface morphology and surface composition study techniques, such as optical and electron microscopy, atomic-force microscopy,

Auger spectroscopy, and others. Study of the epitaxial material quality grown on these surfaces will also be important. For the epitaxial material characterization, photoluminescence, cathodoluminescence, and optical loss studies can be conducted in addition to microscopy.

5.3 Improvements on IBAE Configuration and Operation Procedure

The most important motivation for modifying the IBAE system and its mode of operation is to obtain more consistent etching performance. For example, etched facet laser performance reported in Section 4.4 would have been improved if the optimal etching conditions obtained during the etch optimization described in Section 3.6 were achieved again during the laser fabrication. Upon comparing the etch quality demonstrated during the etch study, Figure 3.12a, and during facet fabrication, Figure 4.7, for the GaAs core heterostructure, and the etch optimization, Figure 3.12b, and laser facet, Figure 4.10, for the InGaAsP core material, insufficient etch reproducibility can be seen. The cause of the etch inconsistency lies in the insufficient control of bromine flow, substrate temperature, and beam current density, and perhaps ion impingement angle.

Currently, bromine flow is controlled by a leak valve, and is measured by aligning one of the two nozzles from which bromine comes out with a nozzle of a pressure measuring device (Baratron). The flow is adjusted before commencement of the etch, but only periodic measurement and adjustment occurs during the etch, since the nozzles are not aligned during the etch. An inconsistency in the established bromine flow can occur in the alignment of the nozzles. Though they are about 1.5 cm apart, slight change in the alignment changes the Baratron reading, and variations of about 5% often occur. At some operating points, this can have a relatively significant effect on the etch rate, as can be seen in Figure 3.8. Consequently, the first improvement suggestion to the IBAE system would be to install a stop for the Baratron nozzle handle, so that this nozzle is always brought to the

same point. Even with the improvement in the nozzle alignment, the bromine flow fluctuates during an etch, often without the operator's knowledge. Thus, installation of a mass flow controller, which measures and controls the flow automatically, would be the best solution. As is done presently, the bromine lines should be pumped out to the low 10^{-7} Torr range after each etch to avoid mass flow controller degradation.

Etch characteristics are very sensitive to substrate temperature, so good control of the temperature is important. The discrepancy in the substrate temperature in our system is primarily due to the inconsistent thermal contact between the stainless steel sample holder and the sample. Small gaps can sometimes occur between parts of the sample and holder. This is particularly the case for small samples held at the very edge by one clip. Thus, the clipped sample should always be inspected visually for any gaps before inserting the loader into the machine. If possible, two clips on opposite side should also be used. However, using an adhesive film between the sample and the loader would be the method of a higher likelihood of providing a consistent thermal contact. A material with good thermal conductivity would be optimal, but any material would be an improvement because it would provide better thermal conductivity than vacuum. An important consideration for the choice of adhesive material is its subsequent removal. The sample should be easily removed from the holder, and it would be preferable to have a smooth surface on the back of the sample after the removal. Furthermore, no contamination of the front of the sample should occur, since it would compromise further processing steps. Contamination during the etch should also be avoided, and therefore the adhesive material should be removed from the periphery of the sample prior to etch. The material should also not outgas significantly. Finally, the adhesive material should be able to withstand temperatures up to 150°C .

Indium, wax, and vacuum grease are some of readily available materials. Indium is the alternative with the highest heat conductivity. It can be applied easily on the heated sample holder, but is a little harder to remove. Procedures for removal are often used in the MBE practice. Waxes, such as “Crystal Bond”, can be applied on a heated holder, and can be removed with a solvent. They, however, have low thermal conductivities, and could conceivably leave residues even after solvent cleaning.

In addition to bromine flow and substrate temperature, ion beam current density consistency is important. The current inconsistency stems from possible inconsistent measurement of the current, neutralization of the beam, and ion production. This inconsistency manifests itself in the drop of the unneutralized ion beam current density with an increase in the cathode current beyond a certain cathode current. The maximum ion current density and the cathode current at which it occurs increases with increasing beam voltage. Beyond this point, however, the total beam current displayed by the ion source supply continues to increase. This effect is not described in the literature, which reports continuously increasing beam current densities until saturation (not decrease) occurs at high cathode currents [50, 51]. One explanation of this phenomenon could be excessive space charge formation and consequent spreading of the beam. This phenomena causes a problem, since the current is measured before neutralization, and when space charge decreases after neutralization, the actual beam current density can be larger than expected. Thus, the first suggestion for possible improvement in the equipment and it's operation would be to install a power supply to bias the Faraday cup to deflect the electrons in the neutralized current, so that the ion beam current can be measured after neutralization. This would further allow for a better correspondence between the displayed total ion beam current and the measured ion beam density by the Faraday cup. Thus, the control of beam current density during the

etch (when the Faraday cup is out of the beam) can be more reliably done by the total beam current reading.

Many of the ion beam current inconsistency problems are also caused by the difference of the cathode and neutralizer filament performance in the presence and absence of bromine. This is particularly true for the neutralizer filament, which is much more exposed to the bromine flow. Thus, installing a hollow cathode neutralizer, in which the active components are much farther removed from the bromine, in place of the filament neutralizer should further improve ion beam current consistency. Finally, once the Faraday cup bias supply is installed, the ion beam current density should be measured prior to etch with the neutralization and bromine present. This current density should be the one to be used as the etch parameter.

5.4 IPSEL Fabrication

The work done for this thesis produced etched facet lasers and 45° deflectors in InGaP/GaAs material system. For the final completion of the project, an integrated OEIC system must be made with single mode parabolic-deflector IPSELS. The first step in this process is to fabricate parabolic-deflector broad area lasers. For this step the titanium oxide mask definition process will have to be established. Furthermore, once the suggestions in Section 5.3 are implemented, optimum etch parameters will need to be reestablished. More precise etch rates for InGaP and GaAs can then be obtained. These, together with a heated motorized tilted stage (currently under construction) will be used to etch the facet and the deflector separately. To make a single mode laser a ridge will also have to be etched. A proposed structure is shown in Figure 5.1. The ridge will be etched through the whole laser cavity length, except at the ends. The large section at the end will provide for more alignment tolerance for the facets and deflectors. The distance between the facet and the deflector is one of the critical parameters in this structure, and to keep it fixed, a self-

aligned process will be used, where the same mask will define both the facet and the deflector. The top contact will be defined inside the stripe, whereas the bottom contact will be made through the wafer for bulk devices, and through the implant and ohmic metal on a chip.

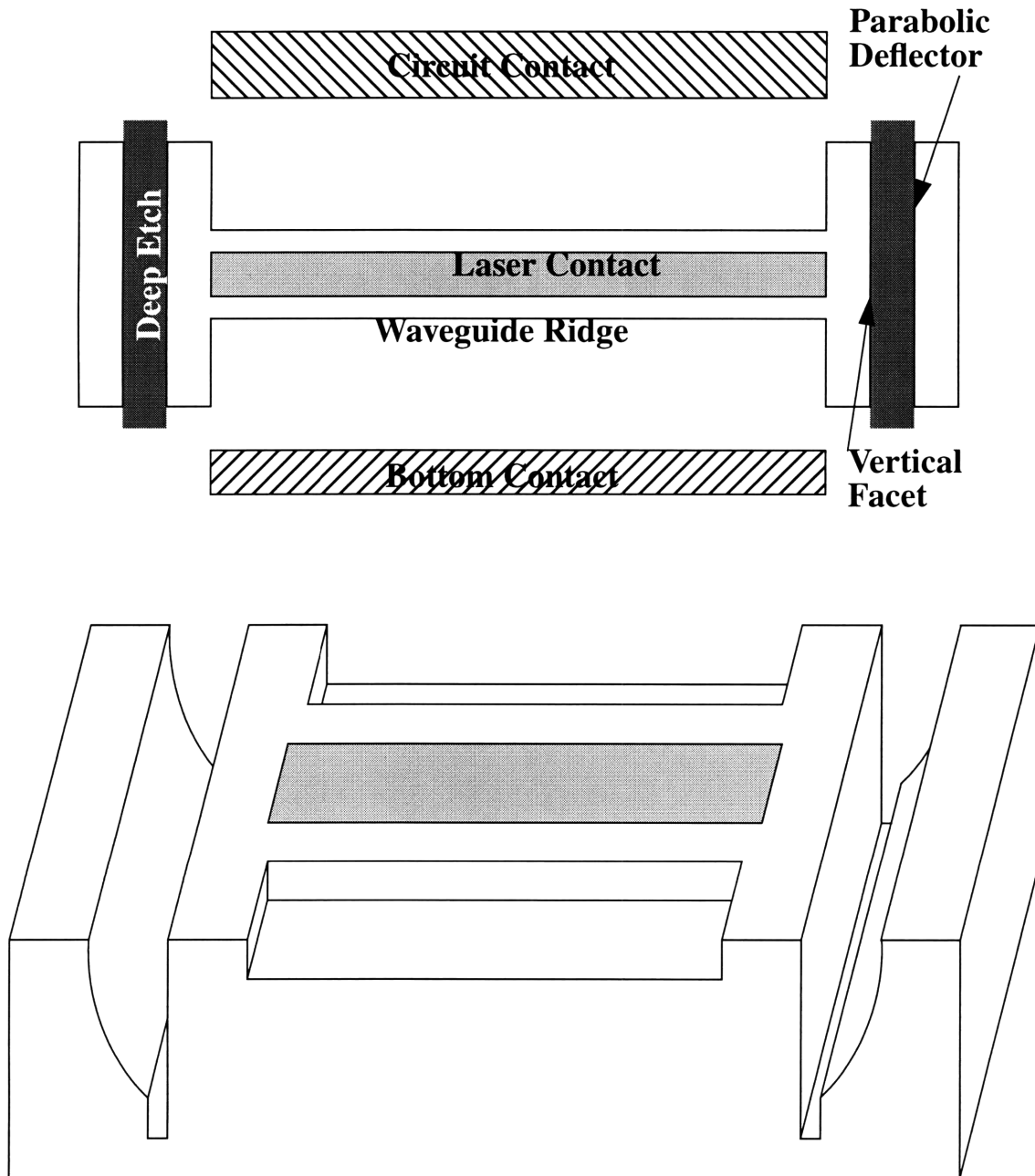


Figure 5.1: Top and side view of a proposed single-mode parabolic-deflector IPSEL.

The single-mode parabolic-deflector IPSELS will be integrated with GaAs transistors and detectors. A chip containing test structures for integration has already been designed, and submitted for fabrication. A cell from this design is shown in Figure 5.2.

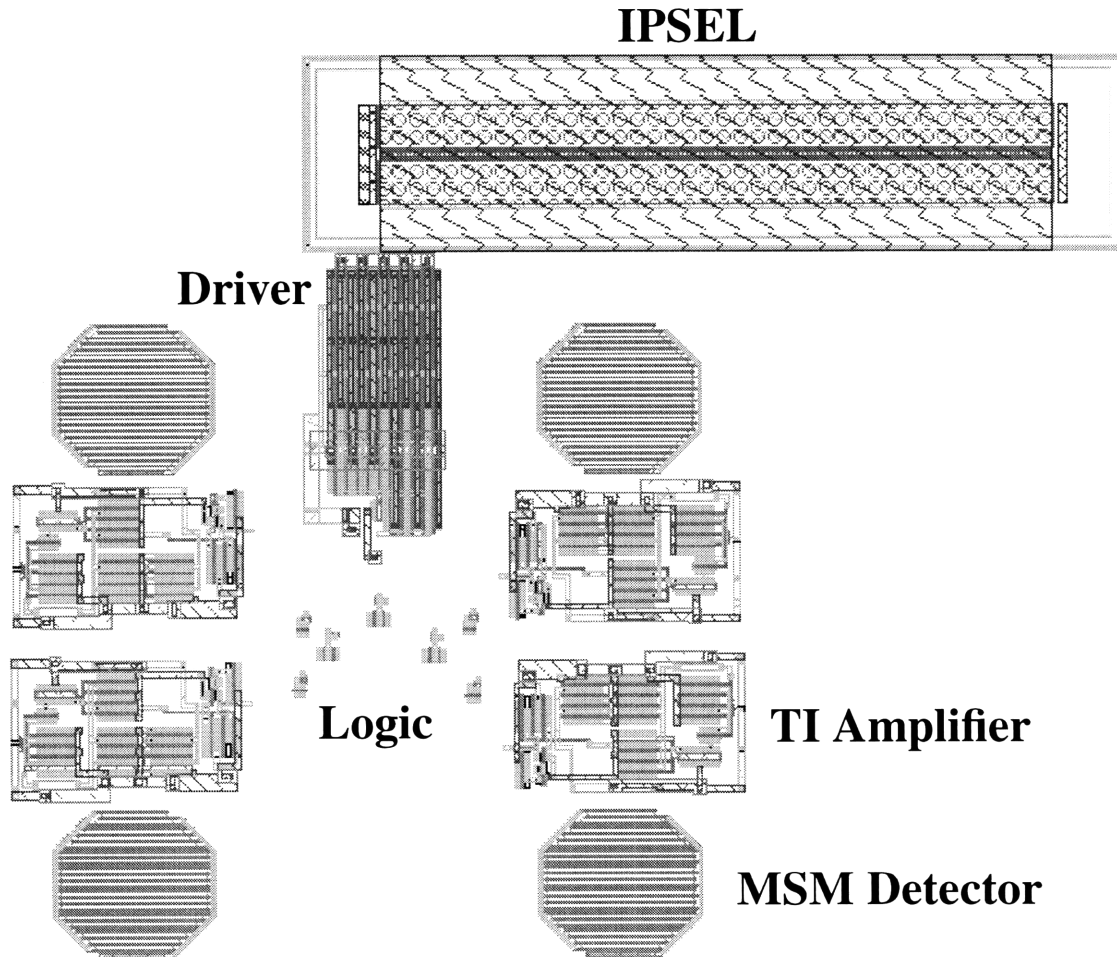


Figure 5.2: An optoelectronic logic gate cell, including PSEL, driver, photodetectors, amplifiers, and DCFL logic [89].

This cell [89] includes the IPSEL, which will transmit the output signal. Four input signals will be detected by MSM detectors, amplified by transimpedance amplifiers, and processed by DCFL logic. Cells like these will be arrayed to form OEVLSI circuits. In the future such arrays will be put together with refractive and reflective optical components to

make highly parallel specialized computation systems, operating at about 1GHz. In order to be able to use the Vitesse fabricated detectors, the laser quantum well would have to be changed from InGaAs to GaAs, and the core (well barrier) layer will have to be lattice matched InGaAsP. This would require additional epitaxial growth effort, but should not effect the fabrication procedures.

The IPSEL OEVLSI is an intermediate step to high-density OEVLSI. For many applications, IPSELS will be replaced with vertical-cavity surface-emitting lasers (VCSELs), which have smaller areas and lower threshold currents, both requirements for high-density integration. Other optoelectronic circuits will also be integrated using E-o-E technology. Edge-coupled devices, such as edge coupled lasers, waveguides, modulators, switches, and detectors, or any combinations of these, are all possible candidates. For some of these devices, such as waveguide couplers, submicron pattern definition is required. Thus, their development must be postponed, until better dielectric stack planarization is introduced into the Vitesse process and full-wafer projection alignment photolithography patterning is available for the optoelectronic device fabrication.

Appendix A

Fabrication Procedures

A.1 Dielectric Growth Window Cleaning

A.1.1 Initial Chip Degreasing

Chips are soaked in 1-methyl 2-pyrrolidinone (NMP), heated to 90°C, for 10 minutes. The NMP soak is continued in an ultrasonic bath in the same solution for 10 more minutes, then soaked in acetone in an ultrasonic bath for 10 minutes, then in methanol in an ultrasonic bath for 10 minutes. The chips are rinsed individually in isopropanol spray, and blow dried. Next, the chips are soaked in heated trichloroethane (TCA) for 10 minutes. The soak is continued in the same solvent in an ultrasonic bath for 10 minutes, then in acetone in an ultrasonic bath for 10 minutes, then in methanol in an ultrasonic bath for 10 minutes. Each chip is rinsed individually in isopropanol spray, and blow dried. (The chips are degreased in batches by keeping them in a Teflon subdivided dipper during the soaks and transfers. The dipper and beakers are designated specifically for this process. Transfer from one solvent to the next should be done quickly, so that the samples do not dry during the transfer. For this reason, cooling of the heated solvents is essential before transfer.)

A.1.2 Bondpad Protection Oxide Deposition

About 0.7mm of silicon oxide is deposited after the degreasing. The usual method of deposition was sputtering, since it provided good uniformity, oxide density, and sidewall coverage. During sputtering equipment malfunction, PECVD and pyrolytic silicon oxide deposition systems were also used.

A.1.3 Photolithography

Chips are briefly dehydrated on a 120°C hotplate. Hexamethyldisilazane (HMDS) is liberally deposited on the samples to promote photoresist adhesion and allowed to rest for 10 seconds before spinning. The HMDS is then spun at 3krpm for 40 seconds. Shipley

1827 photoresist is spun at 3krpm, for 40 seconds. (The type of spin chuck used is important to obtain proper resist thickness uniformity and reduce the extent of the edge bead. The chuck used is flat with a single hole, large enough in diameter that a bubble of resist can be formed over the chip, starting well outside the chip boundary, but not spilling from the sides of the chuck.) The edge bead is removed with a razor blade wrapped in a cleanroom wipe. Photoresist is removed from the back of the sample with cleanroom compatible swabs lightly soaked in acetone. Softbaking of the resist is done on a 120°C hotplate for 90 seconds. The photoresist is exposed for 60 seconds on a standard Zeiss contact aligner, with 6 mW/cm² intensity. The photoresist is developed in Shipley MF319 Positive Photoresist Developer for 120 seconds. Hardbaking of the photoresist is done in a 130°C oven for 15 minutes.

A.1.4 Dielectric Stack Dry Etching

Dry etching is done in a MIT Microlab Plasmatherm Series 700 RIE system which is usually pumped down to 3×10^{-5} Torr before etching. The samples are O₂ plasma cleaned for 5 minutes under the following conditions: O₂ flow - 50 sccm, pressure - 50 mTorr, power - 100W, DC bias - 100V. The dielectric stack is dry etched most of the way to the substrate in the DGWs with CHF₃/O₂ plasma under following conditions: CHF₃ flow - 45 sccm, O₂ flow - 2.5 sccm, pressure - 50 mTorr, power - 210W, DC bias - 180V. The etch is 5.5-5.75 hours. About 0.1-0.2µm and 0.5µm of dielectric remains in the implanted and unimplanted regions, respectively. The sample is then oxygen plasma cleaned for 10 minutes under the following conditions: O₂ flow - 50 sccm, pressure - 50 mTorr, power - 210W, DC bias - 200V. Photoresist is stripped after the dry etch.

A.1.5 Photoresist Stripping

Each chip is rinsed in an acetone stream, soaked in acetone in an ultrasonic bath for 10 minutes, and soaked in NMP, heated to 90°C, for 10 minutes. The NMP soak is continued in an ultrasonic bath in the same solution for 10 minutes. NMP is rinsed in an acetone

ultrasonic bath for 10 minutes, which in turn is rinsed in a methanol ultrasonic bath for 10 minutes. Finally, each chip individually rinsed in an isopropanol spray, and blow dried.

A.1.6 Dielectric Stack Wet Etching.

The bottom portion of the dielectric stack in the DGWs is wet etched in Buffered Oxide Etch (BOE). Etch time depended on the amount of undercutting, 6-12 minutes. Etch is repeated until the bottom of the DGWs is crystal color, then one more wet etch is done. After each etch, the photoresist is stripped and repatterned as described above. A minimum of two wet etch steps are done.

A.2 Polycrystalline Material Removal

A.2.1 Chlorine ECR IBAE

Silicon oxide, 0.3 μ m, is deposited on the chip. Shipley 1827 is patterned as described above to protect the crystalline material. The oxide is etched in the MIT Microlab RIE for 60 minutes, under the following conditions: CF₄ flow - 45 sccm, O₂ flow - 5 sccm, pressure - 50 mTorr, power - 210W, DC bias - 185V. The photoresist is removed with acetone, and then the acetone is rinsed off with methanol. The polycrystalline material is etched in a chlorine Ion Beam Assisted Etching (IBAE) system for 18 minutes under the following conditions: Ar flow - 3 sccm, Cl₂ flow - 9 sccm, ion beam current - 40 mA/cm², ion beam voltage - 500V, substrate temperature 195°C. Shipley 1827 photoresist is patterned as above to protect the dielectric stack, and to expose the oxide on top of the crystalline material. This oxide is wet etched in BOE for 3 minutes. The photoresist is stripped with acetone spray.

A.2.2 Bromine Kaufman Gun IBAE

Chips are briefly dehydrated on a 80°C hotplate. Hexamethyldisilazane (HMDS) is liberally deposited on the samples and allowed to rest for 10 seconds before spinning. HMDS is spun at 5krpm, for 30 seconds. Shipley 1650 photoresist is then applied and spun at 5krpm, for 30 seconds. The edge bead is removed with a razor blade wrapped in a

cleanroom wipe. Photoresist is removed from the back of the sample with cleanroom compatible swabs lightly soaked in acetone. Softbaking of the resist is done on a 80°C hotplate for 20 minutes. The photoresist is exposed for 60 seconds on a standard Zeiss contact aligner, with 13mW/cm² intensity. The photoresist is developed in 5:1 H₂O to Shipley 351 Positive Photoresist Concentrated Developer for 36 seconds. Hardbaking of the photoresist is done in a 120°C oven for 15 minutes.

The polycrystalline material is then etched for 75 minutes in the bromine IBAE under the following conditions: Ar flow - 3.0 sccm, Br₂ flow - 6.0 mTorr reading, ion beam voltage - 600V, ion beam current - 60mA/cm², substrate temperature - 70°C. The photoresist is stripped in an acetone spray, and the acetone is removed with methanol and isopropanol.

A.3 Bulk Etched Facet Lasers

A.3.1 Degreasing

The samples are rinsed in a trichloroethylene (TCE) stream for 1 minute, rinsed in an acetone stream for 30 seconds, rinsed in a methanol stream for 30 seconds, rinsed in an isopropanol stream for 15 seconds, and low dried with pressurized nitrogen.

A.3.2 Etch Mask Deposition and Patterning

A PlasmaLab Microwave Plasma Enhanced Chemical Vapor Deposition (PECVD) system is used to deposit about 0.6-0.7µm of silicon oxide, with following the process parameters: NO₂ flow - 60%, SiH₄/N₂ - 11%, pressure - 200mTorr, microwave power - 200W, substrate temperature - 350°C, time - 24 minutes.

The sample is briefly dehydrated on a 80°C hotplate (unless it is just after PECVD) Hexamethyldisilazane (HMDS) is liberally deposited on the samples and allowed to rest for 10 seconds before spinning. HMDS is spun at 5krpm, for 30 seconds. Shipley 1400-17 photoresist is then spun at 5krpm, for 30 seconds. Photoresist (if any is present) is removed from the back of the sample with cleanroom compatible swabs lightly soaked in

acetone. Softbaking of the resist is done on a 80°C hotplate for 20 minutes. The photoresist is then exposed for 7 seconds on a standard Zeiss contact aligner, with 13mW/cm² intensity, using “ROYTER3 LASERS ETCH NEG” or “ROYTER3 LASERS 90 MINUS” masks. Careful alignment of the mask to the crystallographic axis of the sample, indicated by the cleave, is critical. After exposure, the sample is soaked for 8 minutes in chlorobenzene. The photoresist is then developed in 3:1 H₂O to Shipley 351 Positive Photoresist Concentrated Developer for 10-12 seconds.

Next, the sample is coated with 60 nm of Ni in a electron-beam evaporator, which is evacuated to about 3x10⁻⁷ Torr before evaporation. The metal on top of the photoresist is lifted off with regular and compressed nitrogen forced acetone sprays. Acetone is removed with methanol and then isopropanol, and then the sample is blown dry with nitrogen.

The silicon oxide with the Ni etch mask is etched in a SemiGroup RIE for 200 minutes under the following conditions: PDE100 (CF₄/O₂(17%)) flow - 70%, pressure - 160-170 mTorr, power - 12% (63W), DC bias - 250V. The sample is oxygen cleaned before and after the etch in the same chamber. The pressure before the start of the etch is 2x10⁻⁶ Torr.

Nickel is etched from the sample in sulfuric acid based Transene Nickel Etchant, heated to 50°C, for 5 minutes. The sample is etched in Transene Buffered HF for 3 seconds before loading in the IBAE.

A.3.3 Facet Etch

The facets are etched with the above etch mask in the bromine Kaufman gun IBAE system under the following conditions: Ar flow - 3.0 sccm, Br₂ flow - 6.0 mTorr reading, ion beam voltage - 600V, ion beam current - 60-70mA/cm², substrate temperature - 110°C for the quaternary active layer lasers and 90°C for the GaAs active layer lasers, time - 50 minutes for the quaternary active layer structures and 40 minutes for the GaAs active layer

structures. The sample is cleaned with an Ar ion beam with the above parameters for 2 minutes, before the commencement of the etch.

A.3.4 Contact Patterning

The silicone oxide mask is stripped in Transene Buffered HF. Chips are briefly dehydrated on a 80°C hotplate. Hexamethyldisilazane (HMDS) is liberally deposited on the samples and allowed to rest for 10 seconds before spinning. HMDS is spun at 5krpm, for 30 seconds. Shipley 1650 photoresist is spun at 5krpm, for 30 seconds. Photoresist is removed from the back of the sample (if any is present) with cleanroom compatible swabs lightly soaked in acetone. Softbaking of the resist is done on a 80°C hotplate for 20 minutes. The photoresist is exposed for 60 seconds on a standard Zeiss contact aligner, with 13mW/cm² intensity, using “ROYTER2 LASERS POSITIVE” mask. Etched alignment marks on the sample and masks are used for alignment. The sample is soaked in chlorobenzene for 20 minutes. The photoresist is developed in 3:1 H₂O to Shipley 351 Positive Photoresist Concentrated Developer for 30 seconds. The sample is then immediately loaded into the evaporator.

30 nm of Ti, followed by 0.6µm of Au are evaporated onto the sample in an electron-beam evaporator. The metal on top of the photoresist is lifted off with regular and compressed nitrogen forced acetone sprays. The acetone is removed with methanol and then isopropanol, and the sample is blown dry with nitrogen.

A.3.5 Isolation Etch

Chips are briefly dehydrated on a 80°C hotplate. Hexamethyldisilazane (HMDS) is liberally deposited on the samples and allowed to rest for 10 seconds before spinning. HMDS is spun at 5krpm, for 30 seconds. Shipley 1650 photoresist is spun at 5krpm, for 30 seconds. Photoresist is removed from the back of the sample (if any is present) with cleanroom compatible swabs lightly soaked in acetone. Softbaking of the resist is done on a 80°C hotplate for 20 minutes. The photoresist is exposed for 60 seconds on a standard

Zeiss contact aligner, with 13mW/cm^2 intensity, using “ROYTER4 ETCHED FACET LASERS” mask. Gold alignment marks on the sample and masks are used for alignment. The photoresist is developed in 5:1 H_2O to Shipley 351 Positive Photoresist Concentrated Developer for 36 seconds. The photoresist is hard baked in 120°C oven for 20min.

The sample is then etched for 12 minutes in the bromine IBAE under the following conditions: Ar flow - 3.0 sccm; Br_2 flow - 6.0 mTorr reading, ion beam voltage - 600V, ion beam current - 60mA/cm^2 , substrate temperature - 60°C . Photoresist is stripped in acetone spray, and the acetone is removed with methanol and isopropanol.

A.3.6 Lapping, Polishing, and Backside Contact

A 3” quartz optical flat is heated on a hot plate to about 100°C , and white wax is melted in the center and four locations close to the perimeter, each 90° from the other. The sample is placed up side down in the center, and blocking pieces of GaAs are placed polished side up in the four other melted puddles of wax. The GaAs pieces have to be at least as thick as the sample. All the pieces are gently moved around to distribute the wax evenly underneath. The flat is removed from the hot plate, a piece of Nitrile (section of a thick old glove) is placed on top, and a weight, slightly larger than the sample is placed on top of the sample, but not on the blocking pieces. The optical flat is allowed to cool, and the excess wax is rinsed off in a stream of trichloroethylene. The edges of the sample and the blocking pieces are gently scraped with a razor blade to remove excess wax, however contact with the sample is minimized. The optical flat is rinsed with TCE again. (Excess wax on top of the sample and blocking pieces will cause uneven material removal. Furthermore, excess wax anywhere will bind grit particles together, making larger size grit, which will cause scratching of the sample that could cause false cleaves.)

A thin grit paste is deposited on a surface of a large (10”) optical flat, ground to have an intentional roughness of $12\mu\text{m}$. The paste consists of dry grit and a lubricating solution

of either or both “Basic H” soap solution and lubricant. The optical flat that the sample and blocking pieces are mounted on is moved on top of the large optical flat, covered with the grit suspension, in a “figure eight” pattern, rotating the flat with the sample a quarter turn every few “figure eights”. Only very light downward pressure is provided. Depending on the sample thickness, either 9 μm or 5 μm size grit is used at first. For a particular size grit, lapping should be stopped at least ten times the size of the grit size away from the target thickness. For this project we used as much as twenty times the grit size buffer. Grit size is gradually reduced. Usually 9 μm , 5 μm , and 2 μm or 5 μm , and 2 μm grit size sequences are used. Usually, 5 μm grit is used to lap until about 275 μm sample thickness, and the 2 μm grit to 200 μm thickness. The optical flats and the vicinity of the lapping area are well cleaned to remove any of the large grit particles, each time the grit size is switched to the next smaller one. Lapping is finished with 2 μm grit.

The lapped sample, while still mounted on the small optical flat, is next polished down to the target 150 μm thickness in a 1% solution of bromine in methanol. The solution is prepared just before the polishing. A large sheet of lens paper is held down with a rubber band against another optical flat. The flat with the sample is moved in the similar motion to the one used for lapping, while the bromine/methanol solution is poured on top. The solution is used a few times until the desired sample thickness is obtained.

The thinned sample is removed from the flat by immersing them in heated TCE. The time of immersion depends on the size of the sample, and is on the order of 20 minutes. When the sample slides freely (it should not be forced to slide) on the flat, it is removed from the TCE bath. It is sprayed with TCE, as it is coming out from the bath, so that the TCE never dries. The TCE is rinsed off with acetone, and the acetone is rinsed away with methanol and isopropanol.

For the back-side contact to the n-type GaAs substrate, 30 nm of Ge, 60 nm of Au, 30 nm of Ni, and 200 nm of Au, are deposited, in that order, in an e-beam evaporator on the already polished back side of the wafer. The sample is annealed in Heatpulse 200 annealer for 30s at 450°C.

Scribing of the sample is done on Loomis scriber. The scribed sample is cleaved by placing the sample in between two pieces of thin clinging plastic, and then on top of a flexible piece of sheet metal. A metal rod is placed on top of the back side of the sample parallel to the cleave and rolled in the direction perpendicular to the cleave, causing slight flexion of the metal, and cleaving along the faults started by the scribes.

Appendix B

IBAE Standard Operation and Maintenance Procedures

The information in this appendix is intended not for the general reader, but for those who will continue the work on this project. Much of this information is possessed in parts by others who have worked and maintained this IBAE system. However, since the author participated in most of the etching runs and in many maintenance and repair sessions, information here should be useful as a cohesive description of the accumulated knowledge. The procedures listed here are just guidelines, and though the order of certain procedures is crucial, others are not. Understanding the principles of operation described in Section 3.2 and in references therein is crucial to successful operation of this equipment. Finally, the experience gained in the past year of operation of this equipment caused us to rethink the proper modes of operation. Some of the suggestions for improvements to the procedures outlined here are listed in Section 5.3.

B.1 Standard Operating Procedure

B.1.1 Sample Mounting

1. Clean the stainless steel part of the sample holder with methanol soaked cleanroom compatible wipe.
2. Arrange the clips on the sample holder, so that the sample can be positioned in the center of the beam.
3. Often, the sample is pretreated with a 3 second buffered HF etch, and a deionized water rinse before loading.
4. Sample should be clipped firmly to the sample holder. There should be no space visible between the sample and the holder. If possible, two clips should be used on opposite sides of the sample.

B.1.2 Sample Loading

1. Check inside the load lock for any damage to the o-rings.
2. Tilt the loading mechanism and shake slightly over a cleanroom wipe to check for proper mounting.
3. Insert the rod of the loading mechanism into the load lock until the outside ring of the loading mechanism is against the protrusion on the load lock. Some force will be needed to do this, and if difficulty is encountered, the vacuum valve can be opened slightly to assist the insertion. Opening the valve too much will cause excess pull on the loading mechanism, which will slam into the loading dock with possibly damaging consequences.
4. Open the valve to the mechanical pump fully.
5. Close the nitrogen bleed valve to the mechanical pump.
6. When the pressure in the load lock is stabilized and is at least below 100 mTorr, turn off the vacuum valve.
7. Turn on the nitrogen bleed valve.
8. Turn off the ion gauge
9. Open the load lock gate valve all the way.
10. Using the crank, insert the rod of the loading mechanism until the outside ring of the loading mechanism pulls back due to the rod reaching the end of the load lock.
11. Turn the ion gauge on.
12. Connect the power cord to the heater and the plugs for the thermocouples.

B.1.3 Establishing the Etch Parameters

1. Wait until an acceptable pressure. (If the vacuum system is properly operational, this pressure should be at most 1×10^{-7} Torr.)
2. If the pressure is below 1×10^{-7} Torr, readjust the Baratron reading as close to zero as possible.

3. Turn on the Variac AC voltage controller and adjust the voltage to start the substrate heating. The temperature has to be watched while establishing other parameters. When the temperature is within 3°C of the desired value, the voltage should be adjusted to the expected steady state voltage.
4. Turn off the ion gauge, and turn on the argon valve and the argon flow controller. Establish 3 sccm argon flow.
5. Turn on the ion gun control panel, and the two switches next to the on switch.
6. Turn on the cooling water valve, the thermocouple indicators, and the multimeter. Set the multimeter to AMPS and press ZERO CHECK button to turn off this option.
7. Two minutes after the argon flow has been established, briefly turn on the ion gauge to check the pressure. It should be about 2.3×10^{-4} Torr.
8. Bring the DISCHARGE voltage to 60 V
9. Increase the CATHODE current until the DISCHARGE light does not blink. This should require about 3-5 A of filament current
10. Increase the BEAM VOLTAGE to the desired value, and the ACCELERATOR voltage to 60V.
11. Increase the CATHODE filament current until the desired beam current density is established, as measured by the multimeter. (Make sure the shutter is in the zero position.) Note the beam voltage supply current.
12. Increase the NEUTRALIZER current until the beam current density is approximately zero, as read on the multimeter. Make sure the current does not go above 7 Amps.
13. Recheck and adjust the voltages. Adjust the CATHODE filament current so that the beam voltage supply current is again at the value noted before, and then readjust the NEUTRALIZER current.

14. At this point all the beam parameters are established, and the sample preclean procedure can be performed. If this is desired, open the shutter by rotating it counterclockwise. Two minutes is the usual duration of the preclean.

15. During the pre-etch sample cleaning, make sure the bromine leak valve is closed. Then, open the bromine bottle by turning the stopper 1.5 turns. Open the valve to the chamber. The leak valve isolates the bromine from the chamber. This step can be performed any time after the argon is turned on to allow the bromine pressure in the tubing to stabilize.

16. Close the shutter by bringing it to the zero position.

17. When the temperature is finally established, bring the Baratron nozzle in front of the bromine inlet nozzle. (Observation can be done directly through the window port, or through the mirror.)

18. Slowly open the leak valve, observing the relative pressure on the Baratron readout. Bring the pressure to the desired value. For consistency, adjust the position of the nozzle to maximize the reading.

19. Move the Baratron nozzle away from the bromine nozzle.

20. Bring the NEUTRALIZER current to 7 Amps to compensate for decreased emissivity in the presence of bromine.

21. Adjust the CATHODE current to bring the beam voltage supply voltage to the previous value.

B.1.4 Etching

1. Make sure the substrate temperature and ALL the beam parameters are correct.

2. Open the shutter (counter-clockwise) and start timing the etch.

3. Regulate the temperature by making slight adjustments of the Variac voltage throughout the etch.

4. Keep the beam voltage supply current constant by adjusting the CATHODE filament voltage.
5. Every 10-15 minutes check the bromine flow by briefly aligning the Baratron and the bromine inlet nozzles.
6. Check over the system periodically during the etch.

B.1.5 System Shutdown

1. Close the shutter when the etch is over.
3. Close the bromine bottle.
3. Turn off the Variac supplying the substrate heater.
4. Realign the nozzle, and pump out the bromine tubing by opening the leak valve a little at a time. To make sure the bromine flow does not go too high, keep the Baratron reading around 9.0. Keep the ion beam on during this stage.
5. After the leak valve is totally open (100-200 on the dial), allow the reading on the Baratron to decrease below 0.150 before shutting off the ion beam.
6. To shut down the beam, lower the NEUTRALIZER current, BEAM VOLTAGE, ACCELERATOR voltage, CATHODE current, and DISCHARGE voltage, in that order, until all of the knobs are rotated fully counter-clockwise. Also shut off the multimeter.
7. Allow the argon to flow for another 5 minutes before shutting it off. First, turn off the flow, then the flow controller, then the valve. Move the nozzle away.
8. Pump on the bromine tubing until the pressure in the chamber is below 5×10^{-7} Torr. Then shut turn off the leak valve, and shut off the gas valve.
9. Turn off the cooling water and the thermocouple.

B.1.6 Unloading

Unloading can be done anytime after the ion beam is turned off. Unloading during argon flow slightly reduces the backflow of air. Unloading after the system has pumped down allows for the sample holder to cool and outgas.

1. If the ion gauge is on, turn it off.
2. Using the crank, pull out the sample holder rod.
3. Close the gate valve and turn on the ion gauge.
4. Vent the loadlock with nitrogen.
5. Pull out the loading mechanism, and remove the sample.
6. Turn off the nitrogen and cover the loadlock with a protective cover.

B.2 System Maintenance

Consistency is very important in etching. To retain consistent performance, the etching system has to be regularly maintained. Maintenance is particularly important due to the use of corrosive gasses in this system. Proper procedures of maintaining pumps, the vacuum chamber, the ion source, and the gas supplies is outlined here. Most of these procedures are common to the operating procedures for other vacuum equipment with corrosive gasses. So far, no major differences were noticed with the bromine system as compared to the chlorine system. Perhaps, in the next year, these differences will be more evident. A very important part of maintenance is the regular observation of system behavior and performance. Such observation will also help in learning more about the system.

B.2.1 System Observation

Due to the experimental nature of the system, it is very important to observe as many parameters as possible when the system is running or is in the standby state. Observations should then be compared to previous observations. To assist with this task, the *Run Sheet*

should be filled out during each run, while comparing the recorded parameters with previous *Run Sheets*. The following parameters should be regularly observed.

1. *Chamber Pressure*. Overnight (close to steady state) chamber pressure should be observed. Also, pumpdown time to 1×10^{-7} Torr and to the steady state pressure should be noted. The chamber pressure should be looked at as often as possible in case a power failure shuts down the cryogenic pump.

2. *Mechanical Pump Pressure*. Normally the thermocouple should read 60-100 mTorr due to the nitrogen bleeder. If it is lower, the nitrogen bleeder valve should be checked. If the pressure does not go below 10 mTorr when the nitrogen is turned off, the pump should be checked. Oil change or pump rebuilding might be required.

3. *Argon Flow*. If the proper flow during the etch cannot be established or if for a certain flow the ion gauge or the Baratron readings are different than before, the argon supply should be checked. The Baratron pressure should be checked during the etch as well.

4. *Bromine Flow*. If significant changes of the leak valve position required for a certain flow is observed, the presence of bromine in the bottle should be checked. Otherwise, bromine level should only be checked every few months. If bromine is present, the leak valve might have to be cleaned or replaced. The Baratron pressure should be checked during the etch as well.

5. *Ion Beam Power Supplies*. The stability of the BEAM VOLTAGE, DISCHARGE, and ACCELERATOR voltage supplies should be checked during etching. The currents through CATHODE and NEUTRALIZER filaments required to obtain certain ion beam current density and neutralization for it should be compared with previous values. If these values change significantly from one run to another, these filaments should be changed soon. If the maximum ion beam current density drops significantly from one run to the other, first the shutter position should be checked, and if set at zero, then the filaments

should be suspect. During the etch, when the shutter is open, the BEAM CURRENT should be checked periodically. In case of a sudden change, all the parameters should be rechecked, and etch terminated. Of course, argon flow change can also be a cause of such changes. Finally, the ACCELERATOR CURRENT, which is displayed by default on the right display on the supply panel, should be checked for consistency.

6. *Loadlock Pumpdown.* The pumpdown pressure of the loadlock should be relatively constant. If increases are observed, then the rod of the loading mechanism and the o-rings in the loadlock should be checked.

B.2.2 Vacuum System Maintenance

The most common maintenance task on the vacuum system is the cryogenic (cryo) pump regeneration. Venting the chamber occurs even more often, but will be described with the ion beam source maintenance procedure. Due to corrosive gas pumping, it is a good idea to regenerate the cryo pump often. Every time or every other time the filaments are changed is a reasonable frequency. Simultaneous regeneration and venting can be performed, however it might be best to do them separately, so that sources of leaks can be isolated more easily. The following procedure should be followed during a cryo pump regeneration:

1. Close the cryo pump gate valve.
2. Shut off the cold head and the compressor.
3. Close off the valve between the mechanical pump and the common access port.
4. Open the nitrogen flow valve to the common access port.
5. Open the valve between the common access port and the cryo pump (the one BELOW the gate valve).
6. Wrap a heating strap around the cryo pump, and insert a thermocouple between it and the pump. Heat the pump somewhere between 70-90°C overnight with the nitrogen flow-

ing through.

7. Turn off the heat and let the pump cool a couple of hours.

8. Open the pump exhaust port, and unscrew the pop-out exhaust valve.

9. Clean the o-ring on the exhaust valve well with methanol.

10. Turn off the nitrogen to the common access port. Replace the exhaust valve. Improper execution of this step is the most likely cause of improper pump operation. Reattach the exhaust port.

11. Open the valve to the mechanical pump to start pumping on the cryo pump. Make sure the nitrogen bleeder valve is closed.

12. Turn on the heat to the cryo and allow the mechanical pump to pump for several hours.

13. The thermocouple vacuum gauge should be zero, when the heat to the pump is turn off. Allow to cool for a couple of hours.

14. Close the valve to the mechanical pump, and observe the TC gauge for a rise in pressure. If a rise in pressure is observed, there could be a problem with the seating of the exhaust valve, and the procedure from Step 8 might have to be repeated after the pump is revented with nitrogen.

15. Close the valve between the cryo and the common access port. Open the valve between the mechanical pump and the common access port, and turn on the nitrogen bleeder valve.

16. Turn on the cold head. 30 seconds later turn on the compressor. Allow the pump to cool for a couple of hours. If frost on the outside is observed, there is a leak, and the whole procedure has to be repeated.

17. Make sure the main chamber is pumped out. To check this, close the bleeder valve, close the mechanical pump valve, and open the valve between the chamber and the com-

mon access port. If the pressure is below zero then no pumping is necessary. If not, then open the mechanical pump valve, and pump for a while. Then close the chamber valve, and open the bleeder valve.

18. Open the cryo pump gate valve. After some pumping, the ion pressure gauge can be turned on. The pressure should drop to the steady state overnight if the cryo was properly regenerated.

B.2.3 Changing the Filaments

Both the cathode and the neutralizer filaments degrade due to ion sputtering and reaction with corrosive species. This degradation can be seen as a change in the filament current needed to obtain the same beam current. We also observed the unneutralized maximum beam current density to decrease over time. Eventually, the filament becomes thin and breaks. The system manual suggested a change of filament of every 20 usage hours. Even when corrosive bromine was used, up to 24 hour filament change period has been used. Only one filament (neutralizer) failure has been observed for this filament change schedule. However, performing important etches with more than a 20 hour old filament is not recommended. It is very difficult to change the filaments alone, so two people should be present. The following procedure should be used to change the filaments:

1. Wrap a heating strip around the main chamber, insert a thermocouple in between, and heat the chamber at about 90°C overnight.
2. Allow the chamber to cool.
3. Close the cryogenic pump gate valve.
4. Close the mechanical pump valve to the common access port.
5. Open the chamber valve to the common access port.
6. Open the nitrogen valve to the common access port. The pressure on the TC gauge should start to go up.

7. Loosen the screws on the cathode filament port.
8. Unscrew the argon line connection.
9. Unscrew, and take out the bolts for the bolts of the ion gun port. Leave two loose bolts in to hold the gun.
10. When the chamber pressure is at atmosphere, take out the argon gun plastic tubing. Then pull out the whole ion gun assembly.
11. Remove the copper gasket.
12. At this point, cleanroom compatible gloves should be used to protect the gun. Unscrew the two nuts that are holding the straight neutralizer filament, and remove the filament itself.
13. Replace the filament. It should be straight, but not too taut.
14. Place the gun assembly back onto the port keeping the correct gun orientation. Use a new copper gasket. Make sure the gasket is seated properly! The bolts should all be inserted, and they should be tightened just to make sure everything is held in place.
15. Fully unscrew the cathode filament assembly and take it out.
16. Unscrew the nuts holding the cathode filament and take it out.
17. Replace it with a new piece of piece of tungsten filament, so that it forms a U shaped bend about 1 inch long. Use the previous filament as a guide. If the filament is too long or wide, it will short to the anode or the body.
18. Replace the cathode filament assembly and lightly tighten the screws.
19. At this electrical check should be performed. Remove all the electrical connections to the gun, and check for a connectivity on the cathode and neutralizer current connections, and check that the cathode is not shorted to the anode, body, or ground. Then reattach the connectors.

20. Close the nitrogen valve.
21. Place the argon line back on, and tighten it well.
22. Open the mechanical pump valve, and start pumping on the system. Make sure the bleeder valve is closed.
23. Tighten well the gun assembly port bolts, and the cathode filament assembly screws.
24. After a couple of hours, the TC gauge should read zero. If not, there is a large leak. Also, if when the mechanical valve shut, the pressure rises rapidly, there is a large leak. Tighten the ports with more force, or revent the system.
25. At this point a second electrical test can be performed by turning on the gun and seeing if the discharge voltage can be raised to 15 V and if the body voltage can be raised to 75 V. Small currents can also be applied to the two filaments to check that there is no open circuit.
26. Shut off the valve between the chamber and the common access port. Keep the mechanical pump valve open, and open the bleeder valve.
27. If the cryo pump was regenerated simultaneously, then it had to be on for at least an hour. Meanwhile the chamber should be pumped with the mechanical pump.
28. Open the cryo pump gate valve. The pressure should be back to steady state overnight.
29. If the pressure is not back to normal, the UTI mass spectrometer can be used to leak check the system with helium. If the cryo pump was regenerated, then either the ports or the cryo exhaust valve can be at fault.
30. When the system is at a normal pressure, gun operation should be checked. The gun should be run for half an hour before important etching is conducted.

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