A Three-Level Buck Converter to Regulate a High-Voltage DC-to-AC Inverter

by

Kenneth C. Schrock

[S.B. EE, M.I.T., 2006]

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology
January, 2008

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Author_____
Department of Electrical Engineering and Computer Science
January 7, 2008

Certified by_____
James C. Mayes, Electrical Engineer, Schlumberger
VI-A Company Thesis Supervisor

Certified by_____
Associate Professor David J. Perreault
M.I.T. Thesis Supervisor

Accepted by_____
Arthur C. Smith
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Theses

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ABSTRACT

A three-level buck converter is designed and analyzed, and shown to be suitable as a high-voltage down converter as a pre-regulation stage for a 600 watt DC-to-AC power inverter. Topology selection for the inverter is examined, and a three-stage system is chosen to satisfy high voltage (1.1 kV), isolation, size, and efficiency requirements. Control of the buck converter is discussed in detail, including advanced features that allow extremely low output voltages in unloaded conditions. Optimization is included for both magnetics and switching losses. A prototype of the three-level buck converter is shown to perform as expected and meet all specifications.

Thesis Supervisor: David J. Perreault

Title: Associate Professor of Electrical Engineering

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Acknowledgements

I would like to thank my parents for all of their support in my education and in life. Without them, I would not be where I am today.

I also wish to extend thanks to Professor David Perreault and Shehab Ahmed. Professor Perreault assisted with the writing of this thesis and provided support in all technical matters. Mr. Ahmed pointed me in the right direction and kept me on track while I researched and built a prototype of the converter.

Finally, I would like to thank Schlumberger for funding my thesis, providing equipment and space to work, and giving me a great six months in Texas.

1 Introduction and Background

Many electronic components are unable to operate in very high temperature applications. In these settings, only a few devices may be available and circuits that will operate in this environment must be designed around the components' limitations. In this thesis, one of these cases will be examined: a high-voltage power inverter for which the switching devices cannot tolerate the desired input voltage.

A reasonable approach to designing such a system is to first examine the possible circuit topologies. Chapter two introduces the converter requirements and discusses the design trade-offs. Topologies such as a neutral-point-clamped (NPC) inverter were considered; however, a three-stage approach was chosen, starting with a multi-level buck converter to address the aforementioned high voltage problem, followed by two H-bridge inverters that provide isolation and deliver the desired output characteristics.

Chapter three goes into further detail on the three-level buck converter. In this chapter, the experimental prototype is demonstrated, and a control system is implemented. The section concludes with a discussion of four advanced features that were included in the control system and shown to work on the prototype.

As with any high-power system, losses can be huge and the system must be optimized to minimize these losses. Chapter four describes the techniques used to minimize switching losses and to optimize the magnetic components used in all three stages of the converter.

The design and analysis of the three-stage inverter was limited to a six-month period. Due to this time constraint, some unresolved issues remain. Chapter five discusses the remaining problems and some possible solutions that can be implemented to improve the converter's design.

This thesis discusses an inverter capable of handling a high input voltage and splitting this voltage across multiple devices to reduce switch stresses. Furthermore, it demonstrates a working prototype of the high-voltage stage, and discusses the methods used to minimize losses. The applications for this robust design are widespread, including any high-voltage situation needing DC-to-DC or DC-to-AC power conversion, regardless of the environment.

2 Design Trade-Off and Feasibility Study

2.1 Background

DC-to-AC converters (inverters) come in many shapes and sizes. The operating environment, mechanical packaging, and the available control system all help narrow down the possible topologies for a particular design.

There are three questions that are addressed in this section: How will the correct output be generated? How will the high input voltage be handled safely, as to not destroy the switching devices? And how will the converter be controlled?

Simulation was the primary tool used to answer these questions and to see how different stages would interact. For the converter pertaining to this thesis, important discriminators were size and efficiency.

2.1.1 Specifications

The specifications for the DC-to-AC inverter are:

- Inverter input voltage range: 500-1100 V_{DC}
- Output voltage range: 0-500 V_{rms}
- Voltage set point accuracy: +/- 10 V_{rms}
- Set point resolution: 2 V_{rms}
- Maximum output current: 1.6 A_{rms}
- Frequency: 57-63 Hz
- Load regulation: 5 %
- Line regulation: 5 %
- Output voltage ripple: 5 %
- Isolation voltage: 2000 V_{DC}
- Efficiency at full load: 85 %
- Operating temperature: 175 °C

2.2 *Inverting Stage*

One possible implementation of the converter is a unipolar full-bridge inverter. The unipolar design modulates the switches such that for each half-cycle of the AC output, only two switches are under PWM control [19]. As compared to a half-bridge or full-bridge inverter (having only bipolar waveforms), this strategy reduces the harmonic content that needs to be filtered (Figure 2-1).

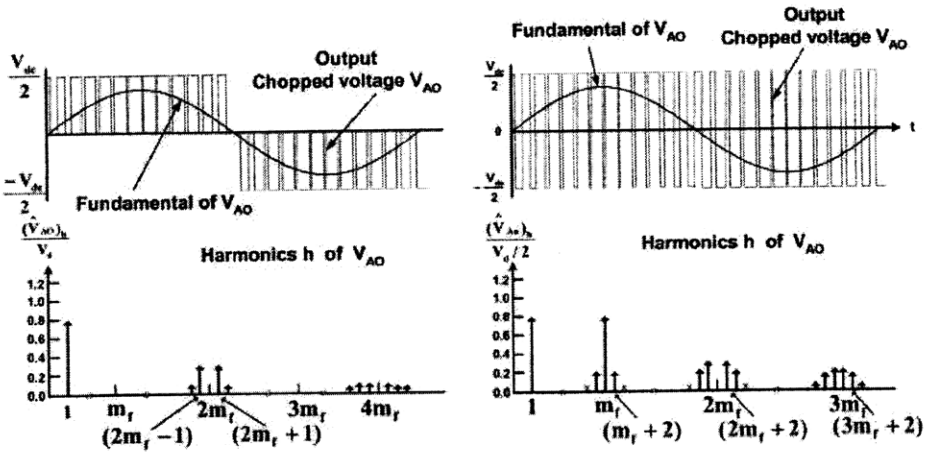


Figure 2-1: Unipolar vs. bipolar waveforms and their harmonic content

A variation on this unipolar topology was examined. In order to provide isolation, a transformer is needed. A 60 Hz transformer at the output is not a reasonable solution, since its size would be much too large for the package constraints. One solution is to use a transformer operating at the switching frequency to achieve isolation, and use a unipolar full-bridge inverter after the transformer as the final inverting stage.

Another alternative is to use a modulating technique that inverts every other PWM pulse, effectively raising the fundamental frequency that the transformer sees to the switching frequency (Figure 2-3). This signal can be transformed, and then demodulated back into a sinusoid [19]. This inverter topology was simulated and found to be a feasible solution (Figure 2-2). However, the transformer does not see a uniform signal, making it more difficult to optimize. Furthermore the modulation and demodulation require a significant increase to the complexity of the controller.

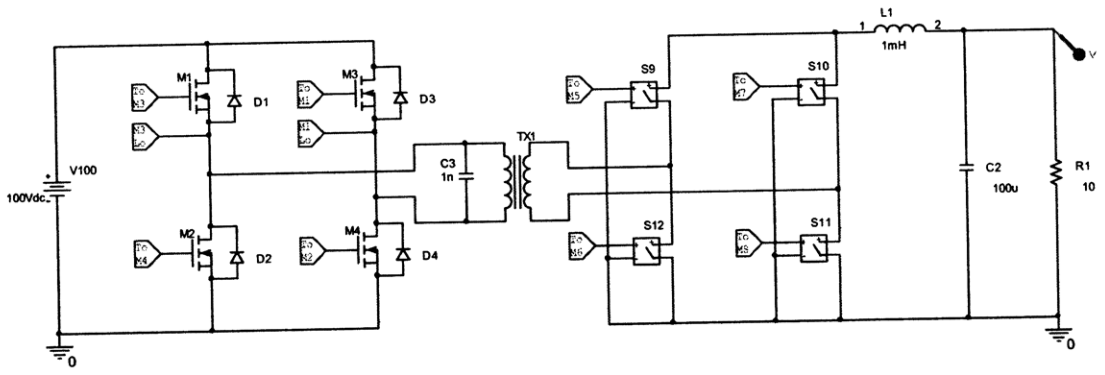


Figure 2-2: Simulated unipolar modulated inverter

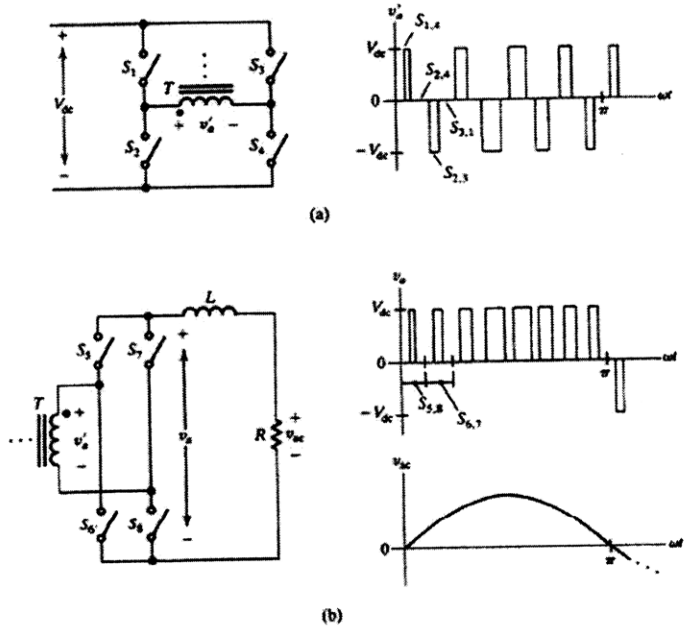


Figure 2-3: Modulated unipolar inverter and its waveforms [19]

The unipolar design was compared to a bipolar full-bridge inverter, where all switches are being modulated simultaneously (Figure 2-1). Although there is more harmonic content, this topology has the benefits of simpler control and better zero-crossing behavior. To provide isolation, a high-frequency DC-to-DC converter can be placed before the inverting stage. A full-bridge inverter with an isolated, rectified output is an option for this DC-to-DC stage. Bridge inverters are proven to be reliable and efficient, so this is an excellent choice for the converter topology.

Other methods of inversion are certainly possible. For example, instead of using a DC-to-DC stage followed by a bridge inverter, the first stage could be left as DC-to-AC, and then an AC-to-AC converter such as a cycloconverter can be used to create the low frequency output. Having fewer components and stages, this design may be more efficient, but it requires very complex, high-bandwidth, phase-dependent control, and is less efficient with single-phase AC (it was developed for use with three-phase power). The bipolar full-bridge inverter is a good choice for the output stage of the converter.

Because of the high input voltage specification (up to 1100 volts), a standard bridge inverter will not work for the isolated DC-to-DC stage. The switching devices that were available to be used (considering their temperature characteristics) are only rated up to 800 volts. The following sections examine multi-level converters which will limit the switch stresses to half of the input voltage—safely within the switching devices' operational range.

2.3 The Neutral-Point-Clamped (NPC) Inverter

2.3.1 The First Stage

Much research has been done on the topic of multi-level power converters [1]-[8]. A common multi-level inverter is the three-level Neutral-Point-Clamped (NPC) inverter, first developed by Nabae [5]. Meynard and Foch expanded this to n-level converters [4]. These converters are needed for very high voltage applications such as power distribution where components would ordinarily breakdown under such high stresses. Dividing these voltage stresses over multiple switches allows more desirable components—which may not have high voltage ratings—to be used.

The theory behind the NPC inverter is that with two switches open and two switches closed, the input voltage will always be divided between the two open switches. This works in steady state if the switches are identical, but during the commutation periods, it is impossible to determine what voltage each device will see.

A flying capacitor that always holds half of the input voltage can be added between the pairs of switches. Figure 2-4 shows that with this capacitor in place, in any state of the inverter, the voltage across each switch will be at most half of the input voltage. If

the capacitor is large enough and if the pairs of switches are operated at equivalent duty cycles, the capacitor will hold the correct voltage even during commutation. To help balance the capacitor, clamping diodes are placed between the sets of switches (Figure 2-5).

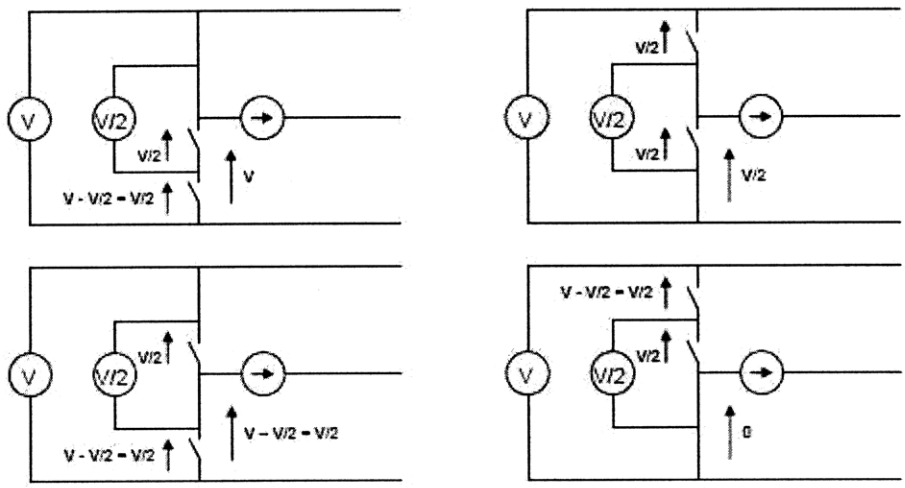


Figure 2-4: Switch stresses in NPC inverter

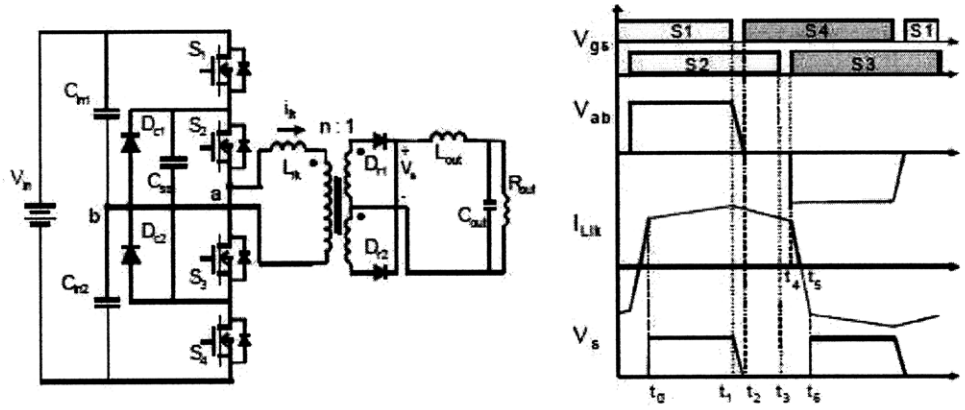


Figure 2-5: The phase-shifted NPC inverter and its waveforms [1]

Abarca's PhD thesis on the phase-shifted three-level DC-to-DC converter further developed the NPC inverter to include phase-shifted control (Figure 2-5) in order to reduce switching losses [1]. This was chosen as a possible implementation for the first stage of this thesis' converter. It would reduce the switch stresses to a maximum of 550

volts (with 1100 volts input) and it could provide the isolated DC-to-DC stage needed before the bipolar inverting stage.

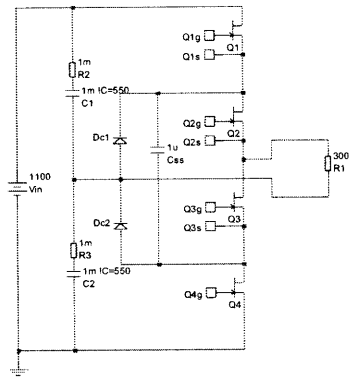


Figure 2-6: Simulated NPC inverter

Simulations confirmed the expected performance of the NPC inverter (Figure 2-6, Figure 2-7). The capacitor remained balanced during various phases when shifting switches 2 and 3, and all switches saw no more than half of the input voltage across them.

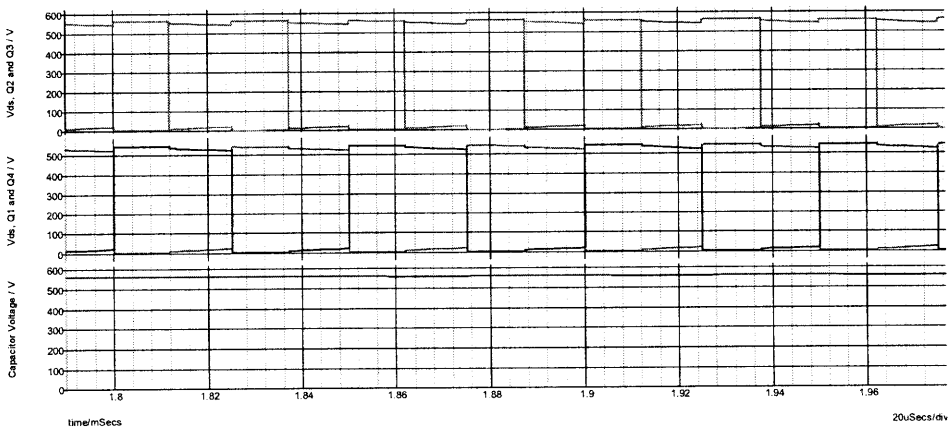


Figure 2-7: Capacitor and switch voltages of simulated NPC inverter

In Simetrix/SIMPLIS—the simulation platform primarily used in this thesis—two driver controls had to be developed: one for the spice simulator, and one for the SIMPLIS simulator which only simulates analog components and digital logic gates. Each control circuit creates a 50% duty cycle, and uses a one-shot multivibrator to delay the pulses for

switches 2 and 3. If the delay increases, the effective duty cycle seen by the transformer decreases. The SIMPLIS one-shot was simulated using logic and passive components, as seen below in Figure 2-9.

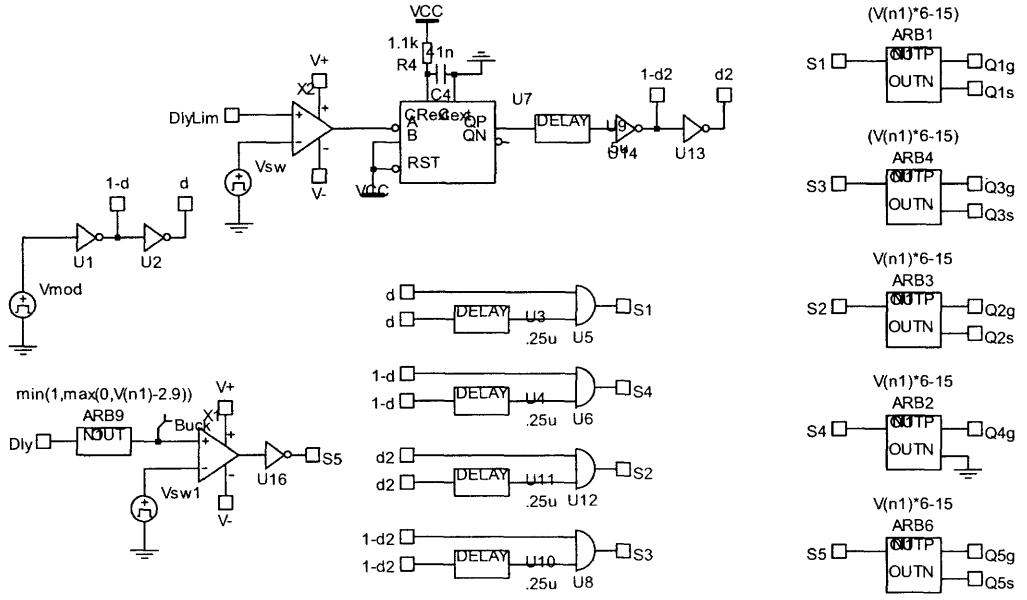


Figure 2-8: Driver circuit for spice simulator

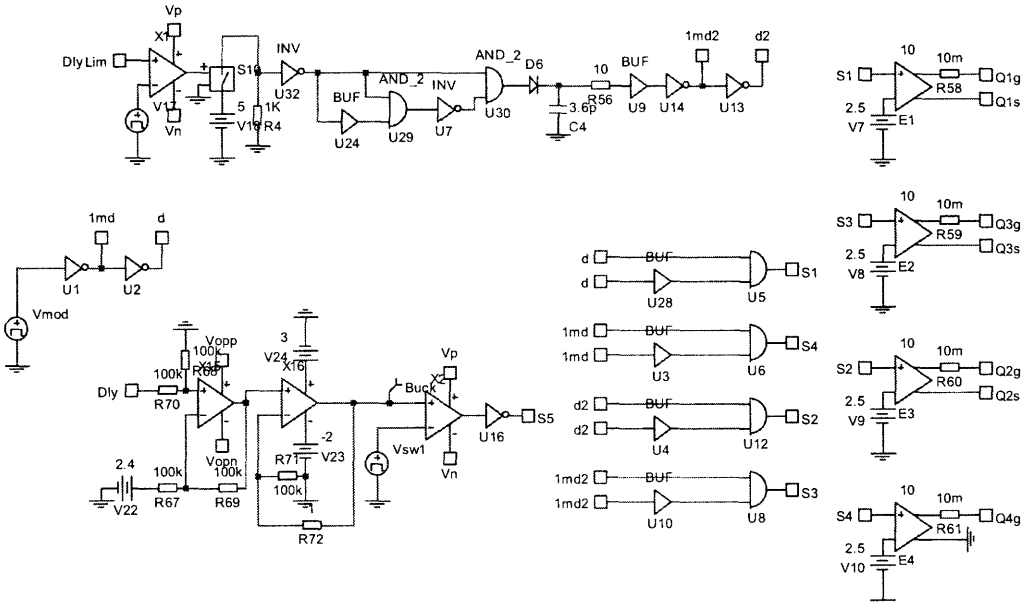


Figure 2-9: Driver circuit for SIMPLIS simulator

2.3.2 The Two-Stage DC-to-AC Converter

The simulations showed the NPC inverting stage working as expected. The entire DC-to-AC converter was then put together as shown in Figure 2-10. Initial simulations confirmed that this topology was acceptable—the converter was stable, and had the proper waveforms at each stage.

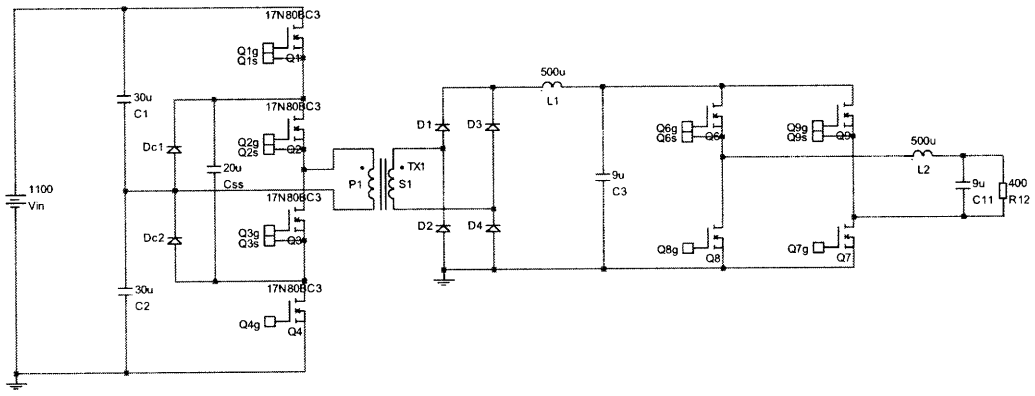


Figure 2-10: AC-Aux with NPC inverter

The control system was then designed and simulated to examine the wide input and output capabilities of the converter. With eight switches in two stages, there are several control strategies that can be used. Since it is desirable to reduce as many losses as possible, one approach is to control the DC-to-DC output in order to vary the AC peak output voltage. This way, when a low output voltage is required, the bipolar inverter stage sees a low input voltage and component losses in later stages are minimal. An added benefit is that the control of the inverting output stage can be left open-loop, and the phase-shifted switch delays can be optimized for zero voltage switching (ZVS) when applicable.

A potential problem of this control method is achieving an output voltage near zero volts. For example, if 10 volts is desired at the output, and the input is 1100 volts, the effective DC-to-DC duty cycle needs to be less than 1 percent. It is very difficult to control switches for such small time intervals, and it is likely that the floating capacitor would become unbalanced. A proposed solution is to add an intermediate bucking stage to the converter before the DC-to-DC filter (Figure 2-11). When the duty cycle

command drops below 5%, the bucking stage can slowly (1 kHz) turn the signal on and off, thus enabling the output DC voltage to be a suitably low value.

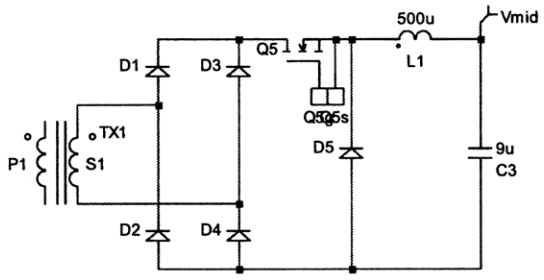


Figure 2-11: Intermediate buck stage for reduced voltage

The control strategies examined were voltage-mode control (direct duty ratio control based on the output) [19], peak current-mode control [16], and average current-mode control [15]. Control will be discussed more thoroughly in section 3.2; however, it was determined that average current-mode control would work best for this topology. Current-mode control provides better dynamic response than voltage-mode by favorably changing the system dynamics with an inner control-loop. Peak current-mode control requires sampling speeds greater than could be practically achieved with the given controller architecture.

A peak-detector was used on the AC output to measure the peak AC voltage level, and a compensator was put in place to tell the DC-to-DC controller the desired mid-point reference voltage level. The compensators were integrators implemented with op-amps.

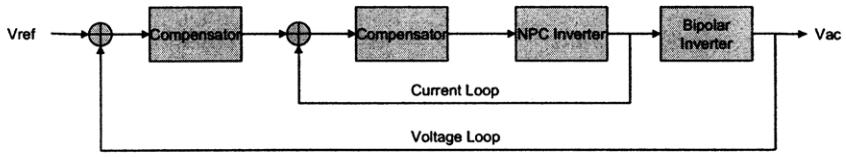


Figure 2-12: AC-Aux NPC control with inner current loop

This control scheme established the correct output voltage levels for the full input and output range; however, the output voltage was not a perfect sinusoid. An additional

control loop was added to correct the DC-offset of the AC output signal. The converter and controller together are shown in Figure 2-13.

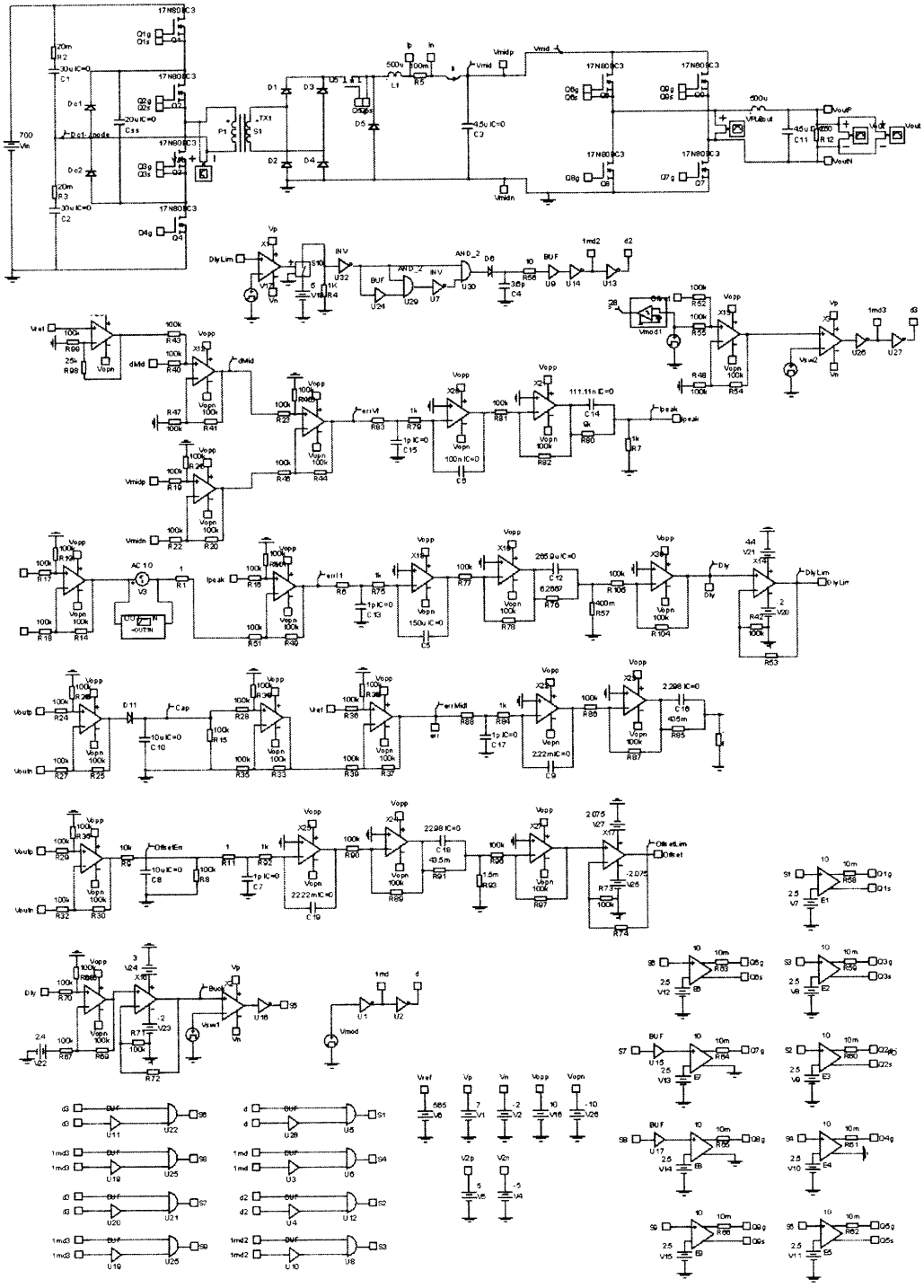


Figure 2-13: Schematic of AC-Aux with NPC stage and full control

The converter behaved well, with zero steady-state error and desirable transient response. Step responses in load and input were tested. Figure 2-14 and Figure 2-15 show the control system operation. The offset error goes to zero over the course of several AC cycles. The average current error approaches zero as the mid-point voltage goes to its reference value. AC analysis of the converter confirmed the overall stability.

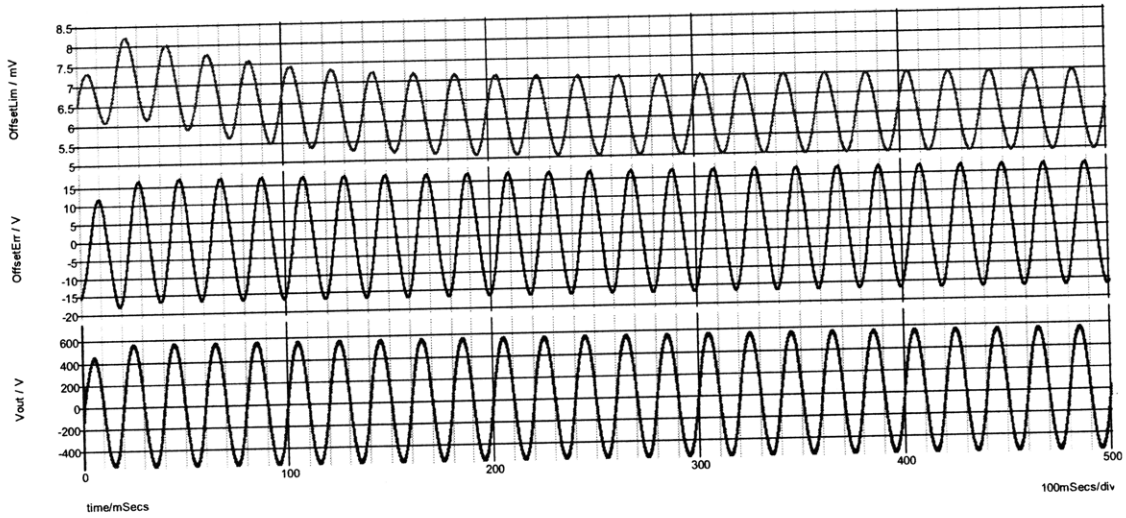


Figure 2-14: DC offset loop transient response

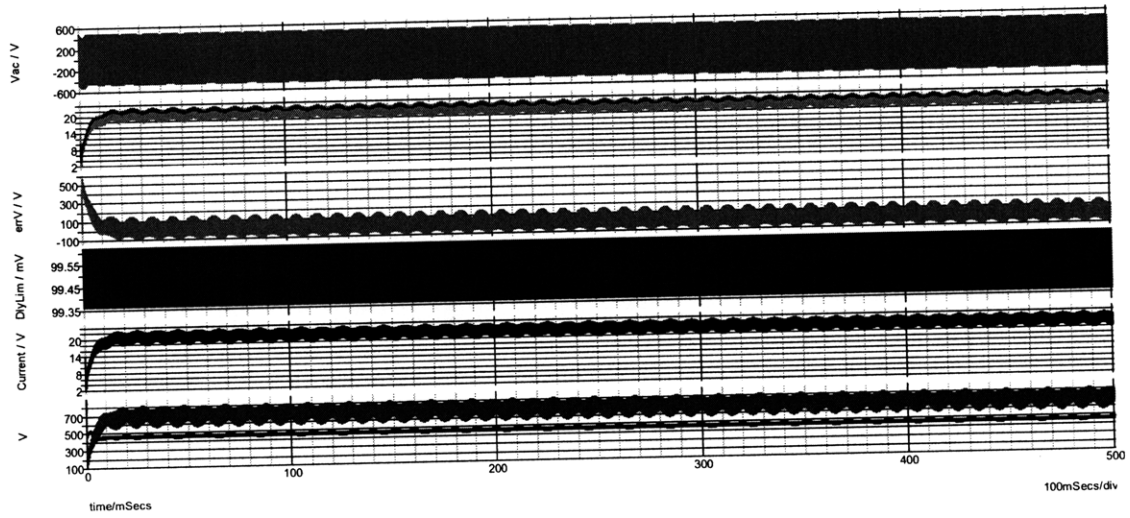


Figure 2-15: Current and voltage loop transient response

This topology worked except for one node in the circuit. The rectified voltage after the transformer is a series of PWM pulses. The maximum voltage this node sees is half of the input voltage times the transformer turns ratio. The DC output voltage needs to be roughly 700 volts in order to provide the desired 500 V_{rms} output, which dictates a turns ratio of 1:3.2. At this ratio, a converter input of 500 volts could achieve 760 volts DC with 95% duty cycle.

However, with an input of 1100 volts, the PWM pulses before the DC filter have a peak of 3.2*550, or 1760 volts. The rectifier diodes cannot handle such high voltage, and even if they could it is better to avoid such high voltages for packaging and EMI considerations.

2.4 The Three-Level Buck Converter

2.4.1 The First Stage

A solution to the problem of the high voltage after the transformer is to use a multi-level bucking conditioner [8] before an isolated DC-to-DC stage. The multi-level buck converter works much like the NPC inverter. A flying capacitor between the pairs of switches keeps the voltage across each switch balanced at a maximum of half of the input voltage [8]. The primary difference is that the three achievable output levels are zero, half of the input voltage, and the full input voltage. In the NPC inverter, the three levels of operation were negative half of the input voltage, zero, and half of the input voltage.

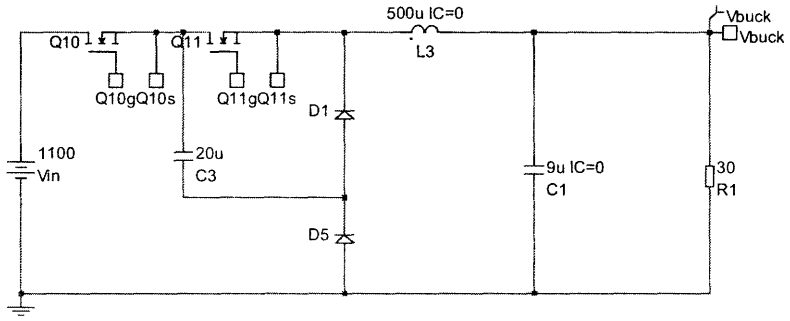


Figure 2-16: The three-level buck converter

Advantages of the three-level buck over the NPC inverter include having fewer devices (no clamping diodes or extra capacitors are required) and using only two active switches, which can be controlled using a simple PWM strategy rather than by phase-shifting.

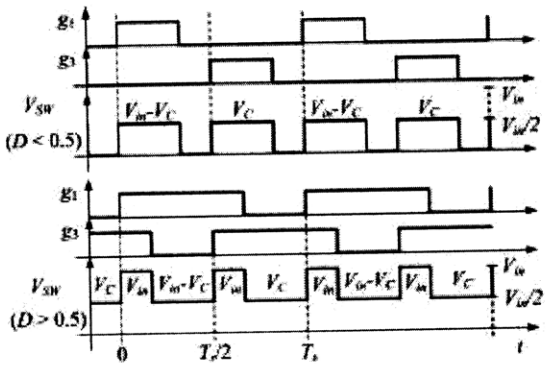


Figure 2-17: Gate and output waveforms for D < 0.5 (top) and D > 0.5 (bottom) [8]

Simulation of the multi-level buck confirmed its feasibility. The voltages across the switches were balanced and never exceeded half of the input voltage, and the output can vary from zero to the full input voltage. Note that when the duty cycle is less than 50%, the output is a pulse from zero volts to half of the input voltage, and when the duty cycle is greater than 50%, the output is a pulse from half of the input voltage to the full input voltage (Figure 2-17 and Figure 2-18). Figure 2-19 shows the simplicity of the controller for the gate drive signals when compared to the driver for the NPC inverter (Figure 2-9).

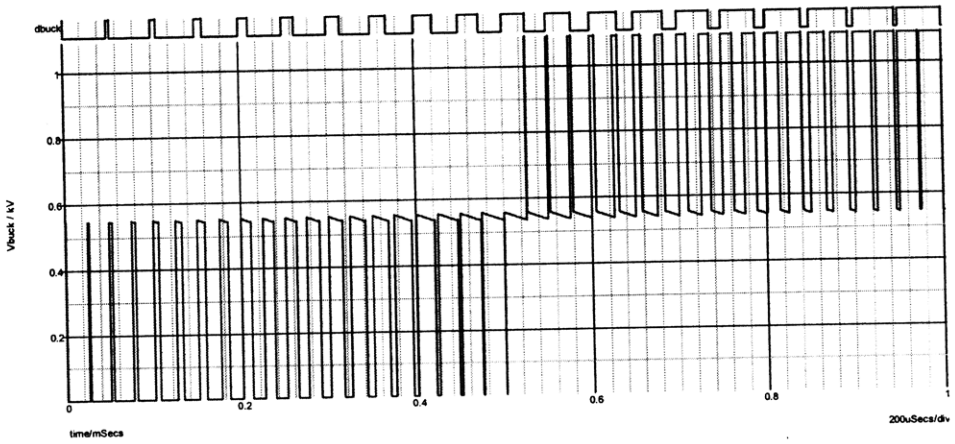


Figure 2-18: Unfiltered output of three-level buck with increasing duty cycle

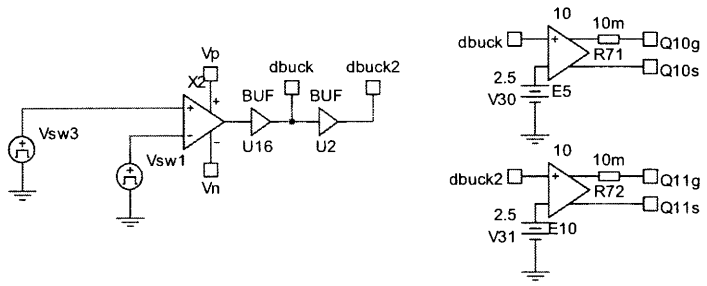


Figure 2-19: Three-level buck driver circuit

The argument can be made that active switches should be used in place of the diodes because conduction losses will be lower with MOSFETs, especially at high temperature. This was first tested in simulation. With 1100 volts input, 225 volts output, and 0.6 amps output, the following data was collected:

- Diodes: total losses for 2 MOSFETs and two diodes = 86 watts
- FETs: total losses for 4 MOSFETs = 130 watts

The diodes are more efficient. Values were gathered from the device data sheets were analyzed to confirm these results. First the conduction losses at 0.6 amps were examined:

FET	T_j = 25 C	$R_{ds,on}$ = .25 ohm	P_{loss} = 0.09 W
	T_j = 175 C	$R_{ds,on}$ = .69 ohm	**P_{loss} = 0.25 W**
Diode	T_j = 25 C	FV = 1.6 V	P_{loss} = 0.96 W
	T_j = 175 C	FV = 2.5 V	**P_{loss} = 1.5 W**

As expected, conduction losses are less when using FETs.

Next, the switching losses were looked at. Turn-on and turn-off characteristics for the MOSFETs were gathered from the device's data sheet. The switching characteristics for the diode were not available, so simulation waveforms were used to find rise times and fall times of the current and voltage. The diode had negligible turn-on switching losses.

In simulation, a 4 amp current spike was seen at diode turn-off. This value was used for the diode current in the simulated case. A 12 amp current spike was seen during FET turn-on and turn-off. A drain current of 6 amps was used for the analysis of the FETs using simulated values.

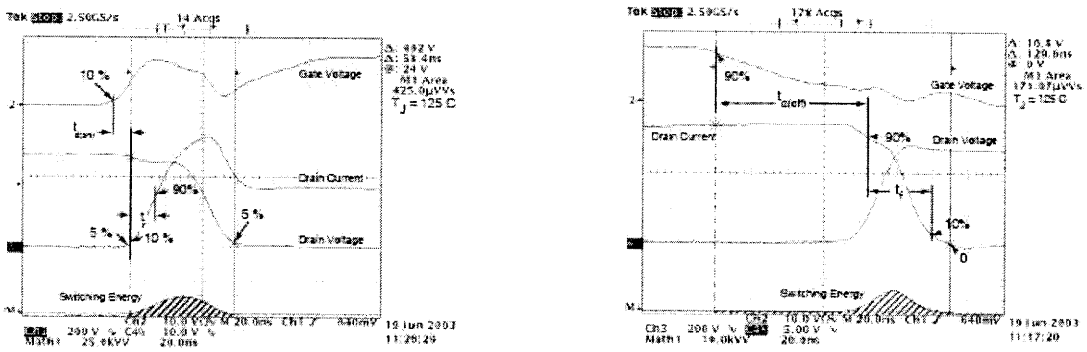


Figure 2-20: Turn-on and turn-off waveforms for MOSFET

$$P_{FET,on} = \Delta t \cdot V_{ds} I_d \cdot f_{sw}; \qquad P_{FET,off} = \frac{1}{2}\Delta t \cdot V_{ds} I_d \cdot f_{sw}$$

$$P_{D,on} = 0W; \qquad P_{D,off} = \frac{1}{2}\Delta t \cdot V_{ca} \cdot I_d \cdot f_{sw}$$

FET	P_{on}	P_{off}	P_{sw}	$\mathbf{P_{total}}$
Theoretical	0.39 W	0.132 W	0.552 W	**0.772 W**
Simulation values	3.85 W	1.3 W	5.15 W	**5.4 W**
Diode				
Theoretical	0 W	0.021 W	0.021 W	**1.52 W**
Simulation values	0 W	0.168 W	0.168 W	**1.67 W**

When using values from the simulation, the analytical calculations match the simulated power loss and show that diodes are more efficient, as can be seen in the table above. If purely theoretical values are used, the FETs are more efficient; however, this is not realistic because it does not reflect the interaction between the switches and other components, nor does it address parasitic reactances in the rest of the circuit. The

MOSFET devices switch slowly and large current spikes are probable if complementary FETs are used. Even if the theoretical case were true and the FETs were more efficient, one could argue that the diodes are a better choice due to the simplicity of the control circuit, and that this scheme reduces gate-drive losses by requiring only two drivers.

Three-stage buck converter efficiency was measured in simulation (Figure 2-21). At full load, the converter is over 98% efficient with both 500 and 1100 volt inputs. As expected, efficiency increases with output current. The 500 volt input is more efficient than 1100 volts because of lower switch stresses and lower parasitic capacitive discharges which occur at every switch device turn-on.

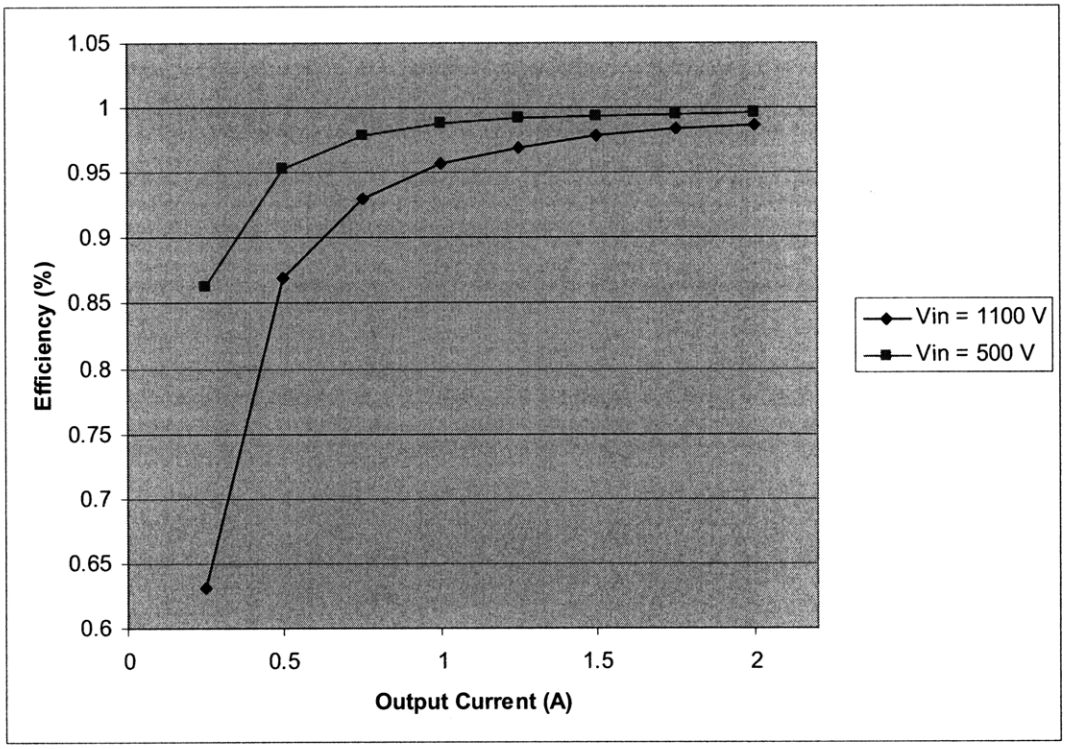


Figure 2-21: Simulated efficiency of the three-level buck converter

2.4.2 The Three-Stage DC-to-AC Converter

Due to the work in the previous sections, the converter topology chosen was a three-stage converter: a three-level bucking stage that will down-convert any high voltage to a reasonable lower level; a DC-to-DC full-bridge converter to provide isolation; and a

bipolar full-bridge inverter to produce the 60 Hz output (Figure 2-22). Simulations showed that the three stages work together as expected. Simulated full-load efficiency of the entire converter is 89%. Further optimization can be done, such as establishing zero-voltage-switching for both bridge inverters. Efficiency of 90% or greater should be attainable.

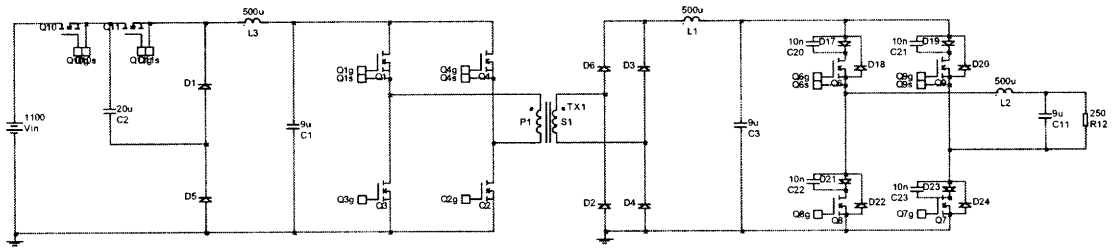


Figure 2-22: The three-stage converter

There are two categories of control strategies that can be used. The first is to control just the buck stage to get the desired output voltage, which is the simplest approach and will increase efficiency in later stages—especially at low desired output voltages. The second is to control each stage, giving more degrees of freedom which could improve the transient characteristics of the converter.

Dynamic performance was not a primary concern for this converter, so the strategy chosen was the first: use the buck stage to achieve a desired output voltage and keep the full-bridge inverters static in open-loop.

Within this control topology, there are other decisions to be made. For example, if current-mode control is to be used, any number of currents could be the controlled variable, such as the buck filter current, the transformer current, the rectified DC filter current, or even the output current.

These strategies were tested, but the propagation delay from the buck output voltage to the AC output voltage limited the speed at which the inner current-loop could operate. Because of this, the simpler voltage-mode control was selected (Figure 2-23). When using integrating compensators, zero steady-state error was achieved.

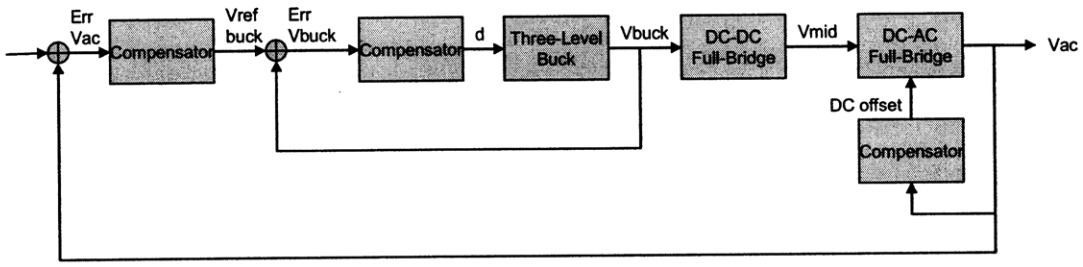


Figure 2-23: Control strategy for the three-stage converter

Simulations showed that this topology is controllable and efficient. The converter meets all specifications:

	Specification	Simulated
Input voltage	500-1100 V	500-1100 V
Output voltage	0-400 V_{rms}	0-400 V_{rms}
Voltage set point accuracy	+/- 10 V_{rms}	+/- 0 V_{rms}
Set point resolution	2 V_{rms}	0 V_{rms}
Output current	1.6 A_{rms}	1.6 A_{rms}
Load regulation	5%	0%
Line regulation	5%	0%
Frequency	57-63 Hz	60 Hz
Output voltage ripple	5%	3.6%
Isolation voltage	2000 V_{DC}	N/A
Efficiency	85%	89%

Through the design trade-off and feasibility study discussed in this chapter, the three-level buck converter was chosen to serve as the front-end of the DC-to-AC converter. The following chapter will examine the three-level buck converter in more detail.

3 The Three-Level Buck Converter

3.1 Experimental Setup

The three-level buck converter was built in laboratory and controlled using a TI EZ-DSP f2812 digital signal processor (Figure 3-1 and Figure 3-2). An existing driver board was used to drive the MOSFET gates. Twelve 225-watt power resistors in a 420 ohm network served as the test load (R1). Isolated laboratory power supplies provided the low-voltage power for the controller and drivers. A Universal Voltronics 3 kV, 3.3 amp power supply served as the high-voltage input.

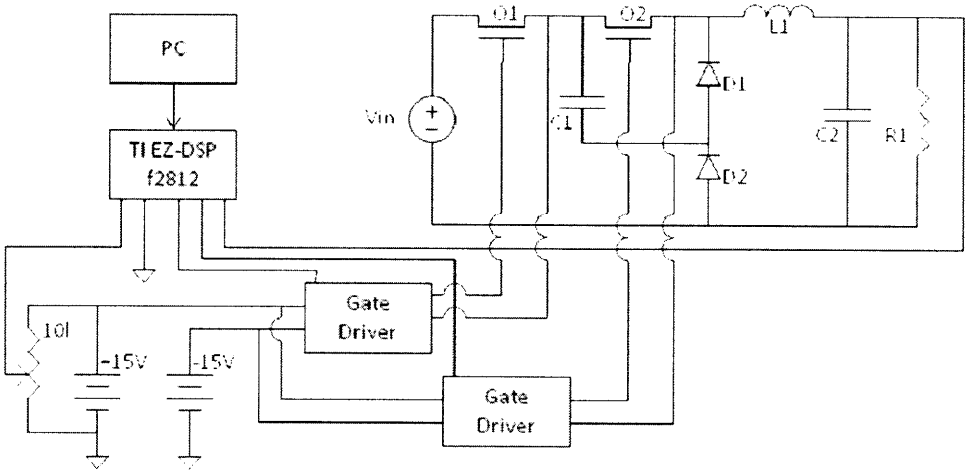


Figure 3-1: Schematic of the experimental setup

The 500 μH filter inductor (L1) was made from a Magnetics molypermalloy 55087-A2 toroidal core with 49 windings (22 AWG). C1 and C2 were high temperature (200 °C) Novacap ceramic capacitors, 20 μF and 4.7 μF respectively. Diodes D1 and D2 were CREE CSD10120s, silicon carbide and rated at 1200 volts and 20 amps. The MOSFETs (Q1 and Q2) were 800 volt, 17 amp TO-247 devices rated to 150 °C. Their characteristics include an R_{DSon} of .29 ohms, 90 nC gate charge, and the devices are avalanche energy rated.

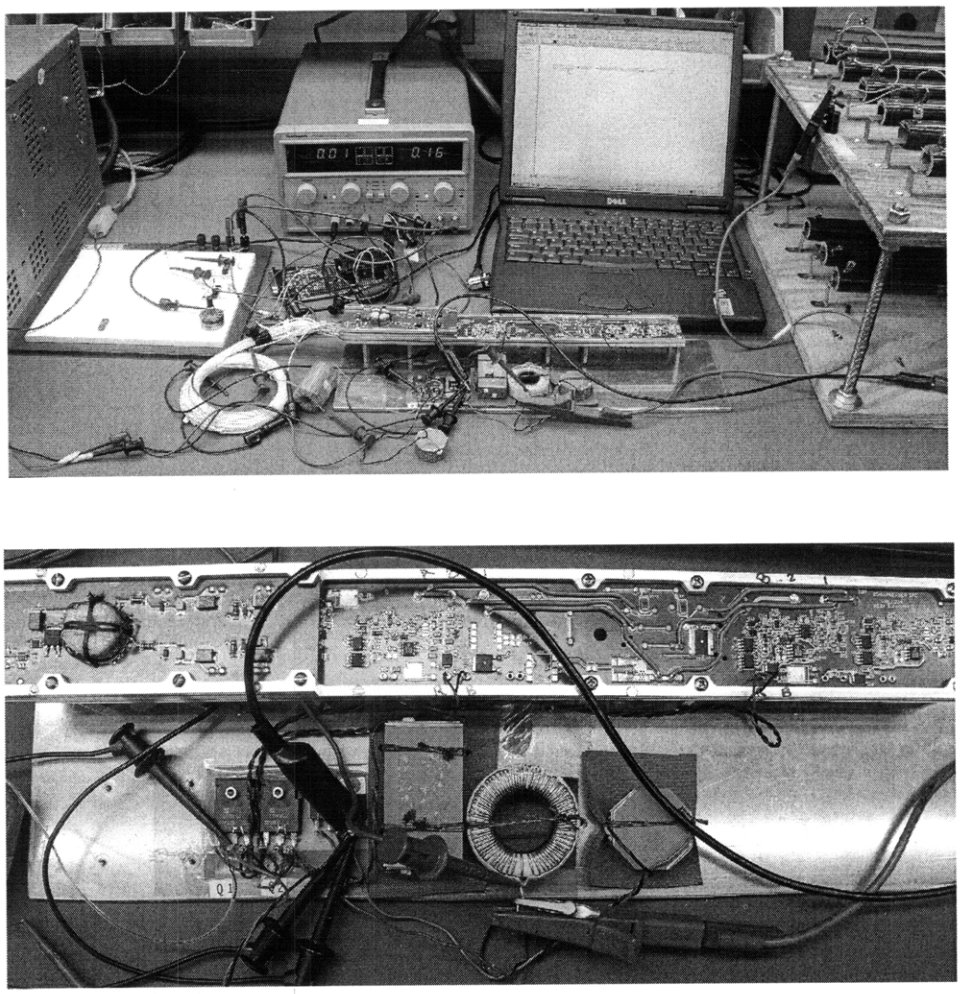


Figure 3-2: Lab setup for testing three-level buck converter (top); the three level-buck converter with driver board (bottom)

Visual Solutions' VisSim program was used to program the DSP. For open-loop operation, the output was controlled with a duty cycle command. Figure 3-3 shows the VisSim interface. A duty cycle command is issued and converted to fixed-point. The duty cycle command is then written to two PWM outputs of the DSP. One of the PWM timers is offset by ½ of the timer count (minus one to account for the current machine-cycle) to provide the necessary 180 degree phase shift.

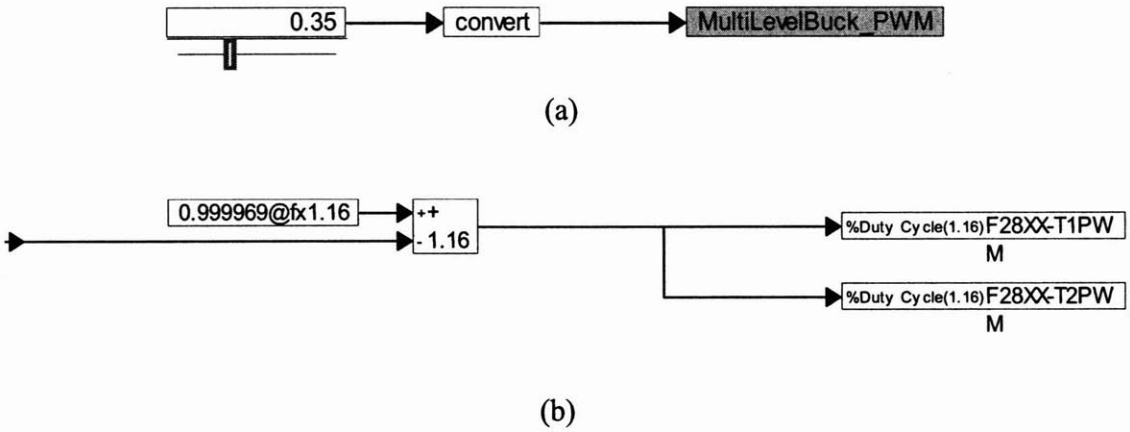


Figure 3-3: (a) Open-loop control with VisSim interface; (b) The MultiLevelBuck PWM block

Due to noise (see section 5.1), the connection between VisSim and the DSP was interrupted at voltages above 50 volts. To test the operation of the converter at higher voltages, a potentiometer was added to give the duty cycle command directly to the DSP. Figure 3-4 shows this VisSim program. An analog channel is read and scaled to give a fixed-point input of 0 to .99, which is written to the PWM output.

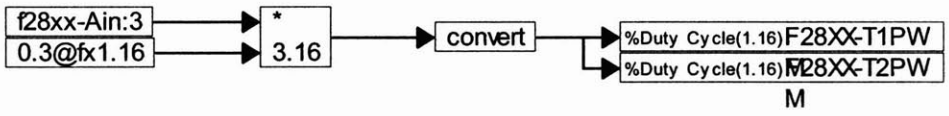


Figure 3-4: Open-loop control with potentiometer input

Closed-loop control was similar to open-loop control, with either the potentiometer or VisSim giving the reference value. The internal PID block was used for the compensator. Figure 3-5 shows a closed-loop control scheme. A reference voltage is given in VisSim and scaled and converted appropriately. Inside the MultiLevelBuck block, this input is compared with the converter's output voltage, read into an analog channel and scaled. The PID compensator produces the duty cycle output.

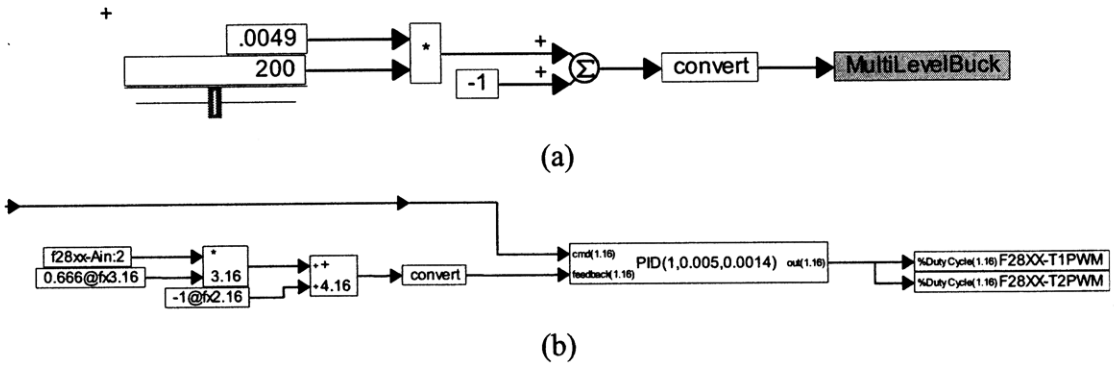


Figure 3-5: (a) Closed-loop control with VisSim interface; (b) MultiLevelBuck block

3.1.1 Open Loop

The converter was first examined open-loop to determine if it was functioning properly and whether it could handle the maximum required load. Figure 3-6 shows the switching waveforms of the FETs and the diodes. With a small inductor (500 uH), there is ringing in the switch waveforms when the inductor is in discontinuous conduction mode (DCM) (Figure 3-7). This does not affect the performance of the converter.

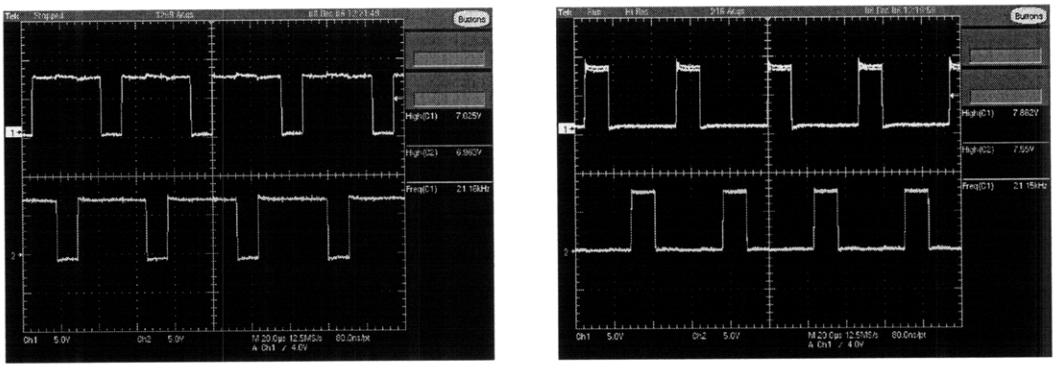


Figure 3-6: Voltage across diodes (left) and FETs (right). [5 V/div, 20 µs/div]

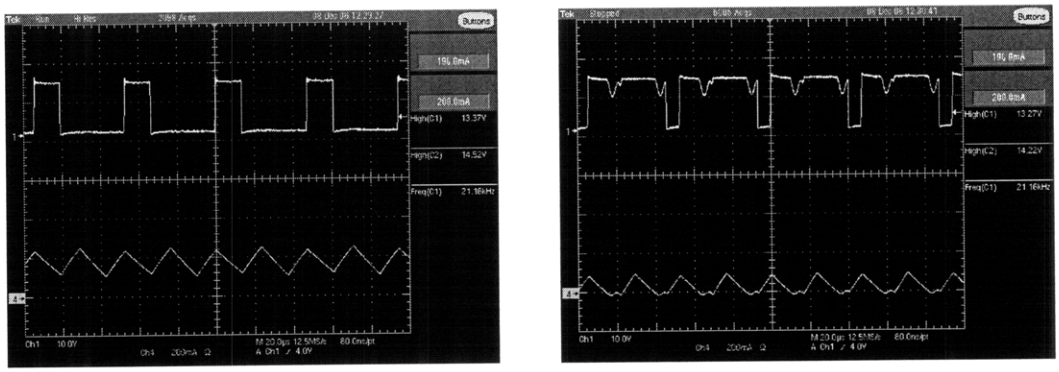


Figure 3-7: V_{ds} of the top FET (top trace) and current through the inductor (bottom trace): CCM (left) and DCM (right). [10 V/div, 200 mA/div, 20 µs/div]

Figure 3-8 shows the output waveform before the output filter, below and above 50% duty cycle. As predicted, the voltage was from zero to half of the input voltage when below 50% duty cycle, and from half of the input voltage to the full input voltage when above 50% duty cycle.

The converter functioned correctly from 0 volts to 1100 volts input at full power (tested up to 700 watts). Though noise was a problem for the DSP at high voltages (see section 5.1), the converter's open loop performance was identical at all voltages. An efficiency calculation was attempted at 500 volts input and 1.0 amp output (500 watts), and the efficiency was too high to be accurately measured. This matched the simulated prediction (Figure 2-21).

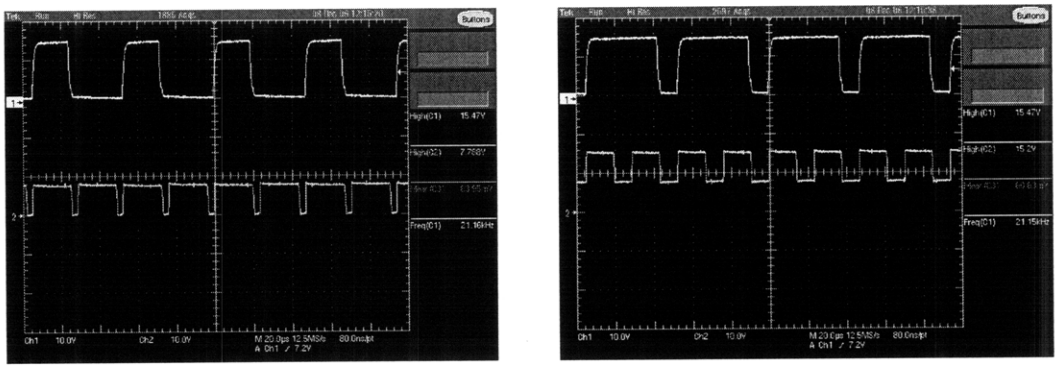


Figure 3-8: V_{ds} of the top FET (top trace) and unfiltered V_{out} (bottom trace) for D < 0.5 (left) and D > 0.5 (right). [10 V/div, 20 µs/div]

The flying capacitor stayed balanced in normal, loaded operation (Figure 3-9) with a 500 uH inductor. However, the capacitor voltage drifted with no load. With no current flowing, there is only a resistive path through the FETs and Diodes to charge the capacitor. The high-voltage power supply's output impedance is in series with this path, and each component has slightly different open-state resistances, which results in an unbalanced voltage divider (Figure 3-10).

A small resistance (20 ohms) was placed in parallel with each switch to test and solve this problem, but this was not a practical solution due to the high power losses associated with these resistors. Figure 3-9 also shows that the output voltage goes to nearly the full input voltage with no load because the diodes do not conduct (which serves to balance the capacitor voltage) when there is no current flowing.

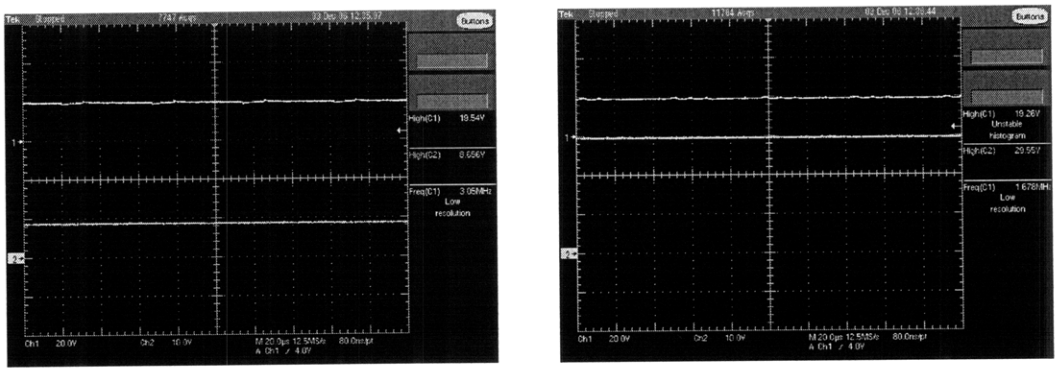


Figure 3-9: Floating capacitor (top) and output (bottom): with load (left) and with no load (right). [ch. 1: 20 V/div, ch. 2: 10 V/div, 20 µs/div]

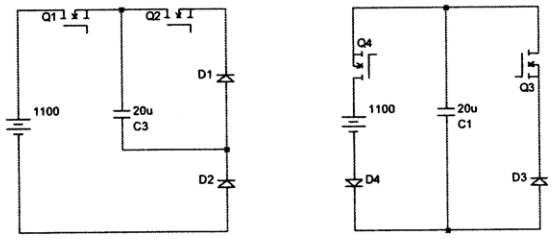


Figure 3-10: The multi-level buck; components rearranged to show unbalanced voltage divider (right)

3.1.2 Closed Loop

A simple integrating compensator was used to test the system with feedback. Closed loop operation was very similar to open-loop operation. When the circuit was loaded, the flying capacitor remained balanced and the waveforms across the devices were as expected (Figure 3-11): the capacitor voltage was half of the input voltage, and each device saw half of the input voltage.

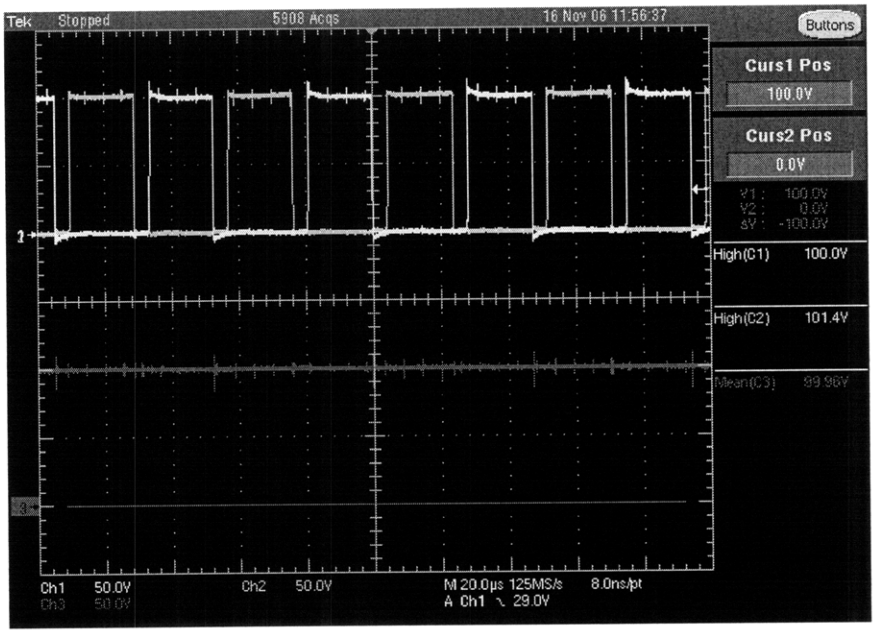


Figure 3-11: Capacitor voltage (bottom) and Vds of both FETs (top) during loaded operation. [50 V/div, 20 µs/div]

With no load, the converter behaved differently in closed-loop. The output voltage still rose to nearly the input voltage, but the duty cycle changed to compensate for this, and the capacitor remained in slightly better balance (Figure 3-12).

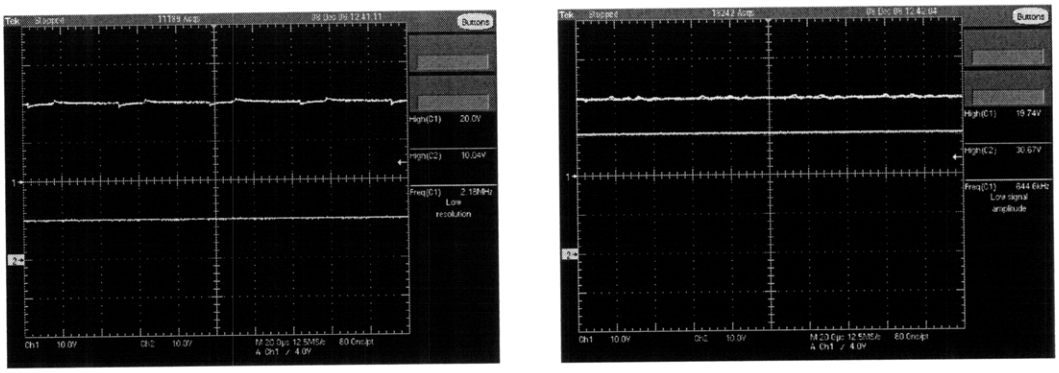


Figure 3-12: Floating capacitor (top) and output (bottom): with load (left) and with no load (right). [10 V/div, 20 µs/div]

The converter tracked the reference voltage well, with an output of 10 volts and inputs of 15 volts and 50 volts (Figure 3-13), and with an output of 300 volts and inputs of 500 volts and 1100 volts (Figure 3-14). In the latter case, noise from the phase-shifted turn-on of the bottom FET caused gate-drive noise that created a momentary turn-on of the top FET, but the controller properly compensated for this and the output voltage remained fixed at the appropriate level.

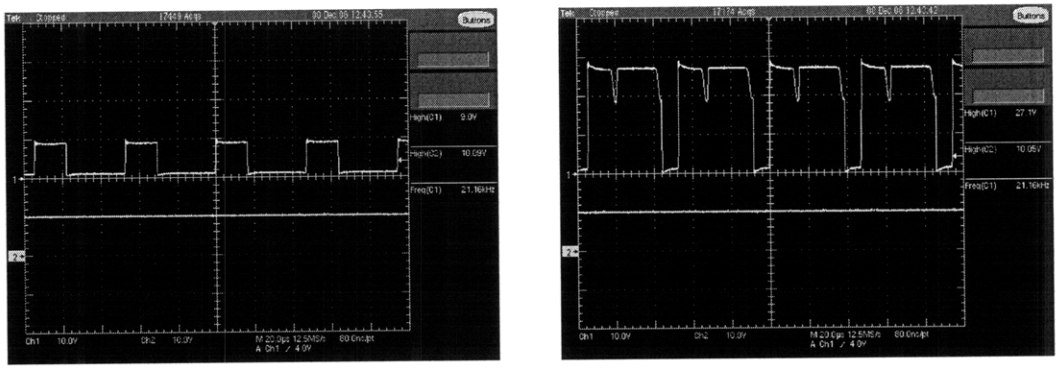


Figure 3-13: Tracking V_{ref} = 10 volts: V_{in} = 15 volts (left) and V_{in} = 50 volts (right). Top trace: V_{DS} of the top FET; bottom trace: V_{out}. [10 V/div, 20 µs/div]

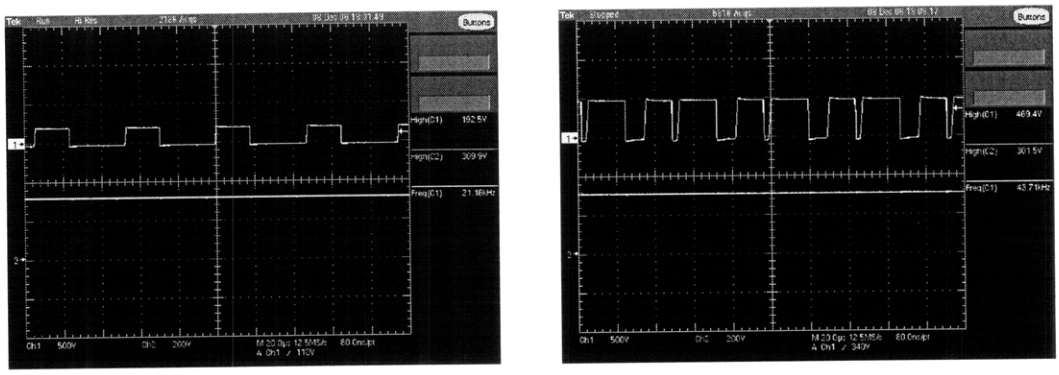


Figure 3-14: Tracking V_{ref} = 300 volts: V_{in} = 500 volts (left) and V_{in} = 1100 volts (right). Top trace: V_{DS} of the top FET; bottom trace: V_{out}. [ch. 1: 500 V/div, ch. 2: 200 V/div, 20 µs/div]

3.2 Control

The three-level buck converter behaved as expected in simulation and in lab. Developing a proper control strategy was needed to improve the dynamic performance of the converter, and was a necessary step for the final DC-to-AC inverter design.

3.2.1 Analysis

The requirement of operating at or near no load implies that regardless of the size of the filter inductor, the converter may be operating in discontinuous conduction mode (DCM) for part of the time. Current mode control becomes complex when transitioning into and out of DCM. Because of this, a single-loop voltage control strategy was chosen.

In simulation, current-mode control was also found to be problematic. The propagation delay from the first stage to the final AC output limited the speed at which the current-loop could run. If the current loop was limited to roughly 500 Hz bandwidth, then the voltage-mode control loop could be at most 10-50 Hz bandwidth. A voltage-control loop by itself can have similar bandwidth and performance with less complexity.

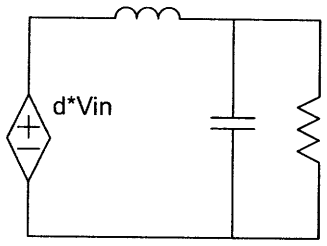


Figure 3-15: Linearized buck converter

After linearizing the switches in Continuous Conduction Mode (CCM) as in Figure 3-15, the voltage transfer function of the buck converter was found to be that of the output filter:

$$\frac{V_{out}}{d \cdot V_{in}} = \frac{1/LC}{s^2 + s \cdot 1/RC + 1/LC}$$

When the converter enters DCM, the input to output voltage relationship becomes a nonlinear function of both the input voltage and the duty cycle D:

$$V_{out}^2 + V_{out}\left(\frac{V_{in} RD^2 T}{2L}\right) - \left(\frac{V_{in}^2 RD^2 T}{2L}\right) = 0$$

Taking this into account, a control system optimized for the CCM converter will need to be reduced in bandwidth, or slowed down, in order to remain stable for both modes of operation and for the transition between them.

A proportional plus integral (PI) compensator was chosen for its zero steady-state-error and dynamic response. The output voltage of the multi-level buck stage is reflected across a transformer in the DC-to-DC stage of the converter. This voltage may be near 800 volts during operation, which approaches the breakdown voltage of some switching devices, so overshoot in the output voltage of the buck stage is unacceptable. Therefore a step response with no overshoot is desired in the control system. This is a tradeoff, and will yield worse noise rejection and bandwidth than otherwise possible.

A MATLAB script [appendix 8.1] was written that takes a transfer function—in this case the transfer function of the CCM buck converter—and tests all combinations of given vectors P and I. The compensator has the form $k_1 + k_2/s$, where k_1 is the proportional gain and k_2 is the integral gain. The script computes the highest possible bandwidth of the loop transfer function while keeping a phase margin of at least 30 degrees. For the theoretical system, the ideal proportional gain returned was 0 and the ideal integral gain was 100.

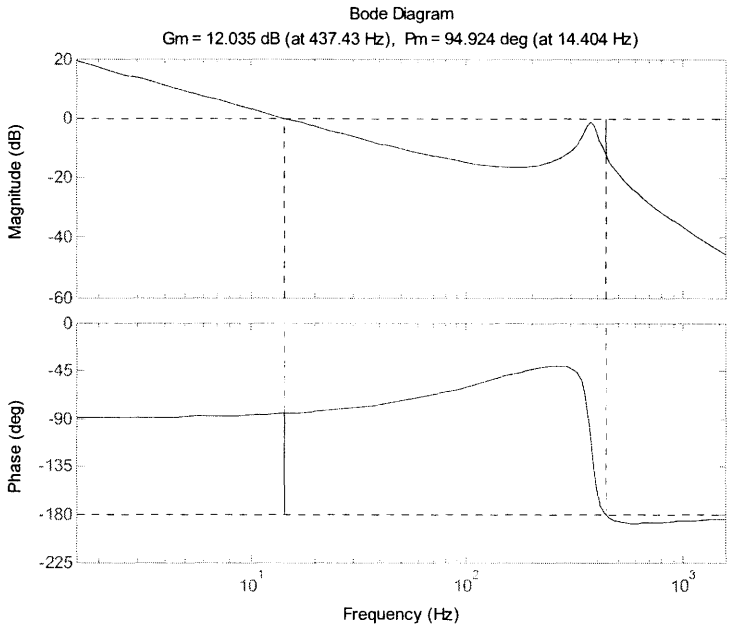


Figure 3-16: Theoretical Bode plot of loop gain

Figure 3-16 shows the Bode plot of the compensated three-level buck converter. The phase margin was near 90° at the crossover frequency of 14 Hz, which was as high as it could be before pushing the resonant peak above zero, at which point the converter would have become unstable. The stability of the converter was verified by the root locus diagram shown in Figure 3-17.

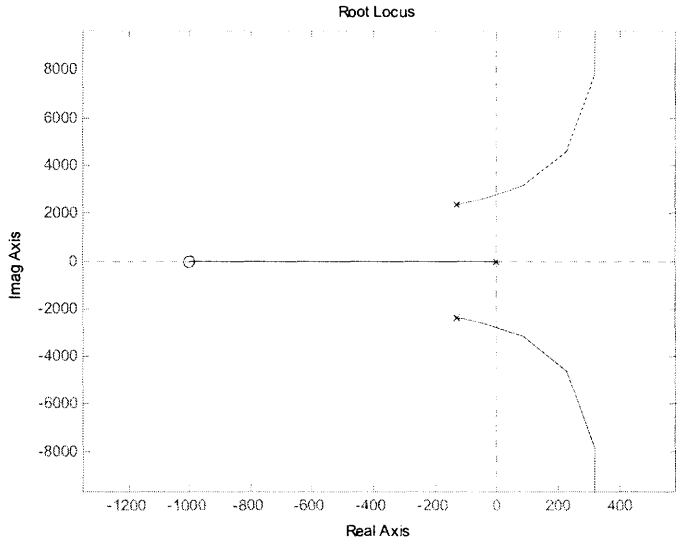


Figure 3-17: Theoretical root-locus plot of loop gain

Figure 3-18 shows that the step response of the closed loop system is nearly first-order; the crossover frequency occurs in a region dominated by one pole. However, due to the narrow margin by which the resonant peak is below 0dB gain, there is some second-order ringing occurring at the resonant frequency.

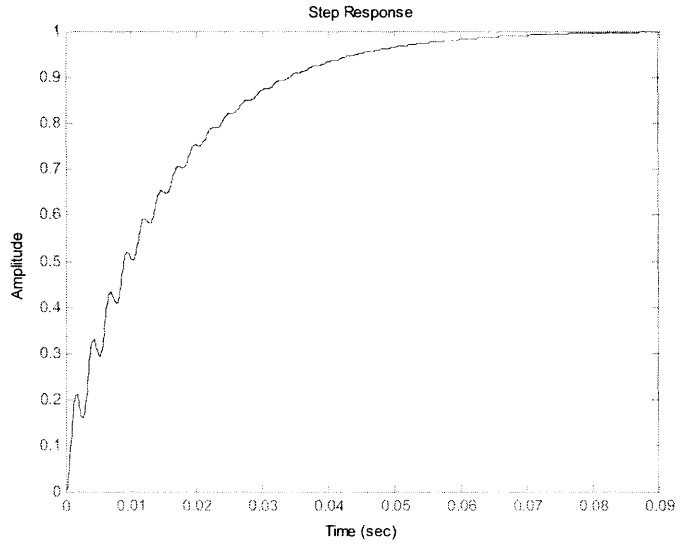


Figure 3-18: Theoretical step response of closed loop system

3.2.2 Simulated

A model of the three-level buck converter with a PI controller was simulated in Simetrix/SIMPLIS (Figure 3-19).

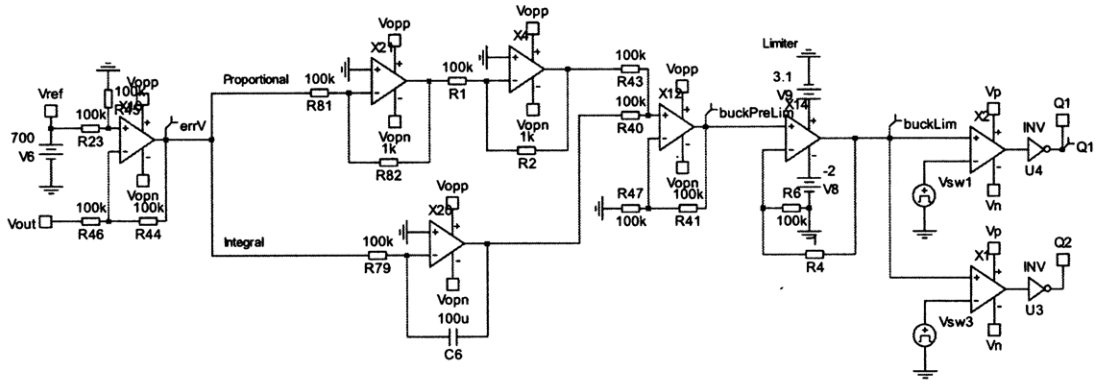


Figure 3-19: Analog PI controller in SIMPLIS

One notable difference from the theoretical analysis to the simulation is that the actual implementation of the controller values had to be limited. The duty cycle command was between 0 and 1, and therefore the compensator could not produce values outside of that range. If the compensator gain remained low enough, these rails were not hit and the control system remained linear.

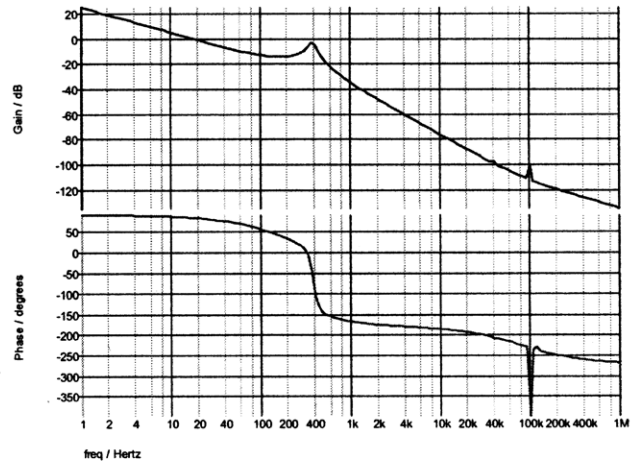


Figure 3-20: Simulated Bode plot of loop gain

The Bode plot in Figure 3-20 shows a crossover frequency of 17 Hz with a phase margin of 83°. 14 Hz and 90° were expected from the theoretical analysis. Similarly, there was an expected resonant peak at 440 Hz. The simulation showed a peak at 400 Hz before the 2nd-order roll-off. Note the high frequency behavior in the simulated Bode plot. There were some higher order poles and zeros in the circuit devices that were not accounted for in the theoretical analysis.

The phase of the simulated circuit showed an important difference from the analysis. The expected phase had a bump before the resonant frequency and then dropped to a constant -180°. The bump did not appear in the simulation's phase, and although the high frequency magnitude remained nearly 2nd order, the phase continued to drop. This is indicative of delays in the control circuit, which take the form e^{-jwt} in a transfer function—a linearly increasing, frequency-dependant phase-shift. This delay limits how high the bandwidth can be pushed before the converter becomes unstable.

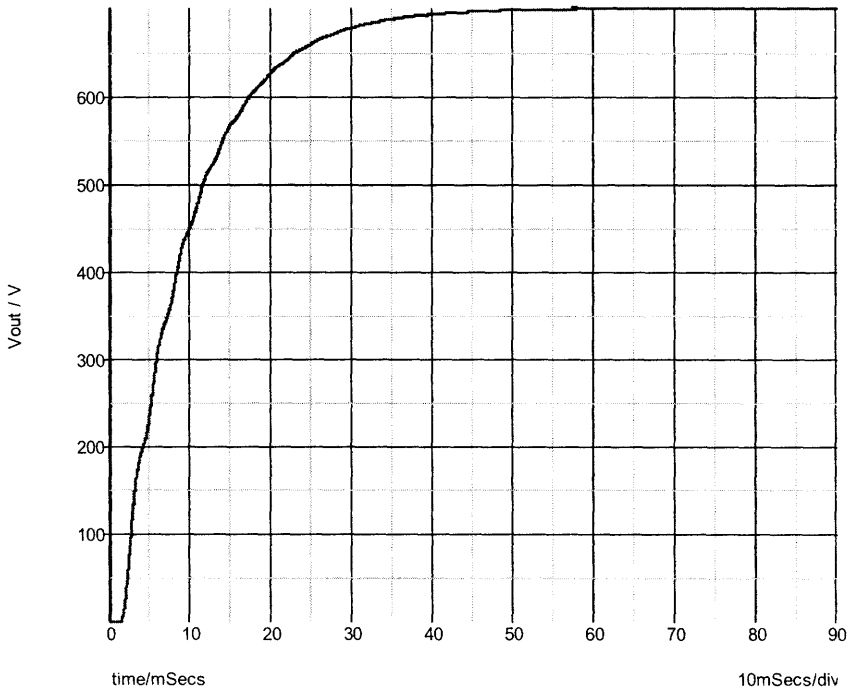


Figure 3-21: Simulated step response of closed loop system

The step response of the simulation was slightly faster than that of the theoretical analysis. This was expected with the higher crossover frequency. Also, the 2nd order ringing was less pronounced, due to parasitic damping and a larger margin between the resonant peak and 0dB.

3.2.3 Experimental

The control strategy was experimentally executed on a TI-F2812 series digital signal processor (DSP). Visual Solution's VisSim, a graphical development tool, was used to program the DSP as described in section 3.1. The PID block was set with P = 0, I = 1 and D = 0. Note that the values are scaled from the theoretical PI values by 1/100. This is because the conversion back to continuous time requires multiplying by the sampling rate of the DSP (100 Hz).

An AP Instruments AP200 network analyzer was used to measure the frequency response of the control system (Figure 3-22). This measurement closely matched the simulated and expected frequency response. Open loop gain crossover occurred at around 40 Hz, which was higher than in simulation and is the result of the scaling of the integral term value. This Bode plot shows a phase margin of around 90 degrees at crossover, as expected. The 400 Hz peak in the gain is not pronounced in the experimental setup. This could be due to damping that occurs in wires and in the filter components themselves.

Note that a buffer circuit was needed to properly measure the loop gain with the network analyzer. Figure 3-23 shows the recommended circuit from the AP Instruments application notes.

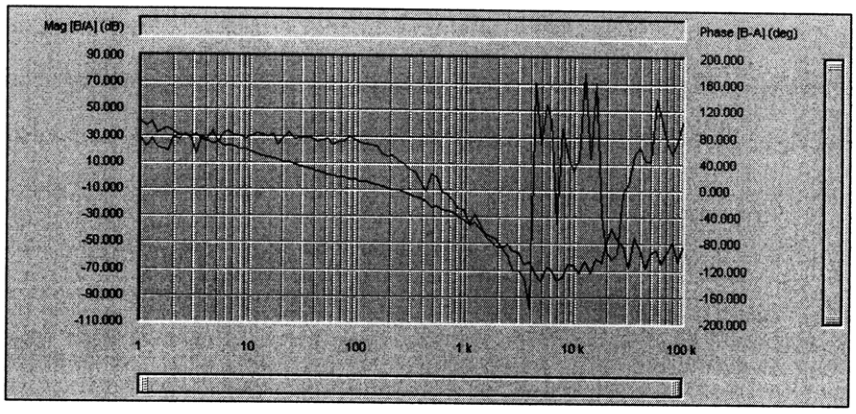


Figure 3-22: Actual Bode plot of the open loop gain

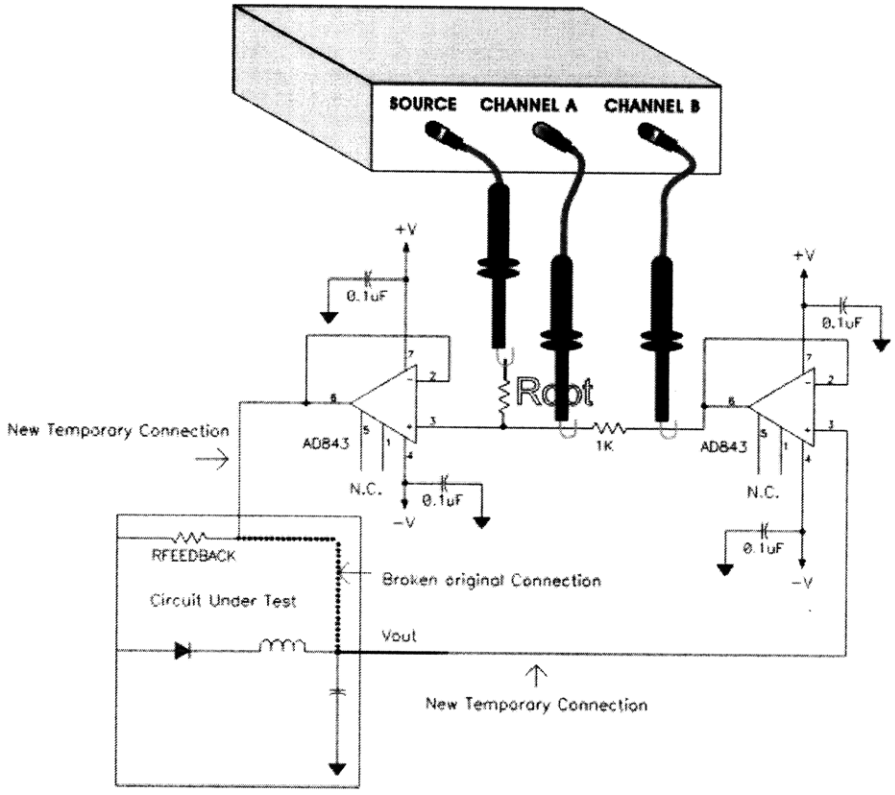


Figure 3-23: Recommended setup for measuring loop gain with an AP200 network analyzer

The step response of the closed-loop system confirmed the expected behavior. The step response rise and fall times were directly related to the crossover frequency of the open loop gain, and the transients were mostly over-damped in shape.

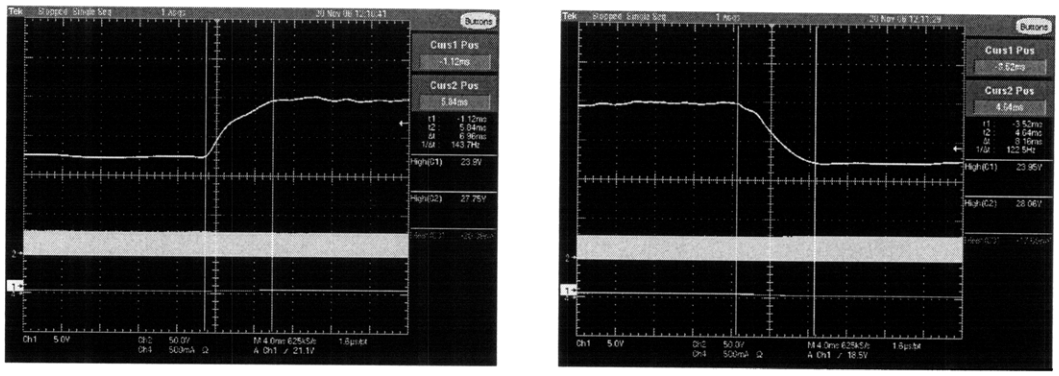


Figure 3-24: Measured step response of closed loop system. Top trace: V_{out}; bottom trace: FET voltage. [ch. 1: 5 V/div, ch. 2: 50 V/div, 4 ms/div]

In the past three subsections, a control strategy was designed and optimized to achieve certain performance criteria. The control strategy was tested in simulation and the experimental implementation was shown to match the expected behavior.

3.3 Advanced Control

There are several improvements that were made to the control system. Some were required for proper converter operation. Others were added features to show the feasibility of the full three-stage converter design.

3.3.1 Filtering

The ADC on the DSP was very fast and very accurate. Because of this, noise was easily detected and injected into the PID controller. Noise in the controller results in incorrect duty cycle commands. Filtering is a practical way to eliminate unwanted noise.

In closed-loop operation, the buck converter's output voltage was read from an analog input channel. Operation was tested both with and without filtering of this input. If a high cutoff frequency was used, noise still affected the duty cycle. Cutting out this noise led to a false reading of a nice, smooth output, and the converter did not react to changes like it should have. No filter was placed at this stage.

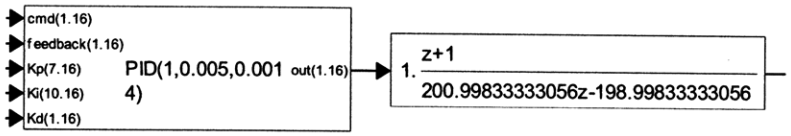


Figure 3-25: PID output filter in VisSim

However, noise in this measurement caused the controller to change the duty cycle even if the actual output was constant. To fix this, the output of the PI controller—the duty cycle command—was filtered, with a cutoff frequency slightly higher than the bandwidth of the controller (100 Hz) (Figure 3-25). This helps stabilize the converter in the event of noise: when the feedback channel sees a noise spike, the controller reacts with a fast and large duty cycle spike, but the output filter ignores this high-frequency content and the duty cycle remains fixed. This method gives the controller all of the possible information, but limits what the controller can do with that information.

Filtering the controller's output affected the frequency response of the system, as could be expected. As long as the filter affects frequencies above the open-loop crossover frequency, there should not be large adverse effects. Figure 3-26 shows a Bode plot with the filter in place. Note the 100 Hz cutoff frequency of the filter.

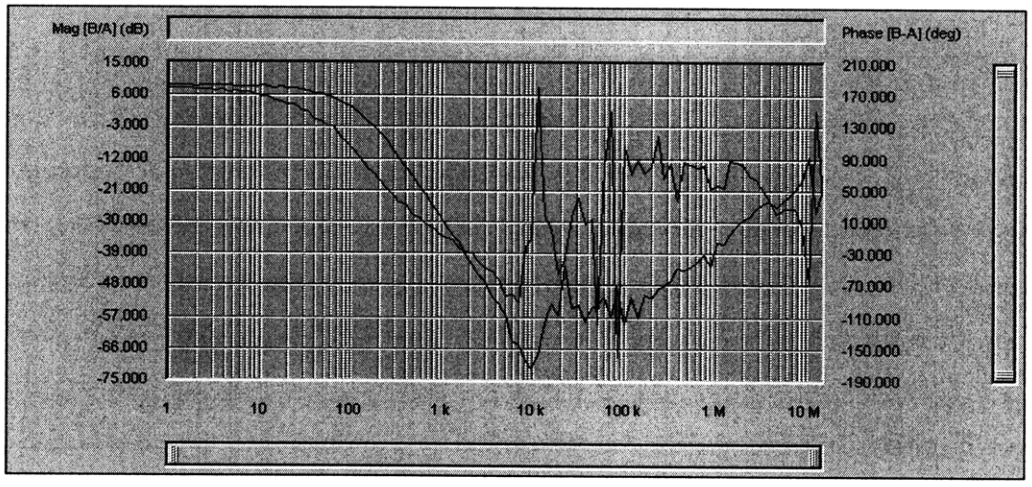


Figure 3-26: Bode plot of open loop gain with PID output filter

There was also noise in the potentiometer input, which was used to set the reference voltage or duty cycle. A similar low-pass filter was placed on this channel. In addition, a sample-hold filter was created (Figure 3-27).

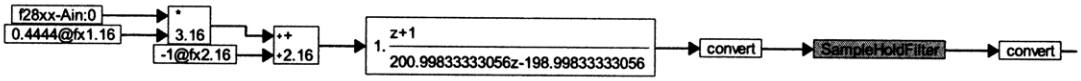


Figure 3-27: Potentiometer input filters

The reference voltage should not change quickly during the converter's normal use. The most common operation is to set the potentiometer to a value, and leave it there for a relatively long period of time. The sample-hold filter (Figure 3-28) takes a sample every 100ms. Ten samples are held and averaged together. This value is the output of the filter.

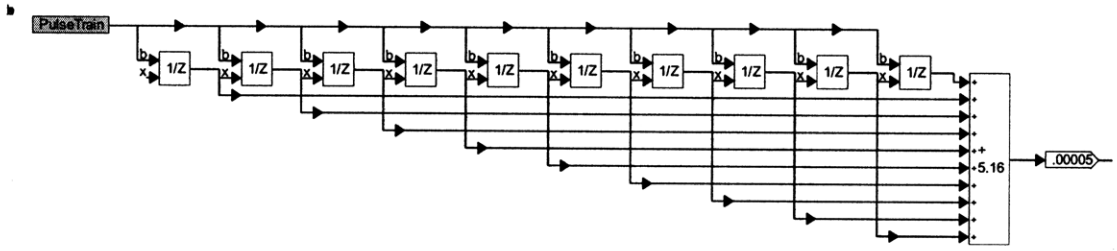


Figure 3-28: The sample-hold averaging filter

Figure 3-29 shows the input read from the potentiometer before and after the low-pass filter, and after the sample-hold filter. After this signal conditioning, the input was approximately constant. The combination of duty-cycle filtering and sample-hold filtering of the reference lead to a very stable output voltage which would still respond quickly to changes in load.

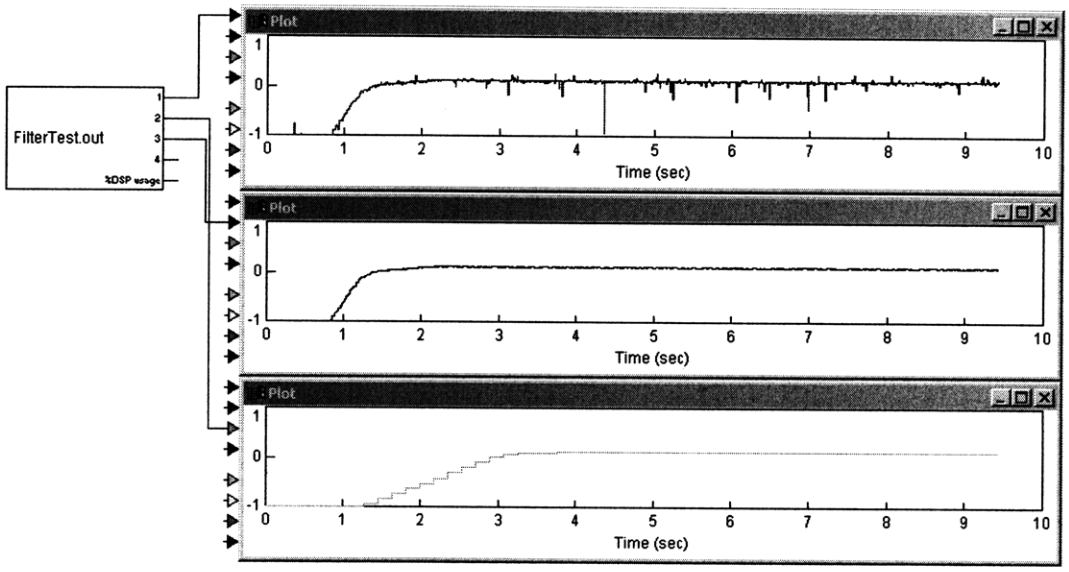


Figure 3-29: Potentiometer input: unfiltered (top); low pass (middle); sample-hold (bottom)

3.3.2 Hysteresis Around 50% Duty Cycle

Below 50% duty cycle, the output voltage of the multi-level buck is a PWM waveform from zero volts to half of the input voltage. Above 50%, it is from half of the input voltage to the full input voltage. In theory, if the converter is at exactly 50%, the switches commutate together in such a way that the output is exactly half of the input voltage. In practice, however, the commutation periods will not be this precise, and the output randomly jumps from zero to half to the full input voltage. At high power, this can easily burn out devices and create large EMI signals.

Hysteresis is needed around 50%. A hysteresis block was created in VisSim that will sample-hold 48% until 52% is achieved on a rising reference signal and vice versa for a decreasing signal (Figure 3-30). Figure 3-31 shows the hysteresis block working with a ramp as the duty-cycle command.

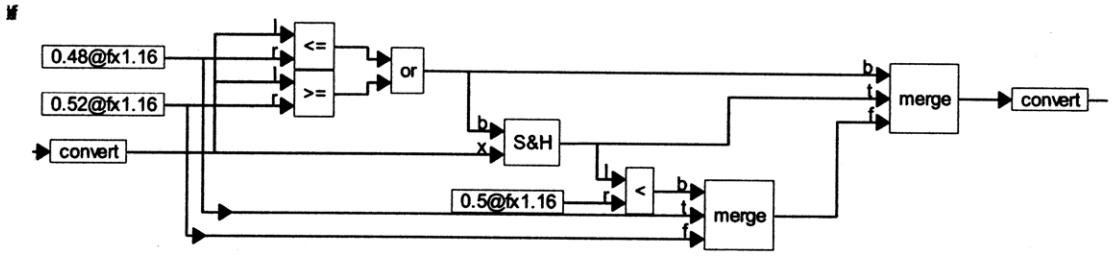


Figure 3-30: Hysteresis block

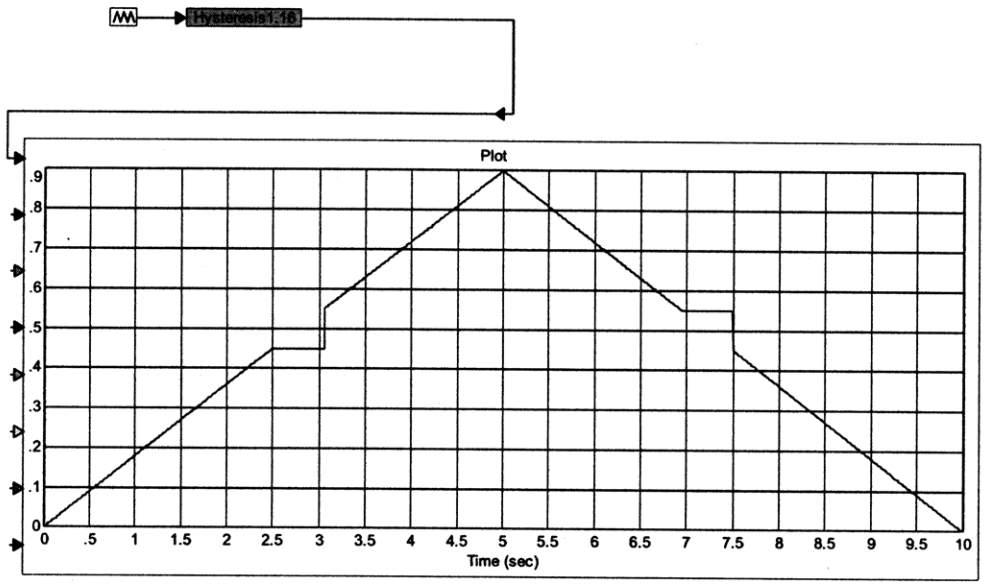


Figure 3-31: Hysteresis around 50%

3.3.3 Burst Mode

There is a potential problem with the three-level buck acting as the only controlled stage of the converter when a very low voltage output voltage is desired. If the converter input is 1100 volts and the desired output is 10 volts, a duty cycle of less than 1% is required. Operating in this range is unpredictable due to switching transients.

One method to lower the output voltage is to disable both FET switches periodically at a lower frequency (1 kHz) than their switching frequency. This is known as burst mode control. If the switches are both opened, the output of the converter goes to zero. By modulating at a low enough frequency, the floating capacitor remains balanced.

Figure 3-32 shows how this technique was implemented in VisSim. The output voltage measurement was low pass filtered to reduce noise. This value was compared to 95% of the reference value. If the comparison showed that the actual output value was greater than the reference (by 5%), the integrating PID block would increase its output. This output was compared to a 1 kHz ramp signal to create a PWM signal. When this signal was high, zero was written as the duty cycle command.

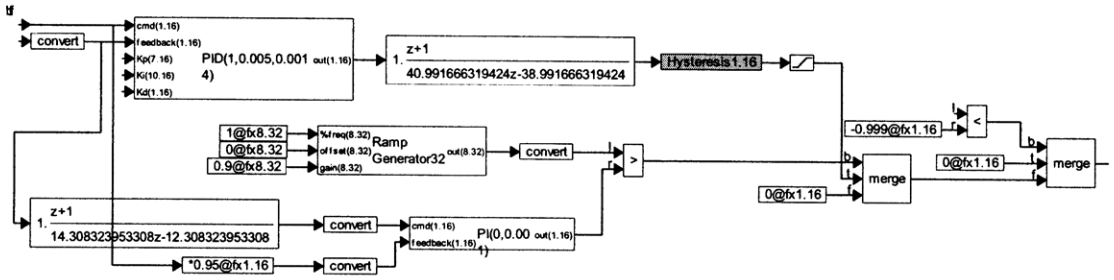
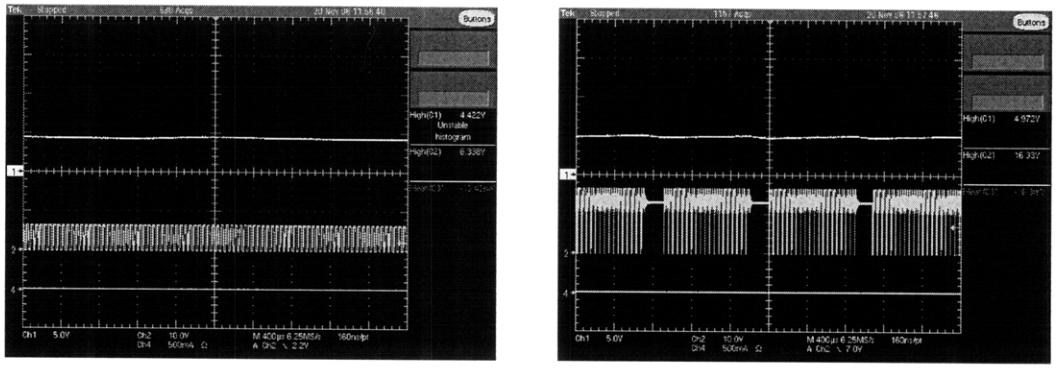
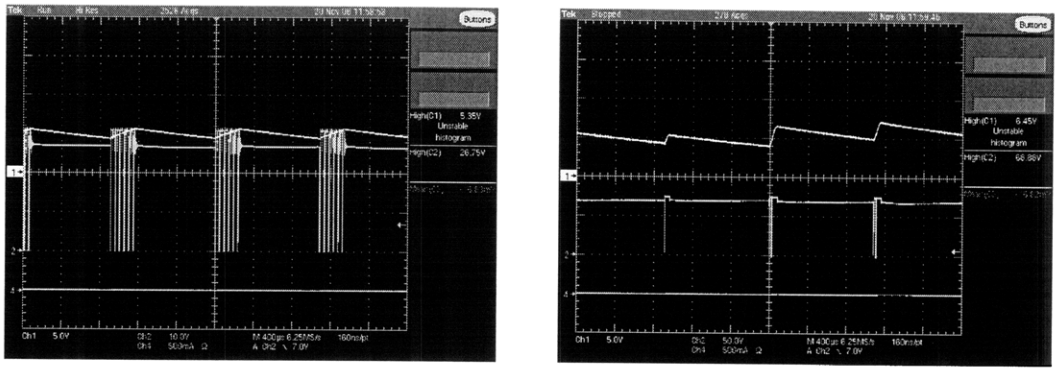


Figure 3-32: Burst mode implementation

Figure 3-33 shows the converter operating when bursting. As the input voltage increased, the time during which both FETs are off increased. Note that as the input increased, the 1 kHz ripple on the output voltage also increased. The output filter did not filter 1 kHz nearly as well as it filtered the 20 kHz it was designed for. Despite the increased ripple, the converter could now achieve very low voltages even with high inputs.



(a) (b)



(c) (d)

Figure 3-33: Converter output (5V, top trace) and V_{ds} (bottom trace) with: V_{in} = 12V (a); 35V (b); 60V (c) ; 150V (d). [ch. 1: 5 V/div, ch. 2 (a-c): 10 V/div, ch. 2 (d): 50 V/div, 400 µs/div]

Since the mode of operation was changed at low duty cycles, the loop gain of the controller changed as well. Figure 3-34 shows the frequency response of the loop gain with a high compensator gain. This was stable for normal (not bursting) operation, but at the crossover frequency of around 300 Hz, the phase margin is less than zero. The converter is not stable.

Because of this change in frequency response, the controller had to be slowed down with a lower gain so the crossover frequency occurred where there was reasonable phase margin. The revised controller had an integral gain of 0.1 instead of 1. Figure 3-35 shows the reduced-gain frequency response. If the gain were increased, the 1 kHz peak would cross zero and the converter would become unstable.

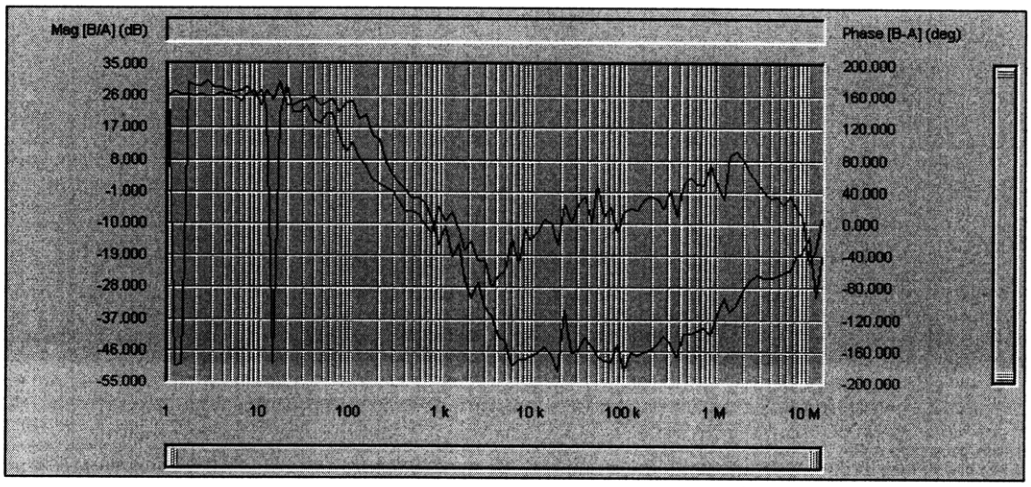


Figure 3-34: Bode plot of loop gain while bursting with high gain

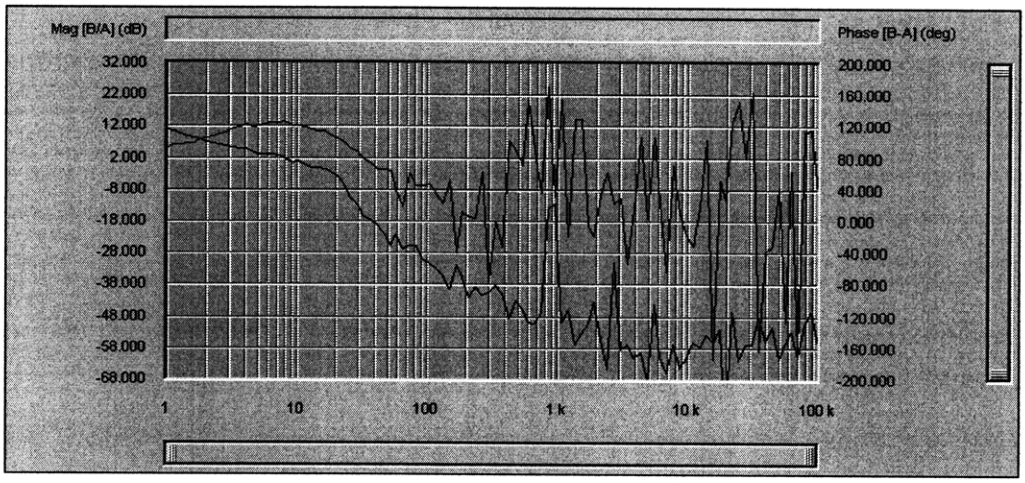


Figure 3-35: Bode plot of loop gain while bursting with lower gain

Figure 3-36 shows the step response of the converter going into and out of burst mode. The dynamic response is stable with no overshoot.

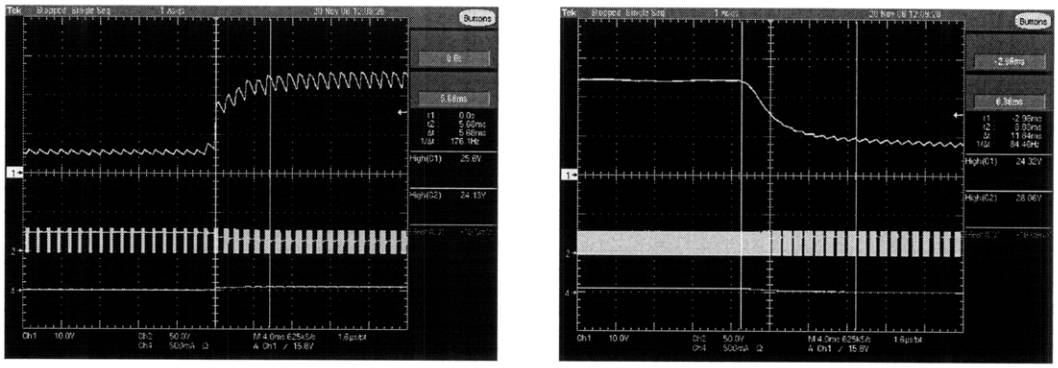


Figure 3-36: Step response during bursting. Top trace: V_{out}; bottom trace: FET voltage. [ch. 1: 10 V/div, ch. 2: 50 V/div, 4 ms/div]

Despite the slower compensator, burst mode was still advantageous. Not only did it allow a very low output voltage, but it also could control the output with no load (Figure 3-37). By turning off both FETs, the floating capacitor was able to discharge through the parasitic resistances in the devices rather than build up to the input voltage (see Figure 3-12). Since unloaded operation was required, this was a crucial achievement.

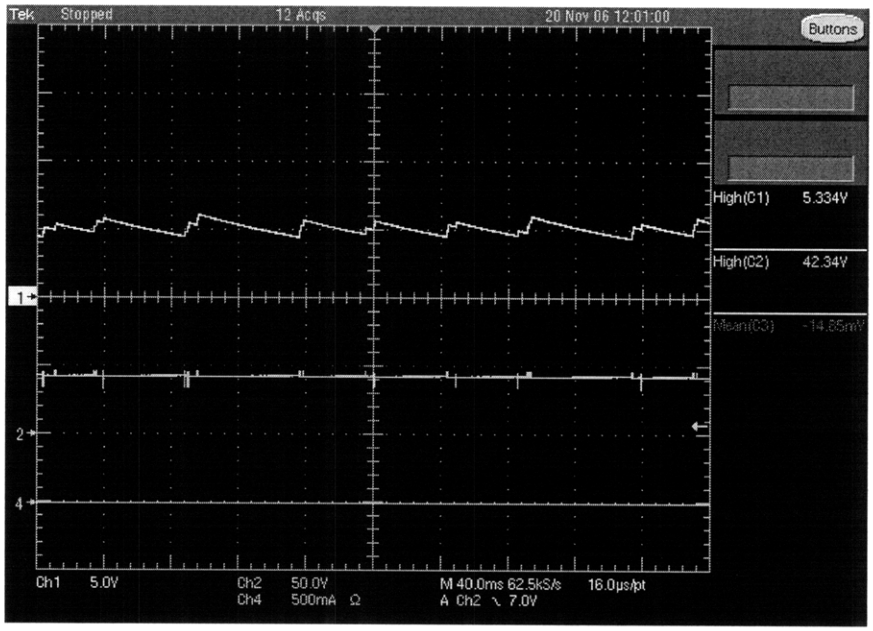


Figure 3-37: Output (5V, top trace) and V_{ds} (bottom trace) with V_{in} = 100 and no load. [ch. 1 5V/div, ch. 2: 50 V/div, 40 ms/div]

3.3.4 The Startup Ramp

The final three-stage converter needed to produce a voltage ramp at startup with a configurable slew rate. This produces a "soft start" of the converter. If the three-level buck converter is to serve as the voltage controller, it must be able to produce such a startup ramp.

This feature was implemented in VisSim. The startup ramp increases at a given rate until it hits the value 1. It will hold this value unless it is reset by a switch to zero. The reference value is multiplied by the ramp such that the output voltage is a linearly increasing voltage that goes from zero to the full reference value. Figure 3-38 shows the startup ramp implementation. Figure 3-40 shows the startup ramp operating at different skew rates.

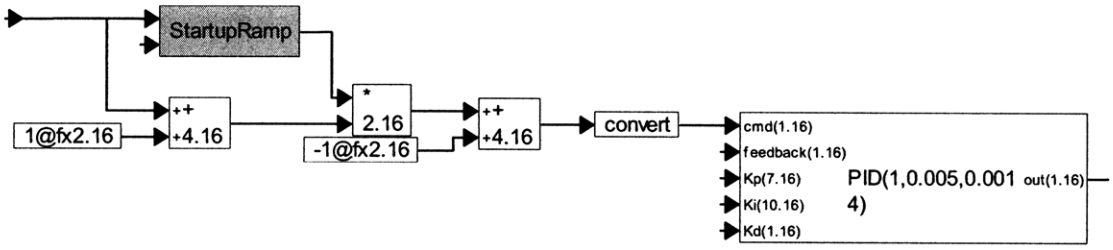


Figure 3-38: Startup ramp command generation in VisSim

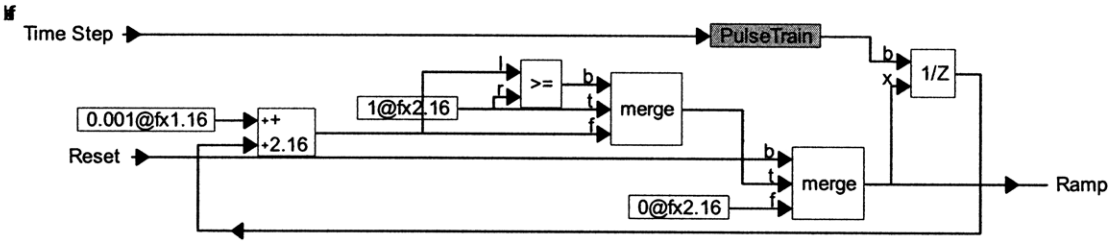


Figure 3-39: The StartupRamp block

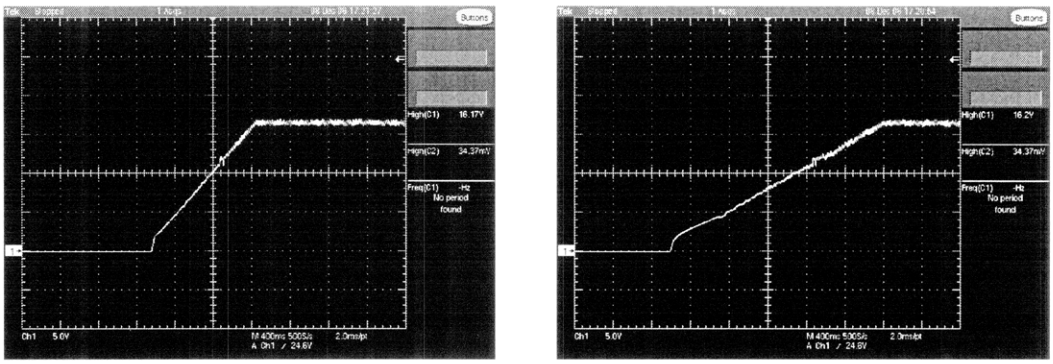


Figure 3-40: The startup ramp in operation, showing V_{out}. [5 V/div, 400 ms/div]

This chapter showed the experimental prototype of the three-level buck converter. The open-loop and closed-loop operation matched the theoretical analysis and simulation. Some extended features were also shown that allowed better performance, including the ability to achieve very low output voltages and drive the system at no load.

4 Minimizing System Losses

Before the three-stage converter could be built, it was necessary to address optimization. Both switching losses and magnetic losses can be optimized in order to achieve higher efficiency. This chapter will address those optimizations.

4.1 The Bipolar Bridge Inverter

4.1.1 Capacitive Divider

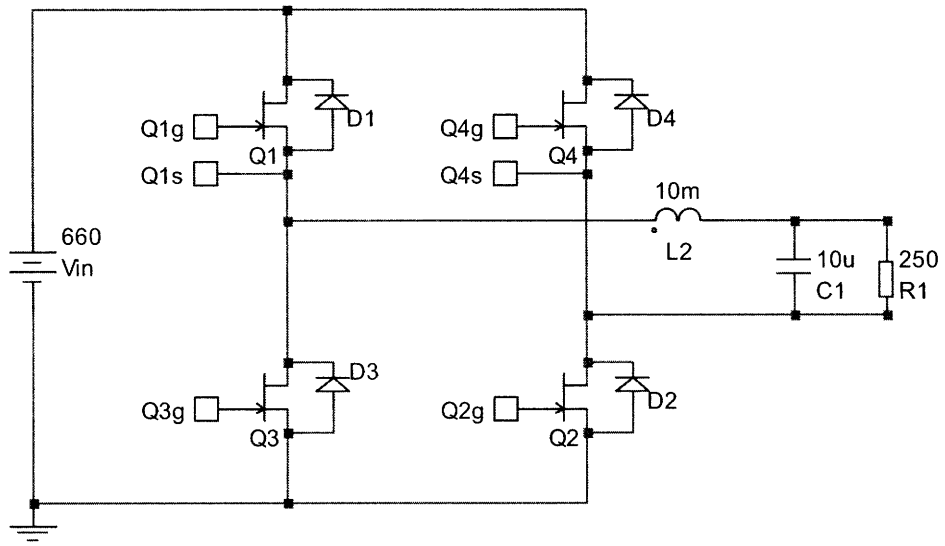


Figure 4-1: Bipolar full-bridge inverter

The final stage of the DC-to-AC inverter is a bipolar full-bridge inverter (Figure 4-1). Switches Q1 and Q3 operate in complementary fashion, as do Q2 and Q4. Figure 4-2 shows a simulated implementation of a controller for this inverter. A sine wave is compared to a sawtooth to create the duty cycle command. A dead-time is added so the complementary pairs do not commutate at the same time. The gate signals for Q3 and Q4 are a constant phase shift from Q1 and Q2, which allows the freewheeling inductor current to turn on the MOSFET's body diode before the MOSFET channel is enabled (Zero Voltage Switching). The output of the inverter is a sine wave with the same frequency as the controller's sinusoid (Figure 4-3).

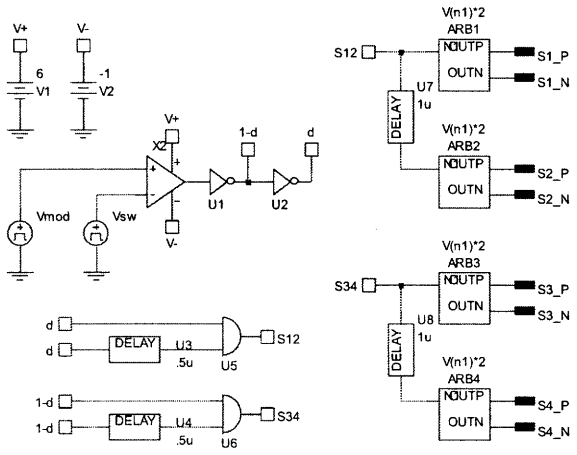


Figure 4-2: Bipolar inverter control

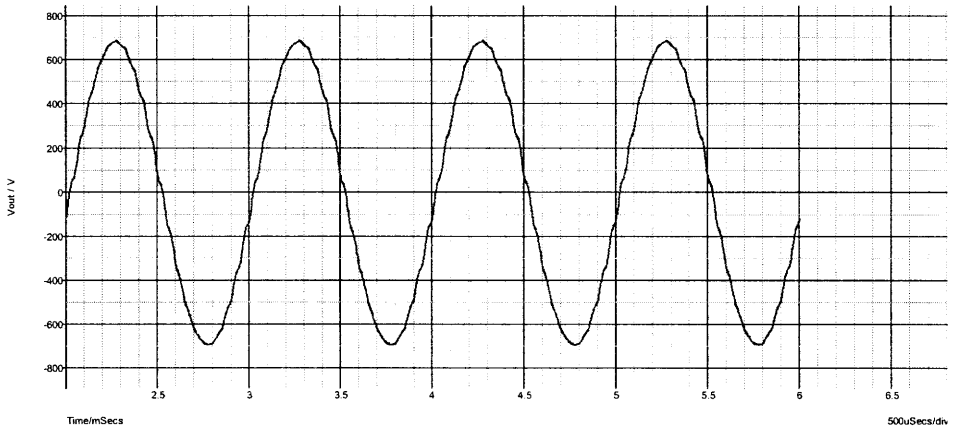


Figure 4-3: Bipolar inverter output voltage

The MOSFETs were chosen for their high temperature characteristics, but the internal body diodes have poor transient characteristics, resulting in high switching losses. Because of these losses, the converter cannot run at full power without burning out the FETs. A potential solution to aid the turn-on transitions was found by adding additional blocking and anti-parallel diodes (Figure 4-4 a). This allowed an external diode with better transient performance to handle the freewheeling current when current was flowing in the source-to-drain direction.

A problem remained that the drain to source voltage of the MOSFET did not fall to zero as expected during the dead time between switches. It held a high-voltage which

resulted in a large current spike in the blocking diode at turn-on. Adding a 10 nF capacitor solved this problem (Figure 4-4 b). This solution had to be analyzed in order to figure out the cause of the problem and to explain the solution.

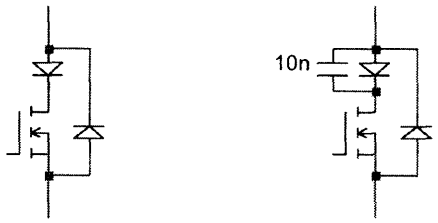


Figure 4-4: (a) FET with blocking and anti-parallel diodes; (b) with added capacitor

4.1.1.1 Simulations

Transim's Simetrix circuit simulator was used to better understand the circuit. Figure 4-5 shows a test circuit that recreates the problem. Switch S1 is closed, thus charging the inductor. It is then opened, allowing the anti-parallel diode D1 to conduct the freewheeling current. Finally, Q3 is turned-on as it would be after a short dead-time. Figure 4-6 shows that this circuit accurately portrays the current-spike and intermediate voltage problems. The top graph shows the current through the anti-parallel diode and the current through the FET. The bottom graph shows how the drain-to-source voltage of the FET plateaus at 400 volts until the FET is turned-on.

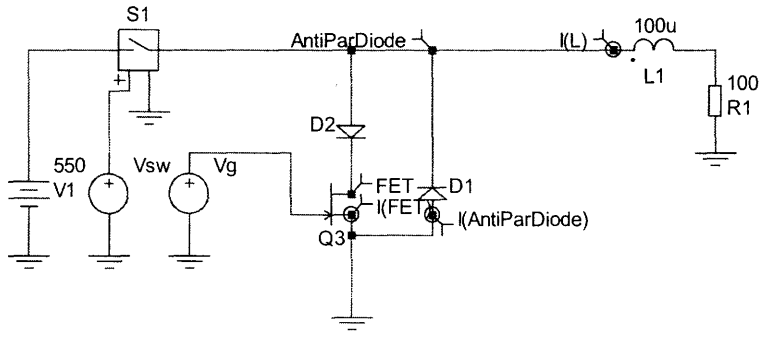


Figure 4-5: Isolated switch test circuit

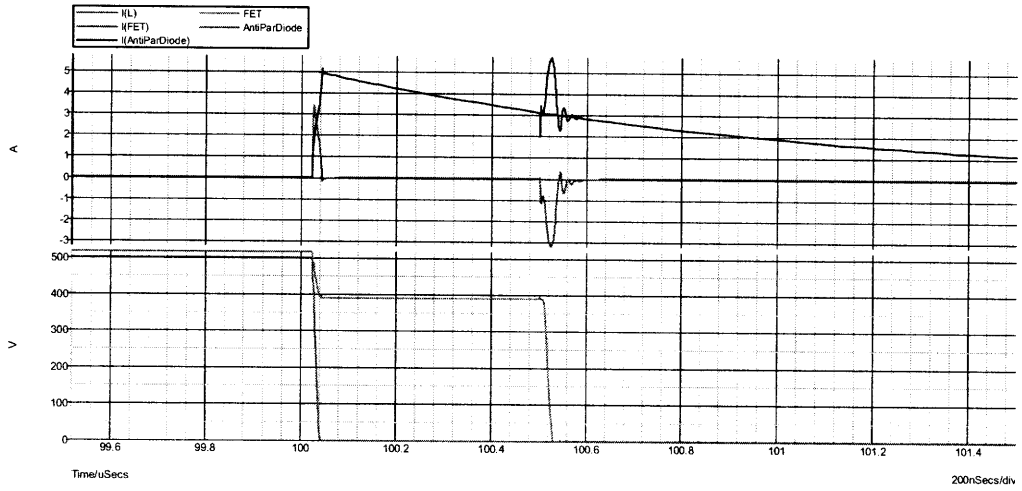


Figure 4-6: Waveforms from isolated switch test circuit

As S1 turns off, the inductor current must come from the FET/Diode leg. During this initial stage before the anti-parallel diode conducts, the current is drawn from the junction capacitance of the two diodes and from the drain-to-source capacitance of the MOSFET. In other words, there is a capacitive current divider for a short period of time. In theory, this would cause the drain-to-source voltage to change until the anti-parallel diode starts to conduct. This voltage would drop to zero as the switch turns on. The simulated results matched this scenario.

Figure 4-7 and Figure 4-8 show a simulation of this capacitive divider with a current source extracting current. The waveforms give the correct response. There is a current spike, and the mid-point voltage drops and levels out to an intermediate value. However, in this simplified model, there is nothing regulating the voltage levels of any of the devices.

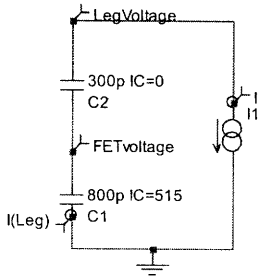


Figure 4-7: Capacitive divider of blocking diode and MOSFET

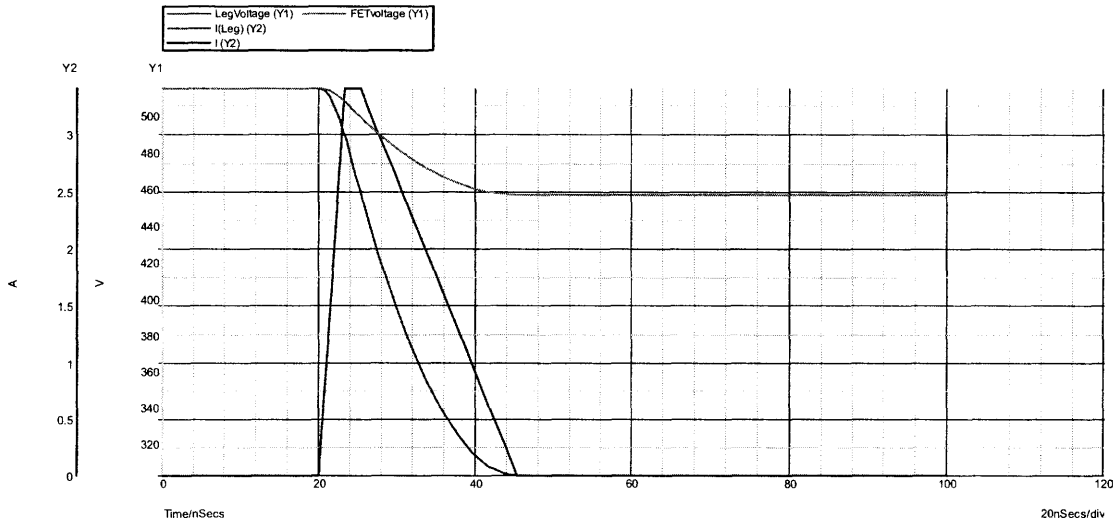


Figure 4-8: Waveforms of capacitive divider circuit

Figure 4-9 and Figure 4-10 show the same capacitive divider with extra circuitry added to regulate the voltage to 500 volts and to incorporate the anti-parallel diode. The voltage and current behave as expected with the appropriate values; the mid-point voltage drops to roughly 400 volts while the anti-parallel diode is commutating, and there is a current spike through the capacitive leg.

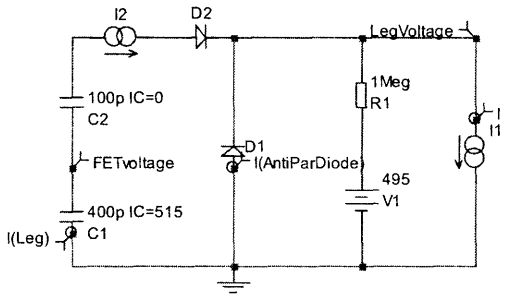


Figure 4-9: Capacitive divider with voltage regulation

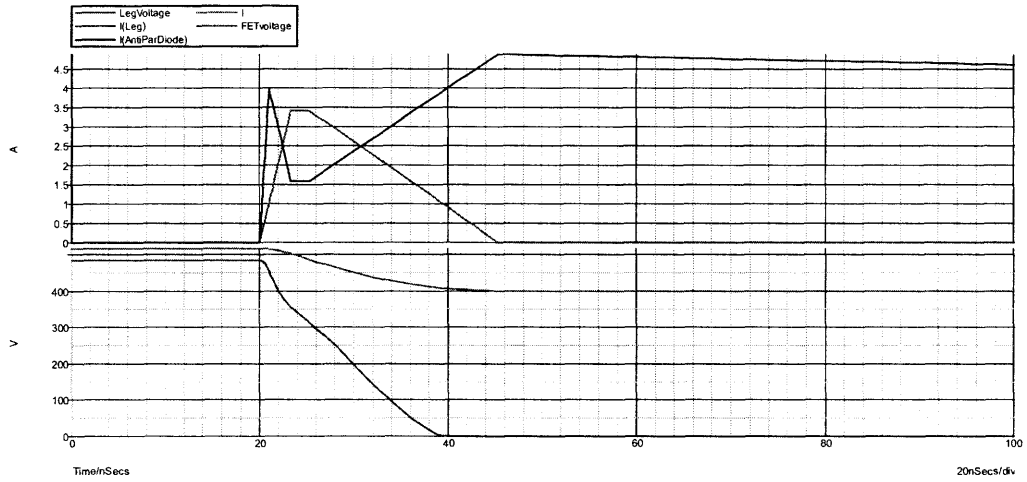


Figure 4-10: Waveforms of capacitive divider with voltage regulation

4.1.1.2 Results

Knowing the cause of the intermediate voltage, it is clear how adding a capacitor can help. By changing the capacitive current divider's values, the mid-point voltage can be controlled. Adding the 10 nF capacitor allowed the mid-point voltage to plateau much closer to zero, reducing the turn-on stresses of the switch. Figure 4-11 shows the dramatic difference of the mid-point voltage with and without a 10 nF capacitor around the blocking diode.

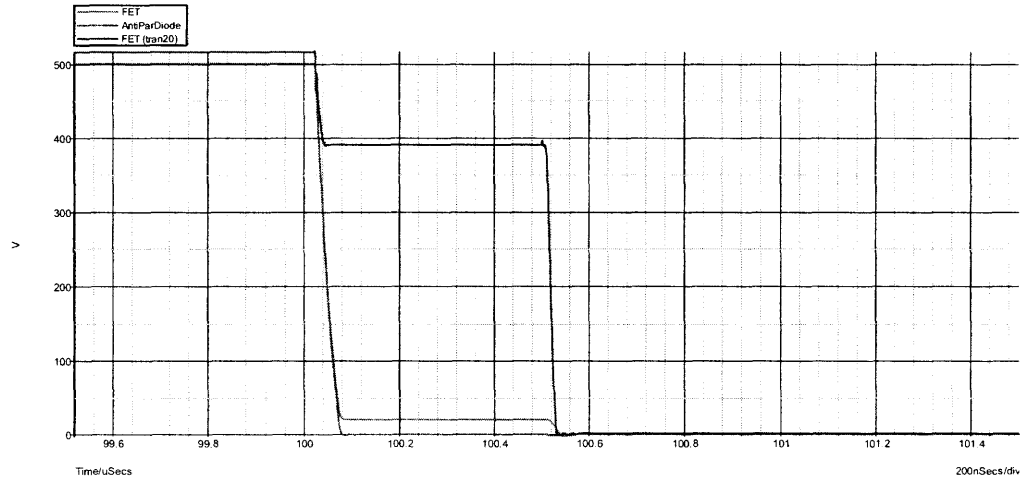


Figure 4-11: Drain-source voltage with and without capacitor

4.1.2 Switch Losses

The primary goal in designing the bipolar bridge inverter was to maximize efficiency. Because of the poor transient characteristics of the MOSFET devices, these losses were looked at first [appendix 8.2]. In order to get an accurate power loss estimate, the area under the power loss curve (total energy) needed to be known. Simetrix could not do this calculation, so a MATLAB function was written to calculate the losses based on the simulation waveforms [appendix 8.3]. An example is provided below for the first calculation.

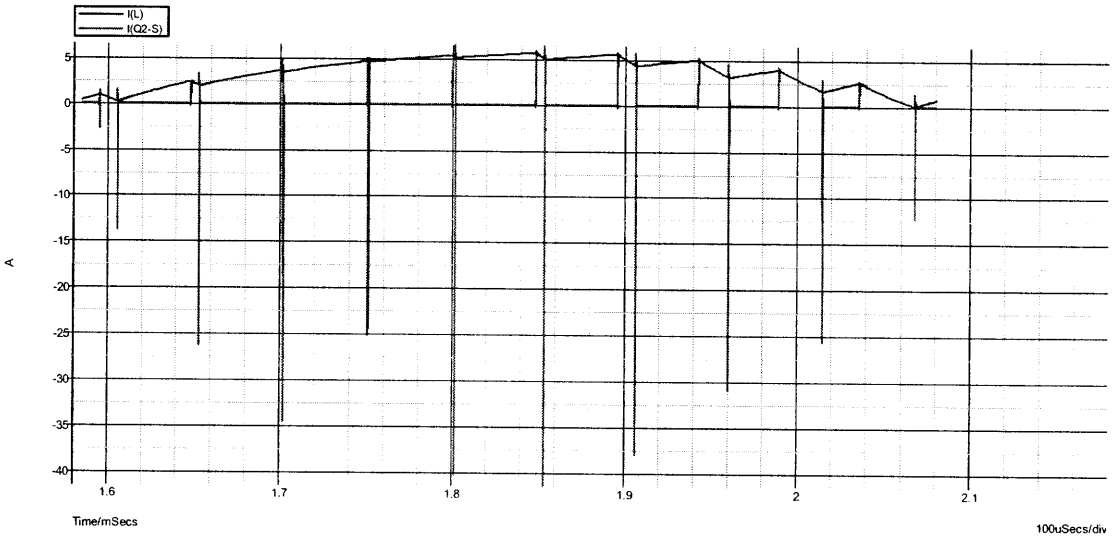


Figure 4-12: Current during source-to-drain half of the AC cycle

First, the section of time was looked at in the 60 Hz AC cycle when the current is flowing in the source-to-drain direction through a switch, as shown in Figure 4-12. The voltage and current data from the MOSFET were exported to a file to be analyzed in MATLAB.

A graph of the current and voltage, as well as the power loss (absolute value of the product of the two) is displayed after running the MATLAB function. For this half of the cycle, an average of 4.79 watts of power is dissipated in the MOSFET.

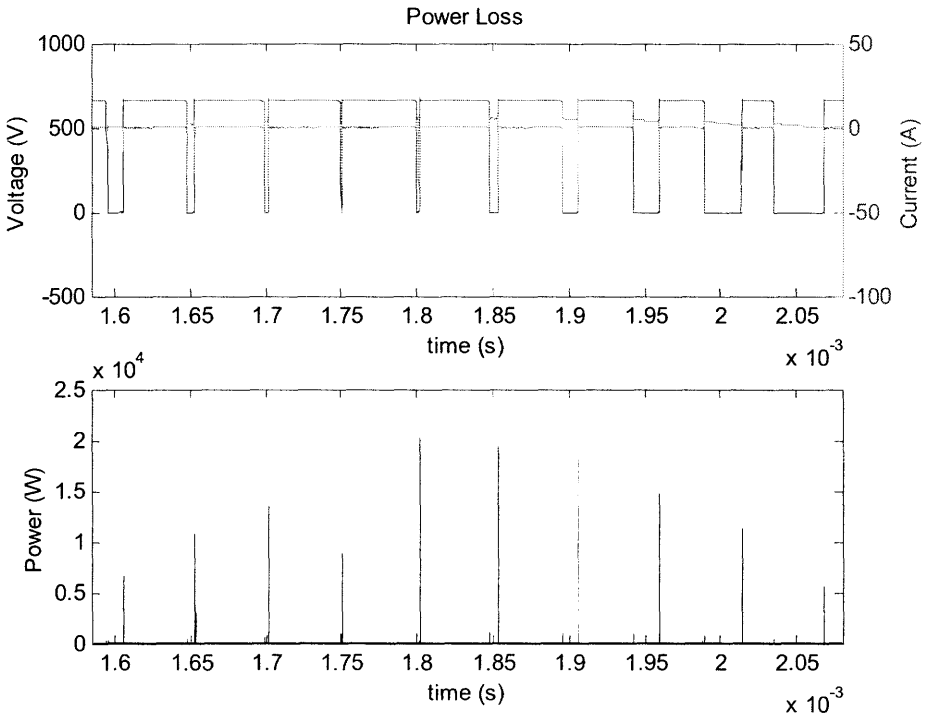


Figure 4-13: MATLAB loss function output

Repeating this for the other half of the AC cycle, the average power loss was found to be 10.3 watts for a full AC cycle. Thus, the greatest power loss occurs when the freewheeling current travels only in the MOSFET channel, not when the body diode can carry the current. This is because the MOSFET must hard-switch during this interval.

Breaking this loss down further, it was found that over 50% of the power loss occurs during turn-on. Due to this dominating factor, efforts were concentrated on reducing the turn-on losses.

4.1.2.1 Simulations

A circuit was designed to simulate this hard-switched turn-on of the MOSFET (Figure 4-14). The test circuit is a half-bridge that keeps a constant current in the load. When the switch Q1 is turned on, the load current flows through the MOSFET channel. Switch Q2 is kept off, acting like a freewheeling diode. Several combinations of loss

prevention techniques were tried using the blocking and anti-parallel diodes as well as turn-on inductive snubbers [19]. Results are discussed in section 4.1.2.3.

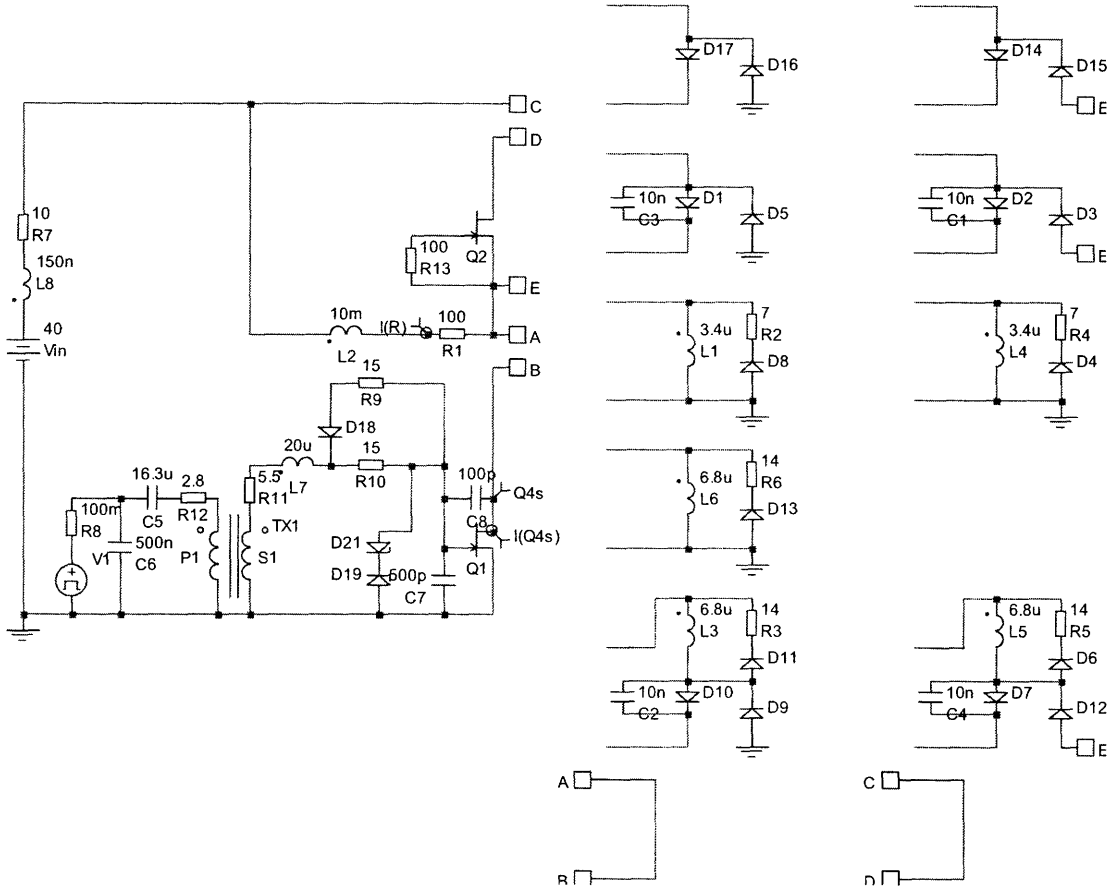


Figure 4-14: FET loss simulated test circuit with parasitics and gate drive

4.1.2.2 Experimental Data

This circuit was also built in the laboratory (Figure 4-15 and Figure 4-16). The left side of the test circuit was a gate driver. The labeled wires on the rest of the circuit could be jumpered together to form the different combinations of snubbers and diode circuits around each FET. The free Magnetics inductor design program was used to compute the windings and cores needed to make the snubber inductors. The 3.4 μH inductors were made with Magnetics 55381-A2 powdered ferrite cores with 9 turns of 22 AWG wire. The 6.8 μH inductors were made with Magnetics 55381-A2 powdered ferrite cores with

13 turns of 22 AWG wire. The capacitors were TDK C1608X8R1H103K surface mount capacitors. The results from these experiments are discussed in the following section.

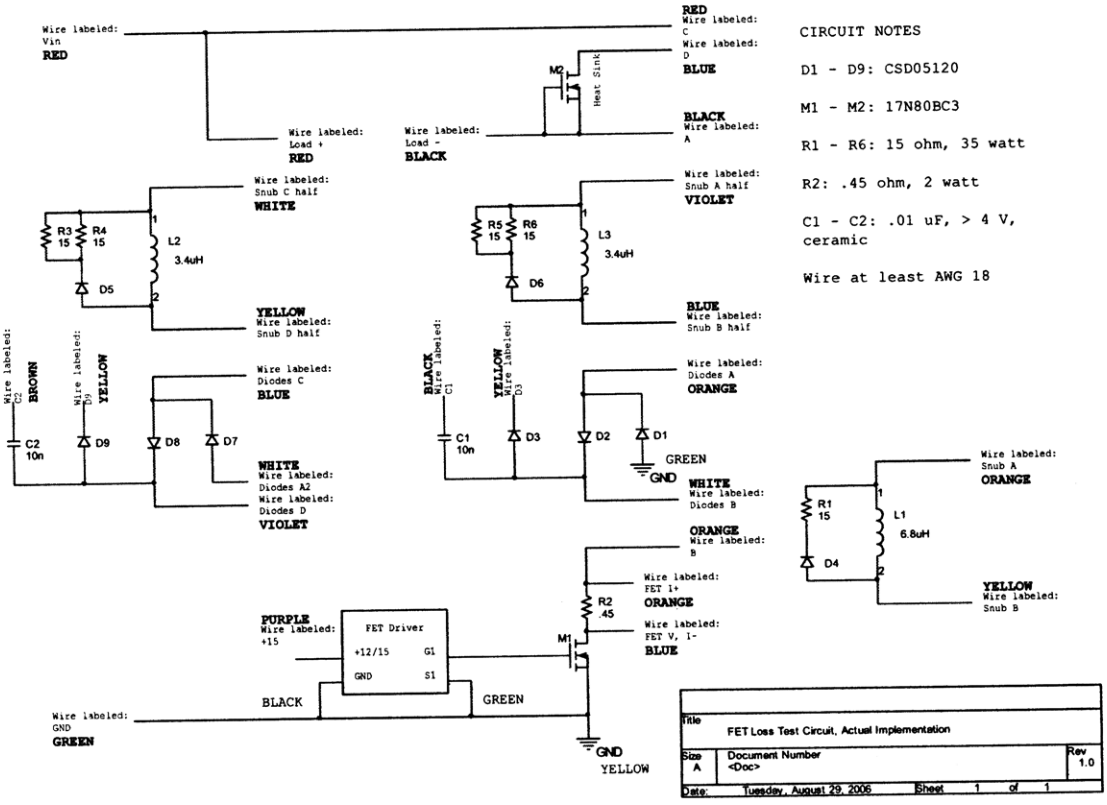


Figure 4-15: FET loss test circuit schematic

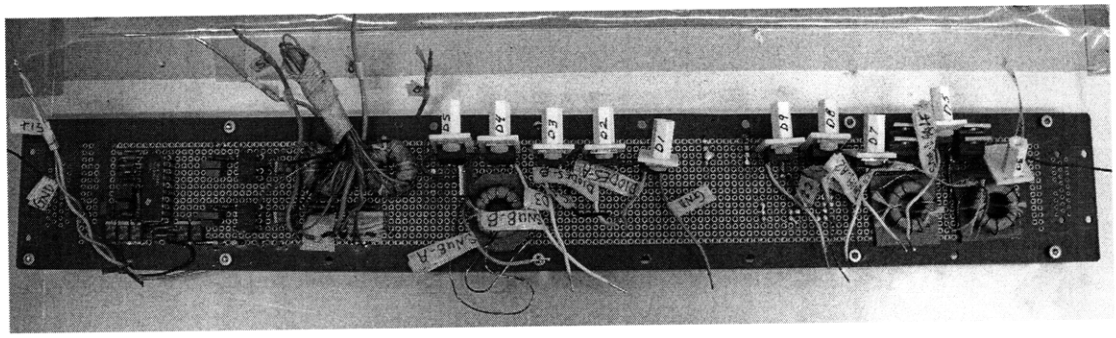


Figure 4-16: FET loss experimental test circuit

4.1.2.3 Results

The results are best viewed with the simulation and experimental oscilloscope graphs side-by-side. The first tests are with Vin = 40 volts. The important tests are as follows:

FETs alone:

- Current spike (*after* Vds drops) of ~ 4 A
- Some ripple after initial current spike
- Peak power ~ 20 W
- Power plateaus at peak current, then ripples

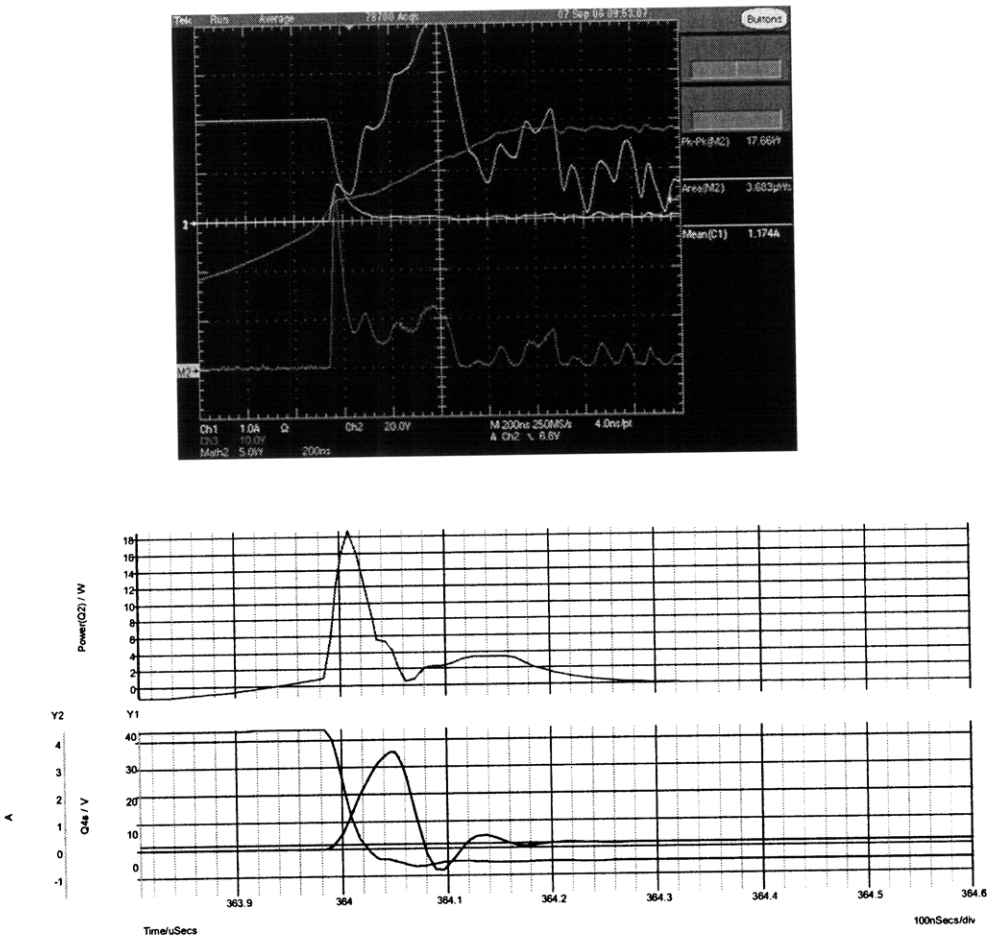


Figure 4-17: FETs alone

In simulation, each MOSFET dissipated roughly 6.7 watts of power over one AC cycle with Vin = 660 volts.

Diodes:

- Smaller current spike (0.8-1.5 A) at turn-on
- Less ripple than with just FETs (more noticeable in experimental results due to extra parasitics)
- Peak power ~ 20 W, similar to just FETs
- Less power loss after peak

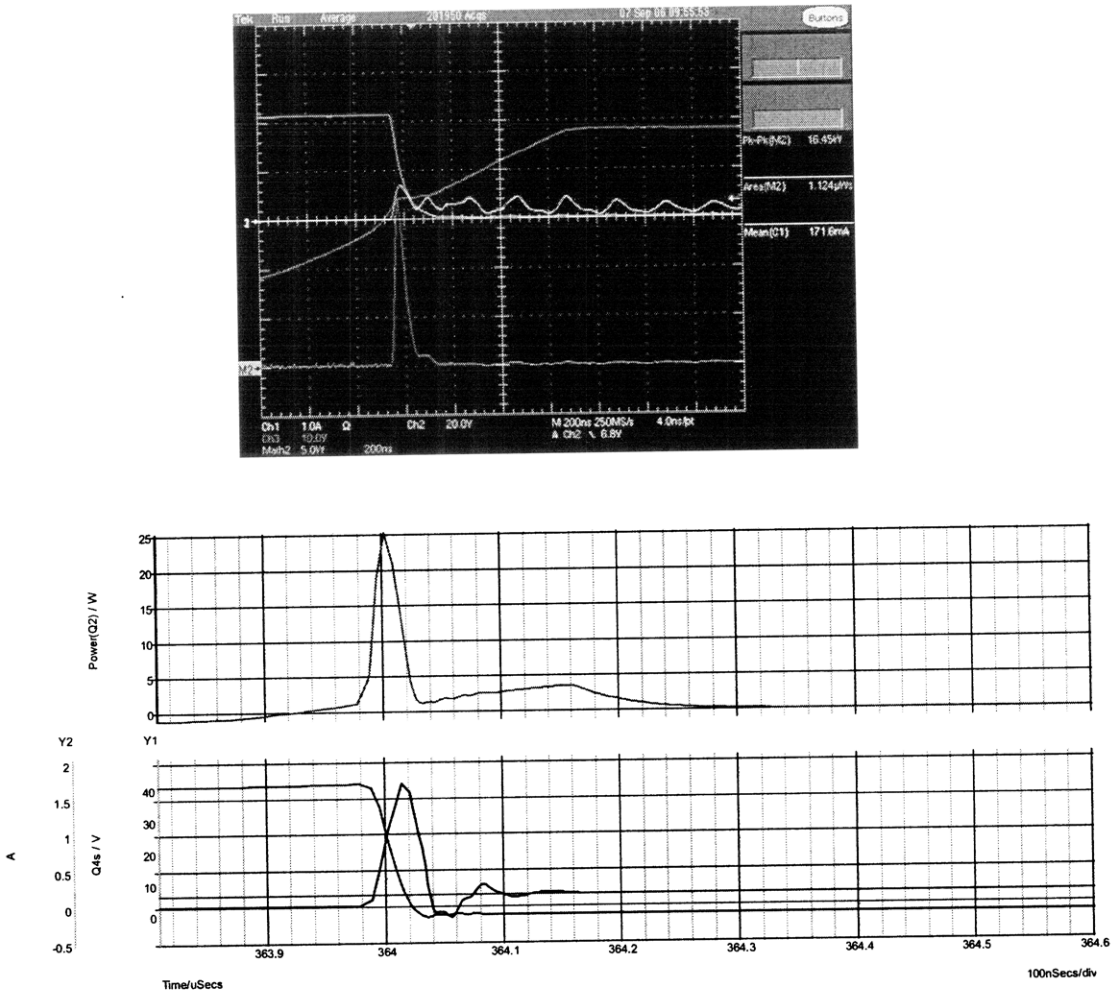


Figure 4-18: Diodes

Diodes with 10 nF Capacitor:

- Almost identical to "Diodes"
- More current ripple
- Peak power ~ 20 W, same as "Diodes"
- Extra ripple in experimental results slightly affect power

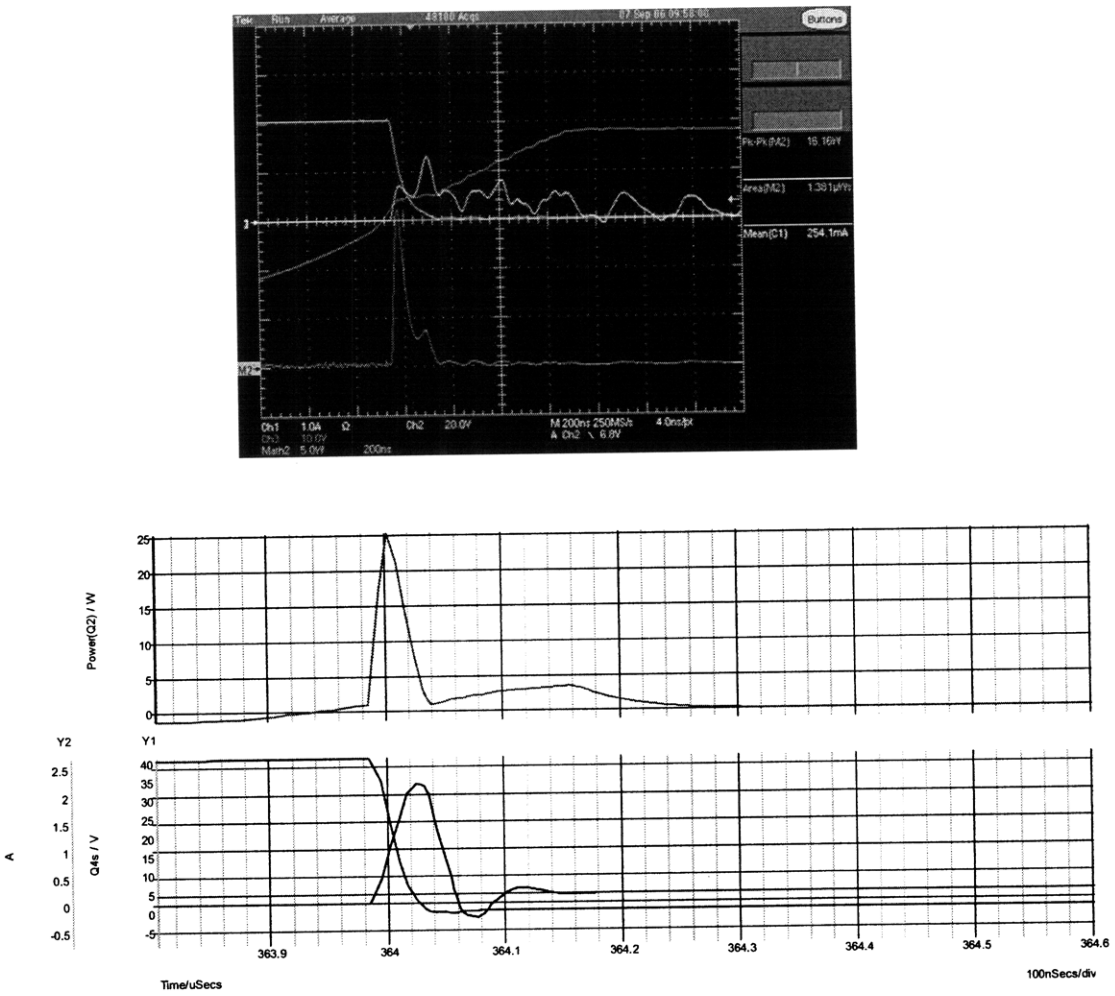


Figure 4-19: Diodes with 10 nF capacitor

In simulation, each MOSFET dissipated roughly 4.6 watts of power over one AC cycle with Vin = 660 volts. The diodes combined for an additional 2.4 watts per pair, for a total of 7.0 watts of power dissipation.

Snubbers (L = 3.4 uH):

- Current spike (*during* Vds drop) of ~ 0.5 A
- Large current spike well after Vds drop
- Peak power ~ 10 W: down from ~ 20 W
- Power peaks, drops, then rises slightly with large current spike

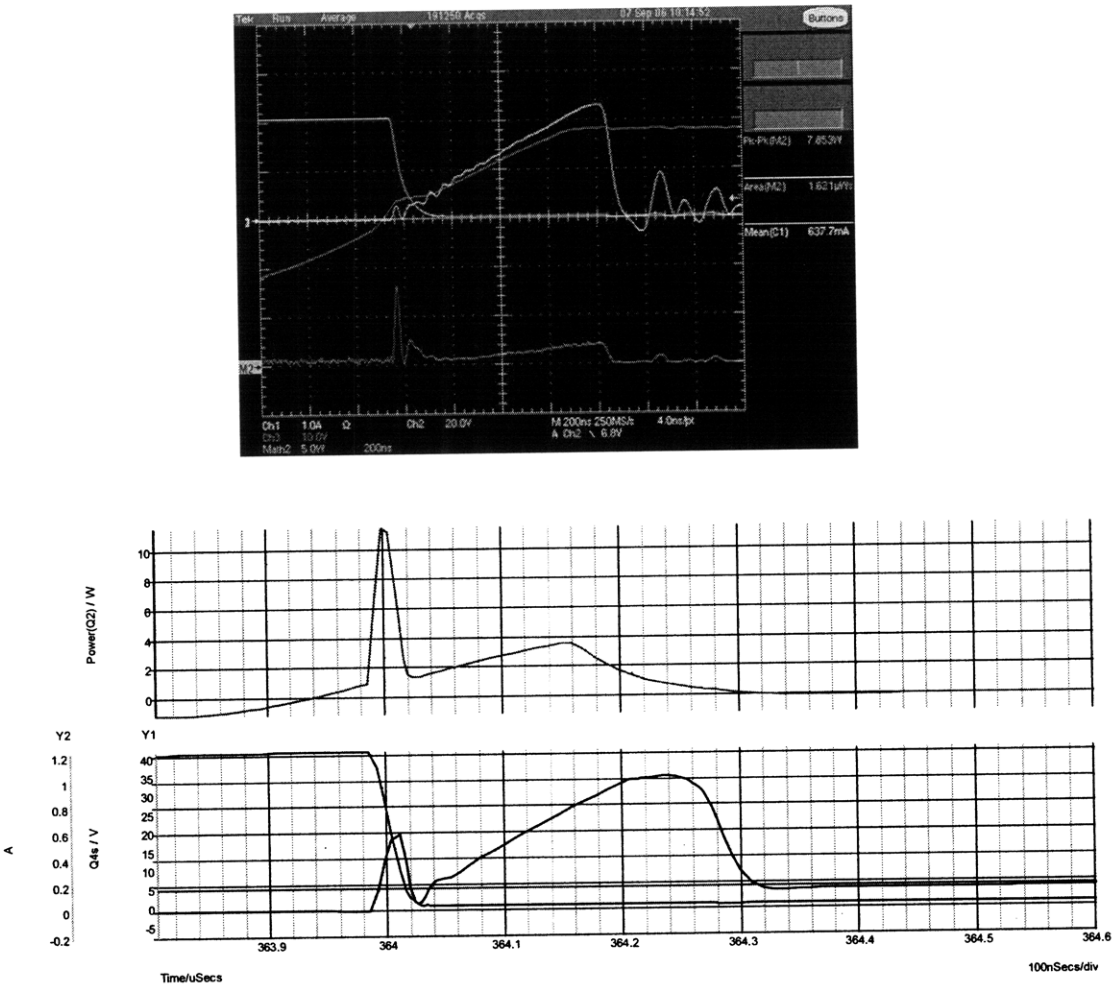


Figure 4-20: Snubbers

In simulation, each MOSFET dissipated roughly 4.3 watts of power over one AC cycle with Vin = 660 volts. The diode and resistor dissipated an additional 4.5 watts, for a total of 8.8 watts.

Bottom FET: Snubber (L = 6.8 uH); Top FET: FET Alone:

- Nearly identical to using both snubbers, half the inductance

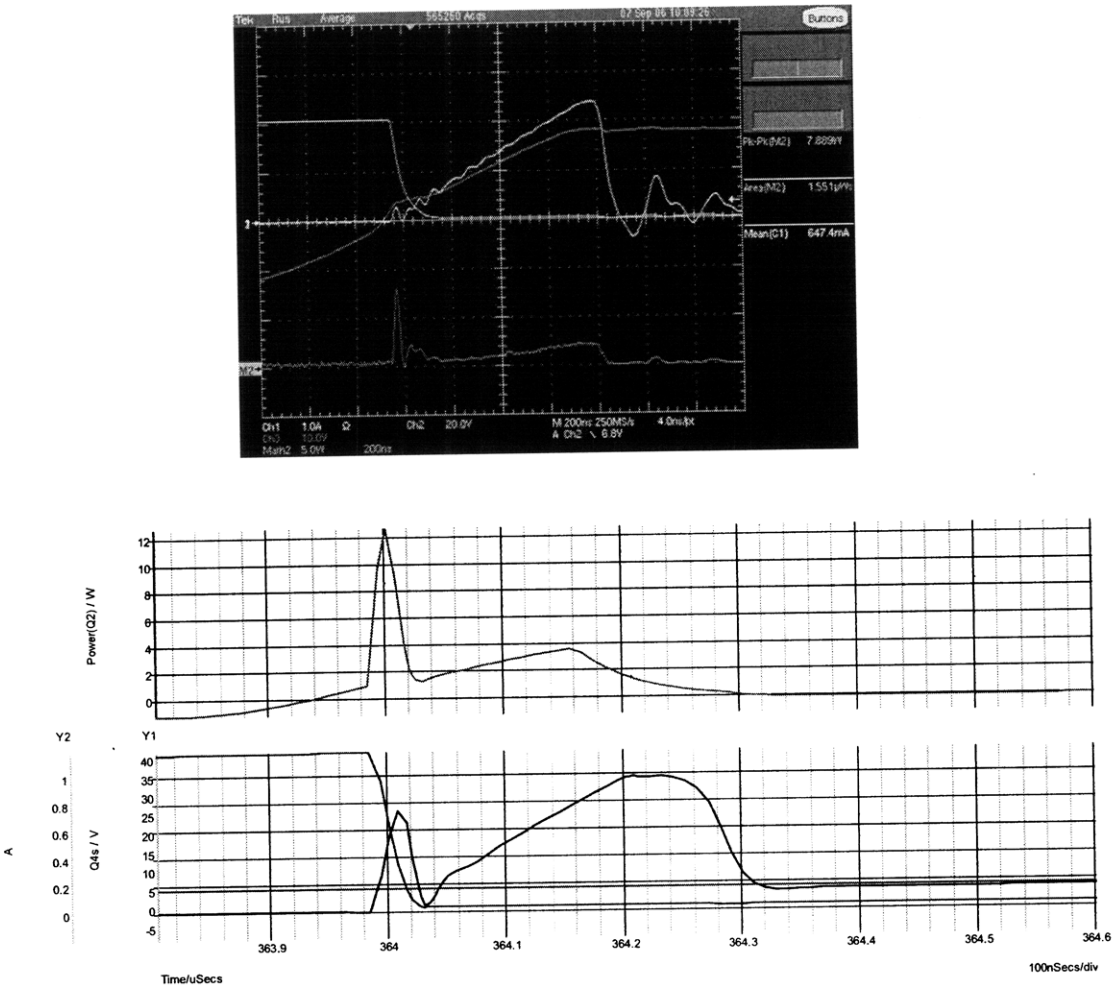


Figure 4-21: Snubber and FET alone

Bottom FET: Snubber (L = 6.8 uH); Top FET: Diodes with 10 nF Capacitor:

- Initial current spike is slightly higher as with the other snubber cases
- Secondary current spike is much lower: ~ same value as first spike
- Peak power remains at ~ 10 W
- Power loss after spike is lower (better seen experimentally)

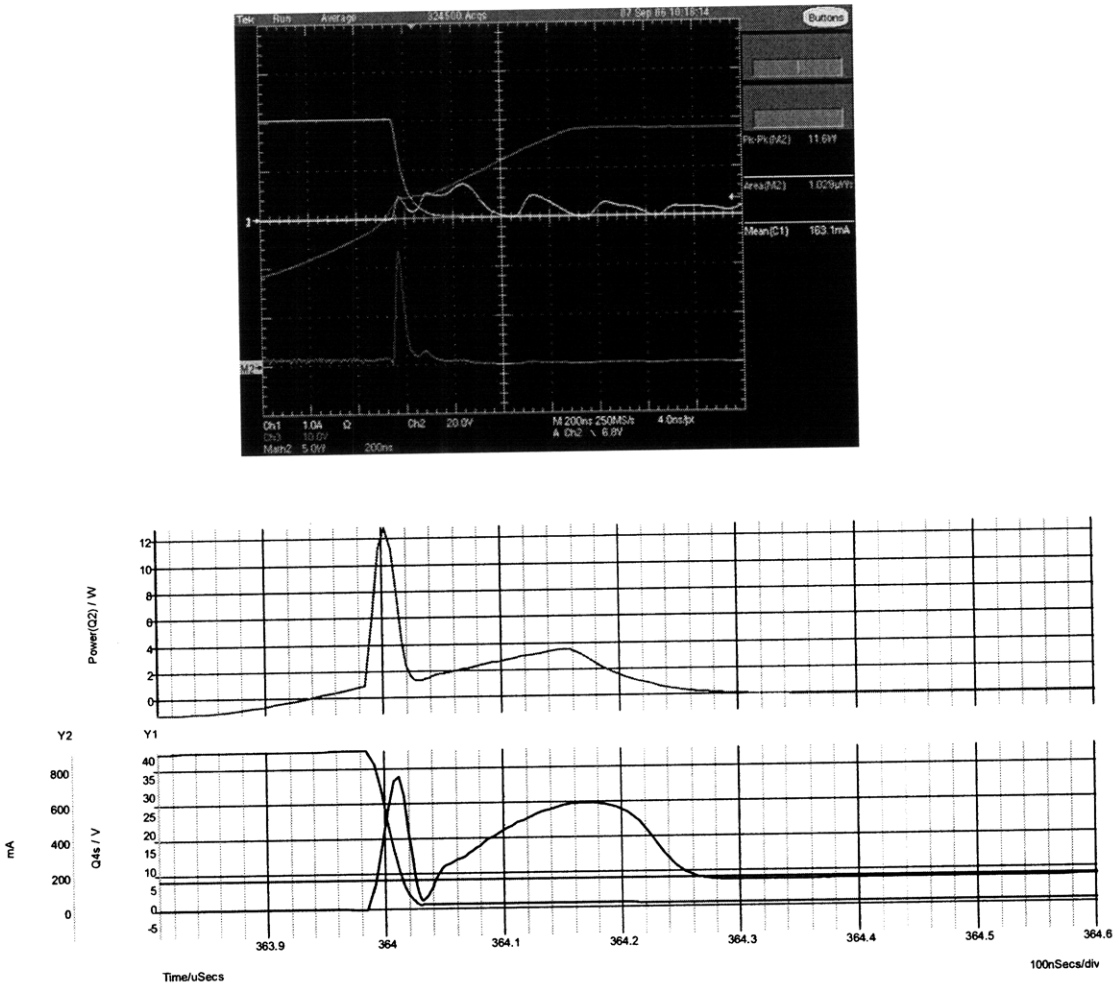


Figure 4-22: Snubber with diodes and capacitor

Diodes (Vin = 200 V):

- Higher voltage to test validity of simulations
- Current spike of ~ 3 A
- Dip and another current spike during turn-on
- Peak power of ~ 300-400 W
- Power plateaus after first current spike, until Vds drops

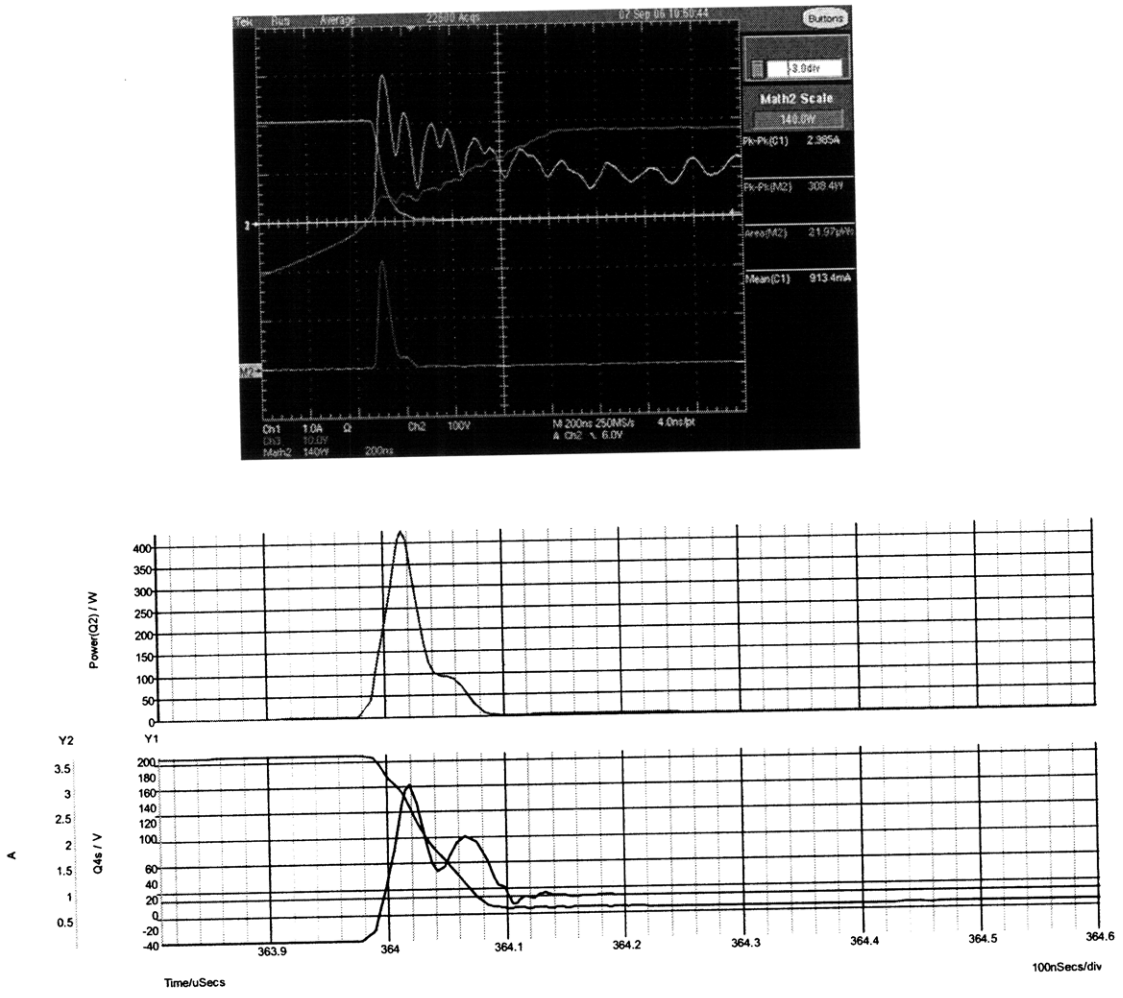


Figure 4-23: Diodes with Vin = 200 volts

Some conclusions can be drawn from this data. With the test circuits, the FETs alone were the most efficient. However, they will not work alone at full power. Adding diodes and a capacitor reduces the FET switching losses and keeps the system almost as

efficient. The snubber configurations reduce the FET losses, but at the price of lower efficiency.

A more important conclusion was the strong correlation between simulated and experimental data. Looking closely at the graph shapes and values, it is clear that the simulation accurately showed how the circuit would work experimentally. Efficiency calculations were simulated at full power with the entire bipolar bridge inverter.

With the FETs alone, the measured efficiency was around 92%. With the additional diodes and capacitor, the efficiency increased substantially so that it could not be accurately measured. This large discrepancy is because the diodes have much better transient characteristics.

The final bipolar inverting stage of the converter will use the topology as shown in Figure 4-24 to minimize MOSFET and overall losses.

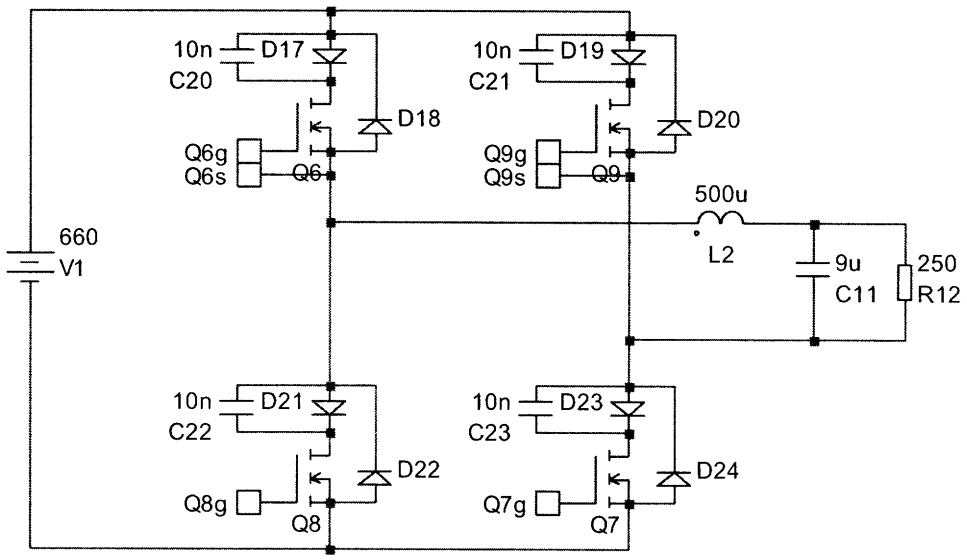


Figure 4-24: Bipolar full-bridge inverter with blocking and anti-parallel diodes

4.2 Magnetics

4.2.1 Inductor Design

Optimization of the magnetic components in a power converter is an often-overlooked aspect of design. The following procedure, sometimes known as the K_g or geometrical constant approach [Erickson, chapter 14], was used to create a MATLAB script to aid in the design of inductors. An example will be followed in detail in the next section.

Note that the Kg method is based on when low-frequency copper loss dominates within an allowed flux density limit. The approach can still be used in this case (even though skin effect, proximity effect, and core losses are not negligible) and will help reduce copper losses, but the result will not be optimal.

4.2.1.1 Process

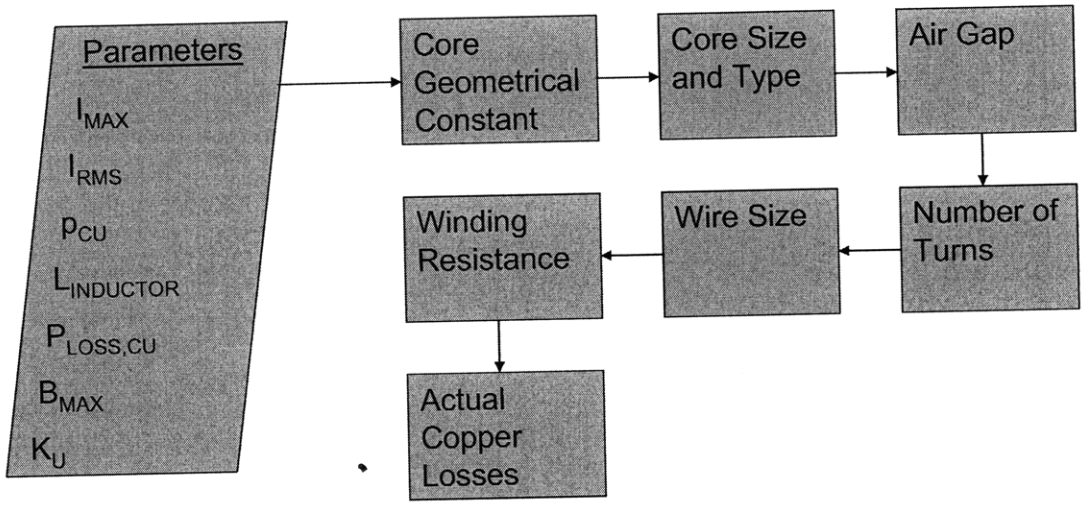


Figure 4-25: Inductor optimization process

One inductor in the DC-to-AC converter is the AC output filter inductor. The optimization procedure will be walked through using this as an example. The algorithm starts by computing all input parameters. The converter is switching at 20 kHz, so an LC-filter breakpoint of around 1000 Hz is desired. A reasonable capacitor to use is a

high voltage, high temperature 9 uF capacitor, as can be found in the Novacap line of ceramic capacitors.

$$f_c = \frac{1}{2\pi\sqrt{LC}}, \text{ or in this case: } L = \frac{1}{(2\pi \cdot 1000)^2 \cdot 9E^{-6}} = 2814uH$$

An inductance of 2 mH gives a maximum output voltage ripple of 3.6% (Figure 4-26 and Figure 4-27) and current ripple of 5 mA. From simulation, the maximum current through the inductor is 6.3 A. The RMS current is 2.6 A_{rms} (Figure 4-28).

Other input parameters include the resistance of copper ($1.724x10^{-6}$ Ω-cm), the ideal copper power loss (1 watt), the saturation flux density of the core material (0.5 T) and K_u, the packing factor of the windings (typically 0.4).

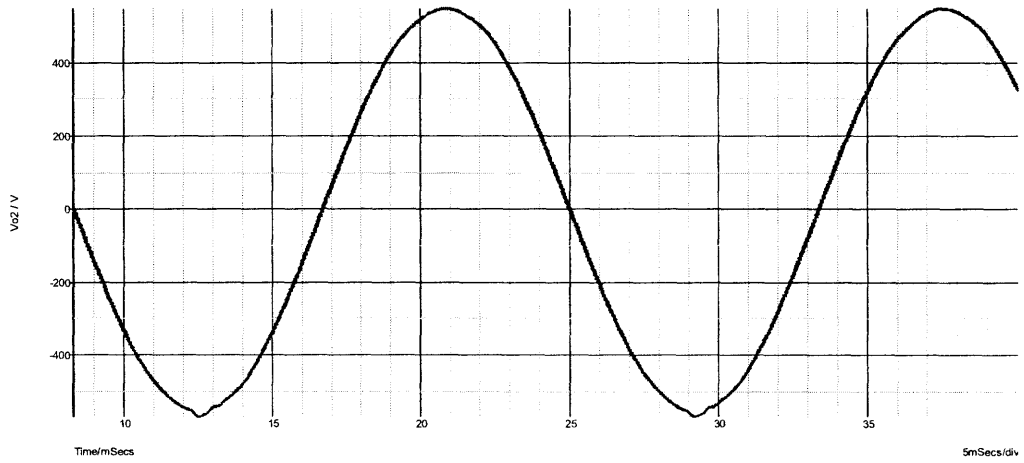


Figure 4-26: Inverter output with 9uF and 2000 uH filter

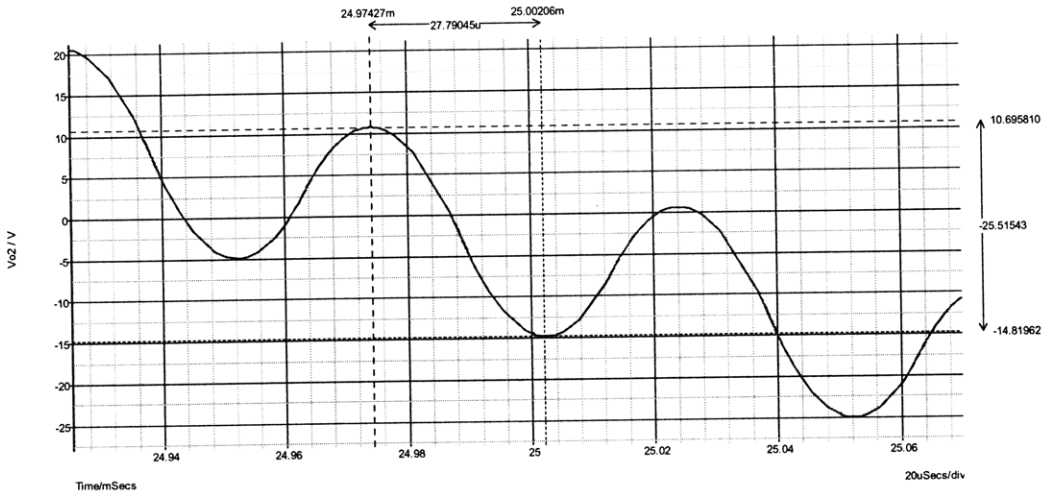


Figure 4-27: Output ripple at zero crossing

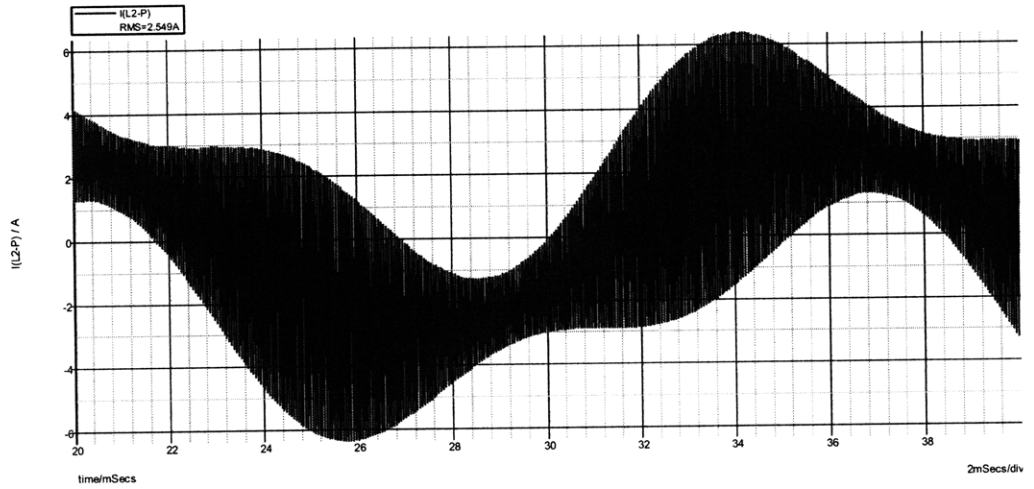


Figure 4-28: Inductor current over 1 AC cycle

These input parameters are entered into an inductor design MATLAB script (Figure 4-29) [appendix 8.4]. After the first run of the script, the ideal geometrical constant (K_g) value is displayed. In this case it should be at least 1.85 cm^5 (Figure 4-30). Using a table of modern ferrite (MN67 in this case) core types versus their geometrical constants [9], the EE60 type E-core with a K_g of 1.38 cm^5 is chosen. Although K_g should be greater than or equal to 1.85 cm^5, the next greater size is proportionally too large (5.06 cm^5).

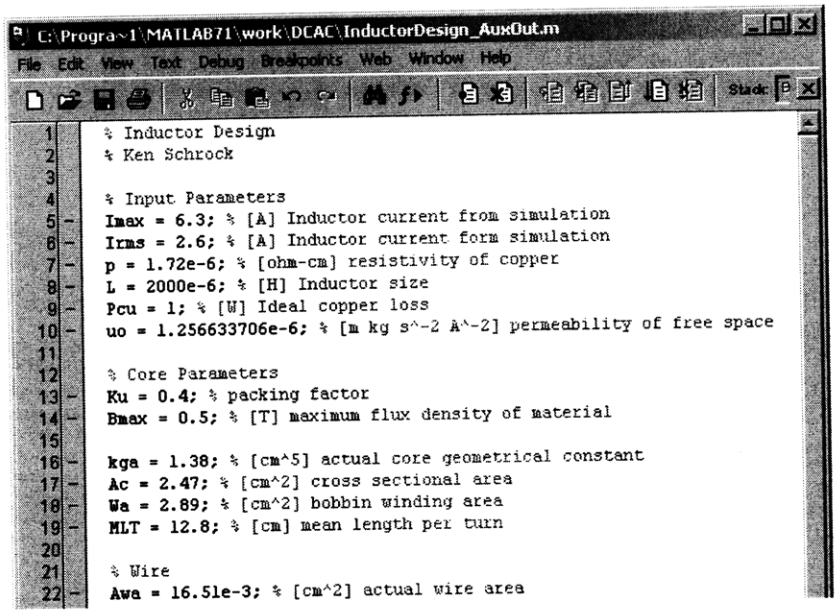


Figure 4-29: Inductor design MATLAB script

Back in the MATLAB script, the new core parameters are entered from the design table: kga, Ac, Wa, and MLT. After running the script again, the ideal wire size can be seen. The wire area can then be chosen [9] and the script is run a third and final time. The last line of the output is checked to see that the inductor meets the ideal power specification. The output also includes the number of turns required.

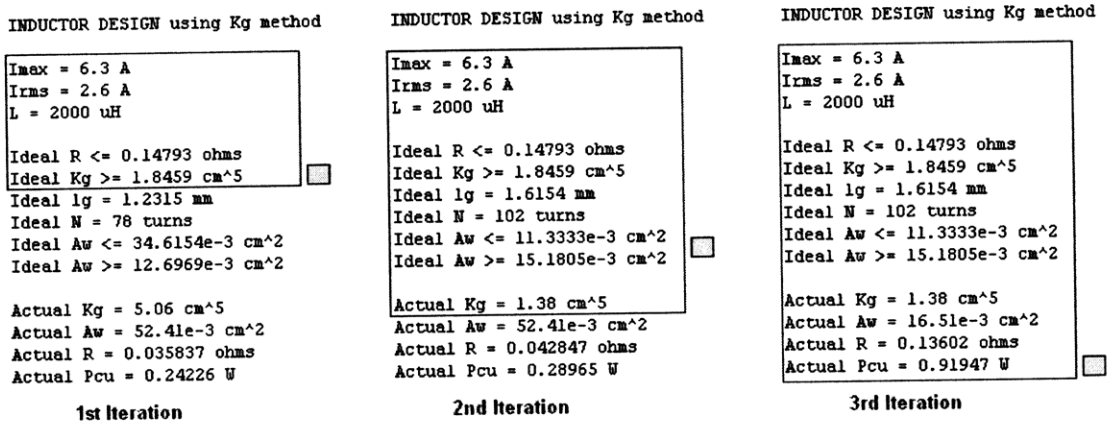


Figure 4-30: InductorDesign MATLAB output

4.2.1.2 Results

The following table gives the results of the inductor design optimization. Each inductor core was MN67 material and was designed for 1 watt of power dissipation.

Inductor	L (uH)	I_{max} (A)	I_{rms} (A)	Core Type	AWG	N turns	L_{gap} (mm)
AC output	2000	6.3	2.6	EE60	15	102	1.62
DC-to-DC output	500	2.0	1.4	EE19	26	87	.437
Buck output	500	2.5	2.0	EE30	26	23	.144

Figure 4-31: Table of inductor design results

4.2.2 Transformer Design

Similar to the inductor design algorithm in the previous section, there are transformer optimization processes. One method was developed by Hurley, et al [11]. The principle of this method is to find the optimal flux density at which to operate in order to minimize the combination of copper losses (higher at low flux density) and core losses (higher at high flux density) (Figure 4-32).

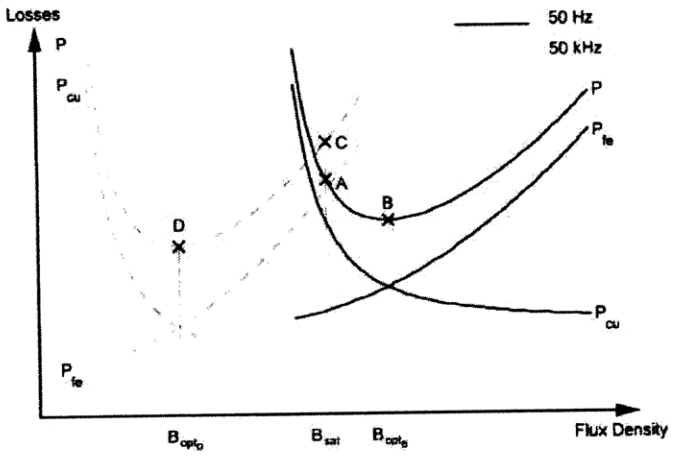


Figure 4-32: Transformer losses vs. flux density [11]

The following section will go through the design of the DC-to-DC stage's transformer.

4.2.2.1 Process

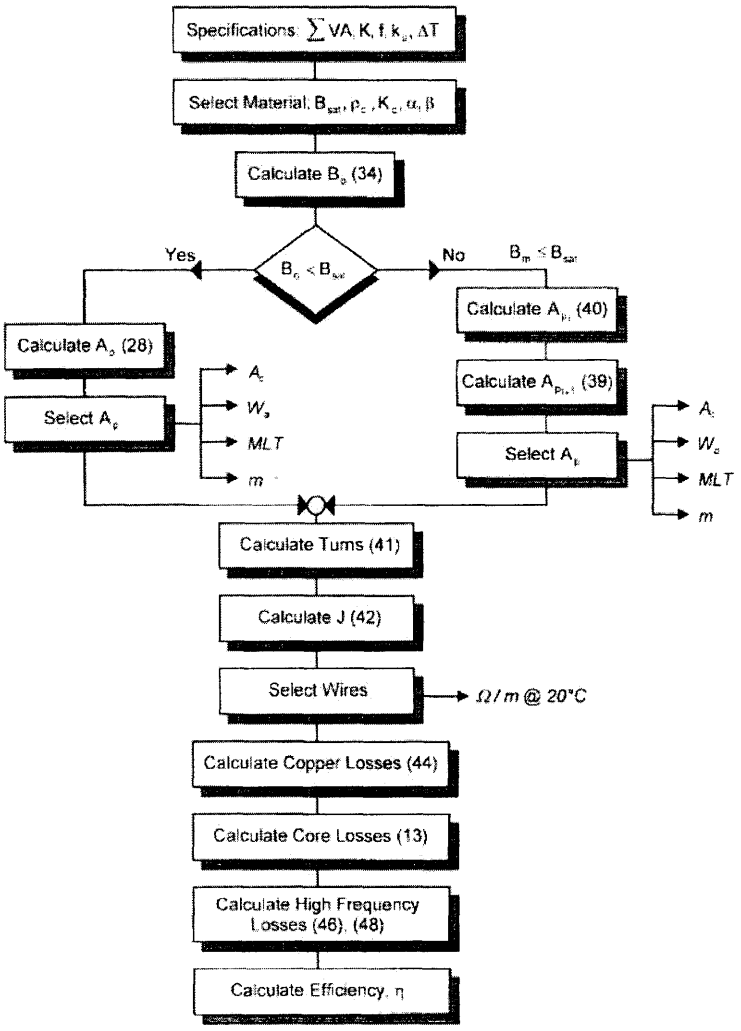


Figure 4-33: Transformer optimization process [11]

The transformer specifications and turns ratio are needed to start the process. The DC-DC stage of the converter has the following specifications:

- Maximum input voltage: 400 V
- Maximum output voltage: 700 V
- Maximum power: 700 W
- Switching frequency: 20 kHz

- Ambient temperature T_A: 175 °C
- Temperature rise, ΔT: 25 °C
- Efficiency, η: 95 %

With 95% efficiency, a transformer turns ratio of 1:1.9 can be used to ensure that the maximum output voltage is reachable.

The derivations for each formula in the process directly follow what was done in Hurley's two papers [10], [11]. The first step was entering the converter requirements into a MATLAB script [appendix 8.5] which was used to iterate the design process (Figure 4-34).

```
% Transformer Optimization
% Ken Schrock
% Single core specification

% Converter Parameters
Vi = 400; % Input Voltage
Vo = 700; % Output Voltage
Io = 1; % Output Current
eta = 0.95; % Efficiency
f = 20e3; % Switching frequency
T = 25; % Temperature rise (C)
Ta = 175; % Ambient temperature (C)

turnsratio = 1.9; % 1:turnsratio
diodedrop = 1.0; % volts
```

Figure 4-34: Core optimization: converter parameters

A custom E-core was designed out of MN67 material from Ceramic Magnetics (Figure 4-35). Five material parameters are needed in the optimization algorithm, but the data sheet only gave the saturation flux density of 2500 G. A mass density was assumed since most ferrites have a density of around 4800 kg-m^{-3}.

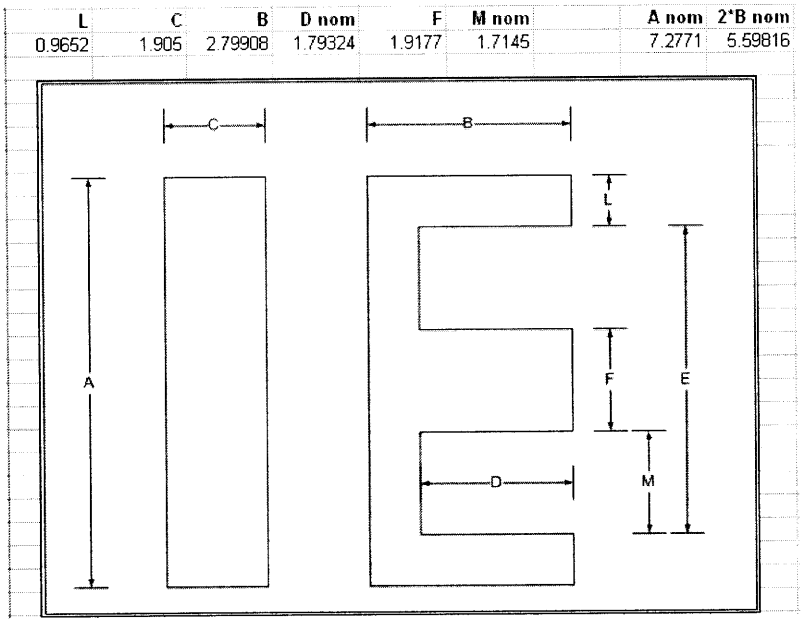


Figure 4-35: Original transformer E-core (units in cm)

Alpha, beta, and Kc were not provided, but power loss curves were given. The following equation holds:

$$P_{fe}[W \cdot m^{-3}] = \rho_m K_C f^{\alpha} B_m^{\beta} = k f^{\alpha} B_m^{\beta}$$

Using this, the values for alpha, beta, and Kc can be found from the power loss graph in the data sheet. Another MATLAB script [appendix 8.6] was used to find these numbers by performing an iterative least-mean-square error calculation (Figure 4-36). Once k was known, Kc could be computed since the density of the core was known. Kc = 3.96×10^{-4}. These material parameters, along with core dimensions, were entered into the script (Figure 4-37).

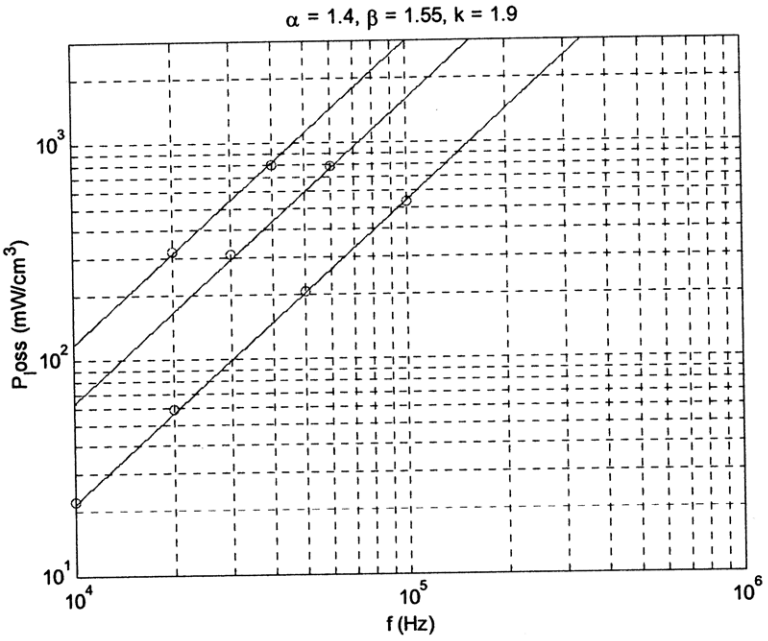


Figure 4-36: MN67 parameter calculation using MATLAB

```
% Magnetic Material
Bsat = 2500; % saturation flux density
alpha = 1.4;
beta = 1.54;
Kc = 3.91e-4;
pm = 4800; % core density (kg/m^3)

% Core Parameters (cm)
Dc = 1.79324;
L = .9652;
M = 1.7145;
C = 1.905;
B = 2.79908;
F = 1.9177;

Wa = Dc*M;
Ac = C*F;
Lc = 13.68827;
Vc = Lc*Ac;
Ap = Wa*Ac;
```

Figure 4-37: Core optimization: magnetic and core parameters

Running the script gives the wire sizes that need to be used (Figure 4-38 a), giving both the area and the diameter. An appropriate gauge can be selected from a table [9], [19]. In this case, #16 was chosen for the primary (d = 1.29 mm) and #21 for the secondary (d = .723 mm). These values were entered into the script (Figure 4-39), which was re-run, giving the output in Figure 4-38 b.

```
>>
TRANSFORMER OPTIMIZATION

Optimal Ap = 42.6448 cm^4
Actual  Ap = 11.2319 cm^4
Bo = 782.5327 Gauss
Bm = 971.7695 Gauss
Np = 129; Ns = 245; (Nmin = 90)
Optimal Aw, primary = 1.3794 mm^2
Optimal Aw, secondary = 0.4973 mm^2
Optimal Dw, primary = 1.3252 mm
Optimal Dw, secondary = 0.79573 mm
Actual Aw, primary = 0.41055 mm^2
Actual Aw, secondary = 0.41055 mm^2
Actual Dw, primary = 0.723 mm
Actual Dw, secondary = 0.723 mm
Bo2 = 1609.3486 Gauss
A = 7.2771 cm
2B = 5.5982 cm

Total Power Loss = 7.1127 W
Efficiency: 98.9955%
```

```
>>
TRANSFORMER OPTIMIZATION

Optimal Ap = 42.6448 cm^4
Actual  Ap = 11.2319 cm^4
Bo = 782.5327 Gauss
Bm = 971.7695 Gauss
Np = 129; Ns = 245; (Nmin = 90)
Optimal Aw, primary = 1.3794 mm^2
Optimal Aw, secondary = 0.4973 mm^2
Optimal Dw, primary = 1.3252 mm
Optimal Dw, secondary = 0.79573 mm
Actual Aw, primary = 1.307 mm^2
Actual Aw, secondary = 0.41055 mm^2
Actual Dw, primary = 1.29 mm
Actual Dw, secondary = 0.723 mm
Bo2 = 1609.3486 Gauss
A = 7.2771 cm
2B = 5.5982 cm

Total Power Loss = 5.1706 W
Efficiency: 99.2678%
```

Figure 4-38: Optimization MATLAB output: (a) first iteration, (b) second iteration

```
38
39    % Wire
40    % Primary winding
41 -  Dwp = .723; % mm
42 -  AwpW = pi*(Dwp/10/2)^2;
43 -  RdcpW = 1.72e-8/(AwpW/100^2)/100; % Resistance of wire
44
45    % Secondary winding
46 -  Dws = .723; % mm
47 -  AwsW = pi*(Dws/10/2)^2;
48 -  RdcsW = 1.72e-8/(AwsW/100^2)/100; % Resistance of wire
```

Figure 4-39: Core optimization: wire parameters

The calculated efficiency of this transformer was very high (99.2%). However, there are several important considerations. First, the efficiency is calculated based on the assumption that the transformer is operating at its optimal flux density. As the converter input and output change, this operating point will change. Also, due to the constraint of the fixed core size, Bo—the optimum operating flux density—and Bo2—the re-calculated operating point—were actually not close. Because of this, the efficiency will be lower than the calculated value.

Another consideration to note is the minimum number of turns. This is calculated and displayed next to the number of primary and secondary turns. It is important to have at least this number of turns or the transformer may saturate [12].

Finally, this program does not compute whether the windings will fit into the core window. This must be checked before a core selection is finalized. Smaller wire can be used at the cost of more copper losses.

Another approach is to design the transformer core to meet the desired flux operating point. Ap was used as a independent variable, which is the product of the window area (Wa) and area of the core (Ac) to ensure the transformer operates at the correct point.

A MATLAB script was written that finds possible core sizes [appendix 8.7]. It uses the same optimization procedure as described above. The same converter parameters are specified, as well as the core properties. However, there are additional constraints that are used when finding the optimum core.

Nmax sets the maximum allowable turns to avoid unrealistically high numbers. Cmin, Cmax, Amin, Amax, B2min, and B2max are the allowable size ranges of the core (depth, height, and width). ApTol sets a tolerance range of allowable deviation from the optimal Ap—for example, a value of .65 will give all cores that meet the other requirements and are within +/- 65% of the optimum Ap.

The parameter n sets the number of sizes within each dimension to try. If n = 20, 20^3 or 8000 cores will be tried. The additional core dimensions are computed in even ratios. For example, L = C and F = 2L, using the naming conventions shown in Figure 4-35. Each core is run through the optimization process, and it is only kept as a possibility if it is within all of the allowances and tolerances. At the end of the computation, a list is generated in the MATLAB window (Figure 4-40).

TRANSFORMER OPTIMIZATION

Index	Bo err	Efficiency	Turns	C (cm)	A (cm)	2B (cm)	Dwire (mm)
1.0000	40.8214	99.1434	186.0000	1.7105	12.0000	6.0000	1.1827
2.0000	43.6692	99.1496	184.0000	1.7105	12.0000	5.7632	1.1805
3.0000	43.6692	99.1496	184.0000	1.7105	11.5263	6.0000	1.1805
4.0000	46.5950	99.1541	183.0000	1.7105	11.5263	5.7632	1.1783
5.0000	46.7204	99.1541	183.0000	1.7105	12.0000	5.5263	1.1787
6.0000	46.7204	99.1541	183.0000	1.7105	11.0526	6.0000	1.1787
7.0000	49.7301	99.1615	181.0000	1.7105	11.5263	5.5263	1.1766
8.0000	49.7301	99.1615	181.0000	1.7105	11.0526	5.7632	1.1766
9.0000	50.0029	99.1615	181.0000	1.7105	12.0000	5.2895	1.1775
10.0000	50.0029	99.1615	181.0000	1.7105	10.5789	6.0000	1.1775
11.0000	52.9557	99.1693	179.0000	1.7105	11.0526	5.5263	1.1750
12.0000	53.1034	99.1693	179.0000	1.7105	11.5263	5.2895	1.1755
13.0000	53.1034	99.1693	179.0000	1.7105	10.5789	5.7632	1.1755
14.0000	53.5507	99.1694	179.0000	1.7105	12.0000	5.0526	1.1771
15.0000	53.5507	99.1694	179.0000	1.7105	10.1053	6.0000	1.1771
16.0000	56.4267	99.1774	177.0000	1.7105	11.0526	5.2895	1.1741
17.0000	56.4267	99.1774	177.0000	1.7105	10.5789	5.5263	1.1741
18.0000	56.7497	99.1775	177.0000	1.7105	11.5263	5.0526	1.1753
19.0000	56.7497	99.1775	177.0000	1.7105	10.1053	5.7632	1.1753
20.0000	57.4056	99.1779	177.0000	1.7105	12.0000	4.8158	1.1778
21.0000	57.4056	99.1779	177.0000	1.7105	9.6316	6.0000	1.1778
22.0000	60.0036	99.1831	176.0000	1.7105	10.5789	5.2895	1.1733
23.0000	60.1793	99.1852	175.0000	1.7105	11.0526	5.0526	1.1740
24.0000	60.1793	99.1852	175.0000	1.7105	10.1053	5.5263	1.1740
25.0000	60.7121	99.1856	175.0000	1.7105	11.5263	4.8158	1.1762
26.0000	60.7121	99.1856	175.0000	1.7105	9.6316	5.7632	1.1762
27.0000	61.6202	99.1891	174.0000	1.7105	12.0000	4.5789	1.1801
28.0000	61.6202	99.1891	174.0000	1.7105	9.1579	6.0000	1.1801
29.0000	63.8712	99.1913	174.0000	1.7105	10.5789	5.0526	1.1734
30.0000	63.8712	99.1913	174.0000	1.7105	10.1053	5.2895	1.1734
31.0000	64.2577	99.1944	173.0000	1.7105	11.0526	4.8158	1.1751
32.0000	64.2577	99.1944	173.0000	1.7105	9.6316	5.5263	1.1751
33.0000	65.0447	99.1954	173.0000	1.7105	11.5263	4.5789	1.1787
34.0000	65.0447	99.1954	173.0000	1.7105	9.1579	5.7632	1.1787

| Index | Bo err | Efficiency | Turns | C (cm) | A (cm) | 2B (cm) | Dwire (mm) |

Cores tried: 8000
Within range: 34

Figure 4-40: Possible cores output in MATLAB

The output is sorted from lowest to highest error in the flux operating point, with the assumption that lower operating point error implies a closer match to predicted efficiency. In order to calculate the turns, wire sizes, etc, the core parameters of the desired selection needed to be known. A custom MATLAB function [appendix 8.8] was used to find these parameters from hidden data produced during the constrained core selection script. An example is below.

```
>> CoreData(results(1,:));

Results Index: 1
Efficiency: 99.1434%
Turns: 186
Duty: 0.92105

D:  2.1447 cm
L:  0.85526 cm
M:  4.2895 cm
C:  1.7105 cm
A:  12 cm
2B: 6 cm
Ap: 26.9177 cm^4
Ac: 2.9259 cm^2
Wa: 9.1998 cm^2
Vc: 60.2119 cm^3
Bo: 0.081798 Tesla
Dwire,p: 1.1827 mm
Dwire,s: 0.70965 mm
Pfe:  2.6669 W
Pcup: 1.4722 W
Pcus: 1.9265 W
```

Figure 4-41: Output of CoreData in MATLAB

The function can be useful to quickly evaluate several core possibilities before choosing a suitable one to optimize. These numbers can then be entered back into the optimization script to calculate the number of turns and to save the sizes and results for future use.

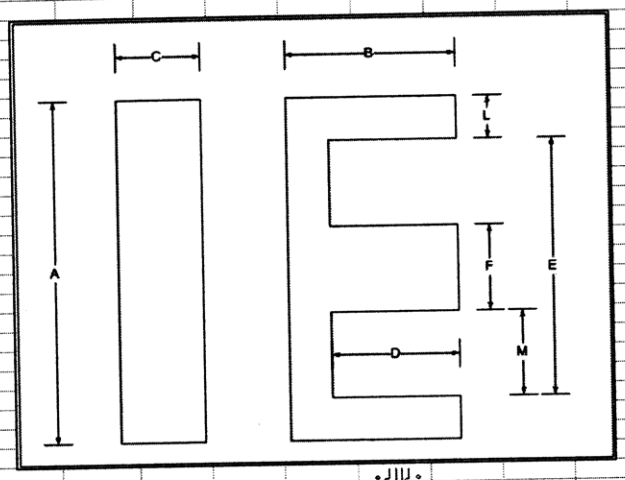
4.2.2.2 Results

Due to the size constraints of the final design, a true optimized core could not be found. However, a core that is roughly twice the size of the original core—closer to the optimal size—was used.

Using this optimization method, two transformers were designed: one for the existing E-core and one for the newer, larger, more optimal core. The wire sizes were reduced in order to fit into the window area of each transformer, so copper losses will be slightly higher than calculated. The winding and core size data can be seen in Figure 4-42.

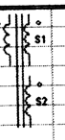
Core 1: two bobbins — Units in cm

L	C	B	D nom	F	M nom	A nom	2*B nom
0.9652	1.905	2.79908	1.79324	1.9177	1.7145	7.2771	5.59816



Bobbin 1:	Windings	Turns	Gauge*
Primary	1	150	21
Secondary	2	180	21

* If windings won't fit, try AWG 22

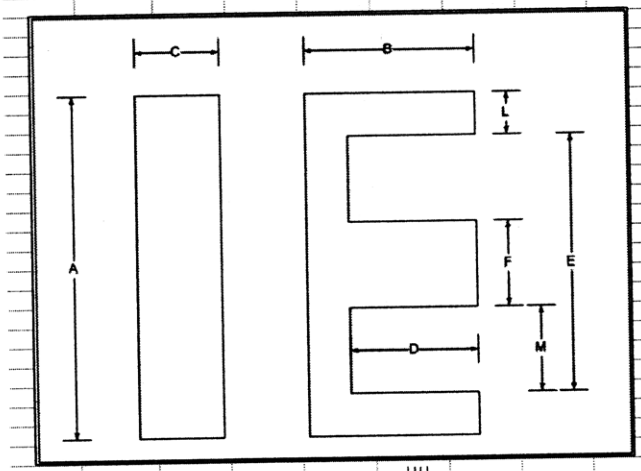


Bobbin 2:	Windings	Turns	Gauge*
Primary	1	69	16
Secondary	1	221	19

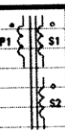
* If windings won't fit, try AWG 17/20, or 18/20

Core 2: two bobbins — Units in cm

L	C	B	D nom	F	M nom	A nom	2*B nom
0.85	1.7	2.99	2.14	1.7	4.3	12	5.98



Bobbin 3:	Windings	Turns	Gauge*
Primary	1	270	21
Secondary	2	324	21



Bobbin 4:	Windings	Turns	Gauge*
Primary	1	101	16
Secondary	1	323	20

Figure 4-42: Final core and winding data

5 Future Work

Much of the design work for the three-level buck converter was completed, and many problems have been discovered and fixed. However, a few issues remain.

5.1 Noise

It is common for power electronic circuits to produce and be susceptible to noise. There may be several voltages throughout the circuit referenced to different levels, making proper grounding difficult to achieve. Another problem is electromagnetic interference (EMI). Power converters switch relatively large amounts of current, which causes electromagnetic radiation. These EM waves can be picked up in loops of wire in other parts of the circuit, as shown in Figure 5-1.

Figure 5-1: V_{out} (top), V_{out} DSP input (middle), DSP gate signal output (bottom). [ch. 1: 100 V/div, ch. 2: 10 V/div, ch. 3: 5 V/div, 20 µs/div]

Noise had several effects on the three-level buck prototype. Since the noise spikes that occurred during switching (Figure 5-1 and Figure 5-3) increased as the input voltage

increased, EMI noise disrupted the USB line through which VisSim and the DSP communicated when input voltages were above roughly 50 volts. This problem was originally dealt with by including a potentiometer to vary the duty cycle and reference voltage rather than using a computer. Software filters were also added to help with noise, and are discussed in section 3.3.1.

A larger EMI problem was found in the MOSFET gate drive signals. At high input voltages, EMI would trigger the FETs, allowing very high current shoot-through for a small period of time (Figure 5-2). Small inductors (500 uH) allowed larger current-spikes; some reaching 40 amps. This shoot-through also caused the floating capacitor to become unbalanced—another problem that is discussed in section 5.2.

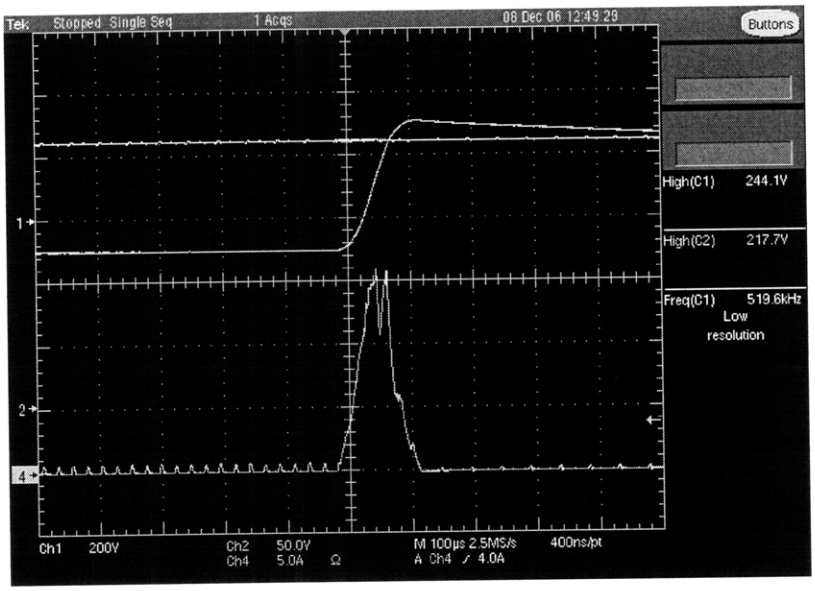


Figure 5-2: Capacitor voltage (middle) and inductor current spike (bottom) with L = 500 uH and Vin = 400 V. [ch. 2: 50 V/div, ch. 4: 5 A/div, 100 µs/div]

Noise also had a diverse effect on the control system. If there were a noise spike at the output voltage measurement due to switching, the compensator would interpret this as an increase in output voltage, and it would decrease the duty cycle, thus lowering the output voltage.

Figure 5-3: Noise caused by switching: V_{out} DSP input (top) and V_{ds} of each FET. [top: 2 V/div, ch. 1,3: 20 V/div, 20 µs/div]

If the compensator's bandwidth (gain) were high enough—10 or 100 times the frequency of the noise—then the converter could respond more quickly than the noise was occurring and the converter would correctly adjust itself. However, the converter is not stable at such high bandwidths (Figure 5-4 a).

At slightly lower loop gains, the repeated noise spikes caused lower frequency oscillations to occur. The compensator would repeatedly lower the output voltage to adjust for a voltage spike, and then raise it when it measured the lower output voltage (Figure 5-4 b).

To avoid responding to these noise spikes, a very low gain is required, which yields a low bandwidth. If the controller responds slowly enough, the noise will be ignored and only the steady-state value will be compensated (Figure 5-4 c).

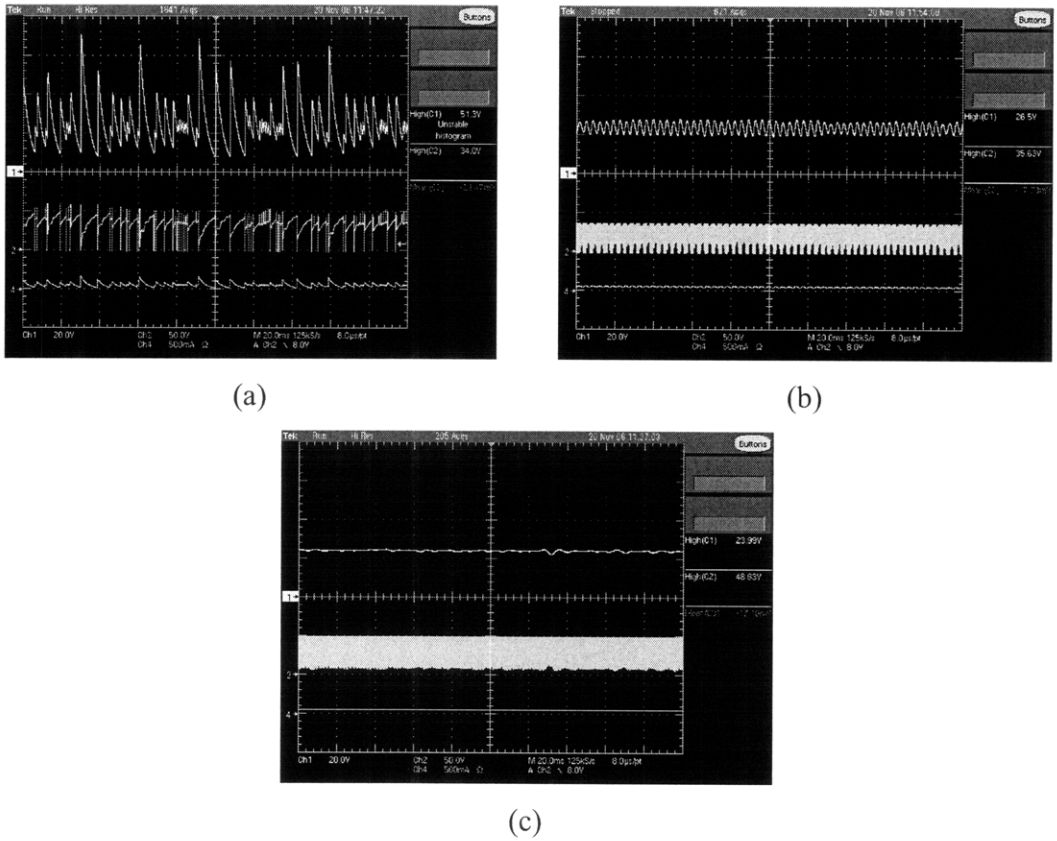


Figure 5-4: Converter output in the presence of noise: high gain (a); medium gain (b); low gain (c). Top trace: V_{out}; middle trace: FET voltage; bottom trace: inductor current. [ch. 1: 20 V/div, ch. 2: 50 V/div, ch. 3: 500 mA/div, 20 ms/div]

Reducing noise in the converter will have positive effects on performance. Prototype testing will be easier with the full features of VisSim if the computer connection does not get reset by noise. More importantly, shoot-through can be avoided and the controller gain can be increased to provide better tracking and dynamic performance.

Much of the noise is due to the layout of the prototype. If care is put into the design of a printed circuit board (PCB) prototype, including proper ground planes, physical isolation of high power and low power circuitry, and avoiding wire loops, many noise issues can be greatly reduced.

5.2 Balancing the Capacitor

The floating capacitor is the key component in multi-level converters. If it does not remain balanced at half of the input voltage, the voltage seen by some devices will be too high, causing system failure. In theory, the capacitor will stay perfectly balanced, regardless of load, as long as the duty cycles for each FET are identical (Figure 5-5).

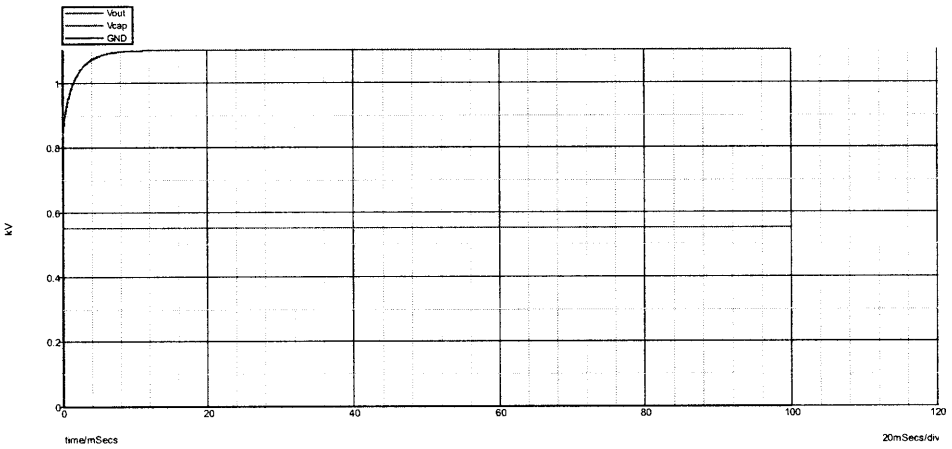


Figure 5-5: Floating capacitor voltage with no load and $D_1 = D_2 = 70\%$

This worked in practice to a certain degree. The DSP ran at a high enough frequency to provide good resolution so the gate drive signals were approximately equal. Like in the theoretical case, if one duty cycle was changed slightly, the capacitor voltage would rise or fall to a new steady-state value as seen in Figure 5-6.

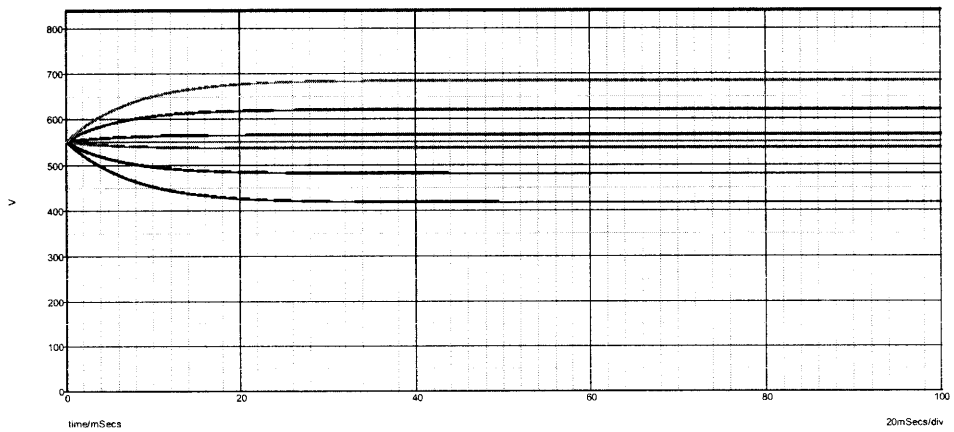


Figure 5-6: Capacitor voltage with one FET duty cycle change ≤ +/- 10%

However, with no load, the capacitor voltage drifted substantially. The power supply's output impedance is in series with the top and bottom switch. Along with slight component differences, these form an unbalanced voltage divider which charges the capacitor to a different steady state value (Figure 5-7). Placing small (20 ohm) resistors in parallel with each device creates a well-balanced divider, since the large open-state resistance values of each device are negligible. This is not a valid solution, however, since power dissipation would be very high in these resistors.

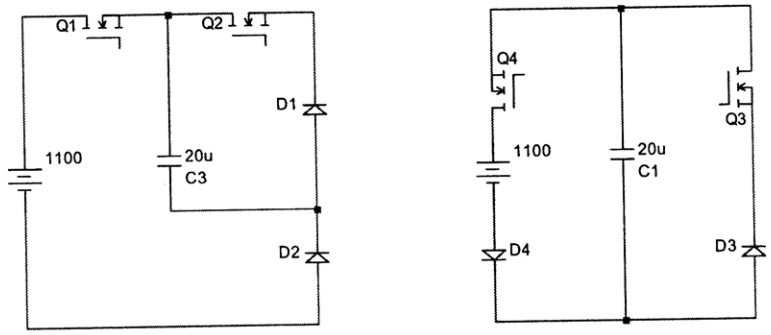


Figure 5-7: The three-level buck; with components rearranged to show unbalanced divider

500 kilo-ohm resistors were placed in parallel with each device. This yielded a steady-state no-load capacitor voltage of approximately 70% of the input voltage (Figure 5-8). The resistors dissipated at most 0.6 watts at full input voltage, and the capacitor voltage drifted to 770 volts: still within the MOSFET breakdown limits.

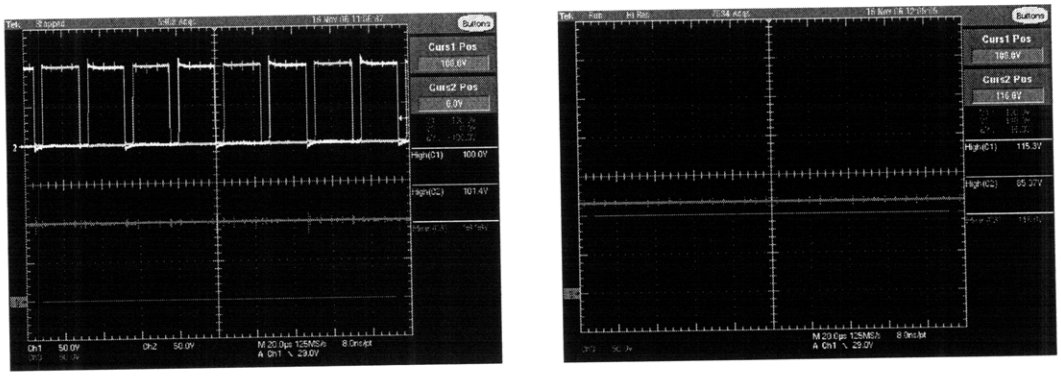


Figure 5-8: Capacitor voltage (ch. 3) with load (left) and without load (right). [50 V/div, 20 µs/div]

Although the parallel resistor solution is acceptable for prototype testing, a final design should not rely on the individual device characteristics and passive balancing. Active balancing can be achieved by measuring the input voltage and the capacitor voltage. An integral controller can be used with these measurements to slowly add to or subtract from one of the duty-cycle commands to ensure that the capacitor remains balanced (Figure 5-9).

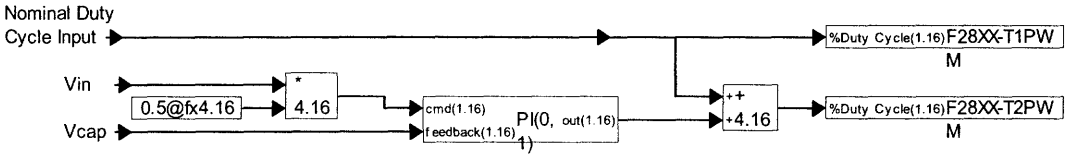


Figure 5-9: Active capacitor balancing implementation

It was also found that if a single FET was turned on and off slowly (1 Hz), the capacitor would remain balanced. The voltage drift occurred over roughly 30 seconds since the RC time constant is very high with no load. Turning on and off a FET periodically discharges the FET's parasitic capacitance, providing enough current to operate the converter for a brief moment. This is enough to re-balance the capacitor voltage. This low frequency switching could easily be implemented in an active balancing control scheme.

The inductor value had an effect on how well-balanced the capacitor remained. With a small inductance (500 uH), the capacitor remained perfectly balanced in loaded operation, but with a large inductance (20 mH), the capacitor exhibited abnormal behavior. Sometimes it was perfectly balanced; sometimes it was extremely unbalanced (5% or 10% of the input voltage); and sometimes it would snap back and forth as the input voltage is changed. Active balancing may resolve this issue as well.

Analysis, simulations, and testing have shown that the three-level buck converter is efficient and can provide the high-voltage power conversion required for the three-stage DC-to-AC converter. Once the issues discussed in this chapter are resolved, the three-level buck converter should be stable and reliable over a breadth of conditions.

6 Conclusion

Environmental requirements are often a limiting factor in engineering. In the case of very high temperatures, electrical components need to be selected carefully. The options for these components that remain may impose other design constraints, as was the case with the DC-to-AC converter discussed in this thesis. The high input voltage had to be split over multiple devices, calling for a multi-level converter.

Topology selection was discussed, and two stages of full-bridge inverters were chosen to provide isolation and the inverted output. A three-level buck converter was chosen over a neutral-point clamped (NPC) inverter because it is more controllable and the maximum voltage seen in the rest of the circuit is reduced. Simulations showed that the entire converter should be able to achieve efficiencies greater than ninety percent.

The three-level buck converter was analyzed in detail. A prototype was made and tested thoroughly. Results confirmed the simulation data: the multi-level buck converter is feasible as an efficient conditioning stage for the high input voltage the converter. A proper controller was designed and then tested both in simulation and in lab. Advanced control features such as hysteresis and bursting were looked at and shown to add crucial capabilities such as achieving a very low output with no load.

Optimization of the converter was examined, and two major areas of the converter were improved upon. First, switching losses in the full-bridge inverter stages were reduced by adding a capacitor and an anti-parallel diode around each switch. This was shown to be the most efficient solution compared to snubber circuits. Second, all magnetic components were optimized using known algorithms and MATLAB scripts. These optimizations will help maximize the converter's overall efficiency.

Finally, future work was discussed. Noise—especially EMI—needs to be reduced before finalizing the design of the three-level buck converter. Actively balancing the floating capacitor will also improve performance and provide more reliability.

The three-level buck converter, presented in this thesis as the front end to a DC-to-AC inverter, is an efficient, controllable, and feasible solution to reduce voltage stresses on switching devices and on other stages of a power circuit.

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7.1 Multi-Level Converters

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7.2 Magnetics

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7.4 Other Related References

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8 Appendix: Code

8.1 Compensator

```
function [params] = compensator(sys)
% Takes a transfer function of the form (as+b)/(cs^2+ds)
% and returns what R1, C1, R2, C2, and R3 should be
% for a compensator of the form: inverting integrator -->
% lead network --> inverting amplifier

[num den] = tfdata(sys);
num = num{1};
den = den{1};

a = num(2);
b = num(3);
c = den(1);
d = den(2);

R1 = 1000;
R3 = b;
R2 = a*d/c-b;
C2 = a/(R2*R3);
C1 = c/(R1*R2*R3*C2);

output = tf([C2*R2*R3 R3],[R1*R2*R3*C1*C2 C1*R1*(R2+R3) 0]);
params = [R1 C1 R2 C2 R3];

sys
output
disp(['R1 = ' num2str(R1)]);
disp(['C1 = ' num2str(C1)]);
disp(['R2 = ' num2str(R2)]);
disp(['C2 = ' num2str(C2)]);
disp(['R3 = ' num2str(R3)]);
```

8.2 MOSFET SPICE Model

```
* ------< SPICE Library APT17N80BC3.LIB Created by SPICEMOD 2.4.6
07/04 >------
**********
*SRC=17N80BC3;17N80BC3;MOSFETs N;Power >100V;APT 800V 17A 0.29ohm TO-
247
*SYM=POWMOSN
.SUBCKT 17N80BC3 10 20 30
*     TERMINALS:  D  G  S
M1   1  2  3  3  DMOS L=1U W=1U
RD  10  1  0.137
RS  40  3  8.25M
RG  20  2  8.82
CGS  2  3  2.2N
EGD 12  0  2  1  1
VFB 14  0  0
FFB  2  1  VFB  1
```

```
CGD 13 14  706P
R1  13  0  1
D1  12 13  DLIM
DDG 15 14  DCGD
R2  12 15  1
D2  15  0  DLIM
DSD  3 10  DSUB
LS  30 40  7.5N
.MODEL DMOS NMOS (LEVEL=1 LAMBDA=882U VTO=3 KP=8.24)
.MODEL DCGD D (CJO=706P VJ=0.6 M=0.68)
.MODEL DSUB D (IS=70.6N N=1.5 RS=26.5M BV=800 CJO=4.26N VJ=0.8 M=0.42
TT=550N)
.MODEL DLIM D (IS=100U)
.ENDS
**********
```

8.3 Compute Loss

```
function [P,W_tot,P_sw] = ComputeLoss(fname,varargin)
% ComputeLoss takes in a SIMetrix vector data file of the
% voltage and current of a switching device, then plots and
% computes the switching loss.  P(t), total power in 1 cycle, and the
total
% switching loss are returned.
%
% NOTE: fname is the location of input data file, which must be column
% vectors in the tab-delimited format with one line of header in the
% following order:    Time   Voltage  Current   and must contain only
data
% from the switching period.
% ex: 'D:\Documents\DCAC\Data\filename.txt';

% Ken Schrock
% Schlumberger
% 2006.06.29


%%% Script Variables

if nargin == 1
    f_sw = 20e3;   % switch frequency
else
    f_sw = varargin{1};
end


%%% Read and initialize data

data = dlmread(fname,'\t',1,0);
t = data(:,1);   % time vector
V = data(:,2);   % voltage vector
I = data(:,3);   % current vector


%%% Compute power loss
```

```
P = abs(V).*abs(I);   % power loss P(t)
W_tot = (P(2)-P(1))*(t(2)-t(1))/2;   % energy loss due to switching
for i = 2:length(t)
    W_tot = W_tot + (abs(P(i)-P(i-1))/2+min(P(i),P(i-1)))*(t(i)-t(i-
1));
end
P_sw = W_tot*f_sw;


%%% Plot and display results

figure(1);
clf;
subplot(2,1,1);
[AX,H1,H2] = plotyy(t,V,t,I);
title('Power Loss');
xlabel('time (s)');
set(get(AX(1),'Ylabel'),'String','Voltage (V)');
set(get(AX(2),'Ylabel'),'String','Current (A)');
set(AX(1),'XLim',[t(1) t(end)]);
set(AX(2),'XLim',[t(1) t(end)]);

subplot(2,1,2);
P(1) = 0;
P(end) = 0;
fill(t,P,'k');
set(gca,'XLim',[t(1) t(end)]);
xlabel('time (s)');
ylabel('Power (W)');

fprintf('\n');
fprintf('Total power loss at ');
fprintf([num2str(f_sw) ' Hz: ']);
fprintf([num2str(P_sw) ' Watts\n']);
fprintf('\n');
```

8.4 InductorDesign_AuxOut

```
% Inductor Design
% Ken Schrock

% Input Parameters
Imax = 6.3; % [A] Inductor current from simulation
Irms = 2.6; % [A] Inductor current form simulation
p = 1.72e-6; % [ohm-cm] resistivity of copper
L = 2000e-6; % [H] Inductor size
Pcu = 1; % [W] Ideal copper loss
uo = 1.256633706e-6; % [m kg s^-2 A^-2] permeability of free space

% Core Parameters
Ku = 0.4; % packing factor
Bmax = 0.5; % [T] maximum flux density of material

kga = 1.38; % [cm^5] actual core geometrical constant
Ac = 2.47; % [cm^2] cross sectional area
Wa = 2.89; % [cm^2] bobbin winding area
```

```
MLT = 12.8; % [cm] mean length per turn

% Wire
Awa = 16.51e-3; % [cm^2] actual wire area

% Calculations
R = Pcu/Irms^2;
kg = p*L^2*Imax^2*1e8/(Bmax^2*R*Ku); % [cm^5] ideal core geometrical
constant
lg = uo*L*Imax^2*1e4/(Bmax^2*Ac); % [m] length of air gap
n = round(L*Imax*1e4/(Bmax*Ac)); % number of turns
Awmax = Ku*Wa/n; % [cm^2] maximum ideal wire area
Awmin = p*n*MLT/R; % [cm^2] minimum ideal wire area
Ra = p*n*MLT/Awa; % [ohms] actual winding resistance
Pcua = Irms^2*Ra; % [W] copper loss

% Output
fprintf('\n\n');
disp(['INDUCTOR DESIGN using Kg method']);
fprintf('\n');
disp(['Imax = ' num2str(Imax) ' A']);
disp(['Irms = ' num2str(Irms) ' A']);
disp(['L = ' num2str(L*1e6) ' uH']);
fprintf('\n');
disp(['Ideal R <= ' num2str(R) ' ohms']);
disp(['Ideal Kg >= ' num2str(kg) ' cm^5']);
disp(['Ideal lg = ' num2str(lg*1e3) ' mm']);
disp(['Ideal N = ' num2str(n) ' turns']);
disp(['Ideal Aw <= ' num2str(Awmax*1e3) 'e-3 cm^2']);
disp(['Ideal Aw >= ' num2str(Awmin*1e3) 'e-3 cm^2']);
fprintf('\n');
disp(['Actual Kg = ' num2str(kga) ' cm^5']);
disp(['Actual Aw = ' num2str(Awa*1e3) 'e-3 cm^2']);
disp(['Actual R = ' num2str(Ra) ' ohms']);
disp(['Actual Pcu = ' num2str(Pcua) ' W']);
fprintf('\n');
```

8.5 XfrmOptAux_NewCore

```
% Transformer Optimization
% Ken Schrock
% Single core specification

% Converter Parameters
Vi = 400; % Input Voltage
Vo = 700; % Output Voltage
Io = 1; % Output Current
eta = 0.95; % Efficiency
f = 20e3; % Switching frequency
T = 25; % Temperature rise (C)
Ta = 175; % Ambient temperature (C)

turnsratio = 1.9; % 1:turnsratio
diodedrop = 1.0; % volts

% Magnetic Material
```

```
Bsat = 2500; % saturation flux density
alpha = 1.4;
beta = 1.54;
Kc = 3.91e-4;
pm = 4800; % core density (kg/m^3)

% Core Parameters (cm)
Dc = 2.14;
L = .85;
M = 4.3;

C = 2*L;
F = 2*L;
B = Dc+L;

Wa = Dc*M;
Ac = 4*L^2;
Lc = 4*Dc+4*L+2*M;
Vc = Lc*Ac;
Ap = Wa*Ac;

% Wire
% Primary winding
AwpW = 20.82; % cm^2
RdcpW = 1.72e-8/(AwpW/100^2)/100; % Resistance of wire

% Secondary winding
AwsW = 20.82; % cm^2
RdcsW = 1.72e-8/(AwsW/100^2)/100; % Resistance of wire

% Conversions
Ap = Ap/100^4;
Ac = Ac/100^2;
Vc = Vc/100^3;
Wa = Wa/100^2;
AwpW = AwpW/100^2;
RdcpW = RdcpW*100;
AwsW = AwsW/100^2;
RdcsW = RdcsW*100;

% Computation
D = (Vo/turnsratio)/Vi;
Vp = sqrt(D)*Vi;
Po = (Vo+diodedrop)*Io;
kps = 1;
kpp = 1;
VAsum = Po/(eta*kpp)+Po/kps;
K = 4/sqrt(D);
Ku = 0.4;
Ko = 10*40/sqrt(1.72e-8*10*5.6)*sqrt(2*beta)/(2+beta);
Kt = sqrt(beta/(beta+2)*10*40/(1.72e-8*10));
Bo =
(Ko/Kt^(6/7)*Ku^(1/14)/sqrt(pm*Kc*f^alpha)*T^(4/7)*(K*f/VAsum)^(1/7))^(
1/(beta/2-1/7));
Ap_opt = (VAsum/(K*f*Bo*Kt))^(8/7)*1/(T*Ku)^(4/7)*100^4;
fprintf('\nTRANSFORMER OPTIMIZATION\n\n');
disp(['Optimal Ap = ' num2str(Ap_opt) ' cm^4']);
```

```
disp(['Actual  Ap = ' num2str(Ap*100^4) ' cm^4']);
disp(['Bo = ' num2str(Bo*1e4) ' Gauss']);
Bm = ((Ko/Kt)^2*T/(pm*Kc*f^alpha*Ap^.25))^(1/beta);
disp(['Bm = ' num2str(Bm*1e4) ' Gauss']);
Nmin = ceil(Vi*1/(2*f)/((2*(Bsat/1e4-Bm))*Ac));
Np = floor(Vp/(K*f*Bm*Ac));
Ns = round(turnsratio*Np);
disp(['Np = ' num2str(Np) '; Ns = ' num2str(Ns) '; (Nmin = '
num2str(Nmin) ')']);
MLT = pi*sqrt(C^2+F^2)/100;
Tmax = Ta + T;
pw = 1.72e-8*(1+.00393*(Tmax-20));
J = sqrt((400*sqrt(Ap)*T-pm*Vc*Kc*f^alpha*Bm^beta)/(pw*MLT*Ku*Wa));
Ip = Po/(eta*kpp*Vp);
Awp = Ip/J*100^2;
disp(['Optimal Aw, primary = ' num2str(Awp*100) ' mm^2']);
Is = Io/2*sqrt(1+D);
Aws = Is/J*100^2;
disp(['Optimal Aw, secondary = ' num2str(Aws*100) ' mm^2']);
disp(['Optimal Dw, primary = ' num2str(2*sqrt(Awp/pi)*10) ' mm']);
disp(['Optimal Dw, secondary = ' num2str(2*sqrt(Aws/pi)*10) ' mm']);
Awp = AwpW*100^2;
Aws = AwsW*100^2;
Rdcp = RdcpW;
Rdcs = RdcsW;
disp(['Actual Aw, primary = ' num2str(Awp*10^2) ' mm^2']);
disp(['Actual Aw, secondary = ' num2str(Aws*10^2) ' mm^2']);
disp(['Actual Dw, primary = ' num2str(2*sqrt(Awp/pi)*10) ' mm']);
disp(['Actual Dw, secondary = ' num2str(2*sqrt(Aws/pi)*10) ' mm']);
sigma = 66/sqrt(f);
rop = sqrt(Awp/pi)*10;
if rop/sigma <= 1.7
    Ksp = 1+(rop/sigma)^4/(48+0.8*(rop/sigma)^4);
else
    Ksp = .25+0.5*(rop/sigma)+3/32*(sigma/rop);
end;
ros = sqrt(Aws/pi)*10;
if ros/sigma <= 1.7
    Kss = 1+(ros/sigma)^4/(48+0.8*(ros/sigma)^4);
else
    Kss = .25+0.5*(ros/sigma)+3/32*(sigma/ros);
end;
Racp = Ksp*Rdcp;
Racs = Kss*Rdcs;
Rp = MLT*Np*Racp*(1+.00393*(Tmax-20));
Pcup = Rp*Ip^2;
Rs = MLT*Ns*Racs*(1+.00393*(Tmax-20));
Pcus = Rs*Is^2*2;
Pfe = pm*Vc*Kc*f^alpha*Bm^beta;
Ploss = Pcup + Pcus + Pfe;
Bo2 = (VAsum^2*pw*MLT*Wa/(K^2*f^2*Ku*Ap^2*pm*Vc*Kc*f^alpha))^.25;
A = F+2*M+2*L;
B2 = 2*B;
disp(['Bo2 = ' num2str(Bo2*1e4) ' Gauss']);
disp(['A = ' num2str(A) ' cm']);
disp(['2B = ' num2str(B2) ' cm']);
fprintf('\n');
```

```
disp(['Total Power Loss = ' num2str(Ploss) ' W']);
eff = Po/(Po+Ploss)*100;
disp(['Efficiency: ' num2str(eff) '%']);
fprintf('\n');
```

8.6 AlphaBetaPlot2

```
% Plots the Power Loss graph for a given set of parameters
% Finds best alpha and beta

B = [1 2 3]/10;
f = logspace(4,6,1000);

x = [10 20 50  100 30  60  20  40]*1e3;
y = [22 59 205 530 310 780 320 800];

bestalpha = 0;
bestbeta = 0;
bestk = 0;
besterr = inf;

for alpha = 1.4:.1:1.6
    for beta = 1:.05:3
        for k = .1:.01:3
            P1 = k*x(1:4).^alpha*.1^beta;
            P2 = k*x(5:6).^alpha*.2^beta;
            P3 = k*x(7:8).^alpha*.3^beta;
            y2 = [P1 P2 P3]*1000/100^3;
            err = mean((y2-y).^2);

            if err < besterr
                disp(['alpha = ' num2str(alpha) '; beta = '
num2str(beta) '; k = ' num2str(k)]);
                bestalpha = alpha;
                bestbeta = beta;
                bestk = k;
                besterr = err;
            end
        end
    end
end

alpha = bestalpha;
beta = bestbeta;
k = bestk;
disp('done');

Pl = [];
for i = 1:length(B);
    Bi = B(i);
    Pl(i,:) = k*f.^alpha*Bi^beta*1000/100^3;
end

testx = logspace(log10(x(1)),log10(x(4)),10000);
testy = logspace(log10(y(1)),log10(y(4)),10000);
```

```
testx2 = logspace(log10(x(5)),log10(x(6)),10000);
testy2 = logspace(log10(y(5)),log10(y(6)),10000);

testx3 = logspace(log10(x(7)),log10(x(8)),10000);
testy3 = logspace(log10(y(7)),log10(y(8)),10000);

figure(1);
clf;
% loglog(testx,testy);
% hold on;
% loglog(testx2,testy2);
% loglog(testx3,testy3);
loglog(f,Pl(1,:));
hold on;
for i = 2:length(B);
    loglog(f,Pl(i,:));
end
loglog(x,y,'ro','markersize',5);
grid on;
axis([1e4 1e6 1e1 3000]);
xlabel('f (Hz)');
ylabel('P_loss (mW/cm^3)');
title(['\alpha = ' num2str(alpha) ', \beta = ' num2str(beta) ', k = '
num2str(k)]);
```

8.7 XfrmOptFitAPAux

```
% Transformer Optimization with Multiple Cores
% Ken Schrock
% Same as XfrmOpFitAp but for AC/Aux instead of AC/Main

% Converter Parameters
Vi = 400; % Input Voltage
Vo = 700; % Output Voltage
Io = 1; % Output Current
eta = 0.95; % Efficiency
f = 20e3; % Switching frequency
T = 25; % Temperature rise (C)
Ta = 175; % Ambient temperature (C)

turnsratio = 1.9;
diodedrop = 2.0; % volts
Nmax = 400;

% Magnetic Material
Bsat = 2500;
alpha = 1.4;
beta = 1.54;
Kc = 3.96e-4;
pm = 4800;

% Core Parameters
Cmin = 1; % cm
Cmax = 1.9; % cm
Amin = 6; % cm
Amax = 12; % cm
```

```
B2min = 2; % cm
B2max = 6; % cm
ApTol = .65;

n = 20;

% Computation
D = (Vo/turnsratio)/Vi;
Vp = sqrt(D)*Vi;
Po = (Vo+diodedrop)*Io;
kps = 1;
kpp = 1;
VAsum = Po/(eta*kpp)+Po/kps;
K = 4/sqrt(D);
Ku = 0.4;
Ko = 10*40/sqrt(1.72e-8*10*5.6)*sqrt(2*beta)/(2+beta);
Kt = sqrt(beta/(beta+2)*10*40/(1.72e-8*10));
Bo =
(Ko/Kt^(6/7)*Ku^(1/14)/sqrt(pm*Kc*f^alpha)*T^(4/7)*(K*f/VAsum)^(1/7))^(
1/(beta/2-1/7));
Ap_opt = (VAsum/(K*f*Bo*Kt))^(8/7)*1/(T*Ku)^(4/7)*100^4;
fprintf('\nTRANSFORMER OPTIMIZATION\n\n');

%%%
Di = linspace(Cmin/4,(B2max-Cmin)/2,n);
Li = linspace(Cmin/2,min(B2max/2-Cmin/4,Amax/4-Cmin/8),n);
Mi = linspace(Cmin/2,Amax/2-Cmin,n);
DLM = [];

for i=1:50
    fprintf('.');
end
fprintf('\n');
step = n^3/50;
prog = step;
for i = 1:n
    for j = 1:n
        for m = 1:n
            if (i-1)*n^2+(j-1)*n+m == round(prog);
                prog = prog+step;
                fprintf('|');
            end
            DLM(n^2*(i-1)+n*(j-1)+m,:) = [Di(i) Li(j) Mi(m)];
        end
    end
end

fprintf('\n');

Ci = 2*DLM(:,2);
Fi = 2*DLM(:,2);

Wai = DLM(:,1).*DLM(:,3);
Aci = 4*DLM(:,2).^2;
Lci = 4*DLM(:,1)+4*DLM(:,2)+2*DLM(:,3);
Vci = Lci.*Aci;
Api = Wai.*Aci;
```

```
%%%

results = [];
k = 1;
prog = step;
for i=1:length(DLM(:,1))
    if i == round(prog);
        prog = prog+step;
        fprintf('|');
    end
    Dc = DLM(i,1);
    L = DLM(i,2);
    M = DLM(i,3);
    C = Ci(i);
    F = Fi(i);
    Wa = Wai(i)./100^2;
    Ac = Aci(i)./100^2;
    Vc = Vci(i)./100^3;
    Ap = Api(i)./100^4;

if abs(Ap*100^4-Ap_opt)/Ap_opt < ApTol

Bm = ((Ko/Kt)^2*T/(pm*Kc*f^alpha*Ap^.25))^(1/beta);
Np = floor(Vp/(K*f*Bm*Ac));
Ns = round(turnsratio*Np);
MLT = pi*sqrt(C^2+F^2)/100;
Tmax = Ta + T;
pw = 1.72e-8*(1+.00393*(Tmax-20));
J = abs(sqrt((400*sqrt(Ap)*T-
pm*Vc*Kc*f^alpha*Bm^beta)/(pw*MLT*Ku*Wa)));
Ip = Po/(eta*kpp*Vp);
Awp = Ip/J*100^2;
Is = Io/2*sqrt(1+D);
Aws = Is/J*100^2;
Rdcp = 1.72e-8/(Awp/100^2);
Rdcs = 1.72e-8/(Aws/100^2);
sigma = 66/sqrt(f);
rop = sqrt(Awp/pi)*10;
if rop/sigma <= 1.7
    Ksp = 1+(rop/sigma)^4/(48+0.8*(rop/sigma)^4);
else
    Ksp = .25+0.5*(rop/sigma)+3/32*(sigma/rop);
end;
ros = sqrt(Aws/pi)*10;
if ros/sigma <= 1.7
    Kss = 1+(ros/sigma)^4/(48+0.8*(ros/sigma)^4);
else
    Kss = .25+0.5*(ros/sigma)+3/32*(sigma/ros);
end;
Racp = Ksp*Rdcp;
Racs = Kss*Rdcs;
Rp = MLT*Np*Racp*(1+.00393*(Tmax-20));
% Pcup = Rp*Ip^2*2;
Pcup = Rp*Ip^2;
Rs = MLT*Ns*Racs*(1+.00393*(Tmax-20));
Pcus = Rs*Is^2*2;
Pfe = pm*Vc*Kc*f^alpha*Bm^beta;
```

```
Ploss = Pcup + Pcus + Pfe;
eff = Po/(Po+Ploss)*100;

Bo2 = (VAsum^2*pw*MLT*Wa/(K^2*f^2*Ku*Ap^2*pm*Vc*Kc*f^alpha))^.25;
Nmin = ceil(Vi*1/(2*f)/((2*(Bsat/1e4-Bm))*Ac));
A = 2*M+4*L;
B2 = 2*(Dc+L);
WireAp = Np*(2*rop/10)^2;
WireAs = 2*Ns*(2*ros/10)^2;

if and(min([
        Np >= Nmin
        Np >= 4;
        Np <= Nmax
        Ns >= Nmin
        Ns >= 4;
        Ns <= Nmax
        A >= Amin
        A <= Amax
        B2 >= B2min
        B2 <= B2max
        C >= Cmin
        C <= Cmax
        Wa*1e4 >= WireAp+WireAs
        ]),1)
    results(k,:) = [(Bo2-Bo)/Bo*100 eff Np C A B2 max(2*rop, 2*ros) Dc
L M Ap Ac Wa Vc Bo 2*rop 2*ros D Pfe Pcup Pcus];
    k = k+1;
end
end
end
fprintf('\n\n');
if not(isempty(results))
    fprintf('\tIndex\t  Bo err   Efficiency  Turns\tC (cm)\t  A (cm)
2B (cm)\t  Dwire (mm)\n\n');
    results = [[1:1:size(results,1)]' sortrows(results,1)];
    disp(results(:,1:8));
    fprintf('\tIndex\t  Bo err   Efficiency  Turns\tC (cm)\t  A (cm)
2B (cm)\t  Dwire (mm)\n\n');
end
disp(['Cores tried:  ' num2str(step*50)]);
disp(['Within range: ' num2str(size(results,1))]);
fprintf('\n');
```

8.8 CoreData

```
function [] = CoreData(row);
% Takes a row from the results of XfrmOptTest.m
% And displays the relevant data for XfrmOpt.m

fprintf('\n');
disp(['Results Index: ' num2str(row(1))]);
disp(['Efficiency: ' num2str(row(3)) '%']);
disp(['Turns: ' num2str(row(4))]);
disp(['Duty: ' num2str(row(19))]);
fprintf('\n');
```

```
disp(['D:  ' num2str(row(9)) ' cm']);
disp(['L:  ' num2str(row(10)) ' cm']);
disp(['M:  ' num2str(row(11)) ' cm']);
disp(['C:  ' num2str(row(5)) ' cm']);
disp(['A:  ' num2str(row(6)) ' cm']);
disp(['2B: ' num2str(row(7)) ' cm']);
disp(['Ap: ' num2str(row(12)*100^4) ' cm^4']);
disp(['Ac: ' num2str(row(13)*100^2) ' cm^2']);
disp(['Wa: ' num2str(row(14)*100^2) ' cm^2']);
disp(['Vc: ' num2str(row(15)*100^3) ' cm^3']);
disp(['Bo: ' num2str(row(16)) ' Tesla']);
disp(['Dwire,p: ' num2str(row(17)) ' mm']);
disp(['Dwire,s: ' num2str(row(18)) ' mm']);
disp(['Pfe:  ' num2str(row(20)) ' W']);
disp(['Pcup: ' num2str(row(21)) ' W']);
disp(['Pcus: ' num2str(row(22)) ' W']);
fprintf('\n');
```