Linearity of Power AlGaAs/GaAs HBTs

by
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Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering
at the Massachusetts Institute of Technology

May 22, 1998

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Abstract

AlGaAs/GaAs HBTs are generating interest for their superior power performance in the 1-5 GHz frequency regime for applications such as wireless LANs and cellular telephones. Much of this interest stems from the fact that HBTs exhibit excellent linearity compared to other power devices. There has been little work done to understand and model the linearity of these devices. In this thesis the linearity properties of HBTs are addressed and an approach to developing an analytical model for predicting IMD3, the linearity figure of merit, is presented. The development is based on the two strongest sources of nonlinearity: the collector current and the base to emitter junction capacitance. The HP-Libra Harmonic Balance simulation environment based on the Gummel-Poon model was evaluated to be a good predictor of both one-tone and two-tone device performance. This simulation environment was then used to perform load and source pulls to optimize device operation. Simulations were also utilized to determine the sensitivity of IMD3 to various Gummel-Poon parameters at different biases. From the sensitivity analysis, it was found that the base to collector junction capacitance plays a significant part in the overall nonlinearity of the device at high collector current biases, whereas the base to emitter junction capacitance plays a more significant role at the low collector current biases.

Thesis Supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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I am indebted to my family, colleagues and friends for the successful completion of this project.

I would first like to thank my family for their continuos support and love throughout my life. My parents have always created an environment where education is priority number one, providing the guidance, care and resources for such pursuits and I am indeed grateful.

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Chapter 1 - Introduction

1.1 Motivation

AlGaAs/GaAs Heterostructure Bipolar Transistors (HBT) are attracting interest in high performance power amplifiers (PA) operating in the 1-5 GHz range for applications requiring many tightly packed channels such as cellular telephones, satellite communications, and wireless local area networks (LANs) [1.1, 1.2]. These devices are especially attractive because of their superior linearity properties, high gain, high power density and high efficiency [1.3, 1.4]. There are several performance figures of merit that a radio frequency (RF) power HBT PA must be designed for. These include the gain (G), power output (P_{out}), power added efficiency (PAE), and third-order intermodulation distortion (IMD3) which is a figure of merit that asses linearity. A high G is desired so that the PA can be constructed with a minimum number of stages to reduce the size, weight, and cost. A high PAE is necessary for long talk times on battery operated systems. P_{OUT} is in general a design parameter that is imposed by the system requirements. A low IMD3 is needed so that the signal spillover to adjacent channels is minimized. The IMD3 figure of merit relates directly to the linearity of the device, and the investigation of this figure of merit is the purpose of this thesis.

1.2 Figures of Merit

The P_{OUT} figure of merit is simply the output power dissipated at the load at the fundamental frequency. P_{OUT} is measured in watts or is normalized to 1 mW yielding units of dBm, that is:

$$P_{OUT_{(dBm)}} = 10\log_{10}\left(P_{OUT_{(mW)}}\right) \qquad \text{[Equation 1.1]}$$

In this thesis, the P_{OUT} shall be described in units of dBm.

G is the ratio of P_{OUT} to $P_{available}$, where $P_{available}$ is the available power at the source, that is, the input power at the fundamental frequency when the input impedance of the PA is conjugately matched to the source impedance. In this thesis, G is reported in units of dB defined as:

$$G_{(dBm)} = 10\log_{10}\left(\frac{P_{OUT_{(mW)}}}{P_{available_{(mW)}}}\right) = P_{OUT_{(dBm)}} - P_{available_{(dBm)}} \qquad \text{[Equation 1.2]}$$

PAE, which is reported as a percentage, is simply the ratio of (P_{OUT} – P_{IN}) to P_{DC}, where P_{DC} is the DC power input:

$$PAE = \frac{(P_{OUT} - P_{IN})}{P_{DC}} \approx \frac{P_{OUT}}{P_{DC}}\left(1 - 1/G\right) \qquad \text{[Equation 1.3]}$$

HBT PA with input and output load matching can exhibit G exceeding 15 dB, P_{OUT} of 30 dBm and PAE of 64% [1.5].

If a system is perfectly linear then the system will obey scaling and superposition. If an amplifier is perfectly linear then one can input two signals independently and the sum of those outputs will be identical to the output obtained when the two signals are input to the PA at the same time. A nonlinear system will not obey scaling and superposition and therefore a nonlinear PA will have a transfer function that will depend on all the signals on the input, making it difficult to predict what the output signal will be for a typical multi-tonal input. The linearity of a PA can be specified by several different figures of merit. Among these are the notch power ratio (NPR), adjacent channel power ratio (ACPR), third-order intermodulation-power intercept (IP3), and normalized third-order intermodulation distortion (IMD3).

In the NPR method, pink noise with a small bandwidth notched out is input to the PA. In a perfectly linear system, the output will have no amplitude at the frequencies that are notched out at the input, but in a real system, the notch will 'fill in' a bit. How much it fills in, is a measure of how linear the PA is. In the ACPR method, a complex spectrum is introduced to the input of the PA and it is seen how much of it shows up at an adjacent channel.

IP3 and IMD3 are both two-tone intermodulation methods where two different frequency sinusoidal signals which are representative of the frequencies in the bandwidth being amplified are input to the PA as shown in Figure 1.1. The input and output spectrum of a two-tone analysis are shown as Figure 1.2.

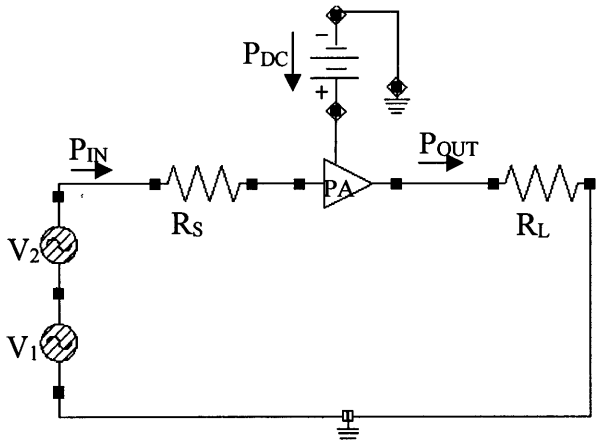


Figure 1.1: Set up for two tone analysis of HBT PA.

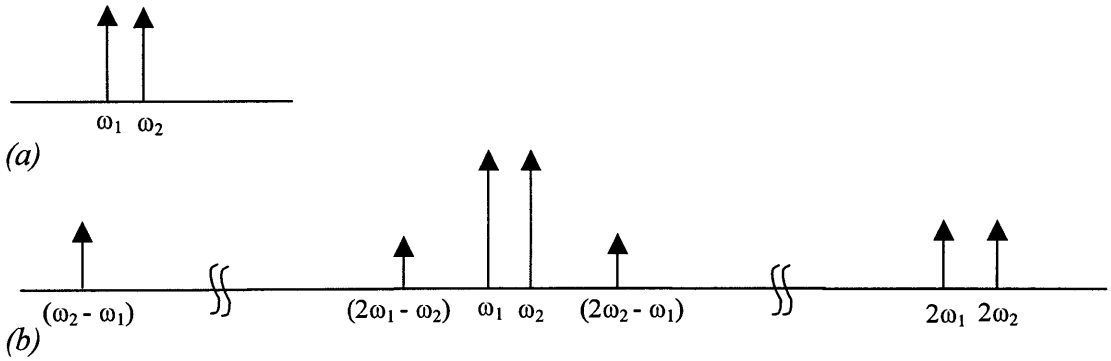


Figure 1.2: Input(a) and output(b) spectrum for two-tone analysis of HBT PA.

At the input, two tones of equal amplitude are presented to the PA. At the output, harmonics, as well as intermodulation (mixing) frequencies are produced as shown above. The input power in dBm where the third-order intermodulation power ($P_{OUT}(2\omega_1 - \omega_2)$) is equal to the fundamental power ($P_{OUT}(\omega_1)$) is the IP3 figure of merit [1.6]. The IMD3 figure of merit is simply the intermodulation power normalized by the fundamental power:

$$IMD3 = \frac{P_{OUT}(2\omega_1 - \omega_2)}{P_{OUT}(\omega_1)} \qquad \text{[Equation 1.4]}$$

This will be the figure of merit that will be used in this thesis as a measure of linearity.

When designing a PA, the trade-offs between these figures of merit must be considered. There is an important point called the 1-dB gain compression point. This is the P_{OUT} where G goes down by 1 dB from the small signal G. G compresses at this point because the output is sufficiently large so that there is clipping on the output due to the transistor

being pushed into cutoff or saturation. PAE is typically very high beyond the 1-dB G compression point, but the trade-off is that G is low and the IMD3 is high in that region. A common-emitter (CE) HBT PA with P_{OUT} of 23.8 dBm exhibits IMD3 of –21 dBc at the 1 dB gain compression point, but at a 1.5 dB back-off in P_{OUT} from the 1 dB G compression point, it exhibits a much improved IMD3 of –30 dBc [1.7].

Currently there is a poor understanding of linearity and methods of modeling the figures of merit relating to linearity. For the purpose of design, it is important to have an analytical model. The work in this thesis provides such a model.

1.3 HBTs

There has been interest in GaAs based bipolar transistors since the early days of silicon bipolar transistors. The general belief was that the high electron mobility and large bandgap of GaAs will result in superior devices which can operate at higher frequencies and higher junction temperatures. These hopes had been stiffled however by a lack of high purity, low defect starting material, inability to create low leakage diffused junctions, and inability to create low resistance ohmic contacts. The critical advancement for GaAs junction technology was the development of molecular beam epitaxy (MBE) which allowed the creation of high quality epitaxial layers on top of GaAs wafers and allowed the formation of heterojunctions. The concept of using a heterojunction to improve junction injection efficiency was first proposed by Shockley in 1948, but the application of this concept did not come to fruition until the advent of the MBE [1.8, 1.9].

HBTs are heterojunction devices. This means that the emitter and the base are composed of two different materials with different properties as shown in Figure 1.2.1. The emitter is made with AlGaAs, which has a larger bandgap than the base material GaAs. The base-collector junction is a homojunction for the devices in this study, but sometimes a large bandgap material is also used for the collector to reduce the offset voltage and charge storage during transistor saturation. The offset voltage may also be reduced by grading the emitter-base junction.

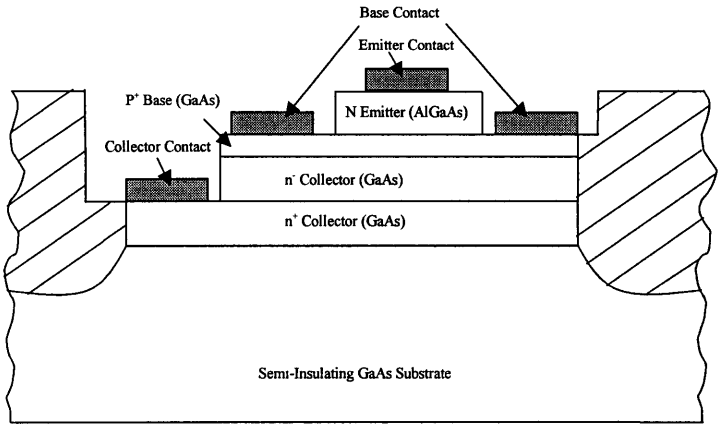


Figure 1.3: Typical Structure of an AlGaAs/GaAs HBT.

The presence of the emitter base heterojunction allows for several desirable properties. In a well designed homojunction transistor, the emitter is doped much more heavily than the base, resulting in a high emitter injection efficiency by reducing the reverse injection current from the base to the emitter. The presence of the valence band difference between the emitter and base (ΔE_V) in an HBT is a natural impediment to reverse injection current. The bandgap difference between the emitter and base allows for a significant increase in the gain than if the bandgap difference is not present. This allows one to increase the base doping to very high levels ($> 10^{19}$ cm^{-3}), in fact higher than the emitter doping without hurting the emitter injection efficiency and gain of the device. The high base doping produces the benefit of a very low base resistance, even for extremely thin bases with reduced carrier transit time. At the same time, the emitter doping can be reduced to decrease the base-emitter capacitance. This yields devices which exhibit high frequency response with a high breakdown voltage, making them ideal for power devices. HBTs with breakdown voltage exceeding 20 volts and f_{max} exceeding 120 GHz have been demonstrated. A highly doped base also yields a negligible Early effect with the Early voltage typically greater than 100 volts. This results in high voltage gain.

The AlGaAs/GaAs system also has an advantage in that the lattice constants of the two materials are similar. The difference in the lattice constant of AlAs and GaAs is 0.14% at room temperature, and even less at typical crystal growth temperatures making it possible to grow high quality interfaces with reliable techniques such as organo-metal chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE). The AlGaAs/GaAs devices used for this project were fabricated by a MOCVD process at Raytheon. The emitter and collector are doped with Si, to produce n-type material, and the base is doped with C to produce p-type material. The emitter-base junction is a graded transition to reduce the offset voltage.

In practice it is found that the HBT exhibits superior linearity characteristics compared to other power devices such as metal-semiconductor field-effect transistors (MESFETs). The efficiency or output power must be sacrificed to achieve the same level of linearity performance in a MESFET PA as compared to an HBT PA. It is not intuitive that the HBT would have superior linearity characteristics compared to other power devices such as MESFETs. The HBT has an exponential dependence of I-V characteristics as opposed to MESFETs which have a square-law dependence. It has been proposed however that the intermodulation arising from the base-emitter capacitance (C_{BE}) is out of phase with the intermodulation arising from the collector current resulting in partial cancellation of intermodulation distortion [1.10]. This will be clarified within this thesis.

1.4 Methodology

To asses linearity it was first important to set up an environment where the linearity as well as P_{OUT}, G, and PAE can be predicted with a simple well accepted device model

such as the Gummel-Poon (GP) model. This GP model must be able to accurately predict the figures of merit of interest over a wide range of bias conditions. After the verification of the model and simulation environment with measurements, it was necessary to investigate different sources of nonlinearity in this model. This has been done to formulate a simple analytical method of predicting the linearity from the simple model parameters. This model was then tested for several bias conditions and frequencies.

1.5 Organization

This thesis is presented in seven chapters. Chapter 2 delves into the methods of device characterization and simulation. Both single-tone and two-tone measurement and simulations are discussed. Chapter 3 presents the measurement and simulation data and compares the two for a wide range of biases and loads. Again both two-tone and single-tone results are examined to verify the simulation environment. Chapter 4 presents load pull, source pull, and optimization results. This is totally simulation based. Chapter 5 presents sensitivity analysis data, where a GP model parameter is varied while holding all other parameters constant at a constant bias and load and source impedances. From this it was found which parameters are most important at different conditions. Chapter 6 presents the analytical model that was constructed by examining the individual sources of nonlinearity, and is compared to simulation data. Chapter 7 summarizes the conclusions of the work.

Chapter 2 Measurement and Simulation Setups

2.1 Introduction

In this chapter the measurement and simulation setups will be presented and discussed. DC measurement setups along with S-parameter, one-tone, and two-tone measurements conducted at Raytheon will be described first. Test benches for DC and S-parameter analysis in the HP-Libra environment is explained next. The use of the Gummel-Poon model for HBTs will be reviewed and the method of harmonic balance analysis of nonlinear circuits will be discussed. This will then lead to presentation of simulation setups and test benches in HP-Libra for single-tone, two-tone, load-pull and source-pull simulations.

2.2 DC, S-Parameter, One-Tone, and Two-Tone Measurements

DC measurements on the HBT in common-emitter (CE) configuration was carried out at MIT on a Cascade probe station using microwave probes. Data was collected on an HP4145B semiconductor parameter analyzer. Initial attempts at the measurement produced intolerable levels of oscillations and measurements could not be made. Using a bias-tee on the base with a 10 dB attenuator on the RF output to ground eliminated these oscillations. The measurement setup is shown as Figure 2.1.

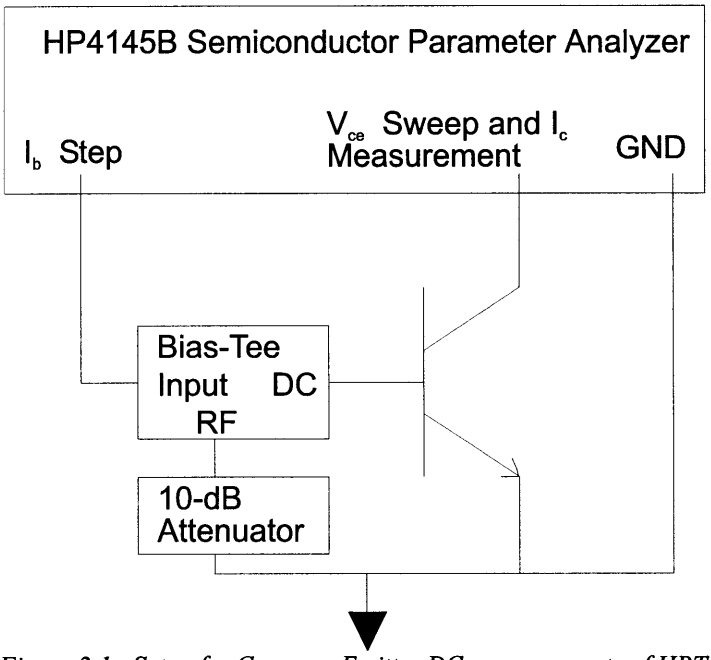


Figure 2.1: Setup for Common-Emitter DC measurements of HBTs.

The S-parameter measurements were made at Raytheon using an HP8510 Network Analyzer. Test structures were utilized to de-embed the effects of the probes and other externalities. The power and intermodulation measurements were done at Raytheon as well. The source was an HP441B Signal generator which feeds the input into FXR brand tuners for tuning the source impedance. The input and output are coupled to the device via HP85108 Bias-tees. On the output there is again FXR brand tuners for setting the load impedance. The output is analyzed on an HP8561E Spectrum Analyzer.

2.3 Gummel-Poon Model

HBTs operating in the large signal regime are typically modeled with the Gummel-Poon Bipolar Transistor Model (GP) as shown in Figure 2.2 [2.1, 2.2]. The GP model is used in many commercial CAD systems such as HP-Libra. The GP parameters for this device have been extracted at Raytheon from DC and S-parameter data. From the GP model, several sources of non-linearity are seen [2.3]. Some of the most significant ones are: the exponential relationship between V_{BE} and I_C, the exponential relationship between V_{BE} and I_B, the V_{BC} dependence of base to collector capacitance (C_{BC}), and the V_{BE} dependence of base to emitter capacitance (C_{BE}). These sources will be evaluated to assess its overall contribution to the linearity of the device in chapter five.

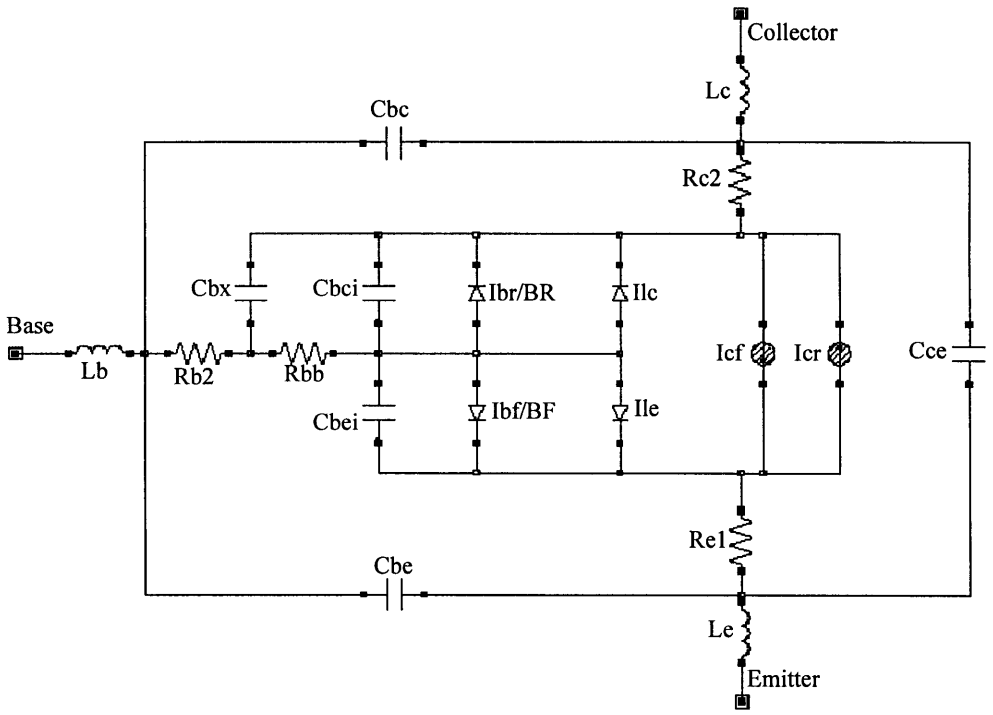


Figure 2.2: Gummel-Poon model of a junction transistor.

2.4 Simulation Environment

The simulation environment used in this study is HP-Libra 6.0 Simulator. Unlike other common simulators like HSPICE, Libra uses a harmonic balance (HB) technique to solve the circuits. In general any generic circuit can be decomposed into a linear and nonlinear portion with the two portions connected by several nodes. HB is a dual domain (time and frequency) technique, where the linear portion is solved in the frequency domain and the nonlinear portion is solved in the time domain as can be seen in Figure 2.3. A flow chart of the HB method is shown as Figure 2.4.

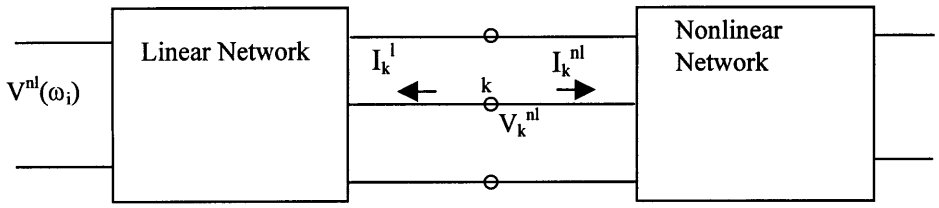


Figure 2.3: The network decomposed into its linear and nonlinear parts for HB analysis.

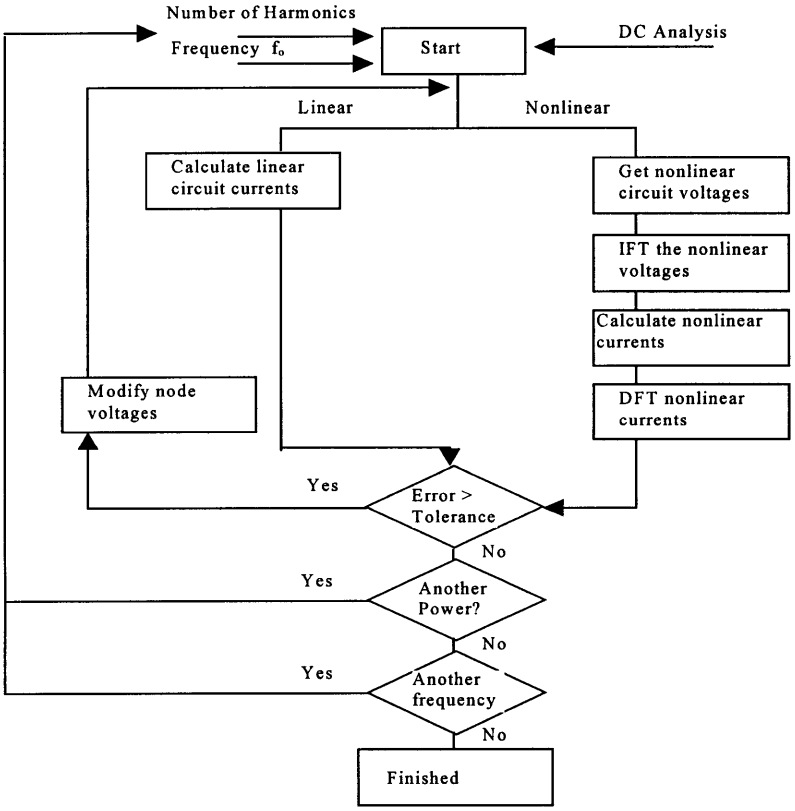


Figure 2.4: Flowchart of the HB procedure.

In a HB simulation, the frequency, f_o, and the number of harmonics to be used, i, must be specified. First a DC analysis of the circuit is done. From the DC analysis, the initial voltages at each node, k, between linear and nonlinear part ($V^{nl}_k(\omega_i)$) are found. Based on these voltages, the currents flowing into each node of the linear parts of the circuit ($I^l_k(\omega_i)$) are solved using frequency domain techniques. An inverse Fourier transform (IFT) is done on the interface node voltage to get the voltage in the time domain ($V^{nl}_k(t)$). Using $V^{nl}_k(t)$, a time domain analysis is done on the nonlinear part, based on the nonlinear model (GP model in this case). This yields the current flowing into the nonlinear ports, $I^{nl}_k(t)$. A discrete Fourier transform (DFT) is done on the $I^{nl}_k(t)$, to get the current in the frequency domain $I^{nl}_k(\omega_i)$. If the difference between $I^l_k(\omega_i)$ and $-I^{nl}_k(\omega_i)$ is within the specified tolerance, then the process is complete. Otherwise, the node voltages $V^{nl}_k(\omega_i)$ must be modified and the analysis repeated. This analysis must be repeated for each desired harmonic frequency [2.4].

2.5 Simulation Setup Files

The basic device description file called *EEGP_ce* was created, which contained the GP model parameters. The device model file is then placed in the CE Biasing circuit shown in Figure 2.5. This is the file where all the biases are set for the device by adjusting **VCC** and **VB1**. These sources are inductively coupled to the device so that it is a high impedance path for RF and is effective in setting the bias.

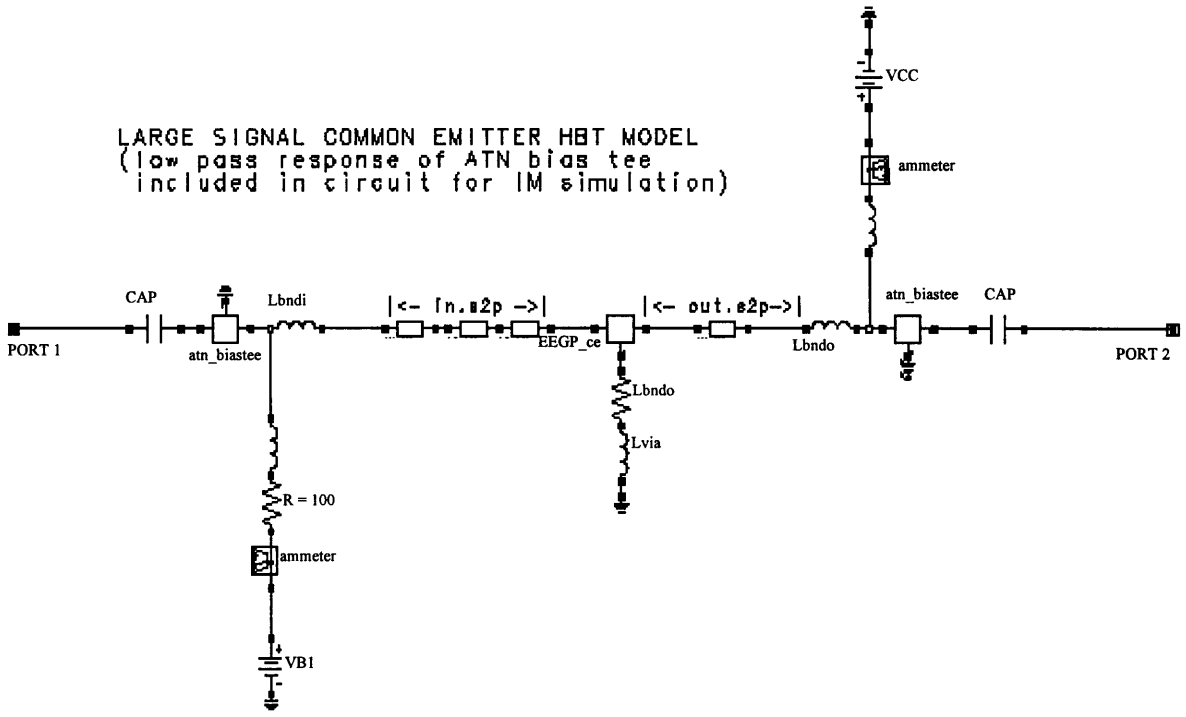


Figure 2.5: CE Biasing Circuit for Simulation.

This file also includes the parasitics from the non-intrinsic parts of the device. The *EEGP_ce* box is the intrinsic HBT model as described by the GP model. *Rblst* on the emitter is for thermal stability. *Lvia* is an inductance on the emitter which models the path to ground for the common-emitter configuration. These extrinsic components model the emitter via. The blocks in *in.s2p* and *out.s2p* are transmission lines of varying lengths and widths. These model the path from the probe contacts to the actual metallurgical contacts. *Lbndi* and *Lbndo* are inductances associated with the bond wires connecting the device to the measurement jig. On the input and the output, there are S-parameter boxes which simulate a bias-tee. The boxes represent a file which lists the four S-parameters of the two port bias-tee at different frequencies. The input and output RF ports are both coupled capacitively to the device. This is to allow a low impedance path to the RF input and output and block the DC biasing. This biasing circuit is used in all of the various simulation test benches.

2.6 DC and S-parameter Simulation

The DC simulations were performed using the test bench of Figure 2.6. In this setup, *bias1* represents base current which is swept from 0 to 500 μA in steps of 100 μA. *Bias2* is the collector voltage, which is swept from 0 to 6 volts in steps of 0.1 volts.

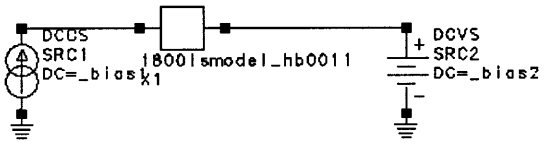


Figure 2.6: DC test bench in HP-Libra.

The S-parameter simulations were conducted placing the two port network of Figure 2.5 in a test bench and specifying the characteristic impedance. The four S-parameters are gotten for frequencies in the range of 250 MHz to 20 GHz.

2.7 One-Tone and Two-Tone Simulations

The test bench for the one-tone power simulation is shown as Figure 2.7. *CE3R* is the biasing common-emitter configuration of Figure 2.5. The frequency of the power source is kept constant while the power is swept from –20 dBm to 20 dBm. The power at the source frequency delivered to *Rload* is evaluated, along with Gain, base current, collector current, and power added efficiency.

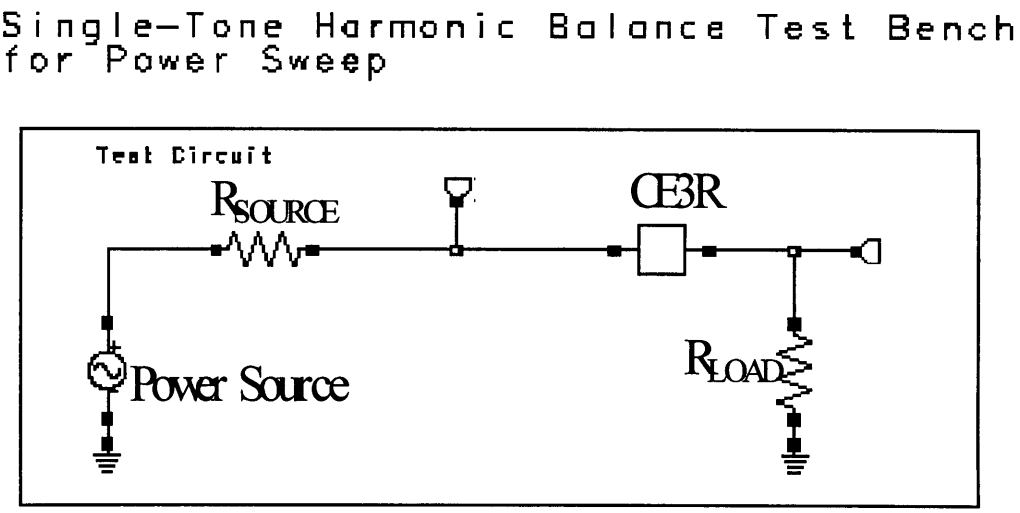


Figure 2.7: One-Tone Simulation Test Bench.

The two-tone power simulation test bench is shown as Figure 2.8. There are two inputs in this simulation test bench one with f_1 = 837 MHz and the other with f_2 = 837.1 MHz. Otherwise the two-tone test bench is very similar to the one-tone test bench. Not only is the $P_{OUT}(f_1)$, PAE, I_C, and I_B found like before, but also $P_{OUT}(f_2)$, $P_{OUT}(2f_1 - f_2)$, $P_{OUT}(2f_2 - f_1)$ are found.

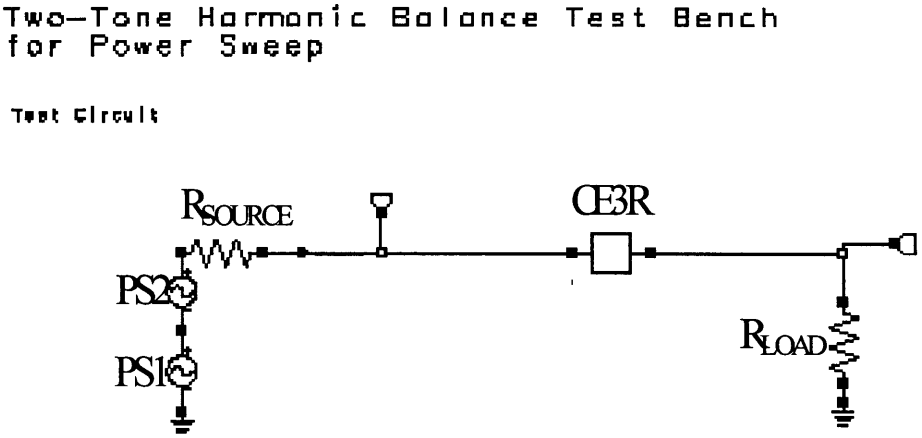


Figure 2.8: Two-Tone Simulation Test Bench.

2.8 Load and Source Pull

The final simulation benches that are needed are the load pull and the source pull benches. The test benches for one-tone and two-tone load pulls are shown as Figures 2.9 and 2.10, respectively. In a load pull, measurements of interest are taken at several different load impedances. In the benches shown, the source impedance is kept constant

as well as the load impedances seen by the harmonics. The load impedance at the fundamental frequency is varied with the *tuneterm* component in the circuit. The load impedance seen by the fundamental frequency is controlled with a tuner, which presents the device with several impedances as specified by the user. Based on this, contours of constant value of these data are plotted on a Smith chart. This is an effective graphical way of seeing what load must be presented to the device to optimize the figures of merit of interest. Since the optimal loads for maximizing different figures of merit will likely be different, this graphical approach allows one to understand the tradeoffs of a particular load.

The one-tone source pull circuit is shown as Figure 2.12. The source pull is very similar to the load pull. Different source impedances for the fundamental frequency are introduced to the device, and the performance is recorded. Then constant contours of the figures of merit are plotted on a Smith chart which represents the source impedance space.

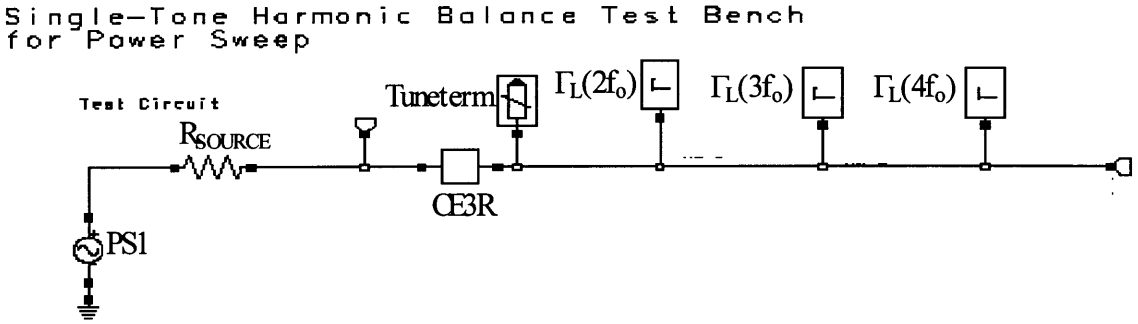


Figure 2.9: One-tone load pull simulation test bench.

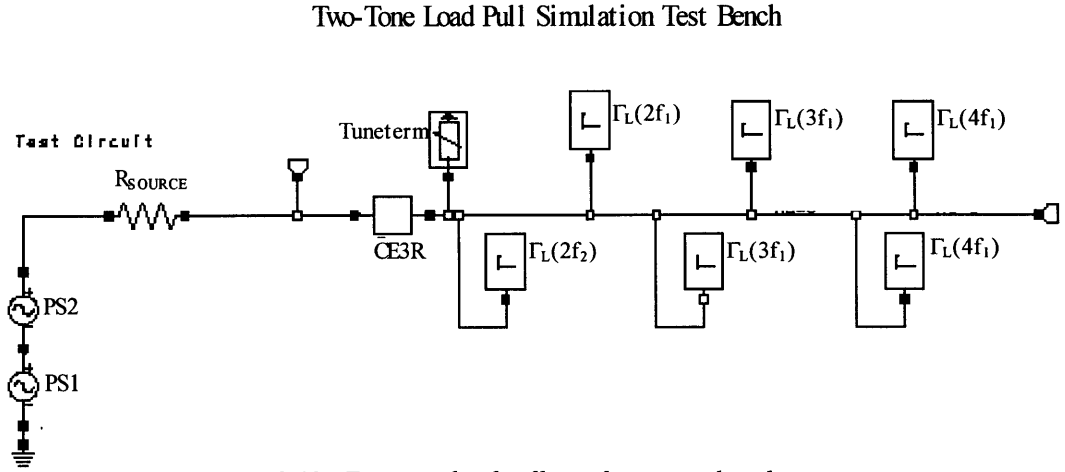


Figure 2.10: Two-tone load pull simulation test bench.

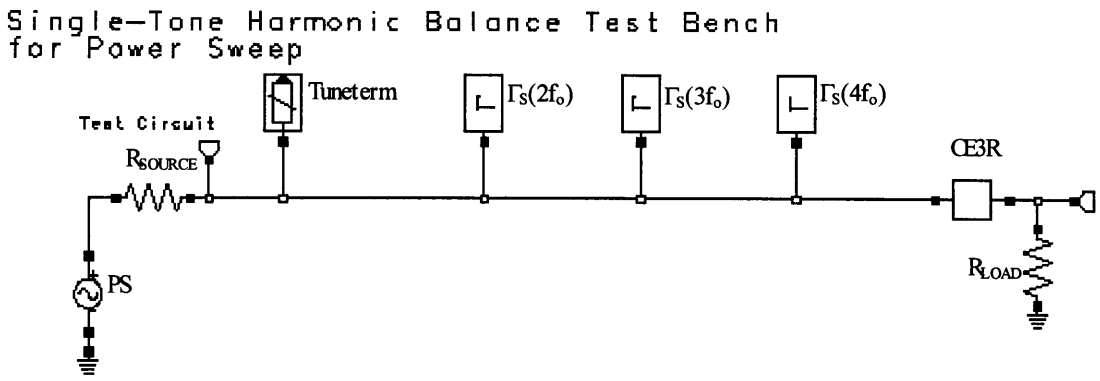


Figure 2.11: One-tone source pull simulation test bench.

2.9 Conclusions

This chapter has introduced the measurement and simulation setups for AlGaAs/GaAs HBTs. The quality of the simulation environment based on these simulation test benches for the DC, S-parameter, one-tone and two-tone measurements will be examined in the next chapter. The fourth chapter will use the load and source pull test benches for device optimization.

Chapter 3-Measurements and Simulations

3.1 Introduction

The last chapter showed the setups that were used to measure and simulate the various figures of merit of interest in this work. This chapter presents the data for DC measurement, S-parameter measurements and simulation, one-tone measurement and simulation, and two-tone measurement and simulation. The figures in this section highlight the effectiveness of the Gummel-Poon model in the HP-Libra simulation environment for device simulation.

3.2 DC Measurements

The result of the DC measurements are shown as Figure 3.1. The device was probed to a maximum collector current of 100 mA, since this is the maximum current that the HP4145B can handle [3.1].

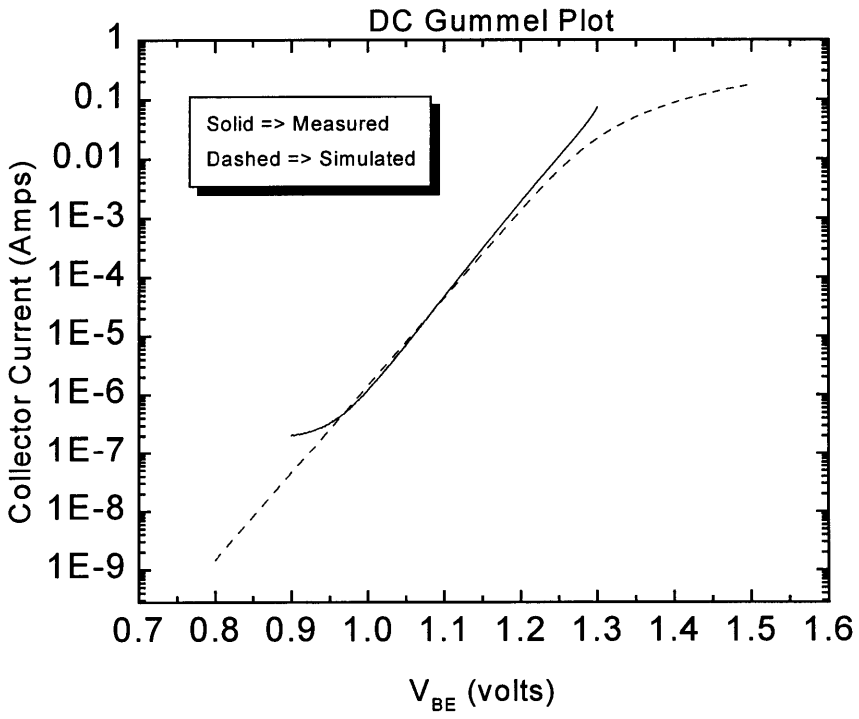


Figure 3.1: HBT DC Gummel Plot.

It is seen that there is a reasonably good match between the measured and simulated collector current.

3.3 S-Parameters

The comparisons of measurements and simulation of the four s-parameters at a bias point of V_{CE} = 3.6 volts and I_C = 45 mA are shown as Figures 3.2-5. It can be seen that the measurements and simulations match well up to frequencies in excess of 2 GHz. This implies accurate extraction of the GP parameters.

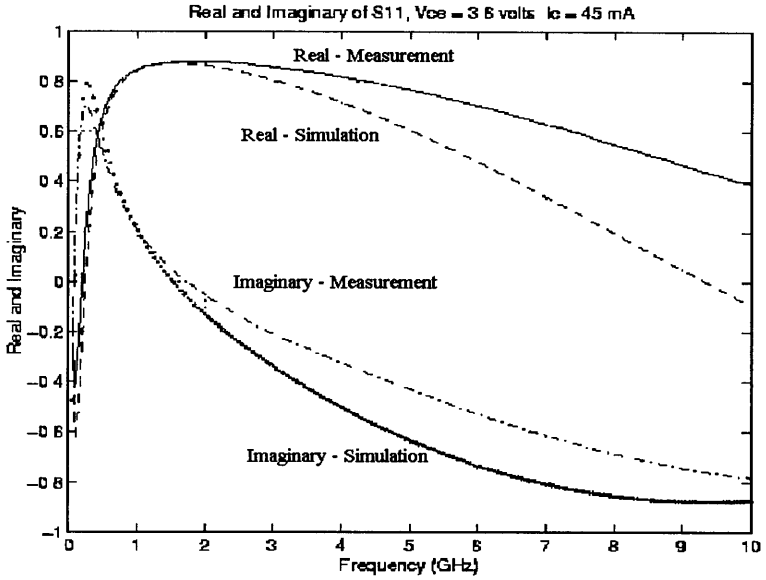


Figure 3.2: S_{11} Real and Imaginary Simulation and Measurement data.

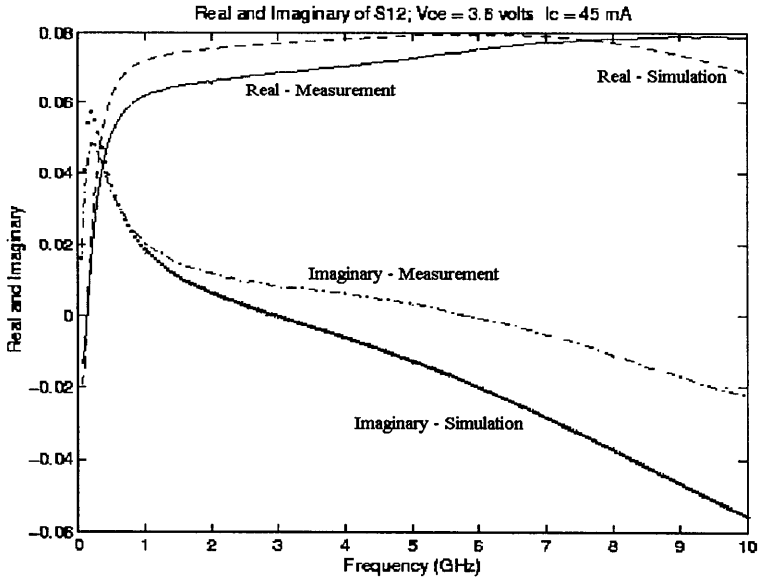


Figure 3.3: S_{12} Real and Imaginary Simulation and Measurement data.

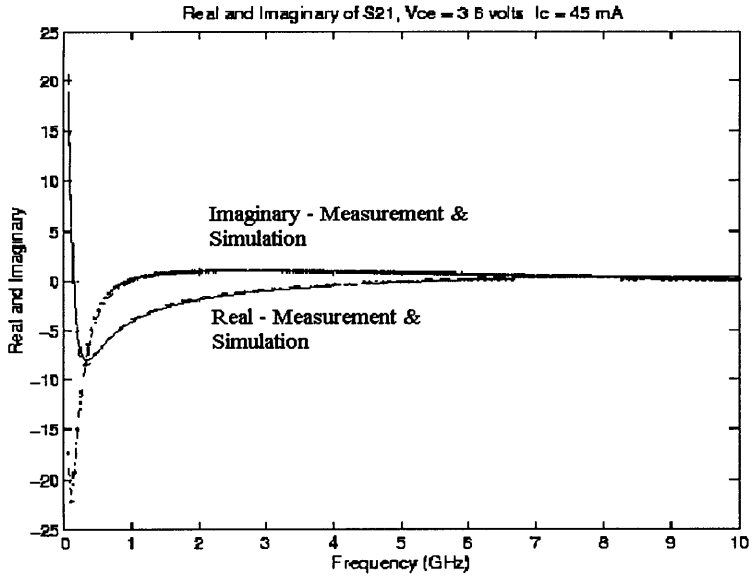


Figure 3.4: S_{21} Real and Imaginary Simulation and Measurement data.

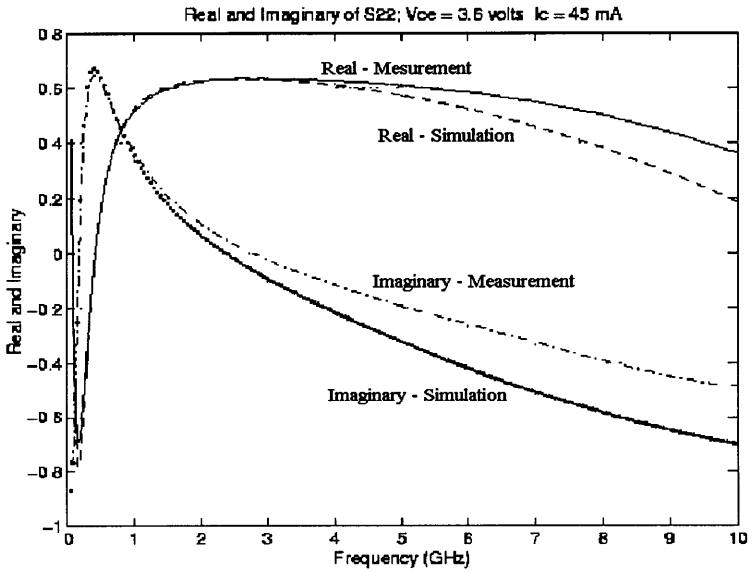
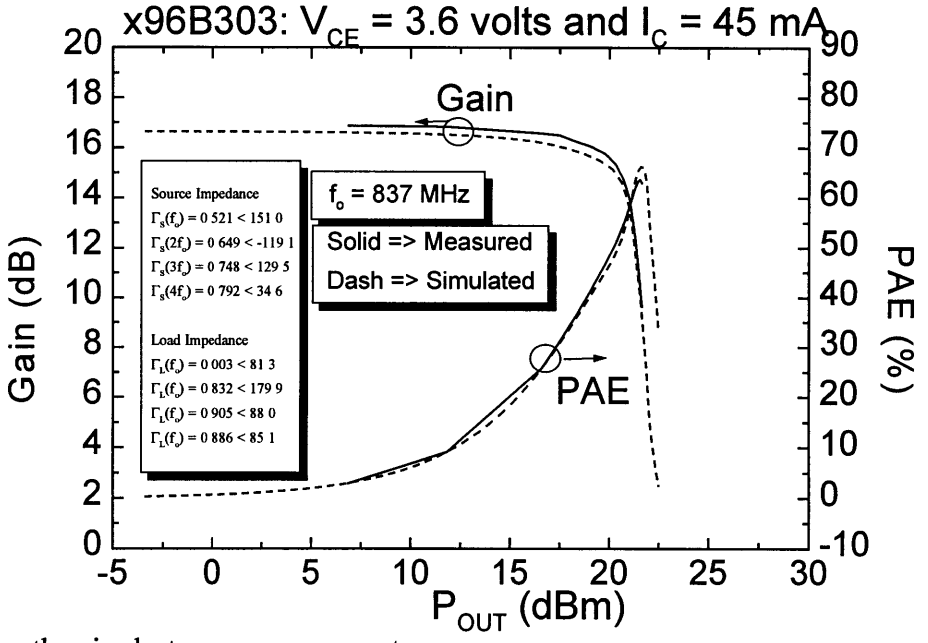


Figure 3.5: S_{22} Real and Imaginary Simulation and Measurement data.

3.4 Single-Tone Measurements and Simulations

An example of the single-tone simulation and measurement is shown as Figure 3.6. The Gain (left y-axis) and PAE (right y-axis) are plotted versus P_{OUT} for both the simulation

and the measurement. It can be seen that the simulation environment is effective in



predicting the single-tone measurements.

Figure 3.6: Single-Tone Simulation and Measurement Results for load $\Gamma_L(f_O) = 0.003\angle 81.3°$.

It is instructive to point out the salient features of this plot at this time. As can be seen, for low output power, the gain is constant at around 16.7 dB and then starts to compress around P_{OUT} = 16 dBm. The 1dB gain compression point is at P_{OUT} = 18.5 dBm. Beyond this point, it is seen that the gain drops off quickly. This is because at this point the output signal is sufficiently large so that the HBT is driven into cutoff, causing clipping of the output, which manifests itself as a sharp reduction in G. The P_{DC} is relatively constant with the P_{OUT}, so PAE increases as P_{OUT} increases. Beyond the 1dB gain compression point, the PAE improves significantly and peaks as the G starts dropping sharply. As the Gain falls off quickly, so does ($P_{OUT} - P_{IN}$), causing the PAE to decrease. The comparisons between simulation and measurements have been done for several load impedances and biases. A few select ones are shown as Figures 3.7-9. Results are shown for collector current bias in the range of 45 mA to 180 mA and several different load impedances. These plots also show similar characteristics to Figure 3.6. For all conditions, the simulations match the measurements relatively well.

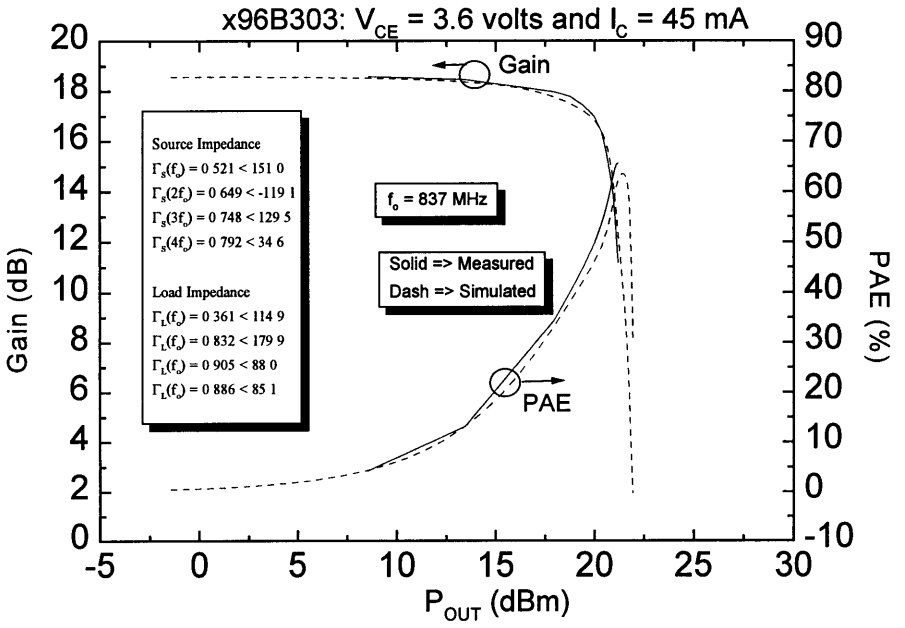


Figure 3.7: Single-Tone Simulation and Measurement Results for load $\Gamma_L(f_O)$ = 0.361∠114.9°.

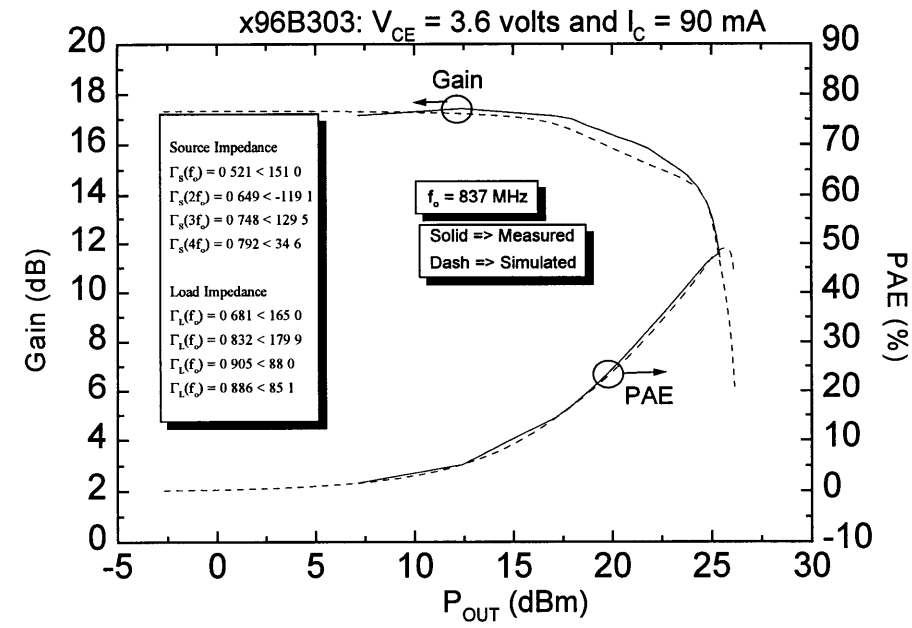


Figure 3.8: Single Tone Simulation and Measurement Results for load $\Gamma_L(f_O)$ = 0.681∠-165.0°.

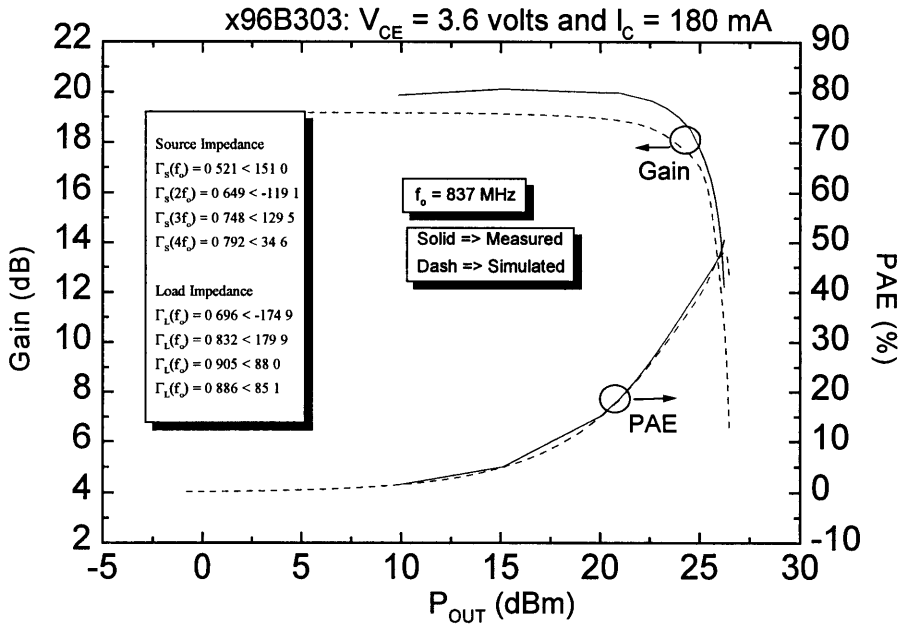


Figure 3. 9: Single-Tone Simulation and Measurement Results for load $\Gamma_L(f_O)$ = 0.696∠-174.9°.

3.5 Two-Tone Simulations

Figures 3.10 shows an example of the two-tone measurement and simulation results from the setups shown in the previous chapter. The P_{OUT} on the x-axis of this graph is the output power at ω_1 only, so the output power needs to be shifted by approximately 3 dBm to compare to the one-tone test output power. The targeted IMD3 for design purposes is –25 dBc. This level is right around the 1 dB gain compression point.

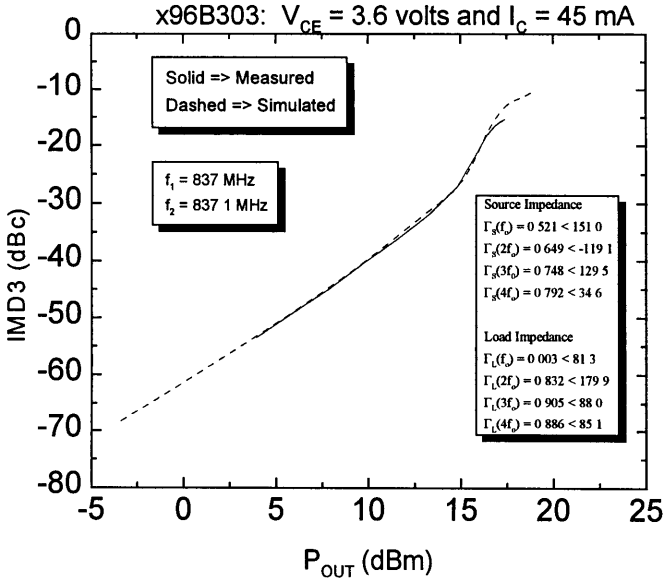


Figure 3.10: Two-Tone Simulation and Measurement Results for load $\Gamma_L(fO) = 0.003\angle 81.3°$.

It can be seen from this figure that again there is an excellent match between the measurements and the simulations. Some of the interesting points here is that the IMD3 seems to be increasing linearly with P_{OUT} with a certain slope up to about P_{OUT} = 15.5 dBm. After this point, which is the 1 dB Gain compression point, the IMD3 increase with a greater slope with P_{OUT} due to output clipping. The two-tone measurements and simulations have also been compared across a wide range of load impedances and biases. Some of these are shown as Figures 3.11-13.

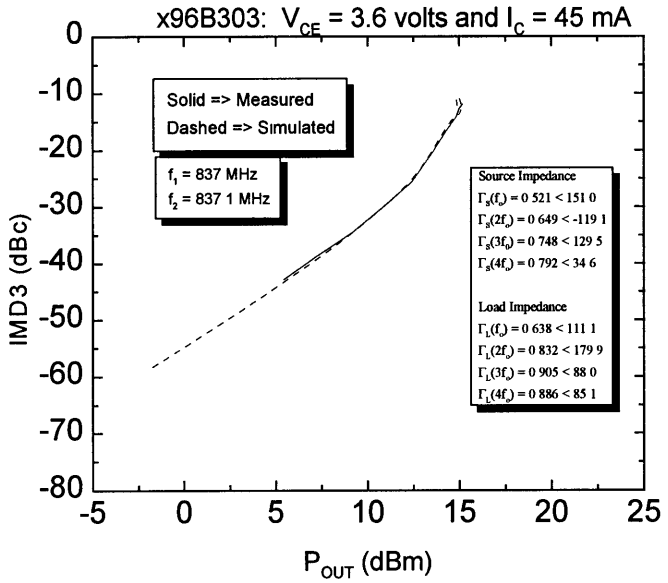


Figure 3.11: Two-Tone Simulation and Measurement Results for load $\Gamma_L(fO) = 0.638\angle 111.1°$.

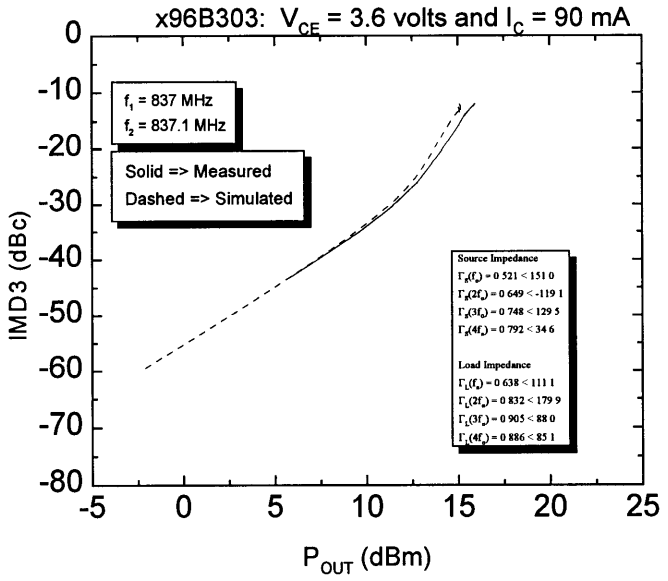


Figure 3.12: Two-Tone Simulation and Measurement Results for load $\Gamma_L(fO) = 0.638\angle 111.1°$.

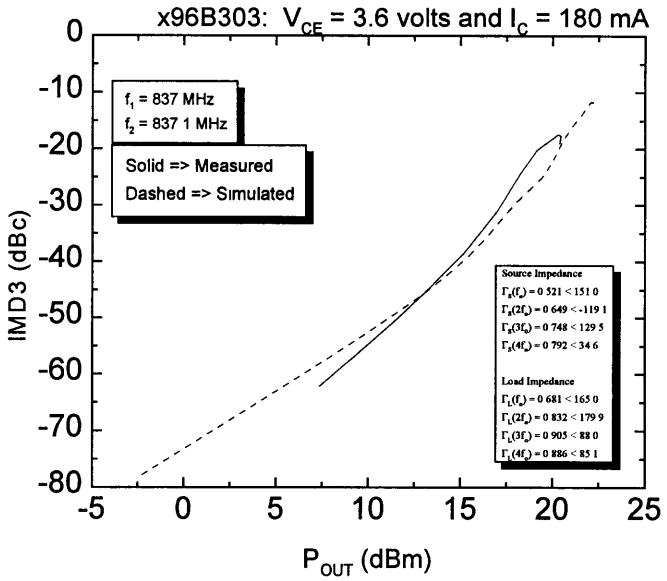


Figure 3.13: Two-Tone Simulation and Measurement Results for load $\Gamma_L(f_O) = 0.681\angle 165.0°$.

3.6 Conclusions

This section showed simulations based on the setups from the previous chapter. The good agreement that is found between the simulations and the measurements, for a wide range of bias points and input and output impedances suggests that the HP-Libra simulation environment with the GP model is effective in predicting device performance, in particular, linearity. The simulation environment should be instrumental in predicting accurate load pull and source pull data. These data are shown in the next chapter along with the source and load optimization.

Chapter 4 - Load Pull and Source Pull Simulations

4.1 Introduction

The previous chapter showed the excellent correlation between measured and simulated data for both one-tone and two-tone analysis over a wide range of biases and loads. Since the simulations work in such a wide range of load impedances, it is fair to assume that the simulations will work in all of the load impedance space. This instills some level of confidence in the load and source pull simulation analysis which is presented in this chapter. The load pull and source pull analysis are used here to achieve an optimal load and source impedance [4.1]. The simulation setups for this type of analysis was shown in chapter 2.

4.2 Stability Space

Before doing load-pull analysis, it is important to determine what load and source impedances may be introduced to the device without the PA becoming unstable due to high feedback gain. The stability for the device can be plotted in impedance space to show such constraints. The input stability circle and the output stability circle are the locus of points where the magnitude of the input reflection coefficient $|\Gamma_{in}|$ and the magnitude of the output reflection coefficient $|\Gamma_{out}|$ are equal to one [4.2]. For the device in question, one may introduce input impedances that lies outside of the input stability circle and output impedances that lie outside of the output stability circle. These plots for three different biasing conditions are shown as figures 4.1-3.

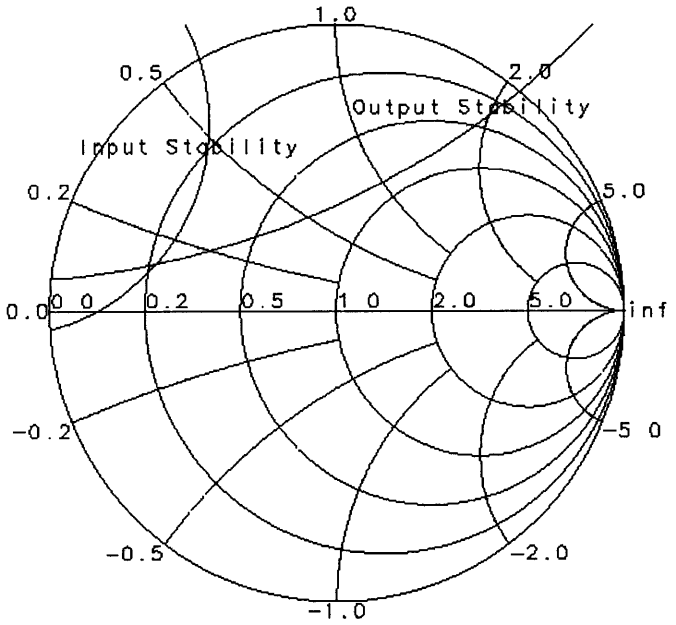


Figure 4.1: Stability plot for V_{CE} = 3.6 volts and I_C = 45 mA.

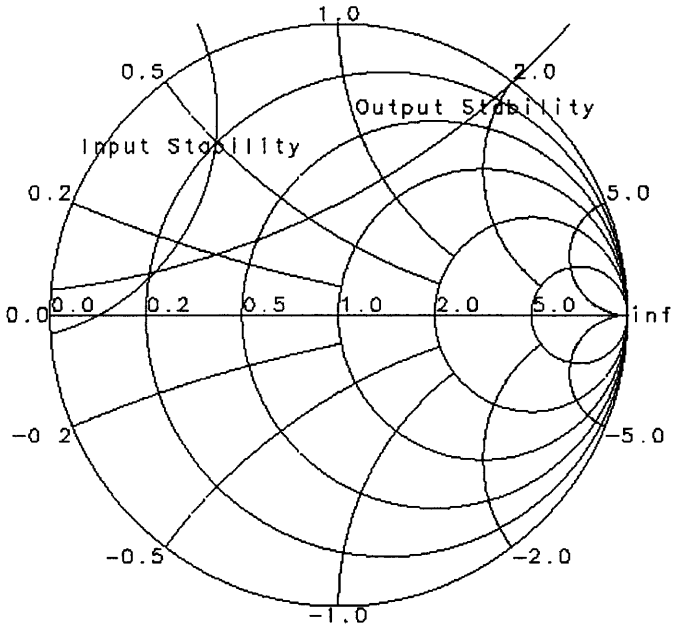


Figure 4.2: Stability plot for V_{CE} = 3.6 volts and I_C = 90 mA.

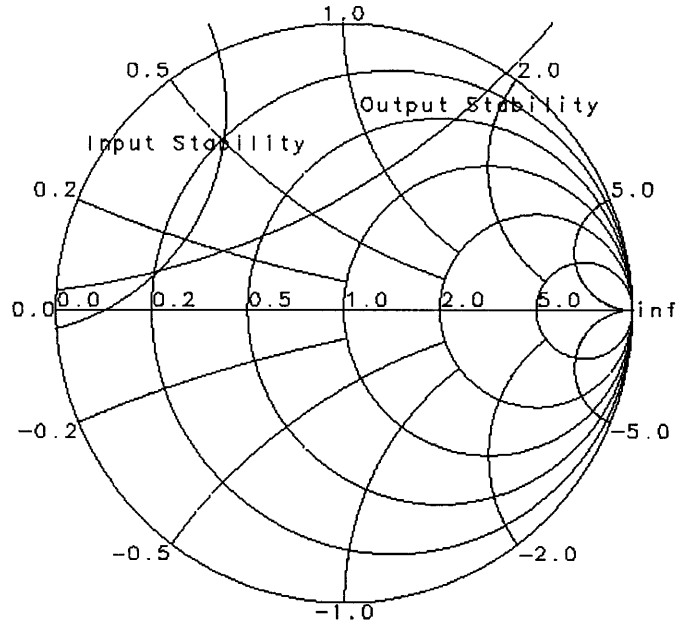


Figure 4.3: Stability plot for V_{CE} = 3.6 volts and I_C = 180 mA.

4.3 One-Tone Load Pull

The one-tone load pull simulation was used to show optimal load biases for the one-tone figures of merit (G, P_{OUT}, and PAE). The load pull simply applies several output impedances and calculates the various figures of merit. After that, the data is used to extrapolate constant contours of the figure of merit being examined. During this simulation the source reflection coefficients and load reflection coefficients at the harmonics are held constant as shown in chapter 2. Examples of these simulations are shown as Figure 4.4 and Figure 4.5, where constant contours of G and PAE are plotted. Since the load pull simulations are conducted at a constant input power, P_{IN}, it would be redundant to plot both G and P_{OUT}. The source reflection coefficients are the same as those used for comparisons in the previous chapter.

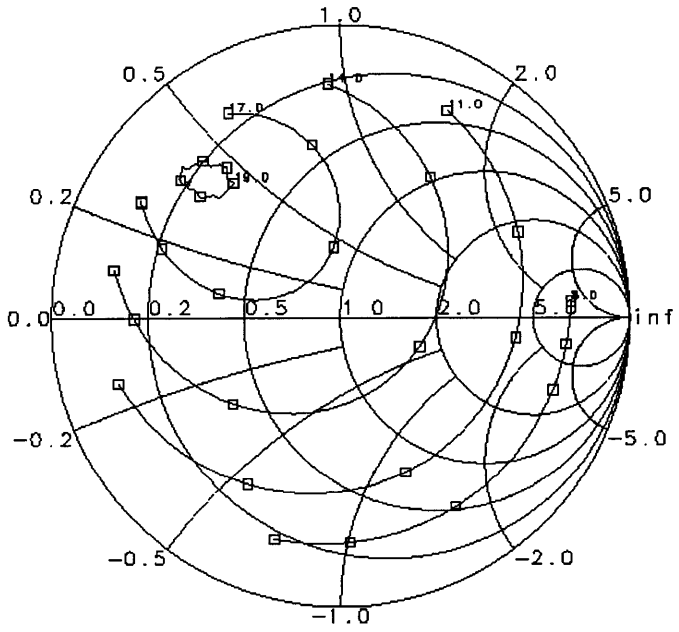


Figure 4.4: One-tone load pull simulation for gain contours at Pin = 0 dBm, I_C = 45 mA, and V_{CE} = 3.6 volts.

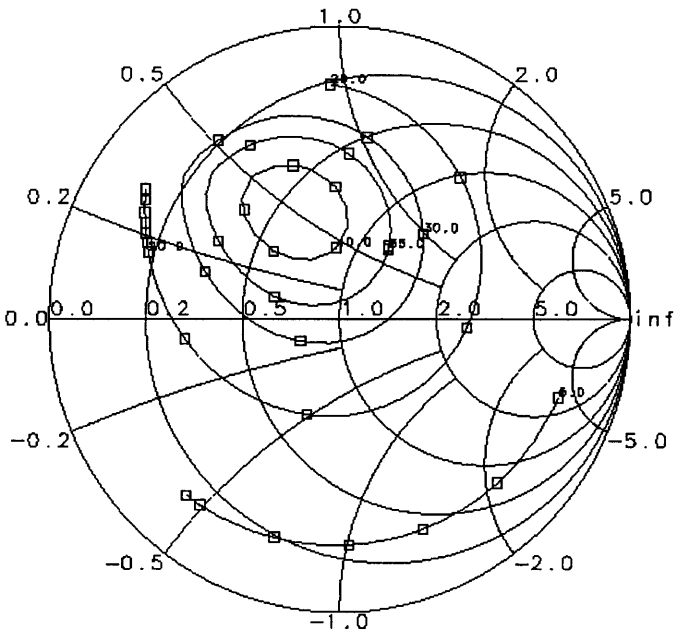


Figure 4.5: One-tone Load Pull simulation for PAE Contours at Pin = 0 dBm, I_C = 45 mA, and V_{CE} = 3.6 volts.

From this plot it is seen that the best possible point with regards to PAE and G is where the two highest contours overlap. Unfortunately, at that load impedance, the PA is not stable, so we must approach the optimal point, but be careful to stay in the stable load impedance space. The point z = (0.5 + j0.2) is a good point for the load. Since Z_o = 50 Ω, the load impedance would be $Z_L(f_o)$ = (25 + j10). This corresponds to a reflection coefficient of $\Gamma_L = 0.356 \angle 150.6°$. The performance at this load is shown as Figure 4.6.

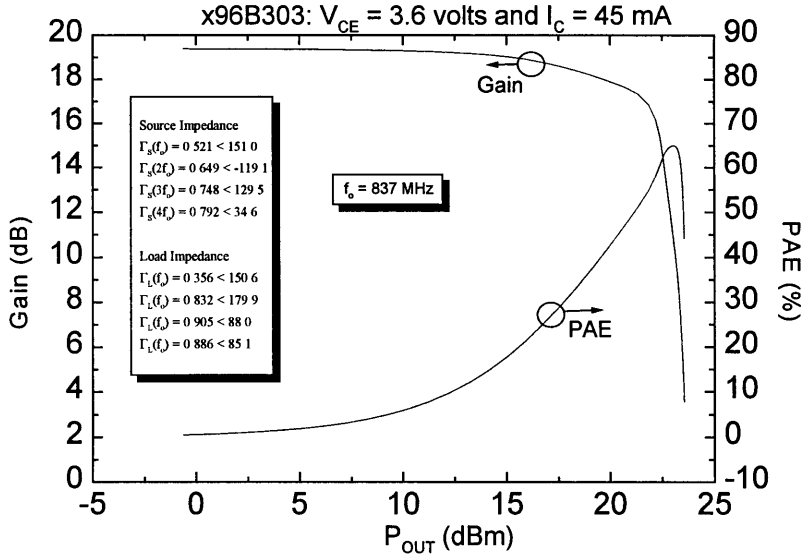


Figure 4.6: Gain and PAE after load optimization via load pull simulation.

From this plot it is apparent that the load pull analysis was effective in finding a good load bias when compared to Figures 3.6 and 3.7 of the previous chapter. At the $P_{IN} = 0$ dBm point, the Gain is equal to the P_{OUT}. This point is around $P_{OUT} = 18.5$ dBm, which is right around the 1 dB gain compression point, where in general, the two-tone IMD3 figure of merit is acceptable (< -25 dBc). The IMD3 will be examined in the next section.

4.4 Two-tone Load Pull

The two-tone load pull analysis is used to asses the dependence of the IMD3 figure of merit on the load impedance at a constant bias and available input power. Like the one-tone load pull analysis, the constant contours of the figure of merit, in this case IMD3, are plotted in the load impedance space as shown in Figure 4.7. From this simulation, it seems that an impedance of $Z_L = 0.356 \angle 150.6°$ will not only result in good one-tone performance, but also good two-tone performance. The two-tone performance at this load is shown as Figure 4.8.

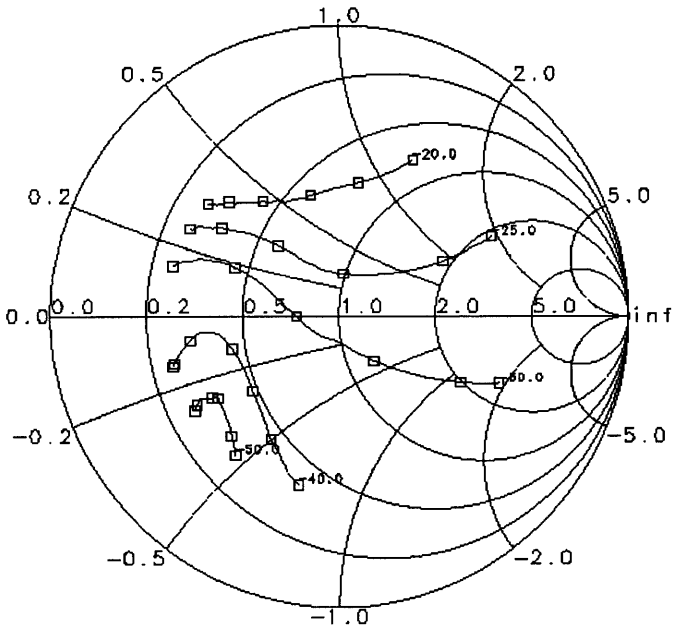


Figure 4.7: Two-tone Load Pull simulation at Pin = 0 dBm, I_C = 45 mA, and V_{CE} = 3.6 volts, showing constant IMD3 contours.

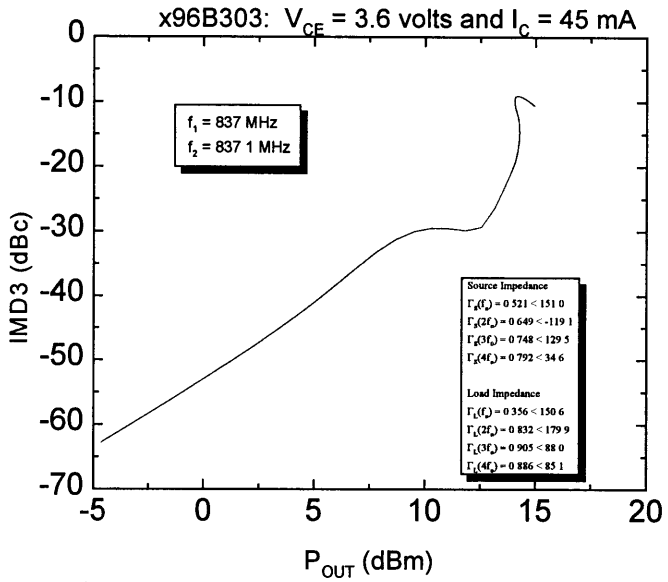


Figure 4.8: IMD3 after load optimization via two-tone and one-tone load pull simulation.

The P_{OUT} of the two-tone simulation with the P_{OUT} of the one-tone simulation are not the same. This is because, when one tone is input into the PA, only the amplitude of that signal will induce the device to reach compression. In the two tone analysis, the superposition of the two signals can push the device into compression sooner. The P_{OUT} reported on the two-tone analysis is the power output at the lower of the two frequencies (ω_1). The load pull was done at a P_{OUT} of 13.1 dBm. At that point, the IMD3 figure of merit is at –26.4 dBc. This figure is within specification, and close to the maximum allowable IMD3 of –25 dBc. This indicates that the points examined on the one-tone and two-tone load pulls are appropriate points to examine for device optimization.

4.5 One-tone Source Pull

One-tone source pull simulations were examined to determine the dependence of the PAE and Gain on the source impedance at the fundamental frequency. The source pull simulation is shown as Figure 4.9. The load reflection coefficient used for this simulation was the optimized $\Gamma_L(f_o) = 0.356 \angle 150.6°$ from the load pull analysis.

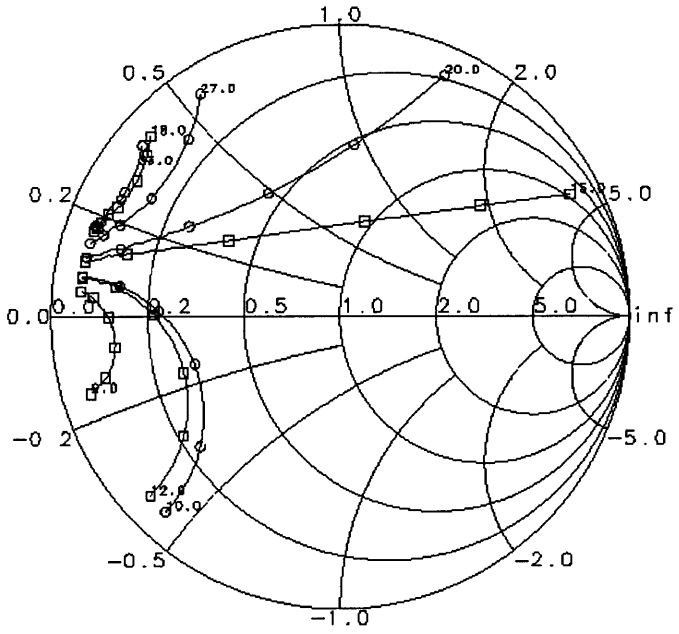


Figure 4.9: Two-tone Source Pull simulation at Pin = 0 dBm, I_C = 45 mA, and V_{CE} = 3.6 volts. Circle markers indicate PAE constant contours and square markers indicate Gain contours.

Keeping the stability requirements in mind, it seems that a normalized impedance of z = (0.35 + j0.2) is a good point for optimal performance. This corresponds to a source impedance of $Z_S(f_o)$ = (17.5 + j10) Ω, and a source reflection coefficient of $\Gamma_S(f_o)$ = 0.569 ∠ 156.6°. This value is very close to the impedance where all the previous measurements and simulations were made. The single-tone and two-tone performances at the optimized source and load impedances is shown as Figures 4.10 and 4.11.

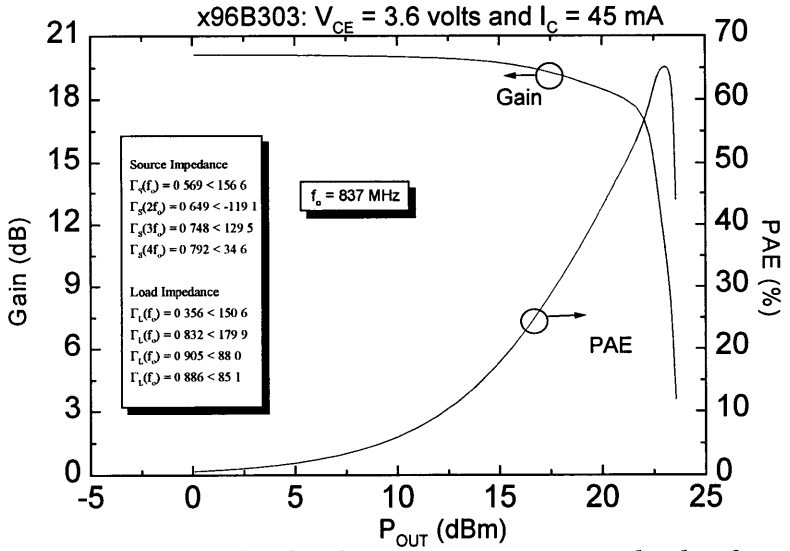


Figure 4.10: Gain and PAE after load and source optimization via load and source pull simulation.

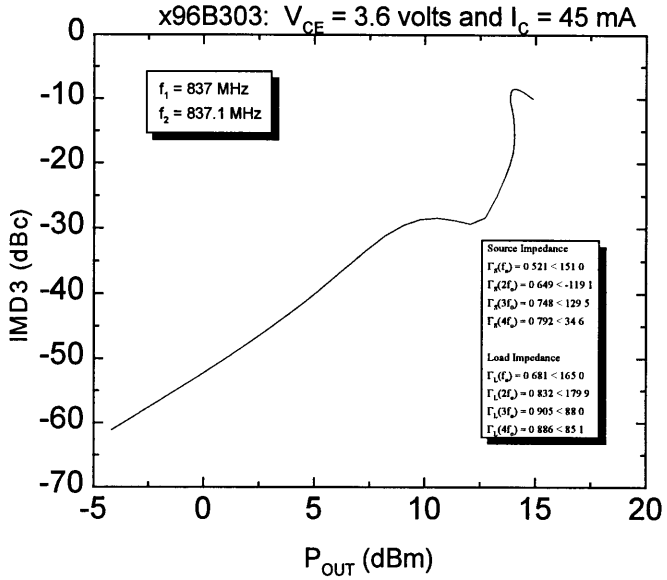


Figure 4.11: IMD3 after load optimization via two-tone and one-tone load pull simulation.

At the point where the IMD3 is –25 dBc, the gain and PAE is at 19 dB and 33%, respectively, which is better than the gain of 18.5 dB and PAE of 33% after just conducting load optimization at the same IMD3. This is best achievable performance at this bias of V_{CE} = 3.6 volts and I_C = 45 mA.

4.6 Conclusions

In the previous chapter, it was shown that the simulation environment was effective in predicting the figures of merit of interest over a wide range of biases and impedances. This provides confidence in the validity of the load and source pull simulations that were shown in this chapter. The input and output stability of the device was first mapped, so that an impedance which renders the device unstable is not chosen. The load pull and source pull were used to optimize the device performance by modifying the load and source impedances at the fundamental frequency. The next chapter will examine the sources of intermodulation distortion.

Chapter 5 - Sensitivity Analysis Simulation

5.1 Introduction

Chapter two showed the simulation setups which were used to asses device performance by predicting the figures of merit of interest. Chapter three showed that this simulation environment is very good at predicting device performance across a wide range of biases and impedances. The purpose of this chapter is to investigate how each of the Gummel-Poon parameters affects the intermodulation distortion purely based on simulation results. The next chapter will examine the intermodulation distortion from an analytical basis.

5.2 High I_C Bias

The sensitivity analysis performed, was to vary the GP parameter of interest by +10%, leaving all the other parameters unchanged in the simulation. The base biasing voltage may have to be modified to maintain the collector current at a constant level of 180 mA. The figures of merit are simulated at this modified GP description. This process is repeated for a –10% modification of the GP parameter of interest. It was found that the intermodulation distortion at a high collector current was affected by the base-collector junction capacitance. The sensitivity analysis of CJC, MJC, VJC, CJE, MJE, and VJE are shown as Figures 5.1-6. These are shown by plotting the IMD3 vs. P_{OUT} after varying the GP parameter by +/- 10%. These simulations were conducted at constant load and source impedances.

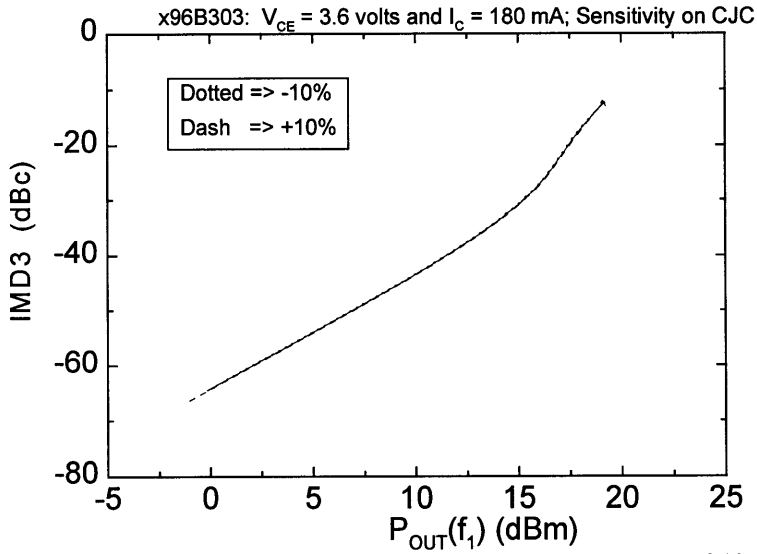


Figure 5.1: Sensitivity Analysis done for CJC, where CJC is increased (dashed) and decreased (dotted) by ten percent.

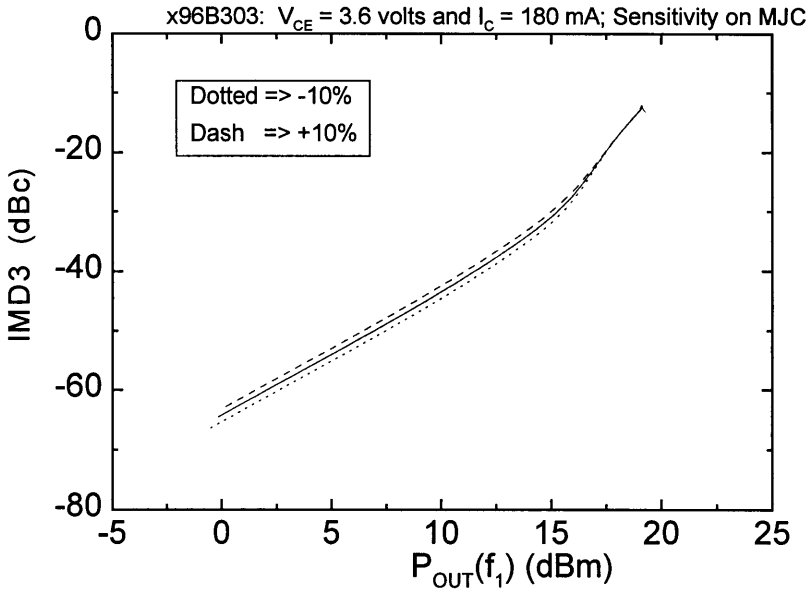


Figure 5.2: Sensitivity Analysis done for MJC, where MJC is increased (dashed) and decreased (dotted) by ten percent.

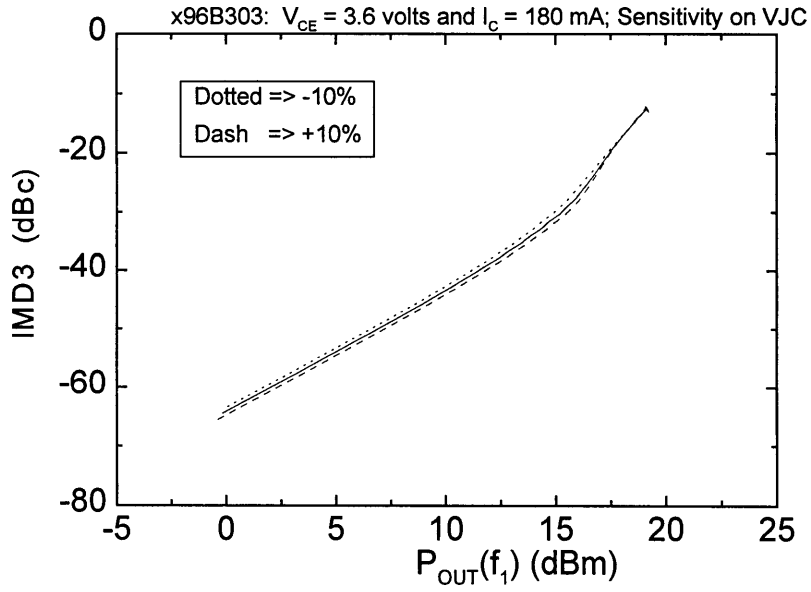


Figure 5.3: Sensitivity Analysis done for VJC, where VJC is increased (dashed) and decreased (dotted) by ten percent.

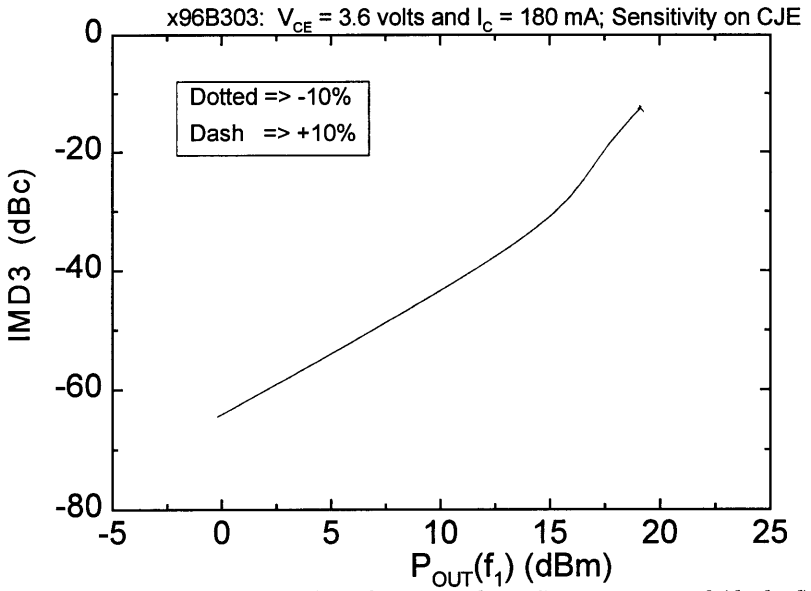


Figure 5.4: Sensitivity Analysis done for CJE, where CJE is increased (dashed) and decreased (dotted) by ten percent.

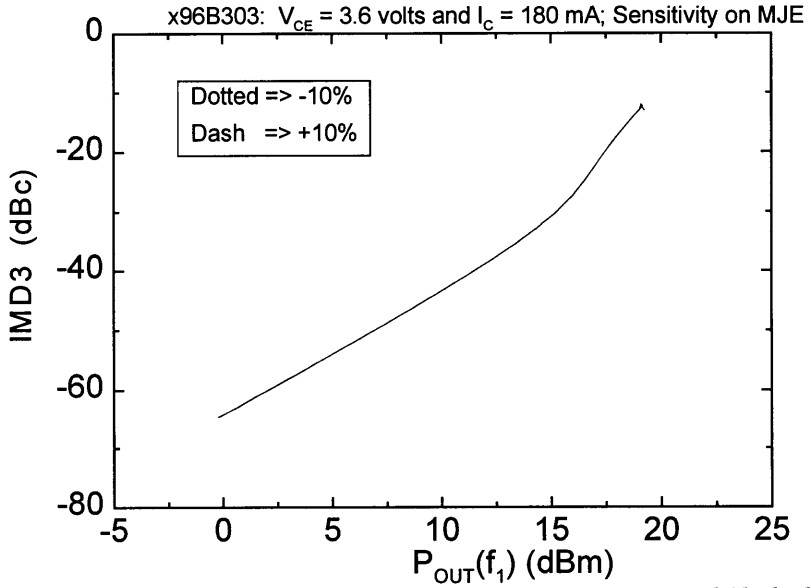


Figure 5.5: Sensitivity Analysis done for MJE, where MJE is increased (dashed) and decreased (dotted) by ten percent.

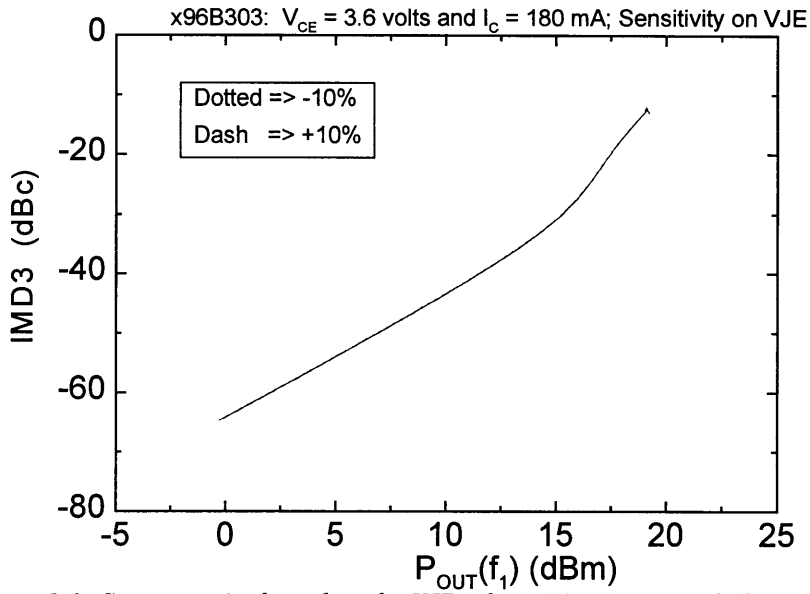


Figure 5.6: Sensitivity Analysis done for VJE, where VJE is increased (dashed) and decreased (dotted) by ten percent.

It is clear that changing CJC does not affect IMD3 very much, but IMD3 improves (i.e. goes down) with decreasing MJC and increasing VJC as shown in Figures 5.2 and 5.3. The equation for C_{bc} is:

$$C_{bc} = \frac{CJC}{\left(1 - \frac{V_{BC}}{VJC}\right)^{MJC}} \qquad \text{[Equation 5.1]}$$

From this equation it can be seen that C_{bc} is nonlinearly related to VJC and MJC and linearly related to CJC. As VJC increases C_{bc} is less nonlinear with v_{BC} and as MJC increases, C_{bc} is more nonlinear with v_{BC}. This seems to imply that a reduction in the nonlinearity of C_{bc}, can result in an overall improvement in the nonlinearity.

It is also seen that at this bias condition, there is little variation in IMD3 with variation in CJE, MJE, or VJE. This implies that at high collector currents, the nonlinearity of the base-emitter capacitance plays a small part in the overall nonlinearity of the device whereas the base-collector capacitance plays a significant role.

The GP Parameters, RE and NF also had an effect on the overall nonlinearity of the PA. The emitter resistance, RE had a small effect. An increase in the emitter resistance resulted in a increase in the overall IMD3. An increase in the base-emitter diode ideality factor, NF, resulted in an increase in the IMD3. This is to be expected, since a higher NF results in greater nonlinearity in the collector current. All the other GP parameters had a negligible impact on the intermodulation distortion.

5.3 Low I_C Bias Conditions

A similar sensitivity analysis was also done for a lower current bias. Figure 5.7-12 show the sensitivity for several parameters at a collector current of 25 mA with the same V_{CE} = 3.6 volts.

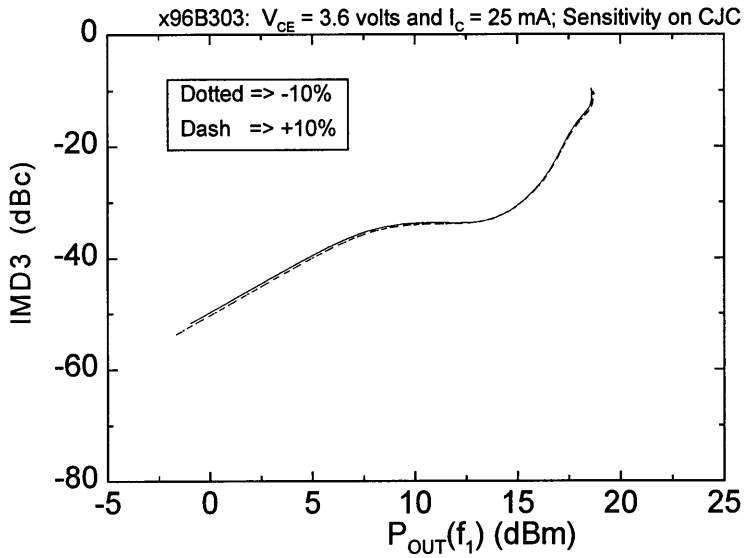


Figure 5.7: Sensitivity Analysis done for CJC, where CJC is increased (dashed) and decreased (dotted) by ten percent.

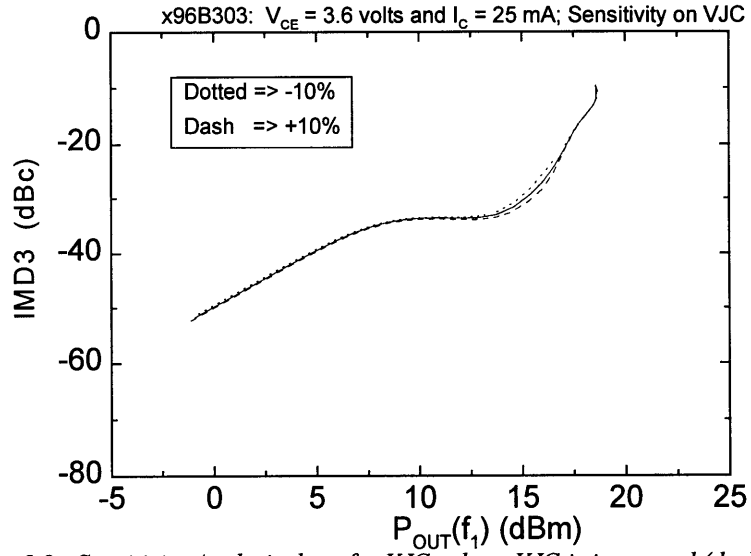


Figure 5.8: Sensitivity Analysis done for VJC, where VJC is increased (dashed) and decreased (dotted) by ten percent.

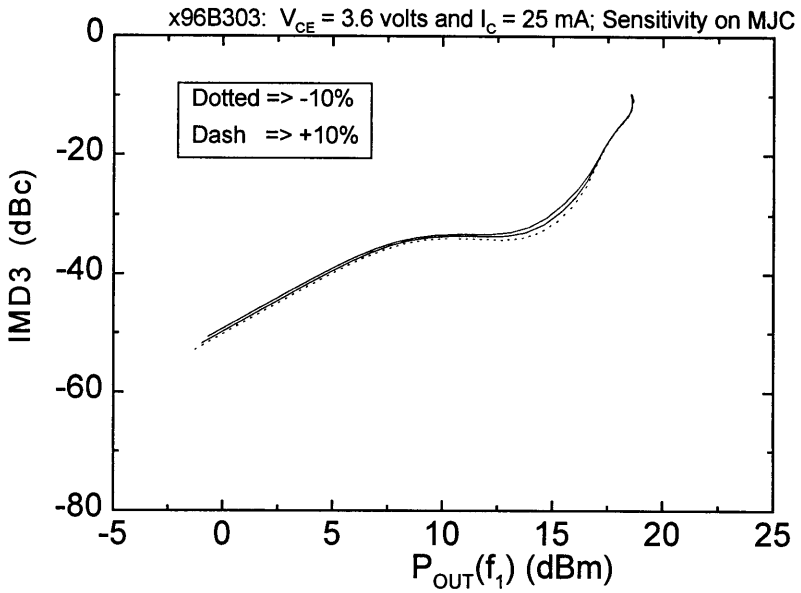


Figure 5.9: Sensitivity Analysis done for MJC, where MJC is increased (dashed) and decreased (dotted) by ten percent.

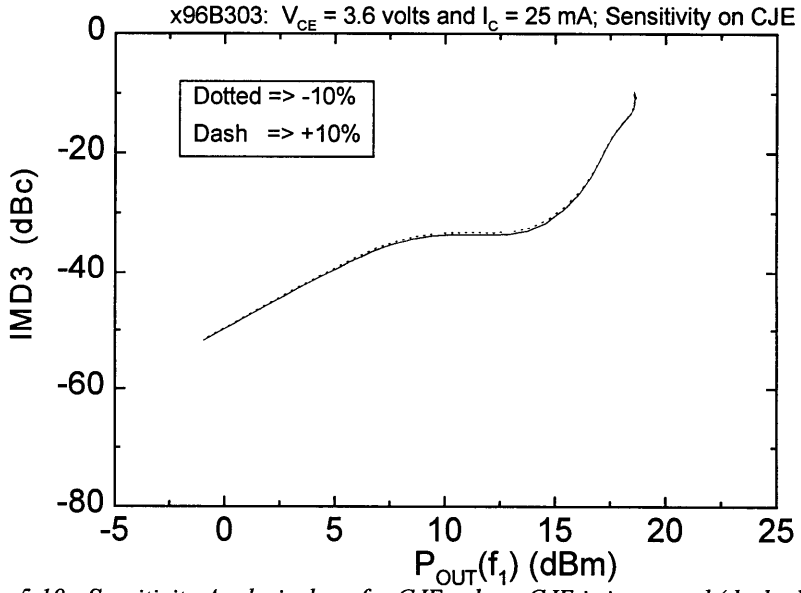


Figure 5.10: Sensitivity Analysis done for CJE, where CJE is increased (dashed) and decreased (dotted) by ten percent.

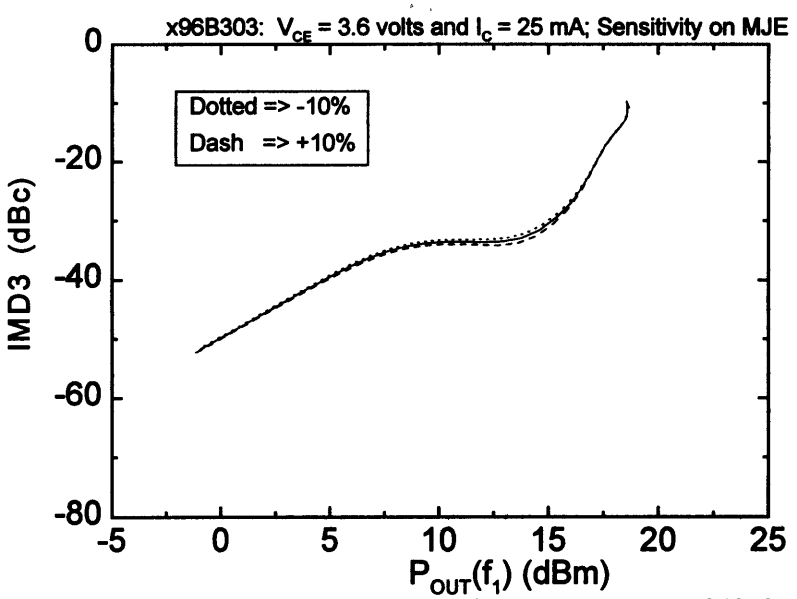


Figure 5.11: Sensitivity Analysis done for MJE, where MJE is increased (dashed) and decreased (dotted) by ten percent.

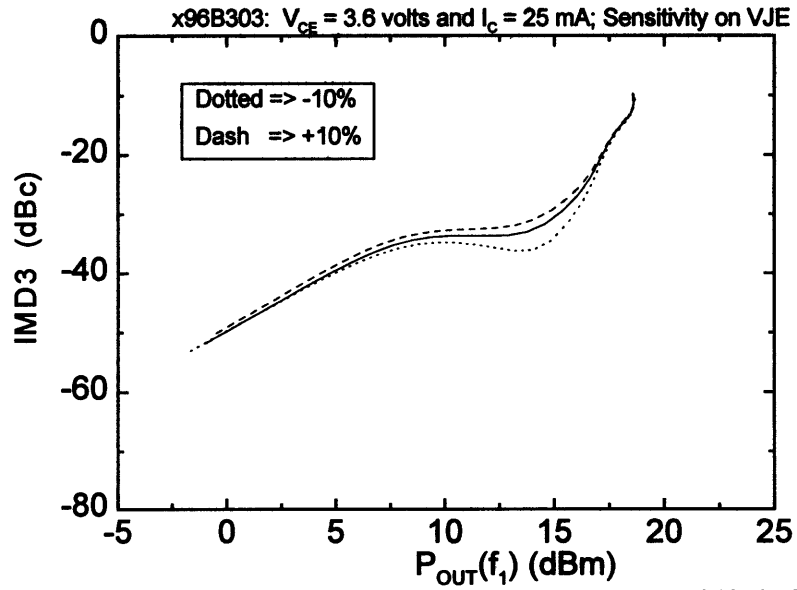


Figure 5.12: Sensitivity Analysis done for VJE, where VJE is increased (dashed) and decreased (dotted) by ten percent.

From these plots, it is seen that there is a difference between the high current and low current case in terms of which nonlinearities contribute most significantly to the overall nonlinearity of the device. It can be seen that variations in MJE and VJE contribute greatly to the overall nonlinearity, which implies that the nonlinearity of the base-emitter junction capacitance plays a significant role in the overall linearity of the device. The expression for this capacitance is:

$$C_{be} = \frac{CJE}{\left(1 - \frac{V_{BE}}{VJE}\right)^{MJE}} \qquad \text{[Equation 5.2]}$$

This equation is similar to the one for C_{bc}. As VJE increases C_{be} is less nonlinear with v_{BE} and as MJE increases, C_{be} is more nonlinear with VBE. From the simulation results it is seen that as MJE increases, the overall IMD3 decreases and as VJE increases, the overall IMD3 increases. This seems to imply that an increase in the nonlinearity of C_{be}, can result in an overall improvement in the nonlinearity of the device.

As in the high bias case, an increase in RE and NF resulted in an increase in IMD3. All other GP parameters had a negligible effect on IMD3.

5.4 Conclusions

In this chapter, simulations were used to examine the contribution that each of the GP parameters have on the overall intermodulation distortion of the device. It was found that for low collector currents, the base-emitter junction capacitance played a key role. At high collector currents, however, it was found that the base-emitter junction capacitance had a negligible effect, whereas the base-collector junction capacitance was more crucial. It was also found that shifts which would cause the nonlinearity in C_{be} to go up, actually caused the overall the nonlinearity to come down. This point will be examined analytically in the next chapter.

Chapter 6 - Analytical Derivations

6.1 Introduction

This chapter outlines a method for developing an analytical model for nonlinearity. The model is based on adding higher-level order Taylor series expansion terms to the traditional small-signal model. This approach has not been fully exploited and more work is clearly needed. Nevertheless, this might be a good starting point for a more detailed analysis of this kind in the future. The two main sources of nonlinearity in the low collector current biases are examined: the collector current (Icf) and the base to emitter capacitance (C_{BE}). Each of these nonlinearities are examined by linearizing all the components in the Gummel-Poon model except for the nonlinearity of interest. The linearization is done by creating a small-signal equivalent element representing the first-order Taylor series expansion of the nonlinear element based on where the device is biased. The Taylor Series expansions for the nonlinearity of interest must be carried out to the order which will produce the intermodulation being investigated.

6.2 Nonlinearity due to Collector Current

In order to have a manageable analytical model, we have simplified the GP model shown in Figure 2.2 as shown in Figure 6.1. Most of the parasitic resistances, inductances, and capacitances, as well as reverse injection currents have been removed since they affect linearity only to the second order.

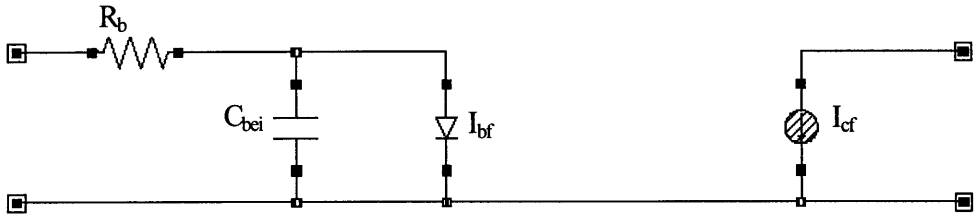


Figure 6.1: Simplification of the GP model for nonlinearity analysis.

The nonlinearity in the collector current is investigated by linearizing everything except the collector current component, as shown in Figure 6.2. The input to this circuit, $V_{in} = V_1 + V_2$. The total base voltage is simply $v_{BE} = V_{BE} + v_{be}$, where V_{BE} is the bias base-emitter voltage. The total collector current $i_C = I_C + i_c$, where I_C is the bias current and i_c is the small-signal current.

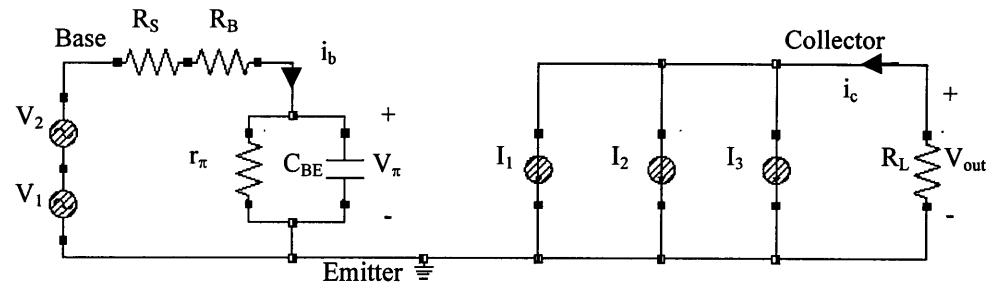


Figure 6.2: Linearized circuit for examining nonlinearity due to collector current.

C_{BE} and r_π is determined at the bias point which for high input power changes with power level. I_1, I_2, and I_3 are the first, second and third order Taylor series expansion of the I_C-V_{BE} relationship:

$$i_C = I_S \exp\left\{\frac{qv_{BE}}{V_T'}\right\} \approx I_C + I_1 + I_2 + I_3 \qquad \text{[Equation 6.1]}$$

with:

$$I_1 = g_m V_\pi \qquad \text{[Equation 6.2]}$$

$$I_2 = \frac{1}{2}\left(\frac{1}{V_T'}\right) g_m V_\pi^{\,2} \qquad \text{[Equation 6.3]}$$

$$I_3 = \frac{1}{6}\left(\frac{1}{V_T'}\right)^2 g_m V_\pi^{\,3} \qquad \text{[Equation 6.4]}$$

Typically only the I_1 term is included in a small-signal model. A third-order expansion is necessary to produce the third-order intermodulation in this case. The thermal voltage V_T = kT/q. k is Boltzmann's constant, T is the temperature, and q is the charge of an electron. V_T' is defined as $n_f V_T$. n_f is the diode ideality factor. V_π is the voltage across r_π and C_{be} as shown in Figure 6.2 and is related to V_{in} by:

$$V_\pi = \frac{r_\pi}{r_\pi + j\omega_1 C_{be}(R_S + R_B) r_\pi + R_S + R_B} V_{in} = F V_{in} \qquad \text{[Equation 6.5]}$$

The output voltage is given as:

$$\begin{aligned} V_{out} &= -R_L g_m i_c \\ &= -R_L g_m \left[V_\pi + \tfrac{1}{2}\left(\tfrac{1}{V_T'}\right) V_\pi^2 + \tfrac{1}{6}\left(\tfrac{1}{V_T'}\right)^2 V_\pi^3 \right] \\ &= B\left[V_{in} + C V_{in}^2 + D V_{in}^3 \right] \end{aligned} \qquad \text{[Equation 6.6]}$$

Several variables are also defined below to simplify the expressions:

$$B = -R_L g_m F \qquad \text{[Equation 6.7]}$$

$$C = \tfrac{1}{2}\left(\tfrac{1}{V_T}\right)F \qquad \text{[Equation 6.8]}$$

$$D = \tfrac{1}{6}\left(\tfrac{1}{V_T}\right)^2 F^2 \qquad \text{[Equation 6.9]}$$

For a two-tone input, the input voltage is $V_{in} = A\cos(\omega_1 t) + A\cos(\omega_2 t)$. The amplitude A is determined by the desired input power. By plugging in the expression for V_{in} into Equation 6.8, and employing some trigonometric identities, one can derive V_{out} at several frequencies, including $\omega=(2\omega_1-\omega_2)$ and $\omega=(2\omega_2-\omega_1)$. The output voltage amplitude at all the frequencies is listed in Table 6.1.

Frequency	V_{out} Amplitude
DC	BCA^2
ω_1, ω_2	$(9/4)BDA^3 + BA$
$2\omega_1$, $2\omega_2$	$(1/2)BCA^2$
$\omega_1-\omega_2$, $\omega_1+\omega_2$	BCA^2
$3\omega_1$, $3\omega_2$	$(1/4)BDA^3$
$2\omega_1+\omega_2$, $2\omega_2+\omega_1$, $2\omega_1-\omega_2$, $2\omega_2-\omega_1$	$(3/4)BDA^3$

Table 6.1: V_{out} at several frequencies.

From the information in Table 6.1, the ratio of the amplitude of the output voltage signal at $\omega = 2\omega_1 - \omega_2$ to the output voltage at ω_1 can be formulated as:

$$\frac{V_{out}(2\omega_1-\omega_2)}{V_{out}(\omega_1)} = \left(\frac{\tfrac{3}{4}DA^2}{\tfrac{9}{4}DA^2+1}\right) \qquad \text{[Equation 6.10]}$$

The intermodulation distortion, IMD3 is given by:

$$IMD3 = 10\log_{10}\left|\frac{V_{out}(2\omega_1-\omega_2)}{V_{out}(\omega_1)}\right|^2 \qquad \text{[Equation 6.11]}$$

Figure 6.3 shows this modeled IMD3 compared to simulation results.

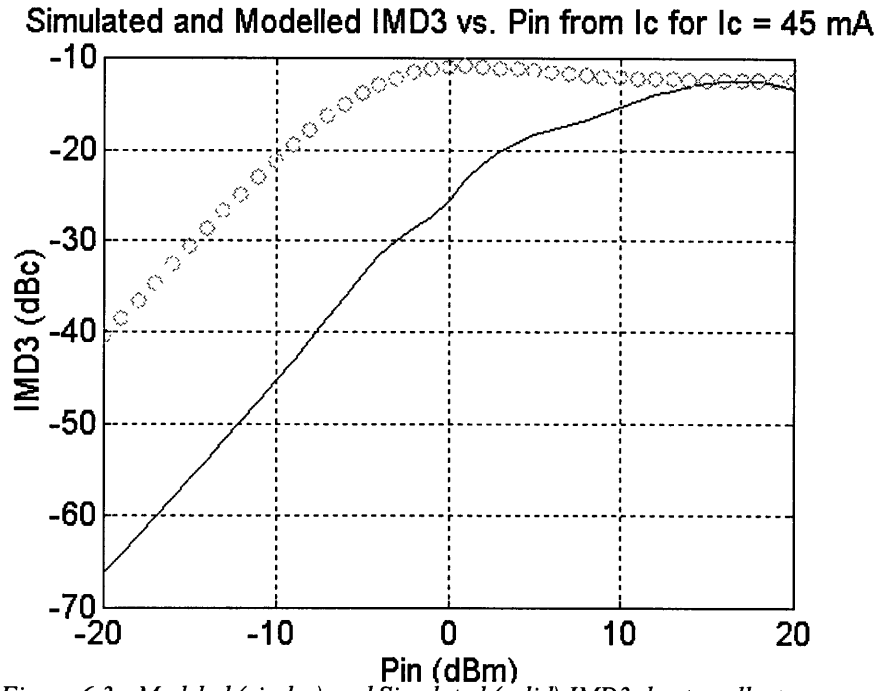


Figure 6.3: Modeled (circles) and Simulated (solid) IMD3 due to collector current.

It is clear that the intermodulation due to the collector current is significantly greater than the over all intermodulation of the device for low P_{IN}. The saturation value of IMD3 at high P_{in} appears to be correctly modeled.

6.3 Nonlinearity due to C_{be}

A similar derivation for the C_{be} nonlinearity is performed using the circuit of Figure 6.4. In this circuit, everything is linearized except for C_{be}, which will be Taylor expanded. Three terms in the expansion will be used to obtain the third-order intermodulation terms. If we denote C_{bias_be} as the base to emitter capacitance at the bias, the Taylor expansion of C_{be} can be written as:

$$C_{be} = C_{bias\_be}\left[1 + \frac{MJE}{VJE - V_{BE}} V_\pi - \frac{MJE(MJE-1)}{2(VJE-V_{BE})^2} V_\pi^2\right] \qquad \text{[Equation 6.12]}$$
$$= C_{bias\_be}\left[1 + (MJE)JFV_{in} - \frac{MJE(MJE-1)}{2} J^2F^2V_{in}^2\right]$$

where Equation 6.5 has been used.

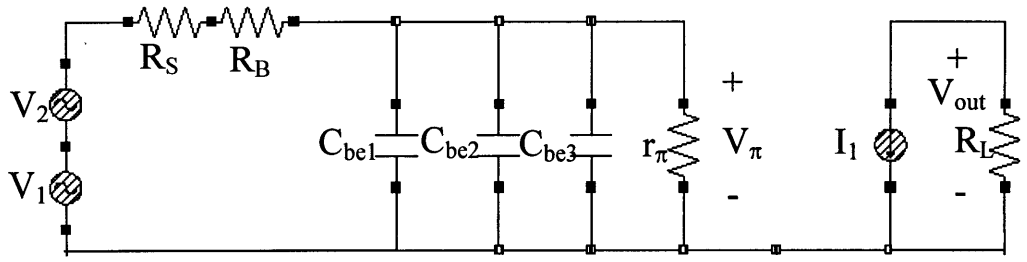


Figure 6.4: Linearized circuit for examining nonlinearity due to base-emitter capacitance.

To simplify the notation, we define:

$$J = \frac{1}{VJE - V_{BE}} \qquad \text{[Equation 6.13]}$$

$$K = \frac{1}{\left(R_S + R_b + r_\pi\right)^2 + \omega^2 C_{bias\_be}^2 \left(R_S + R_b\right)^2 r_\pi^2} \qquad \text{[Equation 6.14]}$$

$$M = R_L g_m \left[j\omega C_{bias\_be} K (R_S + R_b) r_\pi^2 - K\left(R_S + R_b + r_\pi\right) r_\pi \right] \qquad \text{[Equation 6.15]}$$

$$N = j\omega R_L g_m C_{bias\_be} K\left(R_S + R_b\right) r_\pi^2 \left(MJE\right) JF \qquad \text{[Equation 6.16]}$$

$$P = j\omega R_L g_m C_{bias\_be} K\left(R_S + R_b\right) r_\pi^2 \frac{(MJE)(MJE+1)}{2} J^2 F^2 \qquad \text{[Equation 6.17]}$$

The output voltage, V_{out} at different frequencies is listed in Table 6.2.

Frequency	V_{OUT} Amplitude
DC	NA^2
ω_1, ω_2	$(9/4)PA^3 + MA$
$2\omega_1$, $2\omega_2$	$(1/2)NA^2$
ω_1-ω_2, ω_1+ω_2	NA^2
$3\omega_1$, $3\omega_2$	$(1/4)PA^3$
$2\omega_1$+ω_2, $2\omega_2$+ω_1, $2\omega_1$-ω_2, $2\omega_2$-ω_1	$(3/4)PA^3$

Table 6.2: V_{OUT} at several frequencies.

From the data in Table 6.2, the expression for IMD3 is shown as:

$$\frac{V_{out}(2\omega_1 - \omega_2)}{V_{out}(\omega_1)} = \left(\frac{\frac{3}{4}PA^2}{\frac{9}{4}PA^2 + M}\right) \qquad \text{[Equation 6.18]}$$

$$IMD3 = 10\log_{10}\left|\frac{V_{out}(2\omega_1-\omega_2)}{V_{out}(\omega_1)}\right|^2 \qquad \text{[Equation 6.19]}$$

The result of this equation is plotted with simulation data as shown in figure 6.5.

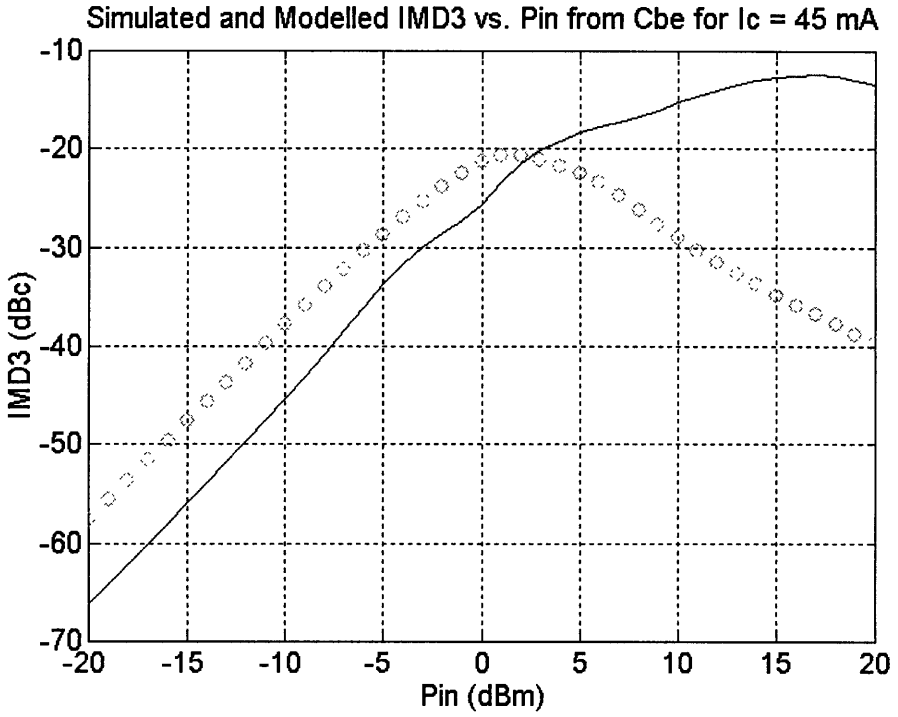


Figure 6.5: Modeled (circles) and Simulated (solid) IMD3 due to C_{BE}.

6.4 Nonlinearity due I_C, and C_{BE}

This section will combine the nonlinearity from the collector current and base to emitter junction capacitance. If the device is relatively linear, the combined V_{out} at ω_1 and at $2\omega_1$-ω_2 are:

$$V_{out}(\omega_1) = \frac{3}{4}BDA^3 + BA + \frac{3}{4}PA^3 \qquad \text{[Equation 6.20]}$$

$$V_{out}(2\omega_1 - \omega_2) = \tfrac{3}{4} BDA^3 + \tfrac{3}{4} PA^3 \qquad \text{[Equation 6.21]}$$

$$\frac{V_{out}(2\omega_1 - \omega_2)}{V_{out}(\omega_1)} = \left(\frac{\tfrac{3}{4} BDA^3 + \tfrac{3}{4} PA^3}{\tfrac{9}{4} BDA^3 + BA + \tfrac{9}{4} PA^3} \right) \qquad \text{[Equation 6.22]}$$

$$IMD3 = 10 \log_{10} \left| \frac{V_{out}(2\omega_1 - \omega_2)}{V_{out}(\omega_1)} \right|^2 \qquad \text{[Equation 6.23]}$$

The result of the model after combining the collector current nonlinearity and base-emitter capacitance nonlinearity is shown as Figure 6.6. It is clear that more work is needed in this model.

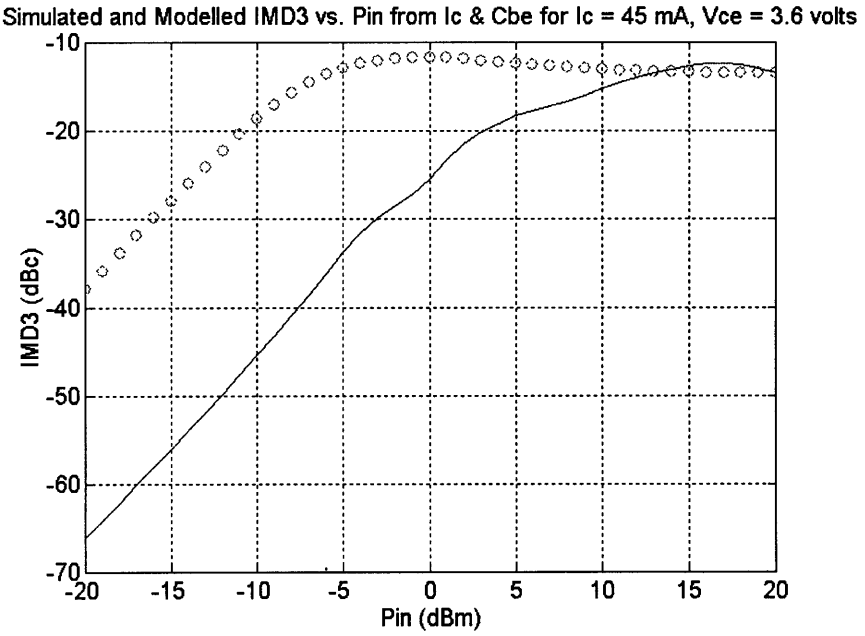


Figure 6.6: Modeled (circles) and Simulated (solid) IMD3 due to C_{BE} and I_C.

6.5 Conclusions

In this chapter, a method for developing an analytical model for IMD3 has been outlined. The intermodulation distortion arising from the collector current nonlinearity and the base-emitter junction capacitance nonlinearity have been examined. The nonlinearities were examined by simplifying the GP model and then linearizing all the GP components by doing a first order Taylor series expansion except the nonlinearity to be examined. The nonlinearity to be examined was expanded to the order which would produce third order intermodulation products. The IMD3 from this analysis overshot the actual IMD3. This may be due to not including the nonlinearities arising from the base-emitter diode

and the base-collector junction capacitance. The model may be improved further by including these other sources of nonlinearity. The next chapter will present the conclusions of this thesis.

Chapter 7 – Conclusions

During the course of the thesis, a discussion of three single-tone figures of merit (P_{OUT}, PAE, and Gain) and one two-tone figure of merit (IMD3) was presented. Simulation and measurement results of these figures of merit were compared to validate the simulation environment. Next the simulation environment was used to conduct load and source pulls to optimize the load and source impedances. A simulation sensitivity analysis was carried out and discussed. Finally, an analytical model for determining IMD3 figure of merit from the two largest sources of nonlinearity was presented.

The one-tone, two-tone, and s-parameter measurements were carried out at Raytheon and the DC measurements of the devices were carried out at MIT. The DC Gummel plot of measured and simulated data showed good correlation as did the s-parameter data well in excess of 2 GHz, which is beyond the application range of these devices. The one-tone and two-tone measurements and simulations were also found to be in excellent agreement. Both of these simulations were tested extensively, across a wide range of biases and load impedances and proved to be quite robust. This was not only served as a verification of the GP model parameters that were extracted by Raytheon based on s-parameter and DC data, but also served as a validation for the HP-Libra HB simulation environment. Since the simulation environment was so robust, it is appropriate to conduct load and source pull simulations to optimize the load and source impedances.

Both single-tone and two-tone load pull simulations were conducted in addition to a single-tone source pull simulation. To effectively choose a proper load and source one must consider the input and output stability circles which had also been presented for these devices at several bias conditions. The final optimized load reflection coefficient was found to be $\Gamma_L(f_o) = 0.356 \angle 150.6°$ and the optimized source reflection coefficient was found to be $\Gamma_S(f_o) = 0.569 \angle 156.6°$. This yielded very good results near the 1 dB gain compression point. The P_{OUT} was found to be 19 dBm with a G of 19 dB and a PAE of 33%. The IMD3 was –26 dBc which is below the –25 dBc specification for typical applications.

The sensitivity was totally carried out in the HP-Libra simulation environment using the single-tone and the two-tone test benches. The results seemed to indicate that the base to collector junction capacitance (C_{BC}) played a significant role in the nonlinearity of the HBTs in high collector current bias conditions and the base to emitter junction capacitance (C_{BE}) played a significant role in the low collector current bias conditions. It also demonstrated that the nonlinearity due to C_{BE} is actually out of phase with the other nonlinearities. This is manifested by the fact that steps taken to increase the nonlinearity of C_{BE} actually results in a decrease in the overall intermodulation distortion of the HBT PA. This is not the case for C_{BC} nonlinearities. Increasing the nonlinearity of C_{BC} results in an increase in the overall nonlinearity of the device. This finding has verified previous claims of nonlinearity cancellation for C_{BE}.

An analytical model of IMD3 in HBT PAs have been developed by only examining the major sources of nonlinearity in the low collector current biases: collector current and base to emitter junction capacitance. This analytical model has been predicting IMD3 which overshoots the actual IMD3. The accuracy of the model could be improved by adding other nonlinearities to the analysis, namely the base to collector junction capacitance and the base to emitter diode.

Future work should concentrate of incorporating other nonlinearities in the analytical model already developed, especially I_{bf} and C_{BC}. This would likely enhance the performance of the model especially at higher collector current bias conditions. Also load and source pulls for optimizing load and source impedances at the harmonics of the fundamental frequency may lead to enhanced PA performance. This should be investigated.

References

Chapter 1

[1.1] T. Yoshimasu, High Power AlGaAs/GaAs HBTs and Their Application to Mobile Communications Systems, IEDM, pp. 787-789, 1995

[1.2] RF Micro Devices Inc., A High Efficiency HBT Analog Cellular Power Amplifier, Microwave Journal, January, 1996, pp. 168-172

[1.3] A. G. Milnes, Semiconductor Heterojunction Topics: Introduction and Overview, Solid-State Electronics, Vol. 29, No. 2, pp.99-121, 1986

[1.4] B. Bayraktaroglu, GaAs HBT's for Microwave Integratred Circuits, Proc. of the IEEE, Vol. 81, No. 12, pp. 1762-1784, December, 1993

[1.5] D. Wu, A High-Efficiency HBT Cellular Power Amplifier with Integrated Matching Networks, IEEE MTT-S International Microwave Symposium Digest, pp.767-770, 1996

[1.6] G. Gonzalez, Microwave Transistor Amplifiers Analysis and Design, Prentice-Hall Inc., Englewood Cliffs, NJ, 1984

[1.7] N. Wang, et al., 7.5-14 GHz CE HBT MMIC Linear Power Amplifier, IEEE Microwave and Guided Wave Letters, Vol. 3, No. 3, pp. 64-66, March, 1993

[1.8] G. O. Ladd Jr., D. L. Feucht, Performance Potential of High-Frequency Heterojunction Transistors, IEEE Transactions on Electron Devices, Vol. 17, No. 5, pp. 413-420, May, 1970

[1.9] P. M. Asbeck, Bipolar Transistors, High-Speed Semiconductor Devices, Edited by S. M. Sze, John Wiley & Sons, Inc., 1990

[1.10] O. Woywode, B. Pejcinovic, Nonlinear Second Order Current Cancellation in HBTs, Solid State Electronics, Vol. 41, No. 9, pp. 1321-1328, 1997

Chapter 2

[2.1] M. E. Hafizi, C. R. Crowell, M. E. Grupen, The DC Characteristics of GaAs/AlGaAs Heterojunction Bipolar Transistors with Application to Device Modeling, IEEE Transactions on Electron Devices, Vol. 37, No. 10, pp. 2121-2129, October, 1990

[2.2] D. A. Teeter, J. R. East, R. K. Mains, G. I. Haddad, Large-Signal Numerical and Analytical HBT Models, IEEE Transactions on Electron Devices, Vol. 40, No. 5, pp. 837-845, May, 1993

[2.3] Hewlett Packard, Advanced Bipolar Transistor Modeling Techniques, July, 1991

[2.4] K. S. Kundert, J. K. White, A. Sangiovanni-Vincentelli, Steady-State Methods for Simulating Analog and Microwave Circuits, Kulwar Academic Publishers, Boston, 1990

Chapter 3

[3.1] Hewlett Packard, Operation Manual - HP4145 Semiconductor Parameter Analyzer, April 1989

Chapter 4

[4.1] F. N. Sechi, Design Procedure for High-Efficiency Linear Microwave Power Amplifiers, IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-28, No. 11, pp. 1157-1163, November 1980

[4.2] K. Chang, Microwave Solid-State Circuits and Applications, John Wiley & Sons, Inc., New York, 1994

Chapter 6

[6.1] M. E. Hafizi, C. R. Crowell, M. E. Grupen, The DC Characteristics of GaAs/AlGaAs Heterojunction Bipolar Transistors with Application to Device Modeling, IEEE Transactions on Electron Devices, Vol. 37, No. 10, pp. 2121-2129, October, 1990