Hot-Carrier Reliability Assessment in CMOS Digital Integrated Circuits

by

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Abstract

As VLSI technologies scale to deep submicron region, the DC device-based hot-carrier criterion is no longer practical for predicting hot-carrier reliability. Understanding the AC hot-carrier degradation of MOSFETs in actual circuit environment and their corresponding impact on circuit performance becomes increasingly important. The purpose of this research is to contribute to the assessment of hot-carrier reliability in digital CMOS circuits. Several critical issues that face circuit-level hot-carrier reliability evaluation are investigated, including AC hot-carrier test circuit design and characterization, AC hot-carrier degradation model calibration, the major factors determining circuit-level hot-carrier reliability, and the trade-offs between circuit-level hot-carrier lifetime underestimation and the amount of information required.

In the area of experimental assessment of AC hot-carrier reliability, this thesis provides a comprehensive understanding of the key issues in designing and characterizing hot-carrier reliability test circuits. Test circuits that can provide realistic stress voltage waveforms, allow access to the internal device nodes, and provide insight about circuit performance sensitivity to hot-carrier damage are presented. New insights about previous test circuit designs are presented and additional test circuit designs are demonstrated. The design trade-offs between realistic waveform generation and internal device accessibility are analyzed and clarified. Recommendations for optimal test-circuit design for hot-carrier reliability characterization and model calibration are proposed.

In the area of circuit-level hot-carrier reliability simulation, this thesis examines key issues involved in the calibration and verification of the hot-carrier degradation models that are used for AC hot-carrier reliability simulation. The need to account for the stress oxide-field dependence of the degradation model coefficients is demonstrated. The statistical confidence limits of the extracted degradation model parameters are analyzed. The sensitivity of degradation to drain and substrate current modeling errors is examined. Base on these results, the AC degradation model's statistical confidence limits are evaluated, and the accuracy and precision of AC hot-carrier reliability simulation is rigorously benchmarked against a comprehensive set of experimental AC circuit measurements. It is shown that statistical variation in the degradation model parameters has as much of an impact on the final degradation model accuracy as major changes in the

circuit-design itself. In addition, knowledge about CMOS digital circuit behavior is shown to be useful in optimizing the calibration of both the degradation and SPICE model parameters. Specific recommendations are made about improving the consistency and accuracy of both degradation and SPICE model parameter extraction.

Finally, the major factors that cumulatively contribute to circuit-level hot-carrier reliability are identified. The inherent inverse relationship between lifetime-underestimation/criteria-overspecification and the amount of known device/circuit information are explored. Lifetime-underestimation/criteria-overspecification are shown to depend quite strongly on the particular "worst-case" approximations used. Each of the above concepts are illustrated using representative circuit examples and case studies.

Thesis Supervisor: James E. Chung
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To My Family

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Chapter 1

Introduction

1.1 Overview

The semiconductor and computer industries have made great progress in the last three decades. Discrete MOS devices have been merged into integrated circuits. Integrated circuits have gradually incorporated more and more functions on each chip. Today, it is possible to put an entire mainframe computer on a single piece of silicon. This tremendous growth is directly attributable to the scalability of the silicon MOS transistor to ULSI dimensions.

With the continued scaling of device dimensions, the power-supply voltage should be reduced according to constant-electric field scaling principles [1.1]. This would enable the reduction of power dissipation and maintain relatively constant internal MOSFET electric fields. However, circuit-speed reduction would then become significant due to the increasing non-scalability of parasitic capacitances for device dimensions below 1 μm; the low signal-to-noise margin would also become increasingly unacceptable due to the non-scalability of the MOSFET threshold voltage and subthreshold slope. In addition, a higher power-supply voltage is desirable for reasons of better tolerance to process variation and compatibility with former process generations. For these reasons, a non-constant field-scaling methodology is used in practice. As a result, the internal electric fields within devices tend to increase with scaling since the operational voltage is only scaled down marginally.

The most important electric fields in MOS devices are the transversal fields in the gate insulator and the lateral field in the channel. The high lateral-electric field generates energetic carriers near the drain region of the MOSFET when the device is biased under saturation conditions. Under the influence of this high lateral field, mobile carriers in the channel gain sufficient energy such that the effective temperature of these carriers is much higher than that of the lattice temperature; these highly energetic carriers are referred to as "hot" carriers.

Hot-carriers may induce a number of performance and long-term reliability problems [1.1]-[1.5]. Hot-carrier-induced impact-ionization produces substrate current that can lead to latch-up in CMOS structures [1.6]-[1.7]. Also, the MOSFET parasitic bipolar transistor can turn on, if excess current in the substrate creates a large enough potential drop over the distributed substrate resistance. The above problems usually occur abruptly and may induce unwanted drastic changes in the device characteristics.

Hot-carriers may also generate damage in the gate oxide [1.8]-[1.17], which can permanently change device characteristics. This oxide damage is caused by the injection of highly energetic electrons and holes from the channel into gate-oxide region. This results in the generation of electron and/or hole traps in the oxide, electrically active states at the $Si-SiO_2$ interface, and gate current. The oxide and interface damage induces gradual changes in key MOSFET parameters such as the drain current, threshold voltage and transconductance. These changes in device characteristics can lead to long-term circuit performance degradation or malfunction.

In order to minimize hot-carrier degradation problems, a number of technological solutions have been proposed. Lightly-Doped-Drain (LDD), Double-Diffused-Drain (DDD) as well as Phosphorus-Drain (PD) MOSFET structures have been developed to

lower the drain-side lateral-electric field and thus reduce the number of hot-carriers [1.18]-[1.22]. Nitrided or fluorinated gate oxides have also been introduced to improve the gate-dielectric robustness against hot-carrier-induced damage [1.23]-[1.24]. However, each of these technological reliability improvements introduces greater process complexity and less ease-of-scalability for a process. It becomes more and more difficult to implement these processes in future technology generations.

Improving reliability, in general, requires some form of performance sacrifice. In choosing a particular device structure and circuit design, it is necessary to optimize between performance and reliability. Since there is no longer the luxury of maintaining such wide reliability margins as had previously existed, it is increasingly important that improved understanding, more quantitative modeling, and better analysis be utilized to insure that the required circuit reliability exists under field-operation conditions, while at the same time, maximum possible circuit performance is enabled.

1.2 Motivation

Traditional hot-carrier criteria have been based on DC device performance degradation, such as a 10% drain current change or a 10mV threshold voltage shift. However, as technology scales, this type of reliability criteria is no longer practical; it poses a very stringent limit on device scaling and it comes at the cost of increasingly complex processes and sacrificed performance. In addition, DC device hot-carrier criteria are very ambiguous because it is not clear which device parameter is the most appropriate parameter for determining the hot-carrier reliability criteria. Furthermore, the amount of device parameter change that is used as the definition of lifetime criteria (such as 10% current degradation, etc.) is often quite arbitrary. It is not obvious how this particular

amount of device degradation actually impacts circuit performance since the design and operating conditions of a given circuit are as important in determining overall hot-carrier reliability as is the degradation of the particular device itself. Thus, understanding the AC hot-carrier degradation of MOSFETs in the actual circuit environment and their corresponding impact on circuit performance becomes very important.

Different approaches can be used to assess circuit-level hot-carrier reliability. One approach is to characterize hot-carrier reliability by testing final products. In order to observe the impact of hot-carrier-induced device degradation on circuit performance within a reasonable amount of time, a significantly higher than operational voltage often has to be applied to accelerate the product degradation. This reliability evaluation process is destructive, time consuming and costly. If the reliability of the final product is found to be unsatisfactory, then the entire development process must be repeated.

An alternative approach is to predict hot-carrier reliability in the early design- and technology-development phase using reliability simulation. This eliminates costly iteration through the overall product development process, although there will still be some overhead required in the early stages of the process and circuit development. Thus, accurate and precise simulation of hot-carrier reliability is essential. The precision and accuracy of hot-carrier reliability simulation depends on the following issues: 1) the validity of the DC hot-carrier degradation model under AC conditions; 2) the accuracy of the simulated device degradation over the time period of interest; 3) the accuracy of the simulated impact of device degradation on circuit performance.

To understand the first issue, this thesis will examine key issues involved in the calibration and verification of the hot-carrier degradation models used for simulating AC circuit-level reliability. Test-circuits will be designed and optimized for reliability

evaluation. Experimental AC hot-carrier degradation results will be compared to reliability simulation results. The AC degradation model will be improved to account for the oxide-field dependence of the degradation model parameters.

To understand the second and third issues, the major factors that cumulatively determine circuit-level hot-carrier reliability will be explored. The relative importance of each factor on circuit reliability will be examined. The inherent inverse relationship between lifetime-underestimation and the amount of known device/circuit information will be discussed.

1.3 Outline of the Thesis

The outline of this thesis is described as follows. Chapter 2 reviews the major hot-carrier degradation models and degradation mechanisms for both NMOS and PMOS transistors. It also reviews the impact of hot-carrier-induced degradation on circuit performance.

Chapter 3 concentrates on hot-carrier reliability test-circuit design and optimization. These test circuits can provide realistic stress-voltage waveforms. They can also provide access to the internal device nodes; therefore the fresh and degraded device I-V characteristics can be individually measured and the AC hot-carrier degradation of devices can be directly related to the corresponding circuit-performance degradation. New insights about previous test circuit designs are presented and additional new test-circuit designs are demonstrated. The design trade-offs between realistic waveform generation and internal device accessibility are explored. Optimized test-circuit design for hot-carrier reliability characterization and model calibration are proposed.

Chapter 4 addresses key issues involved in the calibration of the hot-carrier degradation models that are used for simulating AC circuit-level reliability. First, the oxide-field dependence of the degradation model coefficients extracted from DC device-level stress measurements are shown to have significant impact on the accuracy of hot-carrier degradation prediction, particularly when devices experience a wide range of bias conditions. Second, the statistical confidence limits of the extracted degradation model parameters are analyzed. Third, the sensitivity of degradation to drain- and substrate-current modeling errors is examined. Specific recommendations are made about improving the consistency and accuracy of both degradation- and SPICE-model parameter extraction.

In Chapter 5, the AC hot-carrier simulation models are calibrated using DC stress data. The calibrated simulation results are compared against experimental data obtained from AC test circuits for two representative industrial technologies. The impact of the degradation model's statistical confidence limits on AC hot-carrier degradation prediction is evaluated. Statistical variation in the degradation model parameters is observed to have as much of an impact on the final degradation model accuracy as major changes in the circuit-design itself. Finally, it is demonstrated that knowledge about CMOS digital-circuit behavior is useful in optimizing the calibration of both the degradation- and SPICE-model parameters.

In Chapter 6, the major factors that determine circuit-level hot-carrier reliability are identified. These factors are the following: 1) Hot-Carrier Degradation Model Precision and Accuracy; 2) The Specific MOSFET Terminal Voltage Waveforms; 3) MOSFET Switching Activity; 4) Circuit Performance Sensitivity to Device Degradation;

5) Relative Importance of the Degraded Circuit Path. Each factor is illustrated and its relative importance is analyzed.

Chapter 7 attempts to define different-levels of approximations for circuit reliability evaluation based on the amount of known information about the circuit. The relationship between lifetime-underestimation and the amount of known device/circuit information is explored. The circuit lifetime-underestimation is shown to depend quite strongly on the particular "worst-case" approximations used. These concepts are illustrated using a digital-circuit case study.

Chapter 8 summarizes the research results of this thesis and proposes future work.

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Chapter 2

Overview of Hot-Carrier-Induced Degradation

When a MOSFET is biased in the saturation region, a high lateral-electric field exists which peaks near the drain [2.1]. The channel carriers passing through this high-field region get accelerated to considerably higher energy than the thermal energy of the surrounding lattice and are labeled as "hot" carriers. Some of these hot-carriers can create electron-hole pairs through impact ionization. Others can acquire sufficient energy to overcome the Si - SiO$_2$ barrier height and get injected into gate oxide [2.2]-[2.10].

Figure 2.1 illustrates these hot-carrier effects for an NMOSFET, as well as the corresponding lateral channel-electric field. The injection of hot-carriers into the gate oxide is responsible for various types of oxide damage such as interface states, electron and/or hole traps. This long-term damage of the Si - SiO$_2$ interface and gate oxide leads to degradation in MOSFET device performance.

There has been a tremendous effort to understand hot-carrier degradation mechanisms and to develop models for evaluating hot-carrier reliability in MOSFETs [2.10]-[2.12]. Since all hot-carrier effects have a common driving force, the lateral-electric field in the channel, the more easily-measurable hot-carrier effects can be used as a monitor to predict other, more difficult to measure, hot-carrier effects. For example, both hot-carrier-generated substrate and gate currents can be correlated to the amount of resulting hot-carrier oxide damage. The substrate current can be used as a monitor for

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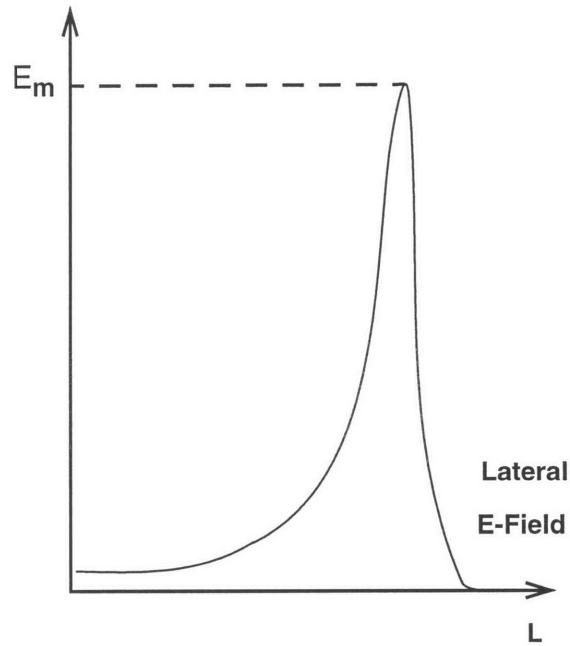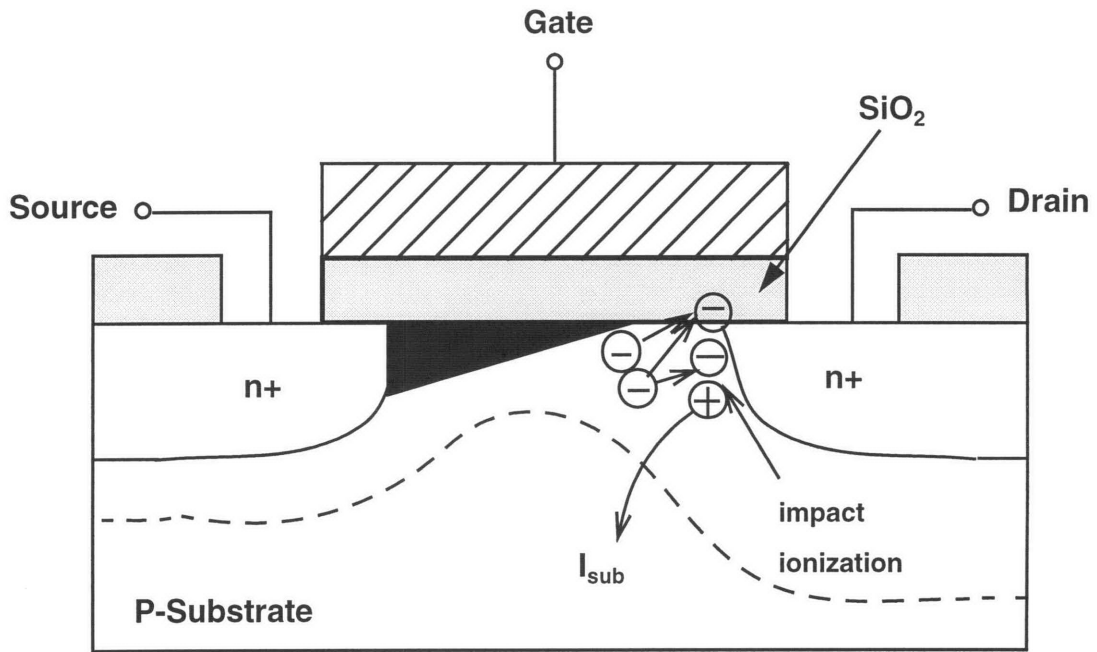
Figure 2.1   Illustration of hot-carrier generation in an NMOSFET and the lateral electric field in the channel.

NMOSFET oxide degradation and gate current can be used as a monitor for PMOSFET oxide degradation.

In this section, the most commonly-used NMOS and PMOS degradation models will be reviewed. The impact of hot-carrier degradation on device and circuit performance will be also illustrated.

2.1 NMOS Hot-Carrier Degradation Model

In NMOSFETs, the most important degradation mechanism is acceptor-type interface state generation [2.1]. Under DC stress conditions, NMOS degradation reaches a maximum at peak-substrate-current stress-bias conditions, when the gate-to-source stress voltage is about one third of the drain-to-source stress voltage ($V_{gs} \sim 1/3\ V_{ds}$). These acceptor-type interface states are neutral when empty and negatively charged when occupied, resulting in a threshold-voltage increase and a mobility decrease for an NMOSFET.

Besides interface-state generation, electron and/or hole trapping may also occur, depending on the applied stress-bias conditions. When the gate-to-source stress voltage is near the threshold voltage ($V_{gs} \sim V_t$) and the drain-to-source voltage is large, positive-charge generation (hole trapping) is observed [2.9]. This positive charge in the gate oxide reduces the local threshold voltage near the drain, thus slightly enhancing the NMOSFET current-drive capability. Therefore, hole trapping is typically not considered a major NMOS device reliability problem.

When the gate-to-source stress voltage is about the same as the drain-to-source stress voltage ($V_{gs} \sim V_{ds}$), negative-charge generation (electron trapping) dominates device degradation [2.10]. Although this negative charge trapping reduces the current

drive, the magnitude of this oxide damage mechanism is typically much less than that of interface-state generation.

Interface-state generation is the dominant degradation mechanism for NMOSFETs. The hot-electron-induced interface-state generation can be modeled as a function of the lateral-electric field [2.1],

$$\Delta N_{it} \propto \left(\frac{I_D}{W} \bullet e^{-\Phi_{it}/(q\lambda E_m)} \bullet t \right)^n \qquad (1)$$

where ΔN_{it} is interface state density, I_D is the drain current, W is the width of the device, Φ_{it} is the critical energy for interface-state generation, λ is the electron mean free path, E_m is the peak lateral-electric field, and n is the degradation rate.

Since it is difficult to measure directly the maximum lateral-electric field E_m, a degradation model with more directly measurable quantities is preferred. The hot-electron-induced substrate current can be used as a monitor of E_m. Substrate current can be modeled by the following relation[2.13]:

$$I_{SUB} \propto I_D \bullet e^{-\Phi_i/(q\lambda E_m)} \qquad (2.1)$$

where Φ_i is the critical energy for impact ionization. By eliminating E_m from the above two equations, the most commonly used DC NMOS degradation model can be derived [2.1]:

$$\Delta N_{it} = \left(\frac{I_D}{W \bullet H} \bullet \left(\frac{I_{SUB}}{I_D} \right)^m \bullet t \right)^n \qquad (2.2)$$

where $m = \Phi_{it}/\Phi_i$ and H is a technology dependent constant. The hot-carrier-generated interface-state density ΔN_{it} is found to be proportional to such common matrix for device

reliability as the percentage change in drain current $(\Delta I_d / I_d)$, the percentage change in transconductance $(\Delta g_m / g_m)$, as well as the threshold-voltage shift (ΔV_t).

2.2 PMOS Hot-Carrier Degradation Model

Compared to NMOSFETs, PMOSFET hot-carrier degradation is typically perceived to be less of problem. This is because fewer hot-carriers are generated due to the shorter mean-free path and higher oxide barrier for holes in PMOSFETs. It is generally believed that electron trapping in the gate oxide is responsible for most PMOSFET hot-carrier degradation. Electron trapping results in a shortening of the effective channel length, which leads to an increase in drain current. This electron trapping also results in a threshold-voltage decrease and a subthreshold-leakage-current increase, which has been identified as a performance-limiting factor for PMOSFETs in the submicron and deep-submicron region.

For PMOSFETs, device degradation reaches a maximum at peak gate-current stress conditions, whereas for NMOSFETs, it occurs at peak substrate-current stress conditions. The PMOSFET hot-carrier degradation models that have been reported [2.8], [2.14]-[2.18] can be divided into two major types.

Certain PMOSFET hot-carrier degradation models are based on gate current [2.15]:

$$\Delta = \left(A_g \cdot \frac{1}{H_g} \bullet \left(\frac{I_G}{W} \right)^{m_g} \bullet t \right)^{n_g} \tag{2.3}$$

where Δ is the hot-carrier-induced oxide damage, I_G is the gate current, W is the width of the device, t is the total time of operation, and m_g, n_g, H_g are the degradation parameters which can be extracted from stressing experiments. Other PMOSFET degradation models are based on the total charge injected into the gate oxide during device operation [2.16]-[2.17].

$$\Delta = (A \cdot (I_G \cdot Q_{inj}^m)^n) \tag{2.4}$$

where I_G is the gate current, Q_{inj} is the amount of charge injected into the gate oxide, A, m, and n are technology-dependent parameters which need to be extracted from stressing experiments.

2.3 Impact of Hot-Carrier-Induced Degradation on Circuit Performance

Under static DC stress conditions, hot-carrier-induced device degradation for both NMOS and PMOS transistors produces changes in the threshold voltage, transconductance and current-driving capability. When the transistors are under the dynamic operating conditions of a CMOS circuit, the MOSFET terminal voltages changes over time. Therefore, the drain current and substrate current should be modeled as functions of time. If the quasi-static assumption is valid, then the hot-carrier degradation model developed under DC static conditions can be modified to predict the degradation of devices undergoing AC circuit operation [2.1]:

$$\Delta N_{it} = \left(\frac{1}{W \bullet H} \int_0^T I_D^{1-m}(t) \bullet I_{SUB}^m(t) dt \right)^n \tag{2.5}$$

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Chapter 3

Digital Test Circuit Design and Optimization for AC Hot-Carrier Reliability Characterization under High Frequency Stress Conditions

3.1 Introduction

The focus of hot-carrier reliability assessment has shifted from device-level to circuit-level evaluation. Under circuit operational conditions, devices experience dynamic terminal voltage waveforms. Therefore, it is important to understand the behavior of hot-carrier degradation under dynamic voltage conditions. It has been reported that the hot-carrier degradation of an NMOSFET under dynamic stress conditions is worse than that predicted by the quasi-static approximations (AC enhancement effect). Some of these enhancement results have been attributed to measurement errors [3.7], others have been explained as the result of alternating hole-electron injection since NMOSFETs are swept through the three different degradation regions (hole injection, interface-state generation, and electron injection) under typical digital circuit operational conditions [3.2], [3.18]. Almost all of these AC enhancement effects were observed when dynamic voltages were applied to discrete devices. Although the proposed alternating hole-electron injection may cause enhanced AC degradation of a single NMOSFET when its gate-to-source voltage is swept from low to high and the drain-to-source voltage is kept at a constant value, however, electron injection of an NMOSFET in actual digital circuits is much weaker since the drain-to-source voltage decreases as the gate-to-source voltage increases.

Therefore, the AC enhancement effect due to alternating hole-electron injection needs to be carefully re-evaluated under circuit operational conditions.

In order to make accurate assessments of hot-carrier lifetime in a realistic circuit environment, hot-carrier reliability test circuits are necessary in order to generate realistic AC stress waveforms which are required for circuit simulation and reliability tool calibration. Test circuits are also needed to provide insight about AC degradation mechanisms and to provide a realistic circuit response to hot-carrier damage.

Earlier studies [3.1]-[3.6], which focused on the AC stressing of individual transistors, suffered from inherently unrealistic stress waveforms; other studies also suffered from mismatch between the external signal sources and the devices under test, and from inductive noise coupling to the power supply terminals [3.7]. In addition, different circuit sensitivities to hot-carrier damage could not be obtained from individual AC device measurements. Recent studies utilized on-chip oscillators to generate realistic voltage waveforms [3.9], [3.13]-[3.16]. However, the design of the test structure was not optimized for typical circuit operational conditions [3.9], or for accurate internal device characterization [3.13]-[3.16], or for relating device and circuit performance degradation [3.13].

Another previously-used option, which characterizes hot-carrier reliability using test circuits which have only been designed for performance evaluation alone [3.8], is also inadequate since, without access to internal device nodes, it is difficult to delineate between NMOS and PMOS device degradation, and to distinguish between the circuit's effect on creating damage from the circuit's sensitivity to that damage.

To address these problems, this chapter discusses key issues involved in designing hot-carrier reliability test circuits that can provide realistic stress voltage waveforms,

allow access to the internal device nodes, and provide insight about circuit performance sensitivity to hot-carrier damage. Insights about previous test circuit designs will be presented and additional test circuit designs will be demonstrated. The inherent design trade-offs that exist between realistic waveform generation and internal device accessibility will be analyzed and clarified. Recommendations for optimal test-circuit design for hot-carrier reliability characterization and model calibration will be proposed.

3.2 Test Circuit Design

For general hot-carrier reliability characterization, test circuits designed as ring oscillators and inverter chains are advantageous because of their relative ease of delay measurement and because of their ability to relate directly the impact of hot-carrier damage to circuit performance. In addition, ring oscillators and inverter chains can easily be designed to cover a wide range of the circuit-design space by adjusting the transistor sizes, fanouts and the number of stages.

Figure 3.1 illustrates a general schematic for hot-carrier test circuits designed in the ring-oscillator configuration; these circuits allow internal node access for the devices of a representative stage within the oscillator. Similar test structures were designed for inverter chain circuits as well. The inputs of the inverter chain circuits were driven by an on-chip voltage-controlled-oscillator (VCO). For both the ring oscillator and inverter chain circuits, no external signal sources were needed; only an external DC power supply was required.
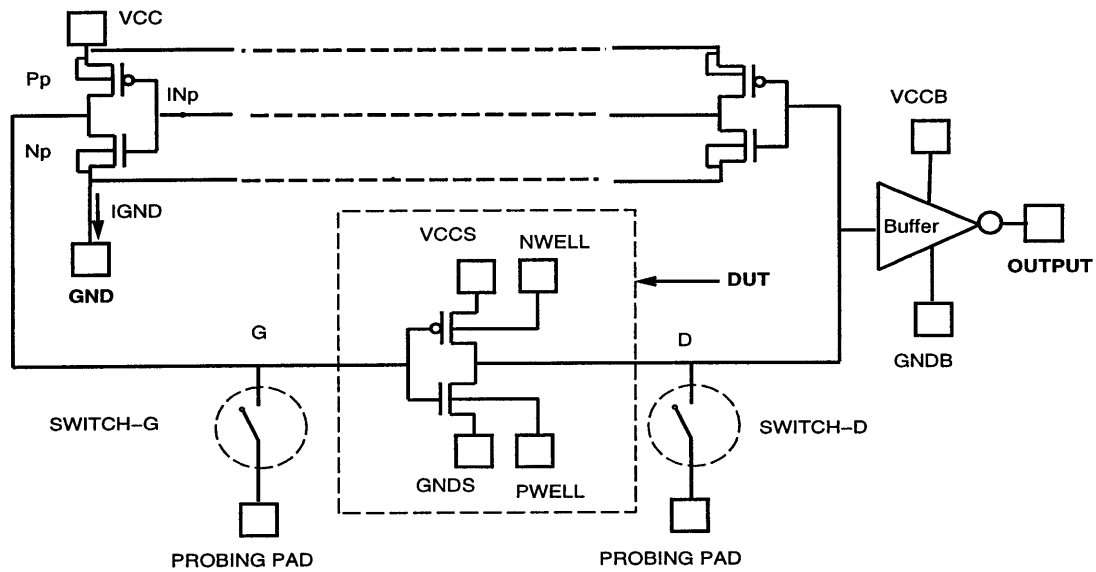
Figure 3.1   General circuit schematic of a ring oscillator AC test structure for hot-carrier reliability evaluation.

The ring oscillator and inverter chain structures were designed such that the ratio of PMOS and NMOS transistors sizes is $(W/L)_p / (W/L)_n = 2$ in order to have relatively equal rise and fall times. In digital CMOS circuits, the typical loading of a stage ranges from 1 to 5 fanins/fanouts. Our test structures were designed to have fanin/fanout values ranging from 1 to 15.

When laying out the representative inverter stage (indicated as DUT in Figure 3.1), it is recommended that the NWELL and PWELL of this stage be separated from WELLS of the other stages, if a twin well process is available. This design allows the substrate currents of NMOS and PMOS transistors of the DUT to be measured accurately. The hot-

carrier test structures can be laid out small enough to fit into a scribe line. Figure 3.2 shows an example of the layout of a ring oscillator test structure.
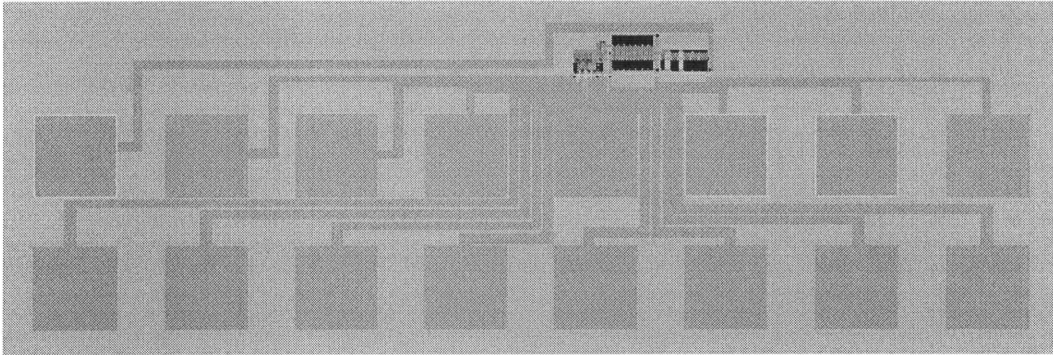
Figure 3.2   Microphotograph of a test structure.

3.3 Test Circuit Operation

For the ring oscillator test circuits (and for the inverter-chain circuits as well), the stress and measurement procedure can be divided into two distinct modes:

3.3.1 Stress Mode

In the stress mode, all the DC probing switches (labeled as switches G and D in Figure 3.1) are turned off and the circuit is isolated from the external probing pads. The design of these switches will be discussed in the next section. The desired stress supply voltage is then applied to pads VCC and VCCS, generating the internal AC stress voltage waveforms.

3.3.2 Measurement Mode

In the measurement mode, the stress-voltage waveforms are stopped, either by floating the power supply, VCC, or by disconnecting the ring oscillator via a pass gate. The probing switches are then turned on, thereby allowing access to the internal device nodes. By properly biasing the relevant nodes, the degraded internal NMOS, PMOS and inverter characteristics can be measured for this representative stage within the ring oscillator.

The output buffers were designed with a separate power supply in order to minimize the effects of inductive noise. During stress, any degradation-induced change in the oscillation frequency was monitored at the buffered output pad (typically using a picoprobe in order to minimize loading). The stage ratio of the output buffer is 3 in our design. The stage ratio is defined as the width of the next stage divided by the width of the current stage.

3.4 Internal Node Switch Design

An ideal switch for these hot-carrier reliability test circuits should have the following characteristics: First, it should minimally disturb the circuit during stress in order to maintain as realistic circuit operating conditions as possible. Second, it should be able to pass through a wide range of measurement voltages in order to allow full measurement of the device characteristics before and after each stress. Third, it should be able to measure accurately the voltage at the internal node of interest.

Shown in Figure 3.3 are four different design implementations (A, B, C, D) for the special probing structures to allow internal node access. Note, that there is always a design trade off between realism of the AC stress waveforms and accessibility to the internal

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devices. It is impossible to access the internal nodes of a circuit without introducing some disturbance to the circuit itself. The goal is to maximize the obtainable information while minimizing the impact on the circuit behavior.

Design A

The most straightforward way to access the individual devices within a ring oscillator is to connect the internal nodes directly to probing pads as shown in Figure 3.3a [3.9]-[3.11]. Although convenient, this direct connection of the probing pads can add significant capacitance to the internal nodes. Figure 3.4 shows that the probing pads can change the voltage waveforms significantly. Thus, this particular test circuit design can only represent the case of extremely large loading; it cannot be used to represent typical circuit operating conditions and is not suitable for high frequency stressing.

Design B

Using a pass transistor to isolate the probing pad (Figure 3.3b) offers a good solution to the previously described problem since it only adds a small capacitance to the circuit (an overlap capacitance and a junction capacitance) while allowing access to the internal nodes.

Figure 3.5 shows that the effect of the probing pass transistors, when turned off, on the ring oscillator waveforms is very small. Note, in Figure 3.3b, that both the TD1 and TD2 pass transistors are necessary, since, during the measurement mode, there is a current flowing through TD2 and the devices under test (DUT) when a voltage is applied to V_{ddrive}. Because of the ensuing voltage drop across TD2, TD1 is introduced to measure the real voltage that exists at node D.
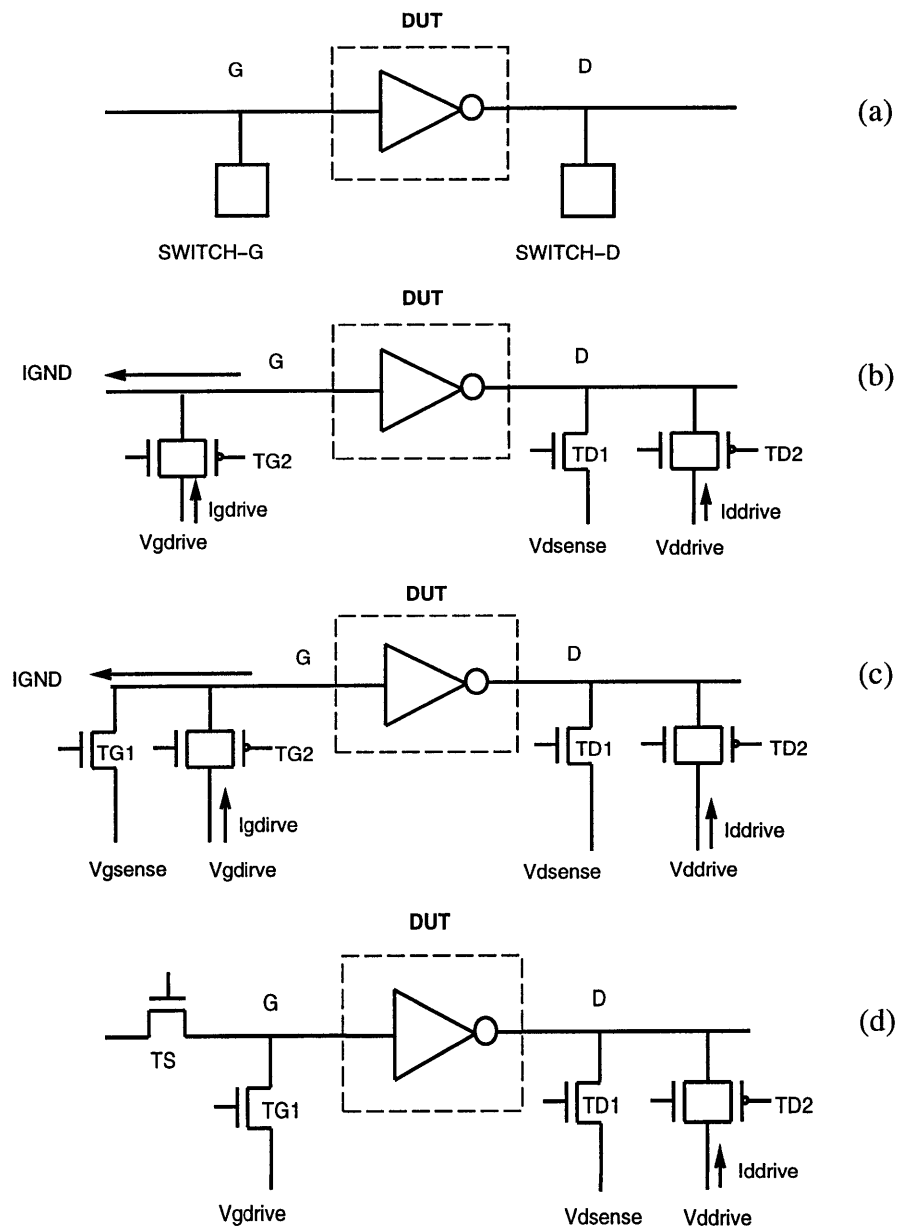
Figure 3.3 Circuit design of special probing structures for internal node access.

Ideally, on the gate side, there should be no current flowing through TG2 during the measurement mode However, we found that there was an unexpected leakage current path going through TG2 and the NMOS device Np (see Figure 3.1) of the previous inverter stage when a voltage was applied to V_{gdrive}. This is because the input node, INp, of the previous inverter stage must have been floating during the measurement mode. This floating node is very unstable and sensitive to capacitive coupling. As the voltage V_{gdrive} is increased, the transistor N_p is gradually turned on due to coupling of the overlap capacitance between the drain and gate. Figure 3.6 shows that this leakage current rises as the voltage V_{gdrive} increases. Thus, the switch design in Figure 3.3b, while allowing a realistic stress waveform, can potentially induce errors due to leakage-current-induced inaccuracies in measurements of the device node voltage V_G (Figure 3.7). Note, that this is an inherent problem not only for this particular test-circuit design, but also for other previous test-circuit designs which are based on the same measurement principle [3.12]-[3.17].

Design C

In order to solve the leakage current problem that exists for Design B, the real voltage that exists at node G, can be directly measured by introducing a new additional pass transistor, TG1, as shown in Figure 3.3c; this greatly improves the accuracy of the I-V characterization. However, even with TG1, the leakage current still exists. For sufficiently high leakage current, the voltage V_G will appreciably differ from V_{gdrive} due to the ohmic drop across TG2. If sufficiently high (the exact value depends on the particular technology), the leakage current can actually limit the maximum applicable measurement voltage that can be applied to the node V_G. It is worth emphasizing that this leakage current is not present during the ring oscillator stress mode since all the pass
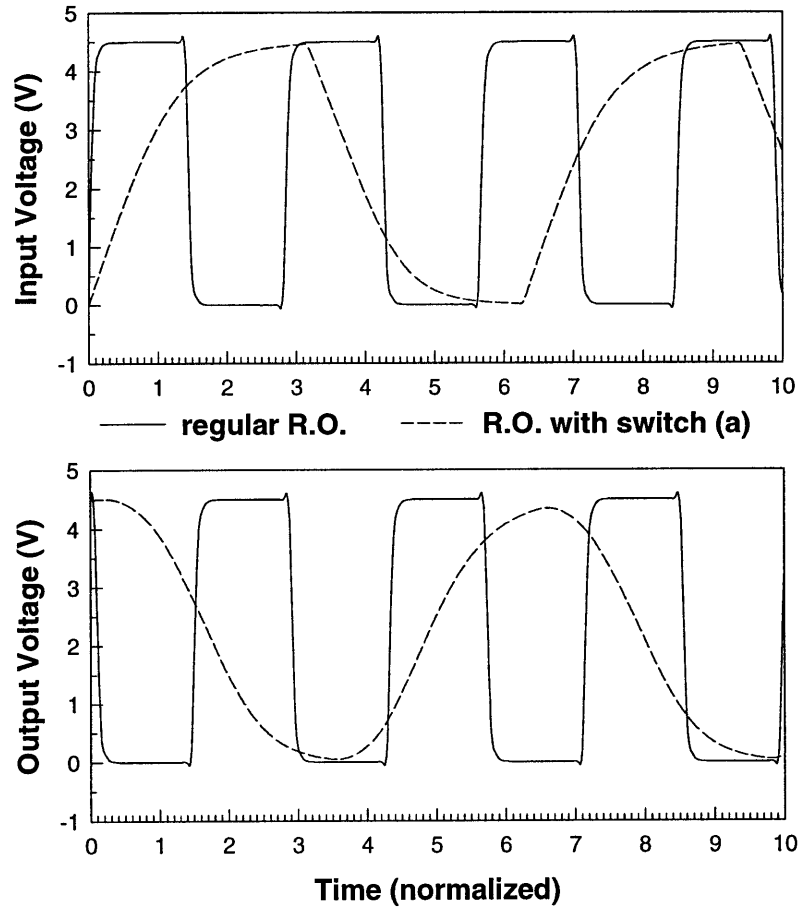
Figure 3.4   Comparison of the input and output waveforms of a CMOS inverter in a regular ring oscillator and in a ring oscillator with probing pads as shown in Figure 3.3a (HSPICE simulation results). The capacitance of a probing pad is estimated to be 1pF. Both ring oscillators have 23 stages and fanout 1. The sizes of the transistors are: $(W / L)_N = 5 / 0.6$ μm, $(W / L)_P = 10 / 0.6$ μm.
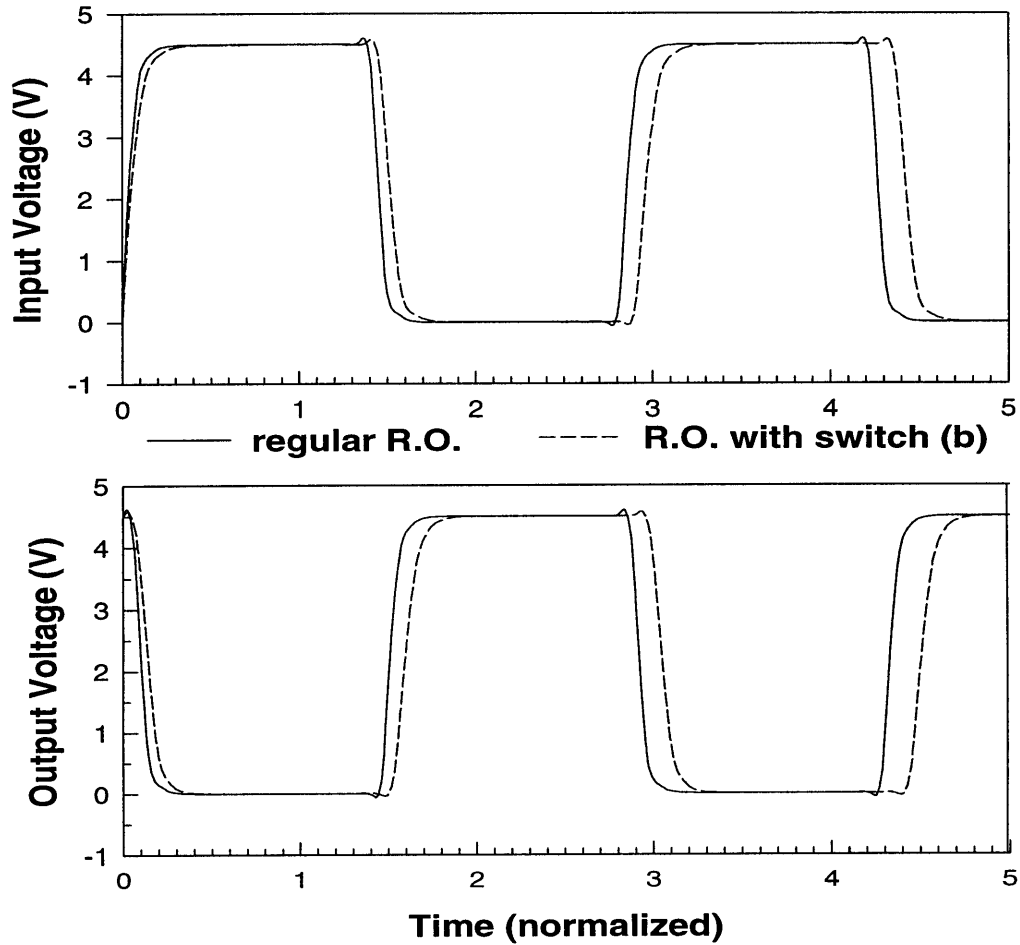
Figure 3.5 Comparison of the input and output waveforms of a CMOS inverter in a regular ring oscillator and in a ring oscillator with the probing structure of Figure 3.3b (HSPICE simulation results).

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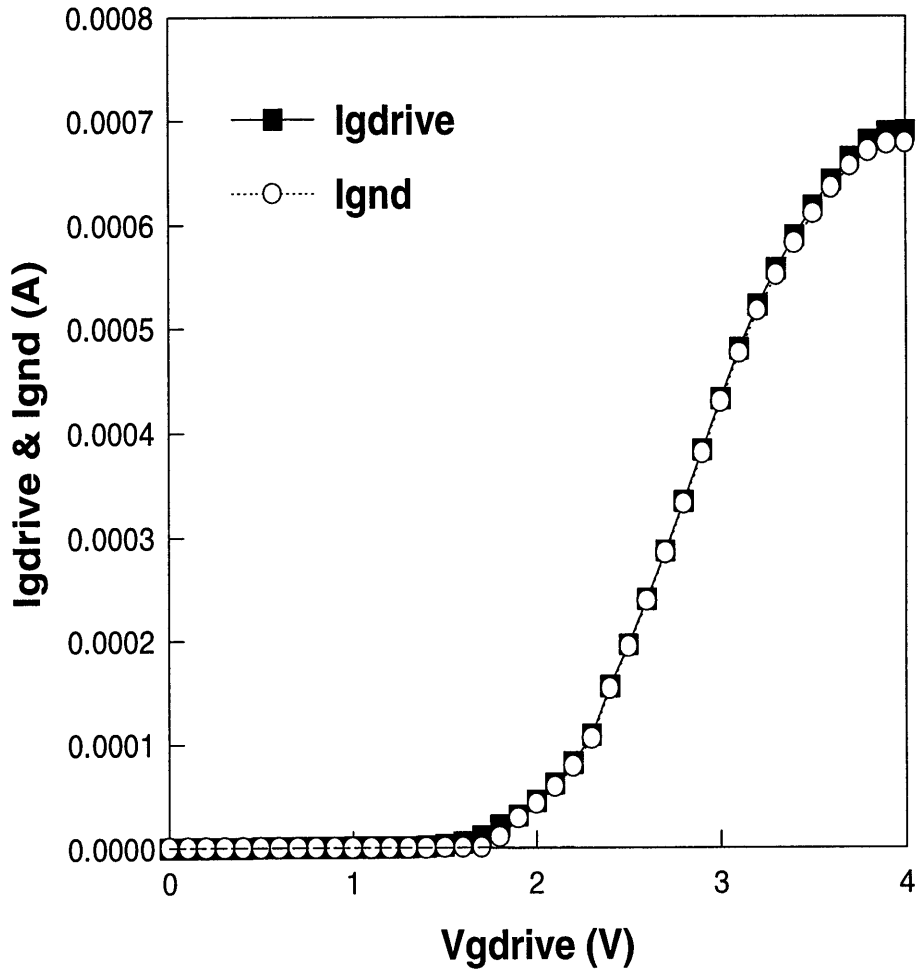
Figure 3.6 Leakage current Igdrive as a function of the voltage applied at the drain of transmission gate TG2. IGND is the current measured at the source of the NMOS device N_p in Figure 3.1 .
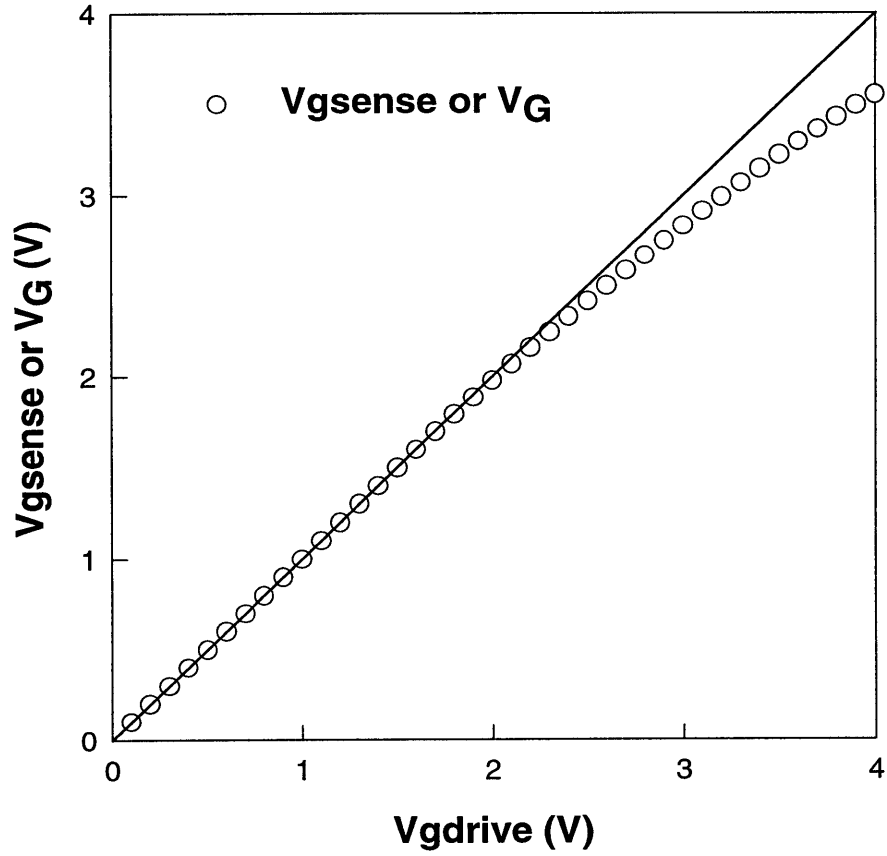
Figure 3.7   The deviation of the voltage V_G (Vgsense) from the applied voltage Vgdrive due to the leakage current.

transistors are switched off and no internal nodes are floating. The design in Figure 3.3c, although it still places limitations on the range of possible characterization voltages, does generate more realistic stress waveforms and allows more accurate internal device measurements.

Design D

Shown in Figure 3.3d is a new switch design which uses an extra switch gate, TS, to cut-off completely the leakage path that exists during the measurement mode. With no leakage current flowing, the node voltage V_G can be accurately measured using just TG1 (no ohmic drop); no limitation also exists on the range of applicable V_G measurement values. However, these benefits come at the cost of adding a small on-resistance during the stress mode.

In the stress mode, the voltage applied to the gate of the switch transistor TS should be at least one body-effected threshold higher than the stress voltage applied to VCC. This is to ensure that the voltage at node G won't be clamped because of the threshold-voltage drop. This is also to ensure that the on-resistance of device TS is kept small. Figure 3.8 shows that the device TS has minimal effect on the ring oscillator waveform. The design in Figure 3.3d, although it produces a small acceptable impact on the stress waveform, allows the most accurate and robust measurement of the internal device nodes.

3.5 Experimental Results

The LDD (Lightly-Doped-Drain) devices and test circuits used for this study were fabricated using either a 0.4um (technology A) or a 0.6um (technology B) NWELL CMOS process. Test circuits in both the ring oscillator and inverter-chain configurations
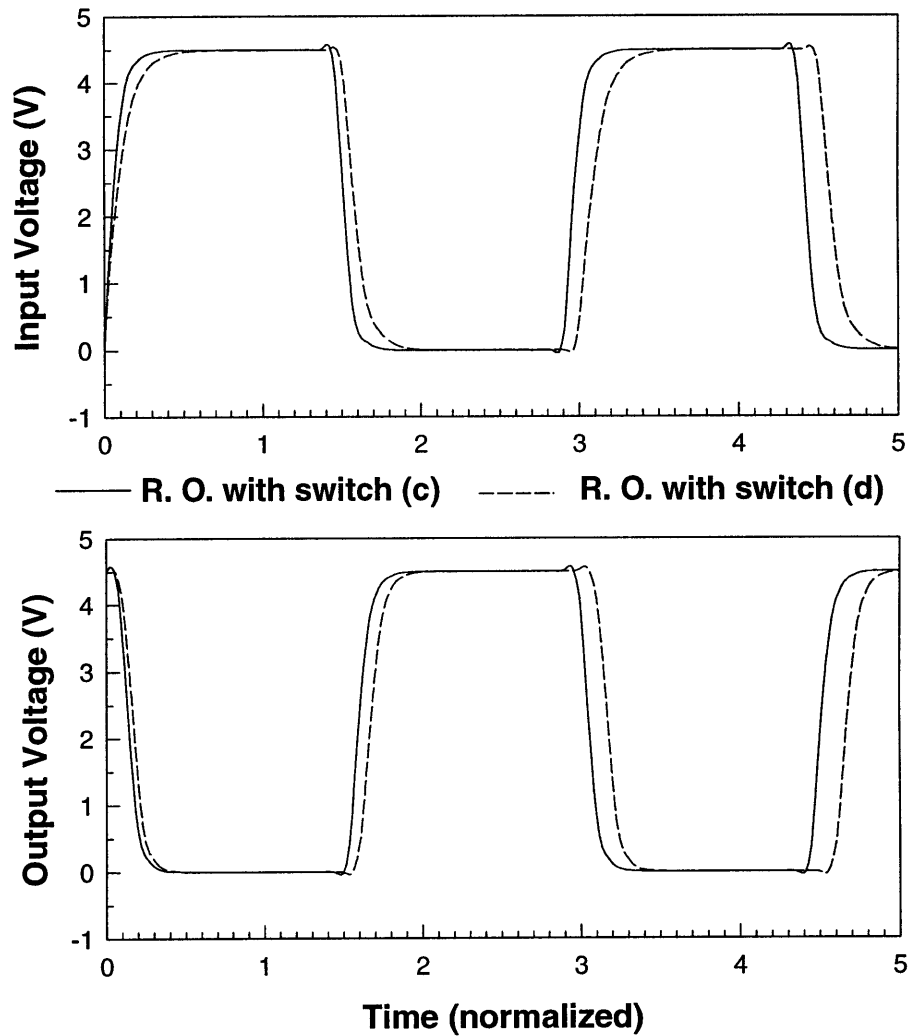
Figure 3.8 Comparison between the input and output waveforms of the probing-structure design in Figure 3.3c and Figure 3.3d (HSPICE simulation results).

were fabricated with an array of different fanouts, number of stages, and structures for internal device node access. For all test circuits, the NMOS and PMOS device widths were 5um and 10um, respectively. Ring-oscillator test structures were stressed with periodic interruptions in order to monitor the degradation of the device and inverter characteristics.

Take the test structure shown in Figure 3.3d as an example. During the stress mode, the switch gate TS is overdriven by setting the gate voltage of TS to (V_{stress} + $V_{th}(B)$), where V_{stress} is the stress voltage and $V_{th}(B)$ is the body-affected threshold voltage. This is to ensure that waveforms at the input of the DUT have a full voltage swing. The VCC and VCCS nodes (Figure 3.1) of the ring oscillators are connected to V_{stress}. The power supply of the output buffer is set at the operational voltage of the ring oscillator in order to avoid any degradation of the buffer due to stressing.

During measurement, the switch gate TS is turned off so that the DUT is isolated from other stages in the ring oscillator. The probing switches TG1, TD1 and TD2 are then turned on. The node voltage V_{gdrive} becomes the gate voltage of the NMOS (or PMOS) device under test, the node voltage V_{dsence} becomes the drain voltage, and I_{ddrive} becomes the corresponding drain current of the NMOS (or PMOS) device. By properly biasing V_{gdrive} and V_{dsence} and measuring I_{ddrive}, the NMOS and PMOS I-V characteristics can be determined. The node voltages V_{gdrive} and V_{dsence} can also be used to determine the inverter transfer characteristic.

Figure 3.9 shows typical fresh and degraded internal NMOS and PMOS DC I-V characteristics taken from one stage of a 23-stage, fanout 1, oscillator test circuit after having undergone high-frequency (100 to 350 MHZ) AC stress for 20 hours. The stress voltage is 4.5V. Figure 3.10 shows the associated degradation in the inverter transfer characteristic.

The complex nature of the device/circuit interaction in hot-carrier degradation necessitates distinguishing between the different NMOS and PMOS characteristics. For example, Figure 3.11 and Figure 3.12 compare the internal device and circuit performance degradation characteristics for ring-oscillator test circuits from technologies A and B. From Figure 3.11, it is clear that for technology A, NMOS device degradation dominates that circuit's performance degradation, whereas, for technology B, first PMOS and then NMOS device degradation is responsible for that circuit's performance degradation (as observed in the initial speed up and then slow down in the oscillation frequency). Without internal node access, allowing direct device measurements, it would be impossible to determine the root cause for the circuit performance degradation from the frequency characteristics alone.

3.6 Summary

We have critically analyzed test circuits for AC hot-carrier reliability characterization and have proposed two new AC test structures (Figure 3.3c and Figure 3.3d) which can provide realistic high-frequency voltage waveforms and can allow more robust and accurate internal device measurements. The degradation characteristics of devices stressed under realistic AC conditions and the impact of hot-carrier damage on circuit performance can be directly obtained.
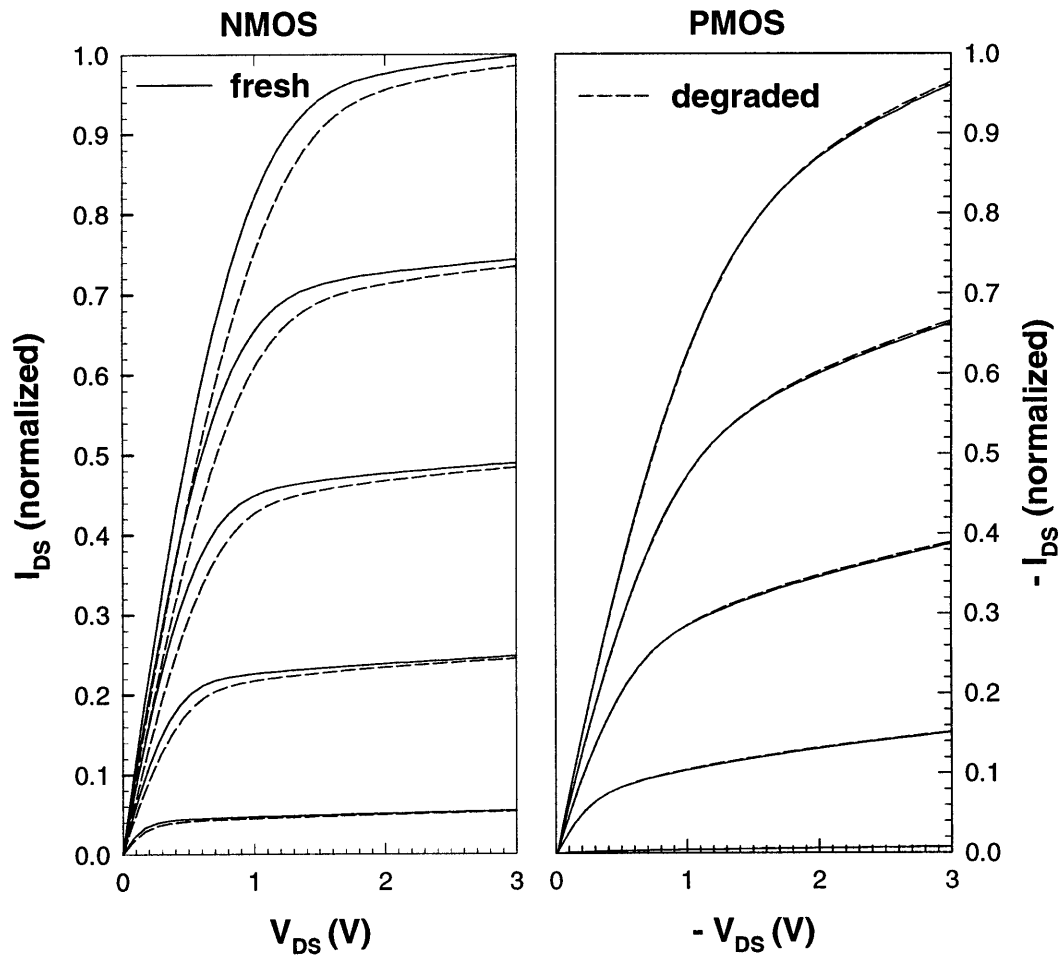
Figure 3.9   AC device degradation before and after 20 hours of stress in a CMOS inverter ring oscillator (23 stages and fanout 1). The stressing voltage is VCC = 4.5 V. The devices are measured at $|V_G| = 1, 1.5, 2, 2.5, 3$ V. The data values have been normalized.
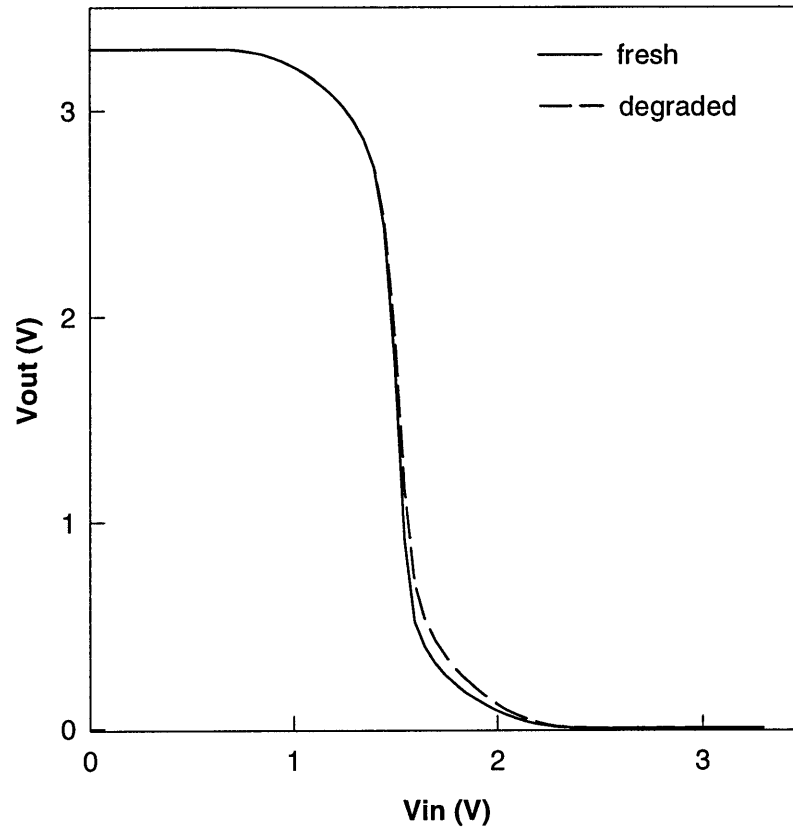
Figure 3.10   DC transfer curve of a CMOS static inverter before and after stress in a ring oscillator (23 stages and fanout 1) for 20 hours at 4.5 V.
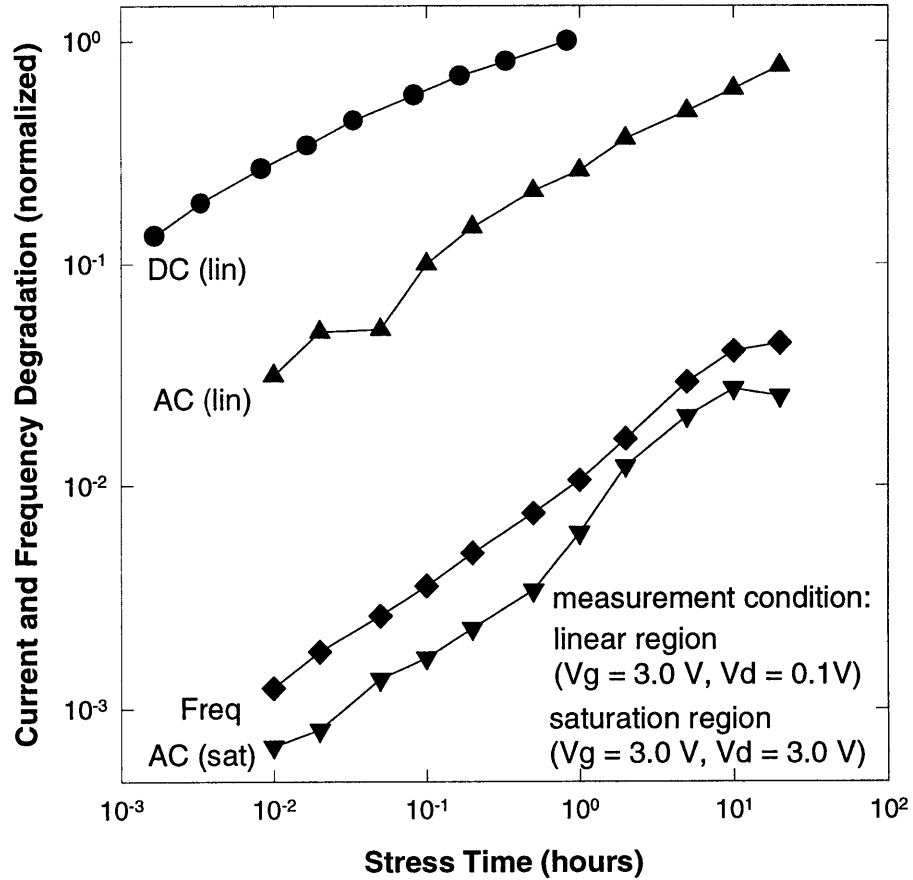
Figure 3.11 Comparison of DC, AC NMOSFET current degradation and frequency degradation. DC stress conditions are $V_G = 1.75$ V, $V_D = 4.5$ V. The stress voltage for the ring oscillator is 4.5V. The frequency degradation is measured at VCC = 3.0 V.
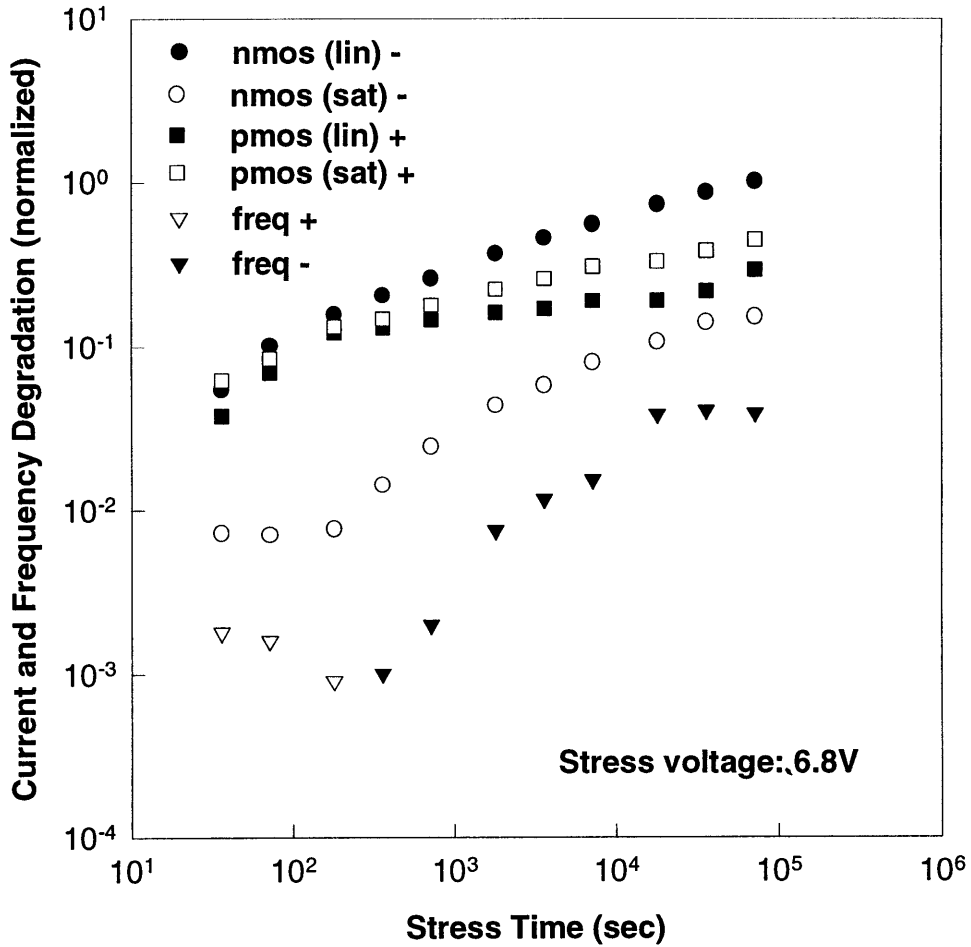
Figure 3.12   NMOS and PMOS AC current degradation in a ring oscillator of 13 stages and fanout 2. Freq stands for frequency degradation. Measurement condition: $|V_G| = 2.5$ V, $|V_D| = 0.2$ V in linear region; $|V_G| = 2.5$ V, $|V_D| = 2.5$ V in saturation region.

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Chapter 4

Key Hot-Carrier Degradation Model Calibration Issues for Accurate AC Circuit-Level Reliability Simulation

4.1 Introduction

In order to establish realistic hot-carrier reliability criteria based on circuit rather than device performance, several different models for predicting AC circuit-level degradation have been developed [4.1]-[4.5]. However, there currently does not exist any complete or consistent methodology on how to calibrate these models to existing experimental data; inconsistent model calibration techniques can result in widely differing predicted AC degradation values. In addition, each AC model suffers from a severe lack of any detailed experimental verification; thus, there is little clear basis upon which to evaluate and compare different models.

In this chapter, key issues involved in the calibration of the hot-carrier degradation models used for simulating AC circuit-level reliability are examined based on device and circuit data from two representative industrial technologies. First, the need to account for the stress drain-oxide-field dependence of the degradation model coefficients extracted from DC device-level stress measurements is demonstrated. Next, the statistical confidence limits of the extracted degradation model parameters is analyzed. Then, the sensitivity of degradation to drain and substrate current modeling errors is examined. Finally, specific recommendations are made about improving the consistency and accuracy of both degradation and SPICE model parameter extraction.

4.2 Experimental Details

The device experimental data used in this study was obtained from two representative CMOS technologies: Technology A is a 0.4 micron, LDD process with an oxide thickness of 7nm; Technology B is a 0.6 micron, LDD process with an oxide thickness of 12.3nm.

DC stress measurements for parameter extraction were performed on NMOS devices distributed across the wafer. Linear-current degradation, measured in the same polarity as the stress bias; was chosen as the principal degradation monitor because of its well-understood relationship to hot-electron-induced interface states [4.6].

4.3 NMOS Degradation Modeling Issues

4.3.1 Degradation Parameter Extraction

As summarized in Chapter 2, the basic DC equation for NMOS acceptor-type interface-state generation, which underlies almost all major hot-carrier reliability simulation tools, is the following [4.7]:

$$\frac{\Delta I_D}{I_D} \propto \Delta N_{it} = \left(\frac{I_D}{W \bullet H} \bullet \left(\frac{I_{SUB}}{I_D} \right)^m \bullet t \right)^n \tag{4.1}$$

where the parameter **n** is the time acceleration coefficient; the parameters **m** and **H** are the voltage acceleration coefficients; I_D and I_{SUB} stand for the drain and substrate current, respectively; W is the width of the device, and ΔN_{it} stands for the hot-carrier-induced interface damage.

Figure 4.1a and Figure 4.1b show the DC forward-linear drain-current degradation characteristics versus time for the two technologies. It can be seen that the asymptote for NMOS hot-carrier degradation follows a simple power-law relationship [4.8], from which the time acceleration factor n and the device lifetime τ can be extracted by plotting the amount of degradation versus time on a log-log scale. In order to calculate the lifetime of a MOSFET due to hot-electron degradation, a lifetime criterion needs to be defined. A typical lifetime criterion is a 10% or 20% reduction in linear drain current.

Traditionally, in order to account for the "worst-case" hot-electron degradation scenario, the stressing condition has been chosen such that I_{SUB} is at a maximum. It has long been believed that the NMOSFET undergoes the most hot-carrier degradation under peak I_{SUB} conditions, because I_{SUB} is produced by the high lateral-electric field, which also creates hot-carriers. However, devices in circuits do not always experience worst-case stress conditions during circuit operations. Since the ultimate goal of degradation model parameter extraction enable predictions of circuit lifetime, it is important to explore the bias dependence of the these degradation parameters.

In this study, a range of different stress biases were applied. For Technology A: V_{gs} = 1.0, 1.1, 1.3, 1.5 V; V_{ds} = 4.0, 4.1, 4.3, 4.5 V; for Technology B: V_{gs} = 3.0, 3.2, 3.4, 3.7 V; V_{ds} = 6.1, 6.3, 6.5, 6.7 V.

For both Technologies A & B, the oxide-field dependence of the time-acceleration factor is observed to be relatively weak. Thus, constant n values are assumed for all subsequent analysis. This assumption allows lifetime extrapolation complications due to non-constant n values [4.9] to be avoided.
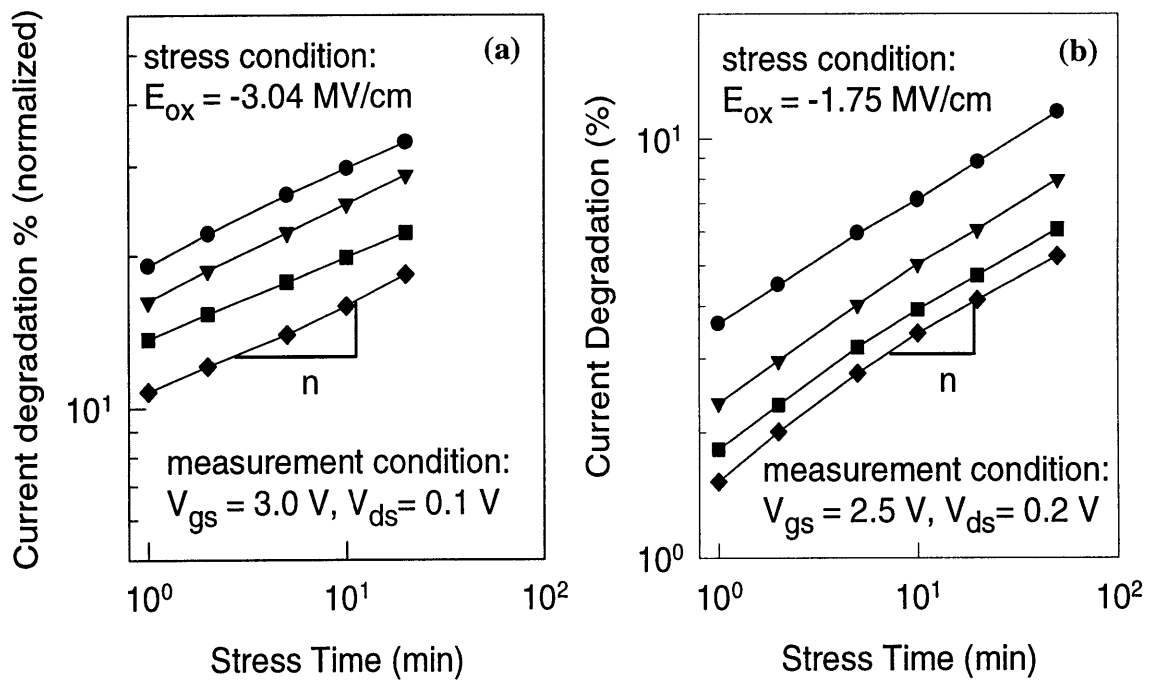
Figure 4.1 Hot-carrier-induced DC linear drain current degradation as a function of stress time for a fixed oxide field. (a) Technology A; (b) Technology B.

To extract the degradation parameters **m** and **H**, the degradation equation (4.1) can be rearranged as;

$$\frac{\tau \bullet I_D}{W} = H \bullet (\Delta D)^{1/n} \bullet \left(\frac{I_{SUB}}{I_D}\right)^{-m} \tag{4.2}$$

where ΔD is the lifetime criteria defined in Equation 4.1, (such as a 10% or 20% linear drain current degradation), τ is the corresponding lifetime extracted from the slope of the log(ΔD) ~ log(t) plot. Based on Equation 4.2, the parameters **m** and **H** can be extracted from the lifetime correlation plot τ I_D/W versus I_{SUB}/I_D on a log-log scale. By stressing devices with different I_{SUB}/I_D ratios, the data can be fitted to Equation 4.2. The parameters **m** and log(**H**) can be derived from the slope and the y-intercept of the fitted line.

Figure 4.2a and Figure 4.2b show the lifetime-correlation plots for the two technologies, from which the voltage-acceleration coefficients, **m** and **H** can be extracted. Both **m** and **H** display a pronounced dependence on the stress oxide-electric field at the drain, which is defined as E_{ox} = (V_{gs} - V_{ds} - V_{fb}) / T_{ox}. For each particular E_{ox}, the observed scatter in the lifetime data is due to statistical variation in the MOSFET structural parameters that impact the degradation process (and which are manifested in variation of the parameters **m**, **n**, and **H**) [4.10]-[4.11].

4.3.2 Evaluating Degradation Model Validity

Although the parameters **m** & **H** depend noticeably on the stress oxide field, E_{ox} [4.12], these two degradation model parameters have often been assumed to be single-valued constants, extractable at peak substrate-current conditions [4.2]-[4.4]. However, in the AC circuit environment, devices experience a wide range of terminal voltages and
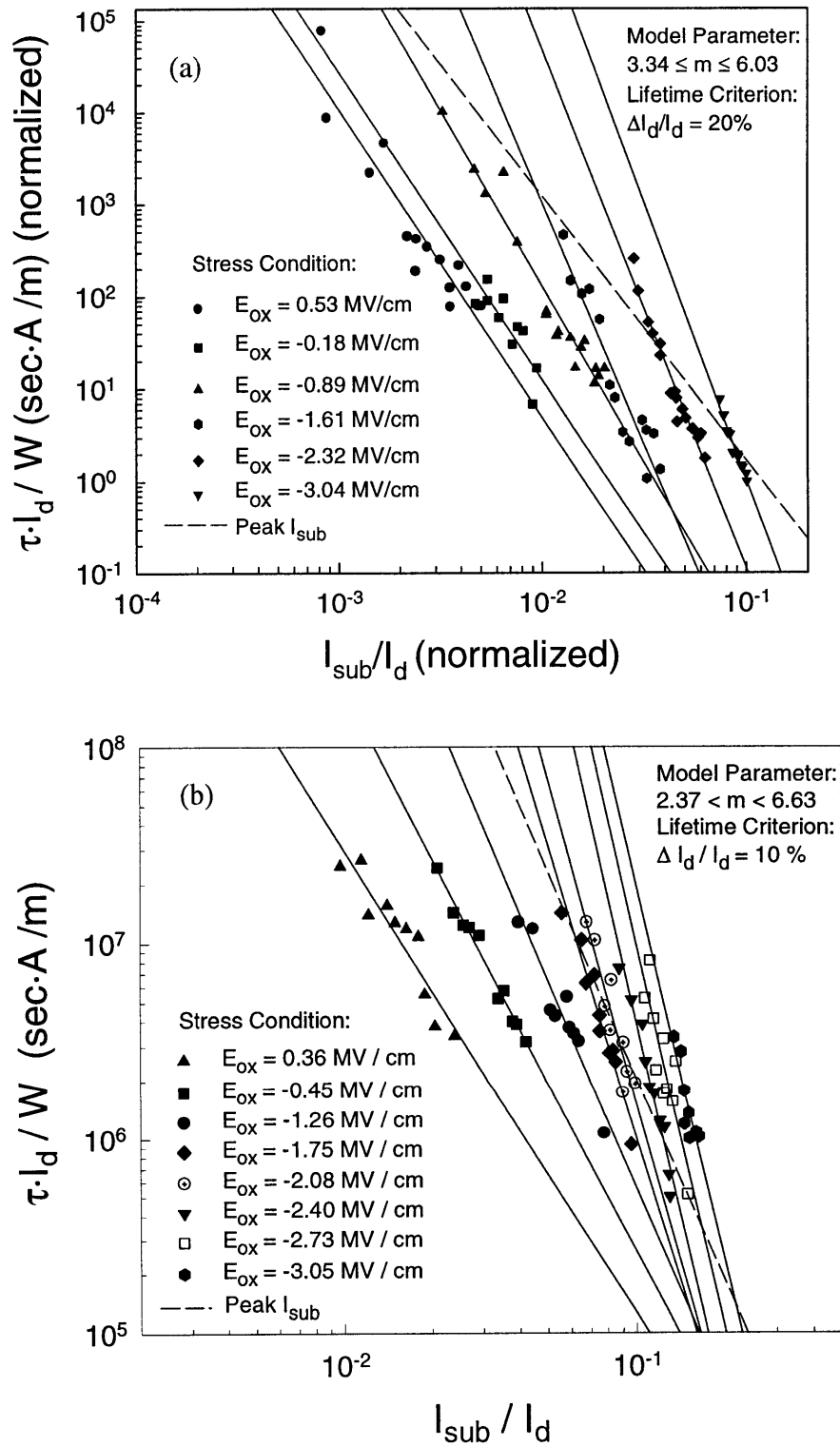
Figure 4.2   Lifetime correlation plots for different stress oxide fields: (a) Technology A, (b) Technology B.

stress oxide fields. Therefore the validity of the degradation model under these circumstances needs to be evaluated.

DC stress experiments were performed over a wide range of stress-bias conditions (Figures 4.2a-b), from which the degradation parameters **n**, **m** and **H** were extracted, based either on variable-E_{ox} or on peak-I_{SUB} conditions. Using these extracted **n**, **m**, **H** parameters, along with the *in-situ* measured DC I_D and I_{SUB} values during stress, DC linear-current degradation was first calculated using Equation 4.1 and then compared with the original experimental degradation data. Figures 4.3a-b illustrate the correlation between the actual measured data and the predicted values for Technology A for the two different sets of extracted degradation model parameters.

Since the DC substrate- and drain- current values used in the calculation were experimentally measured *in-situ* for each device, any discrepancies between the measured and calculated degradation results seen in Figures 4.3a-b must be due to inaccuracies in the degradation model parameter extraction and/or intrinsic statistical variation. As summarized in Table 4.1, for both technologies, a high correlation between the degradation model and data is only achievable if the oxide-field dependence of the parameters **m** & **H** is properly taken into account. It is also shown that using only a single value for the parameters **m** & **H**, extracted based on peak-I_{SUB} data, results in a poor fit to the experimental data.

One speculative explanation for the observed oxide-field dependence of the parameters **m** and **H** is energy band bending of the Si substrate due to the applied oxide field, which forces the drain-current path deeper into the silicon, further away from the Si-SiO_2 interface [4.13]. Figure 4.4 illustrates the energy band diagram near the drain when
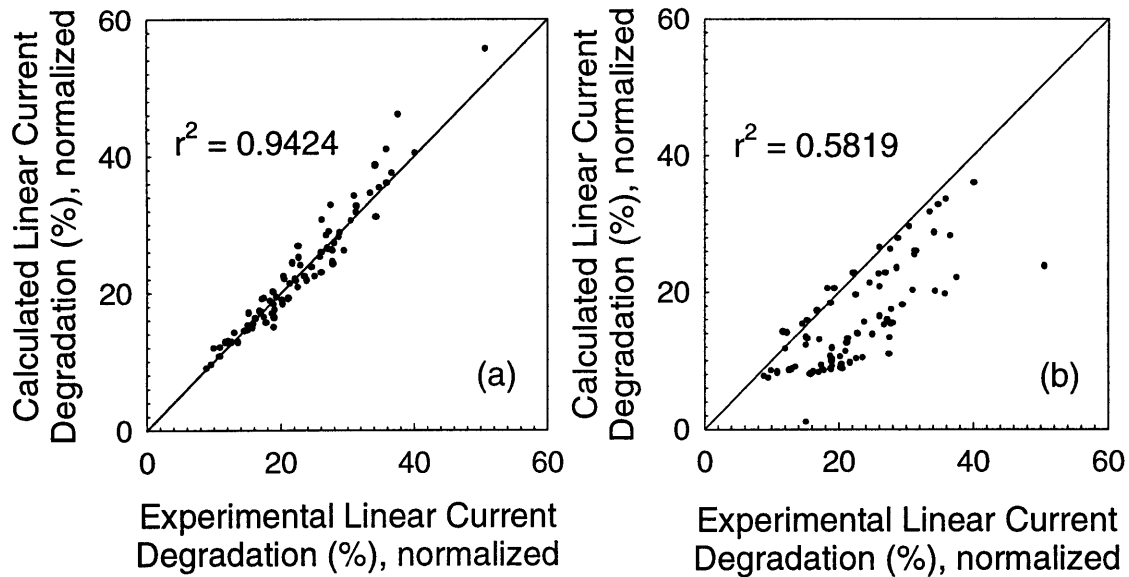
Figure 4.3   Comparison between calculated and measured DC linear drain-current degradation over a wide range of stress-bias conditions. The **m** and **H** parameter values used in (a) and (b) are extracted using the variable oxide field and peak substrate current models, respectively.

Table 4.1: Comparison of Methods for m and H Extraction

Model for m and H	$\dfrac{I_{SUB}}{I_D}$	Correlation Coefficient (r^2) between Experiment and simulation	
		Technology A	Technology B
E_{ox} Dependence	Measured from Experiment	0.924	0.9698
Peak I_{SUB}	Measured from Experiment	0.5819	0.3132

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NMOSFET is biased in saturation region. The higher the oxide field, the larger the amount of band bending, and the greater the distance hot-carriers must travel to reach the gate oxide. As a result, additional energy is required for hot-electrons to cross over the Si-SiO$_2$ barrier height to create interface states.
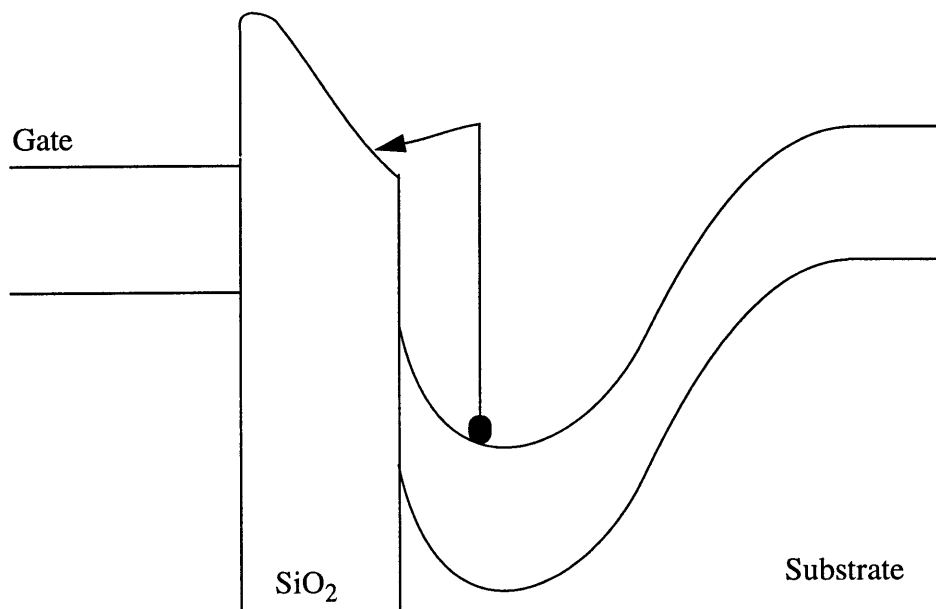
Figure 4.4   The energy band diagram near the drain when NMOSFET is biased in saturation region.

The oxide-field dependence of the degradation parameter **m** can be related to the change in critical energy required for hot-electron-induced interface-state generation. However, the exact functional form for this oxide-field dependence is not known [4.7]. In this study, a piece-wise linear model is adopted with the assumption that the **m** and Log(**H**) parameter values remain constant outside of the regions with experimental data.

Figure 4.5 shows the parameter **m** as a function of E_{ox}, experimentally extracted for both technologies along with empirical fits by piece-wise linear functions, as well as second and third order polynomials. As can be seen from Figure 4.5, the difference between the three fitted expressions is small within the measured range of data, while outside this range, the difference between the three models can be quite large. Sensitivity to the choice of model for the parameter **m** as well as sensitivity to model fitting error can be reduced by fitting the model using **m** values extracted for both a sufficiently large number and over a sufficiently wide range of E_{ox} values.

4.3.3 Evaluating Degradation Model Precision

Across a die, wafer or lot, device degradation characteristics may statistically vary due to differences in poly CD (L_{eff}), oxide thickness, substrate and source/drain doping concentration or LDD spacer dimensions, etc. This device variation produces scatter in the hot-carrier lifetime, as can be observed in Figures 4.2a-b. For each extracted value of **m** & **H** for a particular E_{ox} value, the corresponding statistical confidence interval can be determined.

Figure 4.6 illustrates the mean (dashed line) and the 95% prediction intervals (dotted line) for a linear regression. The two asymptotes of the prediction interval (solid lines) are very good approximations for the prediction interval in the regions of

extrapolation. The 95% confidence bounds for the degradation model parameters **m** and **H** can be obtained from the slope and intercept of each asymptote.

Figures 4.7a-b display the associated 95% and 99% confidence intervals for each of the **m** & **H** values extracted from Figure 4.2 for technology A and B. For simplicity, piece-wise linear interpolation was used to generate analytical expressions for the upper and lower confidence limits as a function of E_{ox}. Note, that differences in the confidence interval size can be caused by (1) larger intrinsic parameter variation, (2) different data sample sizes, (3) different parameter sensitivity to lifetime variation. Reason (3) is illustrated in Figure 4.2b and Figure 4.7b where the lifetime correlation slope becomes increasingly sensitive to lifetime variation as the E_{ox} magnitude gets larger. The statistical confidence intervals can be reduced by taking more data from DC stress experiments.
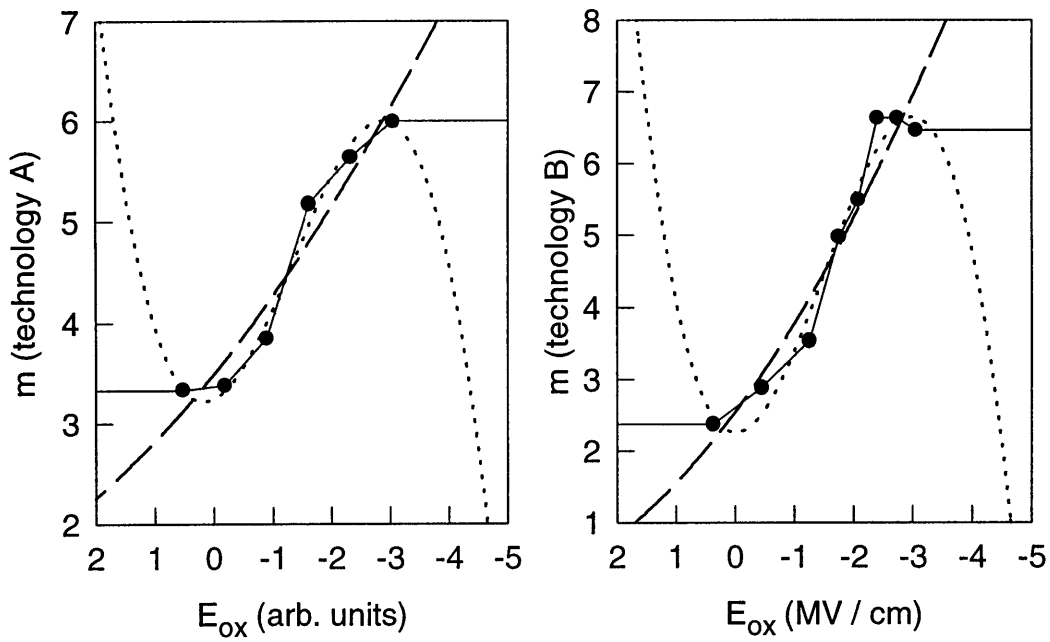
Figure 4.5 Model parameter **m** as a function of E_{ox}. The dashed and dotted lines represent second- and third-order polynomial models, respectively. The solid lines represent a piecewise-linear model. The use of different fitting models can introduce significant differences in **m** values outside the range of data.
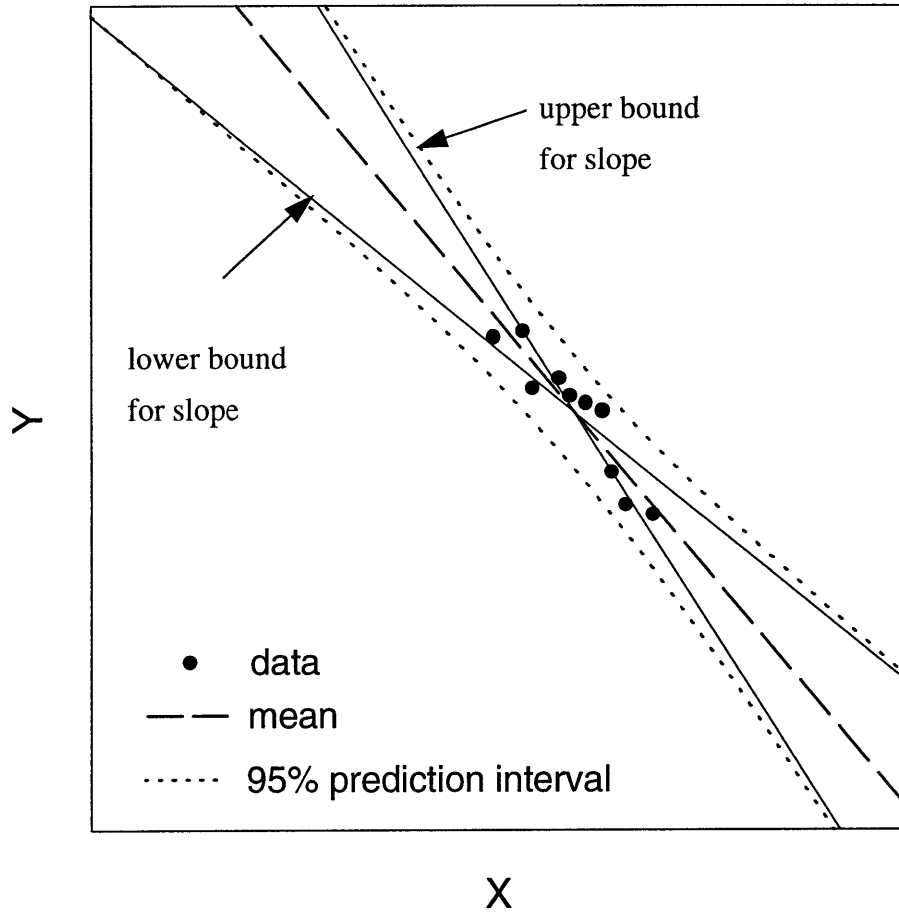
Figure 4.6   Illustration of mean, prediction interval, upper and lower bound of
the slope and intercept for linear regression.
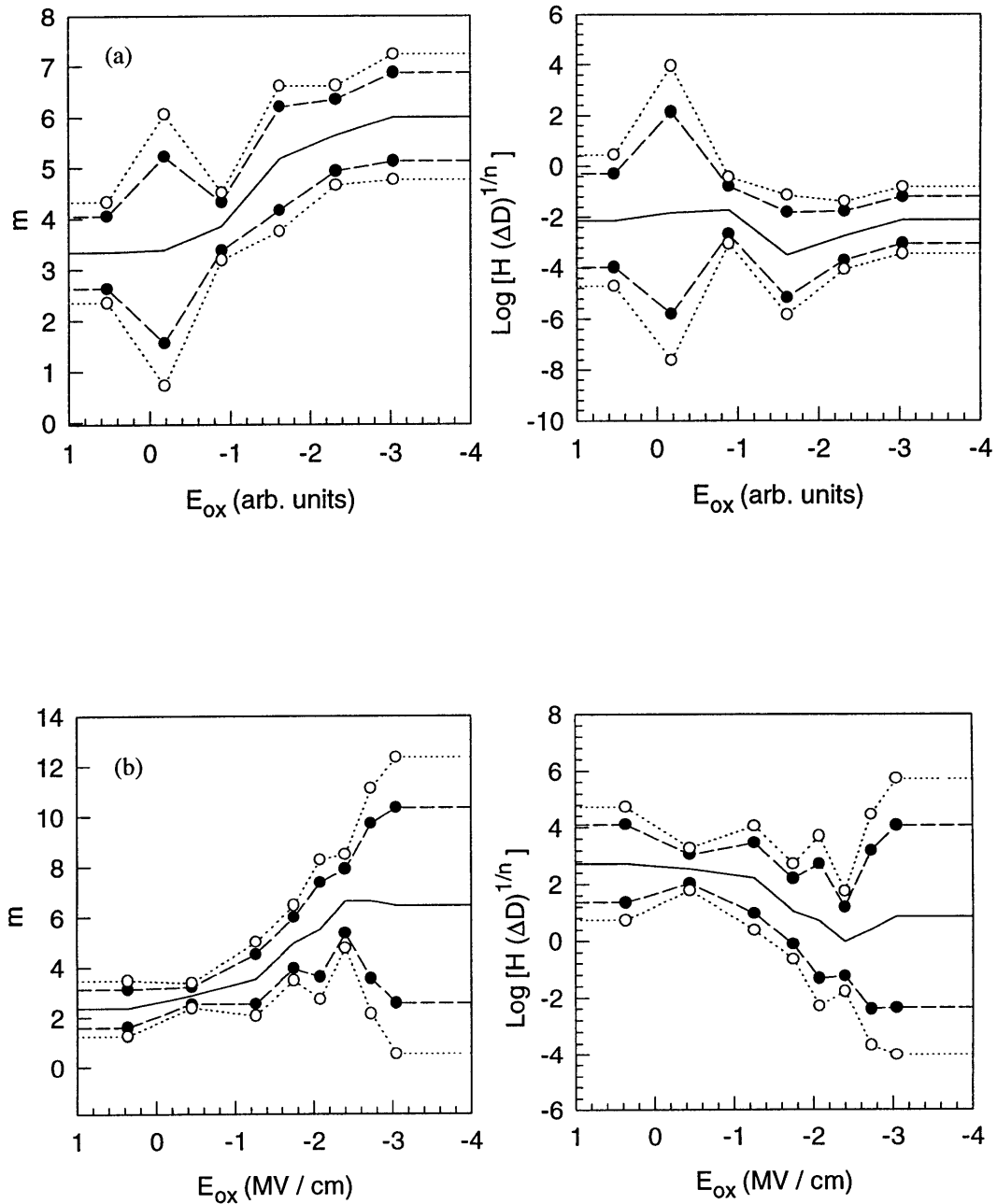
Figure 4.7   The oxide-field dependence of parameters **m** and **H** as well as the statistical confidence intervals. The solid, dashed and dotted lines represent the mean values, 95% and 99% confidence intervals of the extracted **m** and Log(**H**) parameters as a function of E_{ox}. (a) Technology A, (b) Technology B.

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4.4 SPICE Modeling Issues

4.4.1 SPICE Modeling Validity

The calculated amount of hot-carrier degradation is sensitive to the simulated substrate- and drain-current values. Therefore, the SPICE MOSFET model used for degradation simulation should be as accurate as possible in order to minimize lifetime prediction error. Typically, SPICE parameter extraction is optimized for circuit performance simulation. However, since experimental AC hot-carrier degradation data is typically obtained under stress voltage conditions, SPICE I-V parameter extraction should be optimized around these stressing voltages, when comparing AC simulated and experimental results.

Figure 4.8 shows measured I-V data as well as SPICE simulations using two different sets of SPICE model parameters: one optimized around the stress-bias conditions, the other around operational-bias conditions. As can be seen, significant error can be introduced in simulating the drain current around stress conditions, if the wrong SPICE model parameters are used. Note, that although SPICE parameter optimization at high stress voltages is important when performing comparisons between simulations and AC degradation experimental results, it is unnecessary for reliability simulation at operational voltages (for example, to calculate the operational 10-year AC lifetime).

4.4.2 Degradation Sensitivity to I_D and I_{SUB} Variation

Drain and substrate currents vary from device to device due to process variation. These current variations correlate with changes in hot-carrier degradation that are not captured using simulation based on only a single SPICE model to represent the varying
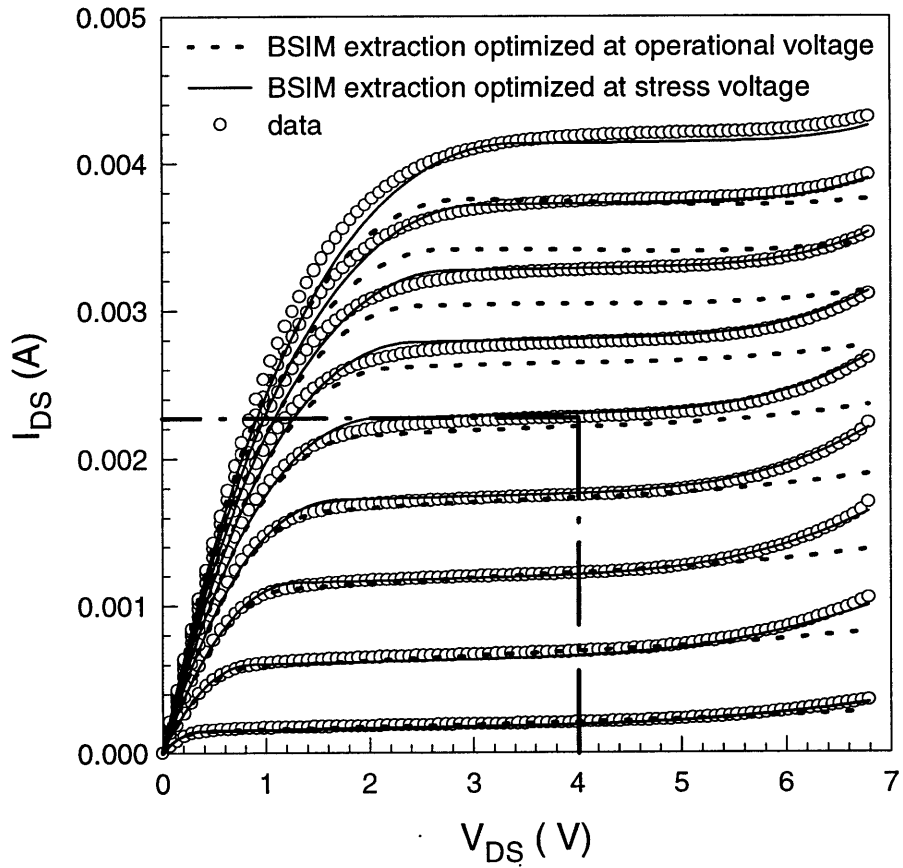
Figure 4.8   Comparison of SPICE model parameter extraction optimized at stress and operational voltages. The area under the dashed lines represents the normal device operational region. Using the SPICE model extracted at operational voltages can introduce significant error in hot-carrier simulation at stress voltages.

device I-V characteristics across a die or wafer. Assume δI_D and δI_{SUB} are modeling errors in the drain current I_D and substrate current I_{SUB}, respectively, and $\delta \Delta N_{it}$ represents the corresponding error in the predicted degradation. Then, based on Equation 4.1 and assuming the parameters **n**, **m**, and **H** as constants, the degradation error sensitivity to δI_D and δI_{SUB} can be expressed as:

$$\frac{\delta \Delta N_{it}}{\Delta N_{it}} = (1-\boldsymbol{m}) \cdot \frac{\delta I_D}{I_D} + \boldsymbol{m} \cdot \boldsymbol{n} \cdot \frac{\delta I_{SUB}}{I_{SUB}} \qquad (4.2)$$
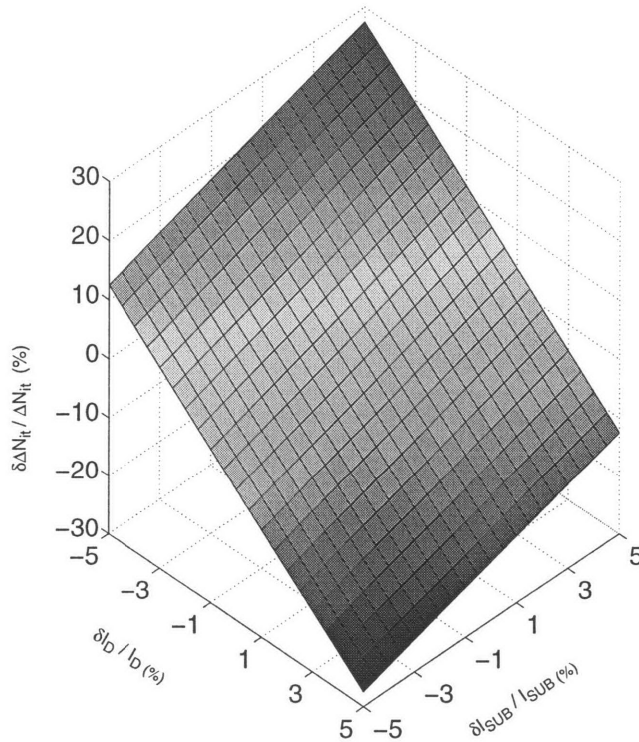
Figure 4.9   Sensitivity of hot-carrier degradation to variations in drain and substrate currents. Degradation parameter values: **n** = 0.3, **m** = 5.

Figure 4.9 illustrates the sensitivity of ΔN_{it} (for degradation parameters $\mathbf{n} = 0.3$, $\mathbf{m}$ = 5) to simulation errors in I_D and I_{SUB}. Depending on the sign of δI_D and δI_{SUB}, as can been seen from Equation 4.2, the two error components can either add constructively or destructively. As one can see from Figure 4.9, 5% errors in I_D and I_{SUB} can result in a maximum of 30% errors in current degradation.

4.5 Summary

This chapter has analyzed key hot-carrier degradation modeling calibration and verification issues. Accurate reliability simulation requires accounting for stress drain oxide-field dependence and inherent statistical variation in the degradation model coefficients as well as errors due to SPICE modeling inaccuracies.

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Chapter 5

Experimental Verification of AC Hot-Carrier Degradation Using Calibrated Reliability Simulation

5.1 Circuit-Level Hot-Carrier Reliability Simulation

Circuit behavior can be analyzed by using circuit simulators which usually consists of several build-in circuit analysis modules. For example, SPICE can perform DC, AC small-signal, transient, as well as temperature analyses. Transient analysis is used for circuit-level reliability simulation. Transient analysis outputs the variables of interest as a function of time over a user-specified time interval, i.e. circuit response to input-stimuli versus time analysis. The idea behind using the transient mode of a circuit simulator, instead of using some dedicated reliability simulator, is to make reliability simulation possible during normal circuit-performance simulation.

However, since hot-carrier degradation is a long term wear-out process, using real-time transient circuit simulation to calculate the actual amount of transistor damage due to hot-carrier effects would require an excessively long analysis time. Therefore, hot-carrier degradation is generally simulated for only the first few waveform cycles, and this result is then used to extrapolate to the user-specified time, such as 10 years, to estimate the total cumulative damage during product lifetime.

Several circuit reliability simulation tools have been developed during the past few years, most of which are based upon transistor-level circuit simulation environments such as SPICE, or different timing simulators. The advantage of using a transistor-level circuit

simulator, that outputs analog node voltage and current waveforms, is two fold. First, it allows failure and degradation prediction in any circuit that the circuit simulator can simulate. Second, model implementation is straightforward because the outputs of the simulator can be used directly to calculate the amount of hot-carrier-induced degradation (using Equation 2.2).

Certain hot-carrier reliability simulators use SPICE-level circuit simulators as their core simulation engine. Among them are the programs BERT, developed at University of California, Berkeley [5.1]-[5.2]; HOTRON, developed at Texas Instruments [5.3]; RELY, developed at University of Southern California [5.4]-[5.5]; iSMILE, developed at University of Illinois at Urbana-Champaign [5.6].

These SPICE-level reliability simulators share very similar characteristics. Figure 5.1 illustrates the flow diagram of these simulators. All these simulators consist of a SPICE-level circuit simulator, a pre-processor and a post-processor. The simulation procedure is as follows. First, the SPICE-level simulator simulates a circuit using fresh device I-V model parameters, and the voltage and current waveforms are obtained for each transistor in the circuit. Next, the post-processor calculates the value of hot-carrier-induced degradation for each transistor. Then, the pre-processor generates new degraded device I-V SPICE model parameters for each transistor based on the degradation level of each transistor. Finally, the degraded circuit performance is analyzed with the SPICE-level circuit simulators utilizing the degraded device parameter files.

There are also hot-carrier reliability simulators which use timing-level circuit simulators as their core simulation engine. Among them are the programs ILLIADS-R [5.7] and iPROBE-D [5.8], developed at University of Illinois at Urbana-Champain.

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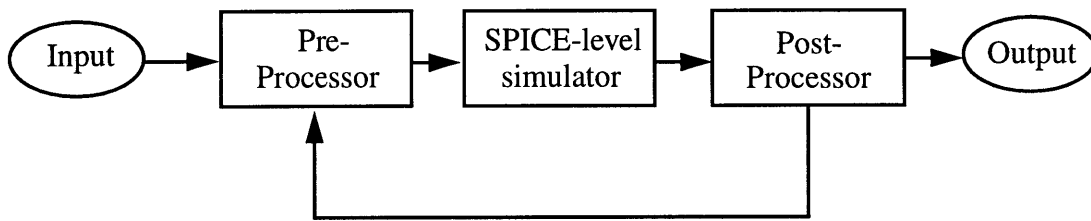
Figure 5.1   General block diagram of a SPICE-level hot-carrier reliability simulator.

The program ILLIADS-R uses a similar simulation methodology as for BERT. First it simulates the circuit using fresh device I-V parameters. The voltage and current waveforms are obtained. Then the hot-carrier-induced damage level of each device is estimated for the user-specified time. This damage level is then used to determine the degraded device I-V model parameters of each device by interpolating the pre-determined aged device parameters of two adjacent stress levels. After that, the aged circuit performance is simulated. The advantage of ILLIADS-R is its improvement in circuit simulation speed. By assuming piece-wise linear input waveforms for the circuit and by using a regional quadratic model for the device I-V characteristics, analytical solutions can be obtained for the voltage and current waveforms. Therefore, the speed simulation gain can be significant when compared to SPICE-level circuit simulators, where differential equations need to be solved in order to obtain the voltage waveforms. The disadvantage of ILLIADS-R is its poorer accuracy due to the non-physical device I-V model and the simplified hot-carrier degradation model.

The program iPROBE-D adopts both timing and probabilistic simulation techniques to estimate hot-carrier degradation. In probabilistic simulation, an event is defined as the switching of a voltage waveform with non-zero probability. Given statistical descriptions of the primary input signals, probabilistic techniques can then be used to obtain the corresponding statistical descriptions of the voltage and current waveforms inside the circuit. These probabilistic waveforms are then used to calculate the degradation of each transistor. Although this method is very fast, it is less accurate than other simulation methods. It also has difficulty in analyzing circuits with feedback.

5.2 Simulation Methodology

Little effort has been spent on comparing and benchmarking the different reliability simulators. Since the program BERT is one of the most mature circuit hot-carrier reliability simulators and has the highest degree of visibility in the literature and in industry, other hot-carrier reliability simulators are typically compared to BERT to evaluate their simulation accuracy. In this chapter, a commercial version of BERT - BTABERT is used for a rigorous comparison between one of the most accurate hot-carrier reliability simulation [5.9] and experimental data.

The program BTABERT simulates changes in the circuit performance due to hot-carrier effects, time-dependent breakdown and electromigration. BTABERT uses HSPICE as its core circuit simulation engine, and uses pre- and post-processors to handle the different reliability calculations and to provide the links to the SPICE simulation results.

In this chapter, we focus on BTABERT's hot-carrier reliability simulation calibration. The main goal of BTABERT is to estimate the amount of hot-carrier degradation each transistor experiences during circuit operation. To accomplish this task, a

parameter called AGE is introduced. This parameter quantifies the amount of degradation of each device as a function of bias conditions and stress time. The parameter AGE is defined as:

$$AGE(T_1) = \int_0^{T_1} \frac{I_{DS}}{W \cdot H} \left(\frac{I_{SUB}}{I_{DS}}\right)^m dt \qquad (5.1)$$

where T_1 is the duration of SPICE simulation (usually a few clock cycles), I_{DS} and I_{SUB} are drain and substrate currents, $\mathbf{m}$ and $\mathbf{H}$ are degradation parameters which need to be extracted from DC stress experiments. The total AGE of a device at the time of interest T, can then be calculated by assuming periodic circuit behavior,

$$AGE(T) = \left(\frac{T}{T_1}\right) \cdot AGE(T_1) \qquad (5.2)$$

Once the AGE(T) of each transistor in the circuit is calculated, the actual aged device SPICE model parameters of each device can be obtained by interpolating each parameter from the pre-stressed device parameters of adjacent AGE levels. Then the circuit performance degradation after stress can be predicted by simulating the entire circuit behavior using the degraded device parameters.

Figure 5.2 shows the flow diagram of BTABERT simulation. The major steps in BTABERT simulation are the following:

(1)   Extract the degradation parameters $\mathbf{n}$, $\mathbf{m}$ and $\mathbf{H}$ as a function of the stress oxide field as described in Section 4.3. In order to allow the user to define the oxide-field dependence of the parameters $\mathbf{m}$, $\mathbf{n}$, and log($\mathbf{H}$) as either piece-wise linear functions or polynomials, a modified version of BTABERT was developed in collaboration with BTA Technology, Inc. The degradation parameters $\mathbf{m}$ and $\mathbf{H}$ for different E_{ox} values were extracted from the DC stress measurements shown in Figures 4.2a-b. The piece-wise lin-

ear functions in Figure 4.7 were used to model the E_{ox} dependence of the parameters **m** and log(**H**) as well as for their associated 95% confidence intervals.

(2)   Extract device SPICE model parameters from a fresh device, followed by successive extractions of the same device after it has been subjected to DC hot-carrier stress for increasing AGE intervals.
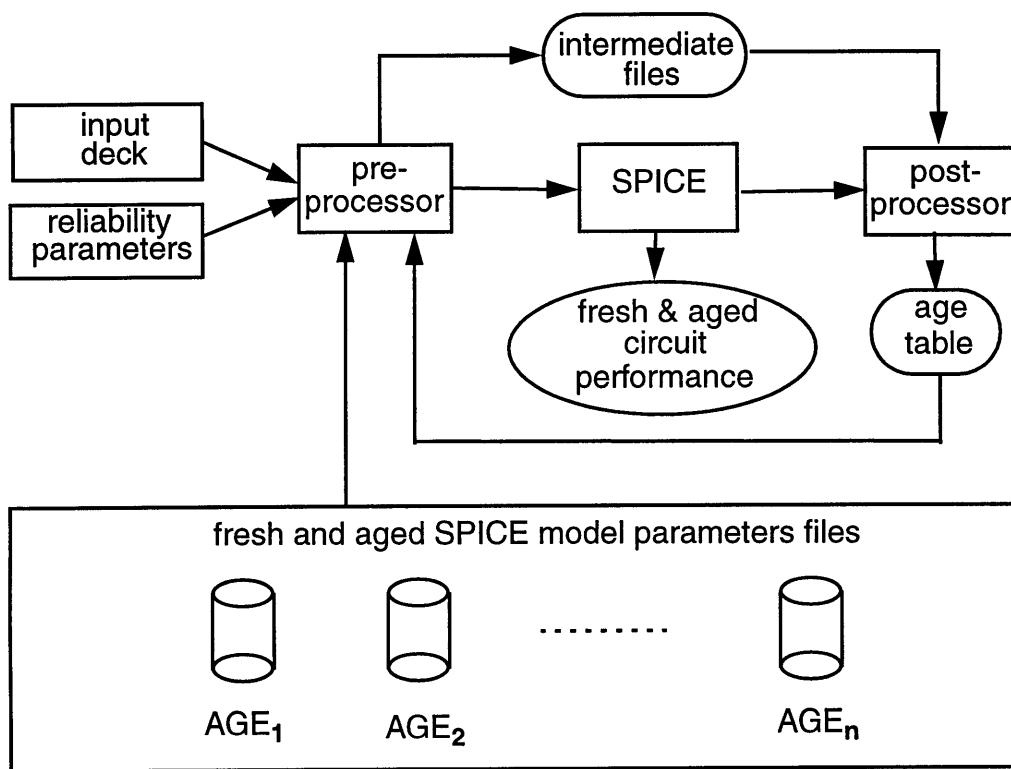
Figure 5.2   BERT simulation flow diagram

(3)   Calculate the AGE for each of the devices in the circuit of interest using Equation 5.1-5.2.

(4)   Simulate the desired circuit using the fresh device I-V parameters.

(5)   Determine the AGE(T) that each device in the circuit would have if the SPICE analysis is repeated up to the user-specified time T.

(6)   Compare the AGE(T) of each device in the circuit with that of the pre-stressed model parameter files, and calculate the new aged model parameters of the devices in the circuit by linear interpolation between the model parameters of two adjacent degradation levels.

(7)   Simulate the aged circuit behavior using SPICE with the set of aged model parameters for each device in the circuit to evaluate the impact of hot-carrier damage on circuit performance.

5.3 Experimental Methodology

AC hot-carrier effects in actual circuit environments can be better understood through the use of test structures which can monitor both post-stress device parameter degradation and circuit performance degradation. Figure 5.3 shows a circuit schematic of a ring oscillator AC test structure with fanout 1 [5.10]. The measurement methodology is the same as described in Section 3.3. The circuit hot-carrier degradation data are obtained from a set of inverter ring oscillator test structures. These ring oscillators are fabricated using two CMOS technologies A and B as described in Section 4.2. The characteristics of the ring oscillators are summarized in Table 5.1.

Figure 5.3   Circuit schematic of a ring oscillator AC test structure with fanout 1 for hot-carrier reliability evaluation.

Table 5.1: Ring Oscillator Test Structures

Technology	Fanout	Number of Stages	NMOS Sizes	PMOS Sizes
A	1, 2, 3, 6, 15	23, 23, 23, 23, 11	5 μm	10 μm
B	1, 2, 4	23, 13, 13	5 μm	10 μm

5.4 Benchmarking Calibrated AC Hot-Carrier Reliability Simulation Using Experimental Results

5.4.1 AC Degradation Model Validation

Using test circuits as shown in Figure 5.3, one can evaluate the validity of the AC degradation model directly by comparing the experimental AC degradation data with BTABERT simulation. Figures 5.4 & 5.5 compare, for both technologies, the DC-stress NMOS degradation, the 95% confidence interval bounds of the simulated AC-stress NMOS degradation, and the experimental AC-stress NMOS data for different circuit fan-outs.

For both technologies A & B, the AC experimental data is observed to fall within the 95% confidence interval for the BTABERT simulations. The general agreement between the simulated and experimental results in both Figures 5.4 & 5.5 is significant in that the simulated results were based entirely on DC-extracted model parameters with no after-the-measurement matching to the AC data.

5.4.2 AC Degradation Model Precision

Comparing Figures 5.4 & 5.5, we observe that the simulated results for Technology B have a wider 95% confidence interval than for Technology A. This is because the corresponding confidence interval for the extracted parameters **m** and **H**, as shown in Figure 4.7, happens to be larger for Technology B than for Technology A in the region of high E_{ox} where the inverters spend most of their switching time.

It is worth emphasizing that the 95% confidence intervals for the NMOS current degradation in Figures 5.4 & 5.5 were simulated without taking into account the impact of any statistical variation in either the drain and/or substrate currents. As discussed before,

these factors can introduce additional uncertainty to the simulation. As a result, the actual 95% confidence intervals in Figures 5.4 & 5.5 will likely be somewhat larger than those shown.

It should also be noted from Figure 5.4 & 5.5 that the AC experimental degradation sensitivity due to different inverter fanouts is of comparable magnitude to the sensitivity due to statistical variations in the parameters **m** and **H**. This suggests that statistical variation in the degradation model can impact the precision of reliability simulation as much as changes in the circuit design itself, and that greater reliability simulation accuracy could be obtained through optimized degradation model parameter extraction procedures.

5.5 Optimizing Degradation Model Calibration for Accurate AC Hot-Carrier Reliability Simulation

In static CMOS digital circuits, most AC hot-carrier stress occurs during switching [5.11]. This time period corresponds to only a certain limited range of stress oxide field across the NMOS device (Figure 5.6). Thus, in calibrating either the degradation or SPICE models, efforts should be focused just on those E_{ox} regions of major importance (as dictated by the digital-circuit AC voltage waveforms).

In modeling the oxide-field dependence of the degradation model parameters **m** & **H**, DC degradation data should be taken within the relative E_{ox} window estimated by prior AC circuit simulation in order to allow for more accurate and efficient interpolation and modeling. Care should be taken since, if the inverter E_{ox} window falls outside of the E_{ox} calibration range, severe extrapolation error can arise.
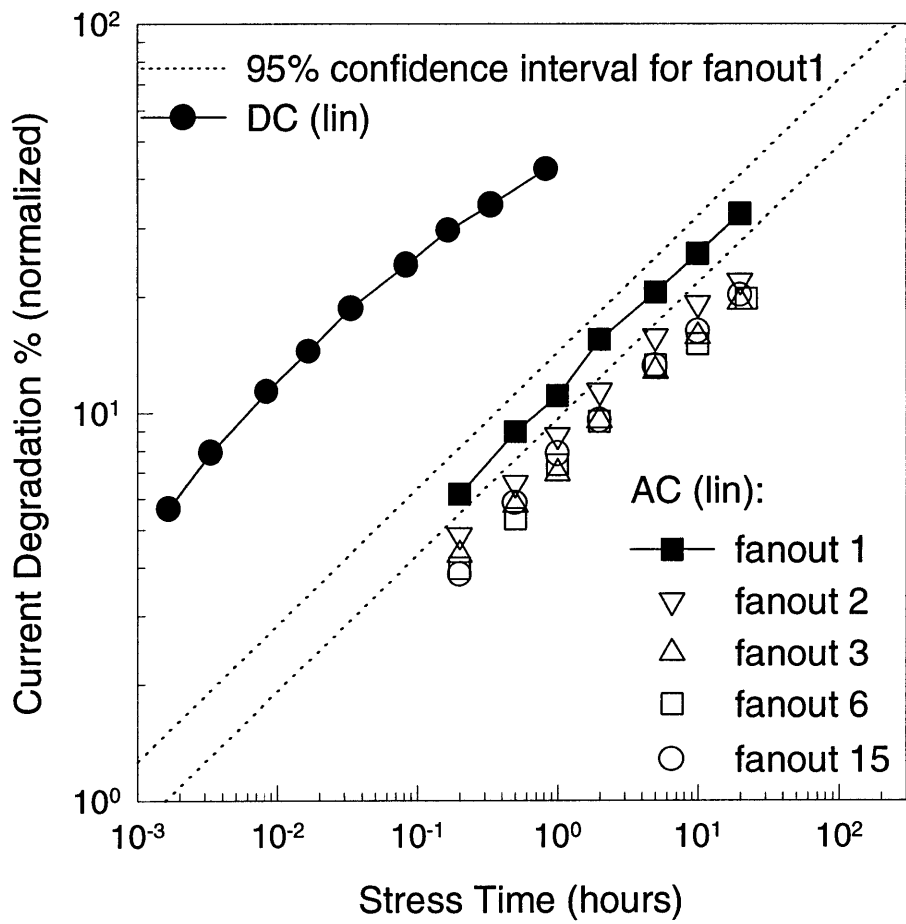
Figure 5.4   Comparison of NMOS DC and AC linear drain-current degradation for Technology A. The experimental AC current degradation values are taken from CMOS ring oscillators. The number of stages for fanout 1, 2, 3, and 6 is 23; for fanout 15, the number of stages is 11. The 95% confidence interval of ring oscillator with fanout 1 is simulated using the upper and lower bounds of the parameters **m** and **H**. The stress voltage is 4.5 V.
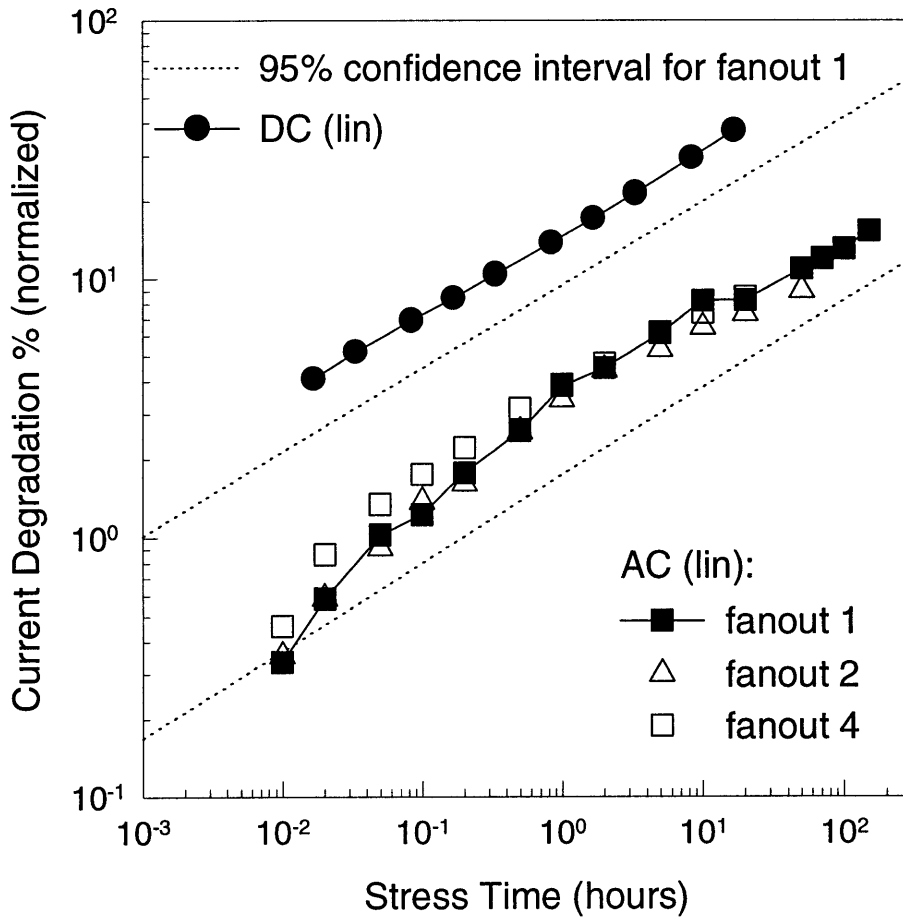
Figure 5.5   Comparison of NMOS DC and AC linear drain-current degradation for Technology B. The experimental AC current degradation values are taken from CMOS ring oscillators. The number of stages for fanout 1 is 23; for fanout 2 and 4, the number of stages is 13. The 95% confidence interval for the ring oscillator with fanout 1 is simulated using the upper and lower bounds of the parameters **m** and **H**. The stress voltage is 6.8 V.
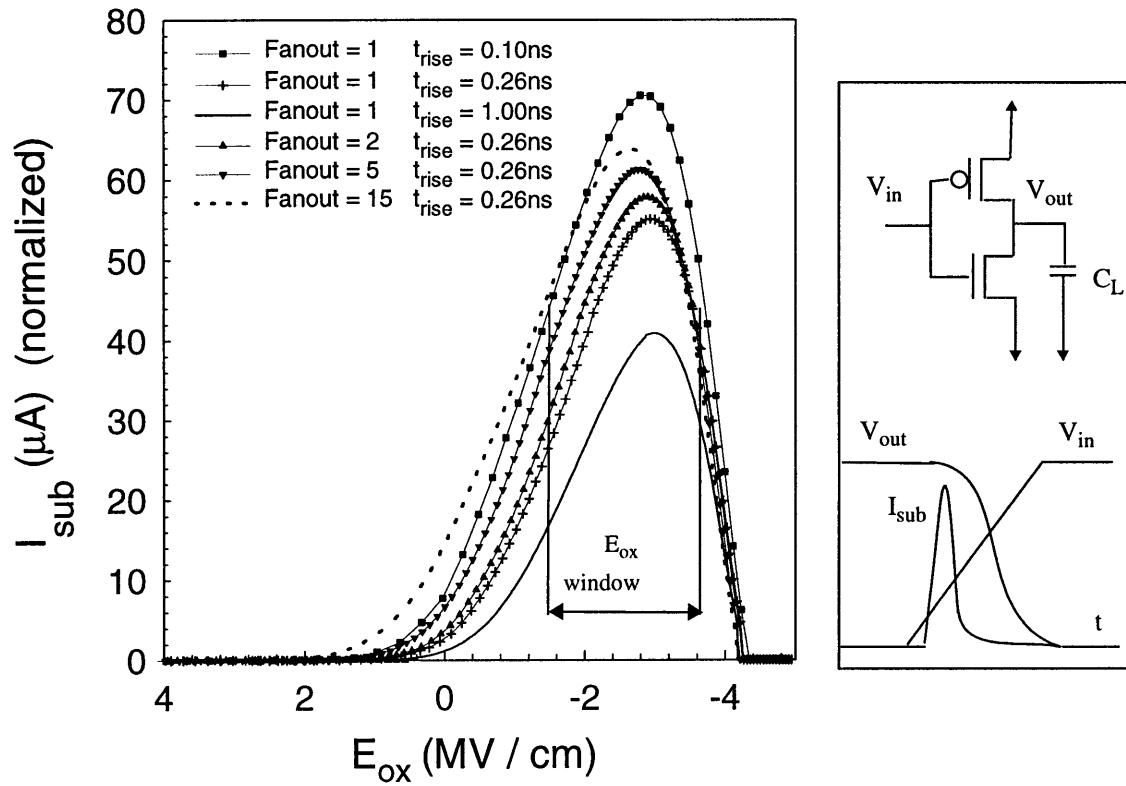
Figure 5.6 Simulated NMOS substrate current in a CMOS inverter for Technology A. The key substrate current region is not very sensitive to different input rise times and different output loads. The power supply voltage in this figure is 4.5 V.

5.6 Summary

State-of-the-art AC hot-carrier simulation models, which have been calibrated solely using DC stress data, have been benchmarked against AC test circuit data from two representative industrial technologies. The AC degradation model's statistical confidence limits have been evaluated, and the accuracy and precision of AC hot-carrier reliability simulation have been rigorously benchmarked against a comprehensive set of experimental AC circuit measurements. Statistical variation in the degradation model parameters is observed to have as much of an impact on the final degradation model accuracy as major changes in the circuit-design itself. Finally, knowledge about CMOS digital circuit behavior is shown to be useful in optimizing the calibration of both the degradation and SPICE model parameters.

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Chapter 6

Major Factors Contributing to Circuit-Level Hot-Carrier Reliability

6.1 Introduction

Existing hot-carrier (HC) reliability criteria, based on device-performance metrics alone, are too ambiguous, resulting in excessive guard-banding, sacrificed device performance, and unnecessary process complexity. Although significant work has been carried out on hot-carrier degradation modeling [6.1]-[6.3] and reliability circuit-simulation tool development [6.4]-[6.6], no consistent method yet exists as to how to assess hot-carrier lifetime in terms of more realistic circuit, rather than device, performance. What is lacking is a comprehensive understanding of the major factors that contribute to circuit-level hot-carrier reliability.

This chapter attempts to define and characterize the major factors that cumulatively determine circuit-level hot-carrier reliability and to determine each particular factor's relative importance.

6.2 Major Factors Determine Hot-Carrier Reliability

NMOS hot-carrier degradation can be modeled as shown in Equation 6.1, where I_D and I_{SUB} stand for drain and substrate currents; n, m and H are the degradation parameters; T_s is the time duration per transition; N_s is the total number of transitions or switches:

$$\Delta N_{it} \propto \left(\frac{N_s}{W \cdot H} \int_0^{Ts} I_D^{1-m}(t) \cdot I_{SUB}^m(t) dt \right)^n \qquad (6.1)$$

This degradation equation provides the link between the specific device terminal voltage waveforms and the corresponding amount of extrapolated possible oxide damage.

We consider two aspects of HC degradation. One is the degradation of individual transistors within a circuit, and the other is the effect of such degradation on circuit performance. Digital circuit-level hot-carrier reliability can be expressed as a cumulative function of the following five major Factors:

6.2.1 Factor I: Hot-Carrier Degradation Model Precision and Accuracy

From Equation 6.1, one can see that the accuracy of degradation parameters **n, m** and **H** affects the simulation results of all the transistors in the circuits. It is observed that degradation model parameters **n, m** and **H** have statistical variation. The impact of this statistical variation on hot-carrier lifetime can be assessed using the statistical confidence interval. Figure 4.7 shows the oxide-field dependence of the degradation model parameters **m** and **H** as well as their statistical confidence intervals. All measurements are performed at the wafer level and at room temperature. Each set of **m** and **H** parameters are extracted under the same oxide field. The oxide field, E_{ox}, is defined as $(V_g - V_d - V_{fb})/T_{ox}$. Details about the impact of the oxide-field dependence and statistical variation of **m** and **H** on AC hot-carrier device degradation have been discussed earlier in Section 5.4.

6.2.2 Factor II: The Specific MOSFET Terminal Voltage Waveforms

From Equation 6.1, one can see that hot-carrier degradation depends on the specific transistor terminal voltage waveforms which determine the amount of damage

created per switching transition. These terminal voltage waveforms depend on two main factors:

II (A). Circuit Topology and Operating Conditions: The terminal voltage waveforms are functions of the input rise/fall times, the capacitive loading and the particular circuit configuration [6.8]-[6.11]. Figure 6.1a shows the simulation results of the NMOS AC degradation/per transition as a function of fanout and input rise time in a CMOS inverter. Figure 6.1b compares the NMOS degradation in an inverter and in a three input NAND gate. The sizes of NMOS and PMOS devices in the circuits are $(W / L)_N = 5 / 0.6$ (um) and $(W / L)_P = 10 / 0.6$ (um), respectively. The simulation was performed at 4V. As we can see from Figures 6.1a-b, degradation is sensitive to input rise time, capacitive loading and circuit topology.

II (B). Capacitive-Coupling-Induced Voltage Overshoot: The terminal voltage waveforms are also sensitive to capacitive coupling [6.12]. This capacitive coupling includes the intrinsic coupling between the gate to the drain device terminals and the extrinsic coupling to different metal lines. The intrinsic capacitive coupling can be considered a local effect, which only involves the transistor itself. However, the voltage overshoot due to extrinsic capacitive coupling to different metal lines can be considered a more global effect. The exact amount of the overshoot depends on the relative timing of the signals on the corresponding metal lines, and the ratio of the coupling capacitance to the load capacitance [6.12]. Therefore, voltage overshoot will depend on the overall circuit input signal patterns and the relative delays of signals. It is difficult to predict when and where the voltage overshoot will occur. The information needed to calculate voltage overshoot includes the coupling capacitance value and the relative timing of the coupled signals involved.
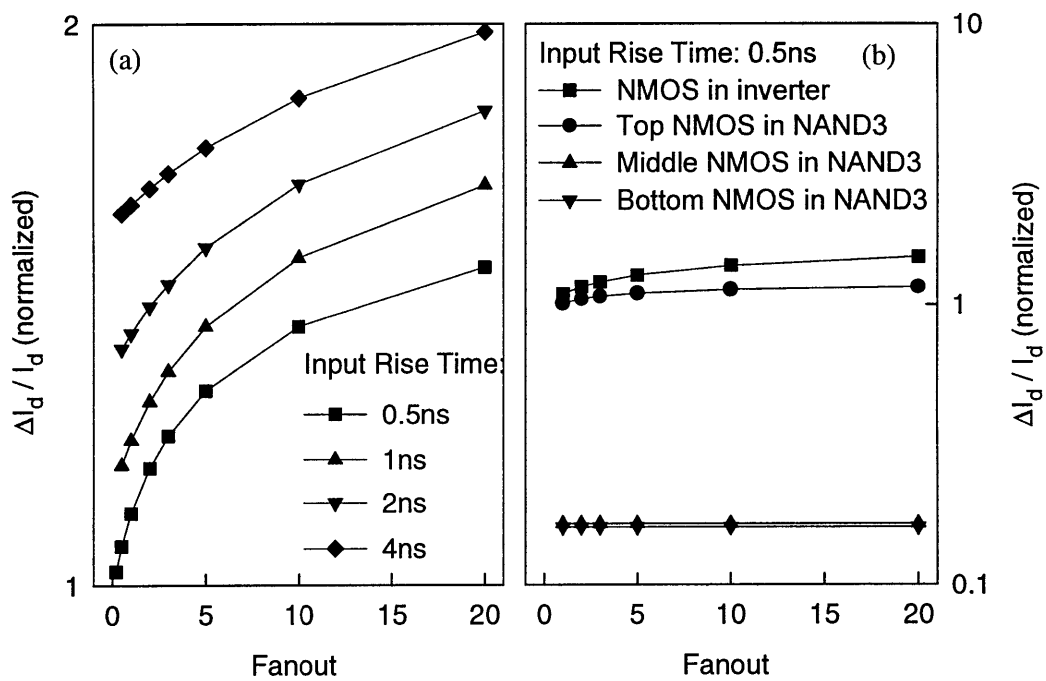
Figure 6.1   Illustration of Factor II (A). Figure 6.1(a) shows NMOS AC degradation per transition as function of fanout and input rise time in a CMOS inverter. Figure 6.1(b) compares the NMOS degradation in an inverter and in a three-input NAND gate. The simulation was performed at 4V.

Figure 6.2 illustrates voltage overshoot due to capacitive coupling. C_{p1} is the overlap capacitance between gate and drain. C_{p2} is the interconnect coupling capacitance. C_L is the fixed load capacitance. $(C_L + C_{p2})$ is total load capacitance C_{total}.

Voltage overshoot due to C_{p1} always occurs at worst-case phasing. It is more severe when the input rise time and output loading are both small. Voltage overshoot due to C_{p2} depends on the relative phase of the input (V_{in}) and coupling signal (V_{couple}) as well as the capacitive coupling ratio C_{p2}/C_{total}.

Shown in Figure 6.2b are the SPICE simulation results for output voltage overshoot due to three different C_{p2}/C_{total} ratios at the worst case phasing. The rise time for V_{in} and V_{couple} are 0.8ns and 0.4ns, respectively. The phase difference between V_{in} and V_{couple} is 0.3ns. The coupling ratio values used in the simulation are: 0 (solid line); 0.1 (dotted line) and 0.2 (dashed line).
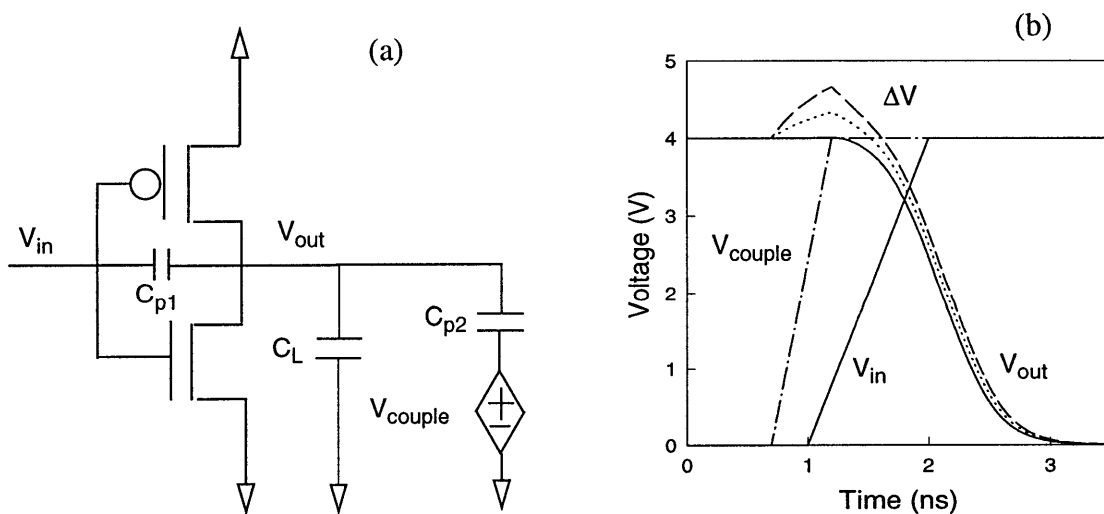
Figure 6.2   Illustration of voltage overshoot due to capacitive coupling. Power supply voltage is 4V. Transistor sizes: $(W/L)_N = 5/0.6$ (um), $(W/L)_P = 10/0.6$ (um). ΔV is the amount of voltage overshoot.

Figure 6.3 shows the impact of voltage overshoot on NMOS device linear-current degradation. As one can see, device degradation increases exponentially as the amount of voltage overshoot (ΔV) increases.
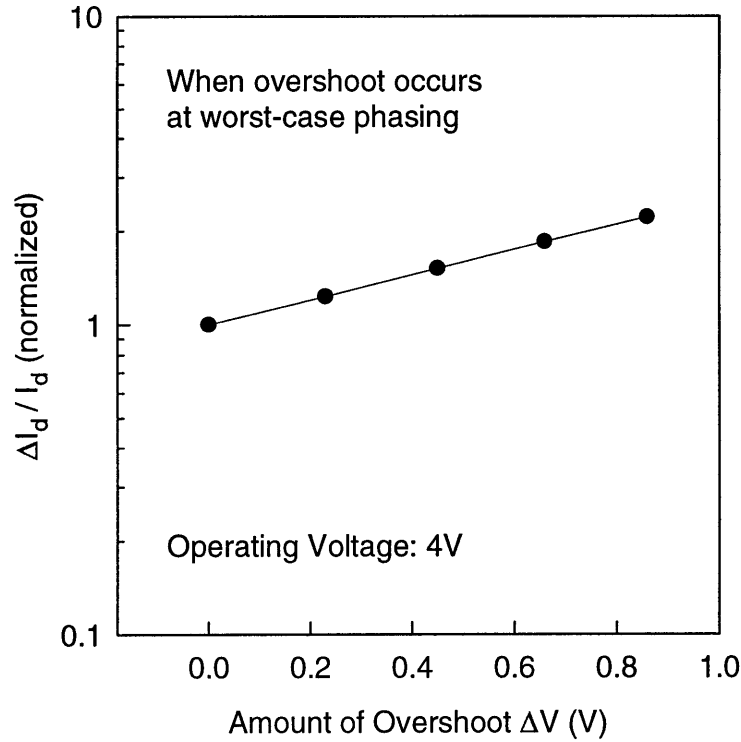
Figure 6.3   Illustration of Factor II(B). AC linear drain-current degradation as a function of voltage overshoot when overshoot occurs at worst-case

6.2.3 Factor III: MOSFET Switching Activity

Most transistor level circuit reliability simulators assume that a set of input waveforms are continuously applied to the circuit inputs. However, the influence of different input patterns also has to be taken into account. Large number of input signals are needed to obtain meaningful average effects on individual transistors. From Equation 6.1, one can see that hot-carrier degradation is proportional to the average switching

frequency of a transistor. The estimation of average switching activity can be performed using probabilistic techniques or Monte Carlo based statistical techniques [6.13]-[6.15]. The amount of switching activity depends on overall circuit input patterns as well as relative timing of each gate. Figure 6.4 shows the transition probability of a 16 bit ripple carry adder. A random input pattern is assumed in this case.
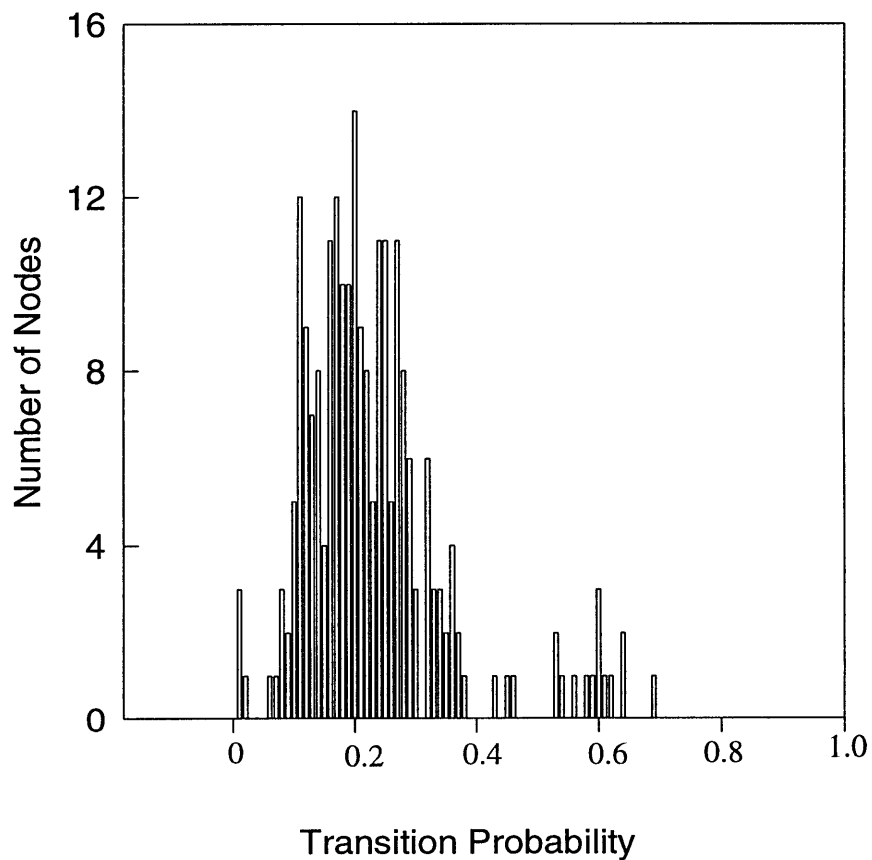
Figure 6.4   Illustration of Factor III. Switching activity in a 16 bit ripple carry adder implemented in static CMOS logic. The schematic of a one-bit adder cell for the circuit is shown in Figure 7.1.

6.2.4 Factor IV: Circuit Performance Sensitivity to Device Degradation

The circuit design determines how overall circuit performance is affected by the hot-carrier-induced degradation of individual devices. Figure 6.5 shows the circuit sensitivity to hot-carrier damage in a CMOS inverter chain with fanout 1. Depending on the particular circuit design, each circuit possesses a certain performance sensitivity to device degradation. For example, analog circuits generally have very different sensitivity to hot-carrier degradation compare to digital circuits. In addition, circuit performance may be more sensitive to some "critical" devices in the circuit than to other devices. For example, a certain transistor T1 may experience 25% drain current degradation but affect the circuit output minimally, while another transistor T2 may suffer only 5% degradation and yet cause substantial degradation in circuit performance. In general, different classes of circuit applications display different sensitivities to hot-carrier-induced device degradation; different circuits also have different "critical" devices which contribute significantly to circuit performance degradation.

6.2.5 Factor V: Relative Importance of the Degraded Circuit Paths

In order to meet specified performance requirements over the lifetime of products, critical paths of circuits need to be evaluated to satisfy timing constraints before and after hot-carrier degradation. Since the amount of hot-carrier-induced degradation depends on specific circuit design and operating conditions, hot-carrier degradation can change the relative importance of circuit critical paths.

6.3 Summary

Factors I-III determine both the magnitude and distribution of hot-carrier-induced oxide damage throughout the circuit. Factors IV and V determine how this created

damage impacts overall circuit performance. Depending upon the particular technology or

circuit design, each of the above reliability Factors can vary significantly in magnitude,

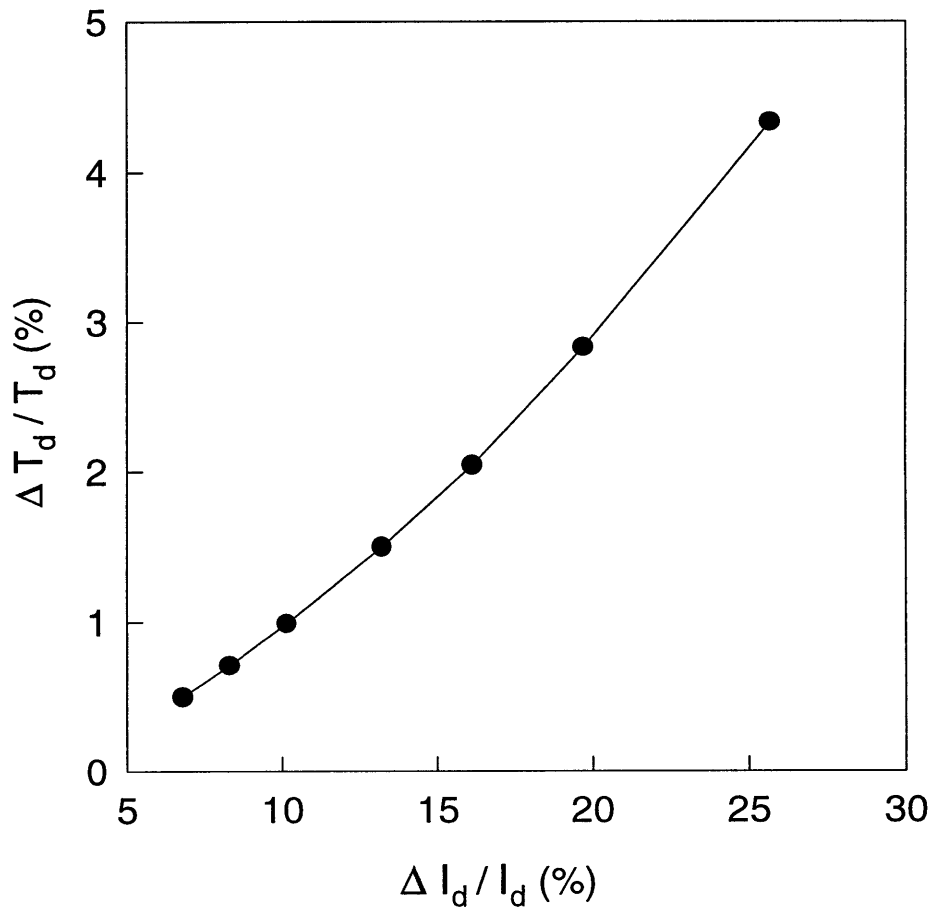having a different impact on the estimated lifetime.

Figure 6.5   Illustration of Factor IV. Circuit sensitivity to hot-carrier damage in a
CMOS inverter chain with fanout 1. The operation voltage is 4V. (W /
L)$_N$ = 5 / 0.6 (um) and (W / L)$_P$ = 10 /0.6 (um).

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Chapter 7

Assessing Hot-Carrier Lifetime Based On "Worst-Case" Approximations

7.1 Different-Levels of Approximation

The degree of lifetime-underestimation/criteria-overspecification strongly depends on the realism of each Factor's "worst-case" approximations. If insufficient data about a Factor exists, then more conservative "worst-case" approximations must be adopted, resulting in greater lifetime-underestimation. However, with sufficient data, more realistic "worst-case" approximations can be used, reducing lifetime-underestimation. Note, that acquiring detailed device/circuit information may not always be feasible (e.g. there is a circuit-size limit to practical SPICE-level simulation; higher-level simulation tools have reduced model accuracy). Thus, each reliability Factor possesses an inherent trade-off between its degree of realism and its ease of evaluation.

In this chapter, the inherent inverse relationship between lifetime-underestimation/ criteria-overspecification and the amount of known device/circuit information will be explored. Lifetime-underestimation/criteria-overspecification is shown to depend quite strongly on the particular "worst-case" approximations used. Each of the above concepts will be illustrated using representative circuit examples and case studies.

For Factors II-IV, Table 7.1 lists different "worst-case" approximations along with the corresponding required level of device/circuit information. Approximation (A) is the most conservative; (B) is more realistic, etc. Depending upon the level of approximation chosen for each Factor, a wide range of different lifetime values can be calculated.

Table 7.1: Worst-Case Approximations

Reliability Factor	Different Levels of "Worst-Case" Approximation	Necessary Device/ Circuit Data
II. The Specific MOSFET Terminal Voltage Waveforms	(A1) Determine device-level "worst-case" DC stress condition (A2) Apply this DC stress condition identically to all devices	(A) Device-level stress data
	(B1) Determine "worst-case" AC hot-carrier stress per switching-transition over circuit's design/ operating space (B2) Apply this AC stress condition identically to all devices	(B) All of (A) plus AC hot-carrier reliability simulation
	(C1) Evaluate AC hot-carrier stress per transition over circuit's design/operating space (C2) Back-annotate each device with its specific AC stress condition	(C) All of (B) plus circuit back-annotation of AC stress information
III. MOSFET Switching Activity	(A1) DC stress condition implies 100% duty cycle	(A) None
	(B1) Use operating clock frequency	(B) Basic circuit operating condition
	(C1) Determine "worst-case" circuit switching activity value (C2) Apply this switching activity value identically to all devices	(C) All of (B) plus switching activity evaluation
	(D1) Evaluate circuit switching activity distribution (D2) Back-annotate each device with its specific switching activity	(D) (C) plus circuit back-annotation of specific switching activity
IV. Circuit Performance Sensitivity to Device Degradation	(A1) Evaluate device degradation over range of possible stress conditions determined from Factors I-III (A2) Simulate performance sensitivity using "worst-case" age for all devices	(A) Parameter extraction for stressed devices and circuit performance simulation
	(B1) Evaluate device degradation over range of possible stress conditions determined from Factors I-III (B2) Back-annotate each device with its specific degraded I-V characteristic (B3) Simulate circuit performance sensitivity	(B) All of (A) plus circuit back-annotation of degraded device characteristics and circuit performance simulation

7.2 Illustrated Case Studies

The above concepts can be illustrated using an example of a 4-bit ripple-carry adder implemented in static CMOS logic. Figure 7.1 shows the circuit schematic of a one-bit adder cell. The circuit and reliability simulation tools [7.17] were calibrated using experimental data from a representative 0.6um N-well CMOS technology. The circuit-level reliability criteria for this case study was defined as a 3% reduction in the critical path delay.
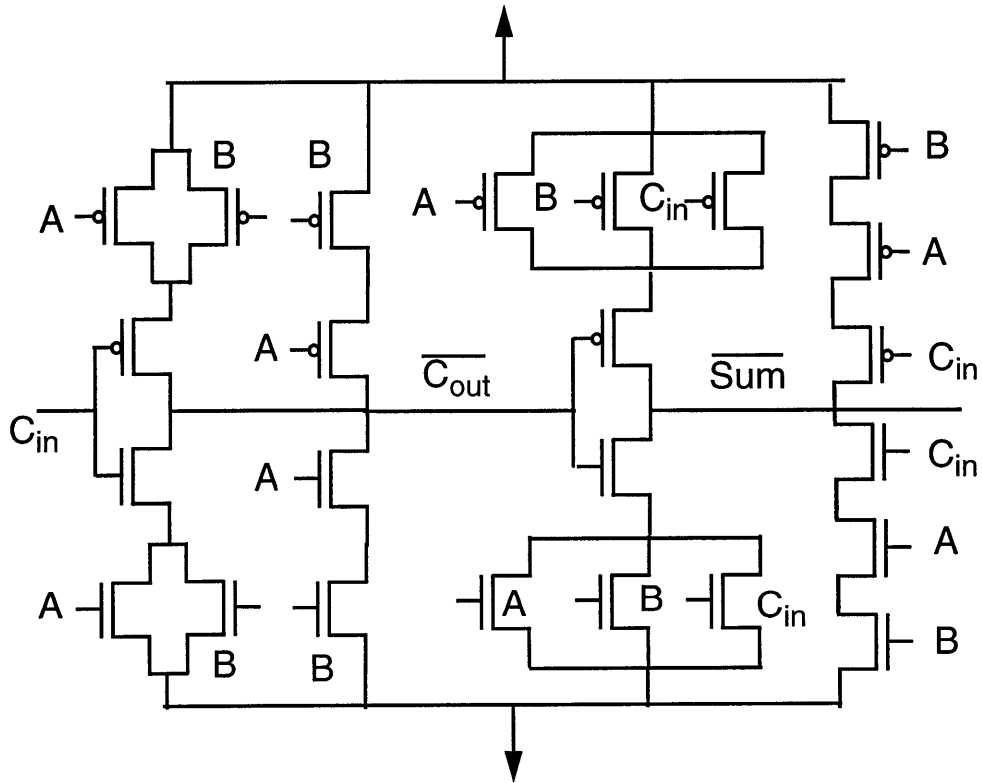

Figure 7.1   Schematic of a one-bit mirror adder cell. Transistor sizes:
$(W/L)_N = 5/0.6$; $(W / L)_P = 10/0.6$.

Table 7.2 summarizes four different case studies, the specific assumptions used for the reliability Factors II-IV, and the corresponding normalized lifetime values.

Table 7.2: Case Study Results

Case Study	Reliability Approximations Used			Life time
	Factor II	Factor III	Factor IV	
#1:	(A1, A2): $V_G = 2V$, $V_D = 4V$	(A1): Duty cycle = 100%	(A1): 20% ($\Delta I_D / I_D$ lin)	1
#2:	(B1, B2): "Worst-Case" stress per transition: 3×10^{-22} at $V_{CC} = 4V$	(B1): Clock frequency = 200MHz	(A2): 3% ($\Delta T_d / T_d$)= 18% ($\Delta I_D / I_D$ lin)	23
#3:	(C1, C2): Distribution of stress per transition: between 1.2×10^{-25} and 3×10^{-22} at $V_{CC} = 4V$	(B1): Clock frequency = 200MHz	(B1, B2, B3)	148
#4:	(C1, C2): Distribution of stress per transition: between 1.2×10^{-25} and 3×10^{-22} at $V_{CC} = 4V$	(D1, D2): Back-annotate switching activities of each device	(B1, B2, B3)	344

[*] Lifetime is normalized to case study #1.

Case study #1 assumes that each device in the ripple carry adder is stressed at the "worst-case" DC stress condition. This assumption implies that the following approximations are made in Table 7.1: (A1, A2) of Factor II, A1 of Factor III and A1 of Factor IV. If the lifetime criteria is defined as 3% delay degradation in the adder's critical path, then the normalized lifetime for this case is 1.

Case studies #2-4 assume more and more realistic "worst-case" approximations, resulting in less and less lifetime underestimation.

Case study #2 evaluates the different amounts of gate-oxide damage resulting from each switching transition over a wide range of circuit topologies and operating conditions for each MOSFET in the circuit of Figure 7.1. The value of the "worst-case" damage per transition is identified and is assumed to apply to each MOSFET in the circuit. To

determine the hot-carrier lifetime, this "worst-case" value is then multiplied by the total number of clock cycles required to reach failure. This assumption implies that the following approximations are made in Table 7.1: (B1, B2) of Factor II, B1 of Factor III and A2 of Factor IV. Note, by applying one "worst-case" value to every device within the circuit, no "back-annotation" (the assigning of specific data to individual MOSFETs) is required. By accounting for the AC nature of the hot-carrier stress, the lifetime underestimation is reduced (compared with the DC estimate) by a factor of 22.8.

Case study #3 is identical to #2 except that now the specific damage per transition value is used for each MOSFET in the circuit (rather than the uniformly applied "worst-case" value). This assumption implies that the following approximations are made in Table 7.1: (C1, C2) of Factor II, B1 of Factor III and (B1, B2, B3) of Factor IV. Although this approximation is more realistic, this method now requires "back-annotation", necessitating a considerable increase in computation and simulation effort. This more realistic accounting for the AC hot-carrier stress conditions reduces the lifetime underestimation by a further factor of 6.5.

As mentioned in previous section, not every MOSFET in a circuit switches at the clock frequency (or undergoes AC degradation every cycle) as is assumed in the prior AC case studies. Case study #4 is identical to #3, except that now, the more realistic switching activity of each individual MOSFET is evaluated and taken into account in the calculation of device degradation. Therefore, additional back-annotation is required. This assumption implies that the following approximations are made in Table 7.1: (C1, C2) of Factor II, (D1, D2) of Factor III and (B1, B2, B3) of Factor IV. This additional analysis reduces the lifetime underestimation by a further factor of 2.3.

7.3 Summary

By making more realistic "worst-case" assumptions, the amount of hot-carrier lifetime underestimation/criteria-overspecification can be significantly reduced. However, the more realistic the "worst-case" assumptions, the more device/circuit information required, and the more effort that needs to be expended. Understanding these trade-offs provides insight in deciding where reliability assessment efforts would be most productively allocated.

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Chapter 8

Summary and Future Work

8.1 Summary

The goal of this research is to contribute to the assessment of hot-carrier reliability in digital CMOS circuits. Several critical issues that face circuit-level hot-carrier reliability evaluation have been investigated, including AC hot-carrier test circuit design and characterization, AC hot-carrier degradation model calibration, the major factors determining circuit-level hot-carrier reliability, and the trade-offs between circuit-level hot-carrier lifetime underestimation and the amount of information required.

Hot-carrier reliability assessment is undergoing a rapid transition from a conservative, device-level approach, to a realistic circuit-level approach. In this transition, one of the most important questions is whether AC hot-carrier degradation can be predicted based on the DC degradation model. If the AC degradation results agree with the prediction based on DC measurements, then AC degradation can be modeled as a quasi-static process. However, if the AC hot-carrier degradation behavior can not be predicted by the DC degradation model, then new physical insights need to be obtained to understand the cause of the deviation. The only way to answer this question is to obtain experimental AC hot-carrier degradation results under realistic circuit operations and compare then directly to the predictions based on calibrated hot-carrier reliability simulation.

This thesis provides a comprehensive understanding of the key issues in designing and characterizing hot-carrier reliability test circuits. These circuits can operate under

realistic stress voltage waveforms and allow access to the internal device nodes to obtain device I-V characteristics before and after hot-carrier degradation. These circuits can also be used relate the circuit performance degradation to device degradation. Insights about previous test circuit designs are presented and additional test circuit designs are demonstrated. The design trade-offs between realistic waveform generation and internal device accessibility are analyzed and clarified. Recommendations for optimal test-circuit design for hot-carrier reliability characterization and model calibration are proposed.

This thesis also examines key issues involved in the calibration and verification of the hot-carrier degradation models used for simulating AC circuit-level reliability based on device and circuit data from two representative industrial technologies. First, the need to account for the stress drain oxide-field dependence of the degradation model coefficients extracted from DC device-level stress measurements is demonstrated. Second, the statistical confidence limits of the extracted degradation model parameters are analyzed. Third, the sensitivity of degradation to drain and substrate current modeling errors is examined. Fourth, the AC degradation model's statistical confidence limits are evaluated, and the accuracy and precision of AC hot-carrier reliability simulation, which has been calibrated solely by model parameters extracted from DC device stress experiments, is rigorously benchmarked against a comprehensive set of experimental AC circuit measurements. Finally, knowledge about CMOS digital circuit behavior is shown to be useful in optimizing the calibration of both the degradation and SPICE model parameters. Specific recommendations are made about improving the consistency and accuracy of both degradation and SPICE model parameter extraction.

Finally, this thesis identifies the major factors that cumulatively contribute to circuit-level hot-carrier reliability. The inherent inverse relationship between lifetime-

underestimation/criteria-overspecification and the amount of known device/circuit information has been explored. Lifetime-underestimation/criteria-overspecification has been shown to depend quite strongly on the particular "worst-case" approximations used. Each of the above concepts have been illustrated using representative circuit examples and case studies.

Experimental and simulation methodology that we have provided in this thesis can serve a wide range of needs, such as AC hot-carrier model verification, circuit lifetime prediction, technology qualification and understanding technology and circuit design trade-offs from a hot-carrier perspective.

8.2 Future Work

All the reliability simulation tools developed so far have been based on transistor-level circuit simulators. These simulators are useful for detailed analyses of circuit nodes. However, they cannot be used to analyze large circuits of several million transistors due to the long simulation time. In addition, these simulators can not provide information about all the major factors that contribute circuit-level reliability in an automated and integrated way. Thus, higher-level reliability simulator need to be developed, which take into account the factors such as switching activity, voltage overshoot and circuit sensitivity to hot-carrier degradation, etc.