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ANALYSIS OF CIRCUITS WITH MULTIPLE-HOLE MAGNETIC CORES

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
RESEARCH LABORATORY OF ELECTRONICS
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Lubomyr S. Onyshkevych

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Abstract

Multiple-hole magnetic cores, also called transfluxors, which have been developed recently, promise to be very useful in computer, control, and other logical circuitry. They are ferrite cores, with square hysteresis loops, of various complicated geometries.

In this report, a workable analysis procedure for circuits that contain transfluxors is developed; it is based on the square-waveshape approximation. This analysis forms a basis for a design procedure. Sample circuits were designed and tested, and the results were found to be within 10 per cent of the predicted values.

The main problems in circuit design were flux division and loading effects. Diode elimination presented another problem, which is treated at some length in this report. Diodeless operation of a transfluxor circuit was found to be possible, but slow, unreliable, and critical.

In the field of logical design, a symbolic notation was developed, and an approach to design was made, using "gate boxes."

A description of the physical properties of transfluxors is given; it includes some new, unpublished, special effects encountered with multiple-hole cores.

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I. INTRODUCTION

1.1 History

In recent years, a great deal of work has been done in the field of ferromagnetism. Numerous devices and new magnetic materials have been developed and perfected. Among the most important are the square-loop materials; that is, materials that have an approximately rectangular hysteresis loop (40). Two kinds of magnetic material that can be made to exhibit this desirable property are in general use: tape-wound, thin-metal cores and ferrites (39, 45). Currently, a new material – thin film – is being developed (46).

Many applications of square-loop materials have been found in the field of computing and control. The development has taken two directions: magnetic amplifiers (22, 23, 24) (circuits using a carrier frequency) and pulse applications (circuits using pulses and no carrier). Only pulse circuitry is discussed in this report.

The first applications of magnetic pulse circuitry were made in the field of information storage. Magnetic shift registers (26, 27, 28) and huge magnetic-core memory matrices (30, 34, 35) have been developed and are being used in most modern computers. Here, the trend is towards bigger, faster, cheaper memories, with the result that new magnetic storage elements are constantly being announced (31, 37). Notable among them is the multiple-aperture ferrite plate (36, 32).

Also, much work has been done on logical-circuitry applications of magnetic cores (19, 16, 20, 15). The object was to develop various logical gating circuits, as well as complete arithmetic units for computers and similar devices. In this area, the efforts were less successful; magnetic cores require coupling diodes and high-current drivers, and are not particularly fast. It was evident that if applications of magnetic cores were to become practical, new kinds of magnetic elements would have to be developed.

Until 1955, the magnetic cores in use were of simple toroidal shape. Then Rajchman of the RCA Laboratories announced a new kind of magnetic core, the Transfluxor (7, 8), which was basically a multiple-hole magnetic core made out of ferrite. This core could do anything that the simple cores could do (for example, in many instances, a single transfluxor could be used in place of several toroidal cores), and it permitted new applications. It could be used as an analog device, operating like a magnetic amplifier with electrically controllable magnetic setting. Also, it could be used as a complicated gate and, therefore, offered the possibility of eliminating diodes from logical magnetic circuitry.

Since that time, investigation on complicated core geometries has been undertaken by various groups; many interesting facts have been uncovered, and useful devices designed. The Potter Instrument Company has designed "Magnistors," which use both square-loop material and soft iron in the same core (6); International Business Machines Corporation has developed four-legged memory cores (4, 5); the General Electric Company has done some very interesting transfluxor research (1, 3); and new facts also

have been forthcoming from Radio Corporation of America, notably the principle of current steering (9). In addition, some work on multiple-hole cores has been done in other countries, especially Germany (2). Work on multiple-hole cores has also been going on at the Research Laboratory of Electronics, M.I.T.; this report describes the first results of this work.

1.2 Objectives

The primary objective of the research undertaken for this study was the development of a method of analysis of logical circuits containing magnetic cores with complicated geometries. It is hoped that from this work a method of synthesis will ultimately result – one that will make possible simple design procedures of large logical systems consisting of such cores. Only logical circuits (including shift registers) are considered; the investigations reported here concern pulse-type application (no carrier) exclusively, and binary digital applications are of prime importance.

In order to understand better the behavior of transfluxors and transfluxor-like devices as circuit components, an investigation into the properties of the core itself was undertaken. In the course of this research, many new facts were brought to light, and theories about them were formulated. Some of those facts have, in the meantime, been discovered and reported by others; some are entirely new. A discussion of all of them and a general background discussion of magnetic cores comprise the second section of this report.

The third section is concerned with the logical design and analysis of multiple-hole magnetic-core circuits, especially with the development of a symbolic system of notation. An attempt to summarize the logical functions obtainable from a few particularly useful forms is also included.

In the fourth section, the knowledge gained from investigation of the properties of transfluxors is utilized to formulate an approximate method of analysis of transfluxor circuits. From this analysis, a design procedure is deduced; sample circuits have been designed and physically tested on the basis of this procedure. The experimental results are compared with expected behavior. An attempt to account for the discrepancies between theory and practice concludes the section.

The fifth section summarizes the results and suggests the paths that, in the opinion of the author, should be pursued in future investigation.

1.3 Experimental Setup

Many different kinds of cores were used in this research, including both simple toroidal and complicated multiple-hole cores. Some of them are illustrated in Figs. 1 and 2. Multiple-hole cores either were obtained directly from RCA or IBM, in which case they were of formed and sintered ferrite, or were drilled with a supersonic drill from blanks obtained from the M.I.T. Lincoln Laboratory.

The cores were tested statically on the static hysteresis curve plotter at the M.I.T.

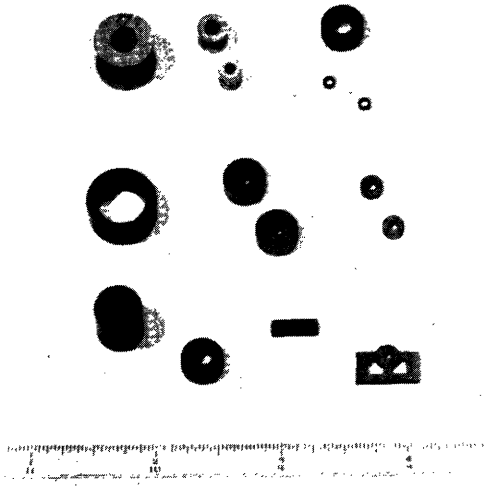


Fig. 1. Some of the cores used in this investigation.

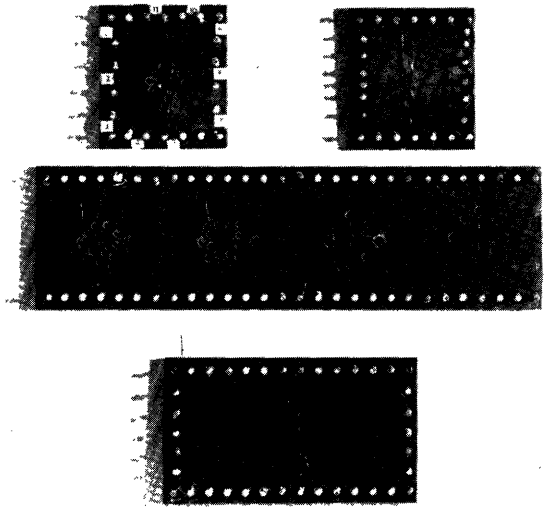


Fig. 2. Examples of wired cores.

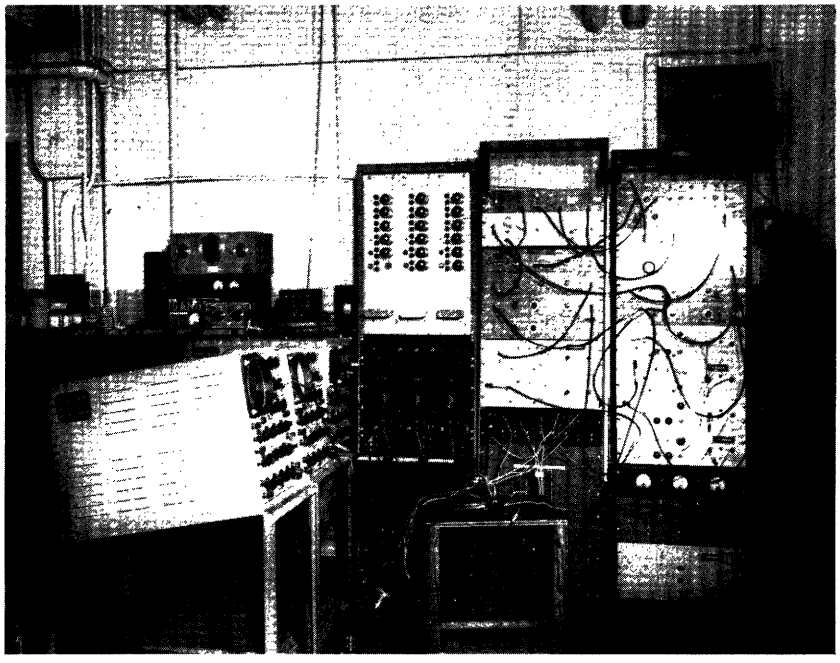


Fig. 3. Experimental setup.

Insulation Research Laboratory as well as dynamically with trains of sharp high-current pulses obtained from the flexible experimental setup assembled and partially built at the Research Laboratory of Electronics. This setup was also used to test complete circuits and for many other purposes. Figure 3 shows the pulse equipment used.

II. PHYSICAL PROPERTIES OF MULTIPLE-HOLE CORES

2.1 Introduction

At the present time, no adequate quantitative theory of physical behavior of a simple core during switching conditions exists, and there is virtually no theory of behavior of multiple-hole cores. In this section, the behavior of the transfluxor, its special effects, and modes of operation are discussed qualitatively. A brief explanation of a simple core is first necessary.

2.1.1 Domains

According to the domain theory of magnetism (38, 41, 42, 43), a ferromagnetic material contains magnetic dipoles that result from unbalanced electron spins. In a small region of the ferromagnetic material, all of the dipoles are parallel and held aligned in the same direction. The forces that hold them in alignment are very powerful, but as yet not completely understood.

The small region of the ferromagnetic material is called a "domain." Each domain is completely magnetized in some direction at all times because all of the magnetic moments are both parallel and in the same sense. However, in some materials, some of the dipoles are antiparallel; such a material is termed "ferrimagnetic." If, in a

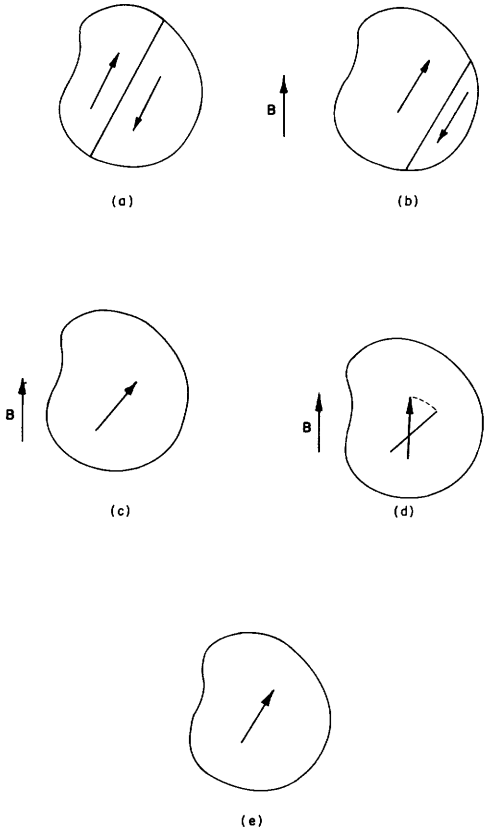


Fig. 4. Domains and switching.
(a) Magnetic material consisting of two domains;
(b) growth of left-hand domain caused by applied magnetic field, B;
(c) all material in left-hand domain after switching by field B;
(d) further magnetization possible only by rotation of flux direction inside the domain;
(e) after removal of external field, domain returns to preferred direction of magnetization and is now in magnetized state.

ferrimagnetic material, all of the antiparallel dipoles exactly balance each other, so that each domain has no net magnetic moment, we term the material "antiferromagnetic."

In a crystalline material, there is usually a preferred direction of magnetization along some crystal axis; this is called "crystalline anisotropy." There can be more than one preferred direction. Moreover, in a polycrystalline material, the crystals themselves can be oriented randomly so that, as a whole, the material may be nonoriented, even though each domain is anisotropic.

Domains are separated by the so-called "domain walls" or "Bloch walls," which are several hundred atoms thick. The walls can move, making one domain larger at the expense of other domains. (See Fig. 4.)

Figure 4 shows a simple explanation of magnetization of a ferromagnetic material. The idea to bear in mind is that, even though each domain is always completely "saturated," the specimen as a whole may be demagnetized because all of the disoriented fields of the individual domains cancel each other.

2.1.2 Ferrites

All of the multiple-hole cores used in this investigation, as well as most of the toroidal cores, were ferrite (44). Ferrite (45) is a ferrimagnetic (48) ceramic material with the general chemical formula:

$$M^{2+}\,O \cdot M_2^{3+}\,O_3$$

where the metal M can be iron, nickel, zinc, manganese, or magnesium, in various proportions. By choosing the proportions of metals correctly, as well as by firing the core in the correct way, the desired characteristic properties of the material can be obtained. For square-loop applications, the ferrites are usually of the MgMn type (45).

2.2 Behavior of a Simple Core

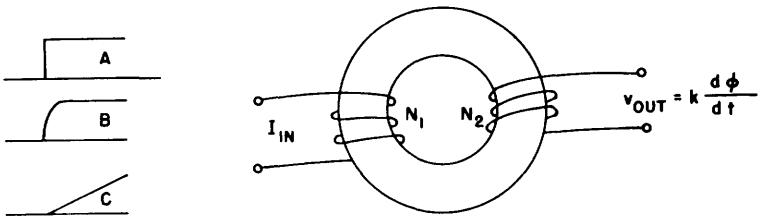
2.2.1 Hysteresis Loop

An idealized hysteresis loop is shown in Fig. 5b. To obtain this loop the core is wired as shown in Fig. 5a. A current is applied on winding N_1, and the voltage across winding N_2 is observed. From these measurements, we can compute the variables H and B at the time T because

$$H\,[\text{oersteds}] = 0.495\,\frac{N_1 I}{L}\left[\frac{\text{ampere-turns}}{\text{inch}}\right] \tag{1}$$

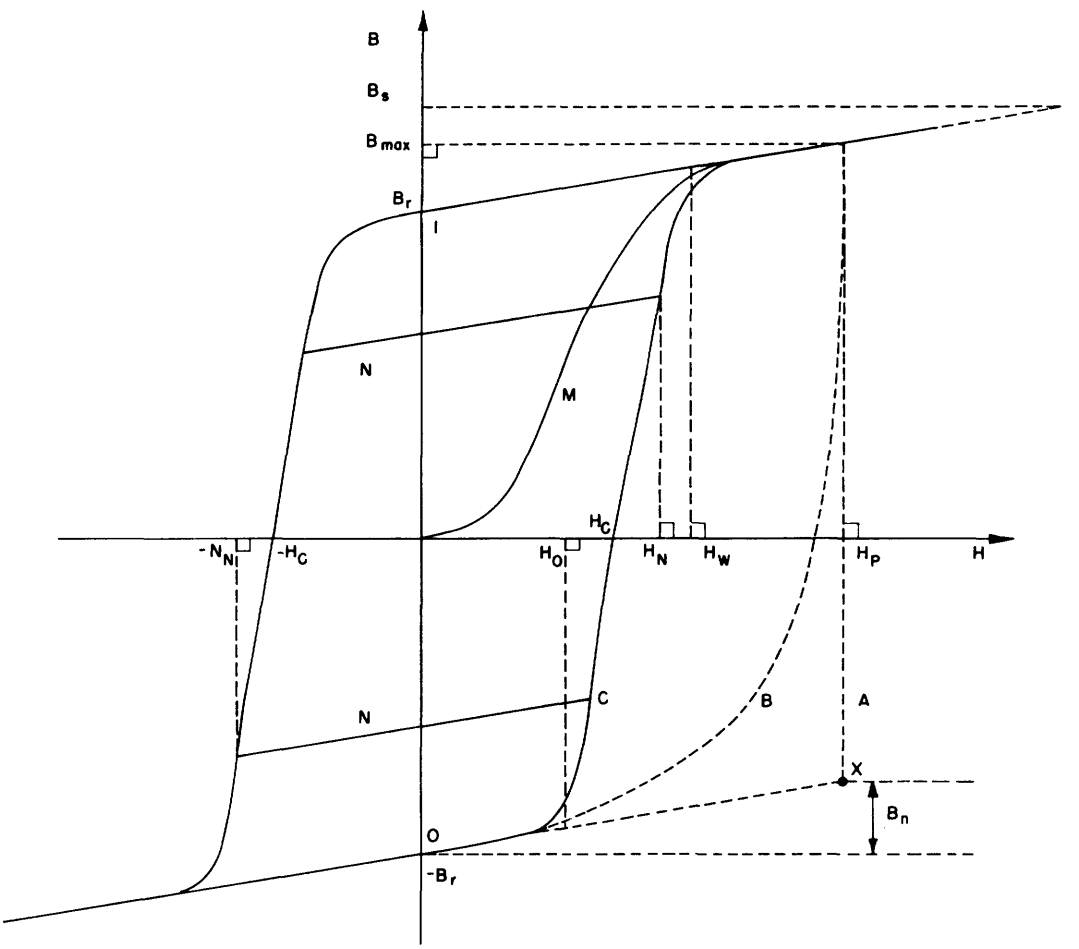
while

$$B\,[\text{gauss}] = \frac{1.550 \times 10^7}{N_2 \times A}\int_{-\infty}^{T} v\,dt\left[\frac{\text{volt-seconds}}{\text{turns-inch}^2}\right] \tag{2}$$



A SIMPLE CORE

(a)



IDEALIZED HYSTERESIS LOOP

(b)

Fig. 5. Switching of a simple core.

where

N_1 = number of turns in winding N_1

N_2 = number of turns in winding N_2

I = applied current

L = length of path, inches

A = cross-section area, $inch^2$

v = output voltage

Ampere-turns and volt-seconds often are used as units of measurement instead of oersteds and gauss.

If the core is completely demagnetized, and then a positive H-field is applied, we travel along the initial magnetization curve M until saturation is reached. When the current is released, the flux will return to the remanent flux B_r. Arbitrarily, we can assign to this point state the number "1". If we now apply a current of opposite polarity, the core will switch into the negative saturation $-B_r$, and after the release of current stay in the state "0". Thus we have achieved a memory – a bistable device. The core can be switched back and forth between states 1 and 0, provided, of course, that the applied H-field is large enough to cause saturation in each direction. If it is not, then the magnetization may follow some minor hysteresis loop like the one marked "N" in Fig. 5b. If the H-field is not large enough to force the magnetization over the knee of the hysteresis loop (H_O), no switching at all will result. Thus the "coercive force" H_C gives some indication of the amount of current to be employed.

The core takes a finite amount of time to switch from state to state. Therefore, if we employ a sharp, fast pulse, the core is not able to follow instantaneously. Therefore, we actually never switch along the hysteresis loop C, called the "static loop," unless the current is applied in the form of a very slow, almost dc ramp. At the other extreme is a current step that causes the core to go along path A. In between we get paths like B, which are normally caused by steps with finite, but fast, rise times.

The ratio

$$s = \frac{B_r}{B_s} \tag{3}$$

is called the "squareness ratio" and is a figure of merit of the material; for a good, square loop, it should be of the order of magnitude of 0.9 - 0.95. Another definition of squareness ratio is:

$$s = \frac{B_{max}}{B_r} \tag{4}$$

where B_{max} corresponds to $H_P = 2H_C$. This is a much more useful definition.

2.2.2 Voltage Waveform

While the core is being switched from one remanent state to the other, a voltage

$$v = k\frac{d\phi}{dt} \tag{5}$$

appears across the winding N_2. The waveshape of this voltage is shown in Fig. 6a. There is no good quantitative explanation of this waveshape; qualitatively, we can explain it (see Fig. 6b) as follows. [This explanation is due to H. K. Rising, and also to W. M. Breckenridge (13).]

Let us suppose that the core was originally in state O and that we applied a sharp current step that tended to reverse the core. The domain walls cannot move instantaneously; we follow path A in Fig. 5b, as explained previously. In this region, magnetization is caused by initial rotation of domains, which is much faster than wall movement. Thus in a very short time, point X is reached, causing a change in flux B_n. This causes the sharp spike at the beginning of the voltage waveform, labeled "O" in Fig. 6b. Afterwards, correct switching of the core produces the bulk of the waveform P. The peak of this part of the waveform is reached when the H axis is crossed. Obviously, the voltage waveform is asymmetrical.

After the current is released, the flux falls to B_r at the "1" point (Fig. 5b). A negative voltage spike R occurs, which has an area proportional to $B_{max} - B_r$.

If the applied H_P is very much larger than H_C, parts O and P come closer and

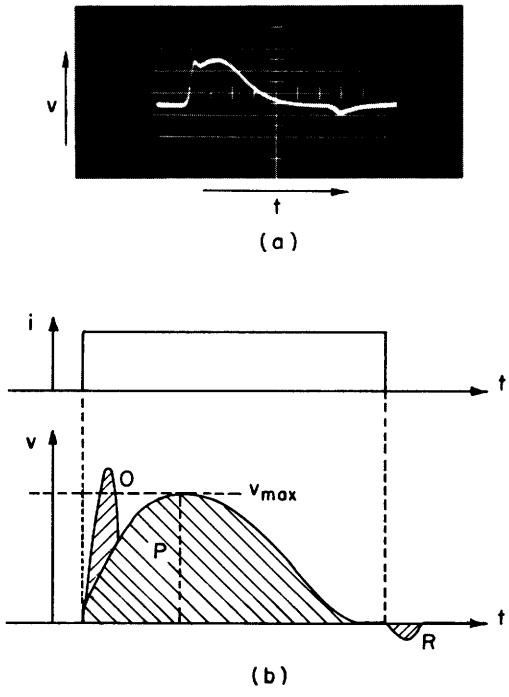


Fig. 6. Switching waveform.

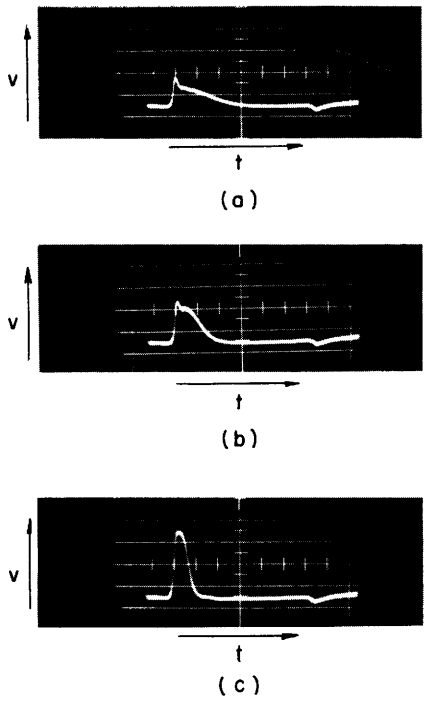


Fig. 7. Switching waveform at various values of switching current.
(a) IN = 1.2 ampere turns;
(b) IN = 1.6 ampere turns;
(c) IN = 2.0 ampere turns.

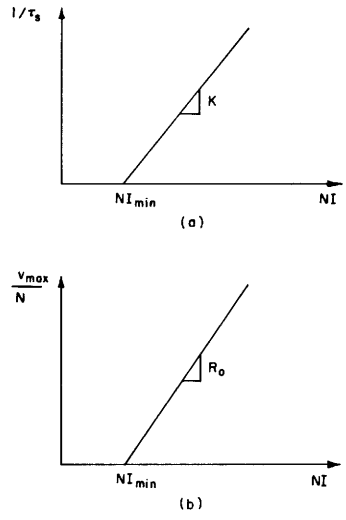


Fig. 8. Switching characteristics.
(a) Inverse of switching time vs. ampere turns;
(b) peak voltage/turn vs. ampere turns.

closer together and finally merge, as seen in Fig. 7.

2.2.3 Switching Characteristics

The net area of the voltage waveform remains constant and equal to $\Delta\phi$, regardless of the ampere-turns applied, provided the core is switched completely. However, the inverse of the switching time and the peak voltage vary almost linearly with the applied mmf (26, 13), as shown in Fig. 8. Thus

$$\frac{1}{\tau_s} = K_1(NI - NI_{min}) \tag{6}$$

$$\frac{v}{N} = K_2(NI - NI_{min}) \tag{7}$$

The slope of the v/N vs. NI characteristic, called R_o, will be very useful later in the design procedure, as will K, the slope of the $1/\tau_s$ vs. IN characteristic.

Note that both NI_{min} (which corresponds to H_W and is close to, but not the same as, H_C) and H_C depend upon the length of path around which the switching is supposed to occur. Thus both NI_{min} and H_C are lower for a toroid of small circumference than are the corresponding parameters for a core of large circumference, the material and

cross-section area being the same for both cores.

2.2.4 Undesirable Voltages

The spikes at the beginning and at the end of the voltage waveform are undesirable, but are usually not particularly objectionable in pulse work. However, another voltage, the so-called "zero" output, is extremely undesirable. This voltage occurs when we try to pulse the core in the same direction in which it is already set. Under this condition, a complete absence of output would be preferable, but we get a voltage, as shown in Fig. 9, that corresponds to the flux value $B_{max} - B_r$. (The net volt-time area is still zero.)

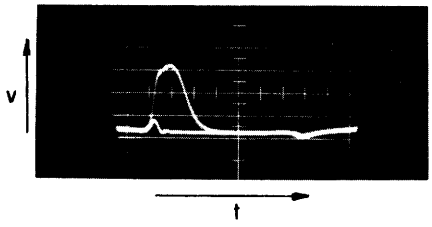


Fig. 9. Zero-one ratio.

The ratio of this "zero" voltage and a full "one" output (due to switching of the core by the same current) is called the zero-one ratio; it is proportional to the squareness ratio and is often employed in testing cores.

2.3 Behavior of an Idealized Transfluxor

Most of the basic ideas about transfluxor operation can be explained by considering a two-hole core, as shown in Fig. 10a. Let us go through a basic sequence of operations that apply to the core pulses, as shown in Fig. 10b.

2.3.1 Basic Operation

In our basic sequence, we first apply a pulse to the winding labeled "block," which saturates the whole core completely in the clockwise direction, as shown in Fig. 10c. Then we apply a pulse to the "unblock" winding, which tends to switch the flux in the counter-clockwise sense. Let us suppose that the applied mmf is strong enough to switch the flux along the shorter path α, but not strong enough to cause flux reversal along the longer path β. We get a flux distribution like that shown in Fig. 10d. Notice that we have, effectively, a closed loop around the small hole (shown with a dotted line in Fig. 10d, with the result that if a pulse is applied to the "drive" winding we can reverse the flux around the small hole and get an output on the output winding. We now have a flux distribution like that shown in Fig. 10e and, therefore, can switch the flux around the small hole back and forth, producing positive and negative voltage pulses at the "output" winding, forever after.

If the "unblock" pulse were missing, the core would still be in the state shown in Fig. 10c when the "drive" pulse arrived, so that switching around the small hole would be impossible. If the "drive" pulse were big enough, we could still switch around the big hole. [This is called "spurious unblocking" (8).] Thus, if we want to have a gate, we must apply a "drive" pulse of the correct magnitude, that is, big enough to switch around

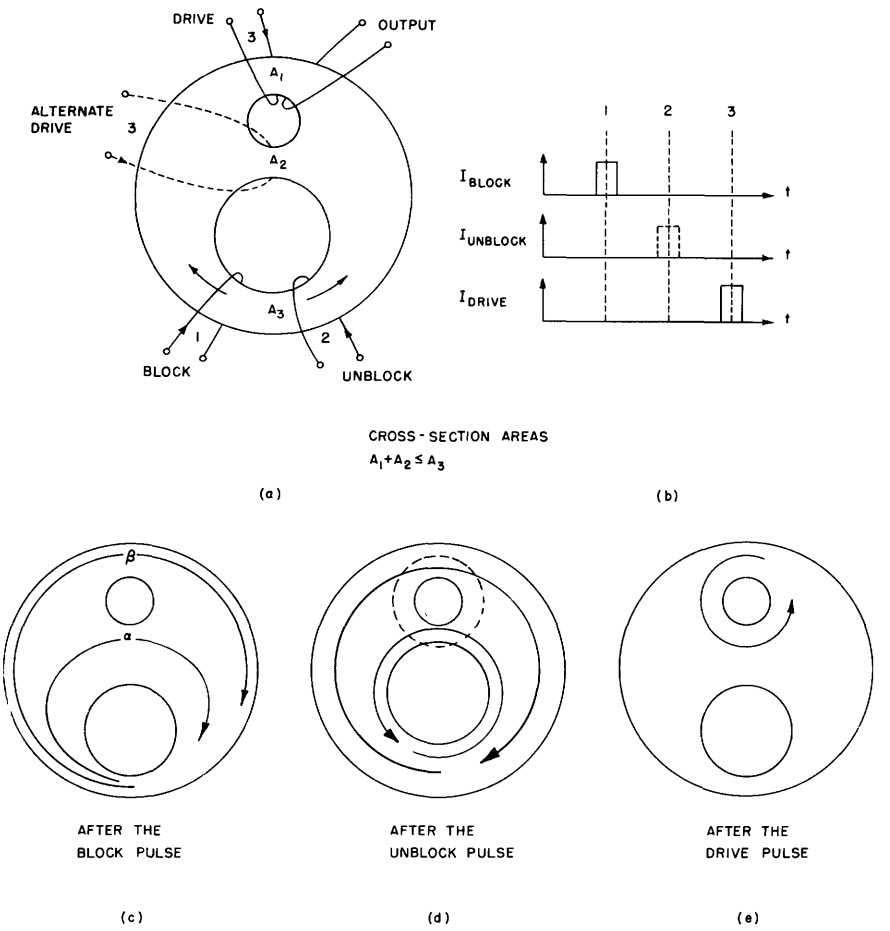


Fig. 10. Two-hole transfluxor.

the small hole, but not big enough to reverse the flux around the large one.

Instead of driving the core on the outer leg, we could apply a "drive" pulse on the inner leg, driving through the winding labeled "alternate drive." Now there is no possibility at all of unblocking the core at time 3 because the "alternate drive" tries to switch the core in the direction in which it is already set; thus, there is now no maximum limit on the driving pulse.

We see that the transfluxor can act as a gate that can be closed or opened by a single pulse. In Sec. III, we discuss many other elementary building blocks that are realizable with this and other forms of multiple-hole cores.

2.3.2 Switching Mechanism

In the previous discussion, it was assumed that we can actually reverse flux α, but not flux β, by applying an appropriate "unblock" pulse (see Fig. 10). In other words, we want exactly one half of the flux reversed – the half that is nearer to the center of the core. The real transfluxor does not behave exactly in this way, but we can discuss

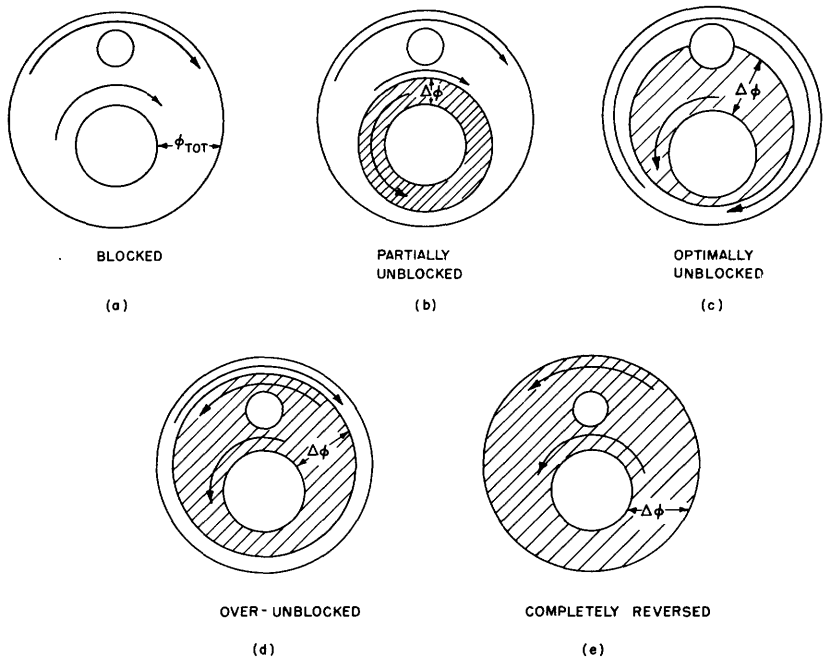


Fig. 11. Switching of a transfluxor.

first an idealized model that does. This idealized model is similar to the explanation of transfluxor behavior published by Rajchman (7, 8).

Let us first imagine that the whole transfluxor consists of one single domain that is magnetized by the blocking pulse in a clockwise direction, as seen in Fig. 11a. If we apply an unblocking pulse to the core in the form of a slow ramp current, the NI_{min} will be reached first in the part of the core that has the shortest path, that is, the part nearest the middle hole. Thus, another domain of counterclockwise saturation begins to grow outward from the center hole, as shown by parts b through e of Fig. 11.

Obviously there is a point at which we have an optimal condition, that is, when exactly one half of the flux is reversed; or, in the notation of Fig. 11, when

$$\Delta\phi = \frac{1}{2}\phi_{total} \tag{8}$$

At this point we have the maximum available flux for switching around the small hole, as seen in Fig. 12:

$$\phi_{available\ max} = \frac{1}{2}\phi_{total} \tag{9}$$

For this, the applied ampere-turns must be

$$NI = NI_{opt} \tag{10}$$

If the reversed flux is smaller, that is, if

$$NI < NI_{opt} \tag{11}$$

$$\Delta\phi < \frac{1}{2}\,\phi_{total} \tag{12}$$

then

$$\phi_{available} = \Delta\phi \tag{13}$$

And if

$$NI > NI_{opt} \tag{14}$$

$$\Delta\phi > \frac{1}{2}\,\phi_{total} \tag{15}$$

then

$$\begin{aligned}\phi_{available} &= \frac{1}{2}\,\phi_{total} - \left(\Delta\phi - \frac{1}{2}\,\phi_{total}\right) \\ &= \phi_{total} - \Delta\phi\end{aligned} \tag{16}$$

From these considerations we get the curve of Fig. 12.

It is surprising that, even though the real transfluxor does not behave exactly in the same way as our idealized core (7, 8), we still get a characteristic very similar to that of Fig. 12. This fact suggests the use of transfluxors as analog devices, perhaps as "magnetic gates with a variable magnetic setting" (8). This application, however, is outside the scope of this report.

2.3.3 Inherent Time Delay

The transfluxor will function in the way described in the preceding section even when we apply a sharp step instead of a ramp. (This statement is idealized and will be modified in later discussion.) In other words, the switching starts near the center and propagates outward. This propagation is stopped at any point either by terminating the current pulse in time or by limiting its amplitude.

It is evident that if we wire the transfluxor at the inner and outer leg of the small hole, as seen in Fig. 13a, we shall get a pickup first at the inner leg and then at the outer leg. See Fig. 13b. This principle can be utilized to obtain fixed delay by using a

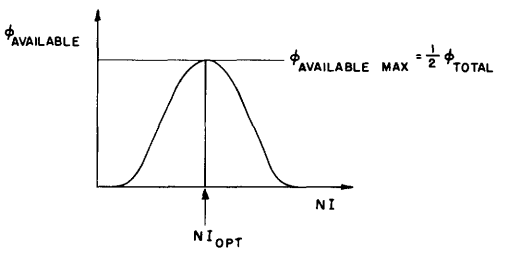


Fig. 12. Flux available for switching around the small hole as a function of unblocking ampere turns.

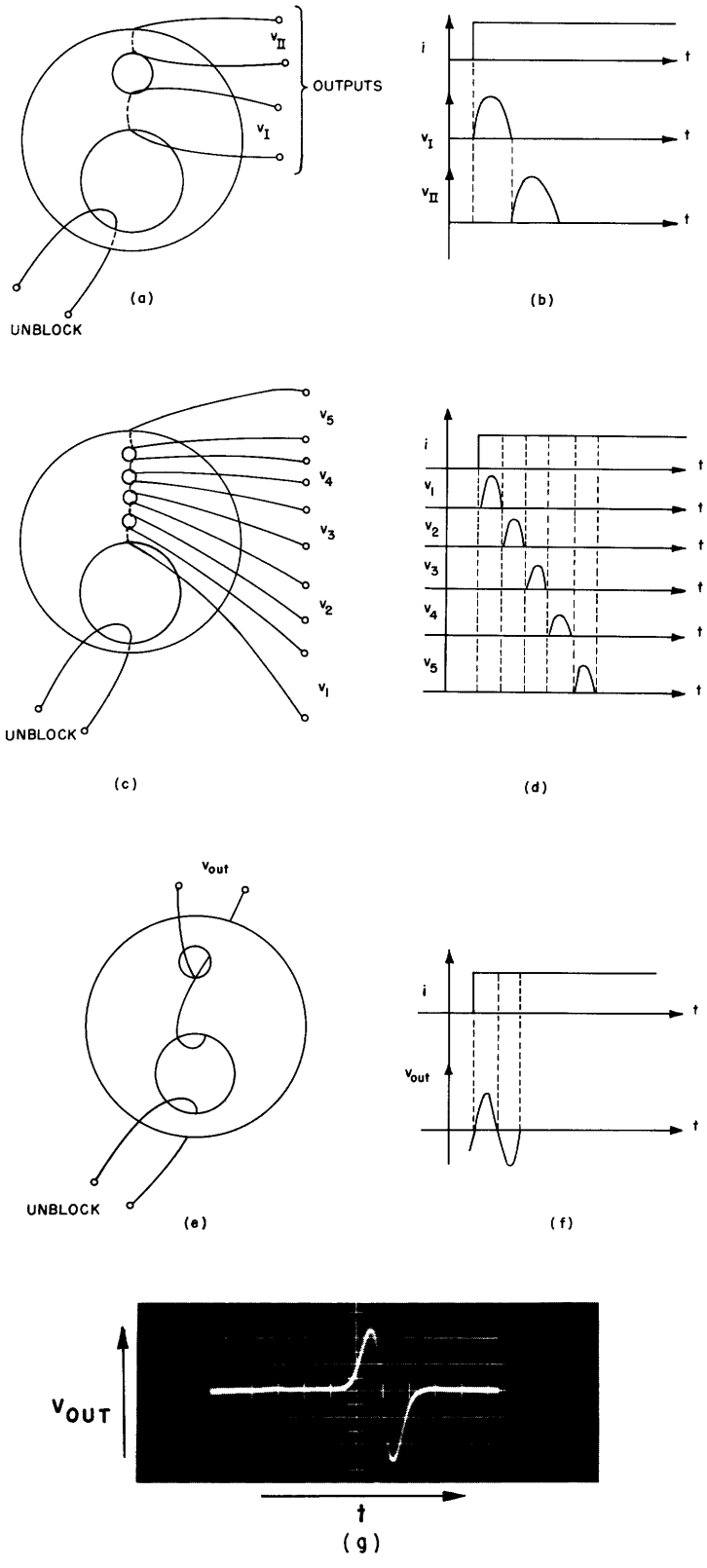


Fig. 13. Inherent time delay.

multiple-hole core, as seen in Fig. 13c and d.

The principle of time delay can best be verified experimentally by winding the core as shown in Fig. 13e, that is, by winding the outputs on the inner and outer loops in opposition. The predicted output of Fig. 13f matches the experimental result of Fig. 13g.

The principle of time delay was actually used by Goldner (3) to obtain many staggered pulse times; the principle was also discovered and studied independently by this author. The real transfluxor does not behave exactly in the way our idealized core would behave. Instead, some overlap occurs between the voltage outputs in Fig. 13b and d, showing that the outer legs begin to switch even before the inner ones finish. These overlaps increase with loading (3).

2.4 Flux Distribution

The motion of domain walls in a polycrystalline ferrite is extremely complicated. Therefore, exact flux distribution pictures cannot be obtained by the direct methods in use (powder method, colloidal-suspension method, etc.). The pictures taken by those methods have proved to be completely meaningless. Until a more powerful method is found, we have to be satisfied with voltage measurements, which indicate only the net change in flux across a given cross section. Moreover we cannot introduce extra holes for measuring purposes because each hole distorts the flux picture.

2.4.1 General Principles

In addition to the voltage measurements, we can take advantage of a few general principles, obtained either from theoretical considerations or from empirical data.

1. All flux lines inside the core are continuous, closed loops. This is obvious from the Laplace equation and from the fact that the measurements show the leakage flux to be virtually nonexistent.

2. Any flux reversal must occur along a closed loop. Thus, in order to reverse the flux at any point, there must be a complete loop of either oppositely magnetized or demagnetized material available for switching. The net flux change along this loop must be the same at any point. The applied mmf must be bigger than NI_{min} for that complete loop. If there is a branch point, the algebraic sum of either ϕ or $\Delta\phi$ going out from this point must be equal to zero. These are consequences of statement 1.

3. An mmf, applied to any leg of the core, that tends to switch the core in the direction in which it is already set cannot cause a net flux change anywhere in the core. This is, perhaps, not as obvious as it sounds.

4. In an unloaded core, if there are two paths of unequal lengths, either of which can be switched at their meeting point, the switching will favor the shorter loop. This is discussed more thoroughly in Sec. IV.

5. If there are many different flux distributions possible at the same time, the core will choose the state of minimum potential energy. This is a general principle of nature.

6. Any flux distribution derived will be just an approximation to the statistical average of the fluxes of the small domains.

2.4.2 Ambiguities

By using voltage measurements to indicate the changes in flux and the "General Principles" of Sec. 2.4.1 for guidance, we can obtain a flux pattern for different states and configurations. Sometimes, however, more than one model is possible, all of the models being completely equivalent as far as external $\Delta\phi$ measurements indicate. A classical example of this is the five-hole transfluxor (see Fig. 14). If we first block the transfluxor completely, as in Fig. 14a, and then apply an "unblock" pulse to reverse the flux completely in leg A, flux reversal will occur along the dotted line. According to voltage measurements at all possible points of the core, two flux distribution pictures are equally acceptable; see Fig. 14b and c. (Because no coupling seems to occur afterwards among the small holes, we consider the model of Fig. 14c preferable.)

2.5 Nonideal Behavior of Transfluxors

2.5.1 Switching

A real core does not actually switch as indicated in the model of Fig. 11. There is no single sharp wall. Instead, the outer leg begins switching even before the inner leg completes reversal, as we have already noted at the end of Sec. 2.3.3. Also, the final flux distribution after unblocking does not look like that shown in Fig. 15a; rather, an approximation of it might be similar to that given in Fig. 15b: some flux has already been reversed in the outer leg, while the inner leg is still not completely switched.

An example of this "flux division effect" is shown in Fig. 15c and d for another kind of core – the five-hole transfluxor. (Measurements were taken both by the static hysteresis loop plotter and by dynamic pulse measurements. Both sets of measurements agree within 5 per cent, which is the experimental error. The percentages in Fig. 15 are from the static measurements.)

This flux division effect is very troublesome in transfluxor circuitry, especially because it is greatly intensified by loading. It is discussed further in Sec. IV, where an approximate method of calculation of flux division is introduced. Here, we only note that it can be thought of as being caused either by a rather wide region of switching – a kind of "transition band" that moves outward from the center – or, alternately, as being caused by two walls moving outward at different speeds, one starting from the center hole, the other from the small hole.

Because nobody as yet seems to have published any convincing evidence to support either of these hypotheses, or any other one for that matter, we shall not hazard a guess. Suffice it to say that the real flux distribution in a polycrystalline, multiple-hole core is infinitely more complex than our simple model would lead us to believe. This is a field in which much research is urgently needed.

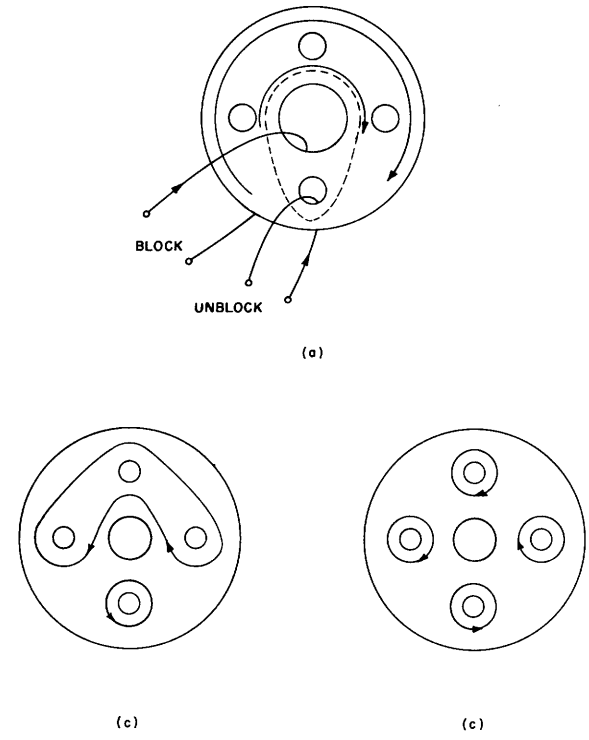


Fig. 14. Ambiguities in flux distribution of a five-hole transfluxor.

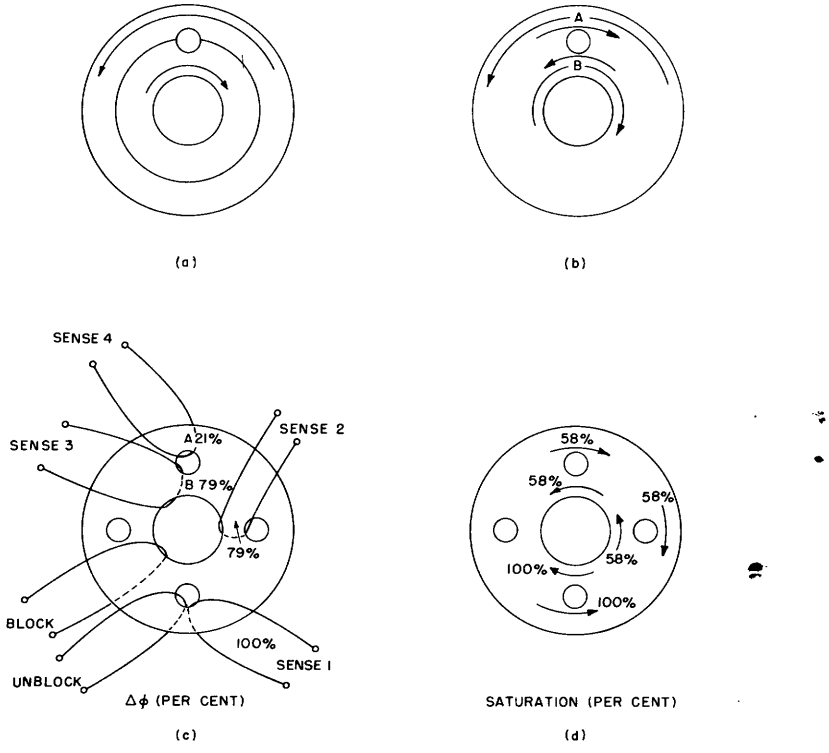


Fig. 15. Nonideal switching of transfluxors.

2.5.2 Effect of Loading

Loading of a core, as in Fig. 16a, by a resistance R has the effects shown in Fig. 16b, c, and d: the switching time gets longer, and voltage amplitude diminishes. This is understandable if we consider that the I_{out} going through the winding W_2 produces a counter mmf, which causes the effective mmf applied around the loop to become:

$$NI_{eff} = N_1 I_{in} - N_2 I_{out} \tag{17}$$

This effect is especially important in transfluxors, since not only the speed of switching but also the final flux distribution may depend on loading. For instance, if, in Fig. 15c, we put a heavy load (e.g., a very small resistance) across the winding labeled "sense 3" and applied a large "unblock" pulse, we would get different percentages from those given in Fig. 15c and d. Instead, most of the switching would occur in leg A, since this leg has a much higher NI_{eff} applied to it.

In Sec. IV the effects of loading that were studied are discussed further.

2.5.3 Noise

There are many sources of noise outputs that can occur in a transfluxor (some of them have already been discussed):

1. Spikes at the time of the beginning and ending of the applied pulse, caused by the slope of the hysteresis loop. This was discussed in Sec. 2.2.2.

2. "Zero" output, that is, output occurring when we try to switch the core in the direction in which it is already set (see Sec. 2.2.4).

3. Outputs caused by the flux division effect, mentioned in Sec. 2.5.2. This effect is intensified by loading.

4. Outputs due to the "near leg" effect, which are peculiar to transfluxors. A discussion of this phenomenon is given in Sec. 2.5.4.

Noise outputs 1, 2, and 4 do not correspond to any irreversible change of flux; this means that they do not cause a net change in the volt-time area. This, of course, does not apply to noise output 3.

2.5.4 "Near Leg" Effect

A peculiar transient effect* that occurs in transfluxors is shown in Fig. 17. If we block, unblock, block again, and so on, the core of Fig. 17a by the respective windings, we expect voltages to appear on winding "sense 2," but not on "sense 1," since there is no net flux change occurring in leg A. But, surprisingly enough, we get a considerable "reversible" voltage, much larger than just the "zero output" voltage, as seen in Fig. 17c.

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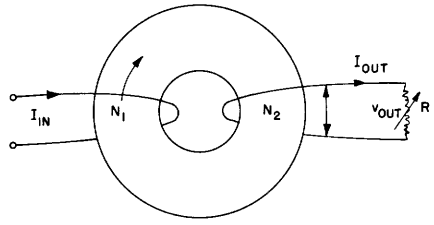
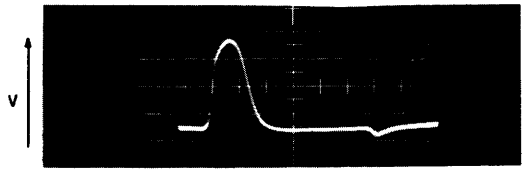
*To the author's knowledge, this effect has not been described or mentioned in any paper and was first observed and studied by the author.



(a)



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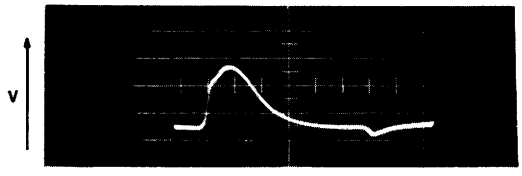

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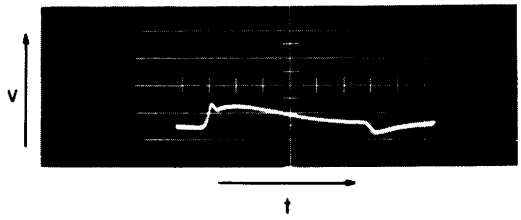
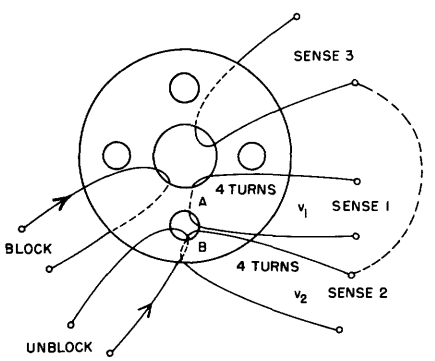
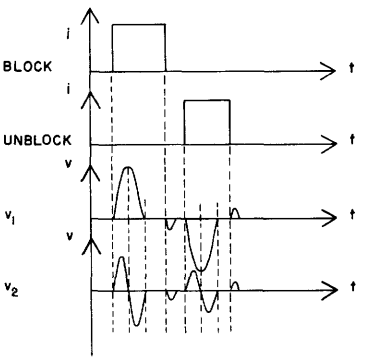


(d)

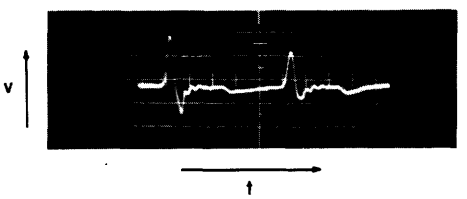
Fig. 16. Effects of loading.



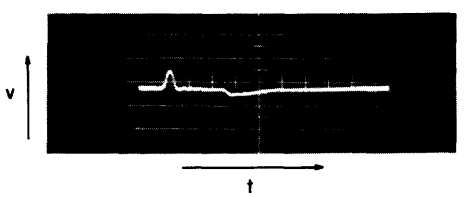
(a)



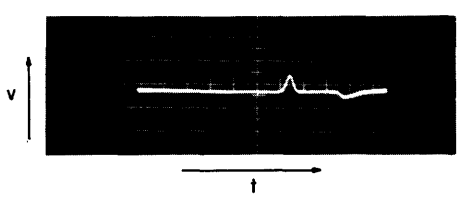
(b)



"NEAR LEG" EFFECT
(WITH BOTH BLOCK
AND "UNBLOCK" PULSES)



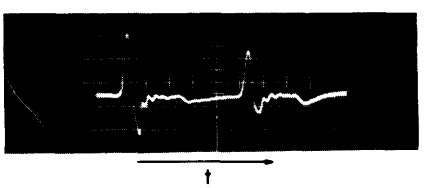
"ZERO" OUTPUT
(WITH UNBLOCK
PULSE ONLY)



"ZERO" OUTPUT
(WITH BLOCK
PULSE ONLY)

OUTPUT AT "SENSE 1"

(c)



OUTPUT AT "SENSE 3" IN SERIES
OPPOSING "SENSE 2"

(d)

Fig. 17. The "near leg" effect.

This voltage consists of a positive and a negative spike (see Fig. 17b) and looks like the derivative of the pulse on "sense 2." The same effect occurs if legs A and B are interchanged.

One possible explanation of this effect is the following: Let us suppose that the core is in the blocked state and we are applying the unblock pulse. Leg B starts to switch. Because the path around the small hole is so much shorter than the one around the big loop, leg A supersaturates, that is, it moves from state B_r towards B_s (see Fig. 5). Later, when the larger loop has had enough time to begin switching, this supersaturation in A has a chance to collapse. This is, in a way, equivalent to saying that the effect is the result of rotation of domains in leg A.

This explanation seems to be supported further by the fact that if we compare (by a series-opposition connection, as shown in Fig. 17a) the voltages on "sense 1" and "sense 3" windings, we see that the voltage on "sense 3" comes later in time (by a small fraction of the switching time), thus showing that the switching of the whole core does not follow instantaneously the switching of leg B (see Fig. 17d).

No claim is made, however, that this explanation is the "true" one, or that there does not exist another, better explanation of this effect. Further research should clarify this phenomenon.

III. THE LOGICAL PROPERTIES OF MULTIPLE-HOLE CORES

3.1 Introduction

Virtually any logical function expressible in Boolean algebra can be realized with magnetic cores. However, because of the inherent synchronous delay, the magnetic core is ideally suited to sequential circuit work.

A multiple-hole core can combine the functions of a few simple cores and can perform some new functions that the simple core cannot perform; for example, asynchronous time delay.

The first necessity in analyzing logical circuits that consist of any new component is a flexible schematic notation. There are two systems of notation for circuits with simple cores: Karnaugh's mirror notation (16), and the scheme introduced by Loev, Miehle, Paivinen, and Wylen (19). Since there is at present no published schematic notation for multiple-hole cores, a notation was developed as a first step in logical analysis. The basis for this notation is the one developed by Loev, Miehle, Paivinen, and Wylen, but the extension to the transfluxor circuits was made by this author.

3.2 Schematic Notation

In the proposed notation a multiple-hole core is represented by a set of dots connected by lines to represent the topology of the core. The dots represent holes, and the connecting lines, the legs between the holes. Dots can be either filled or hollow, to distinguish between the main and supplementary holes in the core. Figure 18a shows the representation of a five-hole transfluxor.

The inputs and outputs to the core in the form of pulses on windings can go either to a leg between two holes, in which case we represent them as going to or from the line between dots, or to a leg between the outside and a hole, in which case we bring them to the dot itself.

The information flow is represented by a hollow arrow going to or from the core representation for input and output, respectively. Only one pulse is associated with each arrow. If many different pulses flow through the same winding at different times, we draw an arrow for each one of them and connect all of them with a double crossbar. Each arrow has a capital letter associated with it that shows the pulse time at which it conducts information. If the pulse can either occur or not occur, depending upon some information conducted, the letter is enclosed in brackets. A small cross arrow can be used to indicate the direction in which the incoming pulse tries to switch the core (for input pulses), or the direction of switching that produces the given pulse (for outputs). All this is much simpler than it sounds, as can be seen from Fig. 18b. It should be noted that the directions of switching indicated are entirely arbitrary, except that they must be consistent for each core.

The use of colors or different thicknesses of lines is helpful in identifying the core and the connecting lines, especially in complicated circuit diagrams.

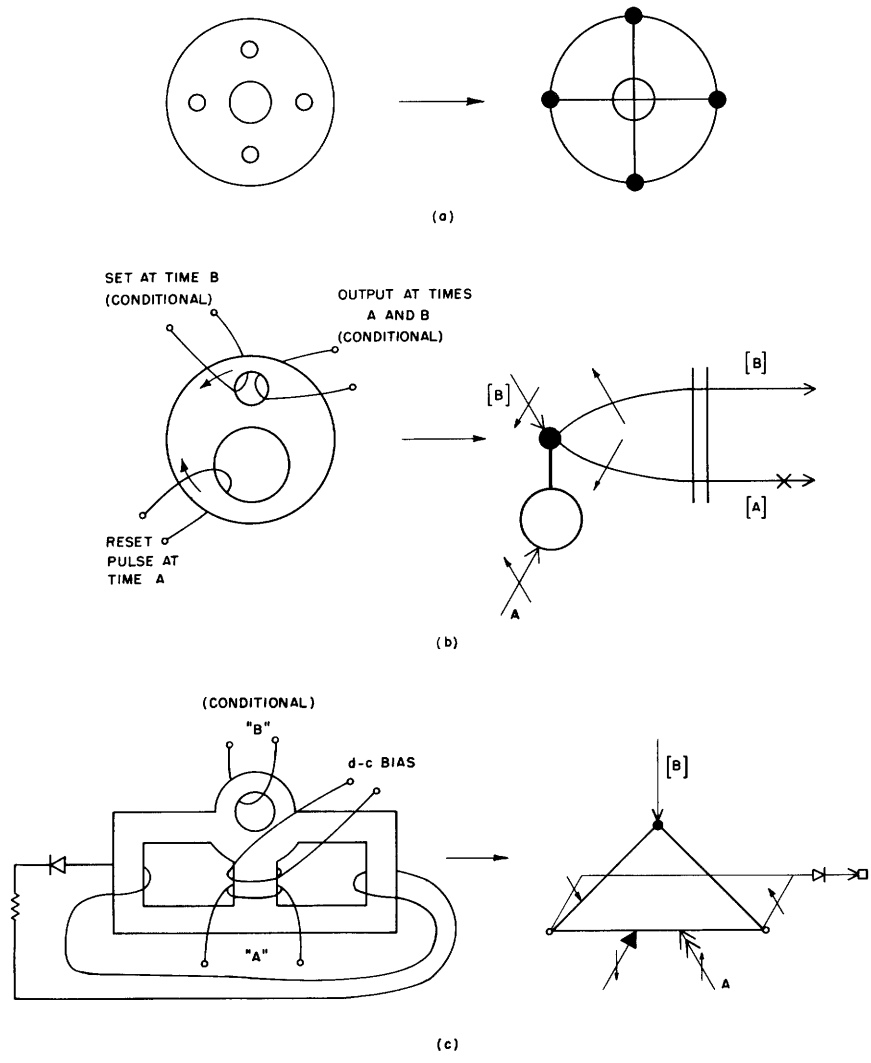


Fig. 18. Schematic representation of multiple-hole cores. (Note: a "conditional" pulse is one that may be either present or not, depending on the information conveyed.)

Other helpful symbols include: filled arrow without associated letters for a dc (biasing) winding; a diode-like symbol for diode; a hollow square for a loading resistor. If the same pulse is either taken from or goes to more than one place on the same core or on a different core, we indicate that by simply branching the arrow line in question. It is also helpful to indicate by a double-headed arrow a pulse that is normally big enough to override either an opposing dc bias or another pulse input that is coincident and opposing. This principle can be extended to multiple-headed arrows. Also an oblique cross can be drawn across an undesirable information flow arrow (see Fig. 18b); this and some of the other conventions are illustrated in Fig. 18c.

This system of notation was used extensively in the present investigation and, on the whole, was found to be very satisfactory. It is simple, easy to understand and to learn, and it conveys all of the pertinent information.

3.3 Problems of Logical Design with Multiple-Hole Cores

3.3.1 General Approach

In the logical design of transfluxor circuits either of two approaches can be followed: (1) design the cores in order to realize our particular circuit; or (2) design circuits using a standard core throughout the system.

The second method was used in our investigation, since there were no easily available facilities for fabrication of special cores.

The following steps in design procedure were found to be most fruitful:

1. Investigation of the given core geometry and listing of all possible modes of operation.
2. Elimination of the less desirable modes, then placement of the remaining modes in a list of standard "gate boxes" with all pertinent information.
3. Design of the circuit, by means of the well-known switching circuit methods, in terms of the standard gate boxes.
4. Substitution of cores for gate boxes.
5. Final circuit design (see Sec. IV).

3.3.2 Modes of Operation

In classifying the modes of operation for a given transfluxor, care should be taken to notice the following:

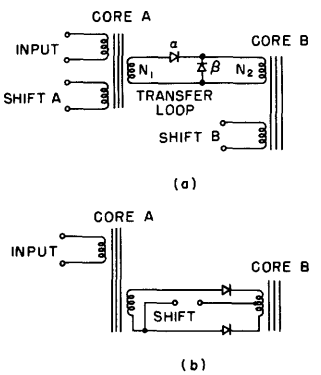


Fig. 19. Basic forms of transfer loops.
(a) "Variable transformer" coupling;
(b) "variable reactance" coupling.

1. "Variable transformer" vs. "variable reactance" operation. The difference is illustrated in Fig. 19 for simple cores (19). The usual method employed is the "variable transformer" coupling. On the other hand, the "current steering principle" (9) uses cores as "variable reactances." This difference is really more important in circuit design (see Sec. IV) than in logical design because, in most cases, the logical circuit can be realized in both ways.

2. Delay. It is important to note how many clock times any given operation requires,

and the number of synchronous delays between inputs and outputs. Asynchronous delays are also of importance if coincidence is desired.

3. Diode vs. diodeless operation. This is discussed further in Sec. 3.3.3 and in Sec. IV.

4. Realization of logical function. It is important to see all of the outputs obtainable from any one mode of operation and all of the times at which they occur. This will help in circuit standarization.

3.3.3 Diode Elimination*

The use of transfluxors instead of simple cores makes possible the elimination of diodes in the transfer loops, partly owing to the isolation properties in the transfluxors themselves (which have many gating functions built in) and partly to the possibilities of the use of the "transfer blocking" principle, which can be employed in the design of transfluxor circuits. Also appropriate turn-ratios can be used for preventing backflow of information.

Let us discuss the reasons for introducing diodes into magnetic-core circuits in the first place. (Only the "variable transformer" operation is considered, since it has not yet been found possible to eliminate diodes in "variable reactor" circuits.) In Fig. 19a the purpose of diode α is to prevent the negative pulse caused by the switching of core A at the "input" time from traveling from core A to core B. In other words, we want an isolation between the input and the output in core A. In this connection it is important to remember the general principle that the volt-time area over the complete cycle at any output of a core is equal to zero, so that for any positive pulse there is an equal area of negative pulses.

Diode β in Fig. 19a has a different function. Its purpose is to prevent backflow of information from core B to core A (by short-circuiting B). This backflow can occur while information is being shifted out of core B by shift B pulse.

The use of diode β can be easily avoided by making the N_1/N_2 ratio sufficiently large to cause the current in the transfer loop to be too small to cause any switching of core A. This idea is further illustrated in Sec. IV. It is sufficient here to say that this can be done almost always in practice, and that in many cases the circuit operation is actually improved because excessive loading of cores by the short circuit through the diode is prevented. Thus, in most instances, diode β is no problem.

Diode α is another matter. It is difficult to eliminate. In transfluxor circuits, the following approach can be used. Figure 20b shows that isolation of input from output has been achieved, that is, there is no [C] on the output winding. However, there remain two outputs of opposite polarities. Usually, we want to use only one of them, the other being an undesirable "noise" pulse.

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*The author has studied the question of diodeless magnetic-core circuitry extensively, and, to his knowledge, no paper on this subject has been published as yet.

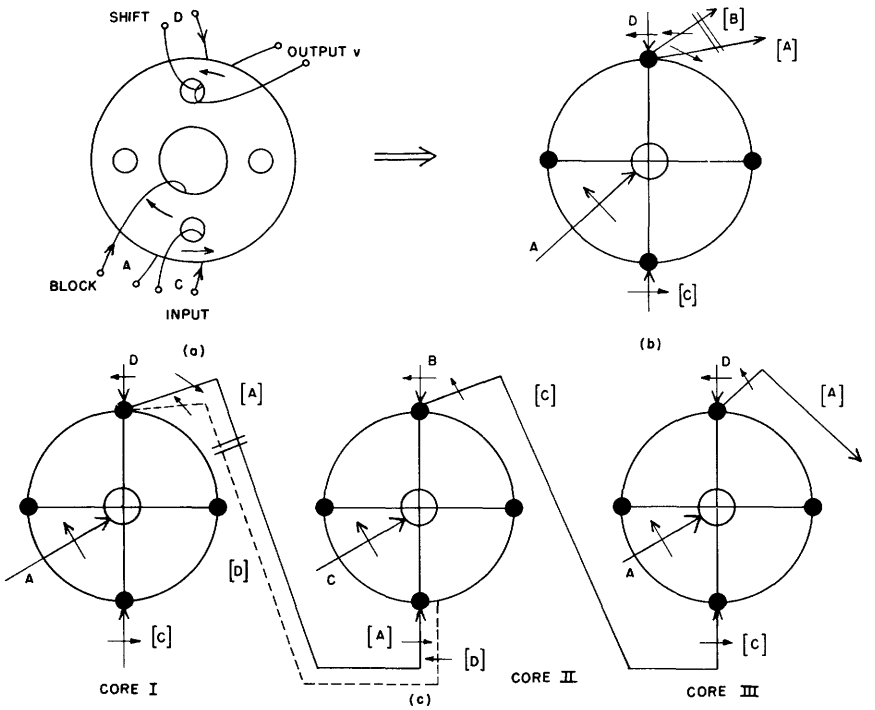


Fig. 20. Example of a diodeless circuit.

Our purpose is to eliminate this undesirable pulse – as can be done with diodes – or to make it harmless by using "transfer blocking," that is, to make sure that one of the following conditions applies:

1. The second core is in a state in which the undesirable pulse tends to switch the core in the direction that it is already set.

2. The second core is being switched at the time of the undesirable pulse in any direction by a pulse that is strong enough to override the effects of the undesirable pulse.

3. A blocking pulse is applied to the second core; although this pulse does not switch anything, it prevents the core from undesirable switching.

4. Both incoming pulses (the positive and the negative) leave the core in the desired "one" condition. This means that the first pulse unblocks the core, while the second one (negative) merely reverses the flux around a small hole and does not affect the information in the core. (This solution is not discussed further in this report, although some work has been done. It shows great promise for the future and should be investigated further. See Fig. 23e and f for examples of core modes that could be used in this fashion.)

In Fig. 20c the first principle is employed to obtain a diodeless shift register with five-hole cores. We can see that core II cannot respond to the undesirable input at time D (shown schematically by the dotted line) because it is always set by pulse C into the position in which pulse [D] tries to set it.

This example illustrates a more or less general principle: for the elimination of

diodes we have to pay a price in terms of additional pulse times and, therefore, additional drivers and a decrease in the speed of operation.

3.3.4 Gate Boxes

The gate boxes, as introduced first in this report, show all of the information required for the use of any particular "core-mode" in logical design. Therefore, they include the following (as in Fig. 21):

1. All of the outputs with the logical functions in terms of inputs. For simplicity, we can eliminate some of the trivial outputs, as in Fig. 21c.

2. All of the desired inputs, with "permitted undesirable pulses" (in brackets), as explained in Sec. 3.3.3. In the notation of Fig. 21 and other similar figures, the bracketed numbers, such as

$$[1,\ 3,\ 3-3,\ 4],$$

mean that pulses of the same polarity as the input pulse are permitted at the times 1, 3, and 4, whereas pulses of opposite polarity are permitted at times 2 and 4; (0 indicates no permitted pulses of the given polarity).

3. The required shifting pulses, if necessary.

4. The times at which the pulses occur relative to each other (inside the box).

5. If desired, the points at which the inputs-outputs are located, as noted by Greek letters and connections between arrows coming from the same point.

6. The polarities of the output pulses are usually obvious – all we care about here is the relative polarities on the same winding. (For example, on β, output B must be opposite in polarity to BC' and BC.) If necessary the polarities can be indicated by different arrows, as shown in Fig. 21b. Note also that the times shown in Fig. 21b above R indicate that the times are modulo 3, and that the indication 4 is the same as 1 (except for outputs when it occurs in accordance with the information of the last cycle).

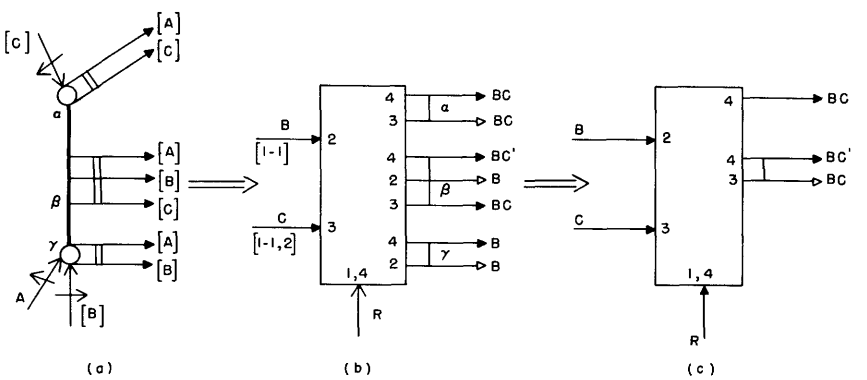


Fig. 21. Derivation of a gate box. (a) Schematic; (b) gate box; (c) simplified gate box.

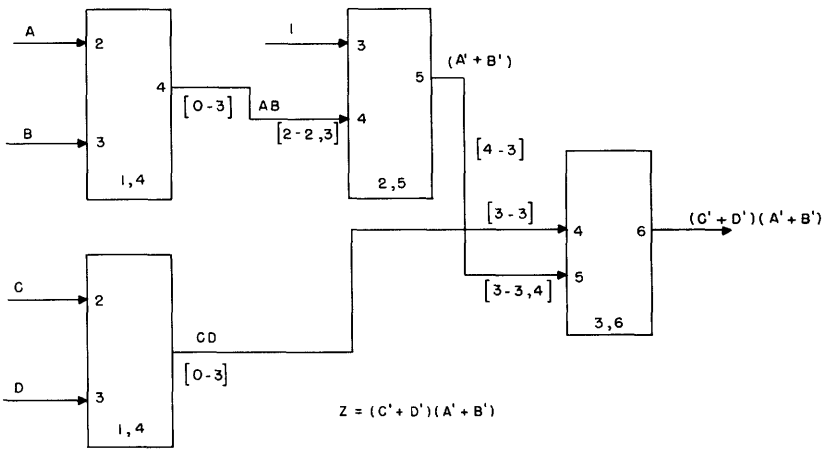


Fig. 22. Example of gate box design. This circuit will not work owing to lack of "transfer blocking" on the (A' + B') transfer.

Figure 22 is an example of a circuit designed in the gate box notation from a problem statement in Boolean algebra. This circuit illustrates the importance of timing: if we compare the times of undesirable pulses (in brackets) for inputs and outputs, we see that all of the transfers work and do not require diodes for coupling, except for the (A' + B'), in which the timing is off. Therefore this part of the circuit will not work, and some other gate box will have to be employed.

3.3.5 Limitations and Precautions

In working with magnetic cores we are not free to do as we please. There are many physical limitations, which are not obvious, that have to be kept in mind. Thus, in order to make our circuits physically realizable we should obey the following general principles when working with the gate boxes:

1. There is a limit to the number of cores that can be switched from one core; to be on the safe side, a maximum of three in "variable transformer" coupling, and a maximum of five in "variable reactor" circuits. This applies both to cores switched in parallel and those switched in series.

2. It is generally safer to avoid the use of series switching, that is, the use of an output at the same time as an input. (To obtain power amplification, the output must come from the shift pulse, and the inputs should be used for presets.)

3. If coincidence is desired, careful investigation of asynchronous delays is necessary. (The synchronous delays are easy to see.)

4. In diodeless coupling, care should be taken not to have an undesired input at a time that is not specifically permitted by the bracketed numbers.

5. In some instances (such as the two-hole transfluxor of Fig. 21), there is both an upper and a lower limit on pulses, and the design, therefore, is more difficult.

6. The effects of loading may make a whole circuit configuration unworkable unless additional blocking pulses are applied; see Sec. IV.

The principles just stated will be discussed further and justified in the circuit design considerations of Sec. IV.

3.4 An Example: The Five-Hole Transfluxor

As an illustration of the discussion in the preceding paragraphs, the five-hole transfluxor is analysed. The known useful modes of operation are listed, and gate boxes are used in a practical circuit. The five-hole transfluxor is chosen because this core was

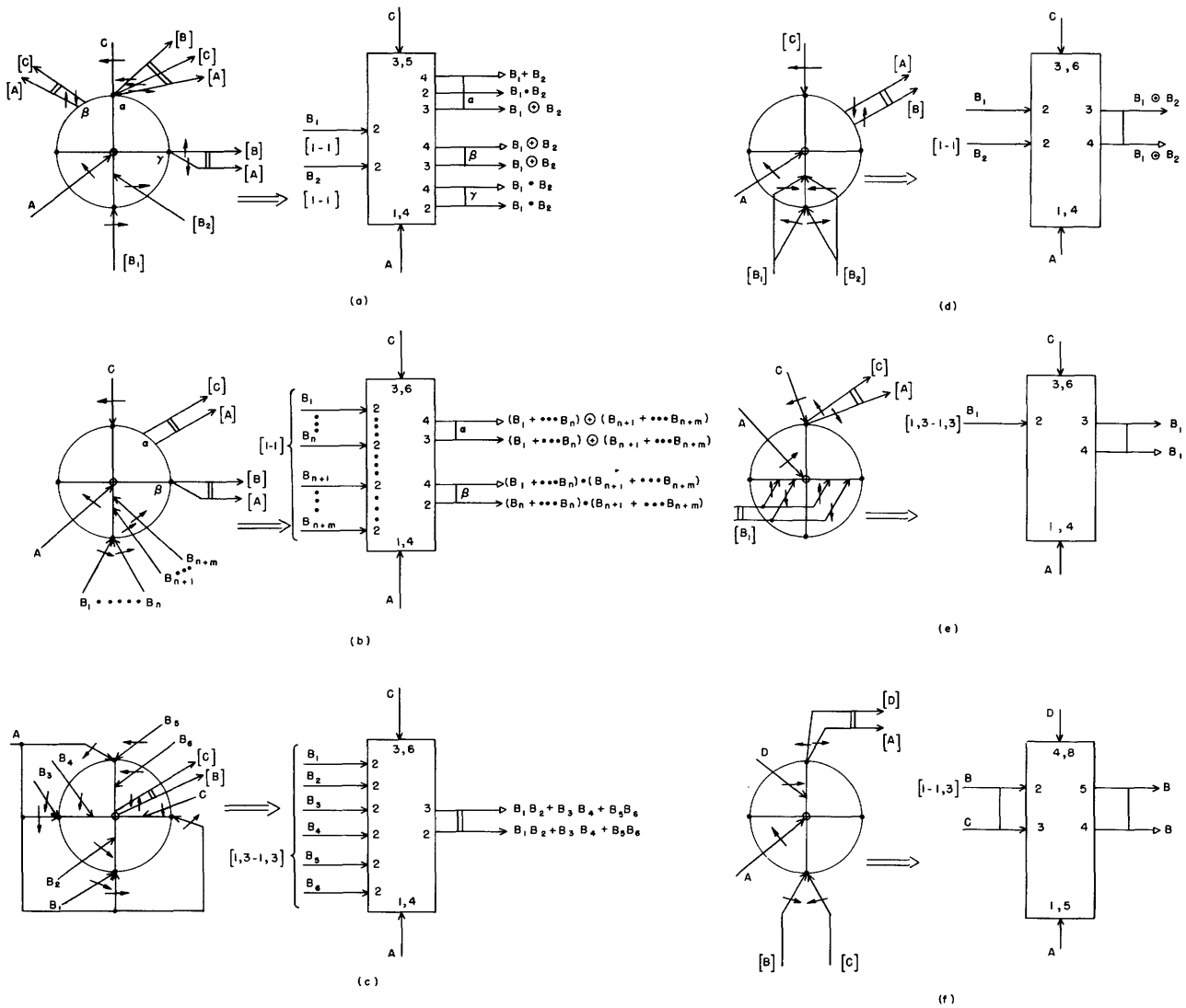


Fig. 23. Modes of operation of five-hole transfluxor; ⊕ ≡ modulo 2 sum.
(a) Core-mode a_1;
(b) core-mode a_2 (a_1 generalized);
(c) core-mode b;
(d) core-mode c;
(e) core-mode d;
(f) core-mode e.

used most in the laboratory investigations, and also because scarcely any mention of it has been made in the literature.

3.4.1 Modes of Operation

The gate boxes derived for the five-hole core are listed in Fig. 23, and most of the useful modes of operation are noted. We can see the exceptional versatility of this core.

3.4.2 A Sample Circuit

Figure 24 shows a sample circuit with five-hole cores. The circuit in question is a parallel accumulator that employs two five-hole cores per digit plane; three digit planes are shown. It is easy to see how to extend this principle for more digits; if the C outputs are fed into the respective A inputs, the accumulator will retain the information indefinitely, recycling it every four pulse times. After digits A and B are fed into the accumulator, the correct outputs will appear after n/2 complete cycles (approximately 2×n pulse times). This delay is caused by the normal problem of carry propagation. A direct carry-through circuit can be constructed; however, it does not conform with principle 2 of Sec. 3.3.5 and is therefore difficult to design.

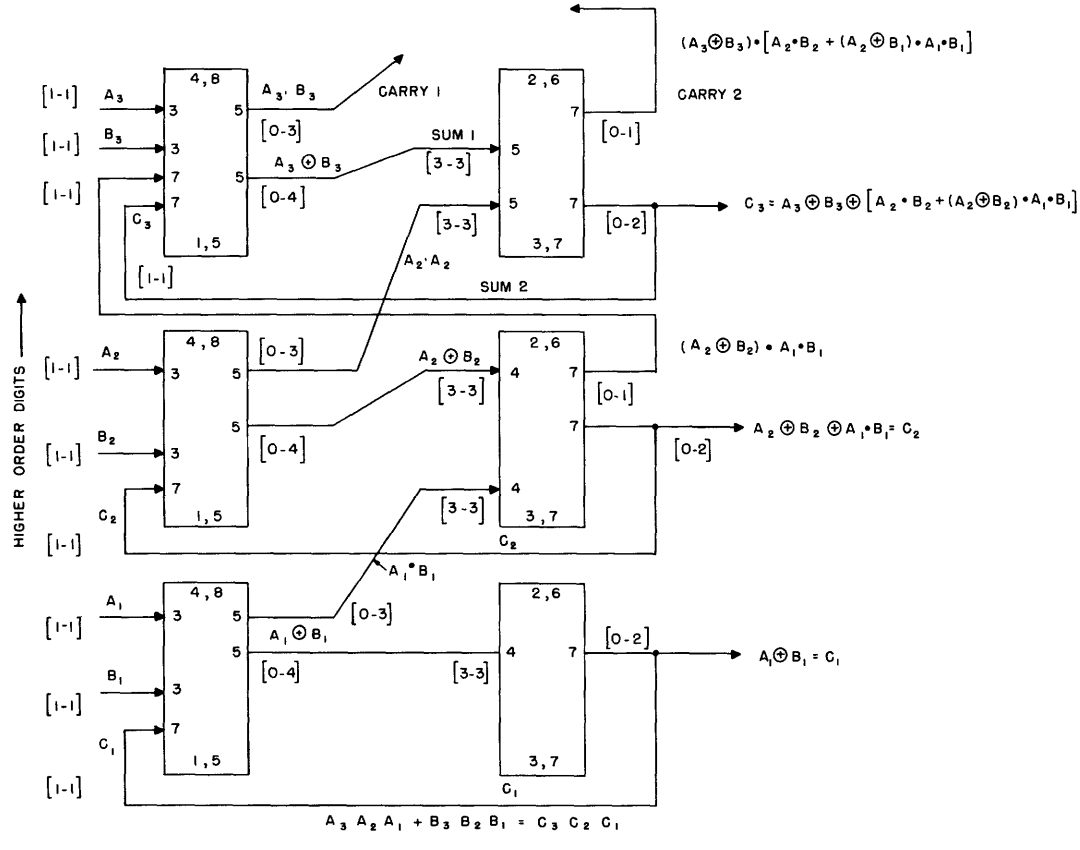


Fig. 24. A parallel accumulator consisting of two five-hole transfluxors per digit plane.

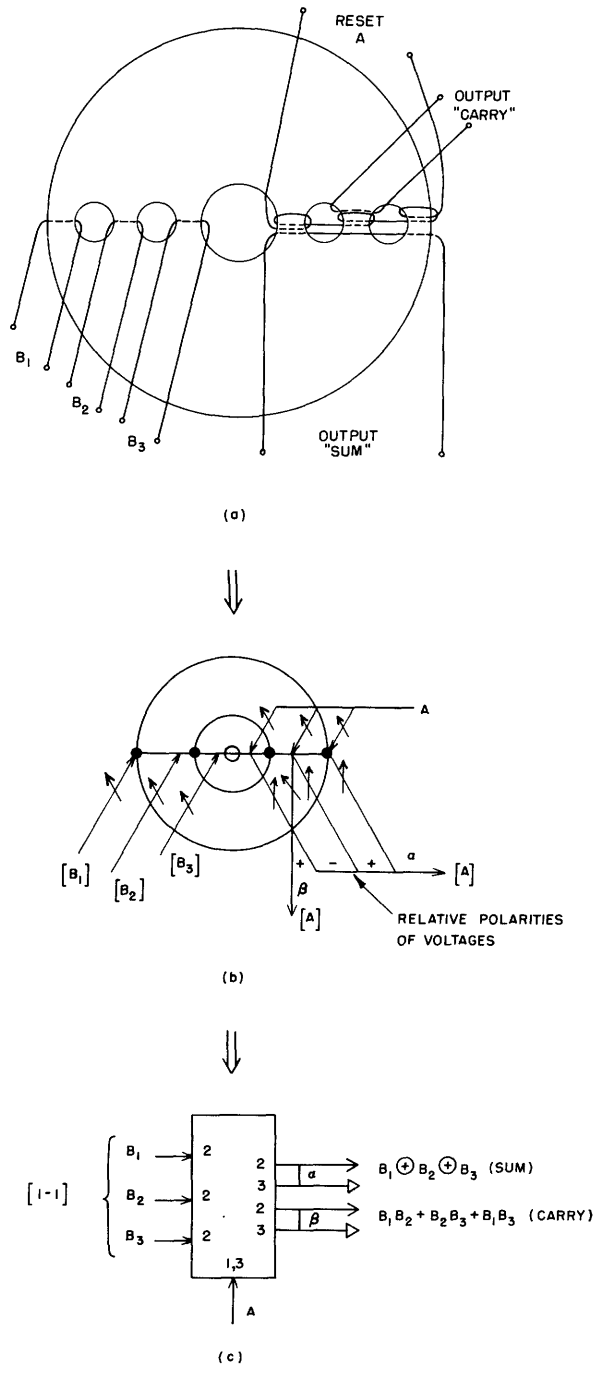


Fig. 25. One-core full adder.

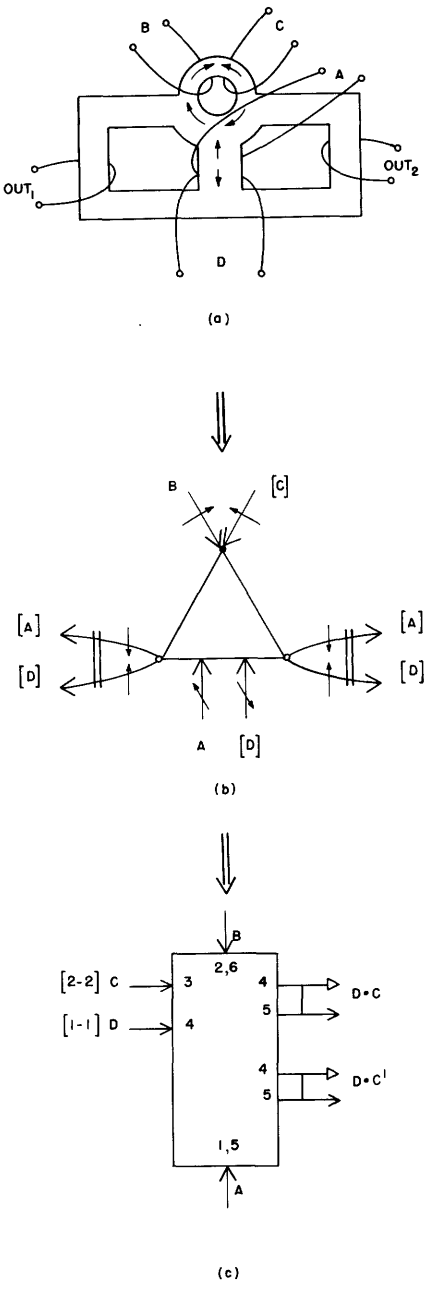


Fig. 26. A magnetic SPDT switch.

From pulse-time considerations it is evident that, although diodeless "carries" can be obtained, the "sum" couplings require diodes. Diodes may be eliminated by using blocking pulses at the appropriate pulse times (see Sec. 3.3.3).

3.5 Extension of the Principles Derived to More Complicated Geometries

By using the principles presented, we could simply list all the available cores with all the available modes of operation and then use them as our circuit required. Of course, there is always the problem of coupling dissimilar cores, but that should be easy to surmount in practice, especially if bigger cores always are used to feed smaller ones.

The more complicated the cores are, the more complicated the functions they can perform. For instance, we can easily make a full adder (1 digit) out of a single core like that of Fig. 25. (A similar core and circuit were first suggested by the IBM research staff.) Another example is the switch shown in Fig. 26; this core was first investigated at the M.I.T. Research Laboratory of Electronics by J. Harrington and the author.

IV. ANALYSIS AND DESIGN OF CIRCUITS WITH MULTIPLE-HOLE CORES

4.1 Introduction

After a logical circuit has been designed by means of gate boxes or some other method, the problem of making the circuit work still remains; we have to design the transfer loops, that is, decide on the number of turns, diodes, and resistors to be used, the right size and duration of driving pulses, and so on. Sometimes the circuit does not work at all, or works only after introduction of special blocking pulses, because the principles stated in Sec. 3.3.5 were not followed. Usually we want to optimize our circuit with respect to such factors as time, energy dissipation, and reliability.

Up to now, no such design procedure for circuits containing multiple-hole cores has been published. There exist, however, some approximate methods (26, 27, 13) pertaining to simple cores, which can be used as a basis for developing methods for multiple-hole circuits. The problems in multiple-hole circuits are much more complicated then those in simple cores, and entirely new effects have to be dealt with.

It should be noted that the circuits analyzed in this report are all of the "variable transformer" type; moreover, the use of extra components in the coupling circuits, such as condensers, inductors, and transistors, is avoided. It was felt that such devices would nullify all the advantages of magnetic-core circuits. The effort was directed instead toward the elimination of even the diodes and toward circuits consisting entirely of cores, with some incidental resistors.

4.1.1 Approximate Analysis of Circuits with Simple Cores

Before going into the analysis of multiple-hole circuits, let us discuss briefly the approximate method of analysis of simple-core circuits formulated by Breckenridge (13) [who in turn based his work on papers by Sands (26) and Rising (25)]; this method forms a first step in our investigations of multiple-hole cores. The analysis is based on the

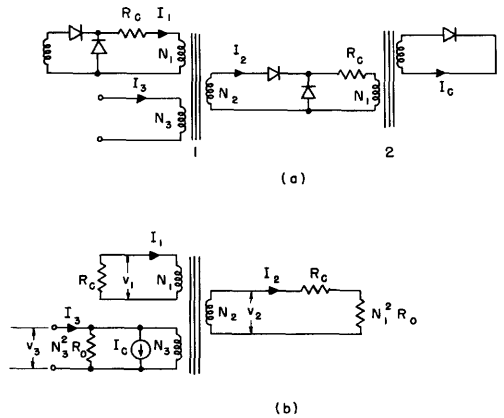


Fig. 27. A simple transfer loop.

assumption of a square voltage waveshape, and therefore upon a model in which the walls move at a uniform rate.

Thus, let us consider first the simple transfer loop shown in Fig. 27a. If we include the forward diode resistances in the coupling resistors R_c and make further obvious approximations, we obtain the circuit of Fig. 27b. The cores are approximated as resistances N^2R_o while switching; R_o is the quantity defined in Fig. 8. On the other hand Sands (26) defines another equivalent resistance

$$\overline{R}_o = \frac{\Delta\phi}{ITN^2} \tag{18}$$

For a comparison of R_o with $\overline{R}_o$ see Appendix A. The basic difference between R_o and $\overline{R}_o$ is that R_o is based upon peak voltage, whereas $\overline{R}_o$ is obtained by averaging. They are therefore related by a shape factor that, from empirical data, is usually about 0.6 to 0.7.

In order to account for the coercivity, we can include the constant current source I_c, where

$$I_c = \frac{NI_{min}}{N_3} \tag{19}$$

in parallel with the resistance $N_3^2 R_o$ (see Appendix A).

Any inductances are disregarded, and the cores are assumed to be short circuits if they are not switching. Also we assume that the voltage waveform is square and that

$$v = \frac{N\Delta\phi}{\tau_s} \tag{20}$$

while the core is switching, and zero otherwise; ($\Delta\phi$ is the total change in flux). If we define:

τ_{s1} = the switching time of core 1
τ_{s2} = the switching time of core 2
F_{12} = fraction of flux in core 1 switched in time τ_{s2}

$$\left.\begin{aligned} r &= \frac{R_c}{N_1^2 R_o} \\ a &= N_2/N_1 \end{aligned}\right\} \tag{21}$$

then we obtain by simple circuit analysis (if we disregard I_c):

$$F_{12} = \frac{1 + r}{a} \tag{22}$$

and

$$N_3 I_3 = N_1 I_2 \left[\frac{(r+1)^2}{ar} + a\right] \tag{23}$$

We know the desired $N_1 I_2$ from the switching characteristic of Fig. 8 and from the switching time required. This graph also gives us R_o. Thus, from the two curves of Fig. 8 and from the equivalent circuit of Fig. 27b we can calculate all of the desired parameters.

This is an elementary analysis; nevertheless it is very effective in many cases, provided that:

1. The characteristics of Fig. 8 are worked in the region where they are straight, that is, the microsecond region.

2. The current pulses applied are flat-topped and of very short rise time (< 0.1 μsec).

3. The hysteresis loop has a good squareness ratio ($s > 0.95$). Even then, the assumptions made are quite far from the real behavior; especially the assumption of square voltage waveshape. Therefore a factor of safety must be introduced in choosing the value of F_{12}; it should not be 1, which would be sufficient for ideal use, but 1/2, for example. That is,

$$F_{12} \leq 1 \tag{24}$$

We should mention that other approaches are possible with models that are more similar to the real core; for example, Rising (25) uses

$$v = v_o \left[1 - \left(\frac{\phi}{\phi_r} \right)^2 \right] \tag{25}$$

for the voltage waveform. The author has investigated various models, starting with the voltage waveform of semisinusoidal, parabolic, and even exponential shape. However, for these models, the mathematical expressions in the analysis of multiple-hole circuits become complicated to the point of impracticality, and the increase in accuracy is rather small. Therefore it was decided to use the square-wave approximation throughout the work that is reported here.

It is important to realize the limitations of this analysis and to use parameters that contain appropriate factors of safety. In particular, the approximation $\bar{R}_o$ is nearer to reality than R_o, but is much harder to measure. But because, for most cases,

$$\frac{\bar{R}_o}{R_o} = \frac{\Delta\phi}{\frac{v_{max}}{N} \cdot \tau} = \text{shape factor} \approx 0.6 \tag{26}$$

we may use

$$R_{eq} = 0.6 \times R_o \tag{27}$$

as our value of equivalent resistance. (For the derivation, see Appendix A.)

4.1.2 New Problems Arising with Multiple-Hole Circuits

The analysis of the previous paragraph ceases to be simple when used for multiple-hole circuits. The new problems that arise are discussed in the remainder of this report.

The chief new complications arise from the following: the flux division between various legs, incomplete switching arising from this division, effects of loading, necessity for blocking pulses, diodeless operation, and asynchronous delays. Also, the sheer increase in parameters, constants, and loops makes the work more complicated. However, these are minor points in comparison with the new phenomena that have to be accounted for in the analysis of multiple-hole circuits.

4.2 Approximate Methods of Dealing with Multiple-Hole Circuits

4.2.1 General Considerations

The circuit shown in Fig. 28a illustrates a simple multiple-hole transfer loop. This circuit shows most of the difficulties encountered in the analysis and design of multiple-hole circuitry.

Let us first view the ideal operation of this loop. Assume that both cores are originally in "0" state, that is, they have the flux distribution shown in Fig. 28d. If there is a "1" input to the first core at the time B, core 1 is put ideally into a "1" state (Fig. 28e); that is, all of the flux change occurs along the dotted line of Fig. 28e. Therefore no output to core 2 exists at this time. If there were no B pulse = "0" input, the core would be still in "0" state.

At pulse time D, a pulse on leg α in the first core switches the core into the perturbed "1" state of Fig. 28f if the core was previously in "1" state, and leaves it in state "0" if it was in "0" state. Thus an output occurs at time D if there was previously an input to the first core; otherwise no output occurs. This output, however, has no effect upon the second core, since it always is in "0" state at that time, and the polarity of [D] output is such that it tends to switch core 2 into the state in which it already is.

At time A, core 1 is reset by a large pulse into "0" state. If there was previously a [D] output, there will now be an [A] output that will set core 2 into "1" state.

This is an idealized picture, and the main trouble points that might prevent successful operation can be seen at a glance:

1. Because of flux-division effect (see Sec. 2.5.1), the state that results after a "1" input is not exactly that shown in Fig. 28e. There is a division of $\Delta\phi$ between the outer and inner leg, as shown in Fig. 15.

2. Pulse D, if applied to the outer leg α, as in Fig. 28a, can cause spurious unblocking along path 3 (Fig. 28d) if it is too big. This would cause a "1" output, even for "0" input. But pulse D has to be big, since it has to switch a severely loaded core (core 2 is virtually a short circuit).

Spurious unblocking can be eliminated by applying drive D to the inner leg β, as in Fig. 28b. Here, however, new trouble occurs; instead of switching along path 1, the

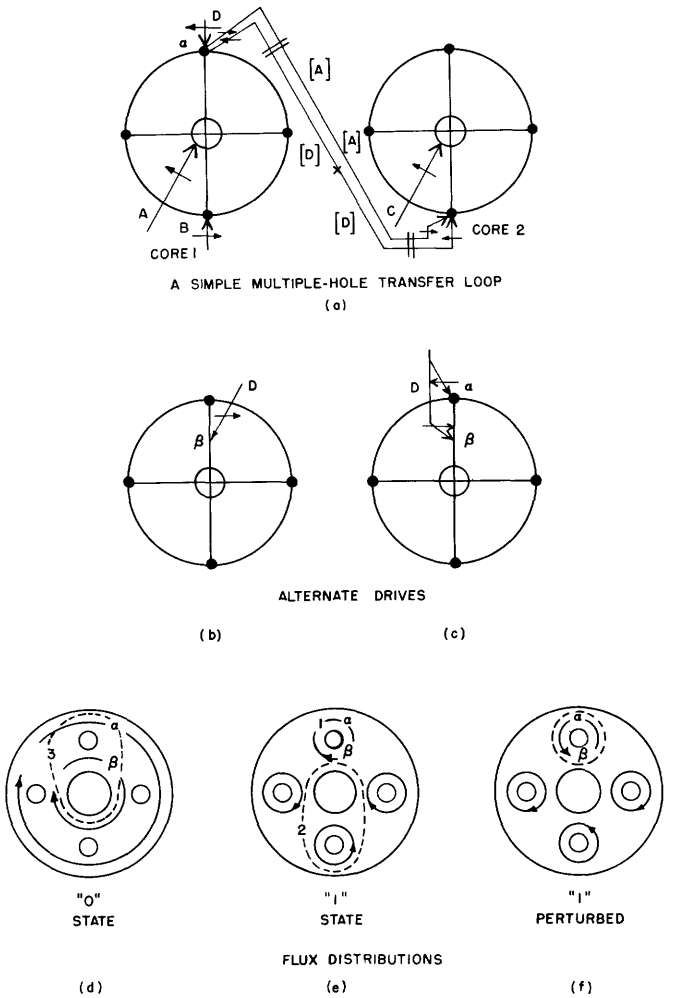


Fig. 28. Transfer loop of a multiple-hole core.

flux divides between paths 1 and 2, as seen in Fig. 28e. Because path 1 is loaded, whereas path 2 is not, most of the switching may occur in the longer path 2. This would cause "0" output for "1" input.

This is a delicate problem. One solution would be to use a divided drive, as in Fig. 28c. Another would be to use blocking pulses, as discussed in Sec. 4.2.4. The design of such a circuit requires some sort of a quantitative analysis.

The parameters that we want to design are those such as driving ampere-turns, resistors, and turns ratios. We base our analysis on the approach taken in Sec. 4.1; that is, we assume that the core looks like a resistance R_{av} while switching and like a short circuit otherwise. The best value for R_{av} would be $\overline{R}_o$, but since this quantity is not easy to measure, we can use the approximation of Eq. 27.

4.2.2 Flux Division and Loading Effects

From the preceding discussion we see that division of the flux change among two or

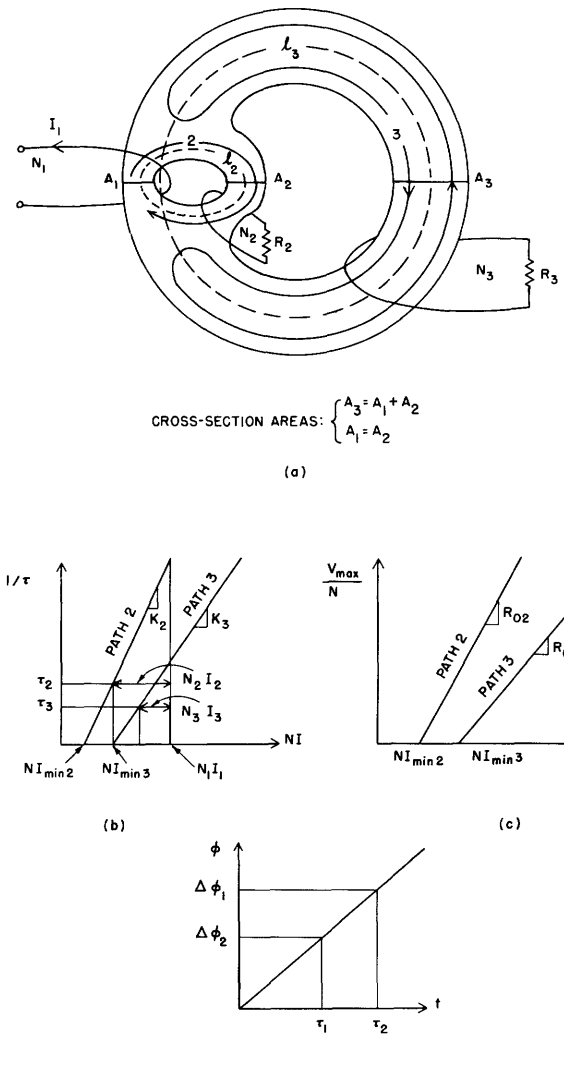


Fig. 29. Division of flux.

more paths is of great importance in the analysis and design of multiple-hole circuits. The problem is complicated further by loading effects. An approximate analysis of this question is attempted in the following paragraphs.

Consider the magnetic circuit of Fig. 29a. We can see that the current I_1 acting on winding N_1 can cause flux reversal in two paths: path 2, which goes through cross sections A_1 and A_2, or path 3, which goes through cross sections A_1 and A_3. The total flux reversal $\Delta\phi_1$ in leg 1 is equal to the sum of the flux reversals $\Delta\phi_2$ and $\Delta\phi_3$ in legs 2 and 3, respectively:

$$\Delta\phi_1 = \Delta\phi_2 + \Delta\phi_3 \tag{28}$$

The exact division between $\Delta\phi_2$ and $\Delta\phi_3$ depends upon the ratio of path lengths (ℓ_2/ℓ_3), and therefore upon NI_{min1} NI_{min2}, and also upon the loading (R_2, R_3, N_2, N_3).

Let us use

$$\left.\begin{aligned} S_2 &= \frac{\Delta\phi_2}{\Delta\phi_1}; \qquad S_3 = \frac{\Delta\phi_3}{\Delta\phi_1} \\ S_2 &+ S_3 = 1 \end{aligned}\right\} \tag{29}$$

The assumption that the voltage waveform is square means that $d\phi/dt$ is constant; that is, ϕ in all legs varies as a linear function of time, as in Fig. 29d. Let us define

τ_1 = time necessary to reverse leg 1 = real time of switching (with loading)

τ_2 = time necessary to switch leg 2 (loaded) completely

τ_3 = time necessary to switch leg 3 (loaded) completely

Thus it would take time τ_2 to reverse the core if there were no leg 3. However, there is path 3, so that the core switches in a shorter time τ_1, and the switching is accomplished before leg 2 has a chance to reverse completely. Since we have assumed a linear relationship

$$\left.\begin{aligned} \frac{\Delta\phi_2}{\Delta\phi_1} &= \frac{\tau_1}{\tau_2} = S_2 \\ \frac{\Delta\phi_3}{\Delta\phi_1} &= \frac{\tau_1}{\tau_3} = S_3 \end{aligned}\right\} \tag{30}$$

with the result that

$$\left.\begin{aligned} \tau_1\left(\frac{1}{\tau_2} + \frac{1}{\tau_3}\right) &= 1 \\ \tau_1 &= \frac{\tau_2\tau_3}{\tau_2 + \tau_3} \end{aligned}\right\} \tag{31}$$

If we make a different assumption about the voltage waveshape, we get a similar but more complicated relationship. The relationship for a semisinusoidal voltage is given in Appendix B. Oddly enough, for this particular assumption, Eq. 31 still holds.

If we now assume that the switching in each leg proceeds independently of the other (except at termination, of course) we can derive the following expressions for the assumption of square voltage waveshape (see Fig. 29b):

$$1/\tau_2 = K_1(N_1I_1 - NI_{min2} - N_2I_2) \tag{32}$$

$$V_2 = \frac{\Delta\phi_1 N_2}{\tau_2} \tag{33}$$

$$I_2 = \frac{V_2}{R_2} \tag{34}$$

After substitution, these equations can be solved to yield

$$\tau_2 = \frac{R_2 + K_2 \Delta\phi_1 N_2^2}{K_2 N_1 I_1 - K_2 N I_{min2}} \tag{35}$$

We can obtain a similar expression for τ_3 that yields

$$S_2 = \frac{\tau_3}{\tau_2 + \tau_3}$$

$$= \frac{1}{\frac{\left(R_2/K_2 + \Delta\phi_1 N_2^2\right)\left(N_1 I_1 - N I_{min3}\right)}{\left(R_3/K_3 + \Delta\phi_1 N_3^2\right)\left(N_1 I_1 - N I_{min2}\right)} + 1} \tag{36}$$

as well as a similar expression for S_3.

4.2.3 Equivalent Circuit

The approximations described in the preceding paragraphs can be used to draw the equivalent circuits shown in Fig. 30. Usually more than one equivalent circuit is needed for the various pulse times and conditions. It is convenient to note the conditions of

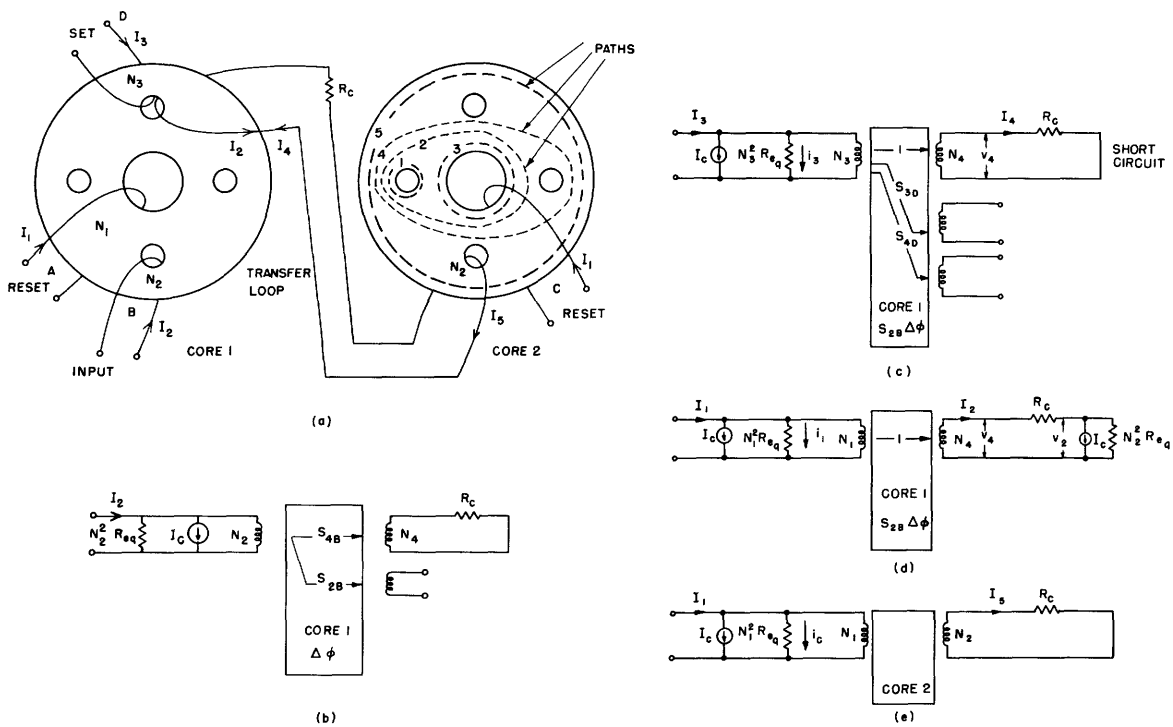


Fig. 30. Equivalent circuits of the five-hole core at various pulse times.
(a) Definitions;
(b) equivalent circuit at pulse time B with a "1" transferred into core 1;
(c) at pulse time D with "1" to be transferred from core 1 to core 2;
(d) at pulse time A with "1" being transferred from core 1 to core 2;
(e) at pulse time C with "1" being transferred out of core 2.

pulse division, as shown in Figs. 30b through 30e. The definitions of the quantities in question are shown in Fig. 30a. It is important to note the four possible flux paths that come under consideration. We need a set of switching characteristics for each of the five paths.

The R_{eq} used throughout should be the equivalent resistance for the particular flux division in question. Because this is not easy to obtain, we might take $0.6\ R_o$, where R_o is for the path that takes the bulk of the switching, or the average value of the R's for the paths if the flux divides about evenly. (R_{eq} is the least accurate figure in our approximation anyway.) The current generator I_c is as defined in Eq. 19 for the path to be switched, and is an average value if switching occurs in two paths about evenly.

From the four equivalent circuits in Fig. 30 we can obtain expressions for all of the parameters in this circuit. Thus, from Fig. 30b and Sec. 4.2.2 we can obtain the I_2 necessary to switch the core in the desired time, as well as S_{2B}.

From Fig. 30c we get the necessary N_3I_3:

$$\begin{aligned} N_3I_3 &= N_3\left(i_3 + \frac{N_4}{N_3} I_4 + I_{c1}\right) \\ &= N_3\left(\frac{v_3}{N_3^2 R_{eq}} + \frac{N_4 v_4}{N_3 R_c} + I_{c1}\right) \\ &= N_3\left(\frac{S_{2B}\Delta\phi N_3}{S_{2B}T_3 R_{eq} N_3^2} + \frac{N_4 S_{2B}\Delta\phi N_4}{N_3 S_{2B} T_3 R_c} + I_{c1}\right) \\ &= N_3 i_3\left(1 + \frac{N_4^2 R_c}{R_{eq}}\right) + N_3 I_{c1} \end{aligned} \tag{37}$$

where N_3i_3 equals the number of ampere-turns necessary to switch the core in time T_3. The analysis given in this section can be used to obtain S_{3D}. Since in "0" state N_3I_3 is working to unblock the core along path length 2, we must be careful that

$$N_3I_3 < NI_{min2} \tag{38}$$

From Fig. 30d we can obtain N_1I_1:

$$N_1I_1 = N_1i_1\left[1 + \frac{N_4^2\left(R_c + N_2^2 R_{eq}\right)}{R_{eq}}\right] + N_1I_{c1} \tag{39}$$

(Note that the reversible flux in Fig. 30d is $S_{2B}\Delta\phi$ and not $S_{2B}S_{3D}\Delta\phi$.) If we define:

F_{12} = the fraction of flux change in core 1 during T_2 (the time it takes for core 2 to switch)

then

$$V_1 = \frac{S_{2B}\Delta\phi N_4 F_{12}}{T_2} \tag{40}$$

$$\left.\begin{aligned} I_2 &= \frac{V_1 + N_2^2 R_{eq} I_{c2}}{R_c + N_2^2 R_{eq}} \\ V_2 &= \frac{\Delta\phi N_2}{T_2} \\ &= (I_2 - I_{c2})\, N_2^2 R_{eq} \end{aligned}\right\} \tag{41}$$

$$\begin{aligned} F_{12} &\approx \frac{1}{S_{2B}}\left(\frac{R_c}{R_{eq} N_2 N_4} + \frac{N_2}{N_4}\right) \\ &\approx \frac{1}{S_{2B}}\left(\frac{1 + r}{a}\right) \end{aligned} \tag{42}$$

where

$$\left.\begin{aligned} r &= \frac{R_c}{N_2^2 R_{eq}} \\ a &= N_4/N_2 \end{aligned}\right\} \tag{43}$$

(The exact value for F_{12} is given in Appendix C.) For proper operation,

$$F_{12} < 1 \tag{44}$$

Preferably, F_{12} should be approximately 1/2.

From the circuit of Fig. 30d we can obtain the conditions necessary for no feedback of information:

$$I_5 N_4 < IN_{min1} \tag{45}$$

The current I_5 is, of course, found from

$$I_1 = i_1 + \frac{N_2}{N_1} I_5 + I_c \tag{46}$$

If this circuit were a part of a shifting register, Fig. 30d and e would be combined, because in a core in the middle of the register both effects would be present. We would get

$$I_1 = i_1 + \frac{N_2}{N_1} I_5 + \frac{N_4}{N_1} I_2 + I_c \tag{47}$$

Equations 39 through 46 are modified accordingly. A similar but more complicated

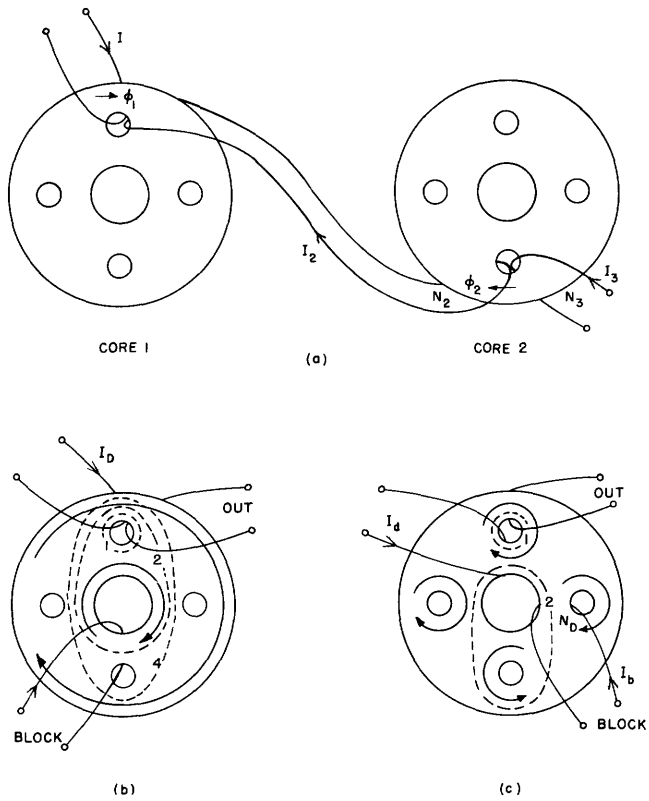


Fig. 31. Use of the blocking pulses. (a) For diode elimination; (b) and (c) for prevention of switching.

derivation could be performed for some other assumption as to the waveshape of the voltage waveform, for example, the semisinusoidal shape discussed in Appendix B.

4.2.4 Design and Blocking Pulses

By using the expressions of Sec. 4.2.3 or deriving similar expressions for other situations, we should be able to design the appropriate parameters for any logical transfluxor network by the method of Sec. III. Moreover, we should be able to eliminate all of the coupling diodes that were shown to be superfluous (by the bracketed numbers in Sec. III), and also some that were not, by the use of blocking pulses.

Blocking pulses can be used to perform two different tasks:

1. Elimination of diodes, as seen in Fig. 31a. Let us suppose that at time A we apply pulse I_1 to core 1 and that ϕ_1 and ϕ_2 have the directions shown. Current I_2 will flow and reverse core 2. If we do not want this to happen we can apply pulse I_3, which opposes I_2, with the result that

$$NI_{min} > N_2I_2 - I_3N_3 \tag{48}$$

We have to be careful to make sure either that ϕ_2 is always in the polarity shown at pulse time A, or that

$$NI_{min} > N_3I_3 \tag{49}$$

If it is the feedback pulse rather than the forward pulse that we want to eliminate,

this method can be also employed. Let us imagine that the fluxes ϕ_1 and ϕ_2 have polarities opposite to those shown in Fig. 31a. Pulse I_3 is being applied to switch core 2. The feedback can be negated by pulse I_1. Note that in the circuit of Fig. 30e (pulse time C) in the previous section, the product I_5N_4 must be less than IN_{min} (see Eq. 45). If this relationship proves difficult to attain, a blocking pulse can be applied to core 1 at this time, with the result that feedback is effectively prevented. The outer leg of core 1 happens to be invariably in the right direction at time C, and therefore a limit is set on the size of the blocking pulse.

2. Prevention of switching in undesirable flux paths. In our example, for instance, we had to limit the size of pulse I_D at pulse time D in order to prevent spurious unblocking of the core along path 2 (see Fig. 31b) if the core was in "0" state. This trouble could be eliminated by placing the drive as shown in Fig. 31c, but we would run the risk of reversing along path 2 instead of loaded path 1.

We could alleviate both of those problems by placing blocking pulses as shown in Fig. 31b and c. There is no limit on the blocking pulse in Fig. 31b, but the core can still spuriously unblock along path 4. (This is not very easy, since path 4 is long.) On the other hand, the blocking pulse in Fig. 31c is limited by the "0" condition:

$$N_b I_b < NI_{min} \tag{50}$$

Through the correct combination of all these approaches we should be able to overcome any difficulties.

4.3 Examples of Design

In order to explain further the design system developed in Sec. 4.2, we shall show two designs of transfluxor circuits that actually have been built and tested.

The transfluxors used in these examples are of the five-hole type and have the parameters given in Table 1 (as obtained from measurements of the switching characteristics).

Table 1.

Path	NI_{min} (amp-turns)	$K\left(\frac{10^6}{\text{amp-turns sec}}\right)$	$R_o\left(\frac{\text{ohms}}{\text{amp-turns}^2}\right)$	$R_{av}\left(\frac{\text{ohms}}{\text{amp-turns}^2}\right)$
1	0.3	2.76	5.00	3.00
2	0.9	2.05	3.69	2.21
3	0.7	2.25	3.95	2.37
4	1.5	1.20	2.16	1.29
5	1.6	1.11	2.00	1.20

The paths are defined in Fig. 30a; other parameters are defined in Fig. 29b and c.

Also, for the core used

$$\Delta\phi = 1.08 \text{ volt-}\mu\text{sec.}$$

Therefore the shape factor $\bar{R}_o/R_o = 0.6$.

4.3.1 Diodeless Shifting Register

A single stage of a diodeless shifting register is shown in Fig. 32. This is similar to the diagram of Fig. 30a, except that the timing is a little different, and we have added blocking pulses I_5, I_6, and I_8. These pulses serve a dual role: they eliminate any difficulty due to flux division and at the same time prevent feedback of information (I_5) and spurious unblocking (I_6 and I_8). The detailed design procedure is shown in Appendic C. This procedure demonstrates the care that must be taken in the design of diodeless circuits. The switching times at times A and C are 0.2 μsec, whereas at times B and D they are 3 μsec. (This disparity is also very characteristic of diodeless switching.) The total operation time would be about 7 μsec at least, and therefore the speed of operation could be about 140 kc (maximum).

4.3.2 Accumulator

As our second example we can use the accumulator of Fig. 24. One level of this circuit is shown in Fig. 33. Here we shall use diodes in the transfer loops and eliminate only the β diodes. Let us use a turns ratio large enough to eliminate all feedback problems. Notice that any feedback in the "carry" circuit will actually aid operation. No blocking pulses are necessary.

The detailed design of this circuit is given in Appendix D. The values obtained are: $R_{c1} = R_{c2} = 15\,\Omega$, $I_1 = 2$ a, $I_2 = 0.4$ a, $N_1 = 20$ t, $N_2 = 2$ t, $N_4 = N_5 = 24$ turns, and $N_3 = N_6 = 2$ turns. The total time of one cycle is approximately 3.4 μsec minimum.

4.4 Experimental Results

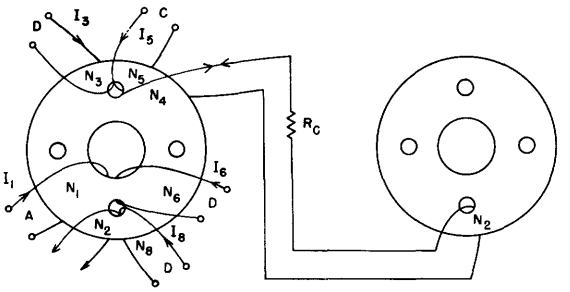
4.4.1 Results of Operation

The circuits described in Sec. 4.3, as well as similar circuitry with minor variations in design parameters, were built and tested in the laboratory. From the experience gained from these circuits, we may draw the following generalized conclusions:

1. The design and analysis equations used are extremely helpful in indicating the relationships between the various parameters.

2. The actual numbers obtained are close to the predicted values, diverging by not more than 10 per cent. This compares favorably with the tolerances in the components used: resistors, diodes, and especially cores, which are not particularly uniform from unit to unit.

3. If the circuits are built with margins of error of more than about 15 per cent they will work as designed, as did our accumulator. If the design is more critical,



$N_1 = 10$ $N_5 = 9$ $I_6 = 0.4$ a $I_1 = 1.66$ a

$N_2 = 1$ $N_6 = 4$ $I_8 = 0.4$ a $I_3 = 0.4$ a

$N_3 = 5$ $N_8 = 2$ $R_C = 0.73\,\Omega$ $I_5 = 1.66$ a

$N_4 = 2$

Fig. 32. Diodeless shifting register.

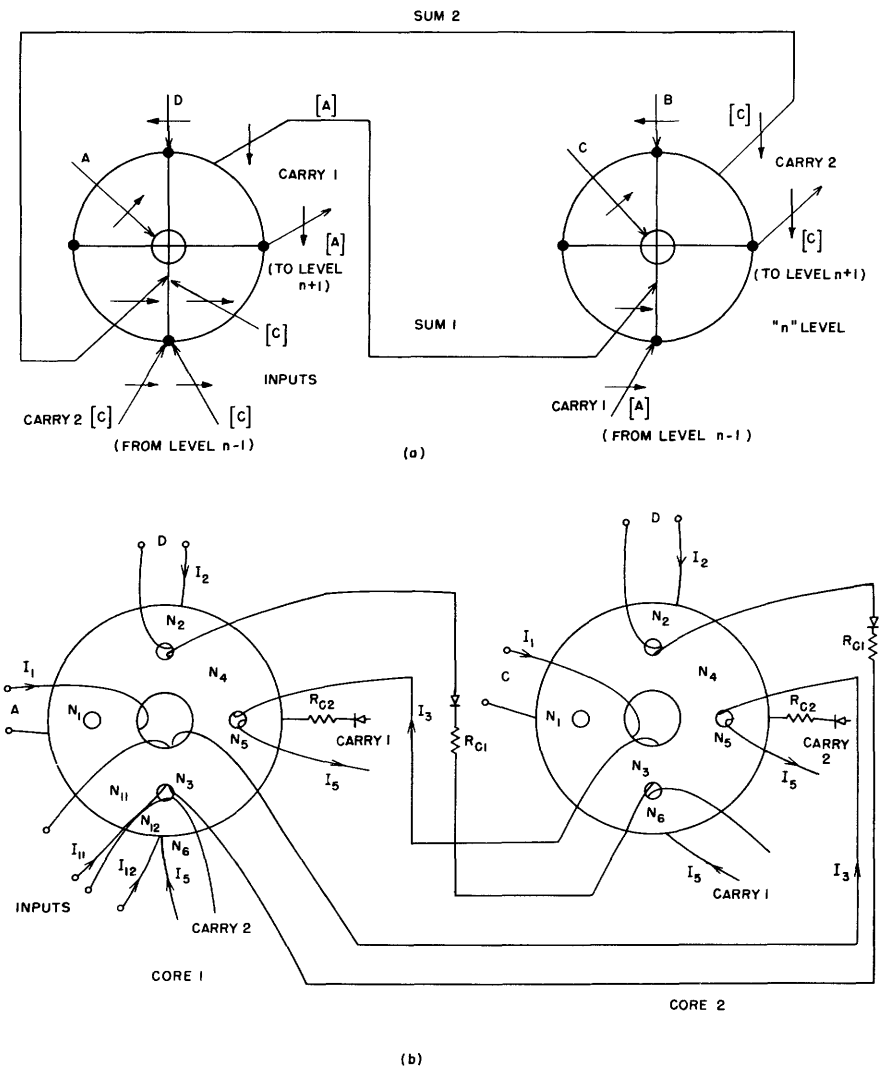


Fig. 33. Accumulator.

then, to make the circuit work, minor adjustments have to be made, the same formulas still being used as a guide. For instance, the diodeless shift register was found to work correctly for some cores only, and did not transfer correctly or spuriously unblock for others. From our design formulae (see Appendix C), it was easy to correct these troubles by increasing T_2 and decreasing I_3N_3.

4. From a comparison of our two circuits we can see the advantages of using diodes: the accumulator was much more reliable and its operation much less critical than that of the diodeless shift register. The accumulator performed satisfactorily for wide drifts in current supplies, as well as for obvious changes in parameters due to heating. On the other hand, changes of as little as 5 per cent in the current sources were enough to destroy the operation of the shift register. The reason for the difficulties caused by diodeless circuits can be understood only if we realize that, in order to have transfer in one direction only, a nonlinearity must exist somewhere in the transfer loop. The diode normally provides this nonlinearity; otherwise we have to use the inherent nonlinearity of the core – the knee of the hysteresis loop. This means that the operation is rather critical and that one of the pulses has to be small and, therefore, long.

5. Both circuits operated satisfactorily for a wide variety of pulse repetition frequencies up to about 50 kc, and even beyond that (up to their theoretical operating limits), except that they tended to overheat at higher frequencies. There should be no reason, however, why they could not operate at 100 kc, for instance, if appropriate cooling is supplied.

4.4.2 Explanation of Discrepancies Between the Theoretical and Experimental Results

As stated in Sec. 4.4.1, discrepancies exist between the predicted results and those obtained. The differences are, in some instances, as much as 10 per cent and may make the first design unworkable without some "debugging."

When all the following causes are considered, we can see that these discrepancies were to be expected:

1. The difference between the real voltage waveform and the assumed square shape.
2. The approximation employed in the flux division calculated, as well as other inherent assumptions.
3. The fact that some flux does change, even though $IN < IN_{min}$; (IN_{min} applies to total switching).
4. Various "noise" voltages, as explained in Sec. 2.5.3.
5. Inductances of the cores, as well as resistances of the wire. Both of these quantities can become important at low impedance levels.
6. Stray capacitances, which become especially troublesome at high frequencies.
7. Variations in circuit parameters due to heating, drifts, and so on.
8. Variations in circuit parameters due to nonuniformities from unit to unit.
9. Nonlinearities and general nonideal behavior of diodes.

V. CONCLUSIONS

5.1 Summary

5.1.1 Problems Studied

The main effort of the research performed was directed toward integrating multiple-hole cores into logical circuitry. This included the following problems:

1. Analysis of circuits with multiple-hole cores; the setting up of a consistent, workable system of approximations that would be as close as possible to the observed behavior.
2. Development of a design procedure based on these approximations.
3. A study of the problem of elimination of diodes and the effect of this upon the circuit behavior.
4. Development of an understanding of logical properties of multiple-hole cores; an attempt at logical design.
5. Development of a workable, schematic notation for multiple-hole logical circuits.
6. Gaining additional understanding of the physical behavior of multiple-hole cores.

5.1.2 Conclusions Reached

All the problems of Sec. 5.1.1 have been at least partially solved. Thus a workable analysis procedure, based on square voltage waveform, has been developed and has taken into account the use of blocking pulses, diodeless operation, loading effects, and – most important – flux division. This analysis can serve as a basis for a design procedure, which has been tested and found to be quite useful, and can give results that, usually, deviate from the actual behavior by not much more than the variations in the components used.

Other, more complicated, basic assumptions were investigated, but they were found too cumbersome mathematically and they did not result in any substantial gain in accuracy.

Much effort was spent on the problems of eliminating diodes from magnetic-core circuits. It was found possible to build diodeless transfluxor circuits through the use of blocking pulses and appropriate timing. However, diodeless circuits were found to be inherently more difficult to design; they may require more pulse times, and thus more drivers; they require at least one long switching time, and thus are much slower than comparable circuits with diodes; they require more driving energy, which dissipates in the resistances; their design is much more delicate, and they are more sensitive to any variations in parameters or drifts in driving currents, and hence much less reliable. Thus, the price for the elimination of all diodes is quite high. On the other hand, in many instances, some diodes can be eliminated without much trouble; for example, the β diodes (Fig. 19a).

In the field of logical design, a schematic notation has been developed, and an

approach to logical synthesis procedure using the developed "gate box" approach has been outlined. This is still not the complete solution, and work should be extended in this area.

As a by-product of this investigation, some effects in the physical behavior of the multiple-hole core were discovered; they may shed some light on the question of switching and physical behavior of transfluxors and cores in general. Thus in Sec. I, we mentioned the flux-division effect, the delay effect, and the near-leg effect.

In general, it was found that multiple-hole cores are, in many ways, superior to simple cores and that the use of multiple-hole core logical circuitry is quite feasible in the microsecond region and could possibly be extended into the 1/10-microsecond area. The multiple-hole cores, like other magnetic cores, are very reliable and are not affected adversely by radiation or other severe conditions that might exclude other components. By making more and more complicated cores we should be able to combine into one core many units that previously were separate, with the accompanying reduction in wiring and other components.

On the other hand, the cores require large drivers, dissipate a great deal of power, and, as yet, are not workable at frequencies higher than about 10 megacycles. At present, it seems that the best field of application for multiple-hole cores would be in the control area.

In any case, multiple-hole cores are very promising components, although practically unknown and unexplored.

5.2 Suggestions for Future Research

The following topics indicate some of the areas of multiple-core design that, in the opinion of this author, are particularly in need of further research:

1. Logical design: applications of switching circuit theory, particularly the sequential switching theory, to transfluxor circuits.

2. Theoretical work on multiple-hole cores. Without a better (quantitative) understanding of the processes of switching and flux distribution, no real further progress is possible.

3. Design of the cores themselves to suit the particular needs of the designer: a topological study of multiple-hole cores and the relationship between the core topology and the logical functions obtainable from it; the design of the cores for minimum energy dissipation, optimum switching time, or signal-to-noise ratios.

4. Optimization of multiple-hole core circuits with respect to time, energy, noise, etc.

5. Design of multiple-hole core circuits using the "variable reactor" or "current steering" principles.

6. Problems of interaction between different kinds of multiple-hole cores, or between multiple-hole and simple cores. Problems of interaction between multiple-hole cores and other (nonmagnetic) circuit elements.

7. Applications of thin films (46) to multiple-hole cores. This is a completely unexplored possibility that definitely is worth studying. This would open up some completely new horizons and might make multiple-hole cores feasible, or even superior, in computer applications.

APPENDIX A

RELATIONSHIP BETWEEN R_o AND $\overline{R}_o$

During switching, the energy input to the core is (27):

$$W_{in} = \int_0^T e\, i\, dt = I \int_0^T e\, dt$$

$$= I \int_0^T \frac{d\phi}{dt}\, dt = I \int_{-\phi_r}^{\phi_s} d\phi \qquad (A.1)$$

$$= I(\phi_s + \phi_r) = I\Delta\phi$$

See Fig. A-1.

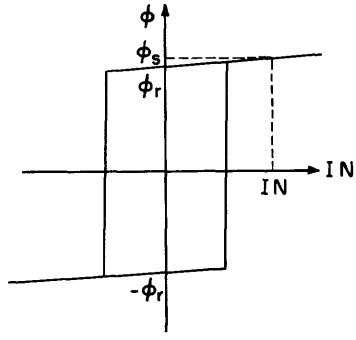


Fig. A-1. Hysteresis loop.

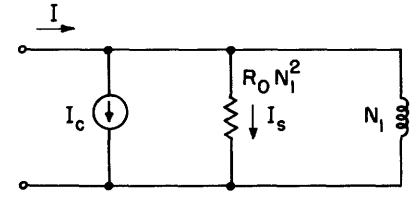


Fig. A-2. Equivalent circuit.

If we disregard the small reversible part of flux change, which is usually too small to make a difference of more than 5 per cent, we can define an equivalent resistance (see Fig. A-2):

$$N_1^2 \overline{R}_o = \frac{W_{in}}{T I_s^2} = \frac{I\Delta\phi}{I_s^2 \tau_s} \qquad (A.2)$$

$$\overline{R}_o \approx \frac{\Delta\phi}{I_s \tau_s N^2} \qquad (A.3)$$

where we can make the approximation

$$I_s = I - \frac{NI_{min}}{N_1} \qquad (A.4)$$

On the other hand, from the switching characteristics (Fig. A-3) we can derive R_o:

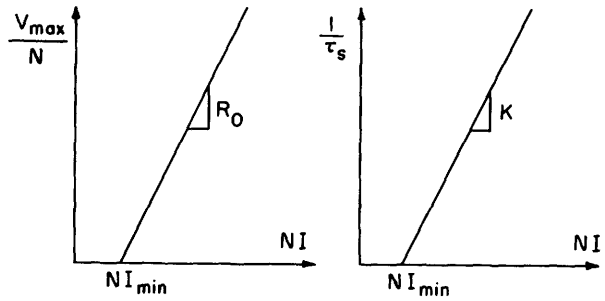


Fig. A-3. Switching characteristics.

$$R_o = \frac{v_{max}/N}{N^2\left(I - \frac{NI_{min}}{N_1}\right)} \tag{A.5}$$

and therefore,

$$\frac{\overline{R}_o}{R_o} = \frac{\Delta\phi N^2(I - NI_{min}/N_1)}{\tau_s N^2(I - NI_{min}/N_1)\, v_{max}/N}$$

$$= \frac{\Delta\phi}{\tau_s\, v_{max}/N} \tag{A.6}$$

but,

$$\frac{\tau_s\, v_{max}}{N} = \frac{R_o}{K_1} \tag{A.7}$$

Therefore, to be consistent we have

$$\frac{\overline{R}_o}{R_o} = \frac{\Delta\phi}{R_o/K_1} = \text{shape factor} \tag{A.8}$$

In most cases the shape factor is approximately 0.6 to 0.7.

APPENDIX B

FLUX DIVISION FOR SEMISINUSOIDAL VOLTAGE WAVEFORM

We can assume the switching voltage waveform to be semisinusoidal in shape, with the result that the flux varies with time, as shown in Fig. B-1:

$$\phi_2 = \frac{\pi\Delta\phi_1}{2\tau_2}\int_0^t \sin\frac{\pi t}{\tau_2}\,dt$$

$$= \frac{\Delta\phi_1}{2}\left(-\cos\frac{\pi t}{\tau_2} + \cos 0\right) \qquad \text{(B. 1)}$$

$$= \frac{\Delta\phi_1}{2}\left(1 - \cos\frac{\pi}{\tau_2}\,t\right)$$

At time τ_1

$$\left.\begin{aligned}\Delta\phi_2 &= \frac{\Delta\phi_1}{2}\left(1 - \cos\pi\frac{\tau_1}{\tau_2}\right)\\ \text{and also}\\ \Delta\phi_3 &= \frac{\Delta\phi_1}{2}\left(1 - \cos\pi\frac{\tau_1}{\tau_3}\right)\end{aligned}\right\} \qquad \text{(B. 2)}$$

Therefore

$$\Delta\phi_1 = \frac{\Delta\phi_1}{2}\left(1 - \cos\pi\frac{\tau_1}{\tau_2} + 1 - \cos\pi\frac{\tau_1}{\tau_3}\right) \qquad \text{(B. 3)}$$

and

$$\tau_1 = \frac{\tau_2\tau_3}{\tau_2 + \tau_3} \qquad \text{(B. 4)}$$

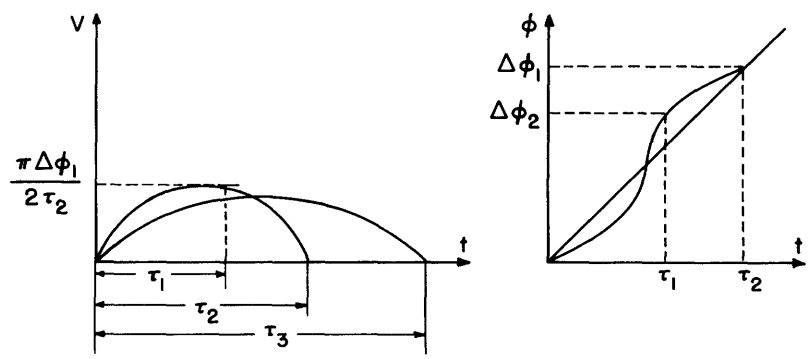


Fig. B-1. Assumed voltage and flux.

APPENDIX C

THE DESIGN OF THE DIODELESS SHIFT REGISTER

From the circuit of Fig. 32, Sec. 4.3.1, we can derive the equivalent circuits shown in Figs. C-1 and C-2.

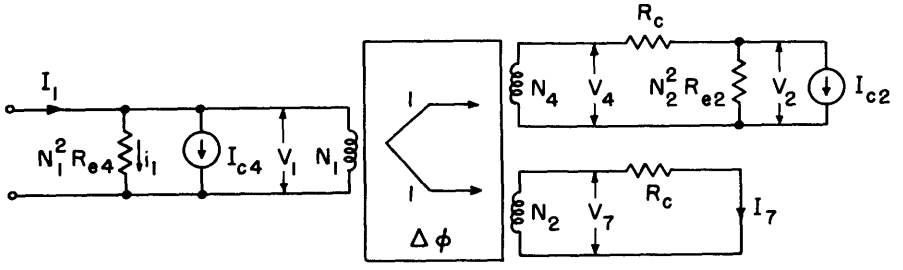


Fig. C-1. Equivalent circuit at time A.

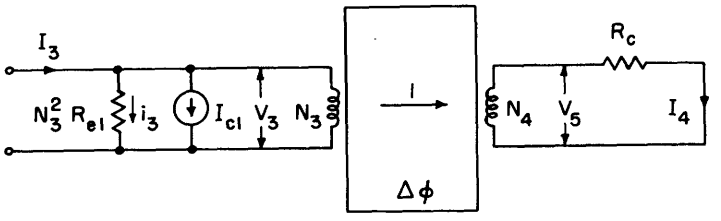


Fig. C-2. Equivalent circuit at time D.

From these two diagrams and the necessary conditions for switching and nonswitching, we can obtain the following limiting conditions (the definitions of flux paths and constants are those given in Table 1, Sec. 4.3):

$$N_3 I_3 - N_8 I_8 < IN_{min4} \tag{C.1}$$

$$N_3 I_3 - N_6 I_6 < IN_{min2} \tag{C.2}$$

$$I_2 N_2 > IN_{min2} \tag{C.3}$$

$$I_2 N_2 + I_7 N_4 - I_5 N_5 < IN_{min4} \tag{C.4}$$

$$I_1 N_1 > IN_{min4} \tag{C.5}$$

$$I_3 N_3 > IN_{min1} \tag{C.6}$$

$$I_8 N_8 < IN_{min2} \tag{C.7}$$

Also, because we want to use only one current supply at any one pulse time (with

series connections),

$$I_5 = I_1 \tag{C.8}$$

$$I_3 = I_6 = I_8 \tag{C.9}$$

The condition for transfer is

$$1 > F_{12} = \frac{R_c + R_{e2}N_2^2}{R_{e2}N_4N_2} + \frac{I_{c2}R_c T_2}{\Delta\phi N_4} \tag{C.10}$$

Other equations used in the design are

$$\frac{1}{T_2} = K_2(I_2N_2 - IN_{min2}) \tag{C.11}$$

$$\frac{1}{T_1} = K_1(N_3i_3) \tag{C.12}$$

These equations are merely the switching characteristics. In addition, we can write the relationships among the various currents:

$$N_1I_1 = N_1i_1 + N_1I_{c4} + N_4I_2 + N_2I_7 \tag{C.13}$$

$$N_3I_3 = N_3i_3 + N_3I_{c1} + N_4I_4 \tag{C.14}$$

where

$$I_2 = \frac{\Delta\phi N_4F_{12} + N_2^2R_{e2}T_2I_{c2}}{T_2\left(R_c + R_{e2}N_2^2\right)} \tag{C.15}$$

$$I_7 = \frac{\Delta\phi N_2F_{12}}{T_2R_c} \tag{C.16}$$

$$i_1 = \frac{\Delta\phi F_{12}}{T_2R_{e4}N_1} \tag{C.17}$$

$$I_4 = \frac{\Delta\phi N_4}{T_1R_c} \tag{C.18}$$

$$i_3 = \frac{\Delta\phi}{N_3R_{e1}T_1} \tag{C.19}$$

If we use $N_3I_3 = 2.1$ (from Eqs. C.1 and C.2) and $N_8I_8 = 0.8$, we get

$$2.1 = \frac{1}{T_1}\left(\frac{1}{2.76} + \frac{1.08N_4^2}{R_c}\right) \tag{C.20}$$

By using Eqs. C.12, C.14, C.18, and C.10, we obtain:

$$F_{12} \cdot 2.21 \cdot 1.08 \cdot N_4 \cdot N_2 = \left(R_c + 2.21 \cdot N_2^2\right) \cdot 1.08 \cdot 2.21 \cdot 0.9 \cdot N_2 R_c T_2 \qquad \text{(C.21)}$$

The following relation is necessary to give real solutions for N_2:

$$(T_2 \cdot 2 \cdot R_c - F_{12} \cdot 2.4 \cdot N_4)^2 \geq 10.4 \cdot R_c \qquad \text{(C.22)}$$

Therefore we choose $T_1 = 3$, $T_2 = 0.2$, and $N_4 = 2$. This, in turn, gives us $F_{12} = 0.726$, $N_2 = 1$, and $R_c = 0.73$ ohm. By application of the remaining equations and judicious choice of the numbers of turns we obtain the remaining parameters, as listed in Sec. 4.3.1.

APPENDIX D

DESIGN OF THE ACCUMULATOR

The circuit for one digit-plane of the parallel accumulator is shown in Fig. 33, Sec. 4.4.1. Of major importance in this circuit is the division of flux between paths 2 (or 3) and 5. (See Fig. 30, Sec. 4.2.3, for definitions of the flux paths.) This flux division occurs if there is one single input. If we ignore feedback currents and use the methods of Sec. 4.2.2, we can calculate the portion of flux in leg 2 (note that there is no loading in either leg):

$$S_2 = \frac{K_2(N_6I_5 - NI_{min2})}{K_5(N_6I_5 - NI_{min5}) + K_2(N_6I_5 - NI_{min2})} \approx 0.75 \qquad (D.1)$$

for large values of N_6I_5. The flux division is much more favorable for flux path 3. The flux division determines the available output at the "sum" winding and the undesirable noise at the "carry" winding.

The limits are:

$$N_3I_3 > NI_{min3} \qquad (D.2)$$

$$N_6I_5 > NI_{min5} \qquad (D.3)$$

$$N_6I_N < NI_{min2} \qquad (D.4)$$

$$N_1I_1 > NI_{min5} \qquad (D.5)$$

$$N_2I_2 > NI_{min1} \qquad (D.6)$$

$$N_2I_2 < NI_{min2} \qquad (D.7)$$

Also:

$$\left.\begin{aligned} N_{11}I_{11} &\approx N_3I_3 \\ N_{12}I_{12} &\approx N_6I_5 \end{aligned}\right\} \qquad (D.8)$$

For the condition of a single input, core 1 can be represented at time A by the equivalent circuit of Fig. D-1.

There may be also a feedback current in the "carry 2" winding, which, however, can be neglected as a first approximation. From this circuit:

$$F_{12} = \frac{R_{c1} + R_{e3}N_3^2}{0.75 \cdot R_{e3}N_4N_3} + \frac{I_{c3}R_{c1}T_1}{0.75 \cdot \Delta\phi \cdot N_4} \qquad (D.9)$$

If we make $N_3 = 2$, $N_4 = 24$, $T_1 = 0.2$ microsecond, and $R_{c1} = 15$ ohms (the forward resistance of the diodes used), we obtain $F_{12} \approx 0.67$, which is sufficient. Also,

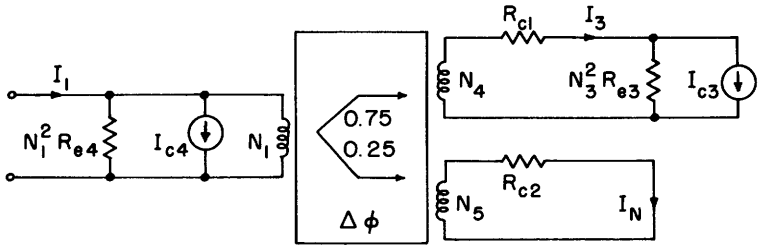


Fig. D-1. Equivalent circuit at time A with 01 output.

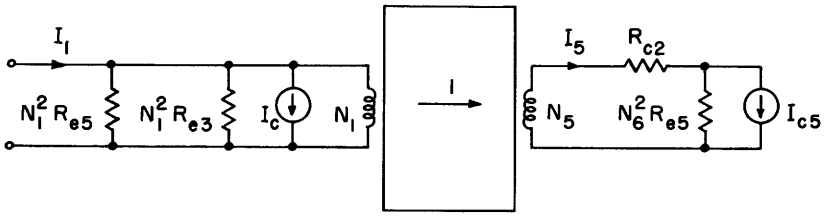


Fig. D-2. Equivalent circuit at time A with 10 output.

$$I_N = \frac{0.25 \cdot 0.67 \cdot \Delta\phi \cdot N_5}{R_{c2}} \qquad \text{(D. 10)}$$

For the condition of two inputs to core 1, the equivalent circuit at the time A is shown in Fig. D-2. (Feedback currents are neglected.)

The rest of the design is simple and similar to that of Appendix C. The results are listed in Sec. 4.3.2.

Acknowledgment

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