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Development of a CMOS Preamplifier for Single Ended Magnetoresistive Heads

by

Iyad Obeid

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degrees of
Bachelor of Science in Electrical Engineering and Computer Science
and Master of Engineering in Electrical Engineering and Computer Science
at the Massachusetts Institute of Technology

May 22, 1998

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ABSTRACT

A CMOS preamplifier was designed to bias and read a single stripe magneto-resistive hard disk drive head. The CMOS circuit is designed as a first pass at replacing an existing Texas Instruments bipolar technology circuit that performs the same task. The design constraints were to match the operating parameters of the existing bipolar circuit, most important of which was the noise floor. The measured input referred noise level of the designed CMOS preamplifier (measured using an integrated noise technique) was $22\mu V$, as compared with that of the existing bipolar circuit, $12.9\mu V$. An alternate architecture was also explored, but was found to have deficient bandwidth.

Thesis Supervisor: Professor Charles Sodini
Title: Professor of Electrical Engineering and Associate Director, Microsystems Technology Laboratory

Company Supervisor: Ken Maggio
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1. Introduction

The goal of this research was to design a CMOS circuit (using one of two different architectures) to perform within the same design parameters as an existing circuit built using bipolar technology. The circuit in question was designed to bias a hard disk drive single stripe magneto-resistive (MR) read head and to sense and amplify the data signal generated by this head. The existing circuitry, currently in production by the TI preamplifier design team in Dallas, TX, uses a bipolar technology to implement a simple feedback loop that forces a constant bias current throughout the MR head, and a current sense mechanism to detect and amplify the input signal. Each of the two new architectures uses CMOS technology, as it is believed that a CMOS read amplifier will be smaller and cheaper to manufacture.

The hard drive preamplifier is a circuit that biases the hard drive read head and amplifies data being read off of this head. Hard drive read heads come in several varieties, each with different characteristics, and thus each requiring a different preamplifier. At Texas Instruments, pre-amps are designed for magneto resistive heads. An MR head can be thought of as a variable resistor. The head typically has a 'resting' resistance of $R_{MR} = 30\Omega$. During the read mode, this head resistance changes slightly in time as the MR head, mounted on the drive actuator arm, passes through regions of different magnetization. This is a result of the device physics of the head, a topic beyond the scope of this paper. The deviations in head resistance in response to areas of different magnetization are the pre-amp circuit's input signal. The preamplifier detects and amplifies this signal and passes it on to the read channel, where the signal is digitized, processed, and interpreted as a binary data bit-stream.

There are several known methods of establishing the pre-amp read circuit, all of which are implemented on the market today in bipolar technology. As CMOS processes improve however, industry researchers have been moving forwards with development of a purely CMOS reader which, if developed, could be mass-produced cheaper than an equivalent bipolar reader. The primary goal of this research was thus to investigate the

development of a CMOS read preamplifier. Two different architectures were considered for the CMOS design. The first such architecture is the same as the bipolar architecture with CMOS components simply swapped in for the bipolar ones. The second proposed CMOS architecture is taken from a paper written by Klein and Robinson [1]. In their paper, Klein and Robinson propose a more complex architecture for the CMOS reader but argue that the added complexities pay off in terms of system performance.

1.1. Organization of this Thesis

For my research, I have prepared a complete analysis of the existing bipolar circuit, as well as a CMOS design for accomplishing the same task. Each is evaluated in terms of the relevant system parameters, namely bandwidth, gain, and most importantly, noise. Since bipolar technology is inherently quieter than CMOS, meeting the system noise requirements is the most technically challenging design aspect.

Section 3 describes the methods of this thesis. In particular, the method of circuit design is discussed, as well as the measurement standard developed for quantifying circuit noise measured in SPICE simulations. Section 4 explains the formulas and physics behind some of the more useful noise equations that are applicable to the read amplifier circuitry.

In Section 5 of this thesis, I will present an analysis of the existing TI bipolar architecture, including circuit simulations predicting performance parameters, as well as circuit equations that verify the simulated results.

In Section 6, I will present a parallel analysis of the TI architecture CMOS design. This will also include circuit simulations and hand calculations to verify the simulated results. An explanation of the functional differences in circuit behavior will also be explained. Section 7 will show the optimization process taken to improve the noise behavior in the CMOS design. The alternate architecture design, which was found to be insufficiently fast to serve as a hard disk drive preamplifier, will be presented briefly in the Appendix.

Finally, in Section 8, the CMOS and bipolar designs will be compared, and recommendations will be made regarding the feasibility of the design of a CMOS preamplifier. The ultimate purpose is to present a clear, factual comparison between the designs in order for the production staff at TI to determine the practicality of pursuing a CMOS pre-amp reader.

1.2. Background

The hard drive preamplifier is typically a dual function IC. While part of the chip is responsible for writing an analog signal onto the magnetic hard drive platters, the other part is responsible for reading the magnetically stored data and preprocessing it for the read channel IC. The scope of this research extends solely to the reader functions of the preamplifier.

The preamplifier reader is typically divided into three stages. The first stage is responsible for biasing the read element (in this case, the MR head) and providing a small amount of signal gain. The second stage provides a high-speed signal gain, while the third stage provides some signal gain as well as some subtle error detection such as thermal asperity detection. The second and third stages are also beyond the scope of this study. Because they consist solely of high-speed differential amplifiers, these stages do not set the fundamental system bandwidth. Furthermore, because of the large gain in each of these stages ($A_v \approx 50$), noise generated there referred all the way back to the first stage input will be divided by the large gain and will thus be relatively negligible. Therefore, it is the first stage that sets most of the preamplifier performance characteristics and thus requires the most analysis.

The goal of the CMOS design is to build the CMOS first stage to meet the system characteristics of the bipolar first stage. These system parameters, as will be shown later, are:

Parameter	Target
Gain	12.9 dB

Bandwidth (low)	176 kHz
Bandwidth (high)	300 MHz
Noise	12.9μV*

*Integrated noise – see Section 3.3

2. Literature Review

Many designs for preamplifiers (both CMOS and bipolar) have been published recently in various industry publications. These preamplifiers are designed for a variety of applications, ranging from audiocassette playback to measurements in particle colliders. Each of these specialized applications places a unique set of constraints on the amplifier design. Most of these designs however are set to operate at conditions unsuitable for hard disk drive applications.

2.1. Bipolar Designs

Several interesting designs in bipolar technology suggest ideas that may be exploited in the development of a low noise CMOS preamp for a magnetoresistive drive head. Monti et al present a design for a low noise tape preamplifier in which a single ended input is fed into a differential pair that is self biased with a feedback loop. The loop is externally compensated with an RC pair [2]. The concept of the self-biased closed loop architecture suggests high stability and will be exploited in the CMOS preamp design. In their design of a CMOS preamplifier for capacitative sensors, Stefanelli et al use PMOS devices as the system input (for high input impedance), but then insist on using bipolar technology for the gain stage [3]. They argue that the higher transconductance of bipolar transistors coupled with their extremely low 1/f noise make them superior to CMOS devices for gain purposes. Overcoming the sub optimal transconductance properties of CMOS will be a repeated problem in this research. These two preamplifier designs are fundamentally inadequate as a guide for the design of an MR head preamplifier however, as they are not required to bias the read element in any fashion. Biasing the MR head with the preamp (either voltage or current bias) will be of central relevance in the MR preamp design.

2.2. CMOS Designs

In addition to the bipolar architectures, several CMOS designs for preamplifiers also exist in the literature, although none possess the bandwidth necessary for a read head in a high-speed disk drive. One design, presented by Kleine et al, shows a folded cascode

configuration that amplifies bioelectrcal signals such as brain activity [4]. The CMOS solution however depends on an operating temperature of 4.2K, which is egregiously below the required read head operating temperature of approximately 300K. Like the Stefanelli preamplifier, this preamp uses the gate of a large FET for a high input impedance pathway. The input FET is made especially large $\left(1000/_2\right)$ to reduce input referred noise [4]. These are both techniques that will be used in the design of the magnetoresistive preamplifier. Unfortunately, the bandwidth is only 300kHz which is quite low compared with the 200-300MHz desired 3dB point for the CMOS MR head preamp.

2.3. Current Mode Designs

So far, all of the papers discussed use voltage mode architectures to amplify the signal. While voltage mode has some inherent benefits (especially with CMOS, namely infinite input impedance into an nFET gate), current mode amplifiers can also be used to achieve the same goal. Anghinolfi et al use a basic current mirror architecture to gain a current input applied to the source of a biased input FET [5]. They adapt this simple concept into a current mode preamplifier by using a resistor as a feedback path. A more elaborate current mode solution is presented by Klein and Robinson who use a programmable current source to bias an MR element and then gain the small signal current input with a current mode amplifier (see Figure 30) [1]. This technique works nicely in theory, using the low input impedance of the current mode amp to boost both gain and power supply rejection. However, the Klein and Robinson architecture is designed for an MR head in a tape drive, and thus operates at speeds too low for hard drive application. This architecture is a good departure for the traditional voltage mode circuitry and is worth exploring further as a possible architecture for the hard drive application.

2.4. Noise Considerations

In all of the reviewed literature, very little is said about standard techniques of measuring circuit noise. Most of the articles offer means of predicting circuit noise by way of equation, but do not present the method by which they determine the single figure

representation of the noise content. This is a matter that will be addressed in the methods section of this study.

Several of the papers suggest a multistage design to reduce input referred noise. The first stage is always the most crucial for noise performance [2], as input referred noise in subsequent stages will be divided by the composite gain of all previous stages and thus greatly reduced. Furthermore, increasing input impedance can reduce input referred noise [3]. In circuits gaining a signal attained from a read head device, it is generally impossible to remove the noise component due to that device [2]. The goal of noise optimization is therefore reduced to the reduction of input referred noise in circuit elements, most of which will tend to reside in the large input device [1].

2.5. Other Constraints

Several other design constraints are suggested by the literature. One such constraint is that when biasing the MR head, the head should be placed as close to ground as possible (Figure 1b). This is done in order to avoid the buildup of a sizeable potential between the MR head and the hard disk surface, which could damage either the MR element or the disk surface if discharged suddenly (Figure 1a) [6].

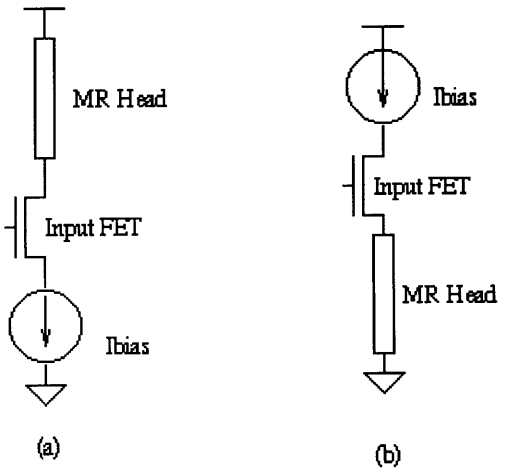


Figure 1: Options for placement of MR head

(a) MR head is placed close to Vdd , (b) MR head is placed close to ground

This means that current biasing sources should be placed between power and the read element, which in turn will connect to ground [1].

Finally, in actual practice, the preamplifier device will be amplifying signals read from a number of different drive heads. Multiple drive heads are often used, generally with one head dedicated for each of the platters in a hard drive. This implies that a multiplexer architecture must also be factored into the design. It is important to choose an architecture that degrades neither the noise performance nor the bandwidth of the original single head device [6].

3. Method

This section will describe the various methodologies used in the design and testing of the CMOS preamplifier.

3.1. Design

The circuit design of the CMOS preamplifier was based closely on the existing Texas Instruments bipolar solution. For the new design, I started with the bipolar block diagram and then designed CMOS circuits to implement each of those blocks

The first stage of the bipolar preamplifier is the primary sensing unit, and is responsible for setting both the noise and bandwidth characteristics of the entire preamplifier. The main blocks within this stage are the transconductance (Gm) block, the Gm biasing block, and the input cascode tree (which included the MR head). The other crucial design block is the multiplexer circuitry, which allows the preamplifier to accept input from any one of eight separate MR heads.

The design is approached in a block-down style, which means that most of the circuit will be implemented with ideal components in SPICE until the circuit is made to function properly. Then, one by one, each of the idealized blocks will be replaced by an actual CMOS design that, when put in the circuit, produces the same result. For the first design pass consisted of the input cascode tree feeding into an ideal differential transconductance amplifier whose second input was an ideal voltage bias. Once this simple circuit had been perfected, the ideal transconductance amplifier was replaced with an actual CMOS circuit that mimicked the performance of the ideal one. Finally, the biasing was replaced with a bias current source that was mirrored to all the nodes requiring a bias current.

All circuit design was performed in Mentor using the Texas Instruments five volt 0.8μm BiCMOS process. Simulations were performed in TISPICE, a TI internal version of the SPICE simulation tool. TISPICE uses the BSIM3 algorithm to model transistor behavior.

3.2. Optimization

Once the basic design was found to work, FET sizes and bias currents were systematically adjusted to procure the optimal speed and noise performance from the preamplifier. The optimization phase was done primarily to determine optimal sizing of M_2 and R_2 (Figure 11) with respect to gain, bandwidth, and noise. This was done by holding all variables constant while varying one parameter (such as M_2 width or length) and running simulations that measured the gain, bandwidth, and noise. Once M_2 was optimized, the process was repeated to determine the ideal size for R_2, and then to a lesser extent, the ideal M_1 size and the ideal bias current level.

3.3. Noise Measurement

The reduction of noise in the preamplifier circuit was of paramount importance, as excessive noise contamination inhibit the ability of the circuit to detect small input signals. In order to reduce circuit noise, a method first had to be devised to accurately quantify noise behavior by computer simulation. There were several possible options for accomplishing this goal. The accuracy of any such methods is ultimately dependent on the accuracy of the SPICE noise models for the process in question. This point introduces a degree of uncertainty into the picture that will be addressed later.

The criteria for a noise measurement method were straightforward. First, the method had to be quick and easy to perform, as dozens of noise measurements were often performed at a time. Secondly, the method had to be an accurate single number representation of the noise performance. It may seem overly simplistic to reduce a noise simulation taken over two or three orders of magnitude to a single number. However, in order to facilitate quick and objective comparisons between noise performances of different circuits, a single figure of merit was necessary.

SPICE offers two techniques of deriving noise performance information about a circuit. The first involves injecting non-deterministic noise at the input of each noise contributing

device and then summing the resultant noise at a specified node. This results in a time domain transient sweep. It was found that this sweep was slow to simulate and difficult to interpret due to the non-deterministic nature of the data. The second method SPICE has is to place an AC source equal to the equivalent input noise for each device at the input of that device. The user specifies both input and output nodes where the noise is to be summed. SPICE produces an AC analysis reflecting the summed input referred noise. Since this simulation is easy to set up, quick to execute, and produces useful data curves, it was selected. A typical input referred noise curve is shown below.

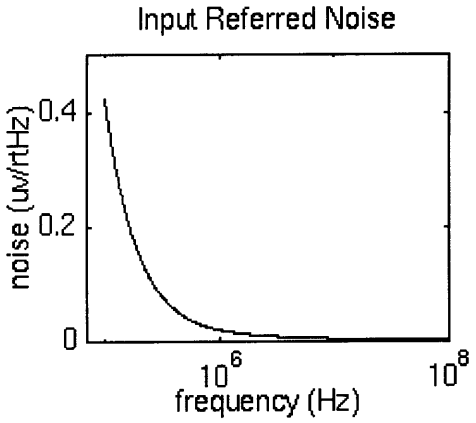


Figure 2: Typical input referred noise curve

The goal now is to reduce this curve to a single figure of merit that accurately quantifies its noise content. One approach is to pick a fixed frequency and read off the noise value at that point. This approach was ignored however because it varies too much from run to run. For example, changing a transistor size will affect the frequency response of the signal. Since input referred noise is divided back from the output by the frequency response, a change in frequency response alone at a specific frequency may be incorrectly interpreted as a change in noise performance at that frequency.

Another approach is to scan for the minimum noise measurement. This idea, while reasonable in theory, proved cumbersome to measure. Furthermore, it does not reflect the noise characteristics at all frequencies, but merely at one point.

A better idea was to calculate a simple arithmetic mean of the data. This idea failed for two reasons. Primarily, the signal plotting software SIMGRAPH does not automatically perform arithmetic means on signals. In order to compute the mean, each signal file must be manually edited, read into MATLAB and averaged there. This was unacceptably complicated. The second draw back of this method was that because the data is produced logarithmically, it becomes difficult to procure an accurte mean. An arithmetic mean taken on geometrically spaced points will be weighted disproportionaltely in favor of lower frequencies.

Finally, after consulting Jim Hellums, the noise analysis expert at Texas Instruments, an acceptable procedure was devised that works by feeding the SPICE analysis output file into a TI internal C program named INTNOISE, which integrates the noise relative to its logarihmic frequency axis. This procedure is quick, easy to execute, and uses every point in the noise analysis. Furthermore, the resulting figure of merit is acutally a quantification of the noise power over the bandwidth in question.

The only caveat about this method is that it is essential to determine the frequency band over which the input referred noise is to be integrated. Since the circuit will never be used outside the boundaries of its –3dB bandwidth, the noise must only be integrated within the –3dB points. However, since the –3dB points tend to shift from simulation to simulation with changes in the circuit, two arbitrary limits were set for the frequency: $1MHz < f < 100MHz$. These were picked because they always contain most of the valid frequency noise data. Thus, in order to procure the desired noise analysis, a typical SPICE stimulus file would contain the following lines to measure noise.

```
.noise v(out2,out1) vmr
.ac dec 200 1e6 100e6
.punch noise inoise
```

In order to determine a benchmark against which to compare noise performance, the originally stated benchmark of $0.5nv/\sqrt{Hz}$ must be integrated:

$$v_i = 0.5nv/\sqrt{Hz}$$

$$\overline{v_i^2} = 0.25 \cdot 10^{-18}\, v^2/Hz$$

$$\int_{1MHz}^{100MHz} 0.25 \cdot 10^{-18}\, v^2/Hz\, df = \left(0.25 \cdot 10^{-18}\right) \cdot \left(99 \cdot 10^6\right) v^2$$

$$= 0.2475 \cdot 10^{-10} v^2$$

$$= 4.98\mu v$$

Therefore, 4.98μv is a valid equivalent benchmark against which to judge circuit noise performance when measured using the INTNOISE function. To check the calibration of the INTNOISE function, a constant of 0.5nV was integrated over 1MHz-100MHz using INTNOISE. This produced a result of precisely 4.98μv. The result is consistant with the prediction, and so INTNOISE is assumed to be accurate. A more interesting benchmark is achieved by measuring the integrated noise in the Bipolar design. This is a more consistent estimator. The integrated simulated noise in the existing bipolar first stage unit is actually 12.9μv, or roughly $1.3nv/\sqrt{Hz}$. Therefore, a sufficiently quiet CMOS first stage will have the same noise performance.

4. Noise Models

A substantial part of the research in this study involved the quantification and measurement of circuit noise. Therefore, it was necessary to understand the basic noise models upon which SPICE circuit simulations are based. These will be explained here.

The noise models used in the hand calculations of this study include only thermal and flicker noise. Other noise sources are ignored as their contribution to the overall noise performance is minimal and their elimination from the noise equations greatly simplifies the math. Thermal noise is associated with resistive components and is modeled as a voltage source of value

Equation 1

$$\frac{\overline{v^2}}{\Delta f} = 4kTR$$

in series with an ideal resistor, where k is Boltzman's Constant, T is temperature, and R is the device resistance. The noise is expressed as a square because it represents the noise power. The literature suggests that flicker noise is generated by random carrier trapping that takes place at the Si/SiO_2 interface [7]. Flicker noise is defined as a current source of value

Equation 2

$$\frac{\overline{i^2}}{\Delta f} = K_1 \frac{I^a}{f^b}$$

in parallel with the element in question, where K_1 is a device constant, I is the direct current, f is the frequency, and a and b are constants.

These noise models are added to standard AC small signal models for bipolar and FET devices to produce device noise models. To simplify circuit analysis in subsequent chapters, all noise sources in a given transistor are referred back to the gate or base (the transistor input) and consolidated. The following figures show the resulting AC noise models for both FET and bipolar devices that will be used for noise analysis later on.

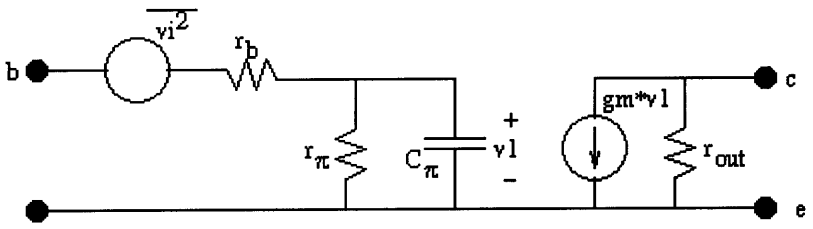


Figure 3: Bipolar small signal noise model

Figure 3 shows the bipolar small signal noise model. For a bipolar device, $\overline{v_i^2} = 4kT\left(r_b + \frac{1}{2gm}\right)$. Figure 4 below shows the FET small signal noise model.

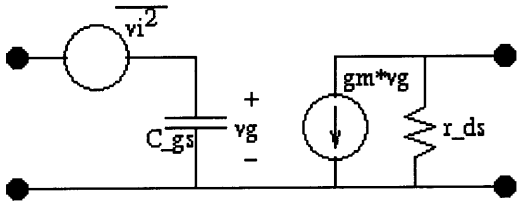


Figure 4: FET small signal noise model

In the case of the FET noise model, the input referred voltage noise can be broken down into the sum of thermal noise and flicker noise. The most accurate expression for thermal noise is disputed. The most popular expression, $\overline{v_{n,thermal}^2} = \frac{8}{3}\frac{kT\Delta f}{gm}$, has been found to be inaccurate, especially in the triode region and when $V_{ds} = 0$. A more accurate thermal noise model is $\overline{v_{n,thermal}^2} = \frac{\gamma 4kTg_{do}\Delta f}{gm^2}$, where $\gamma = \frac{1-\eta+\frac{1}{3}\eta^2}{1-\frac{1}{2}\eta}$, and $\eta = \frac{V_{ds}}{V_{gs}-V_t}$ [7]. g_{do} is the expression for channel conductance at zero drain to source voltage. As the transistor approaches saturation, $\gamma \to \frac{2}{3}$, and thus the thermal noise expression reduces to

$\overline{v_{n,thermal}^2} = \frac{8}{3}\frac{kTg_{do}\Delta f}{gm^2}$. This equation is valid as long as short channel effects do not affect the FET. FET flicker noise is given by $v_{n,flicker}^2 = \frac{K_f \Delta f}{WLC_{ox}^2 f}$ respectively.

5. Existing Bipolar Design

This section will explore the architecture of the existing Texas Instruments bipolar preamplifier. The preamplifier is a three stage structure, and only the first stage will be analyzed here. Multiplexing circuitry is also ignored here. The idea is to provide an analysis of the single head first stage bipolar circuitry so that it can be compared with the design of the single head first stage CMOS design. The analysis results of this first stage determine the design parameter goals for the CMOS design.

5.1. Schematic

Functionally, the bipolar first stage produces a differential output voltage that is proportional to $\frac{\Delta R_{mr}}{R_{mr}}$, where ΔRmr is the incremental change in MR impedance, and R_{mr} is the nominal DC MR impedance value. A circuit topology producing such a dependence protects the circuit output from drifting if the nominal head impedance should change over time with temperature or head wear. A simplified schematic of the existing stage one circuitry appears below in Figure 5:

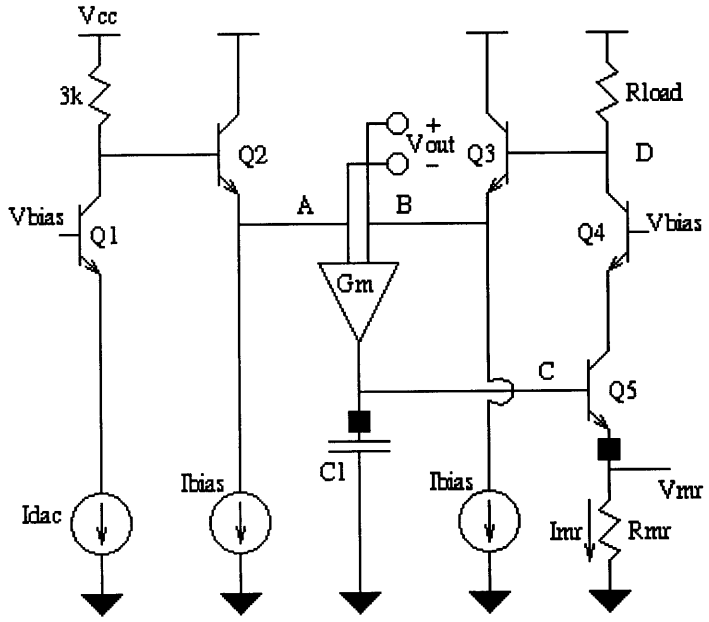


Figure 5 : Existing bipolar first stage preamplifer

5.2. Functionality of Schematic

5.2.1. DC Bias Points

As shown in Figure 5, the primary circuit structure of the existing Stage One preamplifier is a feedback loop that is used to bias transistor Q_5 such that the DC differential output voltage is zero volts. The feedback loop compares V_a to V_b. If they are not equal (ie $V_{out} \neq 0$), the transconductor G_m generates a current proportional to $V_b - V_a$ that either charges or discharges the capacitor C_1 (depending on whether or not $V_b > V_a$). As the voltage across C_1 changes, the voltage bias on R_{mr} changes accordingly (because Q_5 is an emitter follower) thus forcing V_b to change as well. This process continues until $V_b = V_a$, at which point G_m stops producing current, and the cycle is broken.

Once the DC bias points have been established, the circuit detects and amplifies small changes in the impedance of the MR head. Instead of discussing the circuit response to small changes in Rmr, it is more intuitive (and computationally simpler) to consider the equivalent stimulus of ΔV_{mr}, namely small deviations in the voltage across R_{mr}. This ΔV_{mr} signal is amplified by the resistor tree by a gain of $-150/R_{mr}$ to produce the signal V_b at node B. Since the output signal is $V_b - V_a$, the Stage One output is simply the differential signal $V_{out} = (150/R_{mr}) \cdot \Delta V_{mr}$.

It is important to note that since ΔV_{mr} is an AC signal, the AC current it will force the G_m stage to produce will short circuit through C_1 to ground, hence not disturbing the DC bias point on the base of transistor Q_5.

This circuit topology has several key strengths that make it suitable for its application as a preamplifier. One such strength is the ability of the feedback loop to compensate for drift in the nominal DC R_{mr} impedance of the MR head. Should R_{mr} drift over time with either temperature or head wear, the feedback loop automatically adjusts the bias points so that the DC differential output voltage returns to zero. Furthermore, since the output

voltage is proportional to ΔR_{mr} and inversely proportional to R_{mr}, the circuit output tends to reject R_{mr} drift. This is possible because when R_{mr} drifts, ΔR_{mr} will tend to drift as well, and so the ratio of $\Delta R_{mr}/R_{mr}$ will remain close to constant.

5.3. Bandwidth

The existing Stage One preamplifier has a bandpass frequency characteristic. The low frequency pole is produced primarily by the transconductor G_m and the capacitor C_1. Consider the following simplified block diagram of the feedback loop shown below in Figure 6:

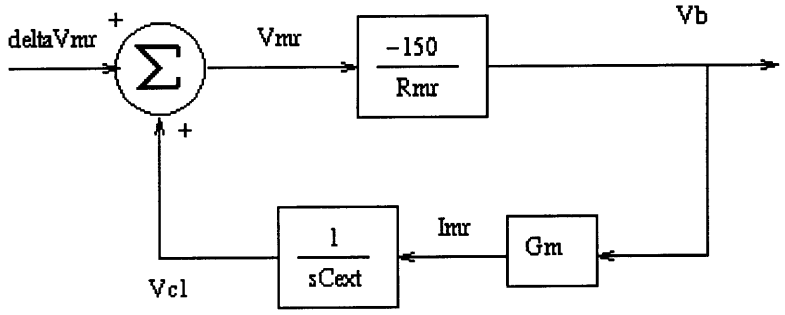


Figure 6: Feedback loop block diagram

From Figure 6, it is evident that:

$$\frac{V_b}{\Delta V_{mr}}(s) = \frac{-150/R_{mr}}{1+\frac{150g_m}{sR_{mr}C_{ext}}} = \frac{150s/R_{mr}}{s+\frac{150g_m}{R_{mr}C_{ext}}}$$

The equation dictates a system zero at $s=0$ and a left half plane (BIBO stable) pole at $\omega = \frac{-150g_m}{R_{mr}C_{ext}}$. To verify this prediction, a SPICE model simulation of the preamplifier

was executed, varying the parameter C_1. Comparisons of the predicted pole locations versus the actual locations are shown below in Table 1 based on the parameters $R_{mr} = 30\Omega$ and $G_m = 5.6\times10^{-3}\Omega^{-1}$:

C_1	f_{3db}(predicted)	f_{3dB}(simulated)	Error
5nF	807 kHz	792 kHz	1.9%
10nF	404 kHz	390 kHz	3.5%
20nF	202 kHz	197 kHz	2.4%
50nF	80.7 kHz	78.0 kHz	3.5%
100nF	40.4 kHz	39.4 kHz	2.4%

Table 1

The calculated breakpoints take into account the emitter resistance of Q_5 in series with Rmr. This parasitic resistance is calculated as:

$$R_{e,Q_5} = \frac{1}{g_{m,Q_5}}$$

where

$$g_{m,Q_5} = \frac{I_{c,Q_5}}{v_{th}}$$

refers to the tranconductance of transistor Q_5. The error between the actual breakpoints (from the simulation) and the predicted breakpoints (from the hand calculations) is most likely due to transistor parasitics not taken into account in the hand calculations.

The location of the high frequency pole is due primarily to an impedance divider at node D between the 150Ω resistor R_{load} and the collector to substrate capacitance of Q_4, shown below in Figure 7:

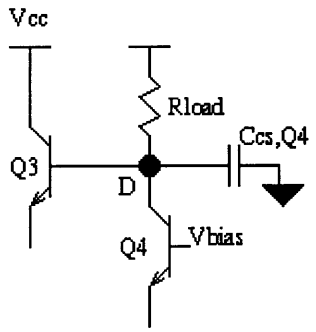


Figure 7: Source of high frequency node

The capacitor shown in Figure 7 is actually a sum of two parallel capacitances:

$$C_{cs,Q4} = C_{cs,\text{intrinsic}} + C_{cs,\text{sim}}$$

$C_{cs,intrinsic}$ refers to the intrinsic collector to substrate capacitance of transistor Q_4, while $C_{cs,sim}$ is a dummy capacitor added to the computer model solely for the purpose of being able to vary C_{cs} in order to verify pole location predictions.

In order to determine the high frequency pole location, Figure 7 is redrawn for an AC analysis. Because all DC sources are AC grounds, Vcc goes to ground, and Figure 7 reduces to:

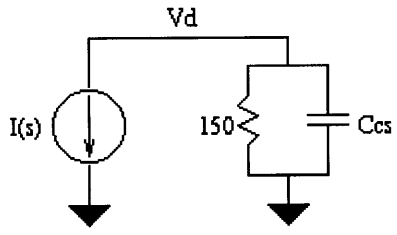


Figure 8 : AC model of the high frequency node

From Figure 8, the voltage at node D is clearly:

$$V_d = I(s) \cdot (150\Omega \parallel 1/sC_{cs})$$
$$= \left(\frac{1/C_{cs}}{s + 1/150C_{cs}} \right) \cdot I(s)$$

The current source, I(s), is generated by the AC input voltage, ΔVmr, divided by the resistance of the MR head, Rmr:

$$I(s) = \frac{\Delta V_{mr}}{R_{mr}}$$

Substituting for I(s), it is evident that the predicted pole location is at $\omega = \frac{-1}{(R_2 = 150\Omega) \cdot C_{cs,Q4}}$. This prediction was verified with SPICE simulations that varied $C_{cs,sim}$. The first simulation was performed with $C_{cs,sim} = 0$ in order to empirically determine the $C_{cs,intrinsic}$ value of Q_4. The remaining simulations verify the high frequency pole locations. Table 2 summarizes the results of this simulation:

$C_{cs,sim}$	f_{3dB} (predicted)	f_{3dB} (simulated)	Error
0pF	$1/(2\pi \cdot 150 \cdot C_{cs,intrinsic})$	2.11 GHz	
1pF	707 MHz	790 MHz	-10.5%
5pF	193 MHz	201 MHz	-4.0%
10pF	101 MHz	105 MHz	-3.8%
20pF	51.8 MHz	53 MHz	-2.3%
50pF	21.0 MHz	21.5 MHz	-2.3%

Table 2

$C_{cs,intrinsic}$ is therefore estimated to be 0.5pF.

Figure 9 shows the overall transfer characteristic of the circuit. It is worth noting that at low frequencies, the frequency response increases at +20 dB/decade, verifying the claim of a zero at $\omega = 0$ and a low frequency pole at

$$f_{3dB} = \frac{(R_2 = 150\Omega) \cdot (gm = 5.6 \cdot 10^{-3}\Omega^{-1})}{2\pi \cdot (Rmr \approx 30\Omega) \cdot (C_{ext} = 22nF)} = 180kHz\,.$$

The high frequency rolloff is slightly steeper, which indicates the presence of some other high frequency pole, most likely due to parasitic capacitances within either Q_4 or Q_5.

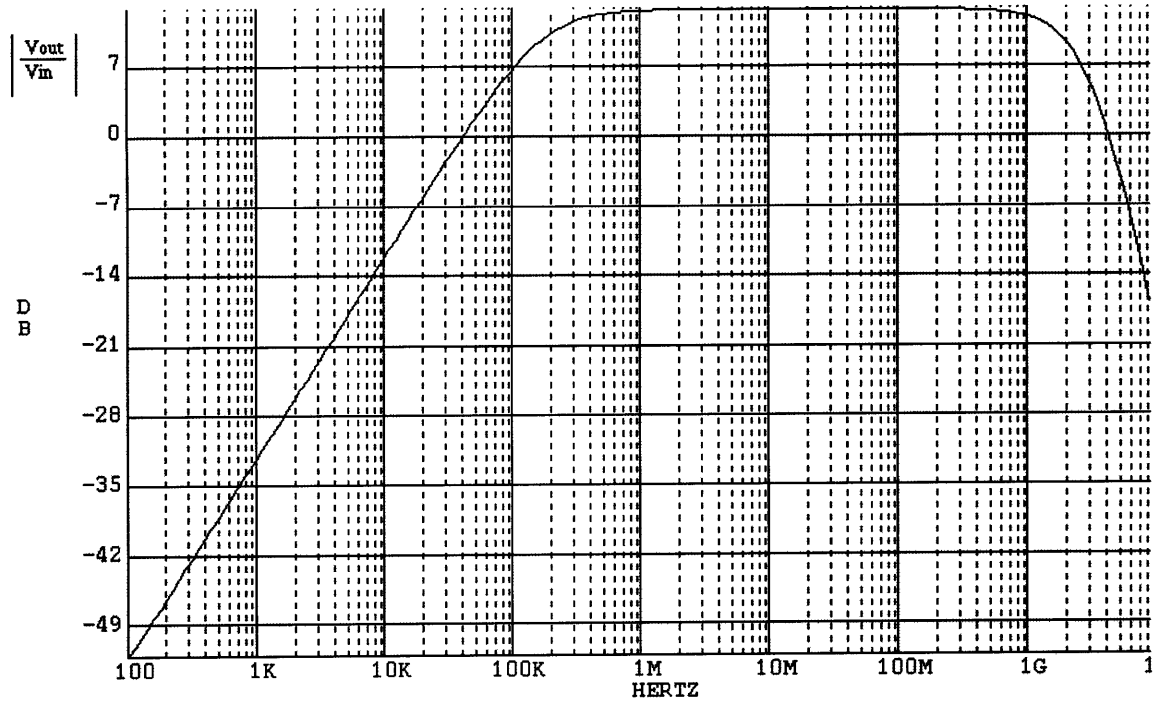


Figure 9: Bandpass characteristic of the bipolar preamplifier circuit

6. CMOS Design

This section will describe the block by block design of the CMOS MR preamplifier that was the goal of this research. As described in the Methods section, this task is most conveniently broken down in design of stage one, design of stages two and three, and design of the multiplexer architecture. The multiplexer architecture will be explained after the first stage predicted behavior has been derived. This is done to reflect the fact that the multiplexer architecture will debilitate performance regardless of the quality of the stage one design.

6.1. Stage One Design

The first stage of the bipolar TI design is responsible for biasing the MR head and detecting small variations in the resistivity of the head. These variations are converted into a voltage signal and then amplified by a small factor. Two different approaches were considered for solving this problem in CMOS. The first was a design based on an article by Klein and Robinson (K&R) that used a current mode solution. The second approach was to use the TI architecture by replacing the bipolar components with FETs. The K&R approach, while offering the promise of superior bandwidth was ultimately rejected, as it was too complex relative to the TI approach and much too slow. A brief review of the K&R design considered as a solution will be presented in the Appendix.

A block diagram for stage one is shown below in Figure 10. This design is based mostly on the TI bipolar circuit:

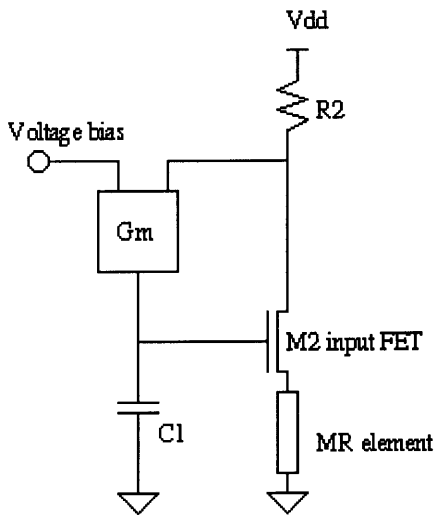


Figure 10: Stage one block diagram

Ideally, the voltage bias feeding into the left input of the transconductance (Gm) block will cause the feedback loop to keep increasing the drain current in M2 until the voltage *vout*− equals *vout*+. At that point, the Gm block stops producing current, and so the M2 gate stops increasing in voltage.

A simplified version of the stage one schematic is shown below in Figure 11. It is simplified in that the multiplexer circuitry is not included. A schematic symbol is used for Gm, and is expanded completely in Figure 12.

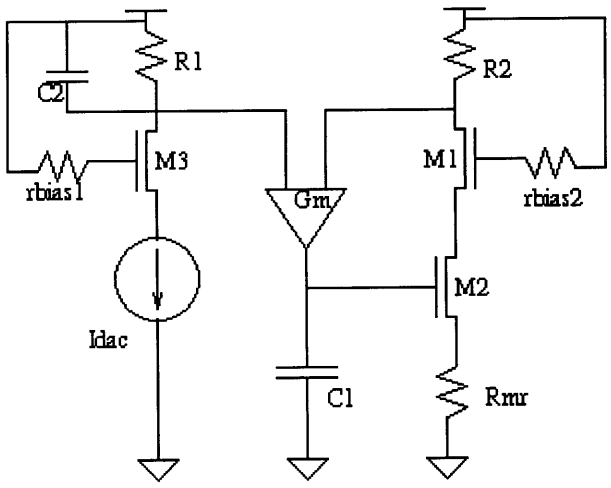


Figure 11: Simplified stage one schematic

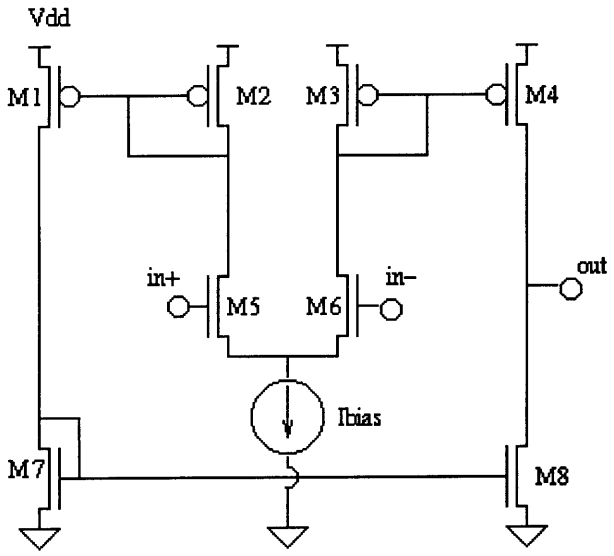


Figure 12: Voltage controlled current source transconductance amplifier

In Figure 11, the circuitry to the left of the Gm block, consisting of the DAC current, R_1, C_2, r_{bias1}, and M_3, are used to set the bias current of the main input cascoded tree on the right. The biasing circuitry produces a bias drain current in M2 of $I_{dac}\frac{R_1}{R_2}$. Furthermore, the DC bias of $vout+$ and $vout-$ is $V_{dd}-I_{dac}R_1$. The user is typically allowed to adjust this bias current by means of adjusting the I_{dac} current via several control bits. This mechanism was beyond the scope of this design. Thus, R_{mr} has been biased. As R_{mr} varies in time, the biasing current running through it remains constant, and so the voltage at N1 changes accordingly in time. This AC ΔV signal is amplified by a ratio of $\frac{R_2}{R_{mr}+\frac{1}{gm_2}}$ to node $vout-$. Taking the output as the differential signal $(vout+)-(vout-)$ subtracts out the DC bias level, $V_{dd}-I_{dac}R_1$. The capacitor C_1 sets up a GmC filter that shorts all high frequency signals to ground, allowing only low frequency components to set the bias by altering $V_{gate,M2}$. C_2 is used to remove all the high frequency noise generated by M_3 and R_1. Without it, the biasing branch becomes a significant noise contributor. Since the bias signal is not changing in time, a large C_2 will not affect the system gain or speed. The resistors r_{bias1} and r_{bias2} are resistors that serve to set the gate bias of M_1 and M_3 at V_{dd}. They are included to protect M_1 and M_3 in case of a power line

spike. In that event, each of those resistors in series with its associated FET capacitance will form an RC filter to low pass filter the power spike and protect the device. Finally, the cascode FET M_1 is included to increase the impedance of M_2, effectively helping reduce the short channel effect in M_2.

The voltage controlled current source Gm block is a standard differential input transconductor that works by mirroring current around from each of the inputs to the output node. The transconductance is set by the bias current and by the ratio $M_1 : M_2$.

6.2. Stage One Predicted Behavior – Transfer Characteristic

Equations can now be derived to predict the band pass behavior of the circuit. This is accomplished by separately analyzing the midband gain, the low frequency pole, and the high frequency pole.

6.2.1. Midband Gain

The midband AC gain is set by the ratio $\frac{R_2}{R_{mr} + \frac{1}{gm_2}}$. This can easily be seen through two simple equations:

Equation 3
$$i_{drain,M2,AC} = \frac{V_{N1}}{R_{mr} + \frac{1}{gm_2}}$$

Equation 4
$$i_{drain,M2,AC} = -\frac{vout-}{R_2}$$

Combining Equation 3 and Equation 4, it is found that

$$\frac{V_{N1}}{R_{mr} + \frac{1}{gm_2}} = -\frac{vout-}{R_2}$$

Equation 5
$$\therefore \frac{vout-}{V_{N1}} = -\frac{R_2}{R_{mr} + \frac{1}{gm_2}}$$

There is no DC gain, as the output, taken differentially, uses the bias circuit on the left of Figure 11 to subtract off the DC component. The M_2 FET degenerates the gain by adding a parasitic resistance in series with the MR head resistance.

6.2.2. Low Frequency Pole

The Gm stage and the capacitor C_1 define the low frequency pole, both of which are found in the feedback loop. The cascode branch, as well as the feedback loop can be modeled as a block diagram shown below in Figure 13.

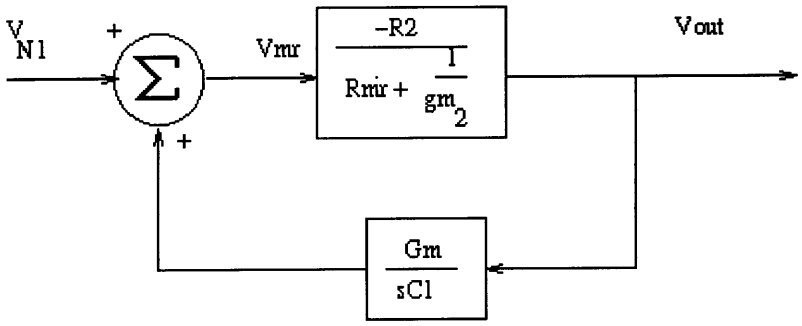


Figure 13 : Low frequency pole block diragram

The transfer function $\frac{v_o}{v_{N1}}$ is now easily calculated:

$$\left(v_{N1} + v_o \frac{Gm}{sC_1}\right)\cdot\left(\frac{-R_2}{R_{mr} + \frac{1}{gm_2}}\right) = v_o$$

$$-v_{N1}\frac{R_2}{\left(R_{mr} + \frac{1}{gm_2}\right)} = v_o\left(1 + \frac{GmR_2}{sC_1\left(R_{mr} + \frac{1}{gm_2}\right)}\right)$$

Equation 6

$$\frac{v_o}{v_{N1}} = -\frac{s\frac{R_2}{\left(R_{mr} + \frac{1}{gm_2}\right)}}{s + \frac{GmR_2}{C_1\left(R_{mr} + \frac{1}{gm_2}\right)}}$$

This predicts a zero at $s = 0$ and a pole at $s = -\frac{GmR_2}{C_1\left(R_{mr} + \frac{1}{gm_2}\right)}$.

Incidentally, at high frequencies, once the pole has sufficiently cancelled out the zero, the flatband gain is $\frac{R_2}{\left(R_{mr} + \frac{1}{gm_2}\right)}$, which is precisely the midband gain predicted in the previous section.

6.2.3. High Frequency Pole

The derivation of the high frequency pole is slightly more involved than that of the low frequency pole. It requires several simplifications and assumptions to make the math more tractable. The high frequency pole is defined primarily by the parasitic capacitances from M_1 and M_2. Consider the input cascode tree and its parasitic capacitances:

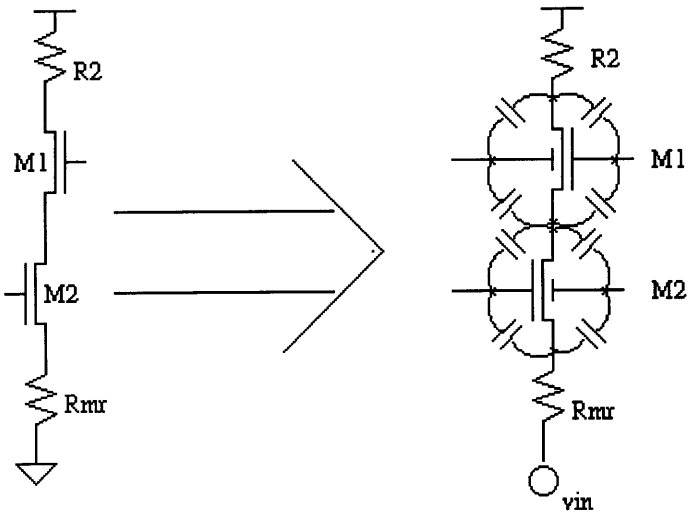


Figure 14 : Parasitic capacitances defining the high frequency pole

The system input can be modeled as an AC source feeding into a stationary R_{mr} (instead of a resistor R_{mr} varying in time) without loss of generality. This is reflected above in Figure 14.

An AC model based on the half circuit above is shown below in Figure 15. All of the parasitic capacitances are lumped into one of these capacitors. This is possible because both the gates and bulks of both the M_1 and M_2 FETs are at AC ground:

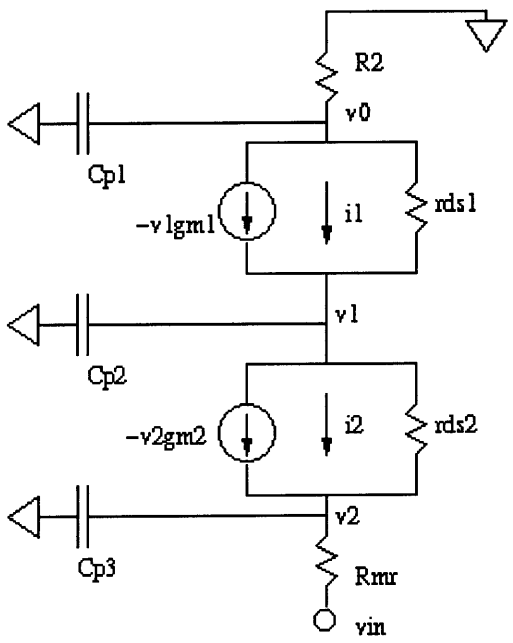


Figure 15: AC model for high frequency pole

where

$$C_{p1} = C_{dg1} + C_{db1}$$
$$C_{p2} = C_{sg1} + G_{sb1} + C_{dg2} + C_{db2}$$
$$C_{p3} = C_{sg2} + C_{sb2}$$

The high frequency pole location is found quite easily by solving the following system of equations:

$$\frac{-v_o}{R_2 \| C_{p1}} = -v_1 gm_1 \cdot (v_o - v_1) g_{ds1}$$

$$\frac{-v_o}{R_2 \| C_{p1}} = sv_1 C_{p2} - v_2 gm_2 + (v_1 - v_2) g_{ds2}$$

$$\frac{-v_o}{R_2 \| C_{p1}} - sv_1 C_{p2} = sv_2 C_{p3} + (v_2 - v_{in}) \frac{1}{R_{mr}}$$

To simplify the solution, it is assumed that $gm_1 >> g_{ds1}$ and $gm_2 >> g_{ds2}$. Solving, it is found that:

Equation 7

$$A_v = \frac{\left(\frac{gm_1 gm_2}{R_{mr} C_{p1} C_{p2} C_{p3}}\right)}{\left(s + \frac{gm_1}{C_{p2}}\right)\left(s + \frac{1}{C_{p3} R_{mr}} + \frac{gm_2}{C_{p3}}\right)\left(s + \frac{1}{R_2 C_{p1}}\right)}$$

The predicted pole locations are therefore

Equation 8

$$p_1 = \frac{-gm_1}{C_{p2}}, p_2 = \frac{-1}{C_{p3}}\left(\frac{1}{R_{mr}} + gm_2\right), p_3 = \frac{-1}{R_2 C_{p1}}$$

This equation makes sense intuitively. Primarily the parallel RC combination of R_2 and C_{p1} sets the –3dB point. C_{p2} and C_{p3} also contribute to the bandwidth, although to a lesser extent. SPICE simulations revealed that increasing R_2 linearly decreases the bandwidth linearly. Increasing the width of M_2 linearly produces a decrease in the bandwidth that is roughly cubic. Increasing W_2 from 1000μm to 5000μm produces a reduction in bandwidth of 70%.

Finally, note that from Equation 7, if s is small (i.e. well below the –3dB frequency), then

$$A_v = \frac{\left(\frac{gm_1 gm_2}{R_{mr} C_{p1} C_{p2} C_{p3}}\right)}{\left(\frac{gm_1}{C_{p2}}\right)\left(\frac{1}{C_{p3} R_{mr}} + \frac{gm_2}{C_{p3}}\right)\left(\frac{1}{R_2 C_{p1}}\right)}$$

$$= \frac{R_2}{R_{mr} + \frac{1}{gm_2}}$$

Thus, the predicted midband gain is the same as that predicted in the two previous sections. This is a good sanity check.

6.3. Stage One Predicted Behavior – Noise Performance

Simulated circuit noise can be predicted accurately using standard CMOS noise generator equations. In this chapter, the CMOS noise models in Section 4 will be used to derive expressions for noise that will be verified with SPICE simulations. Only thermal and

flicker noise sources will be considered, as they are the primary noise sources in FET devices.

6.3.1. Primary Noise Contributors

Most of the input referred noise in the circuit is produced within the component tree consisting of the gain resistor (R_2) the cascode FET, M1, the input FET (M_2), and the MR head (R_{mr}):

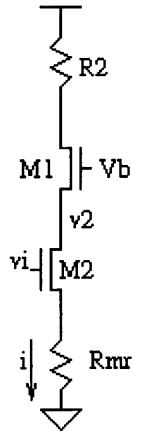


Figure 16: CMOS reader half-circuit

The noise produced by the MR head is independent of the quality of the circuit and will always be present. Hence, it is omitted in all subsequent calculations.

The AC equivalent model of the circuit in Figure 16 is shown below in Figure 17:

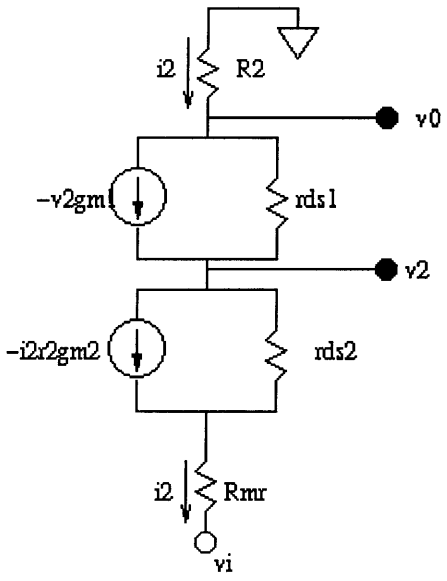


Figure 17: AC equivalent of reader half-circuit

The total noise current can be expressed as the sum of the noise currents in the resistor and each of the two FETs:

$$\overline{i_{on}^2} = \overline{i_{M1}^2} + \overline{i_{M2}^2} + \overline{i_{r2}^2}$$

And since $\overline{i_M^2} = gm^2 \overline{v_n^2}$,

Equation 9

$$\overline{i_{on}^2} = gm_{1eff}^2 \overline{v_{n1}^2} + gm_{2eff}^2 \overline{v_{n2}^2} + \overline{i_{r2}^2}$$

In order to evaluate this equation, expressions will be needed for gm_{1eff} and gm_{2eff}.

6.3.2. gm_{2eff}

To solve for gm_{2eff}, consider Figure 18:

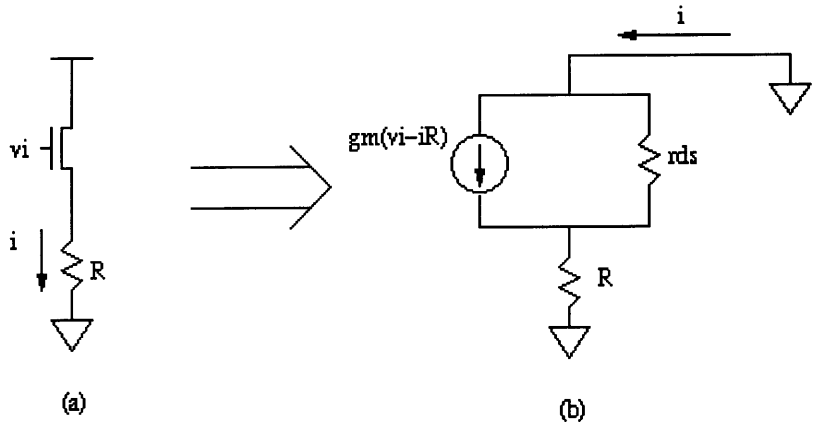


Figure 18 : AC Equivalent Circuit for Solving gm2_eff

Equating currents from Figure 18, it is quite easily seen that

$$i = -iRg_{ds} + gm(v_i - iR)$$

so

Equation 10

$$i[1 + Rg_{ds} + gmR] = gm \cdot v_i$$

Since $gm >> g_{ds}$, Equation 10 reduces to

Equation 11

$$gm_{2eff} = \frac{i}{v_i} = \frac{gm}{1 + gmR}$$

This is the phenomenon known as source/emitter degeneration.

6.3.3. gm_{1eff}

To compute gm_{1eff}, consider Figure 19:

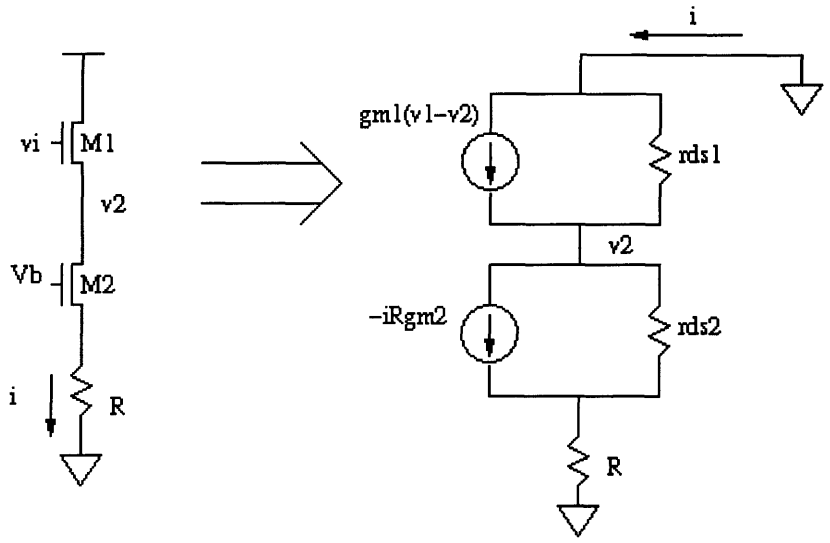


Figure 19: AC Equivalent Model for Computation of gm1_eff

In order to solve for gm_{1eff}, two equations for v_2 will be equated. The first is

$$i = -v_2 g_{ds1} + gm_1(v_i - v_2)$$

Solving for v_2 and assuming that $gm_1 >> g_{ds1}$, it is found that

Equation 12

$$v_2 = \frac{gm_1 v_i - i}{gm_1}$$

Using M2 for the second v_2 equation produces:

$$i = (v_2 - iR)g_{ds2} - iRgm_2$$

Using the same assumption as before about g_{ds2} results in

Equation 13

$$v_2 = ir_{ds2}(1 + Rgm_2)$$

Equating Equation 12 and Equation 13, and solving for gm_{1eff} produces:

Equation 14

$$gm_{1eff} = \frac{i}{v_i} = \frac{gm_1}{1 + gm_1 r_{ds2}(1 + Rgm_2)}$$

This result makes sense intuitively, as it represents a recursive application of the source/emitter degeneration demonstrated in Equation 11.

6.3.4. Thermal Noise

It is now possible to write equations predicting the majority of the thermal noise present in the circuit. The reason that only a majority of the noise is accounted for and not all of the noise in its entirety is that several noise contributing components in the feedback path have been completely ignored in the noise analysis. This is done because their noise contribution referred to the input, relative to the other noise contributors, is minimal. Furthermore, their omission greatly simplifies the noise equations.

Combining Equation 9, Equation 11, and Equation 14, as well as the fact that the input referred voltage thermal noise for a FET is $\overline{v_{n,thermal}^2} = \frac{8}{3}\frac{kTg_{do}\Delta f}{gm^2}$ (Section 4) it is shown that

$$\begin{aligned}\overline{i_{on}^2} &= gm_{1eff}^2\,\overline{v_{n1}^2} + gm_{2eff}^2\,\overline{v_{n2}^2} + \overline{i_R^2} \\ &= \left(\frac{gm_1}{1+gm_1 r_{ds2}(1+gm_2 r_{mr})}\right)^2\left(\frac{8}{3}\frac{kTg_{do,1}}{gm_1^2}\Delta f\right) + \left(\frac{gm_2}{1+r_{mr}gm_2}\right)^2\left(\frac{8}{3}\frac{kTg_{do,2}}{gm_2^2}\Delta f\right) + \frac{4kT}{r_2}\Delta f \\ &= 4kT\left[\frac{2}{3}\frac{g_{do,1}}{[1+gm_1 r_{ds2}(1+r_{mr}gm_2)]^2} + \frac{2}{3}\frac{g_{do,2}}{[1+r_{mr}gm_2]^2} + \frac{1}{r_2}\right]\Delta f\end{aligned}$$

and finally, since $\frac{\overline{v_{in}^2}}{\Delta f} = r_{mr}^2\frac{\overline{i_{on}^2}}{\Delta f}$,

Equation 15
$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kTr_{mr}^2\left[\frac{2}{3}\frac{g_{do,1}}{[1+gm_1 r_{ds2}(1+r_{mr}gm_2)]^2} + \frac{2}{3}\frac{g_{do,2}}{[1+r_{mr}gm_2]^2} + \frac{1}{r_2}\right]$$

6.3.5. Flicker Noise

Input referred flicker noise is calculated in much the same way as thermal noise. The input referred flicker noise for a given FET is

Equation 16
$$\frac{\overline{v_n^2}}{\Delta f} = \frac{K_f}{WLC_{ox}^2 f}$$

Note that there is no flicker noise present in resistors.

Substituting Equation 16 into Equation 9, it is found that

Equation 17

$$\frac{\overline{i_{on}^2}}{\Delta f} = \left(\frac{gm_1}{1+gm_1 r_{ds2}(1+gm_2 r_{mr})}\right)^2\left(\frac{KF_N}{2\mu C_{ox} W_1 L_1 f}\right)+\left(\frac{gm_2}{1+r_{mr} gm_2}\right)^2\left(\frac{KF_N}{2\mu C_{ox} W_2 L_2 f}\right)$$

Since $gm = \sqrt{2I_d \mu C_o \frac{W}{L}}$, Equation 17 becomes

$$\frac{\overline{i_{on}^2}}{\Delta f} = \frac{KF_N}{f}\left(\frac{I_d}{L_1^2(1+gm_1 r_{ds2}(1+gm_2 r_{mr}))^2}+\frac{I_d}{L_2^2(1+r_m gm_2)^2}\right)$$

and since $\frac{\overline{v_{in}^2}}{\Delta f} = r_{mr}^2 \frac{\overline{i_{on}^2}}{\Delta f}$,

Equation 18 $$\frac{\overline{v_{in}^2}}{\Delta f} = \frac{KF_N r_{mr}^2 I_d}{f}\left(\frac{1}{L_1^2(1+gm_1 r_{ds2}(1+gm_2 r_{mr}))^2}+\frac{1}{L_2^2(1+r_{mr} gm_2)^2}\right)$$

Equation 18 is used to calculate a flicker noise curve for a $\left(\frac{5000}{2}\right)$ FET (to predict flicker noise from the M_2 FET), as shown below:

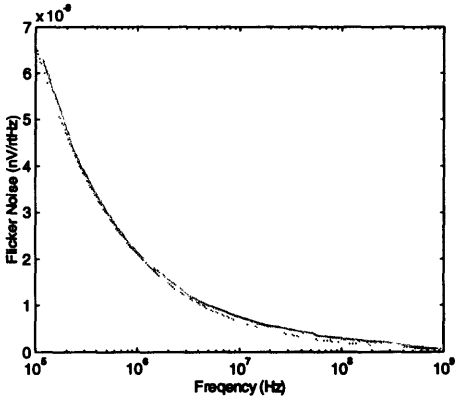


Figure 20: Predicted Input Referred Noise Curve

6.4. Verification of Noise Calculations

As will be shown in Section 7, the primary noise contributor to the circuit will be flicker noise from element M_2. In this section, it will be shown that the hand calculations for M_2 flicker noise agree with the TI SPICE models.

The term for M_2 flicker noise is derived from Section 6.3.3:

Equation 19

$$\frac{\overline{v_{n,M2\,flicker}^2}}{\Delta f} = \frac{K_f}{WLC_{ox}^2 f} \cdot \frac{1}{L_2^2(1+r_{mr}gm_2)^2}$$

Equation 19 shows that, to a first order approximation, M_2 flicker noise decreases as the inverse square of gm_2. By formula, gm_2 can be expressed as

Equation 20

$$gm_2 = \sqrt{2I_d\mu_n C_{ox}\frac{W_2}{L_2}}$$

Equation 19 and Equation 20 together show that (to a first order approximation) M_2 flicker noise is inversely proportional to $I_d\frac{W_2}{L_2}$. Thus, it is expected that if W_2 is increased by a factor of four, then gm_2 will be doubled. Furthermore, if gm_2 is doubled when $L_2 = 1\mu m$ and $r_{mr} = 30\Omega$, then $\frac{\overline{v_{v,M2\,flicker}^2}}{\Delta f}$ is reduced by a factor of $\frac{L_2^2(1+r_{mr}gm_{2old})^2}{L_2^2(1+r_{mr}gm_{2new})^2} = 0.47$ at every frequency, where $r_{mr} = 30\Omega$, $gm_{2old} = 28.3mS$ (for $M_2 = \frac{1000}{2}$), and $gm_{2new} = 2gm_{2old}$. To incorporate this finding into integrated noise savings (integrated noise being the noise standard used in this thesis), the following integration is performed:

$$noise_{old} = \int_{1MHz}^{100MHz} C\frac{1}{f}df = 2C$$

$$noise_{new} = \int_{1MHz}^{100MHz} 0.47C\frac{1}{f}df = 2C(0.47)$$

where C is a lumped constant of all the other coefficients in Equation 19. Therefore, the reduction in integrated noise is a factor of

$$\frac{noise_{new}}{noise_{old}} = \frac{2C\cdot 0.047}{2C} = 0.47$$

Thus, if W_2 is quadrupled, the hand calculations predict that the total integrated noise will be reduced by a factor of 0.47. To verify against the SPICE models, we will compare this prediction with the total integrated noise from Table 7 for $W_2 = 1000\mu m$ and $W_2 = 4000\mu m$:

$$\frac{noise_{W2=4000\,\mu m}}{noise_{W2=1000\,\mu m}} = \frac{29.5 \cdot 10^{-6}}{60.6 \cdot 10^{-6}} = 0.49$$

This verifies the accuracy of the noise equations with regard to M_2 flicker noise, which is the only truly relevant noise source in the circuit.

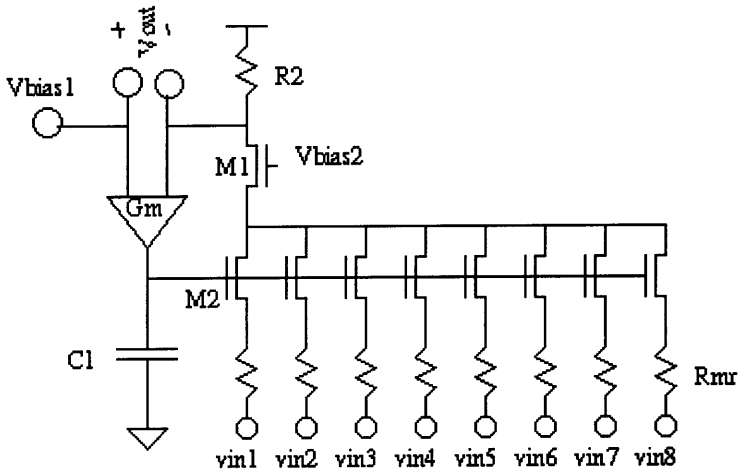
6.5. Multiplexer Design

The next phase after constructing an operational single head preamplifier reader was to design a mechanism to multiplex as many as eight MR heads together. This is done because a typical hard drive consists of several platters, each with its own read head. All of the read heads feed into one preamplifier which must then select the input line and amplify that signal only.

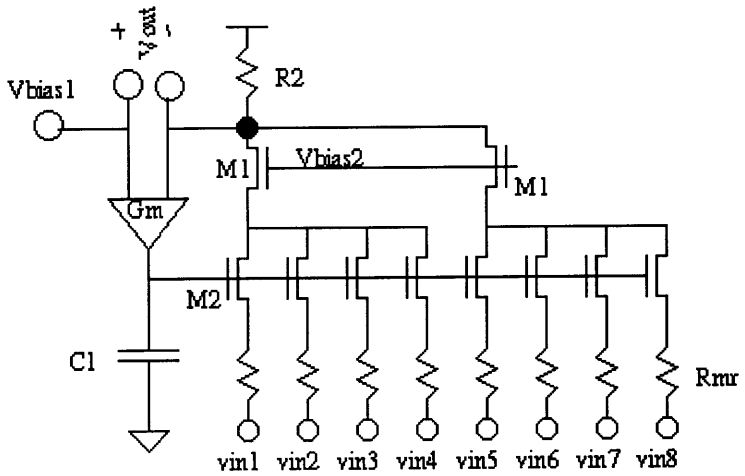
Because each MR head must feed into its own M_2 device (which are typically large in this application to reduce noise), multiplexing produces several design concerns. The first concern is space, as each of these large M_2 devices needs space on the layout. The second, more critical, concern is the reduced bandwidth encountered by introducing parallel arrays of large parasitic capacitances from the M_2 FETs. Thus, size and speed are the main design concerns. The size of the M_2 FETs will not be reduced (in order to maintain noise performance). Rather, different architectures of arranging and wiring these FETs to optimize speed will be considered.

6.5.1. Method

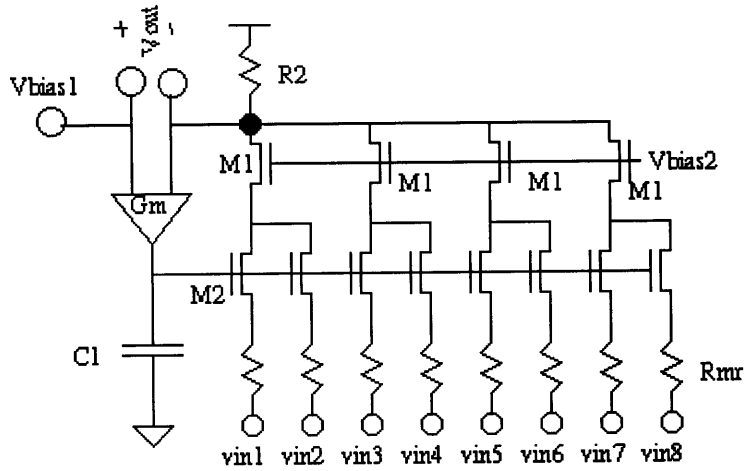
Several different architectures were tested to solve the multiplexer problem. These broadly fell into two categories: architectures with the feedback loop closing only around the first stage and architectures with the feedback loop including the second and/or third stages. Several ideas in the second category were tested, but were found in general to be inferior in bandwidth performance to the first category designs. Four multiplexer designs in the first category were eventually considered:



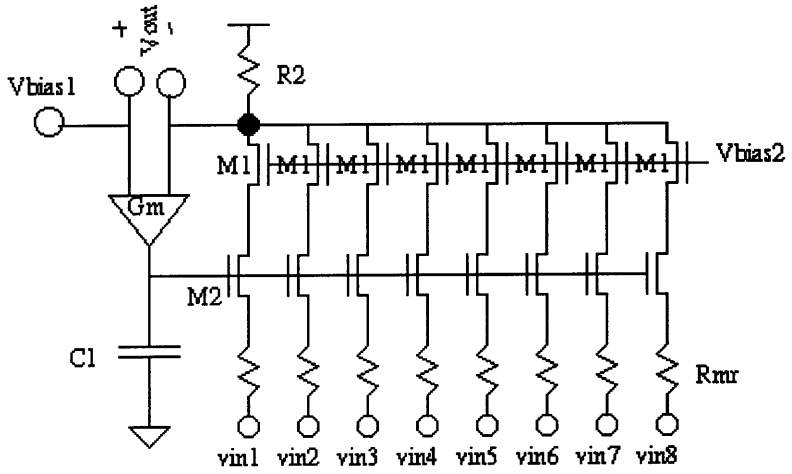
(a) 1x8 configuration



(b) 2x4 configuration



(c) 4x2 configuration



(d) 8x1 configuration

Figure 21: Multiplexer Architectures

Note that in each of these designs, the M_2 gates are separated by a switching pass FET circuit which electrically isolates the M_2 gates and allows the user to select any of the eight heads as active. This circuit is shown below in Figure 22:

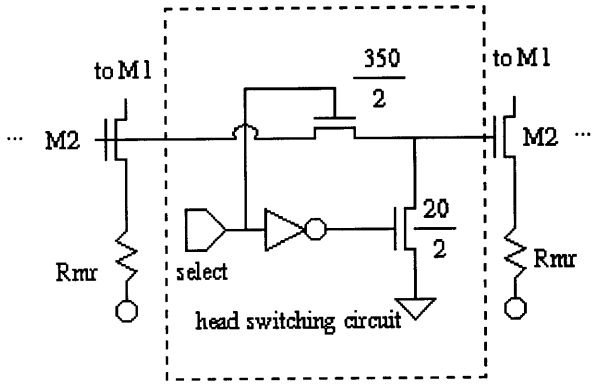


Figure 22: Head selector circuit

Each of the four circuits was simulated by selecting one of the heads as high and applying an AC signal at the v_{in} port. The bandwidth and gain were measured differentially at the output $(v_{out+} - v_{out-})$. The second and third stages were not included in the simulation.

6.5.2. Results

The results of these simulations are as follows:

Configuration	Midband Gain (dB)	3dB Point
1x8	11.9	24.4MHz
2x4	11.9	47.0MHz
4x2	11.8	83.5MHz
8x1	11.8	112MHz

Table 3

The results in Table 3 verify the concept that the more M_2 devices tied together at the drain, the greater the parasitic capacitance at that node. Therefore, since the 8x1 configuration has the eight heads tied together at the drain of the cascoded FET (and not at the M2 FET), it presents the smallest parasitic capacitance out of the four tested architectures.

6.5.3. Decoder

In order to implement this design, a digital decoder was designed that accepted as input three control bits and produced as output eight lines, all of which were low, except for the one specified by the three control bits. This was accomplished with a standard array of digital AND gates. This decoder was included to reduce the number of control bits from eight to three.

7. Optimization

7.1. Gain and Bandwidth Optimization

This section will discuss the optimization of the system component sizes to maximize gain and bandwidth. As mentioned in Section 6.2, the circuit will have a bandpass system characteristic. The first step in the optimization process is to ignore the low frequency pole. This pole is not crucial to the operation of the system. The only requirement is that the low frequency pole lies lower than the intended low frequency operating limit for the system, which is approximately 1MHz. As shown in Section 6.2.2, the low frequency pole is predicted at

$$f_{-3dB} = \frac{1}{2\pi}\frac{G_m R_2}{C_1 R_{mr}}$$

If, for the voltage controlled current source, the following device sizes are used, the value Gm is found to be 5.6mS, which is consistent with the ideal Gm (as used in the Bipolar design):

Gm Block Device	Size
$M_{1,4}$	$\frac{450}{2}$
$M_{2,3}$	$\frac{45}{2}$
$M_{5,6}$	$\frac{450}{2}$
$M_{7,8}$	$\frac{300}{2}$

Table 4

The low frequency pole is now at its predicted location of

$$f_{-3dB} = \frac{1}{2\pi}\frac{G_m R_2}{C_1 R_{mr}} = 203kHz$$

Since $f_{-3dB} << 1MHz$, the low frequency pole can be ignored.

The gain and the high frequency pole are intimately related. Increasing R_2 increases the gain, but also increases the RC time constant set by R_2 and the M_1 parasitic capacitance and thus lowers the bandwidth. The goal is to increase both gain and bandwidth (which tend to oppose one another). Bandwidth is desired to increase the operating speed while

gain is needed to reduce the input referred noise of the first stage. To increase bandwidth, the size of M_1 can be reduced thus reducing the M_1 parasitic capacitance. However, this will increase the voltage drop across M_1, which will lead to overhead concerns before the bandwidth is increased appreciably. On the other hand, R_2 could be decreased. This will cause the current bias through M_1 and M_2 to increase, again causing the V_{ds} for M_1 and M_2 to increase. This can be countered to some degree by decreasing the current bias, but the lower the current bias, the greater that noise performance is sacrificed. Thus, a comfortable balance must be struck in sizing all the devices in order to achieve the required bandwidth and gain.

The final device sizes were decided mostly by trial and error, using the above logic to guide the trial and error process. Table 1 below shows the final device sizes.

Device	Size
M1	300/2
M2	5000/2
R_2	150Ω
I_{dac}	0.4μA

Table 5

These component values produced a midband gain of 11.2dB and a high frequency pole of 200 MHz (measured without the multiplexing circuitry attached). This is close to what is predicted by the high frequency pole calculation of Section 6.2.3. Using similar device sizes, Equation 8 in Section 6.2.3 predicts a high frequency pole of 197MHz. Note also that adjusting the M_1 size doesn't dramatically affect the system noise, as shown in Section 7.1.

7.2. FET Noise Optimization

In this section, the circuit will be optimized to reduce the input referred noise. This task is somewhat tricky, as the TI SPICE models are simulated using the BSIM3 algorithm, which does not correlate highly to actual FET device physics. Instead, the models are based on more of a curve-fitting algorithm. Thus, it can be difficult to evaluate the noise equations from Section 6.3 on the actual TI process parameters. However, it is possible

to verify the noise equations of Section 6.3 qualitatively, and this will be demonstrated here.

To understand the breakdown of noise from each device, a series of SPICE simulations will be executed in which all devices except one will be forced noiseless. This is accomplished in SPICE by setting the NOISE flag for a particular device at NOISE=0. The first device to be examined will be M_1. The transfer function from the gate of M_1 to the system output is shown below in Figure 23a, determined using an AC SPICE simulation with the M_1 gate at the input and v_{out} as the output. The gate of M_1 is considered the input in this case because the input referred noise generated by a FET is referred back to the FET gate.

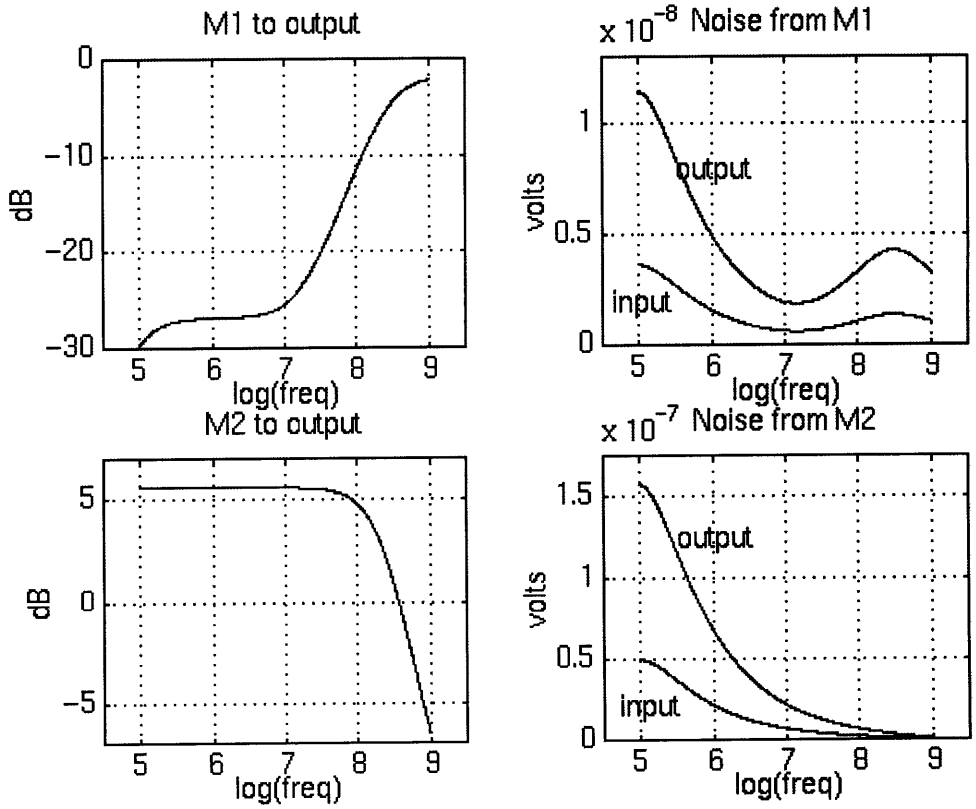


Figure 23 : Noise contributions from M_1 and M_2

(a – top left) Transfer function from M_1 gate to output, (b – top right) Input and output referred noise from M_1, (c – bottom left) Transfer function from M_2 gate to output, (d – bottom right) Input and output referred noise from M_2

Noise injected at the gate of M_1, consisting primarily of thermal and flicker noise, will appear at the output multiplied by the transfer function shown in Figure 23a, resulting in the output referred curve Figure 23b. Dividing this output referred noise by the system bandpass response produces the input referred noise due only to transistor M_1. This is also shown in Figure 23b.

Likewise, the transfer function from the gate of M_2 to the system can be found using an AC SPICE simulation, and is shown in Figure 23c. As with the M_1 noise discussed above, the contribution from the M_2 device is the input referred noise from M_2 multiplied by the transfer function in Figure 23c. This produces the output referred noise shown in Figure 23d. Dividing back by the system bandpass characteristic produces the noise due to M_2 referred to the system input. This is shown in Figure 23d.

Figure 23 verifies that, as expected, M_2 produces nearly an order of magnitude more noise than M_1, despite being an order of magnitude larger. Thus, efforts to reduce system noise should be concentrated primarily on M_2. The other feature worth realizing from Figure 23 is that at exceedingly high frequencies, the M_1 input referred noise is greater than the M_2 input referred noise because of the M_1 to output transfer function.

7.2.1. Method

Reduction of noise in the given architecture was based on a systematic variation of the system components. Three elements were considered: M_1, M_2, and R_2. For each of the three components, the other two components were kept at a constant size while the component in question was varied in size. The integrated input referred noise was measured in each case.

7.2.2. M_1 Noise

In the first stage of the noise optimization, M_2 was sized at $\frac{1500}{2}$ while R_2 was set at 150Ω. L_1 was also held constant at $2\mu m$. Table 6 shows the results of varying W_1 on M1 noise, M2 noise, and total $(M_1 + M_2)$ input referred noise:

W1 (μm)	G (dB)	M1 Noise (μv)	M2 Noise (μv)	Total Noise (μv)
75	8.88	15.5	48.3	51.1
85	9.71	10.3	47.3	48.7
100	10.0	8.4	46.8	47.9
120	10.1	7.22	46.6	47.4
150	10.2	6.2	46.4	47.1
175	10.2	5.6	46.3	46.9
200	10.3	5.2	46.3	46.8

Table 6

Figure 24, shown below, shows the total input referred noise integrated over $1MHz < f < 100MHz$ plotted against M1 width:

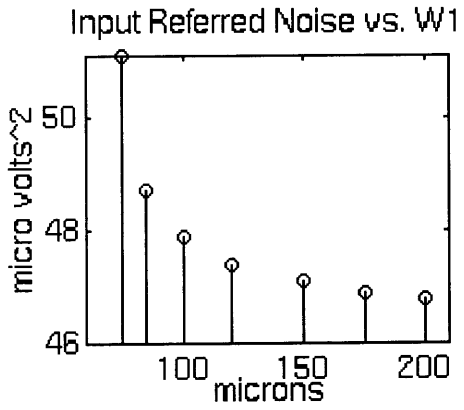


Figure 24 : Total Integrated Noise vs. M1 Width

Figure 25 shows the noise characteristics for different values of W_1:

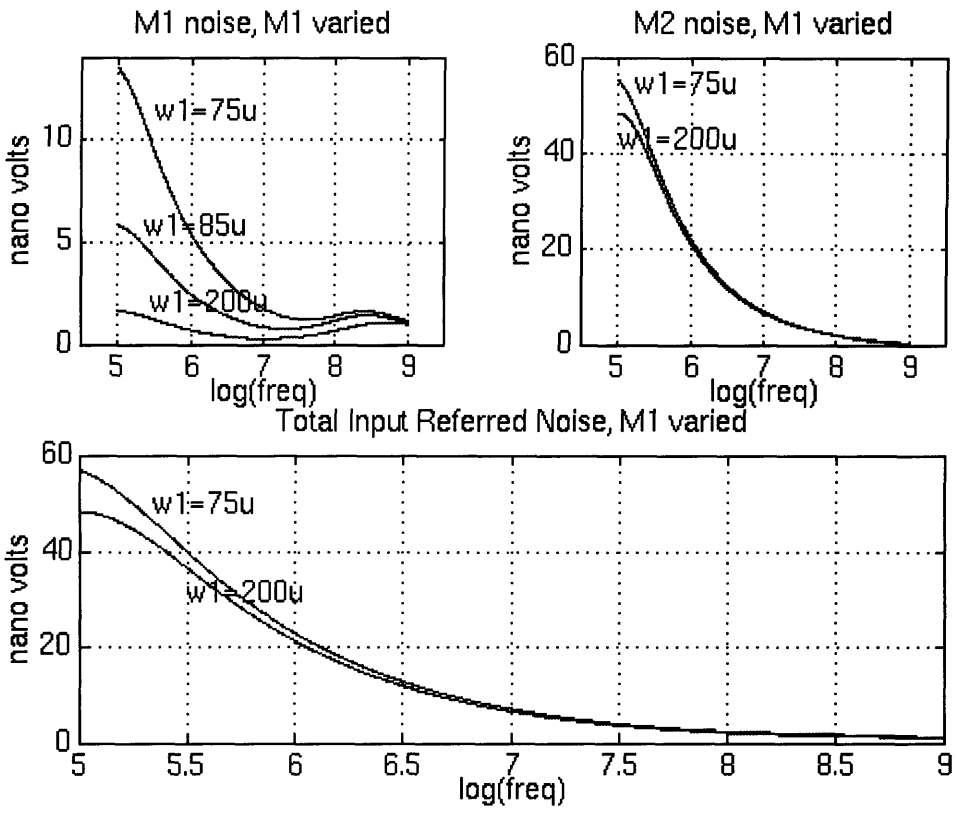


Figure 25: Noise Curves for Various Values of W1

(a – top left) Input referred noise due to M_1 for different widths of M_1, (b – top right) Input referred noise due to M_2 for different widths of M_1, (c – bottom) Total input referred noise for different widths of M_1

Figure 25a shows only M_1 noise at three different widths of M_1, while Figure 25b shows M_2 noise at two different M_1 widths. Figure 25c shows the total input referred noise for two values of M_1. This shows that while M_1 noise is greatly reduced by an increase in W_1, M_2 noise still dominates, and so the overall noise is not greatly improved by tinkering with M_1. Increasing W_1 from $75\mu m$ to $200\mu m$ produces a noise reduction of only 8.4%.

7.2.3. M_2 Noise

In the second phase of the noise optimization, M_2 was varied in width while M_1 was held constant at $\frac{100}{2}$ and $R_2 = 150\Omega$. L_2 is constant at $1\mu m$. Table 7 shows the effects of varying W_2 on M_1 noise, M_2 noise, and total integrated input referred noise.

W_1 (μm)	G (dB)	M1 Noise (μv)	M2 Noise (μv)	Total Noise (μv)
1000	9.16	9.1	59.7	60.6
2000	10.47	8.2	39.8	40.9
3000	11.01	8.2	32	3.33
4000	11.32	8.9	27.8	29.5
5000	11.52	9.7	25.2	27.3
6000	11.66	10.6	23.3	25.9
7000	11.77	11.4	22.0	25.1

Table 7

Figure 26 shows the total input referred noise from Table 7 plotted against W_2. It indicates that increasing W_2 past $7000\mu m$ will probably result in minimal noise savings relative to the extra incorporated area. Figure 27c (bottom) shows the entire noise characteristic versus frequency for 3 values of W_2. This reiterates the conclusion drawn by Figure 26 and Table 7, namely that increasing M_2 drastically reduces system noise. Therefore, by increasing W_2 from $1000\mu m$ to $7000\mu m$, the input referred noise is decreased by approximately 58.6%.

In Section 4, it is shown that for a constant length, both $\overline{v_{n,thermal}^2}$ and $\overline{v_{n,flicker}^2}$ decrease as the FET width increases. Therefore, one would expect input referred noise to decrease continuously as FET width increases. The limiting factor in this case is that as the M_2 width is increased, the –3dB bandwidth decreases (see Equation 8). This phenomenon is forced by the second of the three high frequency poles, $p_2 = \frac{-1}{C_{p3}}\left(\frac{1}{R_{mr}} + gm_2\right)$. The transconductance, gm_2, is proportional to $\sqrt{W_2}$ and thus increases with increasing W_2.

C_{p3}, however, is proportional to W_2, and thus $\frac{1}{C_{p3}}$ decreases with increasing W_2 faster than gm_2 increases with increasing W_2. The net effect is that the p_2 pole decreases with increasing W_2. As the bandwidth decreases, the higher frequencies of the noise curve will be divided back by successively larger gains, and thus the noise will cease to be reduced as W_2 increases. This accounts for the total noise values in Table 7.

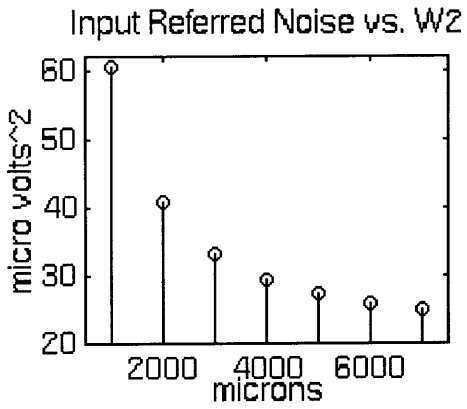


Figure 26 : Input Noise vs. W_2

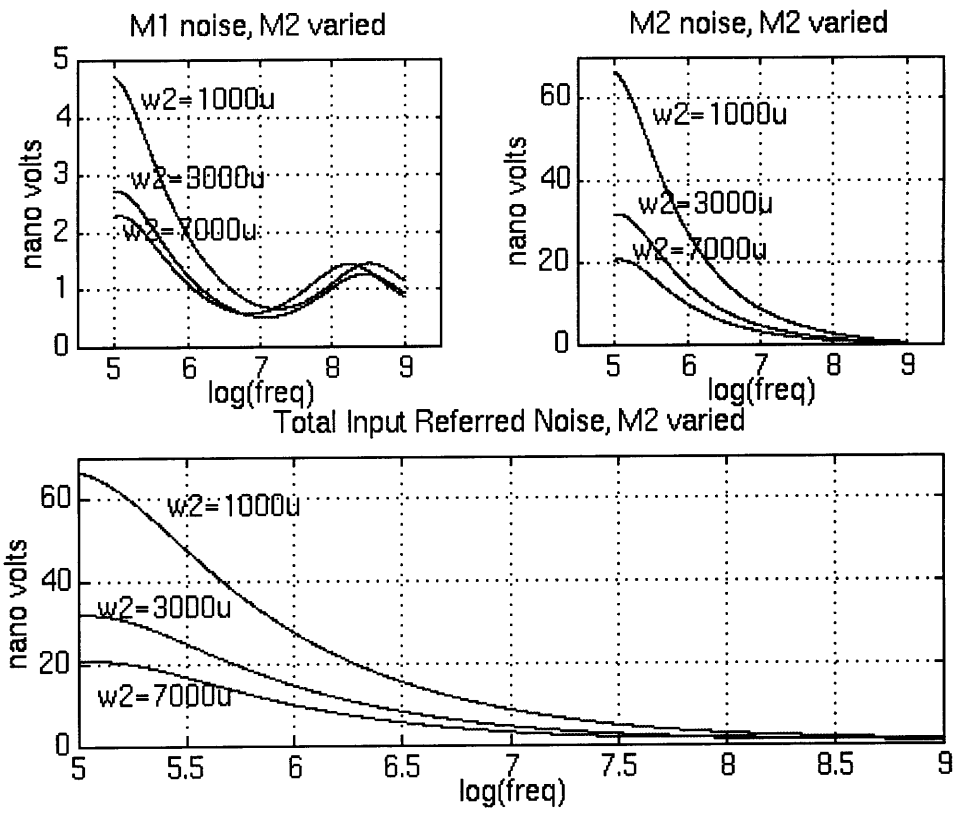


Figure 27 : Noise Curves for Various Values of W_2

(a – top left) Input referred noise due to M_1 for different widths of M_2, (b – top right) Input referred noise due to M_2 for different widths of M_2, (c – bottom) Total input referred noise for different widths of M_2

Clearly the size of M_2 is crucial to the noise performance of the circuit. To determine the ideal size, as well as the effect of drain current density on the noise performance, a large number of M_2 widths and lengths were simulated and the noise response measured. Figure 28 shows the results:

$$\frac{R_2}{R_{mr} + \frac{1}{gm_2}}$$

Figure 28: Noise vs. M_2 Width

Figure 28 verifies the earlier assertion that, in general, as $\left(\frac{W}{L}\right)_2$ increases, integrated noise decreases. Furthermore, Figure 28 clearly shows a marked improvement in noise performance between $L_2 = 1\mu m$ and $L_2 = 2\mu m$ but not between $L_2 = 2\mu m$ and $L_2 = 3\mu m$. From the $L_2 = 2\mu m$ curve, a local minimum is evident at about $W_2 = 5000\mu m$. Therefore, it is shown empirically that, according to the TI SPICE models, the optimum size for M_2 is $\frac{5000}{2}$.

As mentioned before, the conclusions from Figure 28 are somewhat counterintuitive, as the noise models from Section 4 predict noise to decrease as width is increased over a constant length. However, as the width W_2 is increased, the high frequency bandwidth decreases, thus lowering the gain at high frequencies and boosting the input referred noise. Figure 28 suggests that this phenomenon is worse for greater values of L_2. Equation 8 predicts a pole at $s = \frac{-1}{C_{p3}}\left(\frac{1}{R_{mr}} + gm_2\right)$. Remembering that

$gm_2 = k'(\frac{W}{L})_2(V_{gs} - V_T)$, it is clear that as L_2 increases, gm_2 decreases, thus lowering the pole. As the pole is lowered, its effects on the bandwidth become more noticeable, and thus the input referred noise should get worse at greater frequencies.

Another interesting result is to compare four different noise simulations with equal $\left(\frac{W}{L}\right)_2$ ratios but with different values of L_2, as shown below in Table 8:

$\left(\frac{W}{L}\right)_2$	**Total Integrated Noise** (μv)
1500/1	47.3
3000/2	24.9
4500/3	20.5
6000/4	20.3

Table 8

Table 8 verifies that as L_2 increases, noise decreases despite the fact that the W/L ratio stays the same. As L_2 is increased, the current density is decreasing, and so the noise decreases accordingly. Furthermore, flicker noise, which is inversely proportional to the product $W \cdot L$, is decreasing as L_2 increases.

7.2.4. R_2 Noise

The final phase of the noise optimization was to vary R_2 while holding M_1 and M_2 constant at $\frac{100}{2}$ and $\frac{1500}{2}$ respectively. The results are shown below in Table 9.

R_2 (Ω)	G (dB)	M_1 Noise (μv)	M_2 Noise (μv)	Total Noise (μv)
125	8.0	11.5	48.4	50.1
150	10.0	8.4	46.8	47.9
175	11.2	8.0	46.2	47.2
200	12.3	7.8	46.0	46.8
225	13.2	7.7	45.7	46.6
250	13.9	7.7	45.7	46.5
275	14.6	7.7	45.7	46.5

Table 9

Table 9 shows a 7.2% reduction in input referred noise as r_1 is increased from 125Ω to 275Ω. Clearly, R_2 is not a dominant factor in the determination of input referred noise. Figure 29 shows the noise curves for different values of R_2, and thus reiterates this point.

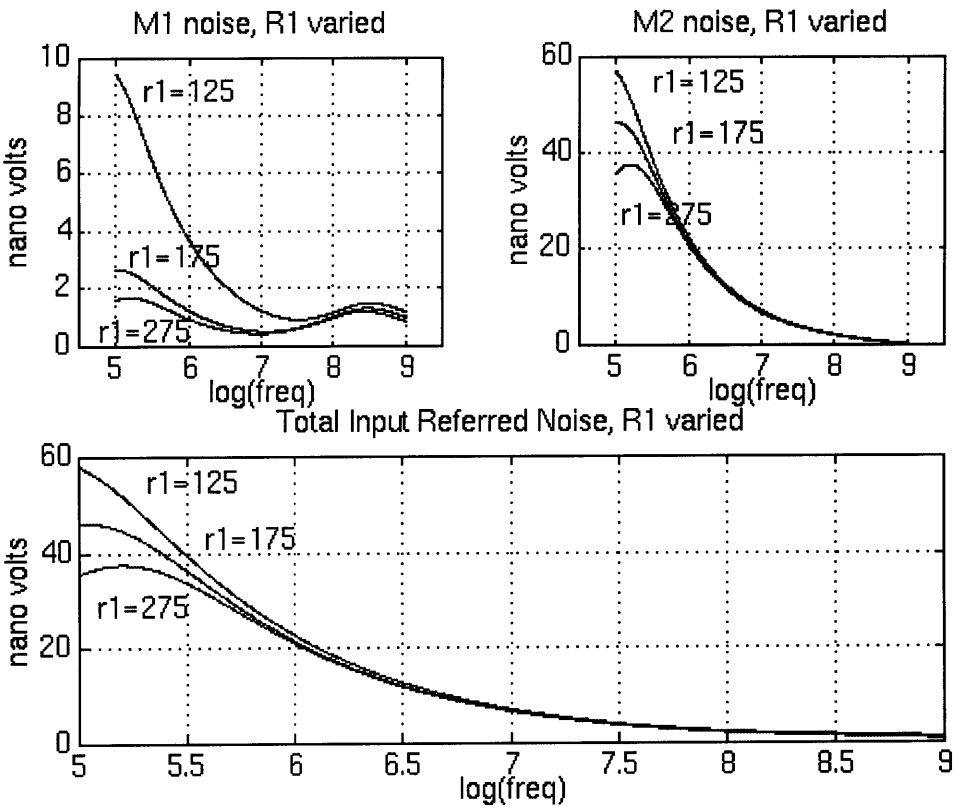


Figure 29 : Input Referred Noise for Various Values of R_2

(a – top left) Input referred noise due to M_1 for different values of R_1, (b – top right) Input referred noise due to M_2 for different values of R_1, (c – bottom) Total input referred noise for different values of R_1

7.2.5. Noise Optimization Conclusion

Figure 25, Figure 27, and Figure 29 collectively demonstrate that the majority of the noise produced is flicker noise from device M_2. Thermal noise is a constant over all frequencies, and tends to appear much smaller than the system flicker noise, which decreases inversely proportionally to frequency.

8. Comparisons and Conclusions

The CMOS preamplifier was successfully designed and simulated at Texas Instruments, although not all of the desired performance parameters were met. This section will discuss some of the shortcomings of the designs and suggest efforts for future design.

At the conclusion of the semester spent working with Texas Instruments, the preamplifier had been designed in three stages. The second and third stages were both very basic differential amplifiers and would need to be overhauled dramatically in an actual IC design. They were included in this test just to get an idea of their contribution to noise and bandwidth specifications. All comparisons below are made between the single head bipolar first stage amplifier and the single head CMOS first stage amplifier, unless otherwise mentioned specifically.

The final simulated system parameters that were achieved (measured without the multiplexer circuitry) are as follows:

Parameter	Value
Gain	11.2dB
Low Frequency Pole	102kHz
High Frequency Pole	200MHz
Noise	$22.0\mu v$

The gain, 11.2dB corresponds to a gain factor of 3.6. Here, the first drawback of CMOS technology is seen. Because the CMOS transconductance tends to be smaller than the bipolar transconductance, the gain will be smaller in a CMOS circuit for the same values of R_2 and R_{mr}. The relatively small CMOS transconductance was also a problem for source followers as buffers between stages. For example, a source follower with a bias current as high as 2mA and input N-FETs sized at $\left(\frac{60}{2}\right)$ passes only 80% of its input signal (-2dB). This is troublesome for two reasons. The first is that if a source follower is placed between every two stages as a buffer, there will be a 2dB loss between each stage, which will needlessly attenuate the gain. The second problem is that with the gain

reduced from stage to stage, the input referred noise becomes larger (dividing back by a smaller gain). Another way to visualize this is to consider that with a loss of gain between each stage, the noise from that particular stage becomes more relevant relative to the signal.

The CMOS low frequency pole, measured at 102kHz, is well within the target boundary set by the bipolar circuit (176kHz). However, the improved bandwidth is unused, as the normal operating frequencies of the MR reader are $1MHz < f < 100MHz$. Designing for this pole, as mentioned before, is relatively simple, as it can be defined primarily by the Gm value of the voltage controlled current source, which affects the functionality of no other part of the circuit.

The CMOS high frequency pole of 200MHz is slightly below the target value of 300MHz. This shortcoming, while bothersome, is not the undoing of the CMOS design. The bandwidth can be increased slightly, but at the cost of other factors, most notably noise and power dissipation. This can be fixed by process technology improvements over time that reduce the drain to gate and drain to bulk capacitances and increase g_m.

Switching circuitry was also developed to multiplex between eight heads. The circuitry was optimized to minimize the reduction in overall system bandwidth. The best multiplexer design reduced the CMOS bandwidth from 200MHz to 112MHz. This measurement is not part of the original scope of the thesis, but was included in the design primarily because it will be useful for the TI design staff in the future. There is no bipolar multiplexer data against which to compare the bandwidth reduction figure.

The noise performance of the designed CMOS circuit was well above the target value. The simulated integrated noise was $22\mu v$, compared with the target value of $12.9\mu v$. This target value was simulated using a single head first stage bipolar amplifier in the same process technology. Thus, the noise percent error was about 71%. Figure 28 leads one to believe that the achieved noise is bordering on a hard limit on noise performance for the given architecture in the given process. This noise level is probably too high to be

competitive on the preamplifier market. This value may be improved by improvements in the process technology (such as reduction of t_{ox}), or by implementing a different architecture. The system noise is dominated almost entirely by flicker noise from device M_2.

Finally, a different architecture was explored to solve the preamplifier problem. The architecture, based on the current mode amplification scheme proposed by Klein and Robinson, was found to be unusable for the purposes of a TI MR head hard disk drive preamplifier, despite the statement in their paper that their tape head design could easily be extrapolated to hard disk drives. The major drawback of this design was a current mode amplifier design that was simply too slow. Despite repeated efforts to improve the bandwidth by employing various design tricks, the –3dB point did not exceed 189MHz (with a gain of 8.4dB).

In order for the CMOS first stage amplifier to become commercially viable for Texas Instruments, one of several improvements must be implemented. One idea is to improve the quality of the BiCMOS process used to fabricate the amplifier, specifically with respect to drain to gate and drain to bulk capacitances. This will speed up the large M_2 FET, thus allowing for a higher gain-bandwidth product. However, since changes in process technologies tend to progress slowly, and market demand for a fast CMOS preamplifier is immediate, a more radical change should be implemented. It is unlikely that drastic improvements in performance can be achieved with the current design as summarized in this thesis. The best solution is to find another architecture or make a significant change to the current architecture. It is possible that a variation on the type of current mode amplifier discussed by Klein and Robinson (see Appendix) will achieve this.

In summary, the design of the CMOS MR preamplifier was successful from a functional standpoint, although it was not built to within the required noise and speed parameters. It is believed that with further advances in process technology, or perhaps with some architectural changes, that the circuit may become viable commercially.

9. Appendix – Klein and Robinson Architecture Design

As part of the research in this project, I explored an alternate method of biasing the MR head and detecting read signals off of it. The design strategy was taken from an IEEE paper written by Hans Klein and Moises Robinson. They proposed a current mode structure that was actually designed for tape drives, which tend to operate at drastically lower speeds than hard drives. Their architecture had several purported advantages, but unfortunately the speed of their setups was insufficient for TI's hard drive purposes.

A block diagram of the design is shown below in Figure 30:

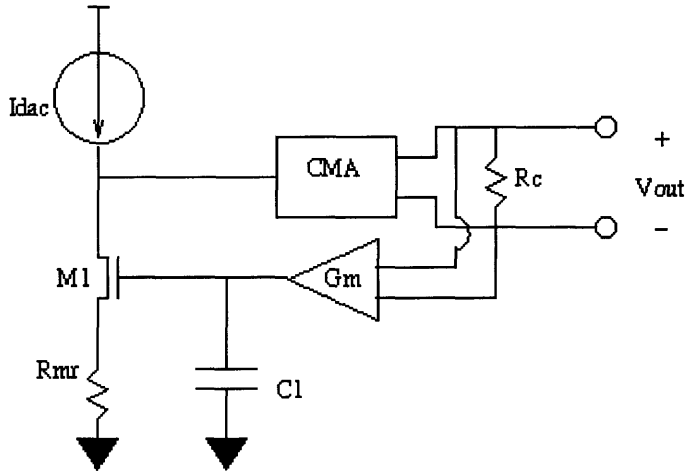


Figure 30: Klein and Robinson architecture block diagram

The ideal functionality of this block diagram is to bias the MR head with a user adjustable current, I_{dac}. This sets up a DC bias voltage at N_1 of $I_{dac} \cdot R_{MR}$. Then, as R_{MR} changes in time, an AC current equal to $i = \frac{I_{dac} \cdot R_{MR}}{\Delta R_{MR}}$ is generated and forced into the current mode amplifier (CMA). The CMA functionality is two-fold. First, it gains the current i by a small constant gain factor, K. Secondly, it converts the single ended current at the input into a differential output signal. The differential current is forced across the resistor R_c, and the differential voltage output is formed. The remainder of the circuit is a feedback loop that adjusts the gate of M_1 to pass the appropriate I_{dac} current.

The system in Figure 30 has a bandpass response. The midband gain, easily seen to be $\frac{KR_C}{R_{MR} + gm_1^{-1}}$, is negatively affected by low CMOS transconductance (as with the actual CMOS design showed in Section 6). The low frequency pole, as in the CMOS design of Section 6, is determined by the operational transconductance amplifier's transconductance (Gm from Figure 30) and the feedback capacitor, C_1. More importantly, the current mode amplifier determines the high frequency pole. Its low input impedance will, in theory, force the high frequency pole up higher.

The CMA proposed by Klein and Robinson is as follows:

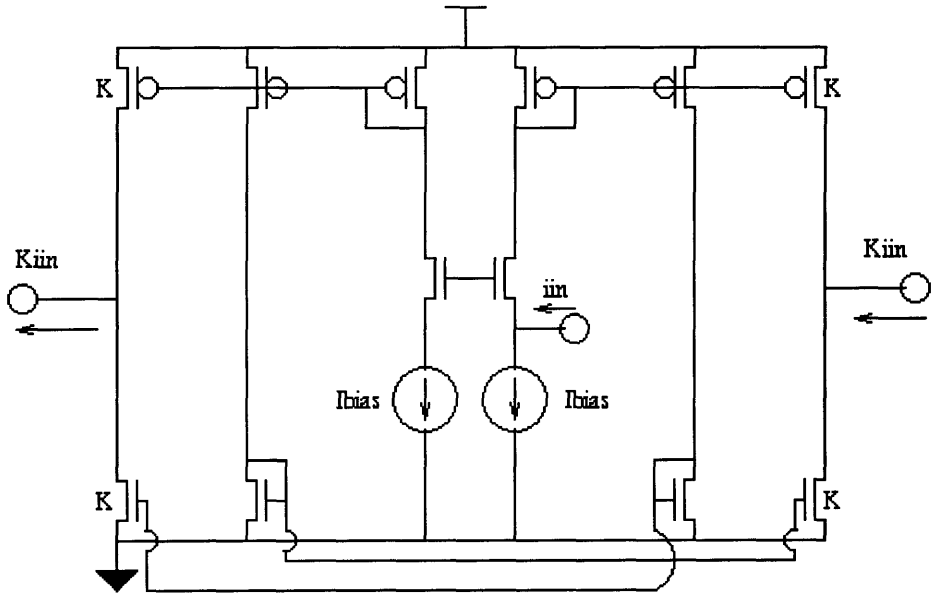


Figure 31: Klein and Robinson proposed current mode amplifier

After extensive simulations with a variety of different FET sizes and bias currents, it was found that the fundamental gain bandwidth product was smaller than that of the CMOS design of Section 6. In Section 6, a gain of 10dB was achieved with a –3dB bandwidth of 203MHz. The current mode amplifier of Figure 2 operates optimally with a gain of 8.4dB and a bandwidth of 189MHz. The CMA gain bandwidth product is thus 77% of the Section 6 design's gain bandwidth product. Since the goal was to use the Klein and Robinson architecture to achieve better system performance, the Klein and Robinson model was thus abandoned.

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