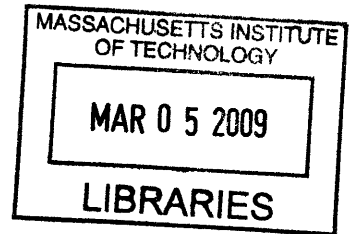
High Quality Metamorphic Graded Buffers with Lattice-Constants Intermediate to GaAs and InP for Device Applications



by

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Submitted to the Department of Electrical Engineering and Computer Science
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Doctor of Philosophy in Electrical Engineering

at the

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Kenneth Eng Kian Lee

Submitted to the Department of Electrical Engineering and Computer Science on December 22, 2008 in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electrical Engineering

Abstract

We have investigated the use of a continuous, linear grading scheme for compositionally-graded metamorphic $In_xGa_{1-x}As$ buffers on GaAs, which can be used as virtual substrates for optical emitters operating at wavelengths > 1.2 μm. Such virtual substrates will allow access to new materials that can be used for designing optical and electronic devices with superior characteristics and performances compared with conventional devices that are grown lattice-matched on standard substrates such as GaAs and InP. In addition, the principles behind such graded buffers can be used to bridge different lattice-constants, which can be a pathway to future integration of previously distinct classes of devices that have been defined by the lattice-constant on which they were built (e.g. Si-based, GaAs-based, InP-based etc.).

Graded buffers with threading dislocation densities (TDD) < 9.5×10^4 cm^{-2}, at a final composition of x = 0.346 were obtained, representing the lowest value ever achieved at or around this composition. Photoluminescence (PL) measurements were carried out on InGaAs quantum wells (QWs) that were re-grown on these buffers, and high luminescence efficiency was observed in the 1.2-1.5 μm wavelength range. Ridge-waveguide QW-separate confinement heterostructure lasers and heterojunction bipolar transistors (HBTs) were also grown on the graded buffers to demonstrate their applicability for device applications. Pulsed threshold current densities of 262 Acm^{-2} at room temperature were obtained for 2 mm long strained-InGaAs QW emitting at 1320 nm, with peak output powers up to 40 mW. Preliminary tests on the unoptimized HBTs revealed that they operate with dc current gains of up to 13.

A new class of graded buffers using all-binary III-V semiconductors has also been demonstrated. Thin constituent layers of GaAs and InP are combined such that they act in a mechanically-similar fashion as a random alloy. We term this combination of many thin layers of constituent materials a Digital Metamorphic Alloy (DMA). The DMAs are used to replace conventional random-alloys in a metamorphic buffer layer. Such a DMA buffer has superior thermal conductivities to, and avoids materials growth-related problems associated with, conventional compositionally-graded random-alloy metamorphic buffers. The method of fabricating DMAs is described. Lattice-constant grading from GaAs to InP has been carried out using both the DMA concept, and a hybrid random-alloy-buffer/DMA approach.

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The path towards a PhD is a long and challenging one, and I owe many people a debt of thanks for helping me reach my goal.

I am filled with gratitude to my advisor, Gene Fitzgerald, who trusted me, an EE student with no prior materials science experience, with his brand new MOCVD reactor, and let me run wild with it. He was always there (even if not in person!) to provide direction and insight when needed, and perhaps even more importantly, his boundless optimism was a great source of encouragement when all seemed dark.

My other thesis committee members, Rajeev Ram and Clif Fonstad, were instrumental in my journey as well. Rajeev was a great teacher who helped in my re-education when I first came to MIT – it had been 5 long years since I last stepped into a classroom, and more than anyone else, he was the one who got me back up to speed. Clif was there to help me navigate the RQE, and continued to guide me till the end.

My entire experience would not have been as fulfilling here, were I not to have made great friends and colleagues in the Fitzgerald group. Michael Mori and Larry Lee were with me from the start as we tackled the new SEL MOCVD. It is no exaggeration when I say that they taught me everything I know about materials science and characterization techniques, and those are but a small fraction of the lessons I have learnt from them. As the SEL MOCVD team grew, I got to work closely with Bai Yu, Yang Li, Chengwei Cheng, Nan Yang, Arthur Pitera and Mayank Bulsara. I could not have chosen to work with a more dedicated and welcoming group of people, and I will remember all the "fun" we have had with the reactor, and their willingness to render me whatever help I needed. I wish them all the best as they stress the reactor with even more cutting-edge growths going forward. Nate Quitoriano was actually the first senior student I got to work with, and he introduced me to the wonderful world of InGaAs graded buffers (see Chapter 3). Steve Boles, Carl Dohrman and Saurabh Gupta were the guardians of the 5th floor CVD lab, and could always be counted on to provide a welcome distraction from the travails we faced in the SEL. Haryono Hartono and Charles Ho came by for a while and reminded me of Singapore, inspiring me to work harder so I could go home. Prithu Sharma is a new addition, and I wish him, and everyone else, luck as he brings more SiGe/III-V mayhem to the SEL MOCVD! I would also like to thank Jenna Picceri for handling all the administrative stuff in the group so the rest of us do not have to.

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TABLE OF CONTENTS

TABLE OF CONTENTS 6
LIST OF FIGURES 9
LIST OF TABLES 14
1. INTRODUCTION 15
1.1 Long-wavelength emission on GaAs substrates 18
- 1.1.1 Dilute-nitride devices 19
- 1.1.2 Quantum dot (QD) devices 20

1.2 Growth on virtual substrates with engineered lattice-constants 21
- 1.2.1 Effects of compressive strain caused by lattice-mismatch 21
- 1.2.2 Critical thickness limits of the QW 22
- 1.2.3 Compressive-strain-induced blue-shifting of band edge energies 25
- 1.2.4 Effect of strain-relaxation 26

1.3 Organization of the thesis 27
2. MATERIALS GROWTH AND CHARACTERIZATION 28
2.1 Metalorganic chemical vapor deposition (MOCVD) 28
- 2.1.1 H_2 and N_2 manifold/carrier gas 29
- 2.1.2 Mass-flow controllers 31
- 2.1.3 Sources 32
- 2.1.4 Gas manifold and CCS technology 36
- 2.1.5 Scrubber 37
- 2.1.6 Glovebox 38
- 2.1.7 MOCVD Operation 39
- 2.1.8 Compositional control for In(Al)GaAs growth 43
- 2.1.9 EpiTT – In-situ emissivity-corrected optical pyrometry 46
- 2.1.10 Maintenance 46

2.2 Materials characterization techniques 49
- 2.2.1 Transmission electron microscopy (TEM) 49
- 2.2.2 X-ray diffractometry (XRD) 51
- 2.2.3 Atomic force microscopy (AFM) 52
- 2.2.4 Photoluminescence (PL) 52
- 2.2.5 Secondary ion mass spectroscopy (SIMS) 53
- 2.2.6 Electroluminescence (EL) 53
- 2.2.7 3ω thermal conductivity measurements 54

3. METAMORPHIC COMPOSITIONALLY-GRADED $In_xGa_{1-x}As$ BUFFERS 55
3.1 Theory of graded buffers 56
3.2 Challenges for InGaAs graded buffers 57
3.3 Experiments 59
3.4 Results and Discussion 61
- 3.4.1 Comparison with previous work 63
- 3.4.2 Examination of parameters affecting graded buffer quality 64
  - 3.4.2.1 Effect of grading rate 65

3.4.2.2 Effect of terminal composition 67
3.4.2.3 Effect of substrate orientation 69
3.4.2.4 Effect of growth temperature 71
3.4.3 Re-grown quantum-well separate confinement heterostructures (QW-SCH) 73
3.5 Conclusion 77
4. METAMORPHIC InGaAs QW LASERS 79
4.1 Design of the QW-SCH laser 79
4.1.1 Challenges in using the quaternary $In_xAl_yGa_{1-x-y}As$ alloy 79
4.1.2 Calculation of materials parameters 80
4.1.3 Calculation of dielectric constants using MDF 84
4.1.4 Waveguide design 85
4.2 QW-SCH laser growth 86
4.3 Device fabrication 89
4.4 Device testing and results 91
4.4.1 CW L-I-V testing 91
4.4.2 Pulsed L-I-V testing 95
4.4.3 Pulsed temperature studies 96
4.4.4 Spectral measurements 98
4.5 Summary 100
5. OTHER MINORITY-CARRIER DEVICES ON InGaAs GRADED BUFFERS 101
5.1 Metamorphic InAlGaAs/InGaAs heterojunction bipolar transistors ... 101
5.1.1 Motivation for metamorphic InAlGaAs/InGaAs HBTs 101
5.1.2 Design of the metamorphic InAlGaAs/InGaAs HBT 102
5.1.3 HBT growth 104
5.1.4 HBT material characterization 104
5.1.5 Device results 107
5.2 Metamorphic photovoltaic cells grown on InGaAs graded buffers 112
5.2.1 Motivation for metamorphic PV cells 112
5.2.2 Preliminary metamorphic InGaP cell results 114
5.3 Summary 115
6. DIGITAL METAMORPHIC ALLOYS (DMA) FOR METAMORPHIC GRADED BUFFERS 116
6.1 DMA design 119
6.2 Experimental details 121
6.3 Growth challenges 122
6.3.1 Intermixing of GaAs/InP 122
6.3.2 Growth rate variation 124
6.3.3 Critical thickness constraints 129
6.4 Results 132
6.4.1 DMAGB1 – DMA graded buffer to low (30%) InP composition; uncapped 132

6.4.2 DMAGB2 – DMA graded buffer to moderate (60%) InP composition; capped with $In_{0.43}Ga_{0.57}As$ 134
6.4.3 DMAGB3 – DMA graded buffer to InP; annealed 136
6.4.4 DMAGB4 and DMAGB5 – Hybrid conventional graded buffer + DMA graded buffer; capped with InP 138
6.4.5 Thermal conductivity measurements 141
6.5 Summary 144
7. SUMMARY OF RESULTS; SUGGESTIONS FOR FUTURE WORK 145
7.1 Research highlights 145
7.1.1 High quality compositionally-graded metamorphic InGaAs buffers 145
7.1.2 Metamorphic strained-InGaAs QW-SCH ridge waveguide laser 146
7.1.3 Metamorphic InAlGaAs/GaAs HBTs and InGaP PV cells 146
7.1.4 Digital metamorphic alloys 146
7.2 Future research directions 147
7.3 Conclusion 149
APPENDIX A 150
REFERENCES 152

LIST OF FIGURES

Figure 1.1 – Bandgap vs. lattice-constant plot of the III-V compounds. The dark blue lines correspond to direct-gap alloys, while the light blue lines correspond to indirect-gap alloys....17

Figure 1.2 – Critical thickness of $In_xGa_{1-x}As$ QWs on GaAs substrates as a function of In content in the QW. The critical thickness plotted here is twice the value calculated from Equation (1.2), which, as noted above, approximately accounts for the metastability of capped QWs....23

Figure 1.3 – Plot of the emission wavelengths that can be obtained for: a) strained-InGaAs QWs on GaAs substrates; b) unstrained-InGaAs QWs on appropriate virtual substrates; c) 1% strained-InGaAs QWs on the same virtual substrates. For (b), the indium mole fraction in the QW and the final composition of the virtual substrate is assumed identical, and in all cases, the QW thickness is set to the lesser of 150Å or the critical thickness as plotted in Figure 1. Emission wavelength calculation parameters are from [23] 26

Figure 2.1 – Photograph of the reaction chamber of the SEL MOCVD that was used to grow the samples reported in this thesis. The flip-top showerhead, through which all gases are injected into the chamber, is currently raised, revealing the 6 × 2" susceptor is currently installed in the chamber....29

Figure 2.2 – Schematic of the gas manifold for the MOCVD.... 37

Figure 2.3 – Screenshot of EpEdit program used to write growth recipes....40

Figure 2.4 – Schematic depicting the difference between (a) a standard source line and (b) a double-dilution line.... 41

Figure 2.5 – Empirically determined values for R_{In} and G for InGaAs alloys.... 45

Figure 2.6 – SIMS scan of an AlGaAs/GaAs QW growth.... 48

Figure 2.7 – SIMS scan of a Si doping staircase.... 48

Figure 3.1 – Summary of reported TDD results for various $In_xGa_{1-z}As$ graded buffers in literature.... 58

Figures 3.2(a) and (b) – (a) PV-TEM and (b) X-TEM images of graded buffer GB1, which has a final cap composition of $In_{0.346}Ga_{0.654}As$.... 62

Figure 3.3 – Plot showing the TDD measured from various graded buffers. Solid symbols represent data from this work, while open symbols represent data from [38]....65

Figure 3.4 – X-TEM of GB3, an InGaAs graded buffer graded at a rate of 1.39% misfit/μm. Note the dislocation contrast that abruptly turns from a misfit into a thread when its glide is impeded at a phase-separated region...67

Figure 3.5 – X-TEM of graded buffer GB6. Periodic contrast characteristic of phase separation is clearly visible near the top of the graded buffer................................ 68

Figures 3.6(a) and (b) – X-TEMs of (a) sample GB7 and (b) sample GB8. The stronger phase separation contrast compared with sample GB6 despite not being graded as far appears to be the result of growing on offcut wafers. The significantly earlier onset of phase separation in GB8, and its strength, leads to large numbers of defects and high surface roughness.. 70

Figures 3.7(a) and (b) – (a) X-TEM and (b) PV-TEM images of sample GB9. While no threading dislocations or clear signs of phase separation are evident in the graded buffer cap, a wavy contrast can be seen, which might signify segregation of the InGaAs alloy into closely-spaced Ga-rich and In-rich regions. PV-TEM shows wavy features on the wafer surface that look like short branch defects aligned in the $[0\bar{1}1]$ direction........... 72

Figures 3.8(a) and (b) – Symmetric (400) RSMs taken by HR-XRD of (a) the graded buffer alone, and (b) with a re-grown QW-SCH. The GaAs substrate peak is the stronger peak towards the right edge of the images (the weaker peak is the Kα2 peak), while the strong peak on the left is that of the InGaAs graded buffer cap and, in the case of (b), the QW-SCH InAlAs cladding and InAlGaAs barrier layers as well. The lack of a clear satellite peak in (b) indicates that the QW-SCH layers and the graded buffer cap are pretty well-lattice-matched.. 74

Figure 3.9 – X-TEM image of a QW-SCH. The image was taken with an on-pole diffraction condition..75

Figure 3.10 – Room-temperature PL spectra for a set of 4 different QWs (each normalized to their respective maxima) grown on the same virtual substrate platform... 76

Figure 3.11 – Normalized low-temperature (20 K) PL spectra for a QW with 49% In. The Si detector was used to pick up the shorter-wavelength emission from the cladding (~595 nm) and SCH (~1050 nm) layers, while the InGaAs detector was able to pick up the emission from the SCH layers and the QW.. 77

Figure 4.1 – Bandgap energy vs. lattice-constant diagram for the InAlGaAs alloy system.. 82

Figure 4.2 – X-TEM image of a QW-SCH grown on an InGaAs graded buffer...........87

Figure 4.3 – PL spectra of the doped QW-SCH structure after various etch times........ 88

Figure 4.4 – Schematic of a processed ridge-waveguide QW-SCH device................90

Figure 4.5 – L-I-V curves for an 8 μm wide, 2129 μm long device, tested under CW conditions. Emission was centered around 1330 nm..92

Figure 4.6 – L-I-V curves for a 20 μm wide, 2129 μm long device from Piece 1, and a 20 μm wide, 2206 μm long device from Piece 4, tested under CW conditions. The device from Piece 1 was tested previously without any interfacial material, while the one from Piece 4 was tested with the Ga-Sn solder. Emission was centered around 1330 nm....... 94

Figure 4.7 – L-I curves for a 20 μm wide, 2129 μm long device from Piece 1, tested at various duty-cycles. The external DQE has also been calculated and plotted..............95

Figure 4.8 – L-I curves taken as a function of temperature for a 1201 μm long and 14 μm wide...97

Figure 4.9 – Optical spectra of a 20 μm wide, 2129 μm long device at 20°C, below and above threshold...98

Figure 4.10 – Optical emission spectra taken at varying TEC temperatures of a device from Piece 4..99

Figure 5.1 – Calculated CBO and VBO values for a lattice-matched InAlGaAs/$In_{0.3}Ga_{0.7}As$ heterojunction as a function of Al mole fraction in the InAlGaAs quaternary alloy. The band gap of the InAlGaAs alloy is also plotted for reference......103

Figure 5.2 – X-TEM image of HBT_1 that was re-grown on an $In_{0.295}Ga_{0.705}As$ graded buffer...105

Figure 5.3 – X-TEM image of HBT_2 that was grown continuously together with an $In_{0.26}Ga_{0.74}As$ graded buffer.. 106

Figure 5.4 – I-V measurements of subcollector isolation. In the figure, "S.I. GaAs" refers to isolation data taken from a control semi-insulating GaAs wafer. "MIT 549" refers to HBT_2, while "MIT 405+406P1 + 525" refers to HBT_1.Figure provided by NTU....107

Figure 5.5 – I-V characteristics of pre-annealed n^+ emitter and n^+ subcollector contacts in HBT_2. Figure provided by NTU...108

Figure 5.6 – MOCVD growth log data for the Si_2H6 n-dopant source during the growth of the device layers for HBT_2. The Si_2H_6 source is configured with a double dilution line, and S_In and S_Final represent the setpoint values of the input and final MFCs, while A_In and A_Final are the actual values of the same MFCs. (See Chapter 2 for a more detailed explanation of the MOCVD source lines)..................................109

Figure 5.7 – X-TEM image of HBT_3 that was grown continuously together with an $In_{0.305}Ga_{0.695}As$ graded buffer...110

Figures 5.8(a) and (b) – I-V data for the (a) base-emitter and (b) base-collector p-n junctions of HBT_3 111

Figure 5.9 – Reference solar spectra at AM1.5 (ASTM G173-03 Reference Spectra), with bandgaps of InAlAs, InGaP and InGaAs lattice-matched to $In_{0.3}Ga_{0.7}As$ overlaid 113

Figure 5.10 – PL spectrum of a metamorphic InGaP PV cell on an $In_{0.3}Ga_{0.7}As$ graded buffer 114

Figure 6.1 – Schematic illustrating the use of DMAs to replace ternary random alloys in the construction of a metamorphic step-graded buffer. The illustration depicts the use of GaAs/InP DMAs on the left and InGaAs ternary alloys on the right 117

Figure 6.2 – Poor quality InP/GaAs DMA layers due to uncontrolled intermixing between the alternating InP and GaAs layers 123

Figure 6.3 – Schematic of the original and modified gas switching sequences. The latter was used to cut down on intermixing between the InP and GaAs layers 124

Figure 6.4 – Graph depicting the growth rate trends observed for InP and GaAs layers as a function of which DMA they are being grown on 125

Figure 6.5 –X-TEM image showing the effect of growing DMA layers beyond critical thickness limits 129

Figure 6.6 – X-TEM image depicting a DMA graded buffer constructed with InP and GaP layers. The GaAs substrate is at the bottom 131

Figure 6.7 – X-TEM image of DMAGB1 with three different DMAs, grown to a terminal composition of approximately 30% InP 133

Figure 6.8 – X-TEM image of DMAGB2, graded up to 60% InP, capped with InGaAs 135

Figures 6.9(a) and (b) – X-TEM images of DMAGB3, (a) as-grown and (b) after annealing 136

Figure 6.10 – XRD reciprocal space map of (400) family of planes for DMAGB4, a hybrid InGaAs random-alloy graded buffer + DMA graded buffer 139

Figure 6.11 – X-TEM image of DMAGB4, a hybrid InGaAs random-alloy graded buffer + DMA graded buffer 140

Figure 6.12 – X-TEM image showing the top of DMAGB5 141

Figure 6.13 – Plot of temperature rise vs. angular frequency from 3ω measurement of conventional analog InGaAs graded buffer.......142

Figure 6.14 – Plot of temperature rise vs. angular frequency from 3ω measurement of DMAGB4.......143

LIST OF TABLES

Table 2.1 – List of gases used in the SEL MOCVD.. 32

Table 2.2 – List of MOs installed in the SEL MOCVD.....................................33

Table 3.1 – Summary of the various graded buffers described in this work. Offcut represents the number of degrees towards the in-plane [011] that the (100) substrate is miscut, with "0°" signifying an on-axis wafer. Terminal composition is the final indium alloy composition of the cap layer at the top of the graded buffer. Relaxation is the amount of misfit between the cap layer and the substrate that is relieved by the graded buffer. TDD is obtained from analyzing PV-TEM images, except in cases where X-TEM reveals the presence of significant numbers of threads in the cap and we establish a lower limit of 10^8 cm^{-2}... 61

Table 3.2 – Peak widths from the RSMs in Figure 7. HWHM values are reported for the 2θ widths as the presence of the graded buffer distorts the width measurement on the high-angle side... 74

Table 5.1 – Layer structures of the AlGaAs/GaAs HBT (Sample A) from reference [75], and of the InAlGaAs/InGaAs metamorphic HBT in the current work..................... 102

Table 6.1 – Thermal conductivities of selected semiconductor materials. Data reproduced from [84]. 118

Table 6.2 – Details of a grading scheme used for DMA graded buffers in this work... 119

Table 6.3 – Summary of DMA graded buffers discussed in this section.................. 132

Table 6.4 – Summary of XRD and X-TEM measurements of DMAGB1................ 133

Table 6.5 – Summary of XRD and X-TEM measurements of DMAGB2................ 135

Table 6.6 – Summary of XRD and X-TEM measurements of DMAGB3 after annealing.. 138

Table A.1 – Table of binary semiconductor material properties used in calculations... 150

Table A.2 – Table of bowing constants used for calculating ternary material properties...151

1. INTRODUCTION

The advent of epitaxy has been responsible for many of our electronic technological advances since the 1960s. Over the last five decades, many advances have resulted directly from semiconductor technology, in fields such as computer and information technology, telecommunications, and consumer electronics, and the key driver of this progress has been the ability to grow high quality semiconductor materials to take advantage of novel and complex device designs.

However, one key limitation that has existed all this time has been the need for lattice-matching to obtain high-quality materials growth for useful, high-performance devices. Indeed, the very definition of epitaxy is that an underlying crystal is used as a seed from which subsequent, identical, crystal layers are grown, which naturally makes putting down dissimilar crystal layers a challenge. This is the reason why heteroepitaxy, the growing of different crystal layers, was considered a vastly important achievement that opened up the parameter space for device design greatly. As a result of improvements to crystal growth processes and technology, the ability to deposit materials possessing different electronic and optical properties with atomically abrupt junctions was gained. Device designs with increasing complexity and functionality could now be realized; they could now include engineered bandgaps and optical waveguides, or even possess built-in electric fields for the modification of carrier transport. Yet, heteroepitaxy, initially, was still limited to lattice-matched heteroepitaxy, such as in the case of GaAs/AlGaAs in which the materials are almost lattice-matched. Due to the almost identical lattice-constants, the different materials could be grown on top of each other with the requisite thicknesses (on the order of hundreds of nm or microns) for devices, without the formation of large numbers of extended defects which would render the devices unusable. However, the choices for device layer materials were limited based on the choice of the starting substrate, as they had to maintain the lattice-matching condition, thereby limiting device designs. Pseudomorphic devices, which include thin strained-layers with lattice-constants different from the substrate, have opened up new possibilities, such as high electron mobility transistors [1] and highly efficient InGaAs quantum well (QW) lasers [2], which are of great importance today. However, the thicknesses of the strained-layers are constrained by critical thickness limits, so by and

large, the bulk of the device layers still have to be lattice-matched to the substrate. Thus, the fundamental problem still exists that there is no way to grow high quality lattice-mismatched materials on a given substrate, as the dissimilarity in the crystal lattices of the epitaxial film and the underlying substrate meant that defects would form during growth.

Indeed, after over 40 years, the situation continues to persist, and we find that device designs are to a large extent still limited by the availability of substrates. In fact, if anything, the semiconductor industry of today's focus on yield, cost and scalability now means that the size of available substrates has become another important consideration as to whether a technology is (economically) viable. That a single-crystal wafer is of high quality may no longer be sufficient for industry to adopt it as a viable platform for a given application, if the wafers cannot be made large enough. A case in point would be mid-IR and thermoelectric devices grown on InAs or GaSb substrates. While single-crystal substrates of these materials are available, they are typically limited to 3" or smaller, due partly to their mechanical softness, and they cost significantly more than more conventional Si, GaAs or InP substrates. This leads to significantly higher costs per device, which might be all it takes to keep promising technologies out of the market.

This is where the work in this thesis comes in. It is geared towards overcoming the lattice-matching constraint, so that new materials that previously had no matching substrate can be grown, and their material properties accessed. This work also forms part of the foundation for the integration of different material systems, to enable greater device functionality on a single platform, as well as potentially reduce costs by migrating material systems onto lower-cost substrates such as silicon that can be used with larger-scale and higher-yield fabrication processes. As alluded to earlier, this could also enable the development of devices and applications which otherwise might not have been deemed viable from a cost standpoint.

We seek to achieve these goals by using metamorphic graded buffers as the means to controllably engineer the lattice-constant from one determined by a given substrate, to another, while preserving the crystal quality. This graded buffer can then be used as a virtual substrate with the modified lattice-constant on which subsequent epitaxial device layers can be grown. In this way, the lattice-matching constraint on

epitaxy can be relaxed, and if done correctly, one can theoretically integrate any arbitrary set of materials onto one's substrate of choice, even mixing material systems such as Group IV crystals (e.g. Si, Ge etc.) with Group III-V materials (e.g. GaAs, InP etc.). Hitherto unusable materials, due to the lack of an appropriate substrate, can now also be used, enabling a wider choice of materials that should allow for more optimal design choices.

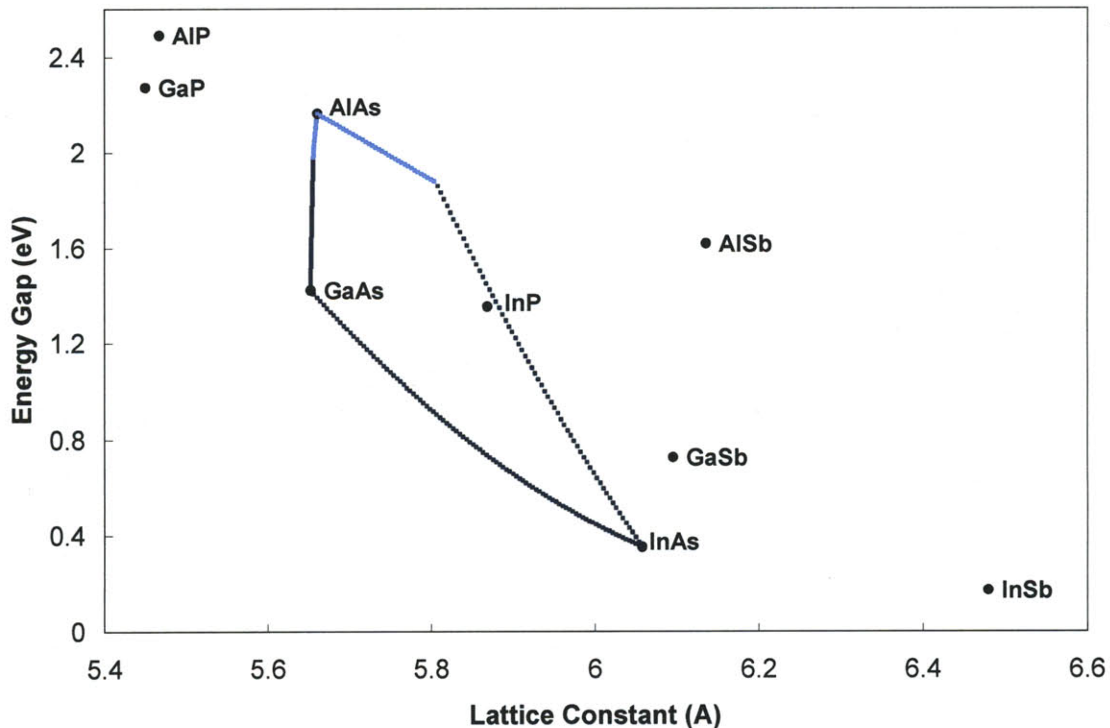


Figure 1.1 – Bandgap vs. lattice-constant plot of the III-V compounds. The dark blue lines correspond to direct-gap alloys, while the light blue lines correspond to indirect-gap alloys.

As can be seen from Figure 1.1, the III-V material family spans a wide range of lattice-constants and bandgaps, which demonstrates the size of the parameter space that can be opened up with the development of metamorphic epitaxial technologies. Of course, for the purposes of this thesis, we can only focus on a small portion of this parameter space, and that portion is the InAlGaAs alloy system, which has been highlighted in Figure 1.1. Even more specifically, the work in this thesis is most concerned with the lattice-constants intermediate to GaAs (5.65325 Å) and InP (5.8697 Å); the InAlGaAs alloys in this space span a bandgap range of about 0.8-2.2 eV,

which makes them useful for many device applications, including optical telecommunications and high speed electronics.

It is therefore our goal to develop high quality metamorphic graded buffers on GaAs substrates to allow us to access the materials in this space which should open up new avenues for novel device design. The question of how to judge the quality and usefulness of our graded buffers now becomes relevant. In most instances, a key determining factor as to whether a material sample is "good" or "bad" is its minority carrier lifetime. This is because this quantity is likely the first to suffer when defects are introduced into a perfect crystalline material, as they serve as traps and carrier scattering centers. Furthermore its importance in determining the performance of certain devices, chief among them are lasers and transistors (and any other electronic devices with one or more p-n junctions), cannot be overstated.

We can therefore conclude that one of the most important properties our graded buffers must possess is the ability to support the subsequent growth of material with long minority carrier lifetimes, and one of the best ways to highlight this would clearly be to develop a laser on the graded buffer. Furthermore, to showcase the enabling technology aspect of graded buffers, we will aim for a device that is not readily achievable on GaAs substrates. One of the main tasks in this thesis is therefore to demonstrate a long wavelength (> 1.3 μm) laser on a metamorphic graded buffer, and in the next section, we will discuss why this is a challenge for GaAs substrates and the solutions graded buffers provide.

1.1 Long-wavelength emission on GaAs substrates

The mainstay of semiconductor emitters at or above 1 μm has traditionally been the strained-InGaAs quantum-well separate-confinement heterostructure (QW-SCH) laser, which has demonstrated low thresholds, high efficiencies and high powers [2, 3]. In these devices, AlGaAs is typically used for optical cladding layers, and GaAs for the barrier layers. To obtain the QWs, indium is added to GaAs, which lowers the bandgap, thereby lengthening the wavelength of emission. However, as more indium is added to the QW, it becomes increasingly compressively strained, which effectively increases the bandgap of the QW as well as limits the thickness of the QW that can be grown, both of

which result in a blue-shifting of the emission. This blueshifting counteracts the lengthening of the wavelength sought by adding indium, and ultimately limits the emission wavelength obtainable to about 1.2 μm [4-6].

Researchers are therefore actively investigating other technologies to obtain longer wavelength emission devices on GaAs substrates. Two of the most common approaches that have emerged are the use of dilute-nitrides (InGaAsN) and the use of In(Ga)As quantum dots (QDs) for the active regions of such long-wavelength devices.

1.1.1 Dilute-nitride devices

In 1991, Weyers *et al* first demonstrated that the addition of small amounts of N to (In)GaAs led to a significant reduction in the electronic bandgap [7], and in 1995, Kondow *et al* suggested exploiting this effect for accessing the longer wavelengths necessary for telecom applications on GaAs [8]. The small atomic radius and high electronegativity of N also lead to reductions in the lattice-constant of the InGaAsN alloy, which reduces the compressive strain of the material with respect to GaAs. This not only suppresses the blue-shifting of the emission wavelength, but also allows the addition of more In into the alloy, further extending the emission wavelength. Thus, only small amounts of N are needed to reach the telecommunications wavelengths – a typical 1.3 μm emitter is $In_{0.3}Ga_{0.7}As_{0.98}N_{0.02}$ [9].

There have been rapid advances in the field over the last few years. Jin *et al* recently reported obtaining CW InGaAsN QW lasers with threshold current densities as low as 150 Acm^{-2} for devices lasing at 1330 nm [10]. However, as more N is introduced into the QWs to further extend the wavelength, device performance suffers. For instance, Jaschke *et al* reported lasers with threshold current densities that increased from 690 to 2900 Acm^{-2}, as the lasing wavelength was increased from 1400 to 1590 nm with the further addition of N [11]. The deleterious effect of N on device performance represents the main issue facing researchers. Thermodynamic calculations suggest that N is immiscible in InGaAs [12], which imply that high quality material with > 2% N is difficult to obtain due to the likelihood of phase segregation, especially at higher growth temperatures which are generally favored for good crystal quality.

1.1.2 Quantum dot (QD) devices

Another technology that holds promise for reaching the telecommunications wavelengths of 1.3 μm and beyond is the use of QD active regions, typically in the GaAs/In(Ga)As system. Typically, the lattice-mismatch between InAs (or high In mole fraction InGaAs) and GaAs is utilized in a self-ordered growth mode to form QDs, allowing one to take advantage of the narrow bandgap of the InAs to access longer wavelengths. The three-dimensional quantum confinement of carriers in QDs leads to the complete localization of electrons and holes, resulting in delta-function-like densities of states (DOS) for the carriers. Thus, QD-based lasers potentially have low threshold currents, high differential and material gain, improved high-temperature performance, and increased tolerances to defects [13, 14].

Results of QD layers published in the literature have exhibited some of these traits, such as very low threshold current densities (< 7 Acm^{-2} per QD layer), low internal losses (~1-3 cm^{-1}) and high QE (> 80-96%) [15]. High power (watt-level) GaAs-based QD lasers have also been reported by Bimberg and Ledentsov [14], which are based on three-fold stacked QDs that emit at 1.3 μm with $J_{th} = 70$ Acm^{-2} (T_o ~ 170 K up to 60°C) and 85% differential quantum efficiency. While impressive, it should be noted that attempts to reach longer wavelengths have not been as successful.

Though the theoretical benefits of QDs have been predicted since 1982 [16], devices have still not been made that fully realize the potential of QDs. The challenge has been to realize QDs of both high density and good size- and shape-uniformity. The high density is required for high gain, while the uniformity is needed to prevent inhomogeneous broadening of the gain profile [17]. The commonly-utilized Stranski-Krastinow (S-K) growth method, being a type of self-ordered growth, means that crystal growers only have limited and indirect control over the qualities of the QDs they grow. Thus, the QDs grown can vary greatly as they are functions of not just macroscopic factors like growth process conditions, but also microscopic factors like strain-fields inherent in lattice-mismatched systems. Therefore, performance gains from using QDs have been limited by growth issues.

Furthermore, due to the significant quantum confinement experienced by carriers in QDs, longer wavelengths can only be obtained from larger dots (> 40 μm) [13]. This is

problematic; firstly, larger dot sizes generally lead to lower dot densities, and secondly, maximal dot sizes are limited by the amount of strain (and therefore lattice-mismatch) in the system – high-In content dots which have narrower bandgaps would experience more strain relative to the GaAs substrate, limiting dot sizes. These factors have made it much more difficult to obtain QD emitters beyond 1.3 μm.

1.2 Growth on virtual substrates with engineered lattice-constants

As can be seen, although the dilute-nitrides and QD devices allow access to longer wavelengths on a GaAs platform, the performances of devices made with these technologies are promising, but there remain significant fundamental challenges that must be overcome to obtain improved performances at longer wavelengths. An alternative strategy involves revisiting the strained-InGaAs QW devices which have demonstrated excellent performances, and attacking the problem limiting the emission wavelength at its source, namely, the compressive strain in the QW.

1.2.1 Effects of compressive strain caused by lattice-mismatch

As mentioned previously, there are two main reasons why emission wavelengths are limited to ~1.2 μm in conventional strained-InGaAs QW devices. Firstly, there is a critical limit to the thickness of the QW that can be grown before the material plastically deforms, which is determined by the amount of strain the QW experiences. Since the confinement energy of carriers in the QW increases as the QW gets thinner, the result is higher transition energies in the QW. Secondly, assuming the layer thickness is kept below the critical thickness and the layer stays pseudomorphic, there is an increase in band-edge energies caused by the biaxial compressive strain experienced by the QW.

The emission wavelength is determined by the total transition energy between the electron- and hole-ground states. This comprises the sum of each carrier's confinement energy in the QW, and the band edge energy of the QW. The critical thickness limit affects the former, while the compressive strain affects the latter. The following sections shall examine each of the effects in turn.

1.2.2 Critical thickness limits of the QW

Lattice-mismatched epitaxy is the growth of a single crystal film with a certain lattice-constant, a_f, on a single crystal substrate with a different lattice-constant, a_s. Due to the lattice-constant difference, a mismatch of

$$f = \frac{a_s - a_f}{a_f} = \varepsilon + \delta \tag{1.1}$$

arises, which is accommodated by the sum of the elastic strain, ε, and the plastic strain, δ [18]. Elastic strain is taken up by the distortion of atomic bonds of each of the atoms in the crystal lattice from a given equilibrium position, while plastic strain accommodates the lattice-mismatch by the formation of dislocations. The energy of formation of dislocations is a finite quantum and is generally greater than that required for small distortions of the atomic bonds, which increases continuously as atoms are increasingly displaced from their equilibrium positions. Thus, in lattice-mismatched epitaxy, the lattice-mismatched film will undergo elastic deformation initially, as the film is strained to match the substrate lattice-constant (which, to good approximation, is assumed to be unchanged, given that the substrate is generally orders of magnitude thicker than the film), and the mismatch in this case is entirely accommodated via elastic strain. This represents the regime of pseudomorphic growth.

As the thickness of the lattice-mismatched film increases, the total amount of elastic strain energy in the system increases, as the total elastic strain energy is proportional to the number of bonds distorted, which in turn is proportional to the amount of material grown (and hence film thickness). At some point, the total elastic strain energy becomes comparable to the energy for formation of dislocations, and when this happens, line defects known as misfit dislocations (or "misfits") form at the film/substrate interface, as it becomes energetically favorable accommodate some of the mismatch plastically. The thickness of the film at which this happens is known as the critical thickness, h_c, and marks the start of the regime of metamorphic growth.

The expression for the critical thickness, as calculated theoretically by Matthews and Blakeslee [19] using a force balance approach and modified by Fitzgerald [18] is given by the following transcendental equation:

$$h_c = \frac{D(1-\nu\cos^2\alpha)[\ln(h_c/b)+1]}{Yf} \qquad (1.2)$$

Here, D is the average shear modulus of the film and the underlying substrate (or SL, in our case). ν, b and Y are the Poisson's ratio, Burgers vector and Young's modulus of the film respectively, and f is the mismatch between the film and the underlying substrate. For 60° dislocations that are the first to form and are glissile [20], $\alpha = 60°$. From this expression, one can observe that h_c decreases rapidly as f increases. This is plotted in Figure 1.2.

It should be noted that in almost all instances, the theoretical figure for critical thickness is lower than experimentally determined values [20]. This is due to the kinetics of dislocation nucleation and glide, which are thermally-activated processes, and typical growth temperatures of 550-700°C are insufficient for the efficient generation and glide of dislocations. Due to this metastability, lattice-mismatched layers that are capped can be grown roughly twice as thick as the predicted critical thickness before dislocation nucleation occurs.

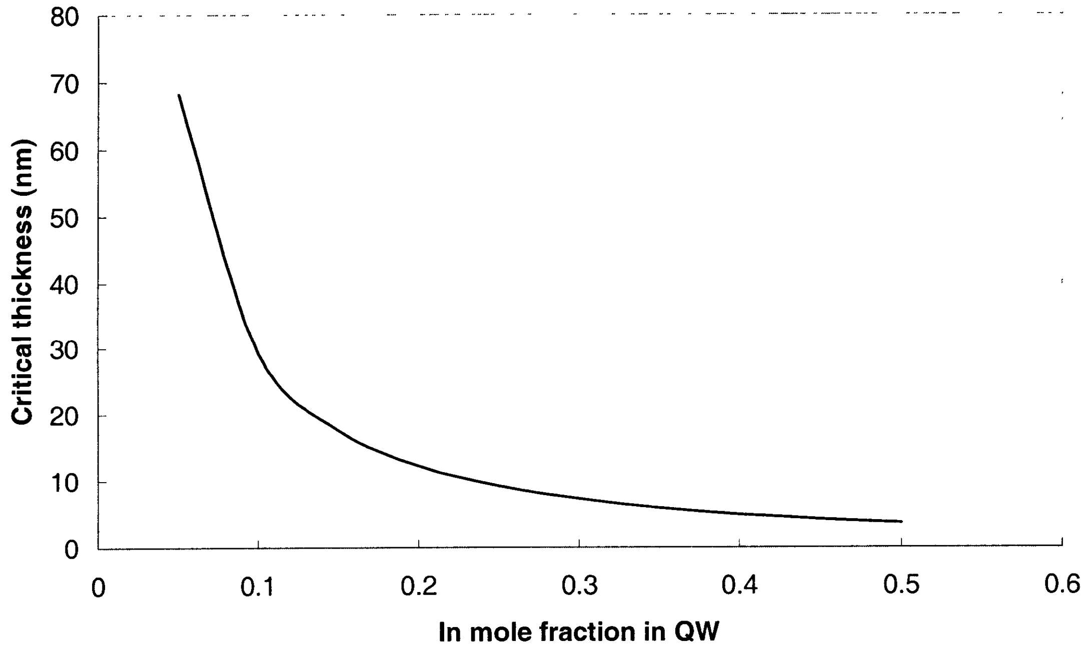


Figure 1.2 – Critical thickness of $In_xGa_{1-x}As$ QWs on GaAs substrates as a function of In content in the QW. The critical thickness plotted here is twice the value calculated from Equation (1.2), which, as noted above, approximately accounts for the metastability of capped QWs.

As Figure 1.2 shows, with increasing In in the QW and therefore increasing mismatch between the QW layer and the underlying substrate, the critical thickness before the QW layer starts to plastically relax rapidly decreases. In addition, higher amounts of mismatch lead to dislocations being nucleated at increasing rates, due to an increase in the strain built up in the QW layer per unit volume.

As dislocations can only terminate at a free surface (i.e. at the edges of the semiconductor crystal), the misfit dislocations have to either extend along the film/substrate interface or make their way through the film to the top surface. These latter dislocations are known as threading dislocations (or "threads"), and are the ones with the greatest impact on device quality, since by threading through the epitaxially-grown films, they will invariably pass through the active device layers. Being extended defects in the crystal, they serve as strong carrier scattering and recombination centers. A TDD that translates to dislocation spacing on the order of the minority carrier diffusion length and/or carrier mean free path will therefore lead to drastically reduced minority carrier lifetimes and/or mobilities, as well as altered electronic band structures [21, 22]. Obviously, this is most felt in minority carrier devices, such as diode emitters, and it is therefore critical that the threading dislocation density (TDD) be kept as low as possible. In general, this means that device layer thicknesses should always be kept below the critical thickness to prevent dislocation nucleation. It should be noted that the deleterious effects of any misfits formed at the interfaces defining the QW are particularly severe, due to the thinness of the QW. Thus, while the TDD might only be low or moderate when the critical thickness is just slightly exceeded for small amounts of mismatch, minority carrier lifetimes within the QW will still be greatly reduced, as the entire QW volume will likely be within the carrier mean free path of the misfit dislocations that are formed.

For QWs, their narrow dimension in the growth direction leads to discretization of the energies in the wells. These leads to an additional quantum confinement energy for each carrier in their respective potential wells which is not present for bulk layers, and which is strongly dependent on the width of the QW. These energy levels are given by the solutions to the eigenvalue equations of the finite well [23]:

$$\alpha = \frac{m_b^*}{m_w^*} k \tan k \frac{L_z}{2} \qquad \text{(even solution)} \qquad (1.3a)$$

$$\alpha = -\frac{m_b^*}{m_w^*} k \cot k \frac{L_z}{2} \qquad \text{(odd solution)} \tag{1.3b}$$

where

$$k = \sqrt{\frac{2m_w^* E}{\hbar^2}} \tag{1.4a}$$

and

$$\alpha = \sqrt{\frac{2m_b^*(V_o - E)}{\hbar^2}} \tag{1.4b}$$

Here, L_z is the width of the well, V_o is the potential barrier height, and m_w and m_b are the appropriate effective masses for the well and barrier respectively.

Solving these equations for E, one can observe that as L_z decreases, E increases rapidly, especially for $L_z < 100$ Å. Thus, as compressive strain in the QW increases, the critical thickness decreases, leading to an increase in the electron and hole confinement energies in the QW.

1.2.3 Compressive-strain-induced blue-shifting of band edge energies

From the previous section, we note that to preserve device performance, the device layers, (including any QW active regions) must be grown pseudomorphically. This implies that for a mismatched film such as a strained-QW, all the mismatch will be taken up as elastic strain. The effect of this strain on the bandgap of a given semiconductor film can be characterized using linear deformation potentials. The band edge shifts are given by [24]:

$$\delta E_c = 2a_c\left(1 - \frac{C_{12}}{C_{11}}\right)\varepsilon \tag{1.5a}$$

$$\delta E_{HH} = 2a_v\left(1 - \frac{C_{12}}{C_{11}}\right)\varepsilon + b\left(1 + 2\frac{C_{12}}{C_{11}}\right)\varepsilon \tag{1.5b}$$

where a_c and a_v are the conduction- and valence-band deformation potentials respectively, b is the shear deformation potential, and C_{11} and C_{12} are elastic stiffness constants. The convention used by [24] is that $a_c < 0$ and $a_v > 0$, and $b < 0$. For strained-InGaAs QWs on GaAs, $f = \varepsilon < 0$, and thus $\delta E_c > 0$. In general, a_c is significantly larger

than a_v and b, hence $\delta E_c > |\delta E_{HH}|$. This means that the effective bandgap of the InGaAs is increased by $(\delta E_c - \delta E_{HH}) > 0$.

1.2.4 Effect of strain-relaxation

The preceding sections elaborated on how compressive strain leads to increases in QW transition energies. However, if the compressive strain in the strained-InGaAs QW can be relieved, longer wavelength emission can be realized. By growing the QW-SCH on an appropriate virtual substrate with a lattice-constant greater than that of GaAs, we can reduce, or even fully relieve, the compressive strain that the QW would have experienced had it been grown on a GaAs substrate. By itself, this can lead to significant increases in the emission wavelength obtainable.

Furthermore, if we re-visit the concept of strained-QW devices, and start to strain the QWs relative to the virtual substrate, we can further extend the emission wavelengths, just as had been done previously with InGaAs on GaAs substrates. The key difference is that the new baseline zero-strain condition is now a QW that contains more In, which results in a longer wavelength. Figure 1.3 summarizes this in the form of three curves, showing the emission wavelengths of strained-QWs on GaAs substrates, and unstrained- and strained-QWs on virtual substrates.

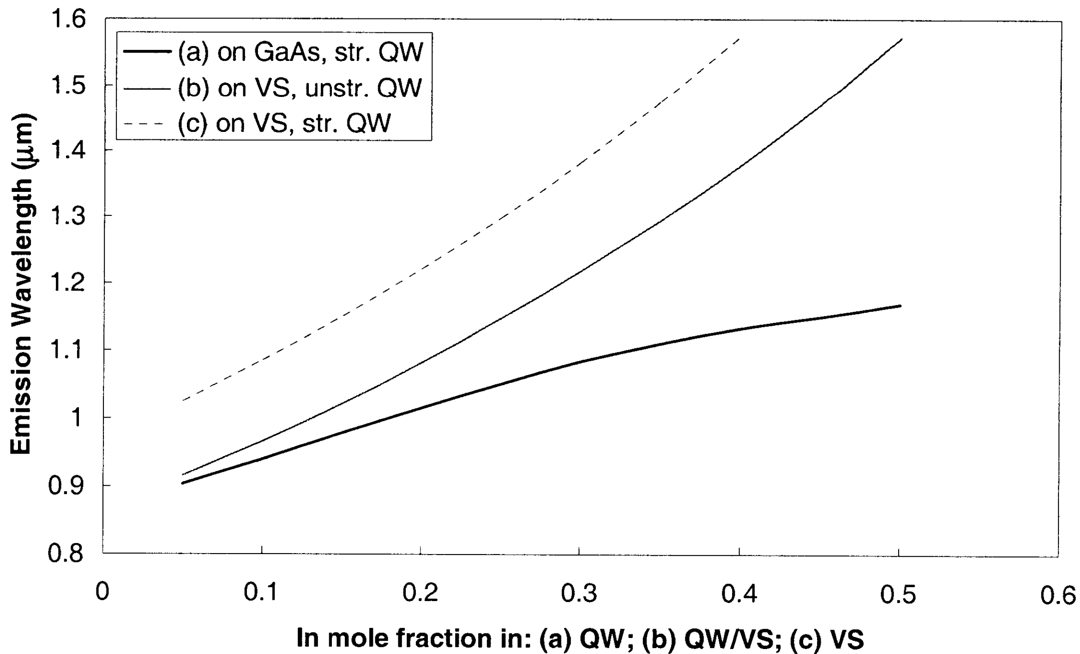


Figure 1.3 – Plot of the emission wavelengths that can be obtained for: a) strained-InGaAs QWs on GaAs substrates; b) unstrained-InGaAs QWs on appropriate virtual substrates; c) 1% strained-InGaAs QWs on

the same virtual substrates. For (b), the indium mole fraction in the QW and the final composition of the virtual substrate is assumed identical, and in all cases, the QW thickness is set to the lesser of 150Å or the critical thickness as plotted in Figure 1. Emission wavelength calculation parameters are from [23].

Clearly, emission wavelengths beyond 1.2 μm will be accessible, with emission up to 1.55 μm expected to be obtainable using $In_xGa_{1-x}As$ virtual substrates with $x < 0.40$. The challenge now is therefore to obtain high quality virtual substrates with low TDD such that such devices can be realized.

1.3 Organization of the thesis

This introduction has listed the motivations for metamorphic epitaxial growth, and stated the premise that high quality metamorphic graded buffers can be used as virtual substrates for high performance devices such as InAlGaAs-based lasers emitting beyond 1.3 μm. The rest of the thesis is laid out as follows. Chapter 2 details the materials growth and characterization techniques that were employed for the work described in the thesis. Emphasis is placed on the growth as a new reactor was used in this work, and the complexities of its operation deserve a more detailed discussion. Chapter 3 then briefly discusses the fundamentals of compositionally-graded metamorphic graded buffers, and details the work done to optimize the InGaAs graded buffers reported in this work. Chapter 4 follows with the design, growth, fabrication and characterization of quantum-well separate-confinement heterostructure (QW-SCH) ridge-waveguide lasers that are grown on the InGaAs graded buffers. Chapter 5 discusses the use of the graded buffer virtual substrates for other device applications, such as high-speed InAlGaAs/InGaAs-based heterojunction bipolar transistors (HBTs) and multi-junction photovoltaic (PV) cells. Chapter 6 explores the development of a new class of metamorphic graded buffers in which the engineering of the lattice-constant is effected in a novel way by replicating ternary random alloys with thin layers of binary semiconductors, which form what we have termed digital metamorphic alloys (DMAs). Finally, in Chapter 7, we summarize the work in this thesis, and offer suggestions of future paths that can be explored to take our work further.

2. MATERIALS GROWTH AND CHARACTERIZATION

In this chapter, we talk about the growth and characterization of the engineered materials grown in this work. The crystal growth performed in this work was almost exclusively done using metal-organic chemical vapor deposition (MOCVD) in a new facility at the Massachusetts Institute of Technology (MIT) called the Substrate Engineering Laboratory (SEL).

Several materials characterization techniques were used to characterize the microstructural properties and overall quality of the grown films, including transmission electron microscopy (TEM), x-ray diffractometry (XRD), atomic force microscopy (AFM) and Nomarski optical microscopy. Photoluminescence (PL) studies were carried out on QW structures to ascertain both the quality of the graded buffers, as well as the epitaxial films grown on them, while secondary ion mass spectroscopy (SIMS) was used to measure dopant and contaminant levels in our grown films. Finally, 3ω measurements, pioneered by Cahill [25, 26], were also used to obtain information on material thermal conductivity.

2.1 Metalorganic chemical vapor deposition (MOCVD)

MOCVD is a non-equilibrium form of CVD typically used for III-V epitaxy, so named because a large number of the precursors used are metalorganics (MO), where the group-III (and group-II, in the case of dopants) metallic species that are used have two or more alkyl hydrocarbon chains bonded to them. These carbon chains make the metallic species inert, such that they only react on a wafer surface, where enough thermal energy is present to pyrolyze the MOs, allowing them to take part in epitaxial growth in the presence of the appropriate Group-V sources.

It is not the purpose of this chapter of the thesis to go into detail about the theory of MOCVD. The reader is directed to other sources, such as Stringfellow's classic text [27], for a detailed treatment. Rather, this chapter will cover some of the operational aspects of the particular MOCVD reactor used for the work in this thesis, as this reactor is heavily customized, and can be said to be unique, in terms of both its configuration and its film growth capabilities. Our reactor is a low-pressure Aixtron/Thomas Swan 7x2" As/P close-coupled showerhead (CCS) configuration reactor that has been modified to

accommodate the growth a wide range of III-V materials, as well as SiGe alloys, in the same chamber. An image of the reaction chamber is shown in Figure 2.1.

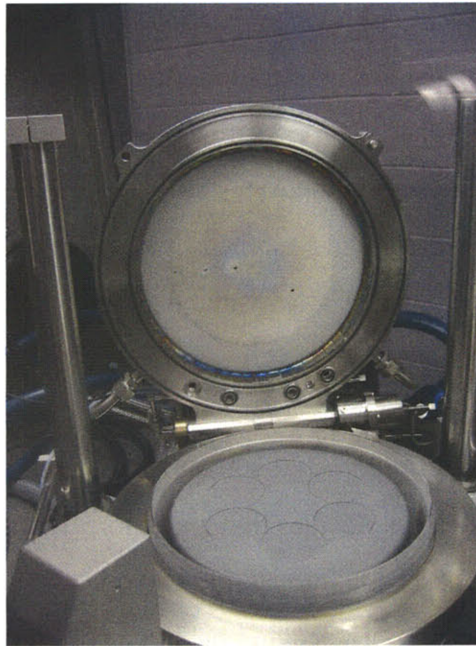


Figure 2.1 – Photograph of the reaction chamber of the SEL MOCVD that was used to grow the samples reported in this thesis. The flip-top showerhead, through which all gases are injected into the chamber, is currently raised, revealing the 6 × 2" susceptor is currently installed in the chamber.

2.1.1 H_2 and N_2 manifold/carrier gas

MOCVD relies on high purity, inert gases to carry reactants to the reaction chamber where they react on the wafer surface, and to carry waste reaction by-products away where they can be treated before being vented to atmosphere. Nitrogen (N_2) and hydrogen (H_2) are typically used together in this role, where N_2 is continuously flowed through the system when it is in idle, while H_2 is used for all parts of the process manifold (i.e. the lines leading into the reaction chamber proper) during growth. This has traditionally been due to the availability of higher purity H_2 as compared with N_2. In reality, either gas can be used for growth, though there have been studies that showed that H_2 leads to higher precursor pyrolysis rates for a given growth temperature [27], while others have demonstrated that N_2 potentially leads to better reactor temperature uniformity and stability [28]. Regardless of which carrier gas one uses for growth, process optimization must be carried out, and work in the group has confirmed that in almost all cases, films of similar quality can be obtained regardless of which carrier gas is used.

Both N_2 and H_2 are available for use as manifold/carrier gas in our MOCVD reactor. N_2 is obtained from boiling off LN_2 (commercially available from Airgas) and passing the gas stream through a Nanochem purifier at the source, and again through a SAES getter before entering the gas manifold in the reactor. The purpose of the purifier is to remove any particulates from the N_2 gas stream, while the getter is used to extract any residual oxygen and water present in the N_2 [29]. The latter is extremely effective, enabling a dewpoint as measured by a Panametrics hygrometer of better than -110°C.

H_2 is obtained from commercially available cylinders of VLSI 5.5 grade (99.9995% pure) hydrogen, fed through a crossover-panel that allows us to swap in and out new cylinders on the fly to cater for longer processes. Once again, prior to the gas entering the reactor's gas manifold, the H_2 stream is passed through a palladium (Pd) diffuser operating at 390°C. H_2 molecules that are adsorped on the "dirty" side of the Pd diffusion cell catalytically dissociate into atomic H, which subsequently gives up its electron to the Pd surface, essentially leaving behind a proton (H^+). Only the protons are able to diffuse through the bulk of the diffusion cell to the "clean" process side, where they recombine to form H_2 molecules once again. Other contaminants are therefore trapped on the dirty side, where a 1 slpm H_2 bleed gas flow sweeps them away, keeping the Pd diffusion cell surface clean for high purification efficiency. In this way, impurities are kept to a minimum, and a dewpoint better than -110°C can in theory be obtained.

In our reactor, we typically use N_2 as the manifold/carrier gas, due to its lower cost compared to H_2, for equivalent purity (after the action of all purifiers). Another practical reason is that the LN_2 storage tanks (refilled weekly) in our facility are able to provide a continuous supply of N_2 without any operator intervention, while for H_2 we are required to continually swap out cylinders as they are spent. Consider that to simply supply the 1 slpm bleed requires about a fifth of a size 300 cylinder per day, and that during growth the H_2 consumption rises to approximately 25 slpm, and the choice to use N_2 becomes obvious. However, a side effect that is generally undesirable is that N_2 is less efficient in removing heat from the system, and therefore at equivalent gas flows and reactor pressures, it takes almost three times as long to cool the reactor under N_2 than it does under H_2. This naturally sets an upper limit at the rate that we can drop the reactor

temperature, which leads to longer growth interruptions being required for temperature changes and limits on the ability to perform temperature cycling.

2.1.2 Mass-flow controllers

To control gas flow, we rely on mass-flow controllers (MFC), which are typically unidirectional-flow devices with a variable iris that is controlled with a feedback loop. The MFC measures the thermal conductivity of the gas flowing through it using an internal temperature probe, and from that determines the mass of gas flowing through it. It then varies the size of the iris to control the flow to the set point. As is readily apparent, given that different gases have different thermal conductivities, it is necessary to calibrate the MFC accurately for the gas that is expected to flow it. All the MFCs used in the reactor are calibrated for N_2, which means that the MFCs can only accurately determine and control gas flow if it is N_2 flowing through them. Fortunately, in the pressure range that we operate the MFCs at in the reactor (10-50 psig), all gases behave in a mostly linear fashion, and we can equate a measured mass flow of N_2 (as read by an MFC) to the actual mass flow of the gas that is actually flowing through the MFC, by the use of a Gas Correction Factor, which basically takes into account the difference in specific heat and density between 2 gases, according to the following relationship:

$$GCF_{ij} = \frac{c_j \rho_j}{c_i \rho_i} \times non-linearity\ correction\ factor \qquad (2.1)$$

where GCF_{ij} is the Gas Correction Factor to calculate the actual mass flow of gas i for a MFC calibrated for gas j. c_i *and* ρ_i are the specific heat and density of gas i, respectively. The non-linearity correction factor is an empirically determined value, and, relative to N_2, a recommended value of 0.88 is indicated for most gases (a notable exception is H_2, which is almost exactly linear with N_2) by MKS Instruments Ltd., which manufactures the MFCs used in our reactor. [30] Table 2.1 lists the gases used in our reactor, and their specific heat, density and GCF relative to N_2.

Gas	Specific heat (cal/g-K)	Density (g/l @ 0°C)	GCF (relative to N_2)
Nitrogen, N_2	0.2485	1.250	1.000
Hydrogen, H_2	3.419	0.0899	1.011
Arsine, AsH_3	0.1167	3.478	0.673
Phosphine, PH_3	0.2374	1.517	0.759
Silane, SiH_4	0.3189	1.433	0.598
Diborane, B_2H_6	0.508	1.235	0.436
Disilane, Si_2H_6	0.3189	2.66	0.322
Germane, GeH_4	0.14	3.28	0.595

Table 2.1 – List of gases used in the SEL MOCVD.

2.1.3 Sources

Like most MOCVD reactors set up to grow As- and P-films, our reactor is installed with the group-III metalorganic sources trimethylaluminum (TMAl), trimethylgallium (TMGa) and trimethylindium (TMIn) which serve as the aluminum (Al), gallium (Ga) and indium (In) precursors respectively, as well as the group-V hydride sources arsine (AsH_3) and phosphine (PH_3) which are the precursors for As and P. Dimethylzinc (DMZn) and 0.01% (balance H_2) disilane (Si_2H_6) are the p-type and n-type dopant sources, respectively. In addition, the reactor also came installed with unsymmetric dimethylhydrazine (UDMH) which is a nitrogen source for growing dilute nitrides, as well as trimethylantimony (TMSb) for growing Sb-films.

The latter two sources are less conventional sources, and relatively few MOCVDs in operation use them, but what truly sets our system apart is the added presence of group-IV sources, specifically silane (SiH_4) and germane (GeH_4), as well as 1% diborane (B_2H_6) for p-doping (n-doping is carried out using PH_3, though AsH_3 can potentially be used as well). This means that the reactor can be used for integrated in-situ growth of both III-V and SiGe films. Our MOCVD reactor was the first ever system with such a capability when it was commissioned in 2005, and, to the best of our knowledge, is likely still the only such system in the world. It has already enabled pioneering work such as the in-situ integration of Ge thin fims on (In)GaAs [31], as well as GaAsP on SiGe [32].

As can be expected, however, given the unconventional combination of precursors available in our reactor, cross-contamination issues are all the more likely to arise. These will be discussed shortly under the maintenance section.

We note at this point that the MOs are liquid sources (with the exception of TMIn, which is a solid source), and therefore they are introduced into the reaction chamber by bubbling (hence the container holding the MOs being called "bubblers") the carrier gas (generally N_2 in our case) through the MO, where it is assumed that the carrier gas gets saturated with the vapor pressure of the MO over the liquid (or solid). The actual amount of MO that is picked up by the carrier gas, the so-called "effective sccm" (which is directly equivalent to the number of moles or the mass of the MO), is given by

$$effective\ sccm\,MO = \frac{p_{MO}}{\left(p_{bubbler} - p_{MO}\right)} \times carrier\ gas\ flow \qquad (2.2)$$

where $p_{bubbler}$ is the total pressure over the MO in the bubbler (sometimes also called the overpressure), and p_{MO} is the partial pressure of the MO at the given bubbler temperature. The partial pressure of each MO has the following relationship with temperature:

$$p_{MO}(T) = 10^{B-A/T} \qquad (2.3)$$

where p_{MO} is the vapor pressure of the MO in torr, T is the temperature in Kelvins and A and B are empirically fitted constants. A summary of the MO sources installed in our reactor, as well as their key physical properties, is listed in Table 2.2 [33].

MO	A	B	Melting Point (°C)	Boiling Point (°C)
TMGa	1703	8.07	-15.8	55.7
TMAl	2134	8.224	15.4	127
TMIn	3204	10.98	88.4	134
TMSb	1697	7.71	-87.6	80.6
UDMH	1812.3	8.272	-58.15	63.85
DMZn	1560	7.8	-42	46

Table 2.2 – List of MOs installed in the SEL MOCVD.

Thus, we can influence the amount of MO that is "picked-up" and sent into the reaction chamber by not only adjusting the carrier gas flow, but also by changing the bubbler temperature and overpressure. In general, bubbler temperatures at or below room temperature are used, to prevent the condensation of the MO out of saturated carrier gas in cooler parts of the reactor. In cases where the vapor pressure of an MO is low and higher temperatures must be used, such as TMIn, holding the bubbler above room temperature requires us to place heat-tape around all the tubing downstream of the bubbler, to prevent any condensation from happening before the MO enters the reaction

chamber. Thus, we also rely on reduced bubbler pressures to enhance pickup, though it should be noted that lower bubbler pressures tend to result in slightly less stable carrier pick up, due to issues with incomplete saturation and increased sensitivity to temperature variation. This last statement points to the fact that to ensure uniform flow of the MO into the reaction chamber, it is necessary to maintain the bubblers at a precisely controlled temperature. This is done with the aid of a refrigerated bath with a thermoregulator, which holds the temperature of the bath (and the bubbler placed inside it) to within 0.1°C

As the majority of the MO gas stream is actually the N_2 carrier gas, the purity of the N_2 is of utmost importance. In contrast, the hydrides, which are gases at our process temperatures and pressures, are flowed directly into the reactor. Thus, there are additional reactive resin purifiers from Millipore attached to the AsH_3 and PH_3 lines, whose purpose is also to remove oxygen and water contaminants from the gas. We have found through experience that to obtain a dewpoint < -95°C in the respective lines, the PH_3 purifier is necessary, while the AsH_3 purifier is not. Consequently, we do not operate with the AsH_3 purifier. This removes a potential source of problems, because Aixtron/Thomas Swan have reported that under stagnant flow conditions (i.e. during idle, when no toxics are flowing), the resin in the AsH_3 purifier outgases some of the previously captured contaminants, leading to a buildup of pressure in the line, to say nothing of the contaminants. Thus, usage of the AsH_3 purifier is more suited to production environments where toxics are flowing essentially continuously, rather that our laboratory research environment where growth processes are usually occurring < 20% of the time.

A final note should be made here of the TMIn source, due to its importance to the work in this thesis. The present work focuses on both lattice-mismatched and lattice-matched epitaxy, and for the InAlGaAs alloys used in this work, changes in the lattice-constant are obtained by varying the mole-fraction of In in the films grown. This means that accurate control over the amount of In incorporated in the films grown is critical, and the main determinant of this is the TMIn flow into the reaction chamber. As mentioned above, TMIn is solid at room temperature. Essentially, the TMIn bubbler contains a large number of TMIn granules, which change in size and move around as carrier gas is flowed through the bubbler. This presents a problem in that as the source is depleted, the, the surface area of the granules exposed to the carrier gas changes. Also, their ability to

redistribute themselves means that channeling can occur, further affecting the pickup. Consequently, uniform saturation of the carrier gas does not necessarily occur, which means poor control over the TMIn flow entering the reaction chamber.

Solution-TMIn, which is marketed by EpiChem, addresses this problem by dissolving the TMIn in a proprietary solvent. However, the effects of this addition to the TMIn source on material growth are not clear, and Aixtron/Thomas Swan does not recommend its usage. We therefore rely on Epison-IIIs to monitor, and if necessary, regulate the flow of TMIn into the reaction chamber. Essentially, the Episons are real-time gas concentration monitors, which determine the composition of a binary mixture of gases by measuring the sound velocity through a specific volume of the mixture at a precisely defined temperature. The composition of the mixture is determined by interpolating between the velocities of the individual components of the mixture, and can be used in this case to tell us the concentration of TMIn in N_2. The measurement can also be used in a feedback loop, in which the Epison measurement is used to adjust the input and dilution flows on the TMIn line to obtain a desired TMIn concentration (and hence mass flow) into the reaction chamber.

While Epison control did help with pickup stability over a run, there were also run-to-run drifts that resulted in the Episons calling for markedly different carrier flow values for the same desired TMIn flow into the reaction chamber. This was the result of gradual changes in the properties of the solid-source TMIn, and started to become noticeable even when the bubbler was still ~70% full. Gently tapping the bubbler on its side before each growth helped to stabilize flows slightly (likely by causing the granules in the bubbler to settle), but clearly wasn't a long term solution. We therefore switched from a pair of "standard" Rohm & Haas TMIn bubblers to a single high-flow bubbler specially designed for solid TMIn by Akzo-Nobel. The new Hiperquad bubbler by Akzo-Nobel has not one, but four chambers holding the TMIn granules. In addition, gas flow through the bubbler is routed in a circuitous manner through each of the chambers, thereby maximizing the path length and time over which the carrier gas is exposed to the TMIn granules, thereby improving the degree of saturation of the carrier gas with TMIn. A further benefit is that the longer exposure time also leads to more stable bubbler

temperatures, as the transient carrier gas is better able to equilibrate its temperature with the contents of the bubbler.

2.1.4 Gas manifold and CCS technology

While the majority of growth occurs on the heated wafer surface in the reaction chamber, chemical reactions can also occur in the gas phase if the group-III and group-V species are mixed too early. These parasitic reactions can lead to the formation of particulates, and depending on where they form, can contaminate the internal piping of the reactor, or worse, the wafers' surfaces. They can also change the amount of reagents entering the growth chamber in unpredictable ways. They should therefore be avoided as far as possible, and the gas manifold is designed to accomplish just that.

To be precise, there are actually three sets of gas manifolds, which are termed the upper, middle, and lower manifolds, following their relative position in the gas cabinet of the reactor. All the group-V sources (AsH_3, PH_3, UDMH, and TMSb) are plumbed through the upper manifold, while all the group-III sources (TMAl, TMGa and TMIn) are plumbed through the lower manifold. Si_2H_6 (n-type dopant source for the III-V materials) is sent through the middle manifold, while DMZn (p-type dopant source for the III-V materials) is sent through the lower manifold, together with the other group-III MOs. The gas streams in the lower and middle manifold meet just before entering the reaction chamber, but are kept separate from the upper manifold gas stream until they pass through the water-cooled CCS ceiling and emerge approximately 1 cm above the wafer surface through an array of small tubes. This makes the reactor an almost-ideal cold-wall system, ensures that gas phase reactions (and thereby particulates) are kept to a minimum, and minimizes gas wastage. For similar reasons, the SiH_4 and GeH_4 are plumbed through the upper and middle manifolds, respectively, while B_2H_6 is also sent through the middle manifold. A schematic of the gas manifolds is shown in Figure 2.2.

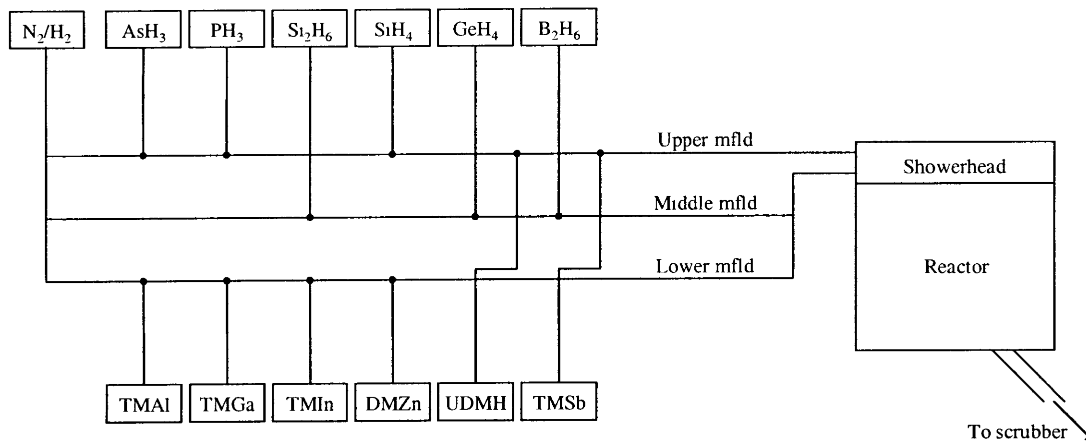


Figure 2.2 – Schematic of the gas manifold for the MOCVD.

Another upgrade that was made to the reactor was the installation of a 3-mm thick quartz deposition shield over the CCS ceiling. The array of tubes that make up the CCS is replicated in the quartz shield, so that the source gas streams stay separated until they pass through the shield. The function of the quartz shield is to further reduce the amount of material deposition that would otherwise occur on the CCS ceiling itself, which would be much harder to service/maintain (a crane would be needed for this maintenance operation). This necessitated a lowering of the rest of the components in the reaction chamber, namely the heater and the susceptor, so as to ensure that the gas flow in the reaction chamber is unaffected. We therefore had to obtain specially machined parts from Aixtron/Thomas Swan. It should be noted that the usefulness of this additional quartz shield in preventing deposition on the CCS ceiling has been established, and Aixtron/Thomas Swan has since started implementing this feature in their other reactors.

2.1.5 Scrubber

The scrubber is an abatement system to capture the toxic gases in the waste stream, most notably the hydrides, to combust them before they are released into the atmosphere. It consists of two large hoppers, each containing over 100 lbs of Calgon activated carbon impregnated with chromium and copper. During normal operation, one of the hoppers receives the exhausted waste stream from the reactor, while the other one

is either in standby, or is being regenerated through a 5-step oxidation process. The unconsumed hydrides from the reactor are chemisorbed onto the activated carbon particles, and thus removed from the exhaust that is vented into the atmosphere. After a growth, air is flowed into the hopper used during the growth, in gradually increasing amounts, which leads to the combustion of the hydrides, thereby regenerating the activated carbon. The chemisorption of hydrides onto the activated carbon surface is a fairly exothermic reactor, and from experience, PH_3 leads to the greatest amount of heat released. We note here that the reactor originally came with a 500 sccm MFC installed for the PH_3 line, but that has since been upgraded to a 1000 sccm MFC, and flowing PH_3 at that rate for extended periods of time can lead to an overtemperature condition of the scrubber.

2.1.6 Glovebox

The reactor comes with an integrated loadlock and glovebox, which helps ensure the integrity of the reaction chamber. N_2 is continuously recirculated in the glovebox, and also passes through a resin de-oxy drier that helps to remove oxygen and water vapor from the glovebox atmosphere. The dewpoint in the glovebox is typically -50°C or better. When it starts to rise beyond this value, it means that the de-oxy drier has been spent and needs to be regenerated. This is done via a timed, automated process, whereby forming gas (2% H_2, 98% N_2 mixture) is passed over the de-oxy drier while it is heated. During this time, N_2 recirculation in the glovebox is stopped, and therefore it is recommended that the regeneration be done during a period of downtime (e.g. overnight, or over a weekend).

Samples are introduced into and brought out of the glovebox through a loadlock, which can be configured to operate with an arbitrary number of pump-purge cycles. This is used to minimize the amount of atmospheric contamination introduced into the glovebox when cycling items in, and also helps to reduce the likelihood of toxic gases entering the laboratory environment. The effectiveness of the loadlock in isolating the glovebox from atmosphere (and vice versa) is a function of the number of pump-purge cycles, as well as the ultimate pressures reached during the pumping and purging stages.

In general, the amount of atmosphere that passes through the loadlock is given by the following expression

$$\left(\frac{p_{low}}{p_{high}}\right)^n \tag{2.4}$$

where p_{low} and p_{high} are the minimum and maximum loadlock pressures reached during pump-purging, and n is the number of pump-purge cycles used. As an example, the loadlock by default is configured to run two pump-purge cycles, with pressure endpoints of 100 torr and 740 torr. This means that $(100/740)^2 = 1.8\%$ of the volume of the loadlock of the lab atmosphere makes it into the glovebox each time anything is cycled into the glovebox.

2.1.7 MOCVD Operation

Generally speaking, the MOCVD reactor has two main modes of operation and four levels of user interaction. The two modes of the MOCVD reactor are "Run"" and "Unload", and the distinction is for safety purposes. In "Unload" mode, the reactor flip-top showerhead can be opened, allowing one access to the reaction chamber, but toxic gases cannot be switched on, regardless of which level of user interaction one is in. In contrast, the reactor flip-top must be shut for "Run" mode to be engaged, and in this mode toxic gases can be flowed, but the reactor lid cannot be open. It should therefore be evident that the two separate modes are to prevent the accidental discharge of toxic gases to the ambient. The four levels of user interaction are "idle", "manual", "service" and "leaktest", in increasing order of control they grant the user over the reactor. In idle mode, the reactor is in its safe state, with manifold gas purging the system, and no toxics flowing. It is from this state that one can run growth recipes, at which point the computer takes over all operation functions. "Manual" allows one to operate all valves and MFCs that can typically be activated during a growth, while "service" allows the user to bring the reactor back on-line after an incident in which it is shut down (e.g. due to lab safety interlock being tripped). Finally, "leaktest" allows the user to access the leaktest manifold is necessary after maintenance operations like MO source changes and filter replacements.

Growth operations are typically carried out by writing growth recipes, in which one specifies several things, the type of step (i.e. standard, ramp, gas switching etc.), the duration of the step, and the various settings for the different parts of the reactor. In general, these settings include heater temperature and reactor pressure, and gas flows, to tell the reactor how to set up the conditions for the growth to be carried out. Figure 2.3 is a screenshot of the EpEdit software used to write growth recipes.

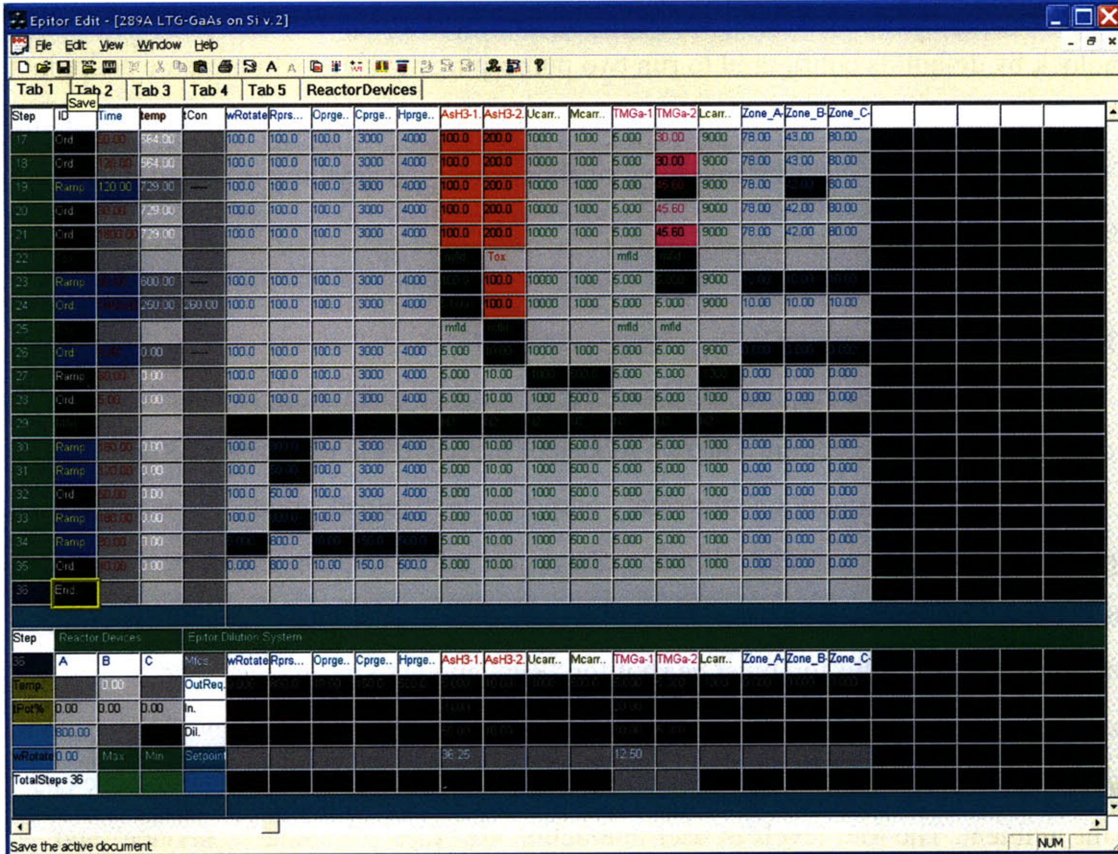


Figure 2.3 – Screenshot of EpEdit program used to write growth recipes.

Fundamentally, epitaxial growth involves bringing calculated amounts of various source materials onto a wafer surface that is heated to provide energy for the reaction. We therefore start with how the sources are brought into the reaction chamber. As mentioned in Section 2.1.2, MFCs are instruments used to control the flow of gases into the reaction chamber, and they ostensibly operate by regulating the volumetric flow of the gas, hence their units of measurement being standard cubic centimeters per minute (sccm), with the word standard meaning at 0°C (273 K) and atmospheric pressure (101.5 kPa). From the ideal gas law,

$$pV = nRT \tag{2.5}$$

and therefore

$$\frac{n}{t} = \frac{p}{RT}\frac{V}{t} = \frac{101500}{8.314 \times 273}\frac{V}{t} = 44.72\frac{V}{t} \tag{2.6}$$

Thus, the number of moles of material injected into the reaction chamber per unit time, n/t, is directly proportional to the volumetric flow rate, V/t. Thus, increasing MFC flow rates would proportionally increase the amount of material sent. This is evident for the gas sources (i.e. hydrides), but from Equation (2.2) we can see it also applies to the MOs. The only issue to consider is the presence of a secondary dilution MFC on the line, which Aixtron/Thomas Swan calls a double dilution line. Figure 2.5 shows the difference between (a) a standard source line, and (b) a double-dilution line, using the TMGa source lines as examples.

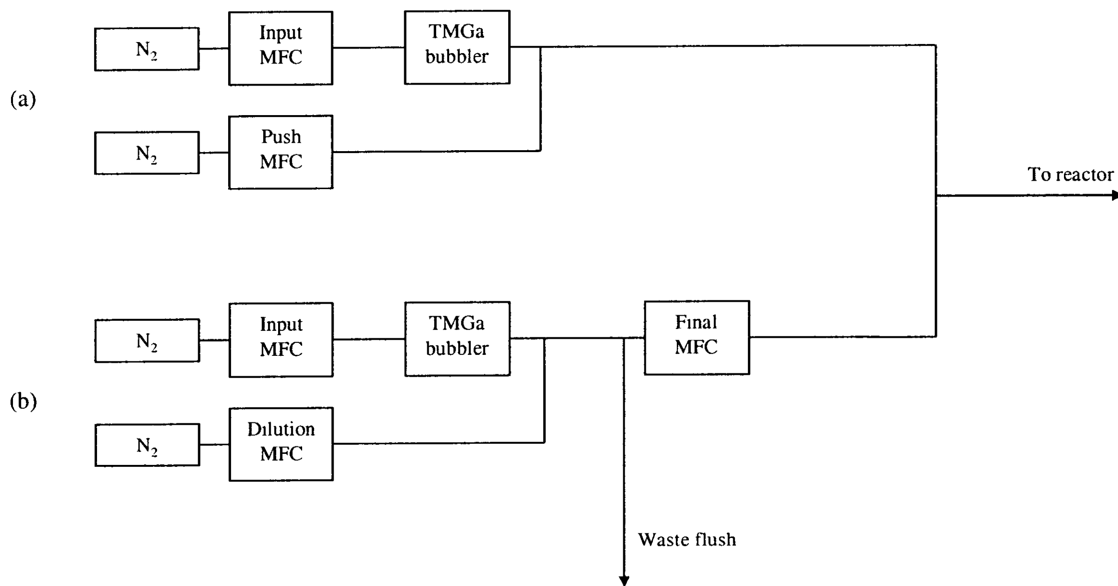


Figure 2.4 – Schematic depicting the difference between (a) a standard source line and (b) a double-dilution line.

From Figure 2.4, it is apparent that in the case of the standard source line (a), whatever amount of TMGa that is carried by the N_2 flowing through the Input MFC will enter the reactor, regardless of the setting of the Push MFC. Thus, from Equation (2.2) the amount of TMGa that enters the reaction chamber is simply

$$F_{input} \times \frac{p_{TMGa}}{\left(p_{bubbler} - p_{TMGa}\right)} \tag{2.7}$$

However, in the case of the double-dilution line (b), the amount of TMGa that ultimately enters the reactor will depend on the settings of all three MFCs (i.e. the Input, Dilution and Final MFCs). At first glance, the amount of TMGa that makes it into the reactor in this case is

$$\frac{F_{final}}{F_{input} + F_{dilution}} F_{input} \times \frac{p_{TMGa}}{\left(p_{bubbler} - p_{TMGa}\right)} \tag{2.8}$$

where F_i is the flow through MFC i, and any amount of ($F_{input} + F_{dilution}$) in excess of F_{final} will be discarded through the waste flush. Therefore it appears that for the double-dilution line, as long as $F_{final} = F_{input} + F_{dilution}$, it will behave similarly to the standard line. However, if we look closely, we will realize that just before the Final MFC, the total amount of gas is actually

$$F_{input} + F_{dilution} + \frac{p_{TMGa}}{\left(p_{bubbler} - p_{TMGa}\right)} \times F_{input} \tag{2.9}$$

and therefore the amount of TMGa actually entering the reaction chamber is

$$\frac{F_{final}}{F_{dilution} + \frac{p_{bubbler}}{\left(p_{bubbler} - p_{TMGa}\right)} \times F_{input}} F_{input} \times \frac{p_{TMGa}}{\left(p_{bubbler} - p_{TMGa}\right)} \tag{2.10}$$

It follows therefore if the vapor pressure of the MO (TMGa in this case) is significant, using the simpler Equation (2.8) for calculating the amount of TMGa that flows into the reaction chamber could result in a significant error, which is why one cannot simply equate the Input MFC flows for the two types of source lines and expect similar results. Note that this nuance only applies to MOs, since we have the carrier gas picking up an additional amount of MO vapor, whereas for the hydrides, there is no such effect. This might seem a fine point, but recall that in our work, we are concerned with accurate compositional control for lattice-matching purposes, and in our reactor, under standard operating conditions, the error might be up to 5%, which is not acceptable from a lattice-matching perspective.

2.1.8 Compositional control for In(Al)GaAs growth

We now turn to how we can accurately control the compositions and growth rates of the ternary and quaternary alloys we need for our project. As the InAlGaAs alloy is a purely mixed-cation compound, the composition of the alloy grown is therefore only dependent on the relative amounts of In, Al and Ga introduced into the reaction chamber. Furthermore, as growth of III-As is carried out under an excess As overpressure, growth rates are therefore dependent only on the total Group-III species flux. In Section 2.1.7, we have learnt how to correctly determine the amount of each component entering the reaction chamber. However, this only represents the mixture of reagents in the gas phase, and we must find some way to relate this to the composition of the solid alloy deposited. We do this semi-empirically, by using two fitting parameters, which we call the R- and G-factors. The former is used to relate the solid alloy composition to the relative source concentrations in the gas phase. The latter is then used to relate the growth rate to the total Group-III flux.

Let us consider the case of the InGaAs alloy. In the gas phase, considering only the Group-III species, the relative concentrations of In and Ga can be specified according to the partial pressures (or equivalently volumetric flows) of the source gases. If the partial pressures of TMGa and TMIn are p_{Ga} and p_{In} respectively, then in the gas phase, the relative concentrations of TMGa and TMIn are

$$\frac{p_{Ga}}{p_{Ga} + p_{In}} \tag{2.11a}$$

and

$$\frac{p_{In}}{p_{Ga} + p_{In}} \tag{2.11b}$$

respectively. We now define two R-factors, R_{Ga} and R_{In}, for the two species. The R-factors are an empirical way of capturing the differences between the sources TMGa and TMIn, in terms of their adsorption on and desorption off the wafer surface, and their pyrolysis rates. The R-factors further include information about the rates at which the pyrolyzed Ga and In species get incorporated into the epitaxial film. Thus, the R-factors are essentially supposed to take into account the ensemble rates of reaction that turn a

MO molecule in the gas phase into a Group-III atom within the III-V alloy. Empirically, we therefore obtain the following expressions for the solid compositions of the alloy

$$x_{Ga} = \frac{R_{Ga} p_{Ga}}{R_{Ga} p_{Ga} + R_{In} p_{In}} \tag{2.12a}$$

and

$$x_{In} = \frac{R_{In} p_{In}}{R_{Ga} p_{Ga} + R_{In} p_{In}} \tag{2.12b}$$

where, clearly, $x_{Ga} + x_{In} = 1$. To simplify the equations, we divide Equations (2.12a) and (2.12b) throughout by R_{Ga}, so we obtain

$$x_{Ga} = \frac{p_{Ga}}{p_{Ga} + R'_{In} p_{In}} \tag{2.13a}$$

and

$$x_{In} = \frac{R'_{In} p_{In}}{p_{Ga} + R'_{In} p_{In}} \tag{2.13b}$$

where we have defined

$$R'_{In} = \frac{R_{In}}{R_{Ga}} \tag{2.14}$$

Equations (2.13a) and (2.13b) therefore relate the concentrations of the source MOs in the gas phase to the solid alloy composition, using a single empirical factor. We can now arbitrarily define $R_{Ga} = 1$ as we are dealing in relative reaction rates, and therefore we have a single R_{In} factor. From empirical results R_{In} is not a constant, and we have found that it is best specified as a function of p_{In}/p_{Ga}, or what we call the In/Ga ratio. Thus, to determine the relationship between R_{In} and p_{In}/p_{Ga}, a calibration sample consisting of InGaAs alloys of various compositions is grown, typically by fixing the TMGa flow and varying the TMIn flow, hence varying p_{In}/p_{Ga}. XRD is then used to determine the compositions of the alloys grown, and R_{In} is obtained for the range of p_{In}/p_{Ga} calibrated. The same calibration sample can be used to determine the G-factor, which is used to relate the growth rate to the Group-III source flows. A semi-empirical equation for the growth rate, which captures most of the physical dependencies of the growth rate on various parameters [27], is

$$Growth\ rate = a_{growth}^{3} \cdot G \cdot \frac{p_{Ga} + p_{In}}{\sqrt{p_{tot}}} \cdot \left(p_{Ga} + p_{In} R_{In}\right) \tag{2.15}$$

where G is the fitting parameter, and a_{growth} is the lattice-constant of the alloy being grown. X-TEM of the calibration sample can therefore be used to determine layer thicknesses, from which growth rates of the various InGaAs alloys can be calculated, hence specifying G for a range of p_{In}/p_{Ga}. In practice, curves similar to the ones depicted in Figure 2.5 are obtained.

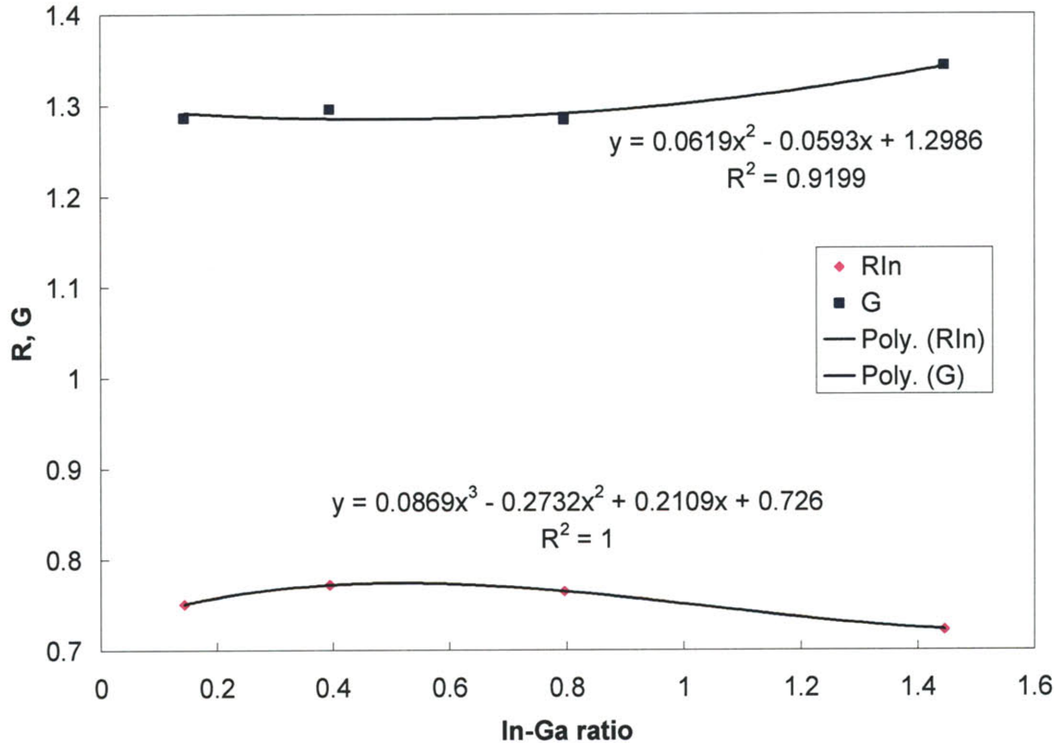


Figure 2.5 – Empirically determined values for R_{In} and G for InGaAs alloys.

It is important to note that for optimal accuracy, the range of p_{In}/p_{Ga} used for calibration should exceed, or at least equal, the range of p_{In}/p_{Ga} that is expected to be used for growth. Finally, we note that these curves are most sensitive to changes in temperature, due to differences in the ways the pyrolysis rates, sticking coefficients etc. of the various species are affected. R_{In} tends to increase with decreasing temperature, due mainly to reduced TMGa pyrolysis and In desorption from the surface, while G tends to increase with increasing temperature.

2.1.9 EpiTT – In-situ emissivity-corrected optical pyrometry

The EpiTT system installed in our MOCVD reactor can provide real-time information on the properties of the film being grown in the reactor. It does this by alternately measuring the reflectivity signal off the wafer surface at 635 nm, and detecting thermal radiation at 950 nm to determine the emissivity of the wafer, as the wafers rotate in the reaction chamber during growth. In theory, the combination of these two pieces of information allows the system to provide the "true temperature" of the wafer surface. However, it requires precise calibration and alignment of the system, such that at a specified temperature, such as the melting point of an Al-Si eutectic which is used for calibration, it reads an fixed reflectivity value. In practice, therefore, because many effects come into play, such as wafer bowing, or deposition on the susceptor affecting wafer placement on the susceptor surface, or even misalignment of the system's optics, the system cannot reliably give accurate temperature information. It is thus most useful, for our purposes, as an in-situ diagnostic tool as to the status of the wafer's surface, and occasionally as a guide to the thickness of the films being grown. For the former, it is clear that as a wafer's surface starts to roughen, the reflected signal would drop significantly, indicating that something about the growth has gone wrong. However, the fact that we often grow lattice-mismatched materials in the reactor means that wafer bow is a common occurrence, which leads to changes in reflectivity as well, complicating the interpretation of the real-time information provided by the system. As to the use of the system for film thickness measurements, during heteroepitaxy, the reflection of the 635 nm signal off a given film's growth surface and underlying interface leads to peaks and troughs in the measured reflectivity signal, and with knowledge of the film material's refractive index at 635 nm, the oscillations can provide information about growth rates, thicknesses and initiation times [31].

2.1.10 Maintenance

Lastly, a uniquely configured reactor like ours brings with it special challenges when it comes to maintenance. Standard maintenance involves the changing of MO sources, hydride cylinders, and particulate filters. These are typically carried out by operators wearing self-contained breathing apparatus (SCBA) equipment, and require the

system to be check for leak integrity after any such operation. In the course of growing in the reactor, unwanted deposition occurs in various places in the reactor, most notably on the showerhead's quartz deposition shield, the J-liner (a piece of quartz surrounding the susceptor that is molded in the form of the letter "J"), and the susceptor. These items have to be periodically removed from the reactor for etching, to remove the deposited material, and then rinsed and baked before being reinstalled. The fact that we grow many different kinds of films in the reactor, with different lattice-constants and coefficients of thermal expansion, means we are significantly more susceptible to the material flaking off, which would compromise our growths. Our maintenance intervals are therefore shortened as a result of this.

Furthermore, the multitude of materials deposited also poses another problem, that of needing to find ways to etch the chemically dissimilar materials off the equipment. We address this by using a combination of etchants, such as slightly diluted piranha (10:1:1 H_2SO_4:H_2O_2:H_2O), aqua regia (3:1 HCl:HNO_3), and hot KOH. The first two etchants are effective in etching most III-Vs and Ge, while the latter is mostly for Si. However, there is no truly effective etchant for SiGe alloys, except for a combination of CH_3COOH, HNO_3 and HF, but these reagents also rapidly attack our SiC-coated susceptors and our quartzware. We have thus sought to address this problem by trying to pre-coat the equipment with GaAs, which we know etches away easily using aqua regia. Also, we have assigned different susceptors for use with different material, for easier etching, but also to avoid cross-contamination issues. Si and Ge are rarely grown via MOCVD, and therefore in the course of our work, we have only recently discovered that Si and Ge layers are very efficient at gettering the oxygen and carbon present in the reactor. For instance, Figures 2.6 and 2.7 are SIMS scans of two growths performed consecutively in the reactor (the growth depicted in Figure 2.6 was first).

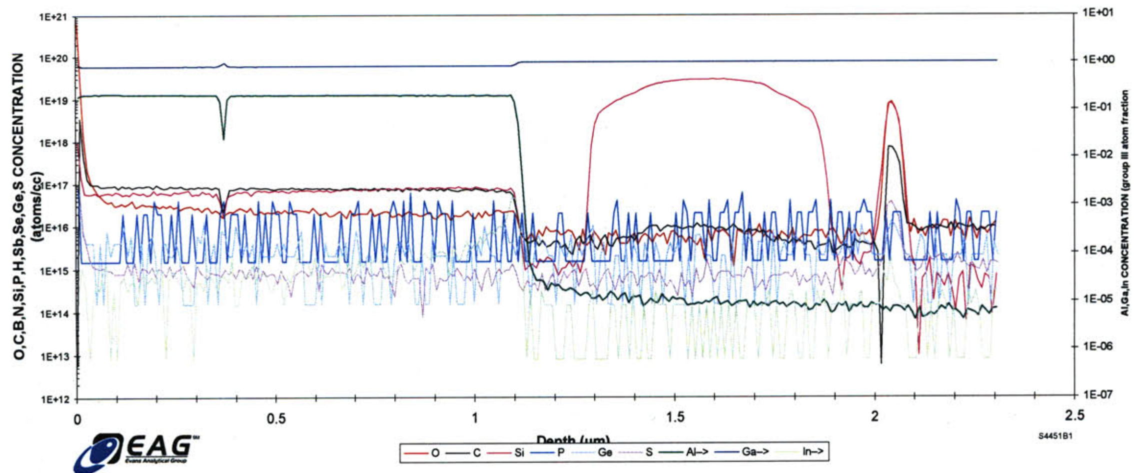


Figure 2.6 – SIMS scan of an AlGaAs/GaAs QW growth.

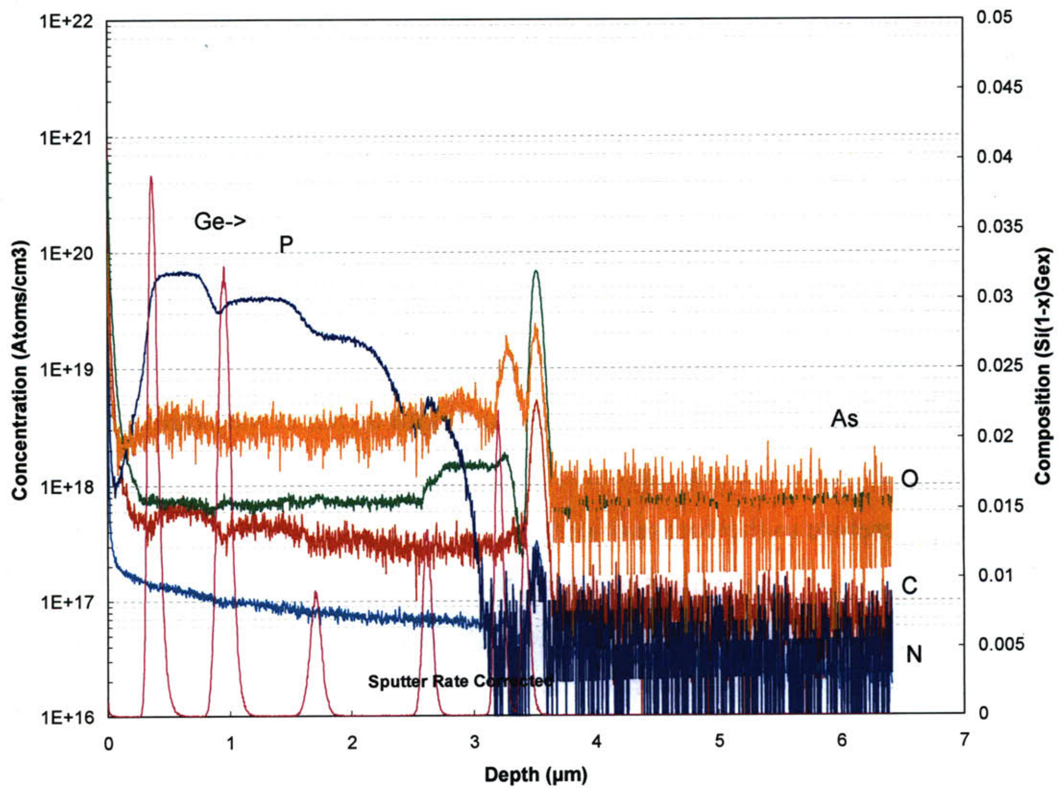


Figure 2.7 – SIMS scan of a Si doping staircase.

As can be seen, the AlGaAs/GaAs QW growth depicted in Figure 2.6 had oxygen levels in the 10^{16} cm^{-3} range, which was very respectable for an Al-containing growth. The Si doping staircase growth immediately following it, however, had oxygen levels

roughly two orders of magnitude higher. Furthermore, Ge, especially, has a very strong memory effect in the reactor, and lingers for extended periods of time, unless a bake and coat (with GaAs, for example), is performed. Sb is another species that causes contamination issues. It is commonly used as a surfactant, and therefore lingers in the reactor for extended periods of time, while modifying the properties of the wafer surfaces during growth. Furthermore, we have found Sb to drastically poison the growth rate of Si, by a factor of ~100. We have therefore addressed this issue in similar ways – by using different susceptors and dummy wafers for different growths, and by performing high temperature bakes and Si or GaAs coats as necessary to prepare the reactor for an actual growth.

A final, and most important aspect of maintenance, is that of temperature balancing. The MOCVD reactor uses a three-zone heater, so called because the heating element consists of three separate graphite coils that are installed in concentric fashion. Each thus heats the susceptor in a different region radially. The goal of temperature balancing is therefore to balance the three heaters' outputs such that the susceptor is uniformly heated in the radial direction, and this is done by measuring the surface temperature of a clean susceptor using optical pyrometry, and adjusting the relative output powers of the heaters (called zone settings), until the temperature variation across the three zones is < 1°C. This is the most important factor in ensuring uniform film growth. Due to the different thermal properties of H_2 and N_2, temperature balancing must be carried out separately for both carrier gases.

2.2 Materials characterization techniques

As mentioned at the start of this chapter, various materials characterization techniques were applied to the samples grown in the MOCVD reactor, depending on what kinds of information were sought.

2.2.1 Transmission electron microscopy (TEM)

TEM is a very powerful imaging tool for examining the microstructural details of the epitaxial films we grow. Imaging is achieved by passing a beam of high energy electrons through a sample that is thin enough so that it becomes electron transparent, and

imaging resolution on the order angstroms can be obtained, due to the short de Broglie wavelength of the electrons.

The electrons interact with the sample as they pass through it, and in the case of our crystalline semiconductor material, they are diffracted as well. Image contrast is obtained in several ways. First, different materials have different electronic structures, and they therefore interact with the electron beam differently, giving rise to what is termed "Z-contrast", where Z refers to the atomic number of the material. Second, in crystalline materials, differences in lattice-constants lead to different diffraction conditions for the electron beams, which once again show up as contrast in the TEM image. This latter effect is very powerful, as imperfections in the crystal lattice, including dislocations, displaced atoms, and other defects, would lead to a distortion of the local crystal lattice, leading to variations in the lattice-constant (or more accurately, atomic spacing) of the material in that region, and depending on the diffraction condition (i.e. the way the electron beam interrogates the sample), these features, if present, can be made to show clearly. Thus, we can obtain high resolution information on the microstructure of the material.

Both a JEOL 200CX and a JEOL 2011 were used in this work. In both cases, he electron beam was accelerated to 200 keV. Three main diffraction conditions were used in this work. The first is the g = <220> two-beam diffraction condition, which was used for enhanced dislocation contrast. The second is the g = <004> two-beam diffraction condition, which enhanced contrast due to strain, and the final diffraction condition used was directly along the <110> pole, for enhancing Z-contrast and taking lattice images.

In this thesis, two kinds TEM analysis were carried out. The first is cross-sectional TEM, or X-TEM, where small pieces of a wafer are cleaved and then stuck together facing each other using epoxy, forming a "sandwich" where the cross-sections of the wafer are revealed. The sandwich is then polished down to ~10-μm thickness, and subsequently milled from both sides to electron transparency using a Fischione Ion Mill operating between 2-4 kV (depending on the sample being milled) so that that the cross-section of the original wafer can be imaged. X-TEM allows us to examine the microstructural characteristics of the films grown, and measure layer thicknesses and

growth rates. The other analysis carried out was plan-view TEM (PV-TEM). This involved thinning the back side of a small piece of a wafer, and again milling the sample (but only from the back side) till electron transparency. PV-TEM allows us to examine the surface morphology of the samples with higher resolution than AFM, and is also used to quantify the threading dislocation densities (TDD) present in various samples.

2.2.2 X-ray diffractometry (XRD)

XRD was used extensively in this work to measure the alloy compositions and strain states of the films grown. The principle behind XRD is the use of coherent x-rays to interrogate the various crystallographic planes in a crystal. The well-defined spacing between these planes serve to provide multiple reflections for the x-ray beam. When the Bragg condition

$$\lambda = 2d \sin \theta_B \tag{2.16}$$

is satisfied, a strong x-ray signal peak results. Here, λ is the wavelength of the x-ray, θ_B is the Bragg angle, and d is the interplanar spacing for the family of planes under observation, and, for a family of planes (xyz) in a cubic crystal, is given by

$$d = \frac{a}{\sqrt{x^2 + y^2 + z^2}} \tag{2.17}$$

where a is the lattice-constant.

As pioneered by Matney and Goorski [34], by measuring the Bragg angles for the symmetric (400) and asymmetric (422) family of planes of a given film relative to a substrate, the composition and strain state of an alloy. Essentially, for a film grown on a (100) substrate, the interplanar spacing of the (422) set of planes can be resolved to provide information on the in-plane and out-of-plane lattice-constant, provided information on the tilt relative to the substrate is available. This necessitates the use of the symmetric (400) scan, which provides the necessary tilt information. Coupled with knowledge of the appropriate elastic constants (most notably the 2-D Poisson's ratio) which relate the in-plane to out-of-plane lattice-constants, the strain state of the film can be fully determined. The reader is directed to the reference above, or the thesis by McGill [35], for a more detailed description of the math. Several XRD instruments were used for this work, including a Bede D3 XRD with a Rigaku RU200 rotating Cu-anode source, a

Bruker D8 system with a sealed Cu-tube, and a Philips PANalytical X'Pert Pro XRD system, also using a sealed Cu-tube.

2.2.3 Atomic force microscopy (AFM)

Atomic force microscopy is a very useful way to characterize the surface morphology of samples over relatively large areas with nanometer-level precision. The method relies on the use of a cantilever tip that interacts with the atoms on the sample surface, leading to a force being registered by the cantilever which is then translated into an image containing information about the surface. AFMs can be operated in several modes, but the mode we used was tapping-mode AFM, in which the AFM cantilever is continuously vibrated as it is swept over a surface, and a feedback loop adjusts the height of the cantilever so that it experiences a constant force from its interaction with the surface. The most physically direct measurement is of relief, where the topology of the surface causes the cantilever tip to displace by varying amounts as it traverses across the surface. This was the data that we sought most often, as the AFM was used to quantify the surface roughness of our samples. The instrument used in this work was a Digital Instruments Dimension 3000 Nanoscope IIIa AFM.

2.2.4 Photoluminescence (PL)

PL is a very useful tool that provides information about both the electronic and optical properties of a material. In our PL measurements, light from the 514.5 nm line of an air-cooled 150 mW Ar-ion laser with a beam spot diameter of 230 μm is chopped and focused onto a sample of interest. The laser light is absorbed throughout the sample, generating large numbers of electron-hole pairs (EHP). Depending on the sample, the EHPs might recombine in the same layers where they were photogenerated, or diffuse into other regions, especially potential wells formed by materials of smaller bandgaps, where they will recombine. Both radiative and non-radiative recombination can occur, and the relative proportion of either process occurring is a function of both material quality and temperature, according to how the radiative and non-radiative lifetimes compare with each other.. Should the material be of high quality with few defects to serve as scattering centers, most of the photogenerated carriers will recombine radiatively

due to the shorter radiative recombination lifetimes as compared to non-radiative recombination lifetimes in such defect-free materials. On the other hand, defective materials exhibit far more non-radiative recombination, thus reducing PL efficiency. The PL signal is typically passed through a monochromator, which allows one to obtain PL spectra. Our setup utilizes an Acton SpectroPro 275 monochromator with ~1 nm spectral resolution. The PL signal is detected by either a Si or InGaAs photodetector (both uncooled) that is connected to a lock-in amplifier. We used PL mostly to examine the quality of QW-SCH devices that were grown. Key metrics that are examined include PL intensity, central wavelength and FWHM, though it must be noted that the measurements from our setup should be considered non-quantitative and therefore PL intensity from different scans might not be directly comparable. Our samples are also mounted in a cryochamber, and low temperature PL (down to 20 K) can be obtained as necessary.

2.2.5 Secondary ion mass spectroscopy (SIMS)

SIMS is a destructive analytical technique through with the chemical concentrations of constituent elements and contaminants alike in a material can be determined as a function of depth. It can therefore be used to determine alloy compositions and predict electronic carrier concentrations, assuming that the species under investigation has been properly calibrated for measurement. The measurement is effected by sputtering off material from the sample as individual ionized atoms (or in some cases molecules), using an ion beam. These secondary ions are detected according to their charge/mass ratio through conventional mass spectroscopy, and their relative yield is analyzed to provide information about each species' chemical concentration as a function of sputter depth. Depending on the species being measured, concentrations as low as 10^{15} cm^{-3} can be detected. In our work, SIMS was mostly carried out to determine the presence of contaminants such as oxygen and carbon in our epitaxial films, or to quantify the dopant concentrations in our various device layers.

2.2.6 Electroluminescence (EL)

EL is used to characterize our diode emitters after they were grown and fabricated. EL is essentially the injection of current into an optoelectronic device-under-

test, and measuring the light output from the device. Due to their sensitive nature, specialized laser diode drivers are used to test our emitters. Pulse testing was carried out using an ILX Lightwave LDP-3840 pulsed laser diode driver, while CW testing was done with a Newport Model 5005 laser diode driver. For our purposes, the EL signal was measured in two main ways, using an ILX Lightwave OMM-6810B optical multimeter with an ILX Lighwave OMH-6708B InGaAs power head, or via an Ando AQ6317 optical spectrum analyzer.

2.2.7 3ω thermal conductivity measurements

3ω measurements, as developed by Cahill [25, 26] for measuring the thermal conductivities of both thin films and bulk substrates, were utilized in a few experiments to quantify the thermal conductivities of our graded buffers. 40-μm wide metal lines, comprising 100 nm of Ti and 5 nm of Au were deposited onto samples to serve as heater stripes, and measurements of the 3ω signal were taken using a lock-in amplifier after the ω signal had been canceled out with the use of a differential amplifier and a balancing load resistor.

3. METAMORPHIC COMPOSITIONALLY-GRADED $In_xGa_{1-x}As$ BUFFERS

InP has long been the substrate of choice for many important device applications, such as telecommunications and high speed electronics. There is motivation to grow such devices on GaAs substrates because of the availability of larger wafer sizes and more modern wafer processing technology, which would lead to increased device yields and thereby lower costs. Doing so would naturally allow for integration of such devices with other GaAs-based technologies, and, further, would be a stepping stone towards integrating with Si/SiGe technologies as well. This has led to much work on metamorphic InP-based transistors on GaAs substrates [36]. Much work has also been devoted to InP/InGaAsP-based optoelectronic devices on GaAs using various buffer layers to form the InP virtual substrate, but, in general, material quality issues have prevented such devices from attaining similar performance to lattice-matched devices [37-39]. Even if these materials challenges are overcome, the InP/InGaAsP system is plagued by issues such as low index-contrast [40]. We propose that by utilizing the InAlGaAs alloy system at the appropriate lattice-constant, optoelectronic devices with performances comparable to or better than native InP-based devices can be obtained, if high quality virtual-substrates at the appropriate lattice-constant can be developed. For lattice-constants obtainable using $In_xGa_{1-x}As$ virtual substrates with $0.30 < x < 0.40$, (roughly 5.78-5.80 Å), the InAlGaAs alloys have electronic bandgaps ranging from 0.85 eV to almost 2 eV, suitable for optical emitters operating between 1.2-1.6 μm. From the Kramers-Krönig relationship, which relates the real and imaginary parts of the dielectric constant, we can infer from the large electronic bandgap range accessible that a commensurately broad range of optical properties (*e.g.*, refractive index) will be obtainable, which opens up many possibilities for optimizing optoelectronic device design. Indeed, Tangring *et al* and Wu *et al* have recently demonstrated promising InGaAs QW laser results on metamorphic buffers [41-43]. However, based upon XTEM micrographs that show the presence of threading dislocation segments in the device regions in that work we estimate the structures have threading dislocation densities (TDD) in the 10^7-10^8 cm^{-2} range. Thus, while defect statistics may allow for regions of limited laser performance on such graded buffers, one can realistically anticipate device variation and long-term reliability problems due to the

formation of dark line defects (DLDs), which are known to be seeded by extended defects such as threading dislocations [44, 45].

3.1 Theory of graded buffers

As alluded to above, for any substrate or virtual substrate, a key metric of quality is the threading dislocation density (TDD). TDD quantifies the dislocation density that would propagate from the substrate into subsequently-grown device layers during epitaxy, where they serve as carrier trapping sites and scattering centers. Furthermore, a TDD that translates to dislocation spacing on the order of the minority carrier diffusion length and/or carrier mean free path leads to drastically reduced minority carrier lifetimes and/or mobilities, as well as altered electronic band structures [21, 22, 46] which severely limits the performance of minority-carrier electronic and optoelectronic devices. It is for these reasons that only essentially lattice-matched layers (*i.e.*, zero to limited strain levels) are traditionally used in device design and fabrication. In contrast, for graded buffer growth, the goal is to obtain a well-relaxed, epitaxial thin film at a desired lattice-constant that is different from that of the starting substrate, while also keeping the TDD low enough to not affect subsequent device operation. Thus, the formation of dislocations at the mismatched-layer interfaces cannot be avoided and is in fact desired, as they are needed to relieve the lattice-mismatch that is intentionally incorporated. Since dislocations must terminate at a surface (or close upon themselves in the form of a dislocation loop), the strategy for bulk films is to nucleate and maintain the absolute minimum (equilibrium) TDD required to relieve the mismatch efficiently. This strategy requires the promotion of dislocation glide while minimizing dislocation nucleation. The two key variables that can be controlled during growth are the growth temperature and the rate at which strain is introduced into the film/buffer. One generally seeks to maintain the maximum growth temperature, which leads to greater dislocation glide velocity, while minimizing the strain introduction rate (mismatch/thickness/time) [18].

This is achieved by slowly varying the composition of the epitaxial film during growth, thereby adding strain to the system in a controlled manner. By doing so, one effectively "paces" the relaxation of the mismatched film, which leads to dislocation nucleation in an orderly fashion over entire volume of the graded buffer (as opposed to at

a single interface), as relatively few dislocations are needed to relax the small amount of mismatch present at any one time. Proceeding in this manner also allows for optimal "recycling" of the threads already present in the bulk substrate, which further reduces the need to nucleate new dislocations. At the same time, encouraging dislocation glide leads to the formation of longer misfit dislocations, allowing fewer misfits to relieve the same amount of mismatch, and maximizing their likelihood of gliding towards the edges and terminating there. There is a small trade-off here, however, as dislocation nucleation is also a thermally-activated process, and too high a growth temperature can lead to the formation of undesired excess dislocations.

The nucleation and glide processes effectively feed into one another. The controlled nucleation allows dislocations to glide further, by reducing the chances of two or more dislocations running into each other and interacting, which would usually lead to a pile-up of dislocations that can no longer glide and therefore would turn into threads. The longer misfits in turn mean that fewer total dislocations are needed, which should translate into fewer threads being ultimately being generated, and all of these go towards keeping TDD to a minimum.

3.2 Challenges for InGaAs graded buffers

Apart from growth temperature and strain introduction rate, there are other variables that are dependent on the materials system that is under consideration. Specific to the InGaAs material system, Quitoriano and Fitzgerald showed that preventing phase separation is critical to obtaining high quality InGaAs graded buffers, and that high temperatures can help in this regard as well, by suppressing spinodal decomposition at the growth surface [38]. However, higher temperatures can also lead to significant problems with indium desorption, as well as increased surface roughening, which can interfere with dislocation motion as well as exacerbate problems with phase separation, and thus arbitrarily high growth temperatures cannot be used. Also, while it is known that heterogeneous nucleation of dislocations at the growth surface can be precipitated by the presence of particulates and contaminants, this fact is rarely addressed directly, as it is by and large a function of the reactor's capabilities and wafer handling practices, especially

for MOCVD where there is no controlled ultra-high vacuum environment, unlike in MBE.

There has been a sizable amount of work done on $In_xGa_{1-x}As$ graded buffers through varied fabrications methods. However, many studies do not quantify the TDD via vigorous characterization methods. Nevertheless, Figure 3.1 captures some key TDD results of prior work done on $In_xGa_{1-x}As$ graded buffers for $0.2 < x < 0.5$, and plots the results we obtained in this study [38, 39, 41, 42, 47-50].

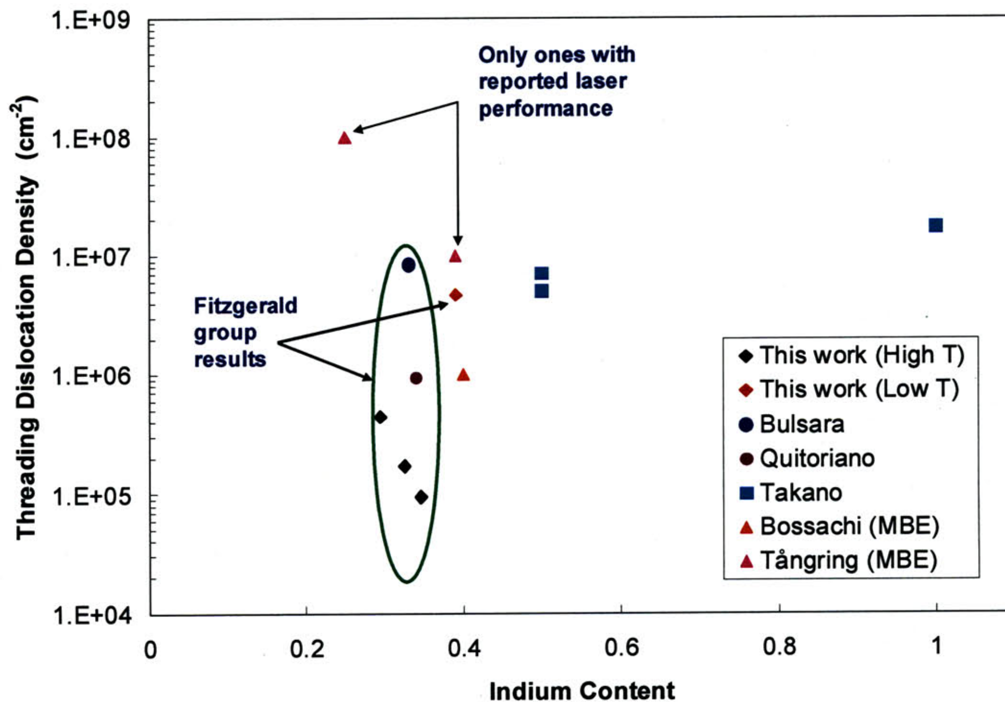


Figure 3.1 – Summary of reported TDD results for various $In_xGa_{1-z}As$ graded buffers in literature.

The results reported in this work are most comparable to the values reported by Quitoriano and Bulsara [38, 48], due to the commonality of high-temperature MOCVD growth and the use of PV-TEM for TDD determination, and we believe that the impact of improved reactor design can be studied by comparing the data in the present work with theirs. As the data in Figure 3.1 shows, there appears to be a significant improvement in graded buffer quality between this work and those of the previous authors, and the data supports the view that the improvement can largely be attributable to the new MOCVD reactor used in this work. We have advanced on the state-of-the-art TDD demonstrated

by previous work in our research group and in the field at large (excluding results that were reported without vigorous defect counting methods to support them).

In this chapter, we demonstrate the growth of high quality graded buffers with very low TDD, and the successful re-growth of device quality heterostructures on them. In this work that was carried out with a new MOCVD reactor, we also investigated how varying design and growth parameters impact graded buffer quality. Through comparison with previous work done with an older generation MOCVD reactor, we sought an understanding of how important a role reactor design plays in determining ultimate graded buffer quality.

3.3 Experiments

The compositionally-graded metamorphic $In_xGa_{1-x}As$ buffers and QW-SCH samples described in this paper were grown by low-pressure metal-organic chemical vapor deposition (MOCVD), in a fully computer-controlled 7x2" Aixtron/Thomas Swan close-coupled showerhead (CCS) configuration reactor, which was installed with an integrated loadlock and glovebox to ensure a clean environment for wafer handling. Growths were carried out at a reactor pressure of 100 Torr, using trimethylgallium (TMGa), trimethylindium (TMIn) and arsine (AsH_3) as sources. Nitrogen was used at the carrier gas at a flow rate of 20 slpm. Specified growth temperatures were taken from the wafer surface, and were determined by emissivity-corrected optical pyrometry measurements using an EpiTT system. An Aixtron/Thomas Swan Epison-III control system was used to regulate TMIn pickup, as it is a solid metal-organic precursor. For the graded buffers, linear compositional grading schemes were utilized. The grading was performed continuously through computer control, by constantly adjusting the TMIn and TMGa flows while keeping the AsH_3 flow constant. The graded buffers were grown on AXT semi-insulating epi-ready 2" GaAs substrates. Graded buffer growth was preceded by a 10-minute bake at the growth temperature under AsH_3 overpressure and deposition of a 500-nm thick GaAs homoepitaxial layer. The TMGa flow was maintained at this point, and a continuous ramp in the TMIn flow was started, until the graded buffer had reached a composition of $x_{In} = 0.15$. At this point, the TMGa flow was continuously ramped down, until the graded buffer reached its targeted terminal composition. This

ramping scheme was necessary due to the practical limits on precursor flow set by the reactor configuration. Thus, in these buffers, the growth rates varied significantly from start to finish (ranging from 3-8 Å/s), increasing during the grade to x = 0.15 as total Group-III precursor flow was increased, then decreasing thereafter. At the targeted terminal composition, 1 µm of $In_xGa_{1-x}As$ at the terminal composition was deposited, followed by a highly strained GaAs cap layer of ~15-Å thickness, to protect the wafers' surfaces. Throughout the growths, the V/III-ratio stayed within a range of 25-42.

To ascertain how well the graded buffers perform as virtual substrates for optoelectronic applications, a set of InAlAs/InAlGaAs/InGaAs QW-SCH samples was re-grown on the graded buffers with the lowest TDD after a wet surface preparation step. Prior to the re-growth, the virtual substrates were treated with a wet surface preparation procedure, with removed the protective strained-GaAs layer and a small part of the InGaAs graded buffer cap. The surface preparation entailed 1:10 HCl:DI, 1:8:80 H_2O_2:H_2SO_4:DI, and 1:10 HCl:DI dips, with DI rinses after each acid step. Finally, the virtual substrates were rinsed with isopropyl alcohol, before they were blown dry with N_2 and immediately loaded into the MOCVD reactor's glovebox. Both doped and undoped QW-SCH samples were grown. The p-dopant source was dimethylzinc (DMZn), while the n-dopant source was disilane (Si_2H_6). The InAlAs claddings and the InAlGaAs barriers were lattice-matched to the underlying graded buffer, and QWs of various compositions were grown. All re-growths were carried out at 700°C. Though reports in literature point to increased roughening of highly-strained films grown at such a high temperature [2, 35] the QWs were grown at the same temperature, in order to avoid a growth interruption.

Transmission electron microscopy (TEM) using either a JEOL 200CX or a JEOL 2011 microscope at 200 kV was performed to examine the microscopic structure of the graded buffers. Both plan-view TEM (PV-TEM) and cross-sectional TEM (X-TEM) analyses were carried out. TEM samples were prepared using mechanical lapping and polishing techniques, followed by low-angle argon-ion milling to make them electron transparent. High-resolution x-ray diffractometry (HR-XRD) using asymmetric (422) and symmetric (400) reciprocal space maps and rocking curves were carried out to obtain information about the graded buffers' composition and strain-state. The measurements

were taken using either a Bede D3 triple-axis x-ray diffractometer using a Rigaku RU200 generator operated at 60 kV and 200 mA, or a Bruker D8 machine with a LiF analyzer crystal and a sealed copper tube operating at 40 kV and 40 mA. Atomic force microscopy (AFM) measurements were also carried out on selected samples using a Digital Instruments Nanoscope III operated in tapping mode. Photoluminescence (PL) measurements used to characterize the re-grown QW-SCH samples were carried out using an air-cooled Ar-ion excitation laser emitting at 514.5 nm with a spot-size of 230 μm that was capable of variable output power up to 150 mW. The PL signal was chopped at 130 Hz and passed through an Acton SpectroPro 275 monochromator with a ~1 nm spectral resolution, before being collected either by a Si, Ge or InGaAs photodetector (all uncooled) connected to a Stanford Research Systems lock-in amplifier.

3.4 Results and Discussion

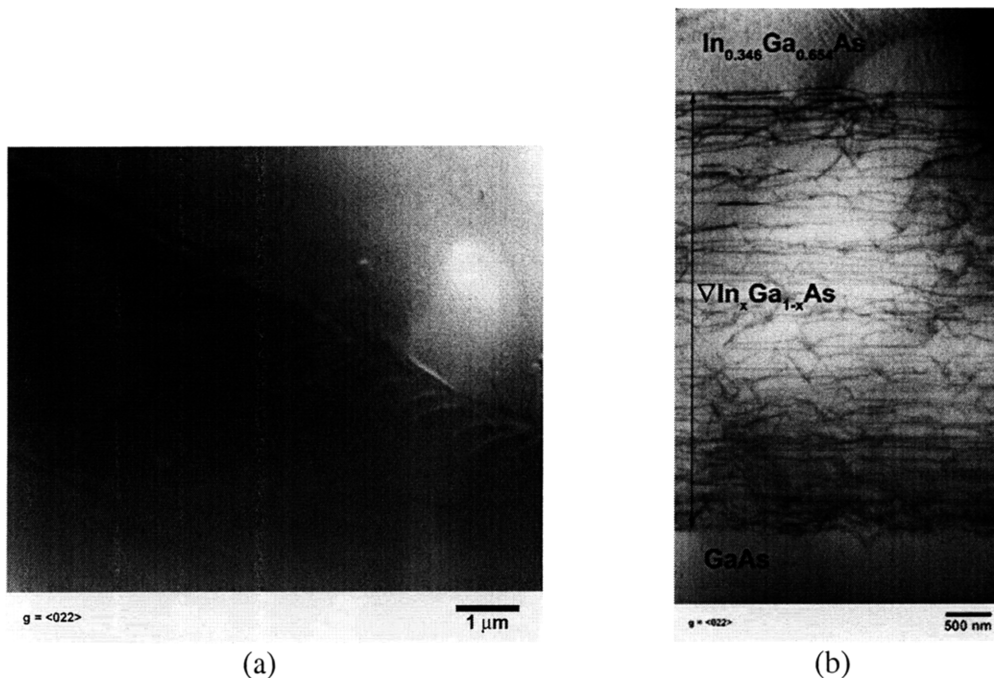
Table 3.1 summarizes the details of the various graded buffers grown.

Sample	Offcut	Terminal In mole fraction	Grade Rate (% misfit/μm)	Percent Relaxation	TDD (cm^{-2})
GB1	0°	0.346	0.51	89.2%	$< 9.5 \times 10^4$
GB2	0°	0.295	0.95	83.1%	4.4×10^5
GB3	0°	0.346	1.39	82.4%	3.8×10^7
GB4	0°	0.325	1.20-0.50	87.2%	$< 1.7 \times 10^5$
GB5	0°	0.367	0.50	87.6%	(similar to GB3)
GB6	0°	0.419	0.55	86.9%	(similar to GB3)
GB7	2°	0.377	0.58	87.7%	$> 10^8$
GB8	6°	0.399	0.55	91.0%	$> 10^8$
GB9	0°	0.391	3.28	87.7%	4.7×10^6

Table 3.1 – Summary of the various graded buffers described in this work. Offcut represents the number of degrees towards the in-plane [011] that the (100) substrate is miscut, with "0°" signifying an on-axis wafer. Terminal composition is the final indium alloy composition of the cap layer at the top of the graded buffer. Relaxation is the amount of misfit between the cap layer and the substrate that is relieved by the graded buffer. TDD is obtained from analyzing PV-TEM images, except in cases where X-TEM reveals the presence of significant numbers of threads in the cap and we establish a lower limit of 10^8 cm^{-2}.

The best result in terms of TDD was sample GB1 in Table 3.1. The final TDD of $< 9.5 \times 10^4$ cm^{-2} is, to our knowledge, the lowest ever reported for a terminal composition with such a high indium mole fraction. The stated TDD is based on sampling just over 1000 μm^2 of area in PV-TEM and not finding a single threading dislocation. Thus, the

figure represents an upper bound that was arrived at by assuming that a single thread was found within the area viewed, and the actual TDD could be significantly lower than the reported value. Despite the low TDD, the PV-TEM on this sample also revealed the presence of weak branch defects such as those shown in Figure 3.2(a), which have been shown by Kim *et al* to signal the onset of phase separation [51]. However, the degree of phase separation at this stage is likely low enough, such that it does not interfere with dislocation glide, leading to the low TDD. X-TEM of the graded buffer (shown in Figure 3.2(b)), which did have slight diffraction contrast in the cap indicative of the onset of phase separation, but is otherwise clean and free of any sign of threads, supports this observation. As is typical of metamorphic graded buffers, a cross-hatch pattern exists on the surface of the wafers, which is the result of the growth variations due to strain fields around the misfit dislocations that form along the <011> directions [52]. AFM measurements on 40 μm × 40 μm and 1 μm × 1 μm areas showed the root-mean-squared (RMS) roughness of the wafer surface to be 13.0 nm and 1.6 nm respectively. This amount of surface roughness is not expected to present too large an issue for most device applications, but chemo-mechanical polishing (CMP) can be employed if necessary to further smooth the surface.



Figures 3.2(a) and (b) – (a) PV-TEM and (b) X-TEM images of graded buffer GB1, which has a final cap composition of $In_{0.346}Ga_{0.654}As$.

3.4.1 Comparison with previous work

The lowest TDD previously reported for a graded buffer with a similar terminal composition (x = 0.34) was 9.5×10^5 cm^{-2}, by Quitoriano and Fitzgerald, who used an older generation Thomas Swan horizontal-configuration atmospheric pressure MOCVD reactor [38]. They achieved this through optimization of the growth conditions for their graded buffer, including the growth temperature, grade rate, and growth rate, and the graded buffer they obtained can therefore be assumed to possess the optimal structure for their reactor system.

We note that through the independent optimization process carried out in this work, we obtained the lowest TDD graded buffers when similar compositional profiles and process conditions were used. It is also important to note that for non-optimized graded buffers obtained on the new reactor, the TDD values rapidly approach the 10^8 cm^{-2} level, similar to what was observed in the previous work. This suggests that the improvement in graded buffer quality is to a large extent attributable to the improved growth process made possible by our new MOCVD reactor, and also that it is only after the graded buffer design and growth is optimized that the configuration of the epitaxial tool used becomes important in determining graded buffer quality. This work therefore allows us to see the contribution of the reactor design towards the TDD for the first time.

We therefore detail the key improvements brought about by our new reactor here. Firstly, the new reactor operates at low pressure (typically 100 Torr), and comes with separate gas manifolds for the Group-III and Group-V precursors, which, together with the CCS design, ensures that the two gas streams do not mix until approximately 1 cm above the wafer surface. In contrast, the older generation reactor operated at atmospheric pressure, and had a single gas manifold to handle all the source gases, which meant that the Group-III and Group-V species mixed much earlier, and traveled together for a meter or more. Therefore, parasitic gas-phase reactions, which are a potential source of particulate contamination, were drastically reduced in the new reactor, cutting down the amount of particulate contamination on the wafers' surfaces, thereby keeping heterogeneous nucleation of dislocations to a minimum. The presence of an integrated loadlock and glovebox further cuts down the amount of contamination from the

environment. Secondly, the new reactor's three-zone heater, coupled with in-situ optical pyrometry measurements afforded us excellent temperature control and uniformity over the entire wafer surface, which was critical for accurate compositional control of the lattice-mismatched films. Together with the showerhead design, which provides a more uniform distribution of reagents over the wafers' surfaces (the new reactor can accommodate up to an 8" wafer), film uniformity over large areas is improved. This results in more even strain relaxation, which helps reduce the occurrence of dislocation pile-ups. It should also be noted that based on the difference between our pyrometric temperature measurement and that of our heater thermocouple (the latter was the only temperature that could be quantified in the old reactor), we estimate that we were growing with a wafer surface temperature approximately 25-30°C higher than in previous work, which is expected to have improved the relaxation kinetics in the mismatched films. The third key difference was the ability to grow the graded buffer with a continuous grading profile, instead of grading with small, discrete steps that contained incrementally larger amounts of indium that was done in previous work [38, 48, 53]. This was enabled by the fact that the new reactor is fully computer-controlled, which allows us to continuously and controllably vary the amount of each reactant entering the reaction chamber, something that was not possible with the old reactor that was operated manually. For a given effective grade rate, continuous grading will result in the smallest amount of strain at the growth surface at any given instant, and thus in theory would lead to the minimum number of dislocations being nucleated. This, in turn, would translate would translate to optimal dislocation glide and graded buffer relaxation. We therefore believe that the order in magnitude decrease in TDD achieved was due to the interplay of all these advantages that were enabled by our new MOCVD reactor.

3.4.2 Examination of parameters affecting graded buffer quality

Various growth parameters were varied, to examine their effect on the quality of the graded buffers obtained, and to see if the reactor differences affected the trends observed. These included the compositional grading rate (measured in percentage units of misfit/μm), the terminal composition of the graded buffers, the crystallographic orientation of the substrate, and, in one experiment, the growth temperature. For the

unique experiment with different a growth temperature, a graded buffer was grown at 450°C to examine the effects of kinetically suppressing phase separation. All other graded buffers were grown at 700°C. Of the graded buffers grown at 700°C, most were grown on nominally on-axis (100) SI GaAs wafers, though several growths were carried out on wafers with varying degrees of offcut toward the [011] direction.

3.4.2.1 Effect of grading rate

As grown with a grade rate of 0.51% misfit/μm, graded buffer GB1 was approximately 4.8 μm thick. To mitigate problems that can arise due to coefficient of thermal expansion (CTE) mismatch, and for more efficient growth, it is often desirable to reduce the total thickness of the graded buffers, by increasing the grade rate. Two other graded buffers (GB2 and GB3) were grown with grade rates of 0.95% misfit/μm and 1.39% misfit/μm respectively. Figure 3.3 shows the results obtained in this study, along with results from previous work [38].

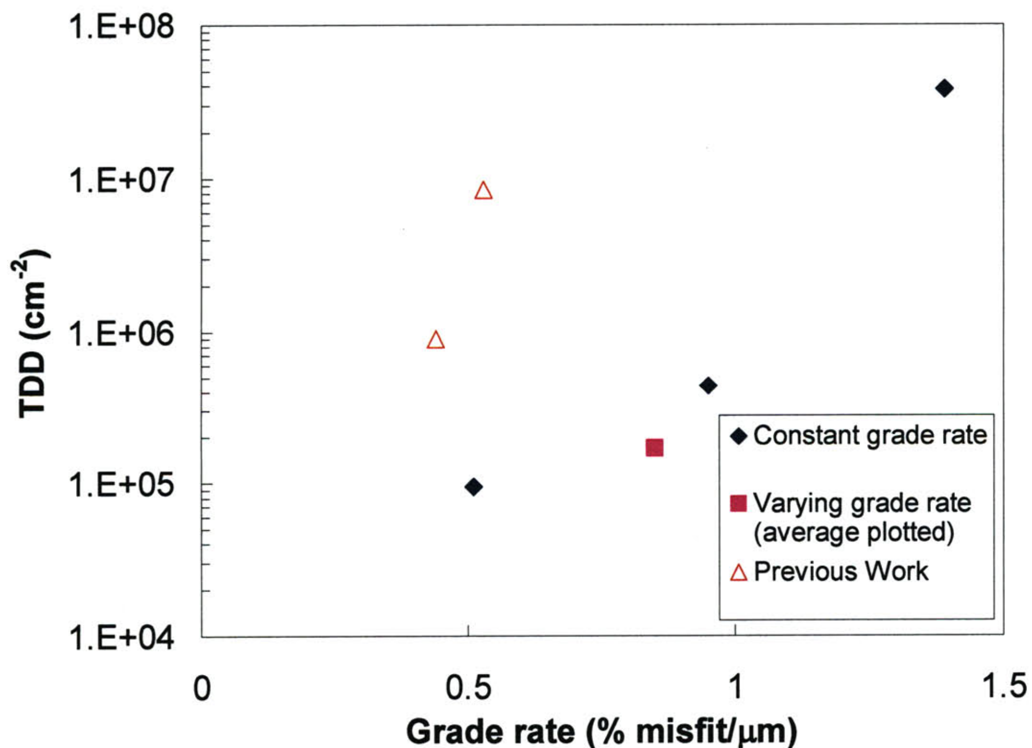


Figure 3.3 – Plot showing the TDD measured from various graded buffers. Solid symbols represent data from this work, while open symbols represent data from [38].

For sample GB2 (graded at 0.95% misfit/μm), despite it having a terminal composition of x = 0.295 (*i.e.* it was not graded out as far as sample GB1), the TDD was measured to be 4.4×10^5 cm^{-2}, which was slightly higher. The increased amounts of strain at the growth surface at any given instant would have increased the rate of dislocation nucleation, leading to an overall smaller volume for each dislocation to glide in, limiting their ability to relieve strain on a per-dislocation basis. Higher grade rates have also been shown to increase surface roughness, which also contribute to poorer dislocation glide kinetics and commensurately higher TDDs[54, 55].

Further increasing the grade rate to 1.39% misfit/μm resulted in a significantly higher TDD of 3.8×10^7 cm^{-2} for a terminal composition of x = 0.346. X-TEM revealed that the over two orders of magnitude increase in TDD as compared with the baseline case was likely the result of the presence of phase separation in the InGaAs layers of this sample, and not solely due to the increased grade rate reducing the effectiveness of the dislocations in relaxing the graded buffer, as was the case for sample GB2. In Figure 3.4, one can see an instance of a dislocation being trapped by a phase-separated region (marked by the slight contrast around the thread), leading to it stop gliding, but instead turn upwards and thread through the surface. Thus, unlike in sample GB1 where phase separation was also observed, but did not appear to cause an escalation in the TDD, the phase separation in sample GB3 was able to arrest dislocation glide. This stronger phase separation, indicative of greater compositional variation, was likely precipitated by the larger strain fields that were at the growth surface due to the faster grade rate [38, 51]. It is important to note at this point that despite the fact that the phase separation is stronger in this sample, it is limited to the top of the graded buffer and the cap, signifying that its onset was around x = ~0.34, which is similar to what was observed for graded buffer 1. This suggests that while its phase separation starts to occur at this point, its strength is a direct function of the strain fields present at the growth surface.

Figure 3.4 – X-TEM of GB3, an InGaAs graded buffer graded at a rate of 1.39% misfit/μm. Note the dislocation contrast that abruptly turns from a misfit into a thread when its glide is impeded at a phase-separated region.

To gain the benefits of thinner buffers through faster grade-rates while preserving graded buffer quality, a multiple-grade-rate grading scheme was attempted. Sample GB4 was grown with a 1.2% strain/μm grade-rate from x = 0 to x = 0.2, a 0.85% strain/μm grade rate from x = 0.2 to x = 0.25, and a 0.5% strain/μm grade-rate thereafter. Here, we took advantage of a faster grade rate initially whilst phase separation was not expected to be a concern, and slowed down the grade rate as we approached the compositions more susceptible to phase separation. This resulted in a graded buffer that was roughly 40% thinner compared with sample GB1, with similarly low TDD (again, the TDD value listed represents a upper bound, due to the absence of threads in the ~600 μm^2 area of PV-TEM images analyzed).

3.4.2.2 Effect of terminal composition

We also examined the effect of terminal composition of the graded buffer on the final TDD observed. Graded buffers GB5 and GB6 were grown under similar conditions to sample GB1, except that grading was extended to x = 0.367 and x = 0.419 respectively. X-TEMs of these graded buffers revealed the presence of several threads in

their caps, which suggested TDDs for both were similar to that observed in GB3, in the 10^7-10^8 cm^{-2} range. In both cases, signs of phase contrast were evident. For sample GB5, the contrast was only evident near the top of the graded buffer, while for sample GB6 (shown in Figure 3.5), the contrast started approximately 900 nm from the top of the graded buffer region, before becoming progressively stronger. Both of these findings are consistent with phase separation starting to become significant at $x \approx 0.35$, which deleteriously affected dislocation relaxation. We note that around the critical $x = 0.35$ composition, a roughly 2% increase in the In mole fraction leads to an increase in TDD by over two orders of magnitude, while further grading by about 5% from that point appears to not have much effect on the TDD. This is despite the fact that the phase separation appears to strengthen significantly with increasing In mole fraction, from which we would expect a commensurate increase in TDD. We surmise that while dislocation glide has been slowed, there is still enough dislocation motion for annihilation of dislocations with opposite Burgers vectors to occur, limiting the TDD.

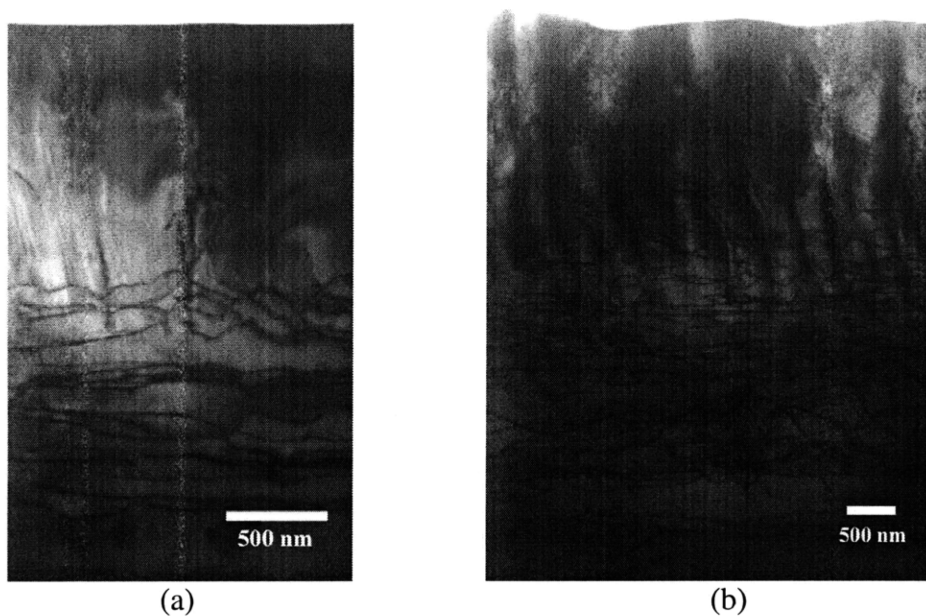
Figure 3.5 – X-TEM of graded buffer GB6. Periodic contrast characteristic of phase separation is clearly visible near the top of the graded buffer.

The fact that phase separation was observed to initiate in samples GB1, GB3, GB5 and GB6 at approximately $x = 0.35$, indicates that at 700°C, it is thermodynamically favorable for phase separation to occur at this alloy composition. However, phase

diagram calculations by Stringfellow found that the InGaAs alloy should be totally miscible across the compositional range [56] at this temperature. Quitoriano and Fitzgerald argued that this meant that the non-equilibrium surface during MOCVD growth must be the cause of the phase separation; i.e. strain fields present at the growth front drive the In and Ga segregation, with increasing strain leading to greater phase separation [38], but did not make the distinction as to whether increased strain leads to phase separation occurring earlier (i.e. for alloys with lower In content). From our results, we deduce that moderate increases in strain do not significantly affect the onset of phase separation – it is instead dominated by surface thermodynamics – but both strain and alloy composition play a role in determining the degree of phase separation once it occurs. It is also interesting to note that this composition also closely mirrors the value found by Quitoriano and Fitzgerald to be the limit for high-quality, almost phase separation-free growth. Given that the estimated wafer surface temperature during the growths was likely <675°C, this suggests that higher temperatures do not appear to be significantly suppressing spinodal decomposition at this alloy composition.

3.4.2.3 Effect of substrate orientation

Graded buffers GB7 and GB8 were grown on (100) GaAs substrate miscut 2° and 6° towards the [011] direction respectively, to investigate the impact of substrate orientation on the properties of the graded buffers. These graded buffers had a terminal composition greater than $x = 0.35$, which, as we have observed above, is the composition at which phase separation becomes significant for on-axis wafers. Thus the presence of phase separation was expected for these samples. However, the microstructural characteristics of these graded buffers on vicinal wafers were significantly different from the previous graded buffers grown on on-axis substrates. Figures 3.6(a) and (b) are X-TEM images of the graded buffers grown on wafers miscut by 2° and 6° respectively.



Figures 3.6(a) and (b) – X-TEMs of (a) sample GB7 and (b) sample GB8. The stronger phase separation contrast compared with sample GB6 despite not being graded as far appears to be the result of growing on offcut wafers. The significantly earlier onset of phase separation in GB8, and its strength, leads to large numbers of defects and high surface roughness.

As can be clearly seen, they both exhibit much stronger periodic contrast characteristic of severe phase separation towards the top of the graded regions and in the cap layers of the graded buffers, with large numbers of defects in the cap layers that signify TDD values $>10^8$ cm^{-2}. When we compare the X-TEM image of GB6 with those of GB7 and GB8, we see that despite the former being graded further out ($x = 0.419$ vs. $x = 0.377$ and 0.399 respectively), the graded buffers on vicinal substrates exhibited far more defects related to phase separation. Once again, by analyzing where the onset of the phase separation contrast is, we observe that for the graded buffer grown on the 2° offcut wafer, the starting point was at approximately $x = 0.34$, while for the 6° offcut wafer, it was much earlier, at approximately $x = 0.24$. The density of defects is therefore much higher for the graded buffer grown on the 6° offcut wafer, as the latter one-third of the graded buffer growth was carried out as phase separation problems evolved.

Thus, increasing offcut appears to increase the strength of phase separation, and, in the case of the 6° offcut wafer, brings forward the onset of phase separation significantly. It is known that whereas on-axis wafers exhibit an irregular distribution of single atomic layer steps on the surface, offcut leads to the formation of regular atomic

layer steps, with increasing offcut leading to greater step density. This fact lends itself to kinetic arguments as to why phase separation evolved differently in the offcut samples, such as modified adatom diffusivity and increased atomic-scale roughness, which might precipitate the clustering of the Group-III species. However, it does not explain why the 6° offcut wafer started to experience phase separation at such a different alloy composition, as results from graded buffers GB1-6 suggest that thermodynamic considerations at the surface dominate.

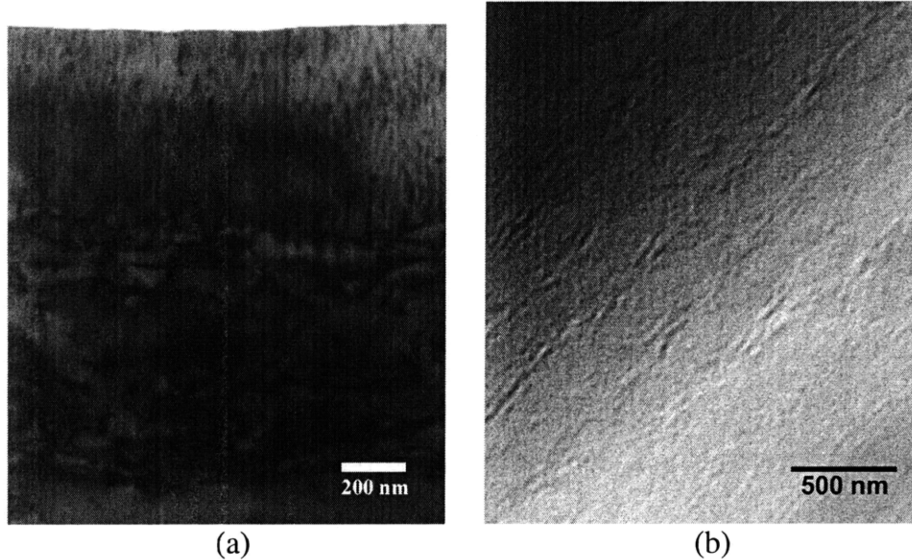
From these results, we can observe that 2° offcut wafers do increase the severity of phase separation once it occurs, but appear to be fine to work with otherwise. In fact, Takano *et al* investigated low temperature InGaAs graded buffer growth on 2° offcut wafers, and found in some cases, they resulted in lower TDD than growing on on-axis wafers [50]. More work needs to be done, however, to investigate and understand the different behavior caused by high offcut.

3.4.2.4 Effect of growth temperature

While MOCVD allows us to grow $In_xGa_{1-x}As$ graded buffers at high temperatures, groups using molecular beam epitaxy (MBE) generally have to perform InGaAs growths at temperatures of 500°C or lower, due to issues with both As- and In-desorption from the wafer surface at higher temperatures [49, 57-59]. To examine the impact of using low growth temperatures to kinetically suppress phase separation on graded buffer quality, and to compare these findings with MBE-grown results, we grew graded buffer GB9 at 450°C, to a composition of x = 0.391, with a grading rate of 3.28% misfit/μm that is similar to values used in MBE.

At x > 0.39 and a growth temperature of 450°C, the driving force for phase separation to occur should clearly be stronger than at x = 0.35 and 700°C, as we should be deeper into the miscibility gap. However, despite the much higher grading rate compared to the high-temperature-grown buffers, there appeared to be no phase separation of the kind seen in samples GB6, GB7, or GB8. Figures 3.7(a) and (b) are X-TEM and PV-TEM images of sample GB9. The X-TEM image reveals a graded buffer cap that is relatively clear of threading dislocations, and instead of the clear periodic

contrast we previously associated with phase separation, there appears to be a more subtle wavy contrast with a much shorter periodicity.



Figures 3.7(a) and (b) – (a) X-TEM and (b) PV-TEM images of sample GB9. While no threading dislocations or clear signs of phase separation are evident in the graded buffer cap, a wavy contrast can be seen, which might signify segregation of the InGaAs alloy into closely-spaced Ga-rich and In-rich regions. PV-TEM shows wavy features on the wafer surface that look like short branch defects aligned in the $[0\bar{1}1]$ direction.

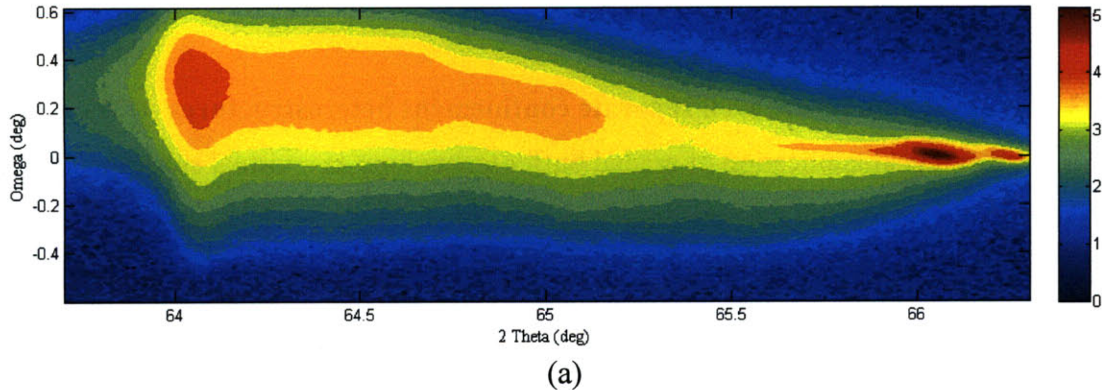
The origin of this contrast is not entirely clear, but we speculate that they could represent segregation on a shorter length-scale of the InGaAs alloy into Ga-rich and In-rich regions, due to the suppressed surface mobility of the In- and Ga-adatoms at low temperature. PV-TEM also revealed features that were not seen in other graded buffer samples. These were wavy lines somewhat akin to short branch defects aligned in the $[0\bar{1}1]$ direction, and could again be the result of reduced surface diffusivity of the In- and Ga-adatoms. The measured TDD value of 4.7×10^6 cm^{-2}, while higher than the values obtained for our optimized graded buffers grown at high temperature, is still significantly lower than the ~10^8 cm^{-2} values observed in the high temperature-grown samples that exhibited significant amounts of phase separation. This suggests that the "strength" of the branch defects in GB9, in terms of their ability to affect dislocation glide, was lower for the sample grown at 450°C. This is similar to what was previously observed by Kim *et al* in the InGaP alloy system, where lower growth temperatures increased the density of the branch defects, but appeared reduce their negative impact on

dislocation glide[51], which points to a similarity between the InGaAs and InGaP alloys systems in this respect.

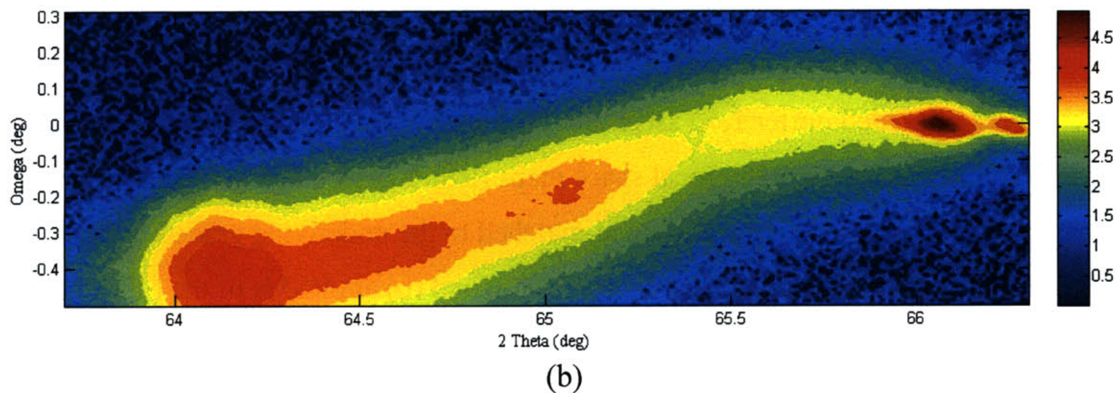
3.4.3 Re-grown quantum-well separate confinement heterostructures (QW-SCH)

For practical application of graded buffer technology as a virtual substrate, low TDD is the key factor, but the ability to re-grow successfully on graded buffers after a growth interruption is also desirable. This would mean that they can be used in identical fashion to conventional substrates, and that people who want to take advantage of the novel lattice-constants do not have to become experts in producing their own graded buffers.

In this vein, doped and undoped QW-SCH samples were re-grown on various wafer pieces of graded buffer 1, to ascertain its potential as a platform for long-wavelength light emitters. Reciprocal space maps (RSMs) taken using XRD confirmed that the QW-SCH layers were well-lattice-matched to the underlying graded buffer caps which formed the virtual substrates. Figures 3.8(a) and (b) are RSMs of the (400) family of planes of the graded buffer only, and of the re-grown QW-SCH on the graded buffer, respectively, and the respective peak widths are tabulated in Table 3.2.



(a)



(b)

Figures 3.8(a) and (b) – Symmetric (400) RSMs taken by HR-XRD of (a) the graded buffer alone, and (b) with a re-grown QW-SCH. The GaAs substrate peak is the stronger peak towards the right edge of the images (the weaker peak is the Kα2 peak), while the strong peak on the left is that of the InGaAs graded buffer cap and, in the case of (b), the QW-SCH InAlAs cladding and InAlGaAs barrier layers as well. The lack of a clear satellite peak in (b) indicates that the QW-SCH layers and the graded buffer cap are pretty well-lattice-matched.

Peak	2θ HWHM (arcsec)	ω FWHM (arcsec)
Graded buffer	250	1396
QW-SCH	228	679

Table 3.2 – Peak widths from the RSMs in Figure 7. HWHM values are reported for the 2θ widths as the presence of the graded buffer distorts the width measurement on the high-angle side.

As can be seen, the XRD peak in Figure 3.8(b) attributable to the InAlAs cladding and InAlGaAs SCH layers in the QW-SCH lines up very well with the graded buffer peak in Figure 3.8(a), confirming that the QW-SCH layers were well-lattice-matched to the underlying virtual substrate. The scans also reveal that the direction of the tilt in the films changed during the re-growth process, indicating that work-hardening took place as the temperature was cycled during the re-growth of the QW-SCH layers. The reduced ω FWHM of the peak after re-growth might also be related to this, as the temperature

cycling could have allowed to the entire graded buffer cap to relax further and attain a more uniform strain state.

X-TEMs of the heterostructures revealed that the layers were flat and even, with no threading dislocations present, attesting to the high quality of the device layers. A representative X-TEM image is shown in Figure 3.9, which is of a QW-SCH with a 210 Å $In_{0.45}Ga_{0.53}As$ QW that is under ~1% compressive strain.

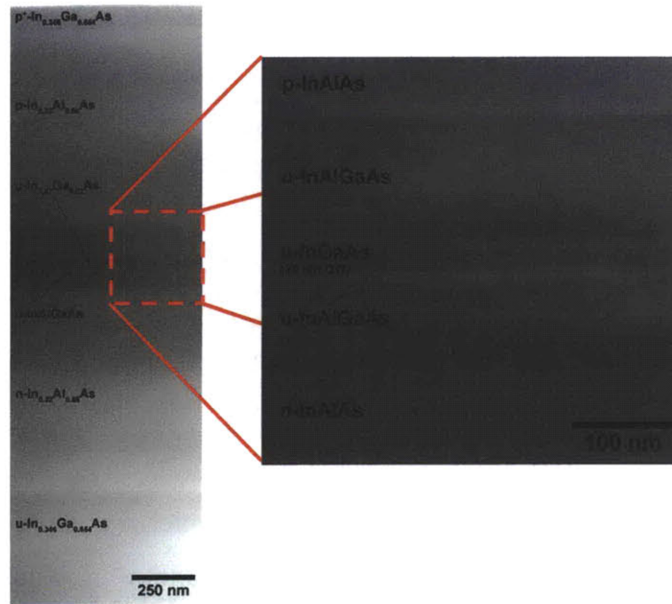


Figure 3.9 – X-TEM image of a QW-SCH. The image was taken with an on-pole diffraction condition.

Room- and low-temperature (20K) PL studies were carried out on the QW-SCH samples. Figure 3.10 shows a set of PL results taken with an excitation laser intensity of 360 Wcm^{-2} at room temperature for a series of re-grown QW-SCH samples with varying amounts of indium (and therefore strain) in the QW, ranging from mild tensile strain ($x = 0.32$) to strong compressive strain ($x = 0.49$). The latter two QW-SCH samples with the highest amounts of indium in the QW were doped, and were subjected to a wet etch to remove the heavily-doped upper cap and part of the cladding layers before PL measurements were carried out. Data for the $x = 0.32$ and $x = 0.39$ samples were taken with an uncooled Ge detector, while the other two samples were measured with an uncooled InGaAs detector.

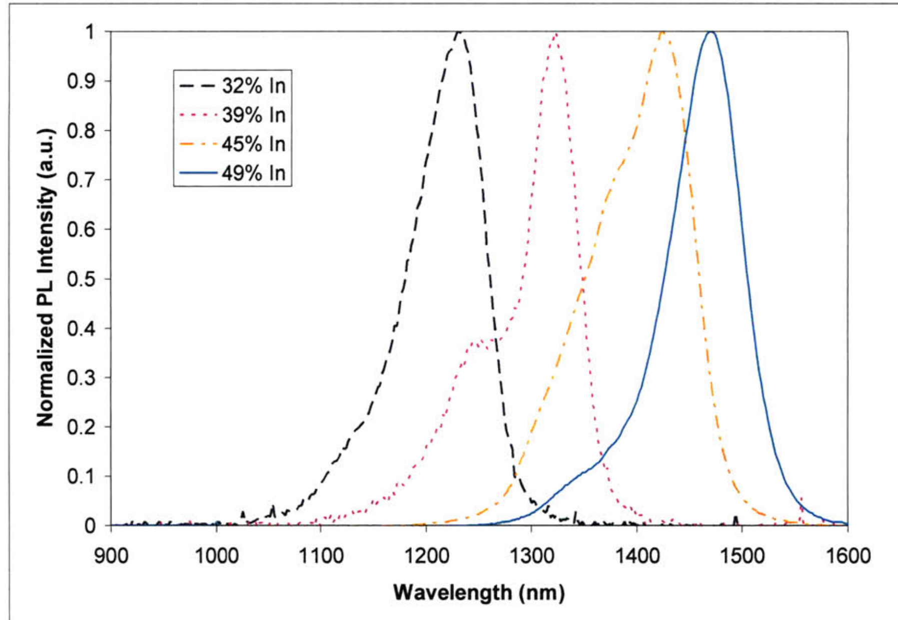


Figure 3.10 – Room-temperature PL spectra for a set of 4 different QWs (each normalized to their respective maxima) grown on the same virtual substrate platform.

As can be seen, a wide range of wavelengths from approximately 1200-1500 nm can be obtained off a single virtual substrate platform, which shows the versatility of this approach for designing and obtaining devices. FWHM for the 49% In QW was 46 meV, or roughly 1.78 kT at 300K, which suggests excellent material quality, and compares favorably with published results [59]. When the laser excitation intensity was reduced to 24 Wcm^{-2}, the FWHM narrowed to 25 meV (~1 kT). No emission was observed from the cladding or SCH layers. Clearly, without the use of the metamorphic graded buffer, efficient photoluminescence at such long wavelengths would not be possible from InGaAs QWs on GaAs substrates.

Low-temperature PL measurements (shown in Figure 3.11) were taken using both Si and InGaAs photodetectors, so as to be able to detect the emission from the cladding, SCH and QW layers.

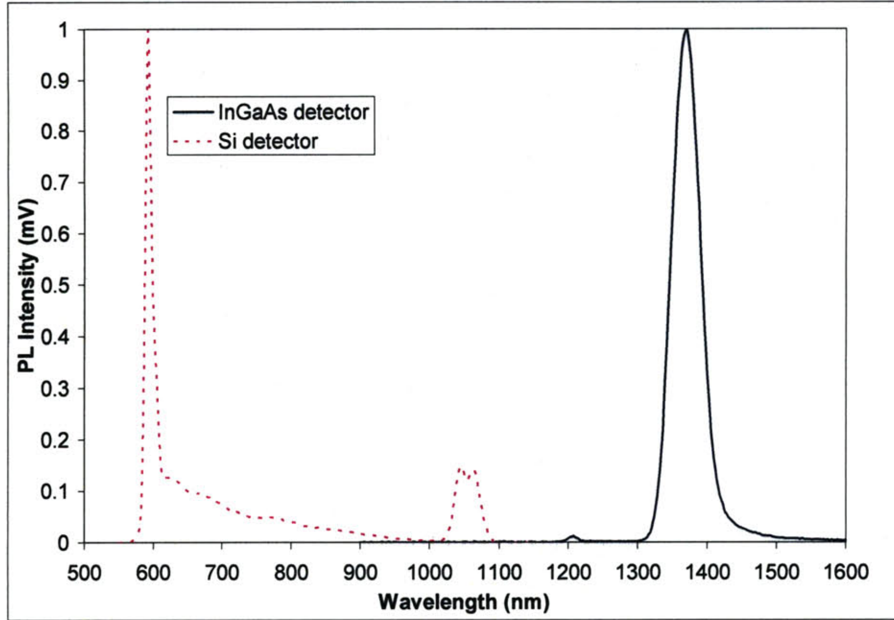


Figure 3.11 – Normalized low-temperature (20 K) PL spectra for a QW with 49% In. The Si detector was used to pick up the shorter-wavelength emission from the cladding (~595 nm) and SCH (~1050 nm) layers, while the InGaAs detector was able to pick up the emission from the SCH layers and the QW.

The results confirmed that most of the luminescence was from the QW, which signified that the layers were of high quality and did not impede carrier flow into the QW. This is evident from the lack of a clear SCH emission peak at ~1050 nm, compared with the strong QW peak at ~1370 nm, in the scan taken with the InGaAs detector.

3.5 Conclusion

We have demonstrated the growth of high-quality compositionally-graded metamorphic $In_xGa_{1-x}As$ buffers, and investigated how various growth and design parameters affect the quality of these graded buffers. The highest quality graded buffer was grown with a grade rate of 0.51% misfit/μm, to a terminal composition of $In_{0.346}Ga_{0.654}As$. The TDD for this sample was measured by PV-TEM to be $< 9.5 \times 10^4$ cm^{-2}, which will allow it to be a platform for high performance and highly reliable devices. We have found that reactor configuration plays an enabling role in obtaining the best graded buffers. We have also re-grown high quality device layers on these graded buffers, demonstrating the viability of these graded buffers as virtual substrates. QW-SCH samples re-grown on this graded buffer showed strong PL emission

from 1200-1500 nm at both room- and low-temperature, and suggest that these graded buffers can be used as platforms for novel, high-performance and high-speed optoelectronic devices.

4. METAMORPHIC InGaAs QW LASERS

In the preceding chapter, we discussed the growth and characterization of graded $In_xGa_{1-x}As$ graded buffers with very low TDD, which we have proposed can be used as high quality virtual substrates for various optoelectronic devices. In this chapter, we describe the design, growth, fabrication and characterization of metamorphic QW-SCH lasers on these virtual substrates, and show that this is a potential method by which long wavelength emission (>1.3 μm) can be obtained.

4.1 Design of the QW-SCH laser

As covered in the introduction, strained InGaAs QW-SCH lasers have been the mainstay of lasers emitting around 1 μm. In these devices that are made on GaAs substrates, AlGaAs is typically used for the cladding layers, (Al)GaAs for the barrier (SCH) layers, and InGaAs for strained-QW. For metamorphic devices on the graded InGaAs virtual substrates, the addition of In to all the layers is necessary to increase the lattice-constants of the materials, allowing them to be grown pseudomorphically on the virtual substrates.

The prototypical QW-SCH device for our work therefore utilizes InAlAs, InAlGaAs and InGaAs for he cladding, barrier and QW layers, respectively. Here, we have chosen to use the ternary InAlAs, and not the quaternary InAlGaAs, for the cladding layers, for two reasons. First, the choice is made to so as to maximize the index contrast between the cladding layers and the barrier layers, to form a waveguide with better optical confinement. Second, and more practically, as the growth of a ternary is more controllable, this will enable more reliable lattice-matching of the cladding layers to the virtual substrate. As we shall see shortly, the cladding layers will be the thickest of the device layers, and proper lattice-matching is therefore important to prevent the nucleation of more dislocations which would likely result in an increase in the TDD through the device layers.

4.1.1 Challenges in using the quaternary $In_xAl_yGa_{1-x-y}As$ alloy

There are several reasons for the additional difficulty in using quaternary alloys like $In_xAl_yGa_{1-x-y}As$ in our device. Firstly, the properties of the $In_xAl_yGa_{1-x-y}As$ layers are

largely unknown. This is because the lack of a native substrate with a suitable lattice-constant for growing these alloys means that their optical and electronic properties have to be determined through interpolations of their ternary constituents (AlGaAs, InGaAs and InAlAs), which in most cases, already represent interpolations of their respective binary constituents (GaAs, AlAs and InAs). This makes accurate knowledge or prediction of their optoelectronic properties very difficult. Secondly, uncertainties are present in the determination of the alloy compositions actually grown. In a ternary alloy such as $In_xGa_{1-x}As$, there is only one variable, x, that fully specifies the alloy composition. XRD or PL can thus be used independently to accurately establish the value of x, due to its direct relationship with lattice-constant and bandgap/emission wavelength, respectively. However, in the case of a quaternary which is defined by two variables, x and y, lattice-constants or bandgaps alone no longer specify unique alloy compositions, and a combination of both XRD and PL is required. However, this clearly requires prior knowledge of how the bandgaps and lattice-constants vary as a function of both x and y, which, as we noted earlier, is not a given.

4.1.2 Calculation of materials parameters

For this work, therefore, the first task was to set up a model that could be used to predict the optical and electronic properties of the various ternary and quaternary materials that would be used in the design of the laser. The most fundamental material parameters that we need to know for laser design are the material bandgaps, band offsets, and refractive indices. Most of the III-V materials' parameters were obtained from a comprehensive review paper by Vurgaftman *et al* [23], including bowing constants that were used to interpolate between the binary endpoints of ternary alloys. The parameters provided in this source were sufficient for calculating most of the materials' electronic properties, including strain effects. Additional parameters, necessary for predicting the optical refractive index of III-V materials using Adachi's Model Dielectric Function (MDF) model, were obtained from various papers put out by Adachi on the subject [60-62]. Where reported values differed between Vurgaftman *et al* and Adachi, the former's numbers were adopted, as they were based on a much broader survey of published

literature. Lists of the material properties and bowing constants used are tabulated in Appendix A.

In general, the materials properties of binary III-V compounds are very well known and generally agreed upon, especially for the III-As materials that are mostly used in this work. The properties of ternary alloys, however, rely on the so-named virtual crystal approximation, which assumes that properties of a given ternary are simply a proportionate average of its component binaries. The most prominent example of this relationship is Vegard's Law, which has been found to accurately describe the lattice-constant of ternary alloys. In the case of $In_xGa_{1-x}As$, it is given by

$$a_{InGaAs}(x) = x \cdot a_{InAs} + (1-x) \cdot a_{GaAs} \tag{4.1}$$

where a_i is the lattice-constant of material i, and x is the mole fraction of In in the InGaAs alloy.

However, from empirical measurements, deviations from this simple linear interpolation clearly exist, most notably in the bandgap. The reason for this has been attributed to various factors, including imperfect disorder in the mixed-cation (or anion) alloy [63], and the different physical bond lengths of the various cation-anion combinations [64]. The deviation typically takes the form of a quadratic bowing in the curve between the two binary endpoints, and results in a relationship of the form

$$T_{InGaAs}(x) = x \cdot T_{InAs} + (1-x) \cdot T_{GaAs} + x(1-x) \cdot C_T \tag{4.2}$$

where T_i is the value of a specific property (such as bandgap) of material i, C_T is the empirically determined bowing constant for parameter T, and x is again the mole fraction of In in the InGaAs alloy.

In contrast, for quaternary alloys, there is less agreement as to the best way to calculate the material properties from either its constituent binary or ternary materials. In this work, we have chosen to use the method recommended by Vurgaftman *et al*, to maintain consistency with their data. This method consists of three steps: 1) Using the interpolation of Williams *et al* [65], find the lattice-constant of the quaternary in question; 2) Find the two ternary (or, in rare cases, a binary and a ternary) endpoints that possess this lattice-constant; 3) Interpolate between the two ternary alloys to obtain the desired parameters for the quaternary. This method is expected to yield more accurate results than the direct interpolation methods of Williams *et al*, Glisson *et al* [66], and Moon *et al*

[67], as the final interpolation in step 3 is based solely on lattice-matched materials, which are theoretically expected to exhibit less bowing in the parameters.

Let us now focus on the InAlGaAs alloy which is the only quaternary that was used in this work. Figure 4.1 is a bandgap energy vs. lattice-constant diagram for this alloy, and its associated ternary curves and binary endpoints. The InP binary is also shown for reference. The black curves represent alloys that are calculated to have direct bandgaps, while the grey curves represent alloys that are indirect.

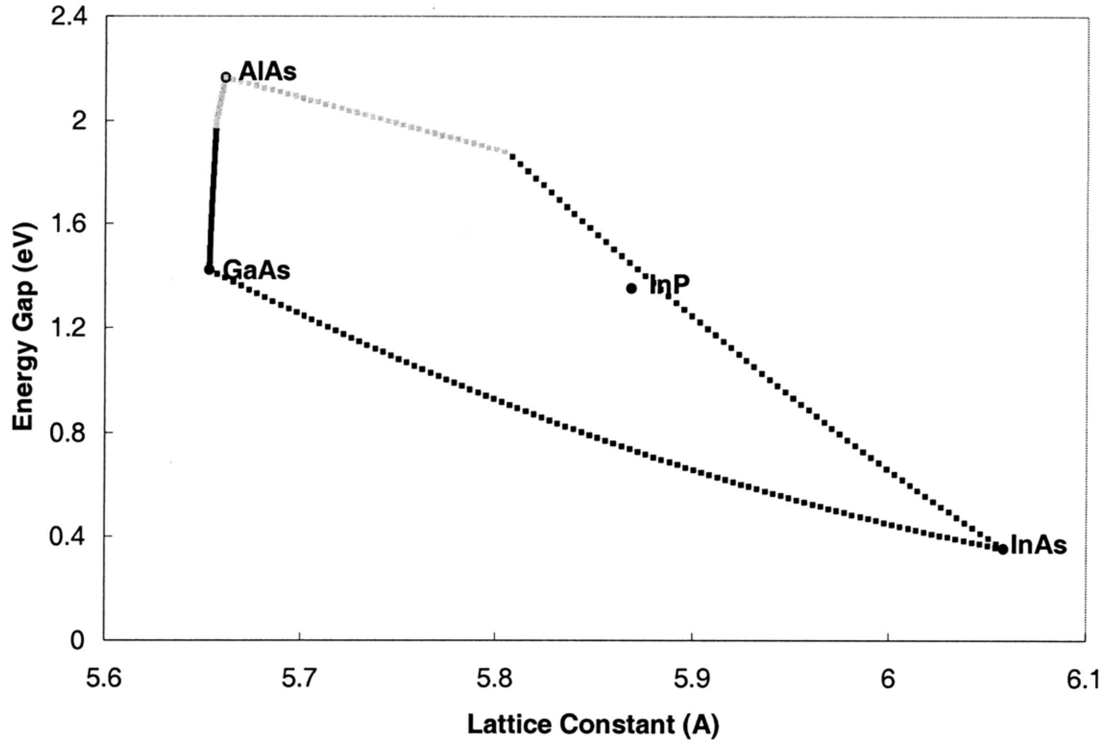


Figure 4.1 – Bandgap energy vs. lattice-constant diagram for the InAlGaAs alloy system.

Now, the lattice-constant of a given $In_xAl_yGa_{1-x-y}As$ quaternary is calculated from the following expressions

$$z = 1 - x - y \tag{4.3a}$$

$$u = (1 - x + y)/2 \tag{4.3b}$$

$$v = (1 - y + z)/2 \tag{4.3c}$$

$$w = (1 - x + z)/2 \tag{4.3d}$$

$$a_{InAlAs}(u) = u \cdot a_{AlAs} + (1 - u) \cdot a_{InAs} \tag{4.4a}$$

$$a_{AlGaAs}(v) = v \cdot a_{GaAs} + (1 - v) \cdot a_{AlAs} \tag{4.4b}$$

$$a_{InGaAs}(w) = w \cdot a_{GaAs} + (1-w) \cdot a_{InAs} \qquad (4.4c)$$

$$a_{InAlGaAs}(x, y, z) = \frac{xy \cdot a_{InAlAs}(u) + yz \cdot a_{AlGaAs}(v) + xz \cdot a_{InGaAs}(w)}{xy + yz + xz} \qquad (4.5)$$

From Figure 4.1, it is evident that for $In_xAl_yGa_{1-x-y}As$, in all cases, the lattice-matched ternary endpoint with the lower bandgap energy will be an InGaAs alloy. On the other hand, the nature of the other endpoint will depend on $a_{InAlGaAs}$; if $a_{GaAs} < a_{InAlGaAs} < a_{AlAs}$, it will be an AlGaAs alloy, while if $a_{AlAs} < a_{InAlGaAs} < a_{InAs}$, it will be an InAlAs alloy, and of course, if $a_{InAlGaAs} = a_{AlAs}$, it will be AlAs.

With this knowledge, we can find the two endpoints. The composition of the lower bandgap energy $In_xGa_{1-x}As$ endpoint would be

$$x = \frac{a_{InAlGaAs} - a_{GaAs}}{a_{InAs} - a_{GaAs}} \qquad (4.6)$$

while the higher bandgap energy alloy will be either $Al_xGa_{1-x}As$ with

$$x = \frac{a_{InAlGaAs} - a_{GaAs}}{a_{AlAs} - a_{GaAs}} \qquad (4.7a)$$

or $In_xAl_{1-x}As$ with

$$x = \frac{a_{InAlGaAs} - a_{AlAs}}{a_{InAs} - a_{AlAs}} \qquad (4.7b)$$

or AlAs.

Once the endpoints are known, interpolation between the endpoints to obtain the desired parameter for the InAlGaAs alloy can be done using the any of the cation (i.e. In, Ga or Al) mole fractions. For example, if, for an $In_xAl_yGa_{1-x-y}As$ quaternary, the lower and higher energy endpoints are found to be $In_uGa_{1-u}As$ and $In_vAl_{1-v}As$, respectively, then

$$T_{InAlGaAs}(x, y) = \frac{x-u}{v-u} \cdot T_{InGaAs}(u) + \left(\frac{v-x}{v-u}\right) \cdot T_{InAlAs}(v) \qquad (4.8)$$

where T_i is once again the parameter in question of material i. Here, we have chosen to interpolate using the In mole fraction, but identical results will be obtained if interpolation was carried out using the Ga or Al mole fractions.

From the steps detailed in this section, almost all the important parameters for any material in the InAlGaAs system can be predicted from the data tabulated in Appendix A.

Using these parameters and solving the eigenvalue equations for a QW (Equations (1.3a) and (1.3b) in this thesis), emission wavelengths for arbitrary QW-SCH designs grown on any substrate or virtual substrate can be calculated. The only other information that is important for laser design is the dielectric constant (and hence optical refractive index), for which further calculation is needed.

4.1.3 Calculation of dielectric constants using MDF

As stated earlier, the refractive indices of the InAlGaAs alloys were calculated using Adachi's MDF model. While there have been some criticisms about the physicality of the MDF model [68], and other models have been shown to fit empirical data better [68, 69], the MDF model remains one of the easiest models to use, with relatively few input parameters needed.

Essentially, it can be used to calculate the real part of the dielectric constant (i.e. the refractive index) based on critical points (CP) present in the electronic bandstructure, or more specifically, the optical joint density-of-states (JDOS), of a given material. This is because the real and imaginary parts of the dielectric constant are related by the Kramers-Kronig relation

$$\varepsilon_R - 1 = \frac{2}{\pi}\int_0^\infty \frac{\omega' \varepsilon_I}{(\omega')^2 - \omega^2} d\omega' \qquad (4.9a)$$

$$\varepsilon_I = -\frac{2}{\pi}\int_0^\infty \frac{\varepsilon_R}{(\omega')^2 - \omega^2} d\omega' \qquad (4.9b)$$

where ε_R and ε_I are both functions of the optical frequency ω', and are the real and imaginary parts of the dielectric constant, respectively. Adachi calculated the contributions of the various CPs to ε_R, which we have used to calculate the dielectric constants of our alloys. For the purposes of calculations of the refractive index used in this work, contributions to ε_R from the E_o, $E_o+\Delta_o$, E_1, $E_1+\Delta_1$, and E_2 critical points were used, and were obtained from Equations (5), (17) and (22) from reference [60]. (For the full derivations of the expressions used to describe the contributions of each CP to the dielectric constant, the reader is directed to references [60] and [62].

4.1.4 Waveguide design

As a starting point for waveguide design and optimization, we decided that the metamorphic laser growth will be carried on a graded buffer with a terminal composition of $In_{0.32}Ga_{0.68}As$, for which we were confident of obtaining TDDs of approximately 10^5 cm^{-2}. Lattice-matched $In_{0.30}Al_{0.70}As$ would therefore be used for the cladding layers, and InAlGaAs with $E_g = 1.12$ eV and $a = 5.7753$ Å was chosen for the SCH (or barrier layers), such that when used with an $In_{0.42}Ga_{0.58}As$ QW layer, a conduction band offset, ΔE_c, of approximately 120 meV, and a valence band offset, ΔE_v, of approximately 85 meV would be obtained. The analysis that follows is for the optimization of the waveguide for a single QW device.

Using Adachi's MDF framework, for a wavelength of $\lambda \approx 1310$ nm, $n_{SCH} \approx 3.66$ and $n_{clad} \approx 3.33$ for materials chosen. With these values, it was possible to solve the following eigenequation for dielectric slab waveguides [24]:

$$\alpha = k_x \tan\frac{k_x d}{2} \qquad \text{(even solution)} \tag{4.10}$$

where

$$k_x = k_o\sqrt{n_{SCH}^2 - n_{eff}^2} \tag{4.11a}$$

$$\alpha = k_o\sqrt{n_{eff}^2 - n_{clad}^2} \tag{4.11b}$$

$$d = L_{QW} + 2L_{SCH} \tag{4.11c}$$

from which the optical confinement factors in the SCH and QW could be calculated:

$$\Gamma_{SCH} \approx \left[1 + \frac{\cos^2(k_x d/2)}{(\alpha d/2)(1 + (\sin(k_x d)/k_x d))}\right]^{-1} \tag{4.12a}$$

$$\Gamma_{QW} \approx \frac{L_{QW}}{d}\Gamma_{SCH} \tag{4.12b}$$

If we now assume that the SCH layers are lossless (since they are nominally undoped), then the total loss experienced by the optical mode in the laser cavity, which is largely the sum of the losses through free-carrier absorption in the doped cladding layers (α_n and α_p) outside the SCH and the distributed mirror loss, will be given by

$$Total\ loss = (1 - \Gamma_{SCH})\frac{(\alpha_n + \alpha_p)}{2} + \alpha_m \tag{4.13}$$

where

$$\alpha_m = \frac{1}{2L}\ln\left(\frac{1}{R^2}\right) \tag{4.14}$$

is the distributed mirror loss. Here, it is assumed that the two output facets of the laser are identical, and if they are uncoated, the optical power reflection coefficient, R, is given by

$$R = \left[\frac{(n_{SCH} - 1)}{(n_{SCH} + 1)}\right]^2 \tag{4.15}$$

The condition for threshold is then obtained by equating the modal gain to the total loss, and we obtain the following expression

$$(1 - \Gamma_{SCH})\frac{(\alpha_n + \alpha_p)}{2} + \alpha_m = \Gamma_{QW} g_{th} \tag{4.16}$$

where g_{th} is the threshold gain and represents that gain value that the QW must attain to reach threshold. In general, the QW gain is a logarithmic function of the injected carrier density in the QW, which in turn is approximately linear with the injected current. Thus, to optimize the laser for low threshold operation we sought to minimize

$$g_{th} = \frac{(1 - \Gamma_{SCH})\frac{(\alpha_n + \alpha_p)}{2} + \alpha_m}{\Gamma_{QW}} \tag{4.17}$$

by adjusting the thicknesses of the SCH and the QW.

Using the above as the basis for optimization, and assuming rough estimates for internal losses ($\alpha_n = 4$ cm^{-1}, $\alpha_p = 35$ cm^{-1}), it was found that for edge-emitting lasers roughly 750 μm long, the optimal (one-sided) barrier thickness was approximately 130 nm. This formed the basis for the growths.

4.2 QW-SCH laser growth

The QW-SCH lasers described here were directly grown on InGaAs graded buffers similar to graded buffer 4 that was described in the previous chapter, with a graded buffer cap composition of $In_{0.32}Ga_{0.68}As$. Thus, for a well-lattice-matched growth, the TDD was expected to be in the low-10^5 cm^{-2} range. We maintained the 700°C growth temperature that was used for the graded buffer for the duration of the QW-SCH growth. This was to avoid the need for any growth breaks, and also to promote the growth of high

quality, oxygen-free layers. After the growth of the 1-μm graded buffer cap, a 1.6-μm thick lattice-matched n-$In_{0.3}Al_{0.7}As$ (Si-doped; n = 2 × 10^{18} cm^{-2}) lower cladding layer was grown. Based on SIMS scans of previous similar QW-SCH growths, we shut off the n-dopant during the growth of the last 50 nm of the lower cladding, as that was approximately the extent of the dopant diffusion that was previously observed. We followed this with a 70-Å thick undoped $In_{0.42}Ga_{0.58}As$ QW that was sandwiched between two 130-nm thick undoped $In_{0.3}Al_{0.07}Ga_{0.63}As$ barrier layers, the thicknesses of which were selected based on waveguide optimization process described earlier. After this, a 1-μm thick p-$In_{0.3}Al_{0.7}As$ (Zn-doped; p = 1 × 10^{18} cm^{-2}) upper cladding layer was grown. Again, taking into account the finite dopant diffusion observed in previous growths, the first 40 nm of this layer were grown without the Zn dopant. Finally, we capped the structure with a 100-nm thick p^+-$In_{0.32}Ga_{0.68}As$ layer. Throughout the QW-SCH growth, the V/III-ratio was maintained between 38-52. Figure 4.2 is an X-TEM image of the QW-SCH, shown with the top part of the graded buffer.

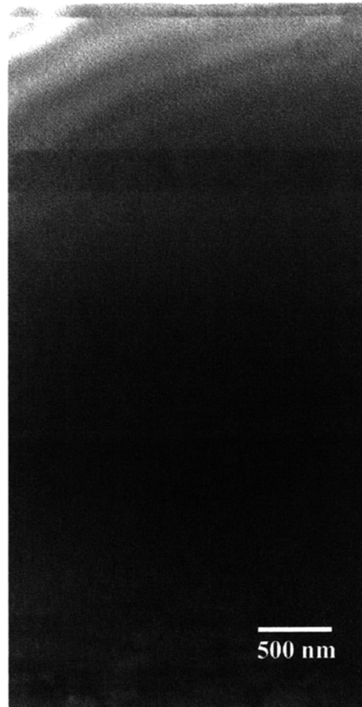


Figure 4.2 – X-TEM image of a QW-SCH grown on an InGaAs graded buffer.

As the image shows, lattice-matching was successfully carried out between the graded buffer and the QW-SCH device layers, as evidenced by the absence of any misfits

at the InGaAs/InAlAs interface, and XRD further supported this observation, Also, the QW-SCH layers were flat and free of dislocations, though some amount of surface roughness is evident. Under close observation, one can see that the surface profile approximately follows that of the top layer of misfits, suggesting that the surface roughness is likely tied to the underlying misfit network, and not due to other phenomena like 3-D growth.

Figure 4.3 contains PL spectra taken of the sample after various etch times in 1:8:80 H_2O_2:H_2SO_4:H_2O, through which progressively more of the heavily-doped p^+ cap and upper p-cladding layer were removed. The etch rate was estimated to be approximately 30-40 Å/s.

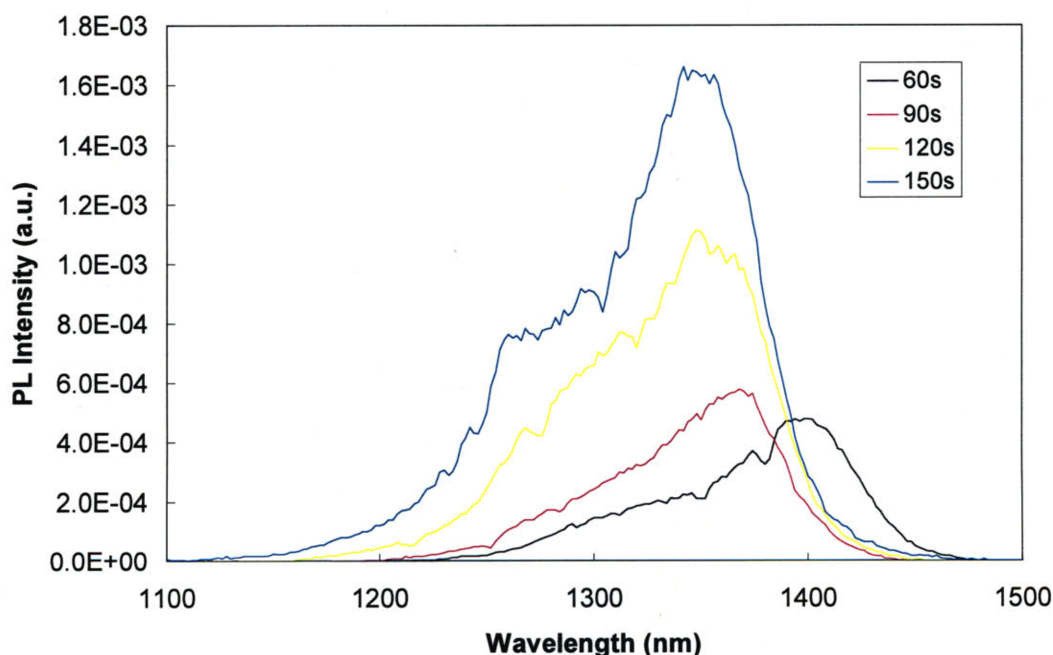


Figure 4.3 – PL spectra of the doped QW-SCH structure after various etch times.

As designed, the QW-SCH was expected to have an emission wavelength of 1330 nm. The blue-shifting of the PL peaks with increasing etch times is likely to signify the gradual removal of the highly absorbing p-doped material above the QW, as the free-carrier absorption in the layers would clearly be stronger for shorter wavelengths closer to the bandgap of the InAlAs cladding layers. Thus, as more of the cladding material is removed, the emission peak shifts closer to the expected value.

4.3 Device fabrication

After growth, the wafer was transferred into the Microsystems Technology Laboratory (MTL) cleanrooms for processing into top contact, ridge-waveguide devices. A four-mask layer process was used to achieve this. The first mask layer was used to form the ridge via wet-etching; the second layer was used to open both n- and p-contact windows; the third layer was a liftoff mask for defining the n-contacts; the fourth layer was another liftoff mask for defining the p-contacts. Standard lithography techniques were used with the first mask layer to put down a 1-μm thick photoresist mask with 100-μm wide openings. A heavily-diluted piranha etchant consisting of 1:8:80 H_2O_2:H_2SO_4:H_2O was used to etch the material in these openings down to the lower n-InAlGaAs cladding layer. The etch rate was approximately 50 Å/s. This served to allow us to make n-contacts to the lower cladding, as well as defined the ridge waveguide for the device. Due to the non-selective nature of the etchant, the etch depth was continually monitored with a profilometer, with a target of approximately 1.6 μm, so as to ensure that we had indeed reached the lower cladding layer, but also that there remained sufficient material so that lateral current diffusion in the layer would not be affected. A 3000-Å thick SiO_2 mask was subsequently deposited using plasma-enhanced chemical vapor deposition (PECVD). After lithography, buffered oxide etchant was used to open contact windows in the oxide mask. The n-contacts were uniformly 40 μm wide, while the p-contact openings ranged from 3 to 20 μm in width. A standard liftoff process using the third mask level was performed to define the metal contacts to the n-InAlAs cladding. The n-contact metallurgy used was 3000 Å of 88:12 Au:Ge eutectic alloy. RTA at 425°C for 30 s was carried out to fully form the contact. Another liftoff process was then used to put down the p-contact metals, which consisted of 100 Å Ti, 200 Å Pt, and 3000 Å Au. A schematic of the finished device is shown in Figure 4.4.

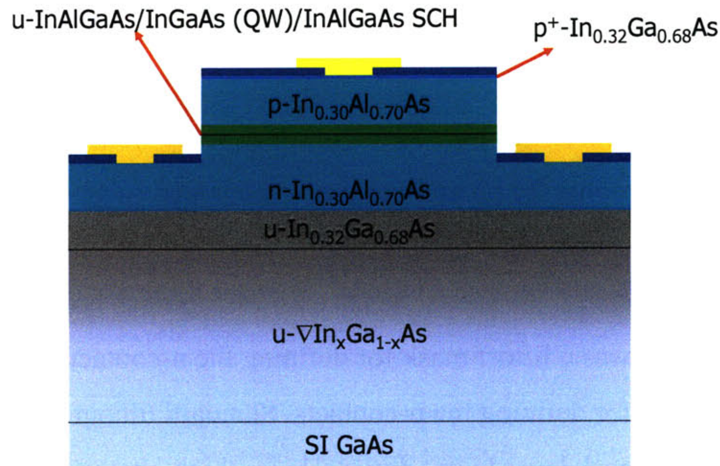


Figure 4.4 – Schematic of a processed ridge-waveguide QW-SCH device.

As grown and processed, the total thickness of the wafer was approximately 360 μm. The processed wafer was then cleaved into several portions, which we will define for identification. Piece 1 was left as is, and was tested without being thinned down or polished. Piece 2 was mechanically polished, using an automatic rotating turntable polisher and sandpaper with varying grades of sandpaper with different grit sizes. While the intention was to thin this sample down to 100 μm thickness (and polish it at the end), measurements after the polishing was done found that the sample had been thinned down to approximately 60 μm instead. It was decided at this point that subsequent samples would be thinned and polished by hand instead. Piece 3 was polished by hand, without undergoing any thinning, and Piece 4 was thinned down by hand to approximately 200 μm, followed by polishing. It should be noted that the quality of the pieces likely varied, in terms of their material quality and "processing" standard. This was because each piece was tested more or less sequentially, as different methods of thinning/polishing/heatsinking the devices were tried. Thus, the first two pieces were the "most prime" of the original wafer real estate (i.e. they came from the center of the wafer), while the third was from the portion of the wafer that had experienced some issues during the liftoff processes used to generate the metal contacts. And finally, Piece 4 was actually from a smaller, piece of the wafer that had broken off the edge of the main wafer during processing, and was therefore processed separately, but at the same time. It also had relatively limited area with good metal contacts.

4.4 Device testing and results

To test a given piece, we cleaved off bars of different lengths, by scribing the back of the wafer with a diamond-tipped scribe, then mechanically applying a force to the top of the wafer opposite the scribe mark until cleavage occurred. Devices away from the scribed and "mechanically deformed" regions were tested as far as possible. Devices of various widths were tested, and where stated, the widths refer to the sizes of the p-contact openings in the SiO_2 mask layer. It should be noted that the nominal ridge widths of the devices were 100 μm, based on mask dimensions. All devices were had uncoated, as-cleaved facets, and thus the power measurements reported are for single-sided output. The devices were tested electrically by mounting them p-side up on a thermoelectric cooler (TEC). Multiple ways of thermally contacting the devices to the TEC surface were used, and will be described in the text as appropriate. The devices were tested under both pulsed and CW conditions, using an ILX Lightwave LDP-3840 pulsed laser diode driver for the former and a Newport Model 5005 laser diode driver for the latter. Optical power output was measured using an ILX Lightwave OMM-6810B optical multimeter coupled with an ILX Lightwave OMH-6708B InGaAs power head. Optical spectra were measured using an Ando AQ6317 optical spectrum analyzer (OSA). Light from the device under test was coupled into a graded-index fiber through an aspheric lens, and sent into the OSA. Lasing from devices ranging from 1-3 mm in length was observed under pulsed testing conditions up to 10% duty-cycle (limited by the pulsed diode driver) at room temperature, but no devices were observed to lase under CW injection at any temperature obtainable with the TEC.

4.4.1 CW L-I-V testing

Figure 4.5 shows the L-I-V curves for a representative 8 μm wide and 2129 μm long device. This was a device from the wafer piece that was neither thinned nor polished, and was directly set onto the TEC surface.

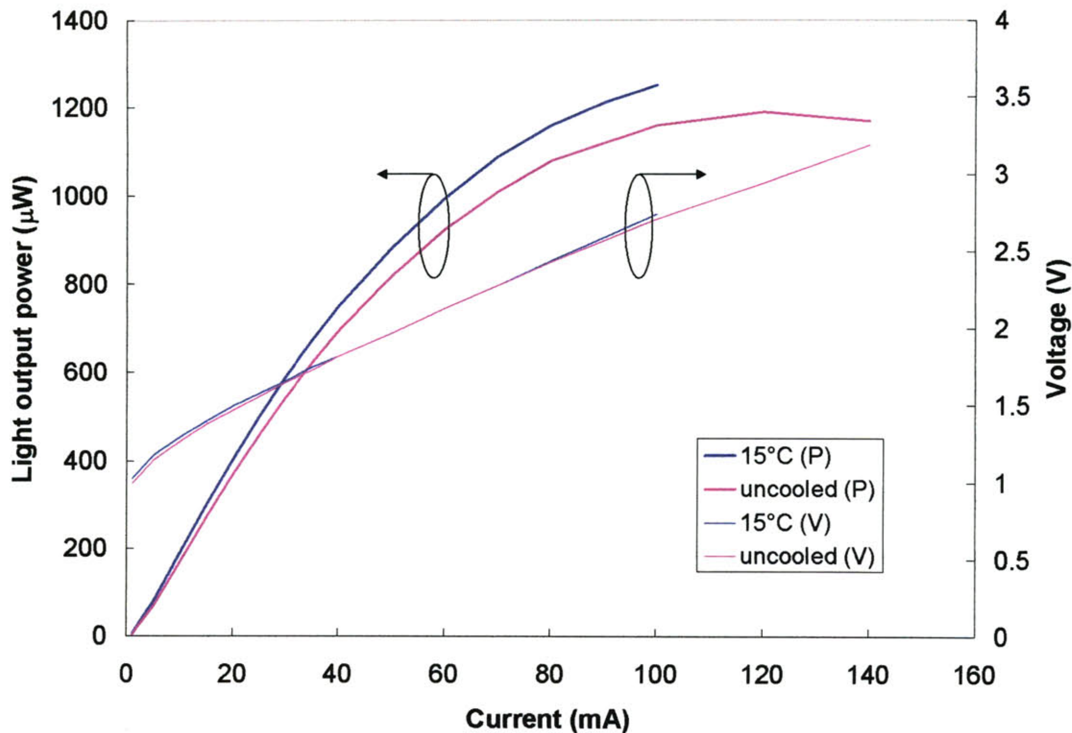


Figure 4.5 – L-I-V curves for an 8 μm wide, 2129 μm long device, tested under CW conditions. Emission was centered around 1330 nm.

As can be seen lasing, only spontaneous diode emission was obtained. The differential series resistance (DSR) measured was approximately 15.4 Ω. For a device with a 20 μm width and a similar length, the DSR was 9 Ω. This suggests that the actual cross-sectional area, in terms of current flow through the device, might be different (i.e. larger) than that of the width opening. If we assume equal amounts of lateral current spreading in both devices, to obtain equal resistivities through the device layers, the amount of total lateral current spreading is approximately 8.8 μm, which would lead to effective device widths of 16.8 μm and 28.8 μm for the 8 μm and 20 μm wide devices, respectively. It is also apparent that there is relatively little difference between the data taken when the sample was uncooled (i.e. the TEC was off – with no heat load, the TEC stayed around 22.5°C), and when the TEC was set to 15°C. This indicates that as-tested without thinning/polishing, and simply mounted on the TEC, there is large thermal resistance between the sample and the TEC, and heat cannot be removed effectively from the device.

At this point, we tried a couple of bars from Piece 2, which had been thinned to ~60 μm. The results (not shown) were actually significantly worse than the results obtained from Piece 1, which we attribute to us having damaged the device material by polishing it down too much. This likely either occurred during the mechanical grinding/polishing process, or when we brought the probe tips onto the sample surface and pressed down to make good electrical contact. For such thin samples, wafer bow was actually fairly obvious, in that when a bar was simply laid on the TEC, an obvious gap between the TEC surface and the back of the bar was seen.

We also attempted to improve the thermal contact between the bars and the TEC by placing a thin sheet of In foil, which is highly malleable, between the bars and the TEC, for bars from both Piece 1 and Piece 2. No improvements in performance were noted in either case, and the only consistent trend was that devices from Piece 2 all had significantly poorer performances than similar devices from Piece 1. Using bars from Piece 3, together with the In foil, led to similar performances to the results obtained from Piece 1. As the difference was so slight, we could not really form any significant conclusions, since, as we noted earlier, the contacts of the bars from Piece 3 were clearly inferior to those from Pieces 1 and 2.

Finally, we used a Ga-Sn solder as interface material to try to improve the thermal contact between the devices and the TEC. However, to avoid contaminating the TEC, the bars in this case were mounted with the Ga-Sn solder onto 2-mm thick copper blanks, which were then pressed firmly down onto In foil that was placed on the TEC. This was done with several old bars from Piece 1 (the bars had been cleaved and simply stored in wafer carriers left out in the room for at least 3-4 months) and new bars from Piece 4. Figure 4.6 shows the L-I-V curves for a device at 15°C from Piece 4 taken using the Ga-Sn solder, and a device with similar dimensions from Piece 1 that was previously taken simply by placing the bar on the TEC. This was done because this was one of the few good devices from Piece 4, but the only bar from Piece 1 that had similar dimensions to this was damaged during testing, due to the Ga-Sn solder creeping out from under the bar and onto the lasers' facets.

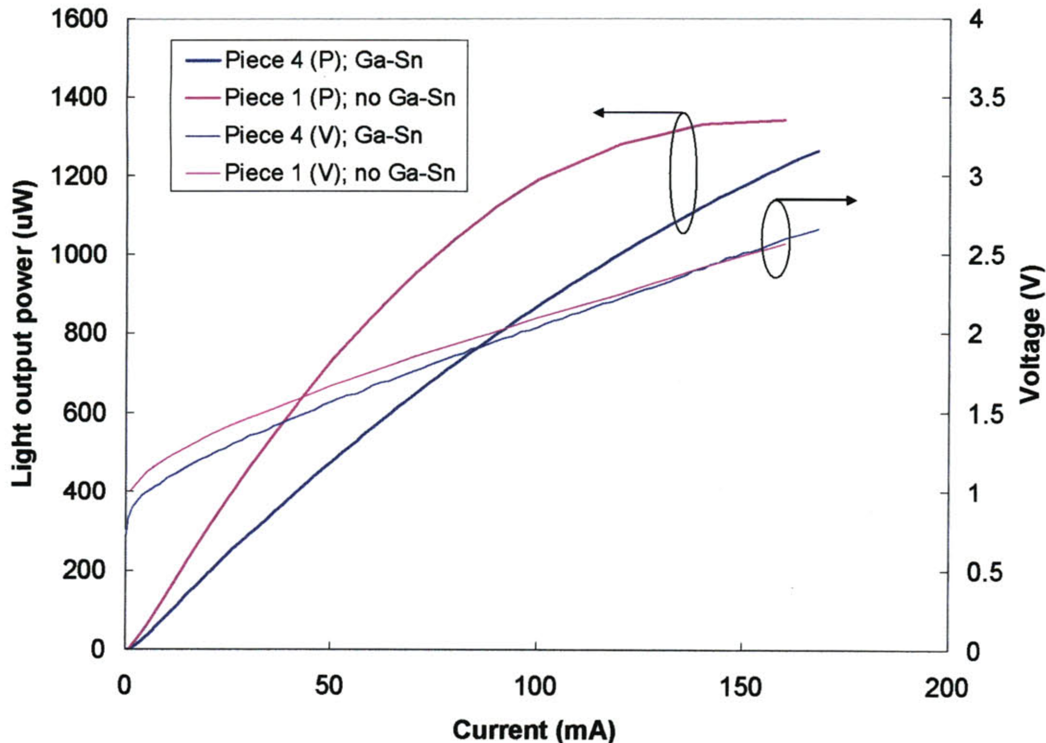


Figure 4.6 – L-I-V curves for a 20 μm wide, 2129 μm long device from Piece 1, and a 20 μm wide, 2206 μm long device from Piece 4, tested under CW conditions. The device from Piece 1 was tested previously without any interfacial material, while the one from Piece 4 was tested with the Ga-Sn solder. Emission was centered around 1330 nm.

Here, it seemed like in terms of preventing output power rollover, the Ga-Sn solder did help, which suggested that it did help in heat removal, but the overall performance of the Piece 4 device was poorer, which is likely due to the difference in device quality between the pieces. A random sampling of devices from other bars from Piece 1 failed to show a clear sign of improved performance with the Ga-Sn solder as well.

Thus, no lasing was observed under CW testing conditions, at all temperatures down to 15°C. The inability to properly heatsink the devices, which can be due to a couple of reasons, appears to be a possible explanation for this. First, the graded buffer is expected to possess poor thermal conductivities, because it comprises ternary InGaAs alloys which have significantly lower thermal conductivities than elemental and binary semiconductors [ioffe]. Second, the residual strain in the graded buffer leads to finite amounts of wafer bow, which results in non-ideal physical contact between the cleaved device bars and the TEC surface. However, as we will see from the examination of the

threshold current's temperature dependence during pulsed testing, the lack of CW lasing operation is likely also due to poor carrier confinement issues.

4.4.2 Pulsed L-I-V testing

While no lasing was observed from CW driven devices, the same devices, under pulse testing up to the 10% duty-cycle limit of the ILX Lightwave pulsed laser diode driver, did exhibit laser action, though on a time-averaged power basis, a fairly significant rollover in the output powers was observed as duty-cycle was increased. Figure 4.7 is shows the L-I curves for varying duty-cycles that were obtained for the same 20 μm wide and 2129 μm long device from Piece 1 that was used to produce the CW measurement shown in Figure 4.6. The performance of this device was representative of the devices from Piece 1. The bar was directly placed on the TEC at 15°C.

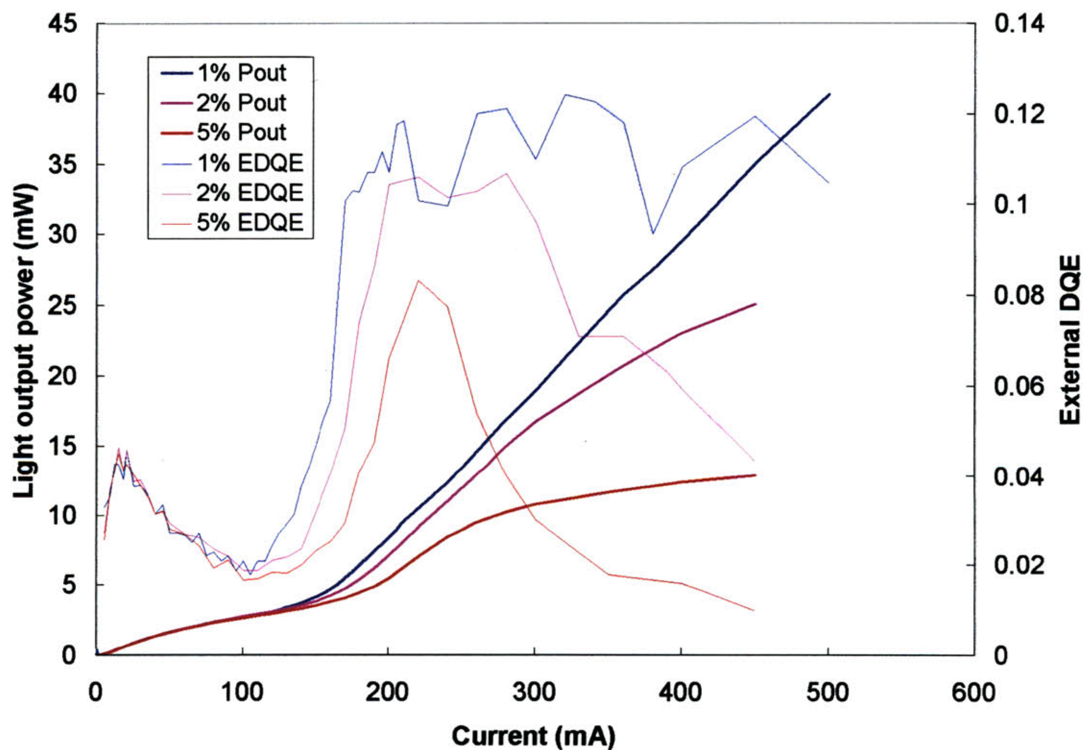


Figure 4.7 – L-I curves for a 20 μm wide, 2129 μm long device from Piece 1, tested at various duty-cycles. The external DQE has also been calculated and plotted.

At 1% duty-cycle (10 kHz repetition rate), the threshold current was approximately 112 mA, corresponding to a threshold current density of 262 Acm^{-2}, assuming a device width of 20 μm. If, however, we assume the width to be 28.8 μm, which was estimated above to be the case if lateral current spreading is taken into account, then the threshold current density is approximately 182 Acm^{-2}, which compares favorably with published results [43]. The external differential quantum efficiency (DQE) is defined as [24]

$$\eta_e = \frac{dP_{out}/dI}{\hbar\omega/q} \tag{4.18}$$

where P_{out} and I are the light output power and current, and $\hbar\omega/q$ is the photon energy of the emitted light, and it was calculated and plotted in Figure 4.7 as well. It is related to the mirror and internal cavity losses of the device, as well as the internal quantum efficiency

$$\eta_e = \eta_i \frac{\alpha_m}{\alpha_m + \alpha_i} = \eta_i \frac{\frac{1}{2L}\ln\left(\frac{1}{R^2}\right)}{\frac{1}{2L}\ln\left(\frac{1}{R^2}\right) + \alpha_i} \tag{4.19}$$

The peak external DQE at 1% duty-cycle was about 12.5%, while the slope efficiency was approximately 0.1 W/A. Varying the duty-cycle, the time-averaged light output power (assuming a square waveform) was found to decrease from ~40 mW at 0.1% duty-cycle to ~10 mW at 10% duty-cycle, while the threshold current density increased from 262 Acm^{-2} at 1% duty-cycle to 305 Acm^{-2} at 10% duty-cycle.

4.4.3 Pulsed temperature studies

The temperature-dependent performances of the devices were measured using devices from Piece 4, with Ga-Sn used for heatsinking, as the thinned and polished devices, coupled with the Ga-Sn solder, were expected to allow for the best thermal conduction from the TEC to the devices' active regions, for accurate temperature studies. Figure 4.8 shows a series of L-I curves taken with a 2% duty-cycle for a 1201 μm long and 14 μm wide device.

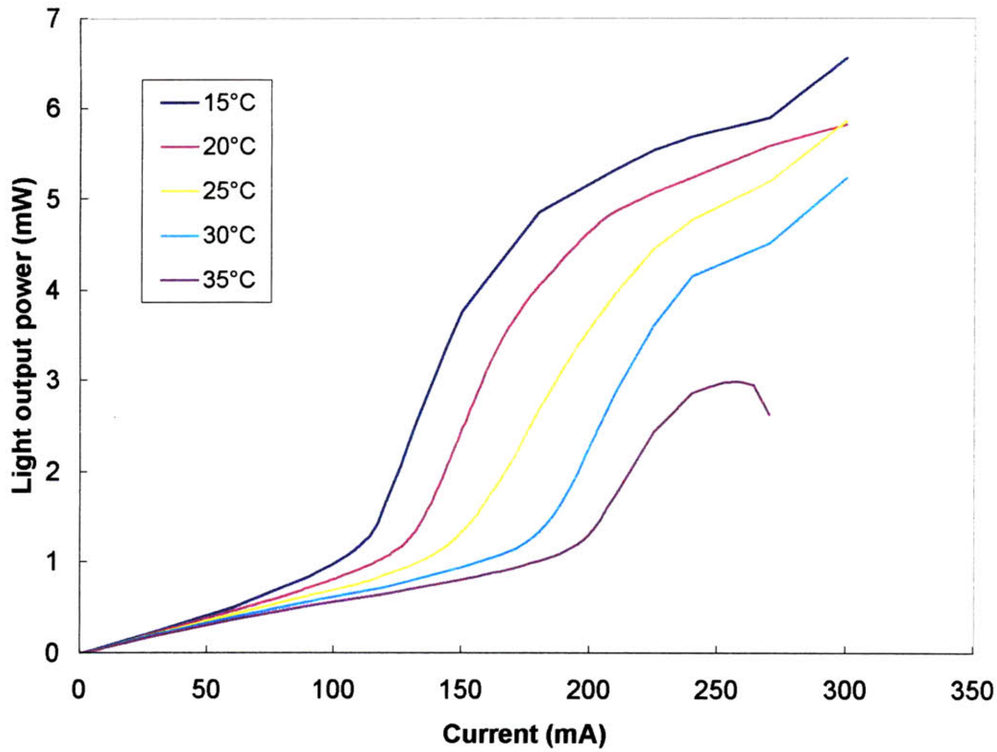


Figure 4.8 – L-I curves taken as a function of temperature for a 1201 μm long and 14 μm wide.

As can be seen, the threshold current rapidly increases with increasing temperature, while the slope efficiencies start to fall off. The characteristic temperatures T_o and T_1 describe these trends in the following semi-logarithmic fashion

$$I_{th} = I_o e^{\frac{T}{T_o}} \tag{4.20}$$

$$\eta_s = \eta_{so} e^{-\frac{T}{T_1}} \tag{4.21}$$

Plotting the measured logarithms of the threshold currents and slope efficiencies, versus temperature, the inverse slopes yield the values for T_o and T_1. For these devices, they were found to be 35 K and 641 K respectively, both of which are very low and indicative of carrier confinement and internal quantum efficiency issues that need to be further addressed and optimized. One thing to note is that the 2% duty-cycle used in the testing might be considered relatively high, especially given the problem encountered in heatsinking the devices. This might have led to additional heating of the active region during testing, which would have led to the overestimation of the change in threshold current with temperature.

At this point, it is interesting to use this result to examine how the active region temperature varied previously with changes in duty-cycle. Examining the variation of threshold current density as duty-cycle is varied, we note that based on a T_o value of 35 K, the increase in threshold current density observed when going from 1% duty-cycle to 10% duty-cycle is the result of a temperature increase of only 5.5 K. This suggests that it might not simply be a problem with heatsinking that is leading to our relatively poor device performance, but that the internal quantum efficiency and carrier confinement might also be issues.

4.4.4 Spectral measurements

Spectral measurements of the lasers were also taken using an OSA. Figure 4.9 shows the emission spectra of a device from Piece 1 that was directly placed on a TEC at 20°C. Data were taken of the device below and above threshold, with the device being pulse with a 2% duty-cycle. The lasing wavelength was 1328 nm for this device.

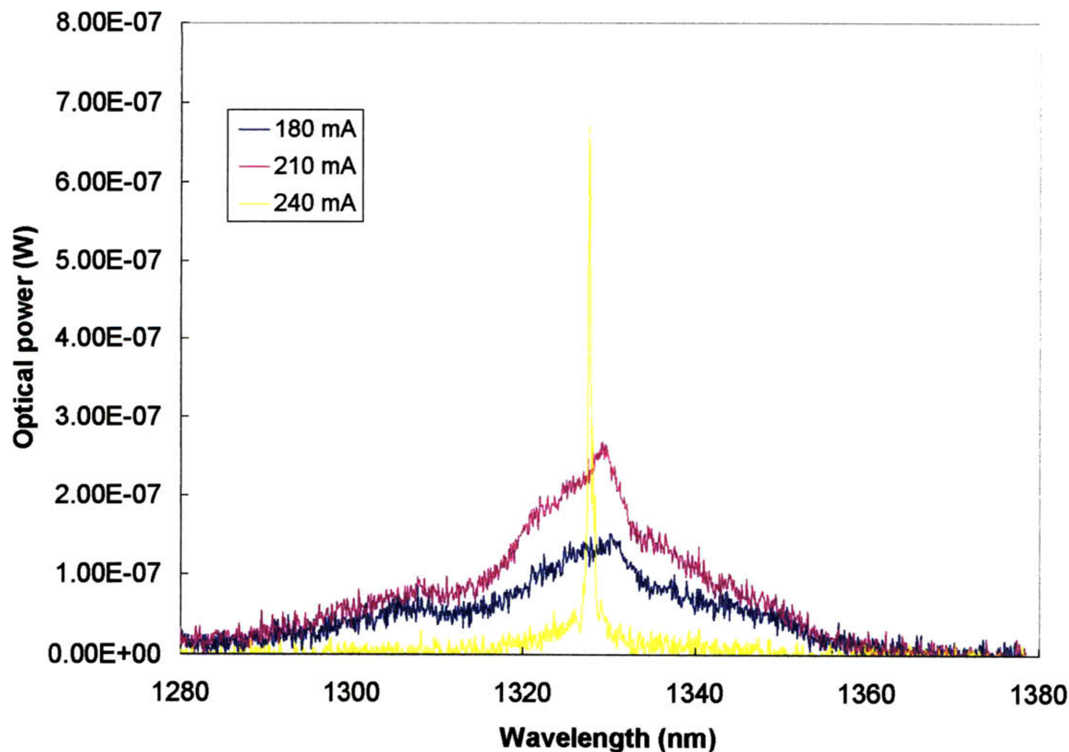


Figure 4.9 – Optical spectra of a 20 μm wide, 2129 μm long device at 20°C, below and above threshold.

The effect of temperature on the emission spectra was also investigated, by using a 14 μm wide and 1201 μm long device from Piece 4. The device was mounted onto a

copper blank using Ga-Sn solder, which was placed onto the TEC with a thin In foil serving as an interface layer. Figure 4.10 plots the various emission spectra as the TEC temperature was varied from 15°C to 30°C. The devices were operated at 10% duty cycle, which was not optimum, but this was necessary to ensure that enough light could be coupled into the OSA for detection at higher TEC temperatures.

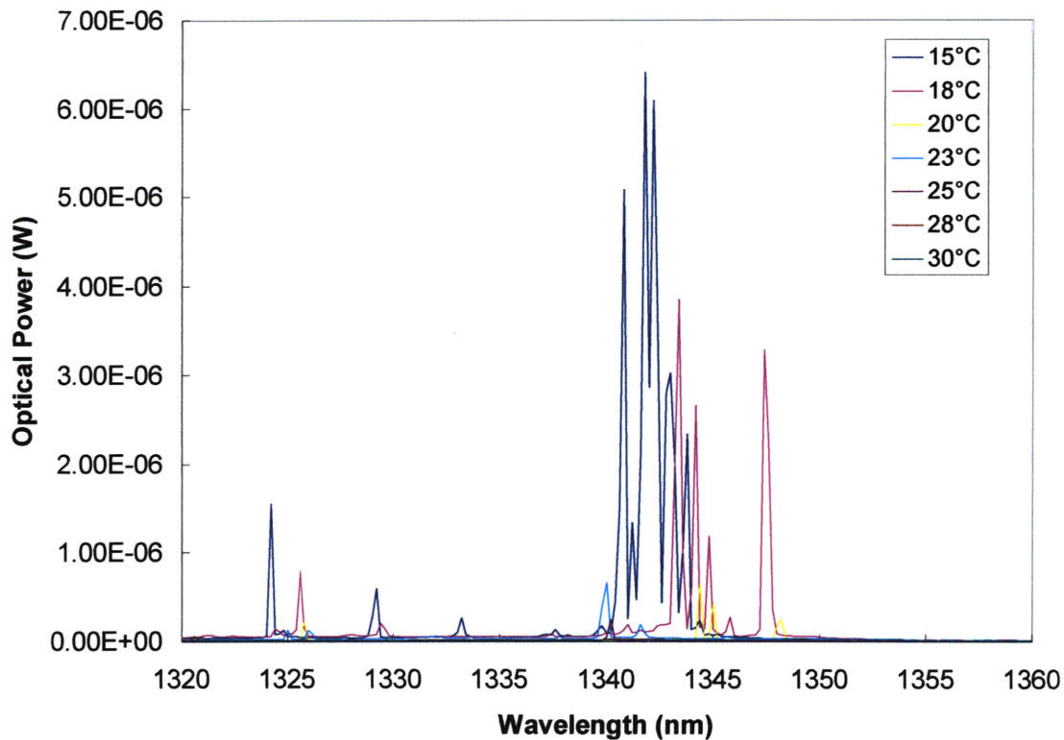


Figure 4.10 – Optical emission spectra taken at varying TEC temperatures of a device from Piece 4.

The edge-emitting Fabry-Perot devices were heavily multi-moded, as can be seen from the multiple peaks in the spectra. It was thus difficult to quantify the wavelength variation with temperature. However, comparison of the spectra at 15°C and 18°C allows us to estimate a roughly 0.5 nm/K wavelength shift in this device. Mode hopping was also evident during the taking of the spectra. Running repeated scans (each taking roughly 2 min) at ostensibly the same current and temperature settings revealed different sets of peaks and relative peak heights in each scan. This suggests the presence of a significant number of competing optical modes, and perhaps an optical cavity that is more susceptible to thermal fluctuations than conventional devices.

4.5 Summary

The design, growth, fabrication and characterization of metamorphic lasers grown on InGaAs graded buffers, and emitting at $\lambda = 1328$ nm have been carried out and discussed. Lasing was observed at duty-cycles up to 10%, but not under CW injection conditions, suggesting difficulties with heatsinking because of the poor thermal conductivity of the graded buffers and the finite wafer bow present in the virtual substrates due to residual strain in the graded buffer layers. Pulsed threshold current densities were as low as 200-250 Acm^{-2} for approximately 2 mm long devices. However, the devices were found to have a low T_o characteristic temperature of 35 K, which suggests that issues with internal quantum efficiency and carrier confinement might be affecting device performance. Additional work needs to be done to definitively identify and address the root causes of this performance.

5. OTHER MINORITY-CARRIER DEVICES ON InGaAs GRADED BUFFERS

In Chapter 4, we reported on the successful development of long-wavelength strained-InGaAs QW-SCH lasers grown on high quality metamorphic InGaAs graded buffers. As stated in the introduction of the thesis, the ability to obtain functional lasers on these InGaAs virtual substrates is a testament to their suitability for minority carrier device applications.

In this chapter, we report on the use of the InGaAs graded buffer for other novel minority-carrier devices, specifically an InAlGaAs/InGaAs heterojunction bipolar transistor (HBT) and an InGaP photovoltaic cell.

5.1 Metamorphic InAlGaAs/InGaAs heterojunction bipolar transistors

InAlGaAs/InGaAs HBTs were grown on the InGaAs graded buffers detailed in Chapter 3, as part of a collaboration with the Nanyang Technological University (NTU) in Singapore. After the growth of the device material using the SEL at MIT, the wafers were sent to NTU for device fabrication and characterization. We report here some of the initial results that have been obtained.

5.1.1 Motivation for metamorphic InAlGaAs/InGaAs HBTs

Currently, most high speed transistors are developed on InP substrates [70, 71] due to the high electron mobilities (~10000 $cm^2V^{-1}s^{-1}$) possessed by $In_xGa_{1-z}As$ alloys that are nearly-lattice-matched to the InP lattice-constant (i.e. around x = 0.53) [72]. Indeed, Chattopadhyay calculated that from a minimum of ~5500 $cm^2V^{-1}s^{-1}$ at x~0.2, the electron mobility steadily rises as x increases, all the way to >20000 $cm^2V^{-1}s^{-1}$ for InAs [73]. The superior performance granted by this material system has even led to efforts by researchers to grow InP HBTs on Ge and Ge-on-insulator (GeOI)/Si wafers [74], for CMOS/III-V integration purposes, and to take advantage of the larger Si and Ge substrates that are available. While the devices grown on Ge and GeOI had dc performances comparable to similar devices grown on InP, the authors noted the

relatively high TDD (~10^7 cm^{-2}) of this platform, which in general tends to lead to poorer performance of HBTs, which are minority-carrier devices.

With the graded buffers that we have developed having TDD on the order of 10^5 cm^{-2} for x~0.3, there is the potential for high performance metamorphic HBTs using the graded buffers as virtual substrates.

5.1.2 Design of the metamorphic InAlGaAs/InGaAs HBT

For an $In_xGa_{1-x}As$ virtual substrate with a terminal composition of x = 0.3, the lattice-constant is 5.7748 Å, which precludes us from using InP (5.8697 Å lattice-constant) as a carrier confinement layer. The natural choice is therefore to use InAl(Ga)As for this purpose. Since HBTs with this lattice parameter have never really been studied previously, we believed that we could adapt an AlGaAs/GaAs HBT design that had previously been attempted on a SiGe virtual substrate as a collaborative effort between NTU and MIT (Sample A in [75]). The device design is reproduced in Table 5.1.

Layer	Sample A from [kk6]		Current work	
Emitter cap	0.03 μm	$In_{0.2}Ga_{0.8}As$: Si (1 × 10^{19} cm^{-3})		
Emitter cap	0.2 μm	GaAs: Si (4.5 × 10^{18} cm^{-3})	0.2 μm	$In_{0.3}Ga_{0.7}As$: Si (1 × 10^{19} cm^{-3})
Emitter	0.1 μm	$Al_{0.25}Ga_{0.75}As$: Si (5 × 10^{17} cm^{-3})	0.1 μm	InAlGaAs: Si (5 × 10^{17} cm^{-3})
Spacer layer	0.005 μm	GaAs (undoped)	0.005 μm	$In_{0.3}Ga_{0.7}As$ (undoped)
Base	0.1 μm	GaAs: Be (1 × 10^{19} cm^{-3})	0.06 μm	$In_{0.3}Ga_{0.7}As$: Zn (1 × 10^{19} cm^{-3})
Collector	0.5 μm	GaAs: Si (5 × 10^{16} cm^{-3})	0.5 μm	$In_{0.3}Ga_{0.7}As$: Si (1 × 10^{16} cm^{-3})
Subcollector	0.6 μm	GaAs: Si (n = 4.5 × 10^{18} cm^{-3})	0.6 μm	$In_{0.3}Ga_{0.7}As$: Si (1 × 10^{19} cm^{-3})
Buffer	1 μm	GaAs (undoped)	1.2 μm	$In_{0.3}Ga_{0.7}As$ (undoped)

Table 5.1 – Layer structures of the AlGaAs/GaAs HBT (Sample A) from [75], and of the InAlGaAs/InGaAs metamorphic HBT in the current work.

While in that work the Sample A design failed to yield good devices, it was due to issues with coefficient of thermal expansion (CTE) mismatch between the AlGaAs/GaAs HBT layers and the SiGe virtual substrate, which was not expected to be a problem in our current work, where we would be working entirely in the InAlGaAs III-V material system. The design of the InAlGaAs/InGaAs HBT was therefore adapted from the AlGaAs/GaAs HBT, based on the following rules. First, the HBT layer thicknesses and doping concentrations were kept as similar as possible. Second, the InAlGaAs alloy composition was chosen so as to provide conduction band and valence band offsets (CBO

and VBO) that were as similar as possible to the AlGaAs/GaAs case. For the $Al_{0.25}Ga_{0.75}As/GaAs$ heterojunction, the calculated CBO and VBO were 222 meV and 137 meV respectively.

Using parameters from Vargaftman *et al* [23], the CBO and VBO for the $InAlGaAs/In_{0.3}Ga_{0.7}As$ heterojunction were calculated as a function of the Al mole fraction in the InAlGaAs quaternary lattice-matched to $In_{0.3}Ga_{0.7}As$. The results are shown in Figure 5.1.

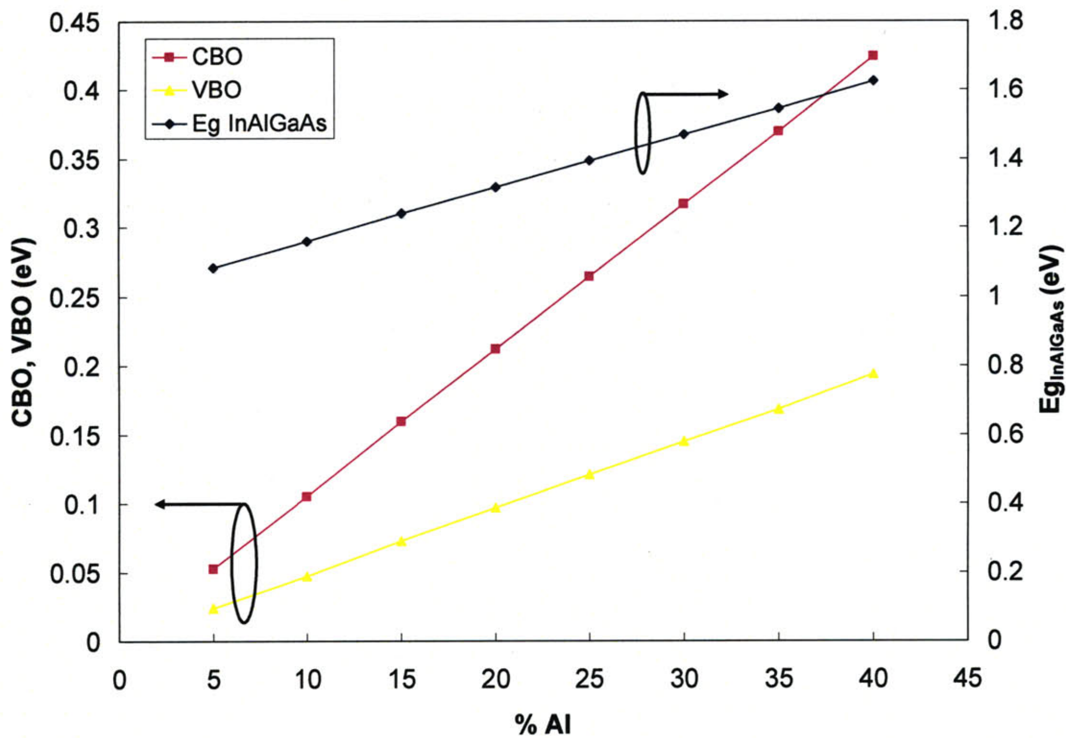


Figure 5.1 – Calculated CBO and VBO values for a lattice-matched $InAlGaAs/In_{0.3}Ga_{0.7}As$ heterojunction as a function of Al mole fraction in the InAlGaAs quaternary alloy. The band gap of the InAlGaAs alloy is also plotted for reference.

Thus, we found that the CBO of the $InAlGaAs/In_{0.3}Ga_{0.7}As$ heterojunction matched that of the $Al_{0.25}Ga_{0.75}As/GaAs$ heterojunction for an Al mole fraction of approximately 22%, while in the case of the VBO, the matching occurred for an Al mole fraction of approximately 28%. We therefore chose the alloy $In_{0.29}Al_{0.25}Ga_{0.46}As$ to be the emitter layer for our InAlGaAs/InGaAs HBT. The final design that was arrived at is listed alongside the AlGaAs/GaAs HBT in Table 5.1.

5.1.3 HBT growth

The InAlGaAs/GaAs HBTs were grown on InGaAs graded buffers, the growth details of which were covered in Chapter 3. For the first HBT growth attempt, the HBT was actually re-grown on a sample of graded buffer GB2 that was described in Chapter 3. This graded buffer had a terminal composition of $In_{0.295}Ga_{0.705}As$, and was measured to have a TDD of 4.4×10^5 cm^{-2}. The re-growth was carried out after a surface preparation step, as described in Chapter 3 in the section on QW-SCH re-growth, and began with a homoepitaxial $In_{0.295}Ga_{0.75}As$ layer before the device layers were grown.

For all other HBT growths, the InGaAs graded buffers and HBT were grown together in a single growth. This was because of a suspected contamination issue with our wet chemical etchants at the time, which, as we shall see shortly, led to fairly defective re-growth for our first HBT attempt. It should be noted that contaminated chemicals were suspected to be the cause of the problems, as several other growths and re-growths that utilized wet chemical surface preparations prior to growth also experienced material quality issues. The device layers were grown with growth rates of approximately 1.5-2.0 μm/hr at 700°C, and the V/III ratio was maintained between 33-45.

5.1.4 HBT material characterization

For the HBT growths, the properties that we were most concerned with the microstructural quality of the device layers (e.g. TDD), and macroscopic parameters such as the layer thicknesses and compositions. X-TEM and XRD were therefore used to characterize the HBT material before it was sent to NTU for device processing.

As mentioned in the previous section, the first attempt at growing a HBT (HBT_1) did not yield good material. X-TEM that was performed on the first HBT sample (HBT_1) revealed the presence of significant numbers of defects in the device layers, with dislocations running across the re-growth interface. Figure 5.2 is an X-TEM image that depicts this.

Figure 5.2 – X-TEM image of HBT_1 that was re-grown on an $In_{0.295}Ga_{0.705}As$ graded buffer.

We ruled out the possibility that the defects were the result of poor lattice-matching, by taking XRD measurements of the sample, which found the device's InGaAs layers to have an In mole fraction of 0.293. The InAlGaAs layer was, however, found to be under ~0.3% compressive strain. Based on the presence of threads and dislocation loops in the X-TEM images of this HBT, the TDD through the device layers was estimated be on the order of 10^8 cm^{-2}. Thus, it was expected that the devices obtained from this sample, even if they exhibited transistor action, would likely perform very poorly.

A second sample, HBT_2, was therefore grown. As mentioned earlier, this HBT sample and its underlying graded buffer were grown continuously, thus avoiding potential problems associated with the re-growth. XRD of HBT_2, however, found that while there were no issues with lattice-matching, the mole fraction of In in the graded buffer cap and device layers was only 0.26, which we attributed to a drift in the heater temperature; specifically, due to the lower than expected In mole fraction, we suspected that the actual growth temperature was slightly higher than the specified 700°C (at temperatures around 700°C, we do expect slightly increased TMGa pyrolysis with

increasing temperature leading to increased Ga-incorporation, while TMIn pyrolysis has effectively saturated, resulting in an overall lower In mole fraction in the InGaAs alloy [27]. Figure 5.3 is an X-TEM image of HBT_2.

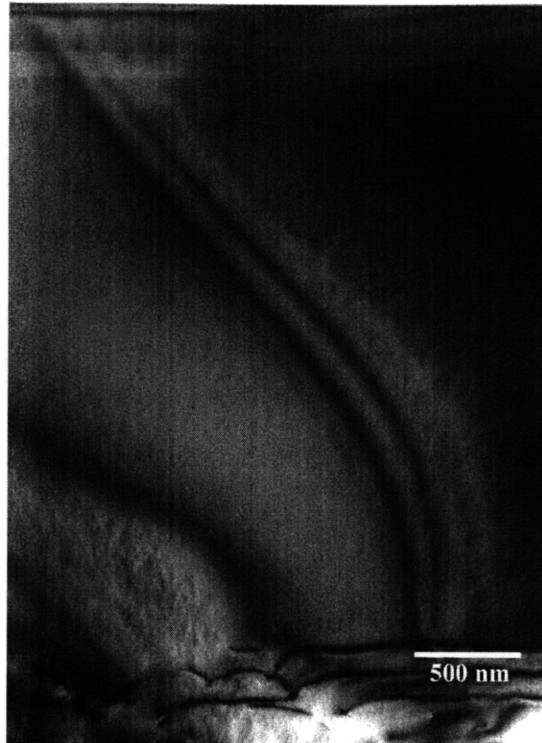


Figure 5.3 – X-TEM image of HBT_2 that was grown continuously together with an $In_{0.26}Ga_{0.74}As$ graded buffer.

Apart from the thickness fringes present in Figure 5.3, we note that the layers were free of dislocations, and that they were flat. The thickness of all the HBT layers in total were approximately 15% higher than expected, which we believe might once again be related to the higher than expected growth temperature. However, a puzzling observation was that while the design called for different growth thicknesses for the n^+-subcollector and the n-collector (600 nm and 500 nm respectively), and they were ostensibly grown that way, they both appeared to be approximately 650 nm thick. We initially attributed this to uncertainties in the thickness measurement, due to relatively limited contrast in the X-TEM image from the different doping levels. However, as we shall see shortly, subsequent device testing revealed a different and relatively clear-cut explanation for this observation.

5.1.5 Device results

After material characterization by X-TEM and XRD, both HBT_1 and HBT_2 were sent to NTU for device fabrication and testing. While poor, or non-performance, or HBT_1 was expected, we felt that the comparison of data from HBT_1 and HBT_2 might serve to highlight the importance of low TDD in HBTs. Indeed, measurements of base-collector isolation on HBT_1 and HBT_2 quickly revealed that high TDD did indeed lead to problems. Figure 5.4, provided by Lew, from NTU, shows I-V data for subcollector isolation.

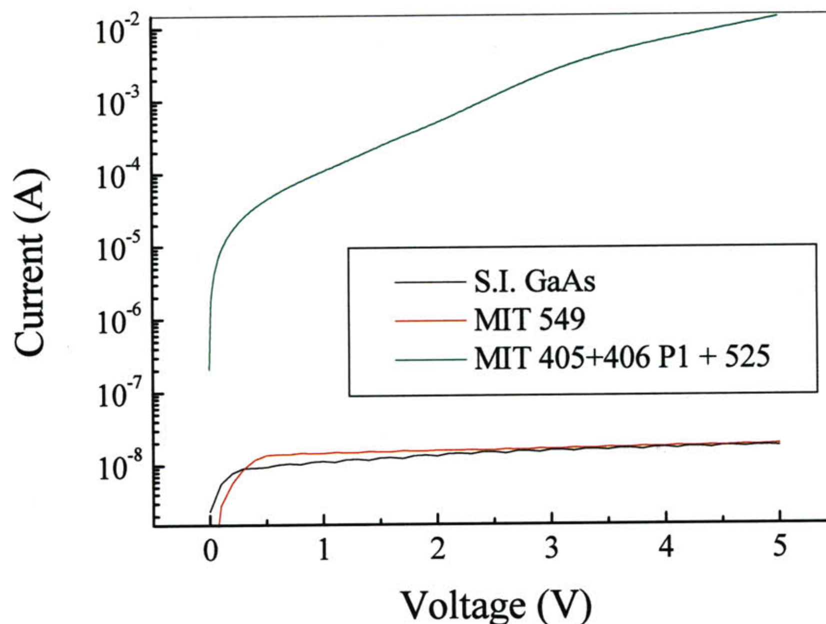


Figure 5.4 – I-V measurements of subcollector isolation. In the figure, "S.I. GaAs" refers to isolation data taken from a control semi-insulating GaAs wafer. "MIT 549" refers to HBT_2, while "MIT 405+406 P1 + 525" refers to HBT_1.Figure provided by NTU.

The subcollector isolation data is measured by probing two metal pads on subcollector layer after the removing of all the device material including the n^+ subcollector between these two pads. Essentially, this provides a measurement of the quality of electrical isolation provided by the undoped InGaAs graded buffer cap layers. Figure 5.4 therefore shows that the leakage current through the HBT_1 material with high TDD is significantly higher, pointing to the importance of a high quality graded buffer for HBTs. In contrast, the material in HBT_2 exhibited excellent isolation, comparable with SI GaAs wafers, once again reinforcing the importance of graded buffer quality.

Not surprisingly, devices from the HBT_1 sample exhibited current gain ($\beta = I_C / I_B$ <1). This was almost certainly due to the high defect density running through the device layers, resulting in poor minority carrier lifetimes and therefore high recombination current in the base region. However, working devices also could not be obtained from the HBT_2 material, which was initially surprising given the apparent high quality material from the growth. In the course of device processing, it was found that the n-contacts made to the subcollector and the emitter cap had significantly different behaviors. This was puzzling since both were supposed to be InGaAs layers of identical compositions and doping levels, and identical reactor growth conditions were used for both layers. Figure 5.5 shows the different behaviors exhibited by the n^+ emitter and n^+ subcollector contacts.

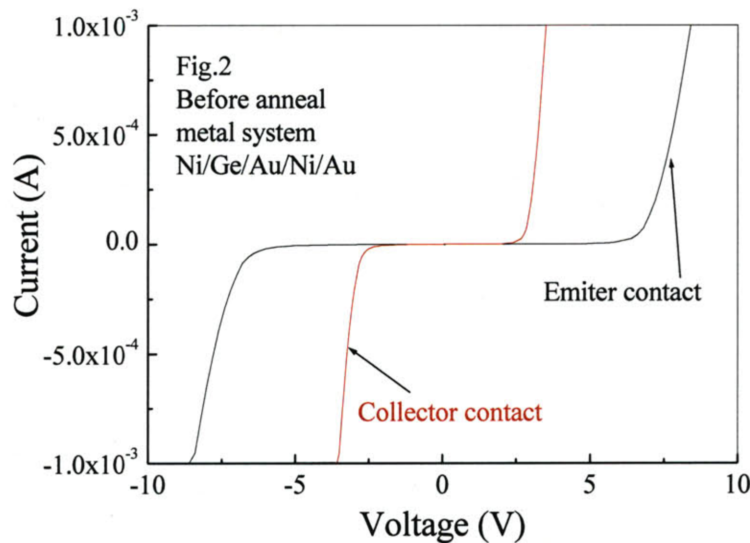


Figure 5.5 – I-V characteristics of pre-annealed n^+ emitter and n^+ subcollector contacts in HBT_2. Figure provided by NTU.

As can be seen, the contacts are both Schottky in nature pre-anneal, which is the expected behavior for the Ni/Ge/Au/Ni/Au metallurgy used, as a rapid-thermal anneal step is required for the Ge in the metal stack to diffuse into and further dope the InGaAs layers before ohmic behavior is observed [76]. The higher Schottky turn-on voltages for the emitter contact suggested a significantly lower doping level present in the emitter layer, as compared to the collector layer. It was subsequently found that ohmic contacts could be successfully achieved for both the emitter and the subcollector once anneals were carried out. However, while the subcollector contact only needed a 1 min anneal at

390°C (approximately the eutectic temperature for 88 wt% Au/12 wt% Ge) for ohmicity, the emitter contact required an anneal at 500°C, which is clearly anomalous, and actually resulted in the destruction of the contact metallurgy (despite ohmicity being finally obtained).

This data suggested that doping in the emitter was much lower than expected, which led us to examine the MOCVD growth logs to try to confirm the cause. Figure 5.6 is data taken from the growth logs for the growth of HBT_2, focusing on the time during the growth of the device layers.

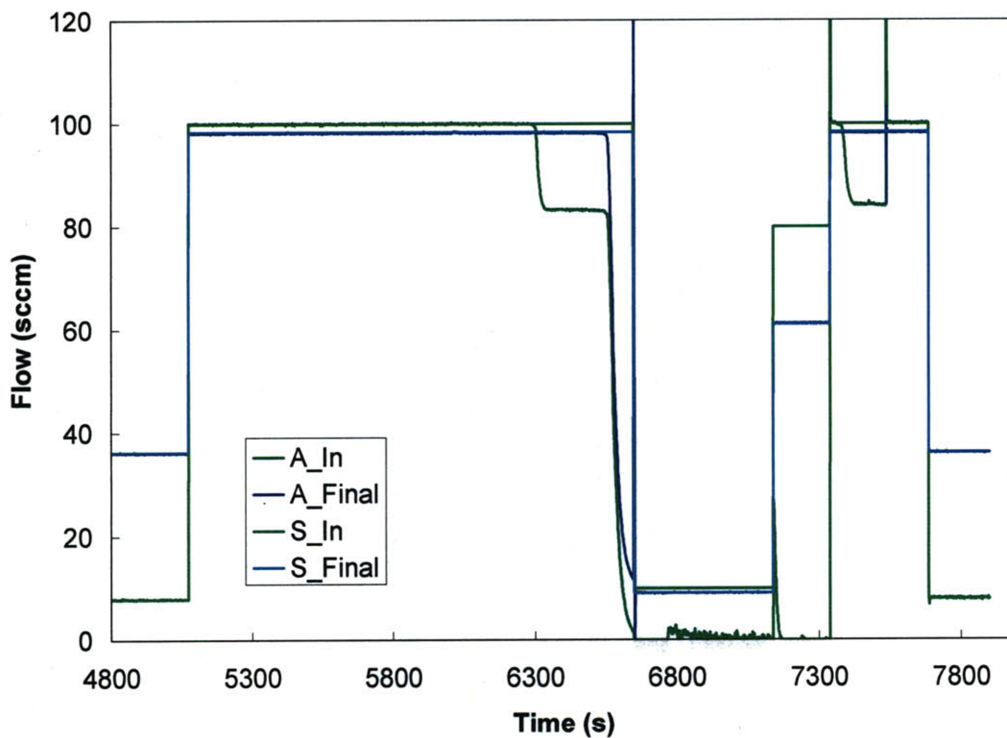


Figure 5.6 – MOCVD growth log data for the Si_2H6 n-dopant source during the growth of the device layers for HBT_2. The Si_2H_6 source is configured with a double dilution line, and S_In and S_Final represent the setpoint values of the input and final MFCs, while A_In and A_Final are the actual values of the same MFCs. (See Chapter 2 for a more detailed explanation of the MOCVD source lines).

In Figure 5.6, growth of the n^+ subcollector is from roughly t = 5100 s to t = 6650 s. As we can see, at approximately t = 6100 s, the actual flow through the input MFC starts to deviate from the setpoint, signifying that the line is starting to run out of Si_2H_6 at that point. (Subsequent deviations between the actual and setpoint values can be explained by examining the dilution MFC flows, but are not important to the discussion here). Thus, it is likely that the doping started to drop starting about two-thirds into the

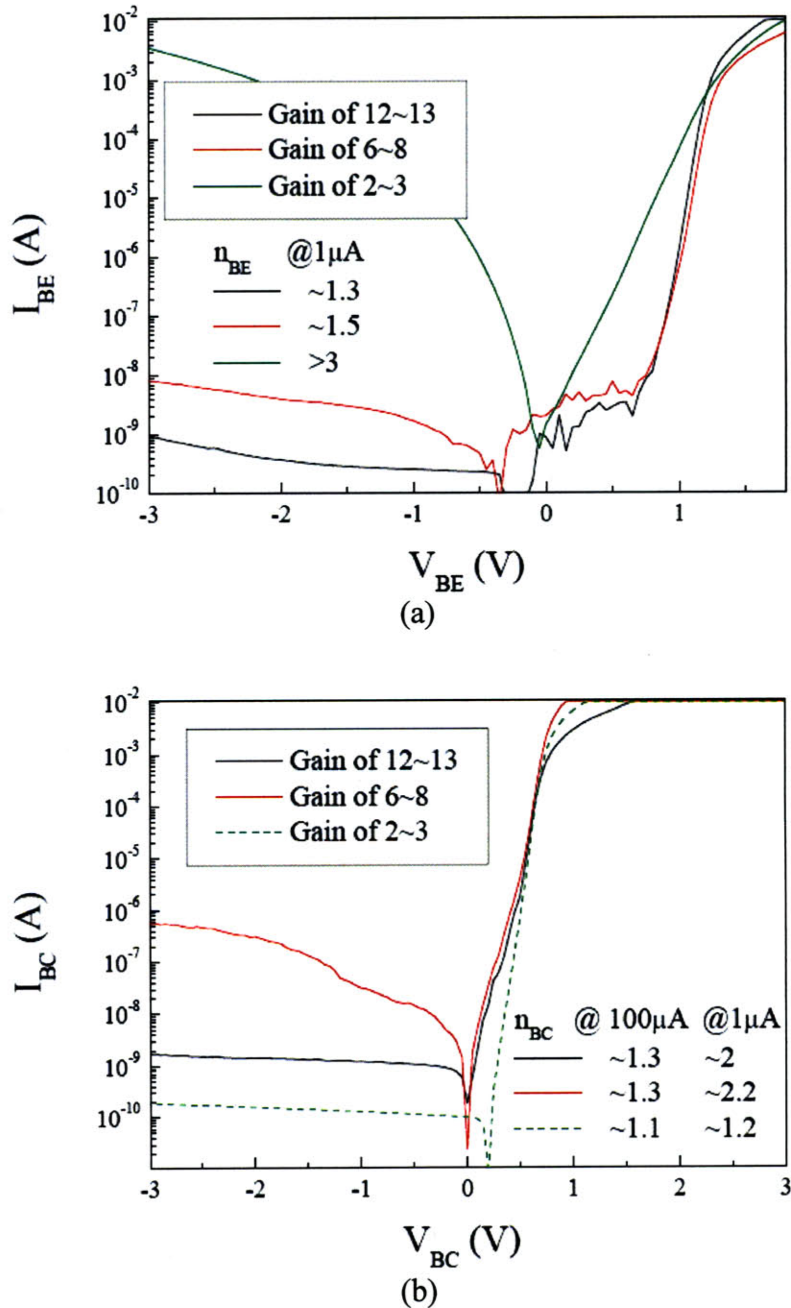
subcollector growth, or roughly after the first 500-550 nm. This would explain why the contrast between the subcollector and collector layers in Figure 5.3 was not good, and also why the subcollector and collector thicknesses appeared to be similar. Furthermore, it is clear that this would have resulted in an effectively undoped emitter, which would account for the poor contact behavior exhibited by the emitter. While unfortunate, it is believed that problems with the actuation of a gas valve in our Si_2H_6 gas cabinet led to this. Thus, the source cylinder was not opened to the reactor, and once the gas in the pressurized delivery line was consumed (over the first ~1000 s of subcollector growth), the supply of Si_2H_6 ran out.

A third HBT structure (HBT_3) was therefore grown, again in a single, continuous growth process. For this device, however, the subcollector and collector thickness were set to be the same. For this sample, XRD determined the InGaAs composition to be $In_{0.305}Ga_{0.695}As$, and the single InAlGaAs emitter layer was well-lattice matched to the InGaAs layers. An X-TEM of HBT_3 is shown in Figure 5.7.

Figure 5.7 – X-TEM image of HBT_3 that was grown continuously together with an $In_{0.305}Ga_{0.695}As$ graded buffer.

The material was processed similarly to HBT_1 and HBT_2, and transistor action was observed. However, the material was found to be non-uniform, and the measured dc

current gain of the devices was found to fall into three separate ranges (2-3, 6-8, and 12-13), depending on the position of the device on the wafer. Figures 5.8(a) and (b) show the I-V characteristics for the base-emitter and base-collector p-n junctions respectively, with representative data from each of the three ranges shown.



Figures 5.8(a) and (b) – I-V data for the (a) base-emitter and (b) base-collector p-n junctions of HBT_3.

It can be seen that there was no clear trend with respect to the current gain ranges in terms of diode ideality for the base-collector junctions. However, the devices with the lower current gains all exhibited poor diode ideality and performance at the base-emitter junction. This suggests that the transistor performance is largely determined by the quality of the base-emitter junction in our case. While a 5 nm spacer layer was included between the base region and the InAlGaAs emitter, there was no sign of it in the X-TEM of HBT_3, suggesting that perhaps dopant diffusion has resulted in there being no abrupt base-emitter junction.

It was also found the base current ideality factor was ~1.75 for the low gain devices, and ~1.85 for the better devices, suggesting that in both cases, the 2 kT current term dominates the base current. Since carrier recombination in the emitter-base space-charge region manifests itself as a 2 kT component of the base current [77], this is indicative of the fact that a problematic emitter-base junction might be limiting device performance.

At the time of writing this thesis, further tests were being carried out on the devices, including ac measurements.

5.2 Metamorphic photovoltaic cells grown on InGaAs graded buffers

High quality InGaAs graded buffers with In mole fraction of approximately 0.3 were also provided to Ohio State University (OSU), for them to realize novel metamorphic photovoltaic (PV) cells.

5.2.1 Motivation for metamorphic PV cells

There is potential for the design of a highly-efficient multi-junction cell at this lattice-constant, such as using an $In_{0.29}Al_{0.71}As/In_{0.78}Ga_{0.22}P/In_{0.30}Ga_{0.70}As$ triple-junction configuration. With this configuration, a triple-junction PV cell can be realized with bandgaps of 1.0 eV, 1.6 eV, and 1.9 eV. Figure 5.9 shows the ASTM G173-03 reference solar spectrum, with the bandgaps of such a cell overlaid.

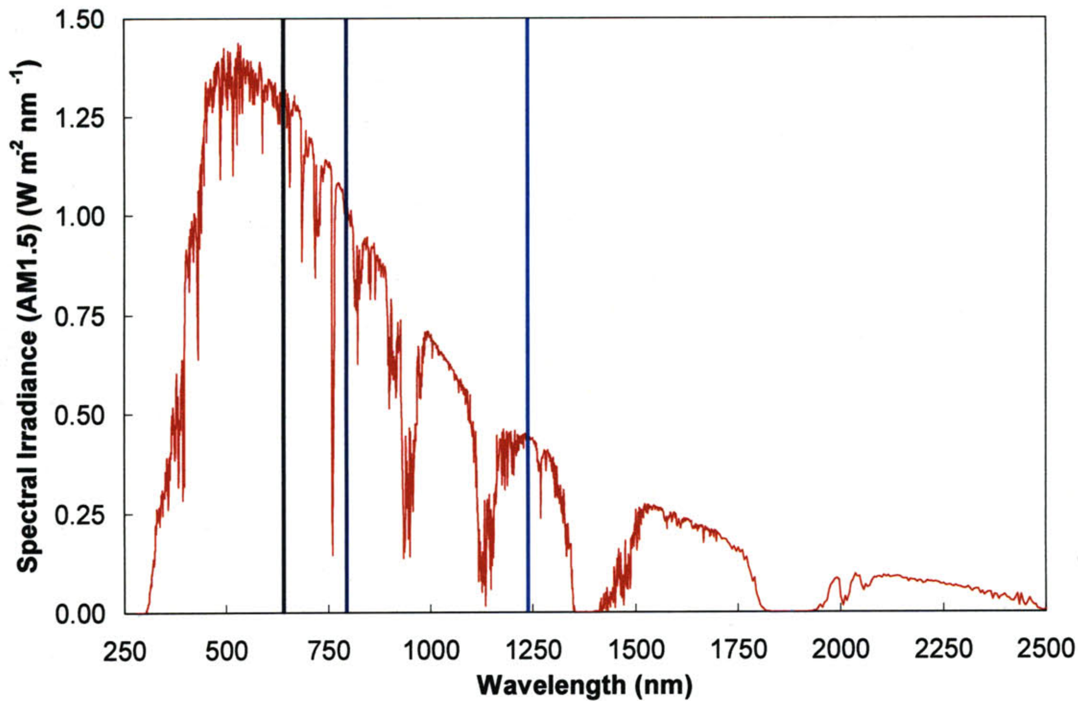


Figure 5.9 – Reference solar spectra at AM1.5 (ASTM G173-03 Reference Spectra), with bandgaps of InAlAs, InGaP and InGaAs lattice-matched to $In_{0.3}Ga_{0.7}As$ overlaid.

For most non-Si-based multi-junction PV cell designs, there is a lack of good material choices with bandgaps suitable for absorbing solar radiation longer than 1000 nm. The most common semiconductor used for this purpose is Ge, which is lattice-matched to GaAs, and has a bandgap of 0.66 eV. However, its low bandgap relative to other subcells in the stack (typically with bandgaps >1.4 eV) leads to significant carrier thermalization and poor current matching, and also limits its open-circuit voltage, V_{oc}. All of these issues limit not only the efficiency of the Ge subcell, but of the entire PV stack. In contrast, PV cell designs with a 1 eV bandgap bottom subcell (i.e. smallest bandgap) in a multi-junction PV stack spanning approximately 1-2 eV have been shown to lead to significantly higher overall conversion efficiencies [78, 79], due to better current-matching between the cells and reduced carrier thermalization, both of which are attributable to the more even spacing of the various subcells' bandgaps in spectral terms. The V_{oc} of the 1 eV subcell will also be significantly higher than a comparable Ge subcell.

Given that PV cells are minority-carrier devices, it is clear that high quality virtual substrates with the appropriate lattice-constants will be needed to realize the highest efficiency cells, and the graded buffers developed in this work represent an excellent platform on which these devices can be developed.

5.2.2 Preliminary metamorphic InGaP cell results

At the time of writing this thesis, OSU had managed to grow a metamorphic single-junction InGaP PV cell on the InGaAs graded buffers provided to them, and the PL spectrum of the cell, taken at room temperature, is shown in Figure 5.10.

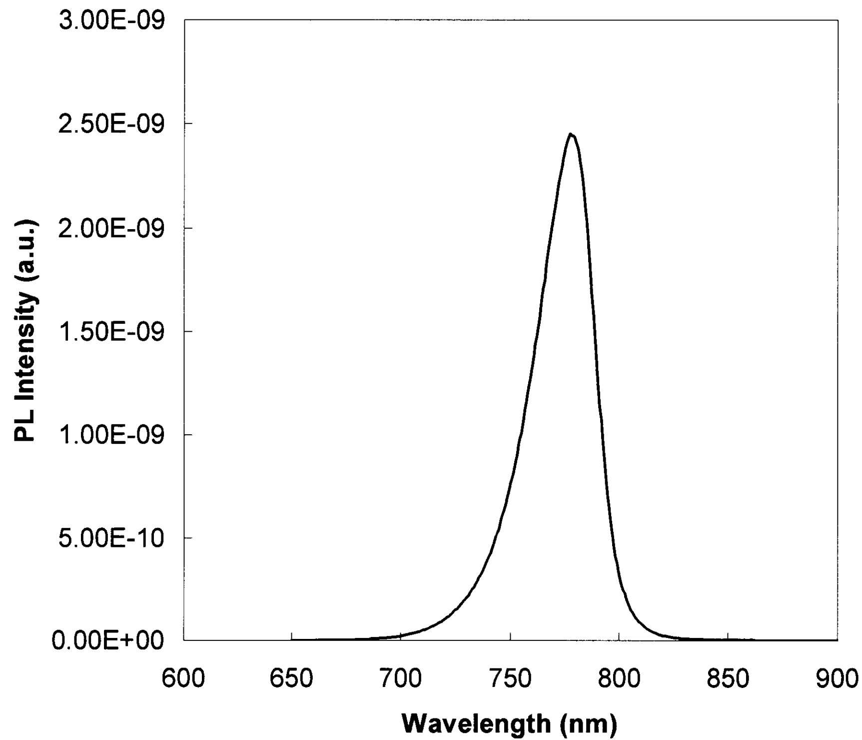


Figure 5.10 – PL spectrum of a metamorphic InGaP PV cell on an $In_{0.3}Ga_{0.7}As$ graded buffer.

As can be seen from Figure 5.10, good PL emission was obtained from the InGaP PV cell. The PL emission peak was at 780 nm (1.6 eV), and the PL FWHM was approximately 2.6 kT, which confirms that the InGaAs graded buffer does serve as a good virtual substrate for the growth of metamorphic PV cells. Thus, there is clearly the

potential for realizing the multi-junction PV cell design envisioned in the previous section.

5.3 Summary

Metamorphic InAlGaAs/InGaAs HBTs grown on our high quality InGaAs graded buffers have been demonstrated. Preliminary measurements made on the devices have recorded current gains of up to 13. Uniformity of the device growth across the wafer appears to be a potential problem, and must be addressed, together with growth optimization to improve the base-emitter junction. We expect that doing so will lead to significantly improved device performance.

Metamorphic single-junction InGaP PV cells have also been realized on our InGaAs graded buffers, and PL measurements have revealed the material to be of high quality. We believe that this demonstrates the viability of our high quality graded buffers for the development of highly efficient multi-junction PV cells.

6. DIGITAL METAMORPHIC ALLOYS (DMA) FOR METAMORPHIC GRADED BUFFERS

In the preceding chapters, we examined the growth and optimization of InGaAs ternary random-alloy graded buffers, and the subsequent growth of device structures on these graded buffers. Two key issues became apparent in the course of this work. First, the propensity of the $In_xGa_{1-x}As$ alloy to phase separate at In mole fractions greater than ~0.35 means that it is not possible to obtain high-quality, low TDD graded buffers at compositions with $x > 0.35$, which in turn limits the virtual substrate lattice-constant to about 5.795 Å. Second, the thermal conductivities of the ternary InGaAs alloys are known to be poor, and the laser device results suggest that this might be a significant issue when it comes to device applications requiring high power and heat densities.

This chapter discusses the use of repeated thin layers of constituent materials such that they act in a mechanically-similar fashion as a random alloy, which is akin to short-period superlattices (SLs) that have been used in many ways to enhance the mechanical, electronic and optical characteristics of materials and devices. For instance, the InAs/GaSb SL system has been used for mid-IR devices [80], the GaN/AlGaN material system for dislocation filtering in nitride-based devices [81], and the GaAs/Al(Ga)As and Si/SiGe/Ge systems, amongst many others for the construction of digital alloys [82, 83]. In all these instances however, the focus has been on either unstrained or strain-compensated structures, where the SL structures are tailored to a specific substrate or lattice-constant, and the constituent layers of the SLs are chosen such that the signs and magnitudes of their respective strains cancel out when averaged over the entire SL structure. This is necessary to prevent the amount of strain being built up from reaching a critical amount, so that the plastic deformation of the SL layers, which leads to the generation of extended defects such as dislocations, is avoided.

Here, we make extensive use of digital alloys, but whereas digital alloys have previously been used to create virtual ternaries from an electronic properties perspective, we use digital alloys here to approximate the mechanical properties of materials with lattice-constants intermediate to their constituent layers. Instead of growing a fully strain-balanced structure with a fixed equilibrium lattice-constant, we combine multiple digital alloys, each with a slightly different lattice-constant. In this way, the digital alloys are

used as replacements for ternary alloys in a graded buffer, allowing us to mimic conventional metamorphic graded buffer growth that has typically been achieved through compositional grading, such as in the $In_xGa_{1-x}As$ alloy system [28, 38]. Figure 6.1 illustrates this schematically.

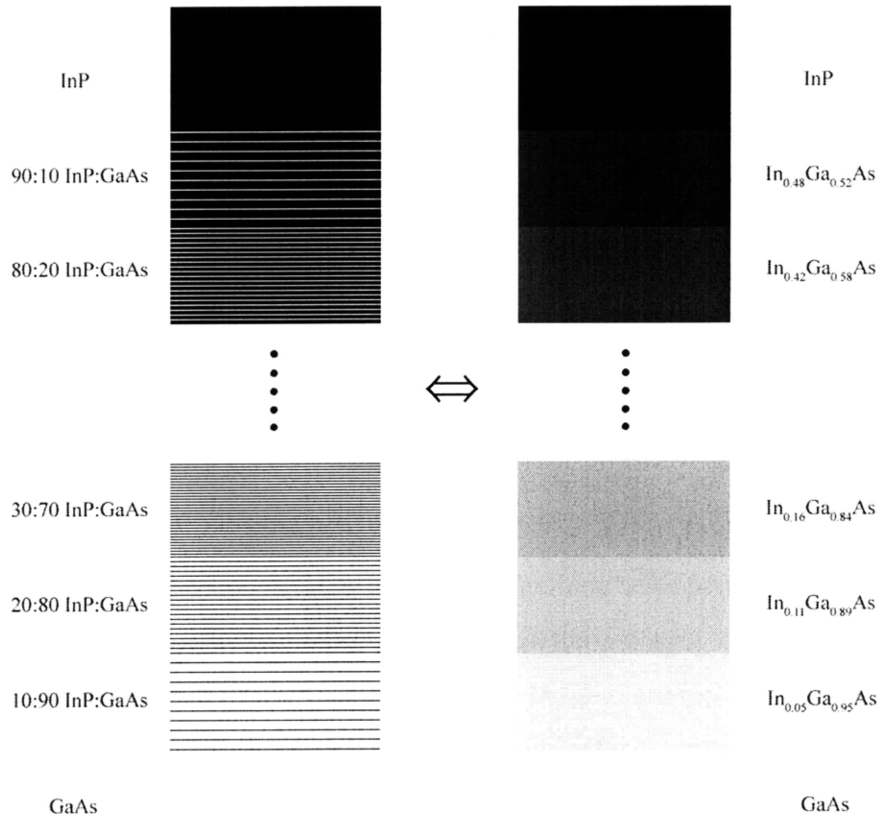


Figure 6.1 – Schematic illustrating the use of DMAs to replace ternary random alloys in the construction of a metamorphic step-graded buffer. The illustration depicts the use of GaAs/InP DMAs on the left and InGaAs ternary alloys on the right.

The right side of Figure 6.1 depicts a conventional compositionally step-graded buffer, where a series of ternary InGaAs alloys with increasing In mole fraction are grown successively. This leads to a gradual change in the lattice-constant from GaAs to InP, which is lattice-matched to $In_{0.53}Ga_{0.47}As$. In contrast, the left side of Figure 6.1 shows how lattice-constant engineering is accomplished by growing a series of digital alloys with different effective lattice-constants. Doing so once again leads to the build-up of strain, and if done correctly, the individual digital alloys behave in a mechanically-similar fashion as random-alloys and undergo strain relaxation, hence leading us to term them digital metamorphic alloys (DMAs).

By using binary III-V compounds as the constituent layers in the DMAs, we can obtain a metamorphic graded buffer constructed entirely of binary semiconductor materials, in contrast with conventional III-V graded buffers, which, because they are compound semiconductors, necessitate the use of ternary alloys. We believe this presents several advantages. First, elemental (Si, Ge) and binary compound (e.g. GaAs, InP) semiconductors have the highest thermal conductivities of all semiconductors, while ternary and quaternary alloy semiconductors have significantly lower thermal conductivities, especially for alloy compositions far from their binary endpoints [84]. This is shown in Table 6.1.

Semiconductor	Type	Thermal conductivity ($Wm^{-1}K^{-1}$)
Si	Elemental	130
Ge	Elemental	58
GaAs	Binary	55
InP	Binary	68
$In_{0.53}Ga_{0.47}As$	Ternary	5
$In_{0.67}Ga_{0.33}As_{0.72}P_{0.28}$	Quaternary	4

Table 6.1 – Thermal conductivities of selected semiconductor materials. Data reproduced from [84].

For metamorphic device applications, a well-designed and grown all-binary DMA graded buffer can therefore potentially provide better thermal performance, in terms of conducting heat away from the device regions. This is especially important in high current/power density active devices, such as lasers, amplifiers and high-power transistors.

A second important feature of all-binary DMAs is that they allow us to circumvent material issues such as phase separation and ordering, which plague ternary and quaternary alloys [27, 35]. While these issues affect the electronic and optical properties of the materials as well, it is their impact on the dislocation kinetics that is most important for metamorphic layers, as they have a dramatic effect on the ultimate threading dislocation density (TDD) obtained, which directly impacts device performance and reliability [38, 51]. This is especially important for epitaxy on offcut substrates, which are necessary for heterovalent epitaxy such as GaAs/Ge [31, 85], as ternary alloys such as InGaAs that are grown on such substrates have shown a propensity for phase separation, as we have observed in Chapter 3.

6.1 DMA design

As in a conventional analog graded buffer, our goal is to controllably engineer the lattice-constant from that of a given substrate to another value, on which device layers can subsequently be grown. In this work, growth was carried out on GaAs substrates, and we investigated applying the DMA concept to the lattice-constants between GaAs (5.6533 Å) and InP (5.8697 Å).

Our goal is to obtain DMAs with various effective lattice-constants. For a DMA comprising alternating layers of two binary compounds A and B, we assume that Vegard's law holds, and that the effective lattice-constant of the DMA constructed is

$$a_{DMA} = x_A a_A + x_B a_B = \frac{t_A a_A}{t_A + t_B} + \frac{t_B a_B}{t_A + t_B} \qquad (x_A + x_B = 1) \qquad (6.1)$$

where a_{DMA} is the effective lattice-constant of the DMA, and x_i, t_i, and a_i are the mole fraction, layer thickness (in a period) and lattice-constant, respectively, of component i. Therefore, to grade the lattice-constant, as we move from one DMA to another, we vary the thicknesses of the component layers in a given period, forming a series of DMAs with slightly different lattice-constants. An example of a grading scheme used in this work is detailed in Table 6.2.

DMA	% InP	a_{DMA} (Å)	t_{GaAs} (Å)	t_{InP} (Å)	# periods	Total DMA thickness (Å)	$t_{crit, GaAs}$ (Å)	$t_{crit, InP}$ (Å)
GaAs	0	5.6533	N/A		N/A	N/A	N/A	17
DMA1	10	5.6749	90	10	10	1000	302	20
DMA2	20	5.6965	40	10	20	1000	124	24
DMA3	30	5.7182	23	10	30	990	71	29
DMA4	40	5.7398	15	10	40	1000	46	35
DMA5	50	5.7615	10	10	50	1000	33	45
DMA6	60	5.7831	10	15	40	1000	24	60
DMA7	70	5.8048	10	23	30	990	18	86
DMA8	80	5.8264	10	40	20	1000	14	143
DMA9	90	5.8481	10	90	10	1000	11	332
InP	100	5.8697	N/A		N/A	N/A	8	N/A

Table 6.2 – Details of a grading scheme used for DMA graded buffers in this work.

In the grading scheme described in Table 6.2, grading from the binary endpoints of GaAs to InP is accomplished by the use of nine DMAs. a_{DMA} is the effective lattice-constant of each DMA (or binary endpoint), while t_{GaAs} and t_{InP} are the layer thicknesses of each of the binary constituents in a period within a given SL. The critical thicknesses

of GaAs ($t_{crit,\,GaAs}$) and InP ($t_{crit,\,InP}$) can be obtained following Matthews-Blakeslee's force-balance calculations, as modified by Fitzgerald [18], and are given by

$$t_{crit} = \frac{D\left(1-\nu\cos^2\alpha\right)\left[\ln\left(t_{crit}/b\right)+1\right]}{Yf} \tag{6.2}$$

Here, D is the average shear modulus of the film and the underlying substrate (or SL, in our case). ν, b and Y are the Poisson's ratio, Burgers vector and Young's modulus of the film respectively, and f is the mismatch between the film and the underlying substrate. In the material systems we are dealing with, 60° dislocations are the first to form, and $\alpha = 60°$.

The critical thicknesses represent the theoretical maximum thicknesses of GaAs and InP that can be grown on each DMA, assuming that the DMA is fully-relaxed and has an in-plane lattice-constant exactly equal to a_{DMA}, before relaxation and the formation of dislocations occur.

The 3.7% lattice mismatch between InP and GaAs is bridged in 10% steps (i.e. each DMA has an effective lattice-constant that is different from the preceding DMA by 10% of the lattice mismatch). The first DMA (DMA1) that is grown on GaAs is composed of 10% InP and 90% GaAs, in terms of thickness (10 Å InP and 90 Å GaAs), which, if fully relaxed, would have an effective lattice-constant of 5.6748 Å, which represents a decrease of 0.37% in the lattice mismatch relative to InP. The next DMA (DMA2) would be composed of 20% InP and 80% GaAs, which would have an effective lattice-constant of 5.6963 Å, which represents a further 0.37% decrease in the lattice mismatch to InP, and so on. The thicknesses of the individual layers of GaAs and InP for a given DMA(n) are chosen such that they are far below their respective critical thicknesses, when grown on underlying DMA(n-1). This is to try to ensure that they do not all relax as individual layers, which would lead to the nucleation of a large number of dislocations. The likelihood that the underlying DMAs are not fully relaxed, and therefore have in-plane lattice-constants that are smaller than expected, which would mean larger effective mismatch and therefore smaller critical thicknesses, is also addressed in this way. A DMA graded buffer grown as described in Table 6.2 will have a total thickness of 900 nm, with a uniform grading rate of approximately 4.1% mismatch/µm. We note here that this is much higher than typical grading rates used

in conventional graded buffers, and fully expect that for the lowest TDDs to be obtained, reduced grade rates must be used. This can be achieved simply by growing each DMA thicker (i.e. with more periods). The purpose of the current work is to test the concept, and using discrete 10% InP jumps aids us by keeping the experiment simple. In principle, it should be possible to achieve a continuous grade by continuously changing the thicknesses of the constituent DMA layers, which should yield superior TDD values.

6.2 Experimental details

We grew multiple DMA graded buffer samples based on the grading scheme defined in Table 6.2, or variations of it, to investigate the DMA concept. The samples were grown by low-pressure metal-organic chemical vapor deposition (MOCVD) in a 7x2" Aixtron/Thomas Swan close-coupled showerhead (CCS) configuration reactor. Pre-growth anneals, and all layers grown prior to the DMAs were carried out at a reactor pressure of 100 Torr, while DMA growths were carried out at 50 Torr, unless otherwise stated. Trimethylgallium (TMGa), trimethylindium (TMIn), arsine (AsH_3) and phospine (PH_3) were used as sources. Nitrogen was used as the carrier gas at a flow rate of 20 slpm. Specified growth temperatures were of the wafer surfaces, and were determined using optical pyrometry. The samples were grown on AXT semi-insulating epi-ready 2" GaAs substrates. All growth was preceded by a 10-minute bake at the growth temperature under AsH_3 overpressure, followed by deposition of a 500-nm thick GaAs homoepitaxial layer. During all DMA growths, the flows of the source gases were kept constant, and only growth times were varied to effect the grading. The V/III-ratios during InP and GaAs layer growths were 270 and 20, respectively. When conventional analog graded buffers were grown, continuous linear compositional grading schemes were utilized, by constantly adjusting the TMIn and TMGa flows while keeping the AsH_3 flow constant, and the As/III-ratio varied from 35-66.

Cross-sectional transmission electron microscopy (X-TEM) was used to characterize the microstructural characteristics of the material and the layer thicknesses, while x-ray diffractometry (XRD) was used to measure film compositions, lattice-constants, and strain states, which were then correlated to the measured SL layer thicknesses. This was done using both symmetric (400) and asymmetric (422) scans.

Analysis of the XRD scans was performed assuming that Vegard's Law held for the GaAs/InP DMAs, and all relevant material parameters were obtained by linearly interpolating between the binary endpoints. Plan-view transmission electron microscopy (PV-TEM) was used to measure threading dislocation densities, and. 3ω measurements, pioneered by Cahill [25, 26], were used to assess the thermal properties of the DMAs grown.

6.3 Growth challenges

The DMA graded buffer growths reported in this work were all carried out at relatively low temperature (for MOCVD) of 450°C, as we want dislocation flow in the entire DMA structure, and not in the individual constituent layers of the DMAs. The low growth temperature also aids in suppressing the formation of 3-D islands. The main constraint that prevented us from going to lower temperatures was the poor pyrolysis of TMGa below 450°C, which would have resulted in excessively low growth rates, and which had been observed to lead to high amounts of carbon incorporation in films grown in our reactor [31]. Furthermore, as dislocation nucleation and glide are both thermally activated processes, we were concerned that poor relaxation kinetics might interfere with our goal of achieving controlled relaxation of the DMA graded buffer. Not surprisingly, growing complicated structures like DMAs entails several challenges, and the non-strain-symmetrized nature of the DMA further complicates matters. We identified and addressed several growth issues before being able to obtain DMA graded buffers that approached the design goal.

6.3.1 Intermixing of GaAs/InP

The gas switching sequence between growing alternating GaAs and InP layers had to be tailored to suppress intermixing between the DMA layers. For bulk layers, the simplest gas switching sequence to go from GaAs (InP) $\rightarrow$ InP (GaAs) would be to turn on (off) the flows of TMIn and PH_3, and turn off (on) the flows of TMGa and AsH_3 simultaneously. This would lead to a small amount of intermixing at the transition interface, typically on the order of ~2 monolayers (ML), which is generally not an issue for thicker layers. However, in our work, with targeted layer thicknesses as thin as 1 nm,

the intermixing which resulted from such a switching sequence severely affected the quality of the DMAs grown. Figure 6.2 is an X-TEM image that shows a DMA grown at 450°C and a reactor pressure of 100 Torr with such a switching sequence.

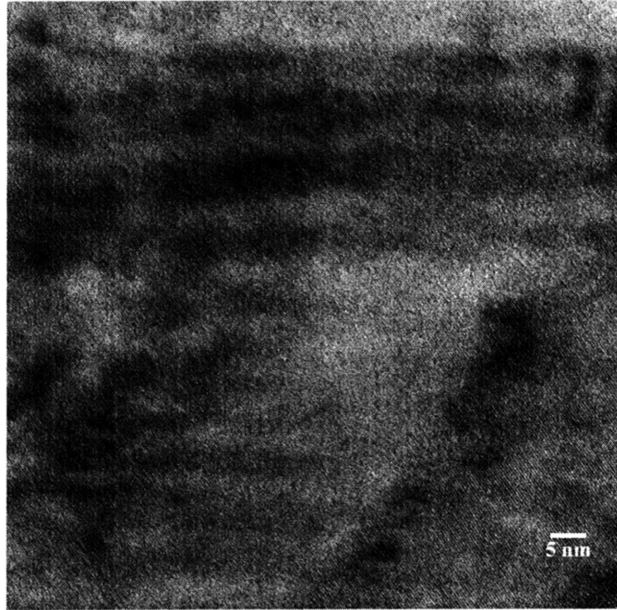


Figure 6.2 – Poor quality InP/GaAs DMA layers due to uncontrolled intermixing between the alternating InP and GaAs layers.

There is poor definition between the InP and GaAs layers, and the many different shades of contrast indicate the presence of intermixing between the species, effectively forming regions of InGaAsP alloys of varying compositions. This is clearly undesirable, as it means that a significant volume of the material is either a ternary or a quaternary alloy, which detracts from our aim of an all-binary structure. We investigated various growth conditions and gas switching sequences, and eventually found that what appeared to work best, and most reproducibly, was the inclusion of a 3 s pause between each layer, and a reduction of the reactor pressure to 50 Torr during SL growth. Figure 6.3 is a schematic diagram showing how the different gas switching schemes were carried out. It is evident that the growth pauses add significantly to the total growth time, but they are necessary to ensure good SL quality.

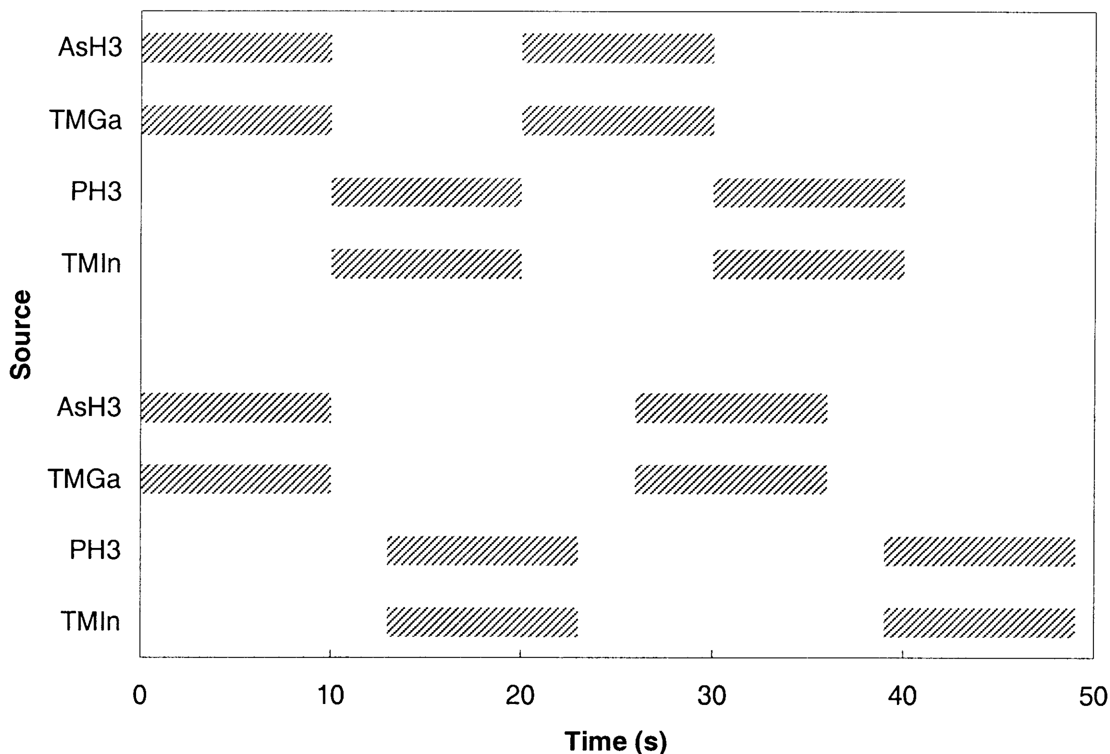


Figure 6.3 – Schematic of the original and modified gas switching sequences. The latter was used to cut down on intermixing between the InP and GaAs layers.

We believe these actions helped sweep the excess precursor species from a given layer out of the reaction chamber, ensuring that when growth of the subsequent layer started, it was done with only the appropriate species present in the gas phase, thereby reducing the amount of intermixing. By keeping our gas flows nominally the same, the reduced reactor pressure led to a shorter transit time of the gas species in the reaction chamber, and the length of the growth pause is estimated to be approximately the amount of time it takes to sweep the entire volume of our reaction chamber at 50 Torr.

6.3.2 Growth rate variation

Another challenge that had to be overcome was an unexpected variation in the growth rates of the InP and GaAs layers that make up the DMAs. In all the DMA growths, we controlled the layer thicknesses by keeping the source gas flows the same and varying the growth times for a given layer. We observed however that while growth rates of a given layer (i.e. InP or GaAs) were relatively constant from period to period within a given DMA, there was a strong dependence of the growth rate on which DMA it

was in. Figure 6.4 plots the trends we observed for InP and GaAs layer growth rates as a function of the composition (in terms of percentage, by thickness, of InP) of the underlying DMA. The data is presented this way because we expect each DMA to behave as a single, mechanically-uniform layer, and so the x-axis serves as a proxy for the in-plane lattice constant that the constituent InP and GaAs layers "see" during their growth. We note at this point, but elaborate later, that the data includes DMAs with different degrees of relaxation, which means that their compositions as measured by relative layer thicknesses are not entirely accurate, due to the distortion of the crystal lattice. We are also therefore unable to precisely determine the in-plane lattice-constant and mismatch that the InP and GaAs layers experience. We believe that this leads to the relatively large scatter in the data when the growth rates are plotted against DMA composition as has been done here.

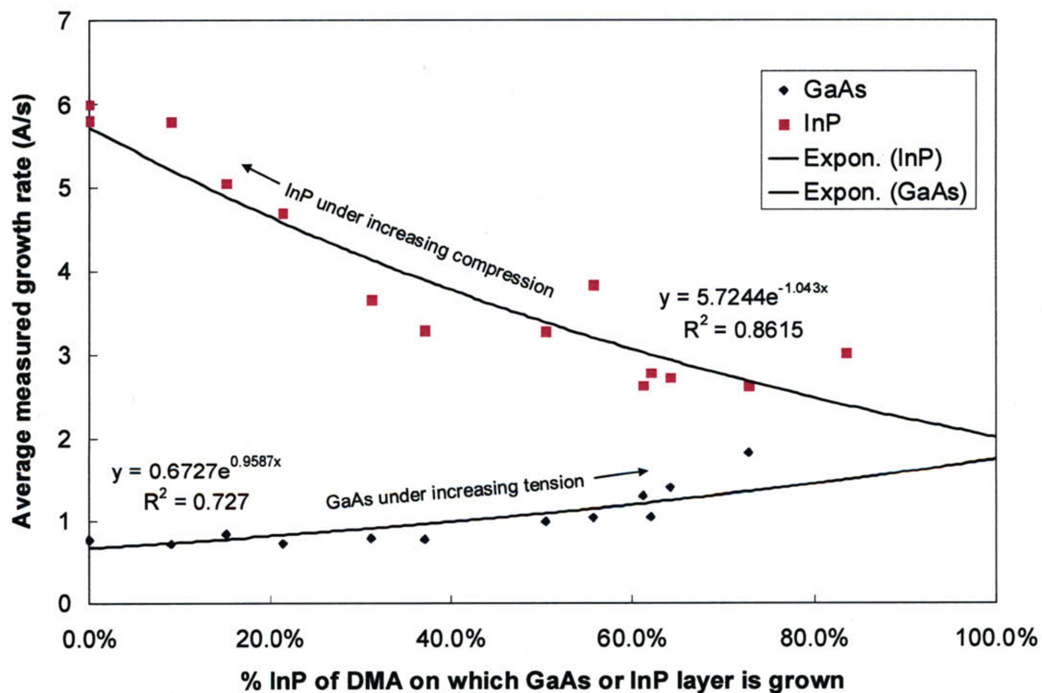


Figure 6.4 – Graph depicting the growth rate trends observed for InP and GaAs layers as a function of which DMA they are being grown on.

As can be seen, the growth rate of the InP layers appears to decrease exponentially as a function of the composition of the underlying DMA, while the GaAs layer growth rate increases exponentially, albeit in a slower fashion. As III-V growth

rates in MOCVD are typically limited by the Group-III species due to the presence of an excess Group-V overpressure, we naturally look towards factors that could influence the behavior of the In and Ga precursors to explain the observation. The low growth temperature of 450°C usually suggests that changing pyrolysis rates of the metalorganics (TMGa and TMIn), due to fluctuations in the wafer surface temperature, might be involved, thus affecting the layer growth rates [27]. However, the two divergent trends for InP and GaAs do not support this, and instead, suggest that the phenomena might be related to strain, given that the two layer experience biaxial strains in opposing directions (compression for InP and tension for GaAs). (An alternative explanation that might occur to some is that the growth rate depends on layer thickness, reflecting the presence of an incubation time, since for DMAs at lower InP compositions, the desired InP layer thicknesses are lower and GaAs layer thicknesses are higher. However, this is clearly not the case, as from Table 6.2, one can see that for InP layers, the targeted thicknesses remain constant at 1 nm for DMA compositions up to 50% InP, and likewise for GaAs layers, the targeted thicknesses are maintained at 1 nm for DMA compositions above 50% InP, and these composition ranges are where we observe the greatest changes in the growth rates of each of the layers).

To begin our analysis, we can consider the effect of biaxial compression on the out-of-plane lattice-constant (i.e. in the growth direction) of InP. For InP, the elastic constants are C_{11} = 122.1 GPa and C_{12} = 56.6 GPa, which results in a 2D Poisson's ratio of

$$\nu = 2\frac{C_{12}}{C_{11}} = 0.9271 \tag{6.3}$$

For a cubic crystal, the relationship between the Poisson's ratio, the in-plane (parallel) lattice-constant and the out-of-plane (perpendicular) lattice-constant is

$$a_{relaxed} = \frac{a_{\perp} + \nu \cdot a_{//}}{1+\nu} \tag{6.4}$$

Thus, assuming a thin InP layer is grown on GaAs, and remains fully strained, we have

$$a_{\perp} = (1+\nu)\cdot a_{InP} - \nu \cdot a_{GaAs} \tag{6.5}$$

Substituting the values a_{InP} = 5.8697 Å and a_{GaAs} = 5.6533 Å, we obtain an out-of-plane lattice-constant of 6.0703 Å for the fully-strained InP thin film, which represents a 3.4% increase over the equilibrium (relaxed) lattice-constant. We therefore note that while biaxial strain can serve to distort the layer thickness measurements obtained through X-TEM, their magnitude is small relative to the growth rate variations seen, and therefore the phenomenon of growth rate variation is real.

Kruger *et al* previously found that the growth rates and the incorporation rates of In relative to Ga in their InGaN quantum wells (QWs) appeared to vary as more wells were grown in a MQW structure, which they attributed to the increase in compressive strain in the system as additional QWs were grown [86]. While they were able to observe that growth rates increased with increasing strain, they did not explicitly state a trend in the In incorporation with strain, and therefore it is not clear if the growth rate increase was related in any way to a lattice-constant increase in the film due to higher In content. Due to our use of all-binary layers, however, we can decouple the growth rate variation from any compositional effects on the lattice-constant, and our results suggest that in situations where a grown InP layer would experience higher compressive strain, such as nearer the start of growth where the lattice-constant is closer to the GaAs substrate, its growth rate is dramatically increased. This is somewhat consistent with Kruger *et al*'s findings [86]. In the case of GaAs layers, it appears that when they are grown under high tensile stress, their growth rates are increased, and therefore it seems that high strain conditions lead to enhanced growth rates for films that are grown with the *same sign of strain*. The origin of this effect is unclear, since from the standpoint of minimization of system energy, it would be favorable for the trends to be reversed – i.e. under higher strain conditions, the system would seek to suppress layer growth that would lead to even higher strain build up, and instead favor layer growth that would lead to a reduction in the overall strain. Explanations that have been invoked for energetically unfavorable (in the bulk) segregation and clustering in ternary and quaternary alloys generally have focused on local non-equilibrium conditions at the surface such as surface roughness and local strain variations due to different cation-anion bonds present in the alloys [87, 88]. However, these do not appear to be relevant here as we are dealing with the growth of binary compounds, which means that the local variation of incorporation rates of a cation (or

anion) species over another is not an issue. Furthermore, we can also rule out the effects of the surface-type on the growth rates, since the InP layers are always grown on GaAs surfaces, and vice versa, in contrast with conventional growth of binary layers on analog buffers (e.g. InP growth on InGaAs buffers), where different strain conditions are always accompanied by different surface species.

While we are unable to speculate on the exact physics, we surmise that the varying effective mismatch between the layer being deposited and the growth surface at different points in the DMA graded buffer is responsible for this effect, given that this is the main difference between the present work and conventional strain-balanced or unstrained SLs, where growth rate variations have not been reported. In fact, the observed growth trends might be an indication of the physics behind two other surface-related phenomena – those of cross-hatch formation and phase separation due to the effect of strain on the growth surface, the latter of which was observed in Chapter 3. Strain fields associated with misfit dislocations have been known to lead to local growth rate variations, leading to characteristic undulations on the surface known as cross-hatch [89-91], though the explicit effect the strain fields have on the growth rate have not be fully understood. Our results appear to indicate that for a surface with regions under both compressive and tensile strain, growth of a compressively-strained layer would be enhanced at regions under compressive strain and depressed at regions under tensile strain, while the reverse would be expected for the growth of a tensile-strained layer. This might also explain the differences in surface morphology between tensile- and compressive-graded buffers that have been observed by others [55]. Extending this analysis, we might also be touching upon the mechanism for phase separation. During graded buffer growth in a ternary alloy system such as InGaAs, the component binaries InAs and GaAs would in general experience opposite signs of strain on a given growth surface. The phenomena observed in this work would suggest that regions of the surface under compressive strain would see enhanced In incorporation, while regions of the surface under tensile strain would similarly see enhanced Ga incorporation. This would lead to phase separation of the ternary alloy into In-rich and Ga-rich regions. Thus, strain fields of larger magnitudes can be expected to increase the likelihood of phase separation

occurring, which is consistent with the increased phase separation observed for faster grade rates [38].

Ultimately, it is clear that small growth variations in earlier DMAs can lead to differences in the thicknesses and strain states of the subsequent DMAs, as the InP and GaAs layer growth rates would be affected in non-linear ways. Thus, growth rate control in the strained DMA system is not easily achieved, and must be characterized over multiple iterations, due to the interplay between growth rate, layer thickness, digital alloy composition, degree of relaxation and lattice-constant.

6.3.3 Critical thickness constraints

Solving the intermixing issue enables us to get well-defined DMA layers, and characterizing the growth rates of the InP and GaAs layers at any point in the DMA graded buffer allows us to accurately construct SLs of the appropriate composition but another aspect of DMA growth that we found to be important for a good DMA graded buffer was to ensure that the individual layers do not reach their individual critical thicknesses and start to relax independently of each other. Figure 6.5 is a X-TEM image of a DMA graded buffer grown on a GaAs substrate that was inadvertently grown with an InP layer thickness of approximately 2.5 nm for the first DMA on the GaAs homolayer.

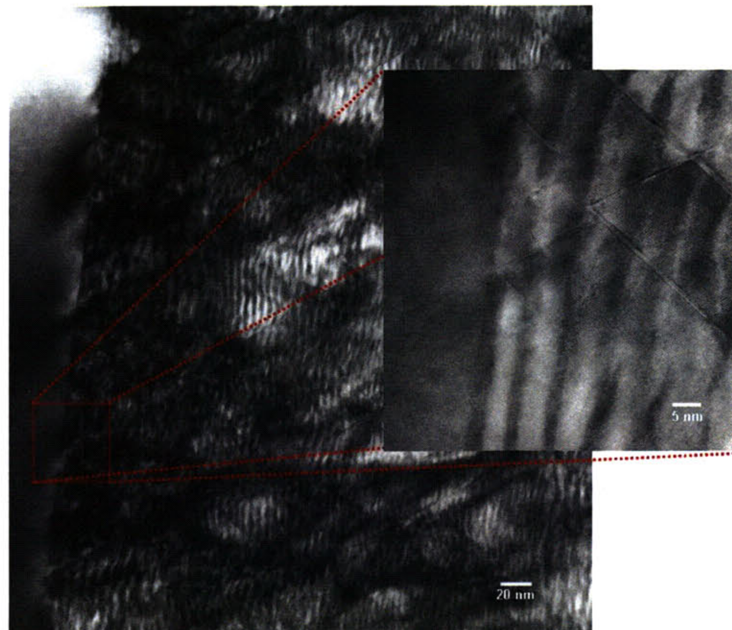


Figure 6.5 –X-TEM image showing the effect of growing DMA layers beyond critical thickness limits.

From Table 6.2, we observe that this is beyond the critical thickness of InP on GaAs, and therefore relaxation of the InP is expected. It is clear that the uncontrolled relaxation of the InP layer resulted in many defects propagating through the entire DMA structure, which also contributed to the rapid roughening of subsequent DMA layers. It is interesting to note from Figure 6.5 (inset) that the defects are predominantly stacking faults, and they appear to originate in the InP layers, which is surprising, since it is usually tensile strain that leads to the separation of dislocations into two partial dislocations, resulting in stacking faults. This highlights the importance of keeping layers well below the critical thickness, but as a result, it also places practical limits on the design and growth of a DMA graded buffer.

First, it can be seen that the 3.7% lattice-mismatch between GaAs and InP means that the use of these layers to bridge the lattice-constants of the same binary endpoints results in minimum critical thicknesses on the order of 1 nm (again, see Table 6.2). This means that growth must be controlled to that level of accuracy, which likely places limits on the maximum growth rate that can be achievable. Furthermore, it also increases the number of periods necessary to achieve a certain grade rate (recall that this is determined by the total thickness of each DMA), and, as a growth pause is necessary when switching between InP and GaAs growth, this leads to overall longer growth times. In our case, growth times of three or more hours were common, depending on how far the DMA graded buffer was graded.

Second, the critical thickness limit also restricts the choices of materials usable for the DMA graded buffer. In theory, the all-binary DMA concept can be applied with any two binary compounds, as long as their lattice-constants span at least as wide a range as those of the desired start- and end-points (GaAs and InP respectively, in this case). Based solely on this criterion, we investigated a DMA graded buffer using InP and GaP as the constituent layers of the DMAs, to see if the absence of any anion intermixing effects would make any difference. The critical thickness of GaP on GaAs is ~11 Å, and it decreases as we move towards lattice-constants closer to InP. As the lattice-constant of GaAs is almost exactly midway between GaP and InP, we started with a nominally 1 nm:0.95 nm GaP:InP DMA, which would have an effective lattice-constant almost equivalent to GaAs. Following that, the thickness of the InP layer was increased

accordingly, while the thickness of the GaP layer was maintained at 1 nm, until the DMA graded buffer was graded to InP. Each DMA was designed to have a total thickness of 100 nm. Figure 6.6 is a X-TEM image of this sample.

Figure 6.6 – X-TEM image depicting a DMA graded buffer constructed with InP and GaP layers. The GaAs substrate is at the bottom.

The image in Figure 6.6 is centered on the first three DMAs, which look somewhat better than the rest of the DMAs, and are most easily identified. The total thickness of each of the first three DMAs are approximately only half the thickness expected. As this was a unique experiment utilizing GaP/InP DMAs, we used identical TMGa and TMIn gas flows as in the case of the GaAs/InP DMAs, and assumed the same growth rate values that were presented in Table 6.2. The fact that the growth rates were not as predicted suggests that once again, there was a growth rate variation due to the mismatch present between the growth surface and the GaP and InP layers. Due to the poor quality of the layers, accurate measurement of the individual layer thicknesses was not possible, especially for the first few DMAs which were composed of layers that were only 1-2 nm thick by design. In fact, they were likely highly intermixed, and essentially ternary alloys, which might explain the lack of signs of relaxation such as those in Figure 6.5. Furthermore, XRD of the (400) family of planes (not shown here) revealed three weak peaks apart from the GaAs substrate and InP cap peaks, corresponding to

$In_{0.34}Ga_{0.66}P$, $In_{0.51}Ga_{0.49}P$ and $In_{0.68}Ga_{0.32}P$. While not entirely accurate, since the films are not necessarily fully relaxed, the fact that the second DMA seems to be roughly lattice-matched to the GaAs substrate, and also that the third DMA is the first with a lattice-constant larger than GaAs would suggest that GaP films on the order of ~1 nm would start to relax uncontrollably starting after the third DMA. This is likely the reason for the drastic increase in defect density starting from the fourth DMA in Figure 6.6. X-TEM images at higher magnification (not shown here) also confirmed that the GaP and InP layers were more distinct from the fourth SL onwards, and stacking faults were once again visible starting from this point.

6.4 Results

The preceding sections detailed the keys to successful growth of the DMAs. By applying them, we grew DMA graded buffers to varying compositions. The work reported in this section all utilize the grading scheme detailed in Table 6.2, unless otherwise noted. Table 6.3 lists the DMAs discussed in this section.

DMA graded buffer	Final composition (% InP)	Capped?
DMAGB1	30%	No
DMAGB2	60%	43% InGaAs
DMAGB3	100%	InP
DMAGB4 (Hybrid)	100%	InP
DMAGB5 (Hybrid)	100%	InP

Table 6.3 – Summary of DMA graded buffers discussed in this section.

6.4.1 DMAGB1 – DMA graded buffer to low (30%) InP composition; uncapped

We grew DMAGB1, which consisted of the first three DMAs listed in Table 6.2, using optimized growth conditions and times. Figure 6.7 is an X-TEM image of DMAGB1, while Table 6.4 contains XRD data from this sample.

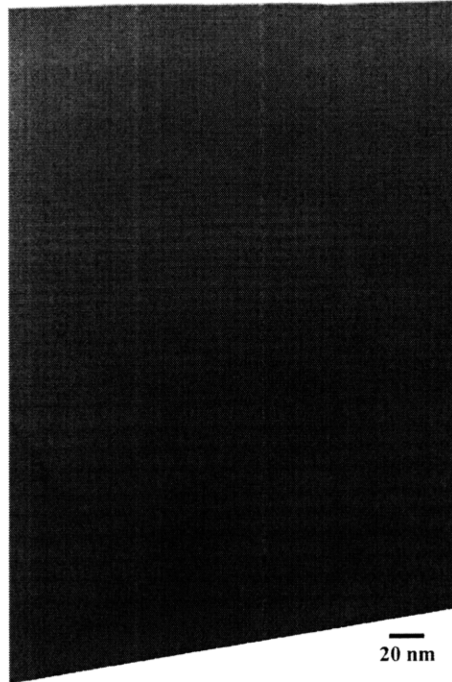


Figure 6.7 – X-TEM image of DMAGB1 with three different DMAs, grown to a terminal composition of approximately 30% InP.

Peak	Relaxed lattice-constant (Å)	Relaxation	%InP in DMA (XRD)	%InP in DMA (XRD; out-of-plane)	%InP in DMA (X-TEM)
DMA1	5.6653	-0.09%	5.55%	11.89%	13.73%
DMA2	5.6805	4.72%	12.58%	22.32%	23.07%
DMA3	5.6963	4.01%	19.91%	36.73%	34.94%
92% InP	5.8542	99.15%	N/A	N/A	N/A

Table 6.4 – Summary of XRD and X-TEM measurements of DMAGB1.

The X-TEM image shows relatively flat and well-defined layers, and the three DMAs can be readily identified, though there is slight variation in the layer thicknesses within each DMA. We attribute this to poor heater control during the growth, which led to temperature swings of ±3°C during the growth. While this image is taken in an on-pole condition, images taken in a g = <022> two-beam diffraction mode for enhanced dislocation contrast revealed few signs of misfits which would signify layer SL relaxation. The XRD data confirms this – three peaks that were attributable to the three different DMAs could be found in both the symmetric (400) and asymmetric (422) scans that were taken, and all three were found to exhibit negligible amounts of relaxation. The apparent discrepancy between the DMA compositions as measured by XRD (column 4 in Table 6.3) and those as calculated from measured layer thicknesses in X-TEM (column 6

in Table 6.3) can be explained by the effects of biaxial strain on the fully-strained layers. As the XRD data of the out-of-plane lattice-constant shows, there is much better agreement between the equivalent DMA compositions obtained from the out-of-plane lattice-constant (column 5 in Table 6.3), and those obtained through X-TEM. This, however, reveals a complication in controlling DMA growth. Our grading scheme is predicated on the assumption that we can control the composition of each DMA by paying attention to the GaAs and InP layer thicknesses within the DMAs. However, we see here the dramatic effect residual strain has on the relationship between layer thicknesses and the relative atomic mole fractions of GaAs in InP in the DMAs. This means that an optimized growth process has to take into account the strain states of the DMAs, and that the growth times must be adjusted based on this. However, as we shall see shortly, accurate information of the strain state, which is only obtainable through XRD measurements, is not always available, because when the DMAs start to relax (which is in fact what we desire), the strength of the XRD signals from the DMAs start to weaken, due to their reduced coherency. Due to this fact, all of the growths reported here were still designed according to data obtained through layer thickness measurements (with slight adjustments according to available strain state information), and assumptions about DMA compositions were checked when meaningful XRD data was available.

A final observation is that there is a last peak in each of the XRD scans that correspond to an almost fully-relaxed layer that is 92% InP, 8% GaAs by composition. This peak is actually a feature that is common to all of our GaAs/InP DMA growths, and is often one of the strongest peaks apart from the substrate, which suggests that it is the aggregated signal from all the individual InP layers in the various DMAs. Its almost fully-relaxed state, even in samples like this one where the DMAs are almost fully-strained, is puzzling, however, and needs to be investigated further.

6.4.2 DMAGB2 – DMA graded buffer to moderate (60%) InP composition; capped with $In_{0.43}Ga_{0.57}As$

We investigated grading further in DMAGB2, to approximately 60% InP according to layer thickness measurements, and attempted to cap it with a lattice-matched InGaAs layer. If the DMA composition was accurate and fully-relaxed, it would possess

the lattice-constant of $In_{0.32}Ga_{0.68}As$, which, as we observed in Chapter 3, is close to the composition at which phase separation in the InGaAs alloy becomes a problem. Figure 6.8 depicts DMAGB2, while Table 6.5 summarizes the data we were able to obtain from XRD measurements and X-TEM.

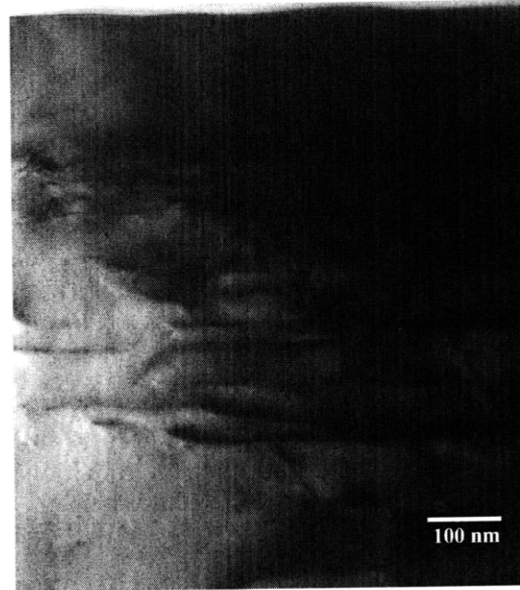


Figure 6.8 – X-TEM image of DMAGB2, graded up to 60% InP, capped with InGaAs.

Peak	Relaxed lattice-constant (Å)	Relaxation	%InP in DMA (XRD)	%InP in DMA (XRD; out-of-plane)	%InP in DMA (X-TEM)
DMA1	5.6772	97.74%	11.05%	10.46%	12.55%
DMA2	5.7329	83.79%	19.03%	21.57%	25.71%
DMA3	N/A	N/A	No peak	No peak	32.16%
DMA4	N/A	N/A	No peak	No peak	44.04%
DMA5	N/A	N/A	No peak	No peak	48.18%
DMA6	N/A	N/A	No peak	57.48%	55.36%
43% InGaAs	5.8284	82.84%	N/A	N/A	N/A
94% InP	5.8564	99.95%	N/A	N/A	N/A

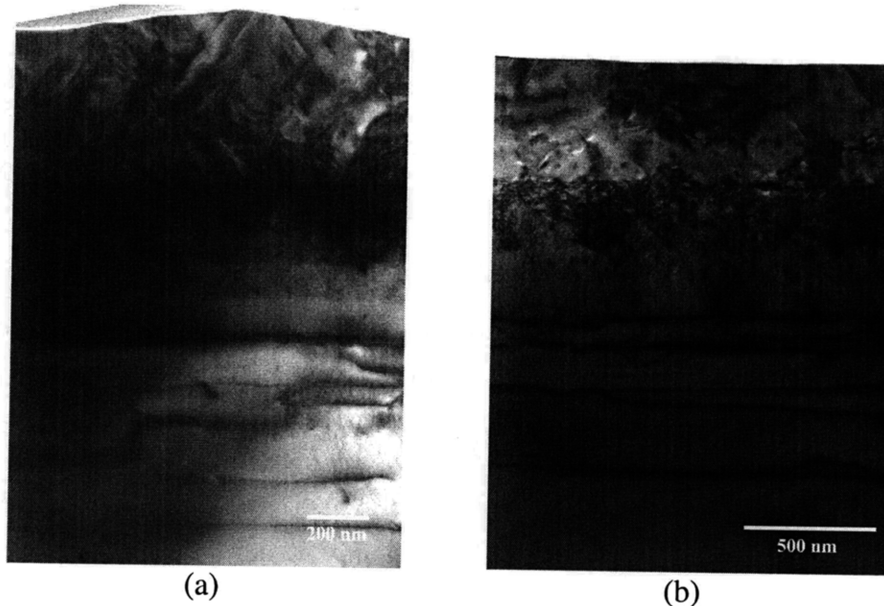
Table 6.5 – Summary of XRD and X-TEM measurements of DMAGB2.

Clearly, while DMA_1 remained fully-strained, the various DMAs of DMA_2 experienced significant amounts of relaxation. This is likely attributable to the increased amounts of strain built up by the additional DMAs, not to mention the InGaAs cap layer which was significantly more compressively strained than expected. It appears from Figure 6.8 that there is a higher density of misfits at the junctions of the various DMAs, as compared to regions within a given DMA, especially earlier on where less strain has built up. This suggests that each DMA is indeed behaving somewhat like a discrete mechanically-uniform material, and thus the relaxation initiates at the start of each DMA.

Also, there appears to be a higher concentration of misfits, signaling increased relaxation, in the latter DMAs. This might explain why DMA peaks for the latter DMAs were not readily observable in XRD, especially in the (422) scans, as theDMAs are no longer as coherent. However, since one would expect the relaxation to initiate from the earlier layers, it appears that relaxation in this case might be driven by the highly mismatched InGaAs cap layer, and we speculate that the DMAs closer to the surface might actually be "screening" those closer to the substrate, leading to the misfit network characteristics observed in this sample. Nevertheless, we believe that the presence of a decent looking InGaAs cap, despite the lack of proper lattice-matching, at least hints at the viability of the DMA graded buffer.

6.4.3 DMAGB3 – DMA graded buffer to InP; annealed

DMAGB3 was a full structure as laid out in Table 6.2, and included an approximately 400-nm thick InP cap. After growth, the sample was retrieved from the MOCVD reactor, and cleaved into two halves, one of which was returned to the reactor to be annealed. We started to flow PH_3 at 250°C, and from that point on, the temperature was ramped up to 650°C over 6 min. After reaching 650°C, the sample was annealed in the PH_3 ambient for a further 20 min, before being cooled. Figures 6.9(a) and (b) are X-TEM images of DMAGB3 before and after annealing, respectively.



Figures 6.9(a) and (b) – X-TEM images of DMAGB3, (a) as-grown and (b) after annealing.

As grown, DMAGB3 had a very rough surface, and can be seen in Figure 6.9(a), with the InP cap layer exhibiting large densities of stacking faults and other extended defects. While there were clear signs of misfits forming in the first four or five DMAs, they did not seem to be present in the same form in the later DMAs. Higher magnifications images of the DMAs revealed that the fifth and sixth DMAs were relatively clean and free of defects, but the seventh through ninth DMAs had numerous stacking faults running through them Also, the GaAs and InP layers in the first five DMAs were relatively flat and distinct, but starting from the sixth onwards, they became increasingly undulated, and thus accurate measurements of their layer thicknesses were not possible. No DMA peaks were visible in the (422) XRD scan, and only five were seen in the (400) XRD scan. The anneal at 650°C appeared to improve the surface morphology greatly, likely due to thermal deformation of the InP at high temperatures, which has been found to result in flatter InP surfaces [92]. Crystalline quality was also improved, as evidenced by the reduction of the stacking fault density in the InP cap. However, from X-TEM, the DMAs did not appear to be significantly changed, in terms of layer thicknesses, the misfit networks and the defects present. There was also no sign of increased intermixing between the SL layers, which means that bulk diffusion is negligible at 650°C. The biggest difference was in the XRD scans, however. Peaks attributable to most of the DMAs could be observed fairly readily after the anneal. The post-anneal results, together with available measured layer thicknesses, are tabulated in Table 6.6. Given that increased DMA relaxation is expected to reduce peak intensity, this suggests that the anneal did not significantly drive DMA relaxation as we had hoped, and the main effect it had was the improvement of the quality of the InP cap. We note here that for uncapped DMA graded buffer samples (not shown here), anneals served to greatly roughen the surface, which we attribute to significant intermixing of the thin GaAs and InP layers that result from high surface diffusivities.

Peak	Relaxed lattice-constant (Å)	Relaxation	%InP in DMA (XRD)	%InP in DMA (XRD; out-of-plane)	%InP in DMA (X-TEM)
DMA1	5.6629	37.25%	4.45%	6.07%	7.42%
DMA2	5.6733	34.14%	9.25%	14.08%	12.16%
DMA3	5.6867	41.86%	15.44%	24.63%	26.33%
DMA4	5.7045	66.98%	23.70%	32.04%	30.00%
DMA5	5.7168	55.37%	29.38%	41.01%	42.25%
DMA6	5.7295	52.46%	35.23%	51.31%	Not measurable
DMA7	5.7454	46.30%	42.55%	64.00%	Not measurable
DMA8	5.7597	48.45%	49.17%	72.97%	Not measurable
DMA9	N/A	N/A	No peak	No peak	Not measurable
InP	5.8686	99.95%	N/A	N/A	N/A

Table 6.6 – Summary of XRD and X-TEM measurements of DMAGB3 after annealing.

Here, we see clearly the problem with designing the growth around measured DMA layer thicknesses. While there is no data for DMA9, it is likely that after the final DMA, we are at a digital alloy composition of no more than 55% InP. The low relaxation values of the DMAs further mean that the in-plane lattice-constant of the topmost DMA is significantly smaller than that of InP. It is therefore no surprise that the InP cap deposited at the top of the DMA is highly defective, due to the large effective lattice-mismatch. Another observation we can draw from the data is that the DMA relaxation peaks at about 67% for DMA4, which is right in the middle of the DMA structure. This is somewhat consistent with what we observed for DMAGB1, where DMAs up to 30% InP did not undergo relaxation, and from these observations, it appears that at the grading rate present in our DMAs (approximately 1.9% strain/µm, or half of the originally intended 3.7% strain/µm), it is only preferential for plastic deformation of the DMAs to occur after DMA4 is grown. It further appears that a given DMA's relaxation is in fact driven by the increasing tensile strain it experiences from the DMAs grown after it.

6.4.4 DMAGB4 and DMAGB5 – Hybrid conventional graded buffer + DMA graded buffer; capped with InP

From the previous results, it is clear that control over the composition and relaxation must be improved for the DMA graded buffer to achieve its full potential. Nevertheless, to ascertain the usefulness of the DMAs in allowing us to circumvent the problem of phase separation in the ternary InGaAs alloy, we grew a hybrid InGaAs

graded buffer plus DMA graded buffer structure. The intention was to start with a high quality virtual substrate capped with $In_{0.32}Ga_{0.68}As$, before phase separation of the InGaAs alloy occurs, and continue grading towards InP with a DMA graded buffer comprising three DMAs. Details of the InGaAs graded buffer growth can be found in Chapter 3. After graded the graded buffer growth was carried out at 700°C, the temperature was ramped down to 450°C, while maintaining an AsH_3 overpressure over the wafer. At 450°C, a 150-nm lattice-matched InGaAs layer was grown, followed by the DMAs of nominally 70%, 80% and 90% InP. This was followed by a 400-nm thick InP cap, also grown at 450°C. To try to encourage better DMA relaxation, the grading rate was reduced to a third of that described in Table 6.2, by tripling the number of periods in each SL. An XRD reciprocal space map of the (400) family of planes is shown in Figure 6.10, while an X-TEM image of the top of the hybrid InGaAs graded buffer plus DMA graded buffer is shown in Figure 6.11.

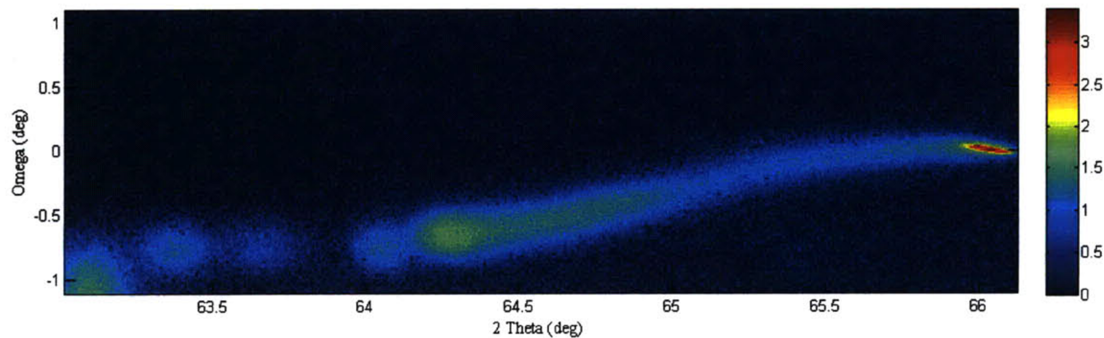


Figure 6.10 – XRD reciprocal space map of (400) family of planes for DMAGB4, a hybrid InGaAs random-alloy graded buffer + DMA graded buffer.

Figure 6.11 – X-TEM image of DMAGB4, a hybrid InGaAs random-alloy graded buffer + DMA graded buffer.

The continuous XRD signal spanning 2θ values of approximately 64.25° to 66.00° is characteristic of the continuously-graded InGaAs random-alloy buffer, witht the peak at 64.25° corresponding to the InGaAs graded buffer cap. The four distinct peaks to the left of that represent, from right to left, the three DMAs and the InP cap. XRD revealed that the actual composition of the final DMA was 79.12% InP, and that it was 78.03% relaxed, which meant that there was still a large effective lattice-mismatch between the InP cap and the topmost DMA. However, the InP cap in this sample appeared to be free of threading dislocation throughout the X-TEM foil, which means that the hybrid structure could potentially have a low TDD. This is in contrast with the InP cap of DMAGB3, which was grown at the same temperature, but exhibited a large number of defects both pre- and post-anneal. We believe that the difference is due to the more complete (in terms of bridging the lattice-mismatch) grading present in DMAGB4, even though it is also by no means optimal. Meaningful PV-TEM analysis could not be carried out on this sample, as the thin cap meant that underlying misfits would be visible in the TEM foil and interfere with the measurement. A new sample, DMAGB5, was grown, where the only difference was an additional high temperature (650°C) InP growth

step at the very end, to obtain a smoother and thicker InP cap. The result is depicted in Figure 6.12.

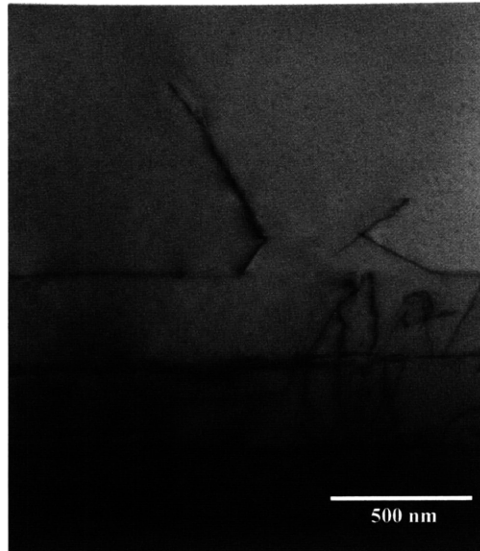


Figure 6.12 – X-TEM image showing the top of DMAGB5.

The InP cap layer in DMAGB5 was thicker and smoother, but there were a significant number of threads present in the cap as well. Also, the DMA layers showed many more signs of not just misfits, but dislocation loops as well, suggesting uncontrolled relaxation of the DMAs had occurred, leading to the high TDD. PV-TEM was carried out on DMAGB5, and numerous dislocation pileups were detected, leading to a measured TDD of 1.7×10^8 cm^{-2}. Clearly, the high temperature InP growth, which in fact amounted to an anneal of the SLs, was not optimized, leading to the nucleation of a large number of dislocations which ruined the material quality. The effect of the anneal on DMAGB3 did not appear to lead to such a dramatic worsening in material quality, but we believe that that was because the as-grown material quality in DMAGB3 was poor to begin with.

6.4.5 Thermal conductivity measurements

While the growth of the DMA structures needs to be further optimized, the present material available is sufficient for us to examine the thermal characteristics of the DMAs. We deposited 40-μm wide metal lines comprising 100 nm of Ti followed by 5 nm of Au on DMAGB4, to use as heaters for 3ω measurements to quantify the thermal conductivity of the DMA structure. For comparison, identical heater lines were deposited

on a sample which only had a conventional analog InGaAs graded buffer that was similar to the one in DMAGB4. Figures 6.13 and 6.14 show the ΔT vs. angular frequency curves obtained using the 3ω method for the analog graded buffer only sample, and DMAGB4, respectively. It should be noted at this point that our structures and heater lines are not optimized for 3ω measurements. The main reason is the multitude of layers with poor thermal resistances present, which have a significant thickness and therefore thermal resistance associated with them. This means that they are not really expected to behave like the prototypical 3ω samples (i.e. single bulk substrate, or single thin film on bulk substrate).

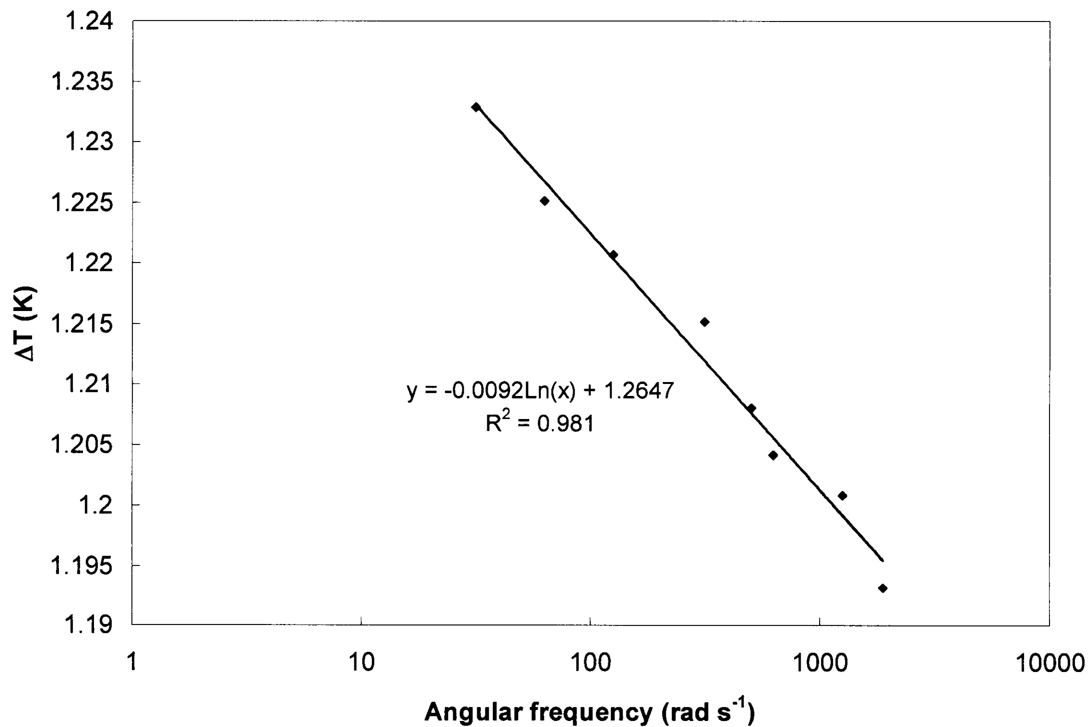


Figure 6.13 – Plot of temperature rise vs. angular frequency from 3ω measurement of conventional analog InGaAs graded buffer.

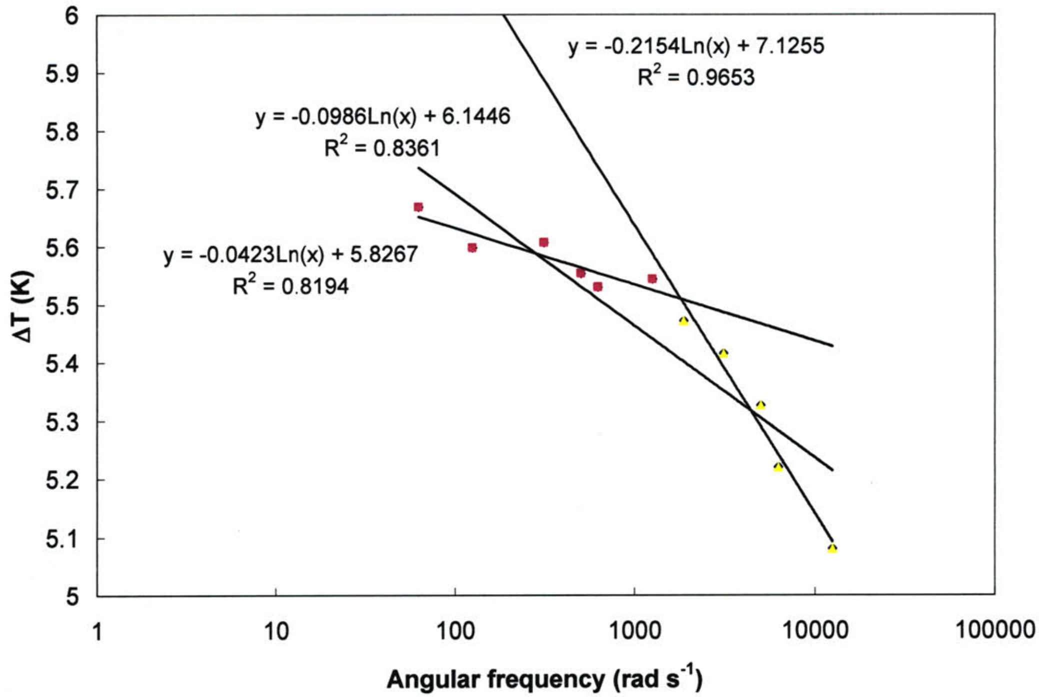


Figure 6.14 – Plot of temperature rise vs. angular frequency from 3ω measurement of DMAGB4.

From the slope of the graph in Figure 6.13, we obtain an effective thermal conductivity of 31.5 $Wm^{-1}K^{-1}$, which is significantly lower than the reported value of 55 $Wm^{-1}K^{-1}$ for GaAs. Thus, we conclude that the sample does not behave like a single thin film. If we assume that the GaAs substrate and the InGaAs graded buffer (referred to as GB from here on) are two thermal resistances in series, with perfect interfacial conductance then

$$\left(\frac{k_{GaAs}}{t_{GaAs}}\right)^{-1} + \left(\frac{k_{GB}}{t_{GB}}\right)^{-1} = \left(\frac{k_{tot}}{t_{tot}}\right)^{-1} \tag{6.6}$$

Substituting the values k_{GaAs} = 55 $Wm^{-1}K^{-1}$, t_{GaAs} = 350 μm, k_{tot} = 31.5 $Wm^{-1}K^{-1}$, t_{tot} = 355.5 μm, and t_{GB} = 5.5 μm, we obtain a rough estimate of k_{GB} = 1.12 $Wm^{-1}K^{-1}$, which seems fairly reasonable for a structure filled with dislocations. Now, a range of gradients can be obtained from the temperature rise vs. frequency data for DMAGB4 in Figure 6.14. They result in total effective thermal conductivity values ranging from 3.2-16.3 $Wm^{-1}K^{-1}$. We believe that the lower frequency range, corresponding to the greatest thermal penetration depth, would be the most "accurate" number. However, we can easily calculate the range of expected values for k_{DMA}. Using an analogous formula to

Equation (6.6), we calculate that k_{DMA} should range from 0.01-0.094 $Wm^{-1}K^{-1}$. While this analysis is very rough and likely to be highly inaccurate, if we take it at face value, it does suggest that the DMAGB4, as it stands, does not give us the desired gains in thermal conductivity. However, it should be noted that X-TEMs of DMAGB4 at higher magnification revealed that the layers were rather rough, including the presence of a significant amount of misfits and other extended defects, and since we ignored all the effects of interfacial thermal resistance, a properly grown DMA might possess far superior thermal characteristics.

6.5 Summary

In summary, we have demonstrated a novel concept to achieve metamorphic grading using only binary III-V compounds. The keys to successful DMA growth include obeying critical thickness limits and controlling constituent layer thicknesses to construct DMAs that behave similarly mechanically as the desired random alloy, both of which require a thorough characterization of the growth rate dependencies on strain/underlying surface. When dealing with DMAs encompassing a large mismatch, such as grading from GaAs to InP, the preferred embodiment of the GaAs/InP DMAs described here are achieved by performing anneals at multiple stages to drive DMA relaxation. If periodic anneals are not performed, rampant dislocation nucleation will eventually occur. Therefore, when grading over a large lattice-constant range (GaAs lattice-constant to InP lattice-constant), periodic annealing is required. Although the examples shown utilize binary constituent layers of GaAs and InP in the DMAs, the concept can be equally applied to other binary and elemental semiconductors, as we have noted above, with similar advantages realized in all material systems. Hybrid structures combining conventional random-alloys with DMAs to form graded buffers have also been demonstrated, and confirm that DMAs also allow us to circumvent materials growth issues such as phase separation and ordering.

7. SUMMARY OF RESULTS; SUGGESTIONS FOR FUTURE WORK

This thesis has been about finding a way to bridge the lattice-constant gap that exists between the two most ubiquitous III-V semiconductors, GaAs and InP, with two overall goals in mind. The first is to solve a small part of the giant puzzle that is how to integrate all the material systems in the III-V space, with heterovalent integration with the Group-IV semiconductors the goal beyond that. Should we succeed, we can finally claim to have fully circumvented the lattice-matching constraint of epitaxy. The second, and more focused aim, was to gain access to the wide range of InAlGaAs alloys in the rich design space between GaAs and InP, which hold the promise for the design of devices with new functionalities and improved performances.

7.1 Research highlights

We believe that we have successfully contributed towards both goals, and our key achievements, which have been detailed in the preceding chapters, are highlighted individually below.

7.1.1 High quality compositionally-graded metamorphic InGaAs buffers

We were able to utilize and advance the knowledge about graded $In_xGa_{1-x}As$ buffers previously built up in the group. By transferring and adapting previously developed growth processes to the new MOCVD reactor, we achieved significant improvement in the quality of the graded buffers around $x = 0.32$, setting a new benchmark TDD of $<9.5 \times 10^4$ cm^{-2} for a graded buffer with a final In mole fraction of $x = 0.346$. In the new reactor, we re-examined the effect of different growth conditions on the final quality of the graded buffers, and learned from the results how best to optimize the graded buffers using the capabilities of the new reactor, such that they can be used as virtual substrates for devices (e.g. lasers, HBT etc.), as well as platforms for carrying out further materials research.

7.1.2 Metamorphic strained-InGaAs QW-SCH ridge waveguide laser

Using the high quality graded buffers we developed, metamorphic lasers using the InAlGaAs alloy system emitting at λ = 1328 nm were demonstrated. All steps, from the design and growth, to the fabrication and characterization, have been carried out and discussed. Lasing was observed at duty-cycles up to 10%, with threshold current densities as low as 200-250 Acm^{-2} and peak powers up to 40 mW obtained from a single facet for approximately 2 mm long devices. The low T_o characteristic temperature of 35 K for these devices are a major weakness and if addressed through improved device design, will likely lead to dramatic improvements over the already highly-promising results.

7.1.3 Metamorphic InAlGaAs/GaAs HBTs and InGaP PV cells

We have also demonstrated metamorphic InAlGaAs/InGaAs HBTs on our high quality InGaAs graded buffers, in collaboration with researchers and the Nanyang Technological University in Singapore. Preliminary dc measurements have confirmed the presence of transistor action, with current gain values up to 13 recorded. The importance of low TDD values, as provided by our graded buffers, to the function of the HBTs, were also clearly displayed.

Another device application that we have explored is that of metamorphic PV cells. Our collaborators at Ohio State University have grown InGaP PV cells on high quality InGaAs graded buffers that we have provided them. PL measurements of the cells reveal that the re-grown cells are of high quality, and show that the use of graded buffers are a potential path towards high efficiency metamorphic multi-junction PV cells.

7.1.4 Digital metamorphic alloys

Perhaps the most novel part of the thesis, we investigated a new method of metamorphic grading by using carefully designed digital alloys constructed using only binary semiconductors. We have termed these materials digital metamorphic alloys (DMA). We believe that the two key advantages the DMA-based graded buffers afford us over conventional graded buffers are that we circumvent materials issues such as immiscibility and phase separation, and that we are working with binary compounds with

significantly higher thermal conductivities. We determined the key challenges that had to be addressed to realize the intricate layer structures of the DMA graded buffers, and developed the techniques to overcome them. We observed specific phenomena such as growth-rate variations that have not been discussed before, and our unique material system enabled us to gain significant insight into the possible reasons for the behavior. The observed gradual, controlled relaxation of the DMA structure proved that our concept is indeed sound, and our success in grading towards InP without encountering phase-separation related issues that have plagued conventional graded buffers is a major technology gain, which we hope to build on.

7.2 Future research directions

Clearly, we have achieved much in the course of working on this thesis, but the reality is that we have much more to achieve. The necessary time limits imposed on our work have led to the development of various "wish-lists" as to what else we would have wanted to try along the way, sometimes very early on as we chose which research directions to focus on at a given critical branching point.

In terms of our core InGaAs graded buffer work, one of the most glaring omissions has been the investigation of doped buffers. Others have already investigated the material properties of such structures[21, 46, 93], but we would clearly have liked to see the impact it would have on our much higher quality graded buffers, and, further, how they impact device performance if electrical contacts were made through the graded buffer regions. Also, successful integration of our graded buffer work with similar efforts in other material systems, such as Si->Ge->GaAs->InP->InAs would be a powerful demonstration that we are on clearly on the path to true materials integration.

We would clearly love to improve the quality of the devices obtained on our graded buffers, and we believe there are two paths down which we can tread. These directions are focused mostly on improving device design and growth, given the already extremely low TDD we have achieved for our graded buffers. The first is to acquire empirical data on the electronic and optical properties of the quaternary InAlGaAs alloys that we have been using, to complement our theoretical predictions, to ensure that we are correctly designing our devices. The second path involves improving the growths of the

device layers, both by optimizing the conditions of their growth, and by improving the quality of the growth surface that the virtual substrate provides. The latter might involve the use of chemo-mechanical polishing (CMP), which is already a routine part of making Ge/SiGe/Si buffers in our group. Once this is achieved, the best acclamation of our graded buffer technology would be to demonstrate more devices, with hopefully significantly superior performances, on them. Candidates include more specialized lasers (e.g. DFB/DBR lasers), the elusive III-V FET, high speed BJTs and photodetectors, and highly efficient photovoltaics; the list is clearly non-exhaustive. We believe a key selling point of our high quality buffers is their promise of device reliability down the road. Thus, even as the drive to demonstrate devices on graded buffers gains momentum, work must clearly be done to show the value, in terms of not just device performance, but also device reliability, that can be captured from our continued efforts to improve graded buffer quality.

The DMA concept, in its current form, is clearly a diamond in the rough. It needs to polished, by building on the initial understanding of the concept that we have developed here. Clearly, the ability to controllably grow what a design calls for is critical, and has to be the initial goal. (It may be anathema to our group which has built itself into a foremost user of MOCVD, but MBE might find a very useful role in this endeavor). Subsequent to that, development analogous to that of conventional graded buffers over the last decade and a half must take place, hopefully at a faster rate given all we have learned. This includes optimizing strain relaxation and keeping dislocation behavior controlled, and, based on our initial results, this would likely entail temperature treatments such as anneals. We hope that in short measure, its advantages over traditional graded buffer technology will have manifested themselves, and then more work can be done to further characterize of its microstructural and thermal properties, to validate the potential strengths of the concept. As in the case of the conventional graded buffers, the DMA is literally only as useful as the devices that are ultimately placed on them, and we believe that it will not be long before devices, especially those with high power and thermal considerations, are attempted on the DMA concept.

7.3 Conclusion

We have demonstrated the potential metamorphic growth holds in terms of realizing novel devices in materials systems previously inaccessible to crystal growers. We believe that we are right at the point where the floodgates are about to open for a wave of innovation in device design and integration of system functionality due to our triumph over the lattice-matching restriction that has restrained us for so long. It is therefore our hope that this thesis provides both a good foundation from which we can launch ourselves into this brave new world, as well as the motivation to help us see this through.

APPENDIX A

Parameter	Units	GaAs	AlAs	InAs	GaP	AlP	InP
a	Å	5.65325	5.6611	6.0583	5.4505	5.4672	5.8687
Eg(Γ)	eV	1.4224821	3.0030361	0.3537939	2.7770395	3.5527098	1.3528857
α(Γ)	meV/K	0.5405	0.885	0.276	N/A	0.5771	0.363
β(Γ)	K	204	530	93	N/A	372	162
Eg(X)	eV	1.8988571	2.1640964	1.3697939	2.2727098	2.4877703	2.273
α(X)	meV/K	0.46	0.7	0.276	0.5771	0.318	N/A
β(X)	K	204	530	93	372	588	N/A
Eg(L)	eV	1.7069643	2.3519643	1.0697939	2.6427098	3.5377703	1.9432857
α(L)	meV/K	0.605	0.605	0.276	0.5771	0.318	0.363
β(L)	K	204	204	93	372	588	162
Δso	eV	0.341	0.28	0.39	0.08	0.07	0.108
me(Γ) (dos)		0.067	0.15	0.026	0.13	0.22	0.0795
me(X) (dos) (3 eq. val.)		0.85	0.7503891	0.64	1.0483457	0.8337072	0.88
me(L) (dos) (4 eq. val.)		0.56	0.7803549	0.29	0.7559526	*unknown*	0.47
γ1		6.98	3.76	20	4.05	3.35	5.08
γ2		2.06	0.82	8.5	0.49	0.71	1.6
γ3		2.93	1.42	9.2	2.93	1.23	2.1
mhh (100)		0.3496503	0.4716981	0.3333333	0.3257329	0.5181347	0.5319149
mhh (dos)		0.5855471	0.7490408	0.4745056	0.6731477	0.7969877	0.8117588
mlh (100)		0.0900901	0.1851852	0.027027	0.1988072	0.2096436	0.1207729
mlh (dos)		0.0826999	0.1645283	0.0264467	0.1321639	0.1866398	0.1129565
Ep	eV	28.8	21.1	21.5	31.4	17.7	20.7
ac	eV	-7.17	-5.64	-5.08	-8.2	-5.7	-6
av	eV	-1.16	-2.47	-1	-1.7	-3	-0.6
b	eV	-2	-2.3	-1.8	-1.6	-1.5	-2
c11	GPa	122.1	125	83.29	140.5	133	101.1
c12	GPa	56.6	53.4	45.26	62.03	63	56.1
c44	GPa	60	54.2	39.59	70.33	61.5	45.6
VBO	eV	-0.8	-1.33	-0.59	-1.27	-1.74	-0.94
∈static	F/m	1.151E-10	8.907E-11	1.341E-10	9.837E-11		1.112E-10
∈∞	F/m	9.642E-11	7.225E-11	1.089E-10	8.066E-11	4.848E-11	8.509E-11
E0	eV	1.4224821	3.0030361	0.3537939	2.7770395	3.5527098	1.3528857
Δ0	eV	0.341	0.28	0.39	0.08	0.07	0.108
E1	eV	2.9	3.82	2.5	3.7	4.5	3.1
Δ1	eV	0.23	0.21	0.28	0.05	0.04	0.15
E2	eV	4.7	4.65	4.45	5	4.95	4.7
A	eV^1.5	3.45	25.3	0.61	13.76	30	6.57
B1		6.37	4.72	6.59	6.35	4.7	4.93
C		2.39	1.56	1.78	2.08	1.25	1.49
γ		0.146	0.0844	0.108	0.132	0.076	0.094
∈1∞		1.6	-1.13	2.8	0	-1	1.6

Table A.1 – Table of binary semiconductor material properties used in calculations.

Parameter	Units	AlGaAs	InGaAs	InAlAs	AlGaP	InGaP	InAlP
a	Å						
Eg(Γ)	eV	**special*	0.477	0.7		0.65	-0.48
Eg(X)	eV	0.055	1.4		0.13	0.2	0.38
Eg(L)	eV		0.33			1.03	
Δso	eV		0.15	0.15			-0.19
me(Γ) (dos)			0.0091	0.049		0.051	0.22
mhh (100)			-0.145				
mlh (100)			0.0202				
Ep	eV		-1.48	-4.81			
ac	eV		2.61	-1.4			
VBO	eV		-0.38	-0.64			
∈static	F/m		-5.932E-12				

Table A.2 – Table of bowing constants used for calculating ternary material properties.

**special*: $1.31\ x_{Al} - 0.127$

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