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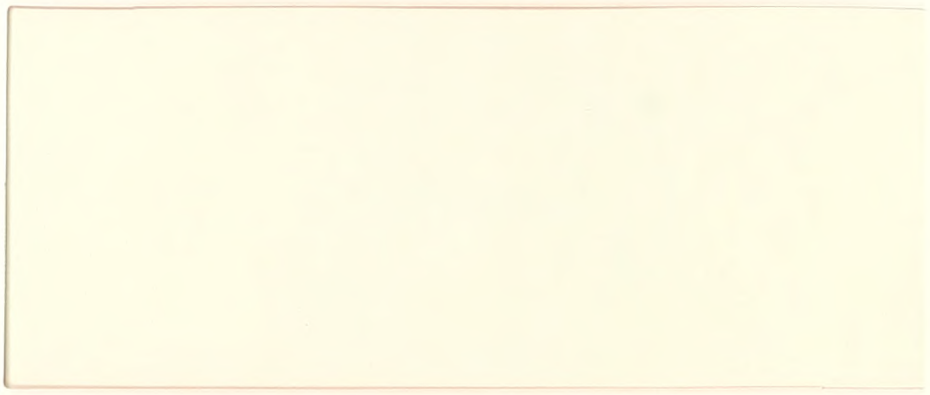
31 August 1993 Sloan WP # 3605-93



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Microenvironment technology holds significant potential for enabling the cost-effective production of semiconductor integrated circuits. However, integrated circuit manufacturers have been reluctant to adopt the technology even though there is substantial empirical evidence of its effectiveness. This paper suggests that the slow acceptance of microenvironment technology can be understood in terms of its weak appropriability and systemic nature.

I. INTRODUCTION

The history of semiconductor technology has been aptly called a "revolution in miniature" (Braun and Macdonald, 1978). This is because the principal goal, miniaturization, is to design circuits with the thinnest possible line widths, thereby permitting the greatest possible degree of circuit integration on a single chip. The sophistication of semiconductors today is attributable in large part to the success of scientists and engineers in pushing line features to their physical limits. During the past decade, the feature sizes of dynamic random access memory (DRAM) chips have been reduced from 2.5μm for 64-kilobit devices to 0.5μm for 16-megabit devices. According to the Semiconductor Industry Association, future generations of DRAMs will have less than one-half micron feature sizes (see Table 1).

The relationship between line geometry and circuit density places stringent demands on the manufacturing discipline necessary to meet the tolerances of sub-micron devices. Particle contamination during wafer processing, in particular, can cause defects on the wafer surface that have a substantial effect on reducing chip yield. Figure 1 illustrates the empirical relationship between the number of defects per square centimeter on a wafer and test yield for 16-megabit DRAM wafer processing.

TABLE 1

Projected Trend in DRAM Integrated Circuit Complexity

	Year					
	1992	1995	1998	2001	2004	2007
Feature size (μm)	0.5	0.35	0.25	0.18	0.12	0.10
Gates per chip	300K	800K	2M	5M	10M	20M
Bits per chip	16M	64M	256M	1G	4G	16G
Chip size (mm^2)	132	200	320	500	700	1000

Source: Semiconductor Industry Association, March 1993

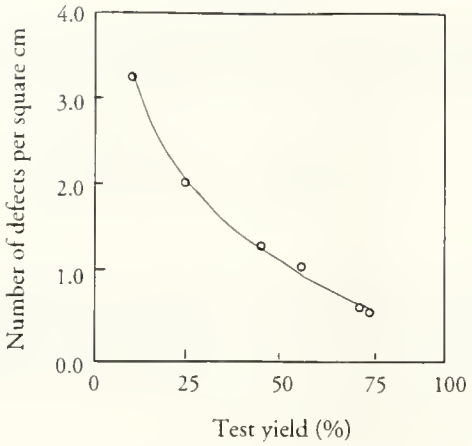


Fig. 1. Relationship between defect density and test yield for 16-megabit DRAMs (Castrucci and Dickerson, 1988)

As line widths shrink, particles that were previously insignificant become detrimental. Typically, particles more than one-tenth of the size of the smallest critical feature on a chip can cause defects (King 1991). Research by the Institute for Microcontamination Control suggests that processing a wafer with 1.0μm line widths under the same conditions as one with 2.5μm line widths will result in a sixfold increase in "killer" particles—that is, particles that reduce manufacturing yield—due to the geometry-related effects alone (Burnett, 1988; Gall, 1990). The problem of submicron wafer processing will become all the more severe because physical forces at the surface of the wafer make it virtually impossible to remove the smallest particles.

The trend in design geometry means that wafer processing must be conducted in an increasingly cleaner environment. This is done by performing wafer processing in elaborate "cleanrooms" where the ambient is carefully controlled to reduce the number of minute particles. However, as the need for cleanliness has increased, the use of cleanrooms has become more costly. The present cost of constructing a state-of-the-art cleanroom for wafer processing can be as much as $1500 per square foot (Dicken, 1990; Sayre et al., 1989). Figure 2 shows the dramatic growth in the overall cost of building and equipping a half-micron DRAM facility, which some manufacturers anticipate may exceed $350 million by the mid-1990s.

The stricter requirements for cleanliness and the escalating cost of cleanrooms, may induce some IC manufacturers to adopt "microenvironment" technologies as an alternative solution to the problem of contamination in wafer processing.[1] The

[1]The concept of microenvironment technology has been given several labels, including "wafer isolation technologies," "local cleanrooms," and "minienvironments." The acronym SMIF—which stands for Standard Mechanical Interface—is a common term first used by Hewlett-Packard, the originator of the concept, and later employed in the trademarks of Asyst Technologies, the commercial pioneer of the technology. To maintain consistency, this paper will use the term "microenvironment" as an encompassing concept, while reserving SMIF to signify Asyst-related technology in particular.

idea behind microenvironment technology is to isolate the environment immediately surrounding the wafer during processing and storage, maintaining this rather limited area—and only this area—in an ultra-clean state. This differs significantly from conventional cleanrooms, in which the entire wafer processing facility—tools, operators, and wafers—is maintained in an ultra-clean state.

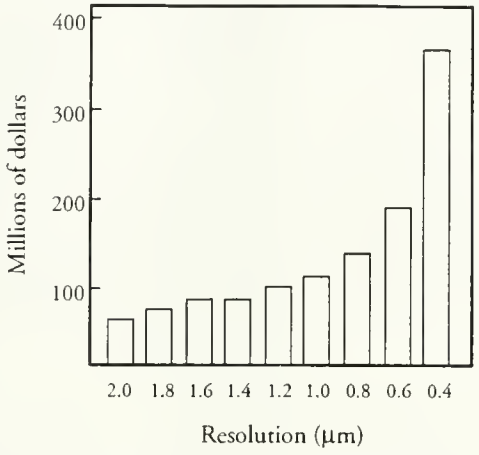


Fig. 2. Increasing cost of advanced semiconductor manufacturing facilities, assuming 800 150mm wafer starts per day (Tolliver, 1991).

In essence, microenvironment technology is a wafer transport and storage system consisting of an integrated collection of robotics, automation techniques, tool enclosures, and wafer "pods" that are used to maintain the wafers in a Class 1 (i.e., one 0.5μm particle per cubic foot) ambient. Even so, it is not an especially complex technology in the usual sense of the term. Indeed, microenvironment technology is fairly straightforward in nature. It consists of nothing more than conventional manufacturing enclosures and robotics for handling and transporting wafers. The "radical" quality of microenvironment technology is not in its complexity, but in the way it alters how manufacturers must think about the wafer processing system.

Curiously, even though microenvironment technology is an appealing concept and the empirical evidence to date supports its effectiveness, its adoption by IC manufacturers has been very slow. This paper explores why this has been the case. At the heart of the argument is the idea that as a "systemic innovation," microenvironment technology presents unique obstacles that inhibit the speed of its adoption among potential users. Before discussing the obstacles to systemic innovation, the next section examines the problem of contamination control in IC manufacturing and the conventional approaches toward cleanroom design. Section III provides a description of microenvironment technology and its rationale, and Section IV reviews the empirical evidence of its effectiveness in reducing particle contamination and improving manufacturing yield.

II. CONTAMINATION CONTROL IN SEMICONDUCTOR MANUFACTURING

The sensitivity of IC fabrication to particle contamination requires that wafer processing be done under extremely clean conditions. The current guidelines for cleanliness are governed by Federal Standard 209D issued in 1988 (Möller, 1991). The standard defines the number of permissible particles per cubic foot of a given size. The current target levels of air cleanliness for the fabrication of submicron IC devices are: Class 0.1 (undefined by 209D) for the atmosphere where wafers are fully exposed; Class 1 for wafers protected in cassettes or enclosed boxes; Class 1000 to Class 10,000 for equipment, technicians, engineering, and operating area—depending upon the type of wafer transport (King 1991).

Recent research pinpointing the sources of particle contamination in wafer processing suggests that equipment operators and the loading and unloading of wafer cassettes from tools each account for 30% of the contaminants (Dicken 1990). Another 25% of the contaminants are found in the process tool itself, while 10% originate in the cleanroom environment and 5% are from the wafer storage cassette.

A tremendous amount of innovative thinking has gone into the design and operation of cleanrooms. One such innovation, known as "laminar" (or "unidirectional") airflow, is essential to achieving the level of cleanliness required for wafer processing. This involves the vertical circulation from ceiling to floor of a high volume of filtered air through the cleanroom. The filters remove 99.97% of the particles, 0.5μm in size or larger. The shower of clean air flowing over the wafer processing area is very effective in reducing the number of airborne particles that would otherwise interfere in the fabrication process.

Another important design innovation is the cleanroom tunnel concept, which separates the wafer processing areas from the circulation and tool maintenance areas. This is done by mounting the process tools such that only the bulkhead, where the operator works, is in the cleanroom tunnel. One advantage of this approach is that the air flow rate can be reduced outside the critical processing area. Another benefit is that it enables the extraction of return air laterally into the maintenance areas.

The tunnel concept, highly efficient air filters, and laminar flow are essential design elements of cleanrooms for IC wafer processing. Nonetheless, the modern cleanroom poses certain problems for efficient wafer processing. Providing laminar airflow, for example, is expensive and especially sensitive to the price of energy. Given the size of the typical cleanroom tunnel, the air handling requirements are substantial (about 1620 cubic meters per hour per square meter) and the investment and operation of air handling units can be quite costly. It is estimated that as much as 75% of the annual operating cost of a cleanroom is directly related to the cost of energy (Schicht 1991).

Furthermore, by minimizing the amount of cleanroom area, careful consideration must be given to the design and layout of the facility, equipment footprints, and material flows. The space constraint means less strategic flexibility to accommodate changing operational requirements, equipment substitutions, or substantial layout alterations. In some cases, new equipment with exceptionally large

footprints, such as cluster tools, may not fit within an existing cleanroom. Even when equipment changes can be made, production shutdowns of the entire cleanroom facility are often required.

Class 1 cleanrooms will also use cassette-to-cassette wafer transport in order to eliminate the handling of wafers by operators. Operators will be fully gowned in cleanroom garments with transparent face helmets. This is of particular concern since it can significantly effect an operator's productivity and can be very costly. Not only do garments restrict comfort, each exit and reentry to the cleanroom in the course of an operator's workday requires a garment change (Toy, 1989).

Given the present trend in IC design geometry, it is clear that the challenge of contamination control in wafer processing will persist. A crucial question is whether or not advances in conventional cleanroom design and construction can keep pace with the needs of submicron technology. Reducing contamination down to a level of 0.05μm particles is non-trivial. Will extending the conventional approach to cleanroom design be sufficient—and if so, at what cost? Or will it require a more fundamental change, such as microenvironment technology?

III. RATIONALE FOR MICROENVIRONMENT TECHNOLOGY

The problem by particle contamination in wafer processing presents a serious challenge to the conventional approach of cleanroom design. The requirements of Class 1 or Class 0.1 for half-micron circuit designs will greatly increase the cost, reduce strategic flexibility, and pose further restrictions on wafer fabrication operators. Accordingly, the concept of microenvironment technologies may present an attractive approach to contamination control.

The basic logic behind microenvironment technology is to recognize that only the area immediately surrounding the wafer—an area that is actually minuscule in comparison to that of the entire cleanroom—needs to be kept particle-free. Bluntly stated, the rationale is quite simple: Why put so much effort and money into maintaining 10,000 square feet of cleanroom at Class 1, when it is only a very small area that actually affects the level of particle contamination on a wafer? The principal sources of contaminants are in close proximity to the wafer. Thus, focusing attention on the area closest to the wafer seems quite logical. Microenvironment technology does precisely this: it isolates and maintains the immediate area around the wafers and within tools at a Class 1 level. The rest of the cleanroom environment can be maintained at Class 1000 or higher.

Hewlett-Packard pioneered the concept of microenvironment technology in the early 1980s, which it called SMIF, an acronym for "standard mechanical interface". However, it is a start-up firm, Asyst Technologies, which has been largely responsible for the commercial introduction of SMIF products since 1984. The basic components of Asyst's system are the SMIF-Pod™, SMIF-Arms™, and equipment enclosures. A SMIF-Pod is an environmentally secure wafer cassette container that reduces the level of particle contamination while loading, unloading, and transferring wafers between process tools. The pod secures the wafer cassette within a Class 10 or better environment and can be transported between stations by manual or

automated methods. Access to the pod occurs through a standardized mechanical porr that Asyst incorporares into various wafer processing tools.

The SMIF-Arm is an integrated system composed of a mechanical port and robot arm that is within the tool enclosure. The arm lowers the wafer cassette from the pod through a porr and transfers it to the equipment indexer for processing. The third element of the system is an enclosure that surrounds the process tool and thereby maintains the tool and wafers in a Class 10 environment—from the pod, through the port to the tool and back. Figure 3 illustrates a SMIF-equipped process tool.

In theory, a SMIF tool can provide several advantages for contamination control in wafer processing. First, it can minimize the effect of organic contamination on sensitive (especially oxides and film) process steps. Second, it can minimize the formation and help control the growth of native oxide and orher ultra-thin surface films via encapsulation in inert gases. Third, it can enable the monitoring and control of the local environment around wafer cassertes. Fourth, it can minimize long-term storage related deposition and film growth effects.

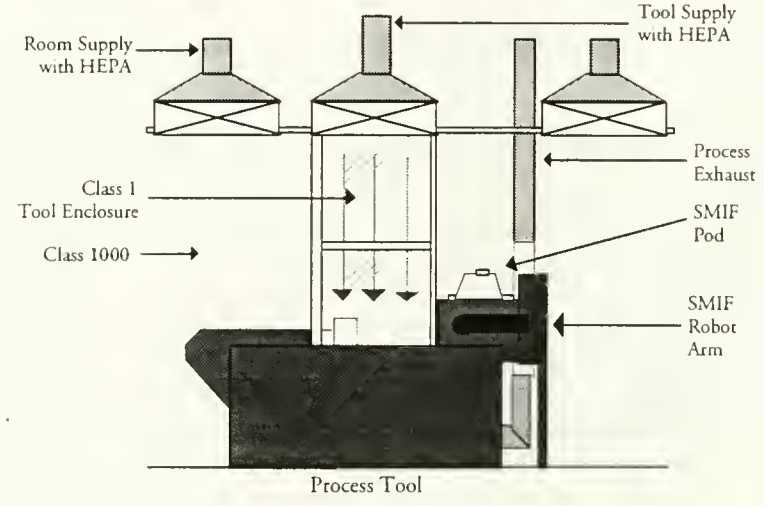


Fig. 3. Typical SMIF microenvironment process tool.

One additional aspect of the SMIF-Pod system is the ability to electronically tag each pod with information regarding the wafer lot and its processing sequence and history. Although this is not a direct concern in contamination control, it is an extremely useful addition to microenvironment technology that takes advantage of the pod as a means for inventory control and management (Brain et al., 1987). It provides convenient access to all information—such as process sequence validation, real time location of material, feed-forward data and material audit trails—and automates data acquisition.

Beyond helping control wafer contamination and managing work-in-process, one of the significant benefits of microenvironment technology is that it is economical to implement. The capital investment in cleanroom facilities is reduced by

the elimination of many special conventional cleanroom design features (Hughes et al., 1988). These features include extra space and structural support for fans, filters, motors; wall, floor and partition materials; air conditioning-related vibration isolation; air showers; garment change rooms; special high volume air conditioning systems; noise-reduction design elements; and special cleanroom furniture. Furthermore, the potential reduction in the total annual operating costs for a large wafer processing facility due to the implementation of microenvironment technology is estimated to be about one-third (Tolliver, 1991).

By isolating the process tools in enclosures and the wafers in pods, microenvironment technology is able to create an ultra clean environment nearest the wafer. This enables the transport and processing of wafers to occur under carefully controlled conditions that reduce particle contamination. Better control of particle contamination reduces defects at the wafer surface, which in turn contributes to improved device yields. Moreover, microenvironment technology greatly simplifies cleanroom construction and operating procedures, thereby reducing capital expenditures and annual operating costs.

IV. EXPERIMENTAL EVIDENCE

There are three kinds of applications by lead users of microenvironment technology (Simon 1988): (1) retrofitting of an existing lower class cleanroom, (2) inserting microenvironment technology into a new or existing higher class cleanrooms—the "belt and suspenders approach," and (3) optimizing cleanrooms with microenvironments and minimizing laminar flow zones and clean islands. At present, the empirical evidence on the effectiveness of microenvironment technology is based on a number of pilot-line experiments. Most studies focus on the reduction in surface and airborne particle contamination, and on the improvement in yield resulting from the implementation of microenvironment technology. In most instances the experiments are based on experience with Asyst's SMIF products.

New Microenvironment Facilities

Two firms operate full-scale microenvironment IC wafer fabrication facilities: Taiwan Semiconductors Manufacturing Company (TSMC) in Hsinchu, Republic of China (Tu and Shu, 1990; Shu and Tu, 1992), and Cypress Semiconductor in Minneapolis, Minnesota, formerly owned by VTC (Workman and Kavan, 1987; Workman, 1988). Only TSMC has published comparative data on the effectiveness of microenvironment technology from controlled experiments. Established in 1987, TSMC is the third largest Taiwan-based IC firm, with estimated 1990 revenues of $100 million. The firm provides foundry services using submicron CMOS technology for application specific ICs and memory products.

At TSMC, the decision to use microenvironment technology is subsumed in one simple question (Tu and Shu, 1990): "Machine and people in a cleanroom or a cleanroom in a machine?" The facility is the first to be designed specifically for the application of microenvironment technology. The conceptual design of the facility is guided by the following criteria: (1) low cost, quick return on invest-

ment; (2) high reliability; (3) high cleanliness; (4) easy maintenance; (5) easy, fast, and accurate tracking of work-in-process.

Table 2 shows that TSMC greatly reduced the number of air handling units and filters. Furthermore, microenvironment technology reduced the volume of clean air circulating through the cleanroom from 4.9 to 2.4 cubic meters per hour. Airborne particle measurements inside and outside the SMIF tool enclosures and in the diffusion furnace area show the effectiveness of microenvironment technology for contamination control. Table 3 shows that the number of particles per cubic foot within the enclosures for all sizes of particles is substantially less than outside the enclosure.

The mechanical functionality of SMIF tools, recovery time, reliability, and wafer breakage are also examined by TSMC. Although the evidence is based on limited operating experience, the data suggest substantial improvements from microenvironment technology. In terms of mechanical functionality, SMIF robot arms were put through 200-cycle runs and 24-hour tests without failure. The recovery time for SMIF enclosed tools (i.e. the time to achieve operation-level cleanliness after shutting-down the tool and exposing it to the ambient conditions) in all cases is found to be less than five minutes. Up-time for SMIF tools registers a level of 98% per month and wafer breakage is measured to be one wafer in 35,000 (Tu and Shu, 1990).

TABLE 2

Filter and Air Handling Unit Requirements of SMIF and Conventional Cleanroom

	Conventional	SMIF
Number of Air Handling Units	103	54
Number of Filters	2,547	1,383
Clean Air Volume (cubic meters per hour)	4.9	2.4

Source: TSMC (Tu and Shu, 1990)

TABLE 3

Results of Airborne Particle Tests Inside and Outside the SMIF Enclosure

	INSIDE ENCLOSURE		OUTSIDE ENCLOSURE	
Particle per cubic foot	mean (s.d.)	n	mean (s.d.)	n
particle size > 0.1μm	0.57 (0.73)	15	627 (1098)	16
particle size > 0.2μm	0.14 (0.25)	34	274 (420)	16
particle size > 0.3μm	0.11 (0.22)	34	117 (171)	16
particle size > 0.5μm	0.10 (0.22)	34	19 (32)	16

Source: TSMC (Tu and Shu, 1990)

TSMC claims a number of cost and productivity benefits resulting from their use of microenvironment technology. By reducing the number of air handling units, TSMC lowered annual operating costs by $1 million. Cleanroom gown expenditures are reduced by $0.5 million per year. Increases in operator productivity are anticipated as a result of reducing the gown requirements. Moreover, microenvironment technology enabled the firm to start-up and test some process tools while installing others, thereby accelerating the ramp-up time to full production. Initial manufacturing data show a 25% yield improvement compared to the firm's previous facility, though how much of this increase is attributable specifically to microenvironment tools is unclear.

Implementing microenvironments at TSMC was not trouble-free. Because microenvironment technology is a new and radically different approach, process tool manufacturers have not uniformly adopted the SMIF interface into their equipment. Therefore, it was the task of TSMC and the system integrator, Asyst, to modify each of the process tools with the SMIF interface. This increases the length of time it takes to outfit an entire facility. If the interface was a standard part of process tools or a vendor option, this would greatly simplify the implementation (Tu and Shu, 1990).

The construction contractor for the TSMC facility reports an estimate of the cost benefits from microenvironment technology (Table 4). Given major reductions in air handling units, filters, clean air volume, electric power consumption, air conditioner capacity, and cleanroom space, the initial capital cost of a microenvironment cleanroom can be as much as $1000 per square meter less than a conventional cleanroom. The annual operating costs for the microenvironment facility are estimated to be $150 per square meter less.

TABLE 4

Potential Cost Saving of SMIF Approach Versus Conventional Cleanroom

COST ELEMENT	DOLLARS PER SQUARE METER
Building construction	200
Cleanroom system	600
Air conditioners	80
Electric power	120
Total initial investment	1000
Annual operating costs	150

Source: Meissner+Wurst (Simon, 1988)

Retrofitted Microenvironment Facilities

Over a six-month period, NCR ran an experiment to examine the usefulness of retrofitting a facility with microenvironment technology (Weiss, 1989a and 1989b; Weiss, 1990a and 1990b). Measurements are made of airborne and surface particles at four process tools and an analysis is conducted of the wafer defect density and

probe yield. Table 5 shows an eight fold reduction in surface particles at the coat/bake track system to a level of just one particle per wafer pass. There is a threefold reduction in surface particles at the projection aligner and a sevenfold reduction at the inspection station. Table 6 shows equally substantial reductions in airborne particles at each tool. The impact of reductions in airborne and surface particles can be seen in the increase in manufacturing yield. Table 7 shows an analysis of defect density at the coater and projection aligner that suggests a 16-20% improvement in yield for a 3.0μm process and about a 19-24% improvement for a 2.0μm process.

TABLE 5

Surface Particle Counts for SMIF and Conventional Process Tools

Process tool	SMIF	Conventional	Improvement factor
Coater	1.0	8.0	8x
Aligner	6.1	18.4	3x
Inspection	0.0	7.2	7x

Source: NCR (Weiss, 1990)

TABLE 6

Airborne Particle Counts (>0.5μm) for SMIF and Conventional Process Tools

Process tool	SMIF	Conventional	Improvement factor
Coater	9	174	19x
Aligner	6	51	8.5x
Particle counter	0.1	26	260x
Inspection	0.6	29	48x

Source: NCR (Weiss, 1990)

TABLE 7

SMIF Probe Yield Improvement on Three ASIC Product Lines

	% IMPROVEMENT		
ASIC PRODUCT	A	B	C
3.0μm devices	20.3	20.0	16.1
2.0μm devices	19.7	19.2	23.6

Source: NCR (Weiss, 1990)

Overall, the results of the NCR experiment are considered to be very successful: "The program demonstrated that airborne and surface particles can be successfully reduced and yields improved within an existing fabrication area without interrupting production. Using a financial payback model, the probe yield improvement justified full implementation of the [microenvironment technology] concepr across the wafer fabrication facility" (Weiss, 1989a). Moreover, operator reaction to microenvironment technology was generally positive. Its use had the effect of focusing attention on contamination control and involving operators in the process. Equipment uptime is 98% and wafer breakage <1 per 10,000 wafers processed.

Microenvironment experiments conducted at Harris Semiconductor provide additional empirical evidence (Titus and Kelly, 1987). One experiment consists of a three-month evaluation of wafer defect densities at a photoresist coater and projection mask aligner. Photolithography is particularly sensitive to particle contamination. Ten consecutive samples of particle counts are taken every day and averaged each day over a 15-day period. The data show significant decreases in airborne particle count with the SMIF equipped coater. On average, the SMIF coater/aligner added 12.9 particles per wafer pass compared to 59.4 particles per wafer pass without SMIF. It is unclear if any improvement in yield can be attributable to the microenvironment equipment.

Another Harris experiment measures the number of particles added per wafer pass using etch-pit calibration wafers (Inbody and Van Eck, 1990) An average of 0.4 particles (≥0.3μm in size) are added per wafer pass. In comparison, the non-SMIF experimental control measures 2.0 particles per wafer pass. The airborne particle tests are favorable, although particle counts did go up to fairly high levels at times—most likely due to maintenance procedures. The experiment found microenvironment technologies to be reliable and equipment recovery times to be within a few minutes.

National Semiconductor also reports results from a microenvironment experiment it called OASIS (Hughes et al., 1988; Hughes and Moslehi, 1988; and Hughes et al., 1990). The experiment includes the mechanical functionality tests of SMIF process tools, air flow visualization tests, airborne particle counts, particles added per wafer pass, and wafer defect density tests. An effort is made to ascertain the level of cleanliness achieved with the SMIF tools relative to baseline cleanroom environments. The experiments use SMIF equipped photolithography tools operating in the ambient of a typical office environment.

The results of airborne particle tests indicate that for each SMIF canopy/enclosure (at rest), the oven and track measures at Class 1, the inspection equipment measures at between Class 1 to Class 10, and the stepper measures at between Class 10 to Class 100. The recovery time for each module is generally less than two minutes; however an additional five-to-ten minutes is required if the tool needs to undergo a wipe-down procedure.

Reported advantages were:

- radically reduced air flow volume and more precise air control;
- lower capital and operating costs;
- improved work environment;

- increased flexibility to handle different types of products and degrees of automation;
- increased equipment safety and reliability; and
- elimination of cross-contamination among process tools during operation, repair, and maintenance.

The electrical tests for defect densities are fairly elaborate. Randomization techniques are used to control for the effect of common process steps (oxidation/metal deposition and etch strip). The data show that wafers processed in the microenvironment line have a yield distribution that is within the distribution curves of the two conventional cleanrooms. This suggests that the yield performance of the microenvironment tools is within the boundary conditions of conventional cleanrooms.

The experience at National Semiconductor suggests that the full-scale use of microenvironment technology will require the greater involvement of process tool manufacturers. Some process tools were re-engineered, cleaned, and modified to improve airflow patterns inside the tool enclosure. By doing so, the overall reliability of some tools may be adversely affected. Furthermore, vendor maintenance procedures may need to be modified to quickly restore tools to normal operating conditions.

Although the isolation of wafer cassettes from the operators using microenvironment tools is advantageous in terms of worker safety and contamination control, it gives rise to certain problems. In some instances it is necessary for an operator to intervene and remove a wafer from the process tool, such as when a wafer jams in an automated mechanism. The microenvironment tool enclosure prevents operators from performing the kind of "quick fix" they frequently use with conventional equipment—causing some frustration. It may be difficult to alter the habits of operators and production managers such that a resistance to microenvironment technologies may persist (Hughes et al., 1988).

The results of an experiment conducted at Intel are shown in Table 8. The experiment involves five different process tools in an existing Class 100 facility: photoresist coat track, stepper, develop track, after-develop inspection microscope, and plasma etch. The data indicate a reduction in defects at each step ranging from 48% to 90%. The results are substantial for particle sizes $\geq 0.7\mu m$. The virtual elimination of the "top wafer" effect is particularly pronounced in the data. Air flow visualization tests indicate good laminar flow, even around the wafer surface. Furthermore, samples of airborne particles within the track and enclosure measure 15 times cleaner than with conventional tools and remains at Class 1 during continuous cycling. Measurements taken at the spin track represent a twelve fold improvement. In over twenty-four thousand hours of operation, there were only three hours of down-time with the SMIF tools. Overall, the results of the experiment were considered quite positive (Sayre et al., 1989).

TABLE 8

Experimental Evidence of Defect Reduction at Five Process Stages Mean Number of Defect Relative to Conventional Cleanroom

PROCESS STAGE	% REDUCTION
Spidermask comparison (number of defects)	≈0.48
Particles added per wafer during 50 load cycles (1)	≈0.76
Particles added per wafer during 10 load cycles at plasma etch (1)	≈0.81
Particles added per wafer during 10 load cycles at stepper (2)	≈0.69
Particles added per wafer during 10 load cycles at develop check (2)	≈0.90

Notes: (1) Particle size ≥ 0.7μm
(2) Particle size ≥ 0.3μm

Source: Intel Corporation (Sayre, et al., 1989)

Siemens reports experiments with microenvironment technology at a manufacturing facility for 256K DRAM (Hainzl, 1989). The SMIF process tools are used on a 150mm wafer production line in a Class 10 environment. The experiments are conducted over six months, with a total of 67,000 wafers processed. The data show a 30% reduction in particle clouds that can be attributed to SMIF technology. However, no improvement in test yield could be detected. Equipment reliability is good, although it is noted that frequent technical faults occur due to the standstill during loading and unloading but that they can be resolved with minor re-engineering work. The "humanization" of the manufacturing environment and process security are also found beneficial.

The results of an evaluation of microenvironment technology at Philips are shown in Tables 9 (Koolen, 1990). The experiment includes a particle measurement system, an ion implanter, and an in-house wafer transport system. Measurements are made of wafer particle accumulation within the pods during transport and storage, and while operating robot arms during ion implantation. The data indicate substantial improvements in particle contamination due to the implementation of microenvironment technology.

TABLE 9

Accumulated Wafer Surface Particles after Cumulative Ion Implant Operations (125mm wafers)

Cumulative Number of Operations	Number of accumulated particles	
	Conventional	SMIF
0	29	9
2	30	9
10	32	9
30	59	9
50	84	10

Source: Philips, NV (Koolen, 1990)

From this experience, Philips designed their own version of microenvironment technology to make it easier to handle. The results convinced Philips management

to introduce SMIF in a Class 10,000 cleanroom: "The SMIF concept is a good one. The adaptation of the SMIF-Arms is rather simple, due to a good design. The contamination tests give good results, especially in a Class 10,000 room when using laminar flow boxes to load and unload the SMIF-Pods. The ease of use is good, operators like to work with SMIF" (Koolen, 1990).

LSI Logic ran a five-month study of microenvironment technology on a six-inch wafer processing line in a Class 10 cleanroom (Crouzet-Pascal, 1990). The experiment includes wafer lots for six different customers. The analysis consists of measurements of yield improvement (die per wafer and yield distribution), tool reliability, and production logistics. The process tools include photolithography (coat/bake, align, develop, and develop inspection) and etch (dry metal etch, dry stripping, and etch/final inspections).

Table 10 shows the results of the experiment. The data on yield improvement are mixed: in one case the SMIF yield is significantly below the yield realized on the conventional processing line, in another case there is virtually no difference, and four in four cases there are significant yield increases which range from 6% to 15% with an average number of die per wafer. Altogether, the yield improvement on the 754 wafers is 7.4%.

TABLE 10

Yield Improvement Factor for SMIF Relative to Conventional Processing

	CONVENTIONAL			SMIF			
Customer	Number of wafers	Average Number of die per wafer	Standard Deviation of Yield	Number of wafers	Average Number of die per wafer	Standard Deviation of Yield	Yield Improvement Factor
A	153	81	19.0	102	72	39.3	0.89
B	285	228	72.6	163	263	47.8	1.15
C	81	184	39.8	69	182	47.8	0.99
D	48	257	79.0	53	287	63.0	1.12
E	82	176	96.7	94	186	64.2	1.06
F	105	217	24.0	61	232	27.3	1.07
TOTAL	754	188	—	542	202	—	1.07

Source: LSI Logic (Crouzet-Pascal, 1990)

The yield distribution data are less conclusive. The results indicate that in terms of yield from wafer-to-wafer, microenvironment tools may not be necessarily more consistent. In terms of tool reliability, equipment up-time is 98% during the five months of study. Furthermore, measurements of cleanliness inside and outside the tool enclosures and in the SMIF pods indicate no significant change in the number of accumulated particles over time.

The LSI experiment indicates that microenvironment technology can offer measurable benefits in yield improvement when used in a Class 10 cleanroom. This result is interesting because the experiment is conducted in a non-microenvironment production line, and because at times the equipment is used in non-isolation mode. Thus, much of the yield improvement may be attributable specifically to the use of the wafer pods.

As in the case of National Semiconductor, LSI Logic found that operators accustomed to handling the wafers manually become frustrated with microenvironment tools. The problem dissipates over time as the need for manual checks becomes less frequent. However, it is necessary to devise procedures for rework loops (since wafers requiring rework could no longer be manually pulled from a cassette) as well as for running test wafers. To ease acceptance of microenvironment tools, operators were involved in the process of change. This helped to mitigate their concerns about how the new technology would affect their jobs. Crouzet-Pascal (1990) states:

> As is true for any new technology, complete acceptance is difficult to achieve prior to implementation. It is human nature to be results oriented, to desire to see what a new technology can do before passing judgment. The most important point we needed to realize about this philosophy was that acceptance of this new technology was crucial to the success of the pilot line.... With this in mind, several SMIF presentations were staged prior to the equipment installation which served to answer questions that the workers had concerning the pilot line.

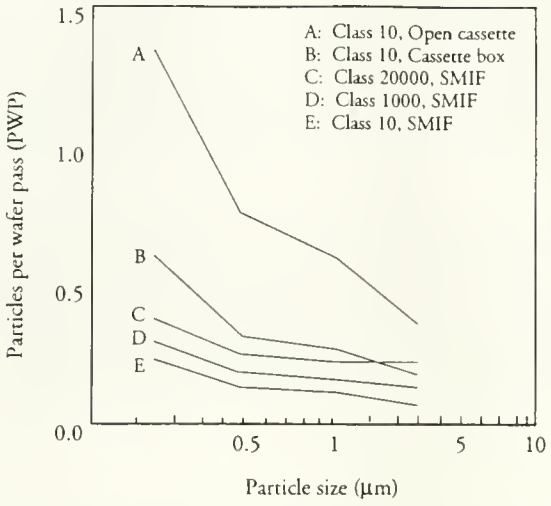
Other Studies of Microenvironments

One of the earliest experiments to understand the effectiveness of microenvironment technology compares the cleanliness of wafer transport under five different conditions: (1) SMIF in a class 10 cleanroom, (2) SMIF in a class 1000 cleanroom, (3) SMIF in a class 20,000 cleanroom, (4) handling of cassettes in conventional blue-box type carriers, and (5) handling of conventional open cassettes. The initial level of contamination at the wafer surface is measured in a Class 10 environment. In the experiment, wafers are transported by gowned operators thirty meters, loaded into a simulated process tool, then transported back to the wafer inspection system and measured again. The process is repeated 100 times for each case. The analysis, shown in Figure 4, plots the number of particles per wafer pass by particle size for each experimental condition (Harada and Suzuki, 1986; Brain, 1986).

The data show the SMIF wafer transport system to be effective in decreasing particle sizes. At 0.5μm, the SMIF system in the Class 20,000 ambient is superior to conventional cassette handling with conventional cassette boxes in Class 10. At 0.22μm, the SMIF system shows a twofold improvement in Class 10. The SMIF wafer pods are found effective in protecting the wafers from particles in the ambient environment when fitted with a special sealing gasket.

Asyst independently reports the experimental results of lead users of its SMIF process tools (Parikh, Bonora and Ortiz, 1988) Table 11 shows comparative measurements for particles per wafer pass (PWP) with and without SMIF tools in nine experiments. The ratios of PWP for conventional and SMIF data range from a low of 2.14 to a high of 8.50. Asyst finds that, on average, lead-users have experienced a fourfold reduction in particle contamination on wafers. A comparison of the typical yield for conventional and SMIF runs, with 2.5μm and 1.5μm features, is shown in Table 12. The data indicate six point increases in yield using SMIF in both cases. Table 13 shows substantial reductions in capital and operating cost experi-

enced by three SMIF users. Capital costs are reduced by 15-25%, while operating costs are reduced by 57-82%.



Note: Particles measured at 0.22, 0.48, 1.09, 2.95μm

Fig. 4. Experimental results comparing SMIF with conventional wafer handling. Source: Shimizu Construction Company (Harada and Suzuki, 1986).

TABLE 11

Comparative Results of Lead Users: Contamination Control Data for SMIF Technology

Company	Particle size (μm)	Test Conditions	Particles per wafer pass		Ratio of Conventional to SMIF
			Conventional	SMIF	
Hewlett-Packard	>1.00	Class 100	0.90	0.25	3.60
Alvey GRP	>1.00	Class 100	0.30	0.14	2.14
Mfg. #1	>0.70	Class 100	2.36	0.66	3.57
Mfg. #2	>0.30	Class 1	0.17	0.02	8.50
Siemens	>0.35	Class 100	—	0.20	—
Shimizu	>0.22	Class 10	0.58	0.22	2.64
Shimizu	>0.30	Class 10	0.43	0.19	2.53
Shimizu	>0.50	Class 10	0.26	0.11	2.36
Harris	>0.40	Class 100	59.4	12.9	4.60

Source: Asyst Technologies (Parikh, Bonora & Ortiz, 1988)

TABLE 12

Comparative Yield Improvement Using SMIF Technology

	2.5μm Technology		1.5μm Technology	
	Conventional	SMIF	Conventional	SMIF
Feature size(μm)	2.5	2.5	1.5	1.5
Wafer size (mm)	100	100	100	100
Die per wafer	136	136	234	234
Die size (sq cm)	0.5	0.5	0.3	0.3
Defect density per sq cm	1.0	0.8	2.0	1.6
Die yield (Murphy model)	62%	68%	57%	63%
Good die per wafer	84	92	133	147

Source: Asyst Technologies (Parikh, Bonora & Ortiz, 1988)

TABLE 13

Percent Cost Savings of SMIF Technology in Three Fabs
(ranging in size from 5-10 thousand sq. ft.)

	FAB 1	FAB 2	FAB 3
Capital cost	0.18	0.15	0.25
Operating cost	0.57	0.69	0.82

Source: Asyst Technologies, 1989

V. SYSTEMIC INNOVATION

The rising cost of contamination control in wafer processing is driven, in part, by design priorities shaped by the historical demands of the semiconductor industry (Schicht, 1991). The highest priority in cleanroom design has been—and will continue to be—effectiveness. Functional safety and the reliability of the cleanroom is also a high priority. In contrast, cost-efficiency traditionally has been a subordinate concern in cleanroom design. But as the requirement for cleanliness in wafer processing increases, and the concomitant cost of maintaining that level increases, economic considerations dictate that the volume of ultra-clean area be reduced as much as possible.

From this perspective, microenvironment technology is an extension of a long-standing trend in wafer processing: that is, the reduction in the volume of area that must be kept ultra-clean. Nonetheless, the adoption of microenvironment technology has been slow, even though the experimental evidence suggests that it is both effective and economical for contamination control. Instead, IC manufacturers are as committed now as ever to constructing—at great cost—elaborate cleanrooms based upon the conventional approach. Faced with such prospects and presented with a seemingly appealing alternative, what might explain the reluctance of IC manufacturers to adopt microenvironment technology?

The adoption rate of a new technology may be affected by a number of factors. One framework for explaining the adoption rate is provided by Rogers (1983: 213-223), who discusses the perceived attributes of an innovation, how the innova-

tion decision is made, the communication channels, the nature of the social system, and the effort of change agents to promote the innovation. In terms of the perceived attributes, Rogers (1983) identifies five criteria that may influence the rate of adoption of an innovation:

- *Relative advantage:* the degree to which an innovation is perceived as being better than the idea it supersedes;
- *Compatibility:* the degree to which an innovation is perceived as consistent with existing values, past experiences, and needs of potential adopters;
- *Complexity:* the degree to which an innovation is perceived as relatively difficult to understand and use;
- *Trialability:* the degree to which an innovation may be experimented with on a limited basis; and
- *Observability:* the degree to which results of an innovation are visible to others.

While relevant to many innovations, these criteria do not adequately explain the reluctance of IC manufacturers to adopt microenvironment technology. First, as the experimental evidence suggests, microenvironment technology can provide a relative advantage, both in terms of contamination control and cost. Second, its compatibility with existing wafer processing technology does not appear to be an issue. The modification of existing process tools with SMIF enclosures and robot arms is straightforward. Third, the technology is not particularly complex, such that users find it hard to understand or operate. Operators usually undergo a period of adjustment with microenvironment tools, but there is no evidence of user rejection. Fourth, as demonstrated in the numerous experiments, microenvironment technology can be implemented on a trial basis and show measurable results.

An alternative framework that might be useful for explaining the slow adoption of microenvironment technology focuses on a firm's ability to appropriate the benefits of an innovation. Teece (1992) suggests the appropriability of an innovation can be weaker or stronger depending upon the nature of the technology and the efficacy of legal protection mechanisms. He states:

> The most fundamental reason why innovators with good marketable ideas fail to open up markets successfully is that they are operating in an environment where their know-how is difficult to protect. This constrains their ability to appropriate the economic benefits arising from their ideas and their product/process concepts (Teece, 1992: 177)

The appropriability of an innovation is said to be strong if there is tacit knowledge involved in its creation and if it can be well protected legally. Conversely, appropriability is weak if knowledge is easily codified and if the technology is difficult to protect legally. Technologies that have weak appropriability are slow to develop because managers are reluctant to expend the resources necessary to

develop an innovation when other firms can quickly imitate it and capture the benefits.

The slow adoption of microenvironment technology can be explained, in part, by its relatively weak appropriability. Lacking technological sophistication, which might otherwise incorporate tacit knowledge or enable strong legal protection, microenvironment technology is very easy to imitate. Interviews with microenvironment experts conducted by Bain & Company (1990) highlight precisely this issue. States one expert: "SMIF is 90% concept and 10% technology." Another person claims, "SMIF is a terrific concept, but I can get the individual components for less money, any machine shop can do a decent job building the enclosures, and the arms are standard robot parts. Even the SMIF pods are sold by [another company]." Yet another person predicts, "As the SMIF concept catches on, I would expect to see other companies, possibly robotics companies, doing very similar things."

Clearly, the weak appropriability of microenvironment technology places lead innovators at a disadvantage. The time and effort they invest in making the technology work effectively may be easily undermined by imitators who capture a large share of the benefits. However, appropriability in and of itself is not the only important consideration. Although it might account for why innovators have moved slowly with microenvironment technology, appropriability does not fully explain why, given the empirical evidence, users or imitators have been reluctant to adopt the technology. Indeed, few imitators have entered the field and among IC manufacturers, only a small number have made any commitment to using microenvironment technology.

The systemic nature of microenvironment technology also is a consideration. In order to be successful, microenvironment technology must be integrated into the large and widely distributed system of technologies and organizations that constitute semiconductor wafer processing. This system is composed of many different kinds of process tools (e.g., inspection systems, etchers, photoresist processing, ion implanters, imaging systems, thermal processors, and deposition systems), that are made by a multitude of equipment manufacturers. Indeed, Semiconductor Equipment Materials International, an international industry association lists over fourteen-hundred members worldwide.

There may be as many as fifty to one-hundred manufacturers in each segment of the wafer processing industry, each producing different kinds of tools, and announcing new models each year. Microenvironment technology must function smoothly with many of these tools in order to preserve the integrity of contamination control throughout the wafer processing facility. One way to accomplish this is for an innovator to outfit each piece of equipment it intends to use with microenvironment technology. In fact, this is precisely what has been done at TSMC. But to the extent that the wafer processing system is greatly varied technologically and organizationally, this can greatly impede the rate of adoption.

Rather than the innovator taking on the burden of adjusting microenvironment technology to accommodate each and every element of the system, it may be possible to mobilize each member of the system to take on this task independently. Indeed, the value of a systemic innovation may hinge on the system acting collectively to adopt it as a standard. In this manner, microenvironment technology may

be characterized as a "network" technology (David, 1992). Network technologies have two distinguishing features: "first, they involve technologies characterized by increasing returns to scale of use or production, and second, they entail choices where considerations of technical relatedness among the components forming alternative systems cannot be ignored" (David, 1992: 138).

How to mobilize the system to accommodate a new technology is the central challenge facing a systemic innovation. What is most difficult is that empirical evidence is largely ineffectual as a basis for mobilization. Data are relevant only when people agree upon the importance of the technology and the basis of comparison. Proponents of microenvironment technology are motivated to generate empirical evidence to support their position, but the design and analysis of their experiments can hardly be perceived as purely objective. Even the best run experiment has assumptions embedded in it that can mitigate its persuasiveness. Moreover, critics are likely to reject such evidence as proof of their opinions without the burden of running their own experiments to support their position. Thus, data alone cannot mobilize the system; it can only form the basis of a *post hoc* justification for the adoption of a systemic innovation.

For example, critics are quick to point-out that there are "several missing pieces of the SMIF puzzle..." (Inbody and Van Eck 1990), since most data regarding microenvironment effectiveness are based upon limited experiments that focus on a few segments of the wafer processing line:

> Although much has been written about SMIF technology, the expression 'totally SMIF-ed fab' is rarely or never used. It should be noted that almost every report with particle data and yield improvement data centers around such automated cassette-to-cassette tools as photo tracks and exposure systems. Since these tests are often performed in engineering environments, they are not subject to real-world commercial volume production (Inbody and Van Eck, 1990).

But where data fail as a basis for mobilizing the system, institutional mechanisms may be more effective. For example, Inbody and Van Eck (1990) recommend two actions which could be taken to accomplish this task: (1) the formation of SMIF user groups to place pressure on process tool manufacturers to meet their needs, and (2) the use of industry consortia such as Sematech to develop parts of the SMIF process environment that are not adequately addressed by tool vendors.

Paradoxically, while the distributed nature of the system is an obstacle to innovation, it is a major strength if and when an innovation takes hold. As previously centralized production processes become decentralized—both organizationally and geographically—over time, new opportunities may arise. Just as today the IC production process (i.e., crystal growth, wafer processing, test, and packaging) is done in different firms and locations, it may be that microenvironment technologies will lead to an even greater segmentation of wafer processing activities. In the future, wafer processing may very well be characterized by a high degree of organizational and geographic dispersion, such that "distributed wafer processing" is the norm.

The widespread adoption of microenvironment technology may ultimately transform semiconductor manufacturing. Distributed wafer processing might spur a

number of changes, including: new strategies for optimizing tool and facility utilization, opportunities for wafer process experimentation with off-site developers, the formation of specialized process vendors for capital-intensive tools such as x-ray lithography, and vendor based processing of test wafers to evaluate the effectiveness of new tools—which would have the effect of shifting the burden of proof for process validation from IC makers to equipment vendors. How soon these changes might come about will depend largely on institutional forces within the semiconductor industry and the ability of managers to reconceptualize the problem of contamination control in wafer processing.

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