Kirchoff’s Voltage Law: (KVL) 

Around any loop: \[ \sum_i V_i = 0 \]

Faraday’s Law:

\[ \nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t} \]  
[differential form]

Integral form is:

\[ \oint_c \vec{E} \cdot d\vec{s} = -\frac{d}{dt} \int_A \vec{B} \cdot d\vec{a} \]

[Recall Stoke's Theorem: \[ \int_A (\nabla \times \vec{G}) \cdot \hat{n} da = \oint_c \vec{G} \cdot d\vec{s} \]]

If \( \frac{d\vec{B}}{dt} = 0 \) in \( A \), then Kirchoff’s voltage law must be satisfied

More generally: 

KVL assumes all magnetic energy is stored inside circuit elements
KIRCHOFF’S VOLTAGE LAW (2)

Undefined Circuit:

Current in loop varies, so
\[ \frac{d}{dt} \int_A \mathbf{B} \cdot d\mathbf{a} \neq 0 \Rightarrow \text{voltage!} \]

i(t) = \cos \omega t

Defined Circuit:

We assume voltage drops occur only across elements, and ignore H fields generated by currents through them.

We use small loops, thick wires, and high-impedance lumped elements

“parasitic inductance”
**KIRCHOFF’S CURRENT LAW (KCL)**

**Kirchoff’s Current Law:** \( \sum I_i = 0 = \text{Total current into any node} \)

**Ampere’s Law:**

\[
\nabla \times \vec{H} = \vec{J} + \partial \vec{D}/\partial t \quad \text{[differential form]}
\]

\[
\nabla \cdot (\nabla \times \vec{H}) = \nabla \cdot (\vec{J} + \partial \vec{D}/\partial t) = 0
\]

\[
= \nabla \cdot \vec{J} + \partial (\nabla \cdot \vec{D})/\partial t
\]

\[
= \nabla \cdot \vec{J} + \partial \rho/\partial t
\]

**Conservation of Charge:**

\[\nabla \cdot \vec{J} = -\partial \rho/\partial t = 0 \text{ at each node} \]

[Recall Gauss's Divergence Theorem: \( \int_V (\nabla \cdot \vec{G}) dv = \int_S \vec{G} \cdot d\vec{a} \)]

**Current Law follows from:**

\[ \int_S \vec{J} \cdot d\vec{a} = \sum I_i = 0 \]

More generally:

KCL assumes nodes and wires store no charge \( (\partial \rho/\partial t = 0) \), or that all electric energy is stored inside circuit elements “parasitic capacitance”
SOLVING CIRCUITS

Generic Circuit Topology:

Assume $b$ branches, $n$ nodes, and $p$ unique loops

We can show $b = n + p - 1$.

Every time we add a branch, the number of nodes or loops (meshes) increases by one.

Voltage sources are branches characterized by $v = V_o$
Current sources are branches characterized by $i = I_o$
Number of Unknowns: Number of unknowns is 2b (v,i for each branch)

Number of Equations: We have one device equation for each branch relating or specifying v and i

We also have n – 1 independent node equations (KCL) and p loop equations (KVL), for a total of:

\[ b + (n – 1) + p = 2b \text{ equations} = \text{number of unknowns} \]

(Recall \( b = n + p – 1 \))

Given initial conditions and all sources we can solve the equations analytically for simple circuits, or by simulation for any circuit.

(Non-unique exceptions: indeterminate flip-flop or chaotic circuits)
Electrostatics:

In general: Everywhere
\[ \nabla \times \vec{E} = 0, \quad \nabla \cdot \vec{E} = \rho/\varepsilon \]

At conductor
\[ \hat{n} \cdot \vec{E} = \sigma_s/\varepsilon, \quad \vec{E}_\parallel = 0 \]

Between conductors,
\[ \nabla \cdot \vec{E} = \rho/\varepsilon = 0 \]

Parallel-Plate Devices:

Field Solution:
\[ \vec{E} = \hat{y}E_0 \quad \text{for rectangular geometry here} \]
\[ \sigma_s = \varepsilon E_0 \text{ [Cm}^{-2}] \]
Relating Fields to Potentials:

Since: \( \nabla \times \vec{E} = 0 \)

We define \( \vec{E} = -\nabla \Phi \) \( \Phi = \int_1^2 \vec{E} \cdot d\vec{s} \)

Where \( \Phi \) is the electrostatic potential of [1] relative to [2]

Therefore here: \( E_0 d = V \), \( E_0 = V/d \)

In general, absolute potential \( \Phi = 0 \) at infinity, by definition
Capacitor Charge Q:

We define: \[ Q = \int_A \sigma_s da = A\varepsilon E_o = A\varepsilon V/d \]

We also define: \[ Q = CV \]

Capacitance C:

Therefore: \[ C = A\varepsilon/d \]

We know: \[ q(t) = \int_{-\infty}^{t} i(t) dt = Cv(t) \]

Therefore: \[ v(t) = \frac{1}{C} \int_{-\infty}^{t} i(t) dt \]

Also, \[ i = C \frac{dv}{dt} \]
**CAPACITORS IN SERIES AND PARALLEL**

Capacitors in Parallel:

\[ C_{eq} = C_1 + C_2 \]

Capacitor in Series:

\[ \frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} \]
SIMPLE RESISTORS

Conductance $\sigma$:

$\bar{J} = \sigma \bar{E} \left[ \text{am}^{-2} \right]$

$I = AJ = A\sigma E_0 = A\sigma V/d$

Resistance $R$:

$R = V/I = d/A\sigma$

Resistors in Series:

$R_{eq} = R_1 + R_2$

$R_{eq} = (V_1 + V_2)/I$

Resistors in Parallel:

$1/R_{eq} = 1/R_1 + 1/R_2$

$1/R_{eq} = (I_1 + I_2)/V$
CHARGE RELAXATION

RC Circuits:

\[ q(t) = Cv(t) = \int_0^t i(t) \, dt + q_0 \]
\[ v(t) = -i(t)R = -RC \frac{dv(t)}{dt} \]

Try:

\[ v(t) = v_0 e^{-t/\tau} \quad [v_0 \text{ is initial condition}] \]

It works if \( \tau = RC \):

\[ v_0 e^{-t/\tau} = (-RC)(-1/\tau)v_0 e^{-t/\tau} \]

Dielectric Relaxation:

\[ R = d/A\sigma, \quad C = \varepsilon A/d \]

\( \tau = RC = \varepsilon / \sigma \) seconds “Relaxation time constant”

independent of geometry