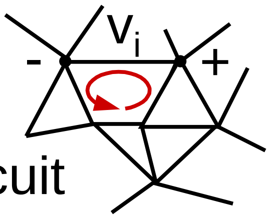
KIRCHOFF'S VOLTAGE LAW

Kirchoff's Voltage Law: (KVL)

Around any loop: $\sum_i V_i = 0$

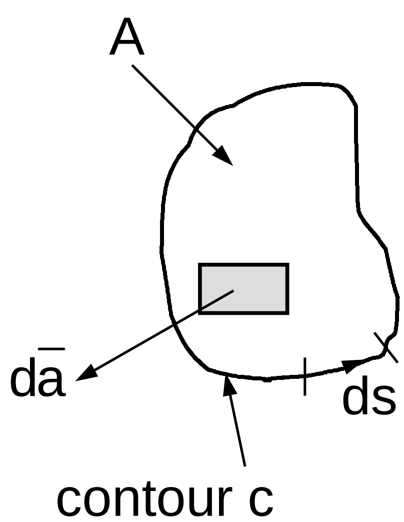


Faraday's Law:

$\nabla \times \overline{E} = -\partial \overline{B}/\partial t$ [differential form]

Integral form is:

$$\oint_c \overline{E} \bullet d\overline{s} = -\frac{d}{dt}\int_A \overline{B} \bullet d\overline{a}$$



[Recall Stoke's Theorem: $\int_A (\nabla \times \overline{G}) \bullet \hat{n} da = \oint_c \overline{G} \bullet d\overline{s}$]

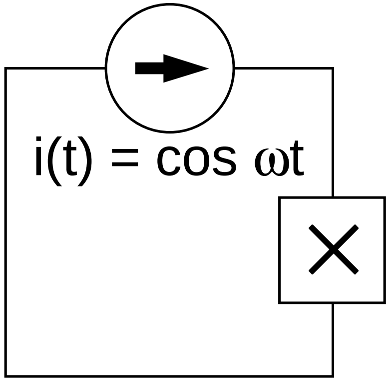
If $d\overline{B}/dt = 0$ in A,   then Kirchoff's voltage law must be satisfied

More generally:

KVL assumes all magnetic energy is stored inside circuit elements

KIRCHOFF'S VOLTAGE LAW (2)

Undefined Circuit:

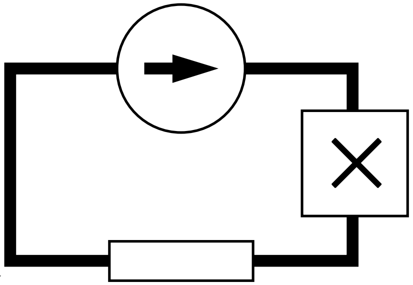


Current in loop varies, so

$$\frac{d}{dt}\int_A \overline{B} \bullet d\overline{a} \neq 0 \Rightarrow \text{voltage!}$$

Defined Circuit:

We assume voltage drops occur only across elements, and ignore H fields generated by currents through them.



Lumped inductor L

We use small loops, thick wires, and high-impedance lumped elements

"parasitic inductance"

KIRCHOFF'S CURRENT LAW (KCL)

Kirchoff's Current Law: (KCL) $\sum_i I_i = 0$ = Total current into any node

Ampere's Law: $\nabla \times \overline{H} = \overline{J} + \partial \overline{D} / \partial t$ [differential form]

$$\nabla \bullet (\nabla \times \overline{H}) = \nabla \bullet (\overline{J} + \partial \overline{D}/\partial t) = 0$$

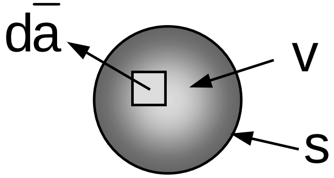
$$= \nabla \bullet \overline{J} + \partial (\nabla \bullet \overline{D}) / \partial t$$

$$= \nabla \bullet \overline{J} + \partial \rho / \partial t$$

Conservation of Charge: $\nabla \bullet \overline{J} = -\partial \rho / \partial t$ = 0 at each node

[Recall Gauss's Divergence Theorem: $\int_V (\nabla \bullet \overline{G}) dv = \int_S \overline{G} \bullet \overline{da}$]

Current Law follows from: $\int_S \overline{J} \bullet d\overline{a} = \sum_i I_i = 0$



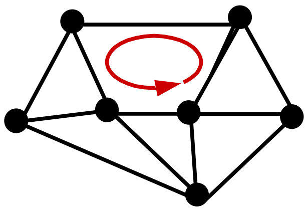
More generally: KCL assumes nodes and wires store no charge ($\partial \rho / \partial t = 0$), or that all electric energy is stored inside circuit elements

"parasitic capacitance"

SOLVING CIRCUITS

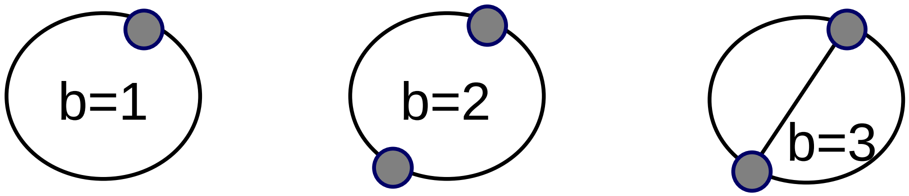
Generic Circuit Topology:

Assume b branches, n nodes, and p unique loops



b=12, n=7, p=6

We can show b = n + p –1.



n = p = 1   n = 2   n = p = 2

Every time we add a branch, the number of nodes or loops (meshes) increases by one.

Voltage sources are branches characterized by $v = V_o$

Current sources are branches characterized by $i = I_o$

SOLVING CIRCUITS (2)

Number of Unknowns:

Number of unknowns is 2b (v,i for each branch)

Number of Equations:

We have one device equation for each branch relating or specifying v and i

We also have n – 1 independent node equations (KCL) and p loop equations (KVL), for a total of:

b + (n –1) + p = 2b equations = number of unknowns

(Recall b = n + p –1)

Given initial conditions and all sources we can solve the equations analytically for simple circuits, or by simulation for any circuit.

(Non-unique exceptions: indeterminate flip-flop or chaotic circuits)

SIMPLE CIRCUIT ELEMENTS, R AND C

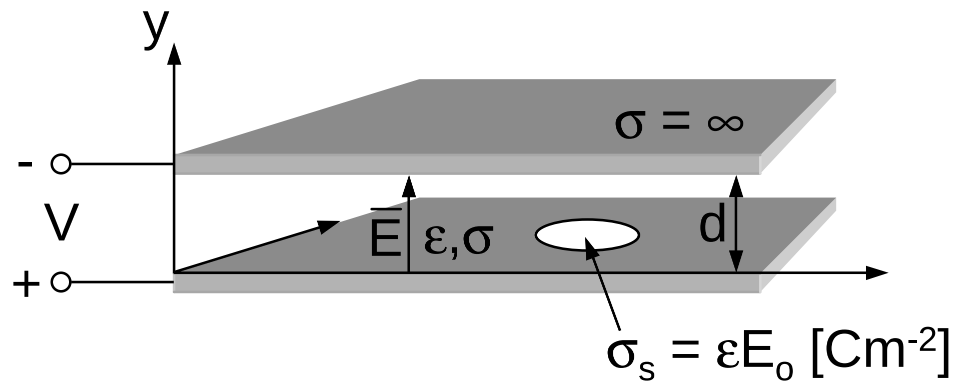
Electrostatics:

In general: Everywhere $\nabla \times \overline{E} = 0, \quad \nabla \bullet \overline{E} = \rho/\varepsilon$

At conductor $\hat{n} \bullet \overline{E} = \sigma_S/\varepsilon, \quad \overline{E}_{//} = 0$

Between conductors, $\nabla \bullet \overline{E} = \rho/\varepsilon = 0$

Parallel-Plate Devices:

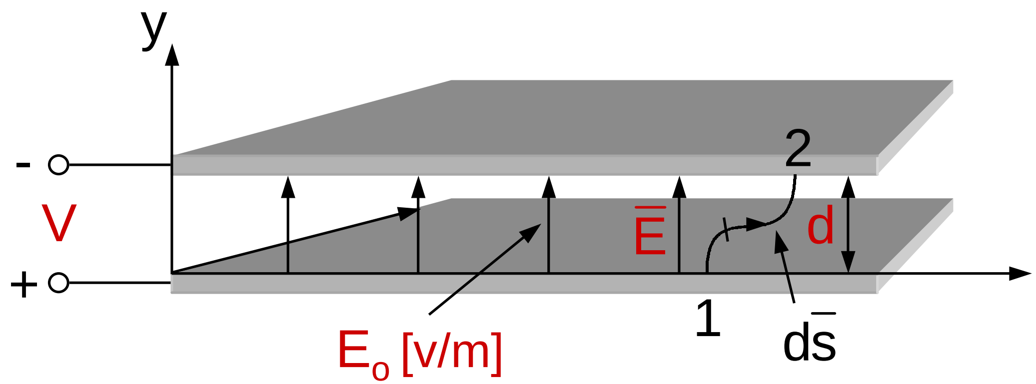


Field Solution:

$\overline{E} = \hat{y}E_o$ for rectangular geometry here

$\sigma_S = \varepsilon E_o$

SIMPLE CAPACITOR



Relating Fields to Potentials:

Since: $\nabla \times \overline{E} = 0$

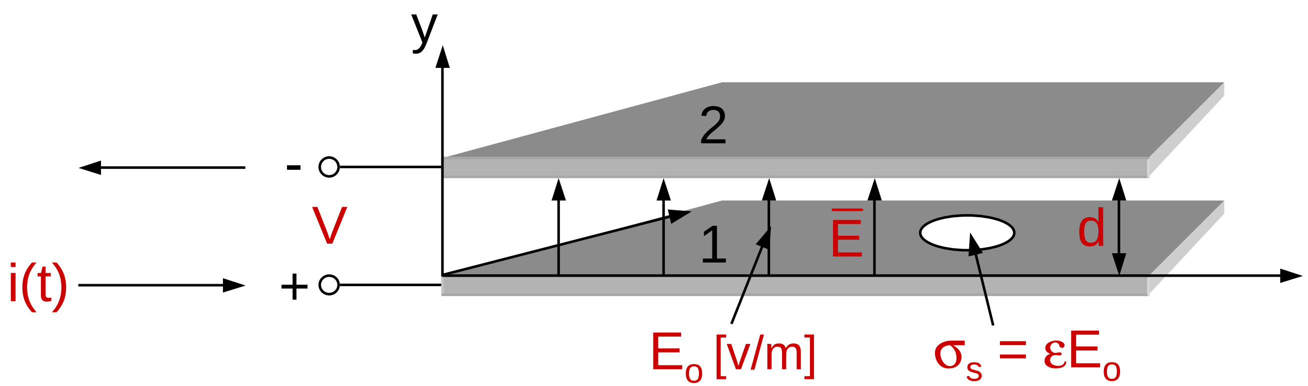
We define $\overline{E} = -\nabla\Phi \qquad \Phi = \int_1^2 \overline{E} \bullet d\overline{s}$

Where Φ is the electrostatic potential of [1] relative to [2]

Therefore here: $E_o d = V \;, \; E_o = V/d$

In general, absolute potential $\Phi = 0$ at infinity, by definition

SIMPLE CAPACITOR (2)



Capacitor Charge Q:

We define: $Q = \int_A \sigma_s da = A\varepsilon E_o = A\varepsilon V/d$

We also define: $Q = CV$

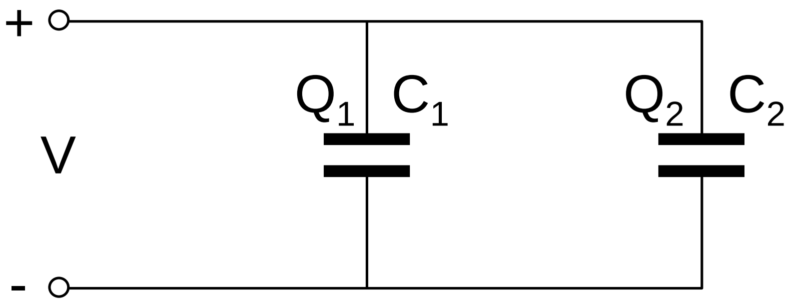
Capacitance C:

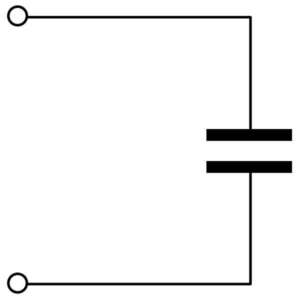
Therefore: $C = A\varepsilon/d$

We know: $q(t) = \int_{-\infty}^{t} i(t)dt = Cv(t)$

Therefore: $v(t) = (1/C)\int_{-\infty}^{t} i(t)dt$ Also, $i = C\,dv/dt$

CAPACITORS IN SERIES AND PARALLEL

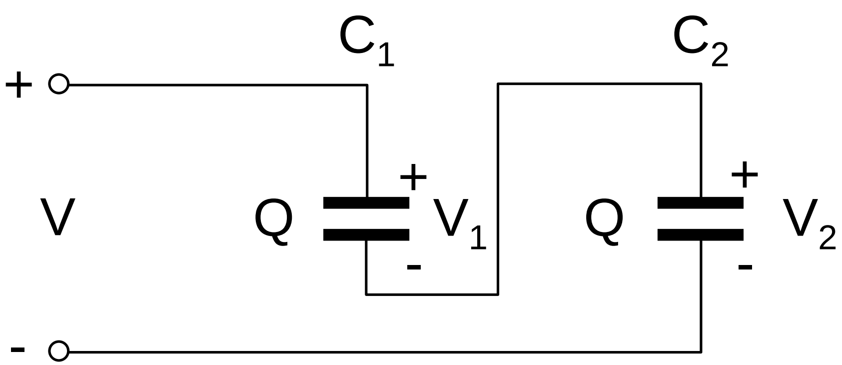


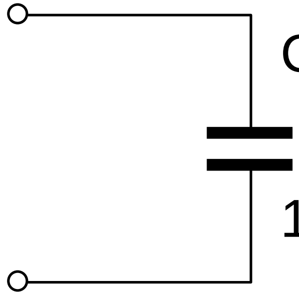


$C_{eq} = Q_{eq}/V =$
$(Q_1 + Q_2)/V = C_1 + C_2$

Capacitors in Parallel:

$$C_{eq} = C_1 + C_2$$





$1/C_{eq} = V/Q = (V_1 + V_2)/Q$

Capacitor in Series:

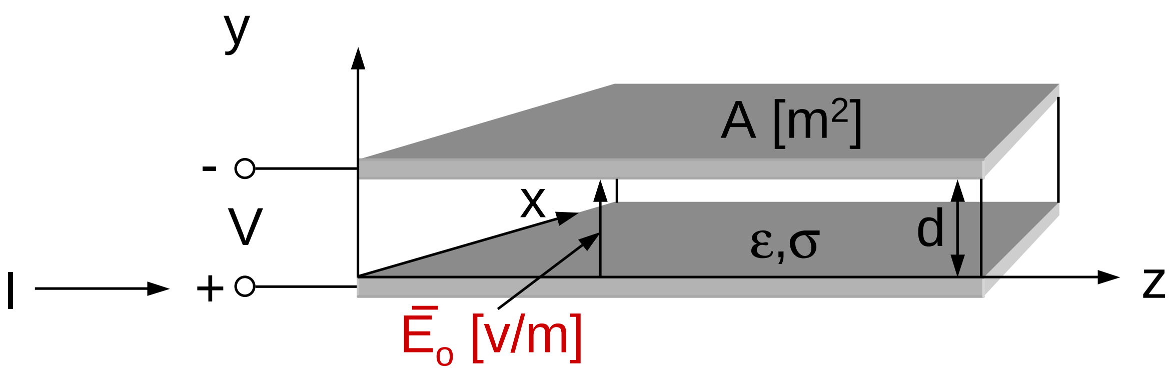
$$1/C_{eq} = 1/C_1 + 1/C_2$$

SIMPLE RESISTORS

Conductance σ:

$$\bar{J} = \sigma \bar{E} \; \left[am^{-2} \right]$$

$$I = AJ = A\sigma E_o = A\sigma V/d$$



Resistance R:

$R = V/I = d/A\sigma$

Resistors in Series:

$R_{eq} = R_1 + R_2$

$R_{eq} = (V_1 + V_2)/I$

Resistors in Parallel:

$1/R_{eq} = 1/R_1 + 1/R_2$

$1/R_{eq} = (I_1 + I_2)/V$

CHARGE RELAXATION

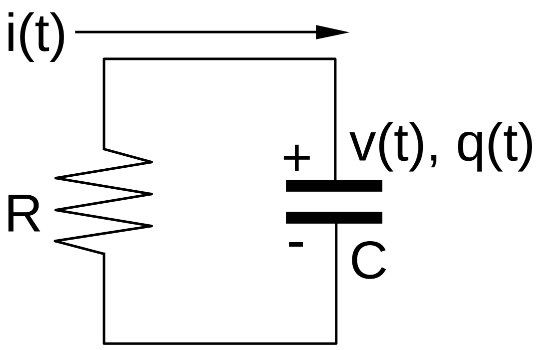
RC Circuits:

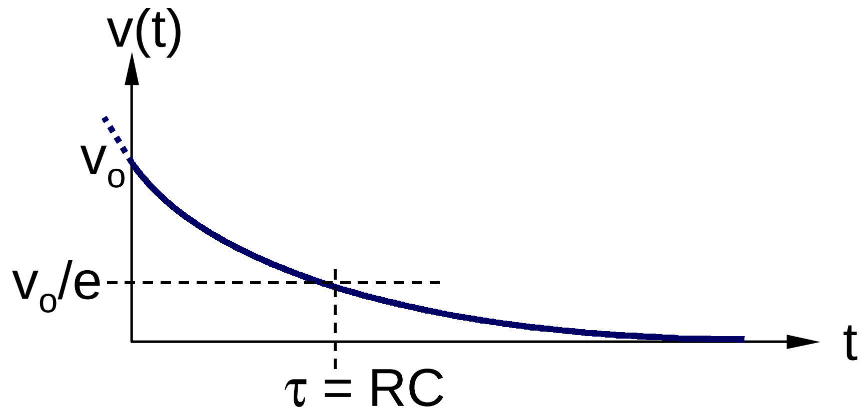
$$q(t) = Cv(t) = \int_0^t i(t)dt + q_o$$

$$v(t) = -i(t)R = -RC\, dv(t)/dt$$

Try: $v(t) = v_o e^{-t/\tau}$ [v_o is initial condition]

It works if τ = RC: $v_o e^{-t/\tau} = (-RC)(-1/\tau)v_o e^{-t/\tau}$





Dielectric Relaxation:

$$R = d/A\sigma,\ C = \epsilon A/d$$

τ = RC = ε/σ seconds "Relaxation time constant"

independent of geometry