

# 6.013 Lecture 10: Introduction to Circuits

## A. Kirchoff's Laws

As suggested in Figure 10-1, circuits are usually analyzed in terms of *lumped elements* (or *branches*) that are connected together at nodes to form two- or three-dimensional circuits. These can be characterized by the voltages at each node or by currents in a set of loops. Although circuit analysis is often based in part on Kirchoff's laws, these laws are imperfect due to electromagnetic effects. For example, *Kirchoff's voltage law* (KVL) says that the voltage drops  $V_i$  associated with each lumped element around any loop must sum to zero, i.e.:

$$\sum_i V_i = 0 \tag{1}$$

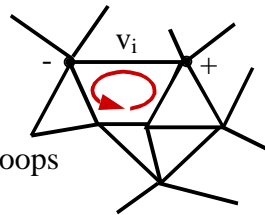


Figure 10-1. Circuit with branches and loops

This follows from Faraday's law, which in differential and integral form is:

$$\nabla \times \vec{E} = -\dot{\vec{B}} \tag{2}$$

$$\oint_c \vec{E} \cdot d\vec{a} = -\dot{\Phi} \tag{3}$$

where the variables are defined in Figure 10-2. If  $\dot{\Phi} = 0$  within the fixed-sized loop, then the integral around the loop (around the contour  $c$ ) is zero and KVL applies.

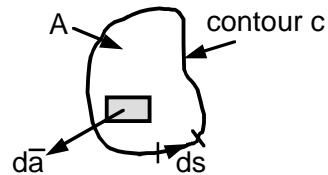
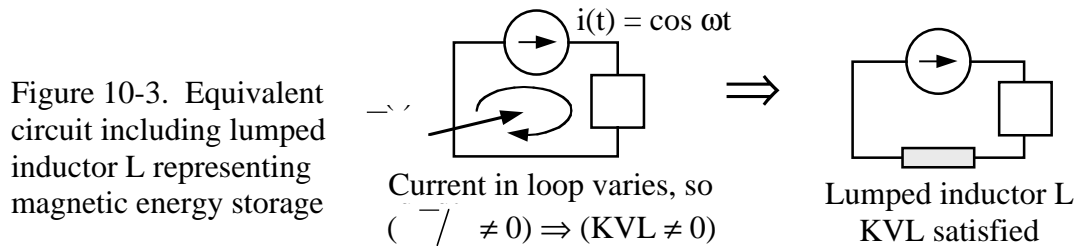


Figure 10-2. Definition of contour and loop variables

But we know that in any physical circuit the current flowing around a loop is typically non-zero and time-varying, so  $\dot{\Phi} \neq 0$  and KVL does not apply! In fact, if the currents around all loops were zero, the circuit would be boring and useless. We resolve this problem by distinguishing physical from mathematical circuits, and by lumping into separate elements the magnetic energy storage and voltage drops associated with these magnetic fields through the loop. One small inductor might be added in series per branch to form an equivalent lumped element circuit for which KVL applies more precisely, as suggested in Figure 10-3. Normally these *parasitic inductances* are small

and can be neglected, but they can increasingly dominate as signal wavelengths drop below a few meters ( $\lambda = c/f$ ), unless the circuit dimensions shrink proportionately.



In a similar fashion *Kirchoff's current law* (KCL) follows from Ampere's law, which in differential form is:

$$\nabla \times \bar{H} = \bar{J} + \partial \bar{D}/\partial t \tag{4}$$

Using the identity  $\nabla \cdot (\nabla \times \bar{A}) = 0$  yields

$$\nabla \cdot (\nabla \times \bar{H}) = 0 = \nabla \cdot (\bar{J} + \partial \bar{D}/\partial t) \tag{5}$$

If (5) is integrated over a small volume V that encloses the node of interest within the surface A, then application of Gauss's law yields:

$$\oint_V \nabla \cdot (\bar{J} + \partial \bar{D}/\partial t) dV = \oint_V 0 dV = 0 \tag{6}$$

where  $I_i$  is the current leaving that node along branch i and positive  $\bar{D}$  points away from the node. Therefore:

$$\sum_i I_i + \partial Q/\partial t = 0 \tag{7}$$

Only if  $\partial Q/\partial t = 0$  for a given node will the sum of currents  $I_i$  into that node be zero so that KCL applies:

$$\sum_i I_i = 0 \tag{8}$$

However, if any node voltage differs from others (the only interesting case), then that node will produce radial electric fields  $\bar{E} = -\nabla V$  so that, in general,  $\sum_i I_i \neq 0$ . Again, the solution is to augment any mathematical circuit with lumped-element capacitors in parallel with each branch to account for this stored electrical energy. Normally these *parasitic capacitances* are small and can also be neglected. If both parasitic capacitances and inductances are non-negligible for a branch, then the question arises whether they should be connected in series or parallel. At this point, or when radiation occurs,

distributed circuit models typically must replace simple lumped-element circuits. Later some simple distributed circuits will be analyzed.

### B. Solving circuit problems

Figure 10-4 illustrates a simple circuit with  $b = 12$  branches,  $p = 6$  loops, and  $n = 7$  nodes. A set of loop currents uniquely characterizes all currents if each loop circles only one “hole” in the topology and if no additional loops are added once every branch in the circuit is incorporated in at least one loop.

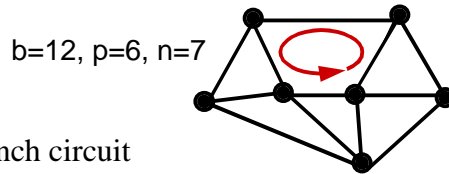


Figure 10-4. 12-branch circuit

By considering the simplest possible circuit, which has one node and one branch, as illustrated in Figure 10-5, it is easy to show that the number  $b$  of branches in a circuit is:

$$b = n + p - 1 \tag{9}$$

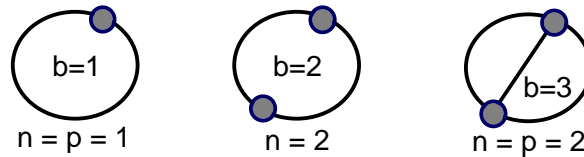


Figure 10-5. Simple circuits

As we add either nodes or branches to this circuit, Equation (9) is still obeyed. If we add voltage or current sources to the circuit, they too become branches.

We can see that the total number of unknowns in a circuit is  $2b$  because each branch is characterized by both its voltage and current. The number of equations is also  $b + n + p - 1 = 2b$ , where the first  $b$  in this expression corresponds to the number of voltage/current relations for the branches,  $n-1$  is the number of independent KCL equations, and  $p$  is the number of loops and KVL equations. Therefore, since the numbers of unknowns and linear equations match, we may solve them. The equations are linear because Maxwell’s equations are linear for R, L, C circuits.

### C. Parallel-plate capacitors

Static electric fields between parallel metal plates are constrained by Maxwell’s equations:

$$\nabla \times \bar{E} = 0, \quad \nabla \cdot \bar{E} = \rho/\epsilon \tag{10}$$

If there is no free charge density  $\rho$  between the plates, then  $\nabla \cdot \bar{\mathbf{E}} = 0$ . Boundary conditions at a perfect conductor are:

$$\bar{\mathbf{n}} \cdot \bar{\mathbf{E}} = \rho_s/\epsilon, \quad \bar{\mathbf{E}}_{//} = 0 \quad (11)$$

Since  $\bar{\mathbf{E}}_{//} = 0$ , any  $\bar{\mathbf{E}}$  must be perpendicular to the conducting sheets, and since the fields must also be both curl-free and divergence-free, the fields must be uniform. Therefore  $\bar{\mathbf{E}} = \hat{\mathbf{y}} E_0$  has the correct form, where  $\bar{\mathbf{E}}$  points away from the positively charged surface, which has charge density  $\rho_s = \epsilon E_0$  [ $\text{Cm}^{-2}$ ]. The conducting sheets lie in the  $x$ - $z$  plane and have area  $A$ , so the total charge on the capacitor  $Q = \rho_s A = \epsilon E_0 A$  Coulombs.

The voltage  $V$  across the plates can be found by integrating the electric field from the positive to the negative terminal, so  $V = E_0 d$ .

We define the *capacitance*  $C$  of such an open structure, independent of shape, to be:

$$C = Q/V \text{ [Farads]} \quad (12)$$

Here, for a *parallel-plate capacitor*,

$$C = \epsilon E_0 A / E_0 d = \epsilon A / d. \quad (13)$$

Although  $Q = CV$  characterizes capacitors in a simple way, it is usually more relevant to relate  $i(t)$  to  $v(t)$ . Since  $q(t) = \int_{-\infty}^t i(t) dt = C v(t)$ , it follows that:

$$v(t) = (1/C) \int_{-\infty}^t i(t) dt \quad (14)$$

which is a familiar and useful relation, as is  $i(t) = C dv/dt$ .

Two *capacitors in parallel* ( $C_1$  and  $C_2$ ) have the same voltage  $V$  and are equivalent to a single capacitor  $C_{eq}$  having the equivalent charge  $Q_{eq} = Q_1 + Q_2$ . Therefore two capacitors in parallel have an increased total capacitance of:

$$C_{eq} = Q_{eq}/V = (Q_1 + Q_2)/V = C_1 + C_2 \quad (15)$$

Two *capacitors in series* have the same charge  $Q$  on each and have a total voltage  $V$  across the pair, where  $V$  is the sum of the voltages  $V_1 = Q/C_1$  and  $V_2 = Q/C_2$ . Therefore,  $1/C_{eq} = V/Q = (V_1 + V_2)/Q = 1/C_1 + 1/C_2$ , and two capacitors in series have a reduced total capacitance of:

$$C_{eq} = 1/(C_1^{-1} + C_2^{-1}) \quad (16)$$

### D. Parallel-plate resistors

The same parallel-plate geometry can be used to form *resistors*  $R$  using a medium of conductivity  $\sigma$  [Siemens  $\text{m}^{-1}$ ] bounded by plates of area  $A$  and separation  $d$ . Since  $\vec{J} = \sigma \vec{E}$  [ $\text{a m}^{-2}$ ] and  $I = AJ = A\sigma E_0 = A\sigma V/d = V/R$  amperes, it follows that:

$$R = d/\sigma A \text{ [ohms]} \quad (17)$$

The same logic used earlier for capacitors applies when two resistors are placed in series or parallel. When they are in series, the two currents are the same and the two voltages add, whereas if they are in parallel, the two voltages are the same and the currents add. This leads to the expressions:

$$R_{\text{eq}} = R_1 + R_2 \text{ ohms [resistors in series]} \quad (18)$$

$$R_{\text{eq}} = 1/(R_1^{-1} + R_2^{-1}) \text{ ohms [resistors in parallel]} \quad (19)$$

### E. Charge relaxation and RC circuits

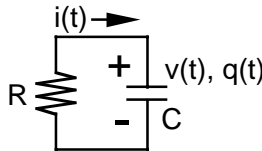
When a resistor and capacitor are connected in parallel, any charge  $q(t)$  on the capacitor will tend to discharge through the resistor, resulting in a decaying voltage as a function of time. We can solve for this voltage  $v(t)$  using:

$$q(t) = Cv(t) = \int i(t) dt, \text{ and} \quad (20)$$

$$v(t) = -i(t)R = -RC dv(t)/dt \quad (21)$$

where the direction of  $i(t)$  in (21) flows into the positive terminal of the capacitor, consistent with the definitions of  $v$  and  $i$  given in Figure 10-6.

Figure 10-6. RC circuit



The differential equation (21) states that  $v(t)$  equals its own first derivative times a constant. Only exponentials (and their sums, e.g. sines and cosines) have that property, so we guess the solution is:

$$v(t) = v_0 e^{-t/\tau} \quad (22)$$

where  $v_0$  is an initial condition. Substitution of (22) into (21) yields

$$v_0 e^{-t/\tau} = (-RC)(-1/\tau) v_0 e^{-t/\tau} \quad (23)$$

which is satisfied if  $\tau = RC$  seconds.

If we consider the parallel-plate resistor of Equations (17) and (13),  $RC = (d/A\sigma)(\epsilon A/d) = \epsilon/\sigma$  seconds, which is the “*charge relaxation* time constant”  $\tau$  of the medium  $\epsilon$ ,  $\sigma$ . It is easy to show that this time constant is not a function of the geometry of the plates or the initial charge distribution within the uniform medium; the charges, electric fields, and voltages retain their initial distribution, but all decay exponentially from that distribution with time constant  $\tau = RC$  seconds.

These two basic elements R and C plus the inductors L to be considered next suffice to build most passive linear lumped-element and distributed circuits.