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Implementation of a Sinusoidal Current Drive for a Brushless Three Phase Motor Using a Common Sense Resistor for Rotor Position Feedback

by

Gregory Emil Swize

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of

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Abstract

As the hard disk drive industry is pressured to lower the acoustic noise of their products, new methods must developed to lower the acoustic emissions from their motors. This paper uses a simple model of the three phase brushless motor to argue that the acoustic noise can be eliminated by driving the motor with sinusoidal currents. A brief analysis is then conducted to determine the voltage waveforms which will drive sinusoidal currents and make maximum use of the power supply.

The waveforms derived do not allow conventional motor position detection because all of the phases are driven simultaneously. Instead of sensing the BEMF as is normally done, a phase-locked loop (PLL) which senses current through one sense resistor is presented to provide the position feedback. The sinusoidal drive and associated phase locked-loop were then implemented on an actual hard drive. The acoustic measurements showed a drastic reduction in the pure-tone acoustic noise of the hard drive, and the testing demonstrated the feasibility of the design.

Thesis Supervisor: James L. Kirtley Jr.

Title: MIT Professor of Electrical Engineering

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I would first of all like to thank all of the people at Texas Instruments whose work and support made this thesis possible. Thanks must go to Ed Jeffrey for being my mentor for the past three years and telling me everything he knows about hard drives. I would also like to thank Ed for having enough confidence in my abilities to include me as a major part of the development team. Recognition and thanks must especially be given to Bert White, who was the man behind two of the sinusoidal detection schemes discussed in this paper. Without his original idea of the hook waveforms, this thesis would not have been possible. I would like to thank Wayne Reynolds for helping me out with the FPGA design tools, and for resetting the server for me whenever it crashed. How did I always forget it when it was so easy2guess? I would like to thank Hao Chen for answering my questions, working longer hours than I did, and taking the time to explain things to me even when he was under considerable time pressure himself. I would also like to thank Bill Sides for being of tremendous help in the lab.

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I must thank my thesis advisor, James Kirtley, for being the fastest professor on the planet when it came to getting back to me. You averaged getting back to me in a day, which is absolutely remarkable. Your speed made up for my lateness. Thank you for putting up with me.

Finally, I would like to thank my parents for sending me away MIT, although judging by the way they've been celebrating these last five years, maybe they should be thanking me that I went. I know they've done a lot for me, and I know that sending me here meant that they had to make some sacrifices. I hope that some day I can repay them.

And to anyone reading this....Enjoy!

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Chapter 1

Introduction

This thesis proposes a new method of driving a brushless three phase motor with the hope that the new drive scheme will reduce the pure tone acoustic noise of the motor. This thesis is geared towards the hard disk drive industry, which is under increasing pressure to reduce the noise emissions of their products. The results in this paper, can, however, be applied to any situation where the acoustic noise of a brushless three phase motor must be reduced.

As the world becomes more and more digital, businesses and people are needing ever-increasing amounts of digital storage capacity to handle the growing amount of digital information. To handle this growing sea of bits, companies which must store large amounts of data use Redundant Array of Inexpensive Drives or RAIDs to store their information. A RAID unit contains multiple hard drives which can be configured to either optimize data output or increase the redundancy of information in the RAID. Typically eight hard disk drives are located within one RAID unit. Because of the great number of hard drives in one unit, the acoustic noise emitted from the entire unit can be significant. The pure tone noise of each hard drive adds up and the result may be unbearable to a human operator which must be near the RAID. RAID manufacturers therefore place acoustic noise requirements on the drives which they purchase for installation in their products. Hard drive manufacturers must meet these demands, or suffer diminished sales [2], [3].

There are generally two avenues engineers can explore to reduce the acoustic noise of the hard drives. The mechanics of the system can be altered, or the electrical drive can be modified. There are a variety of mechanical design rules which can be used to reduce the

acoustic noise; the geometry of ball bearings can be more tightly controlled, or the poles and slots of the motor designed appropriately [1].

In the electrical arena, the acoustics come from the interaction of the phase currents with the magnetic elements in the motor. Harmonics of the current waveform generate forces in the phase windings of the motor. If these forces are at a mechanical resonance of the motor, the motor structure may vibrate and generate audible noise. The pure tone acoustic noise, which is the most objectionable, occurs at multiples of the electrical frequency of the motor.

The generation of this pure-tone noise can be diminished if the driving current is frequency modulated, or dithered. Dithering the current waveform spreads the harmonic energy over a range of frequencies [4]. This reduces the peak energy of the harmonic, and makes the noise less noticeable to the human ear. This technique does not remove the energy of the harmonic. Instead it takes advantage of how the human ear perceives sound, and moves the energy content of the acoustics into a less irritating form. This is a partial solution to the acoustic noise problem, but it is not a comprehensive solution because acoustic noise is still generated.

This paper will seek to develop and implement an electrical drive which will reduce the acoustic noise emissions of a brushless three phase motor. To reach that goal, some background information on a typical drive scheme is introduced in Chapter 1. Chapter 2 describes the thought process behind the generation of the ideal driving voltages which result in the lowest acoustic noise. Chapter 3 introduces the different techniques which may be used to control the phase voltage of the motor.

The most significant portion of this thesis is the phase-locked loop presented in Chapter 4. It is the development of this loop which allows the proposed system to be implemented in practice. Chapter 4 presents valuable relationships which allow the driving waveforms to be synchronized with the rotor position.

Finally, the results of testing the acoustic performance of the system are presented in Chapter 5.

1.1 Motor Model

The motor being examined in this thesis is a DC brushless three phase motor. This section will introduce the motor model, and define key terms for future reference. The model will be used in this chapter and all subsequent chapters to propose solutions and analyze their performance. Later in this section a classic drive system will be presented to illustrate the system-level differences between the drive schemes currently used, and the one proposed in this thesis.

Throughout this work, the motor will be modeled as an ideal, balanced three phase motor. The three phases are connected together in Wye formation. Each phase winding of the motor can be modeled as a series self-inductance, a series mutual inductance, a series resistance, and a back electromotive force (BEMF) generator.

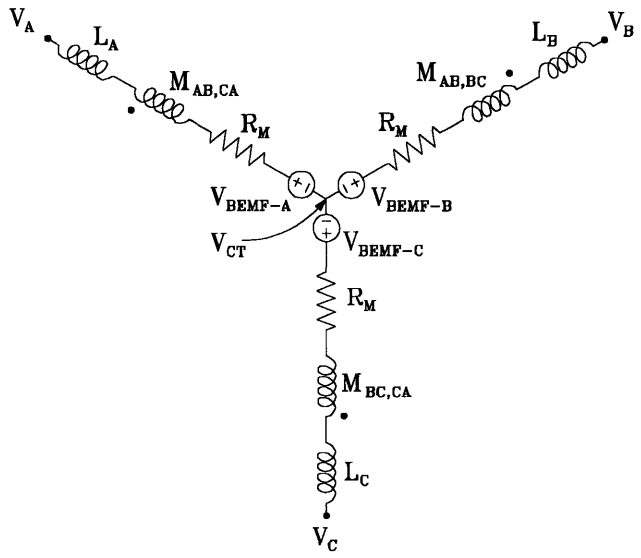

Figure 1-1: Three Phase Motor Model

The mutual inductances, $M_{AB,CA}$, $M_{AB,BC}$, and $M_{BC,CA}$, are the combined mutual inductances in each phase. For illustration, the voltage drop across the mutual inductances in phase A will be

$$M_{AB} \cdot \frac{dI_B}{dt} + M_{CA} \cdot \frac{dI_C}{dt}. \tag{1.1}$$

The phases are all connected together, so the sum of the phase currents equals zero. Assuming that the mutual inductances are equal, and recognizing that $I_B + I_C = -I_A$, the voltage induced in phase A by the mutual inductance is

$$-M \cdot \frac{dI_A}{dt}. \tag{1.2}$$

where $M = M_{AB} = M_{CA}$.

The induced voltages in the phase can therefore be expressed as a single inductance, L_M. L_M is the self-inductance minus the mutual-inductance. The motor model can then be simplified to be

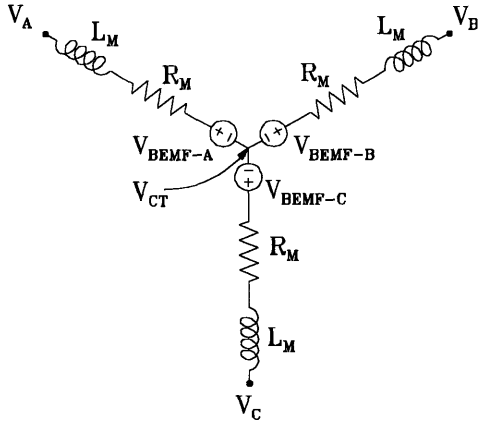

Figure 1-2: Simplified Three Phase Motor Model

The phases of the motor are spatially shifted relative to each other by $\frac{2\pi}{3}$ radians. Because the BEMF generators are proportional to the flux linkage of the motor, the BEMF waveforms are also are shifted by $\frac{2\pi}{3}$ radians. If ω_0 is the electrical frequency of the motor, then the BEMF generators can be written in terms of some periodic function, $f(\omega_0 t)$, as

$$V_{BEMF-A} = V_{BEMF-A}(t) = K_T \omega_0 f(\omega_0 t), \tag{1.3a}$$

$$V_{BEMF-B} = V_{BEMF-B}(t) = K_T \omega_0 f\left(\omega_0 t - \tfrac{2\pi}{3}\right), \tag{1.3b}$$

$$V_{BEMF-C} = V_{BEMF-C}(t) = K_T \omega_0 f\left(\omega_0 t + \tfrac{2\pi}{3}\right), \tag{1.3c}$$

where

K_T = motor constant.

The exact form of $f(\omega_0 t)$ depends upon the construction of the motor. In most cases, the flux linkage of the motor is made to approximate a sinusoidal form, so $f(\omega_0 t)$ is very nearly sinusoidal. In some applications, the BEMF is shaped to be more trapezoidal in an attempt to reduce torque ripple. Although $f(\omega_0 t)$ will always assumed to be sinusoidal throughout this work, equations (1.3) are written generally as a reminder that the acoustic noise of the motor could be due to the mechanics, and not the electronics, of the system.

The phase currents can be easily expressed in terms of the center tap voltage, V_{CT}, and the corresponding phase voltage and BEMF generator. Using bold type to represent the Fourier transforms of the corresponding functions, the currents can be expressed in the frequency domain as

$$\mathbf{I_A}(\omega) = \frac{\mathbf{V_A}(\omega) - \mathbf{V_{CT}}(\omega) - \mathbf{V_{BEMF-A}}(\omega)}{L_M j\omega + R_M}, \tag{1.4a}$$

$$\mathbf{I_B}(\omega) = \frac{\mathbf{V_B}(\omega) - \mathbf{V_{CT}}(\omega) - \mathbf{V_{BEMF-B}}(\omega)}{L_M j\omega + R_M}, \tag{1.4b}$$

$$\mathbf{I_C}(\omega) = \frac{\mathbf{V_C}(\omega) - \mathbf{V_{CT}}(\omega) - \mathbf{V_{BEMF-C}}(\omega)}{L_M j\omega + R_M}. \tag{1.4c}$$

When the motor is operated properly, the phase voltages are driven with periodic voltages at a frequency of ω_0. Like the BEMF generators, the phase voltages are shifted relative to each other by $\frac{2\pi}{3}$ radians. In terms of the periodic function $g(\omega_0 t)$, the phase voltages can be written as

$$V_A = V_A(t) = g(\omega_0 t), \tag{1.5a}$$

$$V_B = V_B(t) = g\left(\omega_0 t - \tfrac{2\pi}{3}\right), \tag{1.5b}$$

$$V_C = V_C(t) = g\left(\omega_0 t + \tfrac{2\pi}{3}\right). \tag{1.5c}$$

For future reference, the terminal characteristics will now be derived. We begin by solving for the center tap voltage, V_{CT}. The center tap voltage can be expressed in terms of the phase voltages and the BEMF generators. The value of V_{CT} can be found by adding the three phase currents in (1.4) together, and setting the sum equal to zero. The equation can then be solved for V_{CT} to give

$$V_{CT} = \tfrac{1}{3}\cdot(V_A + V_B + V_C) - \tfrac{1}{3}\cdot(V_{BEMF-A} + V_{BEMF-B} + V_{BEMF-C}). \tag{1.6}$$

In later chapters, it will be extremely helpful if the center tap voltage is expressed in terms of only one phase voltage and one BEMF generator. The sum of V_A, V_B and V_C in (1.6) can be combined by first expressing V_A by its Fourier series,

$$V_A(t) = \sum_{n=0}^{\infty} V_{An} \cos(n\omega_0 t - \nu_{An}), \tag{1.7}$$

where

ν_{An} = phase shift of nth harmonic,

V_{An} = amplitude of nth harmonic.

Making use of the fact that V_B and V_C are simply phase shifted versions of V_A, the sum of the three phase voltages can be written as

$$\begin{aligned} V_A + V_B + V_C = &\sum_{n=0}^{\infty} V_{An} \cos(n\omega_0 t - \nu_{An}) \\ &+ \sum_{n=0}^{\infty} V_{An} \cos(n\omega_0 t - \nu_{An} - \tfrac{2\pi}{3} n) \\ &+ \sum_{n=0}^{\infty} V_{An} \cos(n\omega_0 t - \nu_{An} + \tfrac{2\pi}{3} n). \end{aligned} \tag{1.8}$$

Using the trigonometric identity $\cos(a \pm b) = \cos(a)\cos(b) \mp \sin(a)\sin(b)$, equation (1.8) can be simplified to

$$V_A + V_B + V_C = 3\sum_{n=0}^{\infty} V_{An} \cos(n\omega_0 t - \nu_{An}) \left[\tfrac{1}{3} + \tfrac{2}{3}\cos(n\tfrac{2\pi}{3})\right]. \tag{1.9}$$

Equation (1.9) can be expressed in the frequency domain as the result of filtering the phase voltage $\mathbf{V_A}$ with some filter, $\mathbf{C}_{\omega_0}(\omega)$. Defining the filter as

$$\mathbf{C}_{\omega_0}(\omega) = \tfrac{1}{3} + \tfrac{2}{3}\cos\left(\omega \tfrac{2\pi}{3\omega_0}\right), \tag{1.10}$$

the sum of the driving voltages can be written in the frequency domain as

$$\mathbf{V_A}(\omega) + \mathbf{V_B}(\omega) + \mathbf{V_C}(\omega) = 3 \cdot \mathbf{V_A}(\omega) \cdot \mathbf{C}_{\omega_0}(\omega). \tag{1.11}$$

For input frequencies which are a multiple of three times the fundamental frequency, $\mathbf{C}_{\omega_0}(\omega) = 1$. For all other integer multiples of the fundamental, $\mathbf{C}_{\omega_0}(\omega) = 0$. The sum of the three phase voltages therefore only contains triple-n harmonics. The relationship expressed in (1.11) can be applied to the three BEMF generators, and that result along with (1.11) can be substituted back into (1.6) to write the center tap voltage as

$$\mathbf{V_{CT}}(\omega) = \mathbf{V_A}(\omega) \cdot \mathbf{C}_{\omega_0}(\omega) - \mathbf{V_{BEMF-A}}(\omega) \cdot \mathbf{C}_{\omega_0}(\omega). \tag{1.12}$$

Equation (1.12) is useful because the phase currents can now be expressed solely in terms of their terminal voltages and BEMF generator. Substitution of (1.12) into (1.4a) allows the current in phase A to be written as

$$\mathbf{I_A}(\omega) = \frac{\mathbf{V_A}(\omega) \cdot \left(1 - \mathbf{C}_{\omega_0}(\omega)\right) - \mathbf{V_{BEMF-A}}(\omega) \cdot \left(1 - \mathbf{C}_{\omega_0}(\omega)\right)}{L_M j\omega + R_M}. \tag{1.13}$$

The transfer function $\left(1 - \mathbf{C}_{\omega_0}(\omega)\right)$ results in the removal of all of the triple-n harmonics of V_A and $V_{BEMF\text{-}A}$. The result of filtering V_A and $V_{BEMF\text{-}A}$ with $\left(1 - \mathbf{C}_{\omega_0}(\omega)\right)$ will be referred to often in this paper. To make the discussion progress more smoothly, two new variables, V_A^* and V_{BEMF-A}^*, are introduced. V_A^*, the composite driving voltage, and V_{BEMF-A}^*, the composite BEMF voltage, are defined respectively as

$$\mathbf{V}_{\mathbf{A}}^{\star}(\omega) = \mathbf{V}_{\mathbf{A}}(\omega) \cdot \left(1 - \mathbf{C}_{\omega_0}(\omega)\right), \tag{1.14}$$

$$\mathbf{V}_{\mathbf{BEMF-A}}^{\star}(\omega) = \mathbf{V}_{\mathbf{BEMF-A}}(\omega) \cdot \left(1 - \mathbf{C}_{\omega_0}(\omega)\right). \tag{1.15}$$

Equation (1.13) can then be written more compactly as

$$\mathbf{I}_{\mathbf{A}}(\omega) = \frac{\mathbf{V}_{\mathbf{A}}^{\star}(\omega) - \mathbf{V}_{\mathbf{BEMF-A}}^{\star}(\omega)}{L_M j\omega + R_M}. \tag{1.16}$$

The final relationship which is of significance for this study is the relationship between torque and current. The torque of a three phase motor has the same functional dependency as the BEMF, so the torques can be written as

$$T_A = I_A \cdot K_T \cdot f(\omega_0 t), \tag{1.17a}$$

$$T_B = I_B \cdot K_T \cdot f\left(\omega_0 t - \tfrac{2\pi}{3}\right), \tag{1.17b}$$

$$T_C = I_C \cdot K_T \cdot f\left(\omega_0 t + \tfrac{2\pi}{3}\right). \tag{1.17c}$$

The sum of the individual phase torques can be expressed using the relation in (1.11). The total torque therefore contains no triple-n harmonics, and

$$\mathbf{T}_{\mathbf{TOT}}(\omega) = 3 \cdot \mathbf{T}_{\mathbf{A}}(\omega) \cdot \mathbf{C}_{\omega_0}(\omega). \tag{1.18}$$

1.2 Conventional Six-State Motor Drive

The standard drive scheme used in the hard disk drive industry is six-state drive. A brief overview of this drive system is presented here to familiarize the reader with drive schemes which are competing against the sinusoidal drive presented in this paper. The drive scheme outlined here will later be implemented and used as a control to test the acoustic performance of the sinusoidal drive. A system top-level diagram of a six-state controller is shown if Figure 1-2.

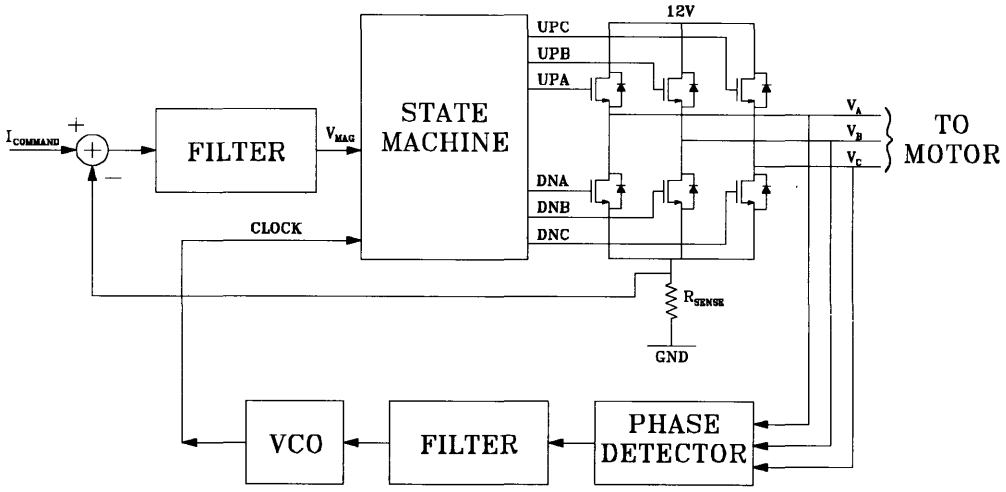

Figure 1-3: Top-Level Control Diagram for a Six-State Driver

Fundamentally, a six-state driver consists of a state machine, three half H-bridge power drivers, a phase detector, and a voltage controlled oscillator (VCO). In each state of the state machine, the gates of the power devices are controlled to put appropriate voltages onto the motor phases. The rotor position is sensed on the phase voltages, and the information used to clock the state machine at the appropriate frequency.

1.2.1 Typical Voltage Waveforms

The six-state drive scheme is commonly used because it is easy to implement and provides a straightforward method of locking the driving voltages to the motor position. In six-state drive, each phase of the motor cycles through three states during one electrical cycle. The phase can be held at ground, driven to some positive voltage, or floated. If the phases are controlled such that one phase is floating, one phase is driven to ground, and the third is driven to some voltage, V_{HIGH}, then the motor can be in one of six states. These six states, and the states of the motor phases, are summarized in Table 1.1.

State	V_A	V_B	V_C
0	Floating	0	Floating
1	V_{HIGH}	Floating	0
2	V_{HIGH}	V_{HIGH}	0
3	Floating	V_{HIGH}	Floating
4	0	Floating	V_{HIGH}
5	0	0	V_{HIGH}

Table 1.1: Driving Voltages for Six-State Control

The voltage V_{HIGH} controls the amount of current, and thus the amount of torque delivered to the motor. V_{HIGH} can either be a constant value, or the average of a pulse-width modulated (PWM) signal. PWM is the preferred method of voltage control because it reduces the amount power dissipated in the power devices. The power devices are n-MOS transistors with built-in body diodes. By switching a transistor either entirely on or entirely off, the power losses in the transistors can be lowered. The drivers are implemented as shown in Figure 1-2.

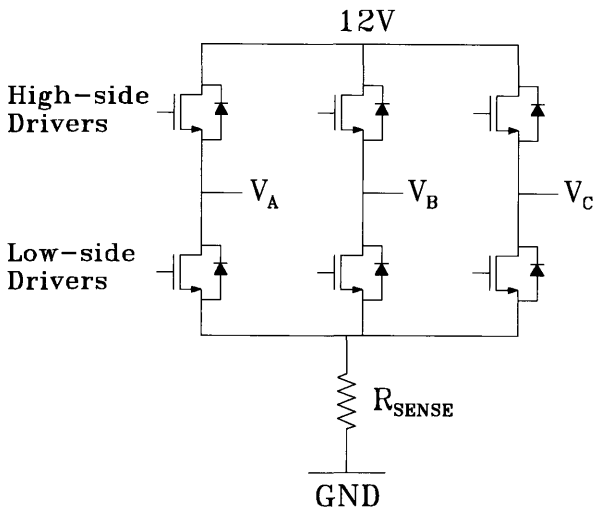

Figure 1-4: MOSFET Drivers Used to Control Phase Voltages

The body diodes allow the current to naturally commutate between the high-side drivers and low side drivers when the transistors switch on and off. If current is being sourced into phase A when the high-side driver of phase A is on, then when the high-side switches off, the current will flow through the low-side body diode. A phase of the motor may be floated by bringing the gate voltage on both the low-side and high-side drivers down to ground.

1.2.2 Locking Voltage Waveforms to BEMF

A significant benefit of the six-state drive is that it allows straightforward detection of the BEMF phase. During the times when a phase is undriven, no current is flowing through the phase, so there is no voltage drop across the winding due to its impedance. When a phase is floated, its voltage is equal to the BEMF voltage plus the center tap voltage. During State Three, V_A is floating, so its phase voltage is

$$V_A = \tfrac{1}{3}(V_A + V_B + V_C) - \tfrac{1}{3}(V_{BEMF-A} + V_{BEMF-B} + V_{BEMF-C}) + V_{BEMF-A}. \qquad (1.19)$$

Solving (1.19) for V_A, we find that

$$V_A = \tfrac{3}{2} V^*_{BEMF-A} + \tfrac{1}{2}(V_B + V_C). \tag{1.20}$$

Equation (1.20) illustrates the important consequence of six-state drive-the BEMF can be detected on the undriven phase. Since one phase is undriven at all times, BEMF phase information can always be acquired. The BEMF waveform is recovered from the undriven phase by subtracting the average of the two driven phases from the undriven phase. The signal is then passed through a phase detector to generate a signal proportional to the phase error of the BEMF. The phase error signal is then filtered and integrated to generate the input into the VCO. The VCO then outputs a clock signal which is used to commutate the motor.

Optimal performance of the motor is obtained by aligning the phase currents with their associated BEMF voltages. This can be approximately done by aligning the BEMF waveform with the voltage waveform as in Figure 1-3.

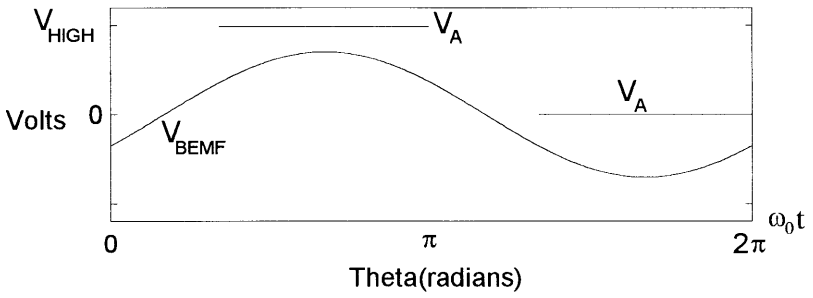

Figure 1-5: BEMF Voltage Aligned with Phase Voltage.

V_A in Figure 1-5 is shown only when the phase is being driven. The regions when the phase is not driven are omitted because the phase voltage will then be as expressed in (1.20). When the BEMF waveform is in phase with the driving voltage, the zero-crossing of the BEMF is visible. A comparator can be used to detect this zero-crossing, and the zero-crossing information used to generate a phase error.

1.2.3 Locking Motor Current to Commanded Current

The magnitude of the driving voltages can either be controlled directly, or by using a current feedback loop. The six-state drive scheme presented in this paper will use a current feedback loop to maintain the proper voltage level of the driving waveforms. If the speed of the current loop is slow, then the loop will set the average current flowing through the motor. If it is fast, then it can have the effect previously described of aligned the current with the BEMF.

1.2.4 Locking Motor Speed to Commanded Speed

The current command, $I_{COMMAND}$, in Figure 1-3 is controlled via an external speed regulation loop. Measurements of the motor speed are made and the error between the actual speed and the desired speed results in a change in the current command.

Chapter 2

Development of Sinusoidal Drive Scheme

In Chapter 1, the six-state control system for a hard drive motor was presented. In this chapter, the sources of acoustic noise in the six-state drive scheme are briefly examined, and the motivation for a sinusoidal current drive presented. Next, possible voltage waveforms are examined and the optimal waveform is derived. The waveforms presented at the end of this chapter were first proposed by Bert White of Silicon Systems, Inc.

2.1 Problem with Six-State: Torque Harmonics

The weakness of the six-state drive scheme presented in Chapter 1 is that it introduces acoustic noise into the motor. The current waveform created by the switching scheme has very abrupt transitions. When phase A is held high, the power supply sources current to the phase and the current magnitude is positive. When phase A is floated, the current in the phase drops to zero as quickly as the inductor will allow. Because the torque is proportional to the current, it too will change abruptly. If harmonics in the torque waveform excite mechanical resonances in the motor, or hard drive assembly, then the noise generated may become audible.

2.2 Solution to Acoustic Noise: Sinusoidal Currents

In order to develop a quieter electrical drive, a driver must be developed which reduces the harmonic content of the torque. Because the phase torque is the product of the phase

current and the flux linkage, which has the same time varying form as the BEMF waveform, the harmonic content of the torque can be modified by modifying the phase current. Ideally, the phase current would be chosen to match the BEMF waveform so that the product of the two equaled the ideal torque waveform. The ideal phase torque is $T_{IDEAL}\cos^2(\omega_0 t)$. The ideal torque waveform has this form because it contains only one frequency at twice the driving frequency. The ideal current waveform is then defined as

$$I_{IDEAL}(t) = \frac{T_{IDEAL}\cos^2(\omega_0 t)}{K_T f(\omega_0 t)}. \tag{2.1}$$

Creation of an ideal phase current for a particular $f(\omega_0 t)$ is not always possible. The function $f(\omega_0 t)$ is proportional to the flux linkage of the motor, so it must pass through zero at some point during an electrical cycle. If the zeros of $f(\omega_0 t)$ do not cancel with the zeros of $\cos^2(\omega_0 t)$, then the ideal phase current must be infinite at those points. Attempting to actually derive the ideal current waveform for any individual motor is impractical. It is best to simply assume that the BEMF is sinusoidal. This means that in order to reduce the harmonics of the torque, the motor must be driven with sinusoidal currents. The phase voltages should therefore be chosen so that the phase currents are pure sine waves.

2.3 Generation of Sinusoidal Currents

In order to drive sinusoidal currents through the motor, a suitable set of driving voltages must be formulated. Referring back to equation (1.16), in order for the phase current to have a sinusoidal form, the difference of V_A^* and V_{BEMF-A}^* must be sinusoidal. We are assuming that the BEMF is sinusoidally varying, so V_{BEMF-A}^* is a pure sinusoid and therefore V_A^* must also be a pure sinusoid as well. Because V_A^* contains all but the triple-n harmonics of V_A, restricting the harmonic content of V_A^* only restricts the harmonic content of V_A at frequencies

other than three times the fundamental frequency. If V_A^* must be purely sinusoidal, then the only non-zero term of the Fourier series of V_A^* is V_{A1} and we can say that $V_A^* = V_{A1}\cos(\omega t - \nu_{A1})$. V_A will therefore contain this term in its Fourier series, along with any other terms at the triple-n harmonics. In general then, the phase voltage which results in sinusoidal currents has the form

$$V_A = V_{A0} + V_{A1}\cos(\omega_0 t - \nu_1) + 0 + V_{A3}\cos(3\omega_0 t - \nu_3) + 0 + 0 + V_{A6}\cos(6\omega_0 t - \nu_6) + \ldots. \tag{2.2}$$

The coefficients and phase shifts in equation (2.2) can be chosen in any arbitrary manner and the composite driving voltage will still contain only the fundamental component. There are countless ways to select these coefficients, and two of the most sensible are presented in this chapter. The first method is the more obvious of the two, and selects the coefficients so that each phase is driven with a sinusoidal voltage. The second method will emerge as the preferred method and selects the coefficients so that the power supply is fully utilized.

2.3.1 Sinusoidal Voltages

Driving each of the phases with a sinusoidal drive is the easiest conceptual way of obtaining the desired harmonic-free current. Because only one power supply is being used, the sine wave must be offset by half of the supply voltage, V_{SUP}. The sinusoidal voltage drive is not, however, the most optimal way of driving the motor. The efficiency of this system can be quantified by examining how effectively the drive scheme makes use of the available power supply. For a phase voltage offset by $\frac{1}{2}V_{SUP}$, the maximum amplitude of the sinusoid is only $\frac{1}{2}V_{SUP}$. The composite driving voltage therefore also has a magnitude of $\frac{1}{2}V_{SUP}$. As will be shown in the following section, this does not make optimal use of the power supply. Although conceptually simple, sinusoidal voltage drives are not the best technique.

2.3.2 Hook Voltages

There are an infinite number of driving waveforms which will result in a sinusoidal composite driving voltage, V_A^*. The only restraint on all of them is that their frequency content consist only of triple-n harmonics and a fundamental component. The Fourier coefficients of V_A may be chosen to create a waveform which makes optimal use of the power supply, or they may be chosen to fulfill some other special requirement of the system. For our system, we will impose two additional constraints on the harmonic coefficients of V_A. First, the coefficients must be chosen so that the phase voltages are never negative. This constraint stems from the fact that only one power supply referenced to ground will be used. This constraint is easily met, because a simple change of V_{A0} will make any waveform non-negative. The second added constraint is that the power supply must be used as effectively as possible. The second constraint is more difficult to meet, and requires the selection of all of the Fourier coefficients and phases.

Finding these coefficients by working with them directly is difficult and clumsy. A better approach is to manipulate the ideal composite driving voltage so that the resulting phase voltages satisfy our requirements. The first step in deriving the optimal waveforms requires rewriting the composite driving voltage in terms of the phase-phase voltages of the system. This is key to formulating an expression for the optimal waveform. The composite driving voltage is equal to V_A minus V_{CT}. If V_{CT} is expressed in terms of phase voltages, then the composite driving voltage can be written in terms of phase-phase voltages as

$$V_A^* = \frac{V_{AB} - V_{CA}}{3}. \tag{2.3}$$

We cannot make any assumptions about the form of V_{AB} and V_{CA}, at this time, but we can prove they must be sinusoidal. If we write V_{AB} in terms of V_A, then since V_B is delayed by $\frac{2\pi}{3}$ radians, V_{AB} can be expressed in the frequency domain as

$$\mathbf{V_{AB}}(\omega) = \mathbf{V_A}(\omega)\left(1 - e^{-j\frac{2\pi}{3\omega_0}\omega}\right). \tag{2.4}$$

The filtering expressed in (2.4) has the effect of zeroing out the triple-n harmonics of V_A. Since V_A must have the form presented in (2.2), with non-zero coefficients only at the triple-n harmonics and at the fundamental, we may conclude that V_{AB} is a pure sine wave with the form

$$V_{AB} = \sqrt{3} \cdot V_{A1} \cos\left(\omega_0 t - \nu_{A1} + \frac{\pi}{6}\right), \tag{2.5}$$

where

V_{A1} = amplitude of fundamental of V_A,

ν_{A1} = phase shift of fundamental of V_A.

The ability to express the phase-phase voltage as a simple sinusoid allows us to rephrase the maximization problem in a more readily solvable manner. In order to make more efficient use of the power supply voltage, the magnitude of V_A^* must be maximized. From equation (2.3), it is seen that maximizing the amplitude of V_A^* is analogous to maximizing the amplitude of V_{AB} minus V_{CA}. This amplitude is maximized by making the phase-phase voltages as large as possible for a given power supply. The phase-phase voltages will be defined as in Figure 2-1.

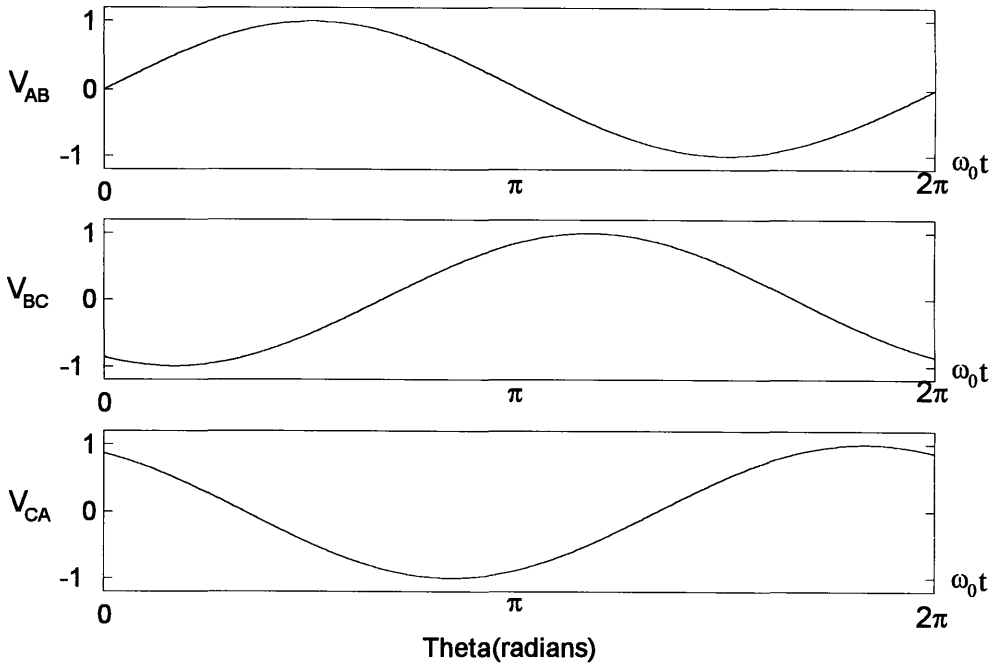

Figure 2-1: Phase-Phase Voltages

The phase-phase voltages must be somehow converted to phase-ground voltages. V_{1A} and V_{1B} will refer to the phase voltages obtained by manipulating the phase-phase voltage V_{AB}. The magnitude of V_{AB} can be made as large as possible if V_{1A} is set equal to the positive portion of V_{AB}, and $-V_{1B}$ is set equal to the negative portion of V_{AB}. Both phase voltages will then be entirely positive each can be raised as high as V_{SUP}. The magnitude of the phase-phase voltage in this case will also be V_{SUP}. V_{BC} and V_{CA} can be broken up in a similar manner to give V_{2B} and V_{2C}, and V_{3C} and V_{3A}, respectively. The results of each of these divisions is presented in Figure 2-2.

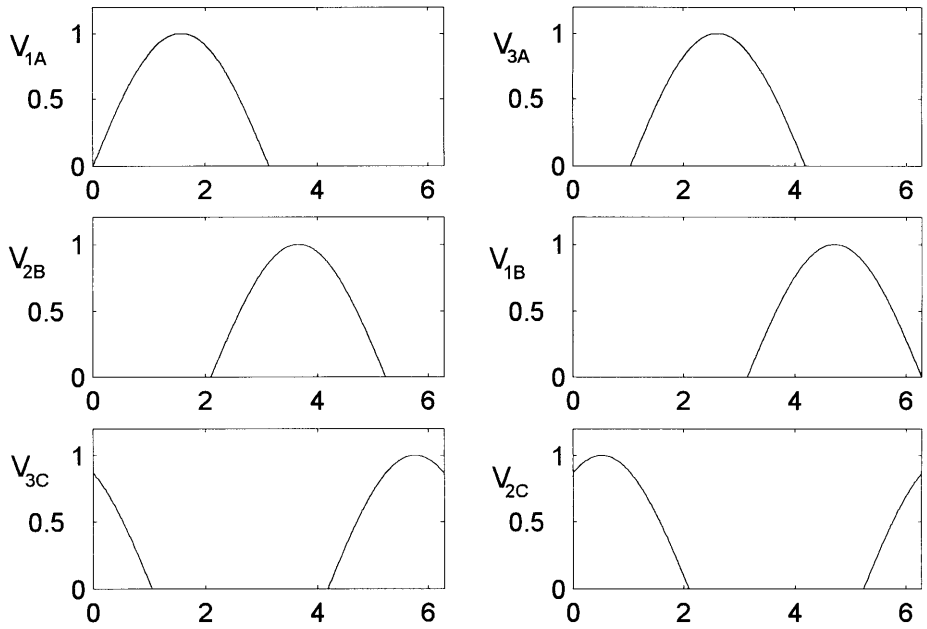

Figure 2-2: Phase Voltages Resulting from Splitting up Phase-Phase Voltages

The phase voltages presented in Figure 2-2 are not compatible with each other. V_{1A} does not equal V_{3A}, and the waveforms for the other phases do not match either. Each phase-phase voltage places different constraints on the phase-ground voltages. The difference between these waveforms must somehow be removed. The inequality between V_{1A} and V_{3A} can be eliminated by adding an appropriate waveform, V_1, to V_{1A} and V_{1B} and a second waveform , V_3, to V_{3C} and V_{3A}. Because V_1 is added into both V_{1A} and V_{1B}, phase-phase voltage V_{AB} will still be sinusoidal. The same is true for V_{CA}. V_1 and V_3 should be chosen so that

$$V_{1A} + V_1 = V_{3A} + V_3. \tag{2.6}$$

Equation (2.6) can be rearranged so that the known waveforms V_{1A} and V_{2A} are on the left-hand side of the equation,

$$V_{1A} - V_{3A} = V_3 - V_1. \tag{2.7}$$

Plotting the left hand side of equation (2.7) results in the waveform in Figure 2-3.

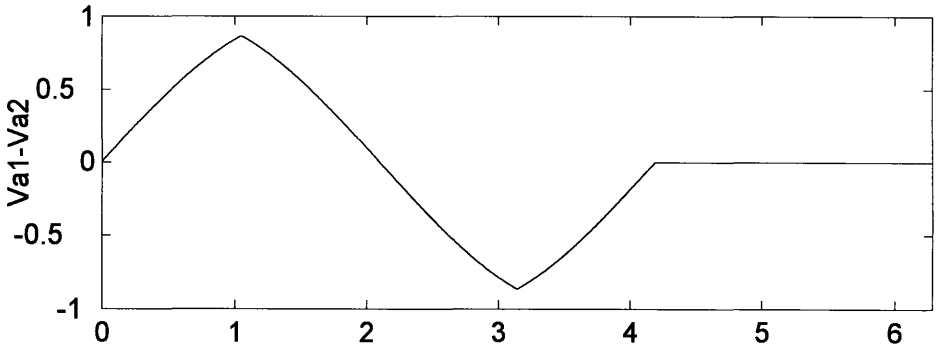

Figure 2-3: Difference of Correction Voltages V_3 and V_1

The waveform in Figure 2-3 is also equal to the difference between V_3 and V_1. V_1 and V_3 must be chosen so that their difference results in the waveform in Figure 2-3. Because V_{1A} is zero for half of the cycle, and V_{1B} is zero for the other half, V_1 must be positive at all times so that the sum of V_1 plus V_{1A} and V_{1B} remains positive. Similar reasoning places the same constraints on V_2 and V_3. This motivates us to set V_3 equal to the positive portion of V_3-V_1 and set -V_1 equal to the negative portion. Similar processing on the other phase voltages lead to a compatible set of correction voltages, V_1, V_2, and V_3. When these correction voltages are added into the original phase voltages, the waveforms in Figure 2-4 result.

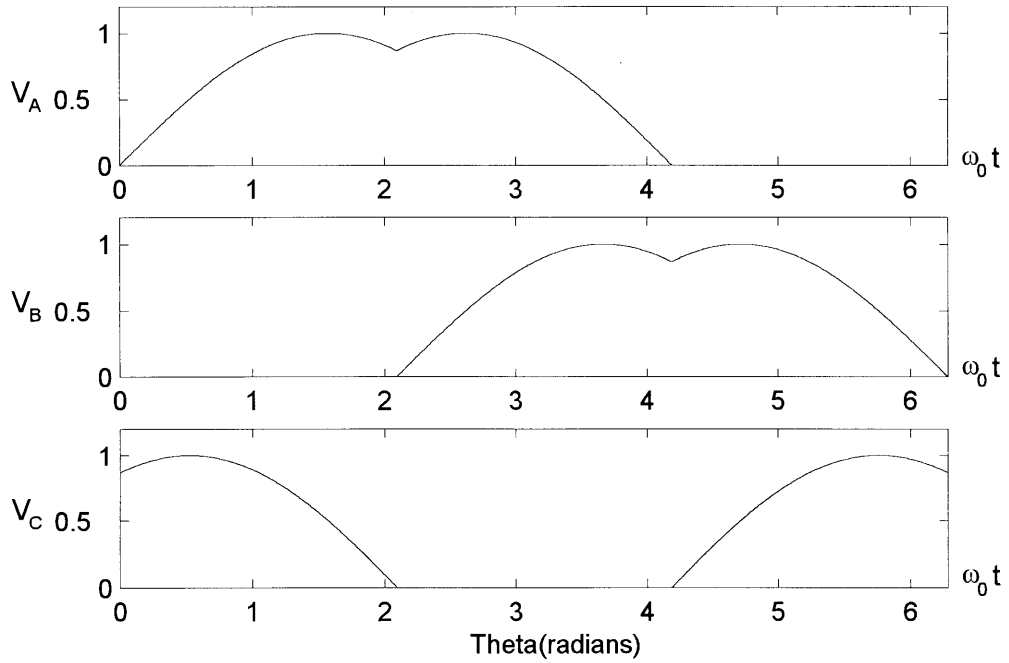

Figure 2-4: Hook Waveforms-Optimal Phase Voltage Waveforms

The waveforms in Figure 2-4 are referred to as hook waveforms and were first proposed by Bert White of Silicon Systems, Inc., as a method of generating sinusoidal currents. If hook($\omega_0 t$) is used to designate the function that returns a hook waveform of height one, then the phase voltages of the motor can be written as

$$V_A(t) = V_{MAG} \cdot \text{hook}(\omega_0 t), \tag{2.8a}$$

$$V_B(t) = V_{MAG} \cdot \text{hook}\left(\omega_0 t - \tfrac{2\pi}{3}\right), \tag{2.8b}$$

$$V_C(t) = V_{MAG} \cdot \text{hook}\left(\omega_0 t + \tfrac{2\pi}{3}\right), \tag{2.8c}$$

where

V_{MAG} = magnitude of driving voltage.

The hook waveform is the optimal voltage drive which will generate sinusoidal currents. When the phases are driven with the waveforms defined as in (2.8), the composite driving voltage is

$$V_A^* = \tfrac{1}{3}\left(V_{AB} - V_{CA}\right) = \frac{V_{MAG}}{\sqrt{3}} \cdot \sin\left(\omega t - \tfrac{\pi}{6}\right). \qquad (2.9)$$

The maximum value of V_{MAG} is V_{SUP}, so the maximum magnitude of the composite driving voltage is $\frac{1}{\sqrt{3}} V_{SUP}$. This method of driving the waveforms is therefore $\frac{2}{\sqrt{3}} \approx 1.15$ times better than the sinusoidal voltages power with respect to supply utilization.

Chapter 3

Controlling the Phase Voltage

The voltage waveforms developed in the previous chapter must now be driven onto the motor phases. As with the six-state drive scheme, the voltage magnitude can be controlled either with a linear controller or a PWM controller. PWM control reduces the amount of power dissipated in the power switching devices, so it will be used to drive the hook waveforms onto the motor phases.

3.1 Generation of PWM Signals

There are several possible ways of generating the PWM signal required to drive the motor. The one which will be discussed here uses comparison of the hook waveform to a triangle wave. Provided the frequency of the triangle waveform is sufficiently fast, the PWM will accurately represent the hook waveform. Setting the PWM signal frequency at 60 times the electrical frequency of the motor results in satisfactory representation of the hook waveform. If the motor spins at 7200 RPM and has 6 poles, then the frequency of the voltage modulation is 21.6 kHz. This frequency is beyond the range of human hearing, so it should not introduce audible noise.

Unlike the six-state case in which only one phase was being modulated in any given state, sinusoidal drive requires that two phases be modulated at the same time. The PWMs of these two motor phases do not necessarily have to be in phase with each other. They can either be in phase, out of phase by π radians, or have any phase shift in between. Only phase shifts of 0

and π radians will be discussed here. These two different modulation methods will have different effects on the appearance of the current waveform.

In order to compare the effects of in-phase switching and out-of-phase switching, the effects during one full cycle will be examined. Recalling the pictures in Figure 2-4, one phase of the motor will be held low during any state, and the other two states will be modulated at duty cycles determined by the height of the waveform. For the following discussion, it will be assumed that phases A and B are being modulated, and that phase C is held low.

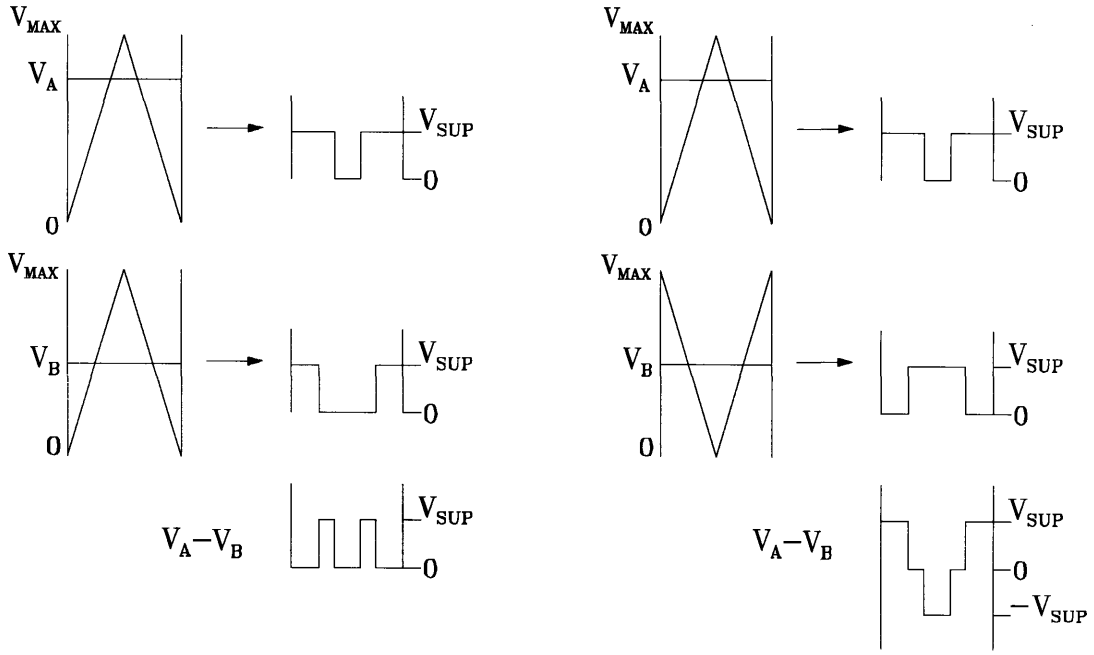

Figure 3-1: In-Phase and Out-of-Phase PWM

3.2 In-Phase PWM

When the two triangle waves are in phase with each other, the pulse associated with one PWM cycle for each phase is as shown in Figure 3-1. It is apparent that in general both phases are held high at the same time during one PWM cycle. The exact amount of overlap depends on the voltage being driven on each phase of the motor. If the voltage level being

compared against the triangle waveform is assumed to be DC, then the pulses will be centered in the middle of the switching cycle.

The fact that the two phases are driven high at the same time has important consequences for the phase-phase voltages. When the PWMs from the two cycles are subtracted from each other to obtain the phase-phase voltage V_{AB}, a new PWM signal is generated. The exact form of V_{AB} depends on the duty cycles of V_A and V_B. As V_A and V_B switch, V_{AB} can cycle through different values depending upon the order of the rising and falling edges of V_A and V_B. Figure 3-2 shows the possible switching orders of V_{AB}.

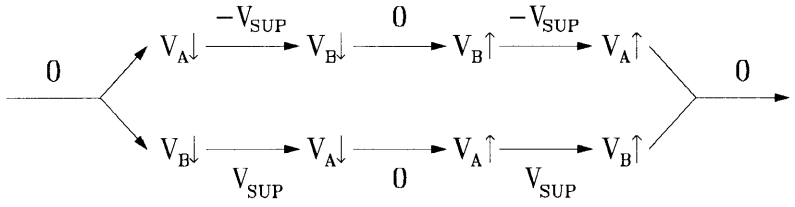

Figure 3-2: Possible Switching Orders for In-Phase PWM

In Figure 3-2, $V_A\uparrow$ indicates a rising edge of V_A, $V_A\downarrow$ indicates a falling edge, and similarly for V_B. The horizontal arrows represent the order of switching events and the numbers above them indicate the value of V_{AB}. When the PWM waveforms are in phase, the waveform V_{AB} only changes between two levels in any given cycle.

3.3 Out-of-Phase PWM

When the two triangle waves are out of phase with each other, the pulse associated with one PWM cycle for each phase is as shown in Figure 3-1. From Figure 3-1 it is apparent that the phases are held high generally at different times during the switching cycle. This will result in a different PWM for V_{AB} than was found for the in-phase technique. The same type

of diagram can be used to represent the switching cycle of the out-of-phase PWM. For the out-of-phase PWM the switching diagram is as shown in Figure 3-3.

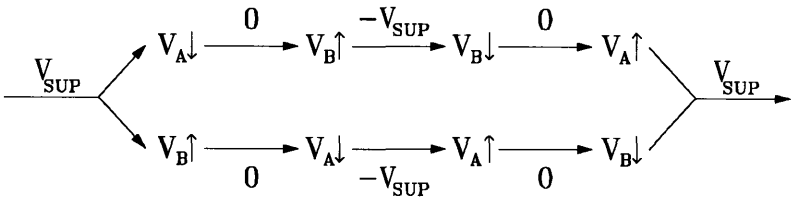

Figure 3-3: Possible Switching Orders for Out-of-Phase PWM

Figure 3-3 illustrates a shortcoming of the out-of-phase switching technique. The PWM of the phase-phase voltage switches over a range of three levels while the in-phase technique switches over only two. These added levels represent a less than optimal means of generating a DC voltage. If the average of V_{AB} over one cycle is between V_{SUP} and 0, then the PWM should switch only between those two levels to minimize the energy in the switching frequency of the PWM waveform. When the two PWM signals are out of phase with each other, the PWM for V_{AB} changes between V_{SUP}, 0 and $-V_{SUP}$. This is twice the switching magnitude of the in-phase scheme. Doubling the swing of the PWM results in a doubling of the energy at the switching frequency. This will most likely not degrade the acoustic performance of the system because the frequency of the PWM is well beyond the range of human hearing. The effects of the two PWM switching schemes will be discussed again in Chapter 4 because of their role in closing the phase locked loop.

Chapter 4

Closing the Phase Locked Loop

In order to effectively operate the motor, the hook waveforms presented in Chapter 2 must be phase-locked to the motor. This chapter discusses the difficulties of acquiring rotor position information via the BEMF and proposes an alternative phase detection strategy.

In the six-state drive scheme, phase information was obtained by using the undriven phase to observe the BEMF waveform. Unfortunately, the proposed sinusoidal current scheme drives all phases at all times, so it is impossible to make a direct measurement of the BEMF. It is possible that the driving waveforms could be modified to allow one phase to be floated. This would allow the BEMF to be detected in the same manner as before. This would also, however, increase the harmonic content of the current waveform, and possibly reduce the acoustic performance. Alternatively, position sensors could be placed on the motor to generate a position signal which can be used to lock the driving voltages to the motor. This however is prohibitively expensive. The approach which will be presented in this thesis makes use of the phase information embedded in the current waveform.

4.1 Inferring the BEMF Phase from the Current Phase

The current flowing through each phase winding is a function of both the driving voltage and the BEMF. Shifts in the BEMF will therefore have some effect on the phase shift of the current. It is possible to exploit this relationship to obtain BEMF phase information from the

current phase. First, however, the exact relationship between these two phases should be developed. In general, the current flowing through a phase of the motor is

$$\mathbf{I_A}(\omega) = \frac{\mathbf{V_A^*}(\omega) - \mathbf{V_{BEMF-A}^*}(\omega)}{L_M j\omega + R_M}. \tag{4.1}$$

The phase voltage is being driven with the hook waveform, so V_A^* is as defined in (2.9). Assuming that the BEMF is purely sinusoidal, the expression for I_A becomes

$$I_A = \frac{\frac{V_{MAG}}{\sqrt{3}}\sin\left(\omega t - \frac{\pi}{6} - \phi_M\right) - V_{BEMF}\sin\left(\omega t - \frac{\pi}{6} - \phi_M - \phi_{BEMF}\right)}{\sqrt{(L_M\omega)^2 + R_M^2}}, \tag{4.2}$$

with

$$\phi_M = \tan^{-1}\left(\frac{L_M}{R_M}\omega\right), \tag{4.3}$$

where

V_{BEMF} = magnitude of the BEMF,

ϕ_{BEMF} = phase shift of the BEMF,

ϕ_M = current shift due to motor impedance.

Equation (4.2) can be rewritten in terms of a single sine function. Using appropriate trigonometric identities to combine the two sine functions we find that

$$I_A = \frac{V_{MAG}}{\sqrt{3}} \cdot \frac{\sqrt{\left(\frac{1}{K}\right)^2 - 2\frac{1}{K}\cos(\phi_{BEMF}) + 1}}{\sqrt{(L_M\omega)^2 + (R_M)^2}} \cdot \sin\left(\omega t - \frac{\pi}{6} - \phi_M - \phi_B\right), \tag{4.4}$$

$$K = \frac{V_{MAG}}{\sqrt{3} \cdot V_{BEMF}}, \tag{4.5}$$

$$\phi_B = \sin^{-1}\left(\frac{-\sin(\phi_{BEMF})}{\sqrt{K^2 - 2K\cos(\phi_{BEMF}) + 1}}\right), \tag{4.6}$$

where

ϕ_B = current phase shift due to BEMF phase shift.

Equation (4.6) shows that ϕ_B has a functional dependence on both ϕ_{BEMF} and K. Ideally a more direct relationship is desired, but the dependence given by (4.6) is enough to draw some relationship between the current phase and BEMF phase. Insight can be gained by considering what happens to the phase shift for extreme values of K. When $V_{BEMF} >> V_{MAG}$, K = 0, and we would expect that the current phase shift has no dependence on the driving voltage. The phase shift of the current would therefore depend exclusively on ϕ_{BEMF}. When $\frac{1}{\sqrt{3}} V_{MAG} = V_{BEMF}$, K = 1, and equation (4.6) reduces to $\phi_B = -\frac{\pi}{2} + \frac{1}{2}\phi_{BEMF}$. When $V_{MAG} >> V_{BEMF}$, K approaches infinite, and there should be no dependence of the current phase shift on the BEMF phase shift. Figure 4-1 plots the relationship between ϕ_B and ϕ_{BEMF} for values of K = 1, 1.2, 2, and 10.

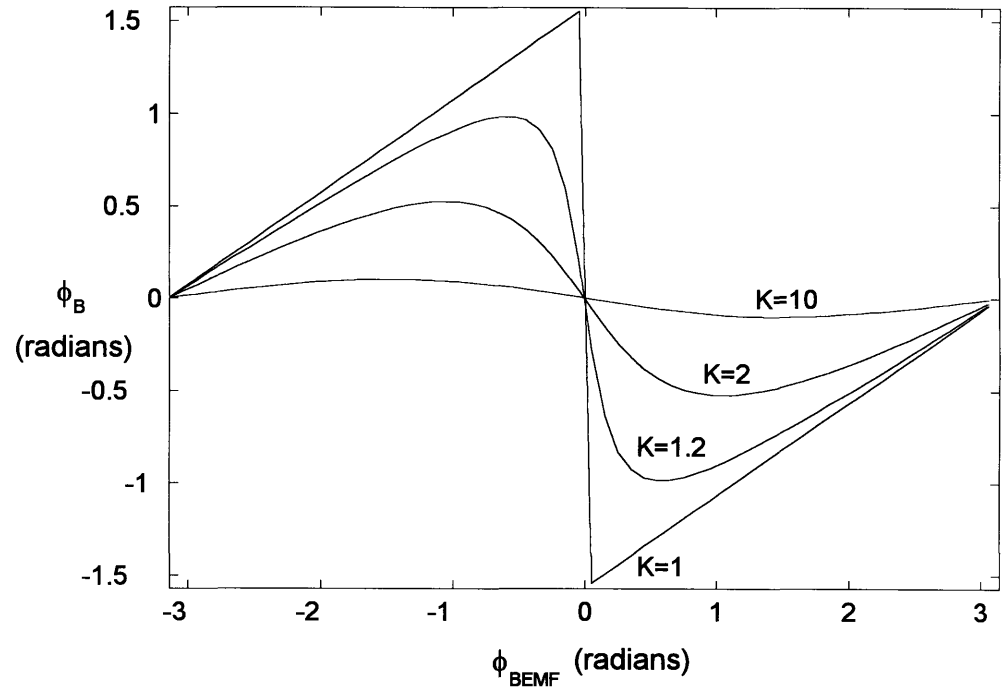

Figure 4-1: Current Phase vs. BEMF Phase

Figure 4-1 indicates some possible constraints on the operating conditions under which there is a satisfactory relationship between ϕ_B and ϕ_{BEMF}. For large values of K, there is little gain from ϕ_{BEMF} to ϕ_B, and it is difficult to determine the BEMF phase from the current phase. The motor is operating in this region when the motor is spinning at low speeds and V_{BEMF} is therefore low.

4.1.1 Selecting Proper Phase Delay

In order to maximize the torque delivered to the motor, the current waveform should be in phase with its corresponding BEMF waveform. In sinusoidal drive, the fundamental of the current lags the driving voltage. The amount of this delay depends on the motor parameters, as well as on the speed at which the motor is run. Table 4.1 lists the motor parameters,

operating speed, and resulting phase shift and BEMF magnitude of two motors which are likely to be driven by the sinusoidal drive.

Motor	L_M (mH)	R_M (Ω)	RPM	K_T (Vs)	P	ω_0 (rad/s)	ϕ_M (rad)	K (max.)
1	0.25	1.43	7177	2.00E-3	6	2,255	0.376	1.54
2	0.25	0.58	7177	2.12E-3	6	2,255	0.771	1.45

Motor parameters courtesy of Seagate Technologies

Table 4.1: Typical Motor Parameters

The value of K in Table 4.1 is given assuming V_{MAG} = 12V in order to operate the motor at full speed. On a 12V supply, this is the largest value of K possible. In order to bring the BEMF into phase with the current waveform, the BEMF phase shift, ϕ_{BEMF}, must equal ϕ_M plus ϕ_B. The resulting equation cannot be solved analytically. Although a solution, if one exists, can be found numerically, it is more beneficial to resort to graphical techniques. The conditions for optimal BEMF current phase shift can be expressed as

$$\phi_{BEMF} - \phi_M = \phi_B, \tag{4.7}$$

then the solution to the equation can easily be interpreted as the intersection of a load line, $\phi_{BEMF} - \phi_M$, with the graph of ϕ_B. Figure 4-2 repeats the graph of ϕ_B with a load line superimposed on top. The phase shift of motor 1 in Table 4.1 is used, and K is assumed to be 1.2.

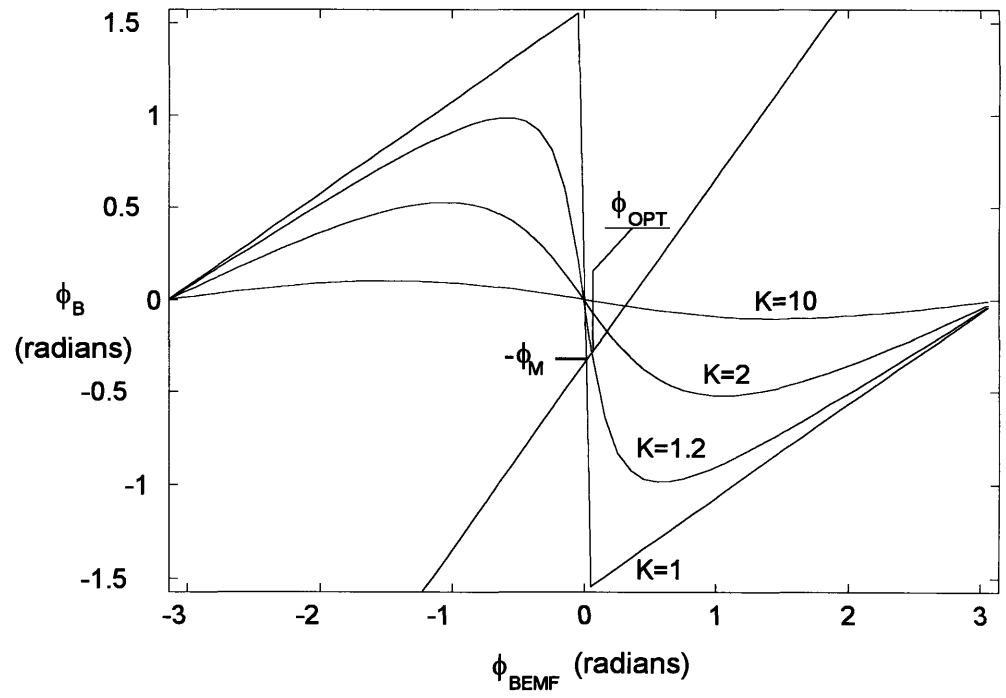

Figure 4-2: Current Phase vs. BEMF Phase with Optimal Phase Shift

Changes in motor impedance will result in sliding the load line vertically up and down the graph. The load line can be used to illustrate several important features of the relationship between BEMF phase and current phase. One of the most important conclusions is that the load line will always intersect ϕ_B, so there is always a solution corresponding to the optimal phase shift. Second, the optimal BEMF phase shift will always be less than the phase shift due to the motor. This is a result of the inverse relationship between ϕ_B and ϕ_{BEMF}. As the BEMF phase is delayed, the current phase is advanced.

For $\phi_M < \frac{\pi}{6}$, very little error is introduced if ϕ_B is linearized. From Appendix A, the slope of ϕ_B at the origin is

$$\frac{d\phi_B}{d\phi_{BEMF}} = \frac{-1}{|K-1|}. \tag{4.8}$$

ϕ_B can then be approximated as a simple line passing through the origin, and equation (4.7) can be rewritten as

$$\frac{-1}{|K-1|}\phi_{BEMF} = -\phi_M + \phi_{BEMF}, \tag{4.9}$$

and solved to give

$$\phi_{BEMF} \approx \phi_M \cdot \frac{K-1}{2}. \tag{4.10}$$

For the maximum values of K in Table 4.1, the optimal phase shift of the BEMF is at worst only 27% of the phase shift ϕ_M.

The dynamic behavior of the loop must next be examined to ensure that the relationship between ϕ_{BEMF} and ϕ_B will allow the phase-locked loop to work properly. Because the gain from ϕ_{BEMF} to ϕ_B is negative, the PLL will interpret a *delay* of the phase current as an *advance* of the BEMF waveform. The loop will therefore increase the delay of the BEMF. Conversely, the loop will interpret an *advance* of the phase current as a *delay* of the BEMF waveform, so the loop will reduce the delay of the BEMF. This action is shown visually in Figure 4-3 by drawing arrows indicating the direction of motion along the ϕ_B curve.

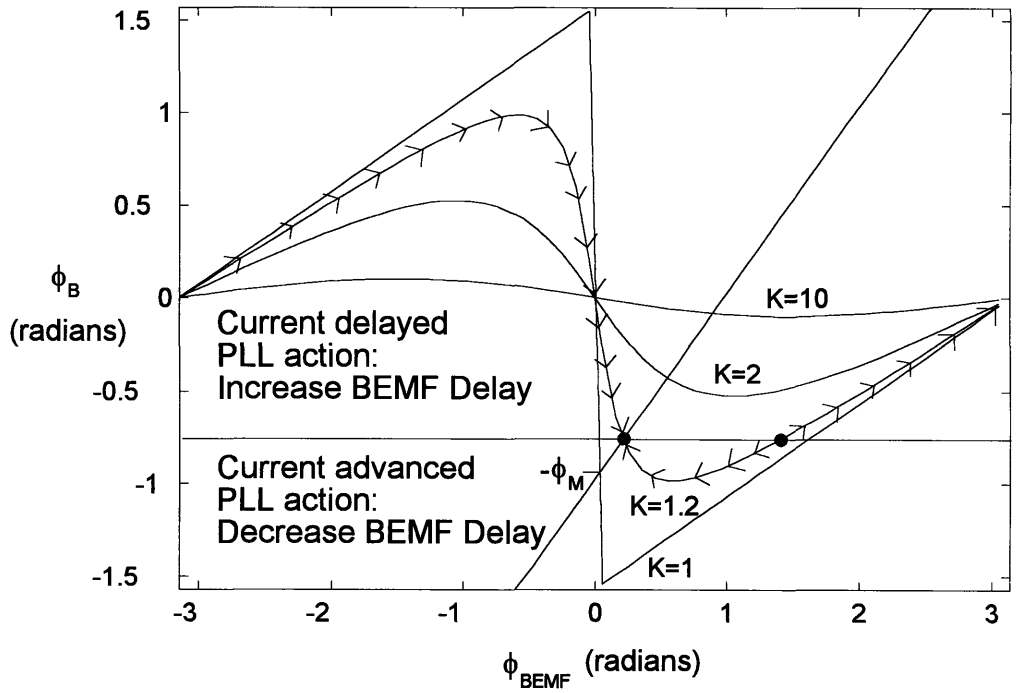

Figure 4-3: Phase Response of PLL

Figure 4-3 illustrates that ϕ_{BEMF} cannot be delayed too much past ϕ_{OPT} or the BEMF phase will enter an operating region in which the PLL forces the BEMF phase to move in the wrong direction. In this region, the loop increases the delay of the BEMF when in fact it should be decreasing it. Based on the typical values of ϕ_M and K in Table 4.1, this should not occur under normal operation.

If the operating point does happen to lie very close to a peak of one of the curves in Figure 4-3, then the likelihood of skipping a cycle increases. In fact, as the operating point approaches the peak of ϕ_B, the operating range of the loop goes to zero. If this situation should ever arise, the loop can be made operational by sacrificing efficiency for stability. The operating point can be moved towards the origin along the curve of ϕ_B, and the operational range of the loop will increase. This will, however, reduce the torque delivered to the motor because the BEMF and current will no longer be in phase. If the operating point is pushed all the way back to the origin, then the maximum loop stability will be attained, but the motor efficiency will be considerably lowered. When the operating point is at the origin, $\phi_B = 0$, so

the current lags the BEMF waveform by ϕ_M radians. Therefore the applied torque will be scaled by $\cos(\phi_M)$.

4.2 Detecting the Phase Current

The preceding section established that there is an exploitable relationship between the current phase and the BEMF phase. It is now necessary to establish a reliable method of measuring the current phase information. Three possible methods of current detection will be explored. The first two were originally proposed by Bert White of Silicon Systems, Inc., now with Texas Instruments. In the first method, three sense resistors are placed in series with the phase windings in order to generate voltages proportional to the phase currents. In the second method, the on-resistance of the power MOSFETs is used to measure the polarity of the current. In the third scheme, which is developed in this paper, the single current sense resistor is used to make readings of the phase current.

4.2.1 Three Sense Resistor Method

This method is quite straightforward and uses three sense resistors placed in series with the motor phases to read the current. The voltage generated across each resistor then gives an exact representation of the current flowing through the phase. From a signal generation standpoint, this is the most ideal way of obtaining the current waveform. Unfortunately economic considerations make this an impractical option. Hard disk drive manufacturers are unwilling to add cost to their products by adding additional components. In addition, the resistors add additional power losses to the system. Hard drive manufacturers are continually seeking to increase the efficiency of their motors, so they are reluctant to adopt a solution which requires putting resistance in series with the motor windings.

4.2.2 MOSFET On-Resistance Method

In response to the need to remove the phase current sense resistors from the current detection scheme, Bert White proposed that the voltage drop across the power MOSFETs could be used to detect the phase current. Essentially, the three sense resistors are replaced by the on-resistance of the six power MOSFETs. The use of MOSFETs instead of discreet resistors requires the current detection scheme to be slightly more refined, because the current is being switched between the high-side and low-side drivers. The current detection scheme must therefore be sophisticated enough to observe the appropriate transistor at the appropriate time. This is easily done because the same logic that controls the power drivers can switch the comparator to the appropriate transistor.

If the on-resistance, $R_{DS(ON)}$, of the FETs is large enough, then a detection scheme built around the MOSFET drivers will work. Unfortunately, the trend in the hard drive industry has been to use FETs with smaller and smaller values of $R_{DS(ON)}$. At the time of this thesis work, National Semiconductor was already producing the NDS8936, a MOSFET power driver with less than 50 mΩ of on-resistance. If the amplitude of the current flowing through the motor at full speed is only 300 mA, then the amplitude of the available voltage signal across the FET is only 15 mV. This number is much too small to accurately detect the zero-crossing of the current, especially when comparator offsets may be on the order of 10 mV. The phase offset, ϕ_{OS}, caused by the comparator offset is equal to

$$\phi_{OS} = \sin^{-1}\left(\frac{V_{OS}}{I_{PEAK} \cdot R_{DS(ON)}}\right). \tag{4.11}$$

The phase offset resulting from the numbers listed above is 0.7 radians, which is entirely unacceptable. While the MOSFET current technique would be able to work in theory, in

practice there is not enough available signal across the MOSFET to accurately determine the zero-crossing.

4.2.3 Single Sense Resistor Method

The first current sense method presented in this thesis depended on the addition of three phase-resistors. This solution allowed exact measurement of the phase current, but was discarded for economic and power reasons. The second current detection scheme took advantage of resistive paths already present in each phase of the motor. This solution, too, was abandoned because the available voltage signal is not large enough to measure accurately. The third and final current detection technique takes advantage of the only other resistive path available for signal detection in the motor-the current sense resistor.

The current sense resistor is used during the motor start-up routine to regulate the amount of current which flows through the motor. It is placed between ground and the source of the pull-down transistors of all three phases. The sense resistor provides a dependable resistance across which the phase currents of the motor can be measured, but unfortunately, the current flowing through the sense resistor changes from one phase to another depending on the state of the power drivers. If V_A is high, and V_B and V_C both happen to be low, then the current flowing through the sense resistor equals the current of phase A. A list of all possible switching states, and the corresponding value of I_{SENSE} is presented in Table 4.2.

V_A	V_B	V_C	I_{SENSE}
0	0	0	0
0	0	V_{SUP}	I_C
0	V_{SUP}	0	I_B
0	V_{SUP}	V_{SUP}	$-I_A$
V_{SUP}	0	0	I_A
V_{SUP}	0	V_{SUP}	$-I_B$
V_{SUP}	V_{SUP}	0	$-I_C$
V_{SUP}	V_{SUP}	V_{SUP}	0

Table 4.2: I_{SENSE} Current as a Function of Switching State

Table 4.2 shows that I_{SENSE} at any point in time can be expressed as the current flowing through only one phase of the motor. The value of I_{SENSE} depends on the state of the driving switches, and therefore on the PWM waveforms driving the motor. I_{SENSE} can be written as the summation of each phase current multiplied by a corresponding masking waveform. The masking waveforms equal one when a particular current is flowing through R_{SENSE}, and equal zero when that current is not flowing through R_{SENSE}. I_{SENSE} can then be easily written as

$$I_{SENSE} = I_A \cdot \left(M_A^P - M_A^N\right) + I_B \cdot \left(M_B^P - M_B^N\right) + I_C \cdot \left(M_C^P - M_C^N\right) \tag{4.11}$$

where

M_A^P = mask for I_A,

M_A^N = mask for $-I_A$,

M_B^P = mask for I_B,

M_B^N = mask for $-I_B$,

M_C^P = mask for I_C,

M_C^N = mask for $-I_C$.

The mask waveforms are easily generated from the normalized phase voltages, $\overline{V}_A$, $\overline{V}_B$, and $\overline{V}_C$. The normalized phase voltages are the phase voltages divided by the power supply

voltage, V_{SUP}. The mask for I_A should equal 1 one when $\overline{V}_A = 1$, $\overline{V}_B = 0$, and $\overline{V}_C = 0$. The mask for $-I_A$ should equal one when $\overline{V}_A = 0$, $\overline{V}_B = 1$, and $\overline{V}_C = 1$. The expressions for masks M_A^P and M_A^N can then be defined as

$$M_A^P = \overline{V}_A \cdot (1 - \overline{V}_B) \cdot (1 - \overline{V}_C), \tag{4.13}$$

$$M_A^N = (1 - \overline{V}_A) \cdot \overline{V}_B \cdot \overline{V}_C. \tag{4.14}$$

It is important to realize that because the duty cycles of the driving waveforms are a function of V_{MAG}, the times when M_A^P equals 1 also depend on V_{MAG}. The relation between V_{MAG} and M_A^P is not a straightforward relationship, so it is most easily explained pictorially. Because the available viewing times of the waveform are dependent on the switching times of the PWM signals, it is expected that there is a difference between an in-phase PWM switching scheme and an out-of-phase switching scheme. Scatter plots of the conditions under which $M_A^P = 1$ and $M_A^N = 1$ are presented in Figures 4-4 and 4-5. M_A^P is plotted in the interval 0 to $\frac{4\pi}{3}$, and M_A^N is plotted between $\frac{4\pi}{3}$ and 2π. There is no overlap of these functions between the conditions for both are mutually exclusive.

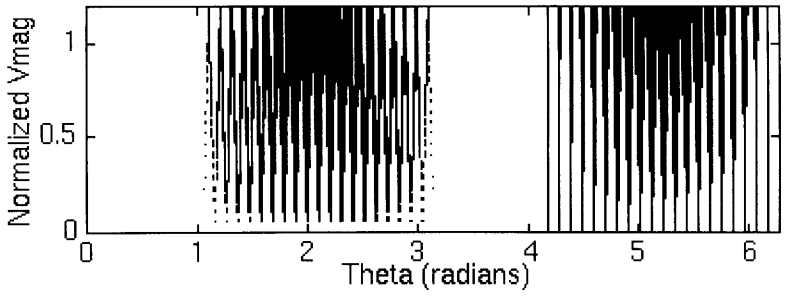

Figure 4-4: Conditions Under Which I_A and $-I_A$ Flow Through R_{SENSE} [In-Phase PWM]

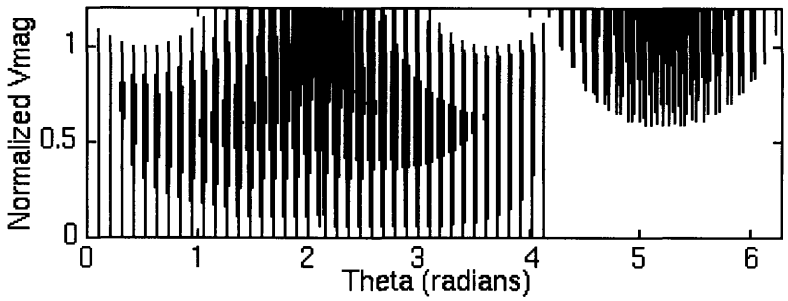

Figure 4-5: Conditions Under Which I_A and $-I_A$ Flow Through R_{SENSE} [Out-Of-Phase PWM]

Both graphs show a notable dependence on V_{MAG}. As V_{MAG} decreases, so does the amount of time I_A spends flowing through R_{SENSE}. This makes sense because one of the conditions for I_A equaling I_{SENSE} is that phase A be held high. As V_{MAG} decreases, the time that phase A is pulled high will also decrease. The times when I_A can most often be measured on R_{SENSE} is centered around $\frac{2\pi}{3}$. This makes sense because the conditions for viewing I_A are that V_A must be high, and V_B and V_C low. Referring back to the waveforms in Figure 2-4, the unmodulated V_A is higher than V_B and V_C between $\frac{\pi}{3}$ and π radians. During this period then, it is expected that the I_{SENSE} current would typically be the current in phase A.

The two switching schemes (in-phase vs. out-of-phase) have different distributions of conditions under which I_A is flowing through R_{SENSE}. The in-phase switching scheme has a wider range of V_{MAG} values over which $-I_A$ can be observed. The out-of-phase switching scheme has a wider range of angles over which I_A can be sensed. This difference will have consequences later when signal recovery is discussed.

It is therefore possible, during specific time intervals of the driving cycle, to detect predominantly one phase on the sense resistor. During these intervals, if the current from only one phase is observed, then it will be possible to detect current phase, and close the PLL.

4.2.4 Extracting Current Information-Track and Hold

During any cycle of the PWM, the I_{SENSE} current may change between any of four possible values. In order to effectively recover the correct phase current during a particular portion of the driving cycle, our system must ignore the other phase currents which are essentially getting multiplexed through the sense resistor. A track and hold circuit will be able to mostly recover the original waveform. If the driving transistor are ever in a state when I_A is observable across the sense resistor, the sense resistor voltage will be tracked. If the switches ever enter a state where I_A is no longer observable, then the circuit will stop tracking and will hold the last valid tracking voltage. If the value I_A does not change considerably over the hold time then the track and hold will return I_A with only a slight error. The output of the track and hold can then be used to generate phase error.

4.3 Generating Phase Error from Current Phase

Because it is only possible to sense I_A across the sense resistor during specific ranges of the driving cycle, phase detection can only be performed on certain parts of the current waveform. From Figures 4-4 and 4-5 it is clear that the best location to sample the current in phase A is in the interval from $\frac{\pi}{3}$ to π. Using equation (4.10), the optimal phase shift for motor 1 in Table 4.1 is approximately 0.1 radians. The zero crossings of the current will therefore not be visible, so phase detection cannot be based on the detection of zero-crossings.

4.4 Generating Phase Error with Peak Detection

Because the peak of the current waveform is located near optimal viewing region, a peak detection strategy can be used to obtain the phase information of the current. Suppose that we wanted to center the peak of a sinusoidal waveform in a window of width Θ radians. From

time $t = -\frac{\Theta}{2\omega_0}$ to $t = 0$, the waveform is integrated with a negative polarity. From time $t = 0$ to $t = \frac{\Theta}{2\omega_0}$, the waveform is integrated with positive polarity. If the sinusoid is exactly centered in the window then the sum of the two integrations is zero. If, however, there is some phase error, ϕ, then the net result of the integration will be some value which is related to the phase shift. Figure 4-6 shows a diagram of the method used to obtain the phase error information.

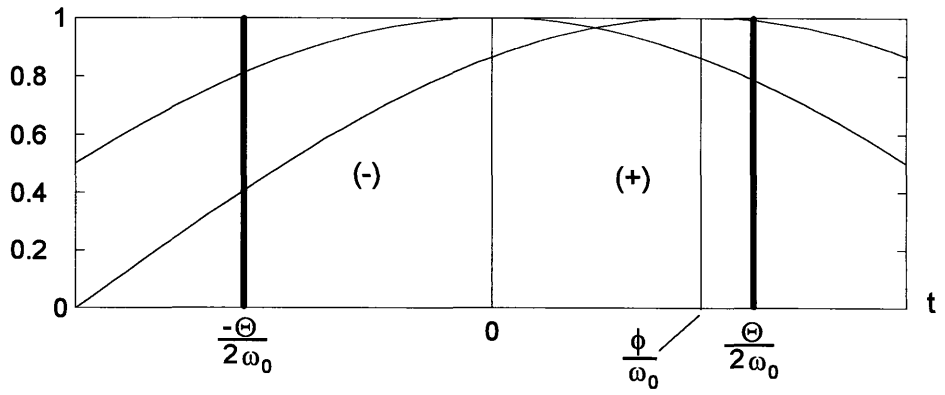

Figure 4-6: Integration Method Used to Generate Phase Error

The response of the proposed phase detector is most easily analyzed by examining its partial responses to the input current waveform. The input to the phase detector is the output from the track and hold. The track hold recovers as much of the current signal as possible, but its output will never equal the actual phase current. The output of the track and hold can be broken up into the actual phase current plus some error I_{error} which is the result times when IA is not flowing through the sense resistor.

$$I_{TH} = I_A + I_{error}, \tag{4.15}$$

where

I_{TH} = output of track and hold,

I_A = actual phase current.

I_A in general has some harmonic content, so the input into the phase detector can be further broken up into

$$I_{TH} = I_{error} + \sum_{n=0}^{\infty} I_n \cos(n\omega_0 t - \alpha_n). \tag{4.16}$$

4.4.1 Errors Due to Phase Current Harmonics

The proposed technique for phase detection was outlined in Figure 4-6. Θ is the width of the observation window in radians, and ϕ is the shift of the fundamental of the waveform relative to the observation window. Positive values of ϕ indicate that the peak of the fundamental of the current waveform is delayed with respect to the center of the observation window.

The phase error due to any particular harmonic of the current is given by

$$PE_n(\phi) = -\int_{-\frac{\Theta}{2\omega_0}}^{0} I_n \cos(n\omega_0 t - (\phi + \alpha_n))dt + \int_{0}^{\frac{\Theta}{2\omega_0}} I_n \cos(n\omega_0 t - (\phi + \alpha_n))dt. \tag{4.17}$$

where

α_n = phase shift of nth harmonic,

I_n = amplitude of nth harmonic,

and it has been assumed that $\alpha_1 = 0$.

After carrying out the integration of equation (4.17) and combining the terms, the expression for $PE_n(\phi)$ becomes

$$PE_n(\phi) = \frac{2 \cdot I_n}{n \cdot \omega_0}\left(1 - \cos\left(n\tfrac{\Theta}{2}\right)\right) \cdot \left(\cos\left(n\tfrac{\pi}{2}\right)\left(\cos\alpha_n \cos\phi - \sin\alpha_n \sin\phi\right) + \sin\left(n\tfrac{\pi}{2}\right)\left(\sin\alpha_n \cos\phi + \cos\alpha_n \sin\phi\right)\right) \tag{4.18}$$

The total response of the phase detector is simply the sum of the responses due to the individual harmonics. The total phase error can be written as

$$PE(\phi) = PE_1(\phi) + \sum_{n=2}^{\infty} PE_n(\phi), \tag{4.19}$$

where it has been noted that $PE_0(\phi) = 0$.

The summation in (4.19) is functionally dependent only on $\cos(\phi)$ and $\sin(\phi)$. If the harmonic content of I_A is known, then the summation in (4.15) will reduce to $\cos(\phi)$ times some coefficient plus $\sin(\phi)$ times another coefficient. The coefficients of the sine and cosine functions reflect the errors introduced into the phase detector by the harmonics of I_A. The total phase error can therefore be written as

$$PE(\phi) = \frac{2I_1}{\omega_0}\left(e_{g0} \sin\phi + e_{gh} \sin\phi + e_{osh} \cos\phi\right), \tag{4.20}$$

where e_{g0}, ideal gain of phase detector, is given by

$$e_{g0} = 1 - \cos\left(\tfrac{\Theta}{2}\right), \tag{4.21}$$

e_{gh}, the gain error due to harmonic content, is given by

$$e_{gh} = \sum_{n=2}^{\infty} \frac{I_n}{nI_1}\left(1 - \cos\left(n\tfrac{\Theta}{2}\right)\right)\left(\sin\left(n\tfrac{\pi}{2}\right)\cos(\alpha_n) - \cos\left(n\tfrac{\pi}{2}\right)\sin(\alpha_n)\right), \tag{4.22}$$

and e_{osh}, the offset error due to harmonic content is given by

$$e_{osh} = \sum_{n=2}^{\infty} \frac{I_n}{nI_1}\left(1-\cos\left(n\tfrac{\Theta}{2}\right)\right)\left(\sin\left(n\tfrac{\pi}{2}\right)\sin(\alpha_n)+\cos\left(n\tfrac{\pi}{2}\right)\cos(\alpha_n)\right). \tag{4.23}$$

The naming convention used in equations (4.19) through (4.23) is based on the role of the coefficients when equation (4.20) is linearized.

$$PE(\phi) \approx \frac{2I_1}{\omega_0}\left(e_{g0}\phi + e_{gh}\cdot\phi + e_{osh}\right) \tag{4.24}$$

4.4.2 Errors Due to Track and Hold Circuitry

The preceding development assumed that the only errors in the phase detector were due to the harmonics of the current. In this section the error introduced due to the track and hold will be analyzed. To make the analysis of this error easier, the phase current will be assumed to contain no harmonics. This makes the mathematical derivation more straightforward and allows us to find an intuitively understandable answer.

As discussed in Section 4.2.3, I_A can only be viewed at the times given by the mask waveform M_A^P. M_A^P is a function of V_{MAG} and $\omega_0 t$. so the phase error due to the action of track and hold will have a similar dependence.

The integration of I_{error} will occur in a window of Θ radians. Where this window is located with respect to the masking waveform depends on the optimal phase shift. If the current is to be kept in phase with the BEMF, then the center of the integrating window must be delayed by ϕ_{OPT}. This means that when the PLL centers the peak of the current in the window, the peak will in fact be delayed by the optimal phase shift. Shifting the integrating window will also effect the tracking times because now the integration occurs over a different

range of M_A^P. The tracking times, and therefore the tracking errors will be determined by V_{MAG}, ϕ_{OPT}, and the width of the window.

For a given V_{MAG}, ϕ_{OPT}, and Θ, there is a completely determinable set of times indicating whether or not the track and hold is tracking or holding. Only at the times when the track and hold is holding will I_{error} be non-zero. Calculating these errors is a task best left to numerical tools such as Matlab. In order to give some intuition, however, the output of the phase detector due to one holding segment is examined below.

4.4.2.1 Error Due to Holding for One Segment

Figure 4-7 shows the form of I_{error} centered in some tracking window of width Θ radians. Each error due to a holding segment can be identified by a location time, t_k, and a holding duration, ΔT_k. Each t_k and ΔT_k correspond to an interval over which the tracking error is non-zero. The center of the tracking window has been shifted to t = 0 in order to make the setup of the analysis more symmetric.

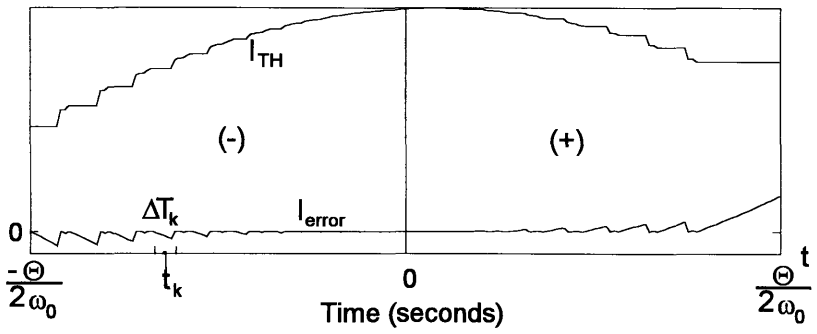

Figure 4-7: Error in Track and Hold Output

The output of the phase detector to one of these regions of error is

$$PE_k(\phi) = \left[\Delta T_k \cdot I_1 \cos\left(\omega_0\left(t_k - \frac{\Delta T_k}{2}\right) - \phi\right) - \int_{t_k - \frac{\Delta T_k}{2}}^{t_k + \frac{\Delta T_k}{2}} I_1 \cos(\omega_0 t - \phi) dt \right] \mathrm{sgn}(t_k), \qquad (4.25)$$

where

ΔT_k = width of holding segment,

t_k = midpoint of holding segment.

The function $\mathrm{sgn}(t_k)$ takes care of the fact that if the holding segment is in the left half of the integration window, the integration should be carried out with a negative sign. After carrying out the integration in (4.25) and rearranging the terms, the expression for the phase error becomes

$$\begin{aligned} PE_k(\phi) = {} & I_1\left[\left(\Delta T_k \cos\left(\frac{\omega_0 \Delta T_k}{2}\right) - \frac{2}{\omega_0}\sin\left(\frac{\omega_0 \Delta T_k}{2}\right)\right)\cos(\omega_0 t_k) + \Delta T_k \sin\left(\frac{\omega_0 \Delta T_k}{2}\right)\sin(\omega_0 t_k)\right]\mathrm{sgn}(t_k)\cos\phi \\ & + I_1\left[\left(\Delta T_k \cos\left(\frac{\omega_0 \Delta T_k}{2}\right) - \frac{2}{\omega_0}\sin\left(\frac{\omega_0 \Delta T_k}{2}\right)\right)\sin(\omega_0 t_k) - \Delta T_k \sin\left(\frac{\omega_0 \Delta T_k}{2}\right)\cos(\omega_0 t_k)\right]\mathrm{sgn}(t_k)\sin\phi \end{aligned} \qquad (4.26)$$

Equation (4.26) can be further simplified if the approximation is made that $\frac{\omega_0 \Delta T_k}{2} << 2\pi$, that is if the tracking period is small relative to the period of the current waveform. The PWM frequency is 60 times the electrical frequency, so the time holding times of the track hold will be less than $\frac{2\pi}{60\omega_0}$, and we can make the above assumption to reduce (4.26) to

$$PE_k(\phi) \approx \frac{2I_1}{\omega_0}\left[\left(\frac{\omega_0 \Delta T_k}{2}\right)^2 \sin(\omega_0 |t_k|)\right]\cos\phi - \frac{2I_1}{\omega_0}\left[\left(\frac{\omega_0 \Delta T_k}{2}\right)^2 \cos(\omega_0 t_k)\right]\mathrm{sgn}(t_k)\sin\phi. \qquad (4.27)$$

Some important results are expressed in (4.27). First, because the coefficient of $\cos(\phi)$ is proportional to $\sin(\omega_0 |t_k|)$, integration of errors in the left half of the integration window will never cancel with those errors on the right. Instead they will reinforce each other.

Conversely, for the coefficients of sin(ϕ), errors from the first half of the integration will tend to cancel with those accumulated during the second half. If the window of integration is not delayed by ϕ_{OPT}, then the tracking and holding times will be symmetric for both the positive and negative regions of integration. The errors will therefore cancel exactly and the coefficient of sin(ϕ) will be zero.

As in the case with the harmonic errors, it is helpful to express the total phase error due to the track and hold by summing all of the errors together and extracting the coefficient of sine and cosine. The gain error, e_{gth}, and offset error, e_{osth}, for the track and hold are given by

$$e_{gth} \approx -\sum_{\text{all k}} \left(\frac{\omega_0 \Delta T_k}{2} \right)^2 \cos(\omega_0 t_k) \operatorname{sgn}(t_k), \tag{4.28}$$

$$e_{osth} \approx \sum_{\text{all k}} \left(\frac{\omega_0 \Delta T_k}{2} \right)^2 \sin(\omega_0 |t_k|), \tag{4.29}$$

so the output of the phase detector due to the track and hold error is

$$PE(\phi) = \frac{2I_1}{\omega_0} \left(e_{gth} \cos(\phi) + e_{osth} \right). \tag{4.30}$$

The gain- and offset-errors due to the track and hold can be calculated numerically using Matlab. Θ was set equal to $\frac{\pi}{6}$. The plots are all normalized by e_{g0}, and plotted as a function of ϕ_{OPT} for $\overline{V}_{MAG}$ = 0.6, 0.8, 1.0 and 1.2. $\overline{V}_{MAG}$ is V_{MAG} normalized by the power supply voltage, V_{SUP}. A value of 1.2 for $\overline{V}_{MAG}$ indicates that the magnitude of V_{MAG} was 1.2 times higher than the triangle waveform which was compared against it.

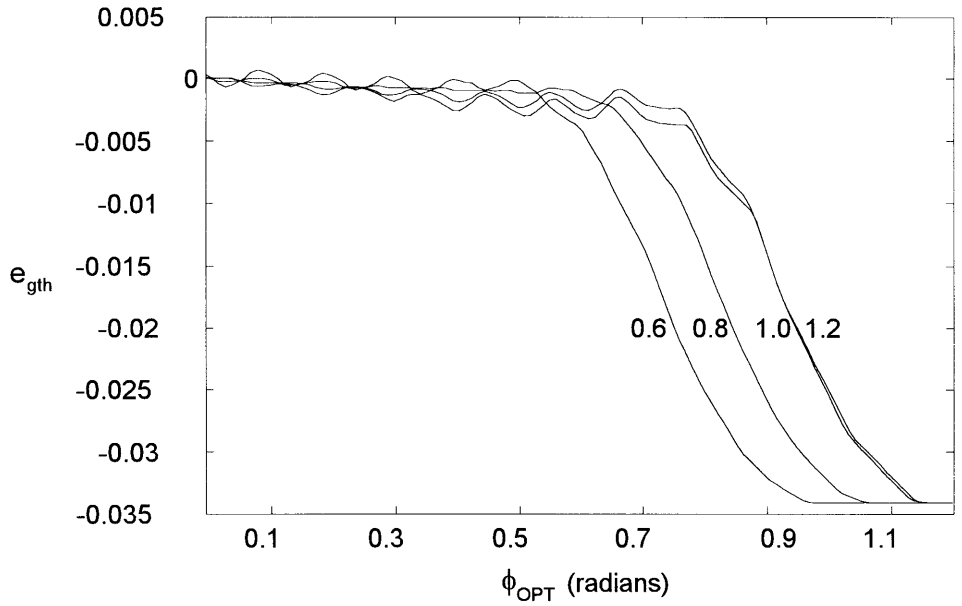

Figure 4-8: Track and Hold Gain-Error for In-Phase PWM.

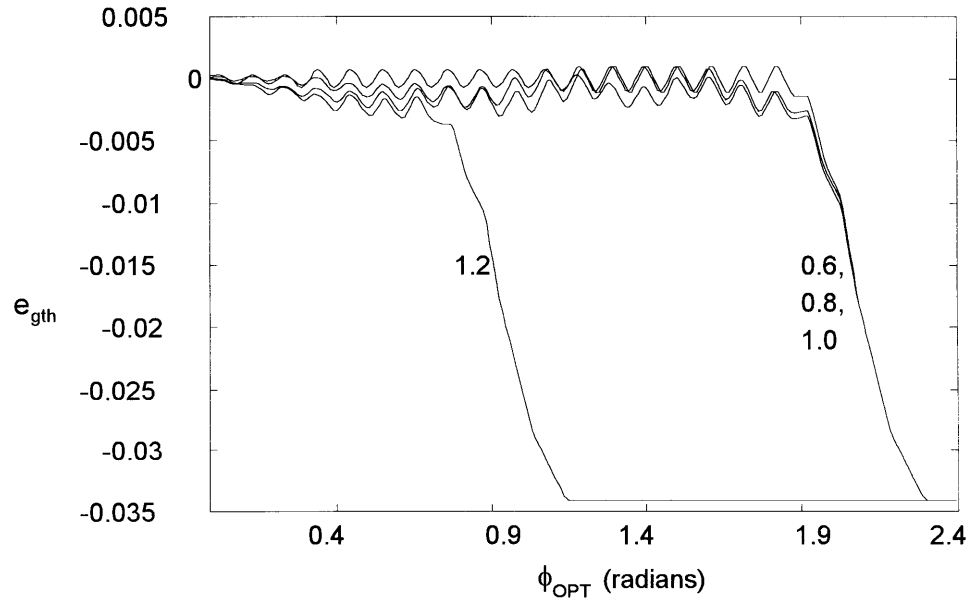

Figure 4-9: Track and Hold Gain-Error for Out-Of-Phase PWM.

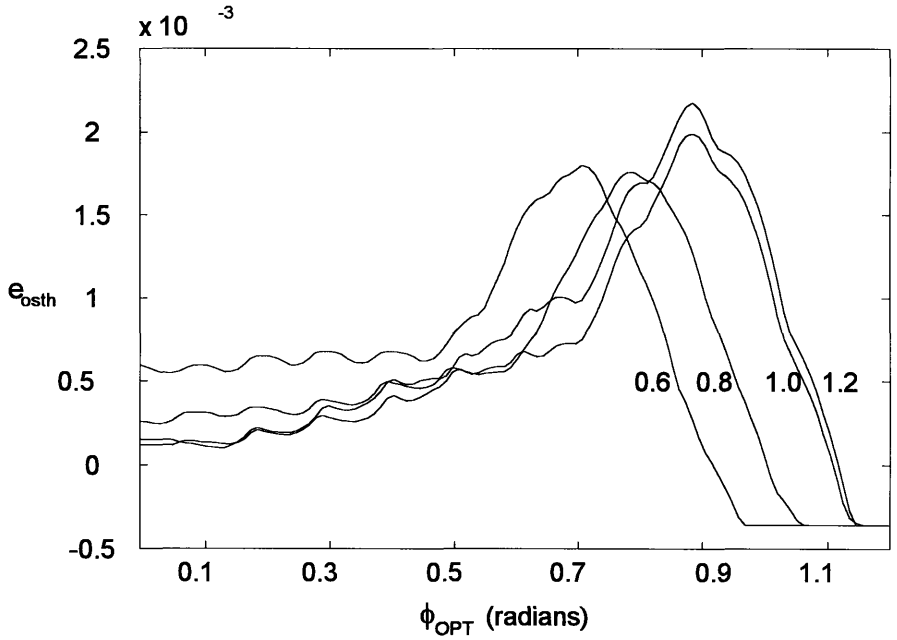

Figure 4-10: Track and Hold Offset-Error for In-Phase PWM

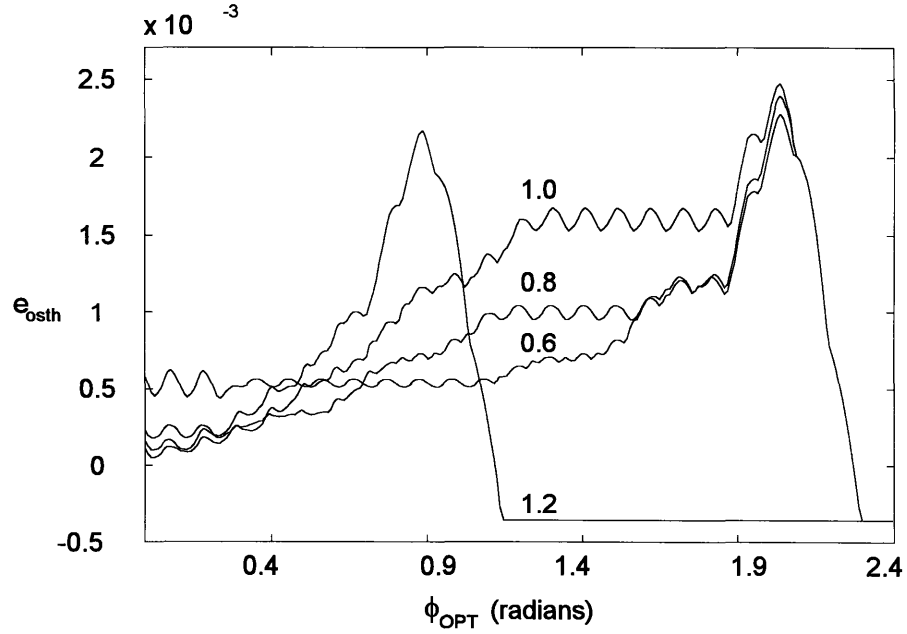

Figure 4-11: Track and Hold Offset-Error for Out-Of-Phase PWM.

The final expression for the output of the phase detector can finally be written as

$$PE(\phi) = \frac{2I_1}{\omega_0}\left[\left(e_{g0} + e_{gh} + e_{gth}\right)\sin\phi + \left(e_{osh} + e_{osth}\right)\cos\phi\right]. \tag{4.31}$$

4.4.3 Phase Error Due to Gain- and Offset-Error

Ultimately, what is important is not the gain- and offset-errors of the of the phase detector, but how this translates into our ability to accurately lock the driving voltages to the motor. If the phase-locked loop drives the phase error, PE(ϕ), to zero, then, using a first order approximation to the phase error, the phase offset, ϕ_{os}, is

$$\phi_{os} = -\frac{e_{osh} + e_{osth}}{e_{g0} + e_{gh} + e_{gth}}. \tag{4.32}$$

Ignoring the effects of current harmonics, the phase offset as a function of ϕ_{OPT} is plotted in Figures 4-12 and 4-13.

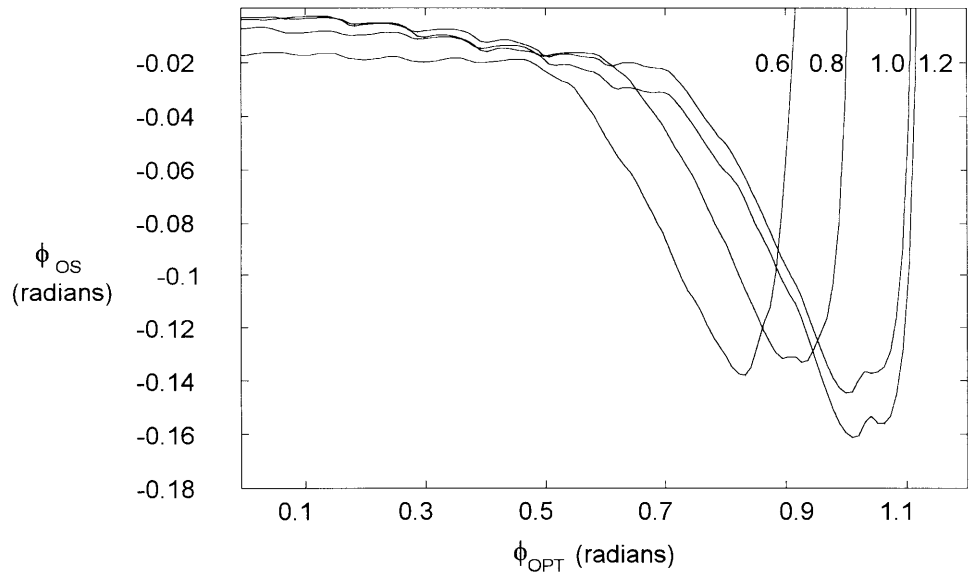

Figure 4-12: Phase Offset-Error [In-Phase PWM]

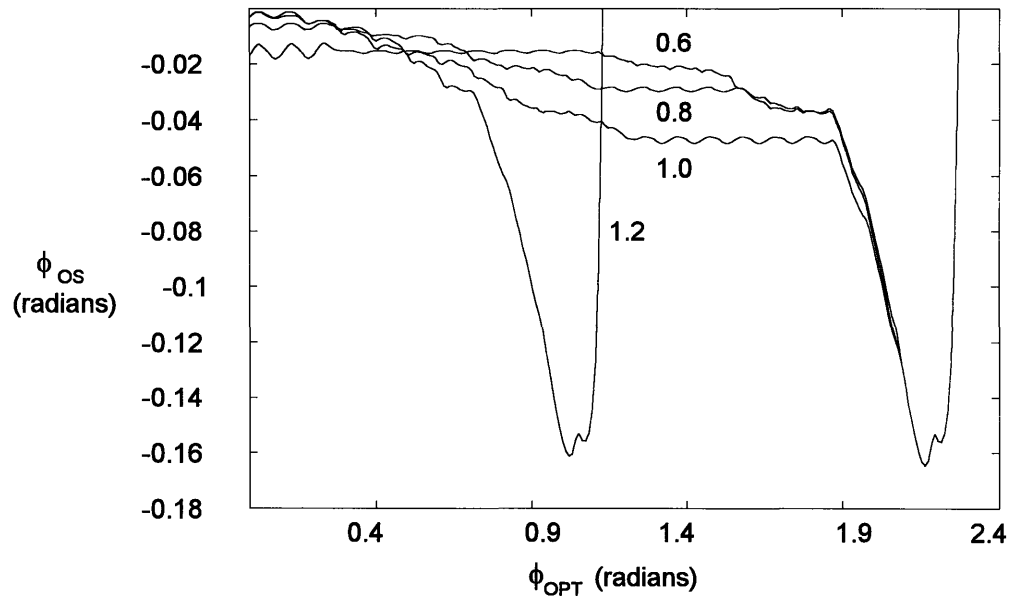

Figure 4-13: Phase Offset-Error [Out-Of-Phase PWM]

Figures 4-12 and 4-13 illustrate a key difference between the in-phase PWM and the out-of-phase PWM. For in-phase PWM, the offset error sharply increases at 0.7 radians. For out-of-phase PWM, the offset error do not start increasing until 1.9 radians. We are therefore motivated to select the out-of-phase PWM scheme because of the greater range of optimal phase shifts over which the offset error is approximately zero. It should also be noted that for larger windows, the offsets will be worse, because the integration window will cover a range of time during I_A is not observable on the sense resistor.

Chapter 5

Testing the System

The sinusoidal drive presented in this paper is much more complex than the conventional six-state drive. In order to test the practicality of the system, as well as the acoustic performance, a test board was built. The conceptual layout of the test board, the testing setup, and the testing results are presented in this chapter.

5.1 Building a Test Board

To conduct a fair test of the sinusoidal drive, a test board was built which can operate as both a six-state drive and a sinusoidal drive. Six-state drive functionality was also included because it is intended that the drive will be started in six-state mode and then switched into sinusoidal mode when the disk drive reaches full speed. The motor will be started in six-state mode due to the fragile nature of the sinusoidal phase detector.

The implementation of the system is conceptually very similar to the six-state drive scheme. A state machine controls the manner in which the driving phases are driven. The motor phase is detected with an appropriate phase detector, and the phase error is used to lock the phase of the driving voltage to the BEMF. As before, a current control loop controls the level of the driving voltage. A top-level system diagram is shown in Figure 5-1.

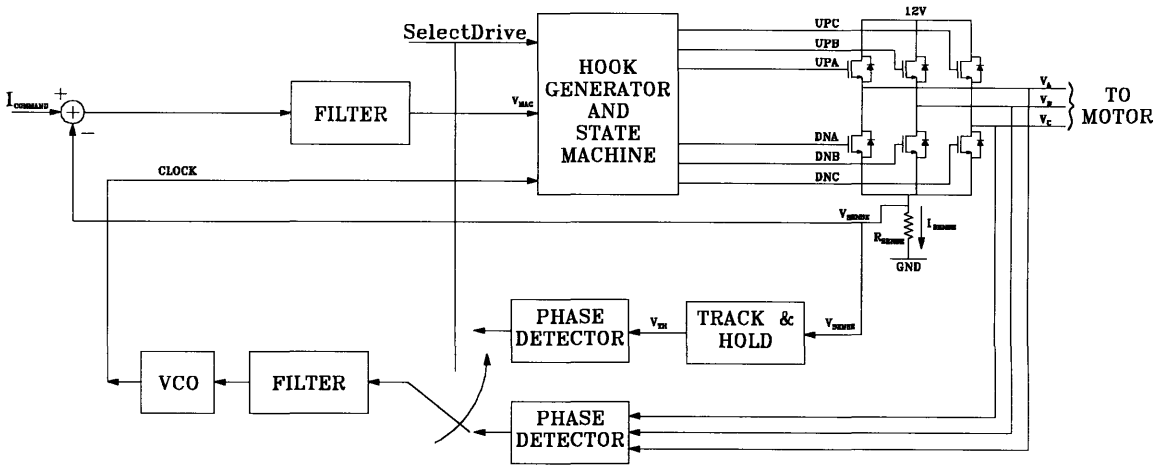

Figure 5-1: Top-Level System Diagram of Test Board

In order to implement the hook waveform, the state machine must drive a different average voltage on the phases for every cycle of the PWM. When operating the PWM at 60 times the electrical frequency, the state machine must have a defined output for 60 states, not just 6 as with six-state. This raises the level of complexity of the state machine, but not prohibitively.

In every state, a PWM signal must be generated which has the appropriate duty cycle. As was discussed in Chapter 3, the PWM signal can be generated by comparing a voltage waveform with a triangle waveform. For each PWM cycle, the state machine can command an appropriate output from a DAC. The DAC is referenced to V_{MAG}, so the output of the DAC scales with V_{MAG}. Because only two phases are modulated at once, only two DACs are needed. If the hook waveforms are broken up into segments of $\frac{2\pi}{3}$ radians, then during each segment one phase is held low, another phase is being driven with the positive-going portion of the hook (uphook), and the third drive is being driven with the negative-going portion of the hook (downhook). Breaking the waveforms up in this manner provides a simple way of obtaining the out-of-phase characteristics which are desired to increase the range of possible phase shifts. The uphook waveforms are compared against one triangle wave, and the

downhook waveforms compared against the out-of-phase triangle wave. The logic of the state machine then directs the correct modulation to the appropriate phase.

The test board was built using the facilities at Texas Instruments, in Dallas, TX. The primary logic of the design was built into a Field Programmable Gate Array (FPGA). A great deal of credit for the system must be given to Bert White, who designed the original three sense resistor sinusoidal drive (Section 4.2.1)

The window of integration employed in the phase detector was $\frac{2\pi}{3}$ radians. For $\frac{2\pi}{3}$ radians the current in phase A was tracked off of the sense resistor. For the next $\frac{2\pi}{3}$ radians, the current in phase B was used as the input to the phase detector, and for the final $\frac{2\pi}{3}$ radians, the current in phase C was used.

5.2 Acoustic Testing Procedure

The hard disk drive array was clamped in a rigid manifold to the top of a table. A microphone was then placed near the hard drive. The signal from the microphone was then passed through a spectrum analyzer and the frequency content measured.

Two different motors were tested in this experiment. One motor was manufactured by Seagate Technology, and the second was manufactured by Nidec. Both motors were operated at 7200 RPM and had 6 poles. The electrical frequency of both motors is therefore 2262 rad/sec or 360 Hz. The testing was conducted in an open air environment at Seagate Technologies.

The testing was initiated by first starting the motor and bringing it up to full speed in six-state mode. After taking measurements in six-state mode, the drive system was then changed to sinusoidal mode. Any transients introduced by changing the drive scheme were allowed to settle out and then acoustic measurements were made again.

5.3 Results of Testing

The results of the acoustic testing are presented in this section. The graphs are all courtesy of John Baker at Seagate Technologies. The graphs are all referenced to previous acoustic measurements of the motors when driven with an older six-state drive. Their standard control system implemented both a normal six-state control scheme and also a dithered variation of the six-state driver. The acoustic response of the drive to the standard controller was used a reference to compare the new drive with the drive system it will be replacing. The following figures present the results of the acoustic testing.

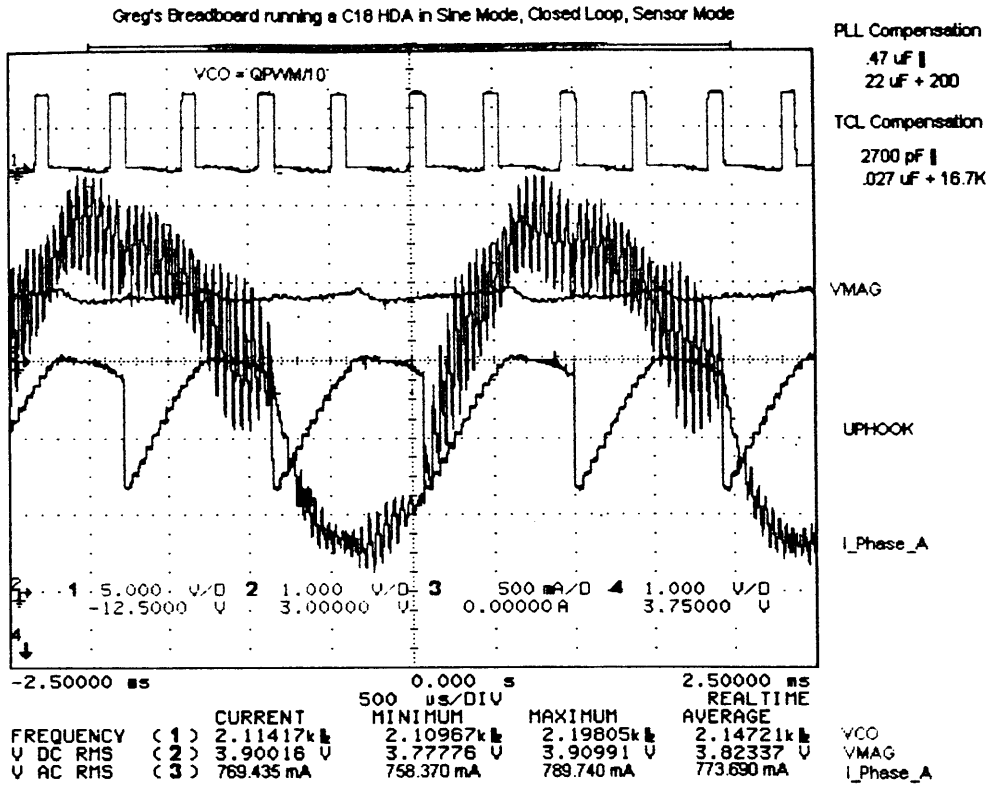

Figure 5-2: Current and Voltage Waveforms for Sinusoidal Drive

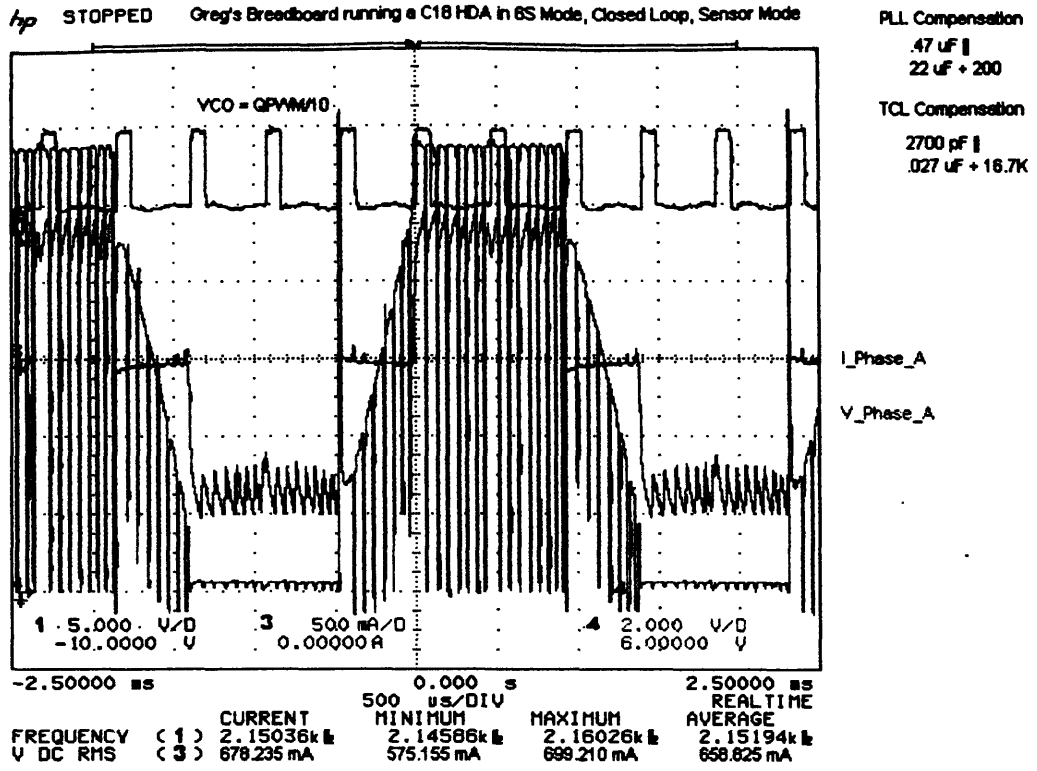

Figure 5-3: Current and Voltage Waveforms for Six-State Drive

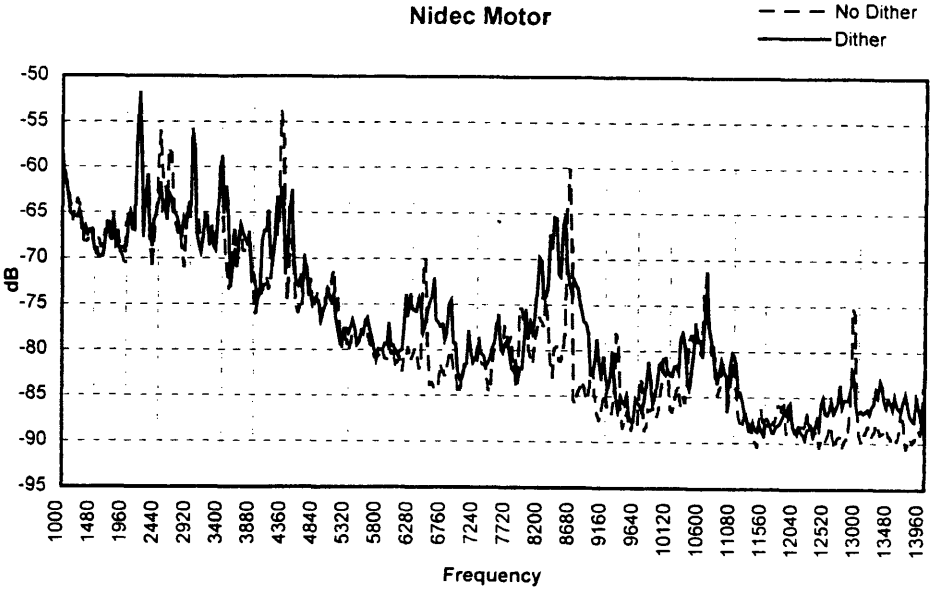

Figure 5-4: Acoustic Spectrum Nidec Motor-Old Six-State vs. Old Six-State (Dithered)

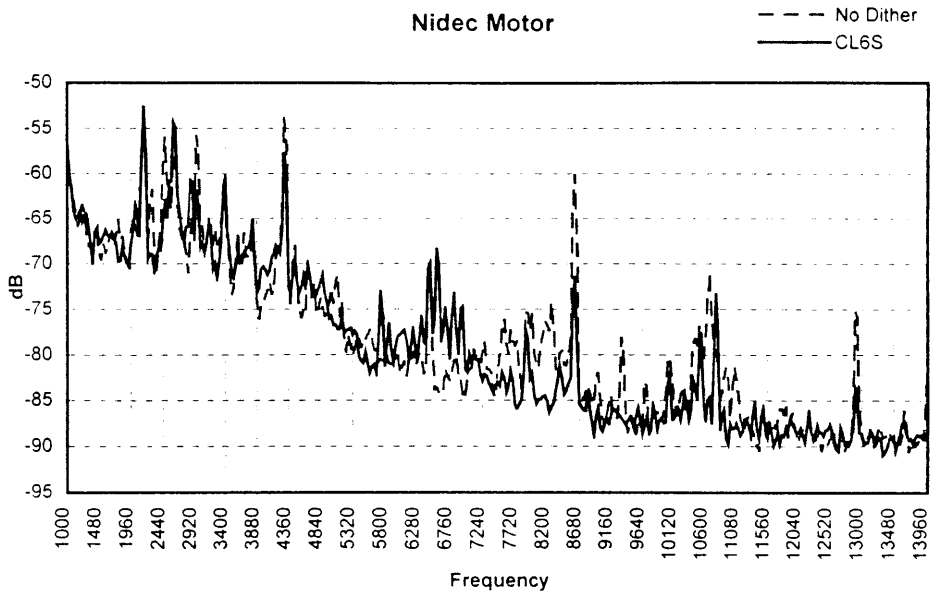

Figure 5-5: Acoustic Spectrum Nidec Motor-New Six-State vs. Old Six-State

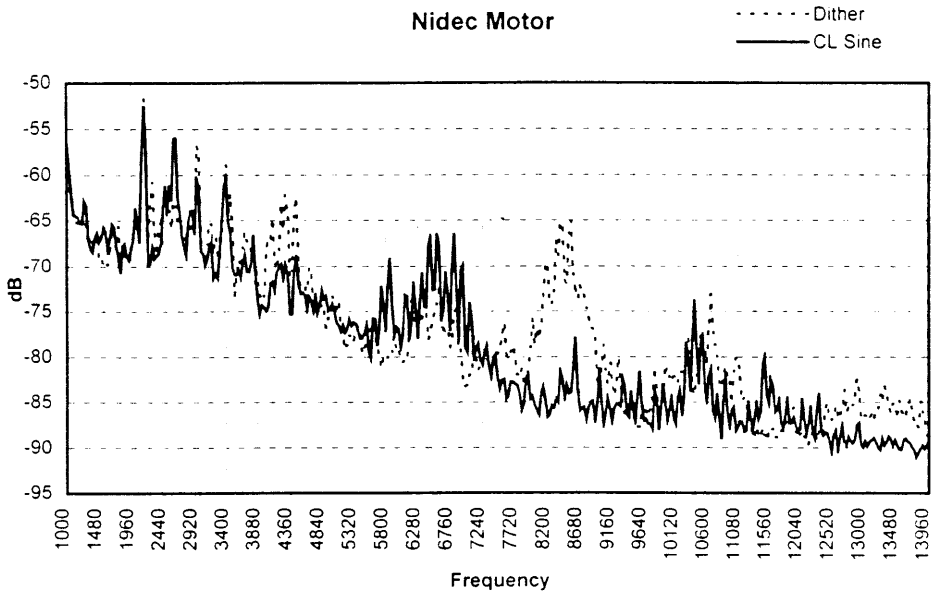

Figure 5-6: Acoustic Spectrum Nidec Motor-Sinusoidal Drive vs. Old Six-State (Dithered)

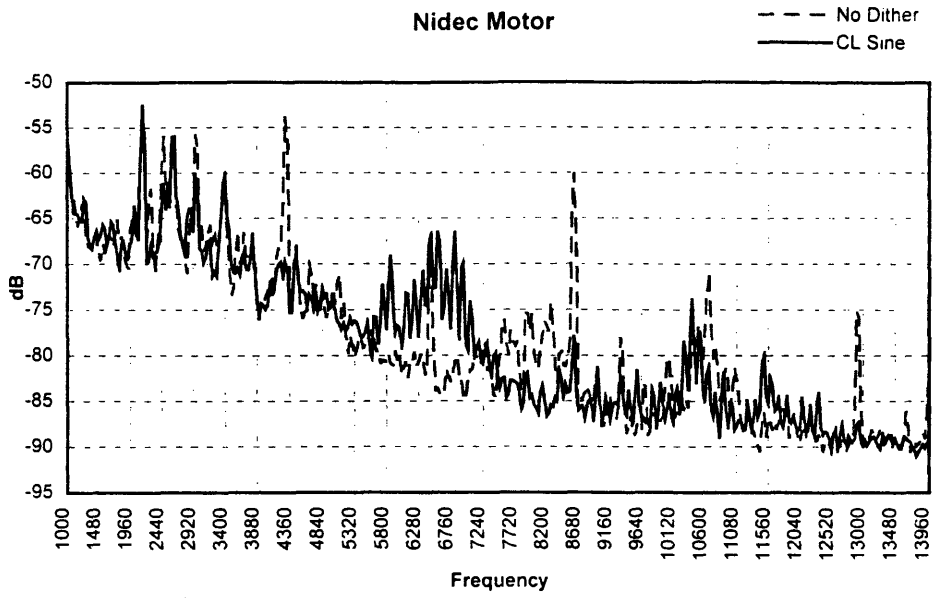

Figure 5-7: Acoustic Spectrum Nidec Motor-Sinusoidal Drive vs. Old Six-State

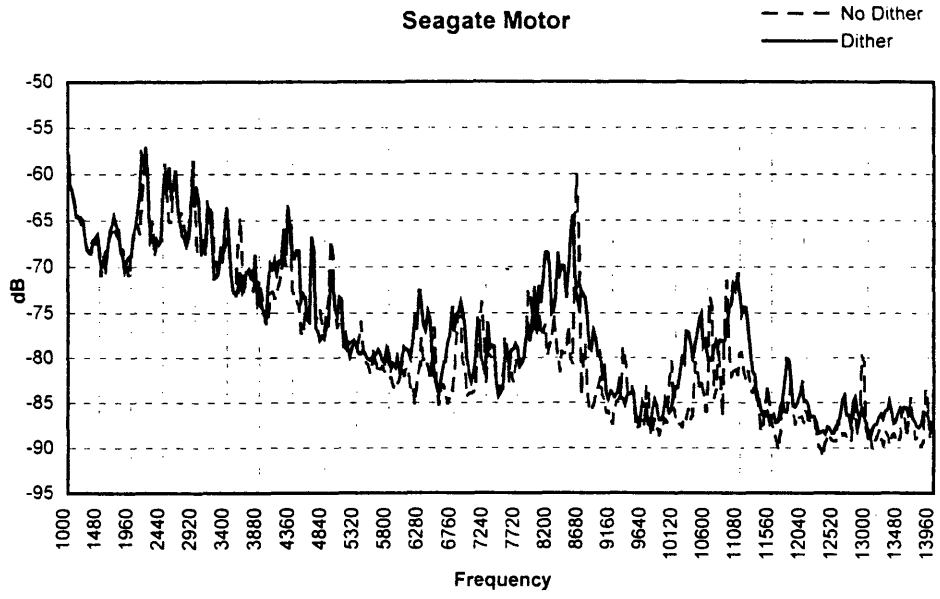

Figure 5-8: Acoustic Spectrum Seagate Motor-Old Six-State vs. Old Six-State (Dithered)

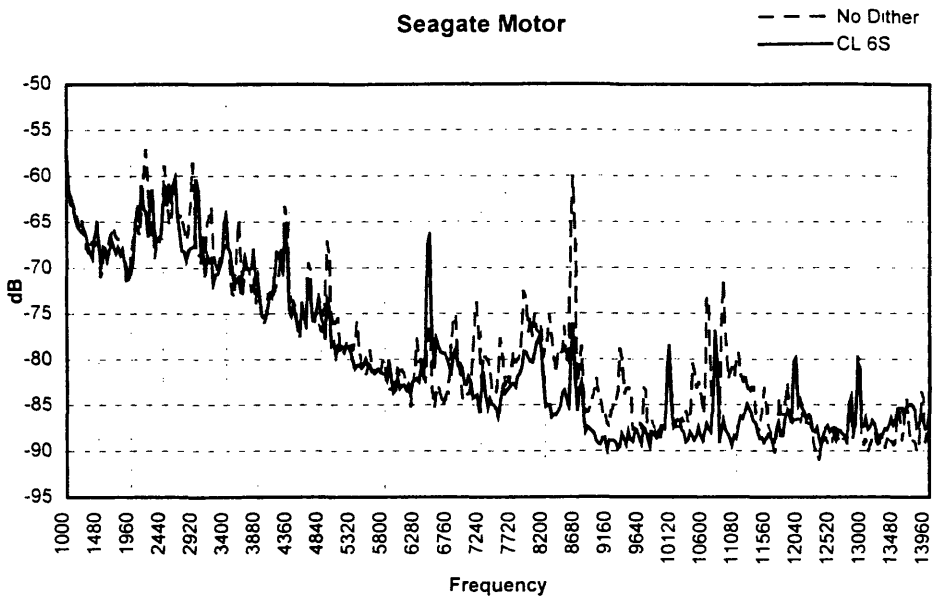

Figure 5-9: Acoustic Spectrum Seagate Motor-New Six-State vs. Old Six-State

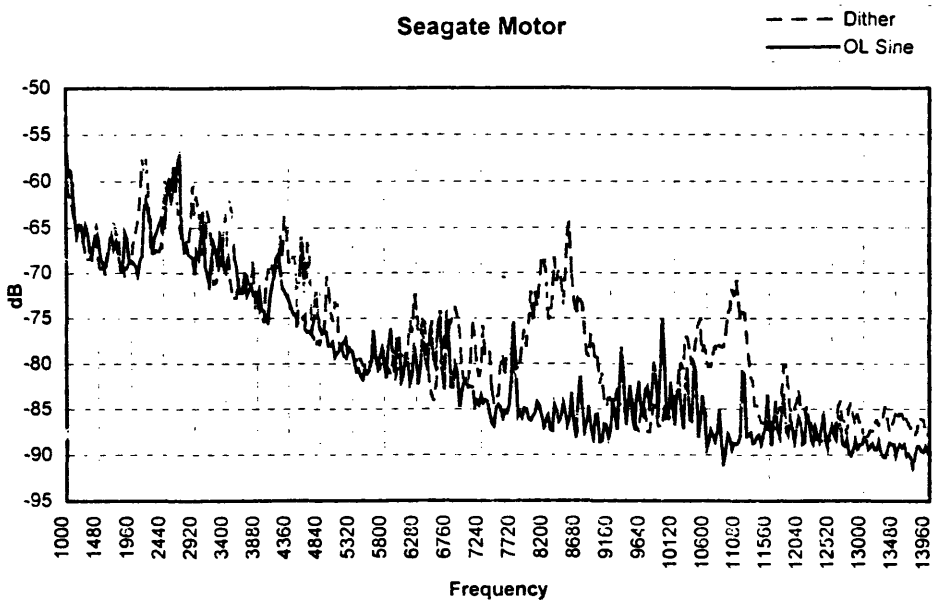

Figure 5-10: Acoustic Spectrum Seagate Motor-Sinusoidal Drive vs. Old Six-State (Dithered)

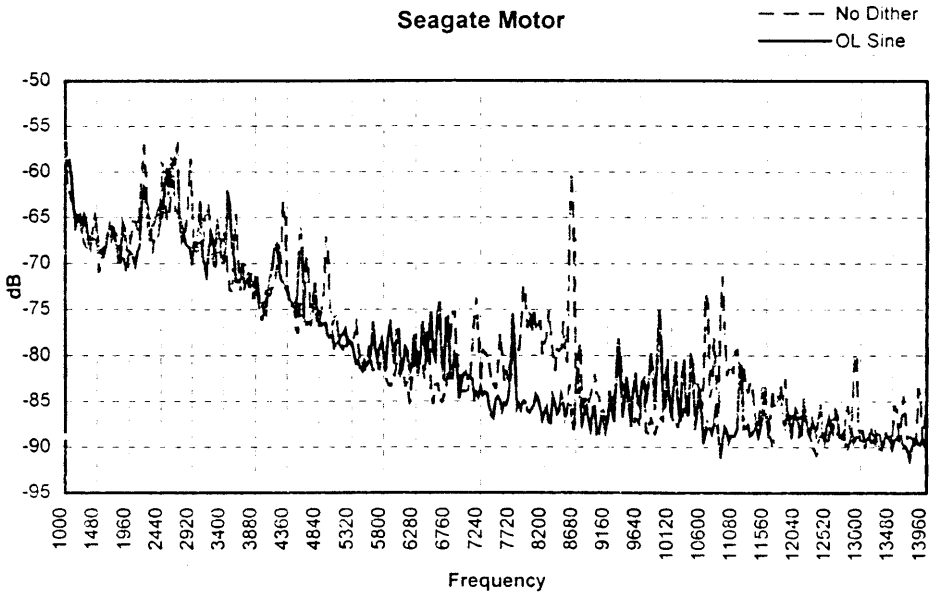

Figure 5-11: Acoustic Spectrum Seagate Motor-Sinusoidal Drive vs. Old Six-State

Chapter 6

Discussion of Results

The primary purpose of the testing was to prove both that the system could lock to the acquired phase information, and also that the acoustic noise of the motor was reduced. The testing shows that the drive system can be implemented, and also that it delivers the acoustic performance it promised.

6.1 Waveform Distortion

The most notable difference between the expected waveforms and the actual waveforms is that as implemented, the currents generated by the test board are not sinusoidal, but contain a significant level of distortion. This can be for a number of reasons. The first reason is that the current feedback loop is responding to the system. This can be seen by the glitches on V_{MAG}. This puts distortion into the hook waveform. The shape of the phase current will therefore also be distorted. The current control loop may be responding because it is too fast, or because there is some error in the actual construction of the test board. The test board was known to be flaky, so it is possible that the errors are due to coupling on the test board.

A second source of possible distortion comes from the implementation of the phase detector. The phase detector described in Chapter 4, outputs a phase error signal only after it has completed both the positive and negative integrations. The test board, however, was implemented so that the phase-locked loop responded to the output of the integrator in the phase detector even during an error detection cycle. This will cause the loop to respond to the instantaneous output of the phase detector, instead of the final output. Even if the current is in

phase with the motor, the output of the instantaneous output of the phase detector will be interpreted by the phase-locked loop as a phase error.

Also, because the output of the phase detector is proportional to the current flowing through the motor, it is possible that changes in V_{MAG} were introducing errors in the output of the phase detector which might have caused some unusual oscillations.

The oscillations present in the current did not effect motor performance as far as the acoustic test, but a cleaner signal would generally be desired to ensure proper functioning of the phase locked loop.

6.2 Reduction of Acoustic Noise

The true test of the sinusoidal drive was whether or not it would succeed in reducing the acoustic noise of the motor. In the testing performed for this thesis, the sinusoidal drive performed exceptionally in this regard. On both motors the sinusoidal drive scheme outperformed the new six-state drive, the old six-state drive, and the dithered six-state drive.

The data in Figures 5-5 and 5-6 illustrate the remarkable ability of the sinusoidal drive to eliminate harmonics of the motor. The new six-state drive in Figure 5-5 exhibits several resonant peaks. These peaks are at 6, 7, 11, 24, and 36 times the electrical frequency of the motor. The sinusoidal drive scheme reduces the 11th harmonic by 10 dB. The resonant peak at the 24th harmonic is reduced by 7 dB, and the 36th harmonic is reduced by 5 dB. These differences in acoustic noise were actually audible during testing. This test clearly demonstrates the improvement of a sinusoidal drive over a six-state drive.

Figure 5-6 compares the performance of the sinusoidal drive to the results of dithering the old six-state drive. It should be noted that there was nothing in common between these two drive systems, so it is possible that differences in the power drivers or other parts of the circuitry played a part. Nevertheless, Figure 5-6 gives compelling evidence of the superiority of a sinusoidal drive in eliminating acoustics. Comparing the acoustic noise spectrum in

Figure 5-6, we can see that the drive system with sinusoidal drive outperformed the dithering technique by substantially reducing the content at the 12th harmonic and the 36th harmonic. The effect of the dithering can be seen in Figure 5-6 by the smearing of the frequency content at 8.3 kHz.

The testing on the Seagate motor supported the conclusion that the sinusoidal drive can substantially reduce the pure-tone noise emitted by a motor, but it also highlighted the frail nature of the system. When the Seagate motor was driven with sinusoidal drive, the speed control loop was not able to maintain the speed of the motor. The testing of the Seagate motor had to be done without closing the speed control loop.

6.3 Future Work and Improvements

The experimentation showed that implementing a sinusoidal drive is a practical solution to the problem of acoustic emissions from motors. The system as presented in this thesis is by no means perfect, however, and much can be done to make the response of the system better.

The reasons for Seagate drive failing to speed-regulate must be investigated and understood. It is not acceptable for the sinusoidal driver to work successfully with one hard disk drive and not another.

The primary work needs to be done on the phase-locked loop, which is the most fragile part of the system. A balance must be found between the smallest integration window which can be used and still provide adequate gain in the phase detector.

Further studies should be conducted concerning the possibility of detecting the phase current both at its negative peak and positive peak. The negative peak of the current will occur in the region where the negative phase current is flowing through R_{SENSE}. These peaks can be used as well to generate phase error. The phase detector would therefore operate on the positive peaks interleaved with the negative peaks. It would then be possible to generate phase

error information on six peaks instead of just three as was done on the test board. The errors due to the track and hold when detecting the negative peaks will be different from the errors generated when tracking and holding the positive peaks, and the result of these differences should be investigated as part of a solution proposing to detect phase on all six available peaks.

Appendix A

A.1 Small Signal Gain of Phase Detector

The small signal gain between the BEMF current and the phase current can be found by differentiating equation (4.6) with respect to ϕ_{BEMF}. Doing so gives

$$\frac{d\phi_B}{d\phi_{BEMF}} = \frac{-1}{\sqrt{1-\frac{\sin^2(\phi_{BEMF})}{|K^2-2K\cos(\phi_{BEMF})+1|}}} \cdot \left[\frac{\sqrt{K^2-2K\cos(\phi_{BEMF})+1}\cdot\cos(\phi_{BEMF})-K\sin^2(\phi_{BEMF})\left(K^2-2K\cos(\phi_{BEMF})+1\right)^{-\frac{1}{2}}}{|K^2-2K\cos(\phi_{BEMF})+1|}\right] \tag{A.1}$$

The slope of the phase relation between ϕ_B and ϕ_{BEMF} is found by evaluating (A.1) at zero. The slope at the origin is therefore

$$\left.\frac{d\phi_B}{d\phi_{BEMF}}\right|_{\phi_{BEMF}=0} = \frac{-1}{|K-1|}. \tag{A.2}$$

A.2 Location of Zero-Slope point of ϕ_B

The location of the point of zero-slope of (A.1) can be found by setting the equation equal to zero and solving for ϕ_{BEMF}. It is assumed that $K>1$. The only way (A.1) can equal zero is if the term in brackets is equal to zero. There is no value of ϕ_{BEMF} for which the square root term on the left can equal zero. We must therefore solve

$$\frac{\sqrt{K^2 - 2K\cos(\phi_{BEMF}) + 1}\cdot\cos(\phi_{BEMF}) - K\sin^2(\phi_{BEMF})\left(K^2 - 2K\cos(\phi_{BEMF}) + 1\right)^{-\frac{1}{2}}}{\left|K^2 - 2K\cos(\phi_{BEMF}) + 1\right|} = 0 \tag{A.3}$$

This equation can be manipulated by,

$$\sqrt{K^2 - 2K\cos(\phi_{BEMF}) + 1}\cdot\cos(\phi_{BEMF}) = K\sin^2(\phi_{BEMF})\left(K^2 - 2K\cos(\phi_{BEMF}) + 1\right)^{-\frac{1}{2}}, \tag{A.4}$$

$$\left(K^2 - 2K\cos(\phi_{BEMF}) + 1\right)\cdot\cos(\phi_{BEMF}) = K\sin^2(\phi_{BEMF}), \tag{A.5}$$

$$\cos^2(\phi_{BEMF}) - \left(K + \tfrac{1}{K}\right)\cos(\phi_{BEMF}) + 1 = 0, \tag{A.6}$$

$$\cos^2(\phi_{BEMF}) - \left(K + \tfrac{1}{K}\right)\cos(\phi_{BEMF}) + 1 = 0, \tag{A.7}$$

$$\cos(\phi_{BEMF}) = \frac{\left(K + \frac{1}{K}\right) \pm \sqrt{\left(K + \frac{1}{K}\right)^2 - 4}}{2}, \tag{A.8}$$

and finally,

$$\cos(\phi_{BEMF}) = K \quad \text{or} \quad \cos(\phi_{BEMF}) = \tfrac{1}{K} \tag{A.9}$$

Since we are assuming that $K > 0$, the correct solution corresponds to $\cos(\phi_{BEMF}) = \frac{1}{K}$. This can be substituted back into (4.6) to find the corresponding value of ϕ_B. Making use of the fact that

$$\sin(\phi_{BEMF}) = \sqrt{1 - \frac{1}{K^2}}, \tag{A.10}$$

We can substitute back into (4.6) to find

$$\phi_B = \sin^{-1}\left(-\frac{1}{K}\right). \tag{A.11}$$

There is a simple relationship between ϕ_B and ϕ_{BEMF}. Replacing the parameter $\frac{1}{K}$ by $\cos(\phi_{BEMF})$, (A.11) can be rewritten as

$$\sin(\phi_B) + \cos(\phi_{BEMF}) = 0. \tag{A.12}$$

The values of ϕ_B and ϕ_{BEMF} which satisfy equation (A.11) fall along a circle centered at the origin. Any valid operating point of the system must be in this circle in order for the relationship between the phase current and BEMF current to be correct.

References

[1] Chalmers, B.J.,ed., *Electric Motor Handbook*, Boston: Butterworth & Co.Ltd., 1988.

[2] Grochowski, E., Hoyt, R.F., "Future Trends in Hard Disk Drives," *IEEE Transactions on Magnetics*, vol. 32, no. 3, pt. 2, May 1996, pp. 1850-1854.

[3] Schirle, N., Lieu, D.F., "History and Trends in the Development of Motorized Spindles for Hard Disk Drives," *IEEE Transactions on Magnetics*, vol. 32, no. 3, pt. 2, May 1996.

[4] Trzynadlowski, A.M, Blaabjerb, F., Pedersen, J.K, Kirlin, R.L, Legowski, S., "Random Pulse Width Modulation Techniques for Converter-fed Drive Systems-A Review," *IEEE Transactions on Industry Applications*, vol. 30, no. 5, Sept.-Oct. 1994, pp. 1166-1175.