FLIP CHIP ATTACHMENT METHODS: A METHODOLOGY FOR EVALUATING THE EFFECTS OF SUPPLIER PROCESS VARIATION AND SUPPLIER RELATIONSHIPS ON PRODUCT RELIABILITY

by

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Submitted to the Sloan School of Management and the Department of Materials Science Engineering in partial fulfillment of the requirements for the degrees of

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Abstract

This thesis examines how variation in supplier processes, as well as supplier relationship strategies, can affect product performance for an automotive electronics company. An examination of supplier process variation is a method that is used to uncover potential problems up front during the development phase. Consequently, processes can be adjusted during the product development cycle rather than after the product is in production when it is much more difficult and costly to adjust processes and correct potential problems. I have proposed a statistical methodology that can be used to determine how modifications in supplier processes can adversely affect product performance. An electronics packaging technology, termed flip chip, provides the technological foundation for the research. More specifically, the manufacturing processes of three materials used in the flip chip package - underfill, solder mask, and IC passivation - were analyzed to determine how variation in these processes could affect the adhesion characteristics of the flip chip package.

The results of the research indicate that the current underfill material used in the flip chip package maintains its adhesion capability even when there is substantial variation in the underfill process. The results indicate that there may be degradation in adhesion capability of the solder mask material with slight changes in the solder mask process. Additional studies indicate that die passivation may also exhibit variation in adhesion capability with changes in passivation process parameters.

Supply chain management strategies play an integral role in the product and process development. A firm's supply chain management strategy will have an impact on the likelihood of obtaining cooperation from suppliers to carry out a process variation study such as the one that was completed during this research project. The role of suppliers in the development of a new technology will be examined. Recommendations for the formation and management of supplier relationships are included, specifically as these relationships relate to the ability of a company to quickly adopt the capabilities to develop and implement a new technology.

Thesis Advisors

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Professor Frederick McGarry, Materials Science Engineering

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The last two years at LFM have been a truly remarkable experience for me. I feel privileged and honored to be a member of the LFM class of 1998. My classmates are an exceptional group of very talented people. I thank them for making my two years at LFM an enriching and fun experience.

I would also like to thank my significant other, Brandon. I feel very fortunate to have him in my life. He has provided me with much joy and happiness during the last few months. I am very appreciative of his support and patience during the writing of this thesis. I am looking forward to spending many more years together with him.

This thesis is dedicated to my family. My wonderful parents Ralph and Nancy have always been there for me. They have provided me with love, support and encouragement throughout my life. My brother Don, along with being a wonderful brother, is a great friend. He always keeps me laughing and helps me to maintain my perspective on life.

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1. Introduction

As the rate of change continues to accelerate in today's global economy, companies must continually strive to shorten their development cycles. As new technologies emerge, the ability to quickly adopt and implement these technologies will be a source of competitive advantage. Along with the focus on the ever-increasing rate of change, there is a greater focus on the need for companies to establish systems that ensure superior product quality and reliability. In order to compete in today's marketplace, companies must have a quality system in place that delivers a defect-free product to their customers. This thesis will propose a methodology to improve quality and product reliability during the product development phase, when it is easiest and least costly to correct potential quality problems. The thesis also examines the role that supplier relationships play in the development of a new technology. Supply chain strategies are just as important as the product and process strategies in the rapid adoption of emerging technologies.

The research for this thesis was conducted at an automotive electronics supplier. In the drive for smaller, cheaper and lighter assemblies in the electronics industry, flip chip has emerged as a key technology to achieve these goals. The Internship Company, Delphi Delco Electronics Systems (DDES), is currently in the process of developing flip chip technology for laminate substrates that will be incorporated into several of its electronic control modules. I will refer to the flip chip package and the components that comprise the flip chip package frequently throughout the thesis. To familiarize the reader with the terminology, a schematic of a flip chip package is shown in Figure 1. A brief definition for each of the components that comprise the flip chip system follows the schematic.

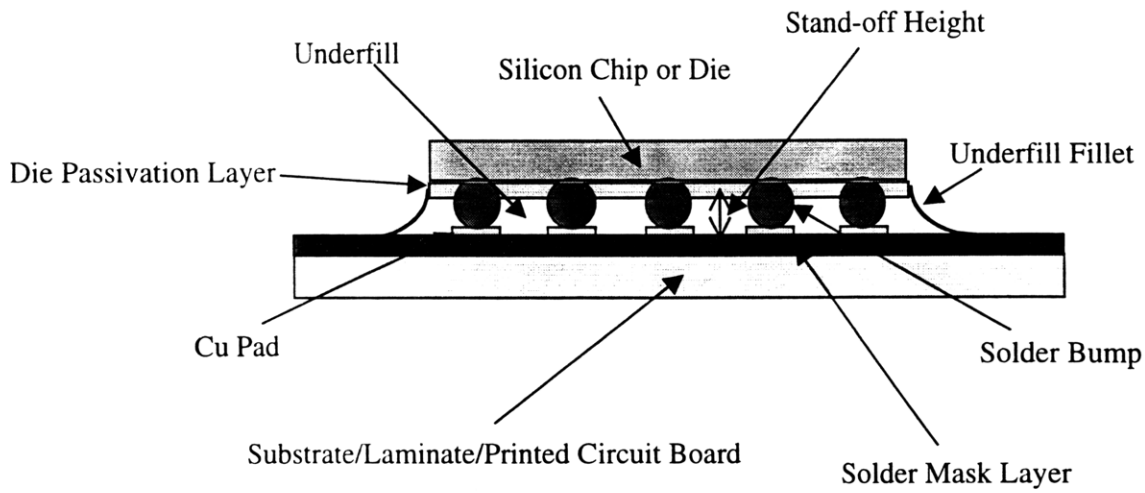

Figure 1 - Flip Chip Package Schematic

Flip Chip

Flip chip employs soldering directly between the integrated circuit die face and the interconnecting substrate. Solder bumps are deposited onto the chip termination lands. The chip is then aligned to the proper circuitry on the substrate and bonded in place using reflow soldering techniques.

Silicon Die or Chip

Silicon die or chip is the integrated circuit. Die, chip and IC will be used interchangeably throughout the thesis.

Die Passivation Layer

Die passivation is a layer of material deposited onto the underside of the IC. . Passivation coats the final metal and chip. Passivation provides moisture, ionic and physical protection to the chip as well as electrical insulation to the limiting metal contained in the IC. The passivation type and deposition method will vary with the chip technology and semiconductor fab facility. Some common types of passivation are silicon nitride, oxy-nitride and polyimide.

Substrate/Laminate/Printed Circuit Board

Laminate substrates are multilayer, organic printed circuit boards. They are formed from epoxy resins reinforced with glass fibers. The conductive material, copper, is plated onto the laminate sheets and etched to form the metal pattern. The substrate type referred to throughout this thesis is commonly known as FR-4 (flame retardant epoxy).

Underfill

The underfill consists of an anhydride-cured, epoxy resin, which is filled with silica particles. Underfill acts to mechanically couple the die and substrate together to locally constrain the Coefficient of Thermal Expansion (CTE) mismatch between the die and substrate. The underfill redistributes the stress from the solder joints to the chip, substrate and epoxy.

Solder Mask Layer

Solder mask (also known as solder resist) is the outermost layer of material on the printed circuit board. Solder mask is applied to the entire PCB surface, except for solder or contact lands, to both prevent solder wetting during the assembly process and to provide protection from environmental damage after assembly. Solder mask is an organic material comprised of epoxy and inorganic fillers.

Solder Bump

The solder bump consists of eutectic 37Pb/63Sn solder. The solder melts during the reflow stage to form the interconnection between the die and the substrate. The solder is deposited onto the die using one of several methods, which depend upon the materials chosen for the solder and the chip design. Three of the most common methods are solder evaporation, solder electroplating and solder screen printing.

Table 1 lists typical dimensions for a flip chip package. These dimensions are typical for a flip chip system and could vary depending on the chip and technology employed. Bump pitch refers to the distance from the center of one bump to the center of

an adjacent bump. Stand off height refers to the vertical distance between the substrate and die.

Attribute	Dimension
Silicon Die	250 mil X 250 mil
Die Thickness	10 mil
Stand Off Height	4 mil
Bump Diameter	6 mil
Bump Pitch	8 mil
Number of Bumps	100

Table 1 - Flip Chip Dimensions

Flip chip technology is not new to the electronics industry. Flip chip attachment methods have been used for over 30 years in hybrid products (which contain ceramic substrates). However, using flip chips on laminate substrates is a new technology for the electronics industry. Because there are many reliability issues involved with using flip chip on laminate in the extreme environment of an automobile, the design and process technologies have undergone extensive capability studies, testing and verification to ensure superior product reliability. The methodology contained in this thesis describes one way in which product reliability can be improved.

1.1 Motivation

The motivation for the research conducted during this internship was to determine if slight variation in supplier processes could adversely affect product reliability in a new technology, which is termed flip chip. Several years ago, DDES made the decision to begin using flip chip as a method of attaching semiconductors to the circuit boards that it assembles. There were several reasons for incorporating this technology into its products. DDES's primary customer, General Motors, wanted one of the engine control modules to be mounted directly on the engine. This meant that there were size limitations in how large the electronic assembly could be. The flip chip attachment method enables a

reduction in size. Flip chip was also a key enabler to meet customer's cost targets, since the cost of flip chip is less than the cost of using traditional packaged die.

Using flip chip attachment methods on laminate substrates is still a largely unproven technology. There are many reliability issues that must be addressed to assure superior product reliability. Several years ago a large study was undertaken to find a set of materials in the flip chip assembly that would exceed reliability targets, which is measured by the number of thermal cycles that are completed. (Mean time to failure, MTTF, is a common measure of reliability.) After expending significant research and development resources, DDES was able to find a material set that would exceed their specifications. However, the reliability of this material set is precarious in that even slight changes in the formulation or processing of any one material could dramatically affect the reliability of the entire flip chip assembly. DDES has experienced situations in which slight changes in the formulations or the processing of a material has resulted in adverse effects in flip chip performance and reliability.

In general, DDES can cite many examples in which slight changes in either its own processes or the processes of its suppliers have resulted in adverse consequences. Performing an ex ante process variation study in the development phase is a method of determining how changes in processes can potentially alter product performance. This information can then be used to communicate to the suppliers what the tolerances for their processes must be in order to assure the needed level of reliability.

In order to successfully complete a process study such as this, cooperation and assistance from suppliers is necessary. The ideal situation is when a supplier is a full partner in the product development cycle. However, it is uncommon for suppliers to be fully integrated in the design and development of a new technology. Rather, suppliers are often competing amongst each other for customers, and in many cases are reluctant to share proprietary information with their customers. The key to having supplier cooperation for a study such as this is designing the appropriate incentive scheme and having the necessary supplier relationship strategy in place so that suppliers are motivated to participate fully in a study such as this. During the course of the internship, I was able

to obtain the necessary cooperation from some suppliers. However, I was not able to obtain assistance from other suppliers, which hindered my ability to fully complete the proposed study. These differences in supplier responsiveness and supplier relationships will be explored later in this thesis.

1.2 Thesis Organization

The thesis has been organized into the following chapters.

Chapter 1 - Introduction

This chapter provides an introduction to the project, the motivation for the project, and a description of the organization of the thesis.

Chapter 2 - Company and Project Background

This chapter provides the reader with some necessary background information on the Dephi Delco Electronics Systems and the project itself. It also describes the goals of the project.

Chapter 3 - Flip Chip Technology

This chapter describes the flip chip technology in detail. Included are overviews of the history of flip chip technology to date, flip chip markets, electronics packaging, and the flip chip assembly process. This chapter also describes the critical reliability issues associated with using a flip chip package on FR-4 (laminate) substrates, and the typical failure modes observed with flip chip packages. Finally, there is a discussion of flip chip adhesion, as well as an explanation as to why adhesion is critical to flip chip reliability.

Chapter 4 - Supplier Material Processes

This chapter describes the three materials that are the focus of my research: underfill, die passivation and solder mask. For each material, I have provided an overview of what the material is composed of, how it is manufactured and what the key product and process parameters are. I have specifically pointed out those parameters that are viewed as critical for flip chip adhesion.

Chapter 5 - Experiments and Data Collection

This chapter describes the experiments that I conducted. An overview of the test methods and the design methodology are described. This chapter also includes summaries of the data and data analysis that were performed during the internship.

Chapter 6 – Supplier Relationship Strategy

This chapter presents all of the management issues and findings that I researched during the internship. I have discussed DDES's recent change in its strategy as a result of a global sourcing initiative and a recent merger with Delphi Automotive Systems. I have compared and contrasted the traditional supplier relationship with the "supplier partnership" that has become popular with many companies. An overview of DDES's current strengths and weaknesses with its supplier relationship strategy is also included in the context of current knowledge in the industry regarding advantages and disadvantages of forming supplier partnerships.

Chapter 7 - Results and Recommendations for Further Study

This chapter summarizes the findings from the data analysis that was performed and provides recommendations for further study. I have also included an overview of the lessons learned from this project, and how a project such as this might best be approached in the future. Additionally, other recommendations that relate to this project are included.

Chapter 8 - Conclusions

This chapter summarizes the key findings in the thesis as well as reiterates the main recommendations.

2. Company & Project Background

This chapter provides the reader with some necessary background information on the Internship Company as well as an introduction to flip chip technology. This chapter also provides the background for the internship project as well as the specific goals for the research.

2.1 Company Background

The analysis in this thesis was developed during a research internship at Delphi Delco Electronics Systems (DDES). DDES is an automotive electronics supplier that is headquartered in Kokomo, Indiana. Approximately 80% of DDES's sales are to its parent company, General Motors (GM). While the majority of DDES's operations are located in the Midwest, the division does have thirty-six facilities in fifteen countries. DDES currently employs 31,000 people worldwide, and its reported revenues were $5.6 billion in 1997. DDES designs and manufactures a variety of automotive electronics components, including engine control modules, air bag modules, anti-lock brake modules, radios, instrument clusters, heater/air controls, pressure sensors and voltage regulators. DDES also has a captive, in-house semiconductor fabrication division that supplies 40% of the ICs required for DDES products.

During the course of the internship, GM merged DDES with the other wholly owned components divisions, collectively known as Delphi Automotive Systems. The integration of DDES with Delphi creates an automotive systems supplier that can more effectively compete in global markets by developing new electronically enhanced vehicle systems. Delphi's strategy is to offer OEM automobile manufacturers competitive products that have complete systems capability and that can be fully integrated into the vehicle architecture. While it is not completely known how the merger will affect DDES, there are certain to be many changes in the organizational structure as Delphi moves to integrate DDES more fully into the division.

During the last ten years, the business climate has changed dramatically for DDES, specifically with respect to its relationship with General Motors. DDES used to

be a captive supplier to GM. It was a given that DDES would supply GM's needs for the automotive electronics that DDES manufactured, at a price that was determined by DDES. However, that relationship has changed with GM's global sourcing initiative. Now, DDES must compete globally with other automotive electronics suppliers on the basis of price, quality and delivery. The increased competition has forced DDES to make significant price cuts. In order to maintain the margins that DDES needs for reinvestment, there is a tremendous cost cutting initiative occurring within the company. In fact, DDES has also begun a global sourcing initiative with its suppliers, similar to that of GM's initiative, in order to drive down the costs of raw materials.

Because DDES is no longer assured of GM's business, DDES is aggressively pursuing new business opportunities outside the realm of GM. Growth in the future will be achieved primarily through seeking new international customers as well as through select acquisitions and joint ventures. DDES's strategy is to aggressively continue to cut costs while offering products with increased electronic functionality through a focus on safety, security, communications and convenience. Additionally, the merger with Delphi will certainly open up new doors and potential customer opportunities by aligning key design, manufacturing and marketing competencies. Competition among the automotive electronics suppliers is intense, and DDES knows it must meet customer expectations in terms of quality, cost and delivery to be able to satisfy its existing customers and to grow its customer base.

2.2 Project Background

In order to achieve the aggressive cost reductions that were necessary to meet its customer's price requirements (and at the same time continue to be a profitable division of Delphi Automotive Systems), DDES had to make some major modifications to the way it had traditionally designed the electronic control modules. One of the major changes, which is the focus of this thesis, was in the way the integrated circuits (IC's) are attached to the circuit board substrate. DDES is planning to incorporate flip chips on laminate printed circuit boards in several of its electronic control modules. Flip chip is a method used to mount bare semiconductor die (known as just die in the industry) to a

substrate. Mechanical and electrical connections are accomplished simultaneously by reflowing solder bumps on the die to make contact with the metal pads on the substrate. Figure 2 displays both a side view and top view of a flip chip attached to the substrate. Chapter 3 presents a detailed description of the flip chip assembly process.

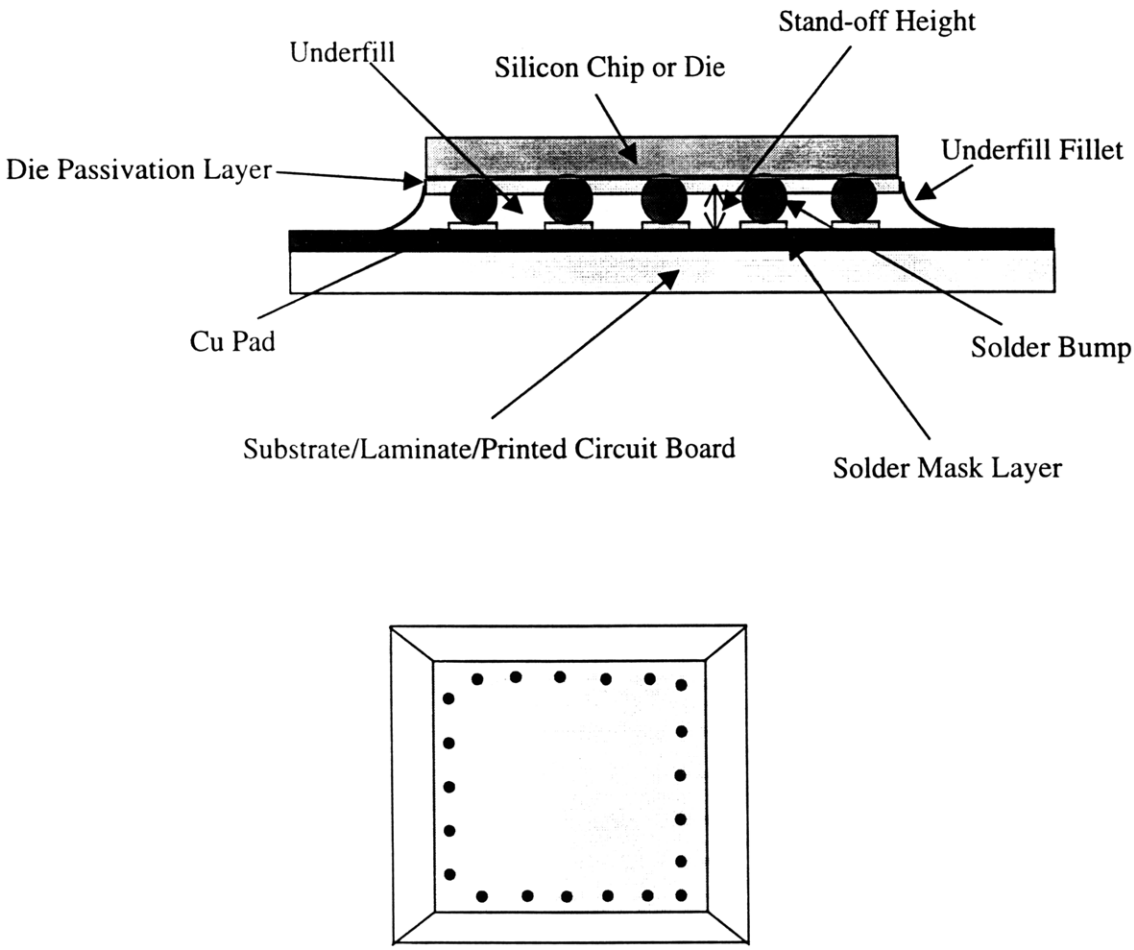

Figure 2 - Side and Top Views of an Attached Flip Chip

Flip chip technology is not new to the electronics industry. The industry, including DDES, has been using flip chips for over 30 years in its hybrid products. In hybrids, an inorganic ceramic serves as the substrate material. However, the flip chip attachment method had not been utilized on laminate substrates in the past. Because this is a new technology for DDES, and because there are many reliability issues involved

with using flip chip on laminate in the extreme environment of an automobile, the design and process technologies have undergone extensive capability studies, testing and verification to ensure superior product reliability. My research during the internship has dealt with one aspect of product reliability: understanding how variation in supplier processes can impact flip chip reliability. Specifically the goals of the internship were as follows:

- Study material variations at the supplier level that can degrade flip chip adhesion. The scope of the project included three materials used in the flip chip mounting process: underfill, solder mask and die passivation.
- Utilize a die shear test method as a means to performing sensitivity analysis experiments on how variation of the key process parameters for each material can change adhesion characteristics.
- Based upon the results of the experiments, communicate my findings back to the suppliers so that they could develop meaningful process specifications for the manufacture of flip chip assembly materials.
- Study the relationships that DDES currently has with its suppliers, and document DDES's current strategy for supplier relations and supply-chain management, specifically as they relate to the global sourcing initiative and the merger with Delphi. I will analyze the strengths and weaknesses of the existing system and make recommendations for improvements based upon current knowledge of the best practices.

3. Flip Chip Technology

The driving forces in the electronics industry are requiring smaller, lighter, and cheaper assemblies. The trend in the microelectronics industry is toward faster device speed, higher heat dissipation, lower cost, higher throughput, higher yields and enhanced reliability. Flip chip connection methods offer numerous advantages as compared with conventional interconnection methods such as wire bonding. (Section 3.3.1.1 includes a description of wire-bonding techniques). Several of the primary advantages of flip chip are: [1]

- In flip chip connections, the short interconnect distances allow for a fast signal response combined with a low inductance.
- Flip chip mounting requires a minimum amount of space on the substrate. This results in significant savings in substrate material as well as in the overall board area required for the circuit board assembly.
- Because of the face-down configuration, the whole surface of the die can be used for different array configurations, which allows for the highest number of input/output connections.

3.1 Flip Chip History

IBM developed the first flip chip application in the early 1960's as an alternative to manual wire bonding. This technology, referred to as Controlled Collapse Chip Connection (C4), was developed as a method of achieving extremely high interconnect densities for high-end mainframe systems.[2] In the C4 process a high melting point 97Pb/3Sn alloy is deposited onto wettable chip pads on the die surface, which is then mounted on a ceramic substrate face down.[2] The solder bumps on the die match up with wettable substrate lands. The solder is reflowed to simultaneously form all electrical and mechanical connections between the die and the substrate. Flip chips mounted on a ceramic substrate have been used extensively for more than 30 years in the computer and

automotive industries. In fact, Delphi Delco Electronics Systems (DDES) was one of the first users of flip chips for ceramic substrate (hybrid) applications.

Due to the high cost of ceramic substrates (and, secondarily, the cost of licensing fees paid to IBM for use of the C4 process), there has been a lot of work directed toward new, cheaper processes, such as flip chip mounted on FR-4 (organic laminate) substrates. IBM at Yasu, Japan has been assembling solder-bumped flip chips on organic printed circuit boards since 1990, mainly for the personal computer and larger mainframe systems.[3] The process resembles the C4 technology in that it uses solder bumps to make these connections between the die and board, but it uses a low melting point eutectic 37Pb/63Sn solder to avoid thermal damage to the laminate substrate.

3.2 Flip Chip Markets

Currently flip chips represent approximately 2% of the semiconductor industry output, but that number is growing rapidly.[4] Today's large users of flip chips for electronics applications are found in various industries, including automotive, computers, hand-held consumer electronics and medical equipment. Each industry has different requirements for its products and varying reasons for using flip chip technology. The automotive industry, for example, requires very good reliability with high temperatures, high humidity, and significant thermal cycling. The computer industry desires high speeds with good electrical performance. The hand-held consumer electronics industry desires small, lightweight products with low self-inductance.

There is extensive research being done to evaluate flip chip processes. Much of the research is focused on developing low-cost, high-volume production processes for flip chip. A low-cost flip chip mounting process, however, is only realized by decreasing the process/assembly costs. This is due to the fact that the cost savings are balanced by the additional cost for the deposition of the bumps and testing of the chips. A key means for achieving reasonable costs is for the flip chip assembly process to be compatible with the standard Surface Mount Technology (SMT) reflow process (and therefore existing equipment and process knowledge).

3.3 Electronics Packaging Overview

Electronics packaging has traditionally served four functions to assure an IC's performance: power distribution, signal distribution, heat dissipation and circuit protection.[5] Each of these functions must be taken into consideration when designing components for circuits, and tradeoffs usually exist which include cost, size, reliability and testability. Electronic packages are typically classified into levels based on the number and sophistication of the electronic assembly of which they are comprised. Figure 3 provides an illustration of this hierarchy scheme.[5]

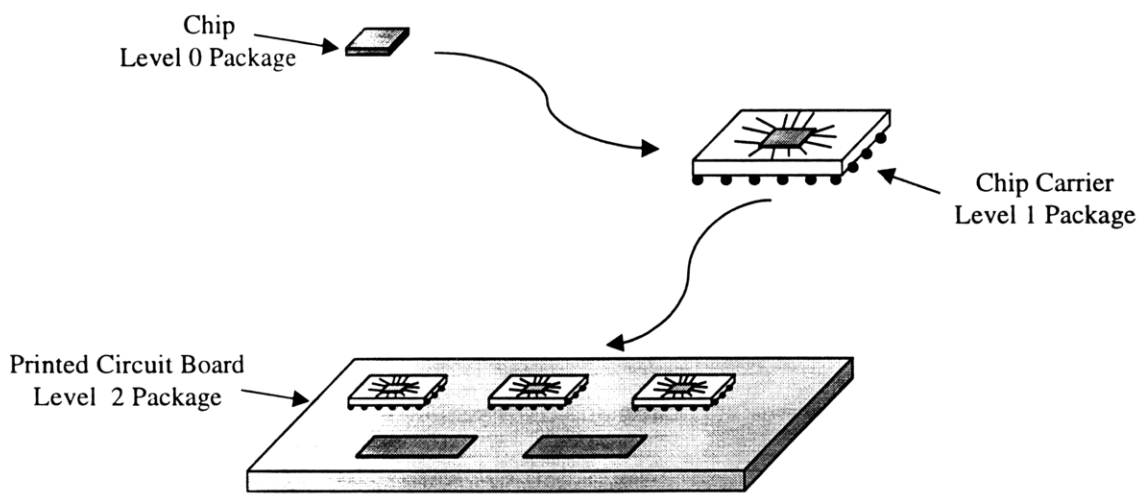

Figure 3 - Electronics Packaging Hierarchy

The semiconductor chip is considered to be the lowest level of packaging. As such it is classified as Level 0. The chip is mounted into a chip carrier module, which is considered the Level 1 connection. Level 2 packaging is sometimes referred to as the electrical circuit assembly. At this level, the individual chip carriers are mounted on a common base, usually a printed circuit board (PCB). Several Level 2 assemblies can be

interconnected into a complete electronics assembly, which represents the Level 3 connection.

3.3.1 Level 1 Technology

Micro-bonding is the collective name for the techniques used to make connections between the electronic circuits on the semiconductor chip and the surrounding circuitry.[6] To allow for connections between the chip and the outside world, single chip carriers usually contain a metallized pattern, which is commonly referred to as a lead frame. The surrounding circuitry may be an IC package or conductors on a substrate. Three methods are commonly used in the industry to make the interconnections between the chip and the lead frame: wire bonding, tape-automated bonding (TAB), and direct chip attach, also known as flip chip. Flip chip will be discussed in detail throughout the remainder of the thesis.

3.3.1.1 Wire Bonding

Wire bonding is the most popular method for connecting the die to the package. Wire bonding is accomplished by mounting the backside of a chip to a package with a conductive epoxy. Gold or aluminum wires are then bonded sequentially using a combination of heat, pressure and/or ultrasonic energy.[1] There are three types of wire bonding: ultrasonic, thermocompression and thermosonic ball/wedge.[1] See Figure 4 below for a schematic of a die wire bonded to a substrate. Chip on board (COB) is a micro-bonding technique used to bond bare die to the PCB. The chip is covered with a glob top after wire bonding.

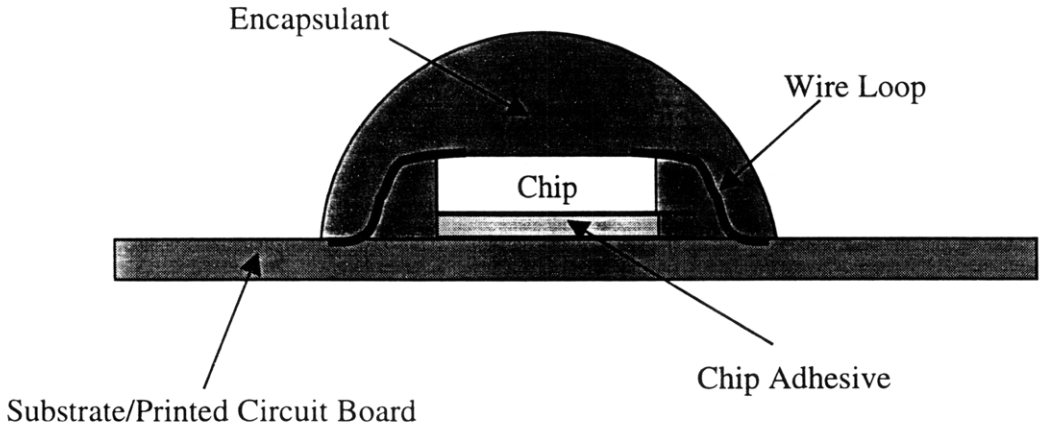

Figure 4 - Wire Bonding Attachment Schematic

Wire bonding is still by far the most commonly used technique for Level 1 connections. There are several advantages to wire bonding. It is fast and flexible, as well as being a standardized and balanced process (up to 7 wires per second), which is compatible with all plastic and hermetic types of packaging.[6] However, there are several notable disadvantages with wire bonding. The minimum pitch for wire bonding is approximately 100 μm, which limits the input/output capacity of the die. (Pitch refers to the distance between adjacent wires). Additionally, wire bonding may lead to parasitic interconnections between wires, and there is a reduced yield for larger number of bondings since each bond is made individually.[1]

3.3.1.2 Tape-Automated Bonding (TAB)

Tape-Automated Bonding (TAB) currently comprises less than 2 percent of the dies assembled worldwide.[6] TAB uses thermocompression bonding to attach bumped die to patterned metal on polymer tape. This is also known as inner-lead bonding (ILB). See Figure 5 below for a schematic of a die attached to a substrate using TAB methods. The chip is then encapsulated and the individual die are then removed from the tape and packaged using outer-lead bonding (OLB).

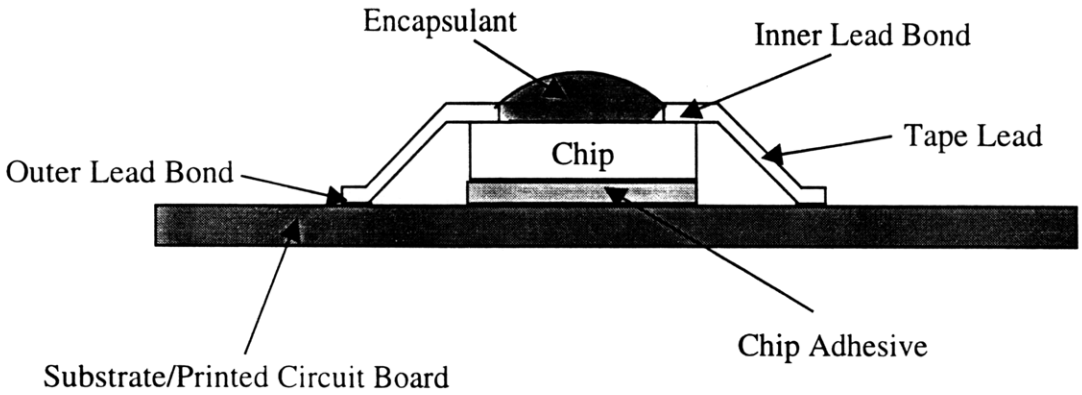

Figure 5 - TAB Attachment Schematic

TAB offers several advantages over wire bonding. A substantial increase in throughput can be achieved since all leads are bonded at once. Additionally, the interconnection density is greatly increased. As with wire bonding, there are several disadvantages to utilizing TAB methods. The ILB process requires the formation of bumps either on the die or tape, which can add cost to the process. Additionally, the tooling and equipment cost may be prohibitive and the availability of the necessary equipment may be an issue.[6]

3.3.1.3 Flip Chip (or Direct Chip Attach)

Flip chip will be discussed in detail throughout the remainder of the thesis. However, I will present a short explanation here to familiarize the reader with flip chip attachment methods. Flip chip employs soldering directly between the integrated circuit die face and the interconnecting substrate. Solder bumps are deposited on the chip termination lands. The chip is then aligned to the proper circuitry on the substrate and bonded in place using reflow soldering techniques. In this way, the interconnection bonds between the chip and substrate are made simultaneously, which reduces fabrication costs. Figure 6 displays a schematic of the side view and top view of a flip chip attached to a substrate.

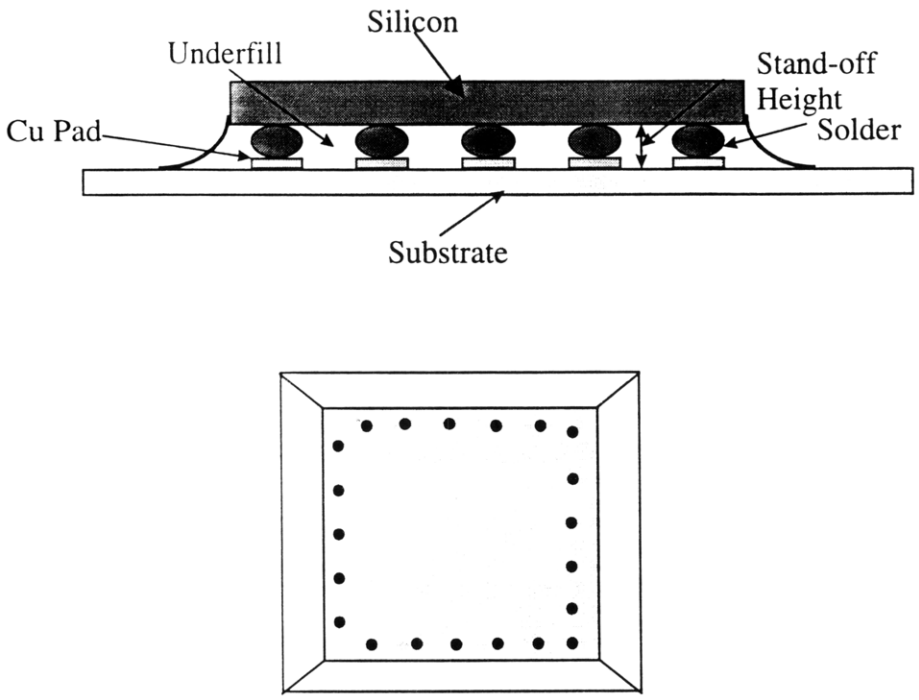

Figure 6 – Side and Top Views of Attached Flip Chip

Flip chip offers several advantages over wire bonding and TAB methods. Because flip chip does not require the use of bonding wires or leads to patterns outside the die's perimeter, flip chip achieves the highest ratio of active silicon surface to substrate area. Additionally, flip chip provides the shortest interconnect distances, the highest packaging density with the most efficient use of the substrate area, and better reliability because of the direct connection between the chip and substrate.[1] The main disadvantages with using flip chip are the potential thermal stress complications, the inability to rework flip chips, difficult flux removal, and the inability to pretest/burn in the die prior to assembly. The thermal stress complications associated with soldering flip chips to laminate substrates will be discussed in detail throughout the remainder of the thesis.

3.3.2 Level 2 Technology

Level 2 technology is the collective name for the techniques used to connect a chip carrier module to an electronic circuit assembly or substrate. The extension of the metal lead frame in the chip carrier to the outside package serves to connect the chip circuitry to the second level of packaging.[7] To facilitate interconnections, metallized conductor paths for signal and power transmission, footprints for mounting the chip carriers, and vias for signal propagation and heat transfer between the various board surfaces are formed on the substrate.[7] There are two primary methods used for the Level 2 connection: through-hole mounting and surface mounting.

3.3.2.1 Through-Hole Technology

Through-hole technology describes a method of connecting electronic components to a substrate by inserting the leaded components into plated through-holes in the substrate. When inserted, component leads protrude through the bottom-side surface of the circuit board. Mechanical attachment is achieved by passing the substrate through a molten-soldering process, commonly known as wave soldering. Electrical connection is achieved from the leads of the chip component through the solder to the plated through-holes. Figure 7 displays a schematic of a through-hole connection.

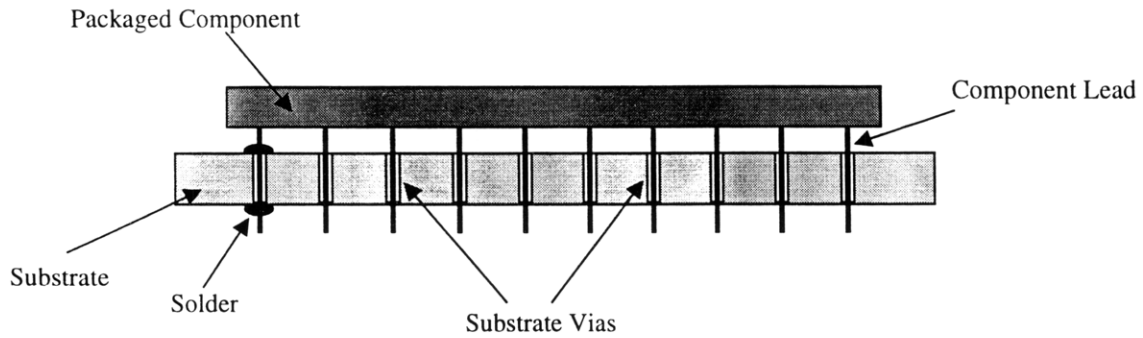

Figure 7 - Schematic of a Through-Hole Connection

3.3.2.2 Surface Mount Technology

With surface mount technology (SMT), electronic components are placed and attached directly to the surface of the printed circuit board. The electrical and mechanical connection is made with solder that has been reflowed. Figure 8 displays a schematic of a component attached by using surface mount technology.

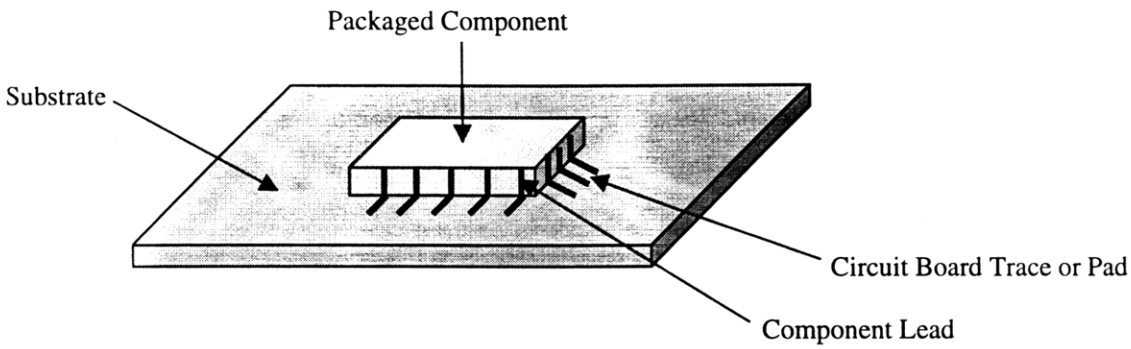

Figure 8 - Schematic of a Surface Mount Connection

SMT grew rapidly during the 1980's, and is now the dominant technology. SMT is largely an automated process, using equipment known as pick-and-place or chip shooters, since component leads and terminal ends must line up accurately with the corresponding pads on the surface of the printed circuit board. SMT is becoming the dominant technology over through-hole mounting, largely because SMT allows the products to have smaller weights and size, which is in line with market demands. SMT also possesses several other advantages as compared to through-hole technology, which are summarized as follows:

- higher functionality and more features: shorter signal paths which gives better signal speeds and high frequency performance.
- higher packing density on the circuit board with a smaller mounting height.
- simpler shape of components allows for simpler automated assembly and the mounting technique is flexible.

3.4 Flip Chip Assembly Process

One of the biggest advantages of using flip chip connection methods is that it is compatible with existing surface mount materials and processes. Traditional pick and place equipment as well as solder reflow ovens can be used for assembling and soldering flip chip packages. This allows greater flexibility for companies who desire to use the same assembly lines for both flip chip and other traditional surface mount components. While flip chip assembly is similar to traditional surface mount processes, there are several notable differences. Figure 9 displays a flow chart of the main processes involved in flip chip attachment. A brief description of each process follows.

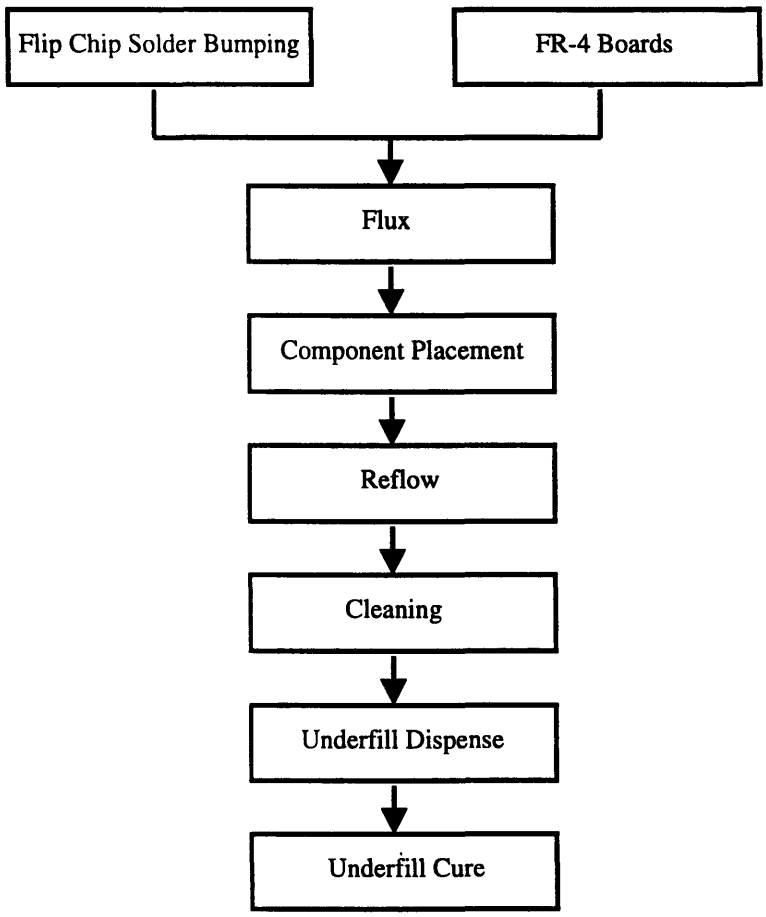

Figure 9 - Flip Chip Assembly Process

3.4.1 Flip Chip Solder Bumping

Solder bumping is the process by which solder is deposited onto the die. There are several methods utilized for bump deposition, which depend upon the materials chosen for the solder and the chip design. Three of the most common methods are solder evaporation, solder electroplating and solder screen printing. Screen printing is used as the deposition method when the pitch size is large. Screen printing is much cheaper than either evaporation or plating techniques. Solder bumps should be evaluated in terms of their electrical, mechanical and material properties. From an electrical point of view the solder bump should provide a low resistance electrical path.[8] From a mechanical point of view the bump interface must form a bond of sufficient strength in order to maintain

integrity during normal operating conditions. Another important mechanical property is the uniformity of the bump geometry across a die. Common defects include missing bumps, damaged or non-spherical bumps, pattern deviations and passivation damage.

3.4.2 Flux Dispense and Component Placement

Flip chips can be placed onto the substrate using automated pick and place SMT equipment. SMT equipment utilizes a machine vision system to achieve the necessary placement accuracy. Flux is applied to either the flip chip (using a dip method) or to the substrate (using a screen printing method) prior to the actual placement of the chip. The flux aids in the wetting of the solder by removing oxides from the surface of the bond pads. Flux also serves as a tacky agent to hold the flip chip in place during solder reflow.

3.4.3 Reflow

Reflowing is the process by which the solder is melted to form the interconnections between the pad limiting metal on the die and the substrate lands (copper pads). The solder on the flip chip is reflowed using a conventional SMT mass reflow process, which is composed of an infrared conveyer system. For the process that was studied during the internship, the solder bumps consisted of eutectic solder (63Sn/37Pb). The temperature used to flow the eutectic solder is approximately 200-220°C,[2] which is below that of the glass transition temperature of the FR-4 substrate. During reflow, flip chip interconnections may have the ability to self-align, which could offset minor placement inaccuracies.

3.4.4 Cleaning

Cleaning of the residual flux may or may not be required, depending upon whether or not a no-clean or fluxless process is used. When deemed necessary, cleaning is used to remove any flux residues that remain after the reflow process. Flux residues can adversely affect underfill adhesion and may lead to degradation in flip chip reliability.

3.4.5 Underfill Dispense

This process consists of dispensing a non-conductive, filled epoxy material between the chip and substrate. Underfill acts to mechanically couple the die and

substrate together to locally constrain the Coefficient of Thermal Expansion (CTE) mismatch between the die and substrate. The underfill redistributes the stress from the solder joints to the chip, substrate and epoxy. Hence, the strain on the solder joint interconnects is significantly reduced, and the flip chip is capable of enduring many more thermal shock cycles than if underfill were not present in the flip chip interconnect system.

Prior to underfill, the substrate is processed through a pre-bake oven, which drives off moisture. Moisture present in an organic substrate may result in poor adhesion of the underfill epoxy material to the substrate. Underfill is dispensed from a syringe along the perimeter of one or two edges of the die. The underfill is pulled under the die by capillary forces. Additional passes must be made along each side of the chip to form the underfill fillet. The fillet is essential to ensure that the entire surface area of the die, including the corners, has sufficient underfill beneath it. To improve the flow characteristics, the substrate is heated prior to the dispensing of the underfill. The capillary pressure, or driving force, pulls the underfill in under the die according to the following equation:

$$\Delta P = (2\gamma \cos \theta)/r$$

where ΔP is the driving force

γ is the surface tension

θ is the wetting angle

r is the standoff height.

This equation says that as the radius of the capillary gets smaller, the driving force increases. For our purposes, the radius is approximated by the stand-off height between the substrate and the die. Thus, once the underfill reaches the opposite side of the die, the flow will cease, since there will be a huge increase in the (effective) radius. The volume of underfill applied must be carefully measured prior to application to insure an adequate

amount without excess. Excess material can weaken the flip chip system, especially if underfill seeps onto the top side of the flip chip.

3.4.6 Underfill Cure

After the underfill has completely filled the gap between the substrate and die, the underfill epoxy must be cured. The time and temperature can vary depending upon the materials, but the cure schedule will typically be in the temperature range of 110-170 °C for durations of 30 minutes to 4 hours. A complete cure is necessary in order for the epoxy to be fully cross-linked. An underfill that is not completely cured is more susceptible to moisture absorption (and thus adhesion degradation) due to the "open spaces" present in the material. Research is ongoing looking for materials with a faster cure schedule to reduce cycle time and thereby reduce manufacturing costs.

3.5 Issues With Using Flip Chip on Organic Substrates

As was stated earlier, flip chips on ceramic and hybrid substrates have been widely used in the automotive and computer industries for many years. In the last several years, interest in using flip chips on organic substrates has grown as the search for lower cost technologies has intensified. The Internship Company, DDES, has invested significant resources in the research and development of flip chip on laminate to meet its reduced size and lower cost targets for its electronic controllers. While the amount of savings varies with the product, the magnitude of savings can be several dollars when laminate substrate is substituted for ceramic substrate. With many ICs, the costs of packaging outweigh the costs associated with the fabrication of the chip itself. Flip chip on laminate substrates is a solution for reducing costs associated with packaging of IC's. While at the same time, assembly costs are not dramatically increased since flip chips can be incorporated into the existing surface mount processes.

3.5.1 CTE Mismatch

The printed circuit board (PCB) forms the basis of the flip chip assembly. It provides the mechanical base for the flip chip package as well as the electrical connections. Flip chip on laminate substrate results in product reliability challenges that are not as significant with ceramic substrates. Namely, there is large coefficient of

thermal expansion (CTE) mismatch between the silicon die and the organic substrate. The CTE of silicon is roughly 2.5 ppm/°C, while the CTE of a PCB is approximately 20 - 25 ppm/°C. Ceramic substrates have a CTE around 6 ppm/°C, which is much closer to that of silicon. Because of the CTE mismatch between silicon and laminate substrates, the accumulation of stress borne by the solder joints will most assuredly result in premature device failure due to solder fatigue and cracking. The thermal mismatch is especially detrimental in the environment of an automobile, where thermal cycling is certain to occur.

Much work (both experimentally and by use of finite element analysis) has gone into demonstrating that the introduction of a rigid encapsulation layer between the chip and substrate, encapsulating the solder joints, enhances the thermal shock reliability of the flip chip assembly. The underfill material acts to mechanically couple the die and substrate together and locally constrain the CTE mismatch, thereby reducing the strain on the solder interconnects.

3.5.2 Failure Mechanisms

From a structural mechanics perspective, the solder fatigue mechanism will remain dormant as long as the mechanical integrity of the flip chip package remains intact. However, there are several high-risk sites that are susceptible to failure if the mechanical integrity of the flip chip system is compromised. Each failure mechanism and its potential risks must be considered when designing the die, materials and the manufacturing processes for flip chip attachment methods. The most frequently seen failure mechanisms for flip chip systems are as follows.

1. Delamination - Delamination at either the underfill/die interface or the underfill/substrate interface almost certainly will lead to reduced reliability. Delamination may be caused by factors such as low adhesion due to incompatible materials, low adhesion due to contamination or low adhesion due to moisture content.[9] Once the underfill has separated from either the die surface or the substrate, the solder interconnects are directly subjected to the strain resulting from the CTE mismatch. Solder fatigue cracking will ultimately lead to device

failure. Flip chip adhesion was the focus of my experimental work during the internship and will be discussed at length throughout the remainder of this thesis.

2. Chip Cracking - Silicon is a brittle material whose mechanical fracture property is dependent upon the fracture toughness of the material and any initial flaw present on the surface of the die.[9] There are tensile stresses present in the top surface of the die, which are caused by bending shear stress and in-plane tensile stress. Minimizing the size of surface flaws on the top side of the package is critical to preventing die fracture. Methods for wafer handling, packaging and transport should be developed that protect the chip from surface defects. Additionally, edge defects caused during the wafer sawing process can also lead to die fracture and device failure.

3. Underfill Cracking - Underfill encapsulant is comprised of an epoxy resin with silica filler added to lower the CTE. Microcracks are typically present in the underfill in the form of surface defects, irregularities, voids or delamination of the resin/filler interface. Under excessive thermal-mechanical loadings or residual stresses, it is possible that the microcracks will propagate. Once the crack starts to propagate, the solder interconnects or the epoxy-chip interface will be exposed to non-uniform stress concentration, which eventually leads to failure.[9] The key is to design the underfill so that these microcracks do not propagate from excessive mechanical stresses during thermal cycling.

4. Solder Fatigue - Fatigue is the primary mechanism for wear out of flip chip assemblies. The cyclic nature of the temperature variation causes the strain experienced by the solder joints to be cyclic, and therefore, the damage in the solder to be a function of the number of thermal cycles. Fatigue is an accumulation of stress due to temperature cycling. Fatigue failure takes place via the initiation and slow propagation of a crack until it becomes unstable. From the structural mechanics perspective, the solder fatigue mechanism will be dormant as long as the mechanical integrity of the entire flip chip package (die, laminate substrate and underfill) remains intact.[9]

5. Excessive Voids in Underfill Material near Solder Joints - The presence of underfill substantially increases the solder interconnect fatigue life. However, it is necessary to ensure that the underfill does not contain excessive voids, especially near the solder interconnects. Voids are caused by air pockets being trapped between the chip and substrate as the underfill is dispensed. Voiding can be minimized by optimizing the dispense process. Lowering the viscosity of the underfill material improves the flow capabilities of the underfill and helps to minimize the occurrence of voids.

3.6 Flip Chip Adhesion

The majority of my work during the internship was focused on determining how process variation can impact flip chip adhesion. The term adhesion refers to the interaction between the closely contiguous surfaces of adjacent bodies, e.g., underfill and die passivation. According to the American Society for Testing Materials (ASTM), adhesion is defined as the condition in which two surfaces are held together by valence forces or by mechanical anchoring or by both together.[10]

The adsorption theory is the most generally accepted of the adhesion theories. Adsorption suggests that if there is sufficient contact at the interface between two materials, the surfaces will adhere because of the pairwise interaction of the involved atoms or molecules. It is believed that the largest contributor to the overall adhesion energy is that of van der Waals forces. In addition to van der Waals forces, chemical interactions also contribute to adhesion. These consist of stronger bonds such as ionic, covalent and metallic binding forces.

Adhesion is a critical property, but it is not well understood. Typically, measurements of adhesion can only be assessed experimentally. The experimental evaluation of adhesion is non-trivial since it consists of contributions from several distinct mechanisms. There are at least four types of interfaces that can be distinguished: abrupt interface, compound interface, diffusion interface and mechanical interlocking.[10] Bonding energy is a function of the physical characteristics of the materials that make up the interface as well as environmental conditions. Any modification or change of the

material set or process history is likely to alter the bonding strength as well as the residual stresses remaining in the interface.[9]

3.6.1 Shear Stresses

During temperature cycling, the flip chip package is subjected to sheer stresses at the underfill/die interface and underfill/substrate interface. Adhesion of the underfill material to the underside of the die surface and to the substrate is critical to the reliability of the flip chip assembly. These interfaces must be able to withstand the shear stresses that they are subjected to under even the most extreme operating conditions. The typical failure mode observed in a flip chip assembly is delamination of the underfill to the chip interface.[11] Once adhesion between these two surfaces is lost, the flip chip solder joints are directly subjected to the strain resulting from the thermal mismatch between the die and the board. Electrical failure will most definitely occur as a result of the solder fatigue cracking, which occurs shortly after the delamination.

3.6.2 Distance from Neutral Point (DNP)

As the industry designs chips with more functions, the size of the chips are increasing. Increasing the size of the chip increases the Distance from Neutral Point (DNP). DNP is defined as the distance from the furthest, functional solder bump to the neutral point on the chip. The neutral point or geometric center of the solder bumps remains stationary relative to the substrate during thermal cycling. The DNP is usually a corner bump. As the DNP increases, the stress borne by the bump increases when it is constrained in a flip chip package. Scanning Acoustic Microscopy (SAM) studies have revealed that delamination occurs initially around the outer perimeter of the chip. Within a short time the delamination proceeds inward toward the center of the chip.[11]

4. Supplier Material Processes

Three materials that are considered critical to flip chip adhesion were included in the scope of the internship study. These materials are underfill, solder mask and die passivation. One or more suppliers supply each material to Delphi Delco Electronics Systems (DDES). Because I needed to determine how process variation in the manufacture of each of these materials could adversely affect flip chip adhesion, it was necessary to study each vendor's process. Some of the key areas that were looked at included the process flows, the process control plans and the key process parameters that could potentially degrade flip chip adhesion. This chapter provides the reader with pertinent information regarding the processing of each of these materials as well as the key parameters that could affect adhesion strength of the flip chip package. Because the underfill is the most important material in the flip chip system, I will focus on the underfill material more so than the solder mask or die passivation.

4.1 Underfill

The innovation and application of an underfill encapsulant to the flip chip on laminate system provided a realistic solution to the CTE mismatch between the silicon die and laminate substrate. The underfill consists of an anhydride-cured, epoxy resin, which is filled with silica particles. Epoxies are used as the resin for underfill applications because in general they exhibit the following characteristics.[12]

- Epoxies exhibit good wetting of and adhesion to the passivation and solder mask.
- Epoxies have relatively low shrinkage during the cure.
- They offer good corrosion resistance.
- Epoxies have relatively high moduli, particularly when the glass transition temperature, T_g, is relatively high. T_g for underfill is in the range of 130-165°C, so test/operating temperatures are below T_g.
- They have viscosities consistent with good flow from the syringe at 25°C and between the die and substrate at temperatures consistent with the assembly materials (typically the substrate is heated to about 75°C).
- Epoxies can be cured with a simple thermal schedule (curing ranges are from 110-170°C for 30-120 minutes).
- They are relatively inexpensive as compared with other polymer resin materials.

4.1.1 Desired Material Properties

Table 2 lists the material properties and ranges of values for underfill. Because underfill is such a complex material, in many cases there can be quite a large range for any given property. The key is to optimize the set of material properties for the specific application and types of flip chips that are utilized.

Material Property	Property Range
Modulus	>9 Gpa
Viscosity	6-10 Pa-s at room temperature and 0.4-0.8 Pa-s at 70 °C.
Coefficient of Thermal Expansion (CTE)	20-25 ppm/°C
Glass Transition Temperature (T_g)	140-180°C
Cure Temperature and Schedule	1-2 hours at a cure temperature of 130-160 °C
Wetting	Measured by Contact Angle (higher angle indicates more wetting)
Shrinkage Upon Cure	Minimal shrinkage
Moisture Absorption	< 1% after 72 hours
Filler Size and Content	< 1.5 mil, 65-75% weight content
Shelf Life and Pot Life	Shelf life: 6 months at -40°C, Pot life: 16 hours

Table 2 - Desired Properties of Underfill Material[12]

Modulus

A relatively high modulus is desired since the value of the underfill relates to its ability to limit the strain on the solder joint resulting from thermal cycling stresses. The silicon die, solder, and substrate have moduli of 155 GPa, 13 GPa, and 13.8 GPa, respectively. Desired underfill modulus is generally described as >9 GPa – still well below that of silicon but perhaps on the order of the best achievable for the current materials.

Viscosity

Viscosity of the underfill material is an indicator of the flow of the material. Viscosity will increase as the material ages, since the material begins to cure once it is exposed to room temperature. The flow of the material can be improved by increasing the temperature of the material while dispensing, which will initially lower the viscosity and allow for faster flow. However, this must be weighed against the reduced time until the material begins to gel. While the viscosity of the material determines the flow of the underfill to a large extent, the desired flow cannot be obtained by specifying the viscosity alone. The flow rate as a function of time depends on various properties of the material such as viscosity, temperature, surface tension, gel time, stand-off height and the wettability. The viscosity of the underfill at the dispense temperature must also be consistent with the syringe dispensing methods since a blocked syringe or uneven dispensing will result in an insufficient or unreliable amount of underfill being dispensed. Values of the desired viscosity can vary, but a typical range is 6-10 Pa-s at room temperature and .4-.8 Pa-s at 70 °C.

Coefficient of Thermal Expansion

Filler is mixed into the resin to lower the CTE of the underfill, since the epoxy resin by itself has a CTE of about 70 ppm/°C. Ideally, the underfill should have a CTE that closely matches the CTE of the solder alloy and FR-4 substrate, both of which are in the 20-25 ppm/°C range. The filler material is usually a silica particle, which has a CTE of about 0.5 ppm/°C. In order to achieve the desired CTE of 20-25

ppm/°C, the percent weight of silica in the underfill is in the 65%-75% range. The viscosity of the material is increased substantially with the filler added to it, and as such there is an important tradeoff between CTE and viscosity (lower viscosities flow better). The effect of filler content on underfill CTE and viscosity is illustrated in Figure 10.[4]

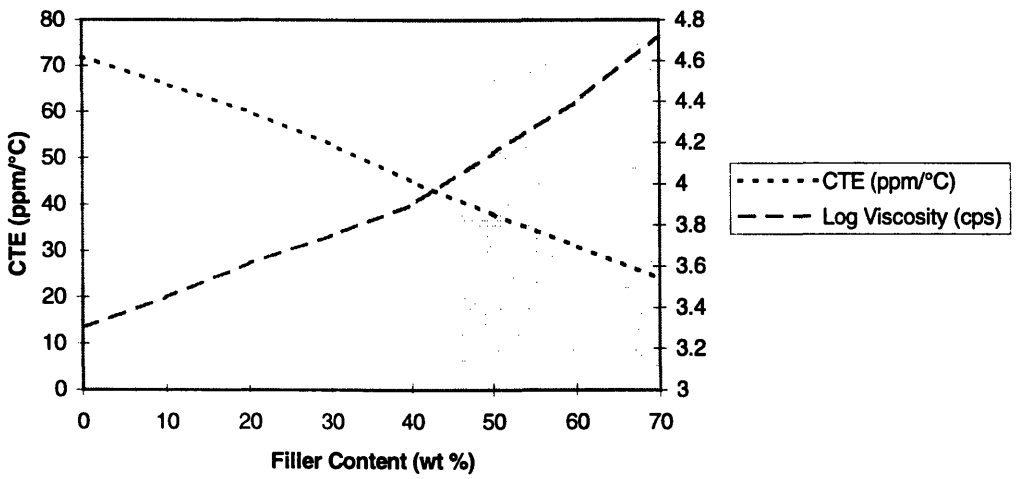

Figure 10 - Effect of Filler Content on Viscosity and CTE

Glass Transition Temperature T_g

The T_g is the temperature at which the underfill changes from the glassy, or hard and brittle state, to a much softer polymer. It is an indication of the level of formulation of the polymeric network and cross-link density, and ultimately the degree of cure.[4] The T_g is a very sensitive index of the degree of cure, especially during the last 10% of the curing reaction. Above and below the T_g the CTE, adhesion strength, electrical properties and other important physical properties may

vary dramatically. The T_g temperature should be within the range of 140-180°C to achieve the desired material properties.

Cure Temperature and Schedule

A complete cure is essential for obtaining optimal and predictable underfill properties. The degree of cure will have direct impact on the underfill performance, particularly on moisture sensitivity as well as fracture toughness. However the time and temperature of the cure must be weighed against the desire to reduce the cycle time and thus increase the productivity of the manufacturing process. Curing times of 30 minutes or less are desirable, but current materials require curing of 1-2 hours at a cure temperature of 130-160 °C. Using a catalyst material will decrease the curing time. However, the use of a catalyst reduces the pot life, which must be weighed against the desire for shorter cure cycle.

Wetting

Good wetting of the substrate is very important for an underfill material since better wetting increases the capillary driving force that pulls the underfill under the chip. It also increases the speed at which the underfill is pulled under the chip since the capillary flow rate is proportional to the wetting rate[13], which is approximated by:

$$dl/dt = r\,\gamma_{LV} \cos\theta / 4\,\eta\, l$$

- where l is the distance traveled in the capillary, or for our approximation, under the chip
- r is the radius, or in this case, the stand-off height between the chip and substrate
- γ_{LV} is the liquid (epoxy) - vapor (air) surface tension
- θ is the wetting angle
- η is the viscosity of the epoxy.

Thus, ideally the underfill material would wet substrate, die, and solder perfectly. Wetting of the solder is expected to be somewhat less crucial since the solder/underfill interface is not subjected to significant stress whereas the

underfill/chip interface and underfill/mask interface are expected to bear the brunt of such stress.

The flow behavior is of utmost importance for the performance of the underfill since if there are voids or defects in the underfill, the stress-relieving properties will be severely compromised.

Shrinkage upon Cure

Low shrinkage upon curing is important because having filled the space between the chip and the substrate, underfill shrinkage would put the underfill itself in tension. This would stress the interfaces and could result in void formation. Ideally the filled epoxy does not shrink at all upon curing. However, some shrinkage is to be expected and the goal is to minimize the amount of shrinkage.

Moisture Absorption

The underfill, in addition to a mechanical function, also serves an encapsulant function for the die. Thus, low water absorption by the polymer is necessary because a water path, in combination with mobile ions (such as Cl^-) and an applied field, can result in significant electrocorrosion. For this reason it is also very important to have very low mobile ion concentrations in the epoxy (generally specified as less than 20 ppm, with lower levels being desirable). Additionally, moisture absorption can lead to degradation in the adhesion capabilities of the underfill. Ideally, no water is absorbed and no mobile ions are present. However, moisture absorption has been specified to be less than 1% after 72 hours of steam aging in a pressure cooker test.[4]

Filler Size and Content

The particle size of the filler must also be considered. If the particles are too large relative to the stand-off height (which is the gap between the die and substrate), the filler could impede underfill flow. Stand-off heights are typically about 75 μm. Conversely, if the particle size is too small, the filler may tend to settle in the underfill resulting in an inhomogeneous underfill that effectively becomes two types of

material. It is also more difficult to disperse smaller particles into the resin because of the increased surface area that must be wetted out. In general, good results are achieved when filler diameters are somewhat less than half that of the stand-off height, or less than about 30 μm. As was stated earlier, in order to achieve the desired CTE of 20-25 ppm/°C, the percent weight of silica in the underfill is in the 65%-75% range.

Shelf Life and Pot Life

Shelf life is defined as the amount of time that the material can be stored before use. Because underfill is a one-component system, it must be stored frozen to inhibit curing. A typical storage temperature is -40°C. Maximum shelf life is typically specified to be 6 months at -40°C. Once the underfill is thawed for use, the pot life (or working life) is defined as the amount of time the underfill can sit at room temperature before it should be discarded. The typical pot life is 16 hours. Viscosity increases at room temperature as a function of time. Once the underfill has been exposed to room temperature for 16 hours, the viscosity of the material begins to increase due to the material beginning to slowly cure.

4.1.2 Process Flow & Key Process Parameters

While each supplier of underfill has its own unique process and "recipe" for making underfill, there is a general process for mixing underfill that most manufacturers will follow. Figure 11 depicts a standard process flow. For each process step, there are one or more Key Process Parameters that must be specified, with tolerances, to ensure that the material will meet the specified quality requirements and material properties. Many of these key parameters were varied and tested by DDES's underfill supplier to gauge the impacts on adhesion.

4.1.3 Key Process Parameters for Underfill

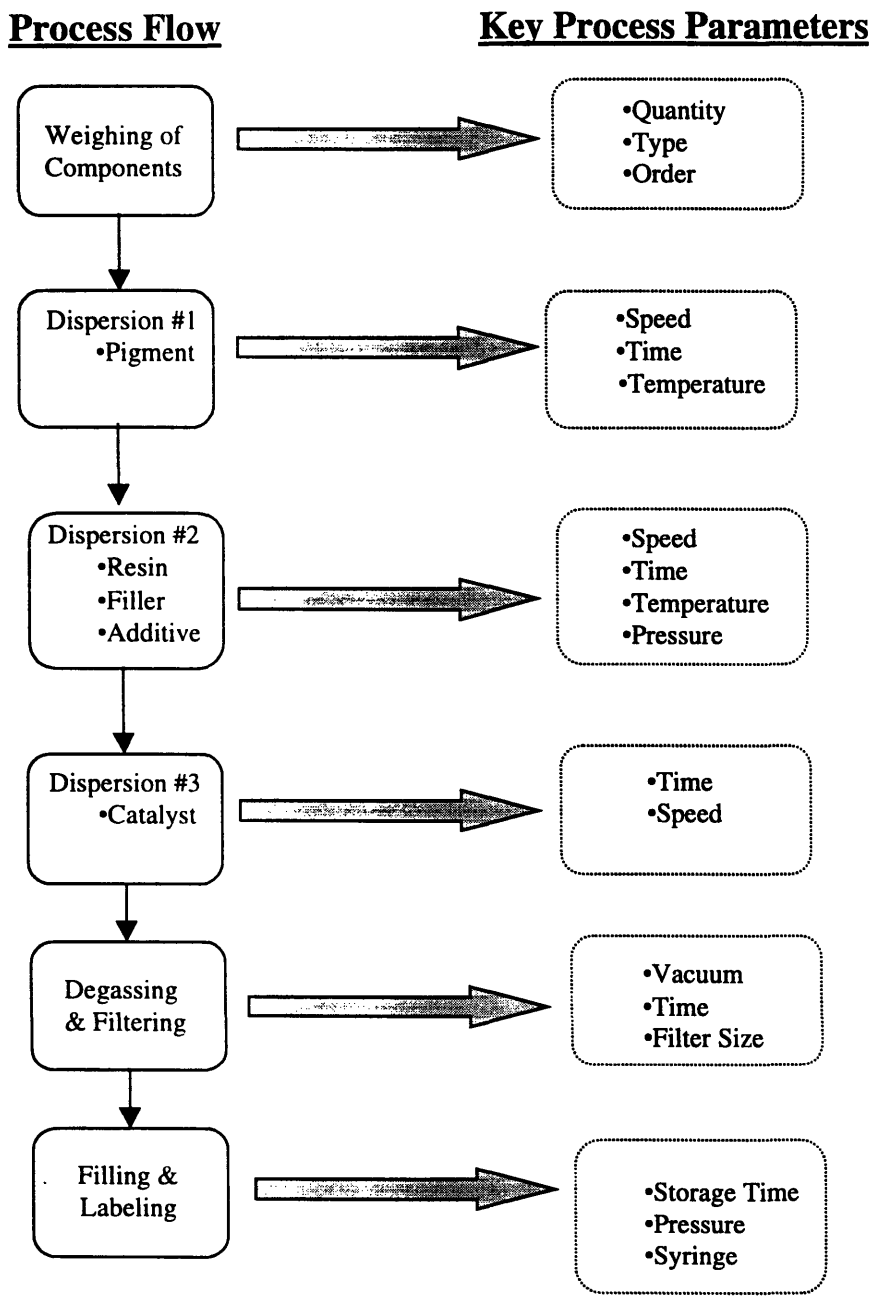

Figure 11 - Underfill Process Flow and Key Process Parameters

4.2 Solder Mask

Solder mask (also known as solder resist) is the outermost layer of material on the printed circuit board. Consequently, there must be a compatible chemistry between the solder mask and underfill for good adhesion at the interface. Solder mask is applied to the entire PCB surface, except for solder or contact lands, to both prevent solder wetting during the assembly process and to provide protection from environmental damage after assembly.[8] As with underfill, each manufacturer of the solder mask has its own process and material "recipe". Solder mask is made in both the liquid and dry form, although liquid, screen printed film is the type most commonly used and will be the process examined in this thesis.

There are two major steps in the application of solder mask. The first step is the actual mixing of the material. Liquid solder mask consists of an epoxy resin with inorganic fillers mixed in. The inorganic fillers serve two purposes. Since this material is screen printed, it needs to be thixotropic. This means that the velocity of the material decreases as the shear force applied increases. Secondly, inorganic fillers help to achieve a matte surface so that solder balls do not adhere to the material. Solvents are also added to the solder mask to control viscosity.

The second major step of the solder mask process is the application of the material onto the circuit board. This can be done in several ways, including screen printing, curtain coating and spray coating. Because screen printing is the method utilized by DDES's supplier, that process will be the only examined in this thesis. Complicating the study of supplier process variation for solder mask is the fact that the mask is mixed at one supplier and then sent to a completely different circuit board supplier for application. Consequently, there are two completely separate processes that have to be examined. Figure 12 depicts the process flow and key process parameters for the mixing of the solder mask. Figure 13 depicts the process flow and key process parameters for the screen printing of the solder mask onto the substrate.

4.2.1 Mask Mixing Process Flow and Key Parameters

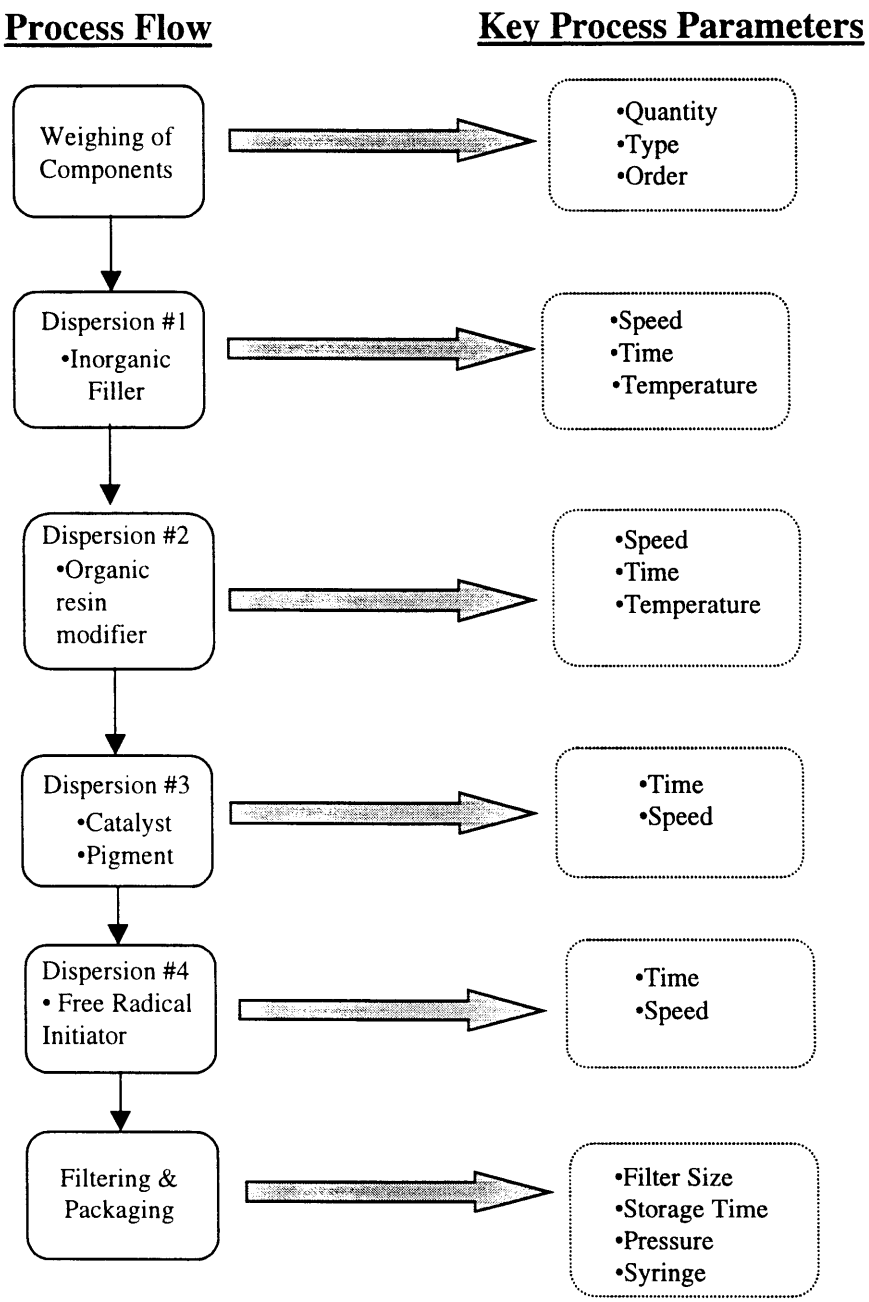

Figure 12 - Solder Mask Manufacture Process Flow and Key Process Parameters

4.2.2 Solder Mask Application Process Flow and Key Parameters

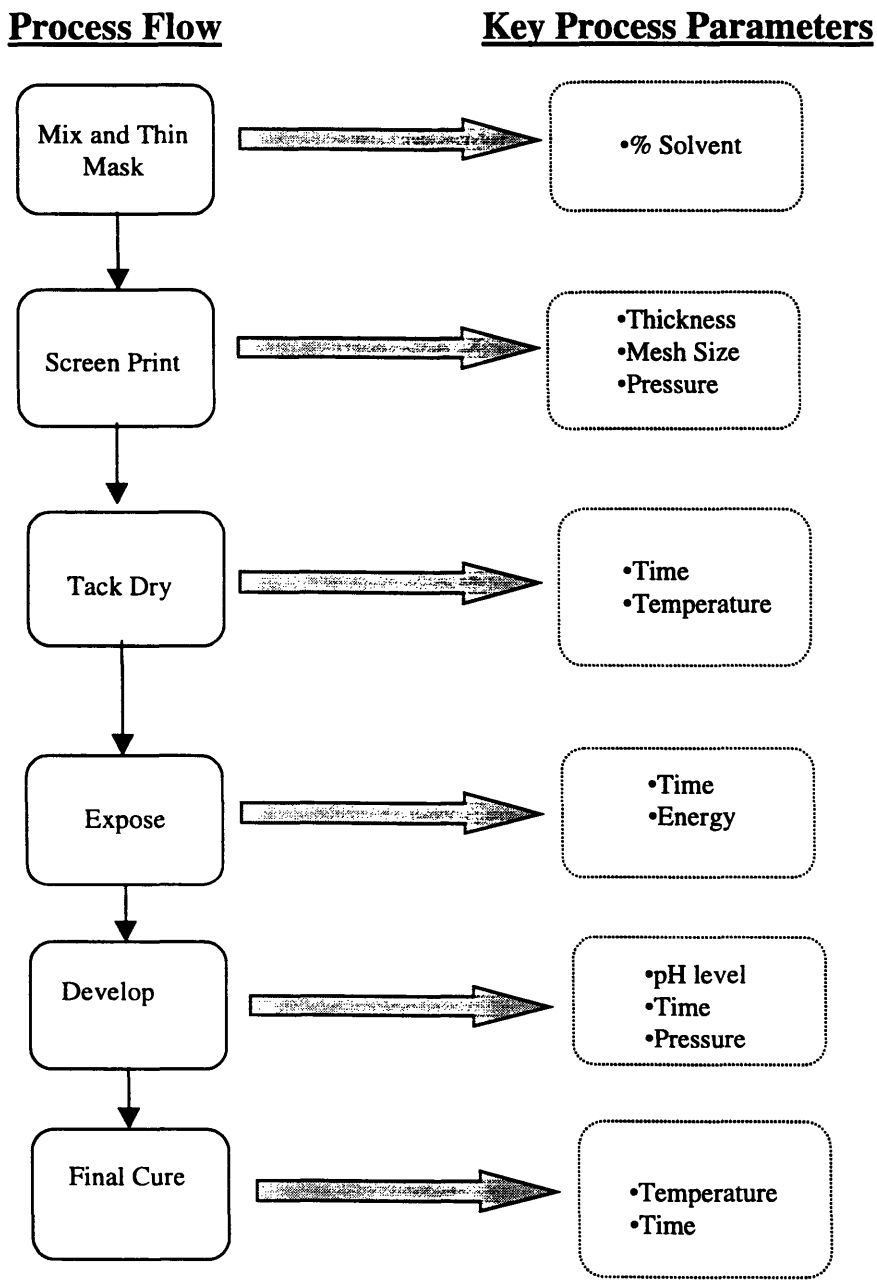

Figure 13 - Solder Mask Application Process Flow and Key Process Parameters

4.3 Passivation

Passivation is equally as important to the adhesion of the flip chip package as solder mask is in the flip chip system. As with the underfill/solder mask interface, there must also be a compatible chemistry between the underfill and passivation to ensure good adhesion at the interface. Passivation consists of a layer of protective film that coats the final metal and chip. The passivation type and deposition method will vary with the chip technology and semiconductor fab facility. There were two primary passivation types that were examined during the course of the internship: silicon nitride and polyimide.

4.3.1 Silicon Nitride

Silicon nitride is one of the most common materials used for die passivation. Because semiconductors cannot tolerate temperatures in excess of 300°C at the passivation stage, the silicon nitride is deposited by using a plasma enhanced chemical vapor deposition process (PECVD). In PECVD processes, glow discharge plasmas are sustained within chambers where simultaneous CVD reactions occur.[10] PECVD is done in a reduced pressure environment. The concept behind PECVD is that techniques other than thermal techniques can be used to bring about the appropriate reactions.

4.3.2 Polyimide

Some IC suppliers have begun using an additional layer of protection in the form of polyimide. Polyimides offer good thermal stability, good planarization capability, and low permittivity.[14] The main role of polyimide is to protect the underlying passivation during the subsequent bumping, probe and assembly processes, as well during the subsequent operation of the IC. The polyimide must have excellent adhesion to the passivation, the underfill and the pad limiting metallization.[15] The polyimide must also have excellent adhesion to the underfill, since failure analysis shows that typical failures of the flip chip systems are due to crack propagation at the underfill/polyimide interface.

Polyimide can be processed using standard IC processing equipment. It can be applied with standard photoresist spinning equipment and can be patterned using

photolithography. Polyimide can be cured in a tube furnace of the type used for oxidation or diffusion.[14]

4.3.3 Passivation Key Process Parameters

There are relatively few process parameters that can be controlled with the deposition of the passivation or polyimide, at least as compared with the underfill and solder mask. For silicon nitride, the two main processing parameters are thickness and stress. Stress is used to indicate the thin film stress of the material, which is nitride in this case. The nitride will either be in tension or compression. However, nonmetals, such as silicon, are brittle materials and must be in a state of compression and are best deposited in this manner. The stress measurement is used to determine how well the nitride will adhere to underlying material and is used in determining the stochiometry of the material. Thickness also plays a role in determining the stress measurement. Generally speaking, thicker films will result in higher internal stress concentrations on the film. Composition also is a key product characteristic that can be measured by the refractive index. Typically, refractive indices should be around 2 for silicon nitrides. However, refractive index is difficult to control directly.

With polyimide, there are also several key process parameters that could have an impact on adhesion. One of the key areas of concern with using polyimide in flip chip applications is that polyimide absorbs moisture. As a result, the cure schedule plays a vital role in the moisture uptake of the polyimide and the subsequent adhesion capability of the material. The cure time and temperature profile should be optimized for the flip chip application. The moisture uptake should be no more than 2% of the volume. Additionally, the ability to apply layers that are free of pinholes and thicker than those obtainable with silicon nitride passivation are parameters that could be important.[14]

5. Experiments and Data Collection

A test method termed Die Shear Testing was the primary means for performing the adhesion studies for this research. Shear tests are performed in a horizontal attitude with a shear force applied to the edge of the die until the die shears completely from either the underfill or solder mask. The force necessary to shear the die from either the underfill or the solder mask is recorded and used to calculate the pounds/square inch measurements. Figure 14 displays a schematic of the tool as it was setup.

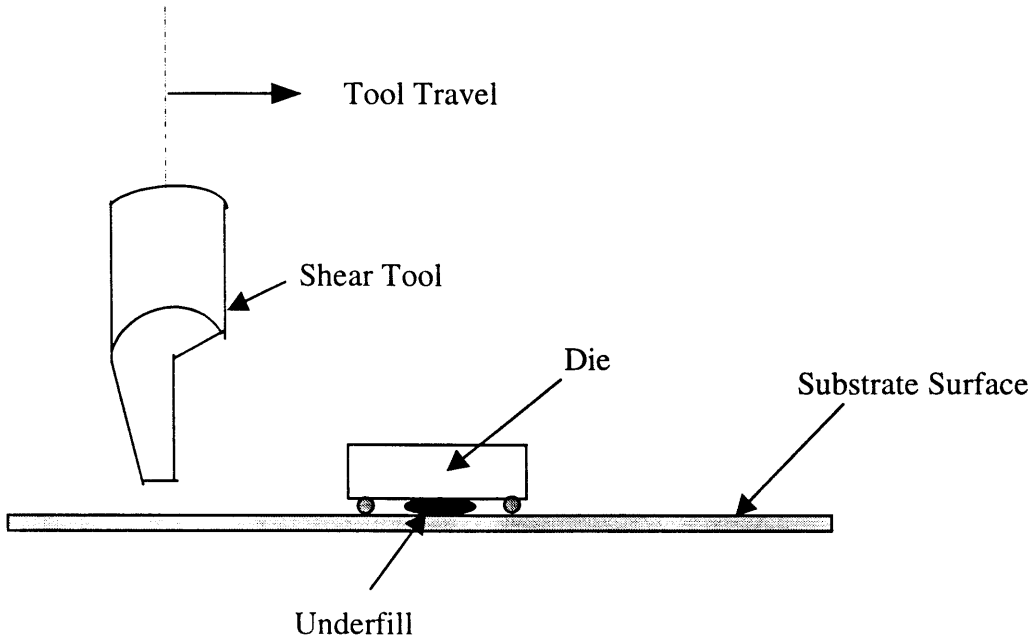

Figure 14 – Side View of Die Shear Tool

5.1 Description of Test Method

5.1.1 Test Equipment

A microprocessor controlled testing device was used for measuring the adhesion strength of the die/underfill interface or the solder mask/underfill interface. The shear tool travels at .26 mm/sec, which is an A.S.T.M specification. As the tip of the shear tool contacts the edge of the die, a pivot transmits the contact force, of the shear tool against the die, to an input plunger of a force transducer. The resulting output signal from the force transducer is transmitted to the microprocessor. This output signal is compared to the force and stroke limit data that was preset. (In this case, a 100-kg shear force was the maximum allowable force, and the maximum distance the shear tool could travel was set to 30 mils). When the output signal reaches either the defined applied force or stroke limit, the test stops. Since die shear testing is a destructive test, the stroke limit was the controlling input signal.

5.1.2 Test Procedure

Figure 15 shows schematics of a solder mask coupon populated with test. All of the tests that were performed during the internship utilized the same general procedure, which is described below.

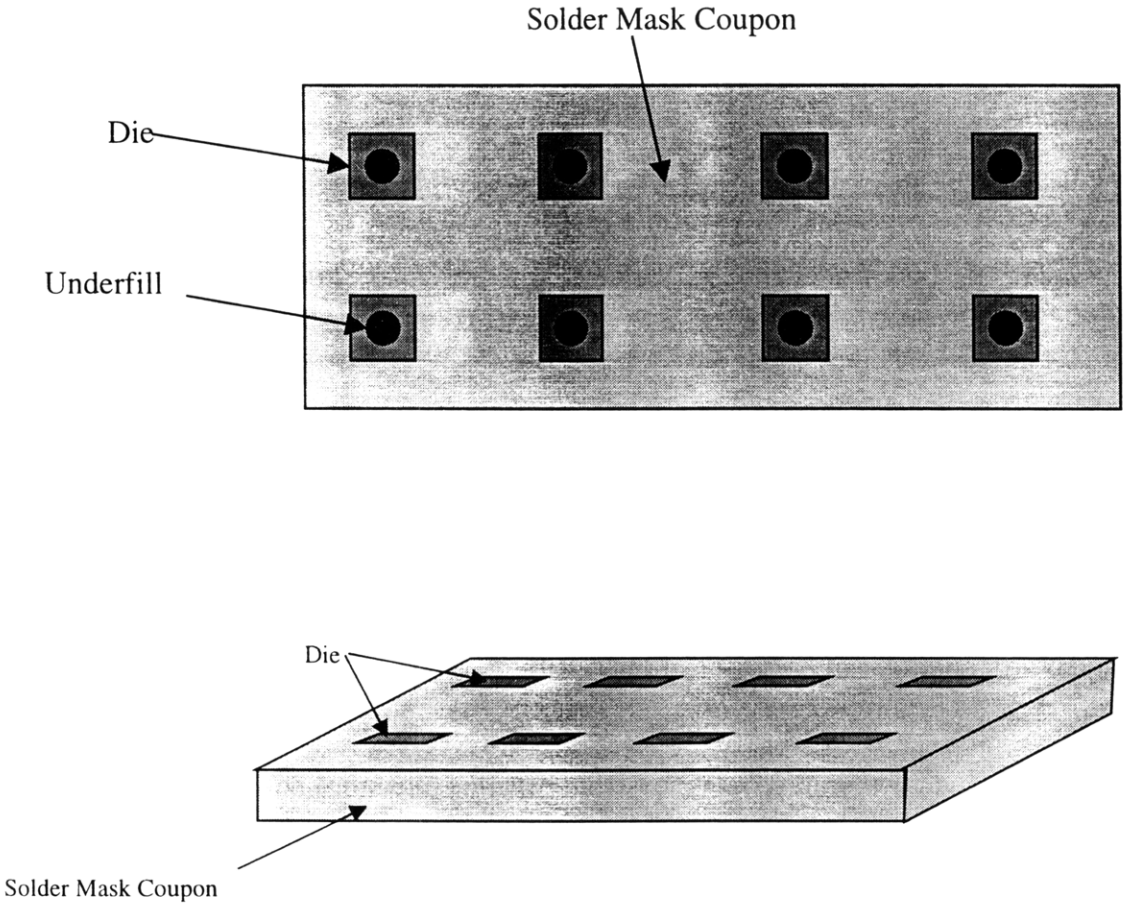

Figure 15 – Top and Side Views of Sample Populated Test Coupon

1. Place a bumped silicon die upside down on a substrate surface. The substrate consisted of a 2" x 1" laminate coated with solder mask. A maximum of eight dice was put onto the coupon.
2. Syringe a small drop of underfill epoxy onto the die surface of each die. The amount of underfill placed onto die chip was not controlled. As a result, there were varying amounts of material put onto each die.
3. Flip the die back over and place onto the substrate surface.
4. Cure the underfill epoxy for 2 hours at 150°C.
5. Shear the die off using the die shear tester described in the previous section and record the force required for shearing.
6. Measure the diameter of the failed interface using a magnified x-y grid table and a digital measuring system. Calculate the area of the failed interface. The area is slightly different for each die since the amount of underfill varies.
7. Calculate the force per unit area.

5.2 Design Methodology

The tests and data analysis that were performed differed somewhat for each of the three materials. However, all the tests were done by comparing the adhesion strength of a standard, or control, sample to one or more variations of the control. Data analysis was performed using Analysis of Variance (ANOVA) techniques. ANOVA is a statistical method in which two or more treatments can be compared. One of the most common uses of ANOVA is to compare the treatment means or averages. The null hypothesis is that the treatment means are equal. Only when treatment means are statistically different can we say for certain that the treatment means are in fact different.

Two key aspects of ANOVA are randomization and blocking. Randomization is the process of allocating treatments randomly to the experimental units. It is necessary to insure that the risk of unspecified disturbances is spread evenly among the treatments. If randomization is not utilized, a confounding of treatments with other variables could occur.

Blocking is utilized to eliminate unwanted sources of variation or when two or more factors are confounded. Factors that that can affect the response but which are not of main interest are referred to as the blocking variables. In the experiments done for

these studies, blocking was often used to eliminate sources of variation with the solder mask coupons. For example, suppose all samples of underfill sample #1 are tested using solder mask coupon A, and all samples of underfill sample #2 are tested using solder mask coupon B. If there are differences in the mean adhesion strength, the reason could either be attributed to the underfill type or the solder mask coupon. It would be difficult to discern the true cause of the differences. The two factors, underfill type and solder mask coupon, are confounded. A better experiment would be to split the two underfill types among the two different solder mask coupons so that the variation associated with the solder mask coupon can be measured and accounted for.

Two of the underlying assumptions with ANOVA are that the distributions of responses are normally distributed and that the variances are the same for all of the treatment groups. In the experiments conducted for this study, these assumptions hold. A description of the design methodology follows for each material.

5.2.1 Underfill

5.2.1.1 Underfill Supplier Results

The underfill supplier, whom I will refer to as US, had completed extensive process variation experimentation prior to the start of the internship. To perform the experiments, US did the following.

- Determined all of the process or product parameters that could potentially have an effect on the adhesion of the underfill to either the mask or die passivation. For example, one process parameter that was evaluated was the time to disperse the filler into the resin.

- For each of those process parameters, US manufactured three samples of material. The first sample was made at the correct specification. This sample was referred to as the standard. (In the example this would be the specified time to disperse the filler). The second sample was made at a level below that of the specification. (In the example, the time to disperse the filler was decreased by 50%). The third

specification was made at a level above that of the specification. (In the example, the time to disperse the filler was increased by 50%).

- US then used each group of samples in adhesion strength tests. The adhesion strength of the standard material was compared to the variants for each group.

Table 3 is the summary of the results that US reported to DDES. In almost all cases, US reported that there was no degradation in adhesion strength. Those cases in which there was degradation are highlighted in Table 3. Looking at this table, the material would appear very robust to quite large variation in almost all of the process parameters. Of course, in reality the underfill supplier would not be able to allow for such wide tolerances in the process parameters. There are many other material properties, such as modulus, CTE and glass transition temperature, that must lie within a tightly specified range in order for the underfill material to function properly. These material properties would surely be altered with such large variations in process parameters as those listed in Table 3.

Process	Parameter	Variation in Parameter				
Weighing		-50%	-10%	Standard	+10%	+50%
	Epoxy Resin	***60***	100	100	100	***80***
	Anhydride	***60***	100	100	100	***80***
	Filler	100	100	100	100	100
	Catalyst	***50***	100	100	100	***100***
	Additives	100	100	100	100	100
Drying of Filler		No Dry	Standard	+50%	+100%	
	Time	100	100	100	100	
Pre-mixing		No Premixing	Standard	+100%		
	Time	100	100	100		
Dispersion 1 (Pigment)		No Dispersion	Standard	+100%		
	Time	100	100	100		
Dispersion 2 (Filler)		-20%	Standard	+20%		
	Temperature	100	100	100		
	RPM	100	100	100		
	Time	100	100	100		
Dispersion 3 (Catalyst)		-20%	Standard	+20%		
	Temperature	100	100	100		
	RPM	100	100	100		
	Time	100	100	100		
Transferring		-50%	Standard	+50%		
	Time	100	100	100		
Degassing		-50%	Standard	+50%		
	Time	100	100	100		
Filling of Syringes		-50%	Standard	+50%		
	Time	100	100	100		
Storage		At Time = 0	At Time = 6 Months			
	Time	100	100			

Table 3 - Summary of Data Reported by Underfill Supplier

5.2.1.2 Duplication of Underfill Results

The underfill supplier, US, had done extensive testing of the adhesion capabilities of the underfill material prior to the internship. Using the data that US reported to DDES, I attempted to duplicate and verify the results that US obtained from its testing. Seven different process and product parameters were chosen, which are as follows:

1. Sample 1: -10% Catalyst
2. Sample 2: -50% Catalyst
3. Sample 3: -10% Anhydride
4. Sample 4: -50% Anhydride
5. Sample 5: No Dispersion of Pigment
6. Sample 6: -20% Time for Filler Dispersion
7. Sample 7: +50% Time for Filling Process
8. Sample 8: Control/Standard Material

Only 7 samples were selected because there were significant costs associated with making and testing each unique sample of material. As can be seen from Table 3, I would expect samples #2 and #4 to provide less than 100% of the adhesion strength of the standard material, while the other 5 samples should show no loss in adhesion strength as compared to the control sample's adhesion strength.

US made each of these underfill variants, along with a control sample. The test procedure described in Section 5.1.2 was used to build and test the experimental samples. A complete 8 X 8 blocked experiment was conducted. The solder mask coupon served as the blocking factor. The seven variant underfills, along with the control underfill, were randomly applied to the sample die and sample solder mask coupons. All of the solder mask coupons were built and cured at the same time to eliminate potential variation in environmental conditions, time and temperature of cure.

5.2.2 Solder Mask

For the solder mask material there were three process parameters that were tested. These parameters were deemed key variables in the manufacture of the solder mask. In doing the solder mask testing, I was examining to what extent there was adhesion degradation as the level of each parameter varied. The three process parameters were:

1. Photoinitiator
2. Photopolymer
3. Filler

For each of the three parameters, there were three levels manufactured: the standard (or specified) level, -10% of the standard, and +10% of the standard. Table 4 displays the matrix of tests that were performed.

Parameter	*-10%*	*Specified Level*	*+10%*	*Control*
Photoinitiator	2 Coupons	2 Coupons	2 Coupons	1 Coupon
Photopolymer	2 Coupons	2 Coupons	2 Coupons	1 Coupon
Filler	2 Coupons	2 Coupons	2 Coupons	1 Coupon

Table 4 - Solder Mask Test Matrix

As with the underfill, the testing procedure described in Section 5.1.2 was utilized to determine the adhesion strength of each variant material as compared to the standard. Additionally, a control solder mask was used as a comparison in the testing. This control material is the solder mask that is manufactured in the full-scale production plant. All of the other samples that were prepared for this experiment were made in the lab on a much smaller scale.

The die were randomly assigned to each of the different solder mask coupons. The underfill material (which was the standard material specified for production) was held constant for all of the mask experiments. All of the testing for each parameter was

done on the same day to eliminate potential variation with environmental conditions and time and temperature of underfill cure.

Because of some difficulties encountered in getting supplier cooperation, no analysis of mask application parameters was performed during the internship. However, there are several key parameters at the mask application stage that should be tested to determine adhesion strength sensitivity to process variation. These recommendations will be discussed in further detail in Chapter 7.

5.2.3 Die Passivation

Neither the internal nor the external die supplier was able to accommodate my requests for a process variation study. As a result, the supervisor for this project suggested that an analysis of adhesion strength from lot to lot might provide some leverage to persuade the die suppliers to comply with our requests. The reasoning was that if I did discover significant variation in the adhesion strength of the die passivation in different lots of the same chip, then that would provide some hard data to justify a complete process variation study on the deposition of the die passivation (as well as the subsequent bumping processes).

To perform the die passivation tests, I requested 2-4 lots of various chip types with 6-8 die per lot. I received 3 different chip types, Chip A, B, and C. Table 5 shows a matrix of the quantities and lots of chips that I received. Again, as with the underfill and solder mask, the die shear test described in Section 5.1.2 was utilized to compare the relative die passivation adhesion strength among the different lots of each chip type. Since each chip type was different from the others, a comparison of the adhesion strengths between chip types was not undertaken.

Attribute	Chip A	Chip B	Chip C
# of Lots/Wafers Tested	4	2	2
Sample Size per Lot/Wafer	8	6	8
Lot/Wafer	Lot	Lot	Wafer

Table 5 - Die Test Matrix

A blocked experiment was performed for each chip type. The solder mask coupons served as the blocking variable. The die from each lot were randomly assigned to the different solder mask coupons. The underfill material (which is the standard material specified for production) was held constant. All experiments for each chip type were performed on the same day to eliminate potential variation with environmental conditions and time and temperature of underfill cure.

5.3 Data Analysis

As was stated in Section 5.2, ANOVA and the students t-test were used for all of the experiments to determine which variants were statistically different from the control materials. The null hypothesis is that the treatment mean for the control sample is equal to the mean for the variant sample. The data was input into spreadsheets in Microsoft Excel and the data analysis tools within Excel were used to obtain the results. Appendices A, B and C contain all of the raw data, which is the basis for the summaries below.

5.3.1 Underfill Data Analysis

Table 6 shows the summary of the results from the underfill experiment. For each sample, there is a comparison of the data that US reported to DDES with the data that was obtained from my experiment. There is very good correlation between the supplier's results and my results. Neither US nor I found any statistical difference in adhesion strengths for samples #1, #3, #4, #5, #6 and #7. However, both US and I found statistically significant differences in adhesion strengths for samples #2 and #4.

	Standard	Sample 1	***Sample 2***	Sample 3	***Sample 4***	Sample 5	Sample 6	Sample 7
Mean (PSI)	9414	9280	***8103***	9444	***8289***	9440	9381	9404
P-value		0.24790	***0.00013***	0.42723	***0.00229***	0.42379	0.42155	0.47392
% of Control		99%	***86%***	100%	***88%***	100%	100%	100%
Supplier Data (measured as a % of standard material)		100%	***50%***	100%	***60%***	100%	100%	100%

Table 6 - Underfill Test Results and Comparison with Supplier Data

The p-values in Table 6 show that sample's #2 and #4 are significantly below the alpha level of .05. Because I am using eight different samples, I could have divided alpha by a factor of 8 to obtain an alpha of .00625. However, this would not change the outcome of the experiment. Samples #2 and #4 would still be statistically different from the control material. Because I obtained identical results with the data provided to DDES from US, there is increased confidence and assurance on the part of DDES that, in fact, the underfill material can withstand slight variations in process parameters without a loss of adhesion strength.

5.3.2 Solder Mask Data Analysis

Table 7 shows the results of the testing that was performed on the solder mask. As can be seen from the table, there were some dramatic decreases in adhesion strength when several of the variables were altered from the specified level. Specifically, the following observations are worth noting.

Component	Nominal Value (Standard material produced in Supplier's Lab)	+ 10% of Standard (produced in Supplier's Lab)	-10% of Standard (produced in Supplier's Lab)	Control (mask which was produced in Supplier's main production area)
Photo Initiator *(% decrease from nominal)*	3013	1884 37.47%	2286 24.13%	1770 41.25%
Filler *(% decrease from nominal)*	3092	2992 3.23%	2946 4.72%	2642 14.55%
Photo Polymer *(% decrease from nominal)*	3121	1797 42.42%	3168 -1.51%	1804 42.20%

Table 7 - Solder Mask Test Results (data in psi)

- When the level of photoinitiator was altered, either by increasing or decreasing the amount by 10%, the adhesion strengths were reduced substantially. The actual tolerances at the supplier are an order of magnitude less than 10%, however any change in photoinitiator may warrant further investigation.
- When the level of filler was increased, there was no statistically significant reduction in adhesion strength. However, when the amount of filler was decreased, the adhesion strength was reduced substantially.
- Neither increasing nor decreasing the level of photopolymer resulted in any statistical degradation of adhesion strength.
- Additionally, another interesting observation of this data is that the control material, which is manufactured in the plant, exhibited much lower adhesion strength than the nominal material that was manufactured in the lab. In two of the cases the control material's adhesion strength was more than 40% lower than the nominal material produced in the lab. This may indicate that there are additional process parameters, such as mixing speed, and blade type, that may

have some impact on the material properties. These recommendations for further study will be covered in detail in Chapter 7.

5.3.3 Die Passivation Data Analysis

Table 8, Table 9 and Table 10 show the results of the testing that was performed on the die passivation. As was mentioned earlier, three different chips were tested. The data analysis for each chip is included below.

5.3.3.1 Chip A

Chip A (sample size = 8)	Lot 1	Lot 2	Lot 3	Lot 4
Mean Adhesion Strength (psi)	7896	8911	8280	9002

Table 8 - Chip A Test Results

There were four lots that were tested for Chip A. Each lot consisted of a sample size of 6 chips. ANOVA and the student's t-test were used to analyze the data. Appendix C contains the detailed ANOVA tables.

- The mean adhesion strengths for lot numbers 2 and 4 are statistically equal.
- The mean adhesion strengths for lot numbers 1 and 3 are statistically equal.
- The mean adhesion strengths for lot numbers 1 and 3 are approximately 10% less than the mean adhesion strengths for lot numbers 2 and 4. In other words, there is a statistically significant difference in mean strengths between lot numbers 2 and 4 and lot numbers 1 and 3.

5.3.3.2 Chip B

Chip B (sample size = 8)	Lot 1	Lot 2
Mean Adhesion Strength (psi)	7896	8911

Table 9 - Chip B Test Results

There were two lots that were tested for Chip B. Each lot consisted of a sample size of 8 die. ANOVA and the student's t-test were used to analyze the data. Appendix C contains the detailed ANOVA tables. The results indicate that the mean adhesion strength for Lot 1 is statistically different from the mean adhesion strength of Lot 2. The mean adhesion strength of Lot 1 is approximately 11% less than the mean adhesion strength of Lot 2.

5.3.3.3 Chip C

Chip C (sample size = 8)	Wafer 1	Wafer 2
Mean Adhesion Strength (psi)	10,107	10,028

Table 10 - Chip C Test Results

There were two wafers that were tested for Chip C. (It was not possible to obtain die from two different lots for this chip). Each wafer consisted of a sample size of 8 die. ANOVA and the student's t-test were used to analyze the data.

Appendix C contains the detailed ANOVA tables. The results indicate that the mean adhesion strength for wafer 1 is statistically equal to the mean adhesion strength of wafer 2. These results are not surprising, since the same process parameters and operating conditions are used for wafers from the same lot.

6. Supplier Relationship Strategy

While working with the various suppliers during the internship, several management issues became apparent that relate to the relationship that Delphi Delco Electronics Systems (DDES) has with its suppliers. This chapter presents an overview of the relationship that DDES has with its suppliers as well as the strengths and weaknesses of the current supplier relationship management strategy.

The Purchasing organization within DDES has changed significantly within the last year. As DDES faces increasing cost pressures from its customers, there is a strong focus on reducing costs for purchased material. Purchased parts, material and equipment account for over one-half of DDES's cost structure. Although price is not the only criteria used for vendor selection, it is definitely given the highest priority. Other criteria include quality, delivery, service and demonstrated responsiveness. New suppliers are chosen mainly on price and product performance, since there is no established history with new suppliers.

6.1 Merger with Delphi Automotive Systems

As previously mentioned, DDES recently merged with the other Delphi Divisions. The merger has affected some areas of DDES more directly than other areas within the division thus far. Purchasing was one of the first groups within DDES to be integrated with the other divisions of Delphi. All of the managers within Purchasing have a dual reporting structure: they report to their management within DDES as well as to the management within Delphi's Purchasing group. This integration has led to a significant change in DDES's supplier strategy. Prior to the merger, the strategy was to reduce the number of suppliers to as small of a number as possible. The goal of having fewer suppliers allowed for the formation of partnerships, or Strategic Suppliers. However, Delphi's strategy is quite the opposite: maintain as many active suppliers as possible on the bid list to maintain a high level of competition and to drive towards the market price. It is interesting to note that this philosophy differs from that of the other major automobile manufacturers.

In several interviews with members of the Purchasing Group, several additional advantages of the merger were highlighted:

- DDES and the other divisions of Delphi can share lists of potential vendors that can be put onto the "bidder's list".
- By combining purchase orders, DDES and the other divisions can obtain volume discounts through its vendors.
- Because DDES and the other Delphi divisions can readily share information on vendor's prices, more information is available to DDES to determine what the market price is for a specific commodity.
- DDES and Delphi can work together to establish new programs that allow for a more systematic approach to sourcing.

The merger gives DDES access to a wealth of information that they did not previously have access to, particularly with respect to the market price of purchased parts and materials.

6.2 Single Source vs. Multiple Sources

As can be expected, a sole supplier can potentially have much more leverage over DDES, especially if the supplier knows that it is the only qualified supplier. Many other groups besides Purchasing are in frequent contact with suppliers. DDES's engineering organization communicates often with suppliers as it works to develop its designs, and Engineering may inadvertently let a supplier know that it is a single source. This, of course, leads to much frustration within Purchasing since its negotiating power is severely limited. The supplier has even more leverage over DDES if the engineering group supports this supplier and does not want to consider alternatives.

A supplier (working in conjunction with employees at DDES) will occasionally use a strategy known as "back door selling" as a means to sell its way into the organization without going through the formal purchasing procedures. The supplier may have a close relationship with an engineer, and hence the engineer will usually want go to

that supplier and work with them during a design phase of the product development cycle. Frequently, a supplier will be "designed into" the product so that the supplier will have a virtual lock on the business. This, again, will put the buyer in a compromised negotiating position and will also tend to create conflict between Purchasing and Engineering. Purchasing will want to seek quotes from as many qualified suppliers as possible, while Engineering will specifically request that one supplier be awarded the business.

Ideally, Purchasing would like to have two or more qualified vendors for a particular commodity. Having only one qualified vendor puts DDES at a disadvantage in terms of the level of negotiating that is possible. While two or more vendors is the ideal, the reality is that in many cases Purchasing only has one qualified supplier from which to source a needed part or material. This is partly due to the fact that DDES's prior strategy was to reduce the number of suppliers with which it dealt.

6.3 Partnerships

Many companies have adopted the philosophy that forming partnerships with suppliers is the strategy companies should adopt to manage its relationships with its suppliers. The notion of supplier partnerships gained popularity in the early 1980's, as one ingredient to the Japanese approach to lean manufacturing. In the widely read book, *The Machine that Changed the World*, Womack et al argued that the key was to "abandon power-based bargaining and substitute an agreed-upon rational structure for jointly analyzing costs, determining prices, and sharing profits."[16]

However, looking at the customer/supplier relationship from the buyer's perspective, the knowledge of and a willingness to use free-market competition is the strongest weapon available to the buyer. When buyers have the right to investigate and pursue alternative sources, the buyer is most likely to obtain the fair market price for the good he is purchasing.[17] However, implicit or explicit in most supplier partnerships is an agreement on the customer's part to not seek alternative sources. The right to seek other sources is usually not explicitly surrendered. Companies usually always maintain the right to seek alternatives. Most often, though, a company simply commits a substantial proportion of its purchases for a significant period of time to its supplier partner.

Frequent investigation of alternatives would not be in the spirit of most partnership agreements. In fact, Japanese lean producers seldom enter into partnership arrangements by conceding the right to pursue alternatives. Toyota, for example, uses competitive bidding very infrequently.[17] However, that is not to say that Toyota's approach is not intensely competitive. Their techniques and practices differ from those of the U.S., which may have lead to a misunderstanding of the Japanese partnership-style supplier management.[17]

A recent study of this issue was published in Sloan Management Review. Kapoor and Gupta argue that there may instances when it may be appropriate for a company to concede its right to pursue alternative suppliers. Two questions, which should be asked, are:[17]

- Are alternative suppliers readily available? With few viable alternatives, the right to pursue them becomes less powerful and valuable.
- Is it easy to change suppliers? If change requires extensive disruption or cost, the threat of switching loses credibility and the right to pursue alternatives becomes less potent.

Kapoor and Gupta argue that each of these questions can be answered independently, either affirmatively or negatively. As a result, there are four situations that can occur. Figure 16 presents a matrix of each situation.[17] Clearly, the only situation in which it may be desirable to form partnerships is the Type 4 situation. In this situation, the switching costs are high, and there are few alternatives. In Type 1 situations, in which the switching costs are low and there are many alternatives, partnerships are not at all advantageous from the buyer's perspective. In Type 2 situations, where there are many alternatives but the switching costs are high, the existence of alternatives provides a credible threat to suppliers. This threat allows the buyer to continue to secure concessions from the supplier as market conditions warrant. In Type 3 situations, where the switching costs are low but there are not many alternatives, the ability of a company to switch easily (especially as technologies evolve and other companies come up to speed) provides a credible threat to suppliers.

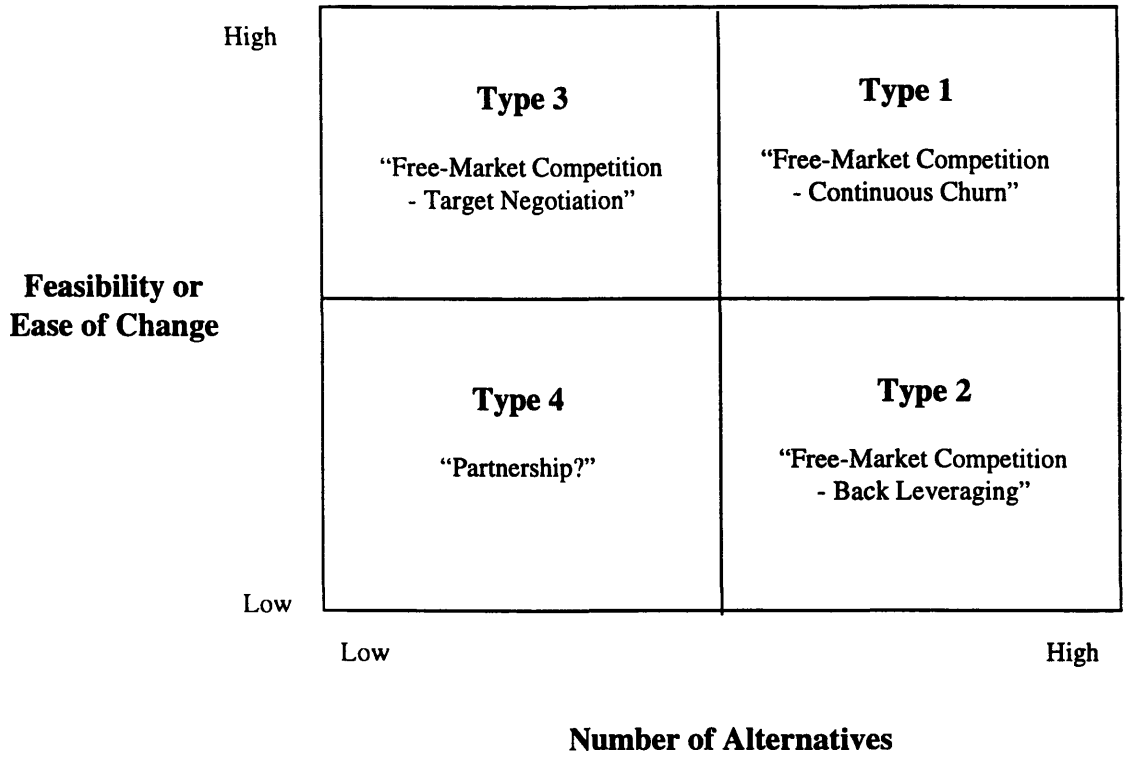

Figure 16 - Alternative Situations in Supplier Management[17]

6.3.1 DDES's Strategic Supplier Partnerships

Because of the recent strategic decision to increase the supplier base, DDES, in general, is not looking to form partnerships with its suppliers. However, DDES does recognize that there are benefits to forming partnerships with certain suppliers. Within DDES there is a proposal currently being reviewed to begin designating certain suppliers as "Strategic Suppliers". This program is also being undertaken within Delphi. The concept behind the Strategic Supplier Program is to designate those suppliers who have a core competency which provides products or processes that give DDES and Delphi a competitive advantage. The main criteria for a supplier to meet this designation are:

- A past history of exceptional performance in cost, quality and delivery.
- High dollar volume supplier.
- Must match DDES/Delphi's cost reduction obligations to its customers.
- Maintain competitiveness in industry segment.
- Commit to achieve benchmark levels of competitiveness.

DDES's goal is to select Strategic Suppliers who possess key technologies and who provide parts or materials that are distinct discriminators in DDES's product designs. Elements of the Strategic Supplier Partnership include:

- Supplier and DDES working together on joint product and process development projects.
- Supplier is granted insight into future DDES/Delphi products and processes.
- Long-term, or in some cases, lifetime global contracts.
- Supplier and DDES sharing in cost reduction achievements.
- Supplier provided additional business opportunities.
- Substantial involvement and support by DDES's and supplier's top management essential to maintain partnership.

Establishing partnerships with suppliers is an evolutionary process. DDES's purchasing organization believes that before a partnership can be established, DDES must first get to the lowest cost. As was stated earlier, the price that a vendor charges is an overriding concern for DDES as it works to decrease its purchased material costs. In the context of the framework that was presented earlier regarding the desirability of partnerships, DDES must ensure that the suppliers that it chooses to form partnerships with are those suppliers for whom DDES has few alternatives and the switching costs are high. (This is the Type 4 situation described above).

6.3.2 Purchasing/Engineering Relationship

One unfortunate consequence of the recent reorganization of the Purchasing department is that tension and conflicts have surfaced between the Purchasing and Engineering groups. Purchasing has changed many of its policies and procedures as a result of the merger with Delphi. One apparent change is that the Purchasing organization has more power than it previously had, and it has levied many more rules and policies upon the rest of DDES in order to further reduce costs. This has created some resentment within the rest of the organization as they struggle to adapt to the new rules and policies that Purchasing has implemented. Purchasing views itself as much more than the "order-takers" for the company. (This may or may have not been the previous belief of individuals and groups throughout the company prior to the merger).

Rather than just acting as the order takers for the company, Purchasing is working towards becoming an integral component of the product development cycle. Advanced Purchasing is a group within DDES that works with engineers in the early stages of the product development cycle to ensure that each supply-chain decision results in the lowest possible design cost. For example, an engineer may design a custom made part to source from a supplier. The advanced purchasing buyer may work with the engineer to determine if perhaps there is an off-the-shelf part that would satisfy the requirements of the engineer's product specification at a lower cost. This obviously would require close cooperation with the engineer and buyer. Purchasing wants to ensure that suppliers are not designed into the product, which limits their ability to maintain alternative sources for a particular part or material. Another advantage with the Purchasing group being involved in the design process in the early stages is that the quoting process can be significantly shortened, thus reducing lead times. Purchasing can request quotes on preliminary designs. In this way, suppliers may have the ability to input their suggestions for improvements before the design is locked in. DDES can leverage supplier knowledge to further reduce costs. Suppliers have incentives to work cooperatively with DDES in reducing costs, since they will have a better chance of being awarded the contract.

6.4 Case Study: Underfill Supplier & Die Supplier

This section presents a brief case study of two of the suppliers that I worked with during the course of the internship. I will present one scenario in which I received a lot of support and cooperation from a supplier. Conversely, I will present another scenario in which I was not able to gather much cooperation or assistance from a supplier. I will compare and contrast the two scenarios to draw some conclusions about when a supplier is likely to be a full participant in such a research effort.

6.4.1 Underfill Supplier (US)

The Underfill Supplier (US) provided me with a tremendous amount of cooperation and support. All of the information, data and product samples that were necessary to perform the underfill variation study were given to me in a timely manner. US was chosen as the underfill supplier because their underfill material performed the best in the numerous Design of Experiments (DOEs) that have been carried out to determine flip chip reliability and confirm product reliability targets. They were very eager to ensure that all customer requests were satisfied. Because I received the needed information and product samples from this supplier, the data and results are much more useful and meaningful to DDES.

6.4.2 Die Supplier (DS)

None of the die suppliers (DS's) were able or willing to provide me with much useful information or with any product samples of varied die passivation. As a result, the experimentation that was performed on the passivation resulted in little concrete data as to the actual reasons for variation in the adhesion strength of the passivation. The experiments that were performed were done ex post. I had no ability to specify under what process parameters the passivation would be deposited. I simply just requested different lots of material to determine to what degree there was variation in the adhesion strength from one lot to another. While the resulting data is meaningful in the context that we now know there is lot-to-lot variation in passivation adhesion strength, it is not as meaningful in the sense that we have no way of knowing why there is variation.

There were several reasons provided to me as to why the die suppliers were unable to assist me with this project. Firstly, the passivation deposition process is very difficult to control. It is not just a matter of "tweaking a knob" to adjust the thickness of the passivation layer for example. Because of this, the die suppliers were reluctant to adjust their process at all for fear of not being able to readjust their process for normal production material. Additionally, both the external and internal die suppliers believed that the adhesion of the die passivation to the underfill was the responsibility of their customers. Their customers were the product teams who had responsibility for developing the manufacturing processes to assemble flip chips. Their reasoning was not entirely unfounded, since the die suppliers wouldn't normally have the ability or knowledge to test the adhesion strength of the passivation to the underfill material. Section 7.2.1 presents a potential solution to this issue by suggesting that an adhesion specification be included in the product specification for both the die supplier and the solder mask supplier.

Table 11 summarizes the key differences between the underfill supplier and the die suppliers. This summary provides the reader with some basic information to determine under what conditions it may be favorable to undertake a supplier process variation study such as this.

Attribute	*Underfill Supplier*	*Die Supplier*
Ease of varying processes	Processes were easily varied and specifications could be adjusted.	Suppliers could not "tweak" process specifications.
Incentive Structures	New supplier to DDES – was eager to meet all customer requests.	Suppliers possessed power and leverage – would not suffer adverse consequences for failing to comply.
Attitude of Supplier Regarding Their Responsibility to Ensure Adhesion Capability of Their Material	Adhesion capability was an important attribute of their material and ensured material met specifications.	Adhesion capability was not their responsibility, but did not have the capability to determine if material met minimum requirements.
Proprietary Process	Process is proprietary, but supplier could share general information and general tolerances.	Processes are proprietary. External supplier believed it could not share processing information.
Up-Front Buy In and Agreement	Obtained buy-in from supplier. Supplier agreed to participate in the study.	Never fully obtained buy-in from the supplier. Supplier never fully agreed to participate in the study.

Table 11 - Comparison of Supplier Attributes

7. Results and Recommendations for Further Study

This chapter summarizes the findings from the data analysis that was performed and includes recommendations for further study. I have also included an overview of the lessons learned from this project, and how a project such as this might best be approached in the future. Additionally, recommendations for the supplier relationship strategy are included.

7.1 Results from Data Analysis & Recommendations for Further Study

7.1.1 Underfill

The results from the underfill data analysis indicate that the current underfill formula maintains a very robust adhesion capability when the underfill manufacturing process is subjected to process variation. The chosen underfill supplier, US, has performed extensive testing on its underfill to ensure the adhesion capability. Table 12 is the summary of the verification study that was performed to attempt to duplicate US's results.

	Standard	Sample 1	***Sample 2***	Sample 3	***Sample 4***	Sample 5	Sample 6	Sample 7
Mean (PSI)	9414	9280	***8103***	9444	***8289***	9440	9381	9404
P-value		0.24790	***0.00013***	0.42723	***0.00229***	0.42379	0.42155	0.47392
% of Control		99%	***86%***	100%	***88%***	100%	100%	100%
Supplier Data (measured as a % of standard material)		100%	***50%***	100%	***60%***	100%	100%	100%

Table 12 - Underfill Test Results and Comparison with Supplier Data

My results match US's results almost exactly, which provides DDES's product development group with some increased confidence that this particular material can withstand slight modifications to the underfill process tolerances. Appendix A contains the detailed AVOVA results showing the statistical significance of each sample mean as

compared to the standard material. My recommendation is that DDES need not undertake any additional process variation studies with the current underfill formulation that they are using.

Currently, DDES has only qualified US as an underfill supplier. This is a case in which the supplier has been designed into the product. Many different underfill suppliers, as well as many different underfill formulations from each supplier, were evaluated and tested for product reliability by DDES's advanced development group. US's underfill performed the best in the accelerated lifetime testing (which involves completing many thermal cycles). However, new and better underfills with different formulations are continuously being introduced into the market. DDES may very well decide to switch to another underfill supplier at some point in the future. It is unknown whether another supplier would be willing to perform the extensive process variation testing that US completed as part of its product development process. Because underfill is such a vital component to the flip chip package, DDES may want to consider making this level of testing a requirement for future formulations of underfill.

Process variation analysis for adhesion strength could be eliminated in the future if the adhesion strength was made part of the material specification. When adhesion is a part of the material specification, all material that the supplier ships must meet the exact specification ranges that DDES specifies. If a supplier process change were to reduce the adhesion strength to an unacceptable level, the supplier would have to readjust the process or formulation to bring the material within specification before they could ship the underfill to DDES. The recommendation to implement an adhesion specification is discussed in detail in Section 7.2 below.

7.1.2 Solder Mask

The results that were obtained from the data analysis on the solder mask are as follows:

- When the level of photoinitiator was altered, either by increasing or decreasing the amount by 10%, the adhesion strengths were reduced substantially. The

actual tolerances at the supplier an order of magnitude less than 10%, however any change in the amount of photoinitiator may warrant further investigation.

- When the level of filler was increased, there was no statistically significant reduction in adhesion strength. However, when the amount of filler was decreased, the adhesion strength was reduced substantially.
- Neither increasing nor decreasing the level of photopolymer resulted in any statistical degradation of adhesion strength.
- Additionally, another interesting observation of this data is that the control material, which is manufactured in the plant, exhibited much lower adhesion strength than the nominal material, which was manufactured in the lab. In two of the cases the control material's adhesion strength was more than 40% lower than the nominal material produced in the lab.

Appendix B contains the detailed data tables showing which of the tested sample means statistically differed from the control mean.

7.1.2.1 Recommendations for Further Study

As was noted in Chapter 4, there are many key process parameters for the manufacture and application of solder mask. During the course of the internship, I was able to test a few of those parameters. However, there are several other process parameters in the manufacture of solder mask that should be varied and tested to gauge their effects on adhesion strength. These include:

- Time of mixing or dispersion for each of the key ingredients (filler, catalyst, pigment, free radical initiator).
- Temperature of mixing pot.
- Mixer blade speed.

Variation in any or all the above parameters may explain why the material mixed in the lab exhibited much different characteristics compared to the material which was mixed in the production facility.

As was mentioned earlier, there was no work done to determine the effects of process variation in the application of the mask. There are many key process parameters that could be tested. However, based upon my discussions with engineers at DDES and at the circuit board fabrication supplier, the following process parameters should be targeted initially for testing and analysis.

- Solvent content at mixing.
- Tack dry time and temperature.
- Exposure energy and time.
- Developer pH and time.
- Final cure temperature and time.

7.1.3 Die Passivation

The data that was collected for the die passivation was collected ex post rather than ex ante. This means that we do not know the causes of variation in the adhesion strength of the different lots that were tested. The semiconductor suppliers were unable or unwilling to vary the passivation process to determine the effects of process variation. However, data were collected to determine to what extent there was variation from lot-to-lot or wafer-to-wafer in the adhesion strength. This was done to gain leverage and obtain cooperation from the suppliers to further explore the effects of variation on adhesion strength. Appendix C contains the detailed data and ANOVA results for the die passivation studies. The data analysis from Chapter 5 indicates that there is statistically significant variation in two of the chip types that were tested. As a result, I have made the following recommendations for further study.

- Determine if a 10%-11% difference in adhesion strength is high enough to warrant further investigation.
- This level of difference in adhesion strength could very well be enough to potentially impact product reliability. Therefore my recommendation is to pursue a study to determine the causes for the differences.
- Determine cause(s) for the variation in adhesion strength.
- Work with IC manufacturers to develop and implement an adhesion specification. (This recommendation is further explored in Section 7.2.1).

7.2 Recommendations for Future Project Approach

The fundamental idea of doing an analysis of supplier process variation can be a valuable addition to a company's reliability studies. This method is a proactive way to uncover potential problems up front (and thus adjust the process) rather than have them surface after the product development cycle has been completed, when it is much more difficult and costly to fix the problems. This is especially true when a company is implementing a new technology, like DDES is doing with flip chip on laminate substrates. Supplier cooperation is absolutely vital to successfully complete a project such as this. In Section 6.4, I presented a case study in which I had cooperation from one supplier but not from another. The results that were obtained from the underfill supplier, who was willing to cooperate with this study, were much more meaningful than the data and results that were obtained from the die supplier, who was unable or unwilling to cooperate.

In the future, it may become necessary to include the adhesion strength as part of the product specification for the solder mask, underfill and die passivation. By doing this, the customer, DDES, can be assured that the material supplier has fully comprehended the fact that its material must meet specific adhesion strength levels. The details of this recommendation are included in the following section.

7.2.1 Adhesion Test Specification and Test Method

Currently there is no adhesion specification in the material specification for the solder mask or die passivation. While a process variation study such as the one performed for this internship can be beneficial, it can also be very time consuming as well as costly to perform. For this particular project, a process variation study would not have been necessary if the underfill, solder mask and die passivation suppliers had been required to meet an adhesion specification as part of the product specification. (There is an underfill specification in place for the underfill material only). However, adhesion strength is not an intrinsic property of any one material. In this case, adhesion strength is determined by measuring how well one material adheres to another material. The ability of one material to adhere to another material can change dramatically even with slight changes in the chemical makeup of one or both materials.

7.2.1.1 Test Method

The test method could be very similar to the test method that was used for the data collection. Each vendor would use a set of "generic" materials for the solder mask, underfill and passivation, so that consistent measurements could be achieved. The supplier for each material could evaluate the adhesion of its material against the other generic materials to determine if a proposed change would alter the adhesion capability of its material. DDES would have to determine an adhesion strength specification for this generic test. This specification would need to correlate with the actual materials and required adhesion of the flip chip package in order for it to be meaningful.

The advantages with incorporating an adhesion specification into the material specification are:

- Suppliers would have the ability to determine if their process specifications achieve the required adhesion strength for flip chip packages.
- Ex ante process variation studies, such as the one conducted for this research project, could be minimized or altogether eliminated in the future.
- DDES would have the ability to test incoming material on a sample basis and reject material for not meeting the adhesion requirements.

However, there are a couple of key issues that would have to be resolved in order to implement an adhesion test specification. Suppliers would more than likely require a price increase. This is counter to Purchasing's goal to reduce the purchase price of purchased parts and materials. Also, the development of the test method and the ability to develop a meaningful correlation between the test specification and the actual performance of the material in the final product could hinder DDES's ability to implement an adhesion specification.

7.3 Supplier Relationship Strategy Recommendations

Developing an appropriate supply chain strategy is a fundamental requirement for a business to succeed in today's global marketplace. Supply chain strategy usually consists of three main components: make/buy decisions, supplier selection decisions and the contracts/relationships that are established between customers and suppliers. Charlie Fine, a professor at the Sloan School of Management, talks of supply chain design as being the meta-core competency of a firm. Supply chain design should go hand-in-hand with product and process design to create a framework for product development known as Three-Dimensional Concurrent Engineering. Knowing which components to make and which components to buy (also known as the make/buy decision) and who to buy them from are key sources of lasting advantage for a company. Thus, decisions and strategies relating to supplier relationships can have a significant impact upon the future success of emerging technologies, such as flip chip technology.

DDES is just beginning to recognize the need to incorporate supply chain strategy into its product and process design strategies. In the case of flip chip technology,

suppliers have developed some key technologies and capabilities that DDES does not possess. DDES worked with these suppliers early on in the development cycle to jointly create a set of materials that would meet product reliability targets. As flip chip technology continues to evolve, supply chain strategy will continue to play a vital role in DDES's ability to exploit and quickly adopt the latest technologies for use in its products. DDES is heading in the right direction by implementing its Strategic Supplier Program. This program targets those current suppliers who possess the key technology drivers necessary for future generations of products. However, the success of this program as well as other programs in the future will be dependent upon DDES elevating the supply chain strategy to the same level as the product and process strategies.

Currently, many different groups within DDES have a part in the creation and the execution of the supply chain strategy. This has led to a fragmented and often conflicting strategy. The conflicts that exist between the Purchasing and Engineering organizations are major contributors to the inability of the organization to development a consistent strategy. When developing its strategy, DDES should attempt to answer the following questions. Will we make or buy? What supplier(s) should be chosen? What criteria should be used in the selection of supplier(s)? How will DDES use its suppliers? Will the suppliers work jointly with DDES on product and process development? Or will DDES simply hand a detailed design off to the supplier?

These are just some of the key areas that must be answered to begin to create a supply chain strategy. The key learning is that DDES recognizes the need for such a strategy, and that it forms the appropriate relationships with its suppliers to successfully carry out that strategy.

7.4 Lessons Learned

There are several key lessons that were learned from participating in this project. As with any project that involves the participation of many different entities, there were several major stumbling blocks that were encountered. In this section I will attempt to document what I feel were the major stumbling blocks that were encountered during the

internship, and then attempt to provide some possible solutions for eliminating them in the future.

- The single most important item is to obtain the buy-in from all parties up front. Suppliers, both internal and external, have to be willing and able to make products that may vary slightly from what they are accustomed to producing. In some cases this may not be feasible from the supplier's perspective. The supplier relationships that have been formed will play a role in the ability to gain cooperation. Additionally, who actually possesses the power in the relationship will have a large bearing on the ability to obtain the needed information and product samples.

- Determine the feasibility of doing process variation. Are the processes to be studied easily adjustable? In the case of the die passivation, the processes are not very easily adjustable, which was a factor in the inability to obtain any product samples with variation.

- Determine if a project such as this is really necessary. What are the downside risks if a process variation project is not performed? Are the costs of undertaking such a project worth the data that will be gained? In the case of my research, the downside risks could be very detrimental since flip chip on laminate technology is largely unproven and has not been used in full-scale production as of yet. The costs for this research project were quite minimal as compared to the potential cost avoidance of not having future reliability problems.

- In this project, one of the stumbling blocks related to differing incentive structures. The internal die supplier had very little incentive to provide the requested product samples, while at the same time faced no adverse consequences by not cooperating. (Other than perhaps some disappointment in not satisfying a customer request). The internal supplier is a profit/loss center with differing incentives and priorities. A project such as this one, which requires the participation of several organizational groups within the

company, should have an appropriate incentive scheme associated with it so that all groups are equally motivated to participate.

- When dealing with outside suppliers, an issue that can become a stumbling block is the reluctance of suppliers to share information regarding proprietary processes. This issue surfaced several times throughout this internship. Flip chip technology is a new process, but it has the potential to be the next big innovation in electronic packaging methods. Suppliers that succeed in developing materials and components that offer superior product reliability will most certainly gain a competitive advantage and profit from their technological innovations. As can be expected, suppliers would most certainly be reluctant or unwilling to share much of their process information, other than what would be necessary for qualification requirements. (All DDES suppliers must be QS-9000 registered to bid for business). Performing a process variation study may require the supplier to share information above and beyond what they would ordinarily have to, and as a result, suppliers may be reluctant or unwilling to fully cooperate.

8. Conclusions

This thesis presents a statistical methodology for performing a supplier process variation study when it is uncertain how slight changes in supplier processes will impact product reliability. Research such as this only needs to be undertaken in certain circumstances. Below are some of the situations in which a company may want to consider conducting a supplier process variation study.

- A new or modified technology.
- Technologies in which there are significant reliability concerns.
- Supplier provided components or materials in which one or more critical attributes of the part or material is not specified in the product specification.
- Situations in which suppliers may make slight modifications to a process that are seemingly transparent to the customer.

The content of this thesis consists of basic experimental methods to determine the adhesion capabilities of three of the primary materials in a flip chip package: underfill, solder mask and die passivation. To some extent the research was a pilot effort at the Internship Company, Delphi Delco Electronics Systems (DDES), to determine the feasibility of using such an approach with suppliers. As I noted above, this research methodology can be used in certain circumstances in which supplier process variation is a concern and requires evaluation.

Throughout the thesis I have operated from several assumptions. First, the fundamental idea of doing an analysis of supplier process variation can be a valuable addition to a company's reliability studies. This method is a proactive way to uncover potential problems up front (and thus adjust the process) rather than have them surface after the product development cycle has been completed and it is much more difficult and costly to correct the problems. Secondly, supplier cooperation is absolutely necessary to successfully complete a project such as this. Without upfront supplier buy-in and cooperation, very little meaningful data can be collected or analyzed. A process study

such as the one conducted for this research can be helped or hindered by a company's supply chain management strategy. It is essential to develop a supply chain strategy that is consistently applied throughout the organization. In addition, the supply chain strategy should be integrated into the product and process development strategies concurrently.

Below are the specific conclusions relating to the technical and managerial components of this thesis.

8.1 Technology Conclusions

The adhesion capabilities of two or more materials in a system usually cannot be theoretically measured. Most of the work that is done to determine adhesion strengths is experimental in nature. As a result, a lot of testing and experimentation goes into verifying the adhesion capability of a material. The same can be said for the materials that were studied during this research project: underfill, solder mask and die passivation. The following conclusions can be drawn as a result of the research that was conducted for this thesis.

8.1.1 Underfill

- The underfill material that has been selected by DDES for the flip chip applications appears to maintain superior adhesion capabilities when the process has been varied within the specified tolerances.

- An experiment to verify and duplicate the underfill supplier's results was performed. The supplier's results correlated very highly with my results.

- These results provide DDES with a high level of confidence in the adhesion capability of the current specified underfill. However, these results cannot be used to conclude that future underfill formulations will possess the same robustness to process variation.

8.1.2 Solder Mask

- Some limited information was obtained with respect to three of the components of the mask material.

- Mask material that was manufactured in the plant behaved differently than the material that was manufactured in the lab. This indicates that there are additional process parameters that should be analyzed in the manufacture of the mask material.

- No product samples were obtained from the solder mask screen printing supplier. There are several critical process parameters at this supplier that should be analyzed for their effects on the adhesion strength of the mask to the underfill material.

- A recommendation was made to require the solder mask manufacturer and screen printer to comply with an adhesion specification as part of the overall product specification for their material. This would ensure that the supplier's process would satisfy all adhesion requirements. (This would potentially reduce or eliminate the necessity of performing supplier process variation studies).

8.1.3 Die Passivation

- Adhesion strength was measured for several different lots of 3 different types of die. A 10%-11% difference in adhesion strength was observed in 2 of the 3 chip types.

- This difference in adhesion strength cannot be attributed to one or more cause(s), since these experiments were not specified ex ante. The reasons for the variation are not known.

- The die suppliers (both the internal and external suppliers) were not able or not willing to supply the necessary product samples for this project. The two primary reasons supplied by the supplier were: (1) it is not their responsibility to ensure the adhesion of the die passivation to the underfill, and (2) the passivation deposition process is very difficult to control and cannot be "tweaked" to supply varied material.

- As with the solder mask suppliers, an adhesion specification requirement as part of the product specification would require the die suppliers to ensure that their passivation process (and subsequent processes) produces a die that is capable of adhering sufficiently to the underfill material.

8.2 Supplier Relationship Conclusions

Table 13 presents a comparison of the strengths and weaknesses of DDES's current supply chain strategy. Most components of DDES's supply chain strategy can be viewed as having both positive and negative aspects embedded within the strategy. The key lesson that DDES should take away from this research is that the supply-chain strategy needs to be elevated to the same level as that of the product and process strategy. A 3-dimensional concurrent engineering approach in which supply-chain, product and process development are all undertaken simultaneously provides DDES with the ability to quickly evolve and adopt the capabilities to compete in today's rapidly changing global markets.

Component of Strategy	*Strengths*	*Weaknesses*
Increase in Number of Qualified Suppliers	Working to reduce costs by increasing number of qualified suppliers – drive towards market price.	Suppliers not willing to commit resources to product development projects.
Strategic Supplier Program/Partnerships	Key suppliers and technologies are identified. Suppliers are formally involved in a dual product development structure with DDES.	Program not broad enough – too limited in scope. Also, there is a danger that the program may become too bureaucratic and political.
Supply Chain Development	DDES has begun to develop a supply chain strategy. The merger with Delphi has facilitated this.	Supply Chain Strategy is fragmented and not consistently applied across the organization.
Supplier Relationships	DDES maintains solid relationships with many suppliers (although relationships are informal and not defined). DDES possesses the "power" in most relationships.	Some suppliers possess the power within the relationship due to DDES being dependent for knowledge and dependent upon suppliers' key technologies.
Global Sourcing Initiative	Potential number of suppliers increases, which results in drive towards market price. DDES is able to reduce costs of purchased parts and material, which account for 2/3 of cost structure.	Suppliers resent the forced price decreases. Suppliers may not be willing to cooperate in future development projects or may force engineering changes in order to increase quoted prices.

Table 13 - Strengths and Weaknesses of DDES Supply Chain Strategy

Appendix A

Table 14 shows the raw data and ANOVA table for the underfill experiment that was conducted (data are in units of pounds per square inch). One of the data points for Sample 1 is missing due to the die shear experiment not shearing the die correctly. T-tests were run for each sample to compare the mean adhesion strength of the variant to the mean adhesion strength of the control sample. As can be seen from the t-tests row of the table, Sample #2 and Sample #4 are statistically unequal to the control sample. All of the other samples are statistically equal. In the ANOVA table, the F values indicate that both the solder mask coupon (which was the blocking variable in this experiment) and the underfill type are significant factors (at an alpha level of .05).

Coupon	Control	Sample 1	Sample 2	Sample 3	Sample 4	Sample 5	Sample 6	Sample 7
1	9210.92	9582.34	7404.98	9507.61	8579.33	9414.75	9525.56	9320.38
2	9132.42	9202.37	8282.71	9025.09	8769.76	9493.57	8935.81	9535.08
3	9789.60	9376.94	9068.41	9666.53	8735.79	9566.37	9960.06	9455.56
4	9407.68		8654.64	9276.01	6798.76	9613.61	9261.34	8883.37
5	9077.75	9743.16	7564.41	9634.49	7245.66	9161.45	9184.13	9332.55
6	9073.88	8522.43	7407.59	9501.16	8685.14	9270.75	9371.59	9718.00
7	9726.41	9203.71	8408.29	9901.62	8724.72	9560.90	9634.61	9550.78
8	9893.07	9332.46	8031.94	9042.66	8769.17	9440.04	9171.68	9436.53
Mean	9413.97	9280.49	8102.87	9444.40	8288.54	9440.18	9380.60	9404.03
Standard Deviation	341.74	388.12	612.70	308.76	792.98	156.05	319.76	246.17
t-test value		0.2479	***0.00013***	0.427232	***0.002286***	0.423789	0.421546	0.473921

ANOVA Results

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Solder Mask Coupons	3188957	7	455565.3	**2.3851**	0.032	2.2032
Underfill Type	17208779	7	2458397	**12.8706**	2.19E-09	2.2032
Error	9168386	48	191008			
Total	29566122	62				

Table 14 - Data and ANOVA Results for Underfill Experiment

Appendix B

The following 3 tables, Table 15, Table 16 and Table 17, contain the raw data and t-tests that were conducted for the solder mask experiments (data are in units of pounds per square inch). For each component, there were two tests that were run at three different levels, -10%, +10%, and a nominal value. Each of these variants was compared with the control material to determine if the mean adhesion strengths were statistically equal with the mean adhesion strength of the control material.

PhotoPolymer Sample	Control	#1 -10	#2 -10	#1 +10	#2 +10	#1 PP	#2 PP
1	3110.174	3459.884	2353.011	2248.568	908.1741	3006.8	2773.563
2	1833.408	3792.331	2835.181	1322.85	1985.054	3546.084	2726.031
3	1549.83	4397.242	2210.273	1753.55	2265.555	3986.79	2057.604
4	1449.4	2044.103	2601.894	1380.109	747.907	1869.704	4026.787
5	1106.083	4290.498	3949.598	1602.819	1659.113	2772.145	2374.618
6	1540.545	2892.333	3099.321	1631.816	2314.786	2745.231	2508.665
7	1845.257	2211.096	2788.842	2075.639	3346.715	4328.409	3542.002
8	1993.796	4560.422	3220.502	1418.444	2106.127	4525.085	3163.289
Mean	1803.562	3455.989	2882.328	1679.224	1916.679	3347.531	2896.57
Stdev	596.5998	983.8819	550.5781	333.6777	829.3908	909.5315	647.6434
T-tests		0.086048		0.232469		0.136232	

Table 15 - Raw Data and t-tests for Photopolymer Experiment

Photoinitiator Sample	Control	#1 -10	#2 -10	#1 +10	#2 +10	#1 PI	#2 PI
1	2862.661	2375.159	3334.3	1357.848	2516.432	2413.158	3213.702
2	1216.974	3173.019	2418.602	1442.764	2421.424	3553.436	3703.328
3	1905.882	1378.57	2954.935	1425.506	1764.438	2980.159	3209.791
4	1627.879	1465.718	2960.252	3029.471	1798.616	2967.11	3187.856
5	1487.798	1215.414	1725.976	1417.811	1738.446	3223.264	2351.784
6	2598.531	3018.313	2298.67	1443.582	2901.123	3466.041	2066.974
7	1205.085	1614.335	3448.464	1597.967	2489.739	3170.328	3679.994
8	1258.216	1081.685	2128.649	1291.837	1515.662	2569.362	2462.231
Mean	1770.378	1915.277	2658.731	1625.848	2143.235	3042.857	2984.457
Stdev	642.0459	825.9627	609.1035	573.7694	497.2891	399.814	616.4436
T-tests		0.029845		0.037239		0.412687	

Table 16 - Raw Data and t-tests for Photoinitiator Experiment

Filler Sample	Control	#1 -10	#2 -10	#1 +10	#2 +10	#1 F	#2 F
1	3253.105	3049.773	2598.143	2558.493	3232.379	1148.774	3440.604
2	1370.381	2986.636	2614.096	2506.487	3172.718	1185.194	3727.851
3	2655.732	3561.619	2434.523	2062.198	3142.861	2248.715	2848.825
4	3433.819	2847.49	2328.193	4133.223	2681.926	3941.364	3389.051
5	3846.216	2011.171	4133.254	3743.029	3964.421	3161.699	4062.814
6	1553.67	2085.649	3633.449	2440.755	2874.76	3360.834	3894.217
7	2956.524	3618.621	2989.443	3177.838	1874.334	3363.162	3436.117
8	2067.445	3456.197	2804.283	3482.831	2832.888	3914.816	2355.938
Mean	2642.112	2952.145	2941.923	3013.107	2972.036	2790.57	3394.427
Stdev	900.8938	624.2294	630.0176	730.0074	590.3991	1130.448	559.0479
T-tests		0.487228		0.451645		0.098546	

Table 17 - Raw Data and t-tests for Filler Experiment

Appendix C

Data for Chip A

Table 18 shows the raw data and ANOVA results for the experiment that was conducted to test the die passivation variation in Chip A (all data are in units of pounds per square inch). Two data points in Lot 1 are missing due to the die shear test not shearing the die at the correct interface. As can be seen from the ANOVA table, the F-statistic indicates that the mean adhesion strengths for the Lot numbers are in fact statistically different.

Chip A	Lot 1	Lot 2	Lot 3	Lot 4
Coupon #1	7776.44	8182.72	8885.57	9005.56
Coupon #1		8721.03	8076.41	8804.63
Coupon #2		9189.59	8625.28	9174.02
Coupon #2	7934.71	9232.22	8057.22	8593.06
Coupon #3	8201.98	8679.53	7508.27	9104.66
Coupon #3	8532.28	8782.90	8755.70	9485.45
Coupon #4	7828.70	9097.47	7866.13	8853.45
Coupon #4	7101.65	9398.58	8463.98	8993.83
Mean	7895.96	8910.50	8279.82	9001.83
Standard Deviation	479.54	394.57	478.69	267.84

ANOVA

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Solder Mask Coupon	2122286	7	303183.7	0.74	0.55	2.58
Lot Number	12566381	4	3141595	***7.67***	8.93E-05	2.93
Error	7370809	18	409489.4			
Total	22059476	29				

Table 18 - Raw Data and ANOVA Results for Chip A

Data for Chip B

Table 19 shows the raw data and ANOVA table for the experiment that was conducted to test the die passivation variation in Chip B (all data are in units of pounds per square inch). As can be seen from the ANOVA table, the mean adhesion strengths between Lot #1 and Lot #2 are statistically different.

Chip B	Lot 1	Lot 2
	11109.46	9664.20
	11252.11	10018.13
	11263.03	10449.77
	10896.97	9209.07
	11213.98	9739.20
	10933.49	10439.78
Mean	11111.51	9920.03
Standard Deviation	161.83	482.49

ANOVA

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Lot Number	4258865.308	1	4258865.308	***32.89***	0.000189	4.96
Error	1294955.01	10	129495.501			
Total	5553820.318	11				

Table 19 - Raw Data and ANOVA Results for Chip B

Data for Chip C

Table 20 shows the raw data and the ANOVA table for the experiment that was conducted to test the die passivation variation in Chip C (all data are in units of pounds per square inch). As can be seen from the ANOVA table, there is no statistical difference in the mean adhesion strengths of Wafer #1 and Wafer #2.

Chip C	**Wafer 1**	**Wafer 2**
	9654.63	10720.06
	9902.49	8121.64
	10471.89	10509.10
	10445.54	10017.81
	9652.67	10746.78
	10361.97	10684.46
	10069.86	9618.63
	10298.24	9805.60
Mean	10107.16	10028.01
Standard Deviation	338.82	887.16

ANOVA

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Wafer Number	206105.5276	1	206105.5276	***0.44712***	0.516363	4.7472
Error	5531550.907	12	460962.5756			
Total	5737656.434	13				

Table 20 - Raw Data and ANOVA Results for Chip C

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