# An Analysis of Revenue and Product Planning for Automatic Test Equipment Manufacturers

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B.S. Electrical Engineering, Worcester Polytechnic Institute, 1990
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Submitted to the Sloan School of Management and the
Department of Electrical Engineering and Computer Science
In partial fulfillment of the requirement for the degrees of

**Master of Science in Management**
**and**
**Master of Science in Electrical Engineering and Computer Science**

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## Abstract

Revenue and product planning for automatic test equipment (ATE) manufacturers has been difficult due to the cyclical nature of the semiconductor industry. Any insight into this area can provide a significant competitive advantage through tighter controls on cost and improved customer service. This work reviews possible improvements in revenue planning and introduces tools to help better understand the market. A model for developing forecasts of ATE demand based on planned semiconductor fab capacity increases is proposed. This is meant to address some of the shortcomings of the current approach, which is based on semiconductor revenue forecasts. The accuracy of the new model's predictions is compared against the existing process's output. Although the data used to support the model has not been in existence for long, early results show some improvement. Both the new and old techniques are then used to assess the impact of possible technology changes that would greatly affect the ATE market. This helps to demonstrate the strengths and weaknesses of each approach. A financial model is also presented which provides a quantitative assessment of tradeoffs in selecting capacity levels. The competition and volatility in the semiconductor manufacturing equipment industry drive the results of this analysis. Sensitivity analysis shows the impact of improvements to forecasting accuracy and flexibility. Finally, more general recommendations and observations are abstracted from each of the models and applications presented. These primarily focus on the need to incorporate forecast error into revenue and product planning.

Thesis Advisors:

Associate Professor Duane Boning, Electrical Engineering and Computer Science

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This thesis is dedicated to my wife, Lea, for her constant love and support.

**Bibliographic Note on the Author**

Paul DeCosta graduated from Worcester Polytechnic Institute, Worcester, MA in June, 1990 with a Bachelor of Science degree in Electrical Engineering, and then from Rutgers University, New Brunswick, NJ in June, 1992 with a Masters of Science degree in Biomedical Engineering. Upon graduation, he worked in the Medical Imaging Systems division of Polaroid Corporation as a senior engineer in hardware manufacturing. He had both technical and managerial responsibilities. Paul joined the Leaders for Manufacturing Program at MIT in 1996, and completed his research internship at Teradyne, Incorporated in Boston, MA. He will be joining Hewlett Packard's Medical Products Group upon the completion of his MIT degrees.

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# 1. Introduction

## 1.1. Problem Statement

Automatic test equipment (ATE) serves the semiconductor manufacturing industry in three ways. It is used to test fabricated wafers in the wafer sort operation, to test packaged die in final test and to characterize the frequency and other performance parameters of devices. It has been an integral part of the semiconductor manufacturing process since the late 1960's [1]. Since the introduction of the personal computer in 1983 and its subsequent success, the ATE industry has had enormous growth, with a compounded annual growth rate of 18.6%. However, this industry is not without its problems. Although current annual revenues are over $3.5 billion, sales have been very cyclical due to the nature of its customers, semiconductor manufacturers. Figure 1.1 shows the annual growth in revenues for the semiconductor industry and its equipment suppliers (data source: VLSI Research).

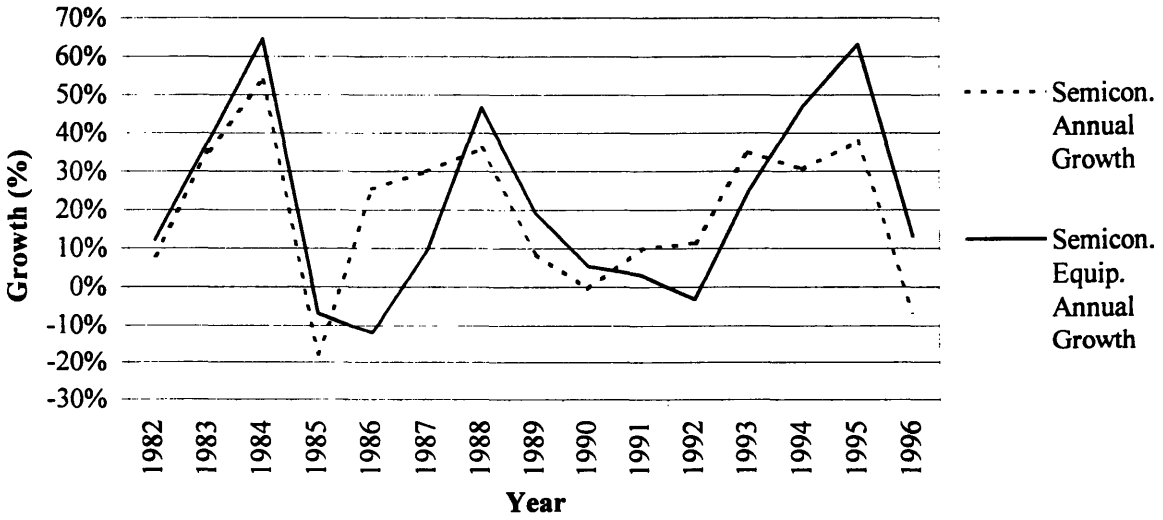



**Figure 1.1 Revenue Growth: Semiconductor and Semiconductor Equipment Markets**

In addition, there are strong efforts to reduce the cost of ATE. The growing complexity of the semiconductor manufacturing process and device requirements have driven up the price tag of a new fab to over $1B. Meanwhile, the price per million instructions per second (MIP, a common measurement for computer power) has been in a steady decline

in accordance to Moore's law. As a result, semiconductor manufacturers are pushing their suppliers to be more cost conscious [2], [3], [4], [5]. The effective management of expenses caused by dramatic swings in demand can be the difference between a successful and unsuccessful semiconductor manufacturing equipment supplier.

Due to the size and interest in the semiconductor industry, there are a variety of firms focusing on developing accurate forecasts of future revenue to help in the management of cyclicality. A common technique used by semiconductor manufacturing equipment manufacturers is to track the percentage of revenue that semiconductor companies spend on their type of equipment. This ratio is called the **buy-rate**. Trends in this percentage are used in conjunction with semiconductor forecasts to create a **top-down** estimate of sales for their respective industry.

In recent years, there has been an increased interest in using more concrete market data to create **bottoms-up** forecasts [6], [7], [8]. Particularly since 1994, when the memory industry was recovering from a dramatic downturn due to over capacity, research agencies and industry journals have been closely following announcements of new fab starts. There have been databases developed dedicated to tracking current worldwide semiconductor fab capacity as well as future projections based on announced increases [9]. Because fabs take more than two years to complete and are very visible, it is thought that the tracking of new starts is a good means to predict future business for manufacturing equipment companies [10], [11]. However, the relationships between increases in worldwide fab capacity and ATE demand have not been explored to the point where the industry can exploit such information.

## 1.2. Thesis Objective

The goal of this work is to investigate improvements to, and gain a deeper understanding of, revenue planning for the ATE market. This includes:

- Testing the viability of using a bottoms-up forecasting process based on current and planned worldwide fab capacity for revenue and product planning.
- Understanding how modeling can be used to investigate the impact on future demand caused by predicted technology changes.

- Quantifying financial trade-offs that exist due to the characteristics of ATE manufacturing and the inevitable error that will exist in forecasting demand.

The benefits of findings in these areas include the ability of ATE manufacturers to take a more proactive approach in supporting changes in customer demand. This could lead to competitive advantages in the market place due to operational improvements such as creating shorter, stable lead-times. Also, operating costs related to reactive capacity expansions/reductions could be greatly reduced.

## 1.3. Research Description

The research for this work centered on modeling. This includes both an examination of existing tools, as well as the development of new ones. Older models reviewed are representations of current policies and processes. Newer models are a conglomeration of internal tacit knowledge, market data, customer input, and statistical techniques aimed at turning data and knowledge into information. These models were based on operations research, particularly those that deal with planning for non-deterministic demand [12], [13], [14], [15]. Although most of the work presented here describes the concepts behind the models and their general effectiveness, there was a concerted effort made to ensure that tools were developed that were practical and applicable.

There were a variety of sources that served as a foundation for the formulation of models and parameters that were used. A large amount of the information was collected by interviewing employees within Teradyne. Also, discussions were held with some of their customers. Sources of market data include several consultant firms and industry organizations such as Dataquest, VLSI Research, Strategic Marketing Associates, SEMI, and Sematech. SEMI and Sematech also served as sources of technical information, along with the SIA and industry journals.

## 1.4. Thesis Structure

This thesis reviews the effectiveness of current forecasting processes, introduces a model to aid in revenue planning using fab announcement data, and reviews the trade-offs involved in capacity planning. Chapter two examines the current process for performing top-down forecasting. Its effectiveness is measured and assumptions that have been

brought into question are outlined. Chapter three reviews the development of a bottoms-up forecasting model which is meant to address some of the concerns with the top-down approach, as well as to take advantage of the detailed market data that now exists on worldwide fab capacity. The effectiveness of this model is compared against the current process. Chapter four addresses the operational impact of the inevitable error that will exist in any forecasting tool. A financial model that has been developed is reviewed which quantifies the trade-offs between excess capacity and lost sales given the market conditions and forecast error. Chapter five explores how either of the two models discussed in the first two chapters could be used to assess the impact of predicted technology changes on the ATE market. This will help to highlight some of the strengths and weaknesses of each approach discussed and demonstrate an application of the models to more strategic planning. Finally, Chapter six summarizes the key findings. This includes abstracting some of the detailed results into more general recommendations. Also, possible directions for future work are identified.

# 2. Top-Down Forecasting

Teradyne purchases forecasts of semiconductor industry revenues from Dataquest, a leading consulting firm to semiconductor manufacturers. They have hard copies of these reports dating back to 1987. They also have diligently tracked the buy-rate for their industry over time, and use this in conjunction with Dataquest forecasts to help in estimating their own future sales. However, reviews of forecasting effectiveness have been focused on internal numbers, which are only a portion of the entire industry. These are heavily influenced by expected market share improvements and specific account wins. The goal of this section of the study is to investigate the variability in forecast error of the underlying data that is used as a basis for internal estimates. This will give some understanding to how effective the current top-down revenue planning process can be. The overall goal of this section of the research is to set up a baseline against which to compare the bottoms-up forecast model.

## 2.1. Model Description

The model used in the top down forecasting technique is very simple. It can be written as follows, where $ATE_t$ represents the revenue in the ATE market at time $t$, $BR_t$ is the buy-rate for the given time period, and $SC_t$ is the revenue for the semiconductor market:

$$ATE_t = BR_t \times SC_t \tag{2.1}$$

This model can be used for the entire market, or for a particular segment. First, the estimate of revenue for a selected group of devices is obtained from Dataquest. Next a value for the buy-rate for the given forecast is determined. Typically, trends in past buy-rates are determined and carried forward to future years. Finally, the revenue and buy-rate forecasts are multiplied to predict ATE demand.

## 2.2. Evaluation of the Model

In order to evaluate the effectiveness of this model, forecasts and actual values from 1987 to 1996 were examined. Dataquest publishes a spring and fall report that contains semiconductor revenue predictions for the current year, as well as for each of the following five years. Therefore, the shortest forecast that exists is one quarter in duration, and there is a forecast every two quarters up to a maximum of 21 quarters in length. For the purposes of this study, one quarter to thirteen quarter forecasts were examined.

The report also breaks down the semiconductor market into device type. In conjunction with Teradyne's typical forecasting process, various types are grouped into the memory, logic, or analog markets, or are identified as not requiring ATE, as in discrete or optical devices. The logic market consists of both microprocessors/microcontrollers and logic ASICs. The analog market is the combination of pure analog devices and hybrid ASICs. The sum of the three markets that use ATE makes up the total integrated circuit (IC) market. In this study, forecast error is assessed for each market individually as well as in total.

Two common parameters used in reviewing forecasting models were used as measures of accuracy, mean square deviation (MSD) and BIAS. As a slight deviation from most applications, both were normalized to create a percentage value. This was done to compensate for the large growth in the industry. The assumption is that the variability in forecasts in this market is proportional to the market size. A review of the data supports this assumption. The resulting formulas for the calculation of the two parameters are as follows, where f(t) is the forecast at time t, A(t) is the actual value, and n is the number of forecast/actual pairs observed:

$$\mathbf{BIAS} = \sum_{t=1}^{n} \frac{[(f(t) - A(t))/A(t)]}{n} \tag{2.2}$$

$$\mathbf{MSD} = \sum_{t=1}^{n} \frac{[(f(t) - A(t))/A(t)]^2}{n} \tag{2.3}$$

Interpreting the results of the study on forecast accuracy requires an understanding of what these calculations demonstrate. The BIAS, which can be either negative or positive, is a measure of the accuracy on average. If the BIAS is negative, the forecast tends to underestimate the actual value. The opposite also holds true. It is important to note that a zero bias does not mean that the forecasts are always accurate, only that over estimates are balanced by under estimates. Conversely, the MSD can only be positive, and is an average squared size of error on the forecast. The square root of the MSD is reported in all of the charts and tables that follow to express this error in more natural units. A perfect forecasting tool would have a zero BIAS and MSD.

### 2.2.1. Market Forecasts for Integrated Circuits

The accuracy of any model has an upper limit, which is set by the data on which it is based. Therefore, the first step in this study was to review the effectiveness of Dataquest's forecasts for each of the market segments, as well as the total IC market. BIAS and $MSD^{1/2}$ values were calculated by lumping forecasts with the same duration. Reports from 1987 through 1996 were used. Table 2.1 shows the results of this study.

| IC Market | Statistic | Forecast Duration | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 1 Qtr | 3 Qtrs | 5 Qtrs | 7 Qtrs | 9 Qtrs | 11 Qtrs | 13 Qtrs |
| Total IC's | BIAS | -0.6% | -1.1% | -0.8% | -4.3% | -6.5% | -8.6% | -5.2% |
| | $MSD^{1/2}$ | 4.3% | 9.3% | 15.5% | 16.1% | 18.1% | 21.6% | 22.4% |
| Memory IC's | BIAS | -2.1% | 0.5% | -0.4% | -4.6% | -9.5% | -11.0% | -8.6% |
| | $MSD^{1/2}$ | 7.6% | 21.2% | 34.7% | 32.5% | 35.0% | 38.4% | 37.5% |
| Logic IC's | BIAS | -0.5% | -1.5% | -1.4% | -3.6% | -5.3% | -7.3% | -4.9% |
| | $MSD^{1/2}$ | 4.2% | 6.1% | 9.6% | 12.7% | 12.1% | 16.9% | 17.0% |
| Mix Signal IC's | BIAS | 0.5% | -0.9% | 1.2% | -1.1% | -2.1% | -2.7% | -1.0% |
| | $MSD^{1/2}$ | 4.5% | 5.2% | 9.3% | 8.9% | 10.7% | 11.9% | 12.9% |

**Table 2.1 BIAS and $MSD^{1/2}$ for Semiconductor Revenue Forecasts**

One of the noticeable characteristics of the data is that there is a negative BIAS that exists in all three market segments for forecasts that are greater than five quarters. In Figure 2.1 the BIAS values by market are plotted by forecast duration. This grows larger as the duration of the forecast increases. In particular, the memory market rapidly drops off to values around -10%. This could be a result of the particular time period tested, but may also suggest that market predictions tend to be conservative. This certainly has a strong influence on the effectiveness of the top-down approach.

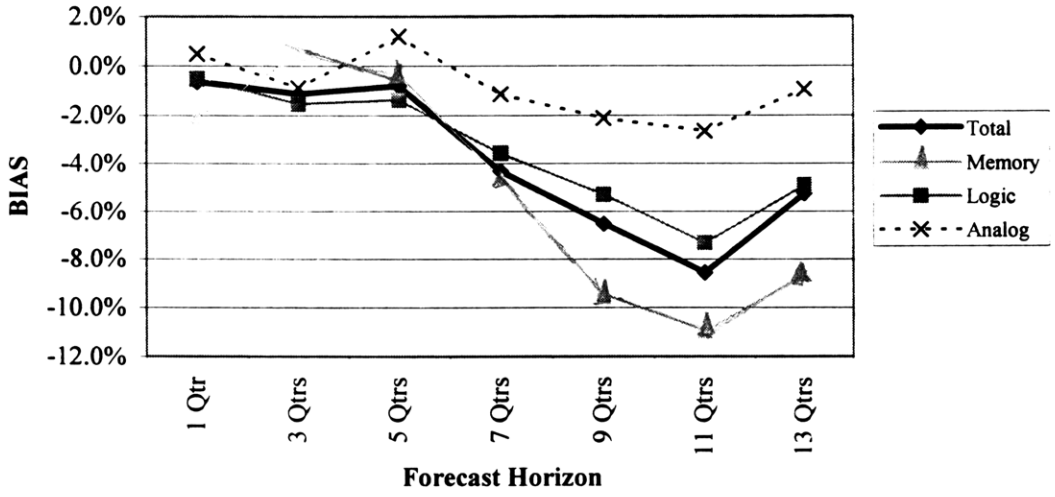



**Figure 2.1 BIAS for the IC Revenue Forecasts (1987-1996)**

As would be expected from any forecasting model, the $MSD^{1/2}$ grows as the duration is increased. In Figure 2.2, all three market segments show an upwardly sloping line for the calculated $MSD^{1/2}$ over duration. Once again however, there is a big difference between the groups. The memory market has a quick increase to greater than 20% in just three quarters, where as the others never reach this value. Again, all of the results could be attributed to the time span that the data represents. However, if it is assumed that this is representative of Dataquest's forecasting accuracy, than a 7% increase can be expected in $MSD^{1/2}$ per year in duration for the market as a whole.

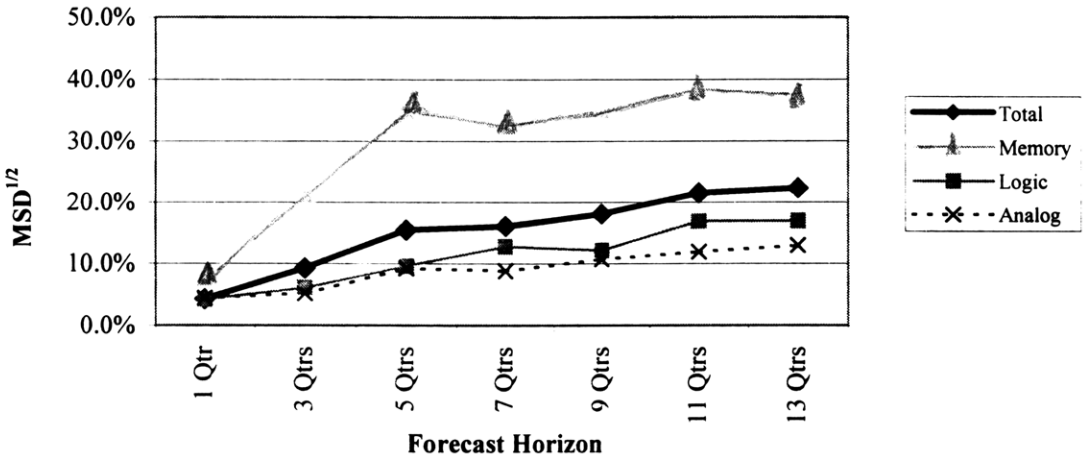



**Figure 2.2 $MSD^{1/2}$ for the IC Revenue Forecasts (1987-1996)**

### 2.2.2. Buy Rates

An important step described above is the selection of a buy-rate for the top-down approach. Teradyne has tracked this ratio over time and has searched for trends that might help in predicting what it will be in the future. The typical method has been to look for an exponential decay. In this section of the study, both a linear and exponential regression were performed to try to understand the trends that might exist in this ratio over time. Buy-rates from 1983 through 1996 were used and values were determined for each market segment. The data sources consisted of Dataquest's report of actual revenue for each semiconductor type per year as well as Prime Research's report of actual ATE revenue. Table 2.2 lists the coefficients from each of the regression tests, as well as the $R^2$ value, which serves as a measure of the accuracy of the regression model. Line fits from the regression results can be seen in Appendix A.

| ATE Type | Exponential Regression | | Linear Regression | |
|---|---|---|---|---|
| | Decay/Year | $R^2$ | Slope/Year | $R^2$ |
| All ATE | 95.64% | 0.716 | 0.15% | 0.688 |
| Memory ATE | 95.74% | 0.400 | 0.15% | 0.373 |
| Logic ATE | 93.64% | 0.888 | 0.19% | 0.852 |
| Analog ATE | 99.01% | 0.074 | 0.04% | 0.068 |

**Table 2.2 Parameters from Buy-Rate Regressions**

The data supports the existence of a general trend in which the buy-rate is decreasing over time. This proves to be most significant in the logic market segment. There was a weak statistical significance to this trend in the memory segment and relatively no significance in the analog market. A possible explanation for the lack of statistical significance for the memory segment is that the cyclicality in this market has had the most dramatic impact, especially on pricing. Fluctuations in memory manufacturer's revenues drown out any downward trend in the buy-rate. The analog market on the other hand is less cyclical, but is less cost focused than technology focused as compared to the logic segment. Therefore, less has been done to reduce the cost of test.

Although there is a great deal of disparity between the market segments, the coefficients from the exponential regression will be used for each segment to determine the forecasted buy-rate value in the overall examination of the top-down forecasting model. This matches the process that is used internally to Teradyne most closely, and has the most plausible long-term result.

### 2.2.3. ATE Forecasts Using Market Data and Buy Rate Trends

ATE forecasts were generated by multiplying the forecasted revenue for a given market segment with its effective buy-rate. Revenue forecasts were taken from Dataquest as described above, from 1987 to 1996. Buy-rates were determined by multiplying the previous year's ratio by the calculated decay coefficient raised to the duration of the forecast. BIAS and $MSD^{1/2}$ values were calculated for the model, again combining forecasts by duration to determine values for these parameters. The ATE market was split into segments corresponding to the semiconductor markets by matching the tester type to the device that it tests. Therefore, actual ATE revenues were compared with the

model's forecast in total and by market segment. The results are shown in Table 2.3.

| ATE Market | Statistic | Forecast Duration | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | 1 Qtr | 3 Qtrs | 5 Qtrs | 7 Qtrs | 9 Qtrs | 11 Qtrs | 13 Qtrs |
| Total ATE | BIAS | -2.1% | -2.5% | -4.8% | -7.4% | -9.2% | -10.3% | -6.7% |
| | $MSD^{1/2}$ | 11.5% | 14.5% | 18.3% | 23.0% | 25.1% | 29.4% | 31.6% |
| Memory ATE | BIAS | -4.1% | -2.7% | -9.3% | -10.0% | -14.7% | -12.8% | -11.1% |
| | $MSD^{1/2}$ | 24.0% | 25.9% | 32.5% | 41.9% | 43.7% | 51.8% | 49.8% |
| Logic ATE | BIAS | -0.2% | -1.1% | -1.4% | -3.5% | -3.6% | -5.3% | -2.1% |
| | $MSD^{1/2}$ | 8.9% | 10.6% | 12.1% | 15.3% | 13.8% | 18.7% | 21.3% |
| Analog ATE | BIAS | -0.6% | -1.5% | -3.8% | -5.7% | -8.3% | -8.5% | -7.7% |
| | $MSD^{1/2}$ | 13.3% | 16.5% | 20.1% | 21.3% | 23.4% | 24.7% | 27.6% |

**Table 2.3 BIAS and $MSD^{1/2}$ for Top-Down Forecasting Model**

Similar to the underlying semiconductor revenue predictions, there is a negative BIAS in all three ATE market segment. However, the rate at which it increases as the duration increases is significantly larger. The memory ATE market reaches as low as –15%. The BIAS values for the top-down model by market and forecast duration are plotted in Figure 2.3. Again, the negative BIAS may be specific to the time period that was used. However, this suggests that this technique produces conservative estimates.

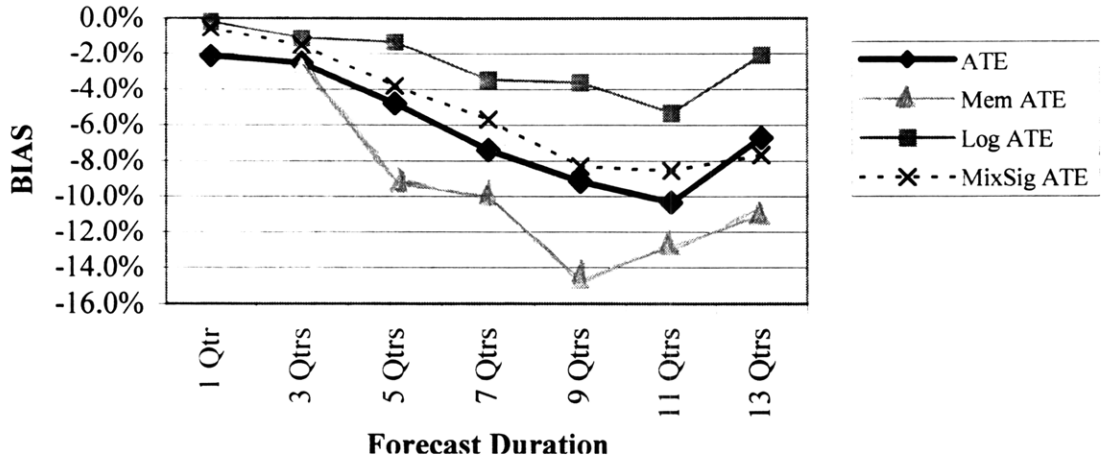



**Figure 2.3 BIAS for Top-Down Forecasting Model (1987-1996)**

The same relationship between semiconductor forecast BIAS and the top-down forecasting model BIAS exists in their $MSD^{1/2}$. The shape of the $MSD^{1/2}$ curves are the same for both, however the parameter grows much more rapidly in the ATE forecast. Also, just as in BIAS measurement, there is a big difference between the market segments. The memory ATE market increases to over 40% after two years, where as the others never reach this value. The model for the market as a whole produced an $MSD^{1/2}$ that increased by approximately 9% per year. Figure 2.4 is a plot of the parameter for the various forecast durations.

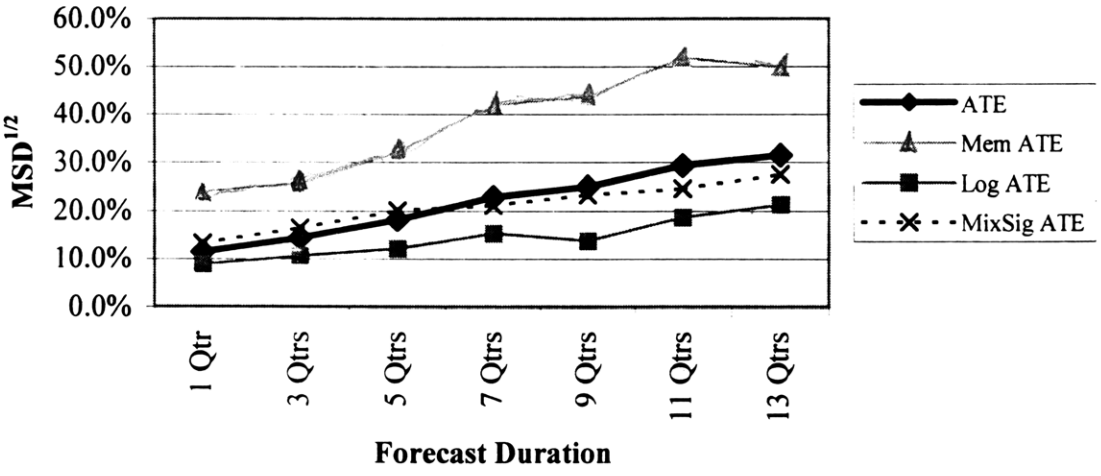



**Figure 2.4 $MSD^{1/2}$ for Top-Down Forecasting Model**

### 2.2.4. Results Summary

A model can only be as accurate as its underlying data. As was the case in this study, it will likely be worse because of the variability that is present in model. As expected, both the BIAS and $MSD^{1/2}$ were larger in value for the top-down forecasting model than the semiconductor forecasts themselves. This resulted in the following characteristics for the total ATE market estimates:

- A one quarter $MSD^{1/2}$ of 10% which increases by 9% per year.
- A negative BIAS which grows more negatively per quarter.

This suggests that forecasts on average will be conservative and have errors reaching close to 50% for five year estimates.

Also, results differed greatly between the market segments. The memory ATE market was less predictable, with a BIAS value of –9% and $MSD^{1/2}$ of 33% for a forecast with a five quarter duration. The logic ATE market had a BIAS of –1% and $MSD^{1/2}$ of 12% for the same type of forecast. The analog ATE market fell in between the two.

### 2.3. Assumptions in to Top-Down Forecasting

In order to understand the sources of error in the forecasting model, it is important to review the assumptions on which it is based. This will also address the possible reasons for the discrepancies in the different market segments. The two assumptions that are fundamental to the success of the model are also the ones that are called into question the most. They are:

- Semiconductor manufacturer's main influence in determining when to purchase ATE is their current revenue.
- Past performance is a good predictor of future action.

There are arguments both for and against the accuracy of the first assumption, that the level of IC revenue drives ATE purchases. Certainly when money is tight for semiconductor manufactures, the purchase of capital equipment and other durable goods is likely to be postponed. In addition, when sales are slow, there is less of a need for test. However, the price of devices is also directly connected to semiconductor revenue. Decreases in price without corresponding decreases in volume would drive total revenue down, without a reduction in the need for ATE. Teradyne has looked for other factors that correspond to the need of their customers to buy their product. With this as a goal, a study was done to compare the strength of correlation between ATE revenue, IC revenue, and IC units shipped for a given year. The values for these three parameters were collected from 1984 through 1996. The results of the correlations are shown in Table 2.4.

**Total Market**

| | IC Units | IC Rev | ATE Rev |
|---|---|---|---|
| IC Units | 1.000 | - | - |
| IC Rev | 0.914 | 1.000 | - |
| ATE Rev | 0.853 | 0.972 | 1.000 |

**Logic Market Segment**

| | IC Units | IC Rev | ATE Rev |
|---|---|---|---|
| IC Units | 1.000 | - | - |
| IC Rev | 0.710 | 1.000 | - |
| ATE Rev | 0.634 | 0.972 | 1.000 |

**Memory Market Segment**

| | IC Units | IC Rev | ATE Rev |
|---|---|---|---|
| IC Units | 1.000 | - | - |
| IC Rev | 0.930 | 1.000 | - |
| ATE Rev | 0.879 | 0.932 | 1.000 |

**Analog Market Segment**

| | IC Units | IC Rev | ATE Rev |
|---|---|---|---|
| IC Units | 1.000 | - | - |
| IC Rev | 0.983 | 1.000 | - |
| ATE Rev | 0.918 | 0.937 | 1.000 |

**Table 2.4 Correlation Coefficients Between IC Units, IC Revenue, and ATE Revenue**

In fact, ATE revenue did show a greater correlation to IC revenue than to IC units. This was true in the ATE market as a whole, as well as in all three market segments. However, because of the conflicts mentioned above, there is still uncertainty around the first assumption in the top-down forecasting model.

The second assumption, that past performance is a good predictor of future action, also has drawn criticism. The selection of a buy rate is determined by projecting past trends to subsequent years. Similarly, semiconductor revenue forecasts are heavily influenced by trends found in previous years. Certainly, dramatic changes in the current paradigm would seriously affect the use of this model. Perhaps more importantly, transitions from growth periods to downturns, and vise versa, are missed. Recognition of these swings is critical to controlling costs and maintaining adequate customer service levels.

The motivation behind the bottoms-up forecasting model described in the next section is to address some of the questions behind these assumptions. In particular, semiconductor manufacturer's existing and planned fab capacity, which has become increasingly more visible to the public, is used as a the basis for ATE demand. Also, this information is not a simple interpolation of past performance, as is the case with revenue forecasts. Instead, it is the ATE customer's own prediction of their future action. With an understanding of the accuracy of the top-down approach, how well the bottoms-up model addresses the possible flaws in previous assumptions can be measured.

# 3. Bottoms-Up Forecasting Model

There are several different databases available that focus on worldwide fab capacity. Strategic Marketing Associates (SMA) publishes a database through SEMI entitled the International Fabs on Disk. This contains a variety of information on announced and existing fabs, including location, wafer size, line width, and wafer starts per month (WSM). SMA also publishes a database which tracks the construction and equipment expenditures made by semiconductor manufacturers in new fabs. Other sources exist which also track these and other characteristics of worldwide fab capacity. However, little has been done to use this data to determine the relationships between semiconductor capacity increases and ATE demand. This section of the study addresses this issue by performing the following:

- Combining data from different relevant databases by matching specific entries as well as sorting information into related groups. This focused on using the two SMA databases mentioned above.
- Using regression techniques to identify and characterize relationships.
- Performing other basic statistical analyses to support regression findings and to fill holes required for a complete bottoms-up model.
- Interviewing key representatives from Teradyne's customer base to both perform a sanity check on previously identified relationships as well as develop new ideas.

The overall goal of this section of the research is to see if a bottoms-up approach has a narrower range of forecast error as compared to the top-down approach. It is thought that this method can address some of the assumptions from the top-down model that might be troublesome.

## 3.1. Model Description

After reviewing results from statistical studies, and interviewing both Teradyne employees and customers, a model was formulated. It consists of a group of five

equations based on ratios of key fab and market data. The first step in the calculation is to determine the expected ATE revenue generated from purchases of wafer sort testers to support new fab capacity. This is achieved by multiplying capacity increase projections by the proportion of processing equipment dollars that is typically spent on wafer sort ATE. This representation can be expressed in equation form. Here $\mathbf{ATE}_{\mathbf{NewFab}}$ is the expenditures on ATE for wafer sort as a result of new fab capacity, $\mathbf{CAP}_{\mathbf{8"WSM}}$ is the new semiconductor capacity in 8" equivalent wafer starts per month[1], and $\mathbf{Equipment}_{\mathbf{NewFab}}$ is the expenditures on capital equipment as a result of new fab capacity:

$$\mathbf{ATE_{NewFab}} = \mathbf{CAP_{8"\,WSM}} \times \frac{\mathbf{Equipment_{New\,Fab}}}{\mathbf{CAP_{8"\,WSM}}} \times \frac{\mathbf{ATE_{NewFab}}}{\mathbf{Equipment_{New\,Fab}}} \tag{3.1}$$

Historical ratios of spending on final test ATE as compared to wafer sort, and characterization ATE to wafer sort are then used to determine the total amount of revenue generated. The baseline value for $\mathbf{ATE}_{\mathbf{NewFab}}$ is multiplied with historical ratios to determine each ATE application's projected revenues to support new capacity. The different applications are then summed to calculate a total. The next three equations summarize these relationships:

$$\mathbf{ATE_{NewTest}} = \mathbf{ATE_{NewFab}} \times \frac{\mathbf{ATE_{NewTest}}}{\mathbf{ATE_{NewFab}}} \tag{3.2}$$

$$\mathbf{ATE_{NewChar}} = \mathbf{ATE_{NewFab}} \times \frac{\mathbf{ATE_{NewChar}}}{\mathbf{ATE_{NewFab}}} \tag{3.3}$$

$$\mathbf{ATE_{NewTotal}} = \mathbf{ATE_{NewFab}} + \mathbf{ATE_{NewTest}} + \mathbf{ATE_{NewChar}} \tag{3.4}$$

---

[1] Ratios of wafer areas are used to adjust the capacity levels for fabs producing with wafers other than 8" in diameter.

Where $\mathbf{ATE}_{NewTest}$ represents expenditures on ATE for final test as a result of new fab capacity, $\mathbf{ATE}_{NewChar}$ is the expenditures on ATE for characterization as a result of new fab capacity, and $\mathbf{ATE}_{NewTotal}$ is the total expenditures on ATE as a result of new fab capacity.

The final step in determining a forecast using this model is to multiply the total ATE revenue expected to support new semiconductor capacity by a ratio which relates it to total ATE spending. This will help to capture ATE purchases that are unrelated to capacity increases such as ongoing support, service, or upgrades. The last equation for this model is as follows, where $\mathbf{ATE}_{Total}$ is the total expenditures on ATE for both new and existing capacity:

$$\mathbf{ATE}_{Total} = \mathbf{ATE}_{NewTotal} \times \frac{\mathbf{ATE}_{Total}}{\mathbf{ATE}_{NewTotal}} \tag{3.5}$$

## 3.2. ATE / Fab Capacity Relationships

The main sources of quantitative data for determining the ratios listed in the equations above were SMA's International Fabs on Disk and the Sourcebook on New Fab Expenditures. These databases were combined by matching entries. Each fab was classified into one of five catagories, foundry, logic, memory, analog, and memory/logic. This was based on the devices that it manufactured, similar to the segmentation of the markets in the top-down approach, and the market that it served. Table 3.1 shows the actual values used for all the parameters in the model. The following sections discuss how these values were selected.

| Parameter | Fab Type | | | | | |
|---|---|---|---|---|---|---|
| | ALL | Foundry | Logic | Memory | Analog. | Memory/ Logic |
| $\frac{Equipment_{New\ Fab}}{CAP_{8"\ WSM}}$ | 0.027 | 0.029 | 0.033 | 0.028 | 0.024 | 0.016 |
| $\frac{ATE_{NewFab}}{Equipment_{New\ Fab}}$ | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 | 0.09 |
| $\frac{ATE_{NewTest}}{ATE_{NewFab}}$ | 1.33 | 1.33 | 1.33 | 1.33 | 1.33 | 1.33 |
| $\frac{ATE_{NewChar}}{ATE_{NewFab}}$ | 0.33 | 0.33 | 0.33 | 0.33 | 0.33 | 0.33 |
| $\frac{ATE_{Total}}{ATE_{NewTotal}}$ | 1.12 | 1.12 | 1.12 | 1.12 | 1.12 | 1.12 |

**Table 3.1 Parameters for the Bottoms-Up Forecasting Model**

### 3.2.1. Fab Equipment / Fab Capacity Ratio

The Sourcebook on New Fab Expenditures outlines equipment expenditures for over 300 specific fabs. Some are still in the construction phase, or were older fabs that were being completed during the start of the database. However, 174 had been followed from initial ground breaking through complete facilitation. These were separated into the five device type groups. The value for the ratio of equipment expenditures to wafer start per month of fab capacity was calculated by performing linear regressions for total equipment expenditures verses 8" equivalent wafer starts per month. Table 3.2 shows the results from this study. The line fits from the regressions can be seen in Appendix A.

| Regression Parameter | Fab Type | | | | | |
|---|---|---|---|---|---|---|
| | ALL | Foundry | Logic | Memory | Analog | Memory/ Logic |
| Slope (Equip $M / 8"eq WSM) | 0.027 | 0.029 | 0.033 | 0.028 | 0.024 | 0.026 |
| $R^2$ | 0.606 | 0.774 | 0.585 | 0.683 | 0.736 | 0.191 |

**Table 3.2 Regression Results for Fab Equipment verses Fab Capacity**

As an example to demonstrate the interpretation of the ratios, a new memory fab would typically be built to support 30,000 WSM. Using the calculated ratio, this fab would require $840 M worth of manufacturing equipment. This number corresponds to estimates that over 75% of the one billion dollar plus fab costs are spent on equipment.

In reviewing the specific ratios calculated, the logic segment proved to require the largest equipment expenditure. This could be supported by the fact that these devices require manufacturing equipment on the leading edge of technology and that this market is not as cost competitive as the memory segment. Also, foundries proved to have the tightest distribution around the regression line. Their construction does tend to follow a specific cost and operational model.

### 3.2.2. Fab ATE / Fab Equipment Ratio

The ratio of wafer sort ATE expenditures to fab equipment expenditures was taken from a study done by SMA. Their findings showed that on average, semiconductor manufacturers spend 9% of their new fab equipment budget on wafer sort ATE. This is also supported by data collected by VLSI Research. They report revenues collected in all semiconductor manufacturing equipment markets. The average ratio of wafer sort ATE revenue (adjusted from total ATE by ratios listed in the next section) to total wafer processing equipment revenue was 9.1% for the time period of 1981-1996. The standard deviation of this measure was 1.5%. When combined with the example supplied above, the parameters suggest that for a new 30,000 WSM memory fab, approximately $76M of wafer sort ATE is required.

### 3.2.3. Other ATE / Fab ATE Ratio

The determination of the ratios for final test ATE to wafer sort ATE and characterization ATE to wafer sort ATE was primarily accomplished through interviews. The values for these parameters, 1.33 and 0.33 respectively, were also supported by quantitative data. VLSI Research has been attempting to segregate ATE sales into application since 1993. The ratios that can be extracted from their data are 1.10 and 0.40, although more recent data is closer to the values reported by Teradyne customers.

This results in the following breakdown of revenue for the various applications of ATE; 37.5% on wafer sort, 50% on final test, and 12.5% on characterization. Continuing the 30,000 WSM memory fab example, expenditures would be $76M on wafer sort ATE, $102M on final test ATE, and $25M on characterization ATE for a total of $203M. This corresponds to internal estimates of approximately $200M to $250M in ATE for a new memory fab.

The last parameter required is the ratio of ATE revenue generated from new fab capacity to other ATE revenue. Its value was determined by reviewing ATE expenditures reported by SMA that were connected to new fab construction from 1994 through 1996 and comparing it against total reported ATE revenue. This was a viable process because the SMA database is a complete set of all new fabs. The ratio remained fairly constant for all three years at 1.12. These results suggest that 89% of all ATE expenditures from semiconductor manufactures are the result of new capacity.

### 3.2.4. Ramp Rate of Fab Capacity

The model also needs to address the relationship between the announced year of first wafer production for the various fabs to actual capacity increases. First a measure of how quickly a fab reaches its full capacity was needed. General consensus in interviews with Teradyne employees and customers was that for a 30,000WSM fab, the typical ramp rate is approximately 5,000 WSM. Therefore, full capacity is reached in 6 quarters. After performing some statistical analysis on the fab database, it was determined that the average number of WSM per fab listed is approximately 20,000. Using 5,000 WSM per quarter as a basis, this corresponds to an average of four quarters to obtain full capacity.

Fab announcements generally only specify the year that production will begin. Because the ramp to full capacity takes 4 quarters, fabs started in the end of a given year will actually drive most of its ATE demand in the following year. Therefore some process was needed to assign fab capacity announced to start in the same year throughout the 4 quarters. For the purposes of the model it is simply assumed that it is equally distributed.

### 3.2.5. Forecast Calculations

It was important that the model be implemented in such a way as to facilitate its use in the future. Microsoft® Excel was used as the application. The model was constructed by linking a series of spreadsheets, which consisted of an input/output worksheet and two calculation sheets. Appendix B shows a typical view of the input/output screen.

## 3.3. Evaluation of the Model

In order to evaluate the effectiveness of this model, forecasts and actual values from 1994 through 1996 were examined. SMA first published its International Fabs on Disk database in October 1994, and has updated it every quarter since. All nine revisions between this first issue and October 1996 were included in the study. Later issues could not be used since actual values for 1997 have not been determined.

Capacity levels in years that have been only partially completed, or are sometime in the future, can be considered "forecasts". Reported capacity for 1994 in the October 1994 issue of the database has a forecast duration of one quarter, and capacity levels in 1995 have a five quarter duration. Therefore, there are forecast durations in quarterly increments. Because of the nature of fab announcements, the accuracy of the database falls off sharply after two years. Therefore, the longest forecast duration included in the study was seven quarters.

To align with the model parameters, the fabs in the database were classified into the five different product or market types. During all of the calculations, the groups were kept separate from each other. However, it was impossible to break down actual ATE revenue so that a correlation could be made to each of the five segments. Therefore, this study focused on assessing forecast error for the ATE market as a whole. Again, the two parameters, mean square deviation (MSD) and BIAS, were used to measure the accuracy of the model. The same normalization step described in Section 2.2 was used.

### 3.3.1. Forecast Results

Capacity forecasts from each revision of the database were separately entered into the Excel based model. Resulting ATE revenue predictions were then compared with actual

values taken from Prime Research marketing reports. Forecasts with the same duration were grouped to calculate the accuracy parameters. Results were compared with those obtained from the top-down forecasting model testing the same time period.

| Parameter | Forecast Duration | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1Qtr | | 3Qtrs | | 5Qtrs | | 7Qtrs | |
| | Top-Down | Bottoms-Up | Top-Down | Bottoms-Up | Top-Down | Bottoms-Up | Top-Down | Bottoms-Up |
| BIAS | -14% | 0% | -12% | 2% | -21% | -5% | -16% | -8% |
| $MSD^{1/2}$ | 15% | 13% | 20% | 35% | 24% | 17% | 16% | 8% |

**Table 3.3 BIAS and $MSD^{1/2}$ for Bottoms-Up and Top-Down Forecast Models**

The most noticeable difference between accuracy measures between the two models is the BIAS. For the bottoms-up forecasting tool, this parameter is significantly closer to the desired value of zero. There is still a drift towards a negative BIAS value as the duration of the forecast increases. However, over the four different durations compared, the BIAS of the bottoms-up model is on average 13% closer to zero. Figure 3.2 shows a plot of the two parameters for the tested forecasts. One possible concern with these results is that the parameters used in the model are correlated to the forecasts used. Although this was avoided as much as possible, some ratios used were primarily derived from the database. Also, it is possible that the improvement to the BIAS is specific to the time period tested. There were only nine revisions of the database tested, which is not a significant amount of data on which to base any clear conclusions.

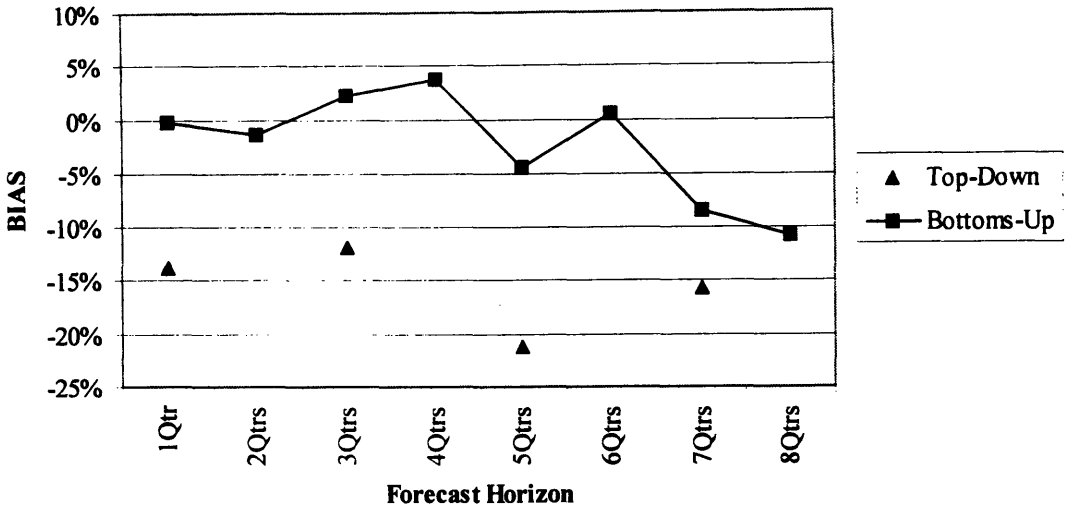



**Figure 3.2 BIAS for Bottoms-Up Forecast Model (Oct 94 – Oct 96)**

The differences between the $MSD^{1/2}$ for the two models are much more difficult to distinguish. Considering the limited amount of data available, the two models appear to have similar $MSD^{1/2}$ values. The expected upward trend as duration increases for both models does not exist. This is definitely a result of the time period and the amount of data studied. The plot of this parameter over the various durations tested is shown in Figure 3.3. A more thorough understanding of the differences between the models will be obtainable as more SMA database revisions are released.

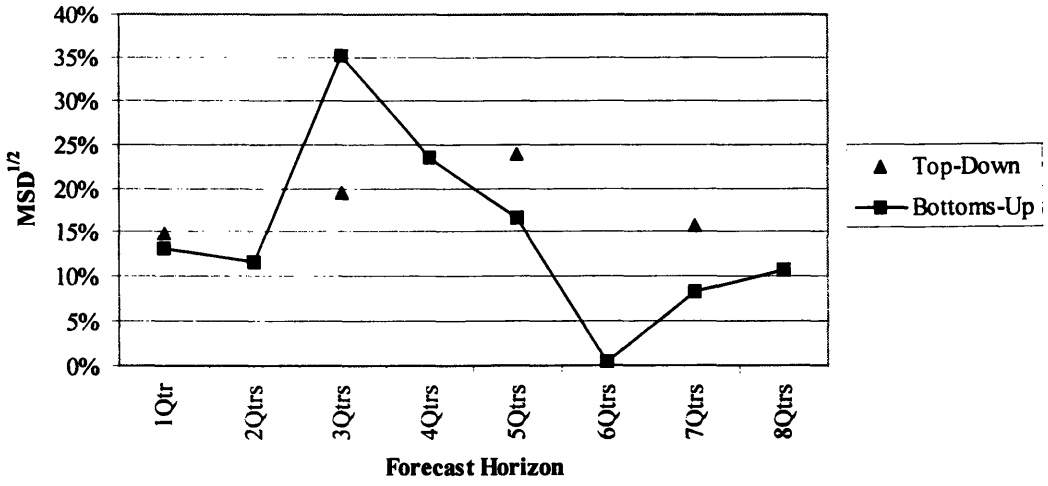



**Figure 3.3 $MSD^{1/2}$ for Bottoms-Up Forecasting Model (Oct. 94 – Oct. 96)**

### 3.3.2. Results Summary

The results of the study comparing accuracy of the bottoms-up forecasting model to the top-down model are very preliminary due to the limited amount of data. However, the new model does appear to show promise. For the data analyzed, it had a BIAS closer to zero for all forecast durations and therefore, should have predictions that are not as conservative on average. It is difficult to determine whether or not the MSD has been improved. The model should continue to be used until statistical significance of any improvement can be judged.

Also, there is significant correlation between the two different models. Not only does the data support this, but it also follows from industry practice. Capacity increases are planned when it is expected that semiconductor demand is going to increase. Similarly, semiconductor revenue forecasts increase when announcements of new fabs are made because of expected extra sales. This reinforcing loop tends to insure that the data from the two models coincide. The hope is that timing issues would make the bottoms-up model more resistant to sudden changes. For instance, if there are points in fab construction where full commitment to capacity is reached prior to ATE purchase, the bottoms-up approach would more closely follow the actual timing of demand swings than the easily adjusted semiconductor revenue forecasts. Conversely, it is possible that the error surrounding the accuracy of fab capacity announcements drowns out any possible timing improvements. These answers will only come over time as the error for both models are tracked.

It has been mentioned throughout this thesis that the three market segments reviewed have different characteristics. This includes varying susceptibility to cycles, as well as products that are at different ends of the commodity to functionality differentiated continuum. There was a hope that the bottoms-up model would work well for those segments with devices that are more commodity-like. However, it was difficult to establish with certainty the types of products that a particular new fab will produce. Therefore, the differences in markets could not be exploited. Hopefully, this will change as more an more experience is gained in using the model.

### 3.4. Assumptions in Bottoms-Up Forecasting

This model was formulated to address issues with the assumptions in the top-down approach. In particular, questions concerning whether or not semiconductor manufacturer's revenue is the best indicator of ATE demand, and if forecasts which rely on projections of past performance can be used in such a cyclical market. Here, capacity announcements replace revenue as a predictor of demand. This method is thought to be more grounded on market data than on projections from the past.

However, this model is also based on assumptions that are questionable. As presented, the ratios used in the model remain constant over time. Different fab costs are growing at very different rates, depending on technology. It is not probable that the ratios used will remain constant and it is unclear as to how they might be predicted to change. This challenge may be more difficult than the tracking of changes to the buy-rate over time.

A more fundamental question involves the reliability of the fab announcement. Semiconductor manufacturers are becoming skilled at responding to market demands by delaying or speeding up facilitation to match capacity needs [16]. Projected dates of first wafer manufacture are surrounded by uncertainty that adds to forecast error. As mentioned previously, the work presented here is a first step. Much needs to be done to measure the effectiveness of this model as more and more data is collected.

Forecasting models will have error. The next chapter looks at how to operate most effectively given this fact. This will help to explain the relative importance of working to develop the model discussed in this section, as well as give general guidance in the area of capacity planning in industries with volatile demand.

# 4. Capacity Planning Model

To effectively deal with variability in forecasts for planning, trade-offs must be made between work in process (WIP), cycle time, service levels, capacity, utilization, and quoted lead times. The characteristics of an industry drive which factors, inventory, labor, sales support, etc., have the greatest impact. For example, ATE manufacturers have extremely costly WIP, as a single unit can cost over $2M. But understanding the driving forces does not make the trade-offs simple. The customers of ATE manufacturers are pushing for short lead times, which requires buffers in capacity and WIP to meet swings in demand. At the same time, these customers are demanding cost reductions, which requires lower WIP levels and longer lead times.

Another option for dealing with volatile demand exists if capacity can be increased or decreased swiftly and inexpensively. In the extreme, if ramp times are negligible and free, a process where capacity is set by reacting to demand can be used. Thus the excess costs required for a safety stock to cover variability are eliminated. However, this ideal case is not likely to exist. Rapid increases in capacity usually result in excess labor costs due to overtime and training, and increased material costs due to expediting and quality issues.

This section of the study investigates the trade-offs in capacity planning for ATE manufacturing for any forecast model given its error variability. The following steps were performed for this purpose:

- Investigate the various costs related to a chosen capacity level by reviewing past financial data.
- Examine the current costs related to the requirements for rapid capacity expansion by reviewing financial results during highly volatile time periods.

The goal of this section of the study was not to create an exact quantitative model for determining the optimal capacity planning strategy. Instead, a tool that could give a quantitative feel was sought, which can help in understanding the relevant issues.

Quantitative analysis is performed, only not to the detailed level in which operating decisions could be made on it alone.

### 4.1. Model Formulation

There are various ways to meet demand for a given time period, each having different cost characteristics. The three options considered for this model are with planned capacity, added capacity, or lost sales. Planned capacity is the level at which the manufacturer chooses to operate over a given time period. The manufacturer also has the ability to add incremental levels of capacity at an increase cost during this time. However, this is limited by how volume flexible the particular manufacturing operation is. The final option for meeting demand, losing the sale, is obviously not the most desirable.

It is important to note that these concepts, as well as the model itself, require a time interval component. A timing convention known as periodic review matches closest to Teradyne's practices. Under this scenario, it is assumed that there is a fixed interval at which capacity levels are reviewed, and a fixed amount of lead-time required to achieve the level desired. Six months is considered the standard amount of time required to change capacity levels at Teradyne, with reviews every six months. Therefore, a planned capacity level chosen today will be available in six months and remain at that volume until a year from date. Any changes during the time in which the planned capacity is available falls in the category of added capacity.

The model created is in the form of an optimization problem where the objective is to minimize the cost of meeting customer demand. The decision variable is the level of planned capacity. This set of criteria can be formulated as follows, where Z represents the total cost of meeting demand:

$$\min_{CAP} Z = c_{CAP}\mathbf{CAP} + c_{\Delta DEM}\mathbf{\Delta DEM} + c_{VCAP}\mathbf{VCAP} + c_{LS}\mathbf{LS} \qquad (5.1)$$

The equation consists of four cost components:

- The cost of planned capacity - $c_{CAP}$**CAP**. For this component, $c_{CAP}$ is the marginal cost of a unit of capacity, assuming all costs are variable. **CAP** is the selected level of planned capacity and is the key decision variable for the entire equation. This captures all costs surrounding materials, equipment, space, overhead, and labor for planned levels of capacity.
- The cost of reducing capacity - $c_{\Delta DEM}$**ΔDEM**. Here, the first variable, $c_{\Delta DEM}$, represents the marginal cost of reducing capacity for the next time period by one unit, and **ΔDEM** is the expected amount of excess capacity for the next time period. Due to the cyclical nature of the semiconductor industry, this cost is of great concern to ATE manufacturers. Often the strongest inhibitor to deciding to increase capacity levels is the fear of excessive costs that will be incurred during the following period because of a down swing.
- The cost of added capacity - $c_{VCAP}$**VCAP**. This captures the cost incurred when extra capacity is added during the time period in review, and includes premiums for procurement, space and labor. $c_{VCAP}$ is the marginal cost of a unit of added capacity. **VCAP** represents the expected added capacity needed to meet the demand distribution
- The cost of a lost sale - $c_{LS}$ **LS**. For this last component of cost to meet demand, $c_{LS}$ is the marginal cost of a lost sale, and **LS** is the expect number of lost sales resulting in meeting the demand distribution. Not only is the marginal revenue that would have been realized had the unit been sold captured, but also any follow-on sales such as service and maintenance. This also includes marginal revenues for future unit sales generated.

The optimization problem described above can be thought of as the division of the demand distribution into the three segments. For this model the demand distribution, **D**, is considered normal, with $\mu$ equal to the forecasted value for ATE, and $\sigma$ equal to the $MSD^{1/2}$ of the specific forecasting model. An example is shown in Figure 4.1. The model selects an optimal planned capacity level such that the sum of the expected costs from each segment is minimized.

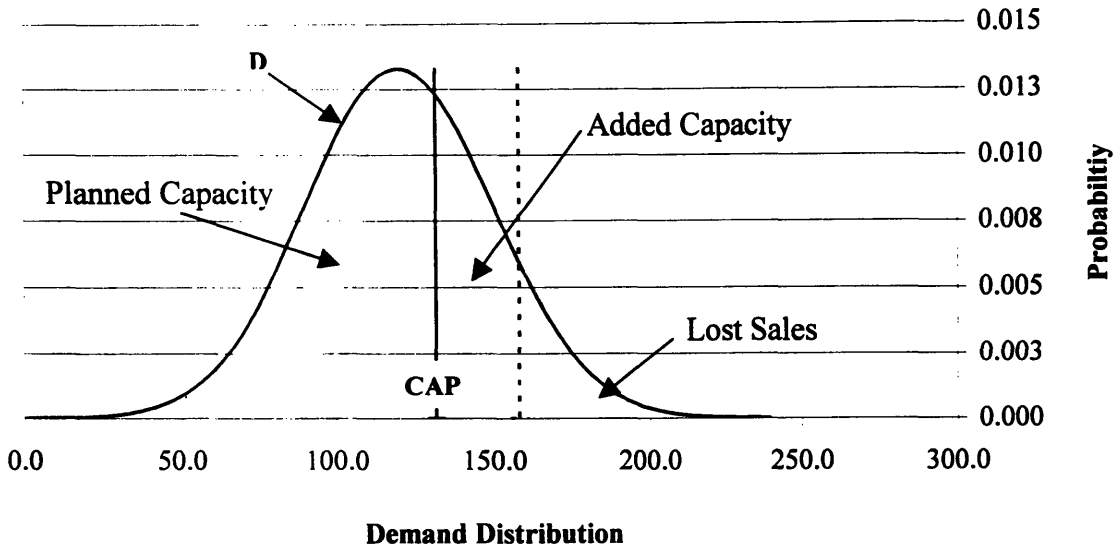



**Figure 4.1 Demand Distribution and Selected Planned Capacity Level**

All of the distribution to the left of the determined level is met by planned capacity and has a cost that is independent of the expected value of this area. The center section of the curve represents added capacity needs. Here, the expected amount over capacity for this area is calculated and multiplied by the appropriate cost. However, for this model, the maximum amount of added capacity is limited, as only a certain amount of extra material, labor and space can be acquired in a restricted amount of time. This imposes a constraint on the optimization, that the amount of added capacity has a maximum. The following equation expresses this relationship, where $\mathbf{MAX}_{VCAP}$ is the maximum amount of added capacity that is possible:

$$\mathbf{VCAP = E[max\{0,\ D - CAP\}] \quad for\ D - CAP < MAX_{VCAP}} \qquad \mathbf{(5.2)}$$

In addition, the marginal cost of the added capacity, $c_{VCA}$ in equation 5.1, is not modeled as a constant. As more and more additional capacity is needed, higher and higher premiums are required to expedite materials, procure space, and hire labor. This is expressed as an exponential growth of a base marginal cost for the first additional unit of

capacity, $c_{VCAPBASE}$. This is represented by the following equation, where **g** is the growth rate of the marginal cost for added capacity:

$$c_{VCAP} = c_{VCAPBASE} \times (1 + g)^{VCAP} \qquad (5.3)$$

The remaining right tail in the demand distribution in Figure 4.1 is the lost sales segment, and is the expected value above the maximum added capacity calculated. This can be expressed in terms of previously described variables as:

$$LS = E[\max\{0,\ D - (CAP + MAX_{VCAP})\}] \qquad (5.4)$$

The other distribution included in the model represents the possible capacity requirements of the next time period, $D_{t+1}$. This was considered a lognormal distribution, with $\mu$ equal to the average percent increase in demand from 1983-1996, and $\sigma$ equal to the standard deviation of these increases. Figure 4.2 shows an example.

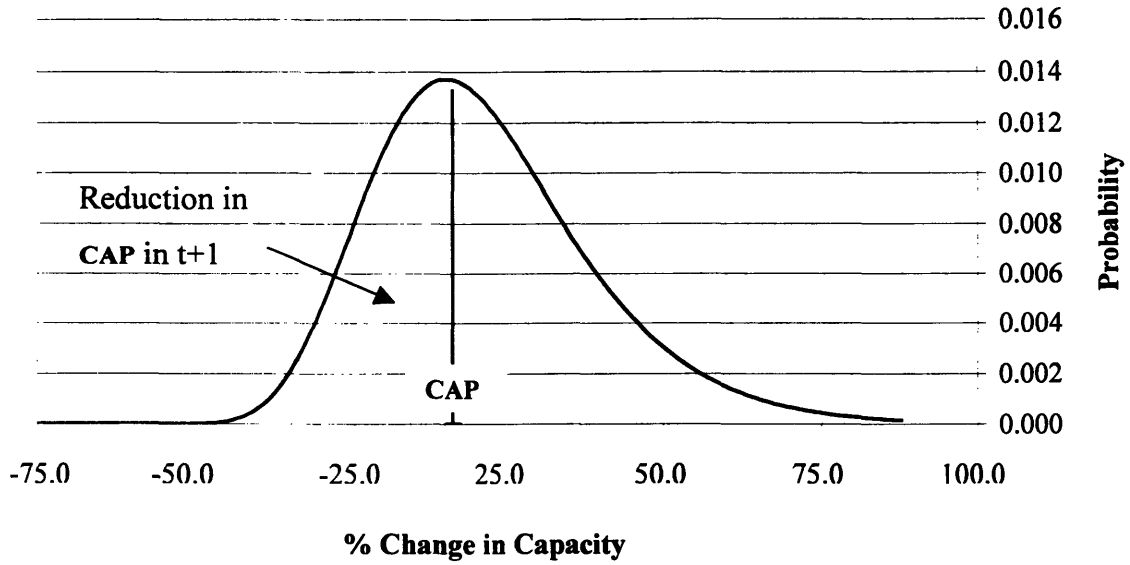



**Figure 4.2 Demand Δ Distribution and Selected Planned Capacity**

Similar to the costs from extracted from the demand distribution, expected values are used to calculate the cost of possible reductions in capacity. Here we are concerned with the area to the left of the selected planned capacity level, which can be summarized by the following equation:

$$\Delta DEM = E[\max\{0, CAP - D_{t+1}\}] \quad (5.5)$$

This represents the probability that reductions in capacity will be required in the following time period. Expected costs for a reduction are included in the optimization.

It is important to note that for any given time period, an exact value of ATE demand will occur. Therefore, this model focuses on the expected costs and can be thought of as the long term running averages for each of these categories.

## 4.2. Selection of Constants

In order to use the model as an aid in capacity planning, it is important to determine accurate values for the constants required. The source for the demand distribution's standard deviation is the results from the testing described in section 2 on the top-down forecasting model. The $MSD^{1/2}$ for a forecast with a five quarter duration matches closest to the timing for the period review, fixed lead time model used. Capacity will come on-line six months from the date it is determined to be needed, and will need to cover six additional months. The mean for the demand distribution was selected to represent a division's forecasted output for a six month time period. Table 4.1 lists the values used as the baseline for this study.

| Distribution | $\mu$ | $\sigma$ |
|---|---|---|
| Demand Distribution | 120 | 30 |
| Demand $\Delta$ Distribution | 138 | 35 |

**Table 4.1 Distribution Parameters for Demand and Demand $\Delta$**

The constants that reflect internal processes were determined by reviewing financial numbers on a specific ATE division with Teradyne.[2] In particular, simple regression techniques were used to understand basic capacity to cost relationships. Figure 4.5 shows a typical line plot from such an analysis. Regression parameters were used as a basis for understanding marginal costs.

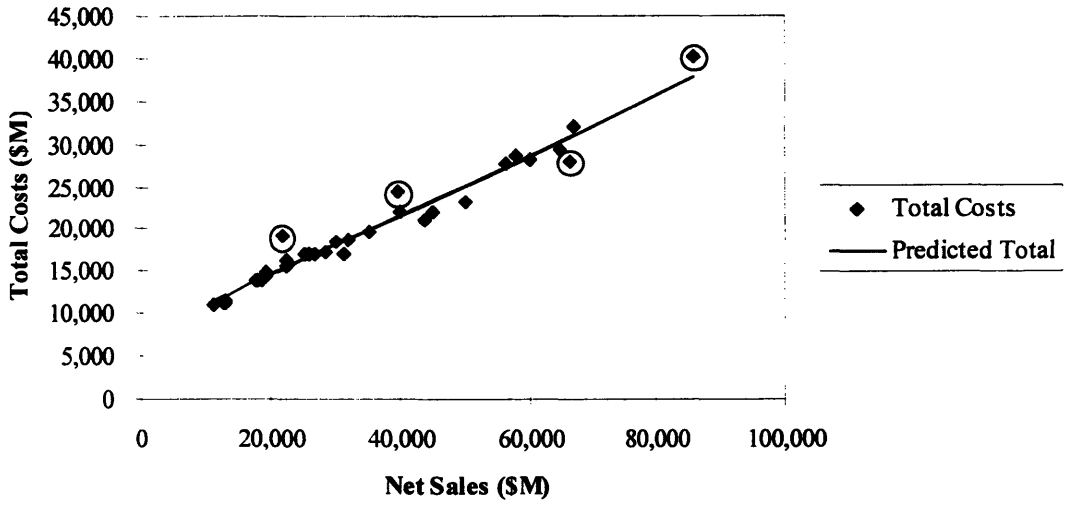



**Figure 4.5 Regression Line Fit: Total Cost Per Revenue Dollar**

Specific points that were further from the regression line were investigated further to understand costs related to over or under capacity. In particular, costs that were related to a requirement to quickly increase capacity were reviewed. Those data points in Figure 4.5 that are circled represent possible candidates to learn about costs incurred during up or down swings. A detailed financial review was performed for those periods to understand the cost factors in such market conditions.

The cost of a lost sale was the most difficult to quantify. A more qualitative approach was taken to settle on baseline values. Marketing and finance personnel within the company were interviewed. Certainly, a variety of opinions existed. However, there was agreement that the cost of lost sales is extremely high due to switching costs and follow-

[2] Values presented in the remainder of this section have been disguised.

on sales. A summary of the values for each of the constants that were derived from internal data can be seen in Table 4.2

| Constant | Value |
|---|---|
| $c_{CAP}$ | $350 |
| $c_{\Delta DEM}$ | $350 |
| $c_{VCAPBASE}$ | $350 |
| g | 0.02 |
| $MAX_{VCAP}$ | 24 |
| $c_{LS}$ | $4,000 |

**Table 4.2 Baseline Constants for the Capacity Planning Model**

## 4.3. Model Use

The first step in using the model to understanding capacity planning trade-offs is to run it using baseline constant values. Then sensitivity analysis is performed to understand how different factors influence baseline results. The decision variable in all cases is the level of planned capacity. Important output values for both baseline and subsequent variations are the level of the decision variable, the expected amount of added capacity required, and the expected number of lost sales. The combination of these values with their appropriate accompanying costs also provides a useful measure of total cost.

### 4.3.1. Calculations

The model was implemented using Microsoft® Excel with the Solver add-in. The distributions within the model were represented by discrete versions with 240 sample points. The input and output were both included on the worksheet. Appendix B shows a typical view of the input/output screen for this model.

### 4.3.2. Baseline Results

Table 4.3 summarizes the results from the baseline case. The optimal planned capacity level is 10% higher than the forecast value. This is driven by the high cost of lost sales. The only reason that this value is not higher is the benefit provided by added capacity.

Amounts listed for added capacity and lost sales are expected values as derived from the demand distribution. As mentioned above, expected values can be considered long term averages and will vary from period to period.

| Output Variable | Value |
|---|---|
| Planned Capacity | 132.0 |
| Added Capacity Need | 2.8 |
| Expected Lost Sales | 1.4 |
| Expected Total Cost ($M) | $56,119 |

**Table 4.3 Baseline Results for the Capacity Planning Model**

### 4.3.3. Sensitivity Analysis - Impact of Forecasting Improvements

In order to understand the impact of reducing the forecast error, sensitivity analysis was performed. The value for the standard deviation of the demand distribution was reduced by 1% and 10%, and model was run under the two scenarios. The results of this study can be seen in Table 4.4.

| Output Variable | Baseline | $\sigma = 29.7$ | $\sigma = 27$ |
|---|---|---|---|
| Planned Capacity | 132.0 | 131.7 | 129.4 |
| Added Capacity Need | 2.8 | 2.8 | 3.0 |
| Expected Lost Sales | 1.4 | 1.4 | 1.2 |
| Expected Total Cost ($M) | $56,119 | $55,885 | $54,061 |

**Table 4.4 Sensitivity Analysis Results for Forecasting Error Improvements**

The resulting optimal fixed capacity was reduced from a 10% increase over the forecast value to 9.75% and 7.8%. The expected total cost reduced 3.7%. These results can serve as a measuring stick to determine if forecasting improvement efforts are worth the investment. They also give a feel for how the accuracy of measurement for the forecast error impacts the use of such a model.

### 4.3.4. Sensitivity Analysis - Impact of Flexibility Improvements

A similar sensitivity analysis was performed on the parameter representing volume flexibility. The value for the maximum amount of added capacity was increased by 1% and 10% from the baseline of 20% of planned capacity. The results of this study can be seen in Table 4.5.

| Output Variable | Baseline | Flex = 20.2% | Flex = 22% |
|---|---|---|---|
| Planned Capacity | 132.0 | 131.8 | 130.5 |
| Added Capacity Need | 2.8 | 2.9 | 3.4 |
| Expected Lost Sales | 1.4 | 1.4 | 1.3 |
| Expected Total Cost ($M) | 56,119 | 56,030 | 55,258 |

**Table 4.5 Sensitivity Analysis Results for Flexibility Improvements**

The resulting optimal fixed capacity was reduced from a 10% increase over the forecast value to 9.8% and 8.75%. The expected total cost reduced 1.5%. Changes in this factor proved to have less of an impact on the output variables than forecast error variation.

Again, this can help in determining the merits of volume flexibility projects. Those opportunities that cost more than the expected return for improving added capacity limits should not be undertaken. These results also help to understand the impact of measurement accuracy of the maximum amount of added capacity on the planning process.

## 4.4. Results Summary

The cost of lost sale dominates the marginal cost of a unit of capacity as well as the cost to reduce capacity. Thus is the driving force for recommendations to implement capacity levels greater than forecasts. Forecast error increases the optimal level chosen, as possible lost sales as a result of demand on the far right of the distribution move farther away from predicted revenues. Therefore, improvements to forecasting models will allow for less capacity buffer. However, the cost of making such an improvement might

be greater than the benefits that could be recognized. Increases in volume flexibility may prove to be an easier, certainly are more quantifiable in the short term.

Most of what has been discussed in this thesis up to now has been tactical. Models for one to two year forecasts, and planning at six-month intervals have been discussed. The next chapter takes a more strategic look at revenue and product planning. Technology often breaks existing paradigms that are integral to tactical approaches. It is important to understand what effects such step function changes could possibly have. Tactical models can be used to help track the impact of the acceptance of such technologies.

# 5. Modeling the Impact of Technology on the ATE Market

Technology can heavily impact the effectiveness of any forecasting model. It can lead to product or process improvements that create step function changes in demand profiles. Or, more dramatically, it can completely break paradigms and make models based on the past obsolete. In the ATE market in particular, the impact of developments and predicted future advances in the area of design for testability (DFT) is expected to seriously affect future revenue growth. The National Technology Roadmap for Semiconductors (NTRS) which is published by SEMATECH and created by the Semiconductor Industry Association was published first in 1992, and subsequently in 1994 and in the end of 1997 [17], [18]. This industry source tracks DFT, among other key characteristics of the semiconductor industry, and highlights the direction of the technologies within this classification. This section examines the impact of technical changes by performing the following:

- Reviewing the latest trends and projections for DFT technology
- Projecting changes to top-down forecasting buy-rates and the resulting effects to future ATE revenues.
- Projecting changes to the bottoms-up forecasting model and the effects on ATE demand.

The goal of this section is to take a more strategic view of revenue and product planning, as opposed to the tactical approach that most of this thesis has taken. This requires an understanding of the long-term technical issues that will drive the direction of ATE demand. Simple models for reviewing this impact have been developed that help to proved a strategic viewpoint as well as to further explore the effectiveness of the top-down and bottoms-up forecasting techniques.

## 5.1. Review and Outlook for Design for Test

Some of the main design alternatives currently considered in DFT are scan, built-in-self-test (BIST), and $I_{ddq}$. Scan testing, which is the most prolific of the three, can be further

broken down into full, partial, and boundary. This method for aiding in test requires additional logic which is placed into the design which allow the tester to access specific parts of the device. Partial and full scan are used to test internal nodes on a device. The main difference between the two is that partial scan requires more complex set of automatic test pattern generation (ATPG). Boundary scan uses latches/flip-flops around the boundary of the device to allow for separate testing of the chip's I/O and its internal circuitry. In addition to the requirement of additional semiconductor real estate, up to 15% additional logic, this method usually is not capable of testing the functionality of high-speed paths.

In BIST, the testing is put on the chip itself. In doing so, it is able to overcome the inability to test high-speed paths found in scan techniques. The chip controls both the input test patterns and output. An added benefit is that testing of devices can be done in the field, where the generation of the current factory testing would not be feasible.

$I_{ddq}$ is a technique that breaks away from traditional functional tests in an attempt to address questions of physical integrity, such as the quality of metal bridging. This results in the detection of process errors that even at-speed tests may overlook. It involves the measurement of leakage current after specific logic states are established through the use of targeted test vectors. There is still a great deal of debate over the extent to which Iddq can be applied.

The NTRS from both 1994 and 1997 identified DFT techniques as a major source for containing test costs for semiconductor manufacturers. Projections from the 1994 issue stated that by the year 2010, the cost of test systems would approach $50M if these strategies were not incorporated. At the time, less than 25% of a typical logic IC was being tested with this methodology, and far less for the memory and analog segments. The prediction when on further to state that by the year 2010, 90% of a device needs to be tested using DFT application, and that the cost of test per pin for testers will reduce from $5-10 K to $0.5-1.5K while the pin count doubles or even quadruples. The 1997 issue of the NTRS is less optimistic about the strength of DFT and shied away from predicting or proposing exact percentages needed. However, it projects that at current levels of approximately 35%, the cost of a test system would approach $20M by the year

2010. And that even with rapid increases in DFT the cost per pin will remain constant at $5-10K. It is clear that the direction that this class of technologies takes will have a dramatic effect on ATE demand.

## 5.2. Projections Using Top-Down Model

The growth of the semiconductor industry's total revenue is a result of two separate factors, increase in volumes and increase in functionality. Growth due to volume is a simple concept to understand. As semiconductors are applied to more and more products, volume requirements increase. Growth in revenue due to functionality is seen when a single IC has more or improved features that demand a higher price from end customers. The trend toward more complex IC's as well as increased use of the semiconductor technology has resulted in both factors growing over the past two decades. A similar statement can be said of the ATE market. Revenue growth comes from both increases in volume to support larger IC production, as well as increases in functional requirements.

### 5.2.1. Model Description

The claims of the NTRS, and other sources that worry about increasing test costs, are that the increase in functionality of semiconductors is causing a proportionately larger increase in the functional revenue growth of ATE. DFT is thought of as a means to correct for , or reversal of this condition. By understanding how changes over time effect the top down model, it is possible to use it as a tool for examining the impact that this technology might have on ATE revenue. The first step is to understand how revenues in both the ATE and semiconductor markets grow over time. The following two equations express this growth as a function of increases in the volume of devices, and functionality provided by these devices:

$$ATE_t = ATE_0 (g_{vol})^t (g_{ATEfun})^t \quad (4.1)$$

$$SC_t = SC_0 (g_{vol})^t (g_{SCfun})^t \quad (4.2)$$

Here $\mathbf{ATE_t}$ is the predicted level of ATE industry revenue at time t. It is a product of the current ATE revenue, $\mathbf{ATE_0}$, the growth of volume in semiconductor devices, $g_{vol}$, and the growth in ATE functionality requirements due to increases in complexity of devices. Similarly, $\mathbf{SC_t}$ is the predicted value for the semiconductor market's revenue at time t. This is also a product of current revenues, $\mathbf{SC_0}$, the growth of volume in semiconductor devices, $g_{vol}$, and the growth in semiconductor revenue due to changes in device functionality requirements. Plugging these into the equation for the top-down model as described in section 2.1, the following equation results, which is the basis for the model with $\mathbf{BR_0}$ equal to the current buy-rate value:

$$\mathbf{ATE_t} = \mathbf{BR_0}\left(\frac{gATEfun}{gscfun}\right)\mathbf{SC_t} \tag{4.3}$$

In order to simplify some of the terms for discussion, the following symbols are used:

$$g_{SC} = (g_{vol})(gSCfun) \tag{4.4}$$

$$g_{ATE} = (g_{vol})(gATEfun) \tag{4.5}$$

$$g_{BR} = \frac{gATEfun}{gSCfun} \tag{4.6}$$

The growth in semiconductor revenue, $g_{BR}$, is expressed as the product of the volume and functionality growth. The same relationship is used for ATE revenue, where $g_{ATE}$ is the variable used to represent the growth. The last representation is the ratio of growth in ATE revenues due to functional increases in semiconductor devices verses the growth in semiconductor revenues due to the same factor. This is termed the buy-rate growth, and is expresses as $g_{BR}$. The current expectation by the NTRS is that the buy-rate growth will be larger than one unless BIST/DFT adaptation increases.

### 5.2.2. Application to NTRS Projections

Values for the various parameters were determined from Dataquest and VLSI Research market data reports, and from projections from the 1994 and 1997 NTRS roadmaps. The four scenarios discussed here are derived from projections from the 1994 and 1997 NTRS roadmaps. The first captures the forecasted parameters from the 94' issue if DFT is not adapted from the initial level of 25% of IC's. The next is the forecasted industry characteristics given an improvement to 90% DFT for IC's. The third is derived from the 97' issue, and represents an adjusted estimate of the market given no further adaptation of DFT techniques. The final scenario is in which the cost per pin of test remains constant, while the total number of pins increases. Table 5.1 summarizes the values for the parameters used for the four scenarios.

| Parameter | NTRS 94' | | NTRS 97 | |
|---|---|---|---|---|
| | 25% DFT | 90% DFT | 30% DFT | Rapid Increase in DFT |
| t (years) | 15 | 15 | 12 | 12 |
| $g_{SC}$ | 1.170 | 1.170 | 1.160 | 1.160 |
| $g_{vol}$ | 1.070 | 1.070 | 1.070 | 1.070 |
| $g_{SCfun}$ | 1.093 | 1.093 | 1.093 | 1.093 |
| $BR_0$ | 0.018 | 0.018 | 0.018 | 0.018 |
| $ATE_0$ ($M) | $1.5 | $1.5 | $2 | $2 |
| $ATE_t$ ($M) | $50 | $1.5 | $20 | $8 |
| $g_{ATE}$ | 1.351 | 1.070 | 1.296 | 1.201 |
| $g_{ATEfun}$ | 1.263 | 1 | 1.212 | 1.122 |
| $g_{BR}$ | 1.155 | 0.915 | 1.109 | 1.026 |

**Table 5.1 Parameters: Predicted Technology Scenarios and the Top-Down Model**

From the results it is clear that the growth of ATE and the growth of the buy-rate could dramatically change as DFT is adopted. Both the 94' and 97' issues suggest that there would be enormous increases in revenues if this technology is not implemented. The earlier issue projects a reduced buy-rate if the industry proceeds along to 90% DFT in

2010. Interestingly, the value for this reduction is similar to that seen in the section on top-down forecasting when looking at changes to the buy-rate in the logic segment over time. This is the area that has had the most success with these techniques and this potentially provides some explanation. Perhaps even more interestingly, the 97' issue backs away from the strong projections of DFT implementation and impact that was seen in 94'.

These results can be used to estimate revenue levels in the future. Some key milestone years are shown in Table 5.2.

| Year | Market Segment | NTRS 94' | | NTRS 97' | |
|---|---|---|---|---|---|
| | | 25% DFT | 90% DFT | 30% DFT | Rapid Increase in DFT |
| 2000 | Logic SC | $115B | $115B | $122B | $122B |
| 2000 | Total SC | $245B | $245B | $230B | $230B |
| 2000 | Logic ATE | $6.2B | $1.6B | $3.2B | $2.4B |
| 2000 | Total ATE | $13.4B | $3.3B | $9.7B | $7.2B |
| 2010 | Logic SC | $554B | $554B | $585B | $585B |
| 2010 | Total SC | $1,183B | $1,183B | $1,108B | $1,108B |
| 2010 | Logic ATE | $127B | $3.1B | $45B | $15B |
| 2010 | Total ATE | $273B | $6.7B | $108B | $37B |

**Table 5.2 Top-Down Model Revenue Forecasts for Predicted Technology Scenarios**

## 5.3. Projections Using Bottoms-Up Model

The bottoms-up model relates ATE demand to semiconductor capacity as opposed to semiconductor revenue. However, similar relationships exist. Capacity also grows from both volume and functionality factors. As it is measured in wafer starts per month (WSM), an increase in volume requirements results in a larger number of starts. Also, as chip functionality becomes more complex, more semiconductor real estate is required. This is especially relevant with the concept of system-on-a-chip where multiple functions are combined into one device.

### 5.3.1. Model Description

Once again, the claims by industry sources are that increases in capacity due to functionality require proportionately larger increases in spending on ATE. Here, DFT can be thought of as the balancing technology that controls ATE costs as chip size and function grows. For this formulation, the bottoms-up model is adjusted to incorporate technology changes. The model formulation is very similar to that used for the top-down model. Again equations that express growth in terms of volume and function are used:

$$\mathbf{ATE}_t = \mathbf{ATE}_0 (g_{vol})^t (g_{ATEfun})^t \tag{4.7}$$

$$\mathbf{CAP}_t = \mathbf{CAP}_0 (g_{vol})^t (g_{CAPfun})^t \tag{4.8}$$

The first equation is identical to equation 4.1. However, for the bottoms up model, the focus is on capacity. Here $\mathbf{CAP}_t$ is the predicted value for the semiconductor market's added capacity at time t. This is a product of current added capacity, $\mathbf{CAP}_0$, the growth of volume in semiconductor devices, $g_{vol}$, and the growth in semiconductor added capacity due to changes in device functionality requirements. Plugging these into the bottoms-up model, the following equation is derived, where $\mathbf{K}_0$ is the current ratio of ATE revenue demand to new fab capacity:

$$\mathbf{ATE}_t = \mathbf{K}_0 \left( \frac{\mathbf{g}_{\mathbf{ATEfun}}}{\mathbf{g}_{\mathbf{CAPfun}}} \right) \mathbf{CAP}_t \tag{4.9}$$

Again, notation is used to simplify terms for discussion:

$$\mathbf{g}_{\mathbf{CAP}} = (g_{vol})(g_{CAPfun}) \tag{4.10}$$

$$\mathbf{g}_{\mathbf{ATE}} = (g_{vol})(g_{ATEfun}) \tag{4.11}$$

$$\mathbf{g}_{\mathbf{K}} = \frac{g_{ATEfun}}{g_{CAPfun}} \tag{4.12}$$

The growth in semiconductor capacity, $g_{RAP}$, is expressed as the product of the volume and functionality growth. The same relationship is used for ATE revenue, where $g_{ATE}$ is the variable used to represent the growth. The last representation is the ratio of growth in ATE revenues due to functional increases in semiconductor devices verses the growth in semiconductor added capacity due to the same factor. This is termed the capacity-rate growth, and is expresses as $g_K$.

### 5.3.2. Applications to NTRS Projections

The scenarios to be reviewed are again derived form the 94' and 97' issues of the NTRS. They include projections from 94' of 20% DFT acceptance in 2010 as well as 90%. Also, the 97' roadmaps for 35% and what is termed rapid increases. The growth rate that is used for capacity is the CAGR for 8" equivalent WSM experienced from 1990-1996. Table 5.3 lists the values for each parameter under the four different cases.

| | NTRS 94' | | NTRS 97' | |
|---|---|---|---|---|
| **Parameter** | **25% DFT** | **90% DFT** | **30% DFT** | **Rapid Increase in DFT** |
| t (years) | 15 | 15 | 12 | 12 |
| $g_{CAP}$ | 1.230 | 1.230 | 1.230 | 1.230 |
| $g_{vol}$ | 1.070 | 1.070 | 1.070 | 1.070 |
| $g_{CAPfun}$ | 1.150 | 1.150 | 1.150 | 1.150 |
| $K_0$ | 0.0073 | 0.0073 | 0.0073 | 0.0073 |
| $ATE_0$ | 2 | 2 | 2 | 2 |
| $ATE_t$ | 50 | 2 | 20 | 8 |
| $g_{ATEfun}$ | 1.263 | 1 | 1.212 | 1.122 |
| $g_{ATE}$ | 1.351 | 1.070 | 1.296 | 1.201 |
| $g_K$ | 1.174 | 0.870 | 1.126 | 1.044 |

**Table 5.3 Parameters: Predicted Technology Changes and the Bottoms-Up Model**

Not surprisingly, the results are similar to those found in the top-down approach. The 90% DFT acceptance projected from the 94' issue produces a decaying growth rate for

the ATE to capacity ratio of 0.870. Also, the adjustments made in the 97' issue project a smaller impact of DFT which result in a growth rate for the ratio of 1.044. Both issues show significant functional growth if the technology stalls.

Table 5.4 shows the projected ATE revenues for each scenario in 2000, and 2010. This helps to provide a better feel for the impact that technology might have as predicted by the above model. Capacity in 8" equivalent WSM grows at a rate over one million per year in 2000 from current levels of 780 thousand, and exceeds ten million per year by 2010. Current total levels are above five million.

| Year | Market | Capacity Increase per Year | NTRS 94' | | NTRS 97' | |
|---|---|---|---|---|---|---|
| | | | 25% DFT | 90% DFT | 30% DFT | Rapid Increase in DFT |
| 2000 | Total ATE | 1,319,202 | $25B | $4.2B | $15.4B | $11.4B |
| 2010 | Total ATE | 10,455,924 | $523B | $14B | $317B | $127B |

**Table 5.4 Bottoms-Up Model Forecasts with Predicted Technology Changes**

## 5.4. Results Summary

This chapter has focused on adapting forecasting models to help in measuring the impact technologies might have on the ATE market. In particular, two factors to growth have been discussed, volume, and functionality. This separation of means to growth can be a useful method to gain a different perspective on the role of technological changes in a market place.

Specifically, DFT could have a dramatic impact on the functionality growth that the ATE market has seemed to enjoy. Various semiconductor associations, such as SIA, see the application of the design techniques in this category as a means to reverse ATE's proportionally larger functional growth per increase in semiconductor functionality. Models presented here suggest that if predictions are true, revenues in this industry will vary by an order or two of magnitude depending on the acceptance of DFT.

# 6. Conclusion

The semiconductor industry and the industries that support it have, and will continue to have, enormous growth opportunities. With the continual interest and developments in areas such as networking, and mobile computing, the need for new devices will certainly increase. However, there is not much reason to believe that the cyclical nature of this market will go away any time soon. The swings in 1997 alone are testimony to the fact that fluctuations will continue.

Therefore, it is important to continue to work on improving forecasting. Modeling is an important technique for making the forecasting process more quantitative and closely connected to tangible characteristics of the market. Other less analytical approaches should also be undertaken. This includes, if possible, working as close as possible to customers. Such relationships can help to alleviate problems, such as over ordering which are frequently found in supply chains. This is certainly an approach that Teradyne and other ATE manufacturers have taken and should continue to do so in the future.

However, it is more critical to understand how to operate most effectively under such volatile market conditions. Trends in the industry have heightened the importance of this fact. The continual increase in worldwide capacity by foundries, which focus on rapid response to their customers, has made lead times of primary concern. Even those companies that do their own semiconductor manufacturing have improved their ability to stop and start capacity increases to time market demand. Suppliers to the semiconductor industry that can develop a competitive advantage in responsiveness will be the ones that survive.

## 6.1. Forecasting in Semiconductor Related Markets

The bottoms-up forecasting model presented here does appear to have promise. The negative bias that has existed in top-down approach was removed for the time period studied. However, this technique is far from proven. The model should continue to be used until the statistical significance of any improvement can be judged. Certainly, the

new model does not need to completely replace the older one, but instead it could serve as a supplement.

An area not reviewed in much detail is the possibility of leveraging the differences in the market segments. For instance, the memory market has had much more volatile revenue totals than other device types. However, the functional requirement of memory makes it much more commodity like. Thus process and product variations are fewer. This is a segment where a closer look at capacity increases makes the most sense.

## 6.2. Operating with Forecast Error

Forecasts by definition are always wrong. The key questions that must be understood are how wrong, and what operationally can be done to most effectively compete with the given error. In the case of ATE, lost sales or even customer dissatisfaction due to long delays in delivery dominate the discussion. Due to the extremely high switching costs between ATE vendors, and the follow-on sales that are attached to each tester, the loss of a sale costs significantly more than the marginal cost of increasing capacity. Under high forecasting error, it is important to plan for volumes greater than those predicted. As forecasting is improved, the amount over the predicted level can be reduced. Certainly, this will result in material write-offs due to obsolescence, as well as other pains in downturns. However, upswings will produce higher revenues and an increase in market share when there is a chance to do so.

A more proactive approach to addressing the issue of operating with forecast error is to recognize the importance of volume flexibility. Often when companies focus on design for manufacturing (DFM), their efforts are on ease of assembly or repeatability. In ATE, the concentration needs to be on effectively dealing with industry cycles. This might include trading off an easy assembly process for a difficult one that include shorter lead-time parts.

## 6.3. Impact of Technology

Clearly, in addition to more tactical approaches, it is important to also have a strategic perspective while performing revenue and product planning. Focusing on near term forecasting improvements could lead a company to miss the big picture. Design-for-test

is expected to significantly reduce the perceived increasingly larger cost growth of ATE per functional improvement in semiconductors. Other technologies that are under investigation could have similar effects. In an industry that is as fast paced as semiconductors and semiconductor equipment, the effects of technology could dwarf the errors in traditional forecasting.

# Appendix A: Regression Line Plots

There are two sets of regression line plots presented in this appendix:

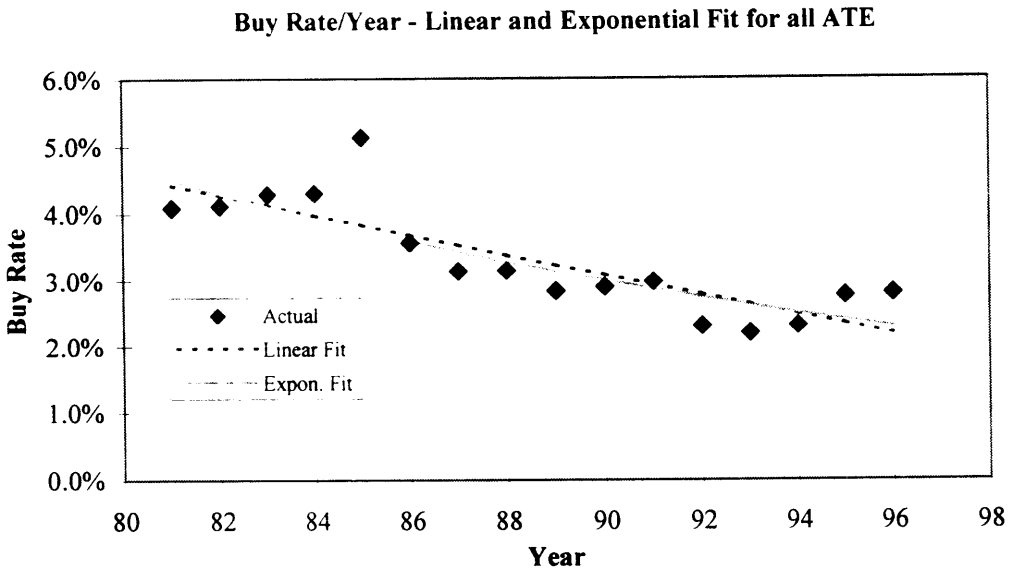
### Buy-Rate/Year Regression Line Fits

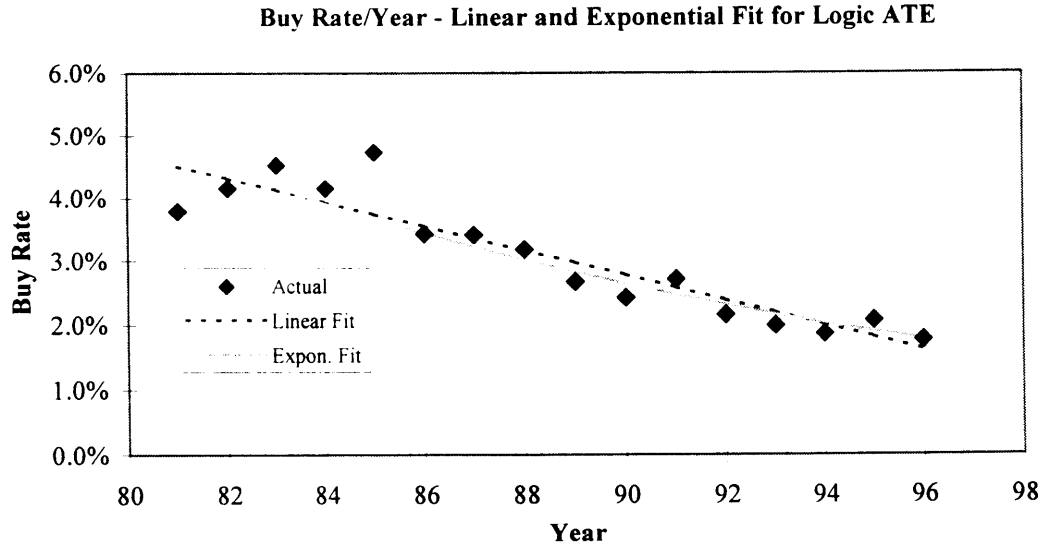
These graphs plot buy-rate verses year for the total ATE market as well as for the individual logic, memory, and mixed signal segments. The data and the regression lines are shown. They contain both exponential and linear fits.

### Fab Equipment/Fab Capacity Ratio Regression Line Fits

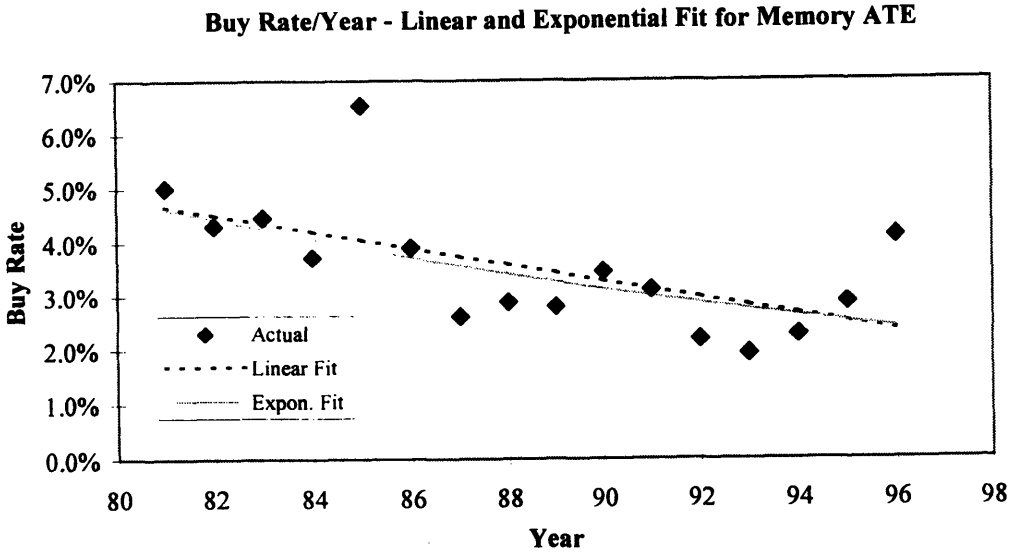
These graphs plot equipment expenditures per 8" equivalent WSM. Graphs are specific to the product that is produced with the wafer. There is also a plot that presents all of the different fab types. For each, the data and the regression lines are shown.

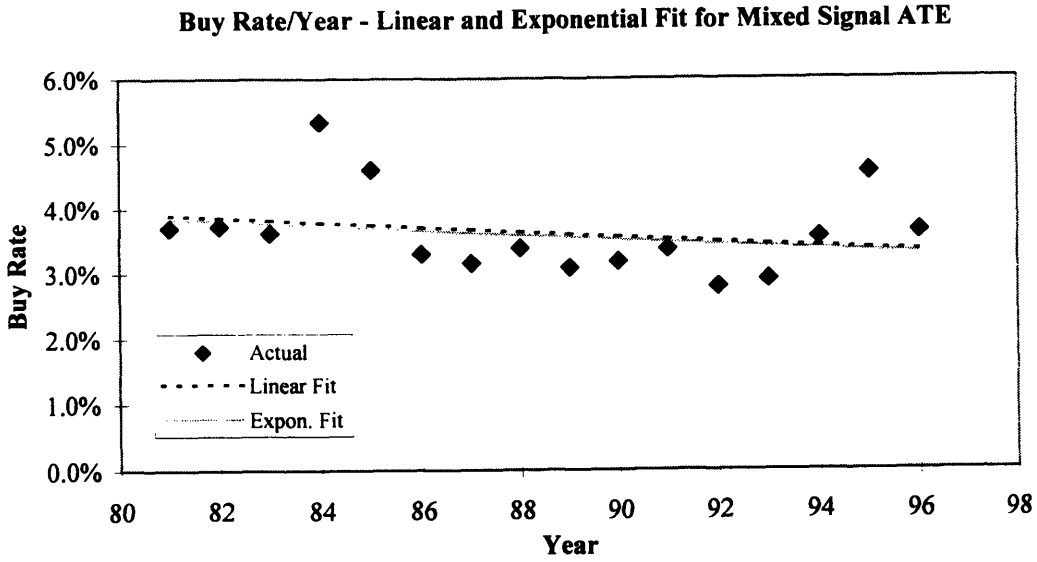
# Buy-Rate/Year Regression Line Fits



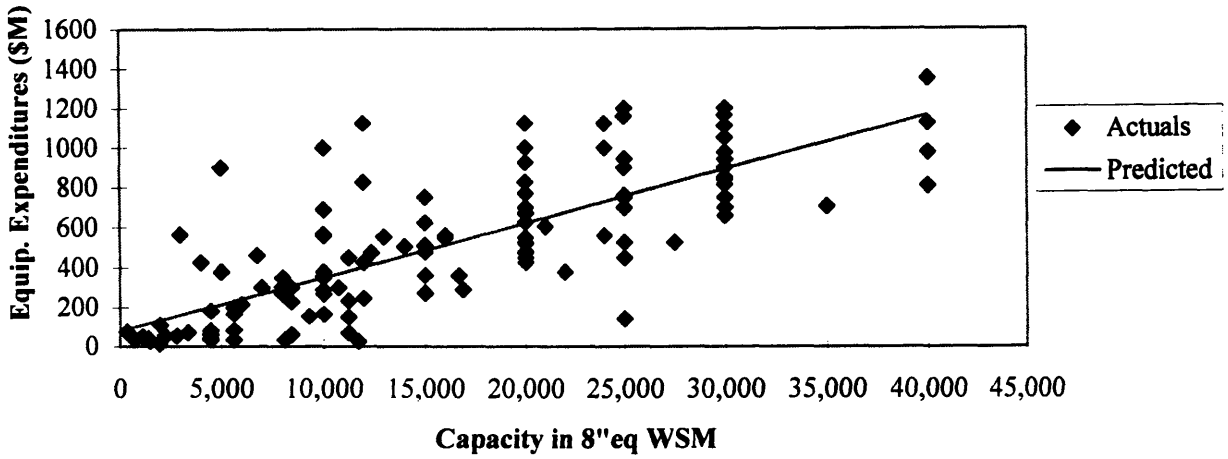
# Buy-Rate/Year Regression Line Fits



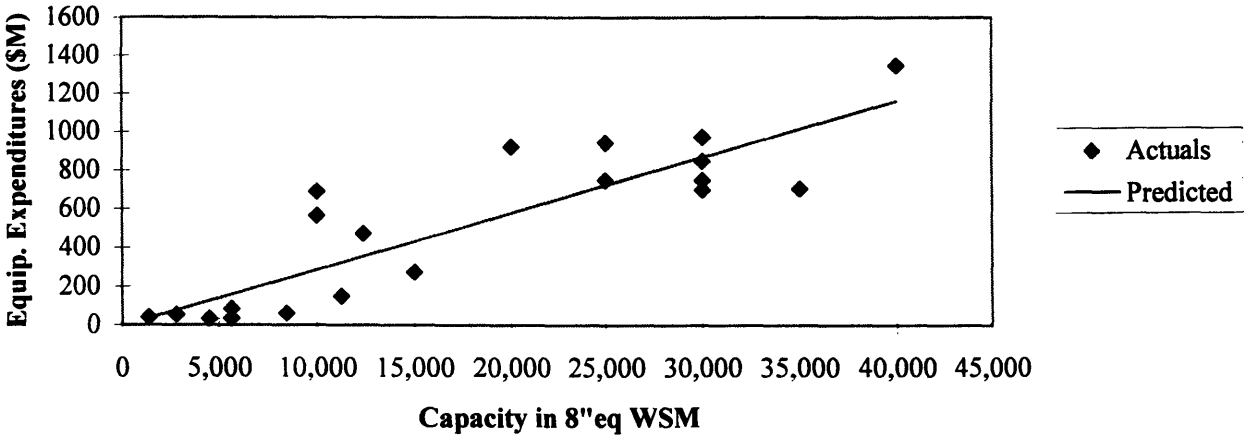



# Fab Equipment/Fab Capacity Ratio Regression Line Fits

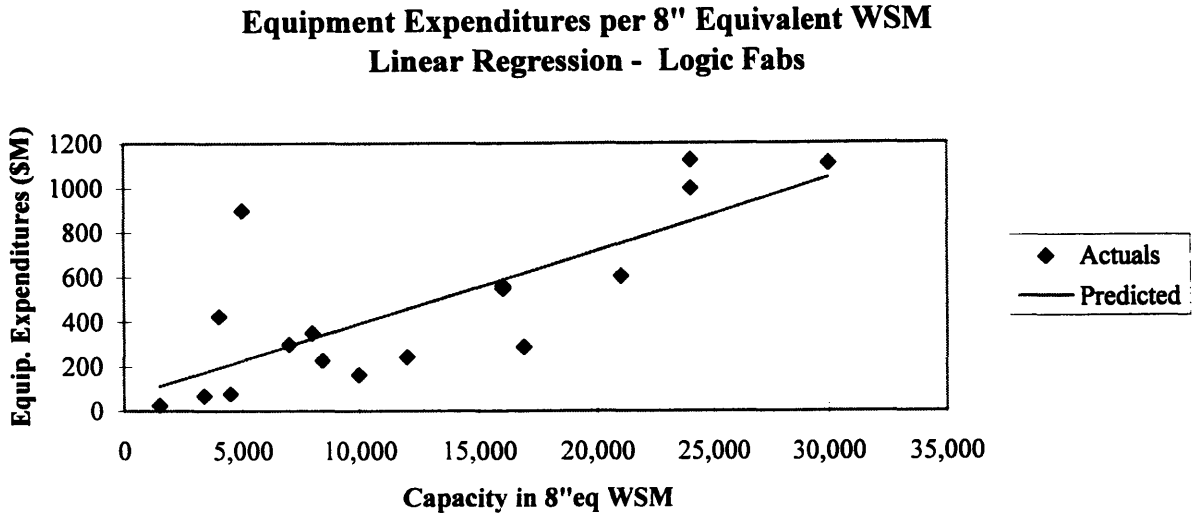
## Equipment Expenditures per 8" Equivalent WSM
## Linear Regression - All Fab Types

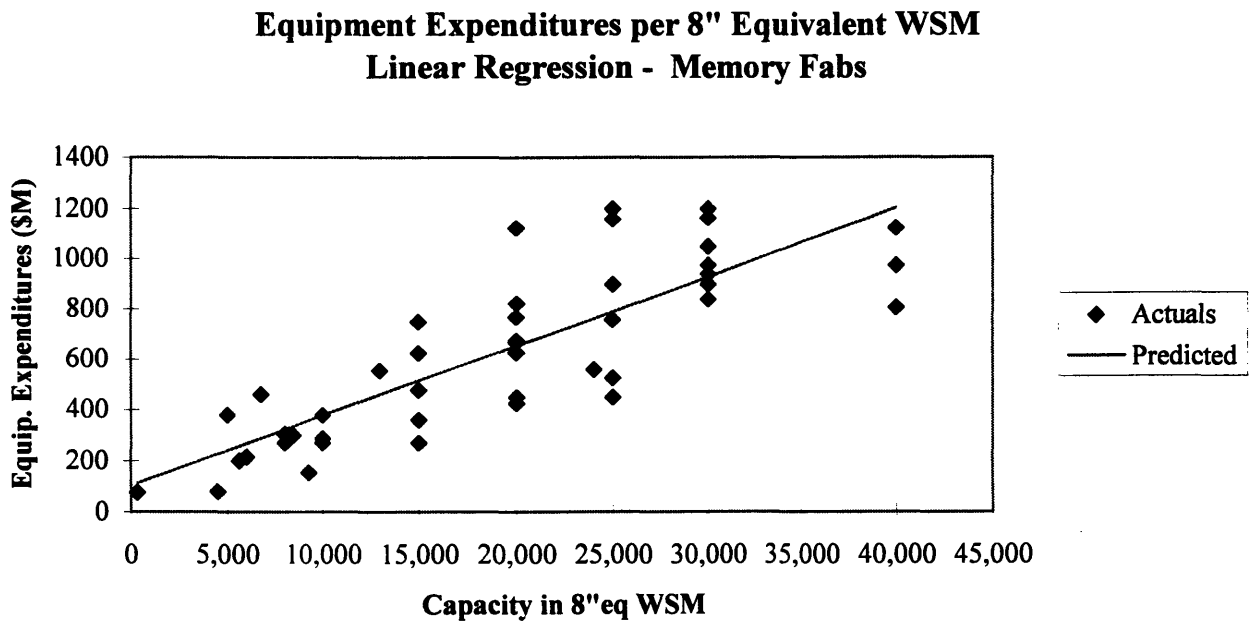



## Equipment Expenditures per 8" Equivalent WSM
## Linear Regression - Foundry Fabs

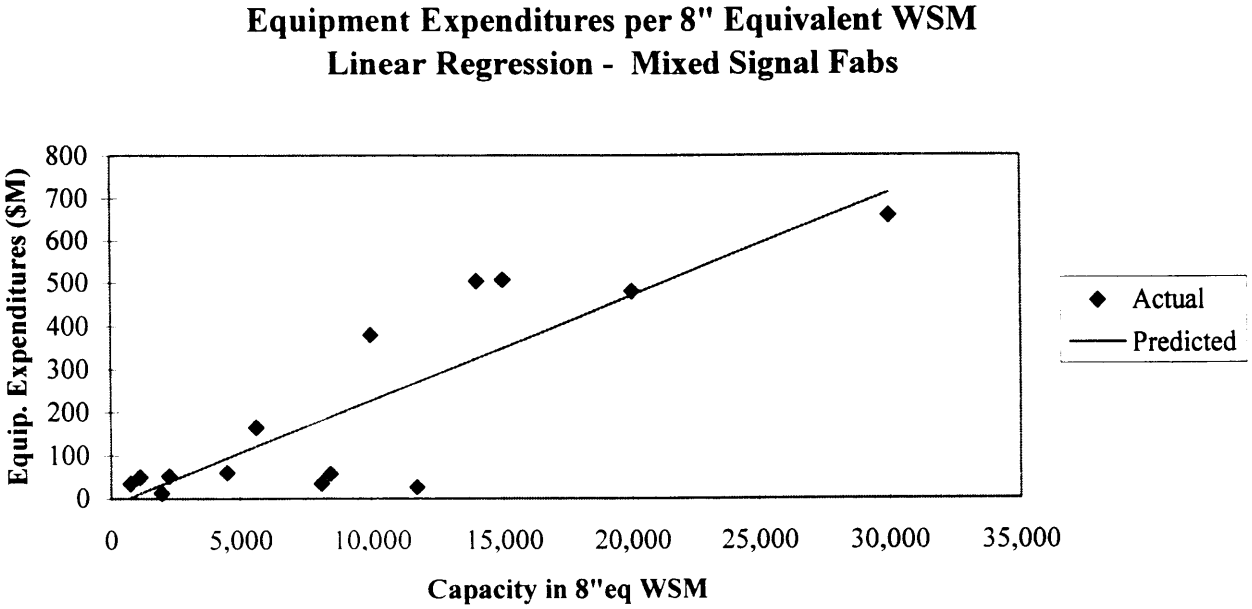


## Fab Equipment/Fab Capacity Ratio Regression Line Fits



## Fab Equipment/Fab Capacity Ratio Regression Line Fits



# Appendix B: User Interfaces for Models

There are two user interfaces shown in this appendix:

### Bottoms-Up Forecasting Model Interface

This user interface consists of two sections. The user inputs capacity projections as determined by fab databases for each product type into the correct year. The results table shows the forecasted ATE revenues for the years in question after the user selects the calculate button.

### Capacity Planning Model Interface

This user interface consists of the data input/output section, graphical representations of the output, and a detailed description of some key parameters. The user enters values for the demand and cost parameters. Then he or she selects the optimize button. The results appear in the results section and detailed output table. The graphs are also updated after this button is selected.

## Bottoms-Up Forecasting Model Interface

### Input - World Wide Capacity

| Product Type | Year | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 |
| Foundry | 34,000 | | 3,938 | 100,000 | 85,656 | 216,300 | 259,000 | 70,000 |
| Logic | 37,125 | 30,888 | 72,219 | 117,797 | 75,500 | 74,688 | 77,000 | 80,000 |
| Memory | 75,063 | 92,313 | 189,481 | 265,400 | 250,094 | 267,781 | 609,850 | 90,000 |
| Mixed Signal | 10,125 | 28,828 | 2,500 | 42,094 | 63,375 | 42,963 | 31,250 | 28,672 |
| Memory/Logic | 54,688 | 70,125 | 75,375 | 79,375 | 143,987 | 135,000 | 87,000 | 8,000 |
| Combination | | 26,563 | 20,000 | 19,063 | 4,000 | 44,000 | 28,000 | 12,000 |
| Discrete | 49,125 | 4,500 | 4,938 | 11,250 | 30,469 | 27,625 | 525 | |
| Not Specified | 2,500 | 11,250 | 8,219 | 500 | 338 | 12,000 | 35,000 | 0 |
| Total | 262,625 | 264,466 | 376,669 | 635,478 | 653,419 | 820,356 | 1,127,625 | 288,672 |

Calculate

### Output - World Wide ATE Demand

| ATE Market | Year | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1992 | 1993 | 1994 | 1995 | 1996 | 1997 | 1998 | 1999 | 2000 |
| Total ATE | $1,015 | $1,846 | $2,510 | $4,030 | $4,744 | $5,548 | $7,623 | $4,589 | $824 |
| Foundry ATE | $174 | $104 | $20 | $523 | $745 | $1,368 | $1,987 | $1,152 | $215 |
| Logic ATE | $213 | $305 | $521 | $925 | $839 | $689 | $699 | $724 | $275 |
| Memory ATE | $361 | $661 | $1,179 | $1,825 | $1,971 | $2,012 | $3,710 | $2,195 | $260 |
| Mixed Signal ATE | $43 | $148 | $84 | $185 | $377 | $344 | $243 | $202 | $73 |
| Mem/Log ATE | $156 | $294 | $335 | $356 | $547 | $632 | $480 | $172 | $14 |
| Combination ATE | $0 | $126 | $171 | $148 | $73 | $221 | $259 | $137 | $34 |
| Discrete | $0 | $0 | $0 | $0 | $0 | $0 | $0 | $0 | $0 |
| Not Specified ATE | $12 | $61 | $71 | $26 | $3 | $58 | $201 | $100 | $0 |

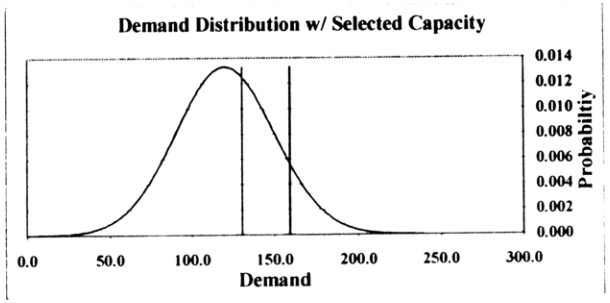
# Capacity Planning Model Interface

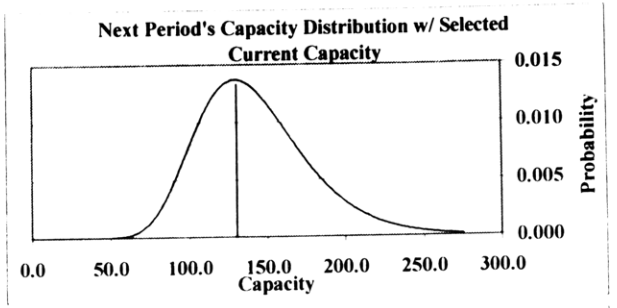
| Demand Parameters | |
|---|---|
| Forecasted Demand | 120 |
| Forecast Std. Dev. | 30 |
| Mean Increase Per Period | 15.0% |
| Period Increase Std. Dev. | 25.0% |

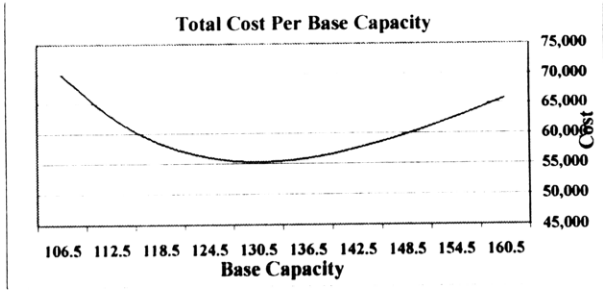
| Cost Parameters | |
|---|---|
| Fixed Capacity - VC | $350 |
| Variable Capacity Base VC | $350 |
| Growth Rate of VC | 0.02 |
| Maximum Flexability | 22.0% |
| VC for Lost Sale | $4,000 |
| VC to Reduce Capacity | $350 |

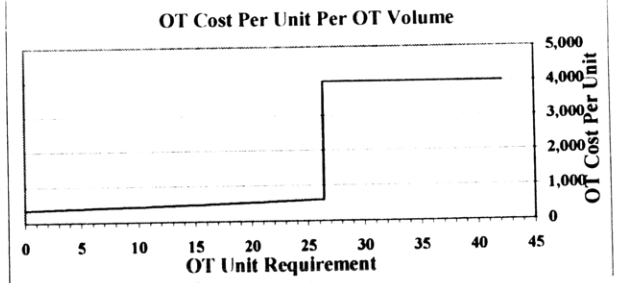
| Results | |
|---|---|
| Fixed Capacity | 130.5 |
| Variable Capacity Need | 3.4 |
| Variable Capacity VC | $374 |
| Expected Lost Sales | 1.3 |

Optimize




| | Center | Range | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Expected Tot Cost** | 55,258 | 69,888 | 62,894 | 58,354 | 56,002 | 55,258 | 55,845 | 57,463 | 59,765 | 62,585 | 65,778 |
| **Fixed Capacity** | 130.5 | 106.5 | 112.5 | 118.5 | 124.5 | 130.5 | 136.5 | 142.5 | 148.5 | 154.5 | 160.5 |
| **Total Capacity** | 135.2 | 121.8 | 121.6 | 125.8 | 130.5 | 135.2 | 140.1 | 145.3 | 150.6 | 156.0 | 161.5 |
| **Variable Capacity** | 3.4 | 3.7 | 3.8 | 3.8 | 3.8 | 3.4 | 2.8 | 2.4 | 1.8 | 1.4 | 1.0 |
| **Lost Sales** | 1.3 | 7.6 | 5.3 | 3.5 | 2.2 | 1.3 | 0.8 | 0.4 | 0.2 | 0.1 | 0.1 |
| **Var + LS Capacity** | 4.7 | 15.3 | 9.1 | 7.3 | 6.0 | 4.7 | 3.6 | 2.8 | 2.1 | 1.5 | 1.0 |
| **Expected Reduction** | 8.448 | 1.9 | 2.9 | 4.4 | 6.2 | 8.4 | 11.1 | 14.2 | 17.7 | 21.6 | 25.8 |

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