Underfill Material Selection For Flip Chip Technology

by

Diana C. Chiang

B.S. Materials Science and Engineering
Massachusetts Institute of Technology, 1997

Submitted to the Department of Materials Science and Engineering
in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Materials Science and Engineering

at the

Massachusetts Institute of Technology

June 1998

© 1998 Diana C. Chiang
All rights reserved

The author hereby grants to MIT permission to reproduce and to distribute publicly paper and electronic copies of this thesis document in whole or in part.

Signature of Author: ______________________________
Department of Materials Science and Engineering
May 8, 1998

Certified by: ______________________________
David K. Roylance
Associate Professor of Materials Engineering
Thesis Supervisor

Accepted by: ______________________________
Linn W. Hobbs
John F. Elliott Professor of Materials
Chairman, Graduate Thesis Committee

Science

Underfill Material Selection For Flip Chip Technology

by

Diana C. Chiang

Submitted to the Department of Materials Science and Engineering
on May 8, 1998 in Partial Fulfillment of the
Requirements for the Degree of Master of Science in
Materials Science and Engineering

ABSTRACT

Six underfill materials were examined for the selection of an appropriate underfill material for Digital Equipment Corporation's flip chip development project. Several tests were performed to determine the material properties, process properties, and the reliability of each underfill material. A material with a fast flow rate, uniform and void free flow pattern, fast curing schedule, good thermal and mechanical properties, and good reliability results is needed to satisfy the requirements for this project. Materials F and E exhibited all the above requirements and were concluded as the two best underfill materials for the flip chip process. Important material properties which contributed to the desired results of these materials include a filler particle content of about 65%, a weight loss percentage during cure of less than 1%, and a T_g of 140°C.

Thesis Supervisor: David K. Roylance

Title: Associate Professor of Materials Engineering

Table of Contents

1.0. Introduction 7

2.0. Background/Theory 7

3.0. Experimental Procedures 10
- 3.1. Flow Rate and Flow Pattern Evaluation 10
- 3.2. Particle Settlement Evaluation 11
- 3.3. Thermal Stress Analysis 11
- 3.4. Reliability Testing 11
  - 3.4.1. Pressure Cooker Testing 12
  - 3.4.2. Thermal Cycling 12
  - 3.4.3. Thermal Shock Testing 13
  - 3.4.4. JEDEC Level 3 Testing 13

4.0. Experimental Results/Discussion 13
- 4.1. Flow Rate and Flow Pattern Evaluation 13
- 4.2. Particle Settlement Evaluation 16
- 4.3. Thermal Stress Analysis 17
- 4.4. Reliability Testing 19
  - 4.4.1. Pressure Cooker Testing 19
  - 4.4.2. Thermal Cycling 23
  - 4.4.3. Thermal Shock Testing 24
  - 4.4.4. JEDEC Level 3 Testing 24

5.0. Conclusion 25

6.0. Appendix 26
- 6.1. Photos of Cross-Sectioned Samples Made with Materials B, C, D, and F for Particle Settlement Evaluations 26
- 6.2. Raw Warpage Data from Mechanical Profilometer for Materials A-F ... 27
- 6.3. C-Scan Images of Underfilled Samples Before and After Pressure Cooker Test 31

7.0. Bibliography 34

List of Figures

Figure 2.1. Underfill dispensing and flow between two parallel plates by capillary action 8

Figure 3.1. Assembly diagram of a solder bumped die on a substrate with underfill .. 10

Figure 4.1.1. Relative underfill material flow times for samples made with bumped silicon chips on glass substrates, using single edge dispense and double edge dispense methods 15

Figure 4.1.2. Relative underfill material flow times for samples made with bumped silicon chips on glass and ceramic substrates, using single edge dispense method 15

Figure 4.1.3. Material filler particle content verses material flow time 16

Figure 4.2.1. Cross section of sample made with underfill material A 18

Figure 4.4.1. C-Scan images of 2 samples made with underfill material D, before and after the pressure cooker test 20

Figure 4.4.2. C-Scan vs. stud-pull correlation of samples after 96 hours of pressure cooker testing. Materials A - C 21

Figure 4.4.3. C-Scan vs. stud-pull correlation of samples after 96 hours of pressure cooker testing. Materials D - F 22

List of Tables

Table 3.1. Materials Properties of Materials A-F 10

Table 3.2. Curing conditions of underfill materials as recommended by their vendors 11

Table 3.3. Different underfilled samples that went through JEDEC Level 3 test 13

Table 4.1. Flow times (in seconds) of underfill materials A-F with different sample sets and dispense methods 14

Table 4.3.1. Highest warpage values of silicon die on ceramic substrate due to thermal stresses 17

Table 4.4.1. Stud pull values and the mode of failure of underfilled samples after the pressure cooker test 19

Table 4.4.2. Stud pull values and the mode of failure of underfilled samples after thermal cycling 24

Acknowledgments

The following thesis work was done at Digital Equipment Corporation, in the Advanced Development group within Semiconductor Packaging and Testing. In order to protect proprietary information, and the names of vendor companies that Digital is involved with, all of the underfill material names and some of their material properties have been excluded from this report.

I would like to thank my supervisor at Digital, Dr. Lidia Lee, who gave me the opportunity to be involved with the underfill materials selection for the flip chip project. She was a wonderful mentor and helped me tremendously in learning the flip chip technology. Her expertise in electronic packaging and in polymer materials was a driving force behind this flip chip underfill project. I would also like to thank Dr. Trirat Hongsmatip who ran many analytical experiments to characterize the material properties of the underfill materials, and the people in MSAL and the reliability lab who contributed to carrying out the experiments.

I'd like to express my appreciation to all the other members of the Advanced Development group, who also helped me become familiarized with the flip chip technology. Also, my sincere appreciation goes to all the people in the SPT lab.

Lastly, I want to thank Professor David Roylance, my thesis advisor, who helped me with the writing of this thesis. I have learned a great deal from the work I have done for this thesis. I greatly appreciate the coop/study opportunity that Department of Materials Science and Engineering has provided for me.

1.0. Introduction

The electronic industry is one that is always in pursuit of faster, smaller, better products. As product size decreases and its signal rates increase, the need for lower profile, lighter weight, and higher density electronic packaging becomes crucial. This need has driven the rapid expansion of the flip chip interconnect technology. Flip chip technology is defined as the mounting of the chip to a substrate by any kind of material and method, as long as the chip surface (active area) is facing the substrate. This technology is able to meet the requirements of higher package density and interconnection better than the otherwise limited face-up wire bonding technology. The flip chip technology has been used for computer, automotive, consumer electronics, and military applications for many years. In 1965, IBM first began using its flip chip process, controlled collapse chip connection (C4).[1] Reliability data collected by IBM showed no field failures.

Since IBM's development of its flip chip technology, many other companies have followed this path. In 1990, Hitachi began their version of the flip chip process technology. Motorola licensed the C4 technology from IBM and began manufacturing C4 products in 1994. Intel has also licensed C4 from IBM for their own flip chip development.

In recent years, the epoxy underfill material for the flip chip was invented. This polymeric material allowed flip chip solder joining for large chips with high I/O interconnects by reducing the stresses caused by the mismatch of the coefficients of thermal expansion (CTEs) between the chip and the substrate. The result of this underfill material was the dramatic increase in the thermal fatigue lifetimes of the solder joints. The material properties and process characteristics of the underfill encapsulant become very important as the need for more reliable flip chip devices increases.

2.0. Background/Theory

There are many different methods of joining a chip on a substrate. Three popular methods are face-up wire bonding, face-up tape automated bonding, and face down flip chip. Among these three methods, flip chip packaging provides the shortest possible leads, lowest inductance, highest frequency, best noise control, highest density, greatest number of I/Os, smallest device footprints, and lowest profile.[2] Flip chip processing can utilize the full active area of the face of the chip with an area array of pads. The chip is turned upside-down, and an array of solder bumps on the chip are joined to a matching array of solder wettable pads on the substrate by reflowing the solder. A typical flip chip system consists of a silicon chip bumped with a Pb/Sn solder with a ceramic or organic substrate. The CTE of a silicon chip is about 2.5 ppm/ °C, while the CTE of the substrate is significantly higher, about 7 ppm/ °C for ceramic and 15 ppm/ °C for organic laminates. This mismatch in the CTEs contributes a high level of thermal stress in the solder joints. However, if an underfill encapsulation material is used between the chip and the substrate, the thermal fatigue life can be improved. This underfill material, typically an epoxy based material, redistributes the stress on the joints thereby reducing it. Epoxy resin is a polymer which contains two or more epoxy groups in a molecule. The epoxy

group also known as oxirane contain an oxygen atom bonded with two carbon atoms, which in turn are bound by separate bonds. Reliability test data showed that underfilling a flip chip could affect the mean number of life cycles by 5-20 times when a ceramic substrate is used.[3] In order to reduce the thermal stresses in the flip chip device, the CTE of the underfill has to closely match that of the solder bumps. This way, both the underfill and the solder would expand at the same rate when the assembly is subjected to changes in the thermal conditions. The CTE of the solder bumps, typically Pb/Sn, is around 23 ppm/ °C. The typical CTE of an epoxy underfill material is around 70 ppm/ °C, which is significantly different from the solder. But by adding about 65-75 wt. % of silica fillers, the CTE of the underfill can be reduced to about 25 ppm/ °C.[4]

Other than the CTE of the underfill, other properties such as wettability, adhesion, glass transition temperature (T_g), percent weight loss during cure, and moisture resistance are also important. When the size of the die exceeds 500 mils on each side, delamination due to stress and weak adhesion can occur in the flip chip devices. By reducing low molecular weight epoxies, thereby reducing the crosslink density of the polymer, internal stresses of the underfill can be reduced. High crosslink density epoxies tend to give high shrinkage upon cure, high internal stresses, and low adhesion. The moisture resistance can also be improved since moisture absorption is another problem with low molecular weight epoxy underfills. A low percent of underfill weight loss during cure is desired because a reduction in the mass of the underfill could affect its other properties. Also, the less weight loss that occurs, the less underfill contaminant is getting re-deposited onto the back of the chip. If there is contaminant on the backside of the chip, it could cause problems in latter processing steps.

The underfill is applied after the chip and substrate assembly has been reflowed. It is dispensed near the gap between the chip and the substrate. The flow of the underfill material can be modeled as a quasi-steady, laminar flow between parallel plates driven by surface tension (capillary action). Figure 2.1 shows the dispensing of the underfill and its flow between parallel plates.[5]

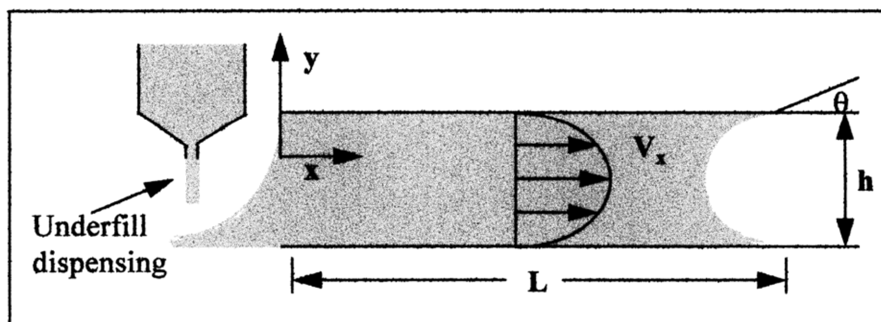


Figure 2.1. Underfill dispensing and flow between two parallel plates by capillary action.[5]

The flow rate of the underfill decreases as the flow front progresses. This is due to the fact that the capillary force driving the flow remains constant, while the amount of material being pulled along increases. The underfill material dissipates energy through viscous shearing and slows down the flow. The flow distance can be described by

$$L = \sqrt{\frac{h\, t\, \gamma \cos\theta}{3\,\mu}},$$

where h is the separation distance, t is flow time, γ is surface tension, θ is wetting angle, and μ is the absolute viscosity. The flow time, in turn, is given by

$$t = \frac{3\,\mu\, L^2}{h\,\gamma \cos\theta}.$$

The underfill flow time is inversely proportional to the surface tension, separation distance and cosine of the wetting angle, and directly proportional to the viscosity and the square of the flow distance.[5]

While the underfill material properties are very important, its processing properties are just as important. The flow time and the cure time of the underfill are big factors in the manufacturing of flip chip devices. A fast flow speed and cure dwell time is needed in order to produce as many devices as possible. The settlement of the filler particles in the underfill is another issue. If the filler particles were to settle to the bottom, then there would be an epoxy resin rich layer at the top. The material properties of the underfill material would therefore not be uniform and cause a poor distribution of stress under the chip. Other processing concerns include voiding, or air entrapment of the underfill during flow. Voids and air bubbles trapped in between the chip and the substrate could cause reliability issues.

Perhaps the most important role of the underfill material is to improve the reliability of flip chip devices. While the underfill material is known to increase the solder joint fatigue lifetime, there are other failure mechanisms to be concerned with for a flip chip assembly. Delamination of the underfill to its respective bonding surfaces is a major risk. An underfill needs to adhere well to its bonding surfaces in order to effectively redistribute the stress within the assembly. Poor interfacial adhesion could lead to the propagation of a crack during thermal cycling conditions and cause opens of interconnect bumps. There is also significant interfacial stress resulting from the CTE mismatch of the underfill and the chip and substrate. This stress could lead to delamination after many fatigue cyclic loadings. Delamination could also be caused by contamination or reactive chemical agents on the bonding surfaces, and moisture absorption of the underfill material.[6] Another issue is die cracking at the backside of the die and its propagation through the die active areas. This can be caused by non-optimized underfill material property and the presence of mechanical defects in the die. It is extremely important to perform reliability tests such as thermal shock, thermal cycling, and pressure cooker test to determine the effectiveness of any underfill material.

Digital Equipment Corporation is currently developing its own flip chip process technology. One major component of this development is evaluating different underfill materials, and selecting the top materials for further process development. Several underfill materials were received from different vendors for the evaluation process.

3.0. Experimental Procedures

Six different underfill materials, materials A-F, from five vendor companies were evaluated for the flip chip project. Most of these underfill materials are epoxy based. For curing of epoxy resins, compounds with active hydrogen atoms, such as aliphatic amines, aromatic amines, and acid anhydrides are typically used. Material analysis was done for each material and the material properties are summarized in Table 3.1.[7] All six materials were used for each of the following experimental evaluations.

Underfill Material	E' 25°C (GPa)	E' 70°C (GPa)	E' 125°C (GPa)	Tg (°C)	CTE (ppm/ °C)	% Wt. Loss during cure	% Particle Filler Content
A	7.53	7.04	5.98	173	22.3	6.596	65
B	7.86	6.93	1.62	125	22.8	5.327	68
C	11.58	10.87	9.69	167	19.7	5.318	74
D	9.36	8.83	7.96	190	22.1	3.691	70
E	12.71	10.81	3.22	140	19.3	0.943	63.5
F	7.2	6.48	4.43	139	26.1	0.059	62

Table 3.1.[7] Materials Properties of Materials A-F.

3.1. Flow Rate and Flow Pattern Evaluation

To determine the flow time of each underfill material, each material was manually dispensed between a solder bumped die and a substrate on a hot plate. The substrate was heated to 80°C to reduce the viscosity of the underfill as it is dispensed and to speed up the process. The underfill material was dispensed along the edge of the die and flowed between the die and the substrate by capillary action. This assembly is shown in Figure 3.1. For each material, three different sets of samples were made: bumped silicon dies on glass slide substrates, bumped glass dies on ceramic substrates, and bumped silicon dies on ceramic substrates. Glass dies and slides were used for the purpose of observing the flow pattern. The underfill flow distance varied with the dimensions of the dies and the substrates used. For the samples with a bumped silicon die and a glass slide, the flow distance was the length of the glass slide, about 688 mils. For the samples with a bumped silicon die on a ceramic substrate, the flow distance was the length of the silicon die, about 787 mils. For the samples with a bumped glass die on a ceramic substrate, the flow distance was the length of the bumped glass die, about 687 mils. The bump heights of the dies were about 3 mils.

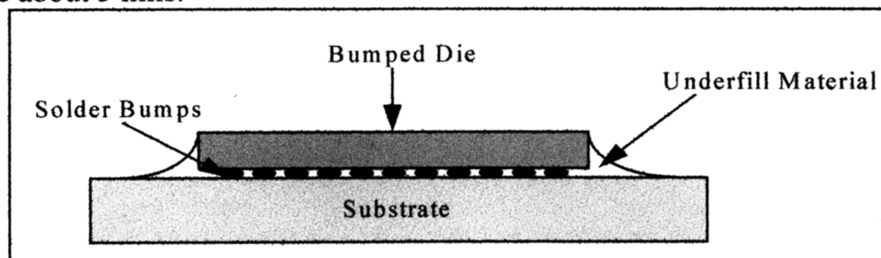


Figure 3.1. Assembly diagram of a solder bumped die on a substrate with underfill.

For the samples with a bumped silicon die and a glass slide, two different dispensing methods were tested: single edge and double edge dispensing. Underfill was dispensed on only one side of the die in single edge dispensing, and for double edge dispensing, underfill was dispensed on two adjacent edges starting at the same corner. For the other samples, only the single edge dispensing method was used. The flow times of the underfill materials were measured and recorded. Uniformity of the flow front was observed. Voids that occurred during flow were also noted.

All samples were cured in an oven after the underfill had flowed through completely. Samples were cured according to the temperatures and times recommended by the materials' vendors. See Table 3.2 for the curing conditions of the samples.

Underfill Materials	Curing Temperature (°C)	Curing Time (minutes)
A	150	30
B	150	30
C	150	120
D	165	30
E	165	90
F	150	15

Table 3.2. Curing conditions of underfill materials as recommended by their vendors.

3.2. Particle Settlement Evaluation

The cured underfill samples made with bumped silicon dies and glass substrates were cross-sectioned to determine the amount of particle settlement in the underfill material. Samples were cut using a Buehler 2000 precision diamond saw. The cut samples were then mounted and polished. The mounted samples were observed under an optical microscope. Pictures of each underfill material were taken.

3.3. Thermal Stress Analysis

The cured samples made with the silicon die on ceramic substrates were measured for warpage caused by thermal stresses from curing using a mechanical contact profilometer and the PPL Mirage, a video imaging measurement machine. The profilometer took die height measurements once across the center of the silicon die, once across the left edge, and once across the right edge of the die for each material sample. The PPL took die height measurements across the whole area of the silicon die for each sample. The varying height of the die on the ceramic substrate showed the amount of warpage, or strain caused by thermal stresses.

3.4. Reliability Tests

The effects of thermal stress and moisture on the interfaces of the underfill to the silicon die and to the substrates were determined by the pressure cooker test, thermal

cycling, thermal shock, and the JEDEC Level 3 test. These reliability tests were performed for the purpose of selecting the top underfill materials for the project and not for predicting the functional lifetime of the materials. The cured samples made with bumped silicon and bumped glass dies on ceramic substrates were thermal shock tested. These sample were held together by the underfill materials only. To determine the effect of flux residue from the solder bump joining of the die to the substrate, reflowed parts with silicon die assembled on ceramic substrates were used for the thermal shock test, thermal cycling, pressure cooker test, and JEDEC Level 3 test. Three different cleaning conditions after reflow were tested: no clean, semi-aqueous clean, and organic solvent clean. The organic solvent cleaning has better flux cleaning capabilities than the semi-aqueous cleaning. However, the semi-aqueous clean is more desirable for production reasons. For each of the cleaning conditions, 3 samples were made with each of the 6 underfill materials for the JEDEC Level 3 test. For the other tests, 3 samples were made for each of the underfill materials with semi-aqueous cleaned parts. These samples were made with an automatic underfill dispense system, which dispensed the underfill using double-edge dispensing on a heated substrate temperature of 90°C. The samples were cured according to the recommended curing condition in Table 3.2.

3.4.1. Pressure Cooker Test

18 parts went through the pressure cooker test. All parts were solder bump joined, and were semi-aqueous cleaned. Three parts of each of the 6 materials were made and tested. All parts were placed in a pressure cooker with conditions of 121°C, 2 atm, and 100% relative humidity for 96 hours. Three samples of each underfill material were C-Scanned at their initial state, and after 96 hours. The effects of moisture absorption from the pressure cooker were determined by the C-Scan. The C-Scanned samples were then pulled apart in a stud pull strength test. The force needed to pull apart the die from its substrate was recorded for each material. The method of failure was also recorded.

3.4.2. Thermal Cycling

18 parts went through thermal cycling testing. All parts were solder bump joined, and were semi-aqueous cleaned. Three parts of each of the 6 materials were made and tested. The samples were placed in a thermal cycling machine where they were cycled from one chamber at -55°C to another chamber at 125°C. The dwell time in each temperature condition was 10 minutes. All samples were tested to failure. Two samples of each underfill material were C-Scanned at their initial state, after 1500 cycles, and 3000 cycles. The number of voids present in the underfill before the thermal cycling were determined by C-Scan. The effects of the thermal cycling test, such as delamination, were also determined by the C-Scan. The C-Scanned samples were then pulled apart in a stud pull strength test. The force needed to pull apart the die from its substrate was recorded for each material. The method of failure was also recorded.

3.4.3. Thermal Shock Test

A total of 18 samples went through the thermal shock test. All parts were solder bump joined and semi-aqueous cleaned. Three parts of each of the 6 materials were made and tested. The samples were placed in a thermal shock chamber for liquid to liquid thermal shock at -55°C to 125°C. The samples were cycled from liquid to liquid with a dwell time of 5 minutes in each liquid. Two samples of each underfill material were examined with a C-mode Scanning acoustic microscope (C-Scan) at their initial state, and after 1500 cycles. The number of voids present in the underfill before the thermal shock cycles were determined by the C-Scan. The effects of the thermal shock test, such as delamination, were also determined by the C-Scan.

3.4.4. JEDEC Level 3 Tests

A total of 54 parts went through JEDEC Level 3 tests, followed by thermal cycling. All parts were solder bump joined. Three different cleaning conditions of reflowed parts were tested: no cleaning after reflow, semi-aqueous cleaning, and solvent cleaning. There were 18 parts of each cleaning condition. Table 3.4 shows the different samples that were tested.

Underfill Material	No Cleaning after Reflow	Semi-Aqueous Clean after Reflow	Solvent Clean after Reflow
A	3 samples	3 samples	3 samples
B	3	3	3
C	3	3	3
D	3	3	3
E	3	3	3
F	3	3	3

Table 3.3. Different underfilled samples that went through JEDEC Level 3 tests.

After preconditioning all the parts at 30°C with 60% relative humidity for 192 hours, the parts went through IR reflow, and then thermal cycling. IR reflow consisted of heating the parts up to reflow temperature of 230°C using IR. The thermal cycling involved cycling from -55°C to 125°C with a dwell time of 10 minutes, tested to failure. Two parts of each category and underfill material were C-Scanned at their initial state, after IR reflow, after 1500 cycles and 3000 cycles of thermal cycling.

4.0. Experimental Results/Discussion

4.1. Flow Rate and Flow Pattern Evaluation

Table 4.1.1 shows the flow times of all the underfill materials with different sample sets and dispense methods. Column 1 is the list of all the underfill materials. Column 2 (sample set 1) shows the flow times for samples made with bumped silicon dies on glass

substrates, with single edge dispensing. Column 3 (sample set 2) shows the flow times for samples made with bumped silicon dies on glass substrates, with double edge dispensing. Column 4 (sample set 3) shows the flow times for samples made with bumped glass dies on ceramic substrates, using single edge dispensing. Column 5 (sample set 4) shows the flow times for samples made with bumped silicon dies on ceramic substrates, using single edge dispensing. The differences in the flow distance of the sample sets have been taken into account, and the flow times have been normalized in order to accurately compare the flow times of different materials and sample sets.

	Sample Set 1	**Sample Set 2**	**Sample Set 3**	**Sample Set 4**
Underfill Material	**Bumped Si/glass (single edge)**	**Bumped Si/glass (double edge)**	**Bumped glass/ceramic (single edge)**	**Bumped Si/ceramic (single edge)**
A	76 seconds	78 seconds	91 seconds	89 seconds
B	190	213	263	204
C	190	118	241	197
D	176	120	215	194
E	91	67	100	98
F	137	118	124	148

Table 4.1. Flow times (in seconds) of underfill materials A-F with different sample sets and dispense methods.

Figure 4.1.1, and figure 4.1.2 show graphical comparisons of the relative underfill times of the different sample sets. Figure 4.1.1 compares the relative underfill times of sample sets 1 and 2. Figure 4.1.2 compares the relative underfill times of sample sets 1 and 4. The underfill materials have been rearranged according to their relative flow times to show the fastest flow material on the left to the slowest flow material on the right.

The data collected for the flow times of the underfill materials shows that Material A has the fastest flow time for 3 out of the 4 sample sets in Table 4.1. Material E has the fastest flow time for the bumped silicon die on glass substrate sample, and slightly slower flow times than Material A for the other samples. Material B has the slowest flow time of all the materials. It can be seen in Figure 4.1.1 that for most materials, double edge dispensing reduced the amount of flow time needed to underfill the entire die with single edge dispensing. This is due to the fact that there are two flow fronts instead of a single one to carry the underfill flow. Materials A and B did not show a decrease in the underfill flow time when double edge dispensing was used instead of the single edge method. This could be explained by materials properties involved which were not tested. Materials A and B were from the same vendor and therefore would have similar materials properties. Another factor which may have impeded the flow of the underfill is the cleanliness of the die or the substrate. Some of the dies or substrates may have had contaminants on the surface with interfered with the underfill flow. From Figure 4.1.2, all materials showed a faster flow time on the glass substrate than on a ceramic substrate. This is because a ceramic substrate has a rougher surface than a glass substrate.

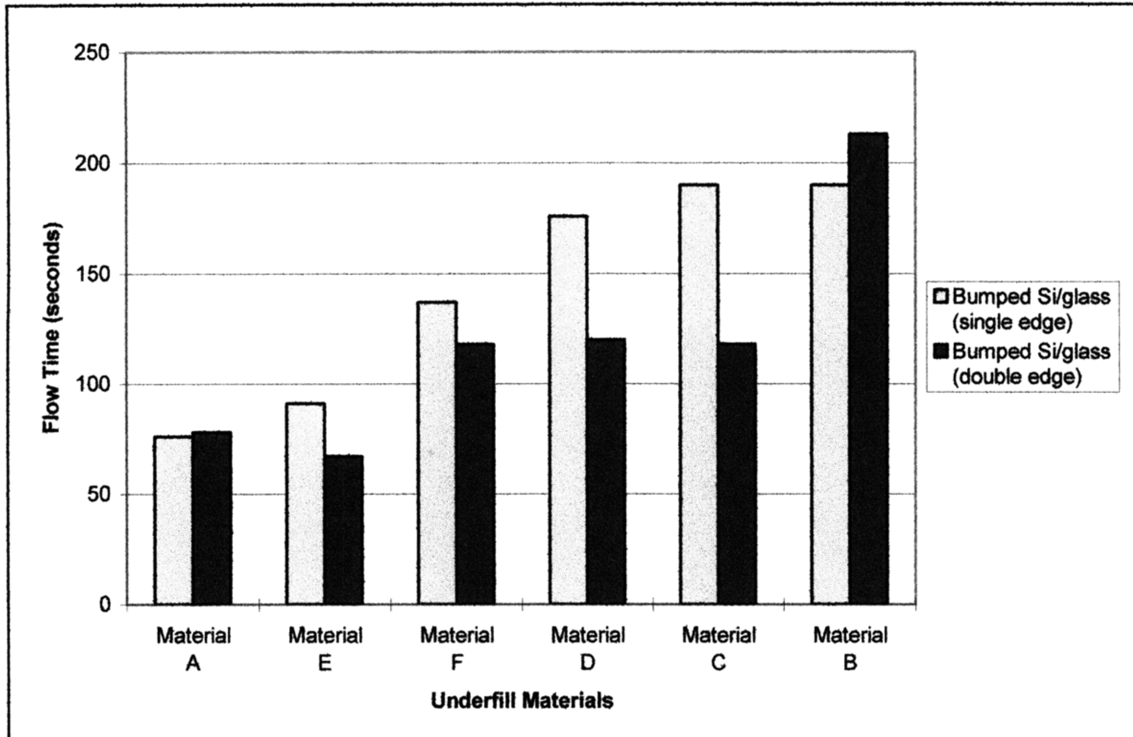


Figure 4.1.1. Relative underfill material flow times for samples made with bumped silicon chips on glass substrates, using single edge dispense and double edge dispense methods.

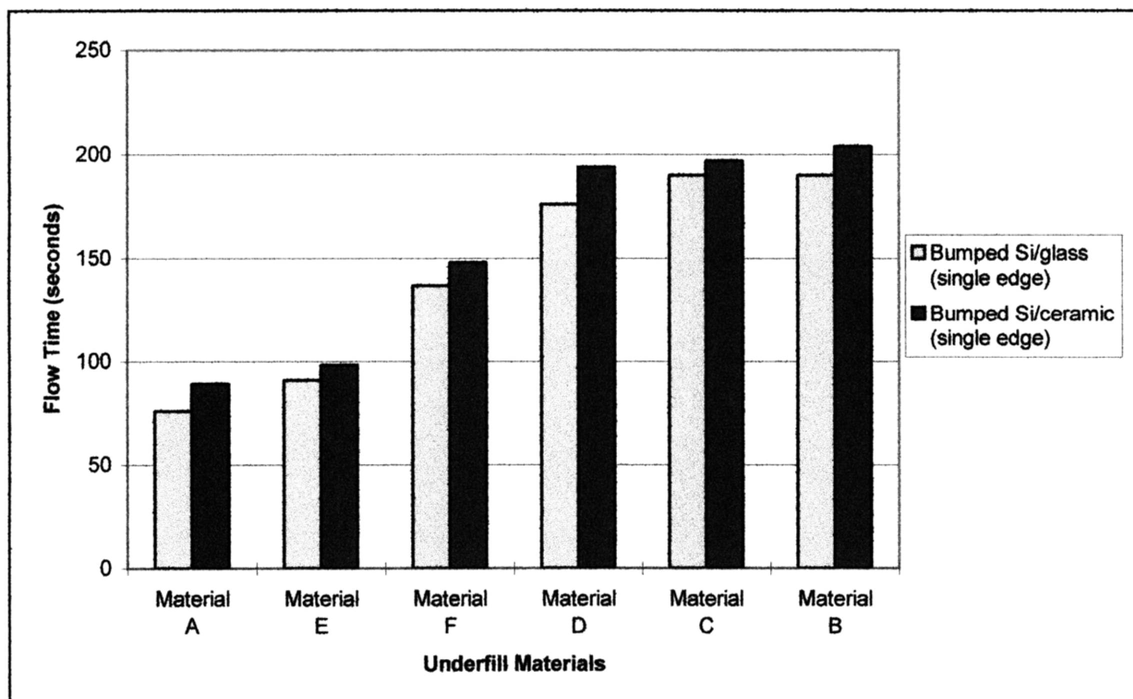


Figure 4.1.2. Relative underfill material flow times for samples made with bumped silicon chips on glass and ceramic substrates, using single edge dispense method.

Materials A, E, and F all have low filler particle contents, 65% or lower, and therefore contributes to the faster flow speeds. However, the filler particle content of the underfill materials do not correlate completely to the flow times, as shown in Figure 4.1.3. Other material properties such as the filler particle sizes and the chemistry of the underfills also contribute to the flow rate of the underfill.

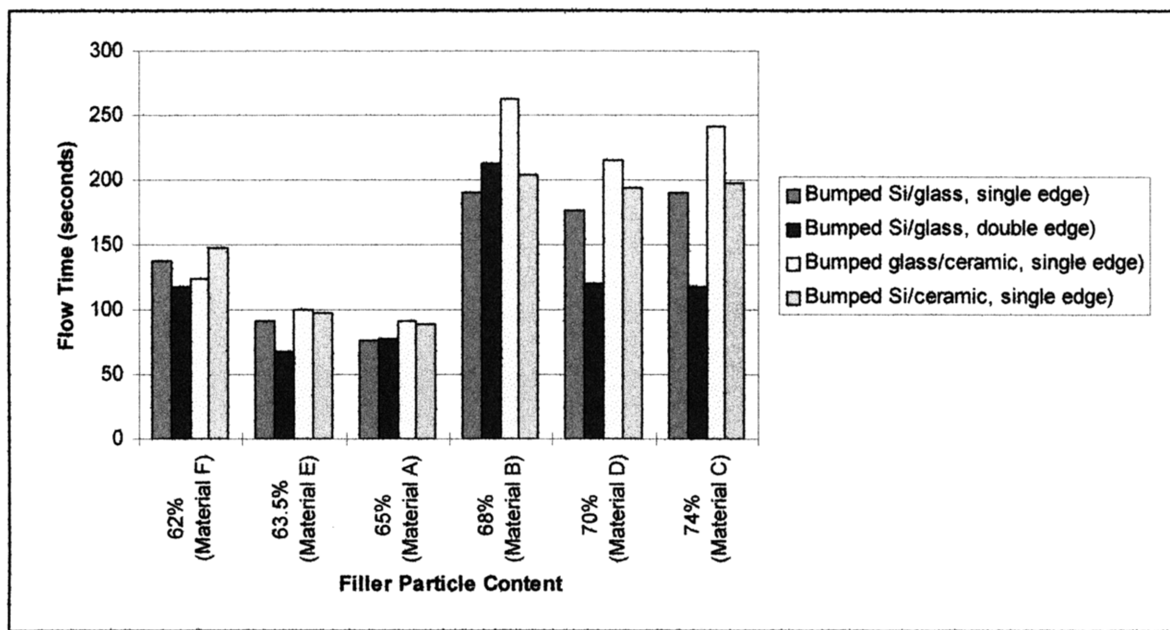


Figure 4.1.3. Material filler particle content verses material flow time.

The flow patterns of the underfill materials were determined by viewing the samples that were made with a glass substrate or a bumped glass die. An even flow front is desired to avoid the formation of voids. Materials D, E and F showed very uniform flow fronts, while the other materials showed non-uniform flow fronts. There were no voiding problems seen with any of the materials during underfilling when using single edge dispensing. However, materials C and D showed voids after curing of the underfill. These voids could have been caused by air bubbles that might have been entrapped within the material inside the dispense tube. Voids could also arise from contamination on the substrates which may affect the different chemistries of the underfill materials. When the samples were made using double edge dispensing, more voiding problems were seen due to the two flow fronts enclosing on itself near the exit end. Materials B and C exhibited this air entraption problem during double edge dispensing.

4.2. Particle Settlement Evaluation

From the cross-sectioning of all the underfill materials, any particle settlement within the underfill material was observed. Materials B, D, and F showed no particle settlement problems. Material E appeared to have a resin rich layer at the top. However, after closer examination, very fine filler particles were found. This showed a very clear distribution of the different particle sizes within the material with smaller sized particles near the top and larger particles at the bottom. Material C showed some particle settlement, with a

slight resin rich layer at the top. Materials A showed significant particle settlement with a distinct resin rich layer at the top. Figure 4.2.1 shows a picture of the cross-sectioned sample made with material A. See Appendix 6.1 for cross-section pictures of other materials. Significant particle settlement within the underfill material could change the material properties in that the resin rich layer will have a different CTE than the particle filled layer. This property difference within the material could lead to reliability problems.

4.3. Thermal Stress Analysis

Table 4.3.1 shows the results of warpage measurements made by the mechanical profilometer. (See Appendix 6.2 for the raw warpage data.) . The CTE of the materials are also included in Table 4.3.1 for comparison with the warpage values. The warpage data collected by the PPL Mirage was not included in this report due to the lack of repeatability of the machine. Warpage in the flip chip package results from thermal stresses caused by the curing step of the process. These thermal stresses are produced by the shrinkage of the polymeric material when it is cured, and also from the CTE mismatch between the silicon chip, the ceramic substrate, and the underfill material. The highest measurements were recorded near the center of the die. Material A showed the highest warpage of the die caused by the curing of the underfill, followed by materials C, D, and F. This positive warpage value of the die imposes a compressive stress on the solder bumps, which reduces the overall shear strain on the solder bumps. This improves the reliability of the whole package. As long as the compressive stress on the die does not cause the back of the die to crack, a higher warpage value is better for the reliability of the solder joints of the flip chip.

The CTE mismatch between the silicon chip, ceramic substrate and the underfill material does not seem to correlate completely to the amount of warpage measured. An underfill material with a higher CTE will have a bigger mismatch with the CTE of the silicon chip and substrate, as discussed earlier in section 2.0. Therefore, there should be a larger amount of warpage in the chip package with these higher CTE underfill materials. However, underfill material F, which has the highest CTE, did not show the highest warpage value. This could suggest that the warpage value depends more on the shrinkage of the polymeric material when it is cured.

Underfill Material	**Highest warpage value across center of die (mils)**	**CTE (ppm/°C)**
A	0.183	22.3
B	0.156	22.8
C	0.166	19.7
D	0.158	22.1
E	0.126	19.3
F	0.158	26.1

Table 4.3.1. Highest warpage values of silicon die on ceramic substrate due to thermal stresses.

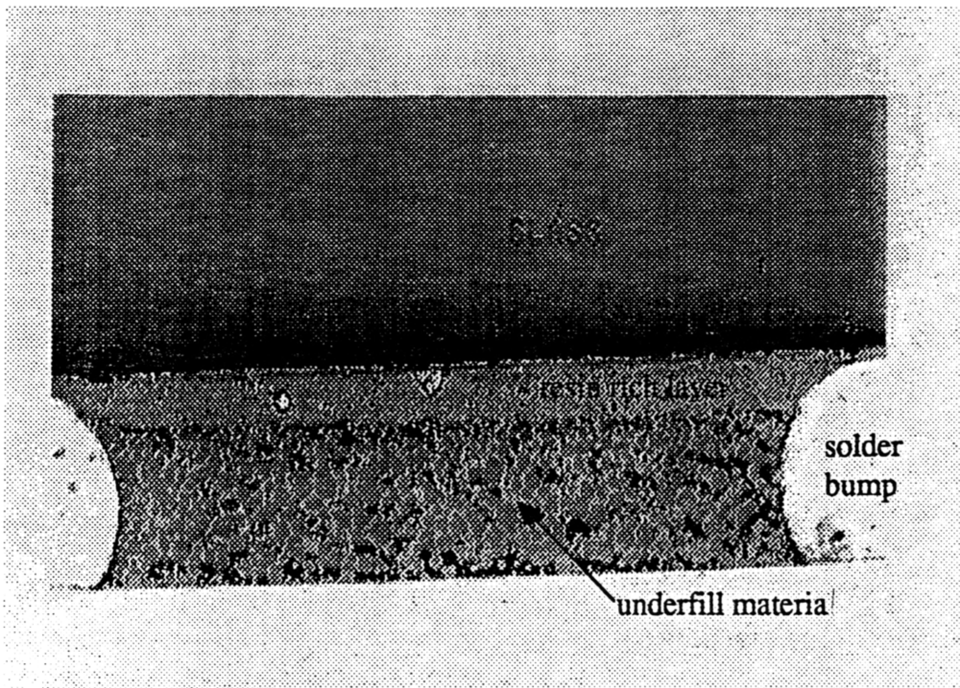


Figure 4.2.1. Cross section of sample made with underfill material A. There is significant particle settlement within the underfill material.

4.4 Reliability Testing

4.4.1. Pressure Cooker Testing

From the C-Scan results of the samples that went through pressure cooker testing, only the samples with underfill material D showed significant changes. Figure 4.4.1 shows the C-Scan pictures of two samples with material D taken at initial conditions and after 96 hours of pressure cooker testing. (The initial state pictures are on the left and the final state ones are on the right.) The lighter colored region seen on the perimeters of the dies in the final state pictures are areas of delamination. It is difficult to determine which interface delaminated from the C-Scan images. Materials A, B, and F showed some changes after the pressure cooker test. Material B showed some delamination at the underfill entrance and exit corners of the die. Materials A and F showed slight delamination areas at the corners of the die. Samples made with materials C and E showed no changes in the C-Scan pictures. (See appendix 6.3 for C-Scan pictures of pressure cooker samples of materials A, B, C, E, and F.)

Table 4.4.1 shows the results of the stud-pull strength test. Materials A, B, C, and D all showed interfacial delamination of the underfill as the method of failure, which demonstrates the fact that they were affected by the moisture of the pressure cooker test. Materials A and C showed delamination at the underfill and substrate interface, while Materials B and D showed delamination at the underfill and chip interface.

Underfill Material	Average Pull Force (lbs.)	Method of Failure
A	290	Delamination at underfill and substrate interface
B	116.85	Delamination at underfill and chip interface
C	257.5	Delamination at underfill and substrate interface
D	95.35	Delamination at underfill and chip interface
E	296.5	Cracked substrate
F	311	Cracked substrate

Table 4.4.1. Stud pull values and the mode of failure of underfilled samples after the pressure cooker test.

The C-Scan images correlated somewhat to the results of the stud pull test. Figure 4.4.2 - 4.4.3 shows the C-Scan images of 6 samples, each with a different underfill, with the corresponding pictures taken after the stud pull. The C-Scan image for material D showed a large area of delamination at the edges of the die. The delamination area would provide the least amount of resistance to a tensile load, which correlates with the mode of failure being delamination at the underfill and chip interface. Material D also had the lowest pull force, due to such a large area of delamination. Materials A and B showed some delamination in their C-Scan images. Even though these delamination regions were small, their respective modes of failure were delamination at the underfill and substrate interface, and delamination at the underfill and chip interface. This suggests that the adhesion strengths of materials A and B were both affected by the

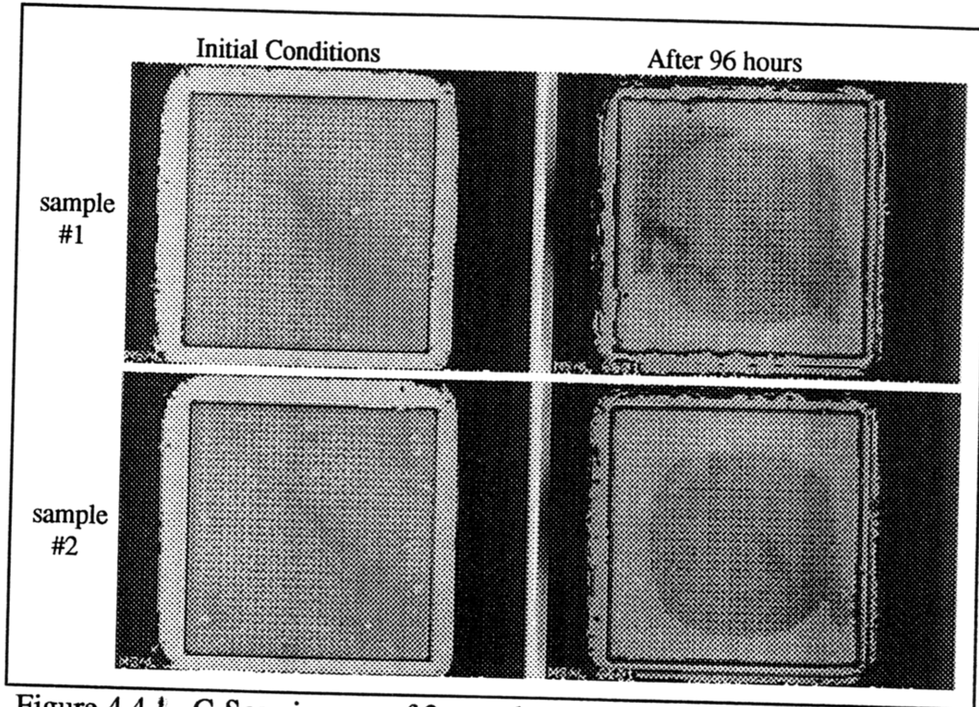


Figure 4.4.1. C-Scan images of 2 samples made with underfill material D, before and after the pressure cooker test. Images on the left are the initial condition images, and the images on the right were taken after 96 hours of pressure cooker testing.

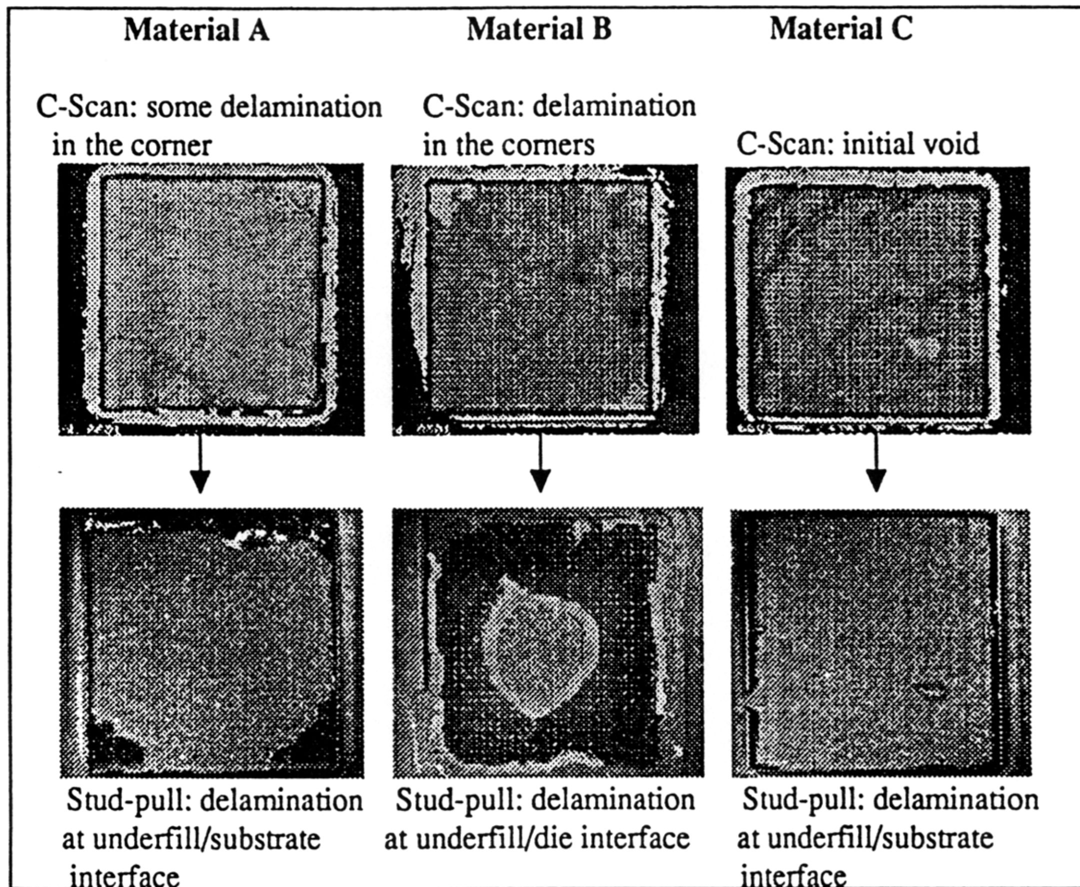


Figure 4.4.2 C-Scan vs. stud-pull correlation of samples after 96 hours of pressure cooker testing. Materials A-C.

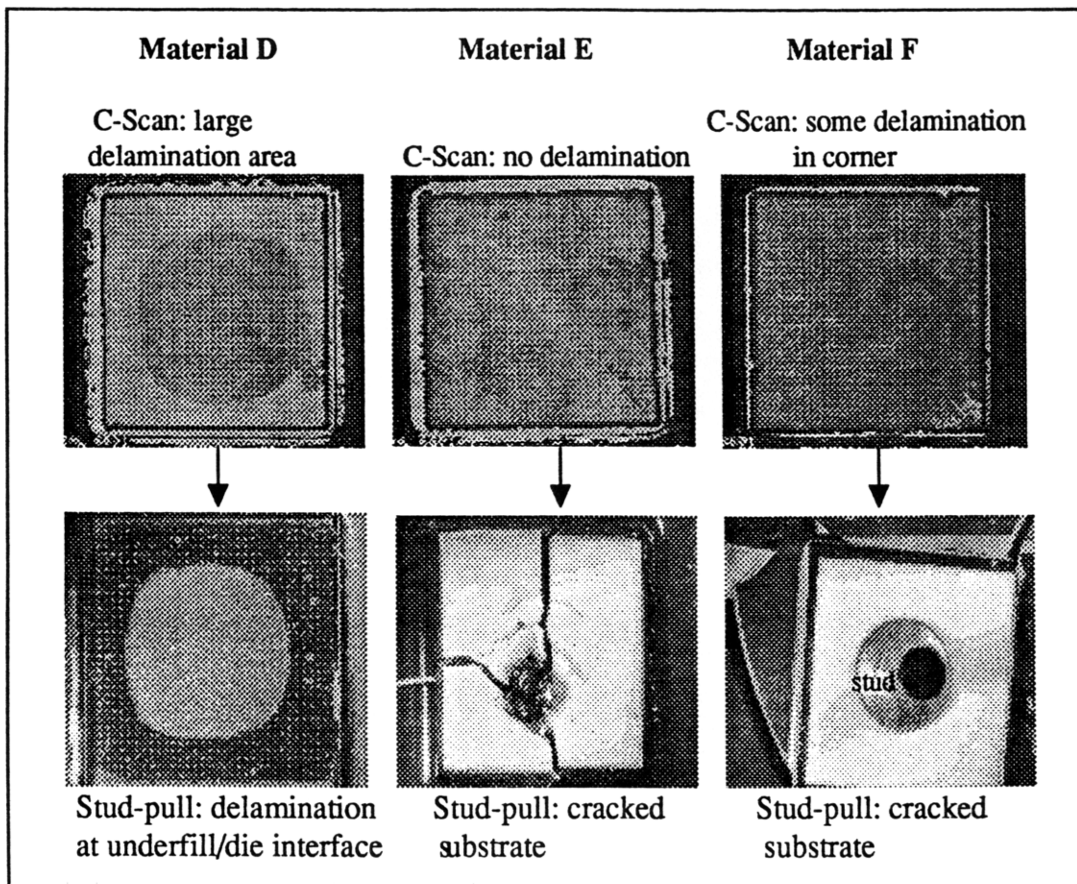


Figure 4.4.3. C-Scan vs. stud-pull correlation of samples after 96 hours of pressure cooker testing. Materials D-F.

moisture from the pressure cooker. For material F, although the C-Scan images exhibited slight delamination at the corner of the die, the samples did not fail due to delamination. This could be due to the fact that the delamination region seen by C-Scan was such a small area that it was not enough to cause delamination of the entire underfilled area. The mode of failure was substrate cracking, which suggests that the underfill adhesion strength was not affected by moisture. Material C showed no changes in the C-Scan images before and after the pressure cooker test. However, the samples failed for delamination at the underfill and substrate interface. This could be caused by the voids which were present in the initial sample. Also, even though delamination was not seen during the pressure cooker testing, the adhesion strength of the underfill material was still affected by the moisture. This weakened adhesion strength, along with the voids, allowed delamination of the underfill to the substrate to occur when put under a tensile load. The C-Scan images of samples made with material E showed no delamination. This data correlates well with the samples' modes of failure, substrate cracking. The adhesion strength of the underfill material E was not affected by the pressure cooker test, and there were no areas of delamination.

Water absorption has been found to decrease with the T_g of a polymer because of strong hydrogen bonds. This would explain the poor result of material D, which has the highest T_g of 190°C. Even though material B has the lowest T_g of all the materials, it did not show the best results. This is probably due to the fact that its T_g is too close to the testing temperature and therefore was affected by the moisture. It seems that a T_g of around 140°C, as it is for materials E and F, is desired to prevent water absorption in the flip chip package.

4.4.2. Thermal Cycling

The C-Scan results show that after 1500 cycles of thermal cycling, materials C, D, E, and F had no changes. Material A showed no signs of delamination; however, some of the bumps on the die looked faded. This could suggest bump interconnection failure. Material B showed some delamination at the corners, and some fading of the bumps. After 3000 cycles of thermal cycling, the C-Scan results show that materials C, E, and F still had no changes. However, material D showed a noticeable amount of bump fading. Material A still exhibited bump fading, and material B showed a larger area of delamination. From these results, materials A, B, and D are more susceptible to thermal cycling failure than the other materials. The bump fading observed in some of the samples can be explained by the incomplete wetting of the solder bumps by the underfill due to flux residue. If the underfill material fails to surround the solder bump completely, this will lead to a delaminated region that has been termed the "halo" defect.[8] This "halo" defect, or bump fading, will eventually cause a failure in the electrical connection.

Table 4.4.2 shows the results of the stud pull strength test. Materials A, B, and D showed delamination of the underfill as the method of failure. This concludes that these materials are more susceptible to failure under thermal cycling. Materials A and D had delamination at the underfill and substrate interface while material B had delamination at the underfill and silicon chip interface. Materials C, E, and F failed by the destruction of the substrate. This shows that the thermal cycling did not have a noticeable affect on the underfill materials' adhesion properties.

The C-scan results correlate well to the stud pull results. Both sets of data show that materials A, B, and D are more likely to be affected and fail when subjected to thermal cycling.

Underfill Material	Average Pull Force (lbs.)	Method of Failure
A	322	Delamination at underfill and substrate interface
B	263	Delamination at underfill and chip interface
C	417	Cracked substrate
D	313	Delamination at underfill and substrate interface
E	415	Cracked substrate
F	425	Cracked substrate

Table 4.4.2. Stud pull values and the mode of failure of underfilled samples after thermal cycling.

4.4.3. Thermal Shock Testing

The C-Scan results show that after 1500 cycles of thermal shock, materials E and F had no visible changes. Materials A, C, and D showed minor bump fading. Material B showed noticeable amount of bump fading and some delamination. The bump fading seen can be explained by the "halo" effect, as previously mentioned. Since this effect is mainly due to flux residue on the solder bumps, it is difficult to conclude that materials A, C, and D have been effected by the thermal shock testing. However, from the facial delamination seen in material B, it can be concluded that material B is susceptible to failure when put under thermal shock.

4.4.4. JEDEC Level 3 Testing

The C-Scan results of the underfilled samples after the moisture preconditioning and IR reflow showed that there were no changes in any of the materials. After 1500 cycles of thermal cycling, C-Scan showed that the underfilled samples which were solvent cleaned had better results than the semi-aqueous cleaned samples and the non-cleaned samples. After 3000 cycles of thermal cycling, the solvent cleaned samples still proved to have better results than the other samples. The semi-aqueous cleaned samples had comparable results as the non-cleaned samples; with materials A, B, and C showing signs of bump fading and delamination, and material F showing no signs of any changes. For the solvent cleaned samples, materials C, and E showed no changes. Materials A, D, and E showed minor bump fading problems and material B had small delamination problems. The solvent cleaned samples should have had the least amount of flux residue, if any. Therefore, the better results seen in these samples is expected. However, some of the materials still exhibited the bump fading problems. This could suggest that the problem is not only due to flux residue, but is also underfill material dependent. From these results, Materials A, B, D, and E seem to be more affected by the JEDEC level 3 testing. These materials exhibit delamination between the underfill and the solder bumps.

This delamination or gap between the underfill and bumps could eventually lead to the failure of the flip chip device.

5.0. Conclusion

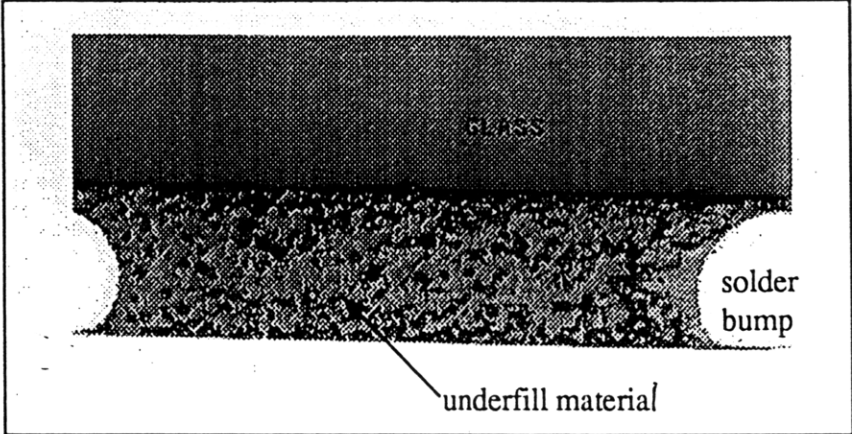
The different variables and material properties that were examined for the selection of top underfill materials did not all possess equal significance or importance. The reliability of the underfill materials was the most important property, followed by the manufacturing variables which affected the throughput time of the whole process, such as material flow time and cure time. The different significance of the variables was taken into great consideration when the overall ranking of the materials was made. The overall rank of the materials from best to worst is: material F, material E, material C, material D, material A, and material B. Materials F and E consistently showed the best overall results, with excellent reliability properties, fast flow time and cure times. Although the tests and evaluations performed were not exhaustive, it is reasonable to conclude that materials F and E are the best choices as underfill materials for the flip chip device. It can also be concluded from the JEDEC level 3 tests that the solvent cleaned samples gave the best results. This should be taken into consideration when the whole flip chip assembly process is designed.

It was difficult to correlate some of the material properties of the underfill materials to their process properties, due to the various processing parameters involved. But a few conclusions can be made regarding the properties an underfill material should possess, according to the results of the best materials F and E. The filler particle content of the underfill should be less than or equal to 65%. It seems that when the filler content is above 65%, the flow speed is reduced. A low weight loss percentage during cure is another desired property. Materials F and E had weight loss percentages of less than 1%. The lack of reduction in the mass of the underfill will prevent its other properties from being affected. This would better ensure that the reliability properties are not affected either. Another material property that both materials F and E had was a glass transition temperature, T_g, of about 140°C. This seems to be an optimal T_g for the proposed flip chip assembly. Too low of a Tg, such as it was for material B, will create reliability problems because it will be too close to operating temperatures. Too high of a T_g will cause moisture absorption problems.

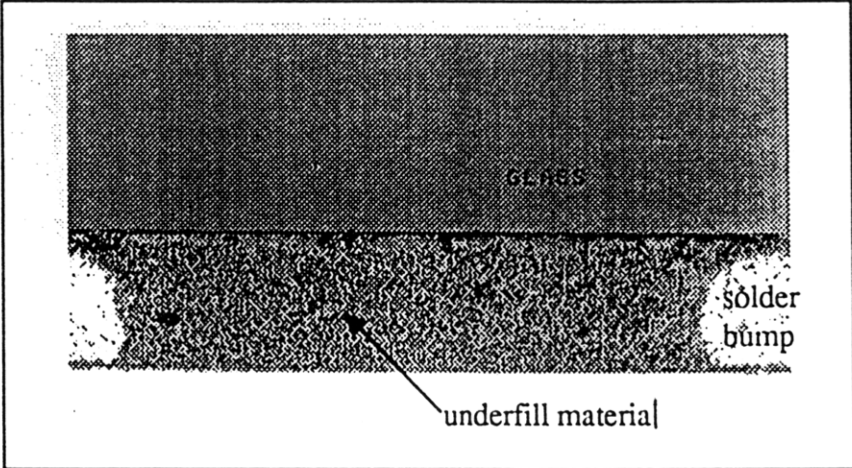
Even though it has been tested and proved that materials F and E have the desired properties for flip chip, more process development and testing should be performed to maximize their manufacturing and reliability properties. For example, the dispense pattern of the underfill material could be altered in order to reach the maximum processing rate. The curing temperature and profile could also be varied to create the least amount of overall stress on the solder bumps. All of these issues should be considered for the next stage of development of the underfill material in the flip chip processing technology.

6.0. Appendices

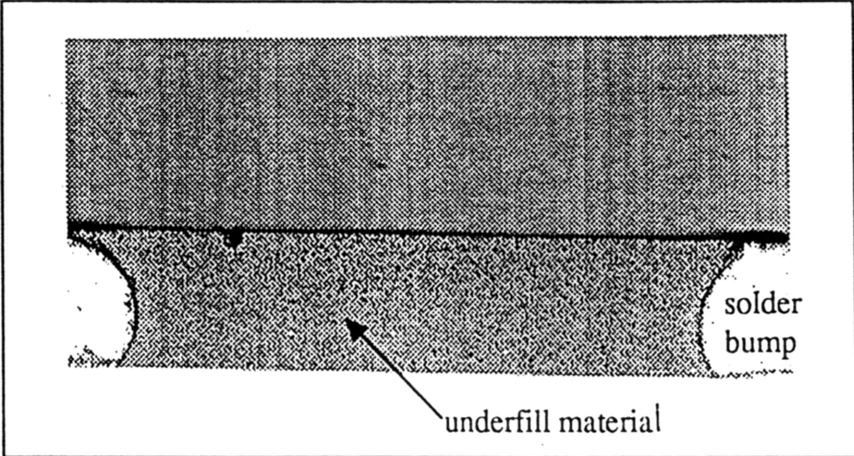
6.1. Photos of cross-sectioned samples made with material B, C, D, and F for particle settlement evaluations.



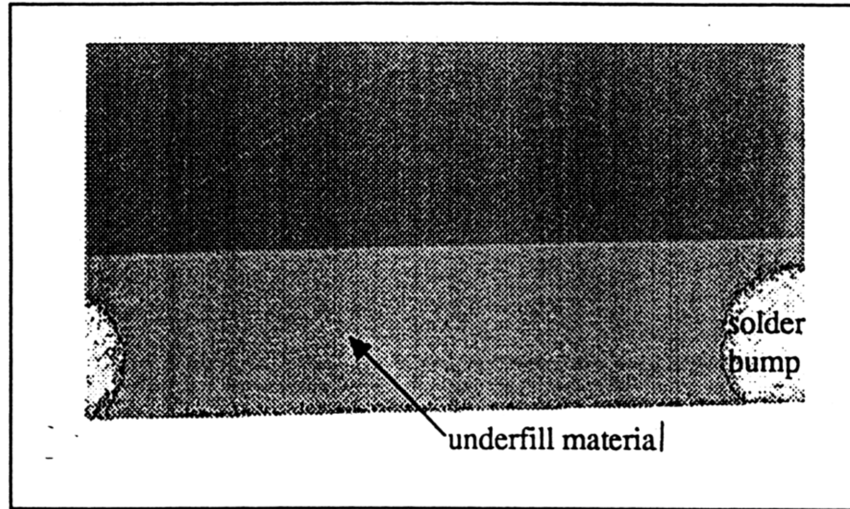
Material B



Material C

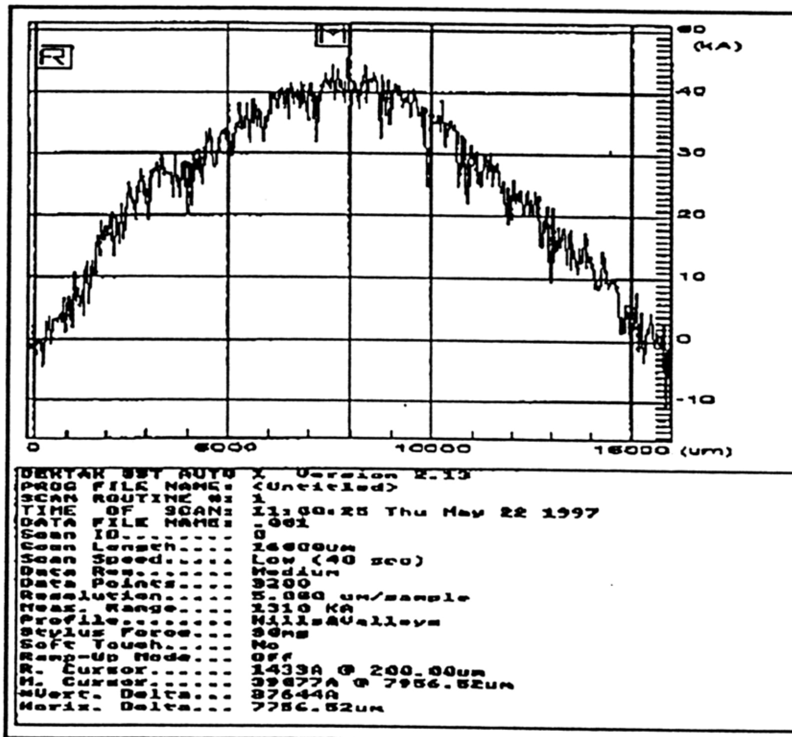


Material D

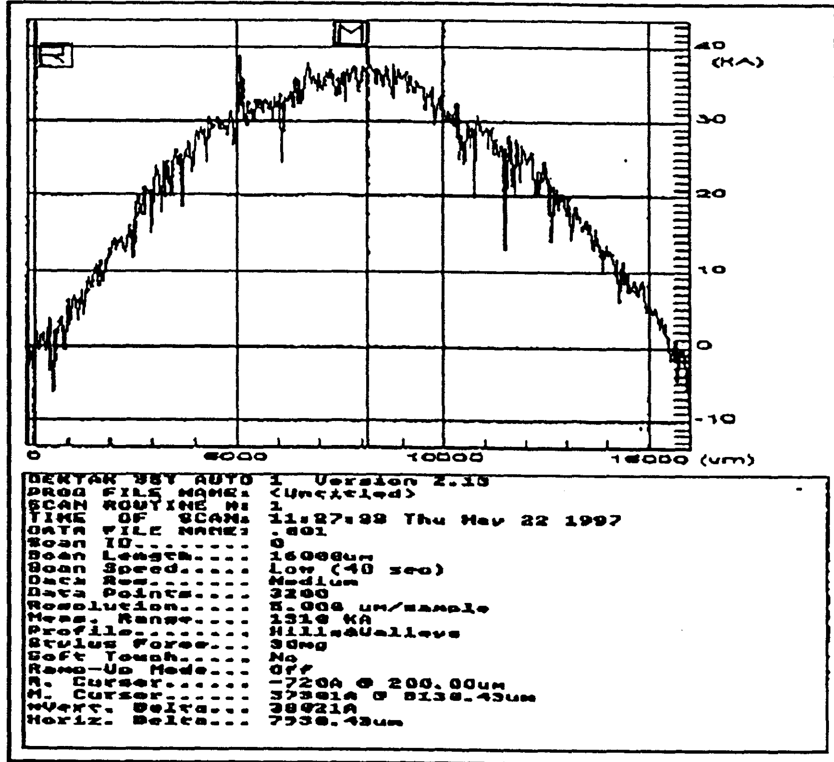


Material F

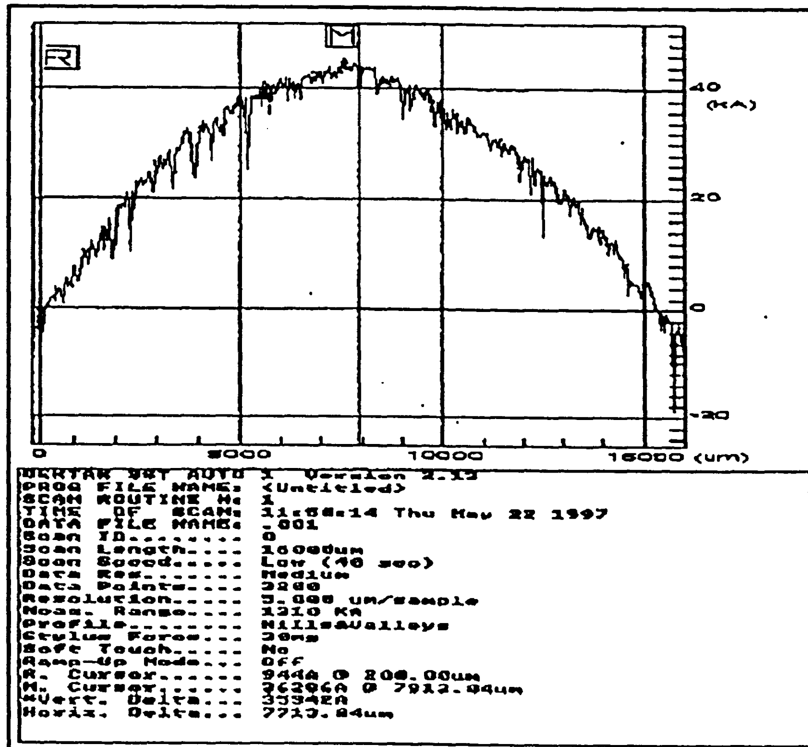
6.2. Raw warpage data from mechanical profilometer for materials A-F.



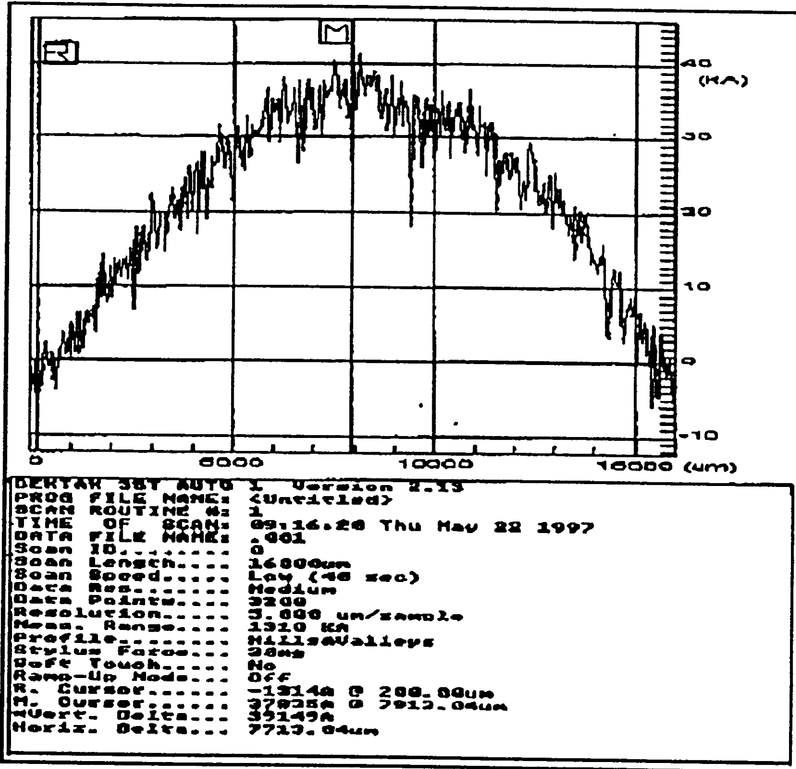
Material A



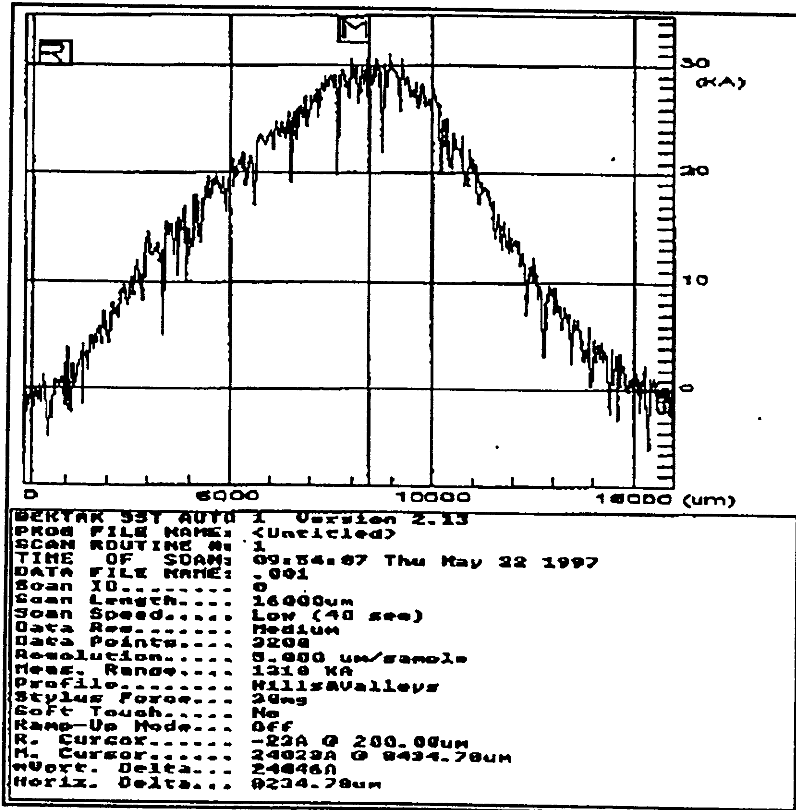
Material B



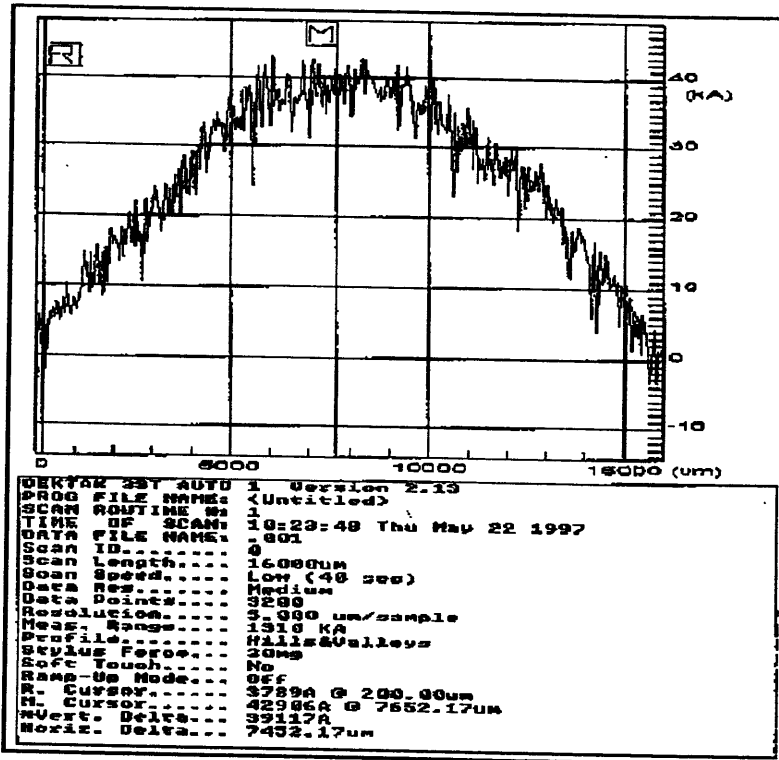
Material C



Material D

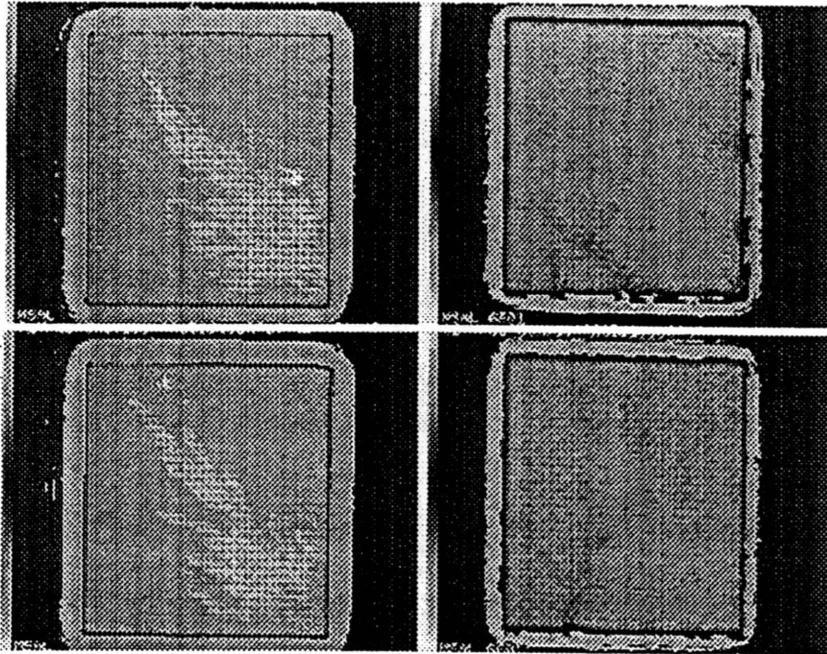


Material E

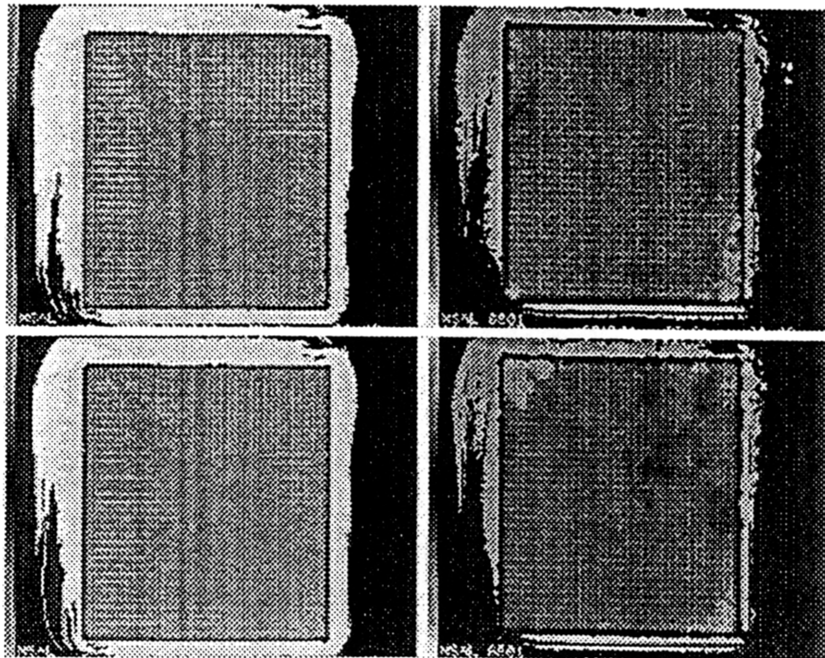


Material F

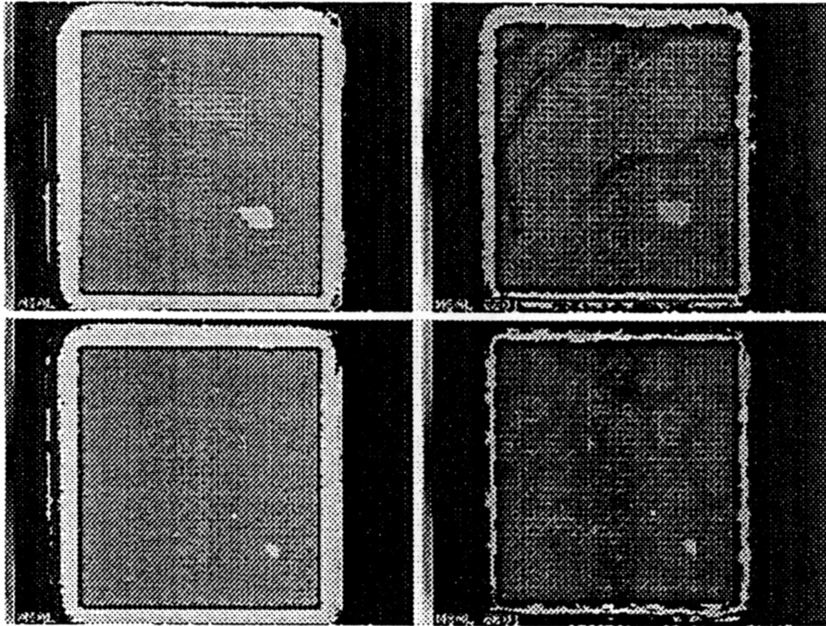
6.3. C-Scan Images of underfilled samples before and after pressure cooker test.



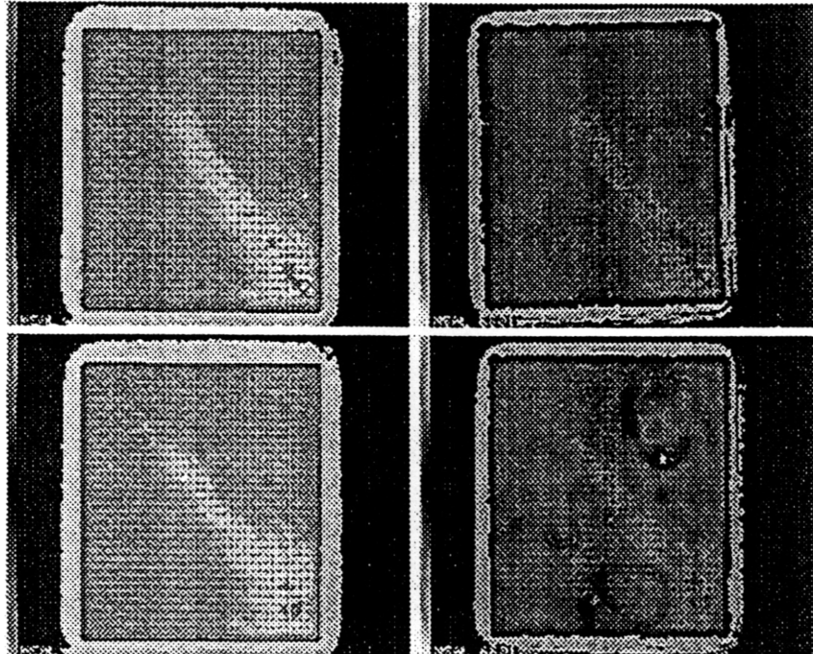
Material A



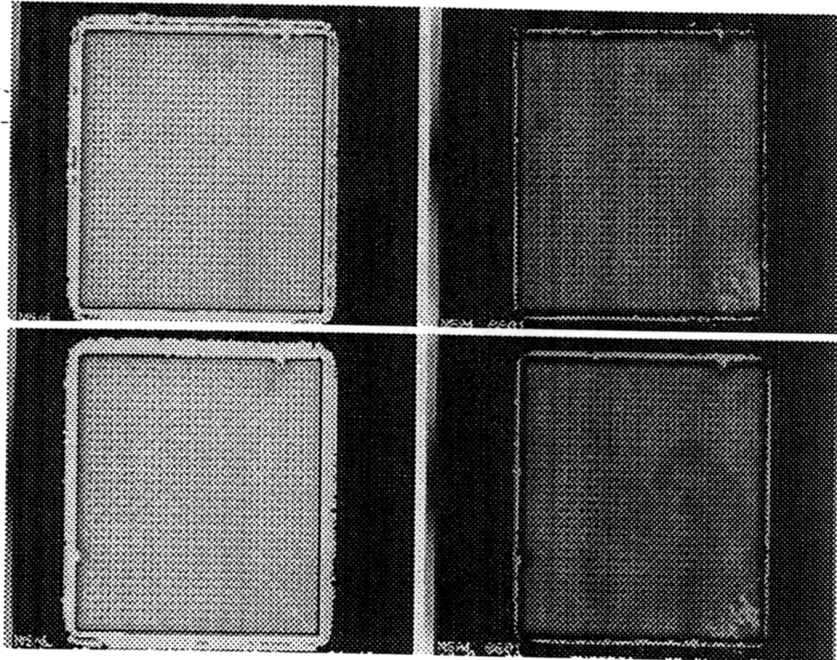
Material B



Material C



Material E



Material F

7.0. Bibliography

1. Shih Hsu, et al., "Flip Chip Interconnect Technology," Digital Equipment Corporation Semiconductor Packaging. October, 1995.

2. John H. Lau, *Flip Chip Technologies,* McGraw-Hill, 1995, pp. 1-82.

3. John H. Lau, "Design, Materials, Process, and Reliability of BGA, CSP, DCA, and Flip Chip Assemblies," Class taken at Digital Equipment Corporation, April 4, 1997.

4. D. Zoba, "Review of Underfill Encapsulant Development and Performance of Flip Chip Applications," *Advancing Microelectronics,* July/August 1996, pp. 10-15.

5. Matthew K. Schweibert, William H. Leong, "Underfill Flow as Viscous Flow Between Parallel Plates Driven by Capillary Action," *IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium,* 1995, pp. 8-13.

6. Chao-Pin Yeh, Wen X. Zhou, Karl Wyatt, "Parametric Finite Element Analysis of Flip Chip Reliability," *The International Journal of Microcircuits and Electronic Packaging,* Volume 19, Number 2, Second Quarter 1996, pp. 120-127.

7. Trirat Hongsmatip, "Flip Chip Underfill Materials Characterization (MSAL 6159)," Digital Equipment Corporation Materials and Structures Analysis Laboratory, April 1997.

8. K. D. "Acoustic Imaging Finds 'Halo' Defect In Flip Chips," *Technology News,* January 1998, p. 30.