Metrology of SIMOX Buried Oxide and Nitride/STI CMP

by

Jung Uk Yoon

Submitted to the Department of Materials Science and Engineering in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electronic Materials

at the

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Abstract

The increase in demand for faster and more powerful microprocessors in recent years has been the driving force to introduce new materials and processes into semiconductor fabrication facilities. As each fabrication facility tries to maximize its yield, it is mandatory that there exist metrology techniques to characterize both materials and processes. This mandate is the motivation behind this thesis. In this thesis, the metrology of two different systems used in VLSI technology are investigated.

The first system is the material, Separation by IMplanted OXygen (SIMOX) buried oxide. SIMOX technology has been studied extensively as a viable alternative to bulk silicon technology in radiation-hard and low-power applications. However, there is still a lack of knowledge on the nature of the defects present in the SIMOX buried oxide and their impact on basic BOX electrical characteristics, such as BOX high-field conduction. In this thesis, greater understanding about the excess-silicon related defects in the buried oxide has been obtained concerning their nature, origin, and impact on the conduction characteristics. Further understanding about the silicon islands in the buried oxide has also been obtained concerning their formation and impact on the high-field conduction characteristics. Finally, a metrological application of the BOX high-field conduction model is demonstrated.

The second system is the process, Nitride/Shallow Trench Isolation (STI) Chemical Mechanical Polishing (CMP). CMP processes have been heralded as a way to planarize films and structures on wafers to a degree which has not been possible before. However, recent studies have shown that the uniformity of CMP processes depends on the layout-pattern density. To address this issue, an oxide CMP model has

been developed to show the relationship between layout-pattern density and the polish rate. However, there is an uncertainty as to how this single-material system model can be extended to other material systems and dual-materials systems. In this thesis, the metrology and modeling techniques for oxide CMP are extended to nitride CMP in order to understand the pattern-density and materials dependence for this particular CMP process. In addition, the planarization and uniformity of the two-material system for STI structures is investigated. A model explaining the relationship between a particular STI layout-pattern density and the resulting planarization is developed.

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"He who dwells in the shelter of the Most High will rest in the shadow of the Almighty. I will say of the Lord, "He is my refuge and my fortress, my God, in whom I trust."
Psalm 91:1-2

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1. Introduction to Metrology

1.1 Motivation for Metrology

Overview of VLSI Technology

Recently, the semiconductor industry has enjoyed enormous growth. This growth has been fueled by a desire for increased automation and for faster and more powerful microprocessors. These products have been used in everything from automobiles to dolls to personal computers. This growth in demand has caused an increase in the number of fabrication facilities to manufacture microprocessors, memory, and other integrated circuits. These fabrication facilities, called "fabs" for short, typically cost $500 million to $2 billion dollars in capital expense plus an enormous expenditure in people and materials. Operating costs for such fabs are prohibitively high so that few companies can afford to build and operate them. Unless these fabs generate profits, they cannot survive. Such a need to generate profits makes it imperative that the fab operate very cost-effectively. To be cost-effective, the fab needs to maximize the output, namely the amount of products, for a given input, namely the amount of raw materials and the operating cost. This ratio of output to input can be thought of as the final yield. Thus, cost-effectiveness is very closely tied to high yield. In such situations, metrology issues become key.

What is Metrology?

The Webster dictionary defines metrology as "the science of weight and measures." However, this definition falls short of describing how metrology is actually implemented in today's semiconductor industry. Metrology has evolved into an

independent discipline for monitoring a particular process step in the manufacturing line and as an aid to increase the yield for that particular step. Metrology can be broken down into three general steps: variation assessment, variation modeling, and variation impact. In variation assessment, the primary goal is to understand the source and extent of variation in a process step. Variation can be divided into either systematic or random components. These may be either process-dependent or random in nature. In variation modeling, a model is developed to describe the systematic variation component. Specific effects of any process parameter on the assessed variation can then be described by this model. In variation impact, the primary goal is to understand the relationship between parameter variation and the resulting performance change of the product or its manufacturability and to identify methods for reducing the impact of variation.

Motivation for Metrology

Metrology, as described above, is crucial for improving the overall yield. Each process step must be monitored to control variation, as the final product-yield is very closely related to the yield of each individual processing step. For the production of microprocessors, a wafer will typically see approximately 400 processing steps before its completion. If each step yields at a seemingly high 99 % value, the final yield will only be 1.8 %. Only when the yield for each step exceeds 99.99 %, will the final yield be above 90 %. Thus, the yield requirement for each process step is very high and the process must be under continual tight control.

Both wafer- and die-level uniformity are very important attributes. As wafers may contain anywhere from 30 to 200 chips, wafer-level uniformity will determine which chips will be functional at the process's end. Even within each die, which is a much

smaller area than that of the wafer, there may exist large variations not seen at the wafer-level. These variations must be monitored and understood in order to reduce the overall variation range, thus improving the yield. For these above reasons, metrology techniques must be developed for each process step in order for better understanding and control.

1.2 Thesis Overview

The goal of this thesis is to study the metrology of two different systems used in VLSI technology. The first system is the material, Separation by Implantation of Oxygen (SIMOX) buried oxide, and the second system is the process, Nitride/Shallow Trench Isolation (STI) Chemical Mechanical Polishing (CMP). Each of these material and process systems is described in more details below.

SIMOX Buried Oxide (BOX)

SIMOX wafers have been studied extensively as a potential next-generation substrate for low-power and rad-hard applications. However, because device engineers have been mostly interested in the properties of the top-silicon layer, not as much work has been carried out on the buried oxide. It is known that SIMOX buried oxide is quite different from thermal oxide both physically and electrically. However, there is still a lack of knowledge on the nature of the defects present in the SIMOX buried oxide and their impact on the basic BOX electrical characteristics, such as the BOX high-field conduction characteristics. This lack of knowledge has led to the lack of a suitable metrology technique for the buried oxide. In order to develop a suitable metrology technique, the physical characteristics of the buried oxide must be better understood in terms of the nature of other defects and their origin. In addition, the impact of defects on

BOX electrical characteristics must be better understood. In this thesis, a metrology technique based on a high-field conduction model is developed and used in conjunction with physical characterization techniques to better understand the defects in the SIMOX buried oxide and their impact on the BOX high-field conduction characteristics.

Nitride/STI CMP

CMP processes have been heralded as a way to planarize films and structures on wafers to a degree which has not been possible before. CMP processes have been used to planarize dielectric layers above interconnects, making it possible to have many more layers of interconnects than previously possible. Although much study has been carried out to understand the oxide CMP process and to improve its uniformity at the wafer-level, recent studies have shown that die-level variation in oxide CMP can be as large or larger than wafer-level variation due to pattern-density differences in the structures underneath the dielectric layer. An oxide CMP model has been developed to show the relationship between layout-pattern density and the polish rate, and explains the die-level uniformity dependence on the pattern density of the underlying structures. In this thesis, the metrology and modeling techniques for oxide CMP are extended to nitride CMP in order to understand the pattern-density and materials dependence for this particular CMP process.

In addition, the metrology and modeling techniques based on oxide CMP are used to understand better the Shallow Trench Isolation (STI) CMP process. STI processes have become the preferred isolation scheme of choice for advanced ULSI technologies. In an STI structure, two materials with different blanket polish rates end up being polished at the same time. The final planarization and uniformity of this two-material system is not

well understood. A model explaining the relationship between a particular STI layout structure and the resulting planarization is developed.

2. Introduction to SIMOX Substrate Materials

2.1 Silicon-On-Insulator (SOI) Technology Background

SOI Technology Description

In recent years, Silicon-On-Insulator (SOI) materials have been investigated extensively as a viable replacement for bulk silicon in Complementary MOS (CMOS) Very-Large-Scale-Integration (VLSI) integrated-circuit technology. SOI substrates are wafers with a single-crystalline silicon device layer which is isolated from the substrate by an underlying insulator layer. Devices are fabricated on the top-silicon layer and isolated using either MESA, LOCOS, or STI isolation schemes. The underlying insulator layer provides complete isolation of devices from each other. The isolated devices are then interconnected in a similar manner to a bulk CMOS process.

Advantages of SOI Technology

The interest in SOI materials arises from the potential advantages that SOI technology has over bulk-silicon technology. These advantages are as follows [1] :

1. SOI technology can reduce MOSFET junction capacitance, thereby reducing of the total circuit capacitance by 15% to 30% depending on the particular design.
2. SOI technology can improve the switching behavior of MOS devices due to its sharper subthreshold slope, allowing a reduction of the MOSFET threshold voltage, thus increasing current drivability at low voltage.
3. SOI technology can lower the threshold-voltage temperature sensitivity.
4. SOI technology can reduce the required MOSFET junction area significantly, which also decreases the leakage current.

5. SOI technology is less sensitive to soft-errors due to its smaller channel volume.

6. SOI technology can also be radiation-hardened. Circuits built on SOI materials can withstand more radiation, such as X-rays, than those made on bulk silicon.

7. SOI technology can significantly reduce the complexity of the CMOS fabrication process. Mitsubishi Electric has estimated that 256Mbit and 1Gbit DRAMs fabricated using SOI substrates would require 40% - 50% less cost to produce compared to conventional bulk-substrate DRAMs.[2]

Memory applications such as SRAMs and DRAMs have been fabricated using SOI technology. The SOI structure for a DRAM cell provides better soft-error immunity and allows a reduction of the cell capacitor area. More than a 5X reduction in the cell capacitor size has been reported by Mitsubishi[3] and NEC[4]. The allowable operating voltage range is also wider on an SOI DRAM cell. This could allow reduction of the supply voltage below 1.5V without sacrificing either noise margin or performance.

Another application for SOI substrates is in satellite applications due to the radiation-hardness of SOI technology. By reducing the top-silicon film device layer thickness and by isolating the substrate from the device layer, soft errors can be reduced. The collection volume for α- particles is significantly reduced by at least one order of magnitude.[5]

Types of SOI Substrate Material

SOI wafers have been produced using many different techniques of which three have become the most prominent and the most widely used. They are the Silicon-On-Sapphire (SOS) technique, the Bonded Silicon-On-Insulator (BSOI) technique, and the Separation-by-Implanted-Oxygen (SIMOX) technique.

A significant amount of work has been performed on SOS, which was one of the first techniques to produce SOI wafers. This technology was developed in the late 1960's by Manasevit.[6] In this technique, silicon is epitaxially grown on sapphire, as sapphire has the same crystal-lattice structure as silicon. In order to grow <100> silicon, several different sapphire orientations have been successfully used, such as <0112>, <1012>, and <1102>. However, the lattice parameter mismatch between the silicon layer and the sapphire substrate is sufficiently large to result in misfit dislocations, as well as stacking-fault and edge-dislocation generation, in the silicon layer near the substrate. Although the defect concentration decreases as the silicon-film thickness decreases, the defect concentration still remains significantly high for 0.5μm thicknesses, which is approximately the thickness required for many VLSI applications. This lower silicon-film quality, combined with the high SOS wafer cost, has limited SOS uses to military and space applications for radiation-hard circuits, where the radiation-hardness advantages matter more than the substrate cost.

BSOI substrates are produced by bonding together two wafers, each with thermal oxide grown on their surfaces. When the two thermal-oxide layers come in to contact with each other, they bond, even at such relatively low temperatures as 500 °C. Once the wafers are bonded together, one of the substrates is etched back down to the desired device silicon layer thickness. Interest in BSOI stems from the ability to control relatively independently the thickness of the buried oxide and the top-silicon layer. In addition, the quality of both the top-silicon layer and the buried-oxide layer is superior to that of SOS and SIMOX. However, it is extremely difficult to achieve good uniformity of the silicon-film thickness over a wafer-level scale. Thus, the ability to control the final thickness of

the top-silicon layer over the wafer becomes a crucial issue in deciding whether or not to adopt this technique for VLSI applications.

SIMOX substrates are made by creating buried oxide through oxygen implantation and high-temperature annealing as shown in Figure 2-1. Of all the different technologies for producing SOI wafers for VLSI applications, SIMOX is the most mature.[7] The advantage of the SIMOX method over other SOI substrate technologies is in its ability to achieve superior silicon-layer thickness uniformity at high throughput rates, and therefore at lower cost. For typical processes at comparative prices, the thickness uniformity of SIMOX is 3nm for a thickness of 200 nm, whereas the uniformity for BSOI is 10 nm for the same thickness. Top silicon-layer thickness uniformity is an essential manufacturing requirement for ultra thin-film SOI devices.

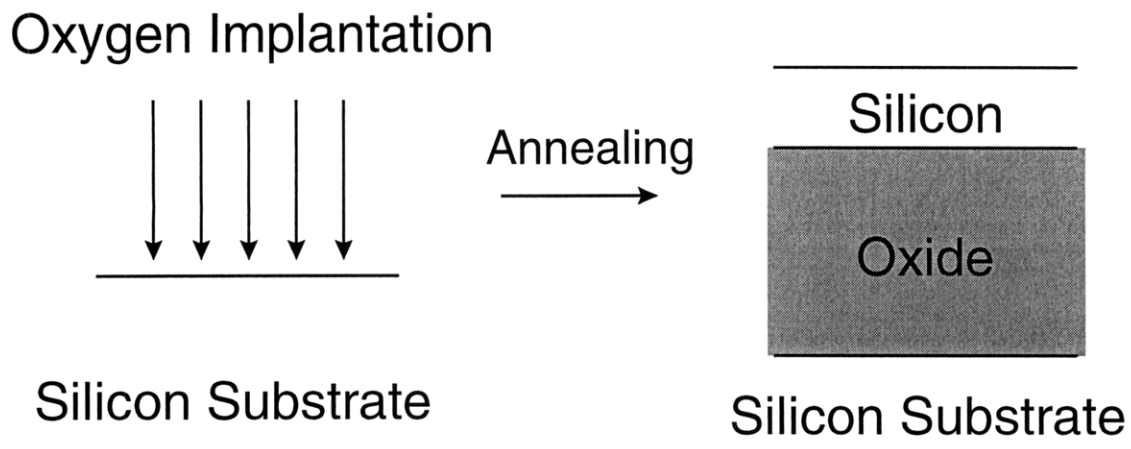


Figure 2-1 Graphical illustration of SIMOX substrate manufacturing process.

2.2 Separation-by-Implantation-of-Oxygen (SIMOX) Technique

History of the SIMOX Technique [8]

This technique was first developed in the 1970's. However, the quality of the top-silicon layer did not meet the requirements for device fabrication, resulting in very leaky transistors. In addition, the effect of different implantation and annealing parameters was not well understood. However, the quality of the top-silicon layer steadily improved over the years. Different vendors started to come out with SIMOX wafers that met the standards for VLSI applications.

Overview of the SIMOX Technique

SIMOX substrates are formed by implanting oxygen ions into a silicon substrate, and then annealing the substrate at a high temperature. Oxygen ions are accelerated at a voltage of around 200 keV before hitting the silicon wafer target. The silicon substrate is kept at a moderately high temperature (around 600 °C) to produce a high-quality single-crystalline silicon layer.[9] This substrate heating is usually generated by the implantation itself, but can also be controlled by separately heating the wafer chuck. The subsequent very high-temperature anneal at around 1300 °C in either an argon or nitrogen ambient is needed to heal the implant damage, recrystallize the top-silicon layer, and to form a continuous buried-oxide layer.[10] A typical dose of oxygen ions for SIMOX processes is $1.5 \times 10^{18} cm^{-2}$, producing a top-silicon layer of 200 nm and buried-oxide layer of 400 nm.

There are two main methods of performing the SIMOX implantation. One way is to implant the entire dose of oxygen at once and then to anneal it at a high temperature. This is called single-implant SIMOX. The second way is to implant the oxygen in small

doses with each implant followed by a high temperature anneal.[11] Usually the implantation is broken into either two or three steps. This technique is called multiple-implant SIMOX. The cumulative oxygen dose matches that of single-implant SIMOX. Because of the longer processing steps involved with multiple implants and anneals, multiple-implant SIMOX is usually more costly and has a lower throughput rate compared to single-implant SIMOX. Thus, although multiple-implant SIMOX wafers are known to have better quality silicon and buried-oxide layers, the single-implant method has become the standard method of producing SIMOX wafers.

General Motivation for Studying SIMOX Buried Oxide

As device quality is very closely related to the top-silicon layer quality, thus far, all of the effort for SIMOX material development has been concentrated on improving the quality of the top-silicon layer where the devices are fabricated.[12] Consequently, there has been relatively little research conducted on the SIMOX buried oxide, under the general assumption that the SIMOX buried-oxide is similar to thermal oxide. This trend is evident in the wafer specification sheet for commercially available SIMOX wafers.[13] The only parameter on the buried-oxide layer supplied by vendors is the buried-oxide thickness and uniformity based on spectroscopic ellipsometry. There is almost no information on the buried-oxide quality and reliability. This lack of BOX information hinders the adoption of SOI technology as a mainstream VLSI technology.

Recently, research has shown that SIMOX buried oxide is different from thermal oxide and that the properties of the buried-oxide layer can affect the device yield and reliability as well as the radiation hardness.[14] It has also been shown that the buried oxide has different electrical characteristics.[15] Thus, it is imperative that a deeper

understanding of the defects present in the buried oxide and the distinct BOX electrical characteristics must be gained in order to continue improving the quality of the buried oxide. A metrology technique for monitoring buried-oxide quality is also needed to insure the necessary quality control.

2.3 SIMOX Substrate Materials

In this thesis, SIMOX wafers with different buried-oxide stoichiometry and silicon-island contents were characterized. Group A includes standard single-implant SIMOX wafers which are known to be non-stoichiometric and contain silicon islands. Group B includes multiple-implant SIMOX wafers which are known to be stoichiometric and contain few or no silicon islands. Group C includes SIMOX wafers with supplemental-oxygen implantation. Supplemental-oxygen implantation is expected to turn the sub-stoichiometric oxide into stoichiometric oxide by supplying extra oxygen to bond with the excess silicon present in the buried oxide. Group D includes SIMOX wafers with supplemental silicon implantation. Silicon implantation is expected to create oxide with a higher level of excess silicon. Group E includes single-implant SIMOX wafers that have gone through different processing steps (changes in substrate temperature during implantation). All SIMOX wafers were made in collaboration with Ibis Co. Specific wafer specifications are shown in Table 2-1.

Group	Sample	Dose (1018cm-2)	Energy (KeV)	Substrate Temperature	Anneal Time (hr)	Anneal Temperature
A	Single #1	1.8	200	600	5	1300
B	Multi #1	1.8	N/A	N/A	N/A	N/A
	Multi #2	1.8	190	>600	6	1320
C	Suppl. O2	1.8+0.1	200	600	5	1310
			180		2.5	950
D	Suppl. Si #1	1.8 O_2	200	600	5	1310
					1	1300
	Suppl Si #2	1.8 O_2	200	600	5	1310
		0.01 Si	180	590	1	1300
	Suppl Si #3	1.8 O_2	200	600	5	1310
		0.05 Si	180	590	1	1300
	Suppl Si #4	1.8 O_2	200	600	5	1310
		0.1 Si	180	590	1	1300
	Suppl Si #5	1.8 O_2	200	600	5	1310
					1	1000
	Suppl Si #6	1.8 O_2	200	600	5	1310
		0.01 Si	180	590	1	1000
	Suppl Si #7	1.8 O_2	200	600	5	1310
		0.05 Si	180	590	1	1000
	Suppl Si #8	1.8 O_2	200	600	5	1310
		0.1 Si	180	590	1	1000
E	Temp #1	1.45	175	540	N/A	N/A
	Temp #2	1.45	175	590	N/A	N/A
	Temp #3	1.45	175	640	N/A	N/A

Table 2-1 Specifications for the SIMOX wafers used in this study. *Processing information regarding multiple-implant SIMOX wafers is proprietary and thus is not available.

2.4 Overview of SIMOX Buried-Oxide Section

This section is divided into four chapters. In Chapter 3, methods used for characterizing SIMOX buried oxide are discussed along with the advantages and disadvantages of each technique. In Chapter 4, the principal characteristics of standard single-implant SIMOX buried oxide are presented: BOX non-stoichiometry and silicon islands are identified as two key BOX defects. Existing knowledge on BOX non-stoichiometry defects is presented. The existing formation theory of SIMOX buried oxide is also discussed. An existing conduction model to explain the observed BOX electrical characteristics in terms of physical properties is presented. Based on this previous work and understanding, the specific BOX issues to be addressed by Chapter 5 and 6 are summarized in Section 4-4. In Chapter 5, BOX non-stoichiometry is examined in terms of the nature and origin of its defects, and its effect on BOX high-field conduction characteristics. In Chapter 6, BOX silicon islands are examined in terms of their formation mechanism, and their effect on BOX high-field conduction characteristics.

3. SIMOX Buried-Oxide Characterization Methodology

3.1 Overview

In this chapter, the main physical and electrical techniques used to characterize buried-oxide characteristics are described, including their theoretical description, sample preparation requirements, specific testing procedure, and relative advantages and disadvantages.

3.2 BOX Physical Characterization Methodology

3.2.1 Transmission Electron Microscopy (TEM)

Theoretical Background of Technique [16]

Transmission electron microscopy offers high magnification and resolution of a sample. The resolution of the TEM can be as high as 0.2 nm and the magnification can be up to 1,600,000X. In transmission electron microscopy, electrons are emitted from a fine tip of either tungsten or LaB_6. Electron emission is achieved either by heating (thermionic emission), applying a strong electric field at a cathode tip of radius $r < 1$ mm (Schottky emission), or by quantum-mechanical tunneling effects (field emission, FE). Thermionic emission is the usual source of electrons for electron-optical instruments.

The TEM image is produced by the differential loss of electrons from an incident beam as it passes through very thin-film samples. The degree of electron loss depends on the sample thickness, phase composition, crystal structure, and orientation of the sample. The contrast in a TEM image also depends on whether the sample material is crystalline or amorphous. In crystalline samples, the contrast is the result of changes in thickness, phase structure, or crystallographic orientation. In amorphous samples, the contrast is the result of differences in sample thickness or in chemical or phase composition.

There are two imaging modes: the bright-field mode (BF) and the dark-field mode (DF). In the bright-field mode, only the primary beam without scattered electrons is collected. The bright-field image will depend on the composition of the materials. In the dark-field mode, diffracted electrons without the primary beam are collected. The dark-field image gives a better resolution of crystallographic defects in crystalline materials.

Sample Preparation Procedure

Samples for cross-sectional TEM were prepared using the following steps. Four $0.5cm^2$ pieces of the sample to be examined were glued together with surfaces toward the center using Hardman epoxy. They were then ground by hand using 250 and 600 grade sand-papers perpendicular to the glued interface down to 200 μm. Then the sample was dimpled down to 10 μm. Before the last step of thinning, each sample was mounted on a ring, which acted as a sample holder. Finally, to reach the very thin dimensions of <0.1 μm, the sample was ion milled until yellow light could pass through the sample.

A JEOL - 200 CX microscope with either a tungsten or LaB_6 tip was used to characterize the SIMOX buried-oxide samples. A Hitachi high-resolution TEM was also used with help of Michael Frangello at the Center for Materials Science and Engineering.

Analysis of the Technique

The advantage of TEM is that it can accurately describe the microstructure of the buried oxide in terms of interface quality and silicon-island densities. However, TEM has several limitations as a metrology technique. The first limitation is in its range of scope. As the field of view is only in the micron range, TEM is not useful for characterizing wafer-level variation or even die-level variation of a process. Good faith must be exercised in assuming that the microstructure under TEM examination is the same throughout the wafer. The second limitation, which is more critical, is the long turn-around time required for analysis. Each cross-sectional TEM specimen takes 1 or 2 weeks to prepare manually, often in a very painstaking manner. If a company were to use TEM to calibrate its process, each lot would have to wait 2 weeks before receiving any TEM feedback.

3.2.2 Scanning Electron Microscopy (SEM)

Theoretical Background of Technique [17]

Development of the SEM technique started in the 1930s. Although the TEM technique had been developed earlier and had much better resolution, faster sample preparation and ease of image interpretation made the SEM method a much more widely used tool. In SEM, an electron gun produces a stream of electrons and accelerates them down a column. Magnetic lenses focus this stream into a small beam, which is rastered across the sample. Electrons that are emitted from the interactions of the incident beam with the sample are detected and displayed on a cathode-ray tube.

There are three different products of the electron/sample interactions that can be detected. The first is secondary electrons (SE) (emitted low-energy electrons with energy < 50 eV). They are produced near the material surface, since they do not have enough energy to escape from far below the surface (about 3 nm is the maximum depth). These electrons contain primarily surface information. SEM image contrast is produced by differences in the number of detected secondary electrons from the sample surface. Thus, surfaces facing the SEM detector appear light while surfaces facing away appear dark, making the data interpretation easy. This is the main mode of operation for characterizing SIMOX buried oxide. Two other products are back-scattered electrons and X-rays. Back-scattered electrons (BSE) have much higher energies than SE. Unlike SEs, the yield of BSEs is directly related to the average atomic number of the sample. Emitted X-rays have energies which are characteristic of the elements in the sample. By using X-ray analysis, the elemental nature of micron-sized materials in the sample can be identified.

Because SEM samples are bombarded with electrons, it is important that the sample be conductive and connected to ground. If it is not conductive, electron charge can build up on the sample, resulting in a deflection of the electron beam away from it. Usually, insulating samples such as oxide are coated with a thin layer of carbon or gold to make them conductive. For this study, a special environmental SEM (ESEM) was used so that no such coating was necessary. In the environmental SEM, there is a high water pressure (~ 5 torr) in the chamber. No coating is necessary because electrons can conduct away from the sample due to these water molecules, avoiding the build-up of electron charge. However, because water pressure makes the mean-free path of electrons much shorter than that of a conventional SEM, the sample stage must be located very near to the electron source and the detector.

Sample Preparation Procedure

The top-silicon layer was etched using a dry plasma etcher and the buried oxide was etched away using buffered-oxide etch (BOE 6:1 NH_4OH:HF by volume) for a very short duration. During the etching, silicon islands stuck to the top surface of the substrate while the oxide around them was etched away.[18, 19]

The ESEM at MIT Center for Materials Science and Engineering was used for this experiment. A beam energy of 30 keV was used and the typical magnification was 30,000X.

Analysis of the Technique

The advantage of the SEM technique is that it is much simpler than the TEM and its turn-around time is much shorter. However, the SEM range of scope is also limited,

though it is significantly larger than that for TEM. In addition, the SEM method also suffers from a slow laborious sample-preparation technique.

Although literature and experimental work has shown that etching SIMOX buried oxide in BOE preserves the silicon islands on the substrate, it is conceivable that not all of them may have stayed on the substrate. Thus, there might be error introduced in calculating the silicon-island density. Because of the error associated with having a certain number of the small silicon islands flow away due to the BOX etch, the silicon-island number that is evaluated using SEM measurements may not be meaningful in terms of an absolute number, but would be a good way of performing comparisons between two different samples.

3.2.3 Electron Spin Resonance (ESR)

Theoretical Background of Technique [20]

The electron spin resonance technique is based on two fundamental discoveries about atomic structure: first, an atom with a net electron magnetic moment can take up only discrete orientations in a magnetic field, and second, the electron magnetic moment is linked to the electron spin.

Electromagnetic radiation may be regarded as coupled electric and magnetic fields oscillating perpendicular to one another and to the direction of propagation. In most cases, the electric-field component interacts with molecules. Similarly, it is expected that a molecule containing a magnetic dipole will interact with the magnetic component of microwave radiation. When such a molecule is irradiated over a wide range of spectral frequencies, one normally finds no absorption attributable to a magnetic interaction. If,

however, the sample is placed in a static magnetic field, the absorption attributable to magnetic dipole transitions may occur at one or more characteristic frequencies. In the absence of a magnetic field, the absorption of radiation will occur only through an electronic transition, not a magnetic dipole transition. The resulting absorption spectrum will not give any information on magnetic characteristics of the sample. Resonant absorption of radiation in a static magnetic field is called "electron spin resonance." This effect has also been referred to as "paramagnetic resonance" and "electron paramagnetic resonance."

Sample Preparation Procedure

For ESR measurements, samples were cut into small pieces of size less than 1 cm^2. Removing the top silicon layer in KOH enhanced the ESR signal from the buried oxide. ESR measurements were performed at room temperature with an X-band (9.428 GHz) Bruker spectrometer at the University of New Mexico.

The defects in the buried oxide must be activated. This activation can be achieved by exposing the buried oxide to vacuum ultraviolet light (VUV). 20 hour VUV illumination is believed to be sufficient to "saturate" nearly all of the buried-oxide paramagnetic precursors.

Analysis of the Technique

The advantage of ESR is that it gives good insight into a material's micro-structure at the atomic-level. However, the ESR signal depends on the particular preparation technique used to activate the precursors that will respond to the magnetic field. The density and clarity of the signal will depend on the amount of time used for

saturating these precursors. In addition, just as with other physical characterization techniques, the ESR technique is destructive and can only measure a small area. So for metrology needs which require fast turn-around time and statistically meaningful amounts of data over the wafer-level, the ESR method is not adequate.

3.2.4 Etch-Rate Study

Theoretical Background of Technique

It is known that the silicon-dioxide etch rate is dependent upon the stoichiometry of the oxide.[21] The presence of excess silicon in the buried oxide decreases the etch rate. Correlation of the etch rate with the amount of excess silicon in an oxide has been shown. Thus, the etch rate of buried oxide can be used as a measure of the amount of excess silicon present in the buried oxide.

Sample Preparation Procedure

A BOX capacitor structure was utilized for measuring the etch rate. In this capacitor structure, silicon capacitor islands were located on top of the buried oxide. The initial height of the silicon capacitor with respect to the buried oxide was first measured using atomic-force microscopy. Then, after a controlled amount of etching of the buried oxide in BOE at a controlled room temperature, the final step-height of the silicon capacitors was then measured again. Measurements on many capacitors were carried out in order to increase the statistical trust-worthiness of the results.

Analysis of the Technique

Although a significant difference in etch rate may exist between different materials, the etch uniformity will be the key factor determining the relative success of

this method. In addition, this etch-rate technique is destructive. Also, as the etchant etches away at the buried oxide, the etchant concentration might undergo change, thus altering the observed etch rate. Thus, it is very important to keep the etchant concentration and temperature as constant as possible in order to get meaningful data. In addition, just as with the other physical characterization techniques described in this section, the etch rate can be only practically measured over a small area.

3.3 BOX Electrical Testing Methodology

3.3.1 Electrical Testing Procedure

The electrical properties of the BOX layers are very important. The BOX conduction characteristics can be obtained by applying a voltage across the buried oxide and measuring the resulting current through the buried oxide.

Testing Setup

All electrical measurements were performed in the Research Group Laboratories (RGL) of the MTL. Tests were performed in a dark, electrically-shield box. Wafers were baked in a convection oven prior to testing and a flow of nitrogen was maintained over the test devices in order to minimize moisture-induced surface current. The minimum current resolution of the measurement system was approximately 10fA. Bias from a Keithley high-voltage source measure unit (Keithley 237) was applied to the top gate of the BOXCAP while the substrate was kept grounded. The Keithley 237 was controlled from a computer using HTBasic programs. Figure 3-1 shows a schematic of this electrical testing setup.

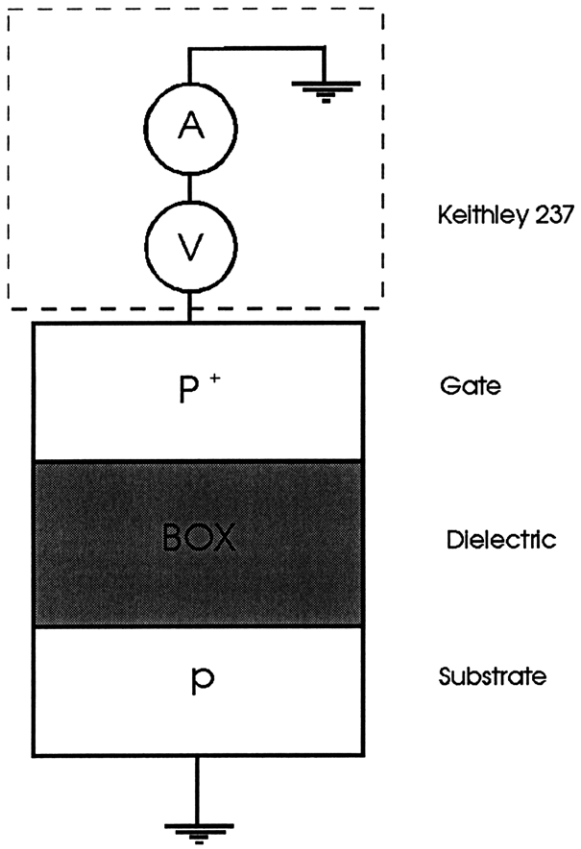


Figure 3-1 Schematic of electrical test set up for high-field conduction characteristics.

Ramp J-E Technique

The first technique for measuring the BOX conduction characteristics is the ramp J-E technique. For ramp J-E measurements, the BOXCAP voltage was step-ramped at 3V/3sec intervals until the BOX catastrophically broke down. At each voltage step, current through the buried oxide was measured. The total time required for constructing a J-E curve is about 300 seconds.

Static J-E Technique

In addition to the ramp J-E technique, the static J-E technique was developed and utilized to measure conduction characteristics. Although the ramp J-E technique provides

a fast turn-around measurement, it cannot decouple the electric-field and time dependence of the buried-oxide conduction characteristics.

Static J-E characteristics were obtained by first performing a series of constant E-field measurements ranging from E=0 until breakdown. These measurements were carried out on "virgin" capacitors in order to eliminate any stress-induced effects on the conduction characteristics. Then, these measurements were combined to construct composite J-E characteristics as shown in Figure 3-2. The main assumption is that each capacitor has similar BOX conduction characteristics as the others. Because of this assumption, the resulting J-E curve may have unwanted variation if the capacitors actually have different material properties.

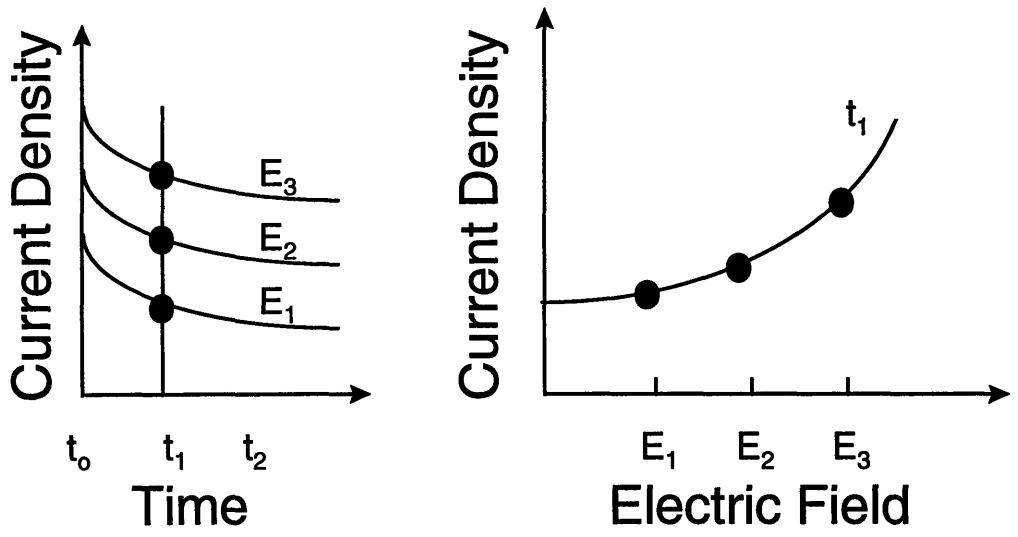


Figure 3-2 The static J-E methodology used to characterize SIMOX buried-oxide conduction characteristics. Constant electric-field data sets (current density vs. time) are replotted as isochronal curves (current density vs. electric field) in order to decouple the electric-field and time dependences.

3.3.2 Electrical Test-Structure Fabrication

Test Mask Design

The test devices used for the SIMOX BOX conduction study were simple MOS capacitors with the top silicon layer as the top gate, the buried oxide as the dielectric, and the substrate as the bottom gate. MOS capacitors were fabricated using a test mask such as shown in Figure 3-3. MOS capacitors with different sizes were used for measuring the high-field conduction characteristics. The size of capacitors was either $0.0025cm^2$ or $0.001\ cm^2$. The different size capacitors were used to check for BOX defects that could affect the conduction characteristics. Capacitors with different perimeters were also used

to check for the effects of edge-leakage current on the conduction characteristics. Guard-rings were also used to minimize the surface leakage current. Approximately 3,000 - 15,000 capacitors were fabricated on each 4-inch wafer.

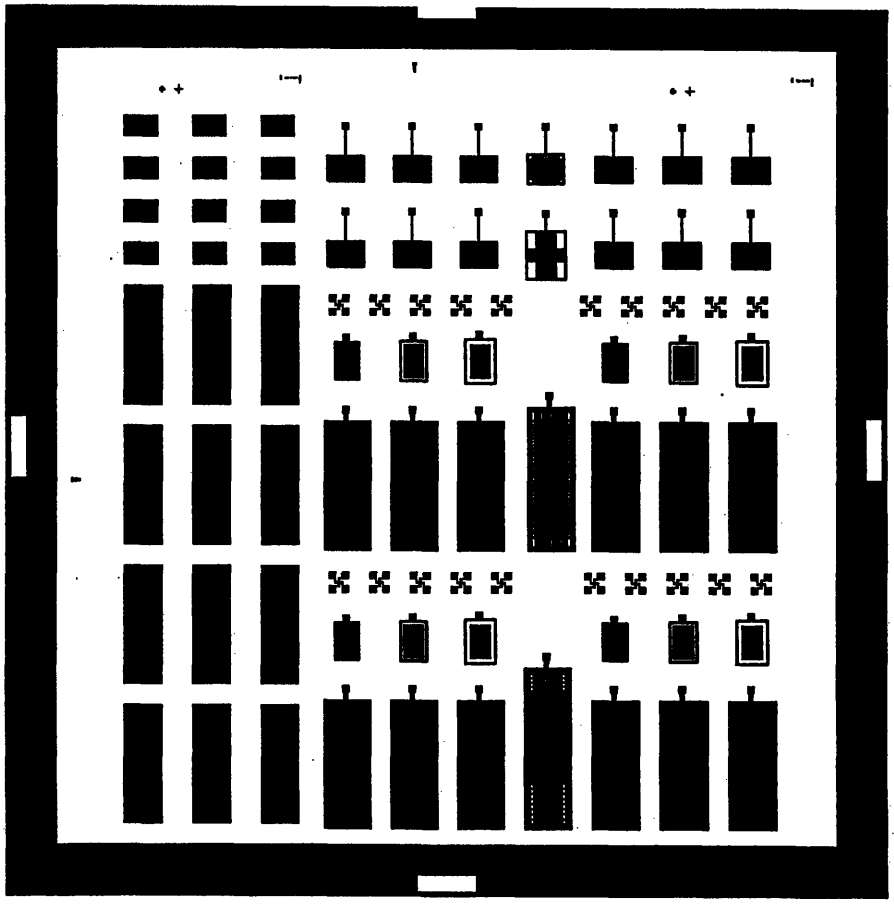


Figure 3-3 An example test mask for fabricating SIMOX buried-oxide capacitors. Note the various capacitor sizes and perimeter ratios used for detecting process-induced damage and macro-defect related conduction.

Fabrication of MOS Capacitors

Capacitors were fabricated in the Integrated Circuits Laboratory (ICL) and Technology Research Laboratories (TRL) of the MIT Microsystems technology Laboratories (MTL). A simple fabrication procedure was used to cut down on any process-induced defects in the buried oxide. In this short-flow process, BOX capacitors

(BOXCAP) were formed by degenerately doping the top-silicon layer using ion-implantation through a screening oxide, defining the capacitors using mesa isolation, and activating the dopants using a 950 °C nitrogen anneal. The dopants used were Phosphorus for n-type wafers and BF_2 for p-type wafers. Various doping and isolation methods were examined in order to insure a relatively "damage-free" process.

Analysis of the Technique

Compared to the physical characterization techniques, the electrical characterization technique has several advantages. By fabricating BOX capacitors across the entire wafer, a statistically meaningful amount of data can be obtained. This data then can be used to map out wafer-level variation. The key in adopting the electrical characterization technique for metrological purposes is in understanding the relationship between the BOX microstructure and observed BOX high-field conduction characteristics.

4. Present Understanding of SIMOX Buried Oxide

4.1 Standard Single-Implant SIMOX Buried-Oxide Characteristics

4.1.1 Physical Characteristics

BOX Island Characteristics

Using TEM, distinguishing features of the buried-oxide microstructure have been identified, one of which is the presence of silicon islands in the buried oxide (Figure 4-1). These islands are about 30 nm thick and 30 to 200 nm long, and are situated at an almost constant distance (25nm) from the bottom interface. These islands are crystalline with well-developed facets along the (001) and (111) planes. Most islands have the same orientation as the substrate, but there are islands which are off-axis by small number of degrees (Figure 4-2). The implantation temperature is known to affect the silicon islands. The crystal orientation of the silicon islands matches that of the substrate at a high substrate-implant temperature (485 °C) while the orientation becomes more random at a low substrate-implant temperature (280 °C).[22] In the case of standard single-implant SIMOX, silicon islands occupy about 2% of the total buried-oxide volume.[23]

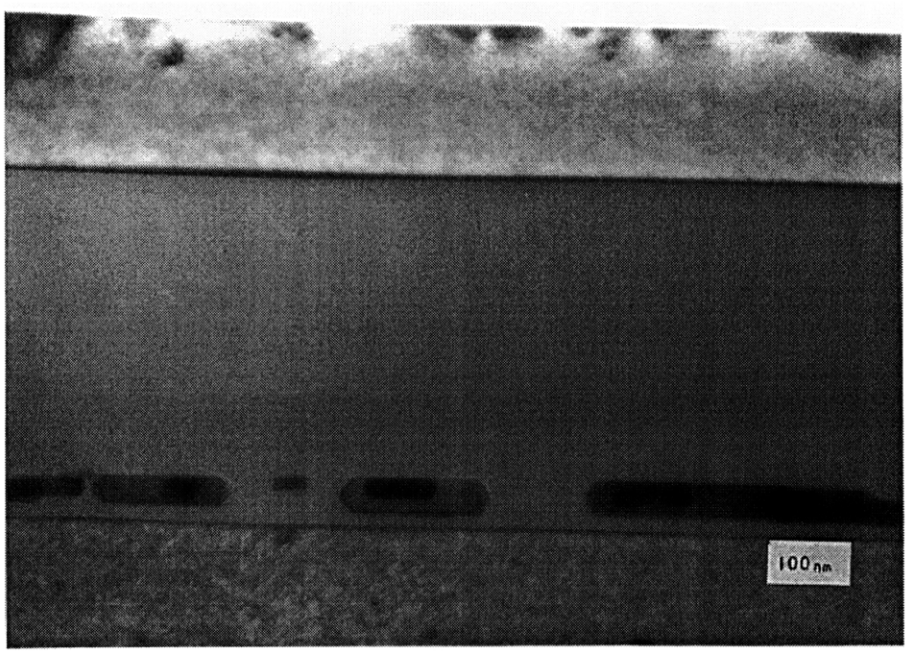


Figure 4-1 Cross-sectional view of standard single-implant SIMOX buried oxide. Note the size and the location of silicon islands which are located near the BOX/substrate interface. (Group A)

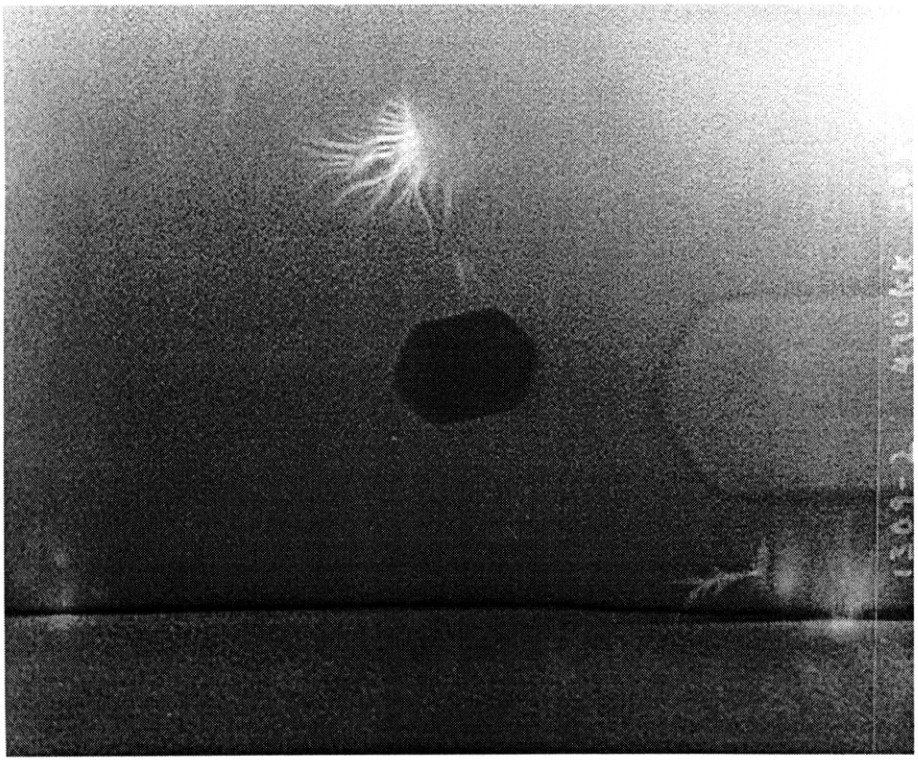


Figure 4-2 Close-up of a cross-sectional view of silicon islands in standard single-implant SIMOX buried oxide. Note the mismatch in orientation between the silicon island on the left with the one on the right. (Group A)

Non-Stoichiometry Characteristics

In addition to the presence of silicon islands, the SIMOX buried oxide is non-stoichiometric. A high density of oxygen vacancies in the form of the strained Si-Si bonds exists within the buried oxide.[24] The refractive index of the buried oxide is higher than that of fused silica indicating a strained SiO_2 structure.[25] Buried oxide is also known to have a slower etch rate than thermal oxide in HF, which indicates that the buried oxide contains excess silicon.[26] Spectroscopic ellipsometry (SE) studies have calculated that about 0.5 % of the SIMOX buried oxide is excess silicon above the stoichiometric level.[27] This SE value was calculated by correlating the optical SE response to the actual thickness of the buried oxide. Electroluminescene measurements also have indicated the presence of excess silicon in the buried oxide. Electroluminescence measurements indicate the presence of a 2.7 eV band. This band is thought to be due to an intrinsic defect related to oxygen vacancies, like neutral oxygen vacancy defects.[28]

4.1.2 Electrical Characteristics

General Conduction Characteristics

The conduction characteristics of SIMOX buried oxide can be divided into two regimes: a low-field conduction regime followed by a high-field conduction regime. The high-field conduction regime is defined as the sharply rising conduction regime shown in Figure 4-3. High-field rather than low-field conduction can be used as a basis for developing an electrical-based metrology technique because of its stronger response and easier data interpretation. For low-field conduction, many sources of error are possible and thus data collection is much more difficult. For example, at low-field measurement

conditions, humidity and surface leakage must be well controlled to collect meaningful data. Using high-field conduction characteristics, the measured data is much more representative of the material itself rather than that of the testing environment.

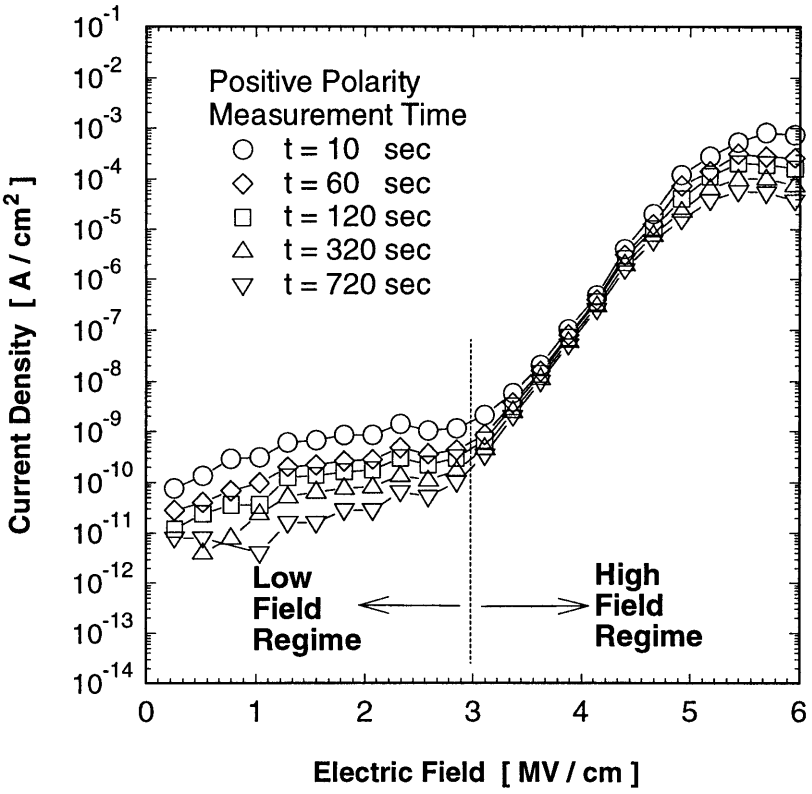


Figure 4-3 Static J-E characteristics of single-implant SIMOX buried oxide showing two distinct conduction regimes: a low-field regime and a sharply rising high-field regime. The onset for the high-field conduction regime depends strongly on the BOX formation recipe (implant and anneal conditions). Also note the different time-dependence of the conduction at low-field and high-field.

Time-Dependent Conduction

Single-implant SIMOX buried-oxide in the low-field regime displays time-dependence. No such corresponding time-dependence is observed for thermal oxide. This time-dependent effect makes use of the static J-E technique necessary. This time-

dependent conduction suggests the existence of traps inside the buried oxide which do not exist in thermal oxide.

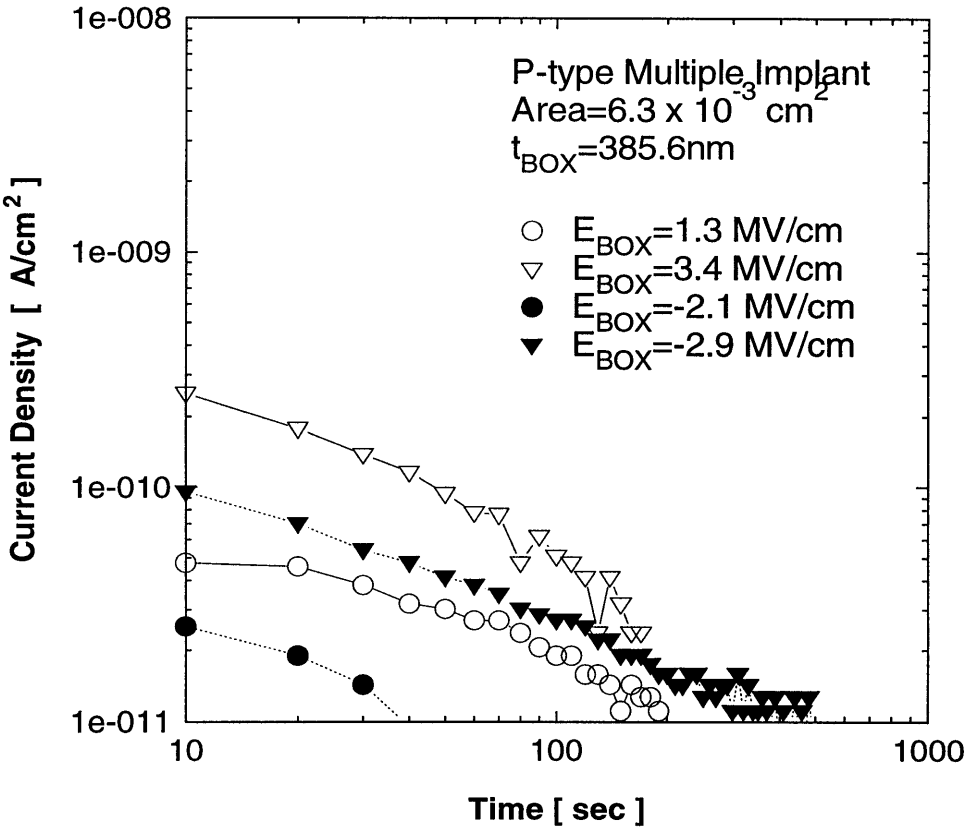


Figure 4-4 Time dependent conduction characteristics of SIMOX buried oxide.

Temperature Independence

The high-field conduction behavior of the SIMOX buried oxide is not dependent on the temperature (Figure 4-5). For both injection from the substrate and from the top-silicon layer, the current density stays relatively independent of the temperature from 29 °C to 250 °C. This result shows that the conduction mechanism is not a temperature-dependent trap-hopping mechanism, such as Frenkel-Poole conduction.[29]

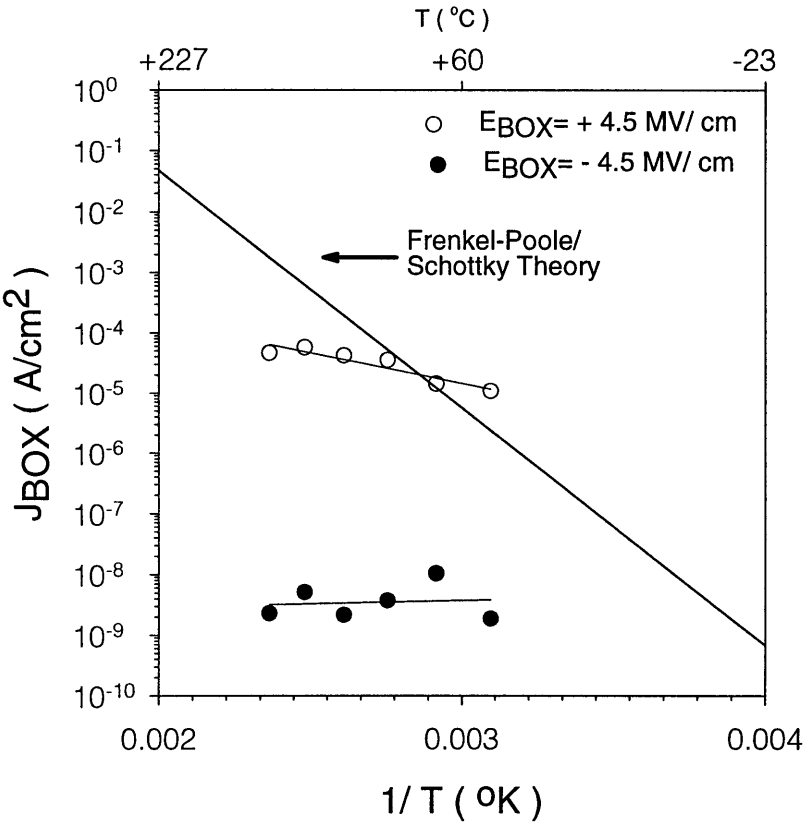


Figure 4-5 The weak temperature dependence of single-implant SIMOX buried-oxide high-field conduction characteristics indicates that high-field SIMOX buried-oxide conduction is not due to Frenkel-Poole or Schottky mechanisms. Similar temperature dependence is also observed for multiple- and supplemental- implant SIMOX wafers. (Group A)

Electric-Field Dependence

Figure 4-6 shows typical single-implant SIMOX BOX high-field conduction characteristics with a thermal oxide high-field conduction characteristic as a comparison. The tunneling regime of the SIMOX buried oxide has a lower onset electric field compared to the thermal oxide. In addition, the onset electric field for electron injection from the bottom SIMOX BOX interface is noticeably smaller than that for electron injection from the top SIMOX BOX interface. The onset for thermal-oxide high-field

conduction is about 6 MV/cm, whereas the onsets for the buried-oxide high-field conduction are 3 MV/cm and 4.5 MV/cm, for injection from the substrate and from the top-silicon layer respectively.

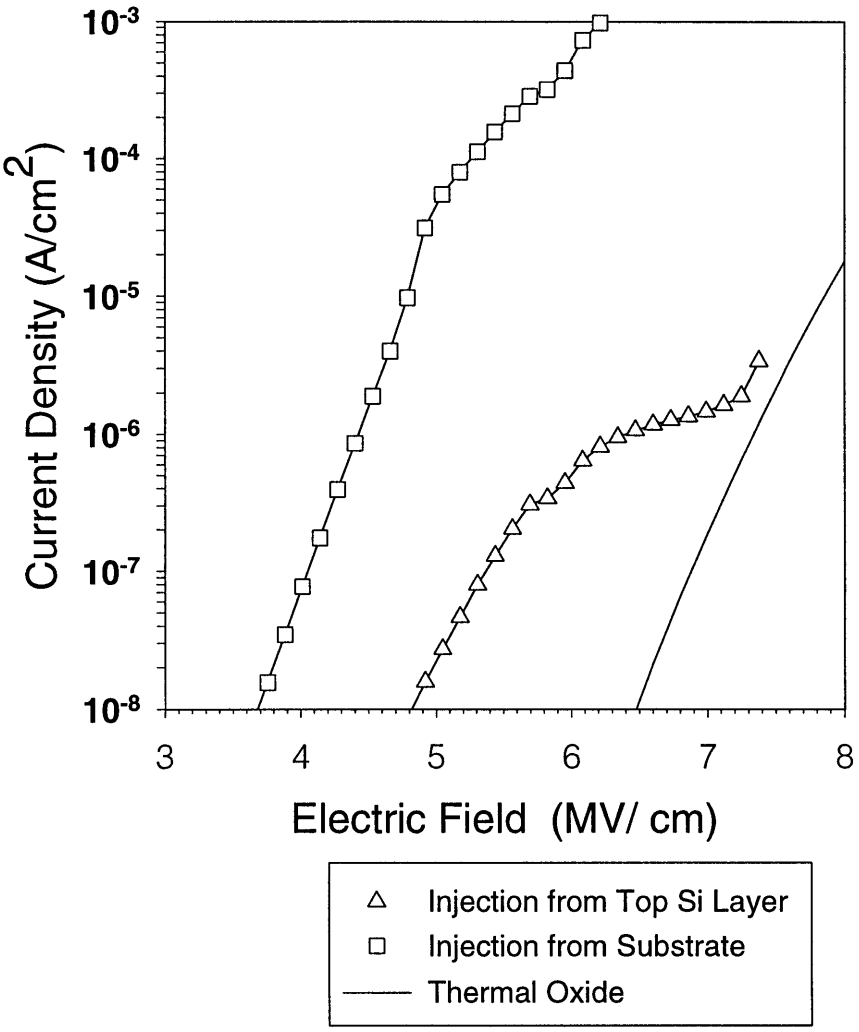


Figure 4-6 J-E characteristics of single-implant SIMOX for electron injection from the substrate and electron injection from the top-silicon layer. Note that the onset for the high-field conduction regime depends on the particular injection layer. The onset for injection from the substrate is lower than injection from the top-silicon layer.

4.2 Existing Understanding of BOX Non-Stoichiometric Defects

Previous research on excess-silicon related defects in the SIMOX buried oxide (using electron spin resonance and capacitance vs voltage methods) have identified three types of excess-silicon related defects in the SIMOX buried oxide.

The ESR studies by Devine *et al.*[30] and Conley *et al.*[31, 32] have shown the existence of Eγ' charged oxygen vacancies. They also showed that these defects can be created by either gamma irradiation or hole injection. The g value for this defect is 2.0005. Figure 4-7 a) shows the schematic illustration of this defect.

Recent ESR studies by Vanheusden and Stesmans[33] have demonstrated the existence of another paramagnetic defect in irradiated SIMOX wafers, which they attributed to a delocalized type of E' centers, termed the Eδ' center.[34] In their model, the delocalized spin of the Eδ' center is based on the existence of clusters of ~5 Si atoms in the buried oxide. They were further able to show that the Eδ' center is not associated with Cl or F, as first tentatively suggested by others working in bulk fused silica.[35] The Eδ' center is identified by its narrow (0.8G) and nearly symmetric line shape, and by its zero crossing g value of 2.0021. Figure 4-7 b) shows the schematic illustration of this defect.

In addition, W. L. Warren et al[36] have proposed the existence of D centers. They have proposed that these centers are amorphous silicon clusters with the g value of 2.0055. The schematic of this defect is shown in Figure 4-7 c).

Of these three excess-silicon related defects, the Eg' and Ed' centers have been widely accepted as defects present in SIMOX buried oxide. However, there has not been

universal agreement regarding the existence of amorphous silicon clusters, the D centers. J. F. Conley et al.[37] could not find any "amorphous silicon" signal in their ESR trace although the spectrometer was sent to optimize the sensitivity of its signal at g =2.0055. Thus, there is currently disagreement as to the existence of the D center defect in the buried oxide.

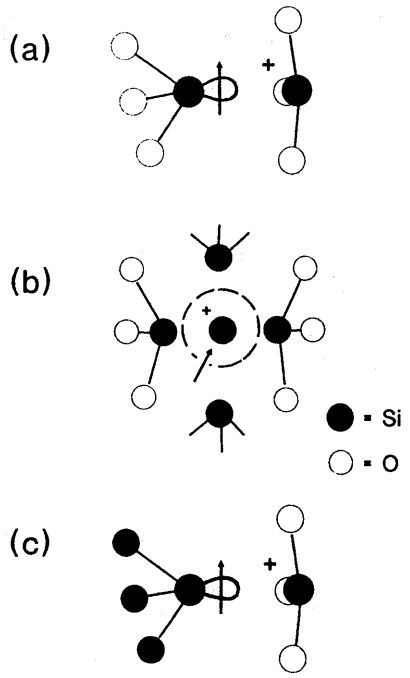


Figure 4-7 Schematic illustration of the oxygen vacancy defects: a) Eγ' center, b) Eδ' center, and c) amorphous silicon cluster, D center.

4.3 Existing Theory of SIMOX Buried-Oxide Formation

The formation of SIMOX buried oxide starts with the implantation of high-energy oxygen ions into silicon substrate. The implant energy determines the location of the peak in the oxygen concentration, and thus the final thickness of the top-silicon layer. The thickness of the buried oxide is determined by the total dose of oxygen ions. When oxygen ions are implanted into the silicon substrate, they initially do not form a

continuous buried-oxide layer. Rather, oxide precipitates form where the concentration of oxygen ions is above the saturation level in silicon. There are bigger oxide precipitates in the middle of the implantation range and smaller ones away from the peak. During the subsequent high-temperature anneal, these precipitates coalesce together to form a single continuous layer of buried oxide.

In growing thermal oxide, the conversion of silicon to oxide normally requires a 2.2-fold increase in volume. This can be accommodated by two mechanisms. One is volume expansion through the viscous flow of the oxide, and another is through the emission of Si atoms which become self-interstitials according to the following relation:

$$xSi + O_2 \rightarrow SiO_2 + (x-1)Si_i \qquad \textbf{Equation 4-1}$$

where Si_i is a silicon self-interstitial, x is the amount of silicon present for the reaction, and O_2 is an oxygen molecule present in the silicon network.

Theoretical and experimental studies on silicon self diffusion reveal that Si_i has a high formation energy and a very low migration energy. The sum of these two activation energies is about 5 eV.[38, 39] Under normal oxidation conditions, the second mechanism should be insignificant compared to the first because of its high activation energy. However, in the case of buried oxide, the conversion of silicon to oxide occurs primarily via the second mechanism because there is a volume constraint which restricts the viscous flow of the oxide. In addition, ion implantation creates numerous silicon vacancies and self-interstitials. [40]

The formation of buried oxide through self-interstitial emission presents an interesting situation. Completely strain-free oxide precipitation requires the emission of 0.63 interstitial Si atoms for each precipitate. Thus, in order for buried-oxide growth to

proceed, there has to be an out-diffusion of silicon interstitials away from the reaction site. Otherwise, self-interstitial super-saturation would build up a chemical potential which would eventually oppose the oxidation reaction. However, the diffusivity of silicon in oxide is very low ($3.3x10^{-17}$ cm^{-2}/s at 1300 °C), which is eight orders of magnitude lower than the diffusivity of oxygen in oxide. This low silicon interstitial diffusivity and the buried-oxide growth through silicon self-interstitial generation have been suggested as the primary causes for the resulting BOX physical characteristics.

The formation of the buried oxide by Si_i migration is supported by numerous other experimental evidence:

1) The SiO_2 precipitates, which form during implantation, are almost free of strain.[41]
2) Buried oxide can form even at liquid nitrogen temperatures due to the very low migration energy of the silicon interstitials. [42]
3) Multiple implantation and annealing results in a high quality non-stochiometric, island-free buried oxide because this particular process prevents the piling up of oxide precipitates which block the silicon-interstitial migration to the surface.[43]
4) Implantation through a screen oxide blocks the migration of Si_i to the surface, thus building up a supersaturation of Si_i towards the top interface. This causes the oxidation reaction to proceed toward the bottom interface and eliminates silicon islands which are typically formed in this area.[44]

4.4 Existing Buried-Oxide High-Field Conduction Model

4.4.1 Fowler-Nordheim Tunneling

Fowler-Nordheim Tunneling

The temperature independence of the observed high-field conduction suggests that it is most likely due to Fowler-Nordheim tunneling rather than Frenkel-Poole emission. Fowler-Nordheim tunneling is an oxide barrier narrowing effect[45] whereas Frenkel-Poole emission is a trap-assisted conduction mechanism which is dominant in insulators such as silicon nitride. The observed SIMOX BOX conduction temperature dependence is much weaker than what is predicted for Frenkel-Poole mechanism.

Fowler-Nordheim tunneling occurs in a dielectric under high electric-field bias. If the applied electric field across the buried oxide is large enough, the rectangular barrier formed by the oxide layer becomes a triangular barrier (Figure 4-8). When the barrier becomes triangular the tunneling distance becomes shorter, enabling electrons to tunnel through. Lowering the barrier height or changing its shape may increase the tunneling efficiency by changing the effective tunneling distance for electrons. In addition, if there is localized cathode E-field enhancement, electrons may tunnel through the oxide at a much lower applied electric field.

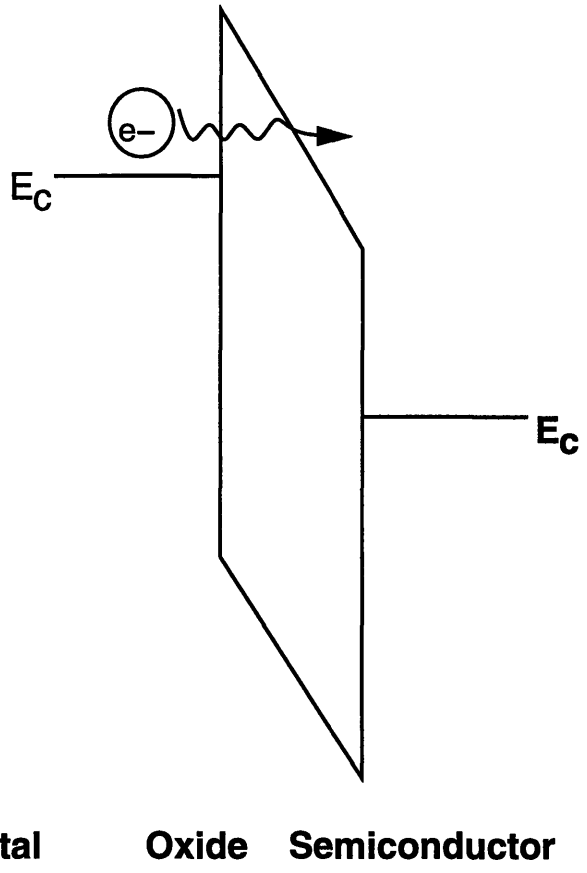


Figure 4-8 Fowler-Nordheim tunneling: electrons "tunnel" across the oxide when the energy barrier is thin enough.

Fowler-Nordheim Equation

The governing equation for the Fowler-Nordheim tunneling theory is as follows. The current density, J, is given in terms of the applied macroscopic electric field, E, as

$$J = AE^2 e^{-\frac{B}{E}} \qquad \textbf{Equation 4-2}$$

$$A = \frac{q^3 m_t^*}{8\pi h m_{ox}^* q\phi_B} \frac{c\pi}{\sin c\pi} \qquad \textbf{Equation 4-3}$$

$$B = \frac{4\sqrt{2m_{ox}}}{3hq}[q\phi_B]^{\frac{3}{2}} \qquad \textbf{Equation 4-4}$$

$$\frac{c\pi}{\sin c\pi} = \text{weak function of temperature} \qquad \textbf{Equation 4-5}$$

where q is charge of an electron, ϕ_B is the barrier height, m is mass of an electron, and h is Planck's constant. The exponential term in Equation 4-1 comes from the WKB approximation.[46] According to this first-order model, C is the only term with any noticeable temperature dependence, and it is a very weak dependence. Therefore, the term sin c/c becomes approximately unity and consequently J becomes effectively temperature independent for most temperatures of interest. The parameter A is inversely proportional to the barrier height, Φ_b. The parameter B is proportional to $\Phi_b^{3/2}$. The barrier height, Φ_b, has a theoretical value of 3.2 eV for thermal oxide. The theoretical values for A and B are $3x10^6$ [A/MV^2] and 240 [MV/cm] respectively.

4.4.2 Injection from the Top BOX Interface

One-Step Mechanism

Electron injection from the top interface may be described by a one-step mechanism with the effective barrier height being lowered due to oxide non-stoichiometry (Figure 4-9). Research in silicon-rich oxide has shown that as the silicon content in oxide is increased, the onset electric field for tunneling is lowered.[47] Silicon implantation into thermal oxide has also yielded oxide in which electrons could tunnel through at a lower electric field.[48]

Excess silicon in the buried oxide also lowers the barrier height for tunneling. Barrier lowering is due to the excess silicon in the buried oxide which acts as hopping centers for electrons to tunnel from one trap to another. This "electron hopping" mechanism causes the energy band of the oxide to appear lower than normal, which translates into an earlier onset for tunneling.[49]

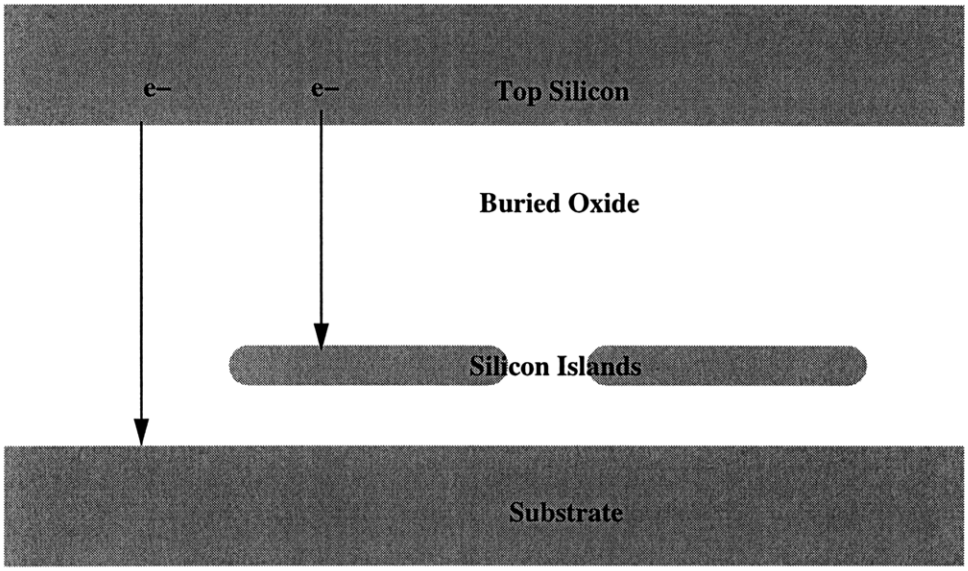


Figure 4-9 Schematic of the conduction mechanism for SIMOX buried-oxide top-silicon cathode injection. Top-silicon cathode conduction is due to Fowler-Nordheim tunneling with increased tunneling efficiency due to the non-stoichiometric nature of the SIMOX buried oxide (the buried oxide contains excess silicon).

4.4.3 Injection from the Bottom BOX Interface

Two-Step Mechanism

Electron injection from the substrate/bottom interface can be described using a two-step Fowler-Nordheim tunneling model with cathode electric-field enhancement (Figure 4-10). In this model, electrons first tunnel to the silicon islands at low electric fields, and then are injected across the oxide from the silicon islands. Due to the shape of the silicon islands, there is electric-field enhancement at the edges of the silicon islands.

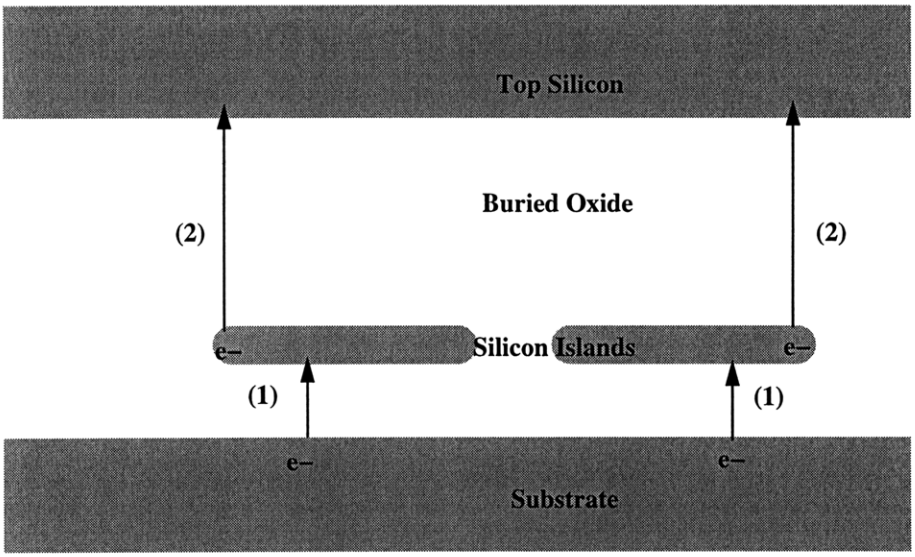


Figure 4-10 Schematic of the conduction mechanism for SIMOX buried oxide substrate-cathode injection. Substrate-cathode conduction is due to electric-field enhancement at the edges of the silicon islands.

2-D electro-static simulations have been performed to examine the effect of the silicon islands on the surrounding electric field. In this set of simulations, the focus was on examining the effect of the silicon island shape, size, and location, rather than on the charge state of the island or the electrodes. Therefore, two assumptions were made. The first assumption was that the top-silicon layer and the substrate were degenerately doped. Therefore, depletion effects in the electrodes could be ignored. Since the buried-oxide is relatively thick, compared to any depletion region, this is likely to be a good assumption. The second assumption was that the silicon island is neutral and degenerately doped. This allows the silicon island to be treated as an equipotential surface with a large supply of electrons.

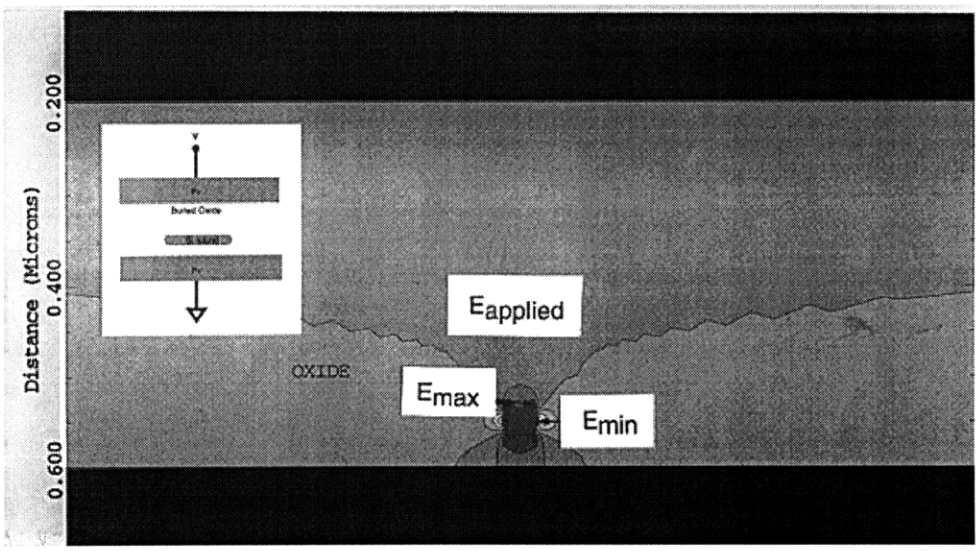


Figure 4-11 2-D electro-static simulation of the impact of a silicon island placed near the bottom of a buried-oxide layer. Constant E-field lines show that significant E-field enhancement occurs at the edges of the silicon islands.

The 2-D simulation, as illustrated in Figure 4-11, shows that there is appreciable electric-field enhancement at the edges of a BOX silicon island. The simulation program on Medicci is shown in Appendix B. and the program Towards the top interface, there is almost no enhancement of the electric field. Thus, it can be assumed that E-field enhancement becomes a factor only for injection from the bottom interface.

The magnitude of the maximum E-field enhancement factor depends on the thickness of the particular silicon island, as well as the distance from the injecting surface of the silicon island to the corresponding anode interface. In Figure 4-12, the parameter α is defined as the distance between the injecting point on the island surface and the anode interface, and the parameter β is defined as the distance between the middle of the island and the anode interface. The ratio α/β is a normalized quantity which accounts for the silicon island thickness and its distance from the anode interface. Figure 4-12 displays the simulated E-field enhancement due to the silicon island as a function of the parameter

α/β. In a typical single-implant SIMOX buried oxide, where the silicon islands are near the back BOX interface, the typical α/β value is approximately 0.9, where the E-field enhancement factor is approximately 1.44X.

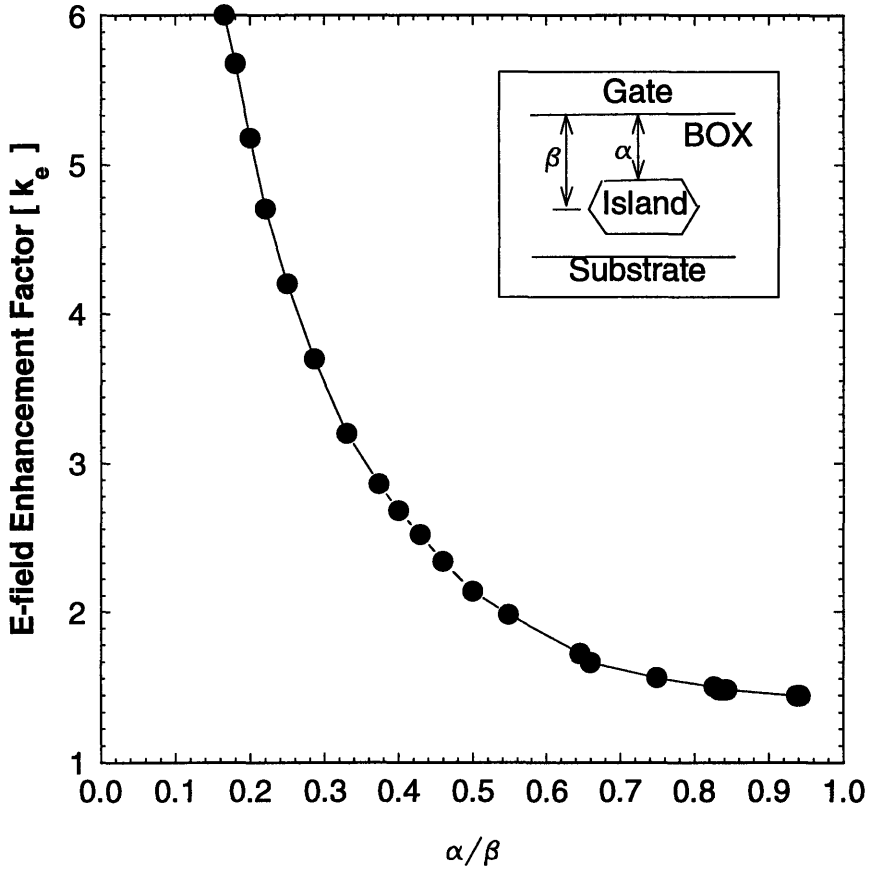


Figure 4-12 The E-field enhancement factor, ke, plotted as a function of the normalized island geometry factor, α/β, which accounts for the silicon-island location and size. For single-implant SIMOX, α/β is about 0.9. As the relative silicon-island size increases and/or the silicon island size approaches the top interface, the electric-field enhancement factor increases dramatically.

4.4.4 Modified Fowler-Nordheim Tunneling Equation

Based on this qualitative understanding of BOX high-field conduction, a quantitative model has been developed which incorporates the important physical phenomena discussed in the previous sections, specifically the electric-field enhancement

at silicon islands and barrier height changes due to oxide non-stoichiometry. In the case of electric-field enhancement, the exact amount of enhancement will depend on the shape and the density of the silicon islands. In the case of a changing barrier-height, the effective tunneling barrier-height will be determined by the amount and distribution of the excess silicon inside the buried oxide.

The parameter for electric-field enhancement at the silicon islands is defined as k_e. The effective area of electric-field enhancement and electron injection is defined as k_a. Changes in the barrier height due to the excess silicon within the buried oxide is incorporated into a modified value of Φ_b. Modifying the Fowler-Nordheim tunneling equation yields

$$J = k_a\left[\frac{A_o}{\phi_B}\right](k_e E_o)^2 \exp\left(\frac{-B_o\phi_B^{\frac{3}{2}}}{k_e E_o}\right) \qquad \textbf{Equation 4-6}$$

$$E_o = \frac{V_{BOX}}{t_{BOX}}\left[\frac{MV}{cm}\right] \qquad \textbf{Equation 4-7}$$

where E_o is the applied macroscopic electric field.

Parameter Extraction

The conduction model can be used to extract meaningful physical parameters that are related to the silicon-island density. The F-N equation can be converted into a log-log plot in order to extract the physical parameters, k_a and k_e. Equation 4-5 can be re-written as

$$\ln\left(\frac{J}{E^2}\right) = -\left(\frac{B}{E}\right) + \ln(A) \qquad \textbf{Equation 4-8}$$

$$A = \frac{k_a A_o k_e^2}{\phi_B} \qquad \textbf{Equation 4-9}$$

$$B = \frac{B_o(\phi_B)^{\frac{3}{2}}}{k_e}$$ **Equation 4-10**

Figure 4-13 shows a graphical conversion of the F-N equation. Here, B is the slope and ln(A) is the intercept of the straight fitted line. By using the least-square linear approximation, the best linear-fit through the data can be found. From the fitted line, both the slope and intercept can be obtained. By using the appropriate value of k_e from 2-D electro-static simulations and the thermal oxide value for the barrier height, the injection area, k_a, can be extracted.

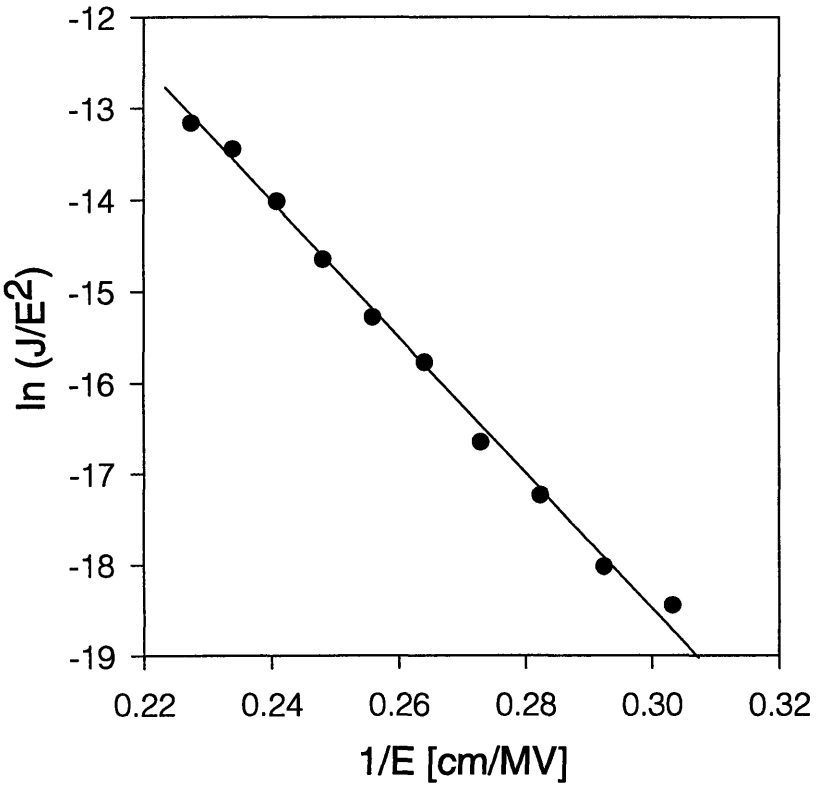


Figure 4-13 Fowler-Nordheim correlation plot used for model parameter extraction. The silicon-island density can be inferred by extracting the y intercept from this graph.

4.5 Problem Statement

Using the BOX high-field conduction model for any metrological purposes will depend on answering the following questions concerning standard single-implant SIMOX buried oxide. This thesis addresses these problems in order to provide greater fundamental understanding of the buried-oxide structure and its electrical conduction characteristics.

4.5.1 BOX Non-Stoichiometry

The first issue to be addressed concerns the nature of excess-silicon related defects. Based on ESR studies, three types of excess-Si related defects have been proposed: oxygen vacancy centers, amorphous delocalized cluster of silicon atoms, and silicon dangling bonds.[50] However, there has been uncertainty regarding the existence of amorphous silicon clusters in the buried oxide. In this thesis, these defects are artificially generated through implantation, and their presence and properties in the buried oxide are characterized.

The second issue to be addressed is the origin of these excess-Si related defects, which are not normally present in the thermal oxide. The existing formation theory of SIMOX buried oxide, described in the previous section, does not describe how these defects could have originated. In this thesis, a kinetic model is developed to describe the origin and distribution of the excess-silicon-related defects.

The third issue to be addressed is the impact of the excess-silicon related defects on SIMOX BOX high-field conduction characteristics. The existing conduction model is

not clear about the detailed changes taking place in the height and shape of the barrier height for Fowler-Nordheim tunneling. In this thesis, a quantum-mechanical-based model is developed to address this issue.

4.5.2 BOX Silicon Islands

The first issue concerns the formation theory of SIMOX buried oxide. The existing formation theory of buried oxide, described in the previous section, does not explain the shape and distribution of silicon islands that occur in standard single-implant buried oxide. The questions exists as to whether the silicon islands are just a manifestation of silicon nucleation and growth, or are they due to some other mechanism. Unless a plausible SIMOX BOX island formation model is developed, improvement in the SIMOX buried-oxide quality and reduction in the BOX silicon-island density will come about only through trial and error, rather than through scientific understanding and prediction. In this thesis, silicon islands are artificially created by implanting silicon into the buried oxide and their shape and distribution are studied to provide insight about existing SIMOX BOX silicon islands. A model based on silicon self-interstitial generation and two different precipitation mechanisms is developed to explain the origin and distribution of SIMOX BOX silicon islands.

The second issue to be addressed is the impact that these silicon islands have on the high-field conduction characteristics. The proposed conduction model is not clear about whether the BOX silicon islands are the main reason for the early onset of the high-field tunneling regime for substrate electron injection or whether BOX non-stoichiometry

also has a comparable impact. In this thesis, the conduction characteristics of different materials are characterized in order to ascertain the answer to this question.

5. SIMOX BOX Non-Stoichiometry

5.1 Nature of Defects

From a thermodynamic point of view, the existence of amorphous silicon clusters after a high temperature (>1300 °C) anneal does not seem likely. In order to confirm the stability and existence of these amorphous silicon clusters, amorphous silicon clusters were artificially created by implanting silicon into single standard SIMOX buried oxide at doses ranging from $1x10^{16}/cm^2$ to $1x10^{17}/cm^2$ followed by anneals at either 1000 °C and 1300 °C for one hour. These Group D samples were then examined for the existence of any excess-silicon related defects. Figure 5-1 shows the ESR result from supplemental silicon-implanted single-implant SIMOX buried oxide that had been annealed at 1000 °C. The curve represents the first-derivative of the absorption spectrum. The absorption band shows the transition for amorphous silicon clusters. This trace was not present in ESR measurements of the sample annealed at 1300 °C. ESR traces corresponding to these so called "amorphous silicon clusters" were found only in samples annealed at 1000 °C and not in samples annealed at 1300 °C. This result shows that it is very unlikely that amorphous silicon clusters could exist in standard single-implant SIMOX buried oxide due to the high temperature anneal it undergoes during normal processing.

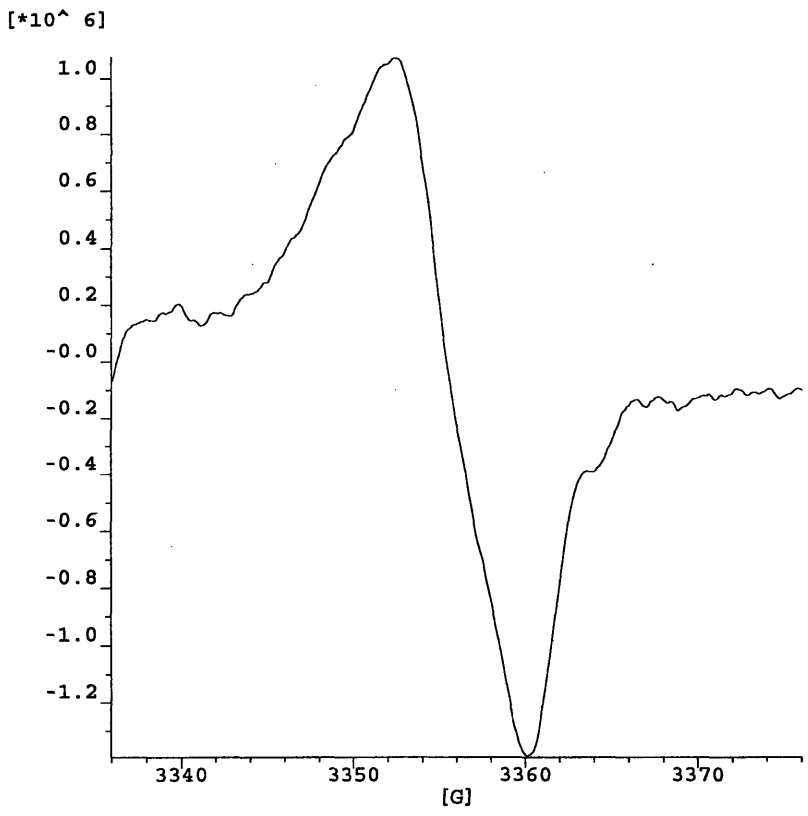


Figure 5-1 ESR spectrum of single-implant SIMOX buried oxide with supplemental silicon implantation and 1000 °C anneal. (Group D)

5.2 Kinetic Model for Formation of Defects

A new kinetic formation model based on the out-diffusion of oxygen is proposed to explain the formation of excess-silicon related defects in the SIMOX buried oxide. The existing SIMOX BOX formation model presented in Section 4.3 does not account for the existence of these defects. From depth-profiling studies of defects in the buried oxide using ESR and etching in HF, it has been shown that there is an increased amount of excess silicon towards the top-Si/BOX interface and an even greater amount of excess silicon towards the BOX/substrate interface.[51] In addition, the existence of oxygen interstitials in silicon layer of poly Si/ oxide/ Si substrate structures after high-

temperature anneal has been shown through infrared absorption studies by R. A. Devine, et al.[52] They proposed oxygen out-diffusion from the oxide into the silicon layer as the defect-generation mechanism. The kinetic model being developed here for SIMOX buried oxide (based on R. A. Devine, et al.'s model) explains the increasing density of the excess-silicon defects towards the interface between the buried oxide and the top-silicon layer and the higher density of these defects in the interface between the buried oxide and the silicon substrate.

The existence of oxygen-vacancy related defects can be understood as the result of oxygen out-diffusion during the high-temperature SIMOX formation anneal. The generation of defects in the region near the top Si/BOX interface can be modeled by a pair of semi-infinite solids joined together. If one assumes that there are no oxygen interstitials in the top-silicon layer, a kinetic model can be set up. We can then use Fick's equation for O diffusion to yield the profile of O interstitials in the top-silicon film, which will be mirrored somewhat by the profile of oxygen vacancies in the buried oxide.

The oxygen-vacancy defects in the region near the top silicon/BOX interface can be modeled as a pair of semi-infinite solids. For the following derivation, all diffusion coefficients refer to the different diffusion coefficients of oxygen (e.g., D_{ox} will mean diffusivity of oxygen in oxide, D_{si} the diffusivity of oxygen in silicon). The concentration of oxygen in the top-silicon layer can be modeled as

$$[O]_{Si} = k[O]^*_{SiO_2} erfc(x / 2\sqrt{D_{Si}t}) \qquad \textbf{Equation 5-1}$$

where $k[O]^*_{SiO_2} = [O]^*_{Si}$ is the solubility limit of O interstitials in Si for the anneal temperature, $[O]^*_{Si}$ refers to the solubility limit of oxygen in silicon, k is the segregation

coefficient, $[O]^*_{SiO_2}$ is the concentration of O in the oxide adjacent to the interface (~ $5x10^{22}$ cm^{-3}), D_{si} is the diffusion coefficient for O interstitials in Si. The latter is given by[53]

$$D_{Si} = 0.17\exp(-2.54eV / kT)cm^{-3} \qquad \textbf{Equation 5-2}$$

From the solution of Fick's equation, we calculate the O profile in the oxide as

$$[O]_{SiO_2} = [O]^*_{SiO_2}[1 - k\sqrt{D_{Si}} / (\sqrt{D_{Ox}} + k\sqrt{D_{Si}})erfc(-x / 2\sqrt{D_{Ox}t})] \qquad \textbf{Equation 5-3}$$

where D_{Ox} is the network oxygen diffusion coefficient given by[54]

$$D_{Ox} = 2.6\exp(-4.7eV / kT)cm^2 s^{-1} \qquad \textbf{Equation 5-4}$$

The oxygen-vacancy profile is then given by the difference $[O]^*_{SiO_2} - [O]_{SiO_2} = [V]_{Ox}$. From Equation 5-1, noting that $[O]^*_{SiO_2} = 5x10^{22} cm^{-3}$, we can estimate that for the anneal temperature of 1320 °C, k ~ 1.7 x 10-5. In this case, $k\sqrt{D_{Si}}$ is approximately two orders of magnitude smaller than $\sqrt{D_{Ox}}$ so that we obtain

$$[V]_{Ox} = [O]^*_{Si}(\sqrt{D_{Si}} / \sqrt{D_{Ox}})erfc(-x / 2\sqrt{D_{Ox}t}) \qquad \textbf{Equation 5-5}$$

The oxygen-vacancy defect concentration at the top BOX interface based on this model is approximately on the order of $8x10^{17}$ cm^{-3}. This concentration decreases towards the bulk of the buried oxide. The oxygen-vacancy defect concentration estimated from ESR measurements on single-implant SIMOX buried oxide is approximately $1x10^{18}$ cm^{-3}.[55] Thus, the model appears to provide a reasonable prediction.

The increased amount of oxygen vacancies in the region towards the BOX/substrate interface can be understood by understanding the key role played by the

BOX silicon islands. Figure 5-2 illustrates the role that the BOX silicon islands play. The BOX silicon islands act as another sink for oxygen out-diffusion from the buried oxide. For the annealing temperature of 1300 °C, D_{Si} is calculated to be 7 x 10^{-9} cm^2 s^{-1}, whereas D_{Ox} is 8.84 x 10^{-16} $cm^2 s^{-1}$. If the time for oxygen out-diffusion from the buried oxide is estimated to be one hour, $\sqrt{D_{Ox}t}$ is 29 nm and $\sqrt{D_{Si}t}$ is 20 μm. As silicon islands are about 20 nm thick, the oxygen interstitial concentration in the silicon islands will achieve a steady-state concentration very quickly so that oxygen out-diffusion from the bulk of the oxide to the silicon islands will be limited.

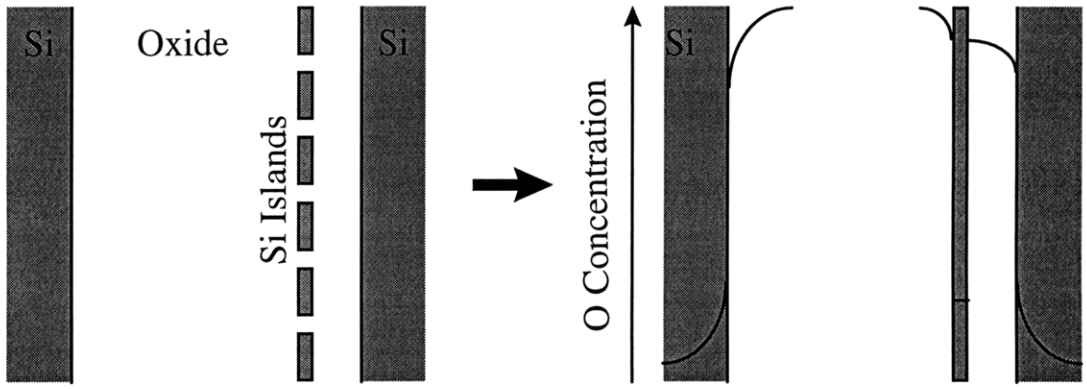


Figure 5-2 Schematic describing the out-diffusion of oxygen from the buried oxide to the top-silicon layer and the substrate. The out-diffusion of oxygen from oxide between the silicon islands and the substrate can be estimated using a thin-film solution model. It results in a higher concentration of oxygen vacancy defects in that particular oxide region compared to the region near the top-silicon layer.

5.3 Modified High-Field Conduction Model

Interface Roughness

The proposed BOX high-field conduction model for electron injection from the top-silicon layer suggests that excess silicon-related defects in the buried oxide are likely responsible for the early onset of high-field tunneling regime. However, another proposed

cause for this early onset of high-field conduction is interface roughness.[56] It has been argued that asperities at the top silicon/BOX cathode injection interface can produce field-enhancement effects at these points. However, there appears to be no observed correlation between interface roughness and the high-field conduction characteristics as shown in Figure 5-3.

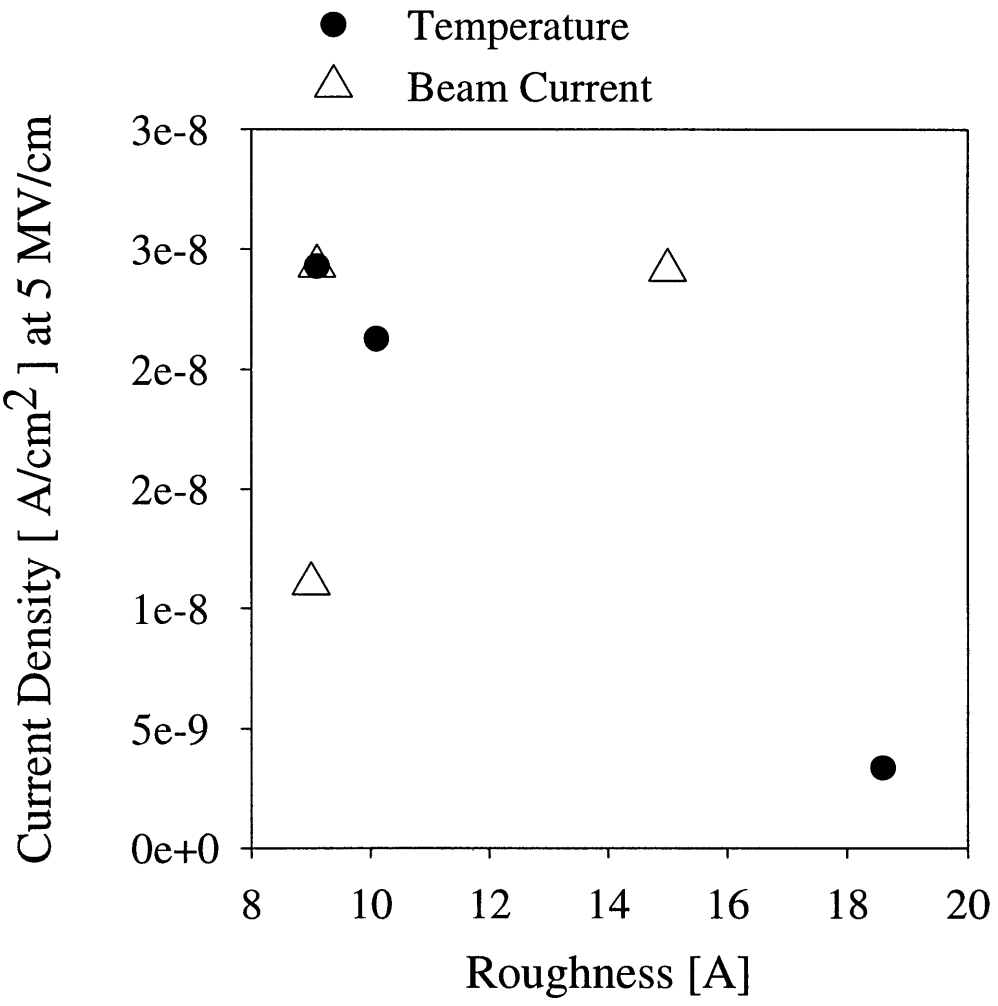


Figure 5-3 Correlation of interface roughness and BOX high-field conduction. Current density at E=5MV/cm2 is plotted against the top-silicon/BOX interface roughness, which was measured by atomic force microscopy after the top-silicon layer had been etched away in HF. (Group E)

Multiple-Implant SIMOX Wafers

Other experiments have been carried out to show that BOX non-stoichiometry is primarily responsible for the observed BOX high-field conduction characteristics. Multiple-implant SIMOX buried oxide, which is known to be stoichiometric, shows electrical characteristics that are similar to thermally grown oxide as shown in Figure 5-4. This comparison between single- and multiple- implant material (from two different source) provides added evidence that the excess-silicon related defects are responsible for the early onset of the BOX high-field tunneling regime from the top BOX interface.

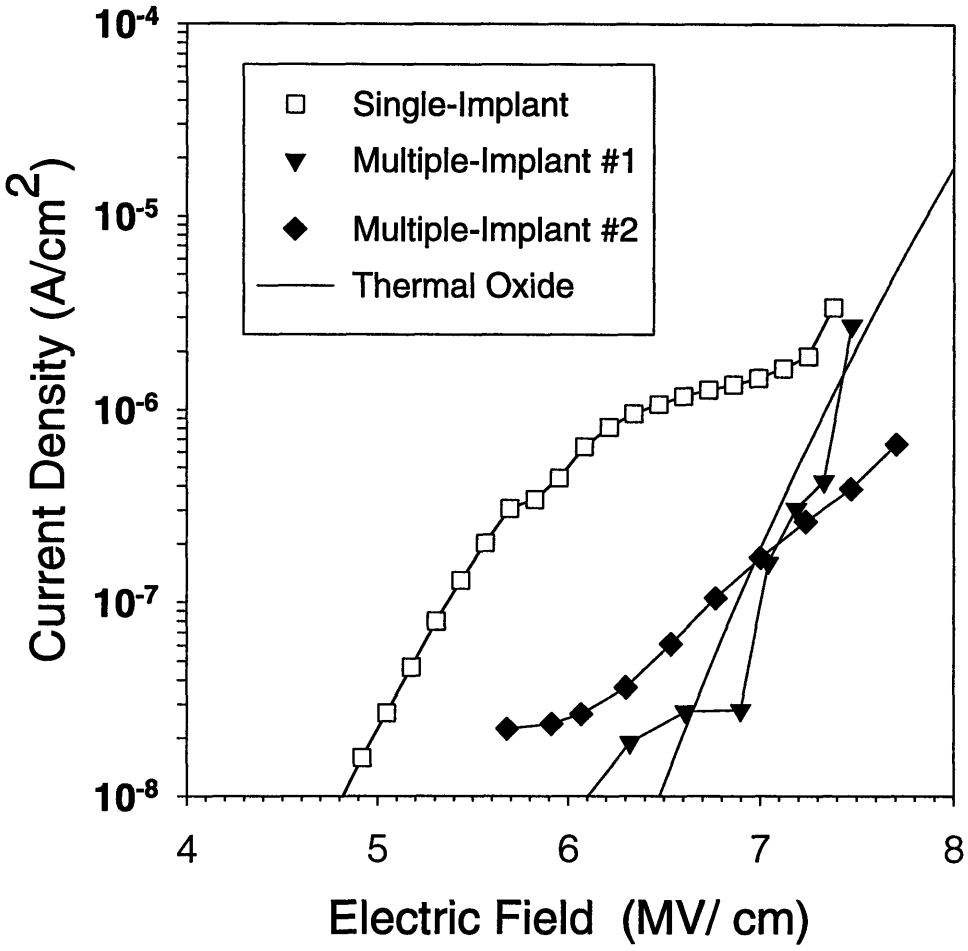


Figure 5-4 Comparison between static J-E characteristics of different multiple-implant SIMOX buried oxides and standard single-implant SIMOX buried oxide. The high-field conduction characteristics of multiple-implant SIMOX wafers resemble the theoretical thermal-oxide characteristics. (Group B)

Supplemental-Oxygen Implantation

Supplemental-oxygen implantation into the buried oxide can return the BOX electrical characteristics back to those of thermally-grown oxide as shown in Figure 5-5. In this thesis, supplemental oxygen implantation is shown to reduce excess-silicon related defects.[57, 58] Low doses of supplemental-oxygen implantation were observed not to make any difference in the conduction characteristics, until the supplemental-oxygen dose was over $1x10^{17}$ /cm^2. Since the total amount of oxygen implanted during the buried-oxide formation itself is about $1.5x10^{18}$ /cm^2, the minimum supplemental-oxygen dose required to return the tunneling characteristics back to those of thermal oxide is at least 7 % of the total dose. Spectroscopic ellipsometry measurements had suggested an excess silicon value of around 5 %.[59] How excess silicon-related defects contribute to the high-field conduction characteristics will be explained later in the chapter using a quantum-mechanical model of the barrier shape and tunneling mechanism.

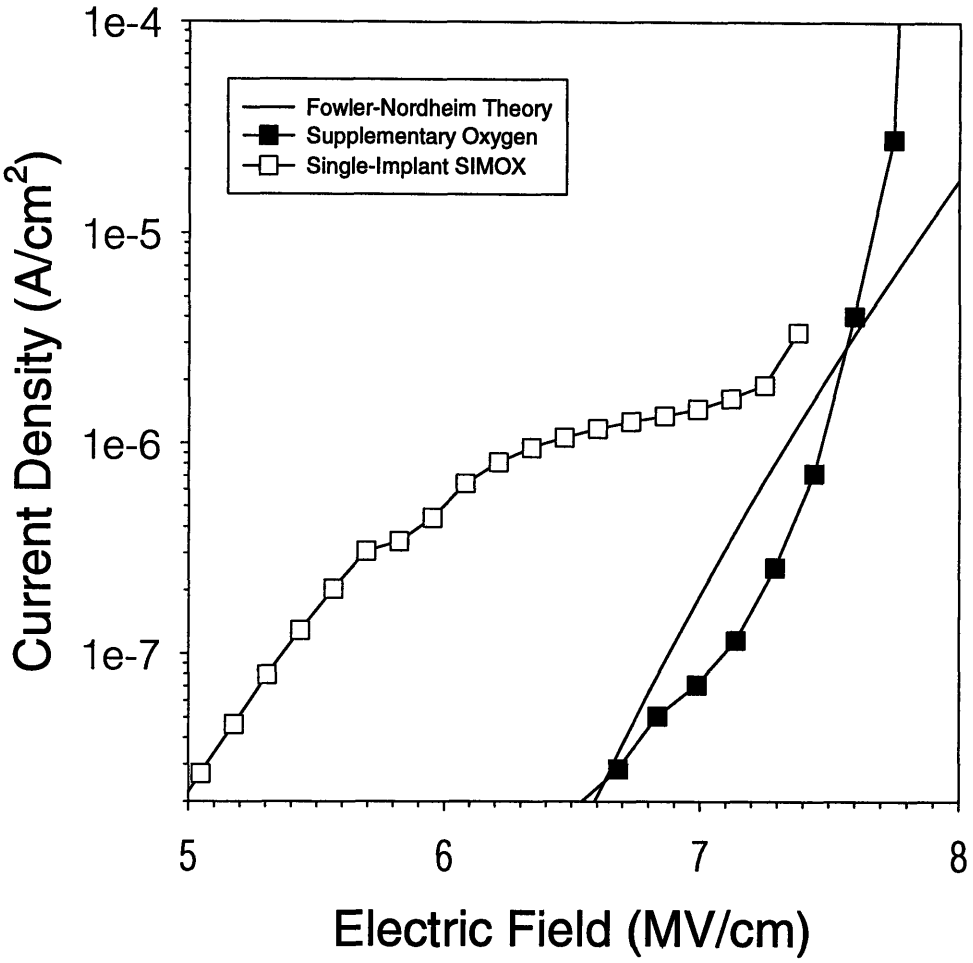


Figure 5-5 Comparison of the static J-E characteristics of supplemental-oxygen-implanted SIMOX buried oxide and standard single-implant SIMOX buried oxide. The high-field onset electric field for top silicon injection of supplemental-oxygen-implant SIMOX buried oxide resembles the theoretical thermal-oxide value. (Group C)

Supplemental-Silicon Implantation

Experiments with supplemental-silicon implantation into standard single-implant SIMOX buried oxide show that as the level of excess silicon was increased, the onset of the high-field conduction regime moved to a lower electric field, in accordance with the expectations of the conduction model (Figure 5-6). For the same dose of either supplemental-silicon versus supplemental-oxygen implantation, the observed shift of the tunneling regime to a lower onset electric field for the supplemental-silicon implantation was smaller compared to the observed shift to a higher onset electric field for the supplemental-oxygen implantation. This can be understood in terms of the over-saturation and precipitation of the excess implanted silicon. As the dose of the supplemental-silicon implantation is increased, the total amount of silicon in the buried oxide hits a saturation limit, thus precipitating out silicon crystalline micro-clusters. As these silicon islands precipitate throughout the buried oxide, the conduction mechanism can change into either tunneling between these precipitates or a trap-hopping mechanism. Such precipitation is confirmed through high-resolution TEM which shows crystalline clusters with various sizes ranging up to 10 nm as shown in Figure 5-7.

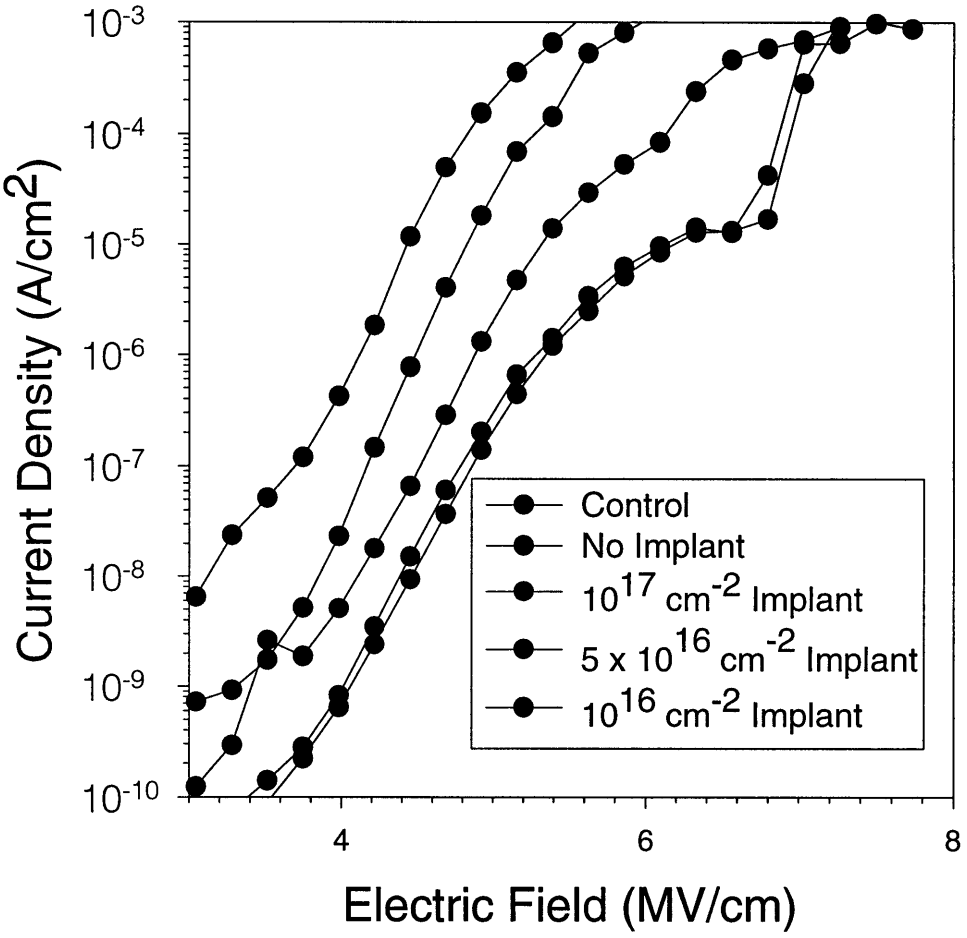


Figure 5-6 Buried-oxide J-E characteristics of the supplemental-silicon-implanted SIMOX wafers annealed at 1300 °C. As the excess silicon density within the buried oxide increases (corresponding to the increasing implant dose as indicated in the legends), the high-field conduction onset electric-field decreases. (Group D)

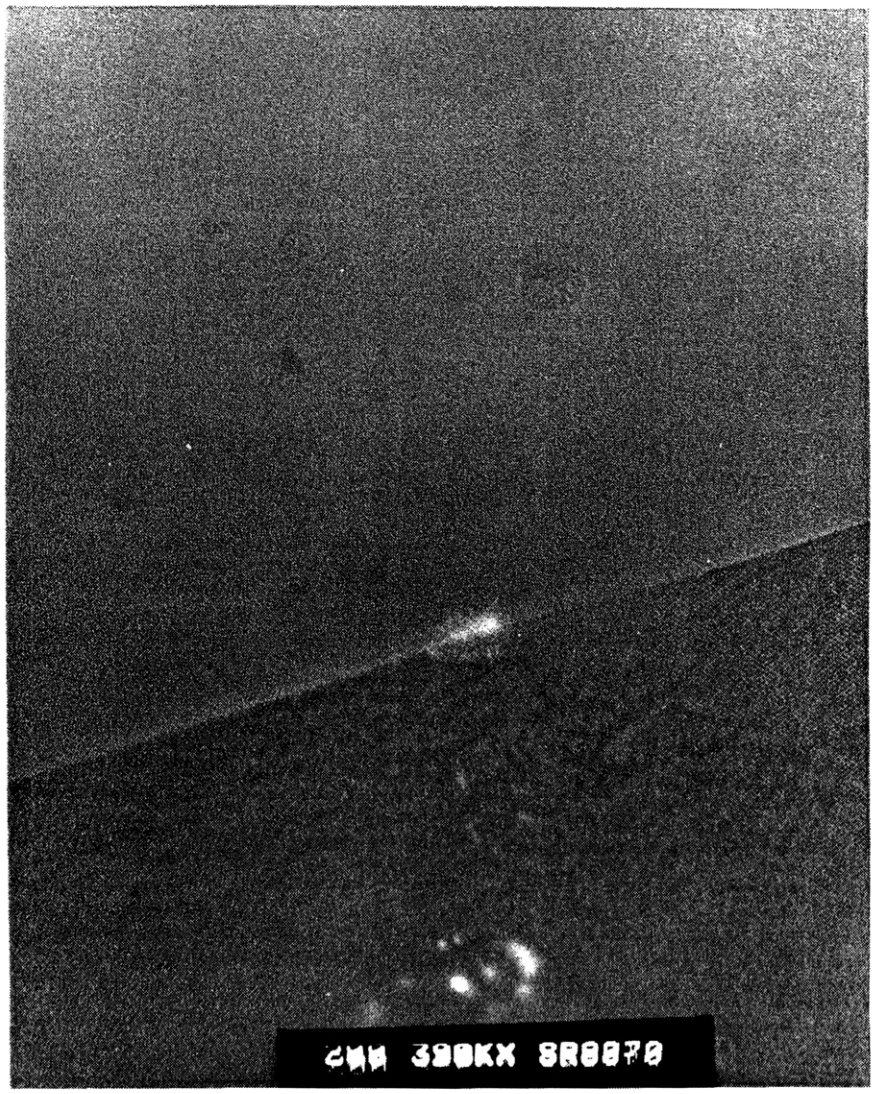
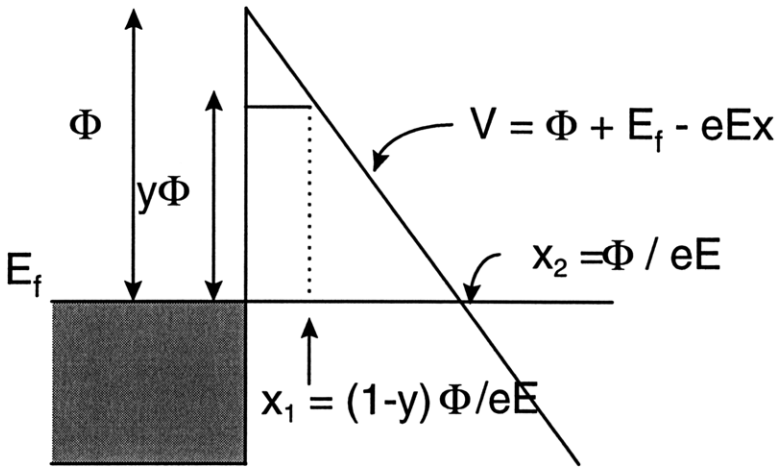


Figure 5-7 High resolution TEM of a $1x10^{17}$ cm^{-2} dose of silicon implantation into standard single-implant SIMOX buried oxide. Note the silicon precipitates present in the buried oxide. (Group D)

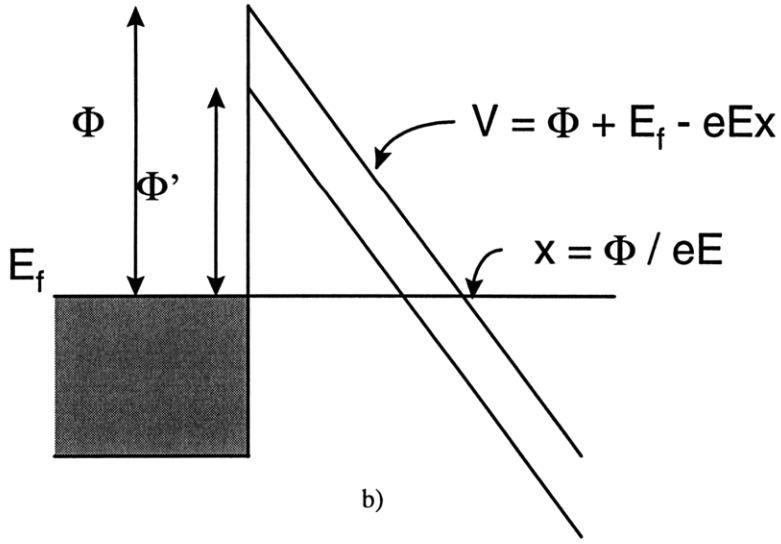
Barrier-Height for Tunneling

Once it has been shown that excess-silicon related defects are mainly responsible for the observed BOX conduction characteristics for top-cathode BOX injection, more detailed modeling of the barrier shape can be carried out. Excess silicon in the buried oxide can affect the barrier height in two ways. The first way is non-uniform barrier-height lowering and the second is uniform barrier-height lowering. The first case would

mandate that the distribution of excess silicon be concentrated towards the top interface, whereas the second case would mandate that the distribution of excess silicon to be somewhat uniform throughout the buried oxide. The tunneling coefficient is calculated for each case by the WKB approximation. [60]



a)



b)

Figure 5-8 The lowered tunneling onset electric-field for top-silicon cathode injection may be due to barrier-height narrowing or barrier-height lowering.

Using the WKB approximation, the tunneling coefficient through a barrier is defined as

$$T = \exp(-2\int_{x_1}^{x_2} k\,dx) \qquad \textbf{Equation 5-6}$$

where

$$k = \frac{\sqrt{2m(V-E)}}{\hbar} \qquad \textbf{Equation 5-7}$$

where V is the potential of the conduction band, E is applied electric-field, m is the mass of electron, and $\hbar$ is Planck's constant. The expression V-E will follow the shape of the potential barrier for electron tunneling. The final solution depends on the distribution of the excess silicon.

Case 1: Non-Uniform Distribution of Excess Silicon

For the first case, where excess silicon is distributed proportionally toward the interface, the shape of the barrier can be approximated as shown in Figure 5-8 a). In this case, the concentration of the excess silicon decreases to zero over a distance shorter than the tunneling distance. The change in the excess silicon concentration is reflected in the slope of the oxide conduction band. For this case, the integral for the tunneling coefficient can be integrated over two regimes: a region where the conduction band is constant, and a region with no change in the conduction band. The following boundary conditions can be set up for such a case, assuming that the changes in conduction band follows changes in the excess silicon concentration and that the final shape of the barrier follows the shape shown in Figure 5-8 a). The parameter $y\phi$ represents the barrier height.

First region : $0 < x < x_1 = (1-y)\frac{\phi}{eE}$

Second region: $x_1 = (1-y)\frac{\phi}{eE} < x < x_2 = \frac{\phi}{eE}$

For the first region, the tunneling coefficient is:

$$T = \exp(-2\int_0^{(1-y)\frac{\phi}{eE}} \frac{\sqrt{2my\phi}}{\hbar} dx) \qquad \textbf{Equation 5-8}$$

$$T = \exp(-2\frac{\sqrt{2my\phi}}{\hbar}(1-y)\frac{\phi}{eE}) \qquad \textbf{Equation 5-9}$$

For the second region, the tunneling coefficient is:

$$T = \exp(-2\int_{(1-y)\frac{\phi}{eE}}^{\frac{\phi}{eE}} \sqrt{2m(\phi - eE)}dx) \qquad \textbf{Equation 5-10}$$

$$T = \exp(-2\frac{\sqrt{2m}}{3\hbar e\mathrm{E}}(y\phi)^{\frac{3}{2}}) \qquad \textbf{Equation 5-11}$$

Combining these two regions, the tunneling coefficient for the barrier shown in Figure 5-8 a) is calculated to be:

$$T = \exp(-\frac{4}{3}\frac{\sqrt{2m}}{\hbar}\frac{\phi^{\frac{3}{2}}}{eE}[\frac{3}{2}(1-y)(y)^{\frac{1}{2}} + (y)^{\frac{3}{2}}]) \qquad \textbf{Equation 5-12}$$

As the concentration at the interface increases, the tunneling coefficient increases. For a y value of 80 %, the exponential term in Equation 5-8 changes to 98 % of the value without a barrier-shape change.

Case 2: Constant Amount of Excess Silicon

For the second case, there is a constant concentration of excess silicon extending deeper into the buried oxide. For such a case, the barrier height is uniformly lowered

(Figure 5-8 b). The form of the tunneling coefficient will then follow the regular tunneling coefficient with the only difference being the value of barrier-height used:

$$T = \exp(-\frac{4}{3}\frac{\sqrt{2m}}{\hbar}\frac{\phi^{\frac{3}{2}}}{eE}) \qquad \textbf{Equation 5-13}$$

where Φ is the modified barrier-height value. For the barrier height that has been lowered to 80%, the exponential term in Equation 5-9 is reduced to 72 % of its original value.

In both of the first and second cases, only the excess silicon near the interface is a factor in impacting BOX high-field conduction. Using the thermal-oxide barrier height which is 3.2 eV and assuming 5 MV/cm for the applied macroscopic electric field, the tunneling distance for electrons is calculated to be about 6 nm. Thus, only excess silicon in the top 6 nm of the buried oxide will have any effect on electron injection from the top interface.

If there is a uniform distribution of excess silicon in the first 10 nm of the buried oxide, then the barrier-height lowering model can be used to link the particular excess silicon level with the tunneling coefficient. For the first case of barrier-shape change, the change in the calculated tunneling coefficient is smaller than what is observed from experiments. Thus, the second case seems a more plausible scenario. In addition, from the kinetic model for defects introduced in the previous section, changes in the oxygen vacancy concentration over 6 nm from the top BOX interface can be estimated to be less than 10 %, assuming a time for oxygen out-diffusion of at least one hour and an anneal temperature of 1300 ^{o}C. Thus, a model assuming uniform lowering of the barrier height appears to be a good approximation for how the actual barrier-shape is impacted by the silicon-rich BOX defects.

5.4 Conclusion

In summary, using electron spin resonance and artificially-introduced silicon defects in the buried oxide, it has been shown that "amorphous silicon" clusters are not present in standard single-implant SIMOX buried oxide. A kinetic model has also been introduced to explain the existence of excess-silicon related defects and their distribution in the buried oxide. Experiments have been carried out to show the effect of excess silicon on the conduction characteristics, particularly on electron injection from the top-silicon layer. Quantum-mechanical modeling has been carried out to study the barrier shape for electron tunneling from the top-silicon layer into the buried oxide. This modeling shows that only the region near the top-silicon interface affects the conduction characteristics. This is in agreement with what is known about excess-silicon related defects. Fundamental understanding of the excess-silicon related defects in the buried oxide is gained: its nature, its origin, and its impact on conduction characteristics.

6. SIMOX BOX Silicon Islands

6.1 SIMOX BOX Formation Model

Silicon-Island Characteristics

The BOX silicon islands were studied using transmission electron microscopy. These islands are about 30 nm thick and 30 to 200 nm long, and are situated at an almost constant distance (25nm) from the bottom interface. They are crystalline with well developed facets along the (001) and (111) planes. Most islands have the same orientation as the substrate, but there are also a small number of islands which are off-axis by a small number of degrees. The existing SIMOX BOX formation model, based on silicon self-interstitial generation due to confinement effects, does not adequately explain the existence of silicon islands nor the reason for their location towards the back interface of the buried oxide. In this thesis, a simple qualitative model is developed to explain the observed shape and location of the SIMOX BOX silicon islands.

Supplemental-Silicon Implantation Experiment

Silicon was artificially introduced into standard single-implant SIMOX buried oxide to study its impact on the existing BOX silicon islands. TEM micrographs from Group D samples show that when silicon was implanted into the buried oxide, what results is a random distribution of small silicon micro-clusters exhibiting random nucleation and growth. A distribution of these clusters arises generally mirroring the supplemental-silicon implantation profile. For the samples annealed at 1000 °C, amorphous and crystalline silicon clusters were formed, as shown through ESR trace and

C-V studies. For the samples annealed at 1300 °C, only crystalline silicon micro-clusters were formed, as shown through TEM measurements (Figure 6-1).

The 1300 °C results can be explained by simple nucleation and growth theories. When silicon is implanted into the buried oxide, there is an oversaturation of silicon which results in the nucleation of very small silicon clusters. During the subsequent supplemental high-temperature anneal, these smaller clusters grow into larger clusters which are now visible under transmission electron microscopy. These clusters that form via nucleation and growth are vastly different from the silicon islands present in standard single-implant SIMOX buried oxide. Thus, the SIMOX BOX silicon islands must be formed by a different mechanism than nucleation and growth.

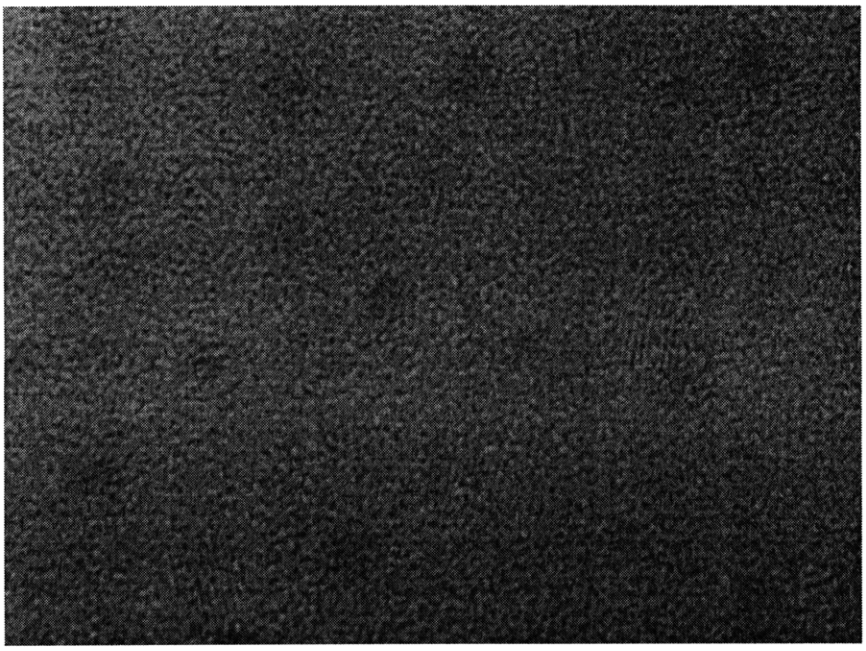


Figure 6-1 TEM of SIMOX buried oxide with a $1x10^{17}cm^{-2}$ supplemental-silicon implant annealed at 1300 °C. The observed silicon clusters have random orientation and shape. (Group D)

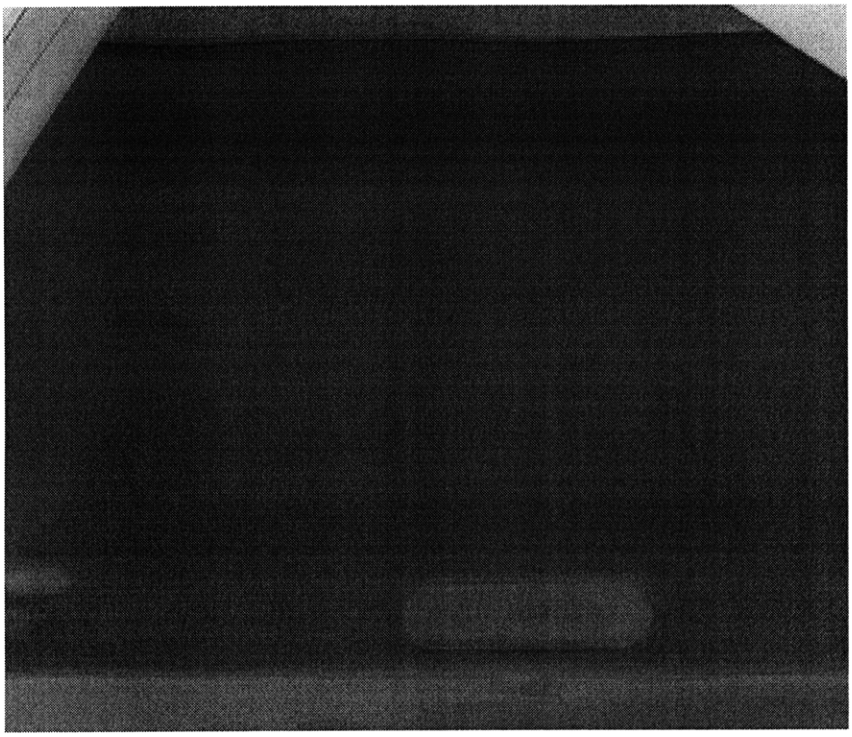


Figure 6-2 TEM of SIMOX buried oxide with supplemental-oxygen implantation. The silicon islands are still present and their distinct shape is preserved. (Group C)

Supplemental-Oxygen Implantation Experiment

SIMOX BOX silicon islands do not appear to be the result of random nucleation. According to the formation model described in Section 4.3, the buried-oxide growth occurs through silicon self-interstitial generation, not volume expansion. BOX silicon islands arise due to super-saturation of these oxidation-induced self-interstitials within the islands which prevents the oxidation reaction from going to completion.

This above hypothesis is supported using data from experiments involving supplemental-oxygen implantation. The supplemental-oxygen implantation is observed to decrease the number of excess-silicon related defects, but to have little impact on the silicon islands themselves. Figure 6-2 shows the presence of silicon islands and their distinct shape. This observation supports the theory that, in a confined space, SIMOX

BOX oxidation occurs through silicon-interstitial formation, not volume expansion. Also, if the silicon islands are the result of silicon self-interstitial build-up and saturation within each of the islands, then the addition of oxygen through supplemental implantation should not be expected to have any impact. Silicon islands, located within buried oxide, can only be oxidized through the following mechanism:

$$xSi + O_2 \rightarrow SiO_2 + (x-1)Si_i \qquad \textbf{Equation 6-1}$$

where Si is the crystalline silicon to be oxidized, O_2 is an oxygen molecule, and Si_i is the silicon self-interstitial.

For SIMOX BOX silicon islands to be oxidized, silicon self-interstitials must form. However, since the islands are isolated from either the substrate or the top silicon layer, there is no sink to which these self-interstitials can diffuse. In addition, there is already a saturation of silicon interstitials inside each of the silicon islands which inhibits further oxidation. Thus, even when supplementally-implanted oxygen diffuses towards the silicon islands, the oxygen can not react with the islands but must instead diffuse into the silicon substrate or stay within the bulk of the oxide.

The following BOX island formation model combines the concept of silicon self-interstitial generation and work done by Spaggiari [61] on homogeneous and heterogeneous oxide nucleation. When oxygen is implanted into the silicon substrate to create buried oxide, there are two mechanisms for oxide precipitation: homogeneous and heterogeneous nucleation. Homogeneous precipitation takes place in the region centered on the most probable penetration depth, x_{max}. This is the region where the concentration of oxygen is at maximum. Only when the dose exceeds a characteristic value of oxygen fluence, Φ_{HO}, which generally depends on the implantation conditions, does

homogeneous precipitation take place. When $\Phi < \Phi_{HO}$, homogeneous precipitation cannot occur and heterogeneous nucleation takes place. In heterogeneous precipitation, oxide precipitates are formed in the region of maximum damage production via the diffusion of implanted oxygen. This mechanism requires a sufficiently high temperature and sufficiently long implantation time to allow for adequate diffusion. Both mechanisms are diffusion-limited, thermally-activated, processes. [62]

Because the depth at which homogeneous precipitation occurs is different from the depth at which heterogeneous precipitation occurs, the silicon layer between them is trapped between oxide layers. As the oxide precipitates coalesce to form a continuous buried-oxide layer, portions of the silicon layer will be trapped forming silicon islands. The build-up of silicon interstitials in these trapped silicon regions blocks the oxidation reaction from going to completion. Thus, these trapped silicon regions become BOX silicon islands and take the form of disks to minimize the surface energy.

6.2 Modified High-Field Conduction Model

Experiments were carried out on the samples (Group B through Group E) mentioned in Section 3.2 to verify that the BOX silicon islands had the expected effects on electron injection from the substrate. This provides fundamental understanding on the effect of BOX silicon islands on the conduction characteristics.

Multiple-Implant SIMOX Wafers

Transmission electron microscopy showed that one of the multiple-implant wafer samples had no silicon islands (Figure 6-3), whereas the other multiple-implant sample

had silicon islands (Figure 6-4). By examining multiple-implant samples known to be non-stoichiometric, meaning that no excess-silicon related defects were present, the effect of silicon islands on BOX high-field conduction could be decoupled from the effect of the excess silicon. There is a clear difference between the onset electric field for single-implant SIMOX buried oxide and for the two multiple-implant SIMOX buried oxides as shown in Figure 6-5. The multiple-implant SIMOX sample without silicon islands shows tunneling characteristics very similar to that of thermal oxide, whereas the multiple-implant SIMOX buried oxide sample with silicon islands shows tunneling characteristics similar to that of standard single-implant SIMOX buried oxide. Thus, only the BOX silicon islands appear to govern electron injection from the substrate.

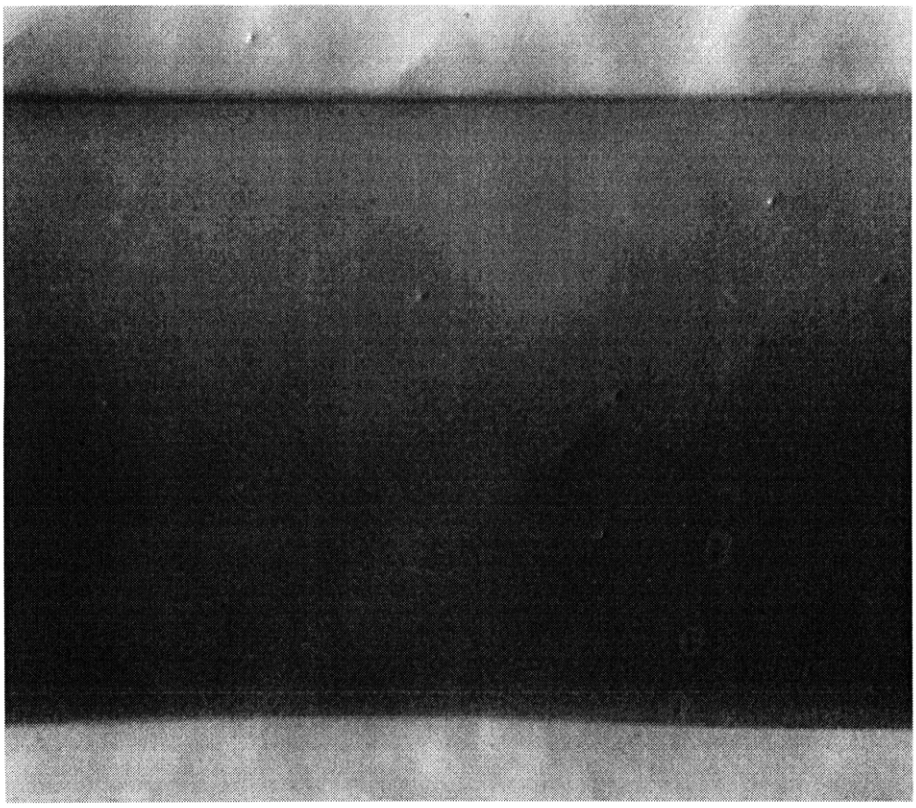


Figure 6-3 TEM of a multiple-implant sample with no silicon islands. (Group B)

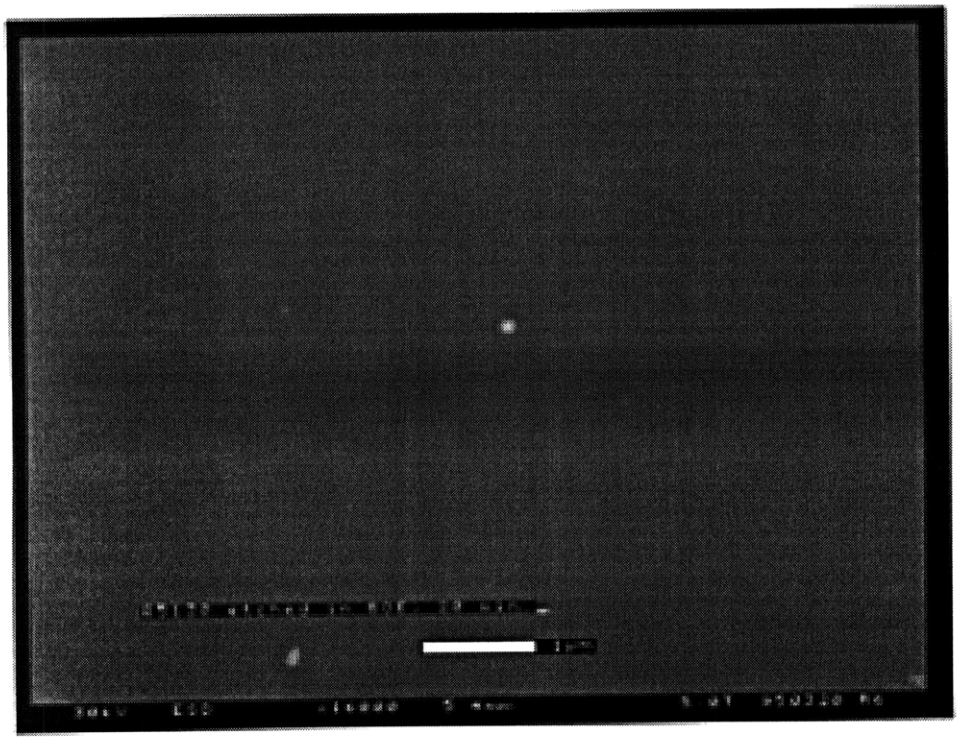


Figure 6-4 SEM of a multiple-implant sample with few silicon islands. The SEM picture shows the distribution of islands within the buried oxide. (Group B)

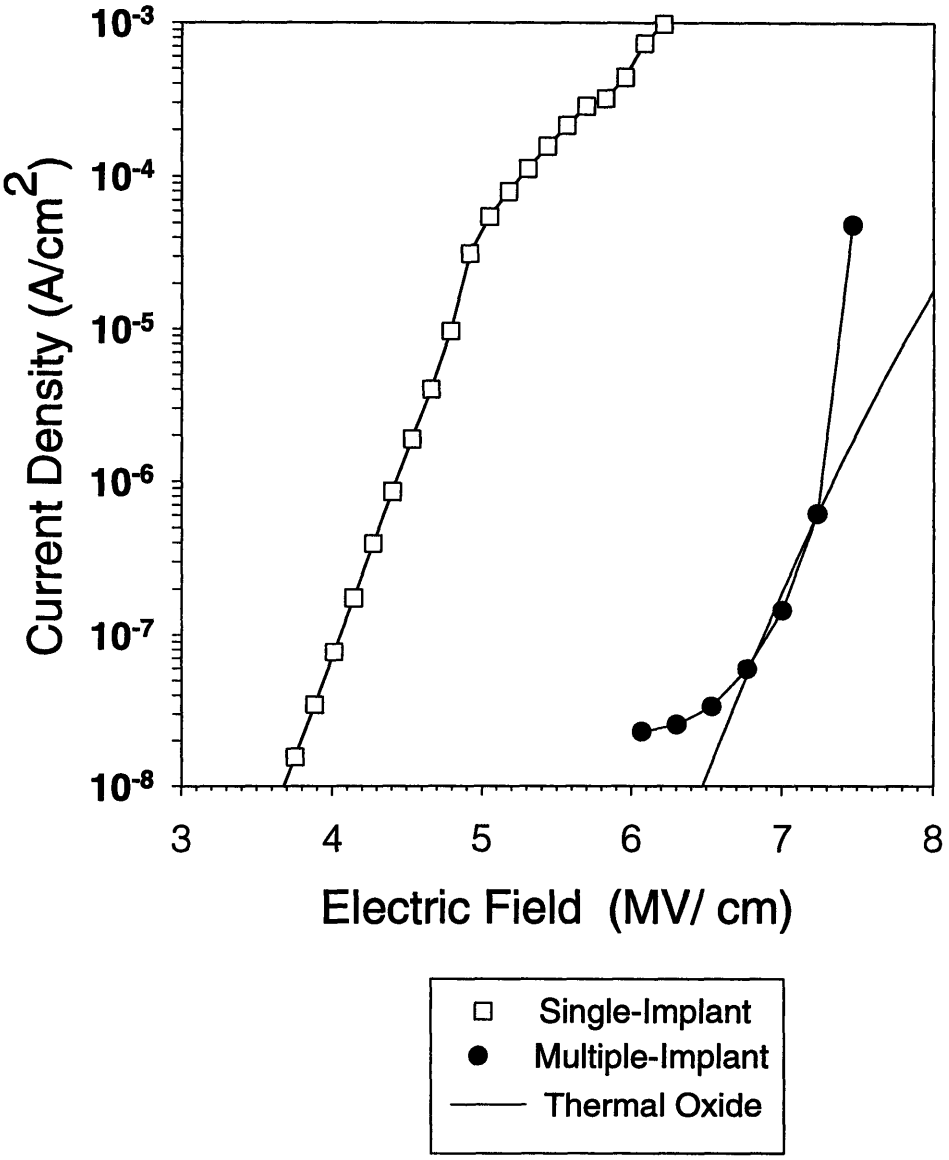


Figure 6-5 A comparison between the J-E characteristics for two multiple-implant SIMOX buried oxide samples and a standard single-implant SIMOX buried-oxide sample. The multiple-implant sample with no silicon islands shows characteristics similar to that of thermal oxide whereas the multiple-implant sample with silicon islands shows characteristics similar to the single-implant SIMOX buried-oxide sample. (Group B)

Supplemental-Oxygen Implantation

Supplemental oxygen implantation into the single-implant SIMOX buried oxide did not have any noticeable effects on electron injection from the substrate, as shown in Figure 6-6. As supplemental-oxygen implantation is known to decrease the amount of excess-silicon related defects in the buried oxide, this shows that electric-field enhancement at the edges of the silicon islands is the dominant factor for electron injection from the substrate.

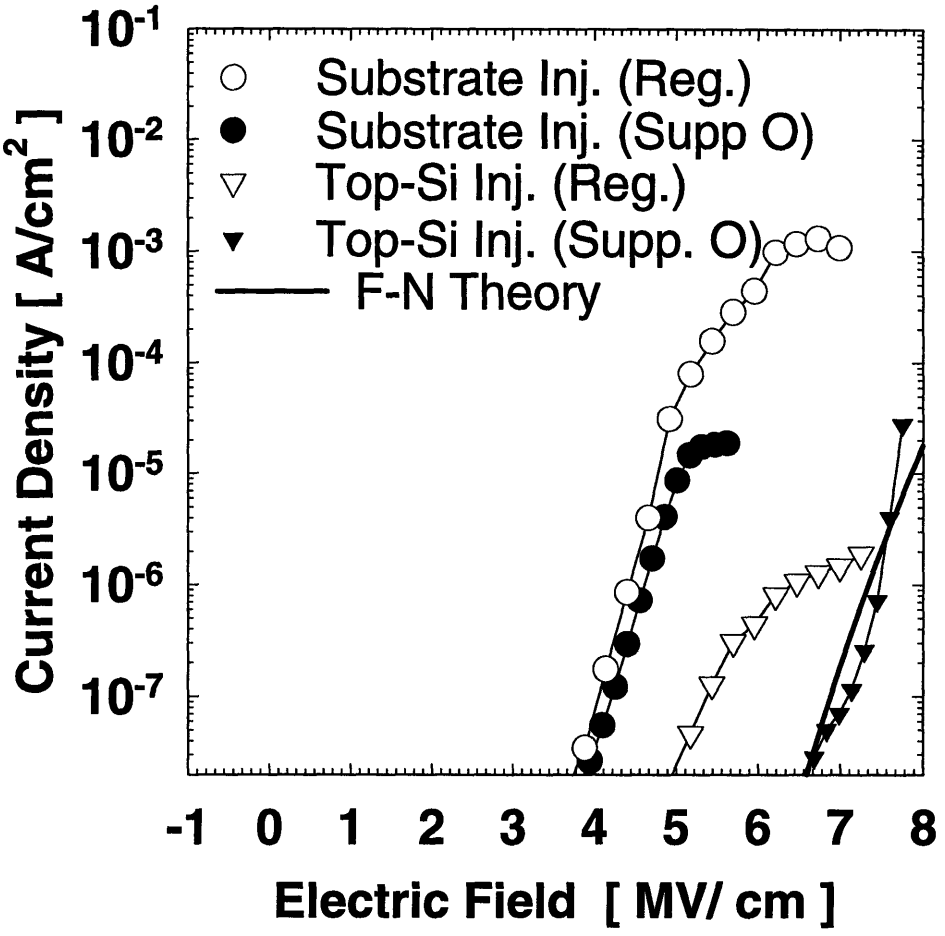


Figure 6-6 A comparison of the J-E characteristics for the supplemental oxygen-implanted SIMOX buried-oxide sample and the standard single-implant SIMOX buried-oxide sample. The supplemental-oxygen implantation did not change the conduction characteristics of the buried oxide. (Group C)

Supplemental-Silicon Implantation

Supplemental-silicon implantation, which has an opposite effect from supplemental-oxygen implantation, does not appear to impact the conduction

characteristics for substrate injection. Changing the level of BOX non-stoichiometry does not impact the substrate-injection characteristics, as shown in Figure 6-7. Also, the introduction of randomly oriented crystalline/amorphous crystalline clusters does not appear to have any impact as well. Because substrate injection is dominated by electric-field enhancement at the silicon-island edges, altering BOX bulk physical properties should not affect the electron-injection characteristics.

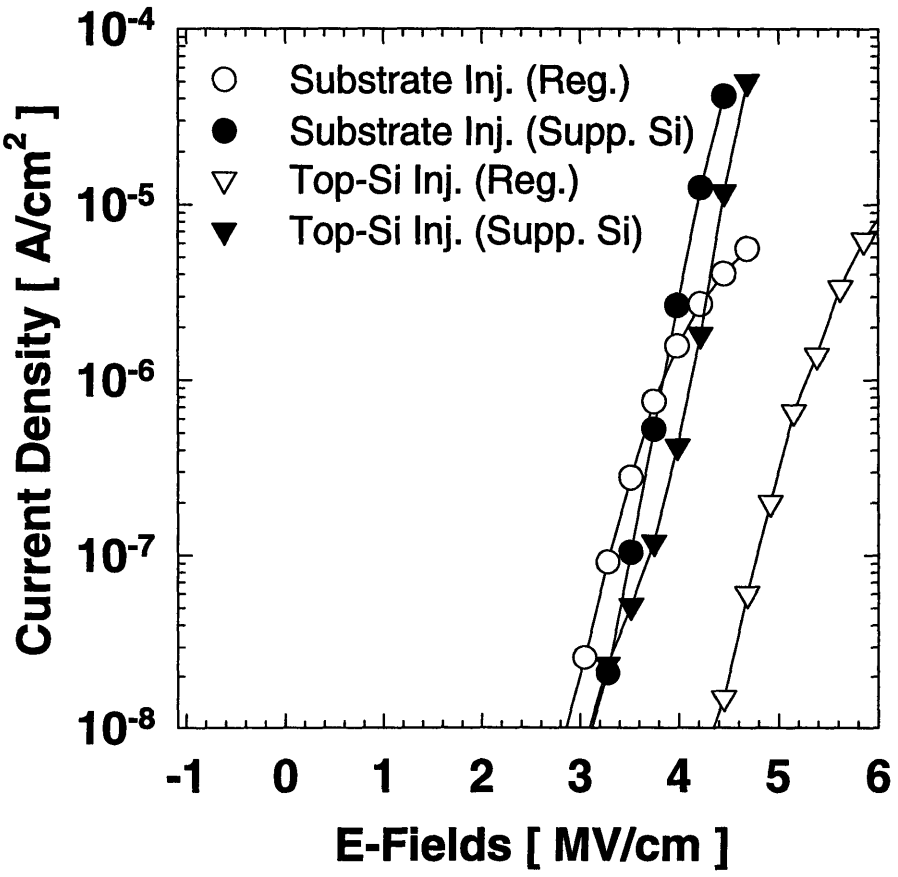


Figure 6-7 A comparison of the J-E characteristics of the supplemental-silicon-implanted SIMOX buried-oxide sample and the standard single-implant SIMOX buried-oxide sample. The supplemental-oxygen implantation did not change the substrate-cathode injection characteristics of the buried oxide. (Group D)

Revised Conduction Model

The existing conduction model can now be revised based on the improved understanding of the BOX conduction physical mechanisms and the BOX microstructure. Because electrons tunnel easily into the silicon islands from the substrate before being injected across the buried oxide, the effective thickness of the buried oxide at the silicon islands should modeled with a value less than the thickness of the entire buried oxide. This shortened distance is now accommodated into the model. From Section 4.4.4, BOX Fowler-Nordheim tunneling is given by:

$$J = k_a \left[\frac{A_o}{\phi_B}\right](k_e E_o)^2 \exp\left(\frac{-B_o \phi_B^{\frac{3}{2}}}{k_e E_o}\right) \qquad \textbf{Equation 6-2}$$

where

$$E_o = \frac{V_{BOX}}{t_{BOX}}\left[\frac{MV}{cm}\right] \qquad \textbf{Equation 6-3}$$

A modified value for t_{BOX} must be used, which is just the average distance from the top-silicon interface to the edge of the silicon islands. From transmission electron micrographs, silicon islands are generally 30nn thick and about 20 nm away from the substrate. In such a case, 50 nm should be subtracted from the BOX thickness of 400 nm. This 10 % decrease in thickness translates into a 11 % effective increase in the bulk electric field at silicon islands. Note, that this increase will be in addition to the electric-field enhancement factor at the silicon islands. In addition, the thermal-oxide value of the barrier height should be used as no difference was shown for samples with different levels of BOX non-stoichiometry.

Single-Implant SIMOX Substrates with Different Substrate Implant Temperature

The substrate implant temperature can affect the properties of silicon islands toward the back interface. Figure 6-8 shows the electrical characteristics of single-implant SIMOX buried oxide that had been processed under three different substrate-implant temperatures.

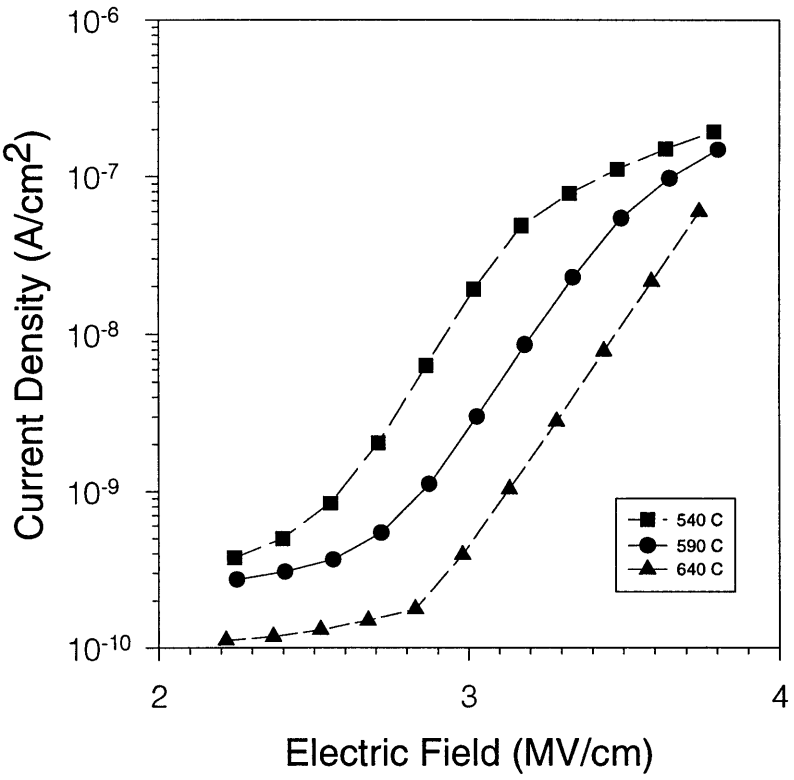


Figure 6-8 Buried-oxide J-E characteristics of SIMOX wafers with different substrate implant temperatures. As the substrate implant temperature increased, the high-field tunneling regime shifted towards higher onset electric field. (Group E)

Correlation between Silicon Island Density and the Extracted Model Parameter k_a

Scanning electron microscopy and transmission electron microscopy were carried out to correlate the measured silicon-island density and the extracted model parameter k_a, the effective injection area (Figure 6-9). There is an observed correlation between the silicon-island density and the parameter k_a. The parameter k_a was calculated using the thermal-oxide value for the barrier-height as well as under the assumption that electric-field enhancement at the silicon islands was both the dominant and limiting factor in electron injection from the substrate. The observed correlation in Figure 6-8 helps confirm the effect of BOX silicon islands on the high-field conduction characteristics.

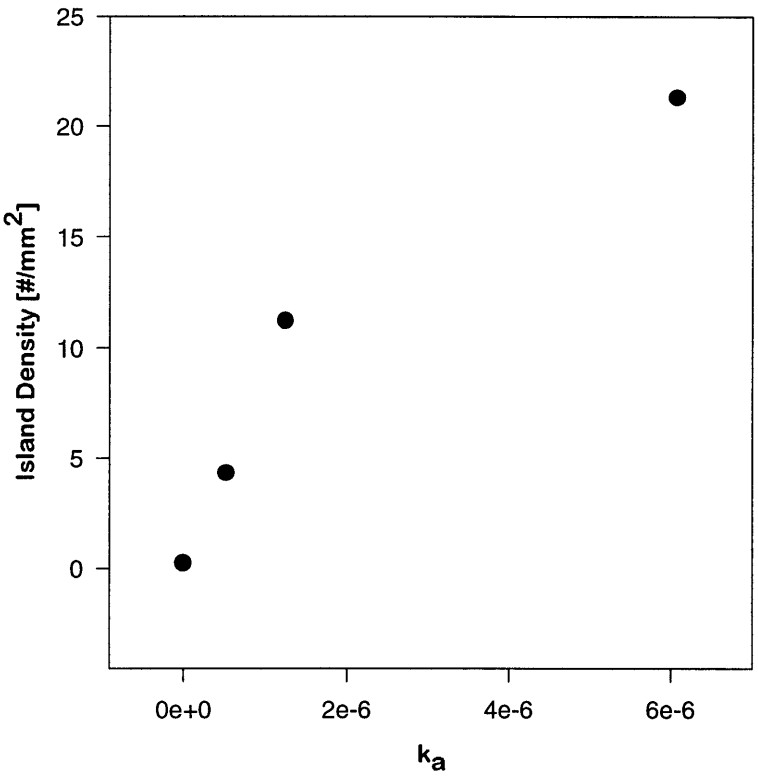


Figure 6-9 Correlation between the extracted parameter k_a and the measured silicon-island density of different samples. (Group A and B)

6.3 Conclusion

In summary, using SIMOX samples fabricated using different processes, oxide growth through silicon self-interstitial generation has been verified and a new BOX formation model, explaining the location and shape of the BOX silicon islands, has been proposed. The effect of BOX silicon islands on electron injection from the substrate has been studied. It has been shown that BOX non-stoichiometry, which had great effect on electron injection from the top-silicon layer, does not affect conduction from the substrate. The BOX high-field conduction model has been revised to accommodate these new findings. The correlation between silicon-island density and the extracted parameter for the effective electron injection area is also shown. Overall, further understanding about BOX silicon islands has been gained about their formation, and their impact on BOX conduction characteristics.

7. Introduction to CMP

7.1 CMP Background (Chemical Mechanical Polishing)

History of CMP

Chemical mechanical polishing (CMP) is the process of smoothing and planing due to chemical and mechanical forces. Historically, CMP has been used to smooth out a variety of materials. Much historical CMP work has been done on making glass lenses. [63] Recently, this technique has been applied to planarize the VLSI-technology interlayer dielectric (ILD) and metallization in order to form interconnections between devices. Planarization of the interlayer dielectric layer is required because the topography that results from VLSI fabrication processes often is not flat due to an underlying previously-patterned surface. A flat surface is mandatory in order to make patterns for the following layer using lithography. Variation in the interlayer dielectric dimensions can also have an adverse impact on circuit performance.

Overview of CMP Processing

The CMP process consists of moving the sample surface to be polished against a pad that is also used to provide support for the sample itself (the pad thus experiences the pressure exerted by the sample). Slurry is flowed between the sample surface and pad and has a strong impact on the polishing and planarization behavior. Abrasive particles in the slurry cause mechanical damage to the sample surface, loosening the material either for enhanced chemical removal or for fracturing off the pieces of the surface into the slurry,

where they either dissolve or are swept away. In a CMP process, there are many variables that must be controlled in order to give reliable and consistent planarization results.

CMP Advantages

The advantages of CMP processes are numerous. It can achieve a greater degree of global planarization than is possible using other processing steps. It can also be applied to many types of surfaces, even for multi-material systems. It can reduce severe topography variations, allowing for VLSI fabrication with tighter design rules and additional interconnection levels. CMP processes also require no hazardous gases or liquids for its operation. [64]

Die-level vs. Wafer-level Variation in CMP

In CMP processing, variation in the final thickness of the interlayer dielectric (ILD) layer can be categorized into two main components: wafer-level variation and die-level variation. Wafer-level variation is variation at the wafer-scale, whereas die-level variation is variation within each die. Most attention so far has been paid to wafer-level variation with less attention being paid to die-level variation. It had been viewed that there was not as much variation at the die-level because the length scale was so much shorter than at the wafer-level. Any die-level variation was assumed to be hidden underneath larger wafer-level variation. However, as shown in Figure 7-1, die-level variation can often be as large or larger than wafer-level variation. This should not come as a surprise if one considers that, within a die, there can be a large variation in terms of the dimensions of structures underneath the dielectric layer that is undergoing planarization. The underlying pattern density has been shown to be a key factor affecting polishing behavior in CMP processes.[65, 66, 67] Thus, it is crucial to be able to

decouple the die-level contribution from the wafer-level contribution for CMP-induced variation.

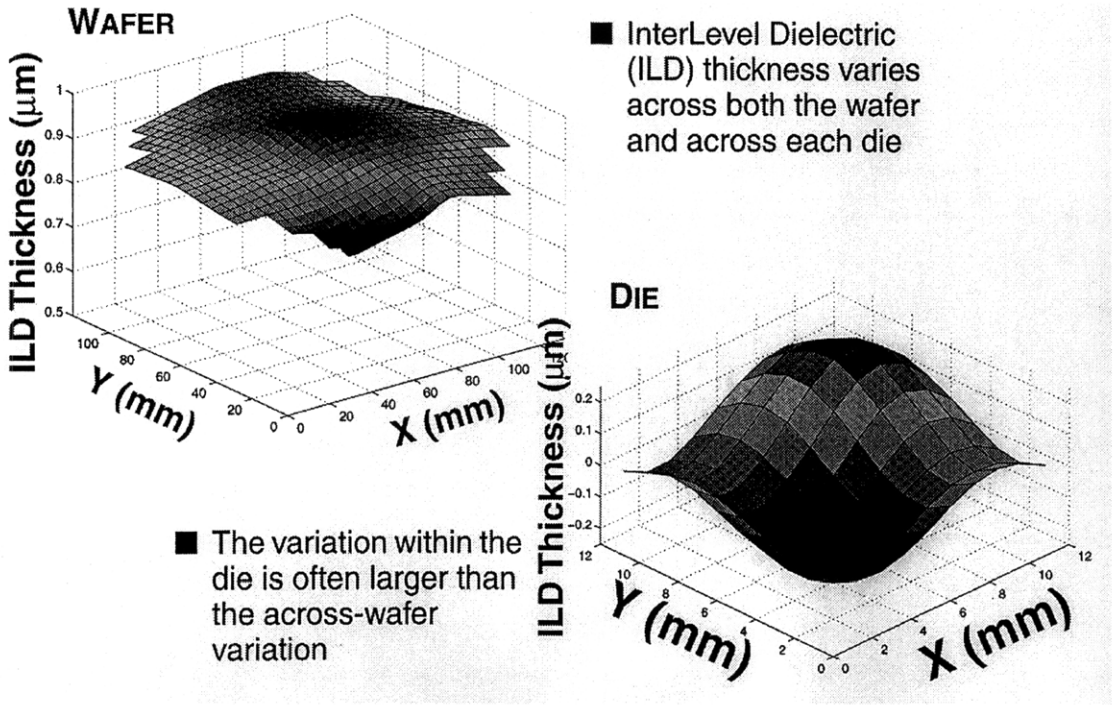


Figure 7-1 Die-level variation vs. wafer-level variation of the inter-level dielectric layer thickness. The die-level variation is as large as the wafer-level variation.

7.2 Background of Nitride/STI CMP

STI Technology

In recent years, Shallow Trench Isolation (STI) has become a widely adopted VLSI isolation scheme. A typical STI process sequence includes the following process steps: pad oxide growth, LPCVD nitride deposition, trench lithography, trench etch, resist strip/clean, liner oxidation, CVD oxide trench fill, planarization, post-CMP clean/light

BHF dip, nitride, strip, pad oxide strip, sacrificial oxide oxidation, sacrificial oxide strip, gate-oxide oxidation, and gate electrode deposition.

One of the most important issues for STI is the trench top-corner profile. Sharp corners and the resulting gate-oxide thinning that can occur there can lead to a high electric field at the corners, produce undesirable kinks in the MOSFET I-V characteristics, produce higher off-current, aggravate reverse narrow-channel effects, and degrade gate-oxide reliability.[68]

Motivation for Studying Nitride/STI CMP

Pattern-dependent effects in oxide CMP have been previously studied. A semi-empirical model has been developed to describe the oxide CMP pattern-dependency and to predict the polish rate based on the patterns underneath the dielectric layer.[69] However, unlike oxide CMP, not much research has focused on nitride CMP. The only data widely known is that the nitride polish rate is much slower compared to oxide. Its pattern-dependency is not known at all. Understanding nitride CMP is vital in developing robust STI processes since the nitride is used as a polish stop in STI structures. The problem in STI processes can be likened to a problem of polishing two materials of different properties at the same time.

7.3 Problem Statement

A semi-empirical model for oxide polish has been previously developed and used to predict the oxide polish rate based on the underlying pattern density. This model gives a physical explanation for the dependency of the polish rate on the pattern density. However, not much is known about nitride polishing behavior, which is important for STI

structures. In addition, no model, either qualitative or quantitative, has been developed for the polishing of STI structures.

In this thesis, the following questions will be raised and addressed: First, the application of the oxide CMP model for nitride CMP will be examined. This will also address the question of whether or not CMP polishing can be explained on purely physical factors or whether it must incorporate a chemical component. Second, the question of whether or not the oxide CMP model can be used to predict the time required to expose the nitride polish stops will be addressed. The polishing behavior of various samples with oxide deposited on top of nitride is investigated to address this issue. Third, in STI structures, after the polish stop is reached, there ends up being two materials being polished at the same time. How this presence of two materials affects the final polished topography will be studied and a model developed to explain this behavior.

7.4 Overview of CMP Section

In Chapter 8, a general methodology used to characterize CMP processes is described. A semi-empirical model developed for oxide CMP is described along with an extraction method for interaction distance which is a key parameter used to describe a CMP process. In Chapter 9, the oxide CMP model is extended to describe nitride CMP behavior. The polishing behavior is shown to be independent of the material type. Differences between single-material CMP and dual-material CMP, such as exists in STI processes, are highlighted. A model is developed to describe the phenomena of dishing

and erosion, which are distinguishing polishing characteristics present in dual-material CMP.

8. CMP Characterization Methodology

8.1 Testing Methodology

8.1.1 Mask Description

A density mask was used to investigate the layout pattern density-dependency of nitride and STI CMP. Figure 8-1 shows the as-drawn density values for each of 25 structures in a die. However, for all experimental values used in this thesis, density for each structure examined within a die was actually measured using a profilometer rather than relying on the as-drawn layout value in order to give more realistic values for the density. The size of the entire die was 1 cm by 1 cm. The pitch was kept constant at 250 μm.

60 %	80 %	90 %	98 %	100 %
40 %	60 %	75 %	85 %	100 %
25 %	40 %	50 %	70 %	100 %
15 %	25 %	30 %	50 %	100 %
5 %	10 %	20 %	30 %	60 %

Figure 8-1 Test-mask floor plan with density values. Density is calculated by taking the ratio of the nitride pillar width over the sum of the nitride pillar and trench width.

8.1.2 Process Splits

The purpose of the nitride test wafers was to study how the semi-empirical model constructed for oxide CMP could be transferred to nitride CMP and to understand the general polishing behavior of nitride in order to understand the role of nitride in Shallow Trench Isolation (STI) processes. In STI process, the nitride is used as a polish stop before being etched away. Devices are built on the exposed silicon area between the remaining oxide pillars as shown in Figure 8-2.

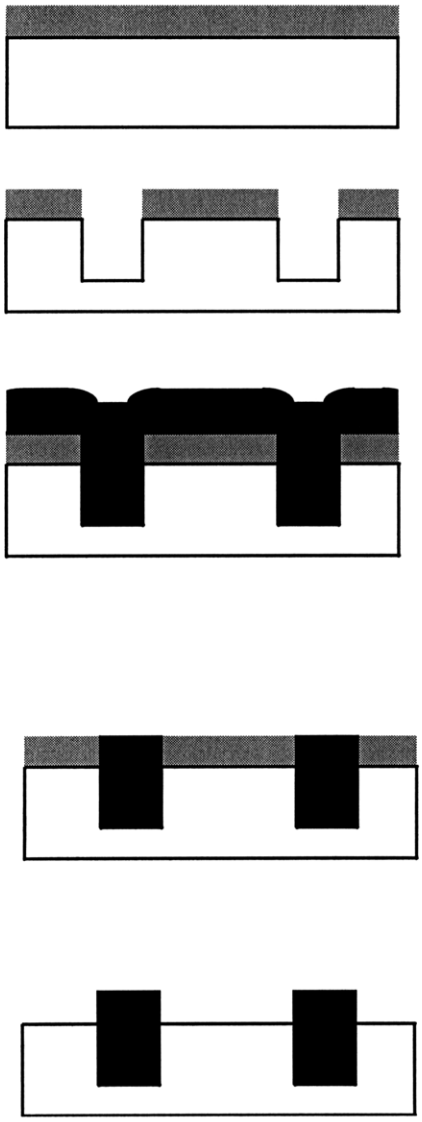


Figure 8-2 Simplified STI process showing the oxide pillars which separate the device regions. CMP is utilized to planarize the nitride and oxide. The white layer is the silicon substrate. The gray layer is the nitride layer. The black layer is the oxide layer.

In this study, two different test structures were fabricated. The first structure was a nitride film that had been patterned using the density mask. Studying the CMP behavior of these patterned structures helps determine the interaction distance of nitride polishing. The second structure was the patterned nitride film covered with an oxide film. These structures simulate STI structures by having the raised area of nitride act as a polish stop,

since it is generally known that the polish rate of nitride is much slower than the polish rate of oxide.

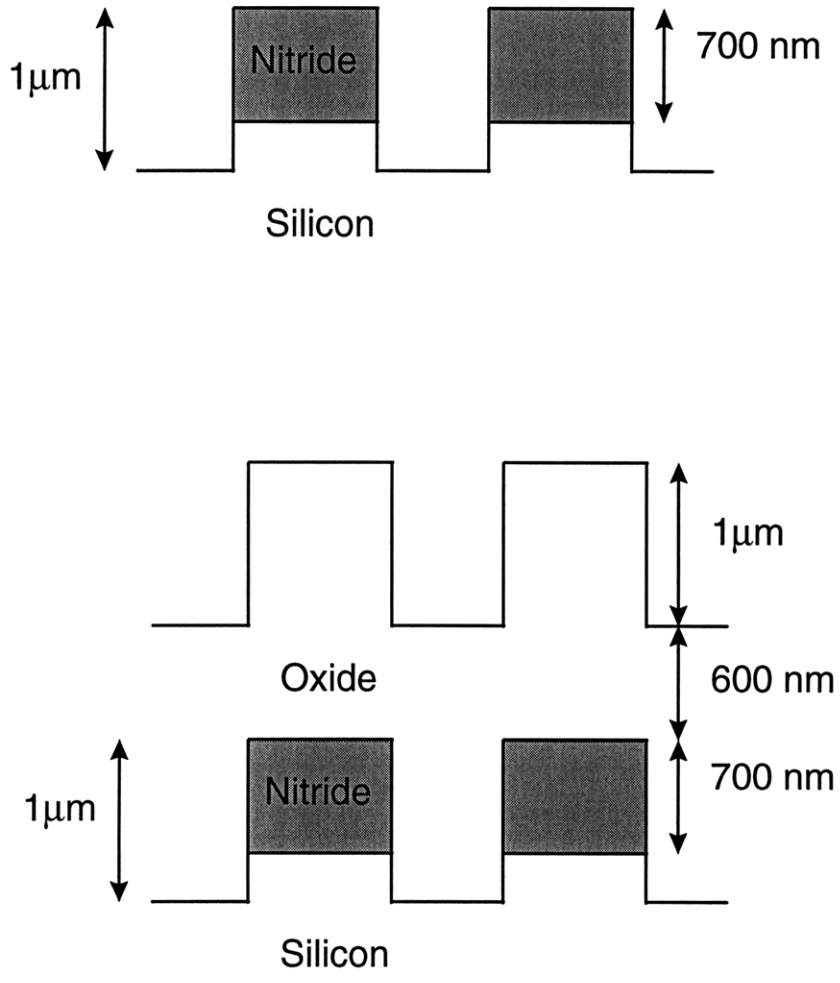


Figure 8-3 Fabricated test structure for nitride CMP and STI CMP.

8.1.3 Fabrication Process

The test structures were fabricated at the Integrated Circuits Laboratory (ICL) of the Microsystems Technology Laboratories (MTL). Figure 8-3 shows two structures fabricated to study nitride and STI CMP. The density mask described in Section 8.1.1 was used to make different density structures for the first type of test structures. A Novellus Concept One reactor was used to deposit 700 nm of PECVD nitride. This film then

underwent a lithography process and an etching process using an AME5000 plasma etch tool. For the second type of test structure, 1600 nm of PECVD oxide was deposited on top of the patterned lines of the first test structure using the Novellus Concept One. Once the fabrication of each test structure was completed, they were polished using a Strasbaugh polishing machine with a Cabot SS-25 slurry, a pH of approximately 9, and silicon particles in sizes ranging from 100 nm to 125nm. A Rodel 1000 double stacked-pad was used. For these experiments, the standard pad and slurry composition used for oxide polishing was used, rather than any high-selectivity slurries which are normally used in industry.

8.1.4 Characterization Techniques

Two different techniques were used to characterize the oxide and nitride polishing behavior. In the first method, an optical measurement tool was used for the thickness measurement of dielectric layers before and after CMP. The second technique was a profilometer for measuring the dielectric-layer topographic profile.

Optical interferometry is a commonly-used technique for directly measuring film thickness.[70] It offers reasonably high throughput as well as an absolute thickness measurement, assuming that the tool is properly calibrated. For each test wafer, a five-die, a nine-die, or a full-wafer sampling scheme can all be used. In a five-die strategy, five-die near the center of the wafer are measured. This is useful for quick analysis and initial model development, but does not provide any information about edge or detailed spatial effects across the wafer. In a nine-die sampling scheme, one die at each edge of the wafer (top, left, right, and bottom) and at the same radius are sampled in addition to the five die

from the center of the wafer. This technique can provide additional information about edge effects. Finally, a full-wafer scenario can be used in which every die is sampled on the wafer. While the throughput of this technique is quite low, more powerful data analysis techniques can then be used. Automated optical metrology is limited to structures with linewidths greater than 10 μm. For smaller structures (down to about 4 μm), optical metrology can still be used, but only in a manual mode with much lower throughput and with less reliable results. For all optical measurements in this thesis, a nine-die sampling scheme was used.

Profilometry is another technique that is often used for CMP metrology. In profilometry, a sharp stylus is dragged across the surface of interest and deflections of the stylus are measured. Profilometry can be used in a three-dimensional (3-D) mode to generate an entire die map, or in a two-dimensional (2-D) mode to generate planarization information over centimeter-scale distances. In profilometry, measurements are susceptible to stage tilt and bias as well as to wafer bow and warp.

8.2 Existing Oxide CMP Model

8.2.1 Density Dependence of Oxide CMP

Previous studies have shown that the interconnect layout-pattern density is the most crucial parameter in determining the oxide the CMP polish rate.[71] This conclusion came from oxide polish experiments performed using area, pitch, density, and aspect ratio masks. Figure 8-4 shows the results of these previous experiments. Note that the pitch mask shows that the final ILD thickness does not appear to be affected by the increase in pitch. Similarly, increasing the aspect ratio does not result in any significant

difference in the final ILD thickness. The area mask does appear to show that the polish rate depends upon the size of the area. However, in this case, note that each area actually has distinct differences in density. Once the density factor is taken out, increasing the area in of itself does not result in either an increase or a decrease in the final ILD thickness. Changes in density can be clearly correlated with changes in the final ILD thickness. As the density goes up, the final ILD thickness goes up, meaning the polish rate goes down.

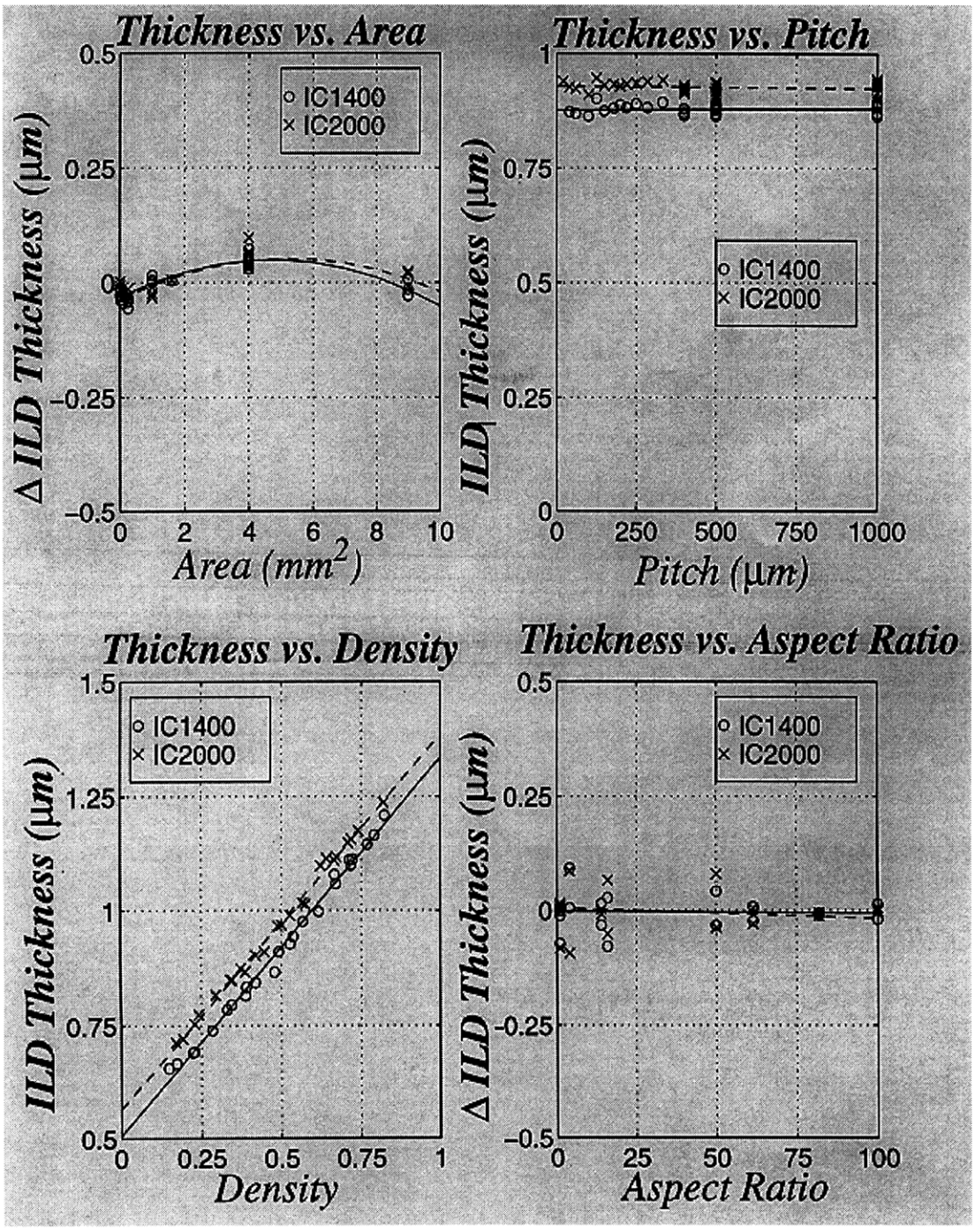


Figure 8-4 Previous CMP experimental results for different test masks. Density has a clear correlation with the final dielectric thickness, whereas the other parameters do not appear to affect the final dielectric layer thickness.

8.2.2 Definition of Pattern Density

Pattern density can be defined as the ratio of raised area over the total area. This is graphically illustrated in Figure 8-5. It shows a simple cross section of a test structure composed of two 1mm wide metal lines separated by a 1 mm and a 5 mm line which is separated from the 1 mm lines by 3.5 mm. As the lines are very wide, it is assumed that the deposition of the dielectric layer mirrors the underlying metal lines. Then the profile of the dielectric layer can be estimated given the layout pattern of the underlying metal. In most cases, though, the deposition profile is different from the patterned metal layer, as the structures are not as wide as assumed here. In such cases, the difference between the dimensions of the underlying layer and the dimension of the actual deposited film must be taken in to account in modeling the pattern density.

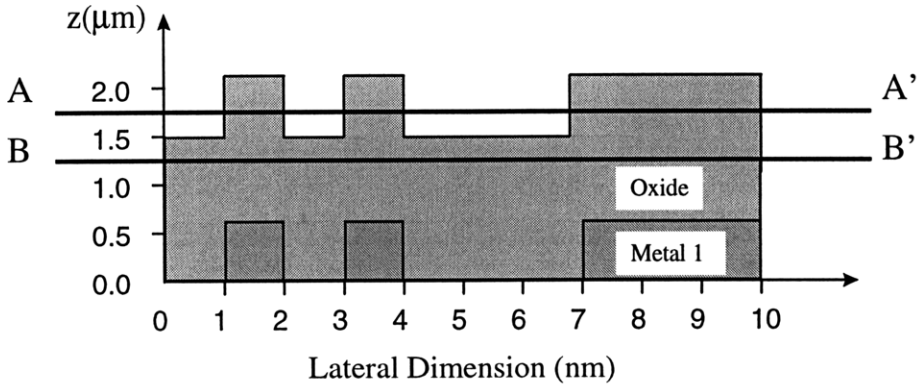


Figure 8-5 Definition of layout-pattern density.

Pattern density can be defined as the volume fraction of oxide within an infinitesimally thin surface. For example, the surface formed by A - A' in Figure 8-5 is dz thick and the total volume of oxide inside this surface is 1 + 1 + 2.5 = 4.5 mm x dz. The maximum volume possible within A - A' is 10 mm x dz. In this case, the pattern density

is 4.5/10 = 0.45 = 45 %. Using this definition, the pattern density can be calculated at any depth within the structure. As Figure 8-5 shows, the pattern density is a function of z. The pattern density at depth B will be different from that calculated at A, as the volume fraction of oxide will be different. For example, the pattern density at B - B' is 10.0/10.0 = 1 = 100 % which is significantly different than the 45 % pattern density at surface A - A'. As CMP is a process that polishes layers down with time, the pattern density that the pad sees will change as it polishes.

Definition of Interaction Distance

Pattern density, as defined, leaves much room for ambiguity. For example, in the previous example, if the pattern density were to be calculated for a window of 5 mm in length in the lateral dimension, the density value will be significantly different from the value calculated for a window of 10 mm in length. For another example, if the density were to be calculated for the entire wafer, then there would be no difference in effective density regardless of where on the wafer the density were to be determined. On the other hand, if the density were to be calculated only for a very small local area, then it could theoretically range in value from 0 % or to 100 % depending on whether the point at which the density was being evaluated lands on the interconnect or the trench. The effective density thus critically depends on the particular window size used for calculating the density.

We define the width of the square which is used for calculating the pattern density as the interaction distance, id. Beyond the interaction distance, the layer pattern is assumed not to affect the density calculation for the point of interest.

Planarization Length

The interaction distance is found to be the same as planarization length. The planarization length is defined graphically in the Figure 8-6. If there is a 100 % density area adjacent to less than 100 % density area, the planarization length is defined as the distance between the end of local planarization in the less-than 100 % region to the beginning of local planarization in the 100 % density region. Thus, any structure that is outside the planarization length would not affect the polishing behavior within the planarization length. The planarization length can be understood in terms of pad bending. As the pad conforms to the different density structures, outside the planarization length, the pad cannot distinguish between the different density regions. The equivalence between planarization length to interaction distance lends physical intuition to the concept of interaction distance.

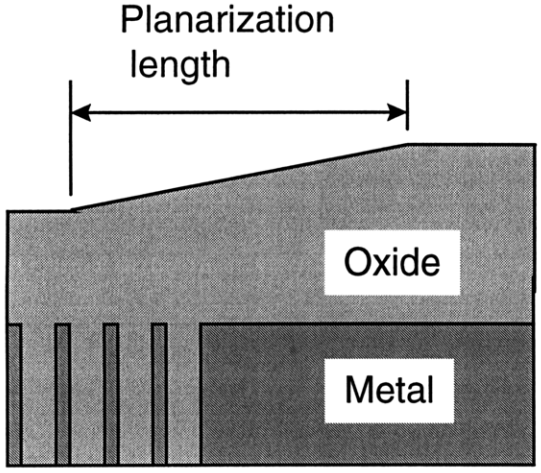


Figure 8-6 Definition of planarization length.

8.2.3 Mathematical Oxide CMP Model

The derivation of a closed-form expression for ILD thickness variation begins with the well known Preston equation[72], which states that the CMP removal rate on blanket films is proportional to the product of pressure and velocity:

$$RR = \frac{dz}{dt} = \kappa P v \qquad \textbf{Equation 8-1}$$

where k is a proportionality constant, P is pressure, and υ is velocity. If the pressure term is represented as F/A, where A is the oxide area contacted by the pad and F is down force, then Preston's equation can be rewritten as:

$$\frac{dz}{dt} = \frac{\kappa F v}{(id)^2 \rho(x, y, z)} \qquad \textbf{Equation 8-2}$$

where the oxide contact area, A has been replaced by a term that contains the density function $\rho(x, y, z)$ and the interaction distance id. The pattern density p is a function of x, y, since density varies across the chip, and it is a function of z since the density can change as oxide is removed. The window size $(id)^2$, multiplied by this pattern density, gives the overall area contacted by the pad. When all the constants are lumped together, the equation can be rewritten as:

$$\frac{dz}{dt} = \frac{K}{\rho(x, y, z)} \qquad \textbf{Equation 8-3}$$

$$K = \frac{\kappa F v}{(id)^2} \qquad \textbf{Equation 8-4}$$

In this case, K can be interpreted as the blanket CMP removal rate.

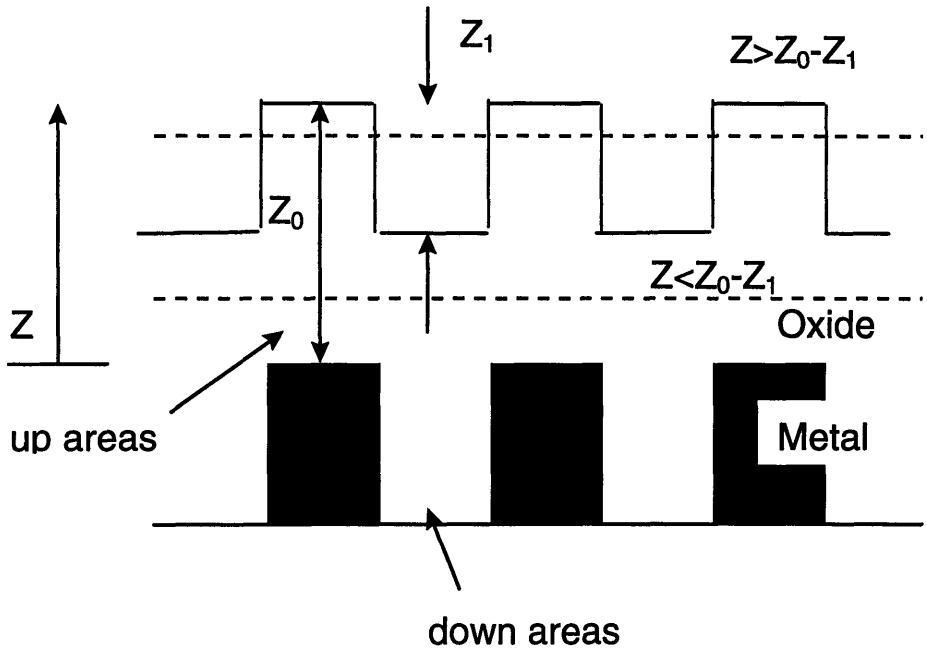


Figure 8-7 Definition of relevant terms for CMP model.

As stated earlier, density is a function of both the depth and the location. If one assumes that the deposition profile closely follows the underlying metal profile, ρ(x,y,z) can be approximated to be in one of two regimes: before achieving local planarity and after achieving local planarity. Before local planarization, the density will depend on the particular (x,y) position, whereas after local planarization, the density value will be 100 %. For an initial oxide step height of z_1, an initial oxide thickness of z_o, and assuming that the deposition profile can be approximated vertically using the underlying metal profile, as shown in Figure 8-7, the pattern density can be expressed as:

$$\rho(x,y,z) = \begin{cases} \rho_o(x,y) & z > z_o - z_1 \\ 1 & z < z_o - z_1 \end{cases} \qquad \textbf{Equation 8-5}$$

In addition, the "down" areas (or regions between the steps) are assumed to polish at a negligible rate compared to the "top" regions (or regions near the top of the steps). Equation 8-3 can be solved for z:

$$z = z_o - \left(\frac{Kt}{\rho_o(x,y)} \right) \qquad Kt < \rho_o(x,y) z_1 \qquad \textbf{Equation 8-6}$$

$$z = z_0 - z_1 - Kt + \rho_0(x,y) z_1 \qquad Kt > \rho_0(x,y) z_1 \qquad \textbf{Equation 8-7}$$

Equation 8-6 implies that if features are planarized for a long enough time (to complete the removal of the local steps), then a linear relationship exists between the layout-pattern density and the ILD thickness. This regime where a linear relationship exists is called the linear regime (Equation 8-7) and the other regime is termed the locally non-planar regime (Equation 8-6). There is a transition time between the locally non-planar regime to the linear regime. This transition time is equal to $\rho z_1/K$ and defines the time, for a given pattern density, required for local planarization to be achieved. Also, it implies that the polishing time to guarantee local planarization over all features is $t = z_1/K$. After this time, no further planarization will occur.

8.2.4 Extraction of Interaction Distance in the Linear Regime

As the pattern density is a function of the interaction distance, it is very important how this parameter is extracted. One technique for obtaining this parameter is to experimentally measure the planarization length by having a test wafer with areas of two different layout densities and polishing them both down to local planarity. The planarization length can then be directly measured. However, this technique suffers from the lack of a suitable and reliable instrument tool for measuring this length. Profilometers or atomic force microscopes for scanning the surface give unreliable data if there exists

any wafer bow or if the required scanning distance is too long. Thus, another method for extracting the interaction distance needs to be developed.

Slope Method for Extracting the Interaction Distance

This method works by first computing the pattern density from the given layout for different interaction distances starting from 2 mm up to some suitably large value. For the density mask, Table 8-1 shows the computed pattern density as a function of interaction distances up to 6 mm for the different sites which were measured. These density value calculations were assisted by customized CAD tools.

site	Exp. po	2	2.5	3	3.5	4	4.5	5	5.5
1	9.84	0.05596	0.175741	0.260778	0.324057	0.372905	0.41172	0.443291	0.469464
2	118.11	0.10552	0.186472	0.239014	0.275846	0.303088	0.324049	0.340676	0.354185
3	112.57	0.19584	0.279463	0.335584	0.375853	0.406155	0.429782	0.448721	0.464241
4	4601.62	0.30936	0.407463	0.472891	0.519638	0.554705	0.581983	0.603809	0.621668
5	5176.2	0.5324	0.552232	0.561299	0.56574	0.567958	0.569023	0.56946	0.569542
6	224.41	0.14548	0.244643	0.30147	0.337515	0.362063	0.379682	0.392849	0.403009
7	2906.1	0.21744	0.215781	0.218877	0.223146	0.227473	0.231505	0.235151	0.238412
8	3920.07	0.30536	0.323356	0.332521	0.337681	0.340793	0.342763	0.344056	0.344927
9	5041.48	0.51	0.534184	0.546253	0.552889	0.55678	0.559163	0.560664	0.561624
10	5629.79	1	0.829556	0.727892	0.661135	0.614273	0.579723	0.55328	0.532435
11	4464.5	0.38368	0.416538	0.446793	0.472493	0.494005	0.512061	0.527342	0.540396
12	4447.87	0.259	0.316203	0.346306	0.363873	0.374898	0.382197	0.387233	0.390823
13	5110.41	0.5036	0.506747	0.510036	0.512967	0.515485	0.517632	0.519469	0.52105
14	5656.57	0.7036	0.710918	0.717349	0.722703	0.727135	0.730828	0.733938	0.736586
15	5866.19	1	0.905974	0.84023	0.791771	0.754608	0.725217	0.701398	0.681708
16	5209.02	0.38368	0.479968	0.538239	0.576961	0.604418	0.624832	0.640572	0.653059
17	5335.2	0.5756	0.566939	0.564578	0.564562	0.565465	0.566709	0.568045	0.569364
18	5729.79	0.7672	0.745002	0.731494	0.722479	0.716063	0.711277	0.707578	0.704637
19	5957.98	0.86	0.86046	0.860078	0.859467	0.858825	0.858216	0.85766	0.85716
20	5973.67	1	0.926083	0.878711	0.845807	0.82164	0.803146	0.788541	0.776717
21	5344.58	0.5916	0.577946	0.570513	0.566022	0.5631	0.561093	0.559654	0.558587
22	5412.87	0.7752	0.683652	0.624466	0.583093	0.552558	0.529101	0.51052	0.495439
23	5704.98	0.896	0.809404	0.751651	0.710388	0.679435	0.655357	0.636092	0.620328
24	5882.35	0.98	0.865991	0.801869	0.761888	0.735085	0.716125	0.702145	0.691492
25	5917.76	1	0.90441	0.834028	0.780495	0.738563	0.704892	0.67729	0.654267

Table 8-1 Computed pattern density as a function of interaction distance.

If all local features have been eroded away ($t>t_t$), then the ILD thickness versus pattern density relationship should be a straight line with a slope of z_1 with respect to density.

$$z = z_0 - z_1 - Kt + \rho_0(x, y)z_1 \qquad \textbf{Equation 8-8}$$

This straight line can be regressed to the measured ILD thickness data as a function of a particular calculated pattern density. By repeating this regression procedure for different values of interaction distance, the regression slope value can be plotted as a function of id. The interaction distance value which yields a slope value closest to the initial step height value, z_1, is then chosen as the optimum interaction distance. As an example, Table 8-2 lists the computed slope of the fitted lines versus different interaction distances. For this example, the optimal choice for id appears to be at about 3.5 mm. For this example, the measured value of z_1 was 0.829 μm.[73]

Interaction Distance (mm)	2.0	2.5	3.0	3.5	4.0	4.5	5.0	5.5	6.0
Slope	0.528	0.636	0.730	0.812	0.885	0.951	1.009	1.062	1.123

Table 8-2 Slope of ILD thickness vs. pattern density across different interaction distances.

R^2 Method [74]

The third method is called the R^2 method. This method also works by first computing the pattern density from the layout for different values of interaction distance starting from 2 mm up to some suitably large value. The ILD thickness as a function of pattern density is plotted for each of the different interaction distances. For each plot, a

linear line is regressed, the R^2 value is calculated, and R^2 as a function of interaction distance is plotted. The interaction distance which gives the highest R^2 value is selected. For the density-mask experiment, Figure 8-8 showing the resulting R^2 vs. interaction distance curve.

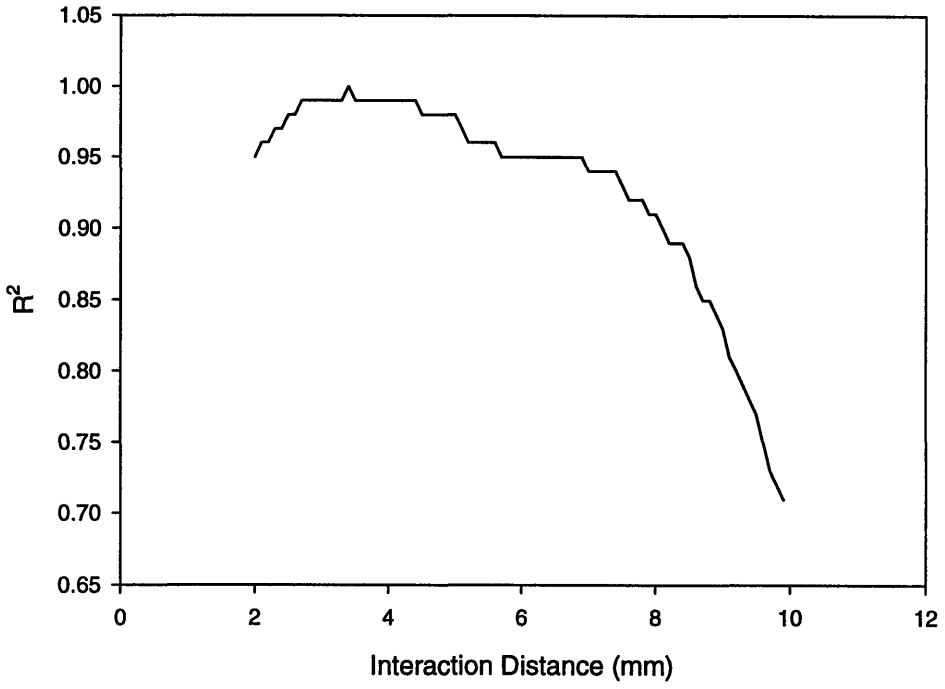


Figure 8-8 Graphical illustration of R^2 method for extracting the interaction distance from the planarized dielectric-layer thicknesses.

8.2.5 Extraction of Interaction Distance in the Non-Linear Regime

It is often advantageous to extract the interaction distance from test structures before local planarization is reached. As there sometimes is no metal layer underneath the dielectric layer being polished, the pattern-recognition mark for optical interferometry

will not be recognizable once local planarity is achieved. Without this pattern recognition mark, measurement of the final ILD thickness is difficult. Thus, the interaction distance must be extracted for the regime $Kt < \rho(x,y)z_1$. We start with the equation:

$$z = z_0 - \left(\frac{Kt}{\rho_0(x, y)} \right) \qquad \textbf{Equation 8-9}$$

which describes the regime before local planarization. This can be converted into:

$$-Kt = (z - z_0)\rho_0(x, y) \qquad \textbf{Equation 8-10}$$

$$\rho_0(x, y) = \frac{Kt}{z_0 - Z} \qquad \textbf{Equation 8-11}$$

where z is the final ILD thickness, Z_0 is initial thickness, K is blanket removal rate, and t is the polish time. Using these known parameters, the effective density ρ can be calculated for each density structure on the mask. Then these values are compared to the effective densities calculated using different interaction distance values. The plot which gives the slope of 1 (or a direct correspondence between extracted values from the layout and experimentally extracted values) will determine the appropriate interaction distance for the process as shown in Figure 8-9.

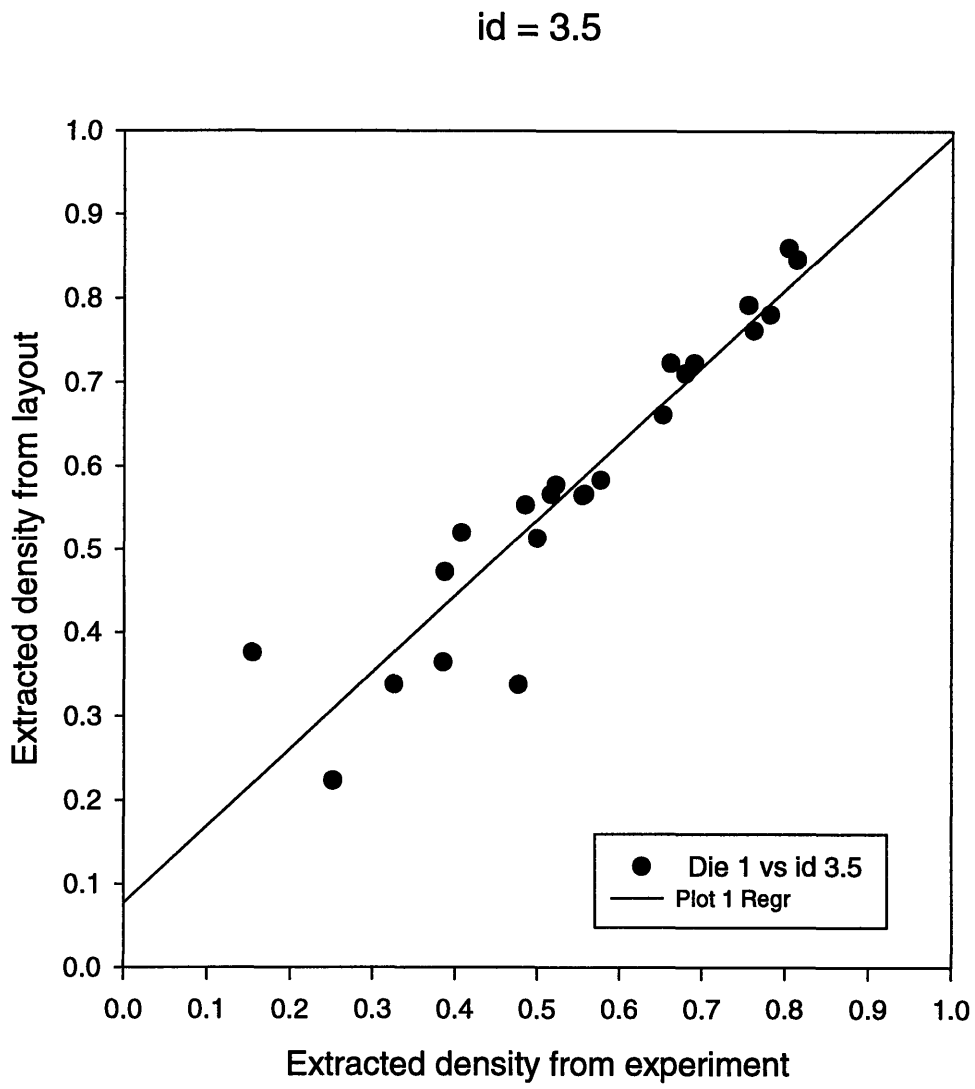


Figure 8-9 Slope method for finding the interaction distance. The interaction distance is extracted by finding the set of density values that gives the slope closest to a unity for the fitted line when plotting the actual ILD thicknesses as a function of density.

Another method to determine the optimum value of id is to calculate the variance based on the following equation:

$$S = \sum_{i=1}^{25} (\rho_{i0} - \rho_{i\exp})^2 \qquad \textbf{Equation 8-12}$$

where ρ_{i0} is extracted layout density, and ρ_{iexp} is extracted density from experiment. When S is plotted versus interaction distance, whatever value of interaction distance that gives the lowest s value is selected as the interaction distance. This particular value is generally easier to determine than finding the interaction distance that gives the closest fit to the slope of one. Thus, for the remainder of the thesis, this methodology will be utilized to extract the interaction distance. Figure 8-10 shows an example of finding the interaction distance using this method.

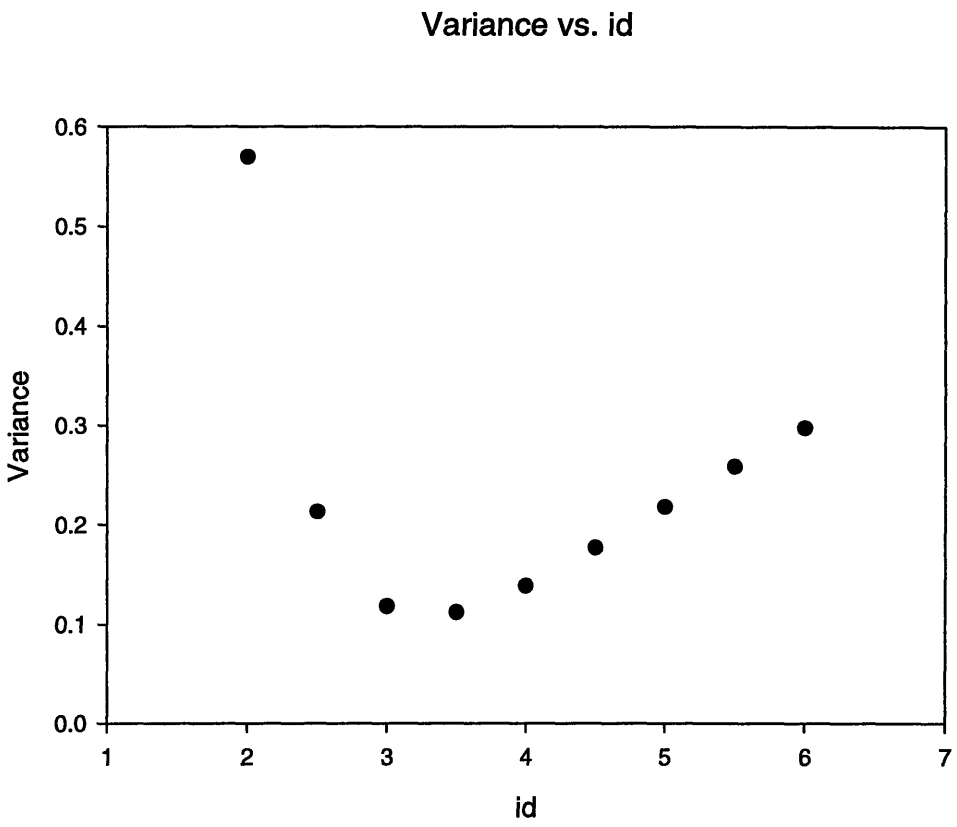


Figure 8-10 Variance method for finding the interaction distance. The interaction distance is extracted by finding the interaction distance that produces the smallest variance value.

9. Nitride/STI CMP Characterization

9.1 Nitride CMP

Materials Dependence of the Blanket Polish Rate

Blanket nitride film and blanket oxide films were polished under the same process conditions. A down force of 2.5 psi, a table speed of 35 rpm and a quill speed of 35 rpm were used. The test wafers were polished for different times to check if the polish rate changed over time. Figure 9-1 shows the polish rate vs polish time. There is a noticeable drop in the polish rate during the first 15 seconds of polish, after which the rate stabilizes. The polish rate of nitride is much slower than that of oxide. The polish rate of nitride was determined to be 0.65 nm/s while the polish rate of oxide was observed to be 2.2 nm/s.

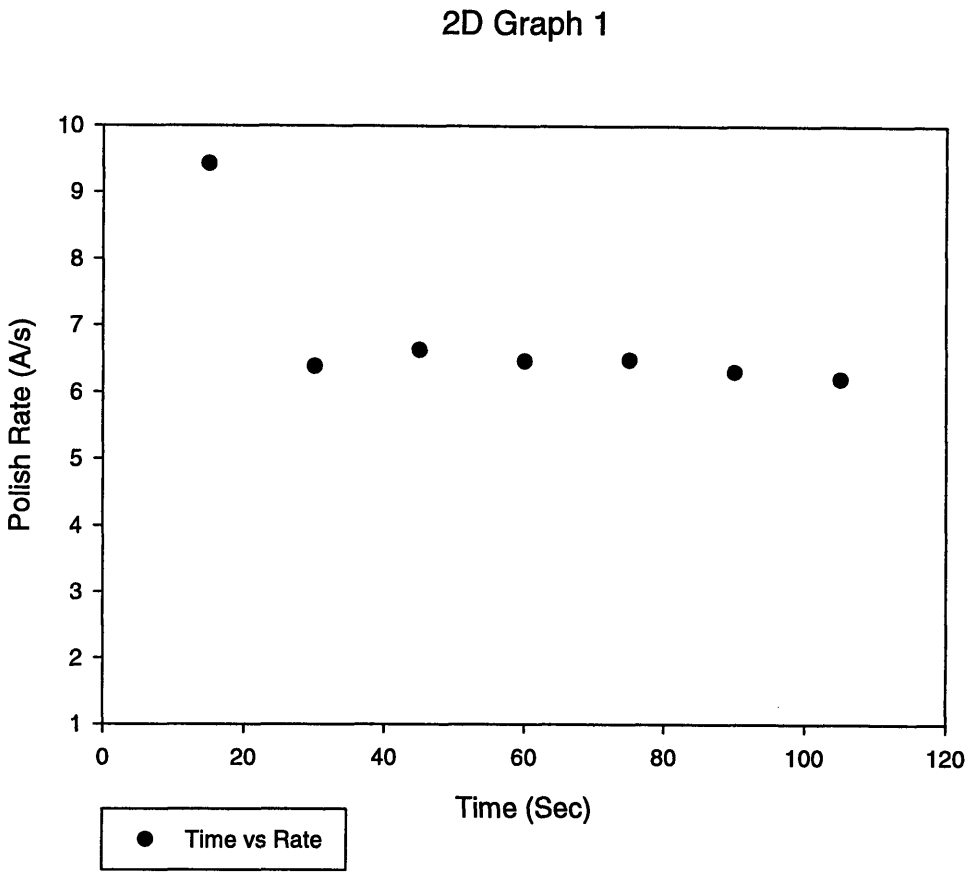


Figure 9-1 Polish rate vs. time for nitride CMP using oxide slurry. The polish rate starts decreases asymptotically to a stable value.

Profile of the Initial Nitride Test Structure

Profilometer traces before CMP showed that the structures to be polished had profiles very similar to the initial as-drawn dimensions. The nitride steps were very clearly defined. Figure 9-2 shows a trace for a 50 % density structure at the center block of a die in the middle of the wafer.

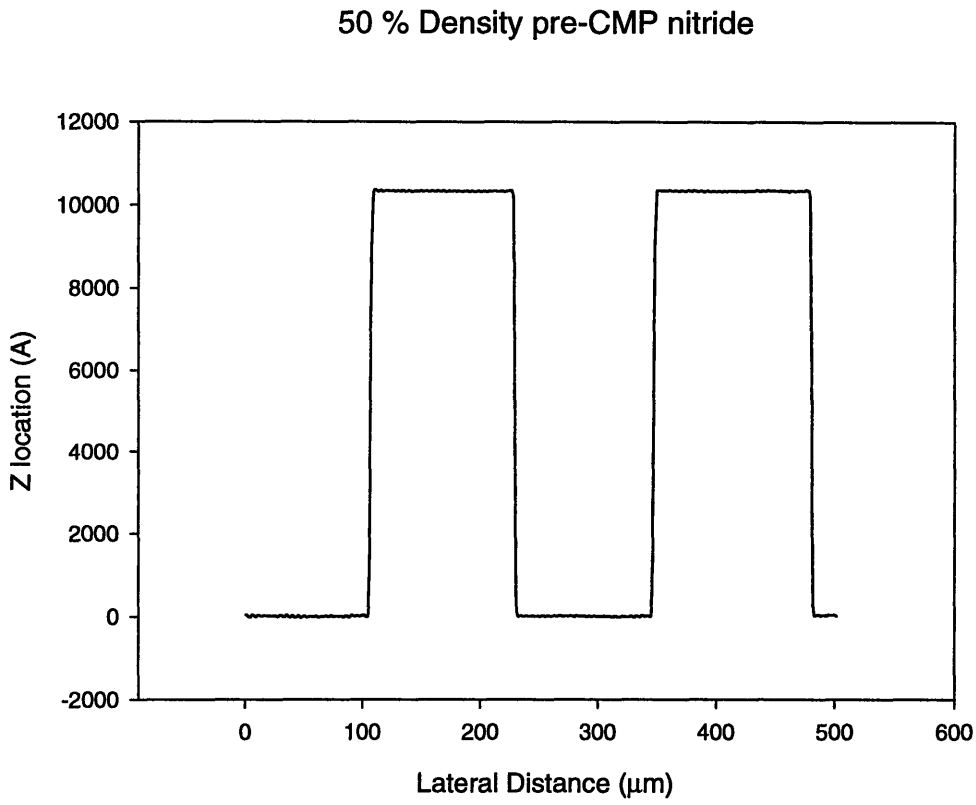


Figure 9-2 Profile of the pre-CMP 50 %-density nitride structure. Note that the edges are sharply defined.

Figure 9-3 shows a trace of the same structure after it had been polished for 167 seconds. Noticeable edge-rounding of the nitride steps can be observed. The effective density seen by the pad at the end of the polish is smaller than the initial density at the beginning of the polish. Thus, the polish rate should increase as edge-rounding continues. However, the change in the effective density is small enough to allow use of a constant density value for the interaction distance extraction. This edge-rounding effect is observed to be stronger at lower-density structures than at higher-density structures as

shown in Figure 9-4. Also, observe that in Figure 9-3, the step-height is slightly actually larger than the initial before-CMP height because the KOH-based slurry etched away the down areas where silicon was exposed. The step-height is smaller than the initial before-CMP height in Figure 9-4 because of the reduction in the nitride pillar height due to their lower effective density.

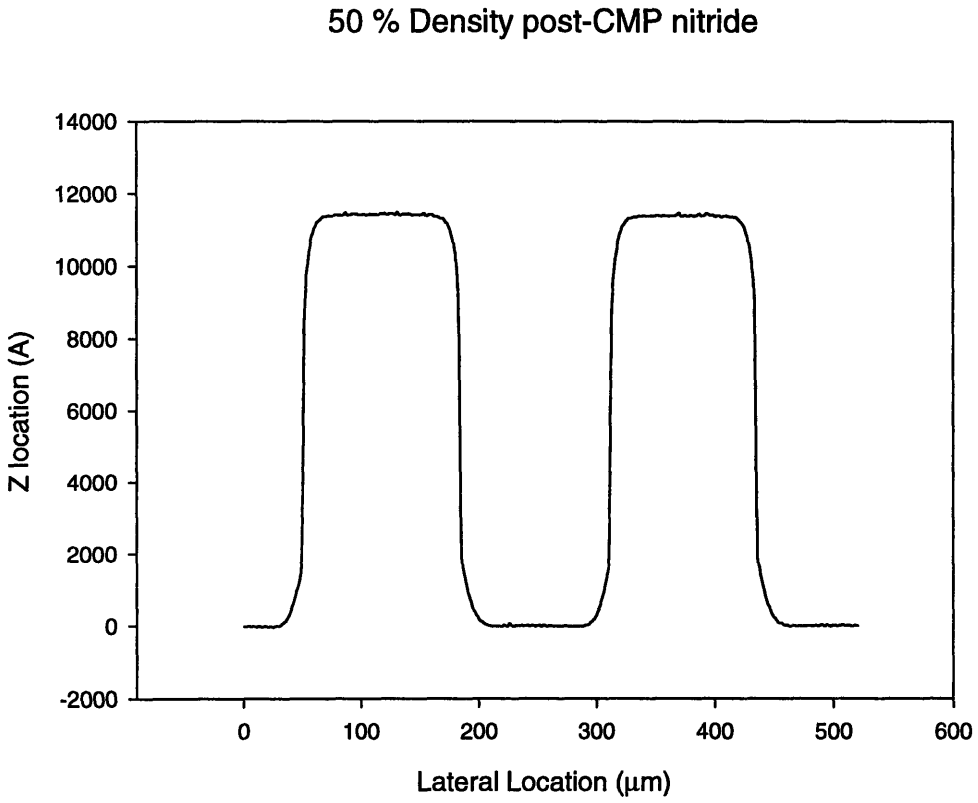


Figure 9-3 Profile of the post-CMP 50%-density nitride structure. Because KOH etched away a portion of the exposed silicon region, planarization has not been achieved.

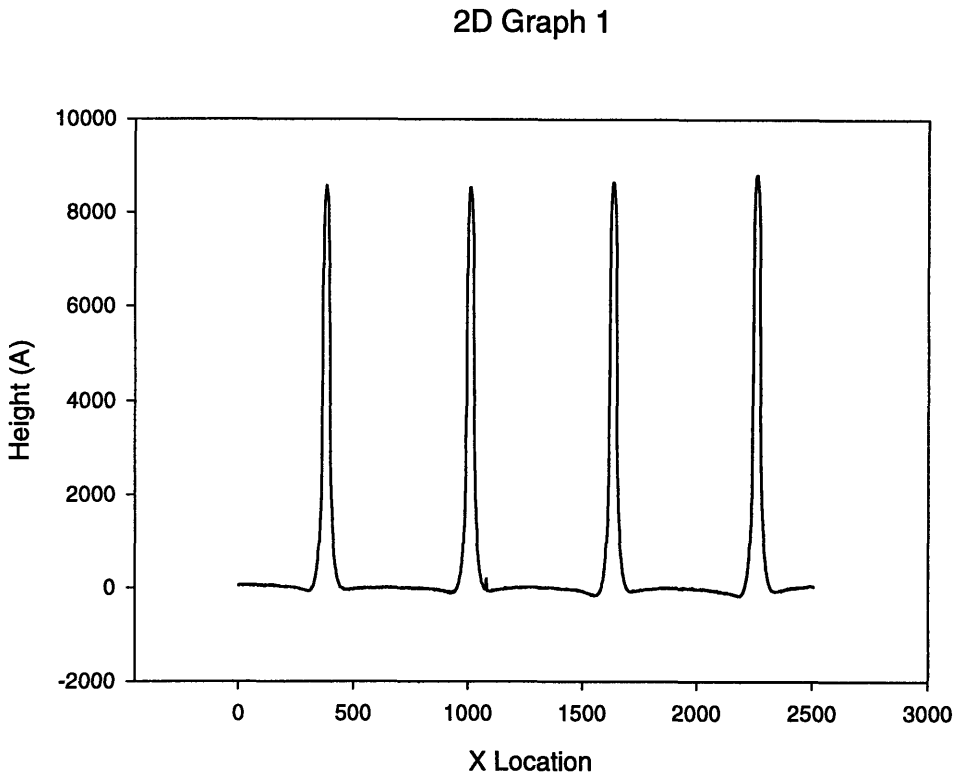


Figure 9-4 Profile of the post-CMP 4%-density nitride structure. This is still in the non-linear polishing regime

Extraction of the Nitride and Oxide Interaction Distance

Using the extraction method described in Section 8.2.5 for the non-linear regime, the interaction distance was calculated. For this particular process, 3.5 mm was determined to be the optimum interaction distance. Oxide CMP results, under the same process conditions, yielded the same interaction distance of 3.5 mm. This similarity shows that the model, which only accounts for the mechanical component of polishing, describes the actual nitride and oxide polishing characteristics very well.

9.2 STI CMP

Profile of the STI Test Structure in the Oxide Phase

Profilometer traces before CMP showed that the STI test structure to be polished had profiles very similar to the initial as-drawn mask dimensions. Figure 9-5 shows a trace of a test structure after it had been polished for 167 seconds. Both the pillars and trenches are oxide; nitride pillars underneath oxide has not been exposed by polishing yet. Noticeable edge-rounding is observed for each of the steps. The effective density seen by the pad at the end of the polish is smaller than the initial density at the beginning of the polish. Thus, the polish rate should increase as the edge-rounding continues. The oxide CMP model can be used to predict the time required to polish through the oxide and to hit the nitride polish stops for a given density and a thickness:

$$z = z_0 - z_1 - Kt\rho_0(x, y)z_1 \qquad \textbf{Equation 9-1}$$

$$0 = z_0 - z_1 - Kt\rho_0(x, y)z_1 \qquad \textbf{Equation 9-2}$$

$$t = \frac{z_0 - z_1}{\rho_0(x, y)K_0} \qquad \textbf{Equation 9-3}$$

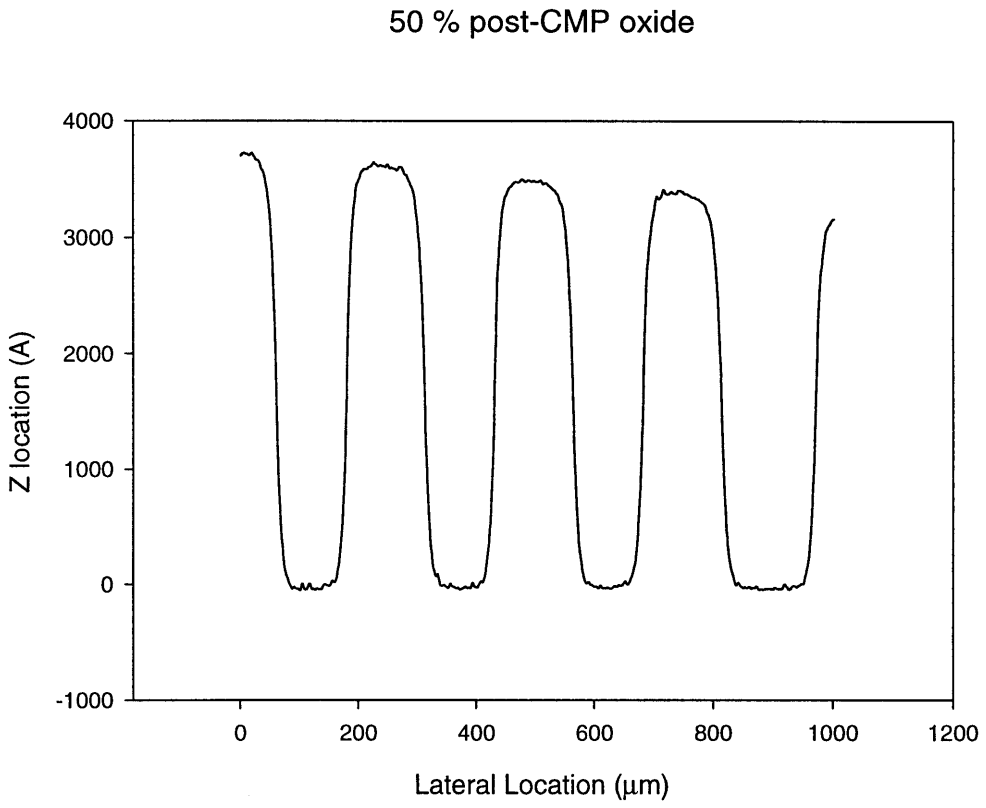


Figure 9-5 Profile of the post-CMP oxide structure. Both pillars and trenches are oxide.

Profile of Structure in the Nitride Phase

Once nitride pillars in the STI structure have been exposed to the pad, it is expected that these nitride pillars due to their slower polish rate, should limit or halt the oxide polish rate. However, several distinguishing features not evident for single-material polishing, are present in this dual-material STI structure. There is the phenomenon of dishing, which appears as a recession of the softer oxide region between the hard nitride regions. There is also the phenomenon of erosion, which appears as the reduced nitride

step height in a lower- density region compared to a higher-density area. Both "dishing" and "erosion" are illustrated in the Figure 9-6.

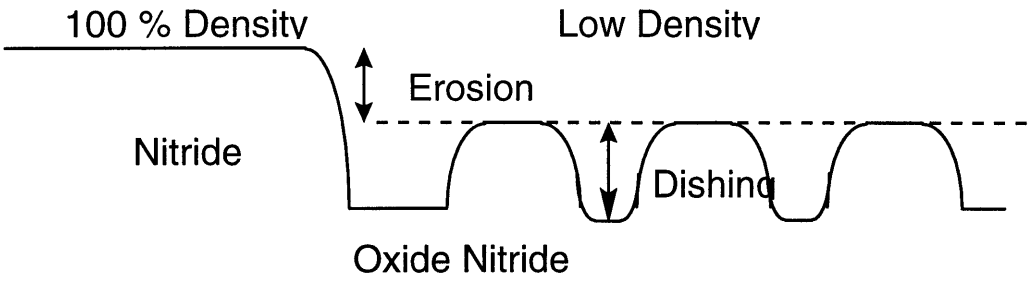


Figure 9-6 Definition of dishing and erosion

Dishing in the Oxide Region

Figure 9-7 shows the profile of the nitride and oxide regions for a 50 % density structure after a 1000 second polish. After the nitride polish-stop has been reached, the up areas are nitride pillars and the down areas are oxide regions. The difference in height between the oxide trenches and nitride pillars is the amount of effective dishing. There are significant "dishing" effects very evident in this profile. The oxide regions between each nitride pillars are now recessed. For an ideal CMP process, the oxide region should have stayed at the same level as the nitride pillars, which acted as the polish stop.

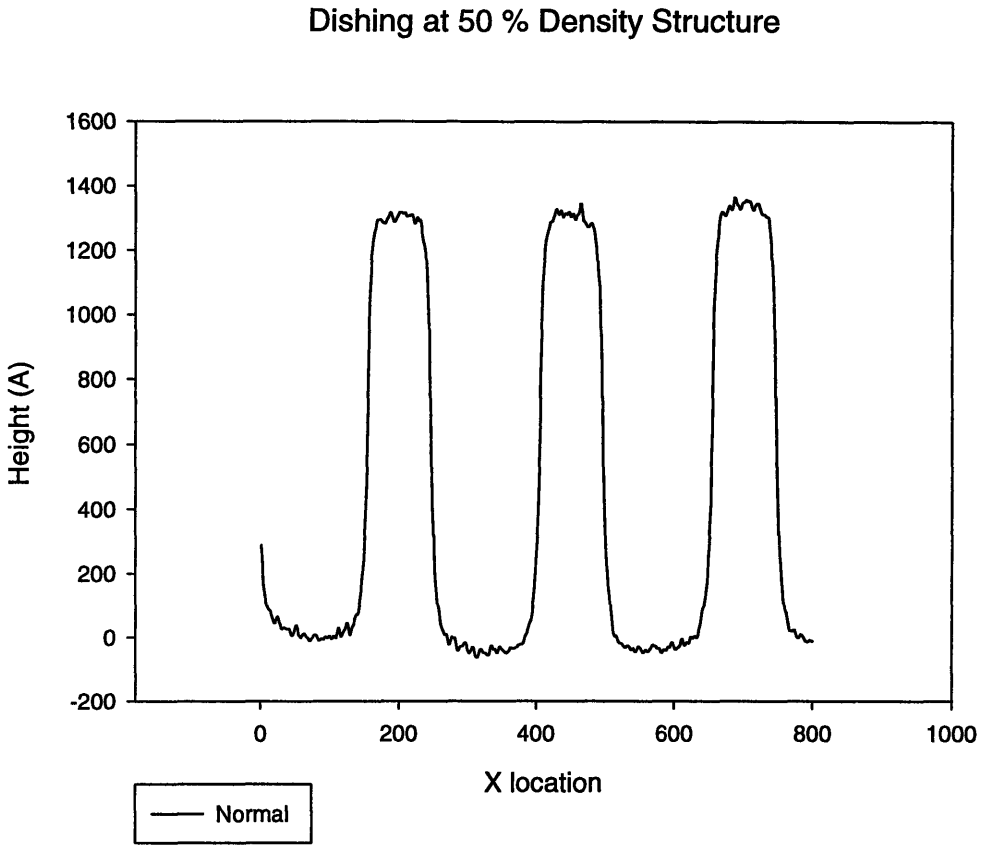


Figure 9-7 Profile of the nitride and oxide structures at 50 % density after the nitride has been exposed. This regime is called over-polish.

This oxide dishing is found to depend on both the oxide-region width and the nitride density. Figure 9-8 shows that the amount of oxide dishing increases with increasing oxide-region width. Figure 9-9 shows that dishing decreases with increasing nitride density. Thus, the increasing oxide width and the nitride density have opposite effects on the dishing behavior of the oxide regions in STI structures.

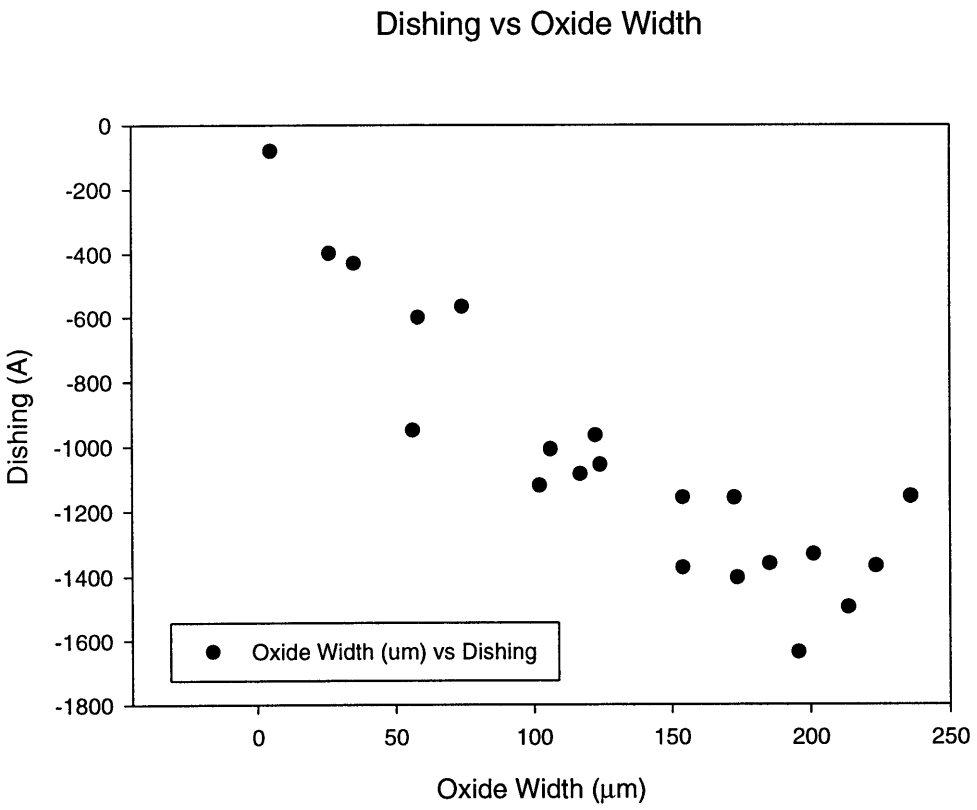


Figure 9-8 Dishing of oxide vs. oxide width.

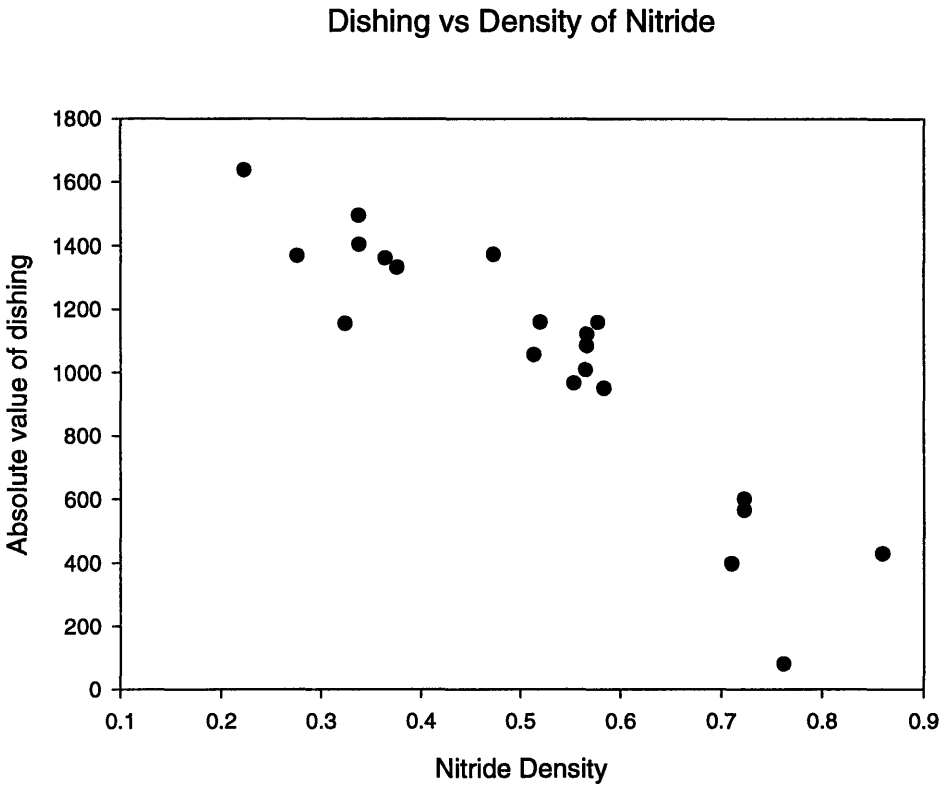


Figure 9-9 Dishing of oxide vs. effective density of nitride

STI Oxide-Region Dishing Model

Several assumptions must be made in order to model the oxide dishing in STI structures. These assumptions are graphically illustrated in the Figure 9-10.

1. The oxide polish rate is assumed to depend upon the oxide width and the amount of dishing (Figure 9-10 a) and b)). As the oxide width increases, the initial polish rate will increase eventually reaching the blanket oxide polish rate at infinite oxide width. As dishing continues, the oxide polish rate will decrease eventually reaching the chemical

oxide polish rate. If K_o is the blanket oxide polish rate, k_dK_o will be the polish rate of oxide in the trenches, where k_d is a function of both the oxide width and the amount of dishing.

2. Erosion is purely due to the pattern-density dependence of the nitride polish stops. As nitride has a much slower polish rate than oxide, it is a good assumption that oxide does not play a role in contributing to erosion. The nitride polish rate is governed by the effective nitride density and can be expressed as by K_n/ρ_n, where K_n is blanket nitride polish rate and ρ_n is effective density of the nitride.

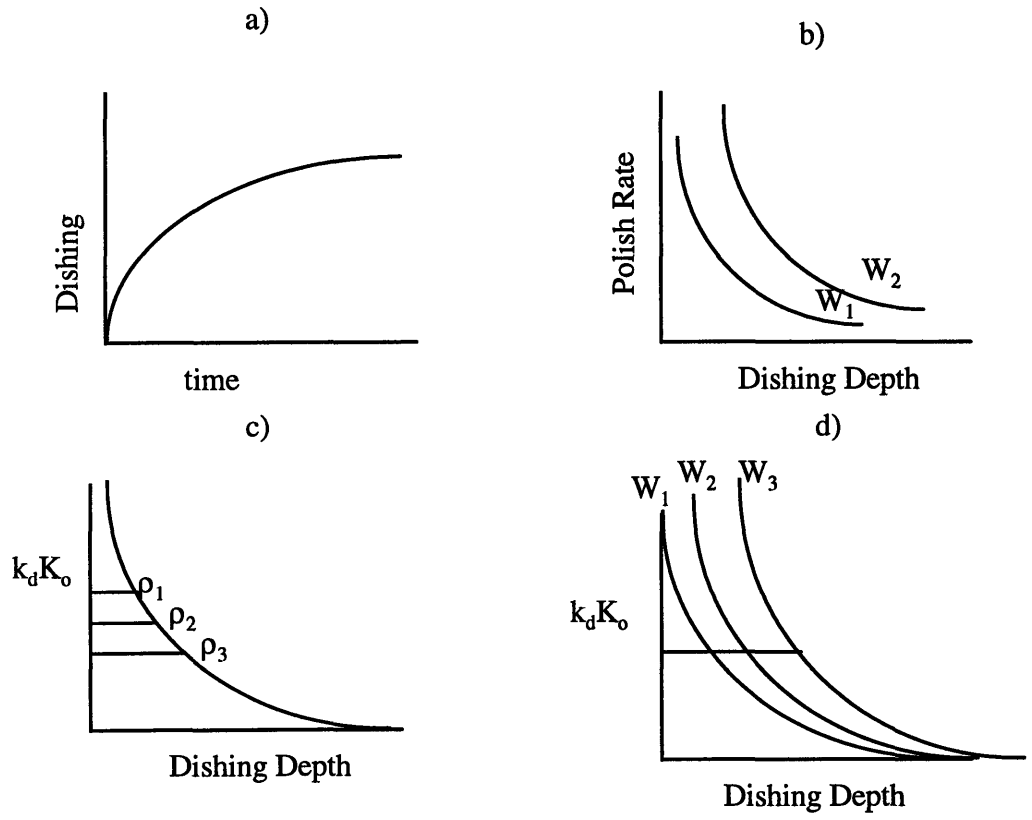


Figure 9-10 Assumptions and predictions of the STI CMP model. A) Maximum dishing depth depends on the time. B) Polish rate changes with dishing depth and oxide width. C) For a given oxide width, the dishing depth will depend only on the nitride density. D) For a given nitride density, the dishing depth will depend only on the oxide width.

At the start of dishing, the polish rate of the oxide region is much faster than the polish rate of the nitride because of the shallow dishing depth (Figure 9-10 b). As the dishing progresses, the oxide-region polish rate decreases and eventually reaches equilibrium with the nitride polish rate which determines the amount of erosion. This equilibrium is reached when

$$k_d K_O = \frac{K_N}{\rho_N} \qquad \textbf{Equation 9-4}$$

where $k_d K_o$ is oxide-trench polish rate and K_N/ρ_N is nitride-pillar polish rate. ρ_N is effective nitride density. For a given density, the nitride polish rate will be fixed by the nitride density while the oxide polish rate will change with the amount of effective dishing. Dishing will continue until it reaches the amount of dishing at which the oxide-trench polish rate is at steady-state with nitride-pillar polish rate.

Based on this model, the following prediction can be made: for the same oxide width, the amount of effective dishing will depend on the particular nitride density (Figure 9-10 c). The oxide-region polish rate will depend on the amount of dishing that has already occurred, whereas the nitride-pillar polish rate will depend solely on the effective nitride density. As the nitride density increases, the nitride-pillar polish rate decreases. Thus, the corresponding equilibrium oxide-trench polish rate will be reached only at a greater amount of dishing. Thus, increasing the nitride density will result in an increased amount of dishing because steady state between the nitride and oxide polish rates is achieved at deeper oxide depth. Figure 9 -11 shows the correlation between the amount of dishing and the nitride density for a constant oxide width. The nitride density is calculated using an interaction distance of 3.5 mm, which comes from the bulk nitride

polish experiments. As predicted, the amount of dishing increases with increasing nitride density. Figure 9-12 shows a profilometer trace over the region where the oxide width was constant but the effective nitride density changed.

Another prediction that follows is that for a given nitride density, the amount of dishing will depend on the particular oxide width (Figure 9-10 d). Figure 9-10 d) shows oxide-polish rate vs. the amount of dishing curves for three different oxide widths. The nitride-pillar polish rate is fixed by the nitride density. So, the point at which the steady-state oxide and nitride-region polish rate is reached depends on the particular oxide width.

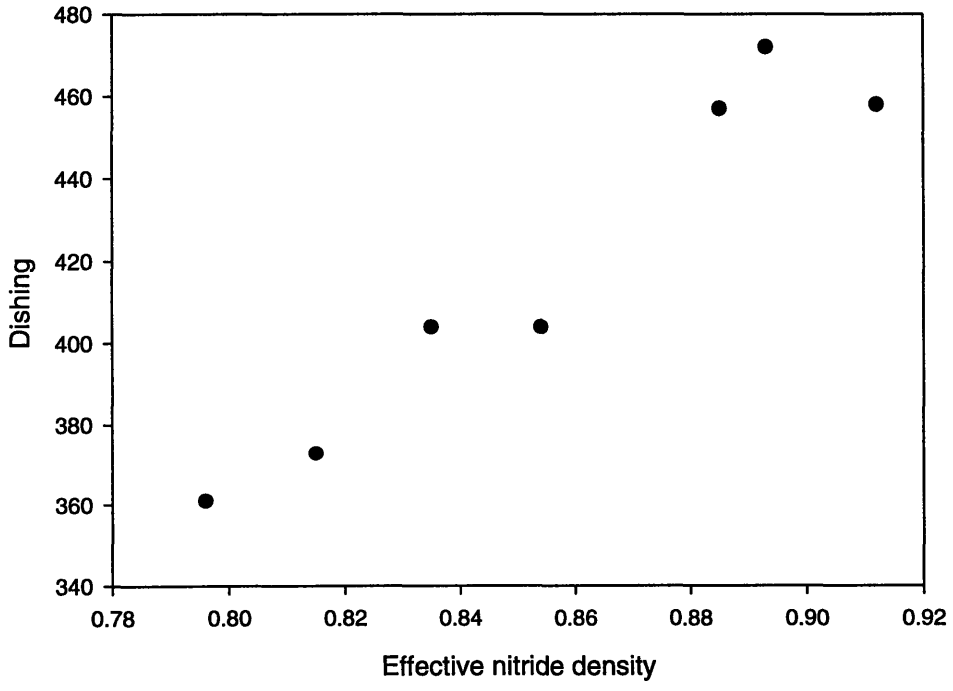


Figure 9-11 Dishing of oxide vs. density of nitride at a constant oxide width. The density of nitride does affect the dishing as expected.

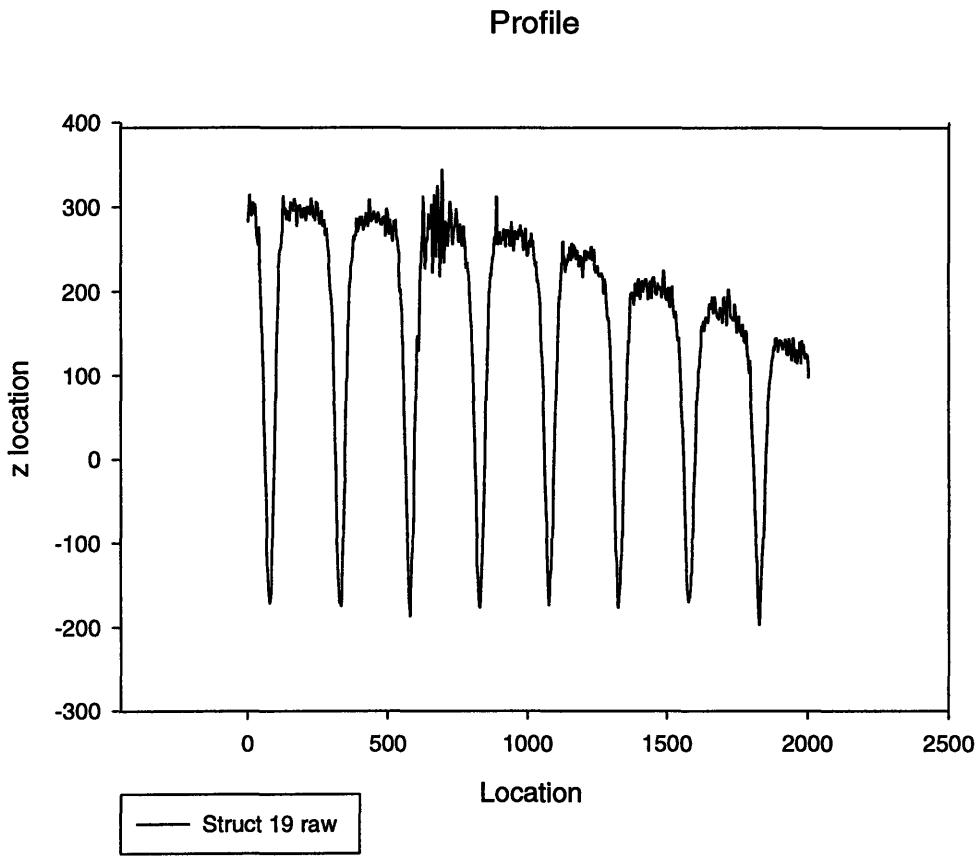


Figure 9-12 Dishing profile of the oxide region: each trench has the same oxide width but a different nitride density, which is calculated using 3.5 mm as the interaction distance. As the density decreases, the observed amount of dishing decreases even though the oxide width remains the same.

If extended to other two-material polish systems, the developed model can explain the discrepancies seen by previous research on tungsten and oxide CMP. Elbel et al.[75] have reported constant dishing over time in tungsten polish while Kranenburg and Woerlee[76] have reported increased dishing with overpolish. Over-polish refers to continuing to polish of the sample even after the polish-stop layer has been exposed.

The discrepancy between the two studied can be explained by the conjecture that dishing will increase with time until steady-state exists between the tungsten-region polish rate and the oxide-region polish rate is achieved. Initially, the tungsten polish rate

will be faster than oxide polish rate, causing dishing. However, the amount of dishing will remain constant with time once steady-state between the oxide and tungsten polish rate has been achieved. As the oxide and tungsten polish rates are closely tied to the selectivity and polish rate of the slurry, differences in the choice of slurry will determine the time to reach the steady-state point. Kranenbrug and Woerlee can be considered then to have not achieved this steady-state in their experimental system, whereas Elbel et. al had in their experimental setup.

9.3 Conclusion

Nitride CMP experiments show that the semi-empirical model developed for oxide CMP can also be used to describe nitride CMP. The extracted interaction distance for nitride CMP is the same as that for oxide CMP, showing that the mechanical polishing component is the dominant effect for polishing these materials. Dishing of oxide in the STI structure has been investigated and a qualitative model has been developed to describe the resulting dishing dependence on nitride density and oxide width. This model also explains that the different oxide dishing-dependences on density found by different researchers do not actually contradict each other, but rather are consistent.

10. Conclusion

Metrology on SIMOX buried oxide and Nitride/STI CMP has been carried out to gain more insight into materials systems and processes. Physical defects in the SIMOX buried oxide have been characterized and their impact on conduction characteristics investigated. Greater understanding about the excess-silicon related defects in the buried oxide has been gained concerning their nature, origin, and impact on the conduction characteristics. Further understanding about the silicon islands in the buried oxide has also been gained concerning their formation and impact on the high-field conduction characteristics. Nitride and STI CMP processes have also been characterized. The materials dependence of the CMP process and the dishing and erosion characteristics of STI structures have been investigated.

10.1 SIMOX Buried Oxide

Using electron spin resonance measurements and test samples with artificially-introduced silicon defects in the buried oxide, it has been shown that "amorphous silicon" clusters are not present in standard single-implant SIMOX buried oxide. A kinetic model has been developed to explain the existence of excess-silicon-related BOX defects and their distribution in the buried oxide. Experiments have also been carried out to show the effect that this excess silicon has on the BOX high-field conduction characteristics, particularly on electron injection from the top silicon layer. A quantum-mechanical model has been used to study how the barrier shape for electron tunneling from the top-silicon layer into buried oxide, which dictates the high-field conduction behavior, depends on the BOX oxygen-vacancy defects.

Using samples with different process backgrounds, buried-oxide growth through silicon self-interstitial generation and a BOX formation model explaining the location and shape of silicon islands has been proposed. The effect of BOX silicon islands on electron injection from the substrate has also been studied. It is shown that BOX non-stoichiometry, which had a major effect on electron injection from the top-silicon layer, does not affect BOX conduction from the substrate. The existing conduction model has been revised to accommodate these new findings. Correlation between the observed BOX silicon-island density and the extracted model parameter for the effective electron injection area has also been demonstrated.

10.2 Nitride/STI CMP

Nitride CMP experiments show that the semi-empirical model developed for oxide can also be used to described nitride CMP. The interaction distance for nitride CMP is observed to be the same as that for oxide CMP, showing that the mechanical polishing component is dominant effect in polishing these structures. Dishing of oxide in STI structures has also been investigated and a qualitative model has been developed to describe the resulting dependence of dishing on density. This model explains how the oxide width and nitride pattern density affect the polishing and dishing behavior of STI structures. If extended to other dual-material systems, this model explains that apparent discrepancies seen by other researchers on tungsten/oxide CMP are actually consistent, not contradictory.

10.3 Future Work

10.3.1 SIMOX Buried Oxide

In this thesis, a metrology technique based on a high-field conduction model has been developed and used in conjunction with physical characterization techniques to better understand the defects in the standard single-implant SIMOX buried oxide and their impact on the BOX high-field conduction characteristics. Future work will involve looking at how the defects identified and characterized in this thesis affect the reliability and quality of devices fabricated on the top-silicon layer.

Another area for future work is in studying new types of SIMOX substrates that are coming into the market. Much research is being carried out to decrease the price of SIMOX substrates through reduction in the oxygen dose needed to create a continuous buried-oxide layer. It would be beneficial to investigate how the knowledge gained on high-dose high-energy single-implant SIMOX buried oxide can be applied to low-dose low-energy single-implant SIMOX buried oxide.

10.3.2 Shallow Trench Isolation CMP

In this thesis, the metrology and modeling techniques for oxide CMP are extended to nitride and STI CMP in order to understand the pattern-density and materials dependence for these particular CMP processes. Future work will involve developing mathematical model for dishing and erosion in STI structures based on the qualitative model proposed in this thesis. Development of characterization masks for STI CMP and a corresponding quantitative model will be beneficial to help reduce the extent of dishing and erosion in STI structures. Investigation of the circuit-impact of dishing and erosion in

STI structures is another area where a major impact on increasing the process yield can be gained.

Appendix A.

Simulation Programs (MEDICI)

```
**********Main Program **********

MESH IN.FILE =md=90nm.m
CONTACT NUM=1 N.POLYSI
CONTACT NUM=2 N.POLYSI
CONTACT NUM=3 N.POLYSI

COMMENT Set V(top)=voltage
SYMB GUMMEL CARRIERS=2
METHOD N.DAMP
SOLVE V1=55 V2=0 V3=7.55
SOLVE OUT.FILE=Ed=90nm.sln

**********End of Main Program **********
**********Program for Generating Mesh**********

MESH RECTANGU SMOOTH.K=2 OUT.FILE=md=90nm.m
X.MESH LOCATION=0.0 SPACING=0.1
X.MESH LOCATION=0.48 SPACING=0.0011 SUMMARY
X.MESH LOCATION=.489 SPACING=0.0011
X.MESH LOCATION=.511 SPACING=.0011 SUMMARY
X.MESH LOCATION=0.52 SPACING=.0011
X.MESH LOCATION=1 SPACING=0.1 SUMMARY
Y.MESH DEPTH=.2 H1=.1
Y.MESH DEPTH=.08 N.SPACES=2
Y.MESH DEPTH=.031 N.SPACES=31
Y.MESH DEPTH=.2 H1=.1

COMMENT Specify Oxide and Silicon regions

REGION POLYSILI NUMBER=1 Y.MIN=0 Y.MAX=.2
COMMENT Tbox
REGION OXIDE NUMBER=2 Y.MIN=.2 Y.MAX=.311

COMMENT Silicon island body
COMMENT Tbox, IsleSize
REGION POLYSILI NUMBER=3 X.MIN=.4945 X.MAX=.5055 Y.MIN=.29 Y.MAX=.301

REGION POLYSILI NUMBER=4 Y.MIN=.311

COMMENT Electrodes: 1=Gate, 2=Substrate
ELECTRODE NUMBER=1 REGION=1
ELECTRODE NUMBER=2 REGION=4
ELECTRODE NUMBER=3 REGION=3
```

```
COMMENT Specify impurity profile
PLOT.2D GRID SCALE FILL

**********End of Program for Generating Mesh**********
```

Appendix B: Process Flow for SIMOX BOXCAPs

1. Screening Oxide
   48 nm dry oxide
2. Ion Implantation
   Top Si thickness = 1800 - 2200 A
   Element = BF2
   Dose = 1x 10^{16} cm^{-2}
   Energy = 40 keV
3. Wet Screening Oxide Etch
   DI rinse and BOE dip until dewet
4. Pattern Silicon Electrode
   HMDS - Prime
   Resist - Coat
   Stepper - Expose
   Develop
   Inspect
5. BOE Dip
   10 seconds
6. Silicon Plasma Etch
   etch rate ~ 5 nm/sec
7. Resist Ash
8. Nitrogen Anneal
   Temperature = 950 °C
   Time = 80 min
9. BOE Dip
   10 seconds

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