

## XV. NONLINEAR CIRCUITS

Prof. E. A. Guillemin  
Prof. S. J. Mason  
Prof. R. E. Scott  
Prof. H. J. Zimmermann

N. DeClaris  
L. W. Massey

R. I. Morganstern  
G. S. Sebestyen  
T. E. Stern  
R. D. Thornton

### RESEARCH OBJECTIVES

The work reported in this section includes continuations of studies that were designated as Analog Computer Research in previous Quarterly Progress Reports. The new heading for this research seems more appropriate, since the efforts of the group are directed largely toward general nonlinear circuit analysis and synthesis problems. Some of the studies do apply to analog computers but also have broader implications. The group has been augmented by several new staff members, and a number of new studies are under way.

Resistive diode circuits are being studied to determine general properties and methods of synthesis.

H. J. Zimmermann

### A. DIODE CIRCUIT CHARACTERISTICS

In the Quarterly Progress Report, July 15, 1954 (p. 86), a new algebraic symbolism was described by Stern. It is an algebra that provides a concise mathematical representation of piecewise-linear networks; it was applied to the synthesis of driving-point resistances and transfer functions of diode circuits.

This investigation bears on the same subject but is concerned only with the general properties of the driving-point resistances of piecewise-linear networks containing no storage elements. Realizability criteria are discussed, with special emphasis on realizability with the theoretically established minimum number of components. No rigorous proofs will be presented unless they are of interest.

Definition I: The state of a diode will be denoted by "1" if the diode is conducting; by "0" if it is not conducting.

Definition II: The state of a network will be defined as the condition in which the state of all its diodes is uniquely specified. For example, state 100110 means that the network contains 6 diodes with the first, fourth, and fifth diodes closed and the others open.

Definition III: As the input variable (input voltage  $E_{in}$ , for example) of a network is increased from  $-\infty$  to  $+\infty$ , the network assumes a succession of states. This succession of states will be called a "code."

THEOREM I: "The input-resistance ( $E_{in}$  vs.  $I_{in}$ ) or input-conductance ( $I_{in}$  vs.  $E_{in}$ ) curve of a network consisting of diodes, resistances, and constant voltage and current sources is a monotonically increasing function."

This is intuitively obvious, since, regardless of whether the diodes in the network are open or closed, we see a positive resistance when looking into any terminal pair of the type of network specified above.

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THEOREM II: "The maximum number of states a network can have is  $2^n$ , where  $n$  is the number of diodes in the network."

This follows, since each of the  $n$  diodes may assume only one of two mutually exclusive states: open or closed. This is true for all piecewise-linear networks, including those that have negative resistances and linear amplifiers in them.

THEOREM III: "The driving-point resistance, conductance, or transfer function of a piecewise-linear network containing  $n$  diodes can have a maximum of  $2^n$  linear regions."

This theorem is not identical with Theorem II, for the latter merely states that the maximum number of states is  $2^n$ , but does not preclude the same state occurring more than once; that is, according to Theorem III, a state can occur in only one range of the input variable. In more concise form, Theorem III states that the code of a network can consist of a maximum of  $2^n$  states. The proof of this is of interest.

Proof (advanced by Prof. S. J. Mason): Assume a network containing  $n$  diodes. This network can be represented by a box with the input terminal pair and the terminals of all the diodes brought outside, as shown in Fig. XV-1. In any specified state  $S$  (state 1001...1 in this example), all of the diode currents and voltages are always positive because the reference convention indicates as positive the forward currents of conducting diodes and the reverse voltages of open diodes. Let us say that we plot  $X_m$  vs.  $E_{in}$ , where  $X_m$  is either a forward current of a closed diode or a reverse voltage of an open diode. In the example given above,  $X_1 = i_1$ ,  $X_2 = e_2$ ,  $X_3 = e_3$ , ...,  $X_n = i_n$ . Since the network in any one state is linear (and stable), the  $X_m$  vs.  $E_{in}$  curves will be straight lines (see Fig. XV-2). It is clear that as either a diode forward current or a diode reverse voltage tends to become negative, a break point occurs and the state  $S$  for which the  $X_m$  vs.  $E_{in}$  curves were plotted in Fig. XV-2 is terminated. The region in which the specified state  $S$  can exist, therefore, is the region in which all  $X$ 's are positive. Since the  $X_m$  vs.  $E_{in}$  curves are straight lines, there is only one such region.

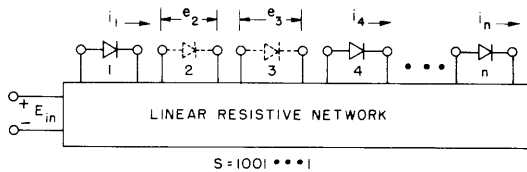


Fig. XV-1

Piecewise linear resistive network.

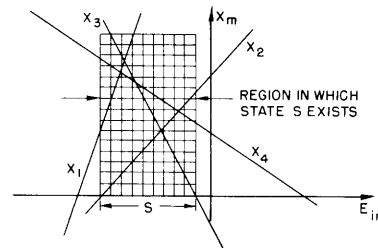


Fig. XV-2

Transfer conductance or transfer function of the network (Fig. XV-1) between the input and the terminals of a diode.

THEOREM IV: "The closing of a single diode in the network will make the incremental resistance across any terminal pair decrease, and the opening of a diode will make the resistance increase."

By employing Theorem IV and Definitions I and III, it is possible to assign a code to a graphical representation of an input resistance or input conductance. Referring to Fig. XV-3(a), for example, an increase in slope corresponds to a decrease in resistance, which means that in traversing the break point at the origin from left to right, at least one "1" has to be introduced into the third state of the code describing the network represented by Fig. XV-3(a). This code, however, is by no means unique for Fig. XV-3(a), even if we restrict the number of variables (diodes) to two and do not permit the repetition of identical states, in agreement with Theorem III. Figure XV-3(b) illustrates this fact by assigning an alternate code to the network represented by Fig. XV-3(a).

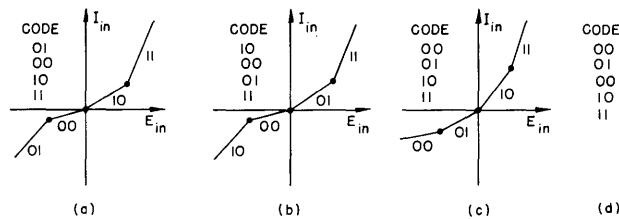


Fig. XV-3

Graphical representation of codes.

### 1. Realizability with Minimum Diodes

Although a driving-point conductance like that shown in Fig. XV-3(c) has only four states, making two the lower bound on the number of diodes necessary to synthesize it, it clearly cannot be realized with only two diodes. To realize it with two diodes, we would have to represent the network by some code such as that shown in Fig. XV-3(c). This code is a possible representation, for the net change in input resistance in going from state 01 to state 10 can be negative and thus correspond to the concave curve of Fig. XV-3(c). The code of Fig. XV-3(c) implies, however, that two diodes switch at the same level of input voltage. Such double switchings can always be broken up into two single switchings by inserting an infinitesimally small battery in series with one of the diodes that partakes in the double switching. One of the possible codes for this new condition is shown in Fig. XV-3(d). This would mean, however, that there are more than  $2^n$  linear regions in a network of  $n$  diodes. This is in direct contradiction to Theorem III, and hence is impossible. The conclusion is that not necessarily all of the  $2^n$  possible codes can be realized with  $n$  diodes ( $2^n$  states can be arranged in  $2^n!$  different ways, giving  $2^n!$  codes).

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a	b	c	d	e	f	g	h	i	j	k	l
00	00	00	00	00	00	01	01	01	01	01	01
01	01	10	10	11	11	00	00	10	10	11	11
10	11	01	11	01	10	10	11	00	11	00	10
11	10	11	01	10	01	11	10	11	00	10	00
x	w	v	u	t	s	r	q	p	o	n	m
11	11	11	11	11	11	10	10	10	10	10	10
10	10	01	01	00	00	11	11	01	01	00	00
01	00	10	00	10	01	01	00	11	00	11	01
00	01	00	10	01	10	00	01	00	11	01	11

Fig. XV-4

Total possible codes ( $2^n!=24$ ) for  $n = 2$ .

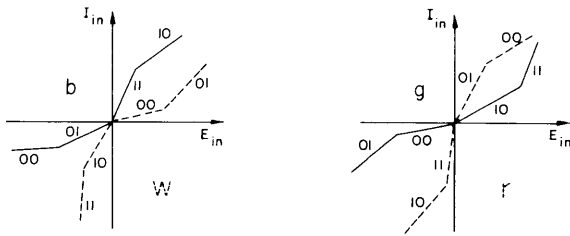


Fig. XV-5

Graphical representation of codes realizable with two diodes.

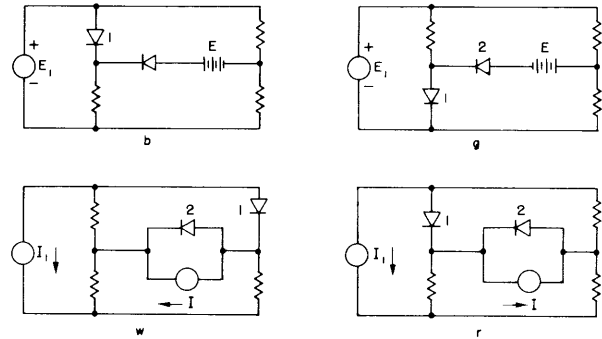


Fig. XV-6

Networks representing all physically realizable codes for two diodes.

The previous discussion poses the question of just exactly how many of the  $2^n!$  codes are realizable with  $n$  diodes. The answer to this question is intuitively that only those codes are realizable in whose successive states only one variable changes. This would be a Gray code. The proof hinges on the previous discussion.

2. Realizations for  $n$  Equals 2

In investigating the possible realizable codes for two variables, a through x of Fig. XV-4, it is seen that there are eight codes (b, d, g, l, m, r, u, and w) satisfying the conditions discussed in the preceding paragraph. Of these eight codes, b and d, u and w, l and r, g and m, however, are actually the same, for they differ only in the number assigned to the different diodes; that is, they are alternate codes representing the same

driving-point resistance or conductance picture. Hence, there are only four different realizable codes for two variables (b, g, r, and w), as shown in Fig. XV-5.

A thorough inspection of Fig. XV-4 will reveal the fact that the vertically adjacent codes are complements of each other – to use the terminology of switching circuits. This suggests the possibility that they may be realized with dual networks, as also evidenced by the dual nature of the plots of Fig. XV-5. There are only eight ways in which four different slopes can be put together so that they will appear different. A possible set of codes corresponding to these eight ways is a, b, f, g, r, s, w, x. Of these, only four follow the Gray code; and hence only four (b, g, r, w) are realizable with two diodes. Codes b and g have been synthesized in the form of the bridge circuits shown in Fig. XV-6, and their duals have been taken according to the rules (1) for obtaining networks represented by codes r and w (dotted lines). These are also shown in Fig. XV-6.

Further investigations are carried on along these lines to uncover the characteristics of piecewise-linear diode circuits with and without negative resistance regions.

G. S. Sebestyen

#### Reference

1. T. E. Stern, Internal memorandum and Sec. XV-B1 of this report.

## B. PIECEWISE LINEAR NETWORK THEORY

### 1. Duality in Diode Networks

Since the addition to a linear network of nonlinear elements that must be represented by directed line segments necessitates a careful consideration of polarity and direction, the first step in dealing with duality in nonlinear networks is to obtain a definition that is clear with regard to polarity and direction. A suitable definition (which does not conflict with the usual definitions for linear networks) will be evolved as follows.

Consider a network N consisting of interconnected two-terminal elements. This discussion will be confined to linear elements, and nonlinear elements that do not contain energy storage. Let us examine the network by making "pliers entries" into each branch, and "soldering-iron entries" across each branch. The current-voltage relationship, looking into a "pliers entry" into branch m, will be known as the short-circuit driving-point admittance for branch m. It will be denoted by  $y_m(e)$ . The voltage-current relationship, looking into the "soldering-iron entry" across branch m, will be known as the open-circuit driving-point impedance for branch m. It will be denoted by  $z_m(i)$ .

Figure XV-7(a) establishes reference polarities relative to the direction of branch m, for determining  $y_m$ . Figure XV-7(b) does the same for  $z_m$ .

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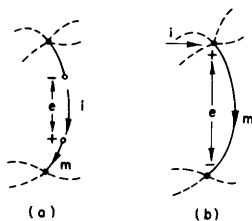


Fig. XV-7

Branch and node reference conventions.

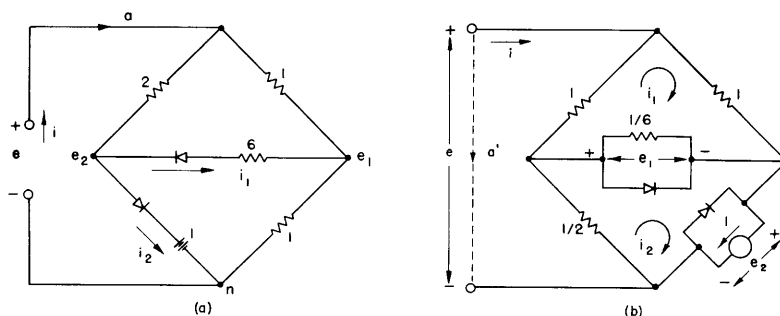


Fig. XV-8

Diode bridge network and its dual.

Now that reference conventions have been established, duality can be defined for nonlinear networks.

Definition: Given two networks,  $A$  and  $A'$ ;  $A'$  is the dual of  $A$  if and only if:

1. To each branch  $m$  in  $A$  there corresponds one and only one branch  $m'$ , in  $A'$ ; and to each branch  $n'$  in  $A'$  there corresponds one and only one branch  $n$ , in  $A$ . (In other words, the branches of the two networks can be put in one-one correspondence.)

2.  $y_m = z_{m'}$ , for all  $m$ .

3.  $z_m = y_{m'}$ , for all  $m$ .

It is clear that this definition implies topological duality as a prerequisite for electrical duality. For example, all branches,  $m, n, p, \dots$ , which appear in series around a loop in  $A$  must correspond to branches,  $m', n', p', \dots$ , across a single node pair in  $A'$ , since  $y_m = y_n = y_p = \dots$ , and therefore  $z_{m'} = z_{n'} = z_{p'} = \dots$ .

One may form the dual of a planar nonlinear network in the same manner as one would proceed with a linear network: replace loops by nodes, and directed branches by their dual branches, always being careful to observe reference directions.

As a first step in constructing the duals of diode networks we must determine the dual of a voltage source, a current source, and a diode.

It can be shown that, subject to the aforementioned convention, the dual of a voltage source is a current source generating a current in the direction of the potential drop of the voltage source, and the dual of a diode is another diode pointing in the opposite direction. It should be noted that these rules are a consequence of the chosen convention, and would be different had a different convention been chosen. Using these rules we may now proceed to the determination of the dual of a typical diode network.

The dual of the bridge network of Fig. XV-8(a) will be determined. The procedure is:

1. Assign labels and reference directions to each branch, reducing the circuit to a network of directed line segments.

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2. Draw the topological dual of this line graph, using any arbitrary reference convention; such as, all branches converging on a node in the original graph will appear clockwise around a corresponding loop in the dual graph.

3. Insert in each branch of the dual, a branch which is the dual of the original branch.

By this procedure we find that the dual of the network of Fig. XV-8(a) is that shown in Fig. XV-8(b). As a check, the node equations for the network of Fig. XV-8(a) are written below on the right, and the loop equations for the network of Fig. XV-8(b) are shown below on the left. Comparison of the two sets confirms the duality of the two networks.

$$\frac{i_2 - i}{2} + e_1 + e_2 = 0$$

$$e = \frac{i - i_2}{2} + i - i_1$$

$$i - i_1 + (-i_1) + e_1 = 0$$

where

$$e_1 = z_1(i_1, i_2) = \left( \frac{i_2 - i_1}{6}, 0 \right) \phi^-$$

$$e_2 = z_2(i_2) = [\infty(i_2 - 1), 0] \phi^+$$

$$\frac{e_2 - e}{2} + i_1 + i_2 = 0$$

$$i = \frac{e - e_2}{2} + e - e_1$$

$$e - e_1 + (-e_1) + i_1 = 0$$

where

$$i_1 = y_1(e_1, e_2) = \left( \frac{e_2 - e_1}{6}, 0 \right) \phi^-$$

$$i_2 = y_2(e_2) = [\infty(e_2 - 1), 0] \phi^+$$

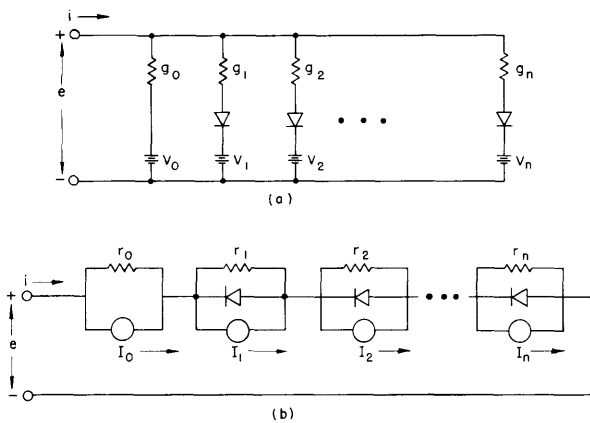


Fig. XV-9

Foster canonical forms for diode driving-point impedances.

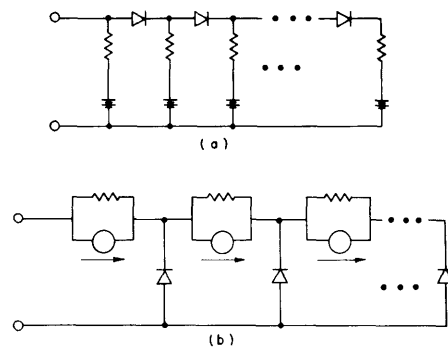


Fig. XV-10

Cauer canonical forms for diode driving-point impedances.

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### 2. Driving Point Impedance Synthesis

The synthesis problem with regard to driving-point impedances (dpi) is as follows: Given a piecewise-linear voltage-current relationship, evolve a diode network that will produce this characteristic as its dpi. This discussion is confined to monotonically increasing functions. These functions can be classified with regard to the number and types of break points they contain. Each break point may be classified as either concave or convex, depending upon whether the slope of the function decreases or increases

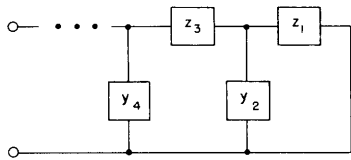


Fig. XV-11

Ladder development for general diode driving-point impedances.

as one passes through the break point from left to right. Thus, for example, an impedance function whose incremental resistance is always increasing from left to right may be classed as strictly concave. The type of network and number of diodes required to synthesize a given dpi depend upon the number and types of break points it contains, and the order in which they occur.

Minimization of diodes in realization of dpi's is discussed in Section XV-A. In this connection, there are a few general rules that can in all cases give upper and lower bounds to the required number; in some cases, actually indicate the minimum number. These are:

1. Any function containing  $n$  break points can be synthesized with  $n$  diodes or less (an upper bound).
2. A function containing  $2^n - 1$  break points requires at least  $n$  diodes (a lower bound).
3. Any function requires at least as many diodes as the excess of concave (convex) break points over convex (concave) break points in the entire function or any section thereof (more stringent lower bound).
4. One diode per break point is a necessary and sufficient number for synthesizing any strictly concave or convex function (special case of 3).

Figures XV-9 and XV-10 illustrate four canonical network forms for synthesizing strictly convex or strictly concave functions. Note that Fig. XV-9(b) is the dual of Fig. XV-9(a) and that these two forms are similar to the Foster canonical forms for linear networks. Likewise, Fig. XV-10(b) is the dual of Fig. XV-10(a), and these latter two forms are similar to the Cauer forms for linear networks. Naturally, any of these networks can be synthesized with either voltage or current sources by making Thévenin or Norton source transformations. Given a particular dpi or driving-point admittance (dpa), one can choose the proper values of the elements in any of these networks quite easily.



There are no canonical forms available for a general function. However, Fig. XV-11 is a block diagram of a network for synthesizing any arbitrary function, using one diode per break point, in a series-parallel arrangement. This is a minimum network if one is considering only series-parallel developments, but one might be able to reduce the number of diodes for certain types of functions by using lattice structures. The ladder structure shown is derived in the following manner. First, the given function is partitioned into strictly convex or strictly concave sections. These sections are then synthesized one at a time by using any of the aforementioned canonical forms. If the sections of the function are numbered from left to right, 1, 2, . . . , then the impedance or admittance elements corresponding to these sections appear in the correspondingly numbered boxes of Fig. XV-11. In general, then, all of the horizontal sections are strictly convex impedance functions, and all of the vertical sections are strictly convex admittance functions. Again, it is not difficult to determine the actual values of the required elements.

T. E. Stern

### C. A PIECEWISE-PLANAR MULTIPLIER

The output of a multiplier ( $Z$ ) should satisfy the equation  $Z=KXY$  where  $X$  and  $Y$  are the two independent variables, and  $K$  is an arbitrary gain factor. This equation may be represented as a surface whose height above the  $x$ - $y$  plane is equal to  $Z$ . The problem of building a practical multiplier, then, is essentially one of reproducing this surface. See Fig. XV-12.

Mr. T. E. Stern describes, in the Quarterly Progress Report of July 15, 1954, a general method for the synthesis of piecewise-planar functions of two variables

with diode networks. He introduces a compact algebraic notation for piecewise-linear functions, and discusses two basic diode building blocks, the "step" element and the "pyramid" element.

The use of this algebraic notation and the development of a third building block, the "ramp" element, make this method particularly adaptable to an approximation of the multiplier surface on a piecewise-planar basis.

The "ramp" element is depicted in Fig. XV-13. The  $x$ - $y$  plane is divided into a grid of equal increments  $\Delta$  of the independent

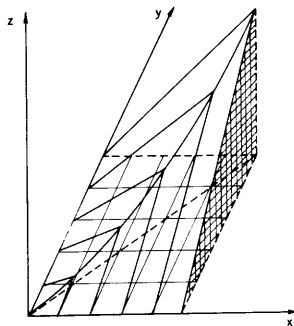


Fig. XV-12

Portion of multiplier surface.

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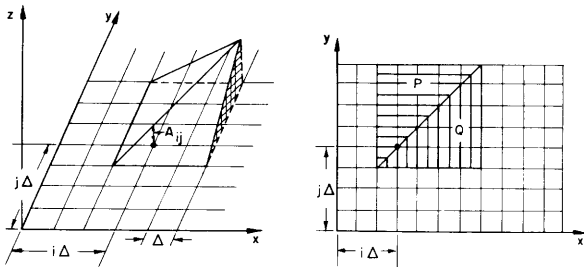


Fig. XV-13  
"Ramp" element.

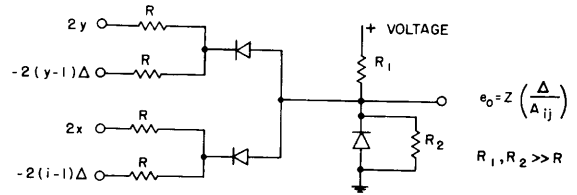


Fig. XV-14  
Realization of "ramp" element.

variables  $x$  and  $y$ . The "center" of the "ramp" element is defined as being at the point  $x=i\Delta$ ,  $y=j\Delta$ , and the "height" of the element ( $A_{ij}$ ) is defined at this point. The equations of the "ramp" element are

1. in region Q  $Z_q = \frac{A_{ij}}{\Delta} [y - (j-1)\Delta]$  for  $y > (j-1)\Delta$
2. in region P  $Z_p = \frac{A_{ij}}{\Delta} [x - (i-1)\Delta]$  for  $x > (i-1)\Delta$

which can be combined, by using the previously mentioned algebraic notation, to

$$Z = [(Z_q, Z_p) \phi^-, 0] \phi^+$$

$$Z = \frac{A_{ij}}{\Delta} \left\{ [(y - (j-1)\Delta), (x - (i-1)\Delta)] \phi^-, 0 \right\} \phi^+$$

(The reader is referred to Mr. Stern's article for background on the notation of this equation.) One suitable network realization of the "ramp" element is given in Fig. XV-14.

The procedure used to approximate the multiplier surface is as follows. The  $x$ - $y$  plane is divided into a grid of points at equal increments of  $x$  and  $y$ . The true values of  $Z$  are tabulated for each of these points in the form of a matrix whose general term  $[a_{ij}]$  represents  $Z$  at  $x=i\Delta$ ,  $y=j\Delta$ . Over each of these points, in general, is centered a "ramp" element. The height of this element is so determined that when it is added to the contribution from all the other elements at the point their sum will equal  $a_{ij}$ , the true value of the function. Thus, an additional matrix is derived whose general term  $[A_{ij}]$  represents the required "height" of the "ramp" element which is centered at  $x=i\Delta$ ,  $y=j\Delta$ .

To reproduce an arbitrary function over a range of  $m$  increments in  $x$  and  $n$  increments in  $y$  would require, in general,  $mn$  "ramp" elements. However, for the particular

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Table I

$a_{ij}$  Matrix

5	$5\Delta^2$	$10\Delta^2$	$15\Delta^2$	$20\Delta^2$	$25\Delta^2$
4	$4\Delta^2$	$8\Delta^2$	$12\Delta^2$	$16\Delta^2$	$20\Delta^2$
3	$3\Delta^2$	$6\Delta^2$	$9\Delta^2$	$12\Delta^2$	$15\Delta^2$
2	$2\Delta^2$	$4\Delta^2$	$6\Delta^2$	$8\Delta^2$	$10\Delta^2$
1	$\Delta^2$	$2\Delta^2$	$3\Delta^2$	$4\Delta^2$	$5\Delta^2$
	1	2	3	4	5

Table II

$A_{ij}$  Matrix

5	$\Delta^2$	0	0	0	0
4	$\Delta^2$	0	0	0	0
3	$\Delta^2$	0	0	0	0
2	$\Delta^2$	0	0	0	0
1	$\Delta^2$	$\Delta^2$	$\Delta^2$	$\Delta^2$	$\Delta^2$
	1	2	3	4	5

case of the multiplier, there is a simplification that results in a large reduction in the number of elements, and consequently in the number of diodes, required.

The  $a_{ij}$  matrix for the multiplier surface over a grid of 25 tabulated points is given in Table I (K is assumed to be 1). The required  $A_{ij}$  matrix is given in Table II. Nine identical elements are required for this example, and it can be shown that in general only  $m+n-1$  elements are needed to reproduce the multiplier surface at  $mn$  tabulated points. Further analysis shows that the maximum error (assuming ideal "ramp" elements) attributable to the linear interpolation between grid points is  $\Delta^2/4$ , which for the particular example is 1 per cent of the full-scale range. The approximation of the surface over the voltage range of interest at smaller increments in  $x$  and  $y$  will decrease the maximum error. This is limited, finally, by holding the elements required to a practical number and by actual circuit component accuracy.

A "ramp" element has been built with an accuracy of approximately 1 per cent of full scale. Nine of these elements were incorporated in a multiplier. Preliminary measurements indicate an accuracy of 3 per cent for this first crude device. These figures can be improved. A means for modifying this device from one- to four-quadrant operation is under investigation.

R. I. Morganstern

D. AN ELECTRONIC VECTOR MAGNITUDE CIRCUIT

This device is one whose output is the vector magnitude of its two inputs; that is,  $Z = (X^2 + Y^2)^{1/2}$ . Since this is the equation of a circular cone, the device must reproduce the surface of a cone. In the Quarterly Progress Report of July 15, 1954 (p. 85), T. E. Stern described a method for realizing a piecewise-planar approximation to an

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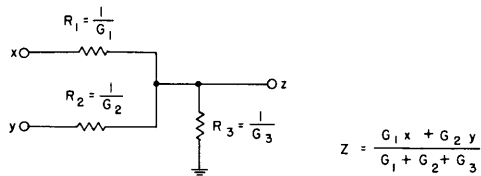


Fig. XV-15

Circuit for obtaining plane coefficients.

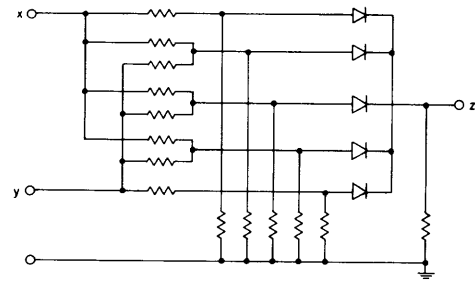


Fig. XV-16

Circuit of vector magnitude computer.

arbitrary three-dimensional surface with diode circuits. Thus a cone may be approximated by a set of intersecting planes all passing through the origin of coordinates.

Because all of the planes pass through the origin, their equations have the form  $Z = Ax + By$ . Since  $(x^2 + y^2)^{1/2} = (|x|^2 + |y|^2)^{1/2}$ , only the first quadrant of the cone need be reproduced if the inputs of the device are preceded by absolute value circuits. Therefore  $A$  and  $B$  are always positive. If  $A + B \leq 1$ , a plane may be easily realized with the circuit shown in Fig. XV-15. The condition  $A + B \leq 1$  can always be met by choosing suitable scale factors for the input.

It can be shown that for any given values of  $x$  and  $y$ , the value of  $z$  which is on that plane that most closely approximates the cone will be numerically greater than the value of  $z$  on any of the other planes. Therefore, it only remains to select the greatest of a set of positive voltages. This can readily be done with diodes. The complete circuit is shown in Fig. XV-16.

A circuit of this sort has been built, reproducing the first quadrant of the surface of the cone. Preliminary tests indicate an accuracy of 1 per cent.

L. W. Massey