Adaptive Predistortion Using a Delta Sigma Modulator for Automatic Inversion of Power Amplifier Nonlinearity

Adaptive Predistortion Using a $\Delta\Sigma$ Modulator for Automatic Inversion of Power Amplifier Nonlinearity

Hyun H. Boo, *Student Member, IEEE*, Sung Won Chung, *Student Member, IEEE*, and Joel L. Dawson, *Member, IEEE*

***Abstract*—This brief demonstrates a new adaptive digital predistortion architecture particularly suited to mobile handset applications. The central idea is to build a lookup table (LUT) that directly captures the static compressive nonlinearity of the power amplifier (PA) and then insert this LUT into the *feedback path* of a $\Delta\Sigma$ modulator. The oversampled $\Delta\Sigma$ modulator automatically performs both the inversion of the PA nonlinearity and the interpolation between LUT entries, permitting complex modulation strategies to be handled with an absolute minimum of LUT entries and with a dramatically simplified computational structure. The advantages of this architecture over previous methods include: 1) there is no need to explicitly invert the PA nonlinearity, reducing the complexity for the system designer; 2) the LUT training is done with an open-loop method, improving the training speed; 3) there is no need to explicitly employ numerical interpolation between LUT entries; and 4) digital-to-analog converter (DAC) nonlinearity is incorporated into the predistortion, allowing fast low-resolution DACs to be used in the final system. We built a proof-of-concept prototype for a 900-MHz, 27-dBm PA transmitting a 16-ary quadrature amplitude modulation (16-QAM) signal with a bandwidth of 3.4 MHz. The predistortion system reduced out-of-band distortion products by 10 dB and improved the error vector magnitude from 3.5% to 2.0%.**

***Index Terms*—Adaptive predistortion, delta–sigma modulator, digital predistortion, PAs, power amplifier (PA) linearization.**

I. Introduction

NEW third-generation and fourth-generation mobile communications systems feature signals that are of high bandwidth and have high peak-to-average power ratios. For signals with a high peak-to-average power ratio, high power amplifier (PA) linearity in the transmitter is critical. Unfortunately, linear PAs are inefficient, which is a major drawback in cost-driven mobile handsets. PA linearization techniques soften the linearity versus efficiency tradeoff of PAs, allowing them to be operated closer to saturation where their efficiency is higher. Digital predistortion has established itself as the dominant technique for PA linearization [1]–[3]. Digital predistortion works by preceding the nonlinearity of the PA with its functional inverse, such that the overall cascade is linear.

To take into account changing conditions, PA aging, temperature swings, etc., many predistortion systems are designed to be adaptive [4]. However, a fundamental difficulty that many of these systems share is stability and/or convergence issues associated with closed-loop control. Some of these systems depend on detailed mathematical characterization of the PA, which they invert to achieve predistortion. Mathematical inversion does not present a fundamental difficulty, but it is computationally intensive.

We propose a simple and effective adaptive digital predistortion technique using the $\Delta\Sigma$ modulator architecture, as shown in Fig. 1. It requires less complexity than other adaptive predistortion techniques and makes practical application to mobile devices more feasible. The use of $\Delta\Sigma$ modulators has previously been explored in RF transmitters to take greater advantage of digital scaling trends [3], [5]–[7]. In our system, the lookup table (LUT) is first trained in an open-loop manner, as shown in Fig. 3. This has a tremendous practical advantage over closed-loop Cartesian feedback training in that the training symbol rate is not limited by stability requirements [4]. Next, the trained LUT is placed in the *feedback path* of a digital $\Delta\Sigma$ modulator. The effect is that the closed-loop transfer function of the $\Delta\Sigma$ modulator becomes the inverse nonlinearity of the PA, and interpolation between LUT entries naturally happens as a result of oversampling and subsequent low-pass filtering. Moreover, because the dynamics of the $\Delta\Sigma$ modulator loop are simple in our first-order loop, introducing nonlinearity here is not problematic from a stability standpoint. Overall, the system inversion and LUT interpolation is achieved in a way that is absolutely simple and direct. This attribute is particularly important for handset applications where system complexity adds to cost. Furthermore, because the nonlinearity of the coarse DACs is incorporated into the LUT during training, the accuracy and therefore the power required by these DACs is considerably reduced.

We organize this brief as follows. In Section II, we describe the details of the $\Delta\Sigma$-modulated digital predistortion linearization architecture and its advantages over other previously explored techniques. Section III highlights prototype design. Experimental results are presented in Section IV. Finally, we provide our concluding remarks in Section V.

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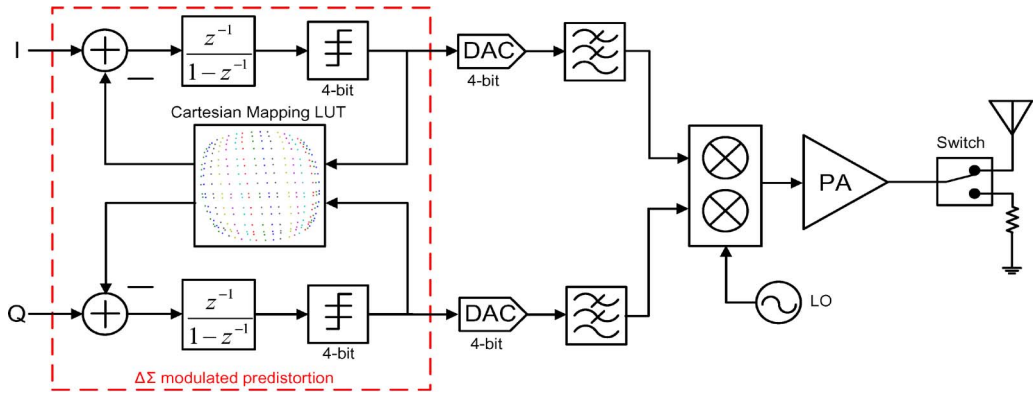

Fig. 1. Proposed ΔΣ-modulated digital predistortion architecture.

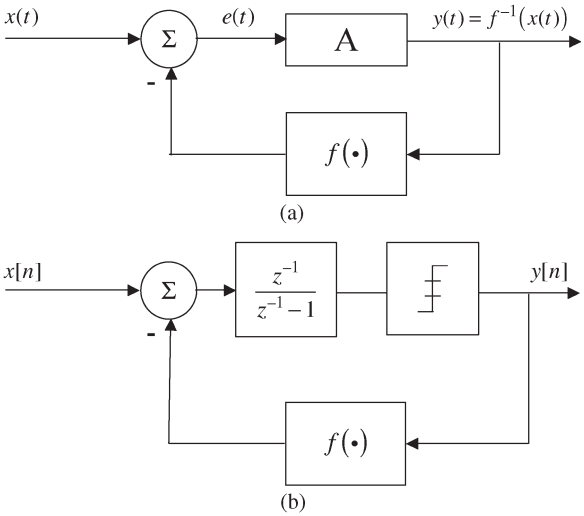

Fig. 2. Using feedback to invert a nonlinearity. (a) Familiar result that if a feedback loop is stable, the transfer characteristic from $x(t)$ to $y(t)$ is $f^{-1}(\cdot)$ for sufficiently high values of A. (b) Result exploited within the context of ΔΣ modulators. The nonlinear function $f(\cdot)$ is realized using an LUT.

II. Using a ΔΣ Modulator for Digital Predistortion

This architecture uses a Cartesian representation of symbols and consists of a ΔΣ-modulated predistorting block, followed by 4-bit DACs, analog filters to remove the out-of-band quantization noise, the upconversion mixer, and a 1–2-W PA. The downconversion mixer and the attenuator are needed for the LUT training. In this section, we describe the LUT training procedure, as well as the digital predistortion operation of the ΔΣ modulator.

A. Nonlinear Inversion Using a ΔΣ Modulator

In our system, the ΔΣ modulator inverts the nonlinearity by inserting its corresponding LUT in the feedback path. We illustrate the concept in Fig. 2. Fig. 2(a) shows the familiar result for a stable feedback loop with a high loop gain and, in particular, a high forward gain A. Under these special conditions, $e(t)$ is small compared to $x(t)$, $y(t)$, and $f(y(t))$. It follows that $x(t) \approx f(y(t))$, and therefore, $y(t) \approx f^{-1}(x(t))$. These approximations pass to equalities as A approaches infinity, provided that the loop remains stable.

In Fig. 2(b), we show how we apply the nonlinear inversion property of feedback systems to a ΔΣ modulator. The feedback path contains the nonlinearity that we wish to invert. In our system, it was particularly convenient to implement this function using an LUT, where each possible output of the quantizer is mapped to its nonlinearly warped counterpart. It is important to note that the 1-bit quantizers commonly used for ΔΣ modulators are not appropriate for nonlinear inversion. The reason is that a 1-bit quantizer only interrogates two points on the nonlinear transfer characteristic $f(\cdot)$. It follows that $f(\cdot)$ can be replaced with the first-order polynomial $p(x) = ax + b$ with no change in system behavior. A similar argument holds for higher order polynomials. In general, if $f(\cdot)$ is a polynomial of order n, the quantizer must have at least $n + 1$ levels.

The number of quantizer bits for our ΔΣ modulator was set by the size of our LUT. We chose to use a 16 × 16 size LUT, giving us a 4-bit quantizer. Although we used a low-order ΔΣ modulator, a higher order can be used to further relax the oversampling ratio. For a given dynamic range (DR), we can choose the appropriate order $\mathbf{k}$, oversampling ratio $\mathbf{m}$, and number of quantization $\mathbf{b}$ bits for the ΔΣ modulator using the equation

$$\mathrm{DR} = 3(2k+1)m^{(2k+1)}\frac{(2^b-1)^2}{2\pi^{2k}} \tag{1}$$

from [8].

The ΔΣ-modulated digital predistortion block continues to benefit in terms of both speed and power as CMOS technology continues to scale. For example, a pipelined ΔΣ modulator operating at 5.4 GHz was validated in [6]. Furthermore, a digital ΔΣ modulator with a multibit quantizer in a 90-nm CMOS for a wireless transmitter presented in [9] shows a submilliwatt power consumption running at 468 MHz for 7-bit signed data. For the DACs, a 6-bit full-Nyquist 3-GS/s DAC has been presented that only consumes 29 mW [10]. We conclude that the fast DACs needed for the oversampled ΔΣ modulator do not add significant power overhead.

B. LUT Training

The LUT training process is shown in Fig. 3. First, an RF switch connects the PA output to a 50-Ω load to prevent the

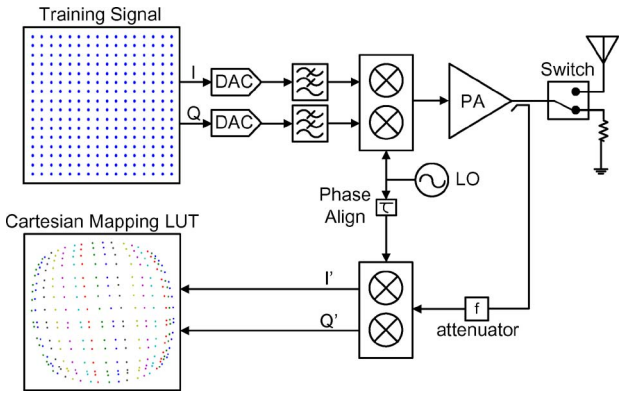

Fig. 3. LUT training procedure. This training procedure is repeated as often as necessary to adapt to changing conditions.

transmission of training signals. Then, the upconverted training signal is directly fed into the PA, and the output is sampled after the downconversion to capture the compressive nonlinearity characteristic of the PA. The RF switch connects back to the antenna for data transmission after the training completes. Phase alignment is necessary in this system, as phase misalignment will degrade stability margins in the predistorted ΔΣ modulator in much the same way that it will affect a closed-loop Cartesian feedback system [11]–[14]. An important advantage to using first-order ΔΣ modulators, as we do in this prototype, is that its sensitivity to phase misalignment is reduced so as to only be a serious concern if the phase misalignment approaches 90°.

Previously explored LUT training procedures in [1] and [2] use feedback and an adaptive algorithm to capture the inverse nonlinearity of the PA. This adds complexity to the transmitter system and also causes convergence and bandwidth issues. Our LUT training, however, only needs to sample the attenuated PA output, which leads to more straightforward and much faster training with minimum computational overhead. As can be seen from Fig. 3, the training symbols are simply all of the available digital address codes for the LUT. For this prototype, the total LUT size was 256 entries. This training procedure is then repeated as often as necessary to ensure adaptation to changing conditions.

It is worth noting that this training method results in corrective predistortion only for memoryless nonlinearity. While this would be a serious shortcoming for base station and other high power PAs, memoryless predistortion has been shown to provide substantial improvement at the lower output powers typical of handsets [15].

C. RF Switch

The inclusion of the RF switch in Fig. 3 makes this system well suited for time-division-duplexing systems such as WiMAX and WiFi. In these systems, there is already a transmit/receive switch between the PA and the antenna [16]. It is therefore possible to arrange for transmission to a dummy load without introducing substantial loss. Frequency-division-duplexing (FDD) transceivers such as those used for 3G cellular systems require a different approach. FDD systems do not employ an RF switch in the transmit chain, and including one for the sake of predistortion training would introduce unacceptable additional loss. Instead, we can exploit any unused spectrum adjacent to the TX bands exclusively for training. The connection to the dummy load would be made through a modified duplexer, whose new path would connect the PA output to the dummy load.

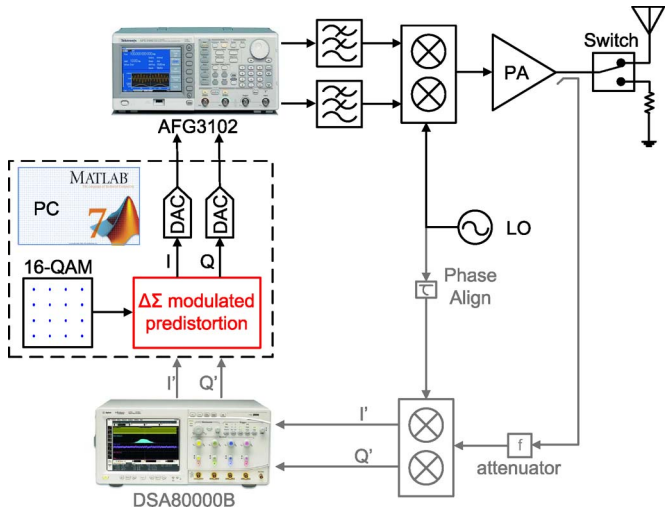

Fig. 4. Predistortion block implemented in MATLAB and loaded into a Tektronix waveform generator. We built a discrete prototype consisting of an upconversion mixer, PA, phase shifter, attenuator, and downconversion mixer. The gray signal path is made active during training stage.

III. Implementation of the Prototype System

The measurement setup is shown in Fig. 4. The gray signal path is active only during the training stage. The ΔΣ-modulated predistortion block and the low-resolution DACs were implemented in MATLAB. We used an oversampling ratio of 128× and a 4-bit quantizer for the ΔΣ modulator. The LUT size is 16 × 16, and each entry has a 12-bit resolution. The LUT is bypassed in the ΔΣ modulator when generating signals without predistortion. For the I and Q channel DACs, we introduced Gaussian-distributed mismatch commensurate with 4-bit performance, as shown in Fig. 5. We implemented a discrete prototype transmitter with a class-A PA, Mini Circuits ZHL-0812-HLN, centered at 900 MHz for our demonstration.

For the LUT training, we generated a 16 × 16 constellation and sent it through the two 4-bit DACs mentioned above. The training signal was transmitted at a symbol rate of 100 kS/s, and an Agilent digital signal analyzer DSA80000B was used to sample the demodulated PA output after proper phase alignment. A total of 32 values were averaged for each LUT entry, resulting in a total training time of 82 ms. By using a higher symbol rate, this training time can easily be reduced to under 10 ms.

The 16-ary quadrature amplitude modulation (16-QAM) signals were pulse shaped and upsampled by a factor of 32 before feeding into the ΔΣ-modulated predistortion block. The predistorted signal and the output of the 4-bit DACs were computed in MATLAB, and the data were loaded in a Tektronix AFG3102 waveform generator.

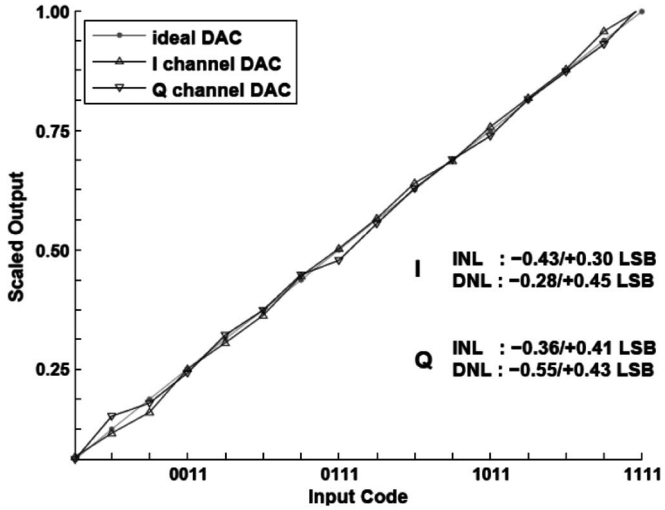

Fig. 5. I channel DAC having an integral nonlinearity (INL) of $-.43/+.30$ LSB and a differential nonlinearity (DNL) of $-.28/+.45$ LSB and Q channel DAC having an INL of $-.36/+.41$ LSB and a DNL of $-.55/+.43$ LSB.

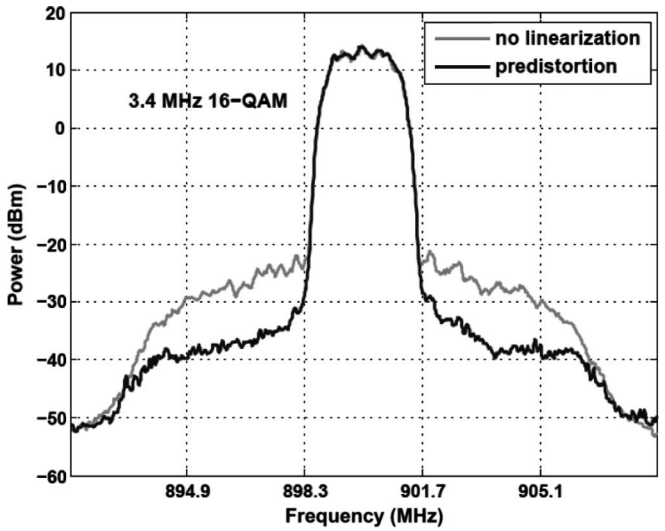

Fig. 6. Measured output spectrum of the linearized PA. The linearization system reduced the out-of-band distortion products by approximately 10 dB.

IV. Experimental Results

Fig. 6 shows the comparison between the unlinearized overall transmitter and the linearized transmitter. We observe an approximately 10-dB reduction in distortion products at a total PA output of 26.7 dBm. This improvement is consistent with other linearization results our group has obtained using the same amplifier [4]. In addition, the measured error vector magnitude (EVM) performance improved from 3.45% to 2.02%, as shown in Fig. 7.

Fig. 8 shows the predistorted signal at a wider spectral span. Filtering the $\Delta\Sigma$ modulator output using Mini-Circuit SLP-5 suppresses out-of-band quantization noise. The unfiltered spectrum, however, has quantization noise initially rising by 20 dB/dec. The drop in quantization noise starting at 100 MHz from the carrier is caused by the AD8349 upconversion mixer's limited modulation bandwidth.

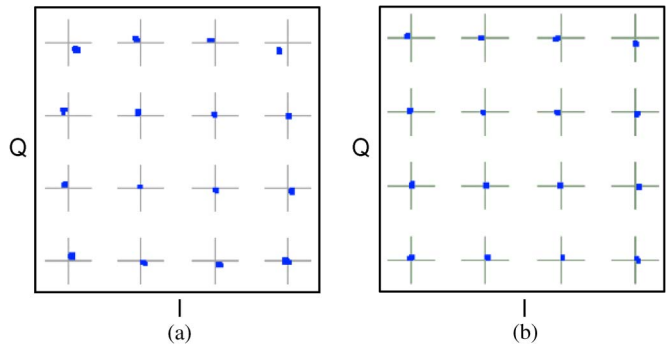

Fig. 7. Measured EVM shows (a) 3.45% when not linearized and (b) 2.02% after predistortion.

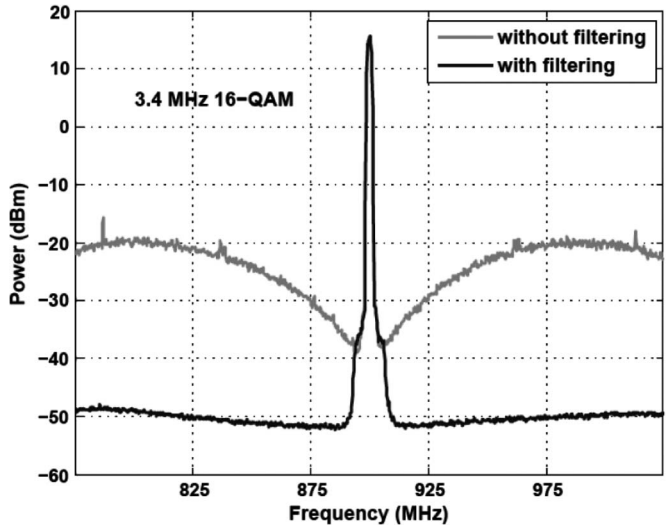

Fig. 8. Broader band (250 MHz) measured spectrum of the linearized PA output with filtering and without filtering.

V. Conclusion

This brief has demonstrated a new digital predistortion architecture that is ideal for mobile handset applications. We have first built an LUT that directly captures the static compressive nonlinearity of the PA and insert this LUT into the feedback path of a $\Delta\Sigma$ modulator. The oversampled $\Delta\Sigma$ modulator then accomplishes both the inversion of the PA nonlinearity and the interpolation between LUT entries and does so with an absolute minimum of computational complexity. We have tested our proof-of-concept prototype on a 900-MHz, 27-dBm PA transmitting a 16-QAM signal with a signal bandwidth of 3.4 MHz. The predistortion system reduced out-of-band distortion products by 10 dB and improved EVM from 3.5% to 2.0%.

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