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Lack of Spatial Correlation in MOSFET Threshold Voltage Variation and Implications for Voltage Scaling

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***Abstract*—Due to increased variation in modern process technology nodes, the spatial correlation of variation is a key issue for both modeling and design. We have created a large array test-structure to analyze the magnitude of spatial correlation of threshold voltage (V_T) in a 180 nm CMOS process. The data from over 50 k measured devices per die indicates that there is no significant within-die spatial correlation in V_T. Furthermore, the across-chip variation patterns between different die also do not correlate. This indicates that Random Dopant Fluctuation (RDF) is the primary mechanism responsible for V_T variation and that relatively simple Monte Carlo-type analysis can capture the effects of such variation. While high performance digital logic circuits, at high V_{DD}, can be strongly affected by spatially correlated channel length variation, we note that subthreshold logic will be primarily affected by random uncorrelated V_T variation.**

***Index Terms*—Spatial correlation, threshold voltage, variation.**

I. Introduction

SCALING has resulted in poor control of parametric variations, increasing focus on such variations as an important design consideration [1]. Many steps within the manufacturing process introduce layout/pattern-dependent or spatial variation, including 1) subwavelength lithography, 2) plasma etch, 3) ion implantation and annealing, and 4) chemical-mechanical polishing [2], [3]. In particular, the physics of the fabrication process, or spatially varying characteristics of the layout (such as pattern density), can act to create deviations in device or interconnect geometry or material properties that have repeatable spatial patterns. In some cases, the matching between devices or structures has a strong dependence on the separation distance between those devices; i.e., there exists significant spatial correlation in the variation.

Much of the existing literature focuses on approaches to efficient modeling of spatial correlations of process parameters and their impact on timing in circuits [4]–[6]. Methods for robust extraction of spatial correlations from noisy measurements have also been reported [7], [8]. Most, if not all, of this literature lacks data to substantiate the models and methods developed. As a result, the assumptions and functional forms of these modeling approaches to spatial correlation remain largely unvalidated.

Recently, the modeling community has had particular interest in the spatial correlation of parametric variations in the hope of developing algorithms and tools that allow designers to take advantage of, or counter, known correlations. While this modeling capability aids in robust design, it also has the potential to provide even more advantage when developing adaptive systems that can detect and respond to parameteric variation. However, the substantial data necessary to compute accurate spatial correlations is often difficult to acquire, leaving the modeling community guessing as to the functional forms of the spatial correlations present (if any).

To date, most spatial correlation data analysis has considered channel length variation ($\triangle L$) [9]. However, there has been increasing attention to the measurement and characterization of V_T variation in large device arrays with the work of Agarwal *et al.*, Rao *et al.* and Mukhopadhyay *et al.* at IBM [10]–[13], Fischer *et al.* [14] and Wang *et al.* [15]. Only a subset of these present data regarding spatial correlation analysis of the measured results. Agarwal *et al.* present spatial correlation analysis of SRAM-sized devices in a 65-nm SOI process, concluding that little spatial correlation in V_T within each die exists at 65 nm. Fischer *et al.* also provide V_T variation data and autocorrelation analysis of 1-M SRAM cells at both the 90 nm and 65-nm nodes, with the results again showing no spatial correlation. Furthermore, both the aforementioned works make little to no effort to isolate threshold voltage variation from variation in channel length or other variation sources. Sabade *et al.* [16] use wafer-level spatial information on chip-level leakage currents to predict neighboring chip leakage currents and screen faulty die [16].

In [17], we described the analytic basis and a custom test-circuit to gather intrinsic V_T variation data, which isolates V_T from other parameters by measuring subthreshold currents of MOSFETS, similar in approach to [10]. Here we contribute the threshold voltage (V_T) variation data, focusing on the analysis and implications of this data. We present extended variation analyses, beyond those in [10], including examination of potential correlations in the variation patterns between pairs of die. A surprising result is that, once variations in channel length are properly isolated, no significant spatial correlations are found in V_T, even in the 180 nm technology used here. Given this lack of within-die spatial correlation, we examine the effects on dy-

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namic voltage scaling (DVS) systems. We find that while circuit performance deviations between nearby circuits might be highly correlated at nominal operating voltages due to high correlation in channel length, this performance correlation quickly falls off as random, uncorrelated V_T variation begins to dominate at lower voltages.

In Section II, we describe the analytic basis in using subthreshold leakage currents to extract threshold voltages. Here, we also detail the test structure used to measure the subthreshold currents from a large number of MOSFETs in a $2\ \mathrm{mm} \times 2\ \mathrm{mm}$ array, and provide simulation results detailing how well the structure is able to isolate V_T variation from other types of variation. This is followed by a detailed analysis of the extracted threshold voltages of these devices in Section III. We then describe the modeling and circuit implications of the observed variations, paying close attention to how correlation (or lack of correlation) in parameter variation affects DVS systems in Section IV. Conclusions are presented in Section V.

II. Theory and Enabling Circuits

In this section, we describe the device operation fundamentals and analytic basis used to extract V_T variation from leakage current measurements, as well as the overall test chip architecture and circuits.

A. Extraction of $\triangle V_T$

The intrinsic or ideal threshold voltage, V_{T_o}, of a MOSFET is defined by (1), where V_{FB} is the flat-band voltage, ϕ_{F_p} is the Fermi potential of the substrate, γ is the body-factor and V_{SB} is the source to body bias. Thus, V_{T_o} is fundamentally dependent only on substrate doping, N_{sub}, and the oxide thickness, t_{ox}, through γ:

$$V_{T_o} = V_{FB} + 2\phi_{F_p} + \gamma\sqrt{2\phi_{F_p} + V_{SB}}. \tag{1}$$

However, due to short-channel effects, notably drain-induced barrier lowering (DIBL), in the deep submicron regime, the actual threshold voltage, V_T, becomes a function of not only N_{sub} and t_{ox}, but also channel length, L, and source/drain junction depth, x_j[18]. To quantify this dependence, V_T is now defined as a summation of the ideal threshold voltage (V_{T_o}) and a shift $(\triangle V_T)$ due to short channel effects, as in [19].

The appropriate modeling of variability requires modeling variability in each of the fundamental parameters. However, measuring variability in many fundamental parameters (e.g., N_{sub}) is often extremely difficult. As such, many modeling and simulation programs, such as Hspice, allow modeling of variability in parameters critical to circuit designers: V_{T_o} and L through the use of the *delvto* parameter and direct manipulation of L in the netlist [20]. This work seeks to characterize the variation and, in particular, spatial variation of V_{T_o} to enable such modeling and simulation. This requires isolation of V_{T_o} from other common sources of variation such as $\triangle L$, and can be achieved to a large degree in the subthreshold regime of transistor operation[1].

[1]From this point forward, we will use V_T and V_{T_o} interchangeably indicative of characterization of the *ideal* MOSFET threshold voltage.

In this regime, the current through the transistor is given by (2), where I_o is the drain current at $V_{\mathrm{GS}} = V_{T_o}$, γ' is the body-effect coefficient, η is the DIBL coefficient, n is the subthreshold slope ideality parameter, defined by (3), and V_{TH} is the thermal voltage:

$$I_D = I_o \cdot e^{\frac{V_{\mathrm{GS}} - V_{T_o} - (\gamma' \cdot V_{SB}) + \eta \cdot V_{\mathrm{DS}}}{nV_{\mathrm{TH}}}} \cdot \left(1 - e^{\frac{-V_{\mathrm{DS}}}{V_{\mathrm{TH}}}}\right) \tag{2}$$

$$n = \frac{\triangle V_{\mathrm{GS}}}{V_{\mathrm{TH}} \cdot \triangle \log(I_D) \cdot \ln(10)}. \tag{3}$$

The $\left(1 - e^{\frac{-V_{\mathrm{DS}}}{V_{\mathrm{TH}}}}\right)$ term in (2) is easily eliminated with $V_{\mathrm{DS}} > 3 \cdot V_{\mathrm{TH}}$, and $\gamma' \cdot V_{SB}$ can be eliminated by shorting the body and source of each device. Minimization of the DIBL component is achieved by reducing V_{DS} to a few hundred millivolts—large enough to eliminate the $(1 - e)$ term, but still small enough to minimize the effect of DIBL. Assuming that V_{GS}, V_{DS}, η, and n are identical for two arbitrary devices, taking the natural logarithm of the ratio of the currents of those two devices will result in a simple, analytic equation for the $\triangle V_T$ of those devices[2], as shown in the following derivation:

$$\ln\left(\frac{I_{D_2}}{I_{D_1}}\right) = \ln\left(\frac{I_o \cdot e^{\frac{V_{\mathrm{GS}} - V_{T_{o2}} + \eta \cdot V_{\mathrm{DS}}}{nV_{\mathrm{TH}}}}}{I_o \cdot e^{\frac{V_{\mathrm{GS}} - V_{T_{o1}} + \eta \cdot V_{\mathrm{DS}}}{nV_{\mathrm{TH}}}}}\right) \tag{4}$$

$$\ln\left(\frac{I_{D_2}}{I_{D_1}}\right) = \ln\left(e^{\frac{V_{T_{o1}} - V_{T_{o2}}}{nV_{\mathrm{TH}}}}\right) \tag{5}$$

$$\triangle V_{T_{1,2}} = nV_{\mathrm{TH}} \cdot \ln\left(\frac{I_{D_2}}{I_{D_1}}\right). \tag{6}$$

It is known that the subthreshold slope between devices can vary, and thus the assumption that n is identical for the devices being compared is not valid in general. Taking this into account, the above equations can be reworked and shown to provide the relationship in (7) between the drain currents, threshold voltages and n:

$$n_1 V_{\mathrm{TH}} \cdot \ln\left(\frac{I_{D_1}}{I_{D_2}}\right) - \frac{n_2 - n_1}{n_2} \cdot V_{\mathrm{GS}} = \frac{n_1}{n_2} \cdot V_{T_2} - V_{T_1}. \tag{7}$$

Since (7) provides no simple, closed-form solution for $\triangle V_T$, the values of n_1, n_2, V_{GS} and at least one device V_T must be known to compute the other and thus a delta between the two. Equation (3) shows that n can easily be computed using two measurements of I_D at differing values of V_{GS}. We also note that by using a small value for V_{GS} we can minimize the contribution of the second term in (7) in two ways: a smaller V_{GS} results in 1) a smaller multiplicand, and 2) as can be seen in Fig. 2, the instantaneous value of n tends to converge at extremely low V_{GS} despite variation in V_T, allowing use of (6) rather than (7).

Ascertaining the value of one of the device threshold voltages is more difficult, but possible by finding the value of V_{GS} where the subthreshold current deviates from the ideal log-linear form. This known V_T can then be used to compute the V_T for every

[2]This $\triangle V_T$ denotes the difference in ideal threshold voltage between two devices and is distinct from $\triangle V_T$ in [19] which describes the shift in a single device's threshold voltage due to short channel effects.

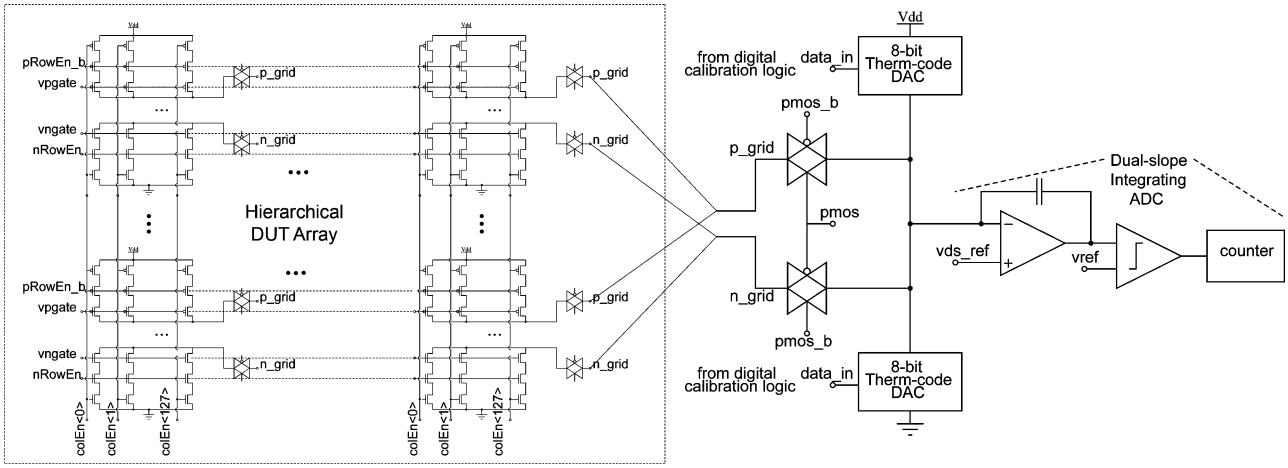


Fig. 1. Simplified V_T variation architecture and circuits.

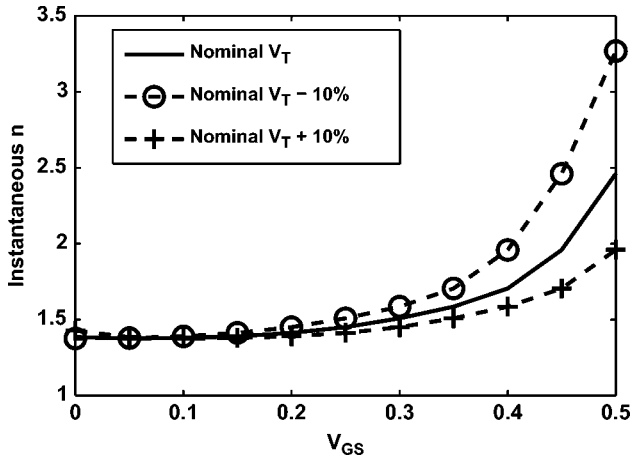


Fig. 2. Convergence of n at low $V_{\rm GS}$ despite V_T variation.

other DUT. By using (7), along with two additional measurements for each DUT (to compute n), a complete V_T map of all test devices across the chip can be ascertained.

A more practical method is to compute an average value, $n_{\rm avg} = 0.5 \cdot (n_1 + n_2)$, where each n can be computed from subthreshold leakage current measurements, and then use $n_{\rm avg}$ in (6). This has the added benefit that post-processing of the current measurements to extract $\triangle V_T$ remains computationally efficient. Furthermore, the error associated with using this average value is small if $n_1 \approx n_2$.

B. Test-Structure Architecture and Circuits

Fig. 1 is a simplified schematic showing the architecture and circuit blocks to measure V_T variation. A dual-slope, integrating analog-to-digital Converter (ADC) is used to measure subthreshold leakage currents due to its suitability to accurately measure small currents. By externally setting $V_{DS_{\rm ref}}$, the operational amplifier enforces a virtual ground at the input nodes, ensuring that each device connected is biased at the same $V_{\rm DS}$. Amplifier gain and mismatch errors will introduce error into the value of $V_{\rm DS}$ seen by the DUTs, but each DUT is affected in the same manner. Large input devices and a high-gain $(> 60$ dB$)$ ensure that this error is small nevertheless.

To measure currents of many devices efficiently, we use a single ADC that is multiplexed among all devices. Apart from the area efficiency achieved by using a single ADC, this ensures that any non-idealities in the ADC are common to all DUTs and therefore do not affect the results. We have chosen to use a hierarchical access scheme analagous to a memory, with rows, columns and sections. Each bank contains 128 PMOS and 128 NMOS DUTs organized in columns, and each section contains 90 rows of banks. Bank enable pass gates steer only the current of the selected device to the measurement circuitry. The test-chip contains 540 banks organized into 6 sections for a total of 540 banks $\times$ 128 columns $=$ $69\,120$ DUTs of each type in a 2 mm $\times$ 2 mm array. All device lengths are minimum length for this technology $(0.18\ \mu$m$)$. The lower portion of this array contains banks with random designed device width ranging from $0.28\ \mu$m, the minimum allowable, to $3\ \mu$m, while in the upper half of the array, each row contains the same device width.

While the row and column access transistors introduce resistance and variation, HSpice simulations show that a $\pm 10\%$ variation in either L or V_T of the access transistors has $< 0.5\%$ effect (Section II-C) on $I_{\rm DS}$ of the DUT being accessed. Despite column access transistors being turned completely off for all other DUTs, a finite leakage current, $I_{\rm leak}$, through the row and column access transistors and the "off" DUTs adds to the $I_{\rm DS}$ of the DUT being accessed. When $I_{\rm DS}$ of the accessed DUT is large, corresponding to a larger $V_{\rm GS}$, $I_{\rm leak}$ is a negligible component and can safely be ignored. However, as described in Section II-A, it is desirable to set $V_{\rm GS}$ as low as possible to benefit from the convergence of n at low $V_{\rm GS}$. At gate biases below 0.25 V, $I_{\rm DS}$ reduces to nanoamps or smaller, so that even small drain-source leakage currents and drain/source-body junction currents accumulate over the "off" DUTs and their access transistors.

Each of the bank enable pass gates are high-V_T devices to minimize these parasitic leakage currents emanating from unaccessed devices. However, even with very small parasitic leakage currents from each of these pass gates, the large number of gates can result in these parasitic currents summing to a current large

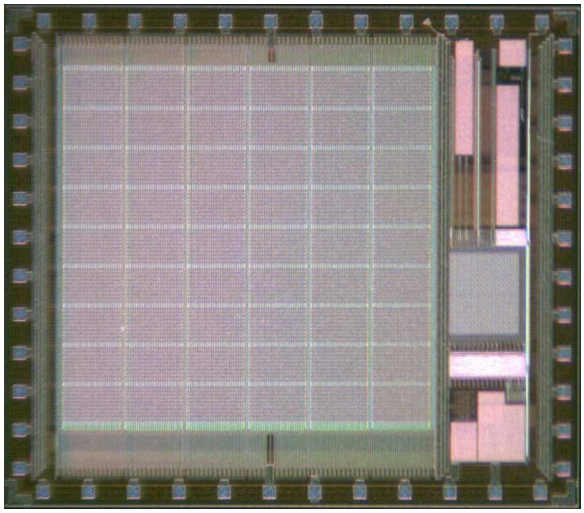


Fig. 3. Test-chip die photo. The DUT array is shown at left, with the ADC and digital control and calibtration blocks at right.

enough to interfere with the current being measured. An active current subtraction scheme was devised and implemented on-chip as shown in Fig. 1. Two (source and sink) 8-bit thermometer-code DACs [21] with digital control logic are added to actively add or subtract current equivalent to $-I_{\rm leak}$. The digital logic implements a binary search algorithm that uses the output of the ADC to converge upon the correct DAC input value and acts as an auto-zeroing mechanism. For example, when trying to measure the first NMOS DUT in a bank, the auto-zeroing is first run when all DUTs in the bank are off. If the ADC output is anything, but 0, after the first auto-zeroing measurement, the digital logic will completely turn on one of the two DACs shown in Fig. 1 in response to the direction of $I_{\rm leak}$. If $I_{\rm leak}$ is being drawn from the measurement circuitry to ground, the algorithm turns on the source DAC (top of Fig. 1) in order to "source" $I_{\rm leak}$ and remove its effect from the measurement. Analogously, the algorithm will turn on the sink DAC (bottom of Fig. 1) to "sink" an $I_{\rm leak}$ flowing from V_{DD} to the measurement circuitry. Subsequent measurements are used to refine the DAC control word in a logarithmic fashion. Auto-zeroing is performed once for each bank being tested at a specific gate bias. Due to the discrete nature of a DAC as well as limited resolution, the auto-zeroing will not be perfect, and residual $I_{\rm leak}$ is treated as an offset and subtracted from DUT current measurements.

The test-chip was implemented on a National Semiconductor $0.18\ \mu$m bulk CMOS process. Fig. 3 is a die photo showing the $3.2\ \text{mm} \times 2.7\ \text{mm}$ test-chip, of which $2\ \text{mm} \times 2\ \text{mm}$ is the dense DUT array.

C. Simulation Results of $\triangle V_T$ Isolation

We next present simulation results showing that the above theory and circuits are effective in isolating and extracting $\triangle V_T$ even in the presence of other types of variation, particularly channel length variation. Furthermore, simulations show that the multiplexing circuitry contributes a negligible error in the measured current.

1) V_T Isolation: Simulations were performed in which a single DUT, with row and column access transistors, charges an integrating capacitor. Since the operational amplifier forces a virtual ground at the inputs, $V_{\rm DS}$ remains constant as the capacitor is being charged, and $I_{\rm DS}$ can then be found using $I_{\rm DS} = C \cdot \triangle V / \triangle t$. Simulations were performed with DUT V_T and channel length being varied by $\pm 10\%$ and $V_{\rm DS}$ being varied across the allowable range, determined by the output stage of the operational amplifier. The range in this design is 0.3 V–1.5 V.

The plots in Fig. 4(a) show the simulation results. The top plot in the figure varies DUT V_T and $V_{\rm DS}$, while the bottom plot varies DUT channel length and $V_{\rm DS}$. Both plots show the relative change in current from the nominal V_T or L at a given value of $V_{\rm DS}$. The plots clearly show that the arrangement detailed above is more sensitive to changes in $I_{\rm DS}$ as a result of V_T variation rather than L variation, especially at low $V_{\rm DS}$. These results are consistent with the theory outlined in Section II-A.

To quantify these results further, the sensitivity of $I_{\rm DS}$ to either $\triangle V_T$ or $\triangle L$ can be computed by taking the derivative with respect to $\triangle V_T$ and $\triangle L$, respectively. Taking the ratio of these derivatives gives the relative sensitivity of the circuit to $\triangle V_T$ and $\triangle L$. Since it is clear from Fig. 4(a) that the circuit is least sensitive to $\triangle L$ at low values of $V_{\rm DS}$, these derivatives are only calculated for the lowest $V_{\rm DS}$ value allowable, 0.3 V. Fig. 4(b) plots the ratio of $\triangle I_D / \triangle L$ to $\triangle I_D / \triangle V_T$ for $V_{\rm GS}$ ranging from 0.35 V to 0.5 V. Lower values of $V_{\rm GS}$ are not plotted, as a trend in decreasing sensitivity to $\triangle L$ with larger values of $V_{\rm GS}$ is evident from the figure. However, Section II-A discussed employing lower values of $V_{\rm GS}$, where the value of n converges despite variation. The results of sensitivity analysis imply that simply measuring the value of n, as discussed in Section II-A, and using a $V_{\rm GS}$ near the nominal V_T for the process provide more benefit in extracting $\triangle V_T$ than attempting measurements at extremely low gate biases. Furthermore, low gate bias values increase the resolution and dynamic range requirements of the ADC, and even more attention must be paid to preventing $I_{\rm leak}$ currents from unselected DUTs.

For all values of $V_{\rm GS}$ plotted, the sensitivity ratio through the majority of the variation range is below 0.1, meaning the circuit is at least 10X more sensitive to V_T variation than to L variation. This is particularly true for $|V_{\rm GS}| = 0.35$ V where all but the endpoints remain < 0.1. Furthermore, sensitivity to V_T variation peaks in the vicinity of the nominal values of V_T and L. Since variation in these parameters are typically normally distributed about the nominal value, the majority of variation measured will be in the high-V_T-selectivity region of operation, giving high confidence that the measured $I_{\rm DS}$ variation is primarily a result of threshold voltage variation.

Simulations were performed where a transistor was subjected to variation (V_T or L or both) and the ADC outputs used to determine the amount of variation with both (6) and (7). All simulations were done with $|V_{\rm GS}| = 0.35$ V and $|V_{\rm DS}| = 0.3$ V and the ADC resolution set to 10 bits. Simulations were also done at $|V_{\rm GS}| = 0.345$ V, the results of which are used in conjunction with (3) to calculate n. Table II-C1 contains the results of these simulations showing the ability of the circuit to measure the known variations. It should be noted that the simulations where only V_T is varied result in approximately a 10% error in

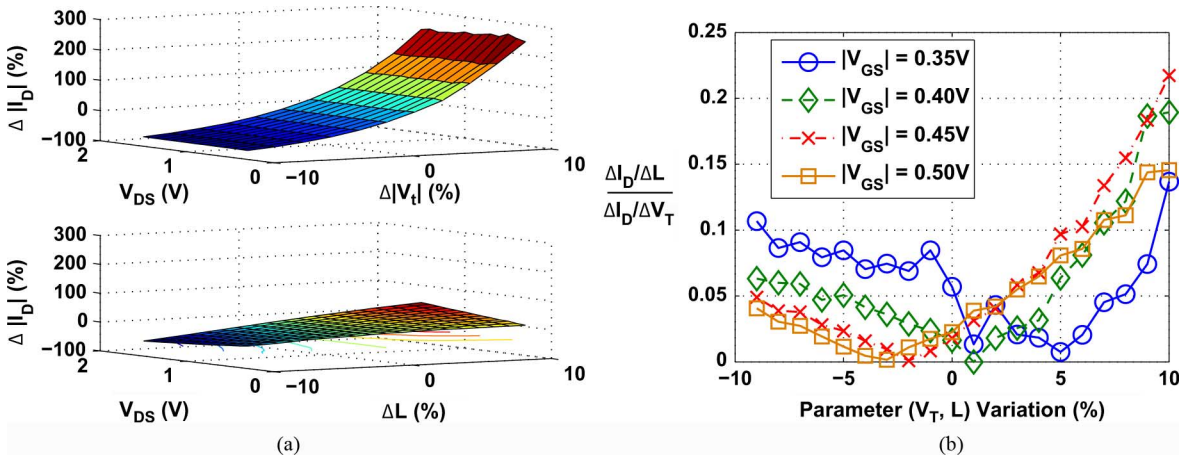


Fig. 4. Current sensitivity to variation in V_T, L. (a) Percent change in current from nominal value at a given $V_{\rm DS}$ when varying V_T (top plot) and channel length, L (bottom plot). (b) Circuit sensitivity ratio.

TABLE I
EXTRACTED V_T VARIATION VERSUS SUBJECTED VARIATION

Variation Type	Extracted $\triangle V_T$
$+10\%V_T$	$+10.9\%$
$-10\%V_T$	-11.0%
$+10\%V_T, +10\%L$	$+11.9\%$
$+10\%V_T, -10\%L$	$+9.3\%$
$-10\%V_T, -10\%L$	-12.0%
$-10\%V_T, +10\%L$	-11.3%
$+3\%V_T, +3\%L$	$+3.6\%$
$-3\%V_T, -3\%L$	-3.1%

TABLE II
SIMULATED CURRENT DIFFERENCES DUE TO INCLUSION AND VARIATION WITHIN ACCESS TRANSISTORS ($|V_{\rm GS}| = 0.35$ V AND $|V_{\rm DS}| = 0.3$ V)

Test Scheme	Relative Difference
DUT w/o access transistors	0.00%
DUT w/access transistors	-0.43%
DUT with $-10\%\triangle L$ in access transistors	0.26%
DUT with $-10\%\triangle V_T$ in access transistors	0.23%

the extracted deltas, primarily a result of the inherent inaccuracy in using (6) which does not account for n varying simultaneously. This alone would indicate that this test-structure can resolve deltas of approximately 1% of the nominal V_T. However, since the sensitivity of the circuit to V_T variation is not infinite, resolution is reduced to approximately 2% of nominal V_T.

2) Access Transistor and Resistance Effects: In order to hierarchically access a large number of DUTs within an array, each DUT requires row and column access transistors, and each bank of DUTs requires a pass-gate. These devices introduce additional resistance, potentially lowering the $V_{\rm DS}$ and corresponding I_D of the DUT due to the finite $R_{\rm out}$ of the devices. However, operation in the subthreshold regime produces small currents which are not perturbed substantially by even fairly large resistances. Simulations were carried out to evaluate this impact. The test circuit was used in these simulations with and without row, column and bank access transistors. Table II-C2 shows that the impact of these transistors and variation within them is less than 0.5% of the simulated current without any access transistors.

Another possible source of inaccuracy in implementing a large array is variation in the distance current must travel to the measurement circuitry, resulting in different resistances seen by each DUT to the ADC. However, simulations show that even with a 1 kΩ difference in resistance, the relative current difference is only 0.1%. Furthermore, the path from each DUT bank to the ADC is implemented as a dense metal grid spanning multiple metal layers to provide the lowest possible resistance. Process data and simulations indicate that a minimum width wire spanning 2 mm has a resistance of approximately 500 Ω. However, the grid is implemented with many 3X minimum-width wires spanning four metal layers, decreasing the overall resistance substantially. Since the resistance difference between any two DUTs cannot be more than the resistance of a single minimum-width wire spanning the entire array, we conclude that resistance variations in the grid will have negligible effect on measured currents.

III. DATA ANALYSIS

We next examine the measured currents from > 50 K devices on each of 36 chips. We first consider the ADC performance in measuring currents, followed by extraction of $\triangle V_T$ from our data. We then analyze device size and separation distance dependencies, and other within- and between-die spatial dependencies.

A. ADC Performance

We first characterize the static performance of the ADC, as this component is critical to our current measurements. Since the input to the ADC is a DC current, dynamic ADC performance is intentionally omitted as it has no effect on the measured currents. To alleviate noise concerns, measurements are repeated ten times and the average over the ten runs is used, as we assume white noise. In light of the limited input to the ADC, the primary metric we characterize is the integral nonlinearity (INL), as this gives the effective resolution of the ADC. Fig. 5 is a plot of the

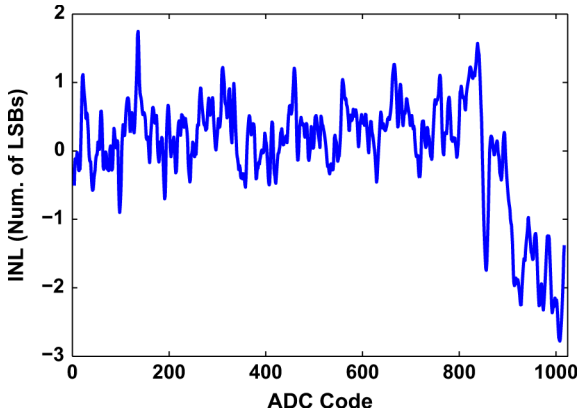


Fig. 5. INL plot for a single ADC.

INL versus ADC code for a single chip, when the ADC is configured for 10-bit resolution and 600-nA full-scale current. At the high-end of the ADC range, the INL begins to degrade due to limited bandwidth of the operational amplifier. This limits the maximum full-scale current to ≈ 600 nA. However, a redesign of the operational amplifier could remove this limitation in future designs. The INL for the ADC shown in Fig. 5 leads to an effective linearity of $10 - \log_2(\mathrm{MAX(INL)} - \mathrm{MIN(INL)}) = 7.81$ bits. Out of the 36 chips measured, the worst case effective linearity is ≈ 6 bits, resulting in an effective resolution of $600\ \mathrm{nA}/2^6 = 9.375$ nA. The minimum resolvable $\triangle V_T$ is then computed according to (6), where I_2 is the maximum current measurable by the ADC, I_1 is the current one ADC step below the maximum current and n is conservatively estimated to be 1.5 for this process. This gives $\triangle V_{T_{\mathrm{MIN}}} = 0.6$ mV, or 0.14% of the nominal V_T for this process—below the 2% limit detailed in Section II-C—giving high confidence that ADC nonlinearity contributes negligible error to the extraction of $\triangle V_T$.

Implementation limitations resulted in disabling of the autozeroing DACs intended to cancel the off-DUT leakage currents. However, each bank is still calibrated by first doing a current measurement with that bank's pass gate enabled but with no device enabled. Subtracting this measurement from the measured device current gives the true subthreshold current of the enabled device, but limits the dynamic range of the ADC.

B. Current Measurements and Extracted $\triangle V_T$

Using the analysis in Section II-A and measured currents from DUTs within the array, we compute $\triangle V_T$ for each device with respect to a reference device in the corner of the array. The values of n needed for the computation are extracted by measuring currents at different V_{GS} biases ($0.275\ \mathrm{V} \leq |V_{\mathrm{GS}}| \leq 0.3$ V in 5 mV increments) and computing a best-line fit on a semilog scale. The slope of this line relative to the ideal 60 mV/decade gives n. A spatial plot of n for one die is shown in Fig. 6(a). From this plot, it is evident that n does vary, although the magnitude is small, so using the average value of n between two devices in computing the $\triangle V_T$ introduces only small errors[3]. Furthermore, due to the limits placed on the full-scale current by the degraded linearity at high current levels (Section III-A), extracting an absolute V_T to use in (7) is impossible, limiting calculation of $\triangle V_T$ to the formulation given by (6). This limitation can also be overcome in future designs.

Once n has been computed from the measured currents for each device, we compute $\triangle V_T$. Fig. 6(b) illustrates the $\triangle V_T$ from each device to the reference device in the bottom right corner of the array for an example chip. While it appears that there may be some correlation in the upper half of the array, this is only due to the systematic designed device width pattern from row to row in this section of the array, resulting in a shift in standard deviation but not correlation as will be shown in the following spatial analyses.

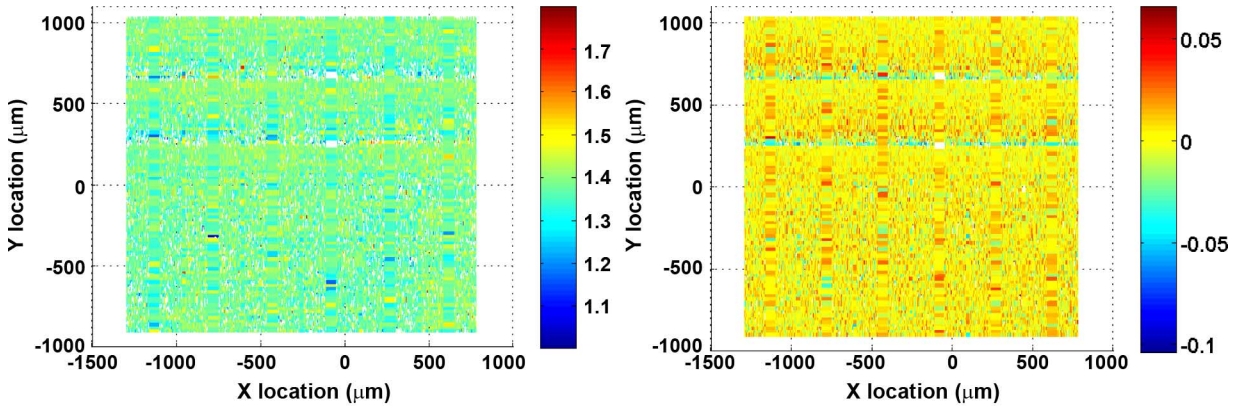
C. Pelgrom Modeling

To understand the effect of device size on standard deviation, we first show a Pelgrom plot of standard deviation of V_T versus $1/\sqrt{\mathrm{Area}}$ [22]. We note that $\sigma(V_T) = \sigma(\triangle V_T)$, where $\triangle V_T$ is with respect to our specified reference device. Based on Pelgrom's theory, we expect to see a linear relationship between $\sigma(V_T)$ and $1/\sqrt{\mathrm{Area}}$. Fig. 7(a) shows this linear relationship for a single chip, where σ has been normalized relative to that for a device having W/L of $0.92\ \mu\mathrm{m}/0.18\ \mu$m. Ideally, the best-fit line should pass through 0, indicating that devices of infinite area should have a standard deviation of 0. Deviation from this ideal in our data may be a result of ADC measurement resolution. Specifically, the data for many of the smallest devices in the array ($W < 0.8\ \mu$m) is excluded as their extremely small currents are smaller than the resolution of the implemented ADC. In such cases, data is either nonexistent (measured values being 0 as the currents were below the resolution of the ADC), or when data was present, gives unrealistic values of $n \gg 2$ due to the large ratio of ADC step size versus absolute current being measured at the bottom of the ADC range. Data is excluded by examining the computed values of n and excluding any devices with a computed $n < 1.0$ or $n > 1.8$. The majority of the excluded data is for small device sizes in the tails of the distribution, artificially lowering the standard deviation for these device sizes. As a result, the data points on the far right of Fig. 7(a) tend to be slightly below the linear fit, and may also cause the fit line to no longer pass through 0. In all further plots and data analysis, the data for devices with $W < 0.8\ \mu$m is excluded to ensure data integrity. We believe that all trends in the data remain applicable to the small device sizes in this technology.

The Pelgrom model includes two terms: 1) an area dependent term with proportionality $A^2_{V_{T0}}$ and 2) a distance dependent term with proportionality $S^2_{V_{T0}}$, as shown in (8). Fig. 7(a) shows a clear dependence on device area, but Fig. 7(b) shows no significant distance dependency. In Fig. 7(b), all pairs of devices within a specific chip having the indicated separation distance D are considered, and the standard deviation, normalized to a $0.92\ \mu\mathrm{m}/0.18\ \mu$m device, across all those pairs is plotted. Results show that placing devices nearer to each other does not decrease the variance between them. This will be discussed further in Section IV:

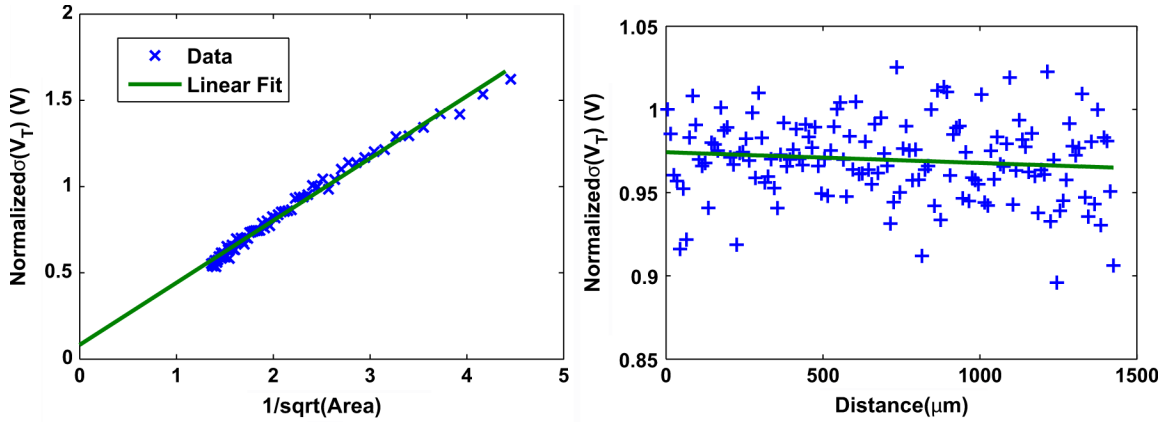
$$\sigma^2(V_{T0}) = \frac{A^2_{V_{T0}}}{WL} + S^2_{V_{T0}} D^2. \tag{8}$$

[3]The error is less than $< 10\%$, as this is the error when no attempt is made to account for n varying as discussed in Section II-C1.



(a) Subthershold ideality parameter (n) (b) ΔV_T

Fig. 6. Spatial distributions of n and V_T for a single die.



(a) (b)

Fig. 7. Pelgrom fits of $\sigma\,(V_T)$. (a) $\sigma(V_T)$ versus $1/\sqrt{Area}$. (b) $\sigma(V_T)$ versus Distance.

D. Intra-Die Spatial Correlation

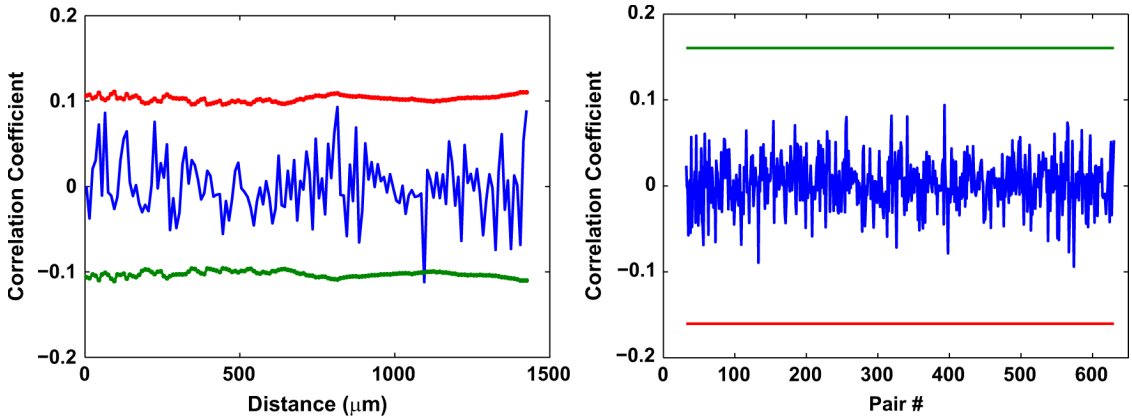
Since $\sigma(V_T)$ depends on device size, separate spatial correlation analysis by individual device size is necessary. Intra-die spatial correlation analysis is performed by computing the correlation coefficient for all devices separated by some distance, D, where $0 \leq D \leq 0.5 \cdot \sqrt{\text{Array}_X^2 + \text{Array}_Y^2}$ as shown in (9), where DVT is the $\triangle V_T$ between a given device and the reference device. These correlation coefficients are then plotted versus separation distance in Fig. 8(a) for a device size of $0.92\ \mu\text{m}/0.18\ \mu\text{m}$. The $\pm 3\sigma$ bounds to determine statistical significance (as a function of the number of available pairs having separation D) are also shown on the plot. No spatial correlation is seen, as all data points fall within the significance bounds. Though this plot shows the data from only one device size on one chip, similar plots (omitted due to space constraints) for other device sizes and chips reveal the same conclusion:

$$\rho_{DVT,DVT\pm D}(D) = \frac{\text{Cov}(DVT, DVT \pm D)}{\sigma^2_{DVT}}. \qquad (9)$$

The lack of spatial correlation indicates that V_T variation is random, and we find it to be normally distributed. Fig. 9 indicates that over 99% of the data points in this data set are indeed normally distributed. As supported by the measurement results at more scaled nodes, such as in [10], [11], [14], this leads to the conclusion that V_T variation must be dominated by random dopant fluctuation (RDF), even at the $0.18\,\mu\text{m}$ technology node. Although line-edge roughness (LER) should be considered as a possible cause of random variation, the $0.18\ \mu\text{m}$ technology node is likely not affected by subresolution patterning affects to the same degree as a 90- or 65-nm process. Furthermore, by measuring subthreshold currents and reducing V_{DS}, we reduce the DIBL effect and minimize any current variations due to channel length variation. Additionally, oxide thickness is relatively well controlled and variation in this parameter is likely to be more spatially smooth. We note that smaller device sizes, including any excluded by our ADC resolution screening procedure, would be expected to be even more susceptible to RDF; an interesting result here is that RDF is discernable and dominates even for larger device sizes.

E. Die-to-Die Correlation

Given the lack of any significant intra-die spatial correlation, inter-die correlation is only expected if the standard deviation of the mean shift between each die is considerably larger than the within-die standard deviation (i.e., $\sigma_{\text{die-to-die}} > \sigma_{\text{intra-die}}$). Computing this requires the absolute V_T for the reference device on each chip, which necessitates current measurements to determine where the I_D versus V_{GS} curve breaks from a straight line on a semilog plot. However, due to the limited dynamic range



(a) Intra-Die Spatial Correlation (b) Die-to-Die Variation Pattern Correlation

Fig. 8. Intra-die correlation versus distance and die-to-die pattern correlation.

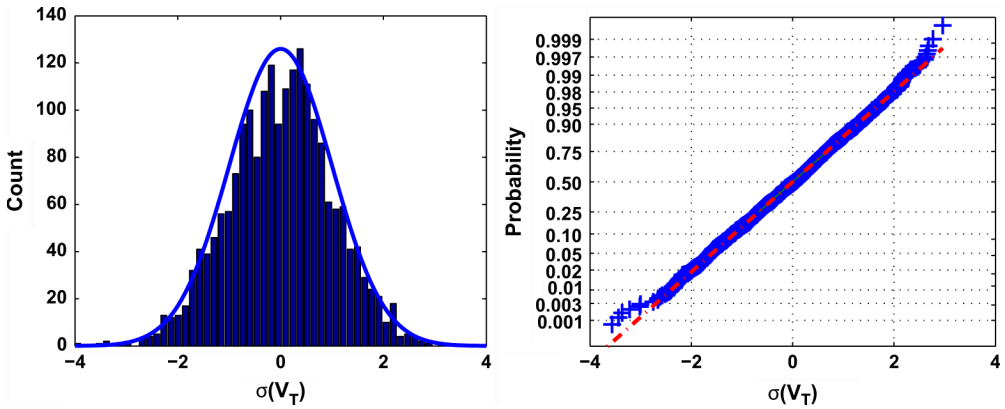


Fig. 9. V_T distribution and normal probability plot for a single die.

of the on-chip ADC, we were unable to measure currents significantly larger than 600 nA, making it impossible to determine an absolute V_T for each reference device. Nevertheless, we are still able to compute correlations in the spatial variation patterns between arbitrary pairs of die. Once again, we choose a single device size to analyze and compute the correlation coefficient, $\rho(i,j)$, between pairs of die using (10), where $DVT_{i_{(x,y)}}$ and $DVT_{j_{(x,y)}}$ are the $\triangle V_T$ of identical devices located at (x,y) on die i and die j, respectively, and μ_i, μ_j, σ_i, σ_j are the means and standard deviations of $\triangle V_T$ of all devices of the given size on dies i and j, respectively. Fig. 8(b) shows the correlation coefficient as a function of all $\binom{36}{2} = 630$ pairwise combinations. All data points fall within the 3σ significance bounds indicating no significant variation pattern similarity between pairs of dies. Larger device sizes show the same results:

$$\rho(i,j) = \frac{\mathrm{Cov}(i,j)}{\sigma_i \sigma_j} = \frac{\frac{1}{N}\sum_x \sum_y (DVT_{i_{(x,y)}} - \mu_i)(DVT_{j_{(x,y)}} - \mu_j)}{\sigma_i \sigma_j}. \quad (10)$$

The previous two subsections have shown that V_T variation is both random and spatially uncorrelated, implying that knowing the variation between two devices gives no further information about two similarly spaced devices on the same chip or even the same two devices on a different chip. This has powerful implications for both circuit designers and the modeling community.

IV. Design and Modeling Implications

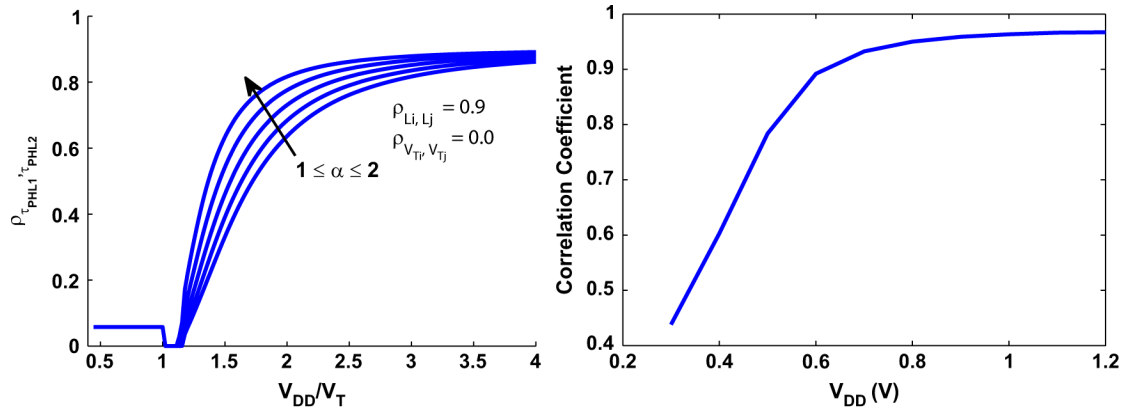
In order to determine the importance of the lack of correlation in V_T variation, we must determine the sensitivity of a given circuit or design to V_T variation. For example, it is well known that subthreshold circuit designs are highly susceptible to V_T variation, while channel length variation has minor impact in comparison. In general, computing circuit sensitivity to individual process parameters is not easily done analytically. However, we can consider a simple inverter where the power-supply to the inverter is scaled from subthreshold to well above V_T to illustrate the differing circuit sensitivities.

A. Circuit Modeling

For a simple inverter operating above-threshold, the propagation delay for a falling transition can be modeled as in (11). However, when the inverter is operating subthreshold, (11) is modified to (12):

$$\tau_{PHL} = \frac{C_L V_{DD}}{K_N \frac{W}{L}(V_{DD} - V_T)^{\alpha}} \quad (11)$$

$$\tau_{PHL} = \frac{C_L V_{DD}}{I_o e^{\frac{V_{DD} - V_T}{n V_{\mathrm{TH}}}}} \quad (12)$$



(a) Correlation in inverter propagation delay (b) Correlation in delay between RO and critical path of 64-bit KS adder

Fig. 10. Circuit performance correlation as a function of V_{DD}.

where $1 \leq \alpha \leq 2$ for modern processes and K_N is a constant determined by the process technology. Given the correlation coefficients for channel lengths $(\rho_{L1,L2})$ and threshold voltages $(\rho_{V_{T1},V_{T2}})$ between the NMOS transistors in two arbitrary inverters, it should be possible to compute the correlation coefficient for their propagation delays. In general, this is a difficult problem to solve analytically, but Monte Carlo simulations provide insight. To setup these simulations, we use the *delvto* parameter in Hspice to apply completely random variation in V_{T_o} and we modify gate lengths in the spice deck using correlated random variation of $\rho_{L1,L2} = 0.9$. This was done in accordance with our results showing lack of correlation in V_{T_o} and the spatial correlation results in L from [9] to highlight the differing impacts of correlated versus uncorrelated variation in different circuit operating regimes.

We easily see in Fig. 10(a) that the overall correlation contains some interesting characteristics. When $V_{DD} > 2V_T$, the correlation asymptotically grows toward $\rho_{L1,L2}$. However, around $V_{DD} = 2V_T$, the correlation falls precipitously, indicating that the gate overdrive is no longer sufficient to mask out RDF-dominated V_T variation. Since (11) becomes less applicable when $V_{DD} \approx V_T$, the computed $\rho_{\tau_{PHL1},\tau_{PHL2}} = 0$, but below V_T it settles to an extremely weak correlation, indicative of the dominant role of V_T in determining subthreshold current.

For simple logic gates, assuming channel length and V_T variation are independent, one can safely assume that $\rho_{\tau_{PHL1},\tau_{PHL2}} \approx \rho_{L1,L2}$ when $V_{DD} \gg V_T$. In contrast, in the subthreshold region it is safe to assume $\rho_{\tau_{PHL1},\tau_{PHL2}} \approx 0$ due to the lack of correlation in V_T variation.

This result demonstrates the importance of modeling correlations in each device parameter individually: the correlation of the particular circuit output metric is, in general, a nonlinear function of the correlations in each device parameter. Furthermore, the overall circuit performance correlation is highly dependent on circuit operating region and the circuit's sensitivity to individual device parameters within the operating region. For regions of operation where correlation is low or insignificant, methods for modeling variation as uncorrelated IID statistics are appropriate, using Monte Carlo or distribution propagation approaches.

B. Circuit Design

Designers face many decisions in today's complex circuits. Increased variation means that designers must now consider how best to ensure robust circuit operation. One approach is to design the circuit to operate correctly given the range and characteristics of known or estimated device variations. A more aggressive approach is to consider active variation sensing and compensation strategies. The results of the previous section imply that the designer must carefully consider the operating region of the circuit when evaluating either robust design or active compensation strategies to counteract variation.

In the above-threshold region where channel length variation dominates circuit performance variation, assuming that channel length variation is spatially correlated, variation sensors can be used to detect variation. Active compensation, such as back-biasing circuits, can then be used to counteract the detected variation. Given high spatial correlation $(\rho > 0.8)$ within a given radius, only one such variation sensor and compensation circuit is required within this radius.

In contrast, subthreshold operation results in no significant spatial correlation due to V_T or L variations. Additionally, Section III-C showed that the variance was not significantly related to distance. Consequently, a designer can only make use of the fact that the variance decreases with increasing device area, as increasing the size of a device effectively averages out variation due to Random Dopant Fluctuation. However, doing so results in negative power scaling due to increased total capacitance, and so there exists a trade-off between yield and power. In [23], the authors analyze the effect of increasing device width on the minimum energy point of subthreshold operation, showing that up-sizing for a constant yield has a negative effect on the minimum energy point. Another method of averaging out variation is to increase logic depth as in [24]. By increasing the number of devices in a logic path, the variance of the propagation delay of the entire path decreases. This technique can prove useful in designs where operating frequency is not the primary metric.

In ultra-dynamic voltage frequency scaling (UDVFS) systems, such as those in low-power systems like mobile devices or sensor networks, both subthreshold and above-threshold operation are used [25], [26]. Such systems often utilize replica

critical paths or variation sensors to determine the appropriate frequency to operate at for a given power-supply voltage. To determine how correlated these replicas are to the actual path they are monitoring while scaling V_{DD}, we performed Monte Carlo simulations with correlated channel length variation of a seven-stage ring-oscillator (RO) and a critical path of a 64-bit Kogge–Stone (KS) adder. Fig. 10(b) shows the results of a 1000-point Monte Carlo simulation with 65-nm predictive technology models [27], where $\rho_{Li,Lj} = 0.9$, $\rho_{V_{Ti},V_{Tj}} = 0$, $A_{V_T} = 5\ \text{mV} \cdot \mu\text{m}$, and $\sigma_L = 5\%$.

The overall correlation in delay between the two paths is ≈ 0.95 for $0.7\ \text{V} \leq V_{DD} \leq 1.2\ \text{V}$. The reason this is greater than $\rho_{Li,Lj}$ is that the load capacitance of the following stage is also correlated as a result of correlated variation in channel length, thereby increasing the overall correlation. In the region of $0.3\ \text{V} \leq V_{DD} \leq 0.7\ \text{V}$, the overall correlation between monitor and circuit decreases quickly, indicating that performance of the monitor/replica is no longer indicative of the performance of the critical path and should not be used to determine correct operating frequency unless a large guard-band is applied. Such a guard-band would undoubtedly subtract away from energy efficiencies achieved by moving to lower supply voltages. A more robust method of controlling operating frequency in such systems is to detect logic errors in potential critical paths and slow down the frequency until timing errors are no longer detected [28], [29].

V. Conclusion

We have implemented a test-chip to analyze spatial correlation of V_T variation. Analysis of the V_T variation data from this test-chip shows that there is neither intra-die spatial correlation nor inter-die correlation in the variation pattern between chips. Using the gathered statistics of V_T variation, we have shown that modeling of correlation in digital static timing is highly dependent on the circuit's region of operation, with timing correlation being approximately equal to channel length correlation when $V_{DD} \gg V_T$ and approximately zero in the subthreshold regime. To accurately model the derived correlation in timing characteristics for all regions of operation, it is necessary to model the correlation of both channel length and V_T variation independently. We have also shown that the design techniques necessary to ensure circuit robustness are equally dependent on the circuit's region of operation.

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