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Gate-All-Around n-MOSFETs With Uniaxial Tensile Strain-Induced Performance Enhancement Scalable to Sub-10-nm Nanowire Diameter

Pouya Hashemi, *Student Member, IEEE*, Leonardo Gomez, and Judy L. Hoyt, *Fellow, IEEE*

***Abstract*—The effects of high-level uniaxial tensile strain on the performance of gate-all-around (GAA) Si n-MOSFETs are investigated for nanowire (NW) diameters down to 8 nm. Suspended strained-Si NWs with ∼2-GPa uniaxial tension were realized by nanopatterning-induced unilateral relaxation of ultrathin-body 30% strained-Si-directly-on-insulator substrates. Based on these NWs, GAA strained-Si n-MOSFETs were fabricated with a Si thickness of ∼8 nm and NW widths in the range of 50 nm down to 8 nm. The GAA strained-Si MOSFETs show excellent subthreshold swing and cutoff behavior, and approximately two times current drive and intrinsic transconductance enhancement compared to similar unstrained Si devices.**

***Index Terms*—Gate all around (GAA), nanowire (NW), n-MOSFET, strained Si, uniaxial tensile.**

I. Introduction

MULTIGATE Si-based devices such as trigate or gate-all-around (GAA) nanowire (NW) MOSFETs are promising candidates for aggressively scaled CMOS due to their excellent electrostatics, low power consumption, and immunity to short channel effects [1], [2]. However, the carrier velocity of these devices is generally degraded due to quantum–mechanical confinement effects, as well as the nonideality of the NW sidewalls [3], [4]. The case is more severe for n-FETs, where the low-mobility (110) vertical sidewalls determine the overall performance of the device [4]. As a result, the strain engineering of the Si NW channel is critical to improve device performance. Patterning-induced lateral relaxation has been used to induce stress in FinFET [5] and trigate [6] n-FETs. However, there are very few reports on the performance enhancement of GAA NWs [7], [8]. In that work, nonuniform process-induced strain resulted in bending of the NWs, making them incompatible with ultralarge-scale CMOS integration. We have recently demonstrated the fabrication of suspended uniaxial strained-Si NWs with stress levels as high as ∼2 GPa [9], with promising extrinsic performance [10]. In this letter, the intrinsic performance of GAA strained-Si n-MOSFETs, based on these NWs, is investigated for various NW dimensions. In addition, the scalability of the GAA strained-Si channel to 8-nm NW diameters is demonstrated, for the first time.

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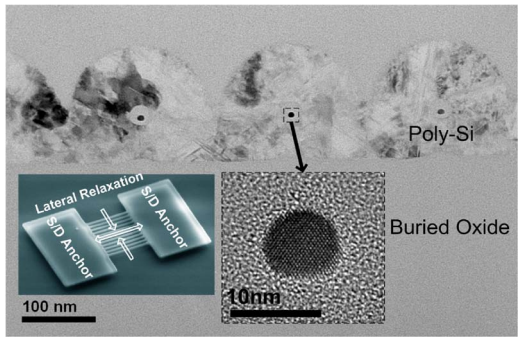

Fig. 1. Cross-sectional TEM image of GAA strained-Si n-MOSFET, looking down the axis of the NWs, showing parallel circular NWs with width $W_{\mathrm{NW}} \sim 8$ nm, thickness $t_{\mathrm{NW}} \sim 8$ nm, and LTO gate dielectric. Inset at left shows the tilted-view SEM image of the Si structure with ten parallel suspended strained-Si NWs (strained in longitudinal uniaxial tension) fabricated by lateral relaxation and undercutting the NWs.

II. Device Design and Fabrication

Starting substrates were 6-in 30% strained-Si-directly-on-insulator wafers (strained to $Si_{0.7}Ge_{0.3}$ virtual substrates), fabricated utilizing a bond-and-etch-back technique [11]. These substrates were biaxially strained to 2.16-GPa tension, as confirmed by UV micro-Raman spectroscopy [10]. The Si layers were thinned to 21 nm by wet chemical oxidation and oxide removal. For comparison, unstrained SOI wafers (thinned down to similar thickness by multiple steps of dry oxidation and oxide removal) were used as control devices. Active layers were patterned by hybrid lithography, where ⟨110⟩-oriented multiple NWs (with widths of 20–60 nm) were defined by e-beam lithography, and the source/drain (S/D) pads were defined by photolithography. The ⟨110⟩ NW orientation was chosen to gain the maximum uniaxial strain-induced performance [6], [12]. The active layers were mesa etched by reactive ion etching, and NWs were then suspended by time-controlled wet etching of the buried oxide. The inset in Fig. 1 shows a SEM micrograph of 20-nm-wide suspended strained-Si NWs. The NWs were previously shown to be uniaxially strained to a high stress level of ∼2 GPa, with little dependence on NW width [9]. This magnitude of stress is higher than the previously reported for strained-Si FinFET or trigate n-FETs [5], [6]. After

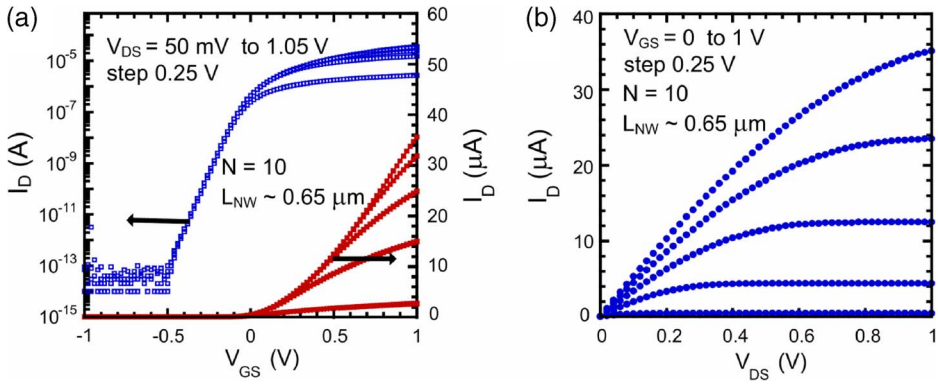

Fig. 2. Typical (a) transfer (I_D–$V_{\rm GS}$) and (b) output characteristics (I_D–$V_{\rm DS}$) for a circular cross-sectional GAA strained-Si NW MOSFET with $N = 10$ NWs, average NW diameter $d_{\rm avg} \sim 8$ nm, and $L_{\rm NW} \sim 0.65$ μm.

RCA cleaning, the NWs were wrapped with low temperature oxide (LTO) and *in situ* n^+-doped poly-Si. Devices with gate lengths in the range of 0.5 to 4 μm were fabricated. S/D regions were then implanted with phosphorus at an energy of 19 keV to a dose of 3×10^{15} cm^{-2}. After poly-Si stringer etch and interlayer-dielectric deposition, S/D regions were activated by rapid thermal annealing at 625 °C for 2 min followed by 800 °C for 10 s. Ti/Al metallization and N_2/H_2 annealing finalize device fabrication. The fabrication yield was improved for the strained devices relative to the unstrained ones, as the uniform tensile strain prevents bending during processing. The device dimensions were calibrated by SEM and cross-sectional TEM. Based on these calibrations, NWs were laterally thinned to various widths in the range of 50 to 8 nm and vertically thinned to thicknesses of ~8 nm, and the corners were rounded during processing. Fig. 1 shows a cross-sectional TEM image of a strained-Si NW device with an average radius of ~4 nm. The lattice image in the inset indicates perfect crystalline structure in the NW channel. It should be noted that stress measurement after device fabrication is very challenging, as the NWs are surrounded by the gate stack.

III. Results and Discussion

Fig. 2 shows the typical (a) transfer (I_D–$V_{\rm GS}$) and (b) output characteristics (I_D–$V_{\rm DS}$) for a circular cross-sectional GAA strained-Si NW n-MOSFET with $N = 10$ parallel NWs, an average NW diameter of ~8 nm, and $L_{\rm NW} \sim 0.65$ μm, corresponding to the TEM image in Fig. 1. The device shows excellent long channel subthreshold behavior, with a subthreshold swing of $SS = 67$ mV/dec and high $I_{\rm on}/I_{\rm off}$. Devices with wider NWs show an SS as steep as 64 mV/dec, indicating high quality interface between LTO gate dielectric and NW channel.

In order to evaluate the effects of uniaxial strain on the performance of GAA n-MOSFETs, the transfer characteristics of 1-μm-long GAA strained-Si NW (SSOI NW) and unstrained Si NW (SOI NW) n-MOSFETs are shown in Fig. 3(a). For fair comparison, both strained and unstrained NWs have similar dimensions with a thickness of ~8 nm and a width of ~20 nm. Devices exhibit an excellent SS of 65 mV/dec. In addition, the GAA strained-Si device shows 1.95X current drive enhancement compared to unstrained-Si device at a fairly

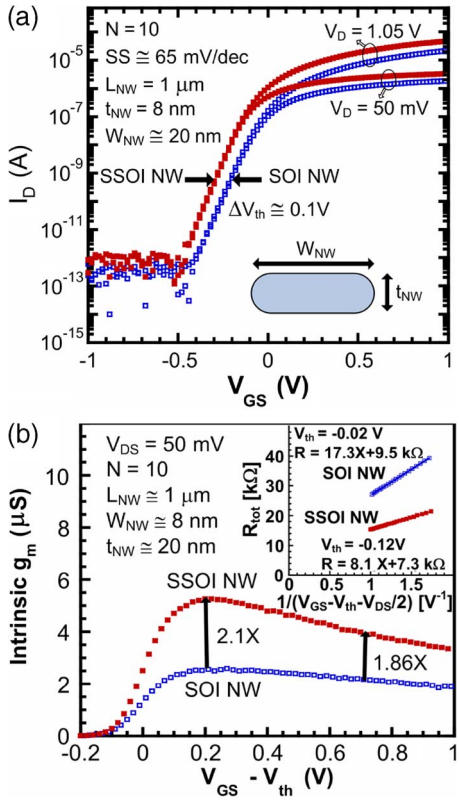

Fig. 3. (a) Transfer characteristics of GAA Si and strained-Si NW n-MOSFETs (with LTO gate dielectric) showing near ideal $SS = 65$ mV/dec, approximately two-times current enhancement, and 100-mV strain-induced $V_{\rm th}$ shift. (b) Intrinsic g_m of SOI and SSOI NWs versus $V_{\rm GS} - V_{\rm th}$ ($W_{\rm NW} \cong 20$ nm; $t_{\rm NW} = 8$ nm) after correction for $R_{\rm ext}$. Inset shows the $R_{\rm ext}$ extraction method for these devices. Enhancement factors of 2.1X at maximum g_m and 1.86X at $V_{\rm GS} - V_{\rm th} = 0.7$ V are due to the uniaxial strain.

low overdrive voltage ($V_{\rm GS} - V_{\rm th}$) range. At higher overdrive voltages, the enhancement is slightly degraded due to increased contribution of series resistance, due to the high resistivity of the ultrathin-body S/D regions. The strained-Si GAA device shows a negative threshold voltage shift of ~0.1 V compared to the unstrained-Si device. This shift is attributed to strain-induced conduction band edge lowering [6], confirming the presence of uniaxial tension in the NWs after processing.

To determine the intrinsic transconductance ($g_{m,\rm int}$) of these devices, the series resistance ($R_{\rm ext}$) was extracted by plotting

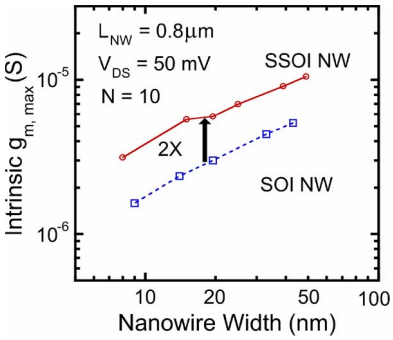

Fig. 4. Intrinsic $g_{m,\max}(V_{\rm DS} = 50$ mV) versus $W_{\rm NW}$ for SOI and SSOI GAA devices with $L_{\rm NW} = 0.8$ μm, $t_{\rm NW} \sim 8 \pm 1$ nm, and $N = 10$, displaying an average enhancement in $g_{m,\max}$ of approximately two times down to sub-10-nm NW dimensions.

the linear total resistance $(R_{\rm tot} = V_{\rm DS}/I_D)$ versus $1/(V_{\rm GS} - V_{\rm th} - V_{\rm DS}/2)$, as shown in the inset of Fig. 3(b). The extracted total $R_{\rm ext}$ was ~7.3 kΩ for SSOI NW and ~9.5 kΩ for SOI NW devices. These values are in reasonable agreement with the results obtained by the L array method [13]. Fig. 3(b) shows the $g_{m,\rm int}$ of GAA strained and unstrained Si devices versus overdrive voltage, at $V_{\rm DS} = 50$ mV after correction for series resistance using the given values. The strained-Si NW device shows an enhancement in peak intrinsic g_m of approximately 2.1X compared to the unstrained Si NW device. Fig. 4 shows the maximum intrinsic transconductance $g_{m,\max}$ (measured at $V_{\rm DS} = 50$ mV and after correction for $R_{\rm ext}$) versus $W_{\rm NW}$ for unstrained and strained GAA devices, illustrating enhancement in $g_{m,\max}$ over the entire range of NW widths investigated. It should be noted that even a 2-kΩ (~25%) change in $R_{\rm ext}$ impacts $g_{m,\max}$ by less than 5% in these devices. An average enhancement of approximately two times extends to lateral dimensions in the sub-10-nm regime, indicating the significant effect of uniaxial strain in deeply scaled Si NWs. Similar enhancement was noted over the range of $L_{\rm NW}$ studied (0.4–1 μm).

IV. Conclusion

The performance of GAA n-MOSFETs with NW diameters down to ~8 nm has been explored. Based on suspended strained-Si NWs with initial uniaxial stress levels as high as 2 GPa, GAA strained-Si NW n-MOSFETs with excellent subthreshold characteristics were fabricated and characterized. The presence of strain in the suspended NWs was confirmed after device fabrication by the negative shift in the threshold voltage, due to uniaxial strain-induced conduction band lowering. An average of two-times enhancement in current drive and intrinsic transconductance has been demonstrated for NW widths from 50 nm down to 8 nm, indicating the promise of this approach for deeply scaled Si n-MOSFETs.

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