## Modeling of Advanced Integrated Circuit Planarization Processes:

# Electrochemical-Mechanical Planarization (eCMP), STI CMP using Non-Conventional Slurries

by

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B.S., Electrical Engineering, North Carolina State University, 2007 B.S., Computer Engineering, North Carolina State University, 2007

Submitted to the Department of Electrical Engineering and Computer Science

in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering and Computer Science at the

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#### Abstract

Progression of technology nodes in integrated circuit design is only possible if there are sustainable, cost-efficient processes by which these designs can be implemented. As future technologies are increasing device density, shrinking device dimensions, and employing novel structures, semiconductor processing must also advance to effectively and efficiently process these devices. Arguably one of the most critical, inefficient, poorly understood and costly processes is planarization. Thus, this thesis focuses on two types of planarization processes. Models of efficient and environmentally benign electrochemical-mechanical copper planarization (eCMP) are developed, with a focus on electrochemical mechanisms and wafer-scale uniformity. Specifically, previous models for eCMP are enhanced to consider the full electrochemical system driving planarization in eCMP. We explore the notion of electrochemical reactions at both the cathode and anode, in addition to lateral current flow in a time-averaged calculation. More efficient and accurate models for planarization of shallow-trench isolation (STI) structures are proposed, with a focus on die-scale and feature-scale uniformity. This thesis captures the fundamental weakness of CMP, pattern dependencies, and uses deposition profile effects as well as the pattern-density to more accurately model and physically represent STI structures during CMP. We model, for the first time, the evolution of pattern density as a function of time and step-height, and use layout biasing to account for deposition profile evolution for the accurate prediction of die and feature-scale CMP.

Thesis Supervisor: Duane S. Boning

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"Be anxious for nothing, but in everything by prayer and supplication, with thanks-giving, let your requests be made known to God and the peace of God, which surpasses all understanding, will guard your hearts and minds through Christ Jesus." Philippians 4:6-7

Giving honor to my Lord and Savior Jesus Christ, without whom I would not have the intelligence, strength, and motivation to have performed this work. Thank you Lord for loving me unconditionally and lavishly. You have been true to your word, you have brought me here, but not left me here and for that I am eternally grateful.

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### Chapter 1

#### Introduction

This chapter introduces the impetus for advanced integrated circuit planarization processes. A literature review of two planarization processes, and a conceptual review of the two respective types of modeling explored in this thesis are discussed. Lastly, the contributions of this thesis to academic and industrial knowledge are presented, and the organization of the remainder of the thesis is summarized.

# 1.1 Motivation for Modeling of Advanced IC Planarization

A product design is only as strong as the manufacturing process used to fabricate that design. Design progression of technology nodes is only possible if there are sustainable, cost-efficient processes by which these designs can be implemented. As future technologies are increasing device density, shrinking device dimensions and integrating novel device structures, semiconductor processing has to also consider alternative approaches and other evolutionary advances to effectively and efficiently process these devices. Arguably one of the most critical, inefficient, poorly understood and costly processes is planarization.

In order to achieve the critical planarity required by future (sub 22nm) technology nodes, there have to be new technology drivers in planarization, for both metal layers and dielectrics. One driver is in the form of models that reduce the consumable cost or consumable usage, which are also accurate enough to provide in-situ knowledge of the process and thus control process variation with optimal performance metrics. The question is modeling of what planarization steps? There are four primary types of planarization performed in IC manufacturing: oxide chemical mechanical polishing or planarization (CMP), Shallow Trench Isolation (STI) CMP, tungsten CMP, and copper CMP. This thesis will focus on the modeling of STI and copper CMP. STI CMP is performed in front-end fabrication to provide isolation between devices using a damascene process that involves dual material planarization. Copper CMP is performed in back-end fabrication to planarize the interconnect layers, and also involves multiple material planarization. While the STI geometry is planarized using traditional CMP, copper interconnects can be planarized one of two ways: by conventional CMP, or through a newly established process using voltage application during polishing known as electrochemical mechanical polishing, or eCMP.

Industry is starting to pull away from the intriguing thought of eCMP for copper planarization, which has significant potential benefits in wafer level uniformity, substantially lower consumable costs, environmentally benign waste and increased ease of process control. ECMP has typically been applied to bulk copper removal on the first platen within a three platen planarization process; existing eCMP processes still employ conventional CMP on the last two platens, to remove the remaining copper and barrier metal after bulk copper removal by eCMP. For industry to get a substantial return on investment (ROI) from this technology, it must replace more of the three-platen process and planarize the full copper layer down to the barrier, and possibly the barrier metal layer as well, using eCMP-based processes. To develop models that extend to a full range of eCMP processes is a large and intriguing challenge.

In order to see a more immediate and significant ROI, most semiconductor companies also need more accurate predictive conventional CMP models that are empirical in nature but physically based on the pad's properties. It is for this reason that the first half of this thesis will focus on CMP modeling of the STI process using novel slurries for consumable reduction and end-point accuracy. The second half of this the-

sis will then return to the modeling of eCMP, to lay the groundwork for the potential use of eCMP in future technology generations.

#### 1.2 Background: Planarization

Planarization is arguably one of the most critical and expensive parts of the silicon integrated circuit (IC) chip fabrication process; ironically it is also considered among the least understood and controlled processes. In 2003, the International Technology Roadmap for Semiconductors (ITRS) stated that "increasingly, planarization has become the enabling step for interconnect solutions. As materials and structures become less conventional and demands on planarization tolerances become more exacting, planarization processes themselves become more closely coupled to the choice of integration scheme" [12]. And again in the 2008 updates, ITRS identifies "planarization effects" as one of the "difficult challenges" for sub-22nm technology development [13].

Originally developed by IBM, chemical mechanical polishing (CMP) is the accepted process for planarizing both dielectric and metal layers. It has helped enable the increase in number of metal layers and the decrease in dimensions and tolerances over the years, but it is quickly approaching its limits in its current state. The supercession of Moore's law by the faster creation of new IC chips with more metal layers and complex scaled structures is placing more stringent demands on CMP that may be difficult to meet without the creation of novel process enhancements. Thus, there is an imperative need for "applications to expand to chemically complex materials and mechanically fragile structures which requires aggressive development of and improvements in all aspects of CMP, slurries, pads, and machines" [14]. These aforementioned applications must be implemented in order to maintain and/or reaffirm CMP as the "state of the art technology" for planarization. Since the mid-1990's, when the switch from aluminum to copper began, CMP has had a monopoly on the planarization processes in IC fabrication. It was not until industry began to approach the 65nm node that conventional CMP started to reveal difficult and possibly inher-

ent limitations. It was then that technologists realized that to continue device scaling with thinner interconnect layers and low-k dielectric films, and to allow the use of higher-resolution optics for photolithography with more stringent requirements, there had to be tighter planarization specifications and process control with lower downforce. It is not yet known if conventional CMP will be able to meet these future needs. A possible alternative solution is electrochemical mechanical planarization (eCMP) technology. As proposed by Applied Materials, eCMP seeks to rise to the challenge by providing a planarization process with dramatically lower downforce, ultra-low shear force, precise process control and reduced dishing and erosion, but with one caveat: it still requires conventional CMP to complete the removal of the remaining Cu and barrier metals [2].

## 1.2.1 Chemical Mechanical Polishing (Planarization) for Shallow Trench Isolation

In IC fabrication there are many process steps that require planarization, to build multi-layer structures as well as to create in-laid features. Primarily, conventional CMP is performed in the front-end to planarize dielectrics and damascene structures, including both single and dual material planarization in fabrication techniques like the commonly used Shallow Trench Isolation (STI), which is modeled in this thesis. STI is the only isolation scheme used in semiconductor manufacturing which can achieve active area pitches in the sub-0.25  $\mu$ m regime. Device isolation is desired in order to form a dielectric separation between the source and drain of neighboring transistors, preventing current leakage [15]. The STI process is the preferred isolation technique not only because it enables effective segregation of devices, but also because it has near zero field encroachment, good scalability, low junction capacitance, and good planarity [1]. STI structures are fabricated using a damascene, or inlaid material, process as shown in Figure 1-1.

First a thin pad oxide layer (approximately 100Å) is thermally grown to serve as an intercessory layer between the silicon substrate and the silicon nitride layer;

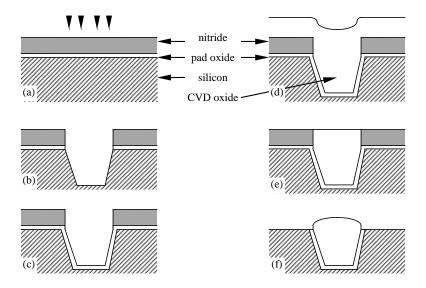


Figure 1-1: STI process flow summary: (a) pad oxide and nitride deposition, (b) anisotropic trench etch, (c) trench sidewall passivation, (d) trench fill, (e) CMP planarization, (f) nitride and pad oxide strip [1]

.

the nitride layer (approximately 1500Å) is deposited using chemical vapor deposition (CVD). Next, the trenches are fabricated using a lithography process and dry-etched to create approximately 5000Å deep trenches in the silicon substrate. The trenches are then filled with silicon oxide using CVD, forming a thick layer over both the nitride area and trenches. CMP is then used to remove the overburden of oxide until all of the oxide above the nitride has been removed. Requirements for the CMP process include high selectivity to stop planarization on the nitride, low erosion of the nitride, and low dishing to the oxide trenches. After planarization, the nitride and pad oxide are stripped, forming the inlaid structures as seen in Figure 1-1.

#### 1.2.2 Electro-chemical Mechanical Polishing (Planarization)

In the back-end of the IC fabrication process, planarization is used to form the metal interconnect layers. Currently copper is the metal of choice for interconnects because of its conductivity and reduced proclivity to electro-migration [7]. Traditionally, tungsten and aluminum have been used to form interconnects, and the aluminum lines have been fabricated with a subtractive dry etch process. Copper is very difficult to

dry etch, thus another CMP damascene process is used to create copper interconnects. This process is similar to that of dual material STI planarization, with the exception that its aim is to "clear the overburden copper and remove the barrier on top of the dielectric spaces separating the copper interconnect lines" [16].

As in STI CMP, requirements on the planarization include low erosion of the dielectric between copper features, and minimal dishing of the copper features. Since there is a highly conductive layer on the surface of the wafer in the damascene copper process, voltage application can be employed to aid in removal, thus the motivating advent of the eCMP process. ECMP is a process in which electrochemical removal is used as a replacement for the chemical-mechanical removal of copper in CMP. Brought to market by Applied Materials in 2005 [17], eCMP creates an equivalent two-electrode electrochemical cell in which the pad and the copper on its back surface serves as the cathode, and the Cu wafer serves as the anode as illustrated in Figure 1-2.

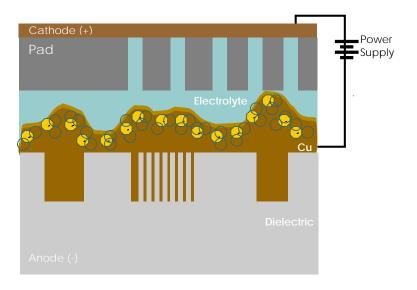


Figure 1-2: Illustration of eCMP setup.

Voltage is applied between the two electrodes; rather than using the traditional CMP slurry, an electrolyte is used to provide an ionic solution, which facilitates the oxidation of the copper atoms. In order to ensure that current is freely flowing from the positively biased pad electrode to the negatively biased wafer when voltage is applied, the wafer is grounded at a wafer contact region consisting of copper beads

which provide sufficient contact at the edge of the wafer [8]. This is shown in the basic hybrid eCMP setup in Figure 1-3.

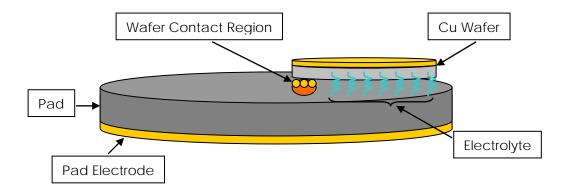


Figure 1-3: Illustration of hybrid eCMP setup.

Once the bias voltages reach a range of 1 to 3V, the applied potential initiates the oxidation (removal of one or two electrons) of the copper in its metallic form to its ions  $Cu^{2+}$  ( $Cu^{1+}$ ) as shown in Equations 1.1 and 1.2.

$$Cu \to Cu^{+2} + 2e^{-}$$
 (1.1)

$$Cu \to Cu^{+1} + 1e^{-}$$
 (1.2)

There exist two competing theories as to what happens next in the process. The first theory is that once oxidation occurs, the resulting Cu ions  $(Cu^{2+}/Cu^{1+})$  interact with the inhibitor in the electrolyte to create a soft passivation layer on the wafer surface which can easily be removed with relatively low downforce (less than 1 psi) while simultaenously protecting the trenches from dishing during planarization [18]. The second theory asserts that a layer of some protective polymer or other thin film is deposited on the Cu surface that has a much higher resistance than the exposed areas, and thus when it is mechanically removed by the pad it allows for localized Cu dissolution/removal [19]. In either case, the working assumption is that exposed Cu oxidizes into  $Cu^{2+}$  such that Cu removal can be calculated: for every two electrons of charge delivered, one Cu atom will be removed [8]. Therefore current density J and

time of current application can be used to calculate and model removal, which will be discussed in further detail in Chapter 3. However, the caveat to this process is that the Applied Materials tool still uses a three platen process, in which the second and third platens use conventional CMP to complete the Cu planarization process, as shown in Figure 1-4, because eCMP is currently unable to completely remove the remaining Cu and barrier metal.

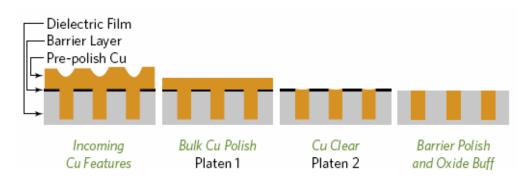


Figure 1-4: Reflexion LK eCMP process sequence [2].

#### 1.3 Background: Modeling

The fundamental reason why planarization is only partially understood and thus difficult to control is the large number of mechanisms which can affect it, including chemical, mechanical, physical, and now even electrical processes. Modeling helps to provide a foundation upon which we can derive an understanding of the matrix of mechanisms that affect the CMP process and its variation. Models allow us the flexibility to try and isolate from the matrix the contribution of a few key parameters in an attempt to predict the dominant effects as well as the variation of the process.

Modeling not only aids semiconductor manufacturers in immediate returns on investment like increased yield and decreased consumable costs, but models are essential to understand the mechanisms that enable removal of material and cause process variation, which affects device performance and process efficiency. In this thesis we will focus on two primary types of variation: die-level variation in STI CMP and wafer-level variation in eCMP. Die-level variation is the variation within a single die

or chip, which typically includes layout or pattern dependent variations in polishing rate, dishing, and erosion. Wafer-level variation is the variation over the entire wafer, which is typically observed as a non-uniformity of some geometric or material parameter, most commonly material thickness. Wafer-level modeling differs from that of die-level modeling in that it will capture tool limitations and process control issues, which is where the key learning begins for a new process like eCMP. In contrast, die-level models focus on the planarization capability of well-defined structures and processes, in order to create more viable process operating windows and pinpoint layout design weaknesses; this is more appropriate for a well developed existing process like STI CMP [7].

Much work has been done in the Boning research group here at MIT, to develop die-level and wafer-level, physical and semi-empirical models for STI and metal (copper) planarization. The work undertaken in this thesis is only possible because of the learning from the work of the following. Stine et al. demonstrated the strong correlation between CMP removal rate and pattern-density, to develop a pattern-density based model [20]. Observing possibilities for model improvements in accounting for pad deformation, Ouma et al. demonstrated the importance of effective patterndensity calculated using an elliptic weighting function [21]. After the advent of the IMEC step-height based model, Smith et al. demonstrated an integrated Pattern-Density and Step-Height (PDSH) model [22]. Bridging the gap between Ouma and Smith's work, Lee et al. devised an integrated PDSH model using effective patterndensity [23]. Gan et al. investigated reverse tone etch back CMP models, which study dishing and erosion predictors in this variant of STI processes [1]. Tugbawa et al. demonstrated a dual-material damascene CMP model [24]. In an effort to return modeling to a more physically-based approach, Xie et al. developed physically-based pattern-density step-height models, based on a detailed physical model that extracts pad and process dependent parameters [7]. Cai et al. created pattern-density and feature size dependent models of copper CMP, and coupled these with models of the electroplating process [25]. A preliminary wafer-level non-ohmic eCMP model was developed by Truque et al [8]. However, as pad design, layout dimensions and designs, and slurry chemistries change, the model must be refined, expanded, and in the case of eCMP, newly developed.

#### 1.3.1 STI CMP Modeling

Extensive die-level modeling of the damascene process to fabricate STI structures in the Boning group, most recently the work of Xiaolin Xie [7], is contributing to the academic study of CMP, as well as to the industrial optimization of the process in production through fruitful corporate interactions with major semiconductor companies. Most of the previous work focused on pure pattern-density models. These models were based around two central assumptions. The first assumption is a linear dependence of removal rate on pressure, as stated in the Preston equation,  $RR = \kappa P \nu$ , where RR is the removal rate of the material,  $\kappa$  is the Preston coefficient (lumped factor of all other effects), P is the applied pressure, and  $\nu$  is the relative velocity between the wafer and pad. The second assumption is that there exists a strong relationship between pattern-density and removal rates based on a sophisticated weighting system of contributing neighboring die features, which defines a "planarization length." Planarization length is a concept adapted by Stine [20], which assumes that the local pressure is only affected by the topography of a finite nearby region of the die. This neighborhood area is defined by the planarization length, and an averaging filter is used to create what will be referred to as the effective pattern-density, as depicted in Figure 1-5.

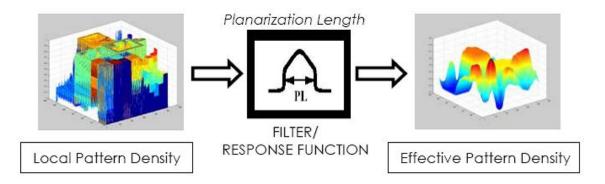


Figure 1-5: Method for calculating effective pattern density.

Xie's work took these models even further by adding in a physically-based set of assumptions, in which the polishing pad is modeled explicitly to estimate pressure in the active and field areas, based on effective topography, step-height, and interactions with the pad. The pad is decoupled into the bulk and the asperities on the surface, yielding two new model parameters, the effective Young's modulus of the pad and a characteristic pad asperity height. Integrating the former pattern-density models, step-height evolution models, and physically based model, Xie was also able to generate an approximate exponential Pattern-Density Step-Height (PDSH) model, which will be used as the foundation for the modeling done in this thesis. It is a semiempirical model, which assumes a continuous dependence on step-height and effective pattern-density, accounting for pressure dependence and step-height reduction effects. This model was hypothesized to be applicable to both dual and single material STI planarization using conventional and non-conventional slurries. However, the model was primarily tuned and demostrated for conventional STI CMP, particularly for oxide stages in the STI CMP process. Our goal is to effectively model practical dual material STI planarization and non-conventional slurry processes, particularly for realistic sized features and topographies used in typical IC products, thus motivating the model extensions proposed in this thesis.

#### 1.3.2 eCMP Modeling

Applied Materials has shown that eCMP is a viable process compared to traditional CMP for the removal of bulk copper, with the introduction of their eCMP tool in July of 2005 [11]. However, a substantial challenge remains to show that eCMP can replace the traditional three platen process for planarizing copper, and new process development is needed to also use eCMP to replace the CMP removal of the barrier metal. In this thesis, we attempt to model this process by adding a third component, electrochemistry, to the traditional planarization picture.

The value of eCMP over the widely accepted traditional CMP process, lies in this third component of electrochemistry. The eCMP material removal mechanism is almost purely electrochemical, as opposed to the wear-driven CMP process. This

allows for the lowering of applied pressure of the polish pad to below 0.3 psi in eCMP, dramatically lower than the traditional CMP standard of 1.5-3 psi. Reduction of the applied pressure has multifaceted benefits: negligible damage to fragile low-K dielectrics, longer pad life, and reduction of pattern dependency [11]. Additionally, the electrolyte used in eCMP, which replaces the need for traditional slurry, is considerably cheaper, potentially enabling a consumable cost reduction of up to 30%, in addition to increasing the throughput by up to 25%. With the combination of the mechanics of CMP and the reactions of electrochemical planarization (EP), the process of eCMP offers the unique possibility to maximize the capabilities to not only reduce dishing and erosion of features, but also reduce cost. ECMP is unique because the electrochemical interactions at the interface of the wafer and the electrolyte creates a passivation, or coating, layer protecting the recessed areas during planarization, which reduces dishing considerably in larger features [11]. This soft passivation layer is thought to be easily removed by the mechanics of the pad, only or predominantly from the raised features. Additionally, some of the process control issues of traditional CMP are avoided, because the direct relationship between charge and removal rate makes the endpoint stable and repeatable 11.

Electrochemistry brings value to the eCMP process, but it also brings challenges to eCMP modeling, because the application of electrochemistry to planarization is poorly understood and it is not yet a complete process. Thus, the modeling of a somewhat ambiguous black box of reactions poses significant challenges and intriguing questions.

#### 1.4 Thesis Contributions

The contributions of this thesis can be split into two specific aims or categories: die-level CMP models for STI CMP and wafer-level eCMP models for Cu CMP.

# 1.4.1 Evolution of Pattern Density Die-Level CMP Model for STI

In this thesis a die-level CMP model for STI is presented, primarily focused on the previously unexplored premise that pattern-density is a function of deposition profile and time (step-height reduction). This model seeks to attack one of the key unknowns in CMP and thus improve the modeling of the process for future technology generations: we improve the physical intuition and understanding of how the deposition profile of the oxide and the morphological changes of the structures being planarized affect the polishing rate of nearby structures. The model proposed in Chapter 2 provides new insight into the deposition profile bias effects and pattern-density effects over time, with the focus of understanding the physical and geometrical changes of the structures being planarized in-situ.

#### 1.4.2 Full Electrochemical Die-Level Modeling for eCMP

In this thesis, a framework for a wafer-level eCMP model for Cu CMP is presented, primarily focused on an accurate representation of the dominant mechanism of electrochemistry. Previous models have been either purely semi-empirical or incomplete representations of the electrochemical reactions taking place in the eCMP process. The model proposed in Chapter 3 takes into account a wider set of the electrochemical reactions taking place in the eCMP process, treating the wafer-electrolyte-pad combination like a prototypical electrochemical cell. This extended model enables accurate representation fo removal rate versus applied voltage, and enables full 3D modeling of eCMP wafer-level uniformity.

#### 1.5 Thesis Organization

This thesis seeks to make theoretical extensions and modeling advancements to eCMP and CMP models, that will allow both processes to take/maintain their place in the overall IC fabrication process. This first chapter served as an introduction to the im-

petus for advanced integrated circuit planarization processes and provided a literature review of these two planarization processes and their respective models. Chapter 2 describes the evolution of die-level CMP models for STI, and the framework for a new evolution of pattern-density die-level CMP model. Chapter 3 describes the history of wafer-level eCMP models for Cu, and the framework for a full electrochemical wafer-level eCMP model. Chapter 4 summarizes the major aims, results, and contributions from Chapters 2 and 3, and suggests key areas for future work.

### Chapter 2

# Evolution of Pattern-Density Die-Level CMP Model for STI

This chapter will propose an evolution of pattern-density die-level CMP model which seeks to account for the deposition profile effects and topography geometry changes which determine pattern-density with respect to time and step-height reduction. A chronological literature review of all previous die-level CMP models for STI from the Boning research group of MIT is presented. The objectives and framework of the new model is then explained in greater detail. Experimental verification for the evolution of pattern-density CMP model is described, followed by a summary.

#### 2.1 Evolution of Die-Level CMP Models

Since 1997 extensive and prototypical die-level models have been explored for both STI and copper CMP. Trending over the past 12 years has generally shown steady improvement in the accuracy, or reduction in the error, of empirical modeling of pattern-varying removal in test layouts and/or structures, as shown in Figure 2-1.

Closely observing the trend in Figure 2-1, the aforementioned steady error reduction is seen until 2002, when there appears to be a transition upwards in RMS error. All of the models prior to 2002, by Stine, Ouma, Smith, and Lee were employing the use of empirical parameters to verify the physical intuition explaining the

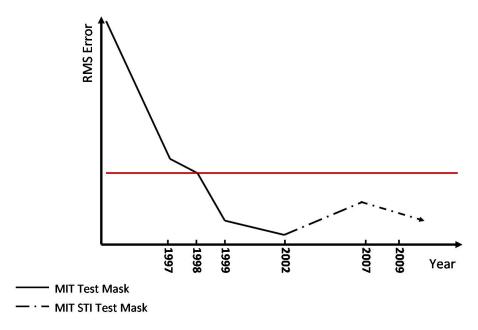


Figure 2-1: Illustration of model evolution of STI for CMP: reported root mean squared (RMS) model error of film thickness predictions from previous work is shown.

pattern-dependent oxide thickness variation, and subsequent removal through modeling. Take for instance the use of the parameter of planarization length; this empirical parameter seeks to provide a "characteristic length over which neighboring topology is affective based on long range pad deformation and pressure distribution." These models have been primarily empirical or semi-empirical in nature, successively adding effects to improve accuracy, at the price of increasingly complex modeling with more semi-empirical model parameters. In 2002, Xie began work to use physical parameters to verify the physical intuition to explain and explicitly model the pad and surface asperities. Xie's work on a physically-based CMP model uses physical properties like applied pressure, pad Young's modulus, and pad asperity height to find the discretized point pressure. Most notably, Xie's implementation of this physically-based model into a PDSH model was able to capitalize on the physical intuition yielded by the physically-based model while also reducing the number of fit parameters without significantly degrading model error.

Although CMP has steadily increased in usage and process precision in state of the art IC manufacturing, the fundamental physical understanding of how the process actually works has not advanced greatly in the past five years or so. Xie's exponential pattern-density step-height model was able to show promise in modeling explicit physical components, using the extracted physical properties as parameters and providing a more physically sound basis upon which to better empirically model topography morphology during removal. However, there were several components absent from his modeling approach, including the attention to the time-evolving morphology of the structures being planarized, and the respective step-height dependent pattern densities as a result of that evolution. Our goal in this portion of the thesis is to review previous CMP models, and then consider this key improvement to the model.

#### 2.1.1 Pattern-Density CMP Model

One of the earliest models to present a closed form solution for effectively predicting removal and ILD thickness variation using a semi-empirical CMP model was proposed by Stine et al. [20]. This model established a baseline for analytical modeling of CMP, on the premise that the key parameter in predicting removal of topography was the pattern-density of the layout, thus focusing the model on explaining the principal vice of planarization using CMP, the variation caused by systematic pattern sensitivies [3].

The key parameter of effective pattern-density, referred to as  $\rho$ , is defined and established in Stine's work as a function of deposition profile, polish time, and the lateral spatial range over which it is computed. This premise is sound; however, Stine makes several limiting assumptions. The first assumption is that the oxide deposition profile is a direct vertical translation of an underlying metal profile as shown in Figure 2-2 below, and thus the raised oxide and the metal layer share the same pattern-density.

This assumption works effectively for relatively large features, e.g., for pitches greater than  $250\mu$ m and line widths greater than  $20\mu$ m, in which there are no significant lateral deposition effects. However, when considering smaller feature sizes using diverse deposition techniques like the more conformal chemical vapor deposition (CVD) versus a high density plasma CVD, one must consider these deposition effects which yield a profile similar to the general case shown in Figure 2-3 below,

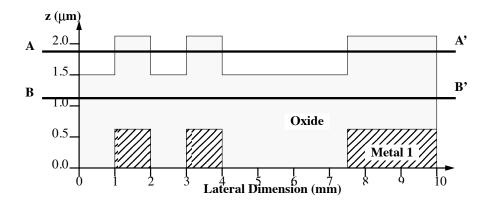


Figure 2-2: Deposition profile: simple example to aid in defining pattern-density [3]. used also to illustrate the definitions used to develop Stine's model.

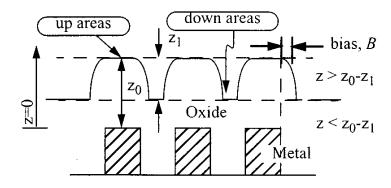
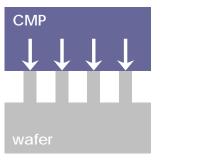


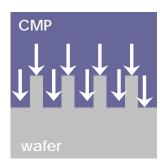
Figure 2-3: General CVD deposition profile, defining variables used in Stine's model [4].

The second assumption made by Stine is that the pattern-density as a function of time is a negligible secondary effect in features of this size, such that the pattern-density is held constant prior to step-height removal as shown at time A and only changed to  $\rho=1$ , after the step-height is removed as shown in time B as illustrated in Figures 2-2 and 2-3 above. In agreement with the former use of the metal vertical deposition profile translation, as long as a step-height exists,  $\rho$  remains the same until removed and it then becomes 1, or the equivalent of a blanket wafer with 100% pattern-density.

The third assumption holds that the range over which the effective pattern-density is computed is a square surface area,  $A_r$ , that has a width known as the *interaction distance* over which the pad conforms to contact the wafer's surface, facilitating

planarization. The physical intuition behind this assumption is based upon an incompressible pad model, illustrated in Figure 2-4 below, which implies that the pad is only in contact with the up areas and not the down areas, until there is no step present (essentially planarization is complete) at a specific transition time,  $t_t$ . In other words, a simple square-shaped filter is employed as a "weighting function" to calculate effective pattern-density, where the interaction distance (id) is equivalent to the planarization length, which is loosely described as the width of the transition ramp between low and high density region thickness variation as pictured in Figure 2-5.





**Incompressible Pad Model** 

Compressible Pad Model

Figure 2-4: Illustration of incompressible vs. compressible pad model [5].

As a result of the three aforementioned assumptions, the calculations for this model are very simple to follow, as shown in Equations 2.1 through 2.5. The derivation begins with the widely accepted Prestonian relation in Equation 2.1, which states that the blanket removal rate is proportional to the product of pressure, velocity, and some proportionality constant,  $\kappa$ . If the pressure term is replaced with force per area (F/A), A can represent the oxide area contacted by the pad in order to rewrite Equation 2.1 as Equation 2.2.

$$RR_{up} = \kappa P \nu \tag{2.1}$$

$$RR_{up} = \kappa P \nu$$

$$RR_{up} = \frac{\kappa F \nu}{(id)^2 \rho(x, y, z)}$$
(2.1)

As previously mentioned,  $\rho(x,y,z)$  is the effective pattern-density as a function of x, y, its position on the chip, and z, the thickness of the oxide layer. A is represented as  $(id)^2 \rho(x, y, z)$ , or the oxide area in contact with the pad according to our square weighting function assumption. Then, we can define the blanket removal rate,  $K = \kappa P \nu$  and replace its constant as shown in Equation 2.3, to arrive at the rate of up area removal,  $\frac{dz}{dt}$ .

$$\frac{dz}{dt} = \frac{K}{\rho(x, y, z)} \tag{2.3}$$

The third assumption is incorporated in the definition of Equation 2.4, where the dependence on step height is only a matter of the presence of the active step, or up area. The pattern-density is either the effective pattern-density,  $\rho$ , or 1, a blanket wafer with 100% pattern-density.

$$\rho(x, y, z) = \begin{cases} \rho_0(x, y) & z \ge z_0 - z_1 \\ 1 & z < z_0 - z_1 \end{cases}$$
 (2.4)

A fourth assumption is that the removal in the down areas is negligible compared to removal in the up areas while any step-height remains and is thus not considered during the removal of the step (up area removal); down areas are then assumed to be polished at the blanket rate, after the removal of the step (down area removal). The differential of Equation 2.3 is thus solved for  $z_{up}$  before and after the transition time, or the time at which the step is removed, in Equation 2.5.

$$z_{up} = \begin{cases} z_0 - \left[\frac{Kt}{\rho_0(x,y)}\right] & Kt \le \rho_0(x,y)z_1 \\ z_0 - z_1 - Kt - \rho_0(x,y)z_1 & Kt > \rho_0(x,y)z_1 \end{cases}$$
(2.5)

This model yields good results in localized structures that are relatively large in size, as previously described, with a simple approach that requires very few parameters. However, the model lacks the complexity and flexibility needed to model smaller, more realistic structures/layouts with non-conventional deposition profiles and process conditions.

# 2.1.2 Pattern-Density CMP Model with Elliptic Density Function Weighting

Following Stine's work, the model was extended to address some of the limiting assumptions. In particular, planarization length was generalized, refining the concept of effective pattern-density [21]. Ouma's work challenges the third assumption made by Stine, considering the physical motivation for averaging the local pattern-density to arrive at the effective pattern density proposed by Stine. Rather than use a square averaging window, Ouma considered long range pad deformation arising from the pad's properties and process conditions, and approximated the response of the pad to an impulse of raised pattern-density, with the use of an elliptic weighting function. Thus the effective pattern-density and therefore the local pressure exerted at any location (x,y) is influenced by neighboring topography in a decreasing function as one gets further from (x,y).

The square averaging filter used by Stine is equivalent to a simple notion of planarization length shown in Figure 2-5. The interaction distance in Stine's model corresponds to the distance over which the pad can bend or conform to wafer surface height differences. At distances greater than id (or planarization length PL), the pad essentially deflects and polishes both regions at the blanket rate. On the contrary, at distances much smaller than id or PL, however, the pad cannot bend and thus only contacts raised features.

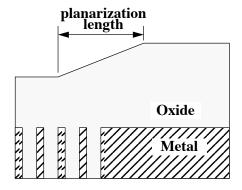


Figure 2-5: Simple example to aid in defining planarization length [3].

In order to effectively model this long range pad deformation, Ouma considered

the mechanics of pad bending to re-evaluate the distance over which raised topography influences local removal rates. A density weighting function is employed to find the effective pattern-density, and is defined as the "spatial density impulse response of the pad for a given process condition" [4]. The pad deformation is based on the fact that the pad is made of polyurethane, a non-linear elastic material, which can be modeled by a symmetric elliptic weighting function commonly used for elastic materials. This also gives a formal definition to planarization length; instead of just being the width of the square averaging area, it now takes into account the neighboring topography in order to properly account for the weight of their contribution to the calculation of the effective pattern-density and removal rate for a particular discretized point on the die layout. Figure 2-6 shows that the local layout density (b) is convolved with the elliptic weighting function, resulting in a smoother effective density profile (c).

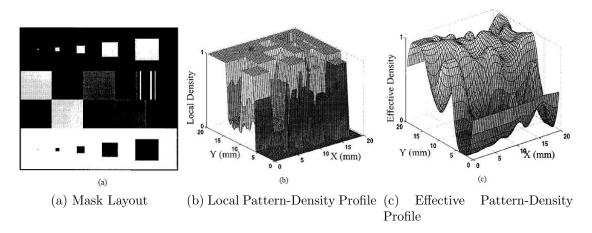


Figure 2-6: Local pattern-density across die evaluated in 40mm by 40 mm cells using the elliptic planarization response function to produce an effective density map [4].

Ouma's model also addressed the first assumption of Stine's model which ignored deposition profile effects, by accounting for the initial deposited film topography with a bias adjustment to account for lateral deposition effects. This is of particular importance to relatively small features which, during high density plasma (HDP) deposition, can sometimes result in small triangular peak profiles, as opposed to the square profiles shown in Figure 2-2, giving areas with these features a local pattern-

density of nearly 0%. These layout features and all other features are adjusted by a bias value or shrinkage value, B, when extracting the local density.

Aside from these two extensions to the model, the primary calculation of  $z_{up}$  remains from the previous section. Now, however, the effective pattern-density can be calculated for each discretized point on the die as in Equations 2.6 to 2.8 below, where d(x, y) is the local pattern-density extracted with the bias, f(x, y) is the elliptic weighting function, and  $\rho_{eff}(x, y)$  is the new effective pattern-density. Here, the convolution or weighted averaging filter operation can be performed using the discrete Fast Fourier Transform to speed up the calculation.

$$\rho(x,y) = d(x,y) \otimes f(x,y) \tag{2.6}$$

$$\rho(n_1, n_2) = \sum_{k_1 = -\infty}^{\infty} \sum_{k_2 = -\infty}^{\infty} d(n_1, n_2) f(n_1 - k_1, n_2 - k_2)$$
(2.7)

$$\rho_{eff}(n_1, n_2) = IFFT[FFT[d(n_1, n_2)] \cdot FFT[f(n_1, n_2)]]$$
(2.8)

Thus, replacing Stine's pattern-density with the new effective pattern-density,  $\rho_{eff}(x,y)$ , the equations for  $z_{up}$  are virtually the same, as given by Equation 2.9.

$$z_{up} = \begin{cases} z_0 - \left[\frac{Kt}{\rho_{eff}(x,y,z)}\right] & Kt \le \rho_{eff}(x,y)z_1 \\ z_0 - z_1 - Kt - \rho_{eff}(x,y)z_1 & Kt > \rho_{eff}(x,y)z_1 \end{cases}$$
 (2.9)

Addressing the long range pad deformation through the weighted effective patterndensity calculation, and addressing the initial deposition profile effect through the biasing of the local pattern-density extraction, significantly improved the model's accuracy. However, this model still retains several of the assumptions of the previous model, including those related to down area removal, pattern-density as a function of time or step height, and use of the incompressible pad model.

#### 2.1.3 Pattern-Density Step-Height CMP Model

Ouma's work was a significant step towards understanding long range pad deformation; however, it still focused on an incompressible pad model and thus was unable to effectively model field (down area) removal between small features. In the interim between Ouma and Smith [22], a refined pad model was proposed by J. Grillaert et al. at IMEC [5]. This model asserts that the pad is in fact compressible, such that both the up and down areas are in contact with the pad for step heights less than some specific contact step-height,  $h_1$ . The IMEC model suggests that the removal rates converge exponentially in time to the blanket removal rate, consistent with Tseng et al. [26]. Smith's work integrates the IMEC model to explain pad contact in the up and down areas, with Stine's pattern-density model to explain localized density effects on thickness and removal variation.

The key parameters in this model now include contact step-height,  $h_1$ , in addition to planarization length and pattern-density. The contact step-height now splits removal into two regimes: prior to the contact step-height, removal follows Stine's model; below the contact step-height, removal is exponential according to Tseng's model, as shown in Figure 2-6.

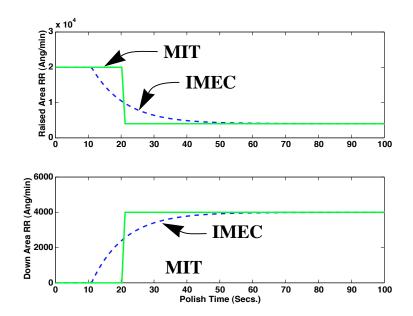


Figure 2-7: Comparison of Stine's (MIT) model and the IMEC model's removal rates [6].

Thus, the calculation now has many terms which must be fitted, as opposed to just two parameters of the two previous models (planarization length and blanket rate). In the derivation below, the additional model parameters include the transition (contact) step-height,  $h_1$ , defined as

$$h_1 = h_0 - \frac{K}{\rho} t_c \tag{2.10}$$

where  $h_0$  is the initial step-height. Additionally, there is an exponential time constant,  $\tau$ , and the actual transition or contact time,  $t_c$ .

Essentially, the derivation is according to the theory as previously mentioned, with the removal rates given with respect to contact time (i.e., contact step-height achieved) as opposed to a transition time when the step-height is *removed* as in Stine's model.

$$RR_{up} = \begin{cases} \frac{K}{\rho} & t_p \le t_c \\ K + (1 - \rho) \frac{h_1}{\tau} e^{\frac{-(t_p - t_c)}{\tau}} & t_p > t_c \end{cases}$$
 (2.11)

$$RR_{down} = \begin{cases} 0 & t_p \le t_c \\ K - \rho \frac{h_1}{\tau} e^{\frac{-(t_p - t_c)}{\tau}} & t_p > t_c \end{cases}$$
 (2.12)

As traditionally derived, we can calculate amount of material removed from the differential equations of removal rate for both the up and down areas, giving Equations 2.13 and 2.14.

$$z_{up} = \begin{cases} \frac{K}{\rho} t_p & t_p \le t_c \\ \frac{K}{\rho} t_c + K(t_p - t_c) + (1 - \rho) h_1 (1 - e^{\frac{-(t_p - t_c)}{\tau}}) & t_p > t_c \end{cases}$$
 (2.13)

$$z_{down} = \begin{cases} 0 & t_p \le t_c \\ K(t_p - t_c) - \rho h_1 (1 - e^{\frac{-(t_p - t_c)}{\tau}}) & t_p > t_c \end{cases}$$
 (2.14)

As a result of the combinative power of both Stine's pattern-density model and the IMEC model, Smith was able to show a 50% reduction in RMS error in this pattern-density step-height model, showing excellent accuracy in the modeling of both up and down area removal in large features. A detrimental artifact of combining these two

models, is the 50% increase in the number of model parameters which are fitted and thus an increase in computational complexity and decrease in statistical reliability. Furthermore, although greater accuracy is achieved using this model versus using Stine's model, there is still poor down area fitting between features, and remaining assumptions that are not addressed.

#### 2.1.4 PDSH CMP Model with

#### Elliptic Density Function Weighting

Following Stine's work, there was still a void between advancements in the effective pattern-density model [21] which accurately addressed long range pad deformation and advancements in the pattern-density step-height (PDSH) model [22] which efficiently addressed pad contact behavior in the up and down areas. Lee's [27] work integrates the two models forcing the contact step-height,  $h_1$ , of Smith's PDSH model to depend on the effective pattern-density,  $\rho_{eff}$ .

Accordingly, there are the same key parameters as in the PDSH model; however, in this integrated model the contact step-height is dependent on the effective pattern-density derived using the elliptic weighting function,

$$h_1 = a_1 + a_2 \cdot e^{\rho_{eff}/a_3} \tag{2.15}$$

where  $a_1$ ,  $a_2$ , and  $a_3$  are fitting constants. However, the removal rate and z equations for both the up and down areas remain the same, Equations 2.13 and 2.14.

This integrated model yielded substantial improvements, reducing the RMS error of both the up and down area removal. It should be noted that there was still some significant model error of the down areas in lower pattern-density regions. Although approximately 100Å accuracy is reached, there remains a large number of parameters to fit. Several approximations and assumptions remain, including the fact that accuracy is only achieved for relatively large features, which are much larger than product (memory or logic chip) feature sizes, the lack of physically-based parameters, and the use of constant pattern-density as opposed to a time or deposition profile dependent

pattern density.

#### 2.1.5 Physically-Based Exponential PDSH CMP Model

As mentioned in the introduction to Section 2.1, the work of Xie [7] diverts from another extension of the previous semi-empirical models with multiple fitting parameters, to the creation of a physically-based model which seeks to extract parameters that will contribute to the physical understanding of the planarization mechanism of the pad. Xie's physically-based model specifically considers the pad bulk and asperities as separate entities, as shown in Figure 2-8, with the goal of modeling pressure dependence as a function of step-height and local pattern-density. Furthermore, the parameters extracted from the physically-based model are used to improve Lee's PDSH model, by introducing an exponential dependence of removal rate on step-height. Both models are verified using a new test mask designed with realistically sized test structures, as well as actual memory and logic product structures.

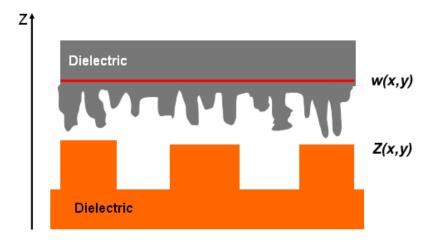


Figure 2-8: Illustration of the decomposition of the polishing pad's bulk and asperities [7].

The key parameters of the physically-based model are effective Young's Modulus E, the applied pressure of the tool  $P_0$ , and characteristic asperity height,  $\lambda$ . As previously mentioned, the pad bulk and pad asperities are decoupled in this model.

Consequently, the bulk can be modeled as an elastic body of material, and a contactwear model used to calculate pad deflections explicitly, as in Equation 2.16.

$$w(x,y) - w_0 = F(x,y) \otimes P(x,y) \tag{2.16}$$

Here w(x,y) is the bulk surface displacement, P(x,y) is the applied pressure, and F(x,y) is the deformation impulse response to a point pressure. The deformation response F(x,y) is inversely proportional to the effective Young's modulus of the pad, allowing one to extract this physical attribute from the model output.

On the other hand, asperities are modeled as separate bodies with negligible width and an exponential height distribution,  $e^{h/\lambda}$ . Since the force exerted is assumed to be proportional to the compressed distance, Hooke's law gives the local pressure as a function of feature step-height as shown in Equation 2.17.

$$P(x,y) = k \cdot \left(\rho(x,y) + (1 - \rho(x,y))e^{\frac{-h(x,y)}{\lambda}}\right) \cdot \lambda e^{\frac{-(w(x,y) - z_{up}(x,y))}{\lambda}} \tag{2.17}$$

where k is a spring constant. The parameters of the physically-based model are exploited in the PDSH model by using  $\lambda$  to determine the nature of the pressure dependence on step-height, as shown in Equation 2.18 below.

$$P(x,y) = \begin{cases} P_{up}(x,y) = \frac{e^{\frac{h(x,y)}{\lambda}}}{1 + \rho(e^{\frac{h(x,y)}{\lambda}} - 1)} P \\ P_{down}(x,y) = \frac{1}{1 + \rho(e^{\frac{h(x,y)}{\lambda}} - 1)} P \end{cases}$$
(2.18)

For comparison, the parameters of the physically-based model can also be replaced in the PDSH model by assuming that that the pressure dependence on step height is exponentially dependent on whether the asperity is in contact with the wafer surface, and compressed using the characteristic step-height variable as shown in Equation 2.19 below.

$$P(x,y) = \begin{cases} P_{up}(x,y) = \frac{1}{\rho} P_0 - \frac{1-\rho}{\rho} P_0 \cdot e^{-\rho h/h^*} \\ P_{down}(x,y) = P_o \cdot e^{-h/h^*} \end{cases}$$
(2.19)

As seen in Figure 2-9 below, both models (the physically-based PDSH model and exponential step-height model) extract two parameters; the former uses planarization length and  $\lambda$ , the latter uses planarization length and characteristic asperity height  $h^*$ .

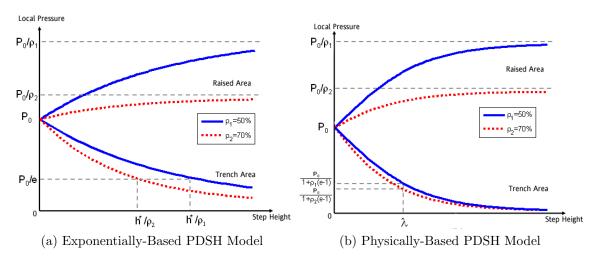


Figure 2-9: Relationship between local pressure and step-height [7].

From the figure we can observe that the two applications of the PDSH model are qualitatively similar, with a smooth transition in pressure dependence based on a characteristic step-height or physical asperity height distribution using  $\lambda$ , as compared to the previous models which had a much sharper transition. Nevertheless, these two models are quantitatively different in that the physically-based PDSH model yields higher experimental data fit errors than the exponentially-based PDSH model.

Recall that the exponentially-based PDSH model has removal rate equations as shown in Equation 2.20.

$$K(x,y) = \begin{cases} K_{up}(x,y) = \frac{1}{\rho} K_0 - \frac{1-\rho}{\rho} K_0 \cdot e^{-\rho h/h^*} \\ K_{down}(x,y) = K_0 \cdot e^{-\rho h/h^*} \end{cases}$$
(2.20)

With these removal rate equations, one can integrate to derive thickness z and the

step-height, h update equation,

$$z_{up} = \frac{1}{\rho} K_0 \cdot t - \frac{1 - \rho}{\rho} z_{down}$$
 (2.21)

$$z_{down} = h^* ln[1 + e^{-\rho/h^*} (e^{K_0 t/h^*-1})]$$
(2.22)

$$h = h_0 + z_{down} - z_{up} \tag{2.23}$$

These can also be extended to dual material polishing using the selectivity as a further model parameter.

The exponential PDSH model does achieve the same order of accuracy as seen for the previous models, applied to large structures. However, the exponential PDSH model can now be applied and verified using structures, pitches and line widths that are half the size or smaller than that of the previous model, and the model is still achieving an accuracy at or above manufacturing design standards. Additionally, this model's enhancements are based on physical intuition and fewer fitting parameters, simultaneously improving the ease of computation while creating more realistic assumptions and statistical reliability verified with more realistic structures. However, one remaining assumption is that pattern-density does not change as a function of time. Our motivation is to build on these previous models, but also consider the effect of topography evolution on pattern density in time. The only piece missing analytically is the limited assumption of pattern-density as a function of time.

## 2.2 Objectives and Framework of Evolution of Pattern-Density Die-Level CMP Model for STI

Originally, the premise of the work proposed in this thesis was to explore the previous exponential PDSH model, and work in collaboration with National Semiconductor to verify its flexibility by extending the model to a single wafer per platen polishing tool (as opposed to the batch tool originally used) and a non-conventional Ceria

slurry. However, we were met with two challenges which opened up the opportunity to transform and further evolve the modeling with respect to understanding the physical basis for the polishing of deposited topography.

The first challenge arose from our observation of accuracy limitations using the existing exponential PDSH model on the oxide-only stage of STI polishing. New experiments using the STI CMP test mask were performed and the existing model fit to measurements, as shown in Figures 2-10 and 2-11. Shown here are the first 20 measurement points in Figure 2-10 and the second 20 measurement points in Figure 2-11 (as described in Appendix A, Figure A-4) during the oxide stage of STI planarization. While several regions in the die fit quite well, we also note regions at the left of the die where the model substantially underestimates the amount of polish. Improvement of the model to overcome this model limitation thus is a key goal.

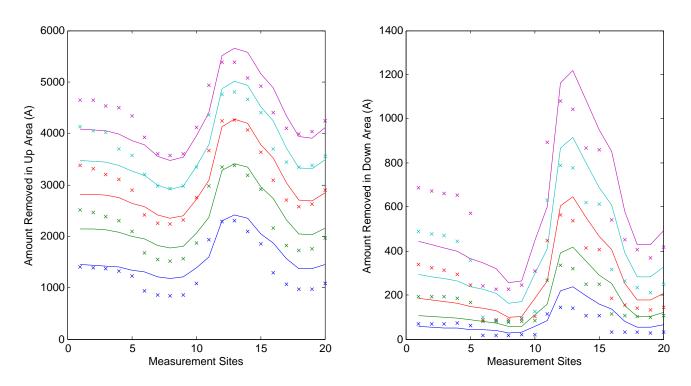


Figure 2-10: Model fit (lines) of exponential PDSH model to new experimental data ("x" points) during oxide stage of STI CMP.

The second challenge was to reassess a continuing assumptions in previous models about pattern-density as a function of time and deposition profile. In all of the

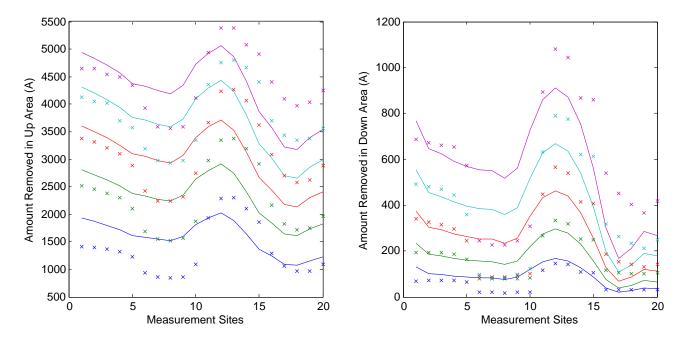


Figure 2-11: Model fit (lines) of evolution of pattern density exponential PDSH model to new experimental data ("x" points) during oxide stage of STI CMP.

previously mentioned models, local pattern-density is assumed to remain constant throughout the planarization process. However, our intuition, motivated by Figure 2-12, is that the pattern-density changes with respect to step-height reduction when the deposition profile is non-vertical. In some versions of the PDSH CMP model, the deposition profile is biased once by some bias factor B to account for an "average" deposition profile geometry, and that "biased" local pattern-density is used throughout the polish. None of our previous models, however, addresses the change in geometry over time, i.e., with respect to step-height reduction.

# 2.2.1 Objective of Evolution of Pattern-Density Model for STI

The objective of the evolution of pattern-density model is to address the two aforementioned challenges by considering pattern-density as a function of both time and deposition profile, as shown in Figure 2-12 below.

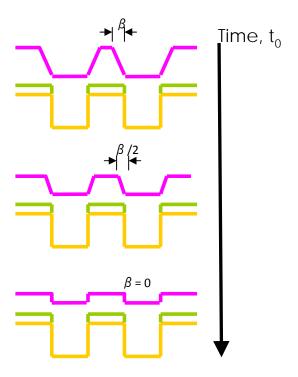


Figure 2-12: Evolution of deposition profile geometry and pattern-density over time.

#### 2.2.2 Role of Evolving Pattern-Density

We can build our physical intuition of the deposition and how it evolves during polishing through AFM measurements of test wafer profiles. The AFM images shown in Figure 2-13 were taken at the initial planarization time step (24 seconds), in the EA region of the test mask as described in Appendix A, Figure A-4. The EA01 structures are designed to be  $1\mu m$  wide by  $1\mu m$  long, with a spacing of  $2\mu m$  between structures; the EA04 region has structures  $0.5\mu m$  wide by  $0.25\mu m$  long, with  $2\mu m$  spacing. In these AFM images, after 24 seconds of polishing, a pyramidal profile is seen, consistent with the schematic diagram of Figure 2-12.

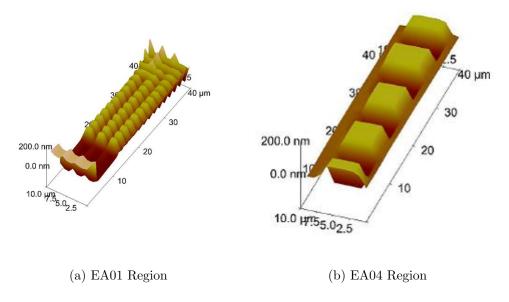


Figure 2-13: AFM images of test structures on MIT STI test wafers from NSC experiments.

Based on the presence of non-vertical deposition profiles, we challenge the assumption that the local pattern-density remains constant over the course of the polish time, and instead assert that the deposition profile evolution plays a key role in determining pattern-density. Our hypothesis is that pattern-density will change over time, with the bias-induced geometry of the deposition profile affecting the removal rate and resulting amount removed as a function of pattern-density, feature size, step-height, and polish time.

In order to determine if our new hypothesis that local pattern-density changes with step-height and polish time, and to understand the possible magnitude of the effect, we performed some theoretically-based mathematical simulations of specific structure on three areas of the chip assuming a geometric deposition profile as pictured in Figure 2-12. These simulations show that, as the step-height is reduced, the local oxide pattern-density increases. In Figure 2-14, we observe a nearly constant dependence of pattern-density on step-height in features that are in the 70-100  $\mu m$  size range (LRPD region). There is a slight linear increase in pattern density, from 0.487 at h=5500 Å, to  $\rho_s=0.5$  at h=0 Å. On the same figure, we observe a relatively small change in pattern-density with primarily linear dependence, slightly

quadratic, of pattern-density on step-height in features that are in the 30-60  $\mu m$  range (ED region). However, for the smallest structures investigated, in the 1-10  $\mu m$  range, we find a very large effect of step-height on pattern-density of almost 30%, and in this case we also clearly observe a quadratic dependence of pattern-density on step-height (EA region). Considering these different regions, we clearly see that small structures are substantially affected by deposition profile, while large structures are perturbed only slightly.

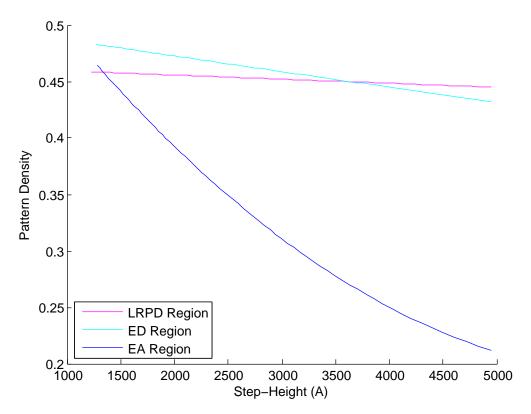


Figure 2-14: Comparison of pattern-density vs. step-height (LRPD, ED, and EA regions).

This dependence can also be seen in the relationship between time and local pattern-density which increase together as shown in Figure 2-15. Note that all three of these regions (LRPD, EA, and ED) have layout pattern densities of approximately 50%; depending on the size of the feature and the step-height vs. polish time, however, the pattern density of topography contacting the pad can vary dramatically.

In order to understand how the deposition profile or biasing effect might impact an example layout, we consider the local pattern-density for our test mask with dif-

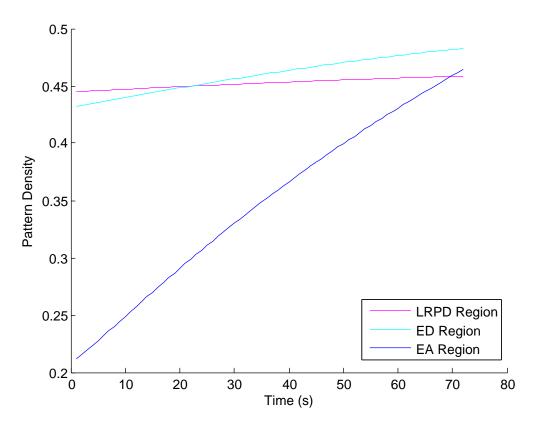


Figure 2-15: Comparison of pattern-density vs. time (LRPD, ED, and EA regions).

ferent amounts of biasing. Consistent with Figure 2-12, we consider three variants of pattern-density extractions from our test chip, as shown in Figure 2-16. First, the density map labeled  $\rho_{\beta}$  is generated by shrinking all layout geometries by a lateral dimension of  $\beta$ , then performing the pattern-density extraction in each  $40\mu m$  by  $40\mu m$  cell. The map labeled  $\rho_{\beta/2}$  corresponds to a  $\beta/2$  shrinkage of all geometries, while  $\rho_0$  is the "unbiased" or direct pattern density map of the original layout. We see that the deposition profile plays an integral role in pattern-density and its changes over time.

We believe that each of these biases represent a snapshot of the increased patterndensity in time: the  $\beta$  bias case represents the initial deposition profile, as previously proposed, the  $\beta/2$  case represents the local pattern-density in each cell when half the step-height has been removed, and the case with no bias represents the near completely planarized case. Interestingly enough in Figure 2-15, in each of the snapshots we see that the region with the smallest features, the EA region ( $< 10\mu$ m feature

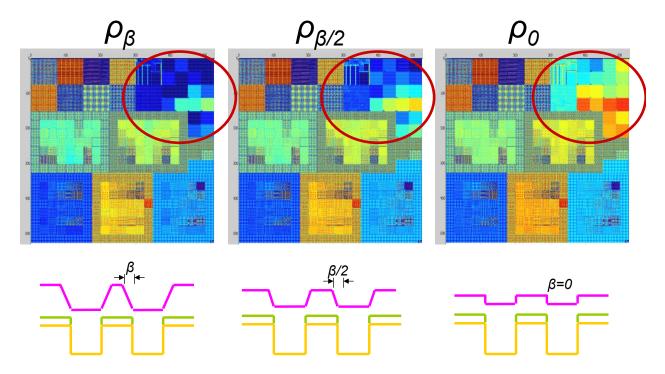


Figure 2-16: Local layout pattern-density based on deposition profile bias.

size), is most significantly affected by this pattern-density evolution. The premise of our model is established around the key parameter of time evolving, step-height dependent local pattern-density, as the deposition profile geometry evolves during the polish. The presence, in Figure 2-16, of regions that change in local pattern-density so dramatically during the process, offers hope for improved model accuracy in nearby regions. Once spatial averaging of the local pattern-density is performed, regions on the chip within a planarization length of these regions will experience a change in effective pattern-density over time as well. Our model will seek to include this neighborhood impact to improve accuracy in polish predictions for structures in or near small feature regions on the chip.

#### 2.2.3 Modeling Framework

The framework for a model to incorporate this idea of time-evolving pattern-density is primarily based on the ability to derive specific geometric profile parameters for each discretized point, based on the local pattern-density extractions in the three previously mentioned cases: without bias, with  $\beta/2$  bias, and with  $\beta$  bias. We can use those values to approximate the pattern-density at the initial, middle, and final step-heights, and then use an equation to predict the pattern-density at all the other step-heights.

In order to derive the equation relating pattern-density to step-height, we consider the extraction window, illustrated in Figure 2-17. We assume there are multiple structures inside of that window whose active areas have a length of  $a_i$  or  $a_j$  and a width of  $b_i$  or  $b_j$ . Geometries labeled with subscript i are assumed to be rectangles fully enclosed within area  $\alpha$ , while geometries subscripted j are "clipped" rectangles only partially within area  $\alpha$ . The layout dimension  $a_i'$  depends on the step-height, h. When h=0,  $a_i'$  is the original layout dimension  $a_i$ , and decreases to  $a_i'=a_i-2\frac{h}{h_0}\beta$  as h increases from 0 to  $h_0$ . A similar shrinkage occurs for dimension  $b_i$ . In the case of the clipped rectangles, only one side of  $a_j$  or  $b_j$  shrinks within the extraction window, so  $a_j'=a_j-\frac{h}{h_0}\beta$ 

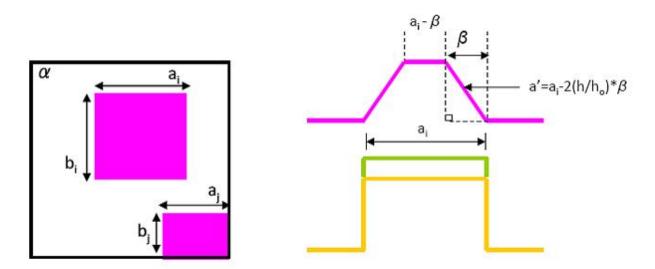


Figure 2-17: Pattern-density extraction based on profile geometry.

A simple geometrical calculation of surface area thus results for each geometry of these two types:

Active Surface Area 
$$\begin{cases} S_i(h) = a'_i \cdot b'_i = (a_i - \frac{2h}{h_o}\beta)(b_i - \frac{2h}{h_o}\beta) \\ S_j(h) = a'_j \cdot b'_j = (a_j - \frac{h}{h_o}\beta)(b_j - \frac{h}{h_o}\beta) \end{cases}$$
(2.24)

Next, we calculate the pattern-density based on the area of the extraction window,

$$\rho_s(h) = \frac{1}{\alpha} (\Sigma_i S_i + \Sigma_j S_j) \tag{2.25}$$

$$\rho_s(h) = \frac{\frac{1}{\alpha} (\Sigma_i a_i b_i - 2 \frac{h\beta}{h_o} \Sigma_i (a_i + b_i) + \frac{4h^2}{h_o^2} \beta^2 + \sum_j a_j b_j - \frac{h\beta}{h_o} \Sigma_j (a_j + b_j) + \frac{h^2}{h_o^2} \beta^2)}$$
(2.26)

Grouping terms in power of h, we clearly see that pattern-density has a quadratic dependence on step-height. Thus we can lump the parameters around the step-height variable, h, into three parameters A, B, and C, simplifying Equation 2.26 above into Equation 2.27.

$$\rho_s(h) = \frac{1}{\alpha} (A + B \cdot h + C \cdot h^2) \tag{2.27}$$

Using the three biased layout extractions described in the previous section, we can relate A, B, and C to the extracted pattern densities  $\rho_0$ ,  $\rho_{\beta}$  and  $\rho_{\beta/2}$ .

$$\rho_{\beta} = \rho_{s}(h = h_{o}) = \frac{1}{\alpha}(A + Bh_{o} + Ch_{o}^{2}) 
\rho_{\beta/2} = \rho_{s}(h = \frac{h_{o}}{2}) = \frac{1}{\alpha}(A + B\frac{h_{o}}{2} + C\frac{h_{o}^{2}}{4}) 
\rho_{o} = \rho_{s}(h = 0) = \frac{A}{\alpha}$$
(2.28)

We can now solve for A, B, and C as shown in Equation 2.29.

$$A = \alpha \rho_o$$

$$B = \frac{\alpha}{h_o} (4\rho_{\beta/2} - \rho_\beta - 3\rho_0)$$

$$C = \frac{2\alpha}{h_0^2} (\rho_\beta + \rho_0 - 2\rho_{\beta/2})$$
(2.29)

.

The quadratic form of our equations here confirm the response in pattern density seen in simulation and in the assumed pattern-density evolution over time and/or step-height reduction in the EA Region.

# 2.3 Verification of Evolution of Pattern-Density Die-Level CMP Model for STI

This section will present the experimental setup for the verification of the proposed model in detail and then present the model fitting versus the experimental data.

#### 2.3.1 Experimental Setup

The exponential PDSH model and evolution of pattern-density PDSH models are verified and calibrated using data measurements from experiments done on the Mirra CMP tool at National Semiconductor's South Portland Maine Fabrication Facility. In order to verify the previous model work and compare tool effects on model accuracy (SpeedFam CMP tool previously used by Xie [7]), the STI test mask described in Appendix A, Figure A-1 was used to pattern the test wafers which were planarized on the Mirra CMP tool. Experimental runs use the conventional silica slurry and the respective time splits are shown in Appendix B, Table B-1. The table shows the single process variable of applied downforce. For this thesis, we only show results for the pressure of 3psi.

The initial STI structure is fabricated as follows (Figure 2-18). The 200 mm silicon p-type test wafers began with a thermally grown 90 Åpad oxide. This was followed by a CVD of 1190 Åof silicon nitride. The wafers are patterned with the STI test mask and etched for a trench depth of 5500 Å. The trench is then filled with oxide for an overburden of 550 Å.

#### 2.3.2 Verifying Model with Experimental Data

We model the CMP process on the new Mirra tool, using the measurements from these experiments and the exponential PDSH model extended to incorporate the new evolving pattern-density. Figure 2-18 shows a relatively good fit, finding the empirical parameters to be 3.69 mm for the planarization length and  $904.3\text{\AA}$  for the characteristic step-height, with an RMS error of approximately  $435\text{\AA}$ . In comparison

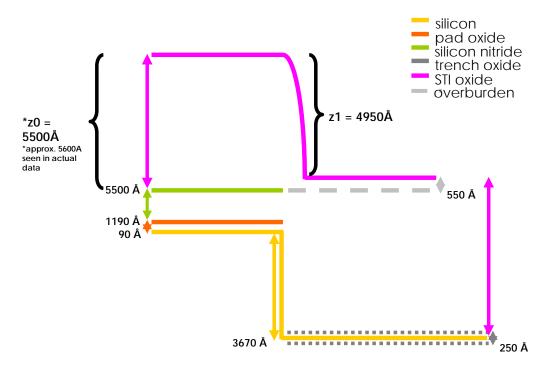


Figure 2-18: Initial STI deposition thicknesses.

to runs that were nearly identical on the previous tool (in Xie's work), the error is slightly lower here, but the empirical parameters are comparable, suggesting that the model form is tool independent, relatively good fit of the model to experimental data is seen in Figures 2-10 and 2-11, except in regions near to small feature regions on the chip. In order to obtain new results with the pattern-density evolution model, refinements to the previous model and the model fit strategy were adopted to enable new ways of effectively modeling STI processes for CMP.

The first refinement made was adopting a coding strategy which used the model simulation of the purely oxide time step data of the polish, to fit the empirical oxide model parameters without the dual material data (i.e., after the nitride clears). Once these parameters were fitted with the purely oxide data, they were input into the dual material component simulation for analysis and fitting of the remaining selectivity parameter, as shown in Appendix C, Figure C-1. This reorganization of the calibration strategy within the model itself enabled us to properly calibrate the dual versus the single material removal parameters.

The second refinement involved incorporating the evolving pattern-density model

concept into the exponential PDSH model as shown in Appendix C. This required changing the model to calculate removal rates based on a fine time interval (1 sec.), shown in Figure C-2, as opposed to direct calculation of final step-height and thickness solutions at the given experimental time intervals, as in the previous model also shown in Figure C-3. The code was extended to input the  $40\mu m$  by  $40\mu m$  discretized extracted pattern density maps for  $\beta$ ,  $\beta/2$ , and zero bias. The projected pattern-densities as a function of step-height are calculated and updated with each time step, as subsequent step-height reduction occurs. This model is more computationally intensive because of the time stepping; however, it updates the local pattern-density, effective pattern-density, and the current step-height with each time step in order to calculate a more physical simulation of deposited topography removal.

The third refinement involved the handling of negative  $\rho$  values. In features that have a side length less than that of the step-height, it is not uncommon that their deposition profile results in a triangular peak as previously mentioned. This will cause the concavity of the pattern density distribution over decreasing step-height (i.e., increasing polish time) to decrease, eventually becoming negative, and then with increasing time and step-height reduction, to become positive once again, as shown in Figure 2-19.

In order to avoid faulty modeling using the negative  $\rho$  values with no physical significance, we employ a clipping of any  $\rho$  values at 0, as shown in Figure 2-20. This ensures that in the model there are no negative pattern densities, since physically there are no pattern densities which increase, decrease, and then increase once again within one polish. It is our assumption that for small features, the pattern density will be well-approximated by zero, until the step-height falls below some point at which time the pattern-density will increase as shown in Figure 2-19.

Once these three refinements were made, we were able to fit the evolution of pattern density PDSH model against the same experimental data. A small decrease in error (roughly 4 %) results, as shown in Figure 2-20 and Figure 2-11 as compared to 2-10 and Figure 2-11. The planarization length of 1.47mm and a characteristic step height of approximately 841 Åare fit by the model. All of our measurement points

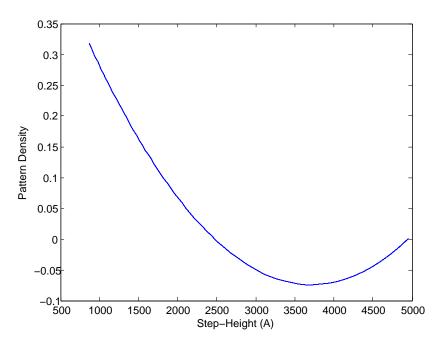


Figure 2-19: EA03 region pattern-density vs. step-height.

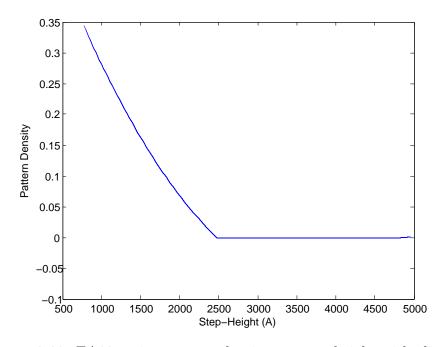


Figure 2-20: EA03 region pattern-density vs. step-height with clipping.

are in the relatively large LRPD region. However, considering the periodic nature of the die position on the wafer, we are able to see that the fitting at the edge which would be nearest to the EA region, i.e.,the first five points, are better fit to the data in that region than in the previous version of the model.

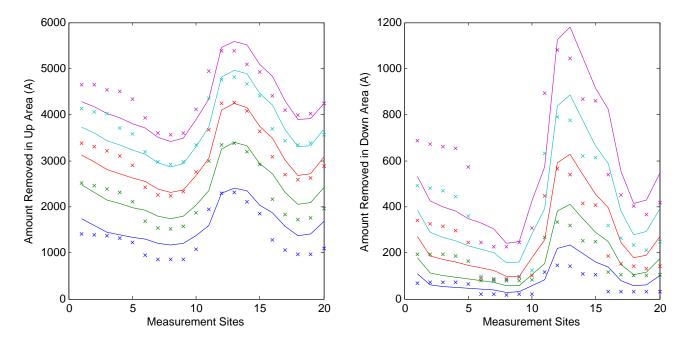


Figure 2-21: Model fit (lines) of exponential PDSH model to new experimental data ("x" points) during oxide stage of STI CMP.

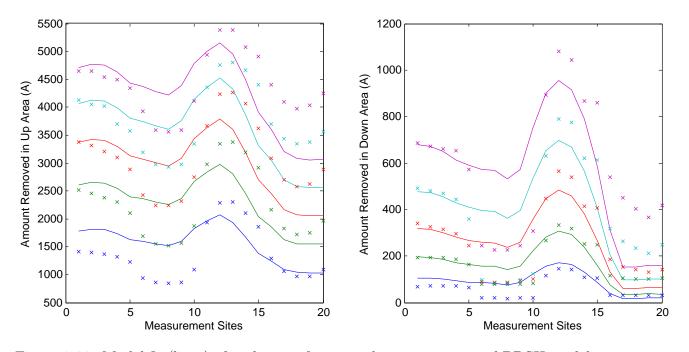


Figure 2-22: Model fit (lines) of evolution of pattern density exponential PDSH model to new experimental data ("x" points) during oxide stage of STI CMP.

#### 2.4 Summary

Using our evolving pattern-density model concept integrated with the exponential PDSH model, we are able to reduce the model RMS error by 4%. However, the test

structures that are measured to verify the model as outlined in Appendix A, Figure A-4, are all larger than the 1-10  $\mu$ m size range proven to be the most affected by our model in Section 2.2. Therefore we are currently taking dense measurements in the EA region with feature sizes in the 1-10 $\mu$ m range in order to explore model accuracy in feature sizes that are more dependent on pattern-density evolution, which are the features closest to those found in actual products.

### Chapter 3

## Full Electrochemical Wafer-Level Modeling for eCMP

In this chapter, we first review previous work on wafer-level eCMP models in Section 3.1. A new model that considers the electrochemistry at both the anode and cathode is then presented in Section 3.2. A semi-3D version of the model is described in Section 3.3, and preliminary results are presented in Section 3.4.

#### 3.1 Evolution of Wafer-Level eCMP Models

Our group at MIT was among the first to take on the challenge of modeling the wafer-level uniformity of the eCMP process, in an attempt to understand its case as a viable alternative to conventional copper CMP. Such a model, coupled to die-level modeling of topography evolution, is also important as extensions are sought to enable eCMP in a three platen process in which copper is not only thinned but also removed to the barrier, and then the barrier metal is removed as well.

#### 3.1.1 Ohmic eCMP Model

A first generation physical, non-empirical model to predict the removal and controlling mechanisms of eCMP was a "time-stepped finite element approach to calculate copper removal" developed by Truque et al. [8]. The crux of the model is an ohmic relationship between voltage and current, coupled with the direct electrochemical relationship between applied charge at the cathode and removal rate as shown in Equation 3.1.

$$I\left[\frac{C}{sec}\right] \cdot \frac{1}{area\left[cm^{2}\right]} \cdot \frac{1atom_{Cu}}{2e^{-}\left[C\right]} \cdot \frac{1mole_{Cu}}{N_{A}atoms_{Cu}} \cdot \frac{63.546g_{CU}}{1mole_{Cu}} \cdot \frac{cm^{3}}{1cm} \cdot \frac{10^{7}nm}{1cm} \cdot \frac{60sec}{1min} = RR\left[\frac{nm}{min}\right] \quad (3.1)$$

The derivation of this equation can be described as follows. Applied current, a charge transfer per second, I(C/sec), is divided by the area to give the current density. Employing the assumptions that two electrons are required for the removal for every one atom of Cu, the molar weight and density are factored by the number of atoms per electron to give the scaled removal rate in nm/min. If this removal rate is then divided by the current, I, the removal rate per unit charge can be obtained as shown in Equation 3.1. This equation is derived both in Truque's thesis [8] and by Smekalin et al. [19] such that for a 300 mm wafer the rate becomes 30 nm/(A-min), or in layman's terms, "for every minute 1 amp of current is applied to the wafer polish process an average Cu thickness of 30 nm is removed" [8]. There can be model adjustments made for edge exclusion [16], grain boundaries in polycrystalline structures, and etching effects due to oxidizing action.

The current density distribution, J, is calculated using a 3-D discretization of the wafer and the electrolyte using a stack of resistance meshes as shown in Figure 3-1.

The first mesh at the bottom of the figure represents the Cu layer on the wafer surface, and is made up of nodes which connect to the respective nodes of the meshes above it, which represent n mesh levels of the electrolyte. The electrolyte is composed of n mesh levels to extend the model to view the current distribution both laterally and vertically through all conductive components (pad, electrolyte, and wafer) and all voltage zones.

The "ohmic" assumption of the model is implemented in the algorithm used to

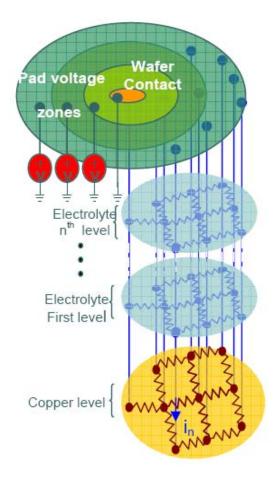


Figure 3-1: Ohmic model mesh representation [8].

compute the conductance matrix, which represents all of the mesh layers. The circuit representation of the model is shown in Figure 3-2. The conductance matrix is assembled in the commonly defined pattern of Kirchoff's Current Law (KCL) equations for each of the respective nodes in a 2-D matrix. The node position (layer), Cu thickness, and neighboring nodes are all kept in a linked matrix to the conductance matrix. At the Cu mesh level, conductances vary only by average thickness between horizontally neighboring nodes, such that  $g_{cu} = \frac{\sigma_{cu}}{T}$  where  $\sigma_{cu}$  is the conductivity of annealed Cu after electroplating and T is the Cu thickness. At the n electrolyte mesh levels, the horizontal conductances vary by cross-sectional areas and thickness given by their position, such that  $g_h = \frac{\sigma_{elect} \cdot h}{n}$ , whereas the vertical conductances between the layers vary with  $g_{\nu} = n \cdot \frac{\sigma_{elect} \cdot d^2}{h}$  where d is the discretization size used,  $\sigma_{elect}$  is the conductivity of the electrolyte, and h is the equivalent electrolyte thickness.

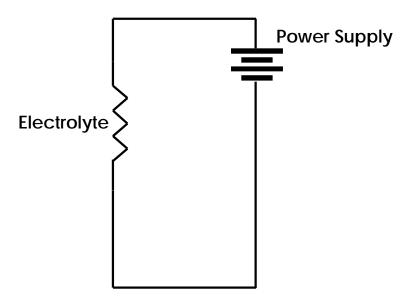


Figure 3-2: Equivalent circuit representation of ohmic model.

The equivalent electrolyte thickness serves as a lumped fitting parameter as opposed to an actual thickness approximation, to account for the perforated structure of the polishing pad, where holes are opened to expose the electrolyte to the metal electrode underlying the pad. Once all of the values of the conductance matrix are properly assigned, the system is solved using the corresponding voltage drops across the matrix based on the voltage applied in each zone, and with the wafer contact region acting as virtual ground. Given the calculated voltages, the static current density defined by Equation 3.2 is found:

$$J = \sigma \nabla \phi \tag{3.2}$$

Here  $\sigma$  is the lumped ionic electrical conductivity of the electrolyte (previously mentioned as  $\sigma_{elect}$ ) and  $\phi$  is the electrical potential assuming that the wafer and pad are static as circuit elements. In order to accurately model the rotation of the pad and wafer on the eCMP platen, the current values are radially averaged in the time frame of a minute, and then divided by the area of the discretized units to give the current

density per node to find the removal rate using Equation 3.1. The removal rate is then multiplied by the time step to obtain removal amount, and the Cu thickness map and conductance matrix are updated for the following time step, until the final time step is reached.

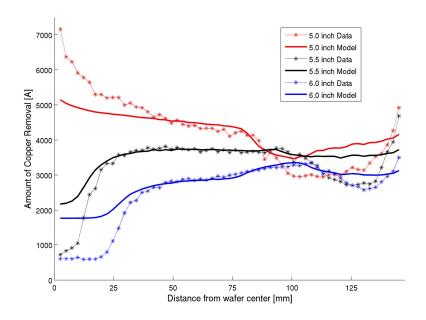


Figure 3-3: Amount of Cu removal for head positions of 5.0, 5.5, and 6.0 inches, and voltage zone setting of V1, V2, V3 = 2, 1, 3V. Basic ohmic model versus data. The RMS error of this fit is  $532\text{\AA}$  [9].

Though this model was a first attempt, it is able to capture the principal spatial-trends of the wafer-level uniformity as shown in Figure 3-3. In Figure 3-3, one can see that the model is fitting fairly well everywhere, with the exception of the first 25 mm (center) and the furthest 25 mm (edge). The discrepancies expose the weaknesses of the model, which will predict spatial dependence of the Cu removal rate based on the spatial distribution of current flow as a function of the applied voltage in different cathode zones. The model does not take into account the "non-ideal" electrochemical reactions at the wafer surface which are the actual source of the current, as the model instead focuses on current flow within the electrolyte and wafer copper layer as a function of the spatial voltage zones, which are modeled as ideal voltage sources. The voltage sources can be modeled as ideal; however, the value of the current is not based solely on a linear resistance, but is rather based on the electrochemical reactions at

the electrodes.

#### 3.1.2 Non-Ohmic eCMP Model

As an extension of the ohmic model, the next phase of eCMP modeling sought to account for the non-idealities at the wafer center and edge. There are many physically-based hypotheses as to the cause of these discrepancies, including the area of the wafer in electrical contact with the grounding region at the center of the pad having different bias conditions, the effect of the location of the polish head relative to the cathode voltage zones, and uneven electrolyte distribution due to the pad pressure and speed variations [9]. However, prior to exploring the empirical effect of each of these process and tool limitations, the actual mechanisms of removal must be further researched, understood, and implemented into the model, most importantly the mechanism of electrochemistry.

The ohmic eCMP model was shown to fit fairly well for a cathode zone voltage biased at 3V or 0V but poorly for intermediate voltages, suggesting that there are non-idealities with respect to biased voltages. Additional experiments were conducted using only one cathode zone biased at five different voltages with a fixed head position, and a nonlinear relationship was observed between removal rate and applied voltage [9] as shown in Figure 3-4.

This observation of nonlinearity is the core of the "non-ohmic" assumption used to correct the non-idealities of the previous model. In Figure 3-4 there is a non-linear relationship observed between the amount of Cu removed and the voltage applied to the cathode zone. Noting that the electrochemical reactions taking place at the anode are a key mechanism for Cu removal, we must take into account the Butler-Volmer model of electrode kinetics. The Butler-Volmer equation relates the surface overpotential at the electrode-electrolyte interface to the current density [10], which will give us the expected nonlinear relationship between the voltage and current density. Equation 3.3 shows this relation in the form of a boundary-value problem on boundary surface  $\Gamma_A$ , in which the current at the anode and cathode is summed as the Faradaic current contribution, and is set equal to the conduction current or

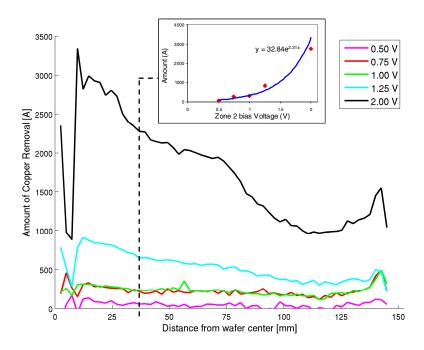


Figure 3-4: Experimentally measured Cu removal in 89 seconds for five different values of V2 (V1 and V2 held at 0V). Figure inset shows the nonlinear relationship observed between V2 and the removal amount for a selected wafer radius [9].

"ohmic" relation used in the previous version of the model [9].

$$-\sigma \nabla \phi \cdot n = i_o \left( e^{\frac{\alpha_a F}{RT} \phi} - e^{-\frac{\alpha_c F}{RT} \phi} \right) \text{ on } \Gamma_A$$
 (3.3)

Here  $i_0$  is the exchange current density,  $\alpha_a$  and  $\alpha_c$  are the kinetic transfer coefficients of the anodic and cathodic components, respectively, of the electrochemical reaction relating how the applied potential favors one direction of the reaction over the other. Also,  $\frac{\alpha_a F}{RT}$  represent the Tafel slope which depends on the transfer coefficient, temperature and universal gas constant.

In this case, solving the boundary-value problem was superseded by the necessity to accurately model, one-dimensionally, the electrochemical interaction effect on the current density and thus the removal rate, as shown in the schematic configuration in Figure 3-5. The configuration consisting of a perforated pad allows for the use of Equation 3.2 without additional effects like "global ion diffusion, drift, or convec-

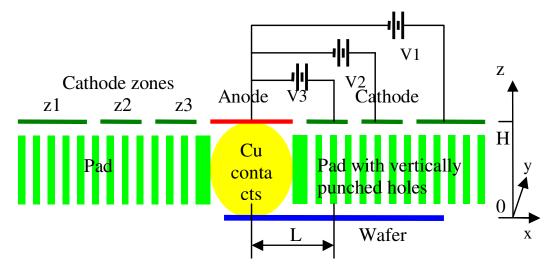


Figure 3-5: eCMP configuration for non-ohmic model [9].

tion" [9], by confining an invariably small and non-mobile amount of electrolyte with virtual direct contact with the pad and the Cu wafer. The lateral currents within the electrolyte are also neglected in the belief that the currents in each hole are independent of one another. In effect, each hole is an individual system decoupled from the whole to maintain an ohmic or "resistor-like" behavior for the electrolyte, and a Butler-Volmer relation or "diode-like" behavior only exists at the wafer (anode) and the pad (cathode). An important approximation is made here to allow the Butler-Volmer overpotential for both the anode and cathode to be represented by one equivalent diode with Equation 3.4.

$$j = j_0 e^{\frac{\alpha_a F}{RT} \eta_s} \tag{3.4}$$

Here  $\eta_s$  is the surface overpotential at the cathode and  $j_0$  is the exchange current density at equilibrium rate constant. Therefore, the equivalent circuit looks like Figure 3-6 as opposed to Figure 3-2, which was the basic 1-D equivalent circuit of the purely ohmic model.

Furthermore, since this is a 1-D model, the calculation is straight forward, but the introduction of electrochemical parameters calls for more fitting. Given the applied

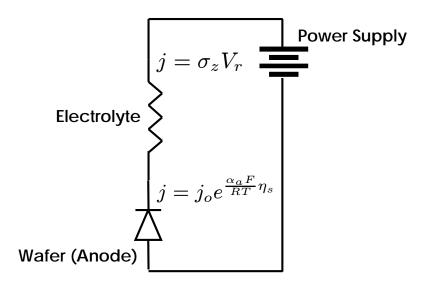


Figure 3-6: Equivalent circuit model for non-ohmic eCMP model.

voltage, V, of the cathode zone (comprised of the voltage across the electrolyte and the surface overpotential at the electrodes) the calculation is now just solving for overpotential of the equivalent currents of Equation 3.4 and Ohm's law, as shown in Equation 3.5 below.

$$\sigma_z V_R = j_0 e^{\frac{\alpha_a F}{RT} \eta_s} \tag{3.5}$$

The one-dimensional currents are calculated for discretized points across the surface of the wafer, and a similar time-average as in the previous model is used to determine removal rates as a function of distance from the wafer center. This non-ohmic eCMP model yields considerably more accurate results than that of the ohmic eCMP model, as shown in Figure 3-7.

Nevertheless, there are still lingering concerns about the fitting at the wafer edge, where the model is still overestimating removal. Initially, one must question the viability of the one-diode assumption made for combining the electrochemical reactions at both the anode and cathode. Another component of the electrochemical reactions taking place at the electrodes is that of the aforementioned passivation layer of soft  $Cu^{2+}$  which forms at the wafer surface, blocking removal in the recesses until there is

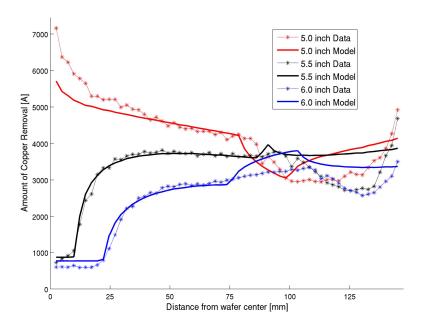


Figure 3-7: Amount of Cu removal for head positions of 5.0, 5.5, and 6.0 inches, and voltage zone setting of V1, V2, V3 = 2,1,3V. Non-ohmic model versus data. The RMS error of this fit is 412Å, a 22% improvement [9].

sufficient downforce and planarity with the up areas. The passivation layer may not be uniformly layered across the wafer, and may not be instantaneously removed as previously assumed. An additional overriding assumption is that the zone voltages each are high enough to facilitate current flow that equals the conduction current and thus directly translates to copper removal, whereas in traditional electrochemistry [10] there exists an activation overpotential at which the current jumps higher than the conduction current such that it becomes the dominant current source, at which point current is no longer equal to conduction current but rather is a substantially higher value.

#### 3.2 Two-Diode Non-Ohmic eCMP Model

In order to transform this modeling effort beyond simply extending the model with incremental gains in error or "goodness of fit," one must understand the driving mechanisms of the current density and its facilitation of Cu removal. In the previous section we have established that the primary driver is the electrochemical reactions

taking place at the electrode-electrolyte interface. However, thus far there have only been assumptions based on empirical evidence as opposed to electrochemical analysis of the system itself. Deeper electrochemical understanding will allow us not only to model eCMP for the first platen, but in the future for all three platens because a complete model based in physical understanding of the process itself is more extendable to additional metals and materials.

To begin with, we consider a typical electrochemical cell as shown in Figure 3-8. This will allow a more complete electrochemical analysis of the reactions and kinetics that drive the model parameters to accurately characterize the eCMP process. The following will explain the convention of the electrical current contributions, chemical reactions, and electrochemical kinetics which are known to govern a typical electrochemical cell like that of Figure 3-8, and relate them to the electrochemical cell created by the eCMP process.

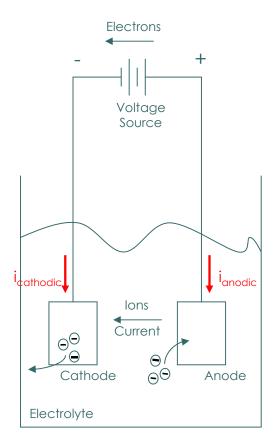


Figure 3-8: Electrochemical cell (After [10]).

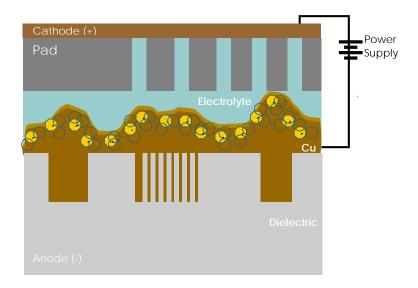


Figure 3-9: Schematic of eCMP Setup

There are three key components of the electrochemical cell: the electrodes, electrolyte, and an external conductor. The typical electrochemical cell has two electrodes where reactions can occur: a cathode, where electrons enter the cell and a reduction reaction occurs, and an anode, where electrons leave the cell and oxidation occurs. In the eCMP process, the Cu plated wafer is the anode, which is where the intended dissolution of Cu or oxidation occurs, and the platen behind the pad serves as the cathode, which is where Cu is slowly replated or reduction occurs. The next component is the electrolyte which is the solution in which ions are the mobile species, as opposed to the electrodes where electrons are the mobile species, allowing for the conductive movement of Cu ions. Lastly, there is an external conductor which provides the continuity of the circuit; in the eCMP process this enables the externally biased zone voltages. The external conductor, or voltage source, provides what is called the conduction current; it follows the Ohm's law calculation of the former ohmic eCMP model. The two electrodes create the Faradaic current which follows the Butler-Volmer relationship for each of their respective reactions, yielding equal and opposite currents as shown in the Equation 3.6. Here  $\alpha_a$  and  $\alpha_c$  are the kinetic transfer coefficients of the anodic and cathodic components of the electrochemical reaction, relating how the applied potential favors the direction of one reaction over the other.

$$\frac{i}{i_o} = e^{\frac{\alpha_a F}{RT} \eta_s} - e^{-\frac{\alpha_c F}{RT} \eta_s} \tag{3.6}$$

We observe once again in Equation 3.6,  $i_o$  is the exchange current density, and now  $\eta_s$  is the surface overpotential created by the electrochemical reacton at the interface, which from the exponential term known as the Tafel slope, is also dependent upon the transfer coefficient determining the reaction rate [10]. The previous assumption in the non-ohmic eCMP model is to cancel the term of the cathodic contribution since the anodic reaction is favored in eCMP (Cu dissolution). The electrolyte also generates different currents when an electric field is applied, but using the assumption of the perforated pad from the former non-ohmic eCMP model, we can neglect migration, diffusion and convection currents to yield an equivalent circuit model for the two-diode non-ohmic eCMP model as shown in Figure 3-10.

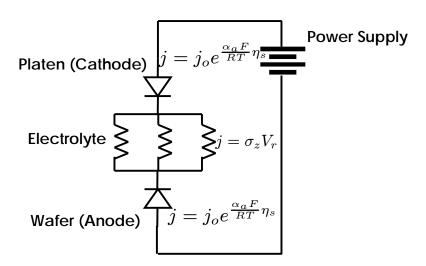


Figure 3-10: Equivalent circuit model for two-diode non-ohmic eCMP model.

Now that we are able to more accurately model the electrochemical reactions and potential distributions at the anode, cathode, and within the electrolyte, the calculations can be re-derived into a form similar to the non-ohmic eCMP model for a 1-D case. Using Newman's derivation of applied voltage, Equation 3.6 and

measurements from a conventional three-electrode experimental measurement to find the two surface overpotentials, we can solve for the only unknown,  $\nabla \phi_{ohm,sol}$  [10].

$$V_{app} = \eta_{s,anode} + E_{eqbm} + \nabla \phi_{ohm,sol} - \eta_{s,cathode}$$
 (3.7)

Then we can plug this value into the equivalent equation from the previous nonohmic eCMP Model, Equation 3.6, for the value of  $V_R$ . Additionally, experimental electrochemical measurements can replace the fitting of the Tafel slope, such that the only fitting done will be that of the exchange current density,  $j_o$ .

This model is still neglecting the lateral current distribution within the electrolyte, because it is only meant to serve as an accurate 1-D electrochemically-based approximation for each mesh level (2-D), as shown in the mesh level representations of the eCMP setup which will be explored in the next section.

# 3.3 Objectives and Framework of Semi 3-D Two Diode eCMP Model

Equipped with the necessary understanding of the electrochemical mechanism that governs the Cu removal in eCMP, the model can transition back to a 3-D model as originally developed in the ohmic eCMP model case. In particular, the contribution of the lateral currents can be added back in, with the advent of the second and third dimensions of the model.

We have determined that, much like the initial ohmic eCMP model, a full 3-D is possible but very computationally intensive; thus, we have settled on a semi 3-D version of the model. Initially we will set up a 3-D resistor and diode grid, consisting of a similar conductance matrix as in the initial model, but now with the non-linear elements to express the anode and cathode reactions, as shown in Figure 3-11, for each of the mesh levels.

The current across each circuit element and voltage at each node will be calculated

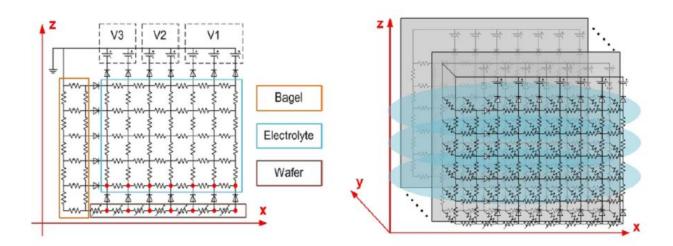


Figure 3-11: 2-D and 3-D representation of matrix for resistor and diode elements in eCMP model setup.

for a given snapshot in time, using the derived Equation 3.7 from the two-diode non-ohmic eCMP model and Kirchoff's current law (KCL). Then, instead of 3-D time averaging and calculation, we will do a 2-D radial time average of the current values in the time frame of a minute, and then divide by the area of the discretized units to give the current density per node, to find the removal rate using Equation 3.1.

# 3.4 Verification of Two Diode Non-Ohmic eCMP Model

The semi 3-D numerical implementation of the two-diode non-ohmic eCMP model proposed in this thesis has been performed by Wei Fan. Here, we show the experimental setup and preliminary results from this numerical model, and discuss on-going work to fit and verify the new model using experimental data.

### 3.4.1 Experimental Setup

The eCMP modeling work will be verified and calibrated using data measurements from experiments done on the Applied Materials Reflexion LK eCMP tool by Truque[8],

in collaboration with Chris Borst of SUNY Albany. The tool has a three platen setup, the first of which is where the eCMP takes place, and the latter two platens and steps used to perform conventional CMP to complete the remaining Cu removal and barrier removal, as shown in Figure 3-12. This tool setup consists of three concentric voltage zones for the polishing pad to more evenly remove material from the three key regions of the wafer when desired, as shown in Figure 3-13. There is also a wafer contact region, which serves as the central contact from the pad to the wafer edge. The proprietary electrolyte used is composed of a "diluted citric acid solution mixed with hydrogen peroxide and proprietary additives" [8] and is allowed to flow freely between the pad and the wafer. This setup is used during the first platen process of the Cu planarization and is the only platen modeled in this thesis.

The process conditions which were varied included that of the head position, varied at 5, 5.5, and 6 inches. In addition, the voltage zones were varied as previously mentioned, typically with the following voltages: V1, V2, V3 = 2, 1, 3V.

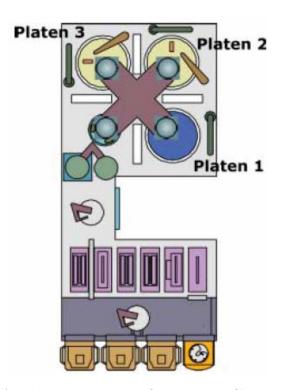


Figure 3-12: Applied Materials Reflexion LK eCMP platform [11].

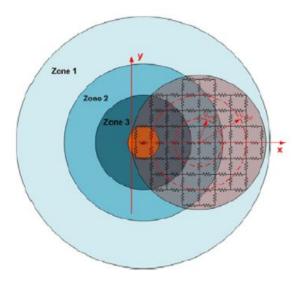


Figure 3-13: Voltage zone top-down view over wafer configuration.

### 3.4.2 Semi-3D Model

Wei Fan has performed the initial simulation for the semi-3D model implementation as shown in the following figures. Figures 3-14 through 3-16 show the application of the model for each voltage zone applied independently with the remaining voltage zones left at 0V. Here we see the voltage distribution at the wafer surface and the time averaged result based on the distance from the wafer's center. These simulations are based on assumed (literature) values for all electrochemical parameters (i.e.  $\alpha_a, \alpha_c$ , etc.). Future work includes fitting these to the available experiment eCMP data. Once fitted with previous experimental data we will be able to determine the accuracy of this semi-3D approach.

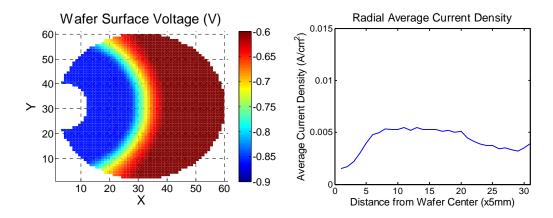


Figure 3-14: Voltage across wafer surface and time-averaged result, Zone 1 = 1V.

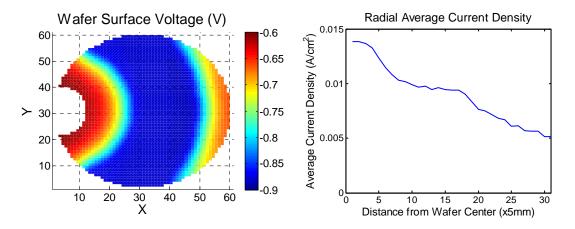


Figure 3-15: Voltage across wafer surface and time-averaged result, Zone 2 = 1V.

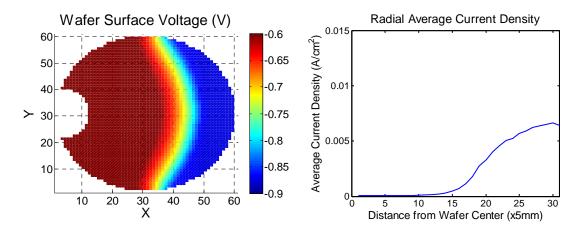


Figure 3-16: Voltage across wafer surface and time-averaged result, Zone 3 = 1V.

### 3.5 Summary

The premise of a new two-diode non-ohmic eCMP model is established in this chapter. This model seeks to more precisely account for the electrochemical reactions at both the interface of the anode and cathode to properly determine the behavior of the current driving removal in copper eCMP. The implementation of this model in a semi 3D model and the simulation capabilities are currently being investigated in collaboration with Wei Fan, to verify the improved model accuracy against experimental data.

## Chapter 4

### **Conclusions**

### 4.1 Thesis Contributions

This thesis makes several contributions to the theoretical modeling and physical understanding of the mechanisms behind both the STI CMP process and eCMP processes, at their respective scales. The following sections succintly describe the primary contributions and future work in both areas.

## 4.1.1 Evolution of Pattern Density Die-Level Model for STI CMP

The evolution of pattern density die-level model is an important contribution to the understanding of the physical mechanisms, deposition profile effects and geometrical topography changes taking place during planarization using CMP. This model addresses the previous assumptions of constant pattern-density by defining the deposition profile geometry resulting from the deposition process parameters and simulating its evolving pattern density effects, which has not been done previously. We have shown numerical simulation verification of the practicality of this model and once verified using product-size features, the model is expected to yield a significant increase in model accuracy in both the up and down areas of sub- $10\mu$ m features.

#### 4.1.2 Full Electrochemical Wafer-Level Model for eCMP

Through the two diode eCMP model proposed in this thesis, we contribute a more complete and accurate picture of the electrochemical cell that drives removal in the eCMP planarization process. The improved model captures the nonlinear dependence on applied voltages in multiple zones in eCMP tools, and incorporates electrochemical effects that are important for eCMP of copper and potentially other metals. A deeper understanding of how the current from the electrochemical reactions at the surface of the anode and cathode, which drive planarization, is employed to allow us to better understand nonlinear removal and possibly aid in future process control. Coupled with the complete simulation of the semi 3-D two diode eCMP model, this model will allow for extension to not only the complete copper removal but additionally provides the flexibility needed to extend to the barrier metal as well. Thus this model framework has laid the foundation for a full eCMP process to be modeled without the use of conventional CMP.

### 4.2 Future Work

In both models explored in this thesis there is work that could be done to further their accuracy and efficiency. In the case of the STI CMP model we are currently in the process of taking dense sets of AFM and Wyko measurements of the EA Region in our test wafers in order to verify the quadratic dependence of pattern density on step-height in small features. Additionally, we have yet to explore non-conventional slurry effects on removal rate, atypical layout effects and more explicit physically-based phenomena models in order to improve our semi-empirical PDSH model, all of which we hope to explore in the near future. In terms of the eCMP model we are currently fitting the semi-3D implementation of the two-diode non-ohmic eCMP model to experimental data in order to determine the accuracy of the new model. Furthermore, in the area of eCMP there has been very little modeling done which leaves many areas for further work including better chemical composition models, electrochemical reaction models, and models for eCMP tools with conductive pads.

## Appendix A

## STI Test Mask Documentation

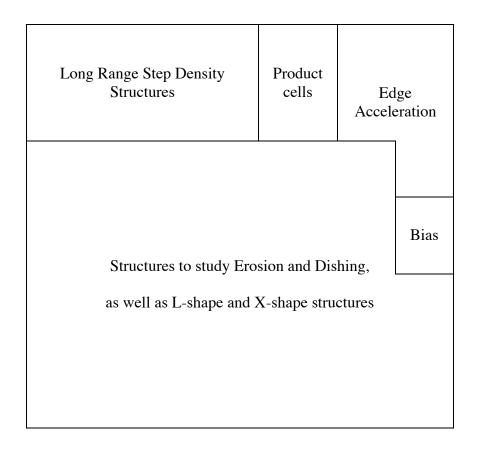


Figure A-1: STI mask floor plan [7].

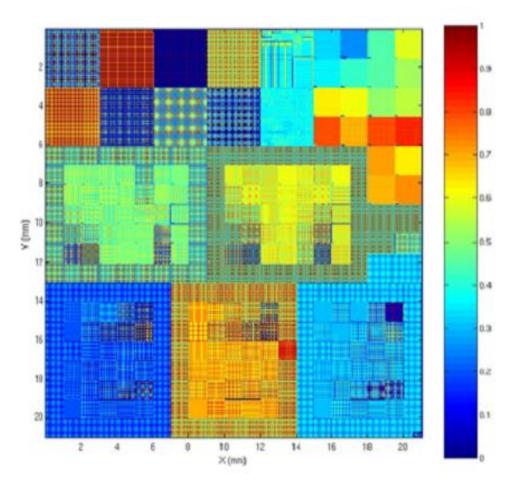


Figure A-2: STI mask local pattern-density map [7].

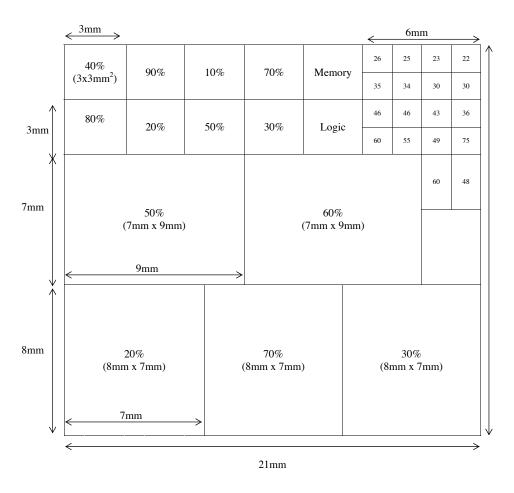


Figure A-3: Density distribution of STI mask floor plan [7].

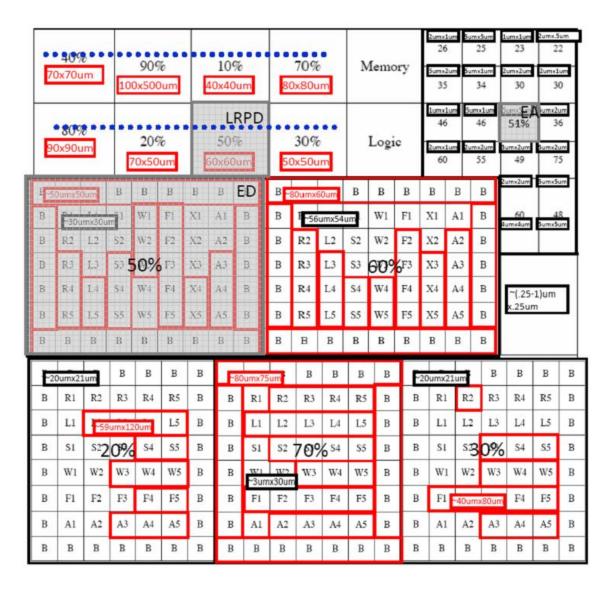


Figure A-4: Feature size specifications and measurement locations of STI mask floor plan. Measurement sites 1 to 20 are from left to right along top cutline, and sites 21 to 40 are from left to right along second cutline.

## Appendix B

**NSC STI Experiment** 

Documentation

	Downforce (psi)	Actual time(sec)	Planned time(sec)	Wafer#
Run 1	1.5	24	20	1
	1.5	48	40	2
	1.5	72	60	3
	1.5	96	80	4
	1.5	120	100	5
	1.5	144	120	6
	1.5	168	140	7
	1.5	192	160	8
	1.5	216	180	9
	1.5	240	200	10
Run 2	1.5	48	40	11
	1.5	96	80	12
	1.5	144	120	13
	1.5	192	160	14
	1.5	240	200	15
Run 3	3	24	20	16
	3	36	30	17
	3	48	40	18
	3	60	50	19
	3	72	60	20
	3	84	70	21
	3	96	80	22
	3	108	90	23
	3	120	100	24
	3	132	110	25

Figure B-1: Silica slurry experiments run table.

## Appendix C

Modeling Illustrations

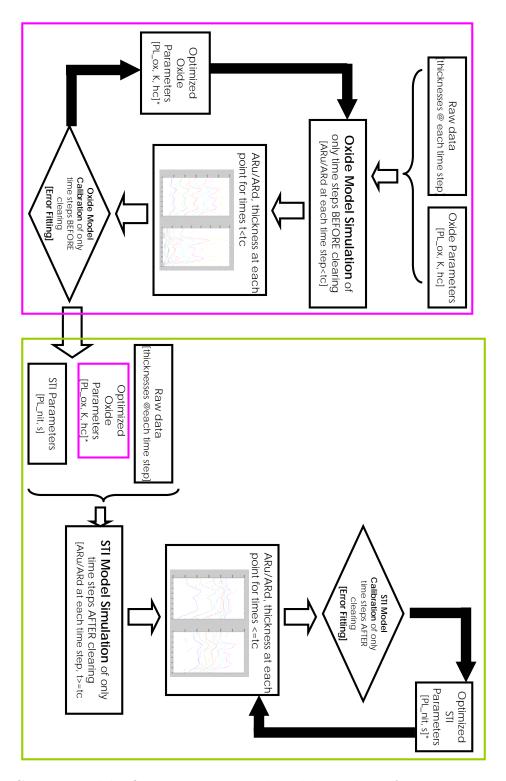


Figure C-1: 1st model refinement: Decoupled modeling scheme for exponential PDSH model for dual material.

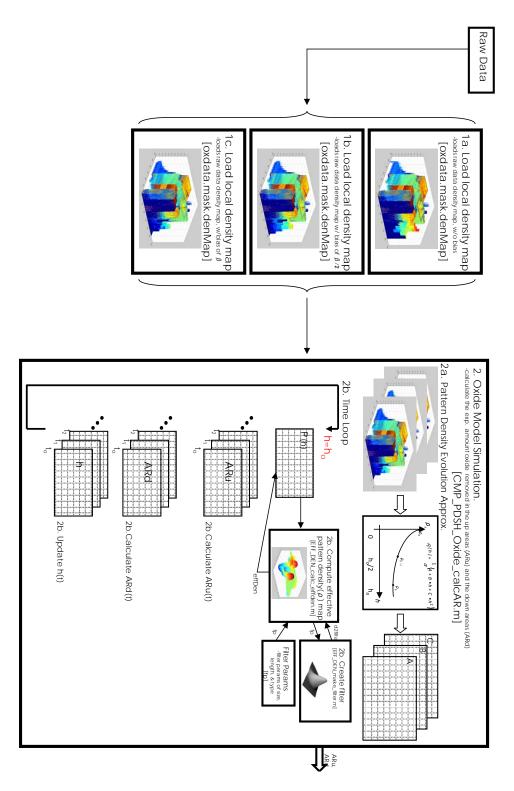


Figure C-2: Evolution of pattern-density exponential PDSH model scheme.

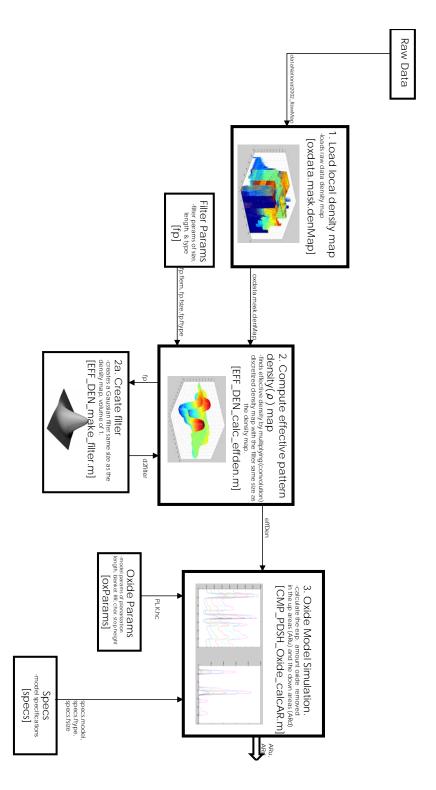


Figure C-3: Exponential PDSH model scheme: Part 1.

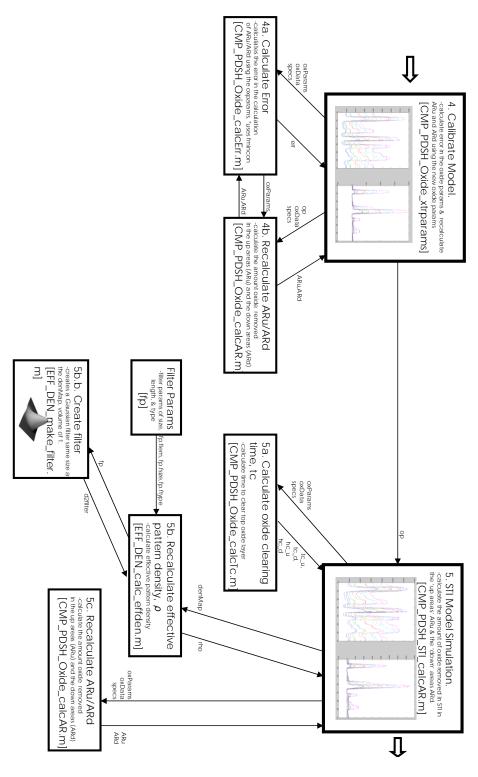


Figure C-4: Exponential PDSH model scheme: Part 2.

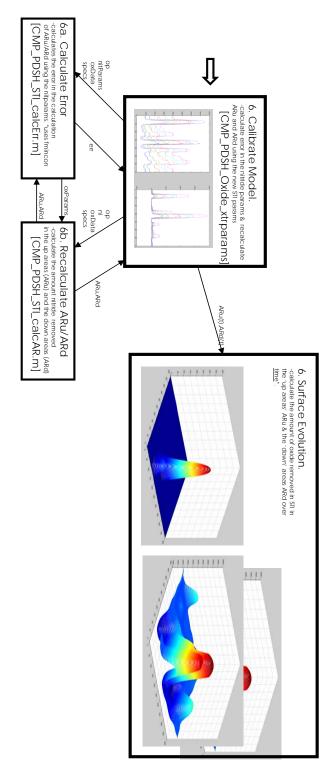


Figure C-5: Exponential PDSH model scheme: Part 3.

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