STANDARDIZING AND IMPROVING TEST WAFER PROCESSES: INVENTORY OPTIMIZATION AND A DAYS OF INVENTORY PULL SYSTEM
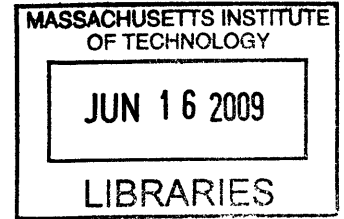
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Standardizing and Improving Test Wafer Processes:
Inventory Optimization and a Days of Inventory (DOI) Pull System

by

David W. Johnson

ABSTRACT

Summary:

Over the past few years, the Intel Fab-17 facility has aggressively pursued lean methodology to reduce the manufacturing costs associated with its aging 200mm diameter wafer process. One area ripe with improvement opportunities is the processes supplying and managing Test Wafers, which are non-production wafers used to verify production tools and operations.

With four test wafer types, hundreds of different sequences of operations (defined as routes), and varying consumption trends, thousands of decisions must be made daily to ensure Test Wafers are available on time and with the proper base characteristics. To further illustrate the magnitude and importance of Test Wafer systems, roughly the same number of Test Wafers are introduced each time period into the fab as production wafers.

Through direct observation and process mapping techniques, I identified two system level projects, each containing enormous cost and performance improvements to the entire facility.

__Project One: Reallocating excess inventory__
In analyzing the Test Wafer inventory quantity and consumption rates in primary stockroom, I noticed that certain routes had excess inventory while others were deficient, thus leading to significantly more expensive Test Wafers types to be used instead. In order to maximize realized cost savings, I developed a linear optimization program which distributed excess Test Wafer inventory to areas of need. Different re-allocation costs, initial material specifications, and forecasted consumption needs constrained the quantity and location for this redistribution.

Per the optimization program's recommendations, I led a team to re-allocate the largest excess Test Wafer inventory area to twelve different locations. The savings for this project correspond to over a year's worth of test wafer inventory now available for these routes and banks.

__Project Two: Determining supply decisions from a Days of Inventory (DOI) metric__
The previous process for supplying Test Wafers into the fab was complicated, lacked standardization, required significant human intervention, and led to tool performance impacts despite high operating costs. To address these issues, I designed, developed, and implemented a

program which prioritized and calculated thousands of test wafer decisions based upon a Days of Inventory (DOI) metric. By prioritizing actions based on the time until stock out, cost-effective decisions were made while ensuring Test Wafers are available at a tool when needed. The program forecasted short term consumption using an Exponentially Weighted Moving Average (EMWA) and pulled real-time inventory and available Test Wafer material to support the calculations and decision logic.

After a successful fab-wide pilot, the "DOI Scheduler" program has now replaced the previous test wafer supply process. As a result, internal fab test wafer inventory will decrease by approximately 35% (as of March 2009, inventory has dropped by 15% and continues downward), Test Wafer availability will improve by approximately75%, and 4 to 5hrs a week of labor resources have been saved. Equally important, the prior non-standard process is now standardized, enabling future Test Wafer improvement projects and allowing root cause analysis on previously unsolvable problems.

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This document has been reviewed and approved by the Intel Corporation. In order to protect Intel, sensitive material has been omitted or replaced with representative data. Aspects such as cost savings and production details are not included for this reason. Ratios and other non-specific metrics are used to quantify results for the reader while not violating Intel's confidentiality.

ACKNOWLEDGMENTS

"Somewhere, something incredible is waiting to be known…"
Dr. Carl Sagan

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[1] The irony of thesis length and contradiction to Clella's advice was quickly noted as the thesis continued to grow with seemingly no end in sight.

ABOUT THE AUTHOR

Often considered idealistic and in constant pursuit of "half full glasses," David Johnson left a rewarding career designing mechanical space systems at the Jet Propulsion Laboratory, NASA to follow his passion of helping people on a larger scale. Consistent with his logical and problem solving strengths, the Leaders for Manufacturing program offered an unmatched opportunity to hone business and technical acumen on the backbone of strong leadership skills. Post graduation, David looks forward to channeling his energy towards efforts in sustainability and environmental conservation.

David is an avid outdoorsman and can frequently be found either participating in or conjuring the next great adventure with his friends. Nothing brings him greater tranquility than a strong cup of coffee served thick and black shared with his fiancée, dog, and a gorgeous sunrise over snow-capped mountains or ocean waves breaking under a slight offshore breeze.

GLOSSARY

A3 Document: *A single page (A3 sized piece of paper or 85."x11" as more typical in USA standards) document which describes the current state, problem statement, hypothesis, and anticipated results. These are used to clearly visualize problem statements and results.*

Bank: *A group of Test Wafer inventory from multiple routes batched together by identical base characteristics.*

Bank Eaters: *Routes who require Test Wafers with the same base characteristics as grouped in a Test Wafer Bank. These routes will pull Test Wafers from this bank as need and availability determine.*

Bank Feeders: *Routes who's cleaned Test Wafers from R-GEN or P-GEN vendors are grouped together by their identical characteristics in the stock room, in a Test Wafer Bank.*

Days of Inventory (DOI): *A metric measuring inventory in terms of time until stock out. It is defined as the inventory quantity divided by the consumption rate in units per day.*

Fab-17: *The name of Intel Corporation's Hudson, MA manufacturing facility where this thesis project was completed. Each manufacturing facility has a particular name and operate as separate facilities although the processes used are interchangeable for each product line. This commonality is referred to the "virtual factory" concept.*

Fab Starts Group (FSG): *The group responsible for determining what, where, and when Test Wafers should be released into the fab. Additionally, FSG is responsible for moving Test Wafer lots from outside of the clean room to the first operation.[2]*

Kaizan: *A lean manufacturing term used to identify a focused improvement event on a particular problem or issue.*

Learning Card: *A single page document used to visually display an improvement hypothesis and test conditions. These are posted in the area of improvement and contain areas for feedback and comments. Once approval from all relevant stakeholders has been obtained and the hypothesis is validated, the improvement is incorporated into the standard work process.*

Lot: *A group of 25 wafers held together by a lot box. All operations and processes are standardized around these lot boxes in a 200mm wafer diameter facility.*

Operation: *A specific activity, movement, or process used to change Test Wafer properties or transfer to the next operations.*

PROC: *The acronym used for "processing." This term is used when wafer lots are moved from one operation to another.*

Route: *A specific sequence of operations linking all movements, pre-process activities, verification/validation steps, and removal course.*

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[2] Only Test Wafer specific activities are mentioned. For simplicity, production wafer activities are ignored for this thesis.

SWARM: *An Intel lean manufacturing term used to identify a group of individuals proactively searching for improvement opportunities often in a particular area or discipline.*

Test Wafer: *a non-production silicon wafer used for validation and verification purposes of various tools and processes. Multiple types of Test Wafers exist with different base characteristics as required by the tool and validation or verification process. The following four types of Test Wafer exist.*

Test Wafer – R-GEN: *A used Test Wafer sent to a vendor to be cleaned or recycled using chemical etching techniques to remove any surface materials and expose the bare silicon.*

Test Wafer – P-GEN: *A REGEN Test Wafer with an added polish step after the chemical etching to ensure a flat surface finish.*

Test Wafer - Reclaim: *A used Test Wafer sent to a vendor for more extreme cleaning or recycling operations. First, a chemical etch removed any surface material. Next, a series of grinding, lapping, and polishing operations commences leaving the bare silicon surface at the expense of greater material loss.*

Test Wafer - Prime: *A new silicon wafer designated to be used for Test Wafer purposes*

Wafer Cost: *The cost to manufacture a single wafer populated with chips. Each wafer is divided into numerous chips. As wafer diameter increases, the number of chips per wafer increases by a square factor drastically decreasing the Chip Cost for a single wafer. For this reason, an increase in wafer diameter is preferred in terms of an economy of scale argument.*

Recipe: *A specific set of cleaning operations (mostly chemical etch operations) used by R-GEN and P-GEN vendors to return a used Test Wafer back to its bare state.*

1 Introduction and Overview

The Intel Corporation is renowned for not only the design of sophisticated semi-conductor chipsets but also the efficient and cost effective manufacturing of such. In order to ensure high quality production, an extensive system of verifications, preventative maintenance, and validations are constantly conducted throughout the manufacturing line. To minimize the risk on high value production wafers, these test operations are run and monitored through the use of Test Wafers, wafers which are designated for non-production purposes.

Fab-17 in Hudson, Massachusetts is a 200mm diameter wafer facility manufacturing Intel products for over ten years. Historically, this facility has started more Test Wafers than production wafers manufactured for a given time period; this being consistent with industry standards. Due to the large usage volume and inherent cost per wafer, Test Wafers have always been a major contributor to the overall cost per production wafer.

This thesis provides a detailed description of two system level Test Wafer improvement hypotheses and their results at Fab-17. Chapter 1 outlines the problem and hypotheses. Chapter 2 contains the background and description of Test Wafers and the existing management systems. Chapter 3 provides a literature review addressing similar issues from industry and academia. Chapters 4 and 5 present the research analysis and approach for each improvement project. Lastly, Chapters 6 concludes with the results and thesis findings. This format was chosen to best inform the reader of the thesis projects in an efficient and effective fashion while providing great detail for those more interested and/or committed.

1.1 The Problem: General

The challenges and rewards associated with inventory management and supply from a general perspective are no different than that of Test Wafers. Cost savings obtained from optimal inventory quantities, minimizing holding costs, ensuring material availability, etc. can be extremely significant on the functioning of an organization and/or product delivery. Understanding how inventory and material supply systems behave will allow for the development of supporting systems ensuring low cost while improving and maintaining system performance. Whether with Test Wafers at Fab-17 or any other inventory material, these same root problems exist.

1.2 The Problem: Overview of Fab-17 Specific

Through a month of direct observations, numerous problems associated with system level Test Wafer inventory management continued to occur. Largely, a lack of standardization in Test Wafer processes led to wasteful operations, quality and process stability issues, enormous amounts of "human glue" and manual intervention, and the inability to easily and properly complete root cause analysis on many problems. Given the available time and resources for this research, two main problems were identified and attacked. The following two sections elaborate on the details with these problems.

It is important to note the significance of cost reduction and process improvement initiatives at Fab-17. With newer Intel sites transitioning to the larger, more cost effective 300mm and 450mm wafer architecture, Fab-17 must continue to drive wafer cost lower to maintain a competitive edge within the Intel network. Ultimately, the wafer cost metric is a deciding factor on the longevity of the plant. Fear of closing Fab-17 motivates many employees to embrace lean methodology and continuous improvement projects that reduce cost and cycle time, and improve quality and yield.

Lastly, the problem statements and hypotheses in this section are discussed prior to a sufficient background description of Test Wafers and their systems and processes at Fab-17. Any confusion regarding these aspects will be clarified in detail in Chapter 2.

1.2.1 Problem 1: Inventory location

A single stockroom located external to the manufacturing clean room manages all Test Wafer inventory. An external vendor provides the workforce to run the shipping/receiving and storage service; all inventory is owned by Intel once it arrives.

For most routes R-GEN and P-GEN Test Wafers are preferred as their cost is significantly less than a Prime or Reclaimed Test Wafer. Through observation, some routes contained seemingly large quantities of cheaper, recycled Test Wafer inventory (R-GEN and P-GEN Test Wafers, whereas other routes had little or small amounts of inventory. It became apparent that the preferred Test Wafer inventory of similar base characteristics was not optimally distributed across the different routes.

In order to better understand the discrepancy between route Test Wafer quantities, the consumption and scrap rates for each route were multiplied with the inventory levels to obtain the time duration until Test Wafer inventory would be depleted for each route.

For a one route, over 30 years of inventory had accumulated, while many other routes were either dry or days away from a stock out scenario. The cost impacts for the routes with inadequate inventory levels were significant; without the cheaper Test Wafers, Intel would need to start Prime or Reclaimed Test Wafers at a cost of approximately an order of magnitude greater. With hundreds of Test Wafer lots being affected, the cost impact was enormous.

Additionally, due to cleanliness issues, Test Wafer lots have a shelf life of roughly one year. Over this time particulates and/or surface oxidation occurs requiring the recycling and cleaning process to be repeated. Preferably, Test Wafer inventory would be used prior to this deadline as to avoid unnecessary re-cleaning costs.

1.2.2 Problem 2: Starting Test Wafers

Fab-17 maintains an inventory of Test Wafers within the fab for each route. The process for determining which Test Wafer types, what quantity, to which routes, and at what time was decided from a non-standard, highly labor intensive process located at the entrance of the fab. A program monitored the available quantity of Test Wafers in the fab for each route and flagged a notification when the actual quantity dropped below a fixed minimum level. Due to an environment highly sensitive to costs, the technicians responsible for communicating the Test Wafer order starting location to the stockroom would often not follow the program's recommendations unless a cheap Test Wafer was available in the stockroom. This behavior drove non-standard operations. To ensure Test Wafer availability, other technicians on the floor would need to communicate their needs adding unnecessary work. This "human glue" also led to frequent Test Wafer stock outs on the various routes.

Additionally, the minimum trigger levels were established many years ago and in most cases were no longer appropriate. Using a calculated consumption rate for each route, roughly half of the minimum levels corresponded to over 75 days of inventory. This excess impacted holding and opportunity costs, and increased the number of shelf-life violations, which resulted in rejecting Test Wafers. The histogram in Figure 1 illustrates the corresponding days of inventory to the total number of routes.
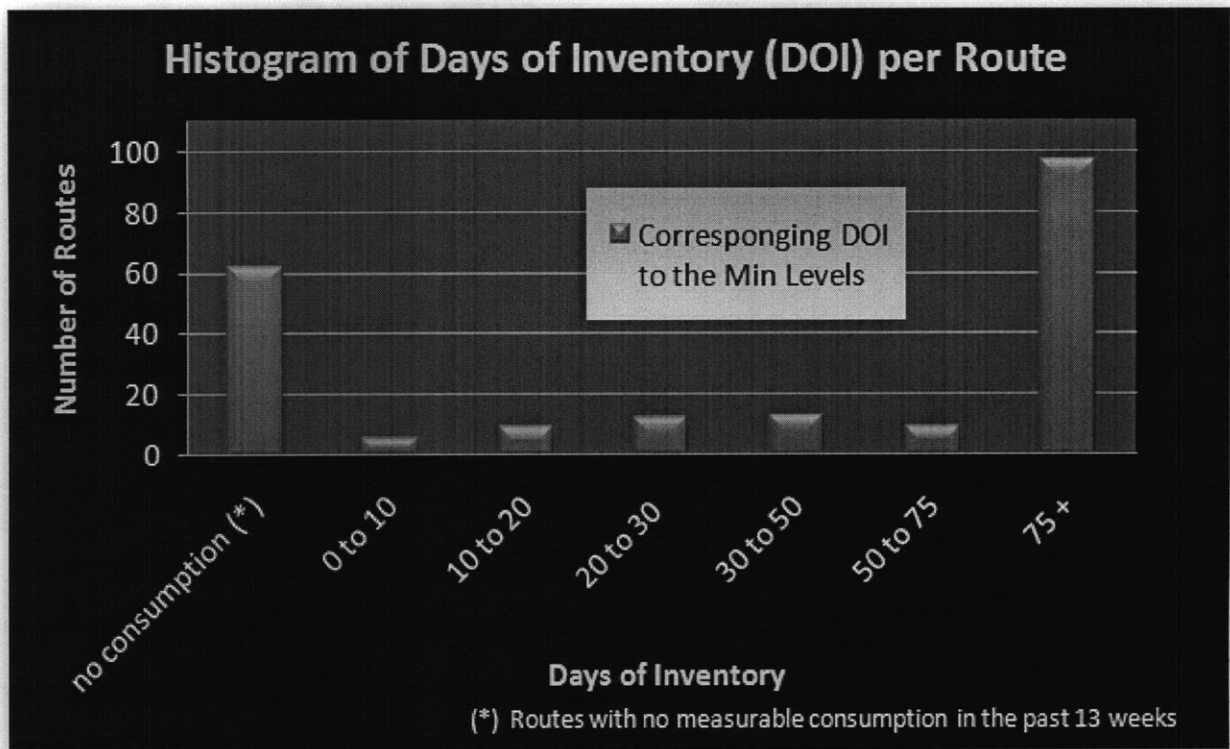
Figure 1: Histogram of DOI per route corresponding to the Min Level triggers

The non-standard process also led to an inability to complete root cause analysis on stock out causes or other Test Wafer starts decisions. On many occasions, a route would have a Test Wafer availability issue and the cause would be impossible to deduce often leading to repeat issues without correction.

In summary, the lack of standardization, required human intervention, non-optimal trigger levels all led to an extremely complicated system which performed only with technician heroics and high costs. Very few individuals understood all aspects leaving the Test Wafer starts process at a precarious position if any one of those individuals was sick or moved to different responsibilities.

1.3 Hypotheses

Two hypotheses were developed to attack each problem described above. By utilizing lean principles in the problem assessment and improvement approach, significant savings in inventory management and costs were anticipated while improving Test Wafer availability and fab performance.

1.3.1 Project 1 – Reallocating excess inventory

If excess Test Wafer inventory is optimally reallocated to starved routes/banks adhering to its base characteristics and requirements, then a total savings equivalent to a year's worth of inventory for

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those affected routes/banks will be observed. Enormous cost savings will be obtained from the monetary difference between starting the cheaper R-GEN or P-GEN Test Wafers instead of the expensive Prime or Reclaim wafers.[3]

1.3.2 Project 2 – Determining supply decisions from a DOI metric

If Test Wafer type, quantity, and location are optimally started based upon the prioritization of routes under a Days of Inventory (DOI) metric, then a robust standard process can be established simplifying work and eliminating human connections while decreasing in-fab Test Wafer inventory levels and improving Test Wafer availability. The DOI metric incorporates the consumption rate of Test Wafers into the metric. This rate would otherwise be communicated through non-value add connections. This approach is the foundation for process standardization allowing for root cause analysis and the foundation for future Test Wafer improvement projects.

1.4 Research Methodology

The research and implementation of the thesis projects occurred through the utilization of lean principles. Initially process and value stream mapping techniques, direct observation, and DMAIC (Design, Measure, Analysis, Improve, Control) strategies were used to establish and understand the current state. One of the largest challenges for this project was determining how to measure Test Wafer performance. Interacting with on-floor technicians and systems experts in all disciplines helped with ascertaining what information was available or easily obtained. Kaizan and SWARM events helped quickly identify key issues and built relationships with principal stakeholders helping ensure future implementation successes. A multi-disciplinary team focused on cost savings was also established which provided a great forum to educate and receive feedback throughout all departments. The details from this initial investigation will be discussed in detail in Chapter 2.

A comprehensive literature review augmented the hands-on research portion. Industry publications, prior LFM theses, and educational textbooks were used to understand inventory management related to Test Wafers. These findings will be summarized in Chapter 3.

Once the project analysis was completed, pilot programs were launched through the use of Learning Cards and A3 Documents. These tools help document and test the hypotheses. Under the approach of "small and rapid improvements," quick modifications were made ultimately leading to successful improvements.[4] The approach for each project will be explained in Chapters 4 and 5 with the results described in Chapter 6.

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[3] The exact monetary savings cannot be published but a estimate based upon public knowledge is provided in Section 5.

[4] Quotation taken from commonly used Lean terminology

2 Background and Current State

Understanding the immensely complex systems associated with Test Wafers has been the great challenge associated with this thesis.[5] As with any project, lasting and measurable improvements cannot occur without first understanding how the Test Wafer environment at Fab-17 operates. This section will attempt to provide a thorough background on the different types of Test Wafers, their usage and consumption, and the systems and processes used. Test Wafers have historically been treated as the "black sheep" of the fab; they are largely ignored and un-glorified until needed. At that point, they are a necessity despite being non-value add. For this reason, resources have not historically been allocated to improve and maintain effective Test Wafer operations. In studying this section the reader will invariably question many of the processes. From the perspective of this thesis, the reader should focus on understanding the state leading up to the specific hypothesis instead of developing new improvement hypotheses for the next LFM intern.

2.1 What is a Test Wafer?

Test Wafers are silicon wafers of the same properties as production wafers with the exception of being designated for verification and validation purposes only. Test Wafers are run in conjunction with maintenance activities, scheduled checks, out of specification operations, etc. Since the cost of scrapping a production wafer is large, due mainly to the number and length of the operations needed to get to the final product, Test Wafers are consumed at a large rate. For a semiconductor manufacturing facility with similar processes and age as Fab-17, the number of Test Wafers started is 1-3 times the number of production wafers started.[6] A few examples of different operations and routes where they are used are the following.

- Verifying the thickness of a deposition layer
- Checking the number of particles in a particular machine
- Running non-production dummy wafers to ensure steady state on an operation

For each route, there are restrictions on the Test Wafer characteristics. These characteristics are based on the process history, base material conditions, and the recycling approaches. The details of the types of routes will be discussed in section 2.2.

In addition, Test Wafers can be recycled and reused numerous times based upon the required Test Wafer characteristics for a specific route. In looking at the example of verifying the thickness of a deposition layer, the important characteristics may be the Test Wafer's thickness and flatness. Other concerns such as copper contamination are carefully controlled. The major input characteristics which distinguish each Test Wafer type are listed in Table 1.

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[5] Note that in many cases "… immensely complex systems…" could be referred to as "… unnecessarily complex systems…"

[6] As determined from internet searches and discussions with numerous individuals familiar with semiconductor manufacturing. The reason for this phenomenon deals with the high cost of scrapping parts in semiconductor manufacturing, particularly near the end of the manufacturing cycle. More Test Wafers (or framed as more cost) is added before running production wafers to minimize part defects.

Characteristic	Description / Significance
Resistance	- Measured in Ohm-cm and deals with capacitance and adherence measurements
Particles and cleanliness	- Measured by the size of particles per specific area. Often multiple tiers are used to separate the number of allowable particles by size and distribution density
Flatness / Thickness	- Physical characteristic parameters critical for many operations
Copper Contamination	- Important to note that once a Test Wafer has been exposed to any type of Copper it is considered contaminated. A copper contamination is extremely difficult to contain and clean. If a contaminated Test Wafer exposes a tool, then the tool may contaminate every subsequent wafer which is run. The copper contamination is then spread throughout the fab. Extreme caution is taken to prevent this from happening.
Doping type	- Adding impurities into the silicon changes the behavior of the silicon by varying the number of valence electrons. Changing this conductance varies the silicon's ability to act as a conductor or insulator.

Table 1: Test Wafer base characteristics

In addition to the base characteristics, Test Wafers are classified into four types as shown in Table 2.

Type	Description
R-GEN	A recycled or cleaned Test Wafer where chemical etching procedures are used to remove any deposition layers until only the bare silicon remains.
P-GEN	A R-GEN cleaning operation but with an additional polish step to ensure surface flatness
Reclaim	Along with a chemical etch procedure, a grind, lap, and polish operation is added to ensure that any surface imperfections are removed. Since a relatively large amount of material is removed, wafers can only be Reclaimed three times before they are too thin for safe use. At that point they are scrapped.
Prime	A virgin or new silicon wafer

Table 2: Test Wafer types

The four types outlined above are ranked in ascending cost. For the R-GEN, P-GEN, and Reclaim Test Wafers, the additional operations are the source of the cost increase. Prime Test Wafers are most expensive due to their virgin or unused status. Depending on the base silicon characteristics, a Prime Test Wafer may be an order of magnitude more expensive than the cheapest R-GEN Test Wafer. Different material structure differentiates Prime Test Wafers. Over time through the recycling and cleaning processes, their geometric characteristics change which affects route restriction compliance. This cost hierarchy is summarized in Figure 2.

R-GEN: Used wafer chemically etched to bare silicon

Reclaim: Chemically etched, lapped, ground, and polished wafer

P-GEN: R-GEN wafer with a polish operation

Prime: Virgin silicon wafer
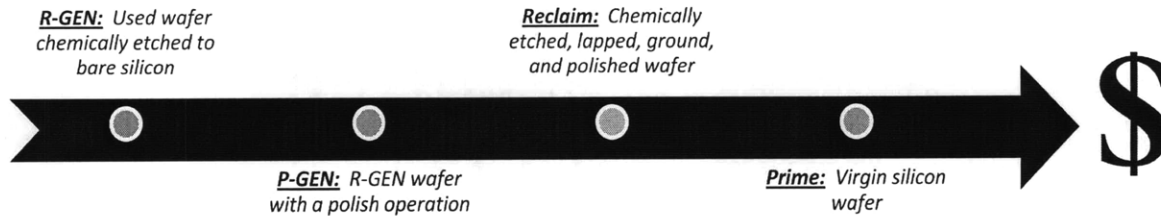
Figure 2: Test Wafer type and cost summary

2.2 Operation and Route Descriptions

Along with understating the details of what a Test Wafer is, it is critical to have a good comprehension of usage nomenclature and processes. Fab-17 manufacturing occurs in a class 10 (ISO equivalent 4) clean room.[7] In the production line, each tool and associated activity is distinguished by a particular operation and operation number. In order to fabricate a production wafer, a large number of operations are run in sequence each adding or subtracting material until a finished product is complete. Test Wafers may run any number of these operations; however, many Test Wafer specific operations also exist since Test Wafers are used for verification, cleaning, and/or validation activities separate from the production sequence.

A route is defined as a particular sequence of operations beginning with the starting operation of releasing Test Wafers into the fab. The subsequent operations are pre-process operations, operations which prepare the Test Wafer for whatever verification or validation purpose it was intended for. These pre-process operations may be additional cleaning, adding deposition layers, etc. Once the pre-process operations are complete, Test Wafers enter a "Test Wafer Ready" (TWR) operation. This is a holding operation where specific route inventory is held awaiting usage. Once needed, Test Wafers enter a "Test Wafer In Use" (TWI) operation. At this operation Test Wafers are used for their verification or validation purpose. Once this operation is completed Test Wafers are placed in exit operations. These are used to send the Test Wafers to be either recycled/cleaned or scrapped. The block diagram and example sequence in Figure 3 and Table 3 illustrates this process. Bar codes and scanners are used to "proc" the Test Wafers from one operation to the next.
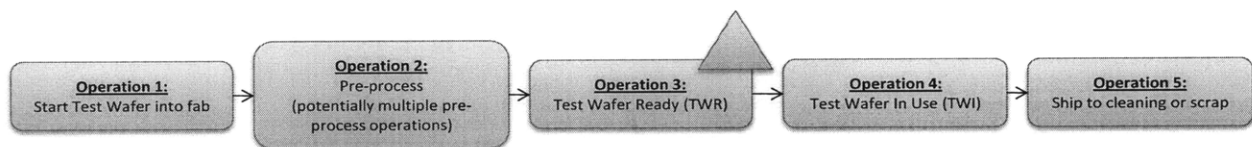
Figure 3: General route block diagram

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[7] Class 10 deals with the particle levels in a specific volume. By definition, a class 10 space has 10 particles greater than 0.5microns per cubic foot. As reference, normal living conditions are at class 1,000,000 (one million particles greater than 0.5microns per cubic foot)

Sequence	Operation Number	Operation Description
1	9001	Starts Test Wafer lot into the fab
2	9050	Pre-process step 1
3	7130	Pre-process step 2
4	3520	Pre-process step 3
5	8550	Test Wafer Ready (TWR)
6	8560	Test Wafer In Use (TWI)
7	1210	Send to external vendor for cleaning

Table 3: Example route sequence of operations[8]

To help quantify the complexity of the Test Wafer operations and routes, there are over 200 different routes. These are needed to ensure that all tools and activities needed to manufacture production wafers are behaving properly. Each of these routes has specific Test Wafer requirements, consumption rates, and lead times. Minimizing the variability of each route is a difficult challenge.

Lastly, in a 200mm diameter wafer facility, all wafers are transported in groups of 25 wafers. One group of wafers is called a lot. Lot boxes are designed to transport 25 wafers as well as interface with transportation equipment and tools. Test Wafer deliveries occur in multiples of 25 wafers for this reason. Only a full lot box can be "proc'ed" to the next operation.

2.3 Test Wafers and Fab-17

Fab-17 is a 200mm wafer facility; meaning all tools and machines are designed for the manufacturing of semi-conductors on a 200mm diameter silicon wafer. Over the past few years Fab-17 has pursued aggressive lean education programs to reduce cycle time, improve quality, and reduce operating costs. Since the majority of Intel's factories are 300mm facilities and the next generation of 450mm facilities is in design, the importance of reducing wafer costs is that much more critical. Fab-17 is at a precarious position in that the cost to upgrade the current facility is greater than building a new "greenfield" site.[9] Rumors of plant closure have help drive improvement projects and a culture focused on reducing its costs.

Figure 4 illustrates Test Wafer material flow at Fab-17. Each block will be elaborated in sections 2.3.1 through 2.3.6.

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[8] All operation numbers are false placeholders

[9] Greenfield: a new site on land previously undeveloped
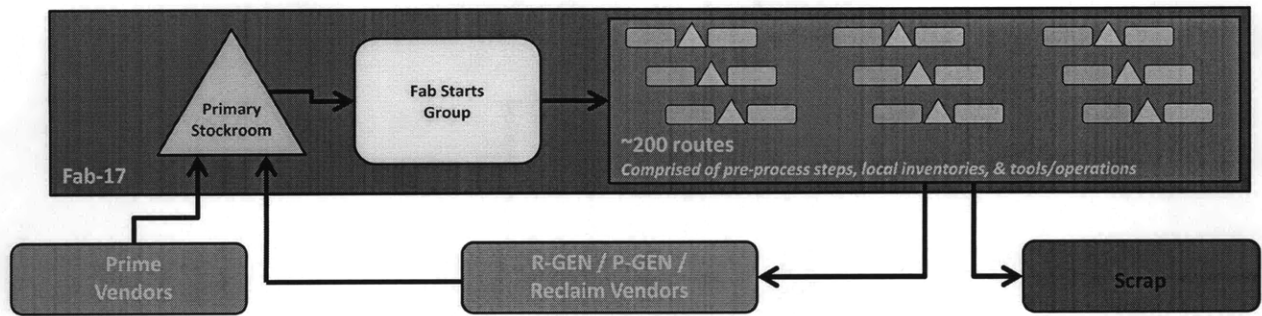
Figure 4: Test Wafer material flow block diagram

2.3.1 Primary Stockroom

Test Wafer inventory is received and stored in the Primary Stockroom outside of the manufacturing clean room. Each Test Wafer lot is individually bagged to minimize the risk of contamination and cleanliness issues. All four types of Test Wafers are held here. For Prime and Reclaim wafers, their quantities are controlled by a forecasting group within Intel. They are grouped together by their base characteristics. Any route which can accept those base characteristics can pull from that Test Wafer batch if inventory is available.

R-GEN and P-GEN Test Wafers are handled in one of two different approaches. The specific routes determine which approach they would prefer; this decision is primarily based upon risk to the tool.[10]

1. **Inventory held married to a particular route:** With this approach, all Test Wafers which leave the fab for R-GEN or P-GEN cleaning procedures are returned to their original route. The primary advantages and disadvantages of this system are summarized in Table 4.

Advantage	Disadvantage
- Control of Test Wafers exposing the route to potential contamination. The risk of a Test Wafer from a different route with contamination or with conflicting base characteristics is low. - The Test Wafers are effectively "owned" by the route. Measuring Test Wafer usage and costs are much easier.	- The consumption/usage variability is accommodated on each individual route. This drives a need for larger safety stock inventory levels

Table 4: Advantages/Disadvantages for inventory held married to a particular route

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[10] Oftentimes, risk is a perceived risk instead of actual risk. Although a culture of improvement is present many route owners are risk adverse and will take more conservative approaches to change

2. **Inventory from multiple routes are lumped together in a "bank"[11]:** With a bank system, Test Wafers returning from R-GEN and P-GEN cleaning procedures with identical base characteristics are lumped together. This single Test Wafer group is called a bank. Any route which can use Test Wafers with those base characteristics can pull from that particular bank. Routes which feed or supply Test Wafers to a bank are called "feeders." Routes which pull or eat Test Wafers from a bank are called "eaters." Not all banks have the same feeders and eaters. Some routes only feed to a bank while others only eat from a bank based upon route Test Wafer requirements. The primary advantages and disadvantages of this system are captured in Table 5.

Advantage	*Disadvantage*
- Individual route consumption/usage variability can be aggregated. This decreases the overall variability and allows for a total smaller safety stock inventory while maintaining the same Test Wafer availability.	- Verifying and ensuring that all Test Wafers in a bank meet the base characteristics is extremely important. Proper quality control and trust in the bank system is paramount.
- Decreases the overall Test Wafer costs for the routes feeding from the bank as additional cheaper Test Wafers are available.	- Directly tracing costs back to a particular route (cost accounting) is challenging

Table 5: Advantages/Disadvantages for inventory held in a bank system

Figure 5 shows a pictorial representation of the route and bank Test Wafer inventory management systems. The Primary Stockroom triangle represents a particular route or bank Test Wafer inventory group. The green box represents the fab with either a single or numerous routes (routes depicted with boxes/triangles for pre-process, TWR, and TWI steps). Further below, Figure 5 elaborates on these inventory management concepts.
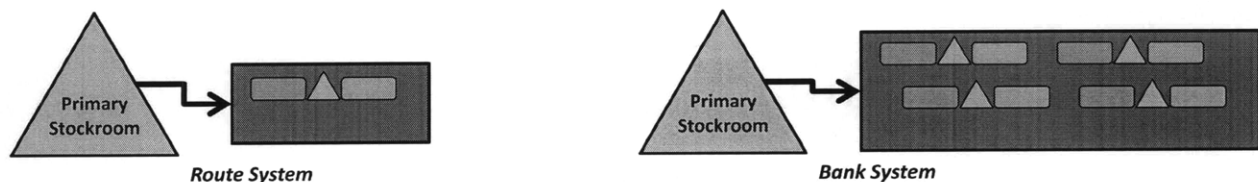
Figure 5: Fixed to route and bank inventory systems

2.3.2 Fab Starts Group (FSG)

The Fab Stars Group (FSG) is responsible for determining what, where, and when Test Wafers should be released into the fab. They are also responsible for physically moving Test Wafer lots from outside of the clean room and "PROC'ing" them into the first operation. It is at this point that previously unassigned Test Wafer lots become associated with a particular route. Lastly, FSG is also responsible for shipping used Test Wafers outside of the fab. In summary, FSG is the intermediary between the Primary Stockroom and the fab routes.

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[11] Note that all bank Test Wafers are of the R-GEN or P-GEN type

FSG is not only a group of technicians but also a location. The technicians complete their responsibilities in a special area which has an airlock allowing transfers to and from the clean room area. Various other tools and equipment are located in this area to help assist with initial Test Wafer checks and lot box identification.

Numerous computers linked to the Intel network have programs which provide information and complete calculations to assist FSG in making the Test Wafer starts decisions. Every shift, FSG must determine the following Test Wafer actions.

1. Which routes need Test Wafers
2. How many Test Wafers are needed
3. What type of Test Wafers should be used

Previously, a program based upon minimum quantity levels per route was used to trigger which routes and how many Test Wafers were needed. This program and the behaviors leading to problems will be discussed fully in section 2.5.2. Project 2 of this thesis addresses these issues.

The type of Test Wafer that should be used is determined by the route owner and is documented in a substitution table. The substitution table is formatted in ascending cost order; the cheapest Test Wafer type meeting the route's base characteristics is preferred first while the most expensive is prioritized last. Often the silicon substitution table order is R-GEN or P-GEN, Reclaim, and then Prime silicon Test Wafers but is ultimately determined by the route's requirements.

Table 6 contains an example silicon substitution preference for five example routes. The text in the "1rst Choice" through "5th Choice" columns corresponds to a particular Test Wafer type with the specified base characteristics. The "Route," Bank," and "Reclaim" text in the boxes correspond to example Test Wafer inventory of that particular characteristic.

	Silicon Substitution Preferences				
	1rst Choice	2nd	3rd	4rth	5th
Route-1	R-GEN Route-1	Reclaim-A	Reclaim-B	Prime-A	
Route-2	Bank-A	Reclaim-C	Prime-B	Prime-C	Prime-D
Route-3	P-GEN Route-3	Prime-A			
Route-4	Reclaim-A	Prime-A			
Route-5	Prime-B				

Table 6: Example silicon substitution table.

Once FSG has determined that a particular route needs Test Wafers, they then check for availability in the Stockroom. In theory, they should start the number of Test Wafer lots required using the cheapest Test Wafer type available.[12] This may be a combination of different Test Wafer types.

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[12] Actual practice will be discussed in section 2.5.2

2.3.3 Test Wafer routes

Once Test Wafer lots are released into the fab, many routes have pre-process operations used to prepare the Test Wafer to whatever state is necessary for their action operation (TWI). The number of pre-process steps and the type of activity at each operation determine the length of time needed for pre-processing before the Test Wafer is ready for use (TWR).

In order to buffer consumption spikes and accommodate this pre-process and delivery lead time, individual routes hold inventory at the TWR operation.[13] The quantity of Test Wafers held in this operation is different for each route. The size of inventory buffer is fixed by the route owner. When the quantity of Test Wafers drops below this value, the system signals FSG to start additional lots.[14]

To minimize the length of time needed to get to the TWR operation, the technicians often need to track down the location of their Test Wafers and communicate their importance to the pre-process tool technicians. Since Test Wafers are seen as non-value add and do not count in area metrics, many technicians will purposely choose to run production wafers instead. The pre-process length variability is large, at times up to a week before a Test Wafer lot arrives at TWR. This "human glue" or human intervention is necessary to keep the system running, albeit at high labor resource and complicated work expense.

Once needed, the technicians "Proc" Test Wafer lots from the TWR operation into TWI. During this operation Test Wafers are used for the route purpose. Once a full lot has been used, the Test Wafers are "Proc'ed" to the final shipping operation and delivered back to FSG. FSG then transfers the used lots out of the clean room where they are shipped to either R-GEN, P-GEN, or Reclaim cleaning operations or scrapped.

2.3.4 Prime and Reclaim Silicon Vendors

Prime silicon Test Wafers come from numerous vendors. With approximately fifteen different base characteristics (flatness, doping type, etc.), different vendors specialize in different types. Intel forecasting models determine how many of each should be available. Cross site sharing also occurs if a large anomalous consumption event occurs and the vendor lead time exceeds Fab-17's need.

Numerous Reclaim vendors also exist. When Fab-17 ships Test Wafers to be reclaimed, the ownership of the wafer transfers to the Reclaim vendor. In return, the Reclaim vendor give Fab-17 credits to be used to purchase clean Reclaimed Test Wafers. The credits received are less than the cost of a Reclaimed wafer; the delta cost being greater than that for a R-GEN or P-GEN Test Wafer. The amount and type of Reclaim Test Wafers available is also determined similarly to Prime Test Wafers by Intel forecasting models; however, this may also be constrained by availability of material within the Reclaim vendors.

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[13] Consumption spikes occur most frequently when a tool goes down unexpectedly. The number of Test Wafers needed to verify the tools health depends on the failure mechanism and type of tool.

[14] Minimum level trigger system discussed in section 2.5.2

2.3.5 R-GEN and P-GEN Silicon Vendors

After leaving Fab-17 the Test Wafers designated for either R-GEN or P-GEN cleaning operations are sent to an outside vendor. They are cleaned per a specific "recipe" that is designated for each route.[15] Through these recipes, the Test Wafers have three types of sorting as described in Table 7. These are mandated by the route owner depending on the risk of contamination.

Test Wafer Sorting Types	Description
Lot Integrity	Test Wafers are married to a particular lot box. All wafers that are shipped out to a R-GEN or P-GEN vendor must always be fixed to that particular lot. Often routes with Test Wafer lot integrity will have partially filled lot boxes since a scrapped wafer cannot be backfilled with another R-GEN or P-GEN wafer.
Route Integrity	Test Wafers are married to a specific route. Wafers can be transferred to any lot as long as that lot is fixed to that same route. This helps minimize the number of partial lots.
Bank Integrity	After route specific recipes return Test Wafers to their base layer, wafers from numerous routes can be batched together by their base characteristics. This minimizes the number of partial lots and helps improve the efficiency of a vendor's polish operation for P-GEN wafers.

Table 7: R-GEN and P-GEN sorting types

Figure 6 illustrates the Test Wafer lifecycle. Four different paths are depicted.

1. Lot Integrity: Test Wafers stay on the same route and in the same lot through all Fab-17 and External Vendor cleaning operations

2. Route Integrity: Test Wafers stay on the same route through all Fab-17 and External Vendor operations

3. Bank Integrity (with Bank Feeder and Eater routes the same): Test Wafers stay on the same bank but can be used on a set number of routes based upon their base characteristics. Test Wafers are differentiated by route once pre-process operations build from their base characteristics and are returned to a single bank after the route specific R-GEN cleaning operation returns them to their base silicon.

4. Bank Integrity (with different Bank Feeder and Eater routes): Test Wafers are treated the same as the third path however one or more routes feed the bank while eating from a Prime or Reclaim silicon type.

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[15] Since each Test Wafer from a particular route has different layers, processes, or characteristics after pre-process, TWR, and TWI operations, a specific "recipe" is needed to be followed to return the wafer to its bare state.
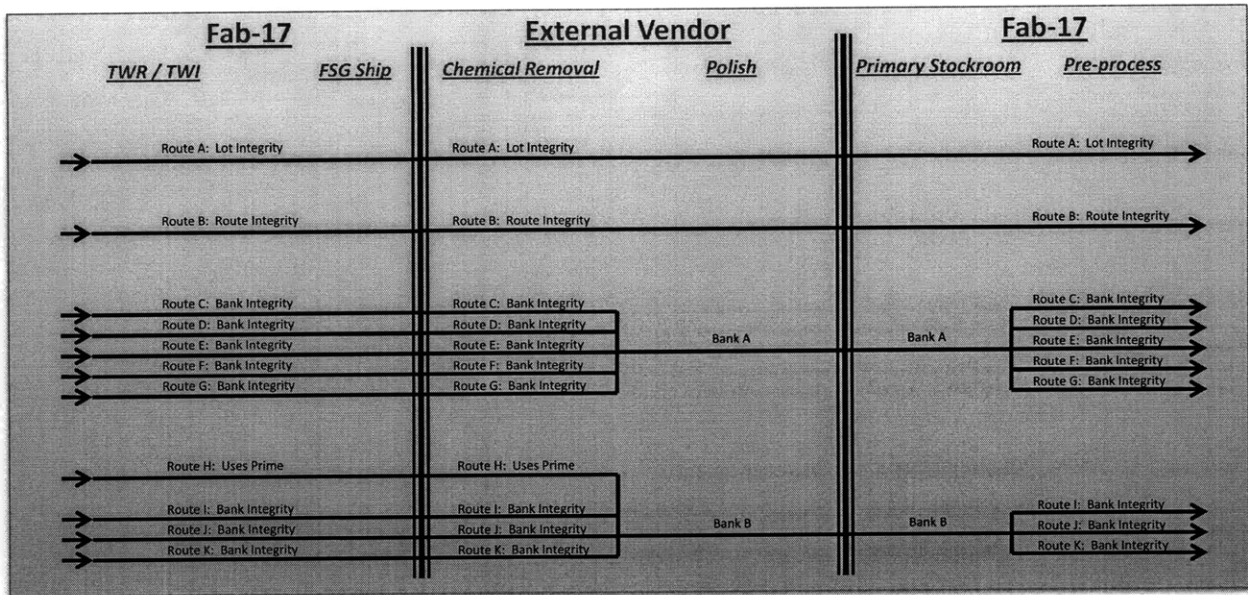
Figure 6: Test Wafer lifecycle

2.3.6 Scrap

Test Wafers are scrapped as soon as they no longer meet their base characteristics or are at risk to the tool or route. Rejection can either occur after a set number of cycles or if the characteristics are out of specification.

2.4 Fab-17 Organization

Since Test Wafers are necessary to guarantee quality production wafers, all organizational levels are interested in Test Wafer issues and decisions. The organizational structure of the fab is depicted in Figure 7. A brief job description and Test Wafer responsibilities are included in Table 8. In summary, under the Plant Manager two departments separate the majority of work responsibilities. On one side, the Manufacturing Department is accountable for all activities involving the tools and processes when they are available. The Process Department is responsible for ensuring minimal tool and processing downtime. The Test Wafer Engineer works across all hierarchical divisions in a separate group to ensure Test Wafers are present for the needs of all organizational levels.
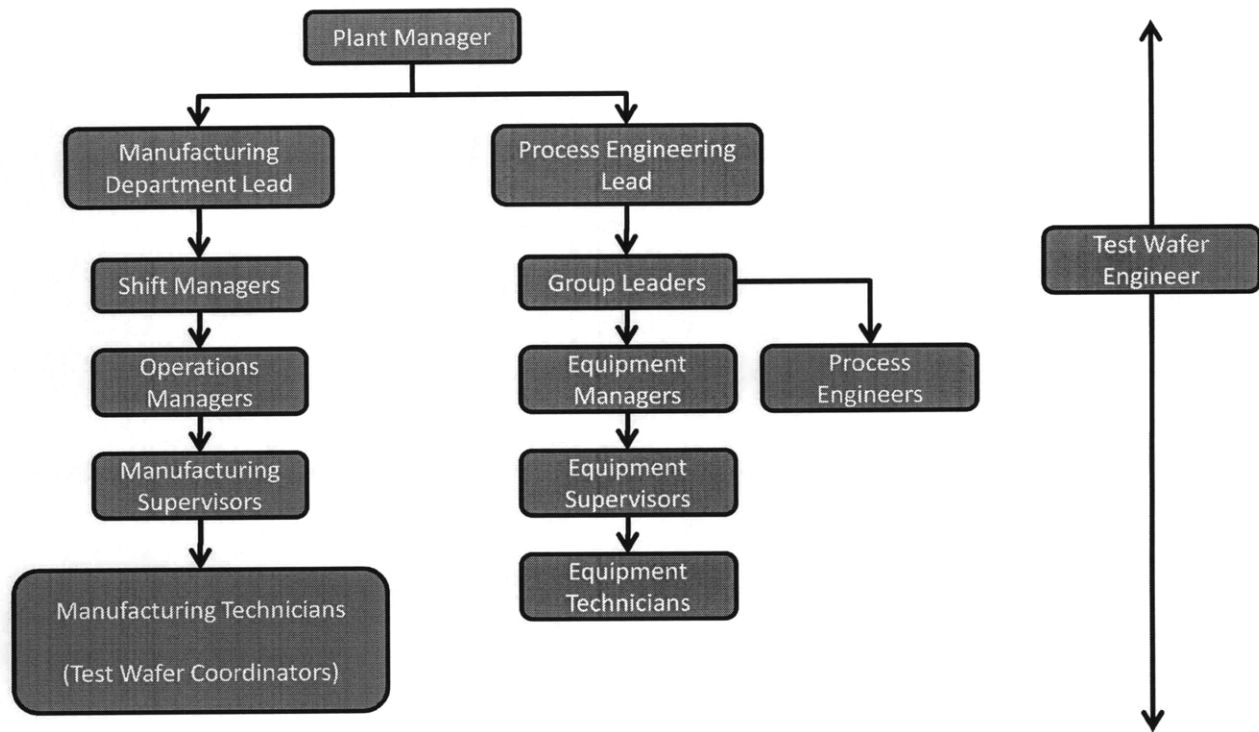
Figure 7: Fab-17 organization structure

Job Title	Job Description	Test Wafer Responsibilities
Plant and Department Leads	Responsible for all plant output, safety, and costs	Concerned only from the big picture perspective and impacts on plant level metrics
Shift and Operation Managers (SM, OM)	Responsible for shift and area manufacturing performance	First and second line of escalation if Test Wafers are not available when needed. Directly responsible for Test Wafer costs and monitor weekly consumption
Manufacturing Supervisors	Responsible for leading Manufacturing Technicians at each area. Liaison between the manufacturing processes and Operations Managers.	Monitor the Test Wafer inventory levels and escalate Emergency Start requests
Manufacturing Technicians / Test Wafer Coordinators	Front-line manufacturing workers. One Manufacturing Technicians per area per shift is the Test Wafer Coordinator and is responsible for all upkeep and maintenance of Test Wafer inventory for that area's routes.	Organize, maintain, escalate any test Wafer issues. Run Test Wafers on the tools and routes as needed.
Group Leaders and	Responsible for ensuring that all tools	First and second line of

Equipment Managers	and processes are available for use. Manage both technicians and engineers supporting this goal	escalation for any Test Wafer issues that can't be resolved quickly.
Equipment Supervisors and Technicians	Complete all maintenance activities including preventative maintenance and unscheduled downtime.	Run Test Wafers to support maintenance activities.
Process Engineers	Actual tool and process owners responsible for efficiency and cognizant of all activities.	Responsible for setting the old Test Wafer minimum level triggers and Test Wafer route requirements
Test Wafer Engineer	Responsible for all Test Wafer issues included quality, cost, supply, and improvement initiatives. Coordinates all work between the fab, external vendors, and stockroom.	The ultimate escalation point held accountable for Test Wafers being available, of the right quality and requirements, and at the correct location.

Table 8: Organization jobs and description

2.5 A "Broken" State

As discussed in sections 1.2.1 and 1.2.2, two problem areas were identified for this thesis project.[16] The next two sections will describe the background details behind these issues. The focus will be on the aspects which could be considered "broken:" those being elements which are non-standard, non-optimal, and preventing smooth working operations.

2.5.1 Managing Test Wafer Inventory

Due to unclear dividing lines between the relationship between Intel and the vendor who provides the stockroom and shipping/receiving service, there is no oversight or management of the R-GEN and P-GEN Test Wafer inventory levels in the stockroom and in the return/reclaim loops. From a contract perspective, the vendor is only responsible for shipping, receiving, and holding R-GEN and P-GEN inventory; there is very little knowledge of how that inventory is used and the cost impacts for non-optimal management. From Intel's perspective, they are currently only monitoring the quantities leaving the facility for cleaning operations and the lead time until that inventory is returned. This scenario leaves a void where inventory levels on certain routes and banks may be in great excess, whereas other routes and banks are starved. The assumption that the steady state condition contains balanced inventory levels is incorrect because of unforeseen tool issues. For example, if a tool is behaving out of specification, a far greater number of Test Wafers may be

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[16] Problem 1 summary: Non-optimal inventory distribution by Test Wafer base characteristics in the stockroom led to expensive stockout scenarios

Problem 2 summary: The process for determining what type, how many, and when Test Wafers were released into the fab was complicated, lacked standardization, required significant human intervention, and led to tool performance issues despite high operating costs.

started and consumed ultimately leading to excess inventory once the tool returns to nominal performance.[17]

Upon inspection of the inventory levels in the stockroom, numerous routes had enormous Test Wafer inventory. With no process to flag this excess or to redistribute it to starved routes or banks, inventory continued to build. The worst case route had built over 30 years of inventory; the volume of which corresponding to an entire wall from floor to ceiling, three lots deep filled with Test Wafers. The inventory for this route was held due to the route integrity constraints that prevent it from being distributed elsewhere.

The impact of this oversight was twofold. First, from a holding cost perspective, the volume needed to store these Test Wafers was encroaching into other occupied areas and would soon need to be addressed. Secondly, numerous routes and banks requiring identical base characteristics were starting Reclaim and Prime Test Wafers at a much greater cost. Enormous cost savings would be achieved by intelligently reallocated these excess Test Wafers to those areas that were starting the expensive Test Wafers; to do this, though, would require obtaining waivers to the route integrity complication.

2.5.2 Starting Test Wafers into the Fab

To help FSG determine how many and for which routes Test Wafers need to be started, a program was developed based upon minimum Test Wafer quantity levels. For each route, the route owner set a fixed minimum level based upon the wanted route safety stock level and the pre-processing time. The actual Test Wafer inventory level was determined by adding the total number of Test Wafer in pre-process, TWR, and TWI operations. Once a Test Wafer lot was started by FSG, the number of Test Wafers in that lot was added to the other Test Wafers in pre-process, TWR, and TWI. If the actual Test Wafer inventory was less than the minimum level, then the program would inform FSG the number of Test Wafer lots to start in order to have the actual amount equal to the minimum level.

Once FSG knew what routes and how many Test Wafer lots were needed, then FSG referenced the silicon substitution table and manually checked the available inventory in the stockroom to determine what type of Test Wafers would be used. In theory, a combination of different types would be started, starting with the cheapest type if the needed quantity was larger than the available inventory.

While this process seems straightforward, the actual process was far more complicated. With pressure to keep costs as low as possible, the route owners often would instruct FSG to only start the cheapest Test Wafers. The route owners might do this if they thought that cheap R-GEN or P-GEN Test Wafers were arriving from the external vendors in the next day or so; hence, they could allow there Test Wafer inventory to dip below the minimum level for a day or two until the next arrival of cheap wafers. However, many times a shipment of cheap Test Wafers would be an inadequate amount or not be on the usable horizon.[18] In this case, a stock out scenario might occur

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[17] To further explain: What a tool goes down, a large number of Test Wafer are required to get it back up and running within its control limits consistently. This burn-in or test time uses far more Test Wafers than normal operation. To meet this demand, Prim Test Wafers may be started if the cheap Test Wafer inventory is inadequate. These Prime wafers are now dedicated to that route in most cases.

[18] If an insufficient number of Test Wafers were available, this probably signals that the total amount of inventory in the system was less than needed. Since the cheap (R-GEN and P-GEN) Test Wafers are recycled and natural attrition slowly depletes Test Wafers

leading to an Emergency Start. Once an Emergency Start was flagged, whatever Test Wafer type that was available would be started, often at great cost and disruption to the line caused by expediting these lots through the pre-process steps and escalating need through multiple levels of supervision.

If the Test Wafer Coordinators (TWC's) or route owners were proactive, they might realize that their Test Wafer levels were low and communicate Test Wafer needs to FSG prior to a stock out. In this case, the human communication was used to express priority and need.

The necessity for human communication for Test Wafer need led to non-standard processes. With different FSG technicians on each shift, there was no consistency on what type, quantity, or number of Test Wafers would be started. Additionally, natural favorites developed where friendships influenced how Test Wafer start activities commenced. Non-standard activity and the human connections added to the job complexity. With hundreds of Test Wafer routes, numerous base characteristics and requirements, and inventory availability, FSG technicians needed to formulate over 2000 Test Wafer starts decisions each shift. This activity took hours of every day which could be used supporting other value added operations.

Lastly, with frequent near stock out situations, the route owners responded by increasing their minimum levels independent of consumption patterns or changes over time. As Figure 1 illustrated, if the routes were filled to their minimum levels, the expected time until a stock out would be unrealistically large for many routes, often corresponding to over two months of inventory.

Table 9 summarizes the problems with the previous starts process.

Problem	Description
Non-standard operations	Impossible to root cause analysis problems, no foundation for future improvement projects (stagnated at a certain level without ability to improve)
Complicated work	Time, communication, legacy and training issues
Non-optimal inventory levels	~50% of routes over two months of inventory, routes without cheap Test Wafers starved
Poor Test Wafer availability	Stock outs, Emergency Starts, Individual heroics needed to make the system work
High costs	Escalation, time, holding costs, expensive Test Wafer types being used
Inability to deduce root cause of problems	Same problems continue to occur without resolution

Table 9: Min level starts process problem summary

from a route, expensive new Test Wafers (Reclaim or Prime) need to be started at some point. By not starting any Test Wafers unless a cheap Test Wafer was available ultimately led to these inadequate inventory levels and drove triage operations once a stock out or near stock out scenario occurred. There was no method to measure or control the total Test Wafer inventory.

2.6 Direct Observation and Establishing the Current State

Along with understanding the principles and systems supporting Test Wafer usage, being able to measure and quantify a current state was also challenging. An old manufacturing proverb best illustrates this:

"You can't improve what you can't measure..."[19]

For both projects, measuring Test Wafer usage characteristics was a balanced juggle between what information was easily obtained, available through various levels of pain and suffering, and physically impossible to generate. The next three sub-sections elaborate on the key measurements and foundation calculations to support the thesis projects.

For all improvement projects and initiatives, a "Learning Card" was generated and submitted. These cards briefly outline the problem, hypothesis, and anticipated results. They are posted in the affected area in the fab with a list of approvers and the duration the test will be conducted. Over the period of testing the hypothesis, feedback can be written on the sheet as well as either a rejection or acceptance signature by the approver. At the conclusion of the test, if full approval has been received and quantifiable improvement results obtained, the new process will be accepted and established as the standard.

2.6.1 Measurement of Human Behaviors

One important success criteria for the thesis projects was developing simple and standardized work processes. Quantifying the improvements on how technicians complete their work was difficult in that easily obtained metrics and data did not always reflect the human behavior elements.

Prior to generating project hypothesis, the current process state was determined including the type, variability, and time technician work required. In particular, the role of the FSG technician and how he/she started Test Wafers into the fab was closely monitored. This was completed using Direct Observation methods including process and value stream mapping techniques, shadowing technicians, and researching the standard processes relative to the actual work conducted. Lastly, a survey and Learning Card focused on quantifying the number and type of communication channels required to maintain Test Wafer levels was completed. The following observations and description of how those observations were concluded is summarized below in Table 10.

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[19] Manufacturing proverb, author unknown

Current State Observation	How Observation Measured
2-3 hours a week used in verifying Test Wafer inventory levels (both within fab and at Stockroom)	Survey (www.surveymonkey.com) and communication/observation with floor technicians
2-3 hours a week needed to escalate Test Wafer issues if inventory levels were critically low	Learning Card implemented to measure the frequency and amount of time escalation occurred per shift
Test Wafer starts process was not standard across all shifts	Direct Observation
Work process was complicated; over four different systems needed to be referenced along with communication with the floor technicians in order to know Test Wafer type, quantity, and location to start	Shadowing technician, Direct Observation, numerous complaints and confusion across many disciplines

Table 10: Human element observation summary

2.6.2 Measurement of Test Wafer Consumption

The key measurement in laying the foundation for both hypotheses was Test Wafer consumption. Due to Intel's current systems and 200mm wafer facility architecture, measuring actual consumption rate is impossible.

Operations are only measured on a per lot basis. There are no tools to measure wafer usage on a per wafer count. "Proc'ing" from one operation to the next can only occur at the lot level. If less than 25 Test Wafers are needed, the established systems do not have any means to measure this consumption. It is possible that a route may consume five Test Wafers a day; however, the system will only be able to register single lot consumption after a five day period. In this example, the technician may have an empty lot box which they use as a receptacle for holding used Test Wafers until 25 Test Wafers have been used. At that point the lot box of consumed Test Wafers would be "proc'ed" to the next operation.

This approach is different from 300mm wafer facilities as they measure all operations on a per wafer basis. To switch to this system would require an entire architecture and paradigm shift.

Previously, Test Wafers consumption was measured by counting the number of lots started per route in a week period. Route consumption was inferred from the assumption that all routes started at FSG directly correlated to the number of Test Wafer lots used that week. However, this assumption over simplified the consumption patterns. Often instead of a steady and consistent Test Wafer input, large Test Wafers batched would be released. Instead of witnessing the actual consumption, a peaking cyclical pattern was observed.

To further elaborate, the measured time period for Test Wafer consumption/starts was from Sunday to Sunday. If Test Wafers were started on Saturday night, they would appear as consumed Test Wafers for that week where in actuality they would not be used at the TWI operation until the following week. With additional Test Wafers in the system, the route would need to start a smaller amount of additional Test Wafer for the subsequent week. This pattern of a large number of Test Wafer starts followed by a period of decreased starts led to this cyclical pattern and promoted false

understanding of the actual Test Wafer consumption rate. In addition, the lack of standardization of the Test Wafer starts process also exacerbated this issue as Test Wafers were rarely started when first requested. Instead of frequent but relatively small quantity Test Wafer starts, instead the Test Wafer starts behavior waited until the last minute and then expedited large numbers of Test Wafer lots to the starved routes. The lack of standardization not only affected the consumption understanding but also helped propagate rush operations and deviations from smooth Test Wafer flow.

The solid white line in Figure 8 shows an example of the actual number of Test Wafer lots started over a 13 week period. The cyclical pattern is present making it difficult to understand the actual consumption rate as well as any consumption trends.[20]

In order to buffer these incorrectly interpreted Test Wafer consumption peaks and valleys, an Exponentially Weighted Moving Average (EWMA) analysis was completed on a per route basis. The EMWA has the benefit of weighting either the most recent or historical data greater through the use of a smoothing parameter, lambda ("λ"). The greater the lambda, the most recent data points become more heavily weighted leading to a quicker response in the EWMA. A lower lambda has the opposite effect; the historical data is more heavily weighted with the EWMA showing a much slower or filtered response.

$$EMWA_i = \lambda * Consumption_i + (1 - \lambda) * Consumption_{i-1}$$

Equation 1: Exponentially Weighted Moving Average

Figure 8 illustrates three different EWMA's with different lambda values.
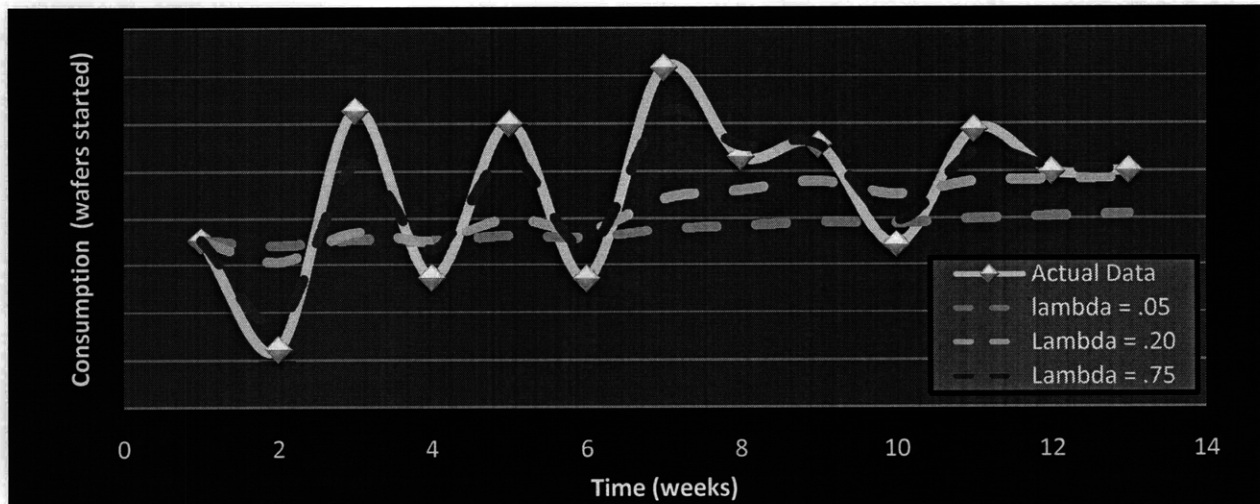
Figure 8: Example route Test Wafer consumption EWMA

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[20] Consumption may either trend up or down depending on the route. If numerous tools had quality issues, then a larger number of Test Wafers would be run to test, verify, or attempt to return the tool to steady state. A problem may take weeks to resolve. Consequently, numerous projects looking to reduce Test Wafer consumption by decreasing the number of Test Wafers used on maintenance or monitoring activities was also occurring.

With lambda set at a high value (λ=0.75), the response is very rapid tracking each peak and valley. If lambda was set at 1.0, the EWMA would equal the actual data. With lambda set at a low value (λ=0.05), the response is very slow with very little change from the first data point. If lambda was set at 0, the EMWA would be a flat, horizontal line equaling the first data point value.

For most uses, a lambda value of 0.10-0.25 is used.[21] For Test Wafer consumption purposes at Fab-17, a lambda value of 0.15-0.20 was used. Through comparisons of actual route consumption rates generated by direct observation and communication with floor technicians, this value produced EMWA results which best matched the previously immeasurable consumption rates. In all cases a 13 week period was used to initiate the EWMA. Approximately three months of data points adequately captured consumption trends as well as buffering out discrepant weeks.[22]

It is also important to note that many routes do have variability in their weekly consumption rates. This variability is often propelled by unplanned tool downtime. Safety stock inventory levels set for each route buffer this variability. The EMWA is used as an average consumption rate baseline.

2.6.3 Measurement of Test Wafer Costs and Performance

Additional Test Wafer measurements were needed to capture current state and future improvements. Many of these aspects already had a method for extracting the data, albeit, for purposes other than the thesis projects described here. Table 11 encapsulates these elements.

Measurement	Source	Notes
In-Fab Inventory Levels	Data reports supporting the old Test Wafer starts program count the number of Test Wafers in pre-process/TWR/TWI by summing the quantity by operation number. The total Test Wafer inventory in the fab is displayed in a separate web-based application which shows the quantity of Test Wafers at each operation per route.	The inventory counts are not always accurate due to the following two reasons. 1. Ghost Lots: Lots which the system thinks are there but are not physically present. This could occur when a lot is removed but not "proc'ed" out of an operation 2. Used Lots: Lots which are used but not "proc'ed" to the next operation. The system thinks a lot is ready and available when it should actually be at the next operation
Stockroom Inventory	The service company in the Stockroom	The accuracy of this systems

[21] Montgomery, Douglas C. (2005). *Introduction to Statistical Quality Control.* John Wiley & Sons, Inc.

[22] A discrepant week is defined as an outlier; a week which either has increased or decreased Test Wafer starts which do not reflect on actual consumption rates. This may occur if a single tool breaks for a short time period, a onetime test, or Test Wafers started right before the weekly count.

Levels	keeps a record of the physical Test Wafer inventory available on-hand. As Test Wafer are received or shipped, the inventory list is manually updated	assumes that the individuals counting and recording the Test Wafer lots complete this activity accurately. Unfortunately, the number of lots are miscounted or recorded in an incorrect Test Wafer part number.
Test Wafer Availability	All Emergency Starts are generated through a website interface. A historical record of when, who, and approval is provided.	The majority of near stock out situations are handled through communication and human heroics prior to the Emergency Start. Since an E-Start requires escalation, often it is faster for technicians to talk directly with FSG and express their Test Wafer needs. To measure this aspect, a clipboard was posted in FSG with the number/type of communications recorded.
Cost	All Test Wafer costs are reported by multiplying the cost per Test Wafer type by the number of Test Wafers consumed. The Finance Department determines the cost per wafer type by a weighted average of all the Test Wafer vendors.	Costs are reported on a weekly basis. As mentioned in the previous section, the actual consumption per week is assumed from the number of Test Wafer starts.
Ability for root cause analysis	Numerous Test Wafer problems have existed for many years. For example, a particular Test Wafer route always has insufficient inventory despite attempts to correct this problem. Work-around "band-aid" solutions have been developed to address such issues.	On many occasions, the cause of the issues was unknown until an improved Test Wafer starts system was implemented. Solved issues were documented in a "lessons learned" presentation format.
Foundations for future improvement projects	With so many improvement opportunities, multiple Test Wafer projects are currently ongoing. Many of these projects are at the subsystem level. Without a robust system-level standard operating procedure, the current and improved state would be impossible to determine or confidently conclude.	Linking the sub-system improvement projects to the measurements and standard process from the two thesis projects enables the incremental savings measurement from each additional improvement.

Table 11: Measurement of Test Wafer performance summary table

3 Literature Review

Prior to launching the thesis projects, an extensive literature review was completed with the purpose of understanding existing Test Wafer and inventory management practices. The review search was separated into four sections each offering a different perspective on these thesis projects. First, industry publications, journals, and public Intel documents were researched providing general inventory and semi-conductor management processes. This literature helped build a framework of prior issues and solutions which were then transferred to Fab-17 specific problems. Next, numerous textbooks and theory or model based sources were investigated. These provided more detailed information into calculations and the theory behind the previous work. Lastly, previous LFM theses were researched to leverage any potential thesis transfers from years prior.

Only the most influential literature sources are discussed here. A full list of sources is provided in the bibliography at the end of this thesis. A more detailed summary of each literature source reviewed can be found in Appendix J.

3.1 Journals and Industry Papers

The majority of relevant industry papers are from IEEE.[23] All develop improved methods for managing and optimizing Test Wafer usage in a semiconductor manufacturing facility. Ozalekan et. al (2006) elaborates on a theory to re-use (or recycle) Test Wafers based upon requirement characteristics and base preferences. This is very similar to the current processes employed by Fab-17 and provided insight into their rationale and original basis. Chuen-Shiun Liou, Lin, Tu, and Chang (2005) developed a forecast and capacity planning model for Test Wafer usage in 2005 with foundations in the number of operations, constraints, and consumption variability. Although different from the EMWA approach taken in the thesis projects, it provided insights into the various factors to consider.

In terms of processes to manage Test Wafer operations, Ferland and Labonte (2004) elaborated on an automation system which controlled Test Wafer release through improved standardization, improved visual systems, and increased automated flow controls. Developed in 2004, significant software improvements have since updated the Fab-17 automation systems from both test and production wafers. In 2003 Chen and Lee published a paper using a pull methodology for managing Test Wafer inventory levels and the downgrading of Test Wafer types. Savings include WIP reduction, increased recycle usage, and reduced downtime related to waiting for wafers.

3.2 Public Intel Specific Documentations

Frank Gleeson and Cathal Smith (2008) in Fab-24 completed a very similar development and implementation of a Test Wafer control system based upon a Days of Inventory metric. Many of these principles were the building blocks for the DOI Scheduler program developed for this thesis. Major differences existed in the consumption and forecast data as Fab-24 is an automated 300mm facility with inherent improved measurement capabilities. Additionally, the decision tree using this improved consumption data is also slightly different. This example provides another independent source showing the benefits of a DOI approach instead of a fixed minimum level system as seen previously at Fab-17.

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[23] The IEEE name was originally an acronym for the Institute of Electrical and Electronics Engineers, Inc. Today, the organization's scope of interest has expanded into so many related fields, that it is simply referred to by the letters.

Mukesh Gogna, a previous Fab-17 intern, developed the algorithm for an improved Test Wafer business application and interface incorporating usage and visualization tools. This document describes this project and gives good insight into the available information and how it can be used to improve the current state. Budgetary cuts prevented any of this work from actually being implemented.

3.3 Academic and Other Publications

Beishel and Smith (1991) co-authored a document detailing the hierarchy of measurements and metrics linking front line operations to the plant level performance indicators. This is helpful reference as a basis for understanding and recommending additional measurements for understanding Fab-17 health.

MIT's Lean Aerospace Initiative (in particular Deborah Nightingale, 2002) wrote a book looking at lean initiatives at an enterprise level. Although the examples were based in the aerospace industry, the implementation challenges and problem solving approach is the same for semi-conductor fabrication obstacles.

Montgomery (2005) wrote a textbook on statistical quality control. This reference has a detailed section on the Exponentially Weighted Moving Average (EMWA) and was used as a reference when developing the forecasting approach in the DOI Scheduler program. May and Spanos (2006) co-authored a book focused on the fundamentals of semiconductor manufacturing and process control. Specifically, the sections on process modeling and control charts were useful in understanding the metrics and measurements used by Fab-17.

3.4 LFM Theses

Numerous LFM thesis discuss inventory management, lean development, and pull system operations. The following two are best suited for Test Wafer issues. First, Jonathon Howe (2001) discusses Test Wafer risk qualification focusing on data driven processes. In this, he develops three different tools to minimize the risk of Test Wafers not being available or ready for use specifically in new manufacturing facilities within the Intel Corporation. This thesis provided background information on Test Wafer capacity forecasting and background information on developing semiconductor manufacturing sites. Second, Gary Tarpinian (1999) investigated cost reduction approaches within Intel. Test Wafers are specifically identified as a cost group with large saving potentials. A database of information was developed to help identify and assist reduction efforts.

4 Research Analysis: Project 1 – Reallocating excess inventory

4.1 Overview: Excess and Inadequate Inventory Levels

Once I identified that there was over 30 years[24] of Test Wafer inventory on a particular route in the Stockroom, I developed a process to identify other route and bank locations that might use this inventory; we then developed a model to determine how much Test Wafer inventory to reallocate. The challenges of completing this reallocation were twofold.

1. Building an optimization program which would determine where and how much Test Wafer inventory should be reallocated. The optimization program must adhere to the stringent Test Wafer base characteristics and contamination concern constraints while maximizing the realized cost savings[25]
2. Developing and implementing a process to complete the optimization program's recommendations

Section 4.2 discusses the specific background data that was needed to assess the problem and future states. Sections 4.3 and 4.4 develop the solutions to the two challenges outlined above.

4.2 Optimization Model Background Data

Test Wafer background data and measurements were discussed in detail in Chapter 2. Specifically for the relocation of excess stockroom inventory project, the following data was needed and summarized in Table 12.

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[24] This value being enormously atypical; however, no action or process was in place to identify such a discrepancy.

[25] Realized Cost Savings: the difference between the amount of money otherwise needed to start Prime Test Wafers and the cost of converting the excess Test Wafer inventory to be usable in the specified routes and banks.

Background Data and Measurements	Description
Test Wafer base characteristic requirements and constraints	Needed to determine where the excess inventory could go. Requirements and constraints assembled in a Silicon Substitution document approved by the route owners
Consumption and scrap rates	Used to forecast the time until a Test Wafer lot would be rejected and a new Test Wafer lot would be started. This rate multiplied by the inventory quantity produced the time until all inventory was used.
Costs (Prime and Reclaim wafers, R-GEN/P-GEN cleaning, and reallocation/inspection)	To optimize inventory allocation decisions around monetary savings, costs for each decision were needed. Prime/Reclaim Test Wafer costs and R-GEN/P-GEN cleaning costs were provided by the Finance Department. Inspection and reallocation costs were derived assuming a base hourly rate for an Intel employee and an estimated time needed to complete the associated task.

Table 12: Project 1 background data and measurements

4.3 Optimization Model Algorithm

The optimization model was built in Excel, 2007 using the Solver package. Being a linear optimization problem of relatively small size this architecture easily supported the analysis while providing simple data transfer and manipulation from existing Intel sources. The program was built on the following criteria. The model interface can be seen in Appendix A with the decision variables highlighted in blue. The constraints are also shown. The results of this model will be discussed in detail in Section 6.1.[26]

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[26] Due to intellectual property and security reasons, the actual optimization model display cannot be shown. The program algorithm developed above describes each action and should be adequate to convey the complexity and importance of this project.

Objective Statement:

Minimize the total cost of meeting the one year forecasted Test Wafer starts allowing excess Test Wafer inventory to be reallocated to accepting routes and banks

- ➤ *In other words, maximize the realized costs savings associated with using excess inventory versus starting Prime silicon*

Given:

1. *Consumption and scrap forecasts*
   - ➤ *Determined from the EWMA consumption rates and the known number of usage cycles before a particular lot was scrapped*
2. *Test Wafer costs*
   - ➤ *Prime wafers*
   - ➤ *Reclaim wafers*
3. *Base characteristics and constraints*
   - ➤ *Each route and bank had a specific set of base characteristics. Since the route with excess inventory was on a route integrity specification, the excess Test Wafers stayed married to that particular route. Cross referencing the route requirements against other routes/banks and obtaining acceptance by the route owners allowed the transfer of this inventory to different locations*
   - ➤ *A total of 11 routes and 2 banks were identified that would accept the excess inventory.*

Constraints:

1. *Time period to optimize the decisions over*
   - ➤ *Based upon the optimization time period, the forecasted amount of Test Wafers used per route/bank changes. As the needed amount of Test Wafers changes, the output also changes.*
   - ➤ *Model was run for the forecasted Test Wafer usage in one year.*
2. *Reallocation costs*
   - ➤ *Before reallocation to the 11 routes and 2 banks, the excess inventory needed to be either cleaned or verified to its base characteristic requirements. This was either a R-GEN or P-GEN cleaning operation or an inspection step completed at Intel based upon a labor rate and time needed to conduct the inspection.*
3. *Only full lots and single lot increments could be reallocated*
   - ➤ *Whole number constraint*
4. *The total number of reallocated lots could not exceed the available lots*
   - ➤ *The number of lots to be reallocated were ~250*
   - ➤ *Any additional lots needed were started with either Prime or Reclaim Test Wafers depending on the route or bank preference.*
5. *The total number of Test Wafer lots needed for the time period must equal the sum of all Test Wafer types to be started*

Decision Variables:

1. *The number and type of Test Wafers to start on each route*

4.4 Organizational Issues

Once the recommendations from the optimization program were verified, the next challenge of developing and implementing a process to reallocate the excess inventory needed to occur. Although seemingly straightforward, numerous organizational and logistical issues needed to be addressed since Test Wafer inventory reallocation has never been completed in the primary stockroom before.

The approval from the route owners to break and accept Test Wafer lots previously fixed as route integrity was the first obstacle. While in theory each Test Wafer should meet all quality specifications associated with its base characteristics and contamination requirements, many route owners demanded an additional verification check before accepting route integrity Test Wafers from a different route into their route. Due to labor resource constraints and costs, the optimal approach to address this issue was to send the questionable Test Wafer lots back to R-GEN and P-GEN cleaning operations. This ensured that any latent particles or layers were removed. This same approach was taken for all lots held in the stockroom for greater than three months.

The route owner of the excess Test Wafers also needed to be assured that this program would not remove his entire safety stock inventory thus leading him to start more expensive Test Wafer types. Looking at this particular route and consumption/scrap rates with the owner and incorporating him into the decision process allowed him to realize the immense Test Wafer inventory excess and associated savings to the fab.

Developing and implementing a process was the final hurdle. A meeting was held congregating representatives from FSG, the stockroom, route owners, R-GEN/P-GEN vendors, and interested managers; the outcome was the establishment of a process and the delegation of work responsibilities to the various parties. This meeting also provided a good opportunity to unify understanding of the issue and the enormous savings for the fab. All flagged lots were reallocated in a period of three weeks.

5 Research Analysis: Project 2 – Determining supply decisions from a DOI metric

5.1 Overview: Using a DOI metric for pulling Test Wafer starts

Project 2 involved developing an improved program to optimally determine what Test Wafer type, how many, and for what routes FSG needed to start. Instead of the highly labor intensive fixed minimum quantity level approach discussed in Section 2.5.2, we incorporated additional consumption and available inventory measurements to determine the trigger point based on a Days of Inventory (DOI) metric. The major differences/improvements between the new DOI system versus the minimum level system are threefold.

1. Automatically and dynamically adjusts trigger levels based upon consumption changes
2. Trigger metric incorporates communication connections previously requiring "human glue"
3. Optimizes starts based on cost while maintaining or improving Test Wafer availability

The DOI Scheduler program was written on a Microsoft Excel, 2007 Excel application.[27] First, Visual Basic macros identified input and populated input data into numerous hidden tabs. This data included current Test Wafer inventory levels both in the fab and in the stockroom as well as the number of Test Wafers started over the last 13 weeks. Next, the Days of Inventory for each route was calculated based upon the available inventory and the current consumption rate. The short term forecast was assumed to equal the EWMA for each route. Once the current DOI for each route was known, this was compared to a set of DOI triggers used to determine when Test Wafers were needed. Once the DOI for a route dropped below these trigger levels, the program used "intelligent" decision tree logic to determine the final action needed based upon the available inventory in the stockroom and the time until a stock out scenario. Numerous calculation tabs completed this logic analysis automatically each time the program was opened. The input data sources also re-generated at set intervals. All calculation and input tabs were hidden to maximize user ease while a total of three tabs showed the final output actions, summary of the decisions, and Bank inventory levels. Figure 9 illustrates a block diagram for the DOI Scheduler program. Later in this chapter, Figure 10 will more fully develop each of the inputs, outputs, and calculation sections.

Calculate DOI on a per route basis with Consumption rate and in loop test wafer inventory

$$Days\ of\ Inventory = \frac{(TWR + TWI + Preprocess\ Inventory)}{Consumption\ Rate}$$

Compare to DOI Triggers and Start values to determine needed actions

Compare actions to available inventory levels

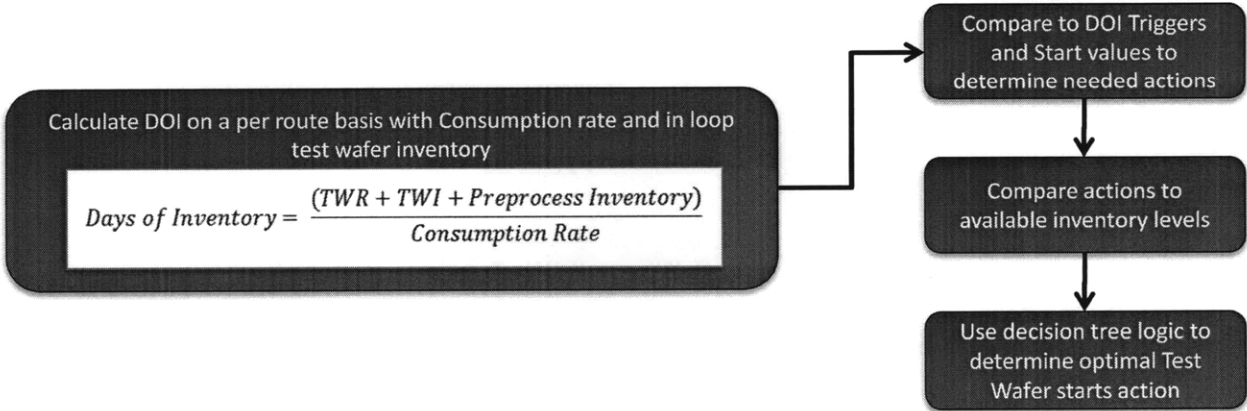Use decision tree logic to determine optimal Test Wafer starts action

Figure 9: DOI Scheduler program block diagram overview

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[27] Appendix B shows a list of most commonly used Excel formulas used in the DOI Scheduler program

The details of the needed input data are discussed in Section 5.2. A detailed description on the program theory, algorithm, logic, and output are expanded in Section 5.3.

Concurrent with the program development was the establishment and execution of a standard operating process and education plan. A strategy to ensure legacy after the conclusion of the internship was also equally important. Section 5.4 explains the approaches to address these challenges.

5.2 DOI Scheduler Program Inputs

The model inputs can be separated into two categories. The first being a set of data describing current and historical state of the fab generated automatically from existing reports. The second category being the input variables to control the response and actions of the program with respect to the logic and calculations built from the first data category. Modifications of the input variables directly influence what actions the program takes to ensure optimal Test Wafer starts decisions; many of these input variables are adjusted on a per route basis to individually cater the response to different pre-process times, consumption variability, and type of usage.

The initial data set used by the DOI Scheduler program and their purpose is summarized in Table 13.

Input Data	*Purpose in the DOI Scheduler Program*
Available inventory (Pre-process, TWI, TWR) per route	Counts all Test Wafer inventory in pre-process, TWR, and TWI. The length of time needed to get to the TWI operation is compensated in the DOI Ideal and Critical triggers discussed in Section 5.3.1. A more robust approach would be to only count Test Wafers in the ready operation; however, limitations in both the data gathering and programming architecture prevented this approach.
Weekly Test Wafer start quantity (over the past 13 weeks)[28]	The quantity of Test Wafers started into the fab summed in weekly increments. This data is used to calculate the EWMA consumption forecast.
Test Wafer minimum level triggers	The minimum level triggers are those used on the previous system. For routes without Test Wafer starts in the past 13 weeks, no information is available to determine a consumption forecast. For these routes the old minimum system is used. This will be discussed further in Section 5.3.2.
Silicon substitution table	The silicon substitution table is used in conjunction with the available Test Wafer inventory to determine the preferential order of Test Wafer types to be

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[28] This 13 week start quantity would shift or index as time passed. It would always show the most recent past 13 weeks.

	started.
Available Test Wafer stockroom inventory	In determining the type of Test Wafer to use, the available inventory needs to be known. Depending on the route status compared to the Days of Inventory triggers determines how many Test Wafers to start.

Table 13: DOI Scheduler input data

The input variables and their impacts on the DOI Scheduler program's output are discussed in Table 14. The DOI Scheduler owner has the ability to modify these values to cater the DOI Scheduler response to optimally perform for each route's needs.[29]

Input Variable	*Impact on the DOI Scheduler Program*
Lambda (λ) – set globally	The lambda value determines how heavily either the most current Test Wafer starts should be weighed in calculating the EWMA consumption forecast. The effects of changing lambda are elaborated upon in Section 2.6.2.
Ideal and Critical DOI trigger levels per route	The DOI triggers are used to flag when the time until Test Wafer stock out is below a set warning value. Each route has a different trigger level to accommodate for route uniqueness and individuality.
Ideal and Critical DOI fill levels per route	Once below the warning trigger levels, the DOI Scheduler system attempts to fill to a set level. The available inventory and time until stock out determine how many Test Wafers and of what type are used.
Route "Active" or "In-active" toggle	This toggle decides whether a route is included in the DOI Scheduler program output or not. A route may no longer be used or for some reason not want to be included in the output.

Table 14: DOI Scheduler input variables

5.3 DOI Scheduler Model Discussion

In order to fully understand the DOI Scheduler output and the reasons for its improvements over the previous system, the following subsections are used to explain how the DOI Scheduler program

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[29] The DOI Scheduler program is read-only password protected. Only a few super-users know the password and have the ability to change the input variables. An archived copy of the DOI Scheduler is kept in a separate folder. Additionally, a tab containing revisions updates serves as configuration control.

works. The model theory is first discussed with the detailed algorithm, logic, and output results following.

5.3.1 DOI Trigger Methodology

The methodology behind the DOI Scheduler program can best be explained by examining the Days of Inventory of an example route over a period of time. The state of a particular route in terms of Days of Inventory can be characterized into three different states, the DOI Scheduler program responding with different actions in each case. Ideal and Critical Days of Inventory triggers are set with different decision logic corresponding to each. Figure 10 illustrates the Days of Inventory associated with an example route to help visualize these states.
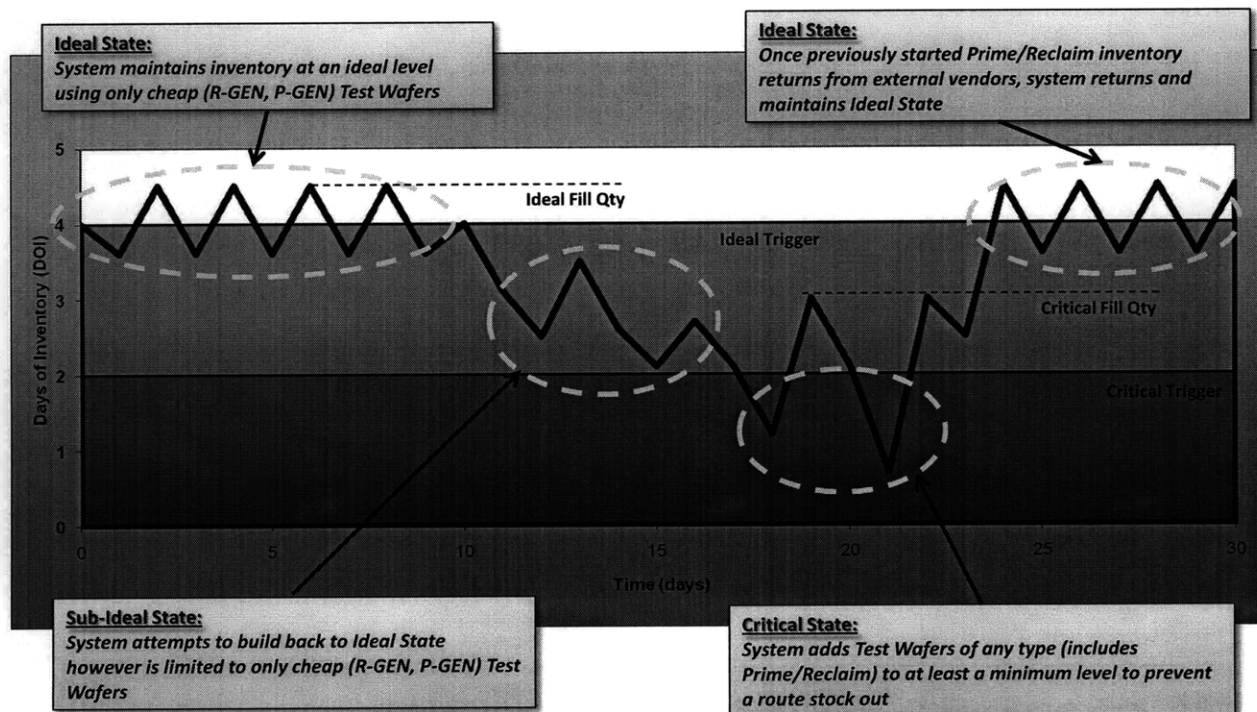
Figure 10: Example route DOI trigger methodology description

Ideal State:

The Ideal State is characterized by an Ideal Trigger and an Ideal Fill Quantity. The DOI Scheduler attempts to maintain the inventory of a particular route at the Ideal State; however, it is limited by only being able to start cheap R-GEN or P-GEN Test Wafer inventory. Assuming adequate R-GEN or P-GEN Test Wafer inventory is available in the stockroom, once the Days of Inventory metric for a route drops below the Ideal Trigger, the DOI Scheduler informs FSG to start a certain number of Test Wafer lots up to the Ideal Fill Quantity level. The Ideal Fill Quantity level is expressed in the Days of Inventory metric but is converted into an actual Test Wafer lot quantity by multiplying the Ideal Fill Quantity level by the EWMA forecasted consumption rate. Over time

with the preferred Test Wafer type available, the DOI Scheduler program will maintain the Ideal Days of Inventory for a particular route in a saw-tooth consumption and fill pattern.[30]

We note that since the "y" axis in Figure 10 displays the Days of Inventory, any consumption changes in a route will not change the horizontal slope of this line. If instead of Days of Inventory the corresponding Test Wafer quantity was used, the Ideal Trigger line would not be flat and instead either slope upwards or downwards depending on changes in the consumption forecast. This change illustrates one advantage of this system. The amount of Test Wafer inventory held at a route should change to reflect consumption changes. If the consumption rate increases, then an increase of Test Wafer inventory needs to be held to ensure the same availability. Conversely, if route consumption decreases, then less Test Wafer inventory is needed. The minimum level triggers from the previous system did not have this dynamic update capability which led to excess Test Wafer inventory in the fab as overall Test Wafer consumption trends downward due to various lean improvement projects.

Sub-Ideal State:

Over time, the amount of available R-GEN and P-GEN Test Wafer inventory in the stockroom will diminish due to natural scrap and attrition. Since the Ideal State is only starting cheap recycled Test Wafers, no new Test Wafers are being added to the overall inventory level. The Sub-Ideal state is characterized when the Days of Inventory at a particular route is less than the Ideal State but above the Critical State. The DOI Scheduler system is attempting to build the inventory levels back to the Ideal Fill Quantity level, however, does not have enough R-GEN or P-GEN Test Wafers to fulfill this task. As the Days of Inventory continues to drop, any Test Wafers which return from the R-GEN/P-GEN cleaning operations will be started. As consumption of Test Wafers in the fab continues with no incoming cheap R-GEN or P-GEN wafers, the state of the route approaches the Critical State.

It is important to note that not starting more expensive Test Wafers in the Sub-Ideal State is another advantage of the DOI Scheduler system. Since the necessity of Test Wafers is incorporated into the trigger metric, the system automatically knows when the route is at a critical level opposed to sub-ideal. With a significant turnaround time with the R-GEN and P-GEN vendors, often times cheap Test Wafers arrive shortly after first triggered. By waiting before starting expensive Test Wafer types, the DOI Scheduler ensures that the most cost effective decisions are made without jeopardizing the availability of Test Wafers on the route.

Critical State:

Once the Days of Inventory for a route drops below the Critical Trigger, this flags the DOI Scheduler program that Test Wafers are needed immediately on the route. Cost issues are no longer a concern since the cost of a Test Wafer stock out far exceeds that of starting more expensive Test Wafer types.[31] Once below the Critical Trigger, Test Wafers are started immediately up to the Critical Fill Quantity level. The Critical Fill Quantity level is purposely held below the Ideal Trigger level. Again, due to the lead time needed by the R-GEN and P-Gen vendors, incoming Test Wafers may be arriving in the near future. By starting a small amount of Test Wafers the DOI Scheduler

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[30] Cheap Test Wafers meeting the required base characteristics and requirements are always preferred over more expensive Reclaim or Prime silicon wafers

[31] [31] Stocking out of Test Wafers prevents a tool from becoming available for production. The time lost is time which production wafer could have been run. Depending on the area, a down tool may stop the entire line. Unplanned tool downtime is minimized as much as possible.

prevents over starting expensive Test Wafer material. This decision is another cost advantage compared to the previous system which did not specify either the need or quantity limit. When starting the expensive Reclaim or Prime Test Wafers, the system is adding Test Wafer inventory to the route. After the new Reclaim and Prime Test Wafers are consumed, they are sent to R-GEN and P-Gen cleaning operations and return as the cheap and preferred option. In this manner, the overall Test Wafer inventory is maintained at an ideal level, another advantage with the DOI Scheduler system.

Exactly like the Ideal Trigger, the corresponding Test Wafer inventory level associated with the Critical Trigger changes as consumption changes. An increase in consumption increases the amount of Test Wafers corresponding to the fixed Critical Trigger and vice-versa.

Return to Ideal State:

Once enough new Reclaim and/or Prime Test Wafers have been added, the route returns to the Ideal State. At this point the process is repeated where only the cheap, preferred Test Wafers are started until, through a decrease in overall Test Wafer levels through attrition and scrap, the Critical Trigger is reached. At that point new expensive Test Wafers are started continuing the process.

The robustness and improvement of the DOI Scheduler program over the previous system is based largely on how the triggers are set. With the numerous route differences in pre-process time and consumption variability, setting the triggers has been challenging. It was obvious that a large amount of excess Test Wafer inventory could be found on many routes as seen by the Days of Inventory per route.[32] However, setting the triggers overly aggressively could lead to route stock outs. As a starting point, the Ideal trigger was set roughly at the corresponding minimum level trigger. Those routes with the corresponding Days of Inventory greater than 20 days were dropped to that more reasonable value.

5.3.2 DOI Algorithm

To understand the sequence of calculations and logic as well as the exact location of where the input data and variables are used, a block diagram algorithm of the DOI Scheduler program is provided in Figure 11. The grey and yellow boxes are the input data and input variables respectively as discussed in Section 5.2. The orange boxes are the calculation and logic boxes. The EWMA consumption forecast and Days of Inventory calculations were covered in the Sub-sections of 2.6. Details on the logic and decision trees will be addressed in the next section, 5.3.3. The red box shows the final decision output which will be described in 5.3.4.

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[32] Figure 1 illustrates a histogram showing approximately half of the routes having over 75 days of inventory
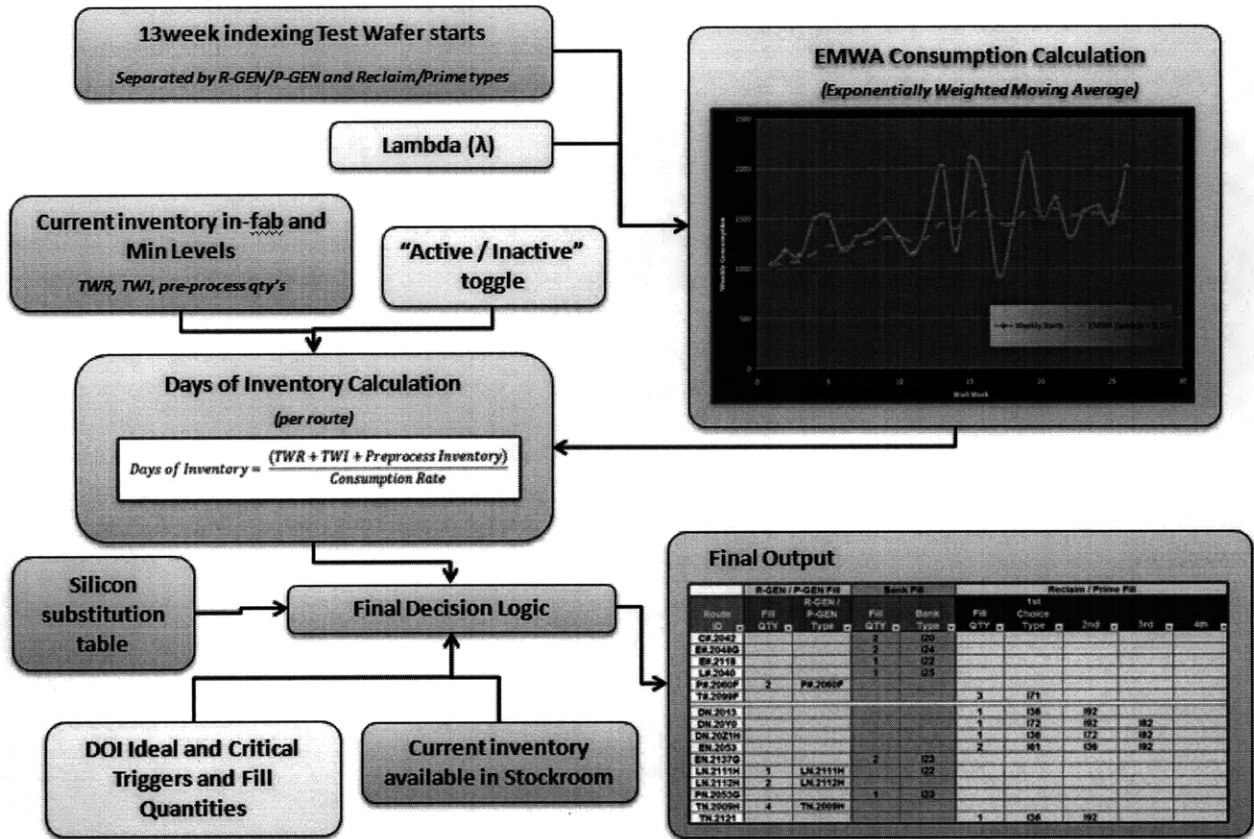
Figure 11: DOI Scheduler program algorithm

5.3.3 DOI Scheduler Logic Overview

As shown in Figure 11, once the Days of Inventory for each route is calculated, the silicon substitution table and available stockroom inventory inputted, and the DOI triggers and fill levels set, then the decision computations can occur. The DOI Scheduler logic ultimately leading into the final output conclusions can be broken into four sections as shown in Figure 12.
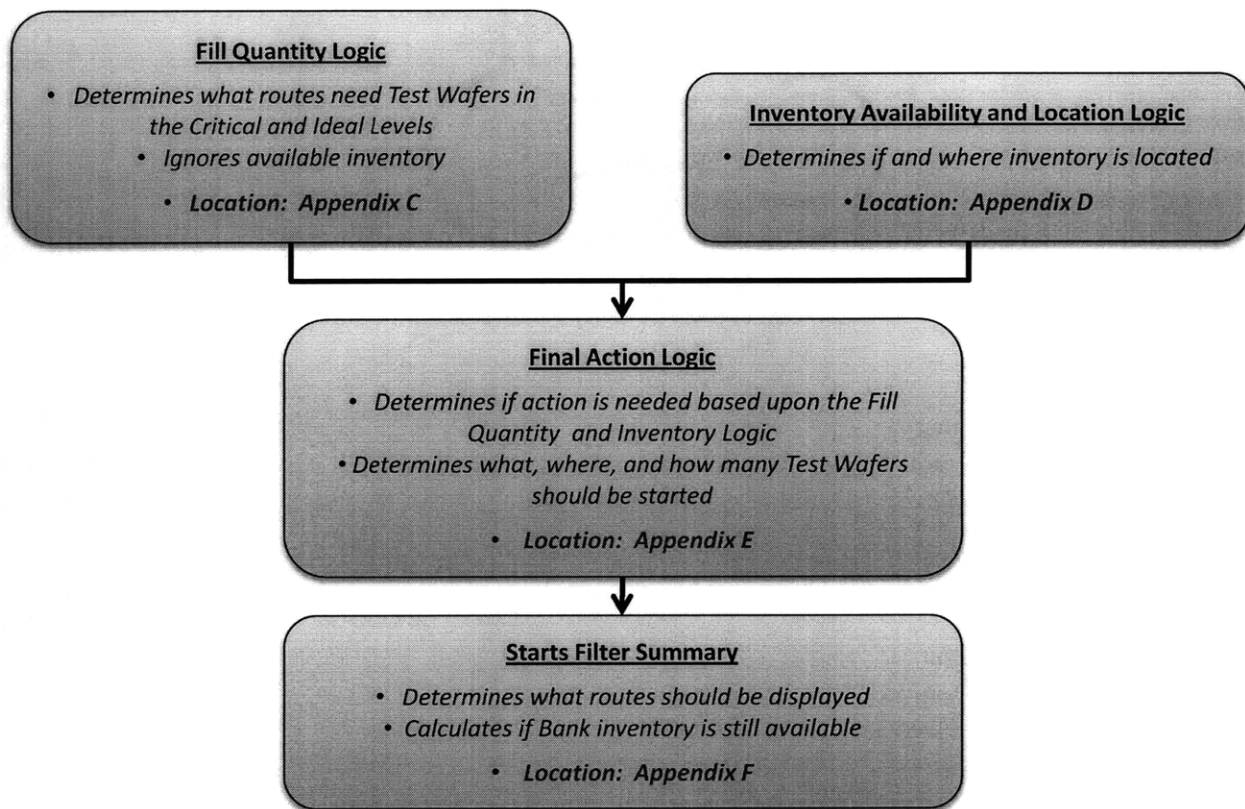
Figure 12: DOI Scheduler program logic categories

First, the "Fill Quantity Logic" deduces which routes and how many Test Wafers are needed. This is completed based upon the Critical and Ideal DOI triggers and fill levels with respect to the current Days of Inventory for each route. These calculations occur regardless of the available or type of inventory. Three examples are provided to illustrate this logic section. On each, the current Days of Inventory is shown in the blue box. If the current DOI state is less than the DOI triggers, then the difference between the fill level and the current state is output. Subsequent logic sections will determine if that amount should be filled depending on the criticality, type, and availability of Test Wafer inventory. Figures 13 through 15 contain example cases to help understand the fill quantity logic. The grey box contains the input variables, the blue box the current route inventory level, and the orange box the final logic output. The purple circle is a placeholder for the fill quantity logic.
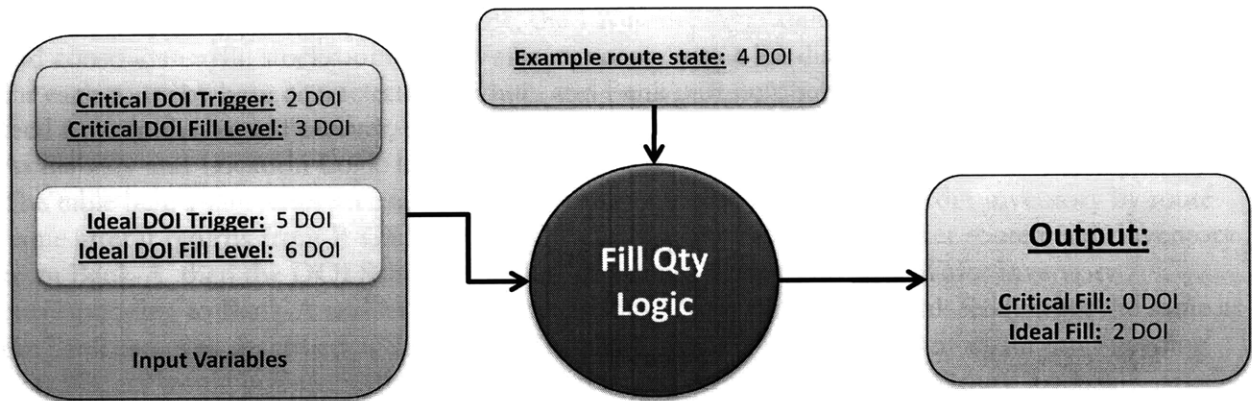
Figure 13: Fill Quantity Logic example 1: Current route DOI is less than Ideal DOI Trigger
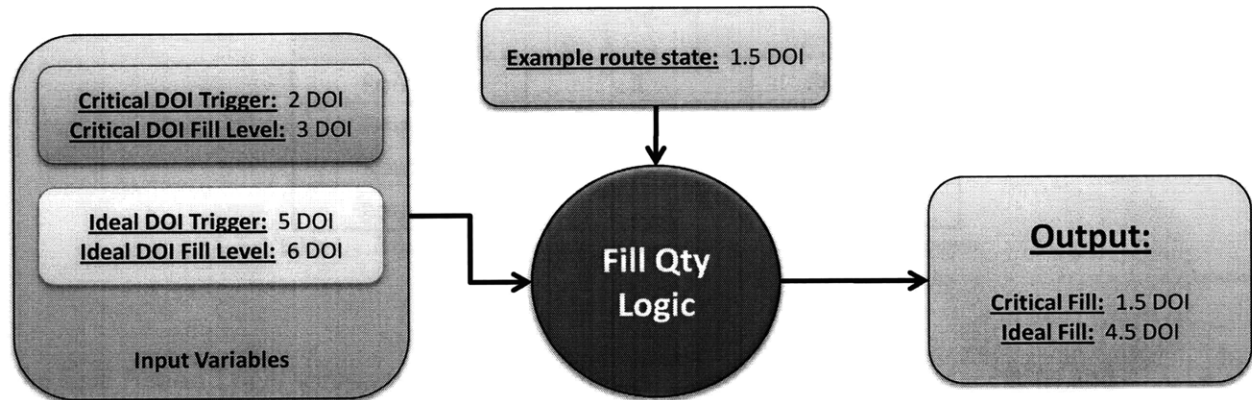
Figure 14: Fill Quantity Logic example 2: Current route DOI is less than Ideal and Critical DOI Trigger
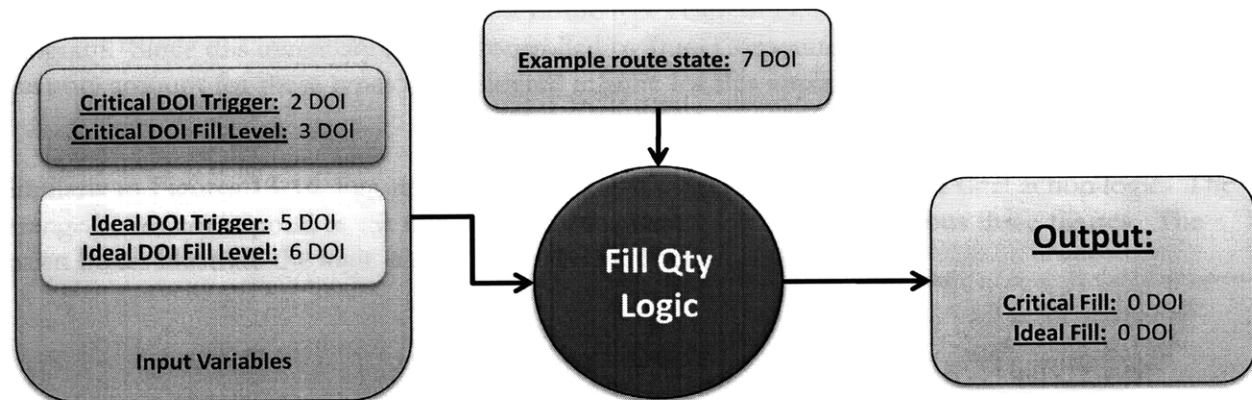
Figure 15: Fill Quantity Logic example 3: Current route DOI greater than Ideal DOI Trigger

Concurrently with the Fill Quantity Logic, the Inventory Availability and Location Logic formats and consolidates the stockroom Test Wafer inventory into a list displaying the available Test Wafers for each route by base characteristics, route, and bank part numbers. For example, many routes may feed a particular bank; however, they are held in the stockroom by their route name. The Inventory Availability and Location Logic identifies their similar base characteristics and sums their quantity. The table below illustrates an example where the stockroom holds bank feeder inventory by route name after it returns from R-GEN or P-GEN cleaning operations. If a eater route needs inventory from Bank-A, then the DOI Scheduler points to a route feeder with Test Wafer inventory corresponding to Bank-A and its base characteristics. Note that not all bank feeders are the same as the bank eaters as described in Section 2.5.3. In the example in Table 15, any route eater needing Test Wafers would pull from the Test Wafer inventory located in any of the route feeders.

Bank-A		
Bank Feeders	Test Wafer Inventory (lots)	Bank Eaters
Route-A	1	Route-B
Route-B	0	Route-C
Route-C	7	Route-E
Route-D	5	

Table 15: Available Inventory and Logic bank and route inventory location example

The final Action Logic section takes the outputs from the previous two logic sections and determines the final quantity and type of Test Wafers needing to be started for a route. For example, a route may want to start 2 DOI for the Ideal fill level, however if cheap R-GEN or P-GEN material is not available, then this logic section will conclude that no Test Wafers will be started. Four examples are provided to illustrate a few different cases.[33] Due to system limitations, the Test Wafer inventory for Reclaim and Prime types cannot be imported into the DOI Scheduler program. Since this inventory level is controlled by Intel Corporate and is conservatively set, the quantity amount for these types is considered infinite for this application.

Similarly to Figures 13-14, Figures 16-19 illustrate two example cases for the final action logic. The orange boxes correspond to the output from fill quantity logic in the previous three figures. The green boxes illustrate the logic output from the final action logic.

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[33] If a route has no start data over the past 13weeks leading to a zero consumption rate, then the route is treated on the minimum level trigger system. For these routes, the required fill amount is considered the same priority as the Critical DOI trigger. Since no consumption data is available to forecast need, the prioritization on when Test Wafers are needed at a route on the minimum level system is impossible to determine.
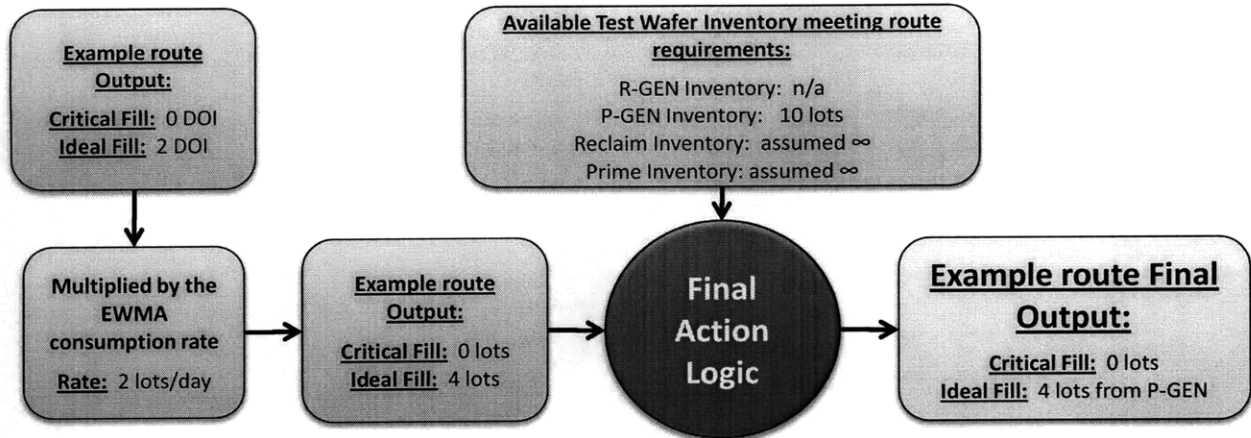
Figure 16: Final Action Logic example 1: Ideal Fill with available cheap Test Wafer inventory

In this first example, shown in Figure 16, the route needs Test Wafers to maintain at the Ideal level. Since cheap P-GEN Test Wafers are available, the Final Action Logic fills to the requested amount.
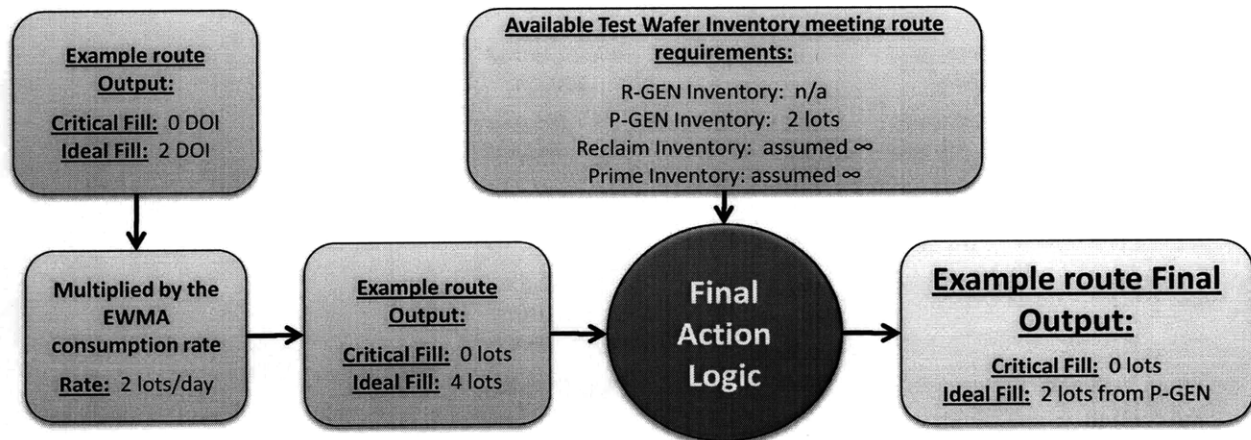
Figure 17: Final Action Logic example 2: Ideal Fill with a partial available cheap Test Wafer inventory

The Figure 17 shows a route with the same inputs as the Figure 16 example except only a partial amount of cheap Test Wafer inventory is available in the stockroom. Since the Ideal Fill can only use cheap Test Wafers, only part of the Ideal Fill request can be filled. Since the route state is above the Critical trigger, expensive Reclaim or Prime silicon is not started.
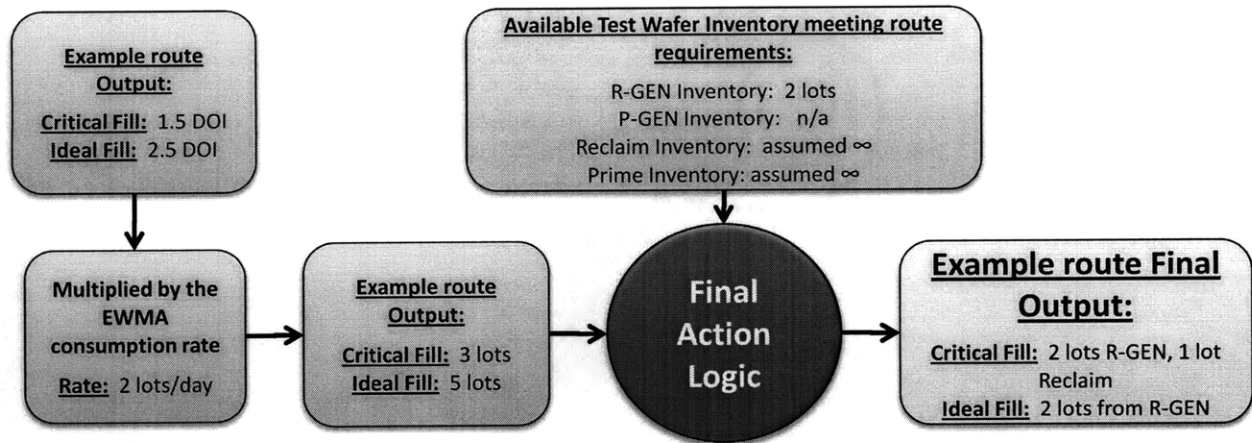
Figure 18: Final Action Logic example 3: Critical and Ideal Fill with partial available cheap Test Wafer inventory

In Figure 18, the route is below both Ideal and Critical trigger levels. Since only a fraction of the Ideal fill amount is available (only cheap R-GEN Test Wafers in this case), only a partial Ideal order is filled. For the Critical amount, that order must be filled to its entirety regardless of Test Wafer type. The two R-GEN Test Wafers are used first and then a Reclaim lot is used to meet the three lot requirement. The Starts Filter Logic discussed next condenses this information into a format easy to read, understand, and acted upon.
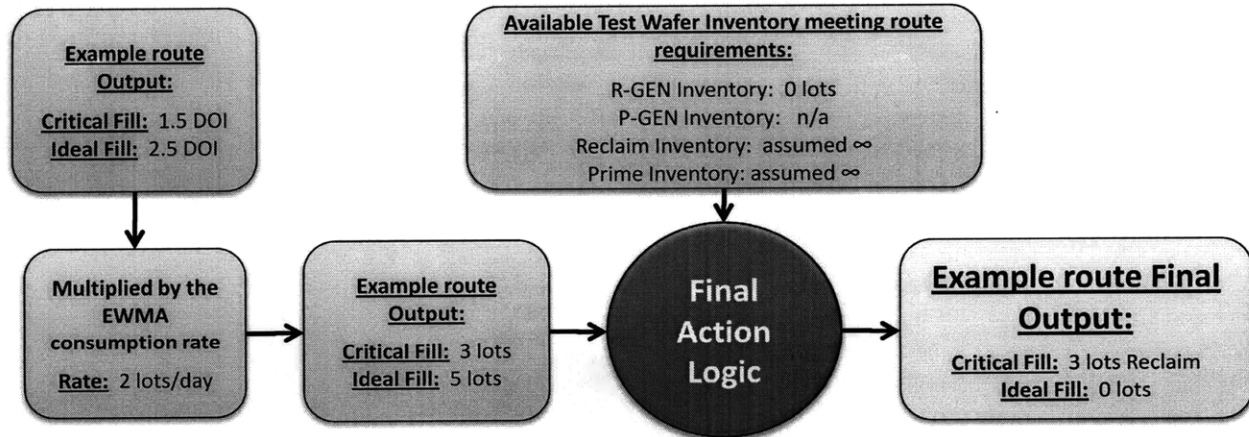
Figure 19: Final Action Logic example 4: Critical and Ideal Fill with no cheap Test Wafer inventory available

Figure 19, the last example, is the same as Figure 18 but without cheap Test Wafer inventory. Without the preferred material, no action is taken for the Ideal fill. All Critical fill needs must be met; expensive Reclaim lots are used.

The final Starts Filter Logic section filters the Test Wafer starts information into a condensed and convenient display. If the Final output described in the third logic section had both Ideal and Critical fill action, then at least the Critical amount is demanded. In addition to a simple Test Wafer

starts interface, the Test Wafer bank inventory locations described in the second logic section are also displayed in any easy reference format. These displays are covered in Section 5.3.4.

5.3.4 Output Results

With the logic complete, four output screens remain visible for the FSG technicians. The first is the total action summary table. This tab separates the routes by copper and non-copper usage. FSG starts Test Wafers destined for copper routes at a different location than the non-copper Test Wafer routes to minimize copper contamination risks. The final action table is also divided into three sections, R-GEN/P-GEN, Bank, and Reclaim/Prime. The R-GEN-P-GEN section (two leftmost green columns) contains all Test Wafer lots being started married to a particular route, assuring route integrity. The Bank section (middle purple columns) shows the Test Wafer lots started from the bank system. The last section (rightmost green columns) holds all Test Wafer lots starting with the expensive Reclaim or Prime Test Wafer type. Figure 20 illustrates an example DOI Scheduler final output screen.

Route ID	R-GEN / P-GEN Fill		Bank Fill		Reclaim / Prime Fill				
	Fill QTY	R-GEN / P-GEN Type	Fill QTY	Bank Type	Fill QTY	1st Choice Type	2nd	3rd	4th
C#.9042			2	Bank - A					
E#.9048G			2	Bank - B					
E#.9118			1	Bank - A					
L#.9040			1	Bank - C					
P#.9060F	2	P#.9060F							
T#.9099F					3	Reclaim - 1			
DN.9013					1	Reclaim - 2	Prime - 2		
DN.90Y0					1	Prime - 1	Prime - 2	Prime - 3	
DN.90Z1H					1	Reclaim - 2	Prime - 1	Prime - 3	
EN.9053					2	Reclaim - 1	Reclaim - 2	Prime - 2	
EN.9137G			2	Bank - B					
LN.9111H	1	LN.9111H	1	Bank - A					
LN.9112H	2	LN.9112H							
PN.9053G			1	Bank - B					
TN.9009H	4	TN.9009H							
TN.9121					1	Reclaim - 2	Prime - 2		

Figure 20: Example DOI Scheduler final output screen[34]

With the previous system, the final action tab was manually generated by the FSG technicians. Each row and column had to be verified and checked with the need on the floor, the Test Wafer availability in the stockroom, and the type needed. The majority of the labor resource savings are derived from the automated calculations and simple formatting with the DOI Scheduler. Additionally, with the logic and priorities contained within the program, FSG technicians now operate on a standard and much leaner process. The ease of use also allows for a faster learning curve further streamlining operations if a primary individual was sick or not working a particular day.

Three additional screens are also available to assist the FSG Technicians in completing and understanding the reasons behind the final output screen recommendations. The first is a summary

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[34] All values, route names, etc. are bogus

of the various banks and associated Test Wafer inventory levels and locations. Secondly, a summary tab of the logic and calculations is provided. This shows all input data and variables and summarizes the decision tree so the reader can understand why the final action is required. Lastly, a configuration control table illustrates program changes and the creator. These are shown in Appendix G.

5.4 Implementation Issues

Coupled with the DOI Scheduler programming challenges, the organizational and process issues also contained obstacles which needed to be overcome. With the previous state characterized with non-standard processes and a culture somewhat hesitant and apprehensive on large scale changes, aligning all organizational stakeholders was crucial in long term sustainability. From a process perspective, developing standard operating processes not only in FSG but also through the fab in pre-process operations and Test Wafer usage was necessary. Much of the success of the DOI Scheduler was predicated on changing human behaviors to support a lean, automated, and standardized system. Organizational alignment in support of these new processes was also important. Fab-wide education programs, networking, and coalition strategies were all employed to gather support and acceptance. The following subsections discuss these implementation issues in more detail.

The DOI Scheduler program was launched as a fab-wide pilot program for six weeks. A Learning Card approach outlining the hypothesis, anticipated outcome, and duration was used. Over this time suggestions were collected and improvements to the DOI Scheduler completed. With all success metrics trending towards the anticipated future condition, the program was released under configuration control as the standard program.

5.4.1 Process Issues

A Learning Card[35] approach was also taken for all process improvements supporting the DOI Scheduler. Two route pre-process areas were focused on during the six month internship as locations with either necessary improvements or large positive returns on investment.

Addressing pre-process time variability for Test Wafer lots was the largest risk to the DOI Scheduler. Since the program triggered Test Wafer starts based upon the time until that material was needed, any variability in the length of that time increased the risk of not having Test Wafers when needed. Additionally, for routes with a long pre-process time, not starting Test Wafers due to pre-process variability could lead to a tool being without material for hours or even days.

One pre-process cleaning operation was notorious for batching Test Wafer lots for extended periods of time. To bound the maximum time a Test Wafer lot could stay in that operation, a priority flag was coded into the system which informed that area which lots to run. Now, after a set amount of time, any Test Wafers not run get bumped to the top of the list ensuring that material moves in less than that ceiling time. A Learning Card was posted supporting the change and the process standardized after Test Wafer pre-process variability dropped.[36]

Similar approaches will be implemented in the future on other areas within the fab to continue to help Test Wafer material flow.

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[35] Defined in the glossary

[36] Initial pre-process times for this pre-process operation ranged from a few hours to over a week. After the improvement, all Test Wafer lots moved to the next operation in less than 36 hours.

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Human behaviors also had an impact on the variability of Test Wafer operations and activities. For example, technicians would often not "proc" Test Wafers to their next operation after completion until multiple lots were batched. This behavior was driven largely by laziness as those technicians felt that their time was better spent elsewhere. Since the DOI Scheduler counted Test Wafer quantity by operation, if used Test Wafer lots were not "proc'ed" to the next operation, the system would think material was available and ready when in actuality this was not the case. With multiple lots being batched and then "proc'ed" into the next operation, the DOI Scheduler would often need to start a large amount (a spike), creating an inventory bubble that adversely affects the material flow. Learning Cards in problem areas and top down education from management levels helped decrease this occurrence.

Lastly, with years of individual heroics supporting the non-standard Test Wafer processes, trusting the DOI Scheduler and new system was difficult for some individuals. A tendency to continue behaving in the same fashion as years prior led to confusion on a few occasions. For example, with FSG only starting material as determined by the DOI Scheduler, some technicians still wanted to base Test Wafer starts off of their direction and intuition. Continuing education programs redirecting this energy to areas like pre-process time variability reduction efforts are on-going.

5.4.2 Organizational Issues

To establish the standard processes supporting the DOI Scheduler, obtaining organizational support was crucial. Prior to any Learning Card improvement, key stakeholders were contacted and convinced of the purpose and outcome of the numerous test hypotheses. Both networking and coalition building techniques were used; the extent and exact approach varied depending on the type of individual and location within the organizational structure. For example, many technicians responded better with a grassroots approach instead of a top down mandate. Identifying influential technicians in the fab and educating them on the importance and direct positive effect of the new processes helped to spread knowledge and acceptance of changes. With other individuals such as long time engineers, obtaining concurrence and direction from plant management was needed to drive change away from the historic approach.

Building trust through all divisions such as the financial department, floor technicians, and lean educators was completed through effective communication, proactively helping on projects not directly related to thesis work, and extracurricular conversations. The use of the MIT, Leaders For Manufacturing title was used sparingly as it provided a positive status recognition for some while others felt the education establishment was too elitist.

A ten minute DOI Scheduler pitch was developed and presented across all shifts at various engineering and manufacturing meetings. Comments and feedback were incorporated into the DOI Scheduler with many of the individual aspects of route particularities captured through these forums.

Besides informal organizational education, a structured education course was also offered on the DOI Scheduler. Four classes, each building from the prior, were offered to any interested individual. These started with the theory behind a Days of Inventory approach and led to a detailed discussion of the actual programming formulas. The ultimate goal was to leave attendees with the knowledge and tools to manage the DOI Scheduler after the thesis internship period. Appendix G shows a few introductory slides from the class, all of the information covered is also in this thesis.

Lastly, a board game was developed to help educate floor technicians on the DOI Scheduler and the system flow of Test Wafers. Poker chips representing Test Wafer lots were moved around the board to different areas simulating the flow of Test Wafers in actuality. An explanation on how this

game works and the actual board is provided in Appendix I. A simulation interface written in Excel plotted the status and location of Test Wafers in an example route and provided great insight into the improvements of the DOI approach versus the antiquated minimum level system. This simulation also allowed for different consumption scenarios to be run and the DOI Scheduler response monitored.

6 Findings and Discussion

After implementation, the future prospects of the projects were based upon their results compared to the test hypotheses. If unilateral improvements occurred, then the continuation of the projects would happen. However, if no improvements or marginal improvements with an increase in detrimental aspects, then the lessons from this exercise would largely be as a warning for future improvements suggestions.

Both the Test Wafer inventory reallocation project and DOI Scheduler program saw both immediate and sustained improvements. In both cases, the full value received will be accrued over a longer period than the six month internship. Sections 6.1 and 6.2 respectively discuss the results from these hypotheses; current as well as future improvement forecasts are developed. A simulation analysis for the DOI Scheduler program is also provided to augment actual data.

Section 6.3 continues with a discussion of project results in terms of general implications. The potential savings for inventory management in other industries and applications are prevalent. The final section, 6.4 outlines future work and opportunities for Intel to continue supporting these projects and other Test Wafer improvement prospects.

6.1 Description of findings: Project 1

As anticipated by the forecasted consumption and scrap rate analysis, the reallocation of excess Test Wafer inventory to starved routes immediately began to return cost savings. The optimization model was based upon the amount of fresh expensive Reclaim or Prime silicon lots needed for slightly longer than one year. For some routes that were highly starved in their Test Wafer inventory levels, expensive Test Wafers would have been started within days if the reallocation had not occurred.

The specific allocation of the Test Wafer inventory was based upon the recommendations from the optimization program based upon the program constraints and requirements. For example, a particular route may have an increased cost to clean excess Test Wafer inventory whereas another route may be immediately accepting. Optimizing over the total Test Wafer material costs forecasted for the year time period led to a distribution of reallocated Test Wafers as well as a backfill of Reclaim and Prime material for those locations still needing wafers to meet the year forecast. The exact quantity of Test Wafer lots needed is proprietary; less than 2% of the yearly consumption will now need to be started with expensive Test Wafer types.

The pie chart in Figure 21 illustrates the location and percentage of the reallocated Test Wafer inventory. Before the reallocation optimization, 100% of the pie was dedicated to Route A.
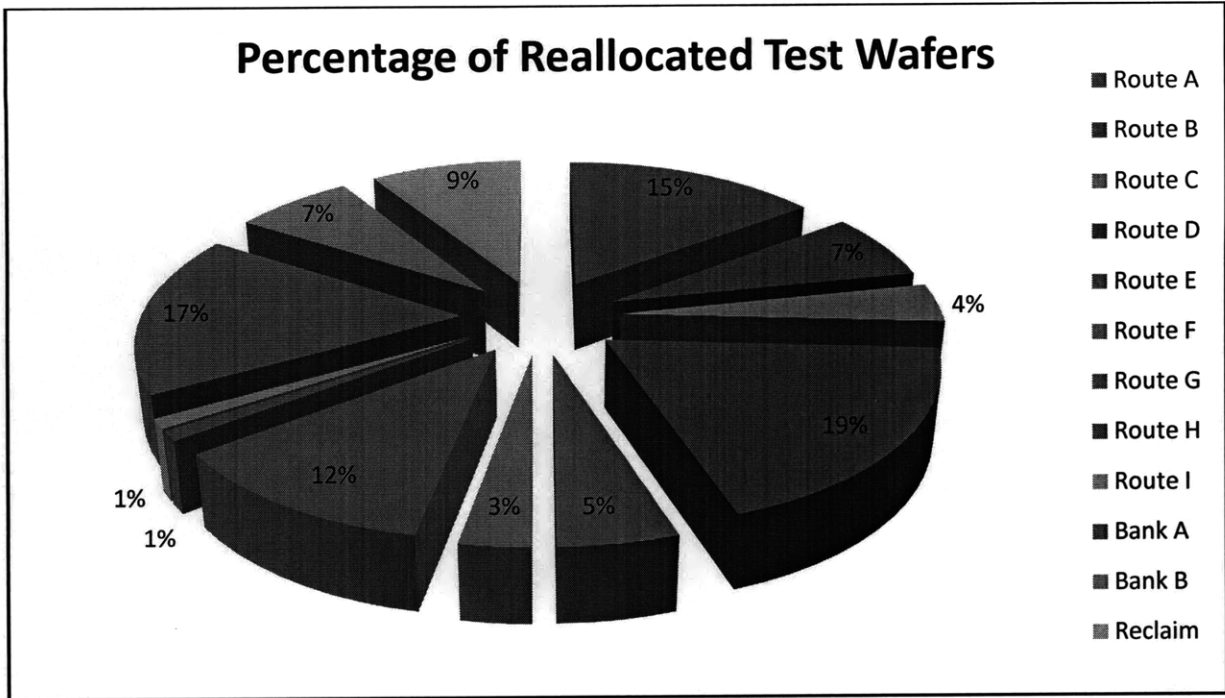
Figure 21: Project 1 results summary: Reallocated Test Wafer inventory quantity and location

Due to the age of some of the Test Wafer lots, a significant contamination risk existed. To mitigate concern, these lots were sent to a Reclaim vendor for a full grind, lap, and polish recycle process. The remaining routes and banks receiving Test Wafers were determined by forecasted need.

Calculating the savings from this project is easy, as we know the fixed cost delta for each reallocated lot used. However, with numerous cost improvement projects ongoing at Fab-17, observing these results in the current accounting and financial recording systems is difficult. Under the current system it is impossible to directly link monthly decreases in cost to this project alone. Additionally, with the forecasted time period over a year, the full realized savings will occur on a longer time period than the internship.

The actual quantity of Test Wafer lots and the corresponding cost savings associated with starting cheap Test Wafer material is Intel sensitive material. In an attempt to convey a rough order of magnitude of the savings, a public online search for Test Wafer costs was conducted. One website claimed that a typical 200mm prime Test Wafer cost $120-175 while 200mm recycled Test Wafers cost $25-50.[37] Using these numbers, a single lot of Test Wafers started with cheap R-GEN or P-GEN Test Wafers instead of Prime silicon would save approximately $2500. Extrapolating these savings over a year's worth of need results in realized savings in the hundreds of thousands of dollars range.

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[37] On-line source: http://www.solid-state.com/display_article/4257/5/none/none/Dept/The-move-to-300-mm-wafers:-A-prime-time-to-consider-reclaim . This value was obtained through a market survey completed in 1997.

6.2 Description of findings: Project 2

Prior to releasing the DOI Scheduler program, a simulation program was developed to analytically observe the program's responses. Two variables were changed over an accelerated time period to test various scenarios.

1. Test Wafer consumption: the rate of which Test Wafers are consumed on a simulated route
2. Test Wafer reject percentage: the percentage of Test Wafers rejected after usage due to natural attrition or quality concerns

Often, this simulation program was used to convince skeptical managers and engineers of the power of the DOI Scheduler approach. The simulation also contained an easy interface allowing real-time inputs and effects, which allowed it to be used in multiple stakeholder meetings. The simulation results for a particular case study are discussed in section 6.2.1.

The DOI Scheduler was initially launched as a fab-wide six week pilot program. Improvements in all of the anticipated results were observed. With improvements continuing and with no major issues, the DOI Scheduler was established as the baseline program at the conclusion of the pilot program. The DOI Scheduler program continues to be relied upon for all Test Wafer starts decisions and is integral in all relevant Test Wafer management processes. There is no plan to return to the previous system in the future. Table 16 outlines the results further discussed in section 6.2.2.

Improvement	Current State	Future State[38]
Test Wafer in-fab inventory levels	~15% reduction	~35% reduction
Test Wafer availability[39]	~25% reduction in Emergency Starts	~75% reduction in Emergency Starts
Human labor[40]	4-5hrs a week saved	4-5hrs a week saved with indirect savings from future process improvements
Root Cause analysis	- Found four issues with the old system otherwise unaddressed and unsolvable - Increased visibility on why decisions have been made	Continued ability to root cause problems and cater to individual route needs

Table 16: DOI Scheduler program summary results table

[38] Future State defined as the state 6-9 months after implementation under the assumption that sufficient resources will be allocated to continue driving the success of this project.

[39] Availability measured by summing the total number of Emergency Starts across all routes. Certain routes have seen a much larger reduction, in some cases eliminating all Emergency Starts. Other routes have increased the Emergency Starts slightly. A root cause analysis is completed on every Emergency Start with the cause being addressed to prevent future issues. In most cases modifying the trigger and fill levels immediately fixes the cause. In other cases, system level problem persist which were previously unable to discover. These are also addressed and solved.

[40] Future labor reduction will be seen; however, will most probably be obtained through process improvements supported by the DOI Scheduler program. These indirect savings are not counted here.

6.2.1 Simulation Results

The simulation model has one input table and three status display graphs from an example route. The simulation (called the "game") accelerates Test Wafer usage and scrap over a 20 day period. The system is modeled in Excel with the different processes corresponding to the game board shown in Appendix I. Figure 22 shows an overview of the DOI Scheduler simulation output.
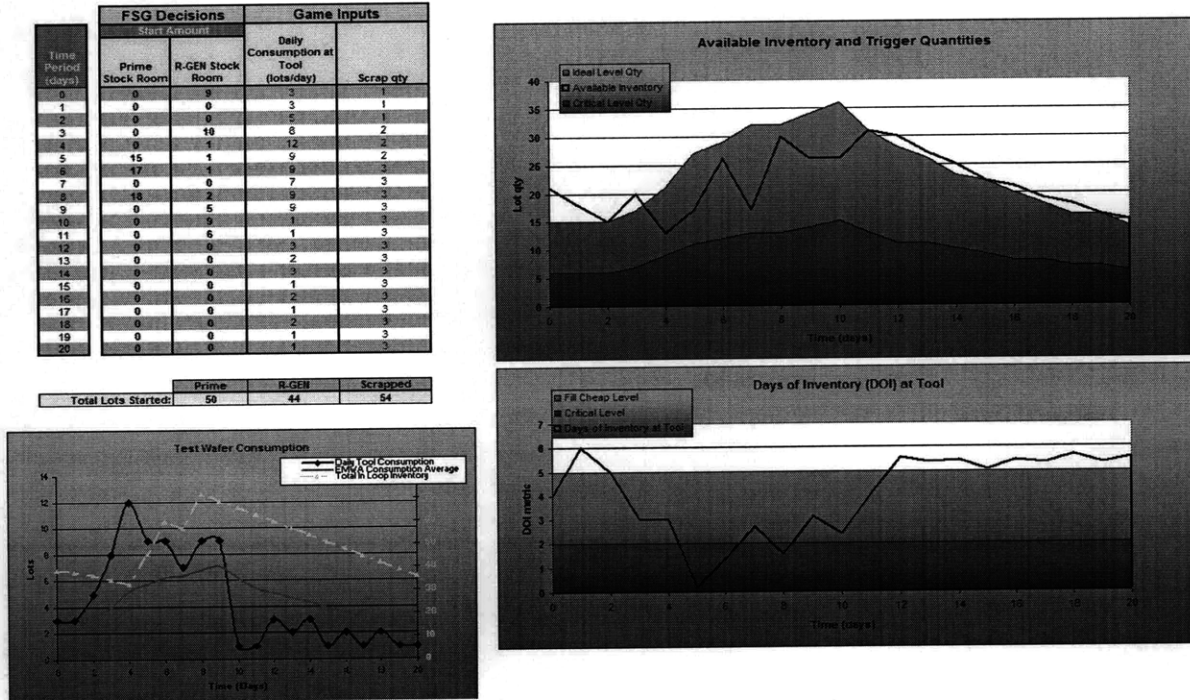
Figure 22: DOI Scheduler program simulation overview

In this scenario the daily consumption increases starting at three lots on day, peaks at 12 lots on day 4, and then tapers to one lot by day 20. The scrap rate is kept predominantly high at ~3lots per day as to accelerate total Test Wafer lot changes. The blue text are inputs, the black text is calculated values. The "Start Amount" column shows what type of Test Wafer was started, the R-GEN inventory being preferred and the Prime material only used when the DOI critical trigger is passed. Figure 23 illustrates the inputs for this simulation example.

Time Period (days)	FSG Decisions Start Amount		Game Inputs	
	Prime Stock Room	R-GEN Stock Room	Daily Consumption at Tool (lots/day)	Scrap qty
0	0	9	3	1
1	0	0	3	1
2	0	0	5	1
3	0	10	8	2
4	0	1	12	2
5	15	1	9	2
6	17	1	9	3
7	0	0	7	3
8	18	2	9	3
9	0	5	9	3
10	0	9	1	3
11	0	6	1	3
12	0	0	3	3
13	0	0	2	3
14	0	0	3	3
15	0	0	1	3
16	0	0	2	3
17	0	0	1	3
18	0	0	2	3
19	0	0	1	3
20	0	0	1	3

	Prime	R-GEN	Scrapped
Total Lots Started:	50	44	54

Figure 23: Input parameters for simulation example scenario

The graph in Figure 24 shows the Test Wafer consumption and inventory levels for the 20week simulation time period. The blue line depicts the amount of Test Wafer consumed each day. The pink line is the Exponentially Weight Moving Average (EMWA) corresponding to the consumption rate of the previous Test Wafer starts. A lambda value of 0.15 is used producing a curve which slowly trends as the consumption pattern changes over time. As described in the program algorithm in Section 5, the EMWA forecasts short term decisions. The dynamic adjusting of the trigger levels will be illustrated in the following two figures. Lastly, the yellow dashed line shows the total Test Wafer inventory in the system. As consumption increases, so does the overall inventory level. As consumption decreases, the overall inventory level decreases. Supporting intuition, the DOI Scheduler program is basing the Test Wafer starts decisions to automatically adjust to the optimal levels.
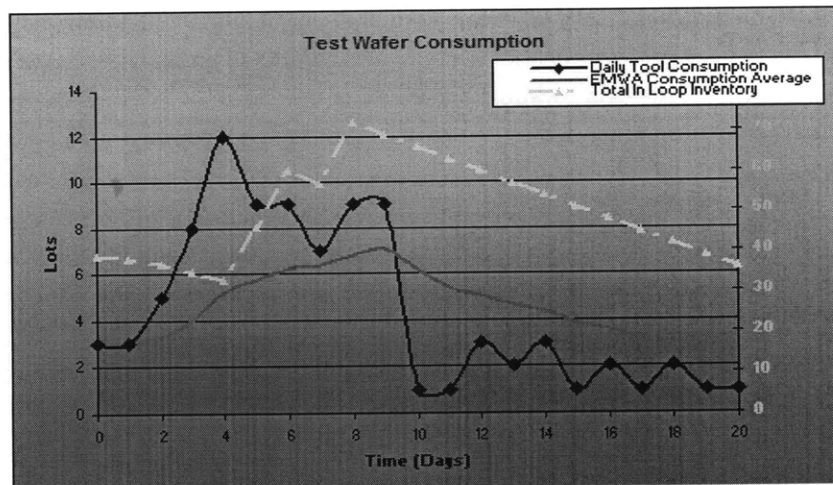

Figure 24: Simulation example consumption and inventory levels

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The second display graph, Figure 25, shows the DOI Ideal and Critical triggers in green and red shading respectively. This graph is the same as the graph used in the DOI Scheduler methodology section (5.3.1) but with a different consumption rate. The triggers are set at 5 DOI and 2 DOI. As Test Wafer lots are no longer available at the stockroom, the DOI Scheduler program releases expensive, prime Test Wafer lots to prevent a stock out. The availability of Test Wafer lots in the stockroom for the simulation is directly related to the consumption and scrap rates. The more Test Wafer lots that are scrapped, the less inventory is available. The higher the consumption rate, the more Test Wafer lots are needed to be started from the stockroom to prevent stock out. In this simulation, as the consumption increased around day 4, prime Test Wafers were started since the cheap Test Wafers were unavailable leading to an increase in overall inventory levels.[41]
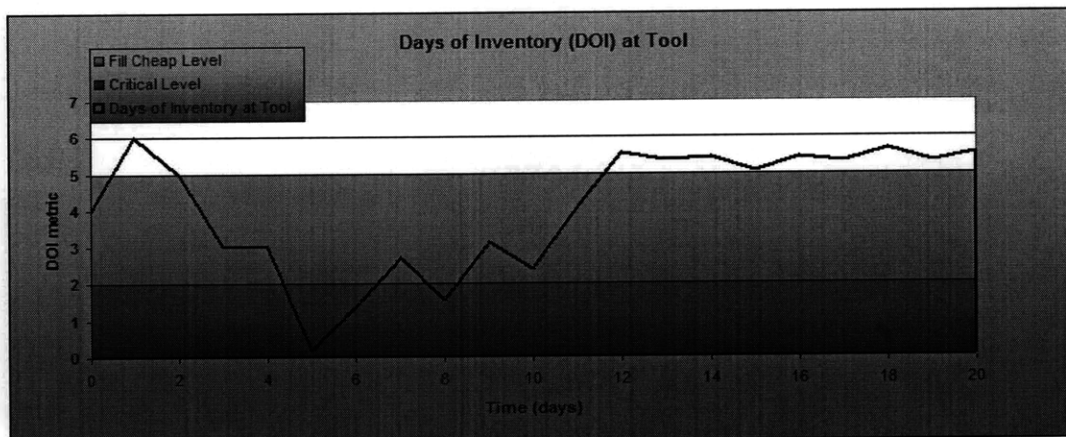
Figure 25: Simulation example inventory DOI graph

The final display graph illustrated in Figure 26 changes the "y" axis from Days of Inventory to actual lot quantity at the tool. The green and red shadings are the corresponding DOI triggers based upon the consumption rate.[42] This helps illustrate the dynamic nature of the DOI Scheduler program. As consumption rate increases, so do the required inventory quantity corresponding to the time until stock out. As the consumption rate decreases, the corresponding inventory levels automatically adjust.

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[41] Figure 23 shows the type of Test Wafers started adjacent to the daily consumption rate. Figure 24 shows the overall inventory level being driven by new, prime Test Wafers being introduced into the system.

[42] Corresponding Lot Qty trigger for the Days of Inventory = (DOI trigger) * (EMWA consumption forecast)

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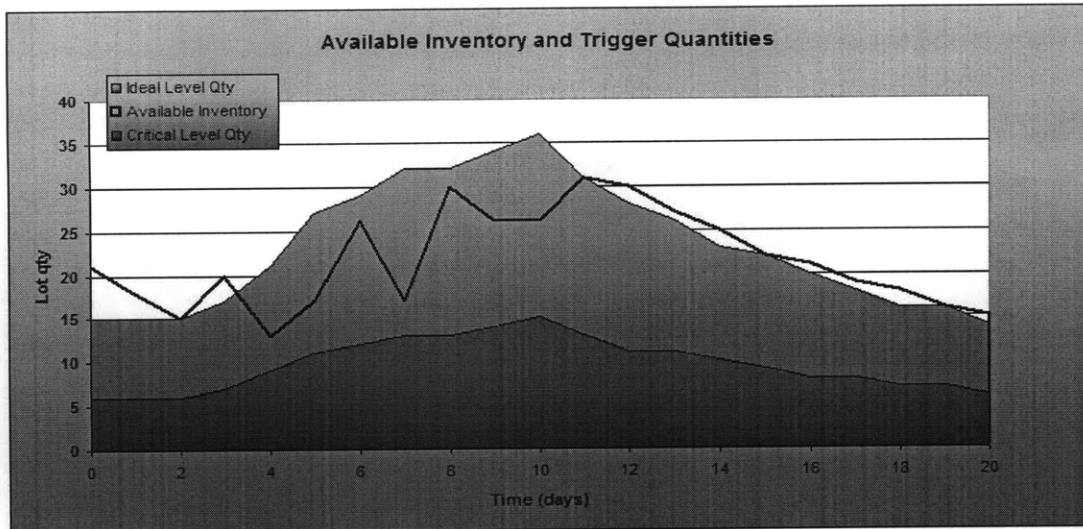
Figure 26: Simulation example lot quantity graph

6.2.2 Actual Results

Four primary measurements were used to determine the success of the DOI Scheduler program. First, a reduction of the in-fab Test Wafer inventory was predicted. By looking at Test Wafer inventory levels in terms of time until stock out instead of a quantity perspective, a histogram was generated showing approximately half of the routes with over two months of Test Wafer inventory. As these routes continue to consume Test Wafers and with the DOI Scheduler program not starting any additional lots, over time the histogram will shift with more routes having a more reasonable 0-20 DOI. The speed at which these results are seen depends primarily on the consumption rate of the routes. Routes with a slow consumption rate can take months or years to consume the Test Wafer inventory excess. Furthermore, some routes are no longer active; their Test Wafer inventory sitting in limbo with no process to consume or remove from the fab.

Histogram of Days of Inventory (DOI) per Route

(*) Routes with no measurable consumtion in the past 13 weeks
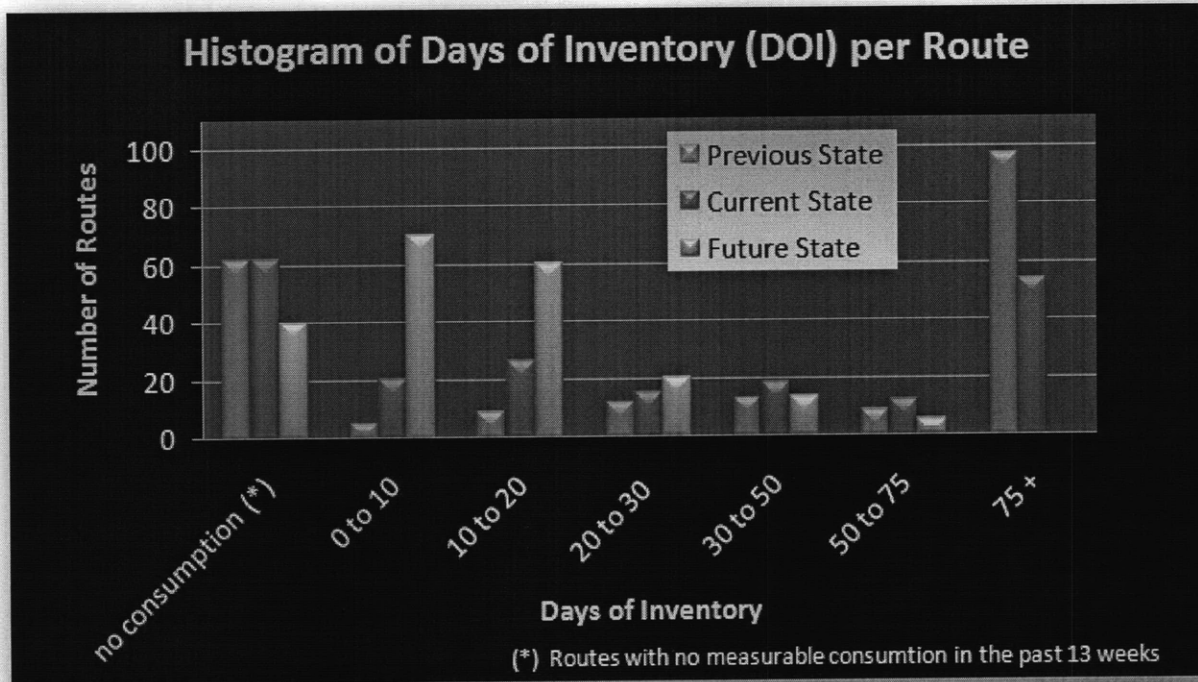
Figure 27: Histogram showing Test Wafer DOI inventory levels per route

Figure 27 shows a histogram of the improved state after the DOI Scheduler program had been implemented for six weeks. Comparing the red bars (current state) to the blue bars (previous state with old system), the decrease in the number of routes with over 75 days of inventory and an increase in the number of routes in the 0 to 10 and 10 to 20 DOI range can be seen. A future state (green bar) shows the final anticipated distribution as low consumption route inventory levels are reduced and inactive route inventory is removed. The corresponding inventory reduction savings can be summarized in Figure 28.[43]

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[43] Actual Test Wafer inventory levels removed for confidentiality purposes
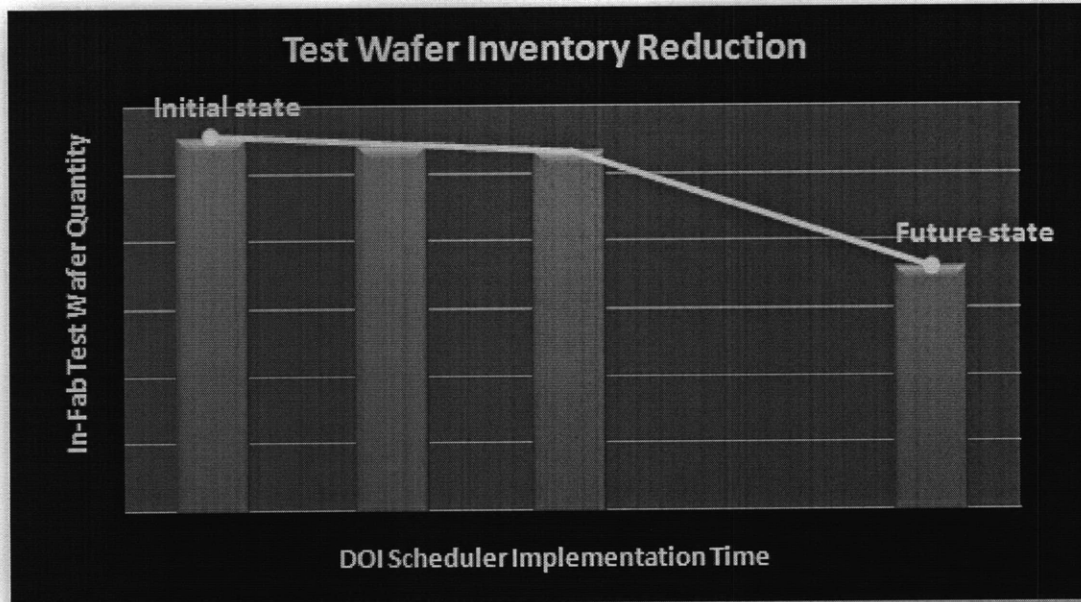
Figure 28: In-fab Test Wafer inventory reduction

Feedback from floor technicians clearly suggested that Test Wafer availability improvements had occurred; being able to quantify that observation was challenging due to the measurement systems. To derive improvement percentages, the Emergency Start list was segmented into two parts, one list of consumption excursions causing stock outs and the other being normal consumption leading to stock out. Approximately 75% of the Emergency Starts were attributed to process issues under normal consumption patterns. With the DOI Scheduler program standardizing the baseline approach, all normal consumption stock outs should be removed.

Currently, a ~25% improvement in the decrease of stock outs on a route basis has occurred and continues to increase. Establishing and executing a fab-wide standard process and setting the DOI Scheduler program triggers and fill levels optimally are two areas of continuing work.

From a human labor perspective, the DOI Scheduler program immediately saved 4-5 hours per week previously spent on required activities to determine and release Test Wafers into the fab. By automating and intelligently measuring the key parameters, FSG's job has been dramatically simplified. Future labor improvements will be seen over time as the process becomes more familiar and the DOI Scheduler program foundation allows additional improvement initiatives. Lastly, the job simplification and documentation will allow easier transitions for new hires and better maintain a sustainable legacy.

Standardized processes are the foundation of lean methodology and its success. The DOI Scheduler program was the key component in launching a set and repeatable process for starting Test Wafers into the fab. Since then, numerous additional Test Wafer improvement projects have been initiated otherwise impossible to achieve their full savings. A few of these projects include:
  - Removing excess and antiquated Test Wafer inventory from the fab to maximize usable space and minimize holding costs

- Expand the banking system with additional routes of identical base requirements
- Educate and optimize Test Wafer processes beyond FSG

Furthermore, the standardized process now enables root cause analysis on previously unsolvable Test Wafer issues. With the full visibility of the DOI Scheduler program, the exact reason why Test Wafers were started is known and archived. If Test Wafer availability is not proper, then the exact reason can be deduced and corrected. Numerous problems with data sources previously thought to be accurate have been uncovered and corrected.

6.3 General Implications for Other Industries

Although Test Wafers are limited to a small number of industries, the basic principles behind these two improvement projects can be applied to many inventory and operations management situations. The approach behind lean manufacturing based improvements was exemplified throughout both the excess inventory reallocation and DOI Scheduler program. First identifying complex problems through direct observations and value/process mapping techniques and then conducting small and rapid improvements to test improvement hypothesis can be applied to any process. Even if the test hypothesis does not yield the anticipated results, any learning will drive future tests.

The foundation of lean manufacturing is built upon standardization. Establishing a standard process then allows a scientific problem solving approach where specific variables can be tested in a controlled environment. Additionally, quality issues and process excursions can be more easily ascertained and addressed. As described in the previous section, one of the great improvements the DOI Scheduler program has provided is the ability to complete root cause analysis. In summary, this thesis is a fantastic example of the success that following a scientific, lean problem solving approach can produce. The elimination of waste, either in over-processing and excess or in waiting and downtime, is the goal of any business operation.

Besides the approach, both thesis projects can be applied to any number of other inventory examples. Understanding the implications of how much inventory to hold enables large savings through optimal availability levels and holding costs. Triggering inventory need from a dynamic forecast approach while simultaneously addressing thousands of constraints and requirements challenges many industries. Incorporating consumption rates into the trigger metric provides greater insight into the appropriateness of inventory levels.

Proper measurement is necessary to fully understand the health of an operation. It is critical to incorporate the correct metrics and indicators to effectively communicate status. By not incorporating key elements in the metric, wasteful connections and interactions will be required to understand actual performance.

6.4 Future Work

Specifically for Fab-17, the future work stemming from the completion of this thesis project revolves around further standardization of Test Wafer management processes and maintaining the continuous improvement approach. The DOI Scheduler program provides a robust foundation for a standard Test Wafer delivery process which automatically optimizes its decisions as future improvement projects decrease Test Wafer consumption and decrease process variability.

The full extent of the improvements seen from both thesis projects will be observed over the next six to nine months. The list in Table 17 identifies a few key activities which the author feels would be beneficial to Intel.

Improvement	Description
Upgrade DOI Scheduler to a web-based application	Transfer the Excel-based program into a more robust and supported web-based application. Develop an easier user interface and have the automation group support any issues.[44]
Clean out old Test Wafer lots	To realize the full inventory savings, old lots from low consumption or no longer active routes must be manually removed.
Improve visualization of Test Wafer status	The current measurement and visualization of Test Wafer status is inadequate. Improve system to allow users to easily understand past trends and the future Test Wafer starts.
Continue education, Test Wafer ownership and accountability	Couple the current Test Wafer education efforts with clear ownership and accountability of Test Wafer performance. Establish clear job specifications and have the Test Wafer Engineer manage all Test Wafer Coordinators in a adjacent organization.

Table 17: Fab-17 future work summary

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[44] The current Test Wafer Engineer now has ownership of the DOI Scheduler program. Unfortunately he is overworked and does not have the time to properly maintain any issues or improvement activities.

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APPENDIX A: REALLOCATION OPTIMIZATION MODEL INTERFACE

Figure 29: Example screenshot of the Reallocation Optimization interface[45]
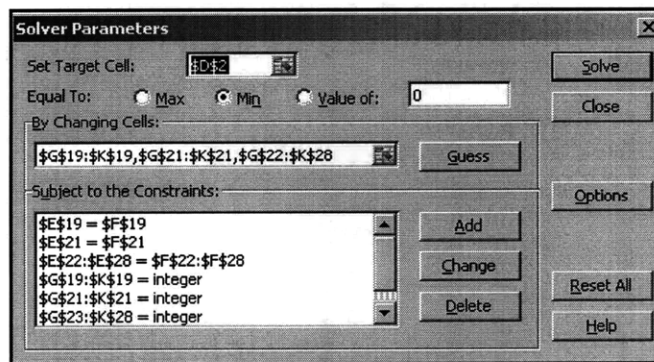
Figure 30: Solver Parameter screenshot

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[45] The screenshots above are provided for reference only. All data and values are bogus.

Appendix B: Common Excel Formulas Used in DOI Scheduler

The following formulas were used extensively throughout the DOI Scheduler. These are provided as reference with a brief description and example on how they can be used.

Logic:

- **IF**
  - *Returns one value if the condition specified is true, returns another if false*
  - *=IF(logic test, value if true, value if false)*
- **AND**
  - *Returns true if all arguments are true, returns false if one or more are false*
  - *=AND(logic1, logic2)*
- **OR**
  - *Returns true if one or more arguments are true, returns false if all are false*
  - *=AND(logic1, logic2)*
- **Nested Example**
  - *=IF(AND(logic1, logic2),value if true, value if false)*

Data handling and lookup:

- **INDEX, MATCH**
  - *References a cell and returns a value from an array*
  - *=INDEX(search array, MATCH(reference cell, reference column in search array, 0), number of columns from array start to return)*
- **ISERROR**
  - *Test if the cell value is in error*
  - *Example:*
    - *=IF(ISERROR(reference cell), value if true, value if false)*

Math functions:

- **ROUND**
  - *Rounds the number specified*
  - *=ROUND(reference cell, number of digits)*
- **ROUNDUP**
  - *Rounds up the number specified*
  - *=ROUNDUP(reference cell, number of digits)*
- **MOD, INT**
  - *Round up to the nearest multiple*
  - *=IF(MOD(number to round, multiple), INT(number to round/multiple) + 1, (number to round / multiple))*
- **SUM**
  - *Adds the cells of a range*
  - *=SUM(range)*
- **SUMIF**
  - *Adds the cells meeting a specific criteria*
  - *=SUMIF(range, criteria, sum range)*

Same as LOOKUP but without the limitation requiring the data to be in ascending order

Table 18: Commonly used Excel formulas

APPENDIX C: DOI SCHEDULER – FILL QUANTITY LOGIC

The decision tree below outlines the logic behind determining how many Test Wafers are needed with respect to the current Days of Inventory compared to an individual route's DOI trigger and fill levels. This logic is calculated regardless of the availability and type of Test Wafer. Those criteria will filter the final action in subsequent logic sections.
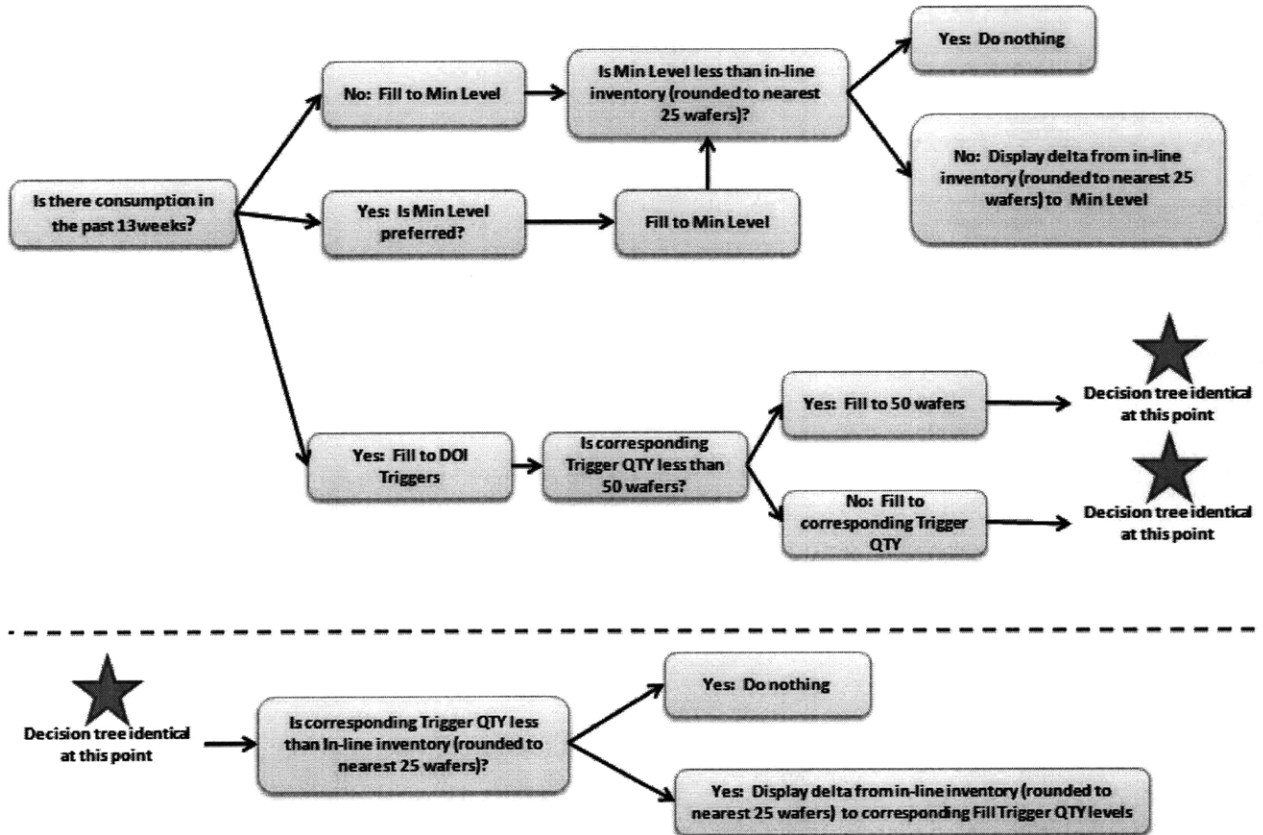
Figure 31: DOI Scheduler - fill quantity decision tree

APPENDIX D: DOI SCHEDULER – AVAILABLE INVENTORY LOGIC

The decision tree below outlines the logic associated with concluding the available Test Wafer inventory in the stockroom. These decisions are further complicated with Route and Bank integrity as well as the silicon substitution table. Once the priority of Test Wafer type for each route is known, then the DOI Scheduler program refers to the available Test Wafer inventory in the stockroom to determine if a cheap R-GEN or P-GEN option is available. The location of this option may be in either lot, route, or bank integrity holding locations.
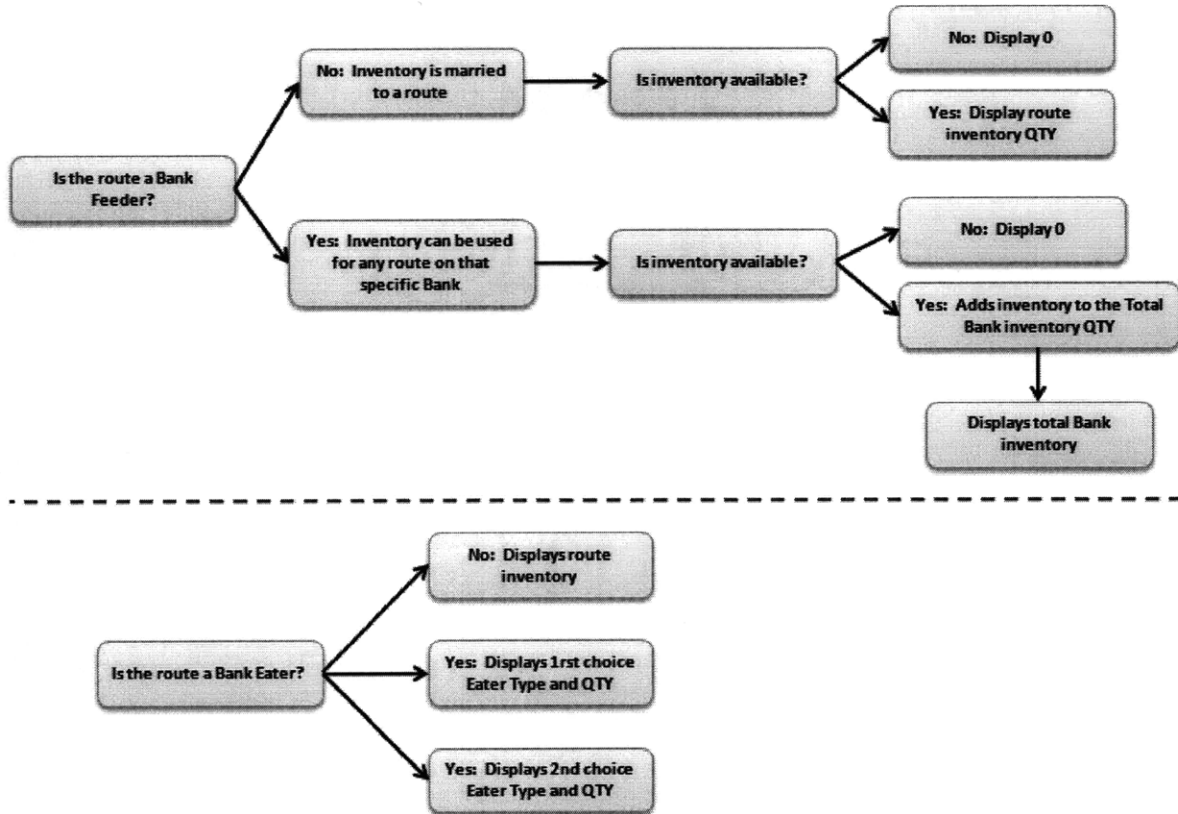
Figure 32: DOI Scheduler - available stockroom inventory decision tree

APPENDIX E: DOI SCHEDULER – FINAL ACTION LOGIC

Once the available Test Wafer inventory and the needed quantity is known, then the decision tree below is used to determine the amount of Test Wafer lots and the type of Test Wafers to use are deduced. This final logic calculation depends on the Days of Inventory of a particular route compared to its trigger and fill levels. Test Wafer lots of different types may be started to get to the required fill level.
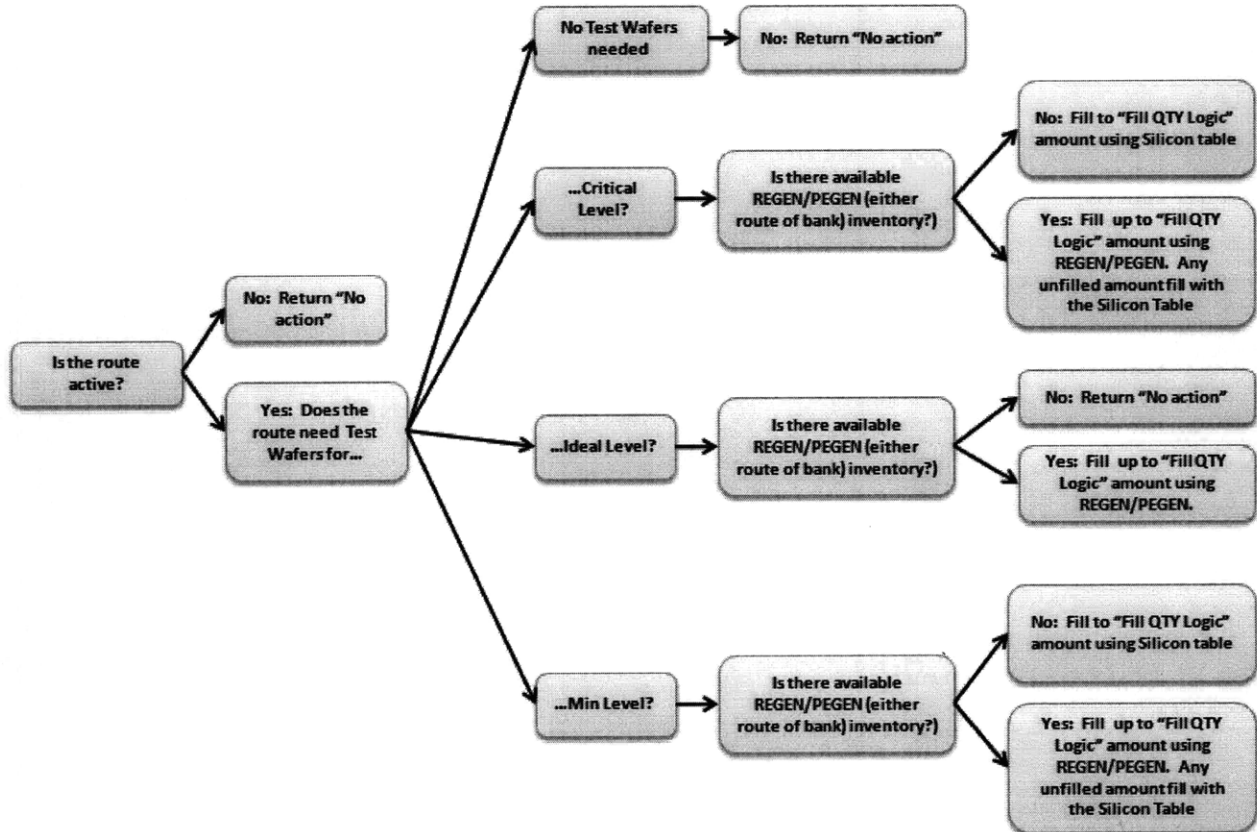
Figure 33: DOI Scheduler - final Test Wafer action decision tree

Appendix F: DOI Scheduler – Starts Display Logic

The final logic decisions filter the information to a succinct list. The location and quantity of Test Wafers for each route are shown while routes with no action needed are hidden. The available bank inventory in the stockroom is also shown as a reference for the FSG technicians.

Figure 34: DOI Scheduler - final output display decision tree

The following three output screens are examples showing the Test Wafer bank inventory summary, DOI Scheduler calculation summary, and configuration control table. These are discussed in detail in Section 5.3.4. All data is for example purposes only and does not reflect actuality.

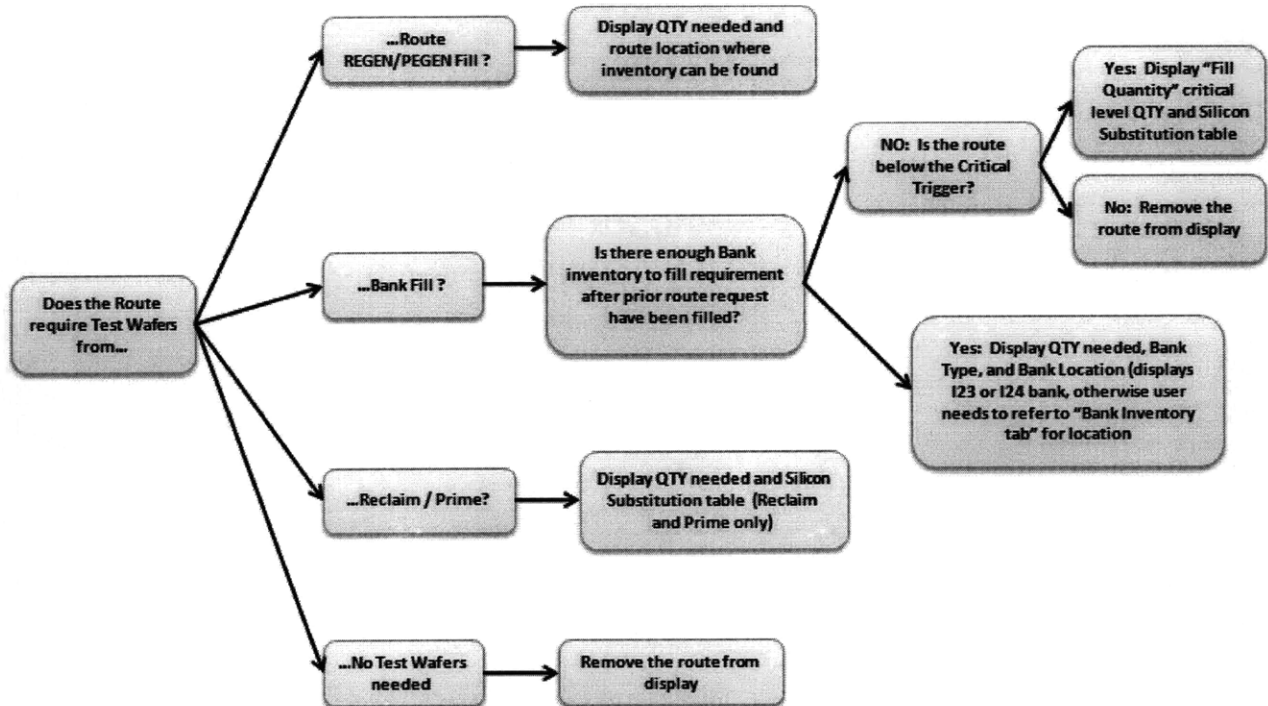| Bank	Inventory location (Stockroom)	Current Inventory
I12	EN.2023H	0
I12	TN.2005H	0
I12	TN.2031H	0
I12	TN.2048H	
I18	DN.20Y0	
I18	DN.21Y1H	
I20	DN.2017H	
I20	DN.20N0H	11
I20	DN.20Z1H	56
I20	DN.21N1H	
I21	PN.2018H	1
I22	EN.2008	
I22	EN.2014	
I22	EN.2015	
I22	EN.2020H	0
I22	EN.2022H	0
I22	EN.2024	
I22	EN.2046H	0
I22	EN.2093H	0
I22	EN.2120	
I22	LN.2000	
I22	LN.2004	
I22	LN.2028H	0
I22	LN.2050H	
I22	LN.2081	
I22	LN.2103H	0
I23	17PGBK	30
I24	#17PGBK	19
I25	L#.2004	
I25	L#.2028	23
I25	L#.2042	
I25	L#.2050	0
I26	T#.2005	2
I26	T#.2024	0
I27	P#.2001	
I29	E#.2016	
I29	L#.2002G	0
I70	DN.20L1	
I70	DN.21L1	

Figure 35: DOI Scheduler final output: Bank inventory summary example

Route	Status	TWR, TWI, in line inventory (wafers)	Consumption Forecast (daily wafer usage)	Days of Inventory (DOI)	Current Min Level (Wafers)	Critical DOI				Ideal DOI				Available Inventory in Schenker?	Action!				
						Trigger (DOI)	Inventory level (DOI)	Trigger (qty)	Inventory Level (qty)	Trigger (DOI)	Inventory level (DOI)	Trigger (qty)	Inventory Level (qty)		Fill REGEN/ PEGEN (qty)	Fill Bank (qty)	Fill Bank (type)	Reclaim or Prime (qty)
PN.2055G	active	113	0.1	1071.4	150	10	11	50	50	15	16	50	50	yes				
PN.2056	active	25	0.0	no consumption	25	10	11	25	25	15	16	25	25	no				
PN.2093	active	50	0.0	no consumption	50	10	11	50	50	15	16	50	50	no				
T#.2005	active	100	7.1	14.2	100	13	15	92	106	16	17	113	120	no				
T#.2009H	active	214	15.3	14.0	325	10	11	154	169	15	16	230	246	yes	1			
T#.2020F	active	218	23.0	9.5	250	7	8	162	185	10	11	231	254	yes	2			
T#.2025H	active	315	89.5	3.5	300	1.5	2	135	180	3	3.5	269	314	yes				
T#.2042	active	171	0.4	444.8	200	10	11	50	50	15	16	50	50	yes				
T#.2086	active	25	1.1	23.3	75	10	11	50	50	15	16	50	50	yes		1	120	
T#.2098F	active	113	5.8	19.5	250	10	11	58	64	15	16	87	93	yes				
T#.2099F	active	143	26.2	5.5	275	5	6	132	158	7	8	184	210	no				
T#.2100F	active	173	29.8	5.8	225	3	4	90	120	5	6	149	179	yes				
T#.2101G	active	149	3.8	39.3	200	10	11	50	50	15	16	57	61	yes				
T#.2103	active	150	16.5	9.1	250	7	8	116	133	11	12	182	199	no				
T#.2105	active	50	0.7	70.4	75	10	11	50	50	15	16	50	50	no				
T#.2107	active	125	8.9	14.0	200	10	11	90	99	15	16	135	144	no				
T#.2112H	active	118	5.3	22.2	300	10	11	54	59	15	16	80	86	yes				
TN.2000	active	50	1.6	31.5	50	7	8	50	50	10	11	50	50	no				
TN.2003H	active	82	4.2	19.6	175	10	11	50	50	15	16	63	67	yes				
TN.2004	active	50	0.6	77.3	75	10	11	50	50	15	16	50	50	no				
TN.2009H	active	341	28.4	12.0	400	10	11	285	313	15	16	427	455	yes	5			
TN.2010	active	49	0.5	90.8	50	10	11	50	50	15	16	50	50	no				
TN.2019	active	50	0.2	237.0	50	10	11	50	50	15	16	50	50	no				

Figure 36: DOI Scheduler final output: DOI calculations and logic summary example

Date	Submitter	Change	Comment
12/23/2008	D. Johnson	Added Change Control tab to track updates to the DOI Scheduler	
12/23/2008	D. Johnson	Updated the Bank QTY logic formulas. Previously the formulas referenced a redundant table. Now the formulas reference the original table simplifying calculations and future spreadsheet modifications	
12/23/2008	D. Johnson	Updated the following Litho routes back to the Min Level system per request from Potsy	
1/5/2009	D. Johnson	Updated columns headings in consumption tabs to "WW -1, WW -2, WW -3, . . ." standard	
1/5/2009	D. Johnson	Added a column in "DOICalc" tab to adjust min floor quantity.	Default currently set at 50 wafers for all routes
1/5/2009	A. Keselman	Updated rt. DN.2052 per B Jubinville with Floor qty from 50 to 75 wfrs with all related time adjustments	
1/5/2009	A. Keselman	Updated rt. E#.2115 per Pat Eboah request with Floor qty from 50 to 75 wfrs with all related time adjustments	
1/5/2009	A. Keselman	Updated rt. E#.2030 per Pat Eboah request with Floor qty from 50 to 100 wfrs with all related time adjustments	
1/5/2009	A. Keselman	Updated rt. E# 2029 per Pat Eboah request with Floor qty from 50 to 75 wfrs with all related time adjustments	
1/6/2009	A. Keselman	Added new route C# 2043A using i51 Reclaim Si ONLY	Default currently set at 50 wafers for all routes
1/12/2009	D. Johnson	updated "DOI Details" tab display such that in-line/TWR/TWI inventory and min levels are displayed for "non-active" routes	

Figure 37: DOI Scheduler final output: configuration control example

A four part education class was held at Fab-17 open to any employee interested in learning more about the DOI Scheduler and how it works. Attendance was supportive with individuals from multiple disciplines and backgrounds in attendance. Much of the materials is repetitive to what is discussed in this thesis; albeit, in a different, presentation format. A few screenshots are provided to show the format and approach.
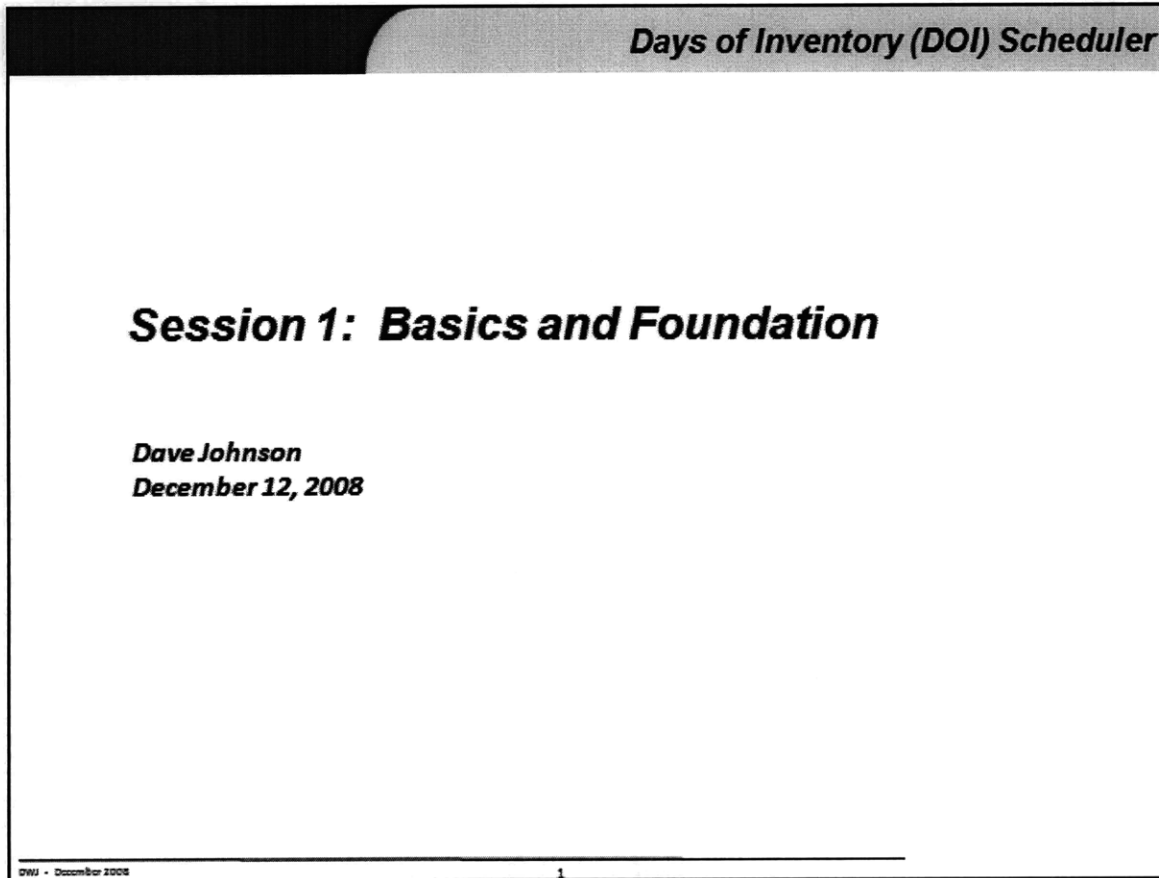

Figure 38: DOI Scheduler Class - Introduction slide

Session 1: Basics and Foundation
- DOI Scheduler advantages
- Big picture – how it works
- Algorithm overview
  - Tab identification and description
  - Input file locations
- Monitoring and sustaining
  - Be able to navigate, understand, and explain the Final Output tabs

Session 2: Primary Calculations and Backbone
- Common Excel formula overview
- Backbone data
  - Master route and information lists
- Consumption calculation
  - Exponentially Weighted Moving Average (EMWA)
- Inventory calculation
  - Bank Feeders/Eaters and Route systems
- DOI Calculation
  - Changing input parameters

Session 3: Logic and Decision Trees
- Fill quantity
  - Ideal and Critical levels
  - Min Levels
  - Outlying routes
- Inventory determination and location
- Action logic
- Fill summary
- Starts filter summary

Session 4: Common modifications and potential problems
- Modifications
  - Removing a route
  - Changing the Bank Eaters/Feeders
  - Adding a route
  - Anomaly consumption spike
- Limitations
  - Filter hierarchy
  - TWC education
- Q&A

Figure 39: DOI Scheduler Class: Agenda slide

Appendix I: DOI Scheduler Game

To educate the floor technicians on the overall Test Wafer material flow and illustrate the improved performance of the DOI Scheduler, a game interface was developed. In this, the players pick cards which randomly contain the number of Test Wafer lots to be consumed and scrapped per day. Each turn corresponds to one day. An Excel based simulation model graphically shows the Test Wafer health for this example route. Each game is different due to the random shuffling of the cards. Total Test Wafer inventory levels, Test Wafer availability, and material location can all be observed.

The Excel simulation model can also be run independent of the game to understand how the DOI Scheduler system would respond to any numerous scenarios.
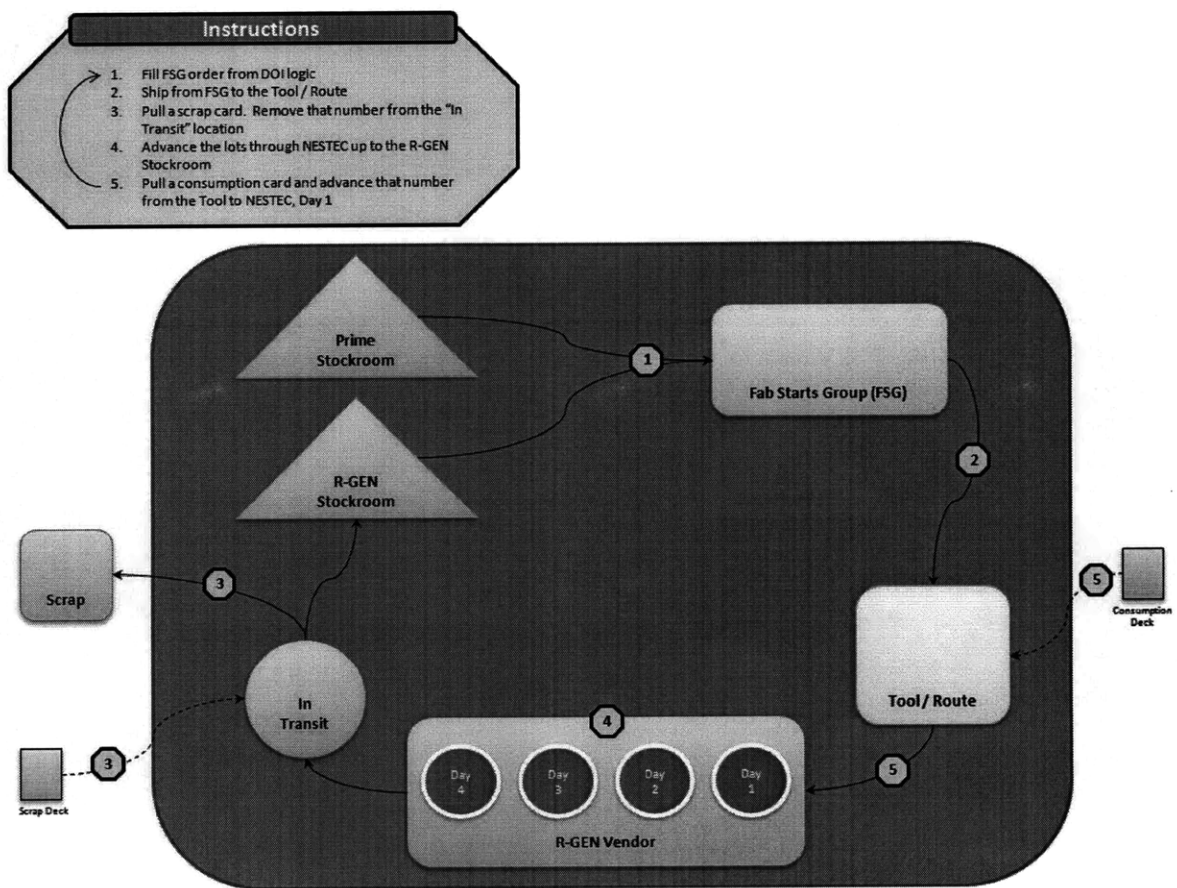

Figure 40: DOI board game

Time Period (days)	FSG Decisions		Game Inputs	
	Prime Stock Room	R-GEN Stock Room	Daily Consumption at Tool (lots/day)	Scrap qty
0	0	9	3	1
1	0	0	3	1
2	0	0	5	1
3	0	10	8	2
4	0	1	12	2
5	15	1	9	2
6	17	1	9	3
7	0	0	7	3
8	18	2	9	3
9	0	5	9	3
10	0	9	1	3
11	0	6	1	3
12	0	0	3	3
13	0	0	2	3
14	0	0	3	3
15	0	0	1	3
16	0	0	2	3
17	0	0	1	3
18	0	0	2	3
19	0	0	1	3
20	0	0	1	3

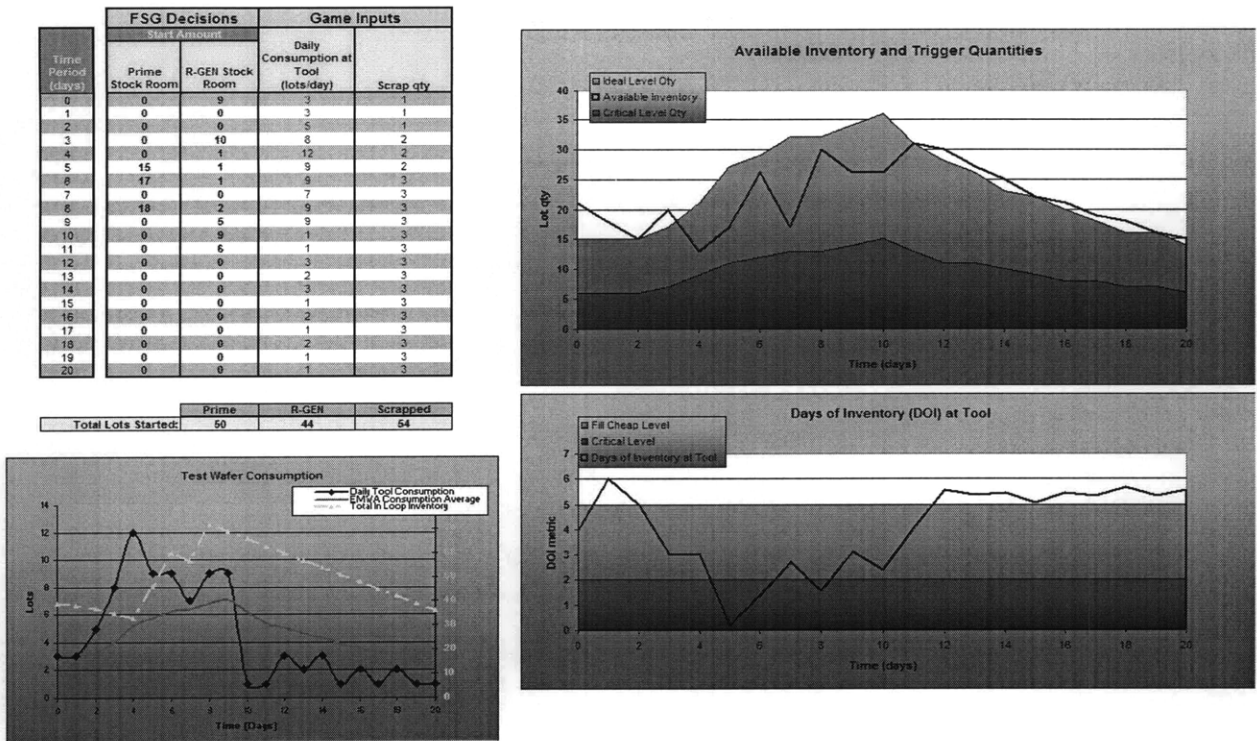|	Prime	R-GEN	Scrapped
Total Lots Started:	50	44	54

Figure 41: DOI Excel simulation supporting the DOI board game

APPENDIX J: DETAILED LITERATURE REVIEW

Journals and Industry Papers:

Title: Test Wafer Management for Semiconductor Manufacturing
Authors: Ozelkan, Ertunda & Cakanyildirim, Metin
Publication date: May 2006, IEEE
Applicability summary: This paper develops a theory which deduces which Test Wafers can be downgraded to a cheaper re-use type. This downgraded type can still meet some route base requirement characteristics and would be used instead of previously rejecting them as scrap.

Title: Capacity Forecast Model for Control and Dummy Wafers
Authors: Chuen-Shiun Liou, TK Lin, Bruce Tu, Alan Chang
Publication date: 2005, IEEE
Applicability summary: This paper develops a theory for capacity planning and forecasting of Test Wafer needs based upon the number of tools and usage constraints. This approach was used as an example different than the EMWA forecast analysis used in the DOI Scheduler program as a reference on what characteristics to consider.

Title: Manufacturing Efficiency Improvement through Automation of Test Wafer Procedures
Authors: Patrick Ferland & Andre Labonte
Publication date: 2004, IEEE
Applicability summary: This paper discusses an automation system used to improve Test Wafer processes through improved standardized, improved visual controls, and increased automated flow controls.

Title: Pull System for Control and Dummy Wafers
Authors: H.C. Chen, C-E. C. Lee
Publication date: 2003, Journal of Advanced Manufacturing Technologies
Applicability summary: This paper describes a proposed pull system focusing on inventory levels and managing the downgrading of control and dummy wafers. Savings include WIP reduction, increase recycle usage, and reduced downtime related to waiting for wafers.

LFM Theses:

Title: Minimizing the Risk Qualification Test Wafers have on the Manufacturing Readiness of a New Microprocessor Fabrication Site through Data Driven Processes
Author: Jonathan E. Howe
Publication date: 2001
Applicability summary: Develops three different tools to minimize the risk of Test Wafers not being available or ready for use specifically in new manufacturing facilities within the Intel Corporation. This thesis provided background information on Test Wafer capacity forecasting and background information on developing semiconductor manufacturing sites.

Title: Cost Reduction Methodology and Management
Author: Gary Tarpinian
Publication date: 1999
Applicability summary: Investigates cost reduction approaches within Intel. Test Wafers are specifically identified as a cost group with large saving potentials. A database of information was developed to help identify and assist reduction efforts.

Internal Intel Sources:

Title: Dynamic Inventory Management for Test Wafers
Author: Gleeson, Frank J. & Smith, Cathal T.
Publication date: 2008
Applicability summary: This paper discusses a TW control system based upon a Days of Inventory metric used at Fab-24. Many of these principles were the building blocks for the DOI Scheduler program developed for this thesis. Major differences existed in the consumption and forecast data as Fab-24 is an automated 300mm facility with inherent improved measurement capabilities. Additionally, the decision tree using this improved consumption data is also slightly different. This example provides another independent source showing the benefits of a DOI approach instead of a fixed minimum level system as seen previously at Fab-17.

Title: Business Process for Fab-17 Inventory Application
Author: Gogna, Mukesh
Publication date: May 25, 2007
Applicability summary: A previous Intel intern developed the algorithm for an improved Test Wafer business application and interface incorporating usage and visualization tools. This document describes this project and gives good insight into the available information and how it can be used to improve the current state. Budgetary cuts prevented any of this work from actually being implemented.

Other Sources:

Title: Linking the Shop Floor to the Top Floor
Author: Mark Beischel and K. Richard Smith
Publication date: October 1991, Management Accounting Journal
Applicability summary: This article describes the hierarchy of measurements and metric linking front line operations to the plant level performance indicators. This is used as a reference for understanding and recommending additional measurements for understanding Fab-17 health.

Title: Lean Enterprise Value, Insights from MIT's Lean Aerospace Initiative
Author: Earll Murman, Deborah Nightingale, et. al
Publication date: 2002, The Lean Enterprise Value Foundation
Applicability summary: This book was used as an educational reference to the successes of lean activities in the aerospace field. Numerous examples illustrated the principle of eliminating waste with the goal of value creation.

Title: Introduction to Statistical Quality Control
Author: Douglas C. Montgomery
Publication date: 2005, John Wiley & Sons, Inc
Applicability summary: This textbook has a detailed section on the Exponentially Weighted Moving Average (EMWA) and was used as a reference when developing the forecasting approach in the DOI Scheduler program.

Title: Fundamentals of Semiconductor Manufacturing and Process Control
Author: Gary May & Costas Spanos
Publication date: 2006, John Wiley & Sons, Inc
Applicability summary: This textbook describes many of the processes used in semiconductor manufacturing. Specifically, the sections on process modeling and control charts were useful in understanding the metrics and measurements used by Fab-17.