Material Selection and Nanofabrication Techniques for Electronic Photonic Integrated Circuits

by

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ABSTRACT

Electronic-photonic integrated circuits have the potential to circumvent many of the performance bottlenecks of electronics. To achieve the full benefits of integrating photonics with electronics it is generally believed that wavelength-division multiplexing is needed; requiring an integrated optical device capable of multiplexing/demultiplexing operations. One such device is a bank of microring-resonator filters with precisely spaced resonant frequencies.

In this work, a fabrication strategy based on scanning-electron-beam lithography (SEBL) is presented for precisely controlling the resonant frequency of microring-resonator filters. Using this strategy it is possible to achieve dimensional control, on the tens-of-picometer scale, as required for microring-resonator filter banks. To correct for resonant-frequency errors present after fabrication, two forms of postfabrication tuning, one dynamic and one static, are demonstrated. It is also shown that hydrogen silsesquioxane (HSQ) can be converted into a high-quality overcladding for photonic devices by optimizing the annealing process. Finally, a postfabrication technique of localized substrate removal is presented, enabling the integration of photonics with CMOS electronics.

Second-order microring-resonator filter banks were fabricated using SiN_x and Si as the high-index core materials. By controlling the electron-beam-exposure dose it is possible to change the average microring-waveguide width to a precision better than 75 pm, despite the 6 nm SEBL address grid. Using postfabrication tuning the remaining resonant-frequency errors can be reduced to less than 1 GHz. By annealing HSQ in a an O_2 atmosphere using rapid thermal processing, it is possible to create thick overcladding layers that have essentially the same optical properties as SiO_2 with the excellent gap-filling and planarization properties of HSQ. Using XeF_2 to locally etch an underlying Si substrate, waveguides with a propagation loss of ~10 dB/cm were fabricated out of polysilicon deposited on 50 nm of SiO_2.

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Table of Contents

List of Figures

List of Tables

List of Acronyms

3D:	Three-dimensional
ADC:	Analog-to-digital converter
CIFS:	Coupling-induced frequency shifts
CMOS:	Complementary metal-oxide-semiconductor
ENOB:	Effective number of bits
EPIC:	Electronic-photonic integrated circuit
FDTD:	Finite-difference-time-domain
FSR:	Free spectral range
HIC:	High index contrast
HSQ:	Hydrogen silsesquioxane
IC:	Integrated circuit
LER:	Line-edge roughness
LPCVD:	Low-pressure chemical-vapor deposition
PECVD:	Plasma-enhanced chemical-vapor deposition
PMMA:	Poly-methyl-methacrylate
Q:	Quality factor
RIE:	Reactive-ion etching
SEBL:	Scanning-electron-beam lithography
SOI:	Silicon-on-insulator
WDM:	Wavelength-division multiplexing

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I would also like to thank Franz X. Kaertner, from whom I have learned many details about integrated optical systems and femtosecond lasers during our weekly EPIC meetings.

Lastly, I would like to thank my friends, family and my wife. They have been a constant source of support throughout my entire graduate career.

Chapter 1

Introduction

Since the fabrication of the first electronic integrated-circuit (IC) there has been a constant drive to make ICs faster, smaller, cheaper, and more energy efficient. This was famously stated in the paper by Gordon E. Moore in 1965 where he predicted the number of components in an integrated circuit, and the density at minimum cost per transistor, would double approximately every two years [1]. This prediction became known as Moore's Law, and although it originally applied to the density of transistors in an IC it is now often used to describe the doubling of computing power every two years. Until recently, this trend has mainly relied on the shrinking or scaling of the transistor size, which enables an increase in speed and density. Some ICs, such as processors, are closing in on the fundamental limits of size scaling, where currently the transistor gate length is ~20 nm [2]. This is forcing processor manufacturers to move to a multicore platform, allowing them to maintain this doubling of computer performance through parallelism. However, this approach has its limitations due to the core-to-DRAM and core-to-core data transfer rate bottlenecks [3]. For other systems, such as high-speed analog-to-digital converters, improving speed through dimensional scaling is not sufficient to improve performance. Currently, the sampling resolution of electronic

analog-to-digital converters is limited by the timing jitter of the electronic clock, not the speed of the individual transistors [4]. These two examples demonstrate that dimensional scaling is no longer the answer for achieving higher performance ICs; a new solution is called for.

One such solution is to integrate photonic devices with electronic devices. The history of the telecommunications industry makes is evident that this is not a far-fetched idea. Telecommunication, a word derived from the Greek prefix *tele-* meaning "far off" and the Latin *communicare* meaning "to share", describes the transmission of signals over long distances for the sake of communication. From 1837, when the electric telegraph was invented, until the late 1980s the telecommunications infrastructure was dominated by electronic cables. The laying of the first fiber-optic transatlantic cable in 1988 changed this, causing the rapid replacement of long-haul electric cables with fiber optics, taking advantage of their enormous increase in data capacity [5]. This increase in data capacity can also be used to solve the data-transfer bottleneck in multicore processors by replacing some of the electronics with photonics. Also, by integrating photonics with electronics one can take advantage of ultra-low-noise optical sources. For example, the timing jitter of a femtosecond laser is more than two orders of magnitude lower than current state-of-the-art on-chip electronic oscillators. Jitter currently limits the performance of ultra-fast analog-to-digital converters [6]. These are just two examples of the many ways photonics can be combined with electronics in a synergistic manner to form an electronic-photonic integrated circuit (EPIC) that surpasses current performance limitations of electronic ICs.

Although certain photonic devices are already being used heavily in telecommunication systems, they can not be easily integrated with electronic ICs. This is because the photonic devices used in telecommunication are relatively large, low-index-contrast discrete components that are made using materials and fabrication methods that are not CMOS compatible. To monolithically integrate photonics with electronic ICs, a switch from the low-index-contrast and III-V material systems of the telecommunications industry to a high-index-contrast (HIC) CMOS-compatible material system must be made. This would enable a decrease in size, with the added benefit of using CMOS compatible fabrication tools. For seamless integration it is also important to develop a fabrication process for integrated photonics that involves minimal customization of the IC fabrication process.

The switch from low-index-contrast to HIC materials is not trivial. Both the design and fabrication challenges increase rapidly as the index contrast increases. The analytic design tools developed for low-index-contrast photonics do not work adequately for HIC devices, requiring the use of rigorous three-dimensional finite-difference time-domain simulations [7]. Likewise, the fabrication challenges for HIC photonic devices are immense. The propagation loss from sidewall roughness scales with the index contrast squared, requiring ultra-smooth sidewalls for HIC devices. Also, for resonant structures such as microring filters, dimensional precision on the nanometer to tens of picometer level is essential for optimal performance. There are also challenges in integrating HIC photonics with electronics since photonic devices require a thick (>1 μm) low-index undercladding layer, which is currently prohibited in high-performance ICs due to thermal constraints.

In this thesis, I address some of the challenges in fabricating CMOS-compatible photonic devices and integrating them with current IC process flows. The main focus will be on the basic architecture and fabrication of filter banks consisting of optical microring-resonators, thought by many to be the basic building block of integrated photonic systems. This will include material selection, means of achieving resonant frequency control without post-fabrication tuning, and post-fabrication tuning methods. Also, a novel fabrication method will be presented that enables the transparent integration of photonic devices with electronic ICs.

This thesis is separated into two main parts. Part I will focus on the fabrication of microring-resonator filter banks that can be used as multiplex/demultiplex devices for EPIC systems. To achieve the resonant-frequency-spacing precision required for these devices, dimensional control on the *tens of picometer scale is required*, which we demonstrate using a novel scanning-electron-beam lithography (SEBL) technique. Also presented, are two forms of post-fabrication tuning, one dynamic and one static, to correct any resonant frequency errors in the filter bank. Using these methods some of the most advanced microring resonator filters and filter banks have been fabricated.

Part II focuses on supporting techniques for the fabrication of EPICs. This includes an optimized annealing technique that allows the use of a spin-on glass to form a high quality overcladding layer for photonic devices. Another supporting technology is a postfabrication technique of localized substrate removal to enable the seamless integration of photonic devices with electronics in a commercial CMOS line.

PART I

Microring-Resonators Filters and Filter Banks

Chapter 2

Background

2.1 ELECTRONIC-PHOTONIC INTEGRATED CIRCUITS

Advances in HIC photonics have enabled increasingly complex EPICs to be designed and fabricated. Examples of these circuits include: ultrafast analog-to-digital converters, optical interconnects for multicore processors, and fiber-optic transceivers [3,6,8]. The photonic components that comprise EPICs typically fall into one of four categories; waveguides, modulators, filters, and detectors (assuming that the light source will not be integrated monolithically). The goal of EPICs is to integrate these basic photonic building blocks with electronic circuits in a synergistic manner to achieve better performance than in current electronic ICs.

Waveguides are the most basic photonic component, and are used to transport light from one point to another. All other photonic structures are comprised of waveguides in one way or another. The most important characteristic of a waveguides is its propagation loss. The loss consists of a material-dependent term (material absorption) and a fabrication-dependent term (typically scattering from sidewall roughness). Propagation loss will determine the overall efficiency of a photonic device, and for most systems should be 3 dB/cm or less. Other important characteristics are index contrast and the confinement factor of the optical mode. These properties determine the minimum

radius of curvature a waveguide can have before incurring excess bending loss. This is important because the minimum bending radius will ultimately determine how densely photonic devices can be integrated.

The next photonic component, optical modulators, have the role of transforming electrical signals into optical signals. This is typically done by changing either the phase or the magnitude of light. Broadband modulators (> 100 GHz) are typically based on a Mach-Zehnder interferometer and use either carrier injection or heating to change the optical path length between the two arms [9]. This changes the interference at the output of the modulator resulting in an amplitude change. Narrowband modulators (<100 GHz), on the other hand, are typically based on resonant structures such as microrings [10]. Here again, either carrier injection or heating is used to change the optical path length of the device. This results in a change in the resonant frequency, allowing one to modulate the magnitude of the signal. The two important figures of merit for a modulator are the speed at which it can modulate, and the energy consumed per bit. Carrier-injection-based modulators are both faster and more energy efficient then thermal ones so they are preferred [11].

Optical filters are used to separate signals carried on different wavelengths. It is generally agreed that in order to maximize the value of integrating photonics with electronics, wavelength-division multiplexing (WDM), (transporting multiple optical signals through a single waveguide on different wavelengths) must be used [12]. This creates the need for filters to separate the signals (demultiplex) and combine them (multiplex). This filtering function can be achieved using a bank of microring resonators that have resonant frequencies corresponding to the wavelengths of the various signals.

In HIC material systems, such as silicon-on insulator, these microring resonators can have radii as small as 1.5 μm, making them ideal for integration [13].

The fourth basic photonic building block, detectors, transform optical signals into electrical signals. Detectors are photodiodes made from Ge, SiGe, and ion implanted Si [14,15,16]. The photodiode material is chosen so that it can efficiently absorb the incoming photon, resulting in the excitation of electron-hole pairs. This creates a photocurrent that is dependent on the flux of the incoming light. A few important characteristics of photodiodes are their detection efficiency and speed. Detection efficiency relates the number of incoming photons to the resulting photocurrent. The speed of a photodiode depends on the how quickly the excited electron-hole pairs can exit the photodiode.

These basic photonic building blocks, when combined with an external light source (laser) and integrated with electronic circuits can, overcome performance bottlenecks that limits analogous electronics-only systems. Two systems that provide a great example of the possible synergy between photonics and electronics are an electron-photonic ultra-fast analog-to-digital converter and an optical many-core processor-to-DRAM network. Both systems address current limitations in integrated electronic circuits by replacing certain parts of the system with photonics, resulting in an increase in performance of more than an order of magnitude. By monolithically integrating photonics with electronics this large performance increase can be achieved without an associated large increase in cost.

2.1.1 Ultra-Fast Analog-to-Digital Converters

With advances in CMOS technologies and parallel-computing architecture, teraflop processor systems are now a reality [17]. The true benefits of these systems can not be fully realized at present due to the limitations of analog-to-digital converters (ADC). The effective number-of-bits (ENOB) versus input signal frequency for existing ADCs, shown in Fig. 2.1, clearly illustrates how the performance of electronic ADCs are fundamentally limited by the timing jitter of the electronic clocking circuits, and the jitter performance of electronic oscillators. State-of-the-art on-chip electronic oscillators currently have a timing jitter of ~100 fs, limiting the sampling resolution of a 20 GHz

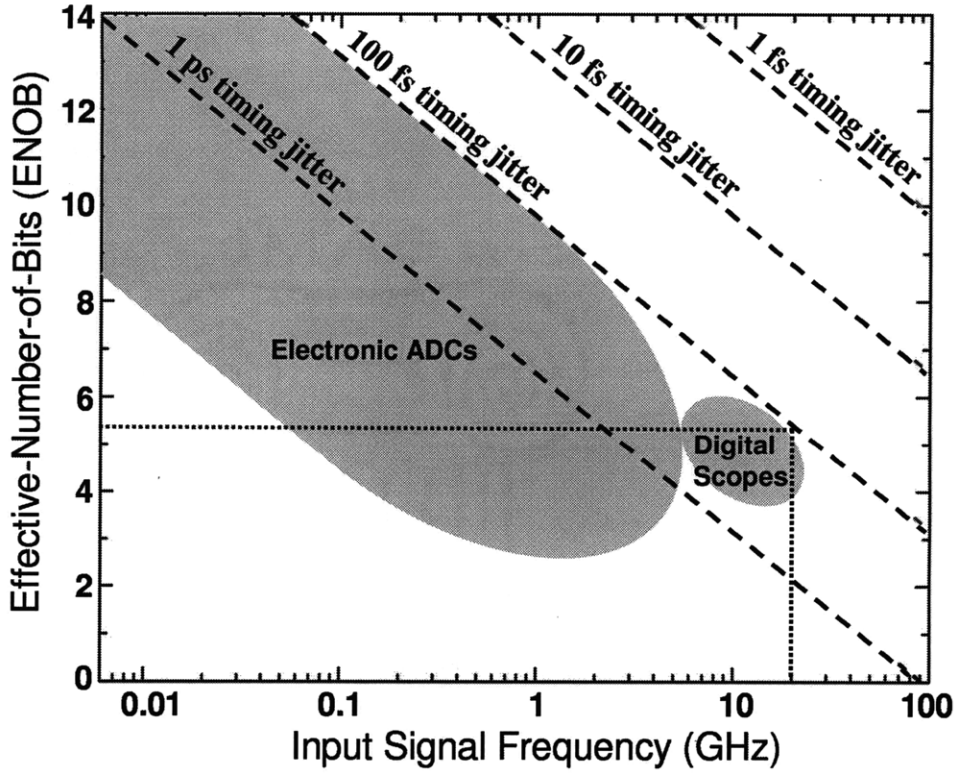


Fig. 2.1: Performance plot for modern electronic analog-to-digital converters showing how the 100 fs timing jitter of electronic circuits limits the resolution achievable for a given signal frequency

analog signal to ~5 ENOB. To increase the sampling resolution to > 6 ENOB for microwave signals a different low-timing-jitter source most be used, such as a femtosecond laser.

Femtosecond lasers have been shown to be very-low-noise sources, with timing jitter of ~10 fs or below [6,18]. The timing jitter of electronic oscillators, dominated by thermal noise (kT), is proportional to the square of the oscillation period (T_0) (Eq. 2.1). This period is on the order of ~100 ps for a ~10 GHz microwave signal. In contrast, the dominant source of timing jitter for mode-locked femtosecond lasers is quantum noise ($\hbar\omega_c$) and is proportional to the square of the pulse width (τ), which is on the order of ~100 fs (Eq. 2.2). This six order of magnitude difference between the square of the pulse width and oscillation period easily overcomes the fact that the quantum noise is significantly larger than the thermal noise (Eq. 2.3). The end result is that femtosecond lasers have a timing-jitter improvement of greater than two orders of magnitude relative to electronic oscillators (Eq. 2.4). This creates the potential of sampling 20 GHz analog signals at a resolution of 10 ENOB.

$$\frac{d}{dt}<\Delta t_{RF}^2>\sim T_0^2\cdot\frac{2}{E_{mode}}\frac{kT}{\tau_{cav}} \qquad \textbf{2.1}$$

$$\frac{d}{dt}<\Delta t_{ML}^2>\sim \tau^2\cdot\frac{2}{E_{pulse}}\frac{\hbar\omega_c}{\tau_{cav}} \qquad \textbf{2.2}$$

$$\hbar\omega_c \sim 50kT \qquad \textbf{2.3}$$

$$\frac{d}{dt}<\Delta t_{ML}^2> \; > 10^2 * \frac{d}{dt}<\Delta t_{RF}^2> \qquad \textbf{2.4}$$

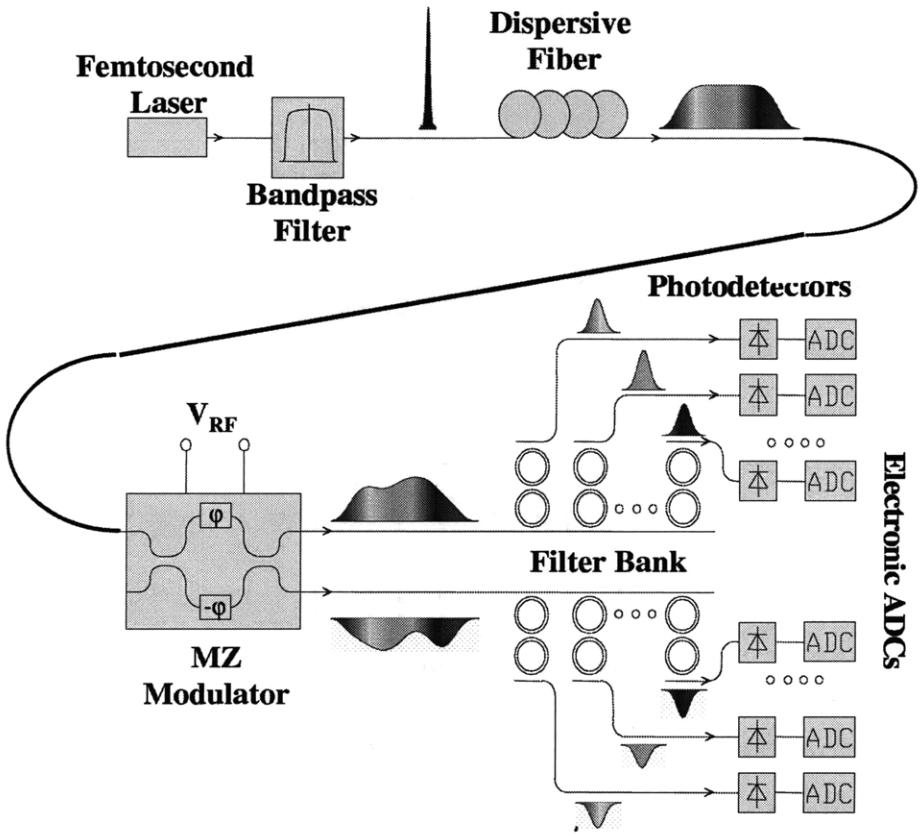


Fig. 2.2: Proposed electronic-photonic ultra-fast analog-to-digital converter capable of >8 ENOB for a 20 GHz input signals. Key photonic components include a low-jitter femtosecond laser, broadband modulator and filter bank.

In order to take advantaged of the low jitter of a femtosecond laser the analog signal must be processed with photonics before being digitized by electronic ADCs. Fig. 2.2 shows a proposed electronic-photonic ultra-fast ADC that takes advantage of the low timing jitter of a femtosecond laser, WDM architecture, and the high resolution of "slower" electronic ADCs, to sample a 20 GHz signal at >8 ENOB. This system starts with a mode-locked femtosecond laser emitting broadband optical pulses at a 2 GHz repetition rate. This broadband pulse then travels through a dispersive fiber that stretches the frequency spectrum in time. The spectrum then travels through a Mach-Zehnder

modulator where the input voltage (V_{RF}) is the 20 GHz analog signal to be sampled. The modulator will imprint the analog signal as an amplitude modulation on the broadband spectrum, effectively converting the analog signal from the time domain to the frequency domain. The spectrum is then demultiplexed into N channels using a bank of microring-resonator filters with precisely spaced resonant frequencies. Each channel is then incident onto a photodetector converting the optical signal into an electrical signal. The electrical signals from the photodetectors are then digitized in parallel by "slower" high-resolution electronic ADCs. The demultiplexing of the signal allows for each frequency to be processed electronically in parallel, therefore the electronic ADCs only need to be as fast as the repetition rate of the laser (2 GHz) not the frequency of the signal (20 GHz). An added benefit of this system is that the complementary output of the modulator can also be demultiplexed and digitized to cancel nonlinearities in the system. The total sampling speed of the system is the repetition rate of the femtosecond laser multiplied by the number of channels in the filter bank.

2.1.2 Many-Core Processor-to-DRAM Networks

The new trend for increasing the performance of processors is to increase the number of cores. In order to maintain the pace of processor performance increase dictated by Moore's Law, these multi-core processors will soon become many-core processors, where the number of cores will be in the hundreds to thousands. One of the greatest problems facing many-core systems is that as the number of cores increases there is a corresponding increase in the memory bandwidth requirements. Without this

increase in bandwidth the increase in number of cores will not result in improved application performance. The ideal solution to this problem must provide the increased memory bandwidth with reasonable power consumption and packaging costs.

One proposed solution is to use monolithic silicon photonic to create an electro-optic global crossbar. Fig. 2.3 shows the schematic of a theoretical system containing 256 cores, 16 DRAM modules, and 16 group electro-optic crossbars. The system takes advantage of dense WDM, allowing single waveguides to carry up 128 signals utilizing 64 wavelengths of light it each direction. As the number of cores increases it is necessary to increase the number of wavelengths to achieve functional scaling, keeping the photonic footprint minimal. To rout a signal from a specific core to the desired DRAM module a network of microring resonator filter banks is used. Microring resonators are

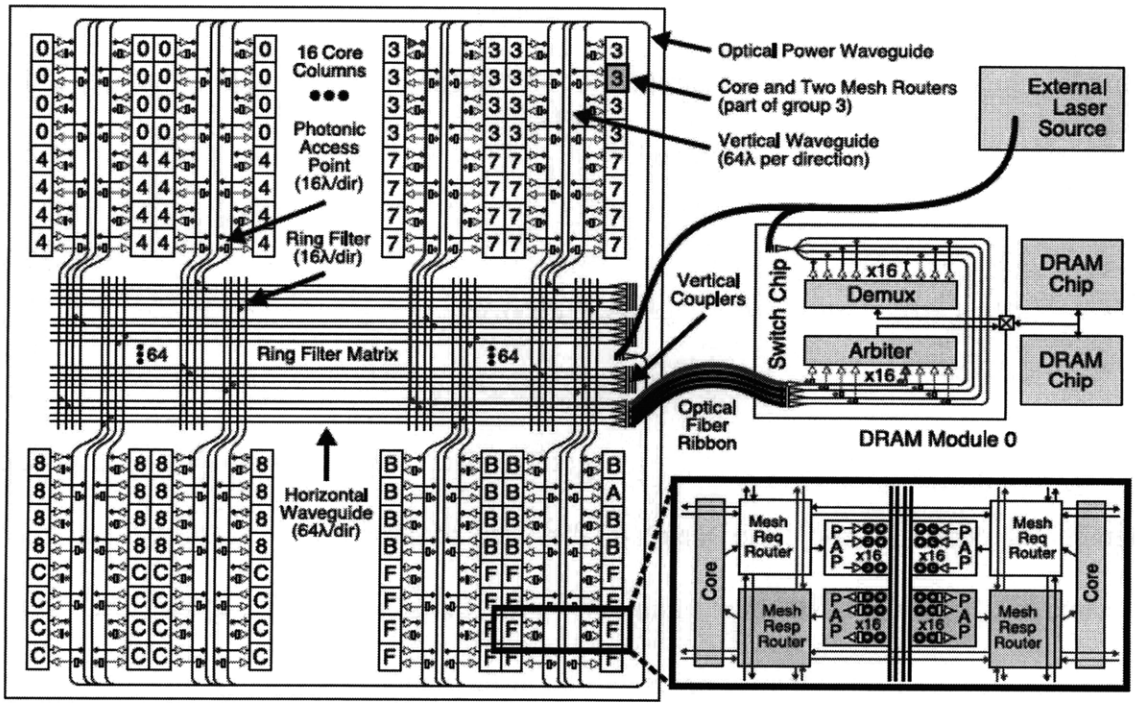


Fig. 2.3: Schematic of a proposed manycore-to-DRAM network consisting of 256 cores, 16 DRAM modules, and 16 group opto-crossbars. Each ring in the left image represents a bank of 16 second-order microring-resonator filters.

also used as modulators in this system to encode the bit signals onto each wavelength of light individually. The figure of merit, energy per bit, for this system is ~250 fJ/bit about a 20X improvement over electronic-only systems [3].

2.2 MICRORING RESONATOR OPTICAL FILTERS

As is evident in the two examples of EPICs described above, microring resonators are essential photonic components. In addition to filtering, it is possible to make switches, narrowband modulators, delay lines, and slow-light structures out of microring resonators. In many ways improving the performance of microring resonators is as essential to the future of integrated photonics as improvements in the transistor were, and still are, to integrated electronics. Also, similarly to the transistor, material properties and fabrication methods for microring resonators need to continuously improve to keep up with the need for higher performance in increasingly demanding applications.

2.2.1 General Operation

The theory for microring resonator filters was first developed in 1969, but it was not until the late 1990s that advances in fabrication methods made these devices feasible [19,20]. A single microring resonator coupled to two waveguides, W_1 and W_2, is depicted in Fig. 2.4a, with multiple signals carried by different wavelengths traveling through W_1. These wavelengths will evanescently couple to the nearby microring with to W_2, transferring the signal to W_2. This is how a microring resonator can filter out a

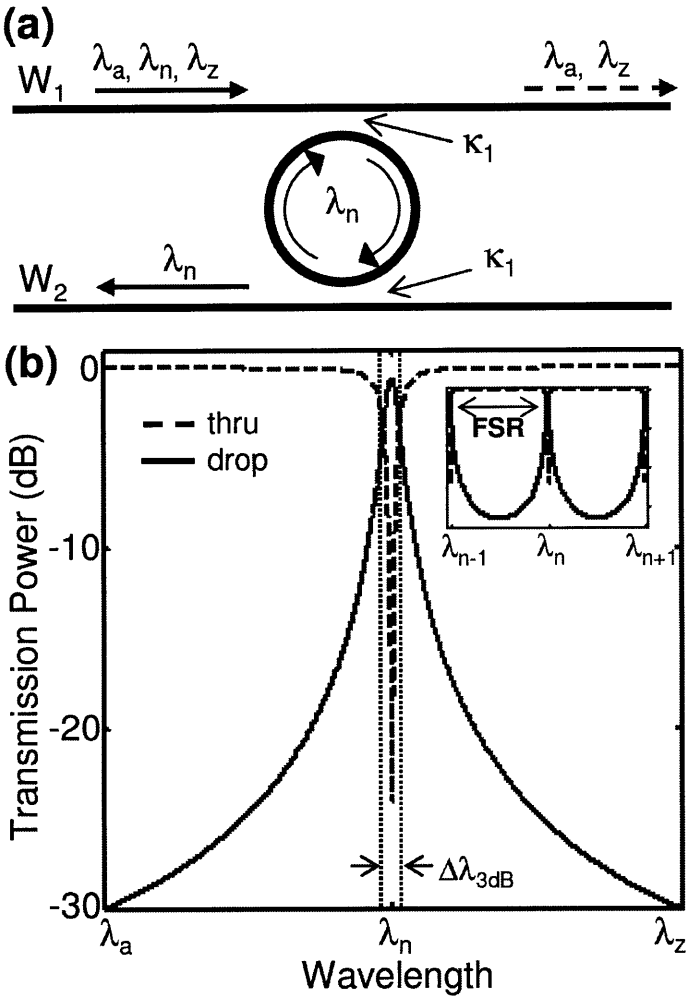


Fig. 2.4: (a) Top-view diagram of a single microring acting as a drop filter. (b) Simulated transmission response of a single microring filter.

coupling strength κ_1. Each time a wavelength evanescently couples from a waveguide to a microring its relative phase is shifted by 90 degrees. Therefore, for wavelengths, λ_n, that satisfies the resonant condition in Eq. 2.5, the light will be 180 degrees out of phase with respect to the light in W_1 when evanescently coupling back into W_1, resulting in deconstructive interference. This results in the coupling to the microring being enhanced for λ_n and suppressed for all other wavelengths. The signal carried by λ_n is thus transferred from W_1 to the microring. Once in the microring, λ_n will evanescently couple

signal carried on W_1 and transfer it to W_2. The operation of the microring resonator is, of course, time reversible; hence a signal carried by λ_n on W_2 can be added to the signals traveling in W_1. This is how a microring resonator can be used as an optical add-drop filter.

$$m^*\lambda_n = 2\pi R^* n_{eff} \qquad \textbf{2.5}$$

The frequency-transmission function for a single microring resonator is shown in Fig. 2.4b. The key parameters of the transmission response are the 3 dB bandwidth ($\Delta\lambda_{3db}$), quality factor (Q), free spectral range (FSR), finesse, drop loss, and roll-off. $\Delta\lambda_{3db}$ is the full-width half maximum of the transmission response and is dependent on the coupling coefficients (κ) between the microring and the waveguides. The Q of a microring is a measure of the filters selectivity, where $Q=\lambda/\Delta\lambda_{3db}$, and is an inverse sum of the internal and external Qs. The external Q is a measure of the power loss due to evanescent coupling to external photonic structures such as waveguides or other microrings. The internal Q is a measure of the power loss to internal factors such as material absorption, radiation scattering losses, and bending loss. The internal Q sets a lower limit on the achievable bandwidth of the transmission response. The FSR is defined as the spectral range between adjacent resonant frequencies of the same microring filter. This range typically defines the maximum usable frequency spectrum for the photonic systems. The FSR is typically increased by reducing the microring radius but can also be increased artificially through the Vernier effect or by using two-point coupling to suppress some of the resonances [21,22]. The finesse of a filter is defined by the FSR/ $\Delta\lambda_{3db}$ and is another way to measure the selectivity of the filter. The

drop-loss is a measure of how much of the incoming signal at the resonant frequency is not transferred to the drop waveguide. For most applications it is desirable for the drop loss to be < 3 dB. Roll-off is a measure of how quickly the transmission response decays outside the 3 dB bandwidth. The roll-off can be increased by increasing the order of the filter, i.e. coupling multiple microrings in series. Fig. 2.5a shows the schematic of a second-order filter consisting of two series-coupled microrings. Fig. 2.5b illustrates the increase in roll-off of the transmission response that is obtained when the filter order is increased.

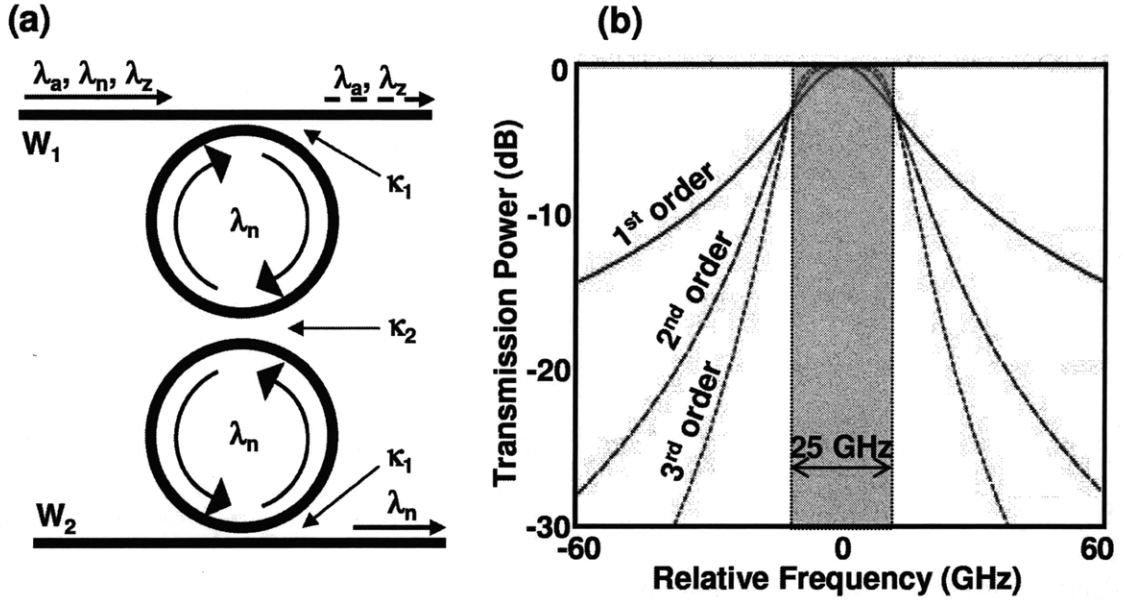


Fig. 2.5: (a) schematic of a second-order microring filter. (b) Simulated transmission response of first-, second, and third-order microring-resonator filters all with the same bandwidth, demonstrating the increase in role-off as filter order is increased.

2.2.2 Material Selection and Fabrication Challenges

To improve the performance of microring-resonator filters it is desirable to move to higher-index-contrast materials while keeping propagation loss minimal. Early microrings-resonators were fabricated using doped glass, providing very low index

contrast, and limiting the bending radius to hundreds of microns [23]. Moving to higher index contrast allows for smaller bending radii without excess bending loss. This has a two-fold benefit of increasing the FSR of the microring and reducing the overall footprint of the device. It has been shown that in silicon-on-insulator it is possible to fabricated microrings filters that have a radius of only 1.5 μm, and a FSR of over 6 THz, without incurring a prohibitive amount of bending loss [13].

As one moves to higher-index-contrast material systems to improve filter performance the fabrication challenges increase dramatically. Propagation loss due to scattering from sidewall roughness scales with the index contrast squared. Therefore, to maintain the same drop loss when switching to higher index contrast the sidewall roughness must be significantly reduced. Also the resonant frequency sensitivity due to small dimensional changes in the average microring waveguide width and height increases substantially with index contrast. For example, for a microring resonator filter with Si as the core and SiO_2 as the cladding, and using the nominal waveguide cross section of 220 nm X 400 nm, the resonant frequency shifts approximately 100 GHz for every 1 nm change in average microring width. In addition to these increased sensitivities, the higher confinement of HIC materials systems means that the evanescent field of the optical mode does not extend very far from the waveguide core. Therefore, to achieve significant coupling to the microring resonator the gap between the waveguide and the microring must be a few hundreds of nanometers, or less. All of these factors mean that moving to higher index contrast results in the need for the development of fabrication methods that are optimized for the specific needs of photonic structures.

Chapter 3

Fabrication of Microring-Resonators

3.1 INTRODUCTION

The challenges in fabricating integrated photonics devices are often very different than those of electronic circuits; however, people often try to make use of the same techniques for both. This approach has a number of limitations. For integrated photonics to be successful new fabrication techniques must be developed. Microring-resonator filters are a prime example on how the fabrication requirements differ substantially from those of integrated electronic circuits. For example, one of the important fabrication challenges of a transistor is scaling the size to make it faster, cheaper and consume less power. Today the transistor gate length is ~20 nm but it can vary by as much as 10% from transistor to transistor on the same chip, this is not a problem for electronics [2]. On the other hand, all of the features of microring resonators are larger than 20 nm, generally much larger than 100 nm, but they require dimensional control of 2% or better, and dimensional precision on the tens of picometer scale. A second example is that electronics are laid out using so-called Manhattan geometries, and current optical-lithography tools exploit this fact with "resolution-enhancement techniques" such as dipole and quadrupole illumination [24]. In contrast, microrings and many other photonic structures rely on

smoothly varying, curved structures, and many of the resolution-enhancement techniques used for Manhattan geometries sacrifice the quality of curved and off-axis features. These are just two of the many differences in the challenges for fabricating integrated photonics compared to integrated electronics.

To overcome these challenges each step of the fabrication process has been optimized for the fabrication of microring-resonator filters while still utilizing some of the same tools that have been developed primarily for the semiconductor industry. During the experiments, two different types of filters were fabricated one using silicon-rich silicon nitride (SiN_x) (n=2.19 @ 1550 nm) and the other using crystalline silicon (n=3.52 @ 1550 nm) as the core material. Scanning-electron-beam lithography (SEBL) with an optimized writing strategy was used to define the features in an electron-beam resist. The rest of the process optimizations included electron-beam resist choice, exposure dose, etch mask material, and etching recipes.

3.2 SILICON-RICH SILICON NITRIDE FILTERS

Silicon-rich silicon nitride (SiN_x) is also commonly known as low-stress nitride and is widely used in the fabrication of membrane-based and MEMS devices. The reason that it is chosen as the core material for these experiments over stoichiometric silicon nitride (Si_3N_4) is two fold. First, stoichiometric Si_3N_4 deposited using low-pressure chemical-vapor deposition (LPCVD) is highly stressed, limiting its maximum thickness to ~300 nm. This combined with its lower index of refraction (n=1.98 @ 1550 nm) limits the achievable FSR to ~1 THz, making it unsuitable for most EPIC systems. Si_3N_4 made

using plasma-enhanced chemical-vapor deposition (PECVD), where the stress can be controlled allowing for thicker films and slightly larger FSR, contains a large amount of N-H bonds that cause significant optical absorption around 1520 nm. These problems are not present in SiN_x because it is produced using LPCVD at high temperature with a very slow deposition rate (~1nm/min), allowing all N-H bonds to anneal out during deposition. Its stoichiometery is controlled to minimize internal stress, which enables thicker films to

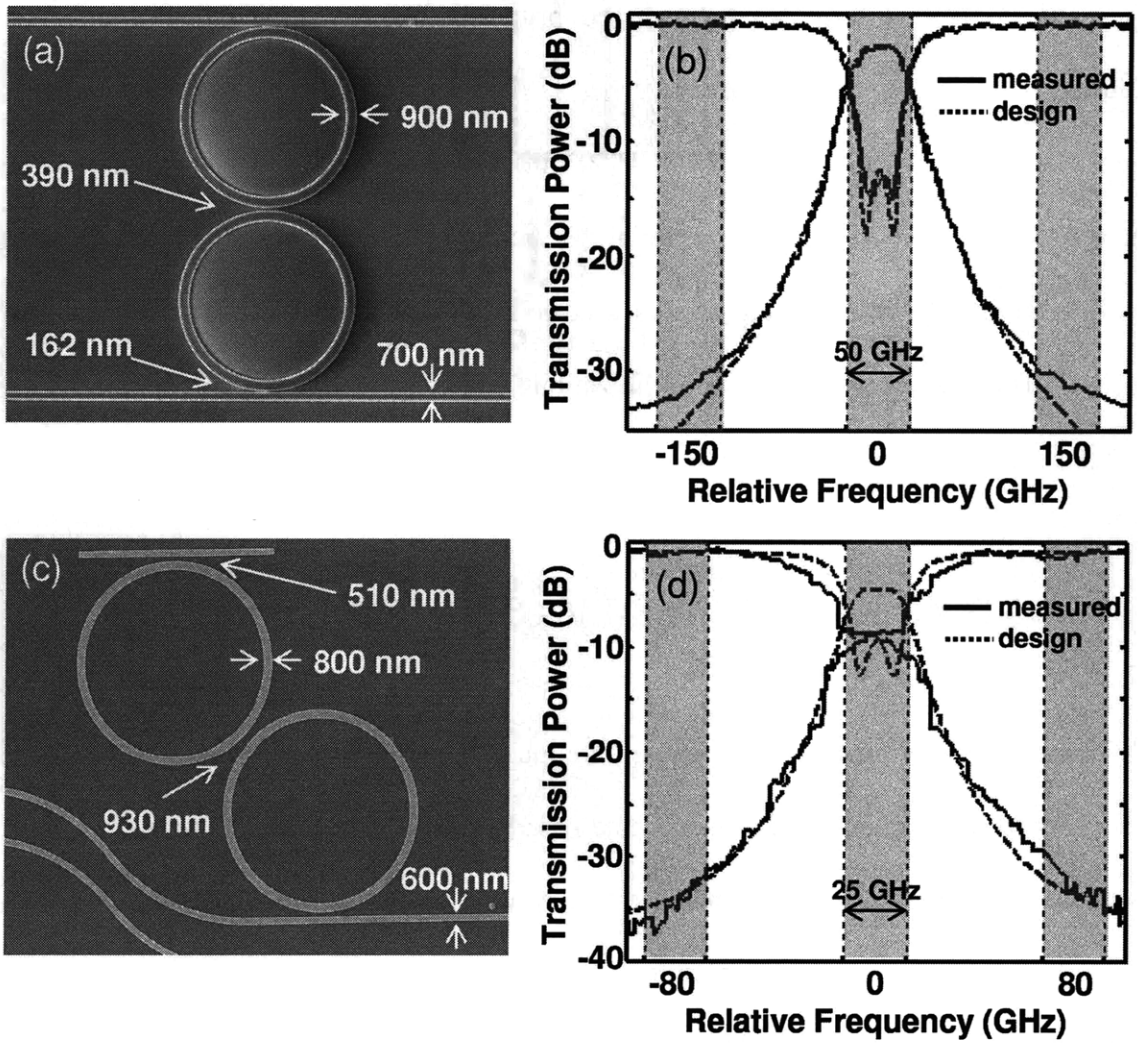


Fig 3.1: (a) Top-view scanning-electron micrograph of fabricated air-clad SiN_x filter design. (b) Designed and measured transmission response of air-clad filter. (c) Top-view scanning-electron micrograph of fabricated oxide-clad SiN_x filter design before cladding. (d) Designed and measured transmission response of oxide-clad filter.

be grown. When combined with its higher index of refraction of 2.19 at 1550 nm FSRs greater than 2 THz can be achieved.

Fig. 3.1 shows two different SiN_x filters as well as their designed and measured transmission responses. These designs were created by Milos Popovic and Anatoly Khilo using rigorous numerical eigenmode and 3D finite-difference time-domain (FDTD) simulations [25]. The first filter design is a second-order air-clad microring-resonator filter with a designed FSR of 2.5 THz and a 3 dB bandwidth of 50 GHz. The second design is a second-order oxide-clad microring-resonator filters with a designed FSR of 2.0 THz and 3 dB bandwidth of 25 GHz. The reason for using second-order microring resonator filters is further discussed in Chapter 6.

The filter designs assume a propagation loss of 7.5 dB/cm, which was calculated by measuring the transmitted powers through so-called "paperclip" structures of different lengths, as explained in Appendix A. The designed and measured transmission responses agree very well for the air-clad design, indicating that the actual fabricated dimensions and propagation loss are very close to the design. The measured transmission response of oxide-clad filter, on the other hand, does not match perfectly with the design. The measured response has both a wider 3 dB bandwidth and a larger drop loss than expected. This combination of differences can only be explained by a larger propagation loss than expected. The SiN_x films used for the two fabrications were deposited by the same tool but over 3 years apart. Although the stress of the deposited SiN_x is measured often to confirm low-stress, the optical properties are not monitored and are found to change significantly over long periods of time, as observed here.

3.2.1 SiN_x Filter Fabrication with PMMA

Poly(methyl methacrylate) (PMMA) was chosen as the electron-beam resist for the fabrication of SiN_x microring resonators because of its high contrast and process reliability. The fabrication process shown in Fig. 3.2 starts by growing a 3 μm-thick thermal-oxide layer on a silicon wafer. Next 400 nm of SiN_x is deposited using LPCVD at a temperature of 700°C. The low deposition rate, ~1 nm/min, of the nitride combined with the high processing temperature results in a nitride film that does not contain any Si-

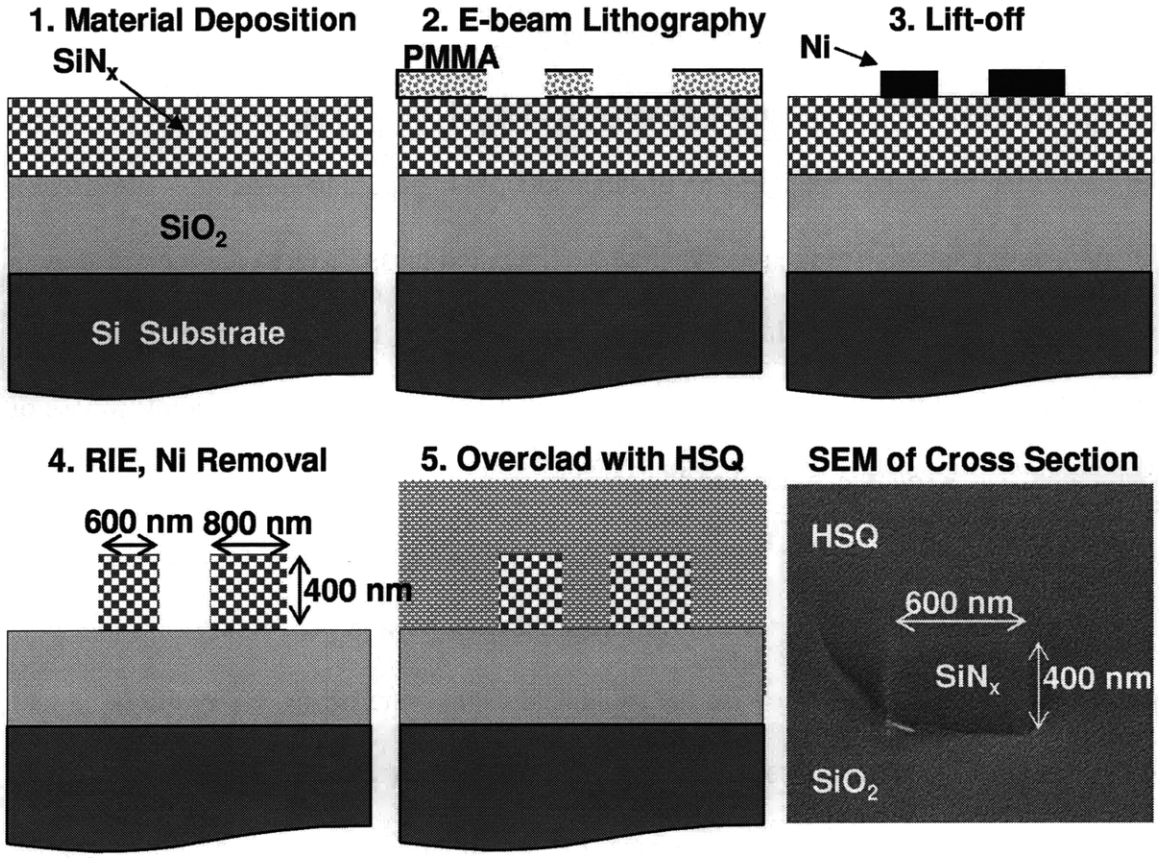


Fig. 3.2: Basic fabrication process for SiN_x filters, using PMMA and lift-off. A scanning-electron micrograph of a fabricated waveguide cross-section is shown in the bottom right image

H and N-H bonds. Next 200 nm of PMMA is spun on the wafer using a spin speed of 4500 rpm and baked in a convection oven at 180°C for 1 hr. Then a 60 nm-thick layer of AquaSAVE, a conducting polymer made by Mitsubishi Rayon, is spun on and baked on a hotplate for 1 min at 90°C. When properly grounded, this conductive layer eliminates charging during SEBL, which can cause beam-placement errors. The SEBL step was performed using a Raith 150 system operating at an accelerating voltage of 30 keV. The exposure dose used was 285 $\mu C/cm^2$ and 333 $\mu C/cm^2$ for the air-clad and oxide-clad designs, respectively. After exposure the AquaSAVE was removed with a rinse in deionized (DI) water. The PMMA was developed by immersing in a solution of 2 parts isopropyl alcohol (IPA) and 1 part methyl isobutyl ketone at 21°C for 60s, followed by immersion in an IPA bath for 60s. The sample was then thoroughly rinsed with IPA and blow dried with a N_2 gun. Next, a 40 nm-thick film of nickel was evaporated on the developed PMMA pattern. Using N-methyl-2-pyrrolidone at 80°C, the remaining PMMA was removed, lifting-off the unwanted nickel and forming a nickel hardmask of the desired pattern. The nickel pattern was then transferred into the SiN_x using a reactive-ion-etching (RIE) process with a CHF_3-O_2 gas mixture, optimized to give smooth vertical sidewalls. For the air-clad design a second RIE step was performed, using CHF_3 gas only, to etch an additional 200 nm into the SiO_2 undercladding layer. After etching, the nickel hardmask was removed using Transene TFB nickel etchant. The samples were then cleaned with a mixture of 5 parts DI water, 1 part H_2O_2 and 1 part NH_4OH at 80°C for 20 min. The oxide-clad design was then clad with 2.0 μm of HSQ using an optimized annealing process described in Chapter 7.

3.2.2 Reactive-Ion-Etching Optimization

One of the critical characteristics of microring resonators is that they require rigorously vertical sidewalls. This is especially important in the coupling-gap region for two reasons. One is that slanted sidewalls will affect the evanescent-coupling coefficient, changing the bandwidth of the filter. The second reason is that the slanted sidewalls can cause polarization mixing to occur. The microring filter designs are highly polarization dependent, and any mixing of polarization states at the coupling region will greatly reduce performance. Therefore, it is important to make the sidewalls as vertical as possible; this can be done by optimizing the RIE process.

To achieve highly vertical sidewalls during RIE, two things are desirable: high selectivity between the masking material and the material to be etched, and the formation of a sidewall passivation layer. Since a Ni hardmask is used for this RIE process the selectivity between the SiN_x and the mask is extremely high, ~40:1. It is also possible to form a passivation layer on the SiN_x surface by adding hydrogen into the etch recipe. This is done by using CHF_3 gas. Although the passivation layer forms on all surface of the SiN_x, ion bombardment helps to selectively remove it from horizontal surfaces, leaving it only on vertical surfaces, i.e. the sidewalls. However, if the sidewall passivation layer grows during the etch or is removed by the etch the resulting sidewall profile will slant out or in, respectively. By controlling the amount of O_2 in the RIE process it is possible to control the growth rate of the sidewall passivation layer. If too little O_2 is used the sidewall passivation layer will grow during the etch, resulting in the sidewall profile to slant outward (Fig. 3.3a). Alternatively, if too much O_2 is added, the

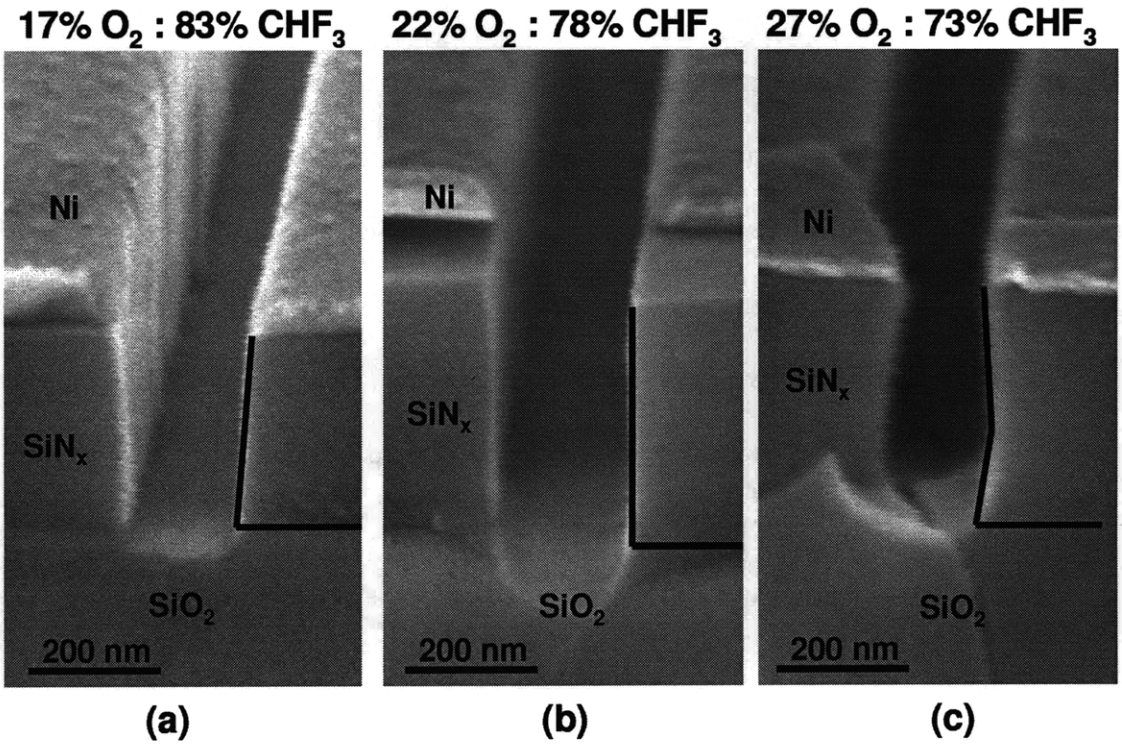


Fig 3.3: Sidewall profile of SiN_x in the gap area for different RIE recipes: (a) outward sloping sidewalls from too little O_2, (b) near vertical sidewall for optimal O_2 concentration, and (c) inward sloping/keyhole profile sidewalls for too much O_2.

sidewall passivation layer will be removed as soon as it develops, resulting in a sidewall profile that slants inward, forming a keyhole profile in the gap region (Fig. 3.3c). If the correct ratio of CHF_3 and O_2 is selected it is possible to achieve a steady state thickness, resulting in vertical sidewalls. For this process it was found that a ratio of 3.5:1 CHF_3:O_2 resulted in nearly vertical sidewalls (Fig. 3.3b).

3.3 SILICON FILTERS

In addition to SiN_x, microring-resonator filters were also fabricated using crystalline Si as the core material. There are advantages and disadvantages to using Si over SiN_x. The main advantage is that Si exhibits very low loss from optical absorption at the

wavelengths of interest. Being a stoichiometric crystalline material it has well known and repeatable optical properties. The SiN_x material, on the other hand, is not stoichiometric or crystalline, and since the deposition parameters are optimized for low tensile stress, its optical properties, including absorption and refractive index, can vary significantly from batch to batch. Another advantage of Si is that it has a higher index of refraction, allowing for smaller radii and denser integration. However, with the increased refractive index comes an increased sensitivity to dimensional changes and sidewall roughness making fabrication much more challenging.

To partially overcome the problems associated with the higher index of Si, we use a filter design having a low-aspect-ratio waveguide cross-section. This low-aspect-ratio waveguide lessens the frequency sensitivity of the microring to changes in waveguide width at the price of an increased sensitivity to the height. This is an acceptable trade-off since the height can be controlled and measured very accurately through oxidative thinning and ellipsometer measurements. Another benefit of this low-aspect-ratio waveguide is that the propagation loss is less sensitive to sidewall roughness. The designed and measured transmission responses for this improved Si filter are shown in Fig. 3.4.

For this filter design the propagation loss in the Si was assumed to be 3 dB/cm. The drop loss of the measured response is lower than the design, indicating, that the actual propagation loss is less than expected. By measuring the Q of a weakly-coupled, large-radius microring resonator the propagation loss was calculated to be ~2.5 dB/cm (see Appendix A). The overall shape of the filter response agrees very well with the

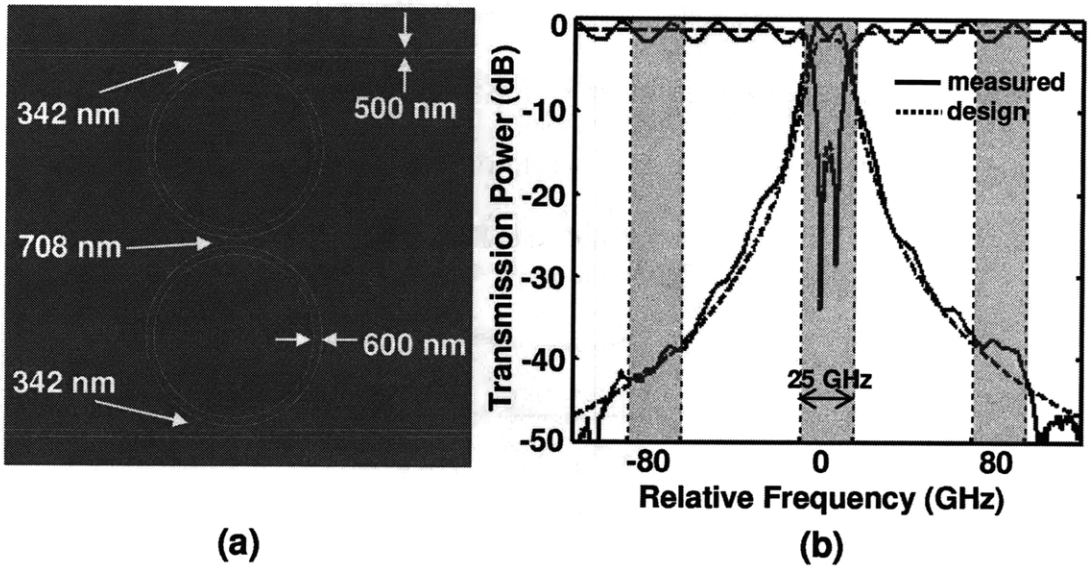


Fig. 3.4: (a) Top-view scanning-electron micrograph of Si filter design before overcladding with HSQ. Arrows on the left indicated the gap dimensions. (b) Designed and measured transmission response of Si filter.

design indicating a high level of dimensional accuracy. The oscillations seen in the measured thru and drop responses are a Fabry-Perot effect due to reflections off the waveguide end facets, not a characteristic of the filter.

3.3.1 Silicide Formation

The first attempt at fabricating Si filters used the same fabrication process developed for the SiN_x filters with a slightly different CHF_3:O_2 gas ratio. The fabrication process visually appeared to work, but when the devices were tested the loss was measured to be very high ~70 dB/cm. This very large loss is an order of magnitude higher than what would be expected from sidewall roughness alone, measured to have a variance of 3.0 nm^2. One possible explanation for this loss would be if $NiSi_x$ was forming from a reaction between the Ni hardmask and the Si. This was thought to be

highly unlikely since there was a 40 nm-thick barrier layer of thermal SiO_2 between the Ni and the Si (Fig. 3.5). At the highest processing temperature used when the Ni was on the wafer, ~150°C, the Ni would be expected to diffuse less than an angstrom into the SiO_2 barrier layer. Also it is important to note that this highest processing temperature is

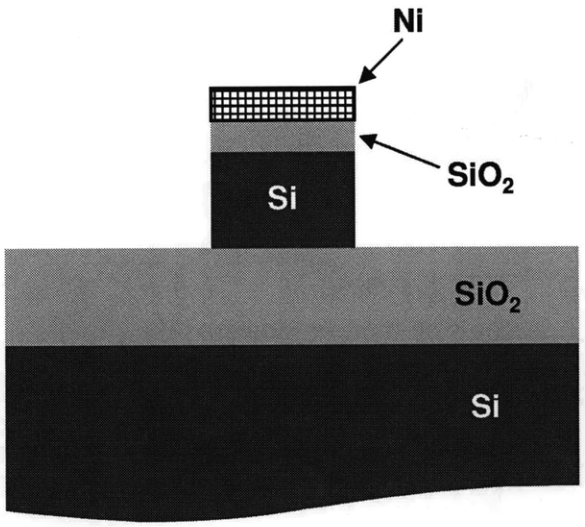


Fig. 3.5: Cross-section diagram of Si waveguide after RIE showing the SiO_2 diffusion barrier between the Ni hardmask and Si waveguide.

still below the formation temperature of $NiSi_x$. Nevertheless, it was decided that the loss must be coming from using a Ni hardmask. To further test this theory various metals were used as a hardmask and the propagation loss and sidewall roughness measured. From Table 3.1 it is seen that the propagation loss decreased as the silicidation temperature of the hardmask metal increased, further supporting the idea of silicide formation from the hardmask. Table 3.1 also shows that there is no correlation between the measured propagation loss and the sidewall roughness for the various metals, confirming that another loss mechanism is dominate. To verify the formation of silicide, a cross-section of the waveguide that had been formed using a Pd hardmask was prepared for scanning-transmission electron microscope (STEM) analysis. The Pd sample was

chosen since it had both the highest loss and lowest sidewall roughness. The cross-section STEM micrograph of the waveguide is shown in Fig. 3.6(a) with boxes displaying different areas that were analyzed by energy-dispersive x-ray spectrometry (EDS). The EDS spectra for each sample point are shown in Fig. 3.6(b).

These spectra confirm the presence of Pd in the Si waveguide 1-2 nm from the sidewall, but not at 8-9 nm from the sidewall. The presence of the Pd confirmed that the metal hardmask was contaminating the Si waveguide, resulting in the excess loss. However, the location of the Pd only on the sidewalls showed that the Pd was not diffusing though the SiO_2 barrier layer. A probable explanation is that the Pd was sputtered from the mask and deposited on the sidewall with enough energy to form a silicide. The metals with higher silicidation-formation temperatures are also sputtered, but do not have enough energy to bond to the sidewall and are later removed at the same time as the hardmask. Although some metals did not appear to form a silicide; these metals all produced very rough edges making them non-ideal for photonics. As a result of this investigation, we changed the process from using PMMA with a lift-off step to using HSQ (a negative tone inorganic electron-beam resist) as the resist and mask material.

Table 3.1 Measured Results for Different Metallic Hardmasks

Metal hard mask	Ni	Pd	Co	Cr	Fe-Ti[c]	Fe
Silicide formation temperature (°C)	200	200	270	400	350 (Ti)	400
Roughness variance[a] (nm^2)	3.0	2.8	4.8	7.7	3.1	4.2
Propagation loss[b] (dB/cm)	~70	>70	>65	<15	<15	<15

[a] Results for nonoptimized lift-off.
[b] Loss for Ni sample measured on ring resonator. Loss for other samples measured on straight waveguides.
[c] Fe-Ti refers to a 5 nm Ti cap on top of 45 nm of Fe to prevent corrosion of Fe during lift-off.

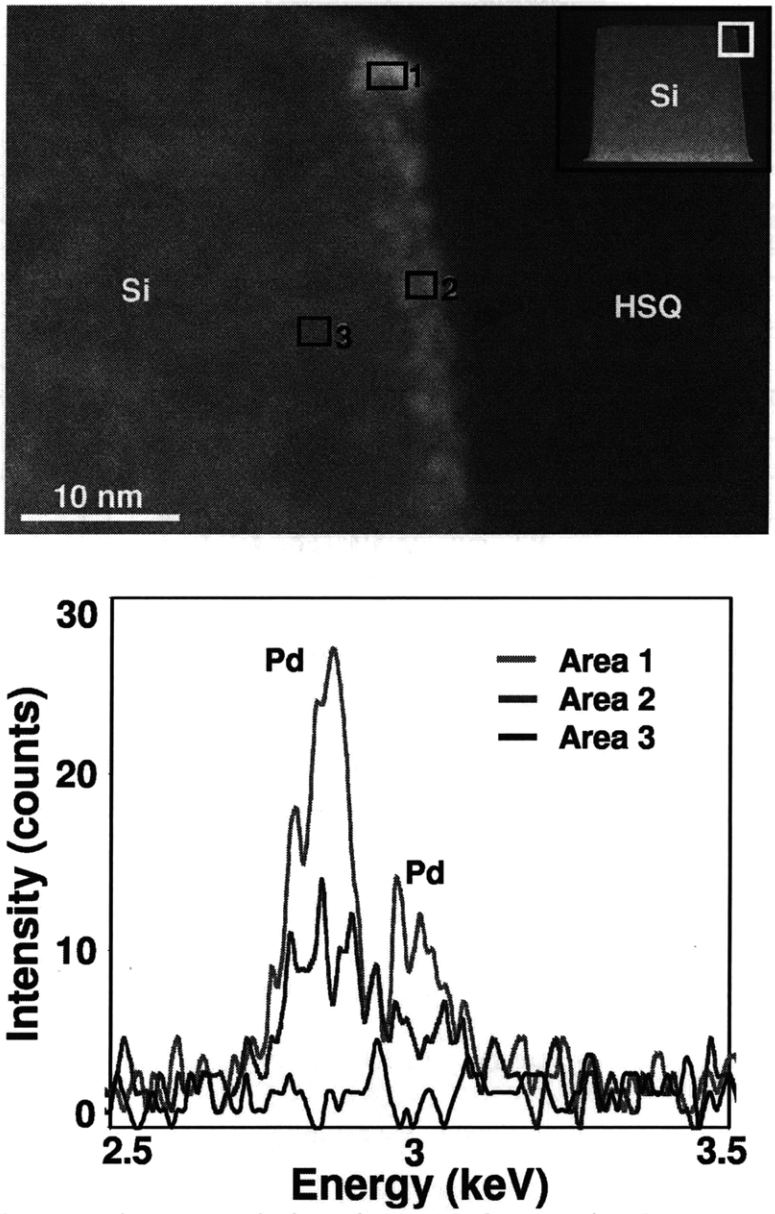


Fig. 3.6: (a) scanning-transmission-electron micrograph of top corner of Si waveguide (whole waveguide shown in inset). Highlighted areas are locations where energy-dispersive x-ray spectrometry was performed. (b) EDS spectrum for corresponding points showing the location of Pd contamination.

3.3.2 Si Filter Fabrication with HSQ

The fabrication process shown in Fig 3.7 begins with a SOI wafer having a 3 μm-thick buried-oxide layer and a 220 nm-thick Si-device layer. The device layer was

thinned to 105 nm using thermal oxidation followed by a hydrofluoric-acid (HF) dip to remove the oxide. The exact thickness was measured with an ellipsometer. Next, the wafer was spin coated with a 65 nm-thick layer of HSQ, a negative electron-beam resist, and baked at 90°C for 60s on a hotplate (HSQ was developed as a spin-on glass; once baked it resembles SiO_2). Unlike the SiN_x fabrication process, there is no need for a conduction layer since the sheet resistance, 10-30 $^{\Omega}/_{\square}$, of the SOI wafer is sufficient to prevent the build up of charge during SEBL. The HSQ was exposed with the same SEBL system and accelerating voltage used previously for PMMA. The exposure dose for HSQ was 1500 $\mu C/cm^2$, significantly larger than what is used for PMMA. The exposed HSQ

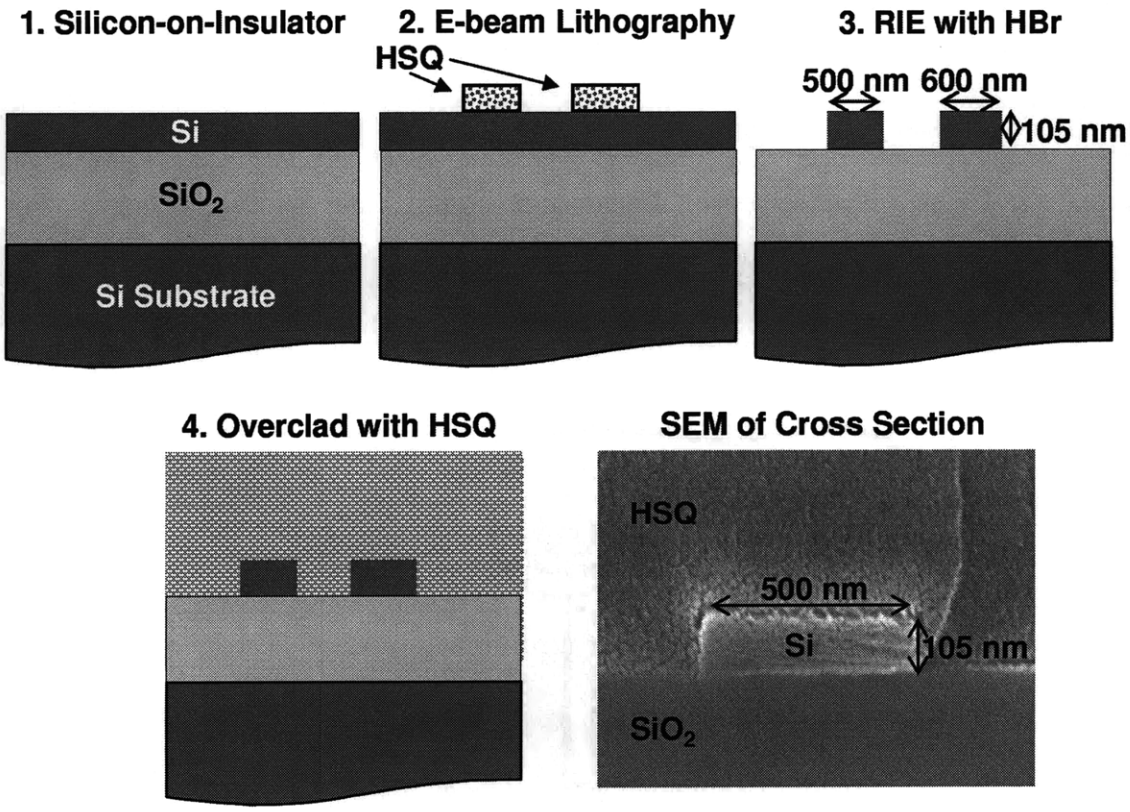


Fig. 3.7: Basic fabrication process for Si filters using HSQ resist and HBr etching. Cross-section scanning-electron micrograph of fabricated waveguide is shown in the bottom right image.

was developed for 2 min. in a 25% solution of tetramethylammonium hydroxide (TMAH) and then rinsed with DI water. The HSQ pattern was then transferred to the Si layer using RIE with HBr gas. The selectivity between the Si and HSQ mask was measured to be 11:1 for this etch. The remaining HSQ mask was removed using an SC-1 clean [26] followed by a 4 min dip in 0.125% solution of HF. Lastly, the fabricated Si devices were overclad with 1 μm of HSQ and annealed for 1 hr at 400°C in an O_2 ambient.

3.4 EXPOSURE OPTIMIZATION

The most critical step in the fabrication of the SiN_x and Si microring-resonator filters is the SEBL exposure. There are many variables that can be controlled in the SEBL process, including: electron dose, dimensional biasing, and writing strategy. For photonic devices it is important to optimize the exposure dose and e-beam resist to minimize line-edge roughness. This roughness will be transferred to the device sidewalls during further processing, resulting in increased propagation loss. Since the exposure dose is optimized for roughness, not dimensional accuracy, biasing must be used to achieve accurate dimensions. Also of great concern is pattern fidelity, i.e., how closely the fabricated microring represents the imputed circular pattern. Errors in the pattern fidelity can occur due to deflection errors, beam blanker timing errors, and intrafield distortion of the write field. By employing an optimized writing strategy it is possible to minimize these errors.

3.4.1 Roughness Minimization

For microring resonators, as well as almost all other integrated-photonic devices, it is very important to minimize sidewall roughness in order to minimize scattering losses. Sidewall roughness arises primarily from the line-edge roughness (LER) of the etching mask, which in turn depends on the SEBL exposure either indirectly, when using PMMA and a lift-off, or directly, when using HSQ.

For the optimization of the dose for the SiN_x designs, using PMMA resist, a series of electron-beam doses were used to expose the filter design and nearby waveguides. The resist was developed, Ni deposited and a lift-off performed. The Ni hardmasks formed for each dose were then imaged with a scanning-electron microscope (SEM). Each imaged pattern, examples of which are shown in Fig 3.8, fall into one of five categories: not cleared, under exposed, optimal dose, over exposed and fused gap. In the not-cleared regime the dose is so low that after development there is still a thin layer of PMMA at the bottom of the exposed feature. In this case when the metal is evaporated there is no way for it to make contact with the substrate, so the entire defined feature is removed during lift-off. In the under-exposed regime, where the resist has been cleared over most of the feature except for small footings at the edges, these footings get covered with a thin layer of metal that is connected to the metal layer at the bottom of the trench. During lift-off the PMMA footing is removed by the solvent but the thin layer of metal remains attached to the mask. This thin layer will either fold over on top of the hardmask or fold down onto the SiN_x. This layer acts as a etch mask during at least a portion of the

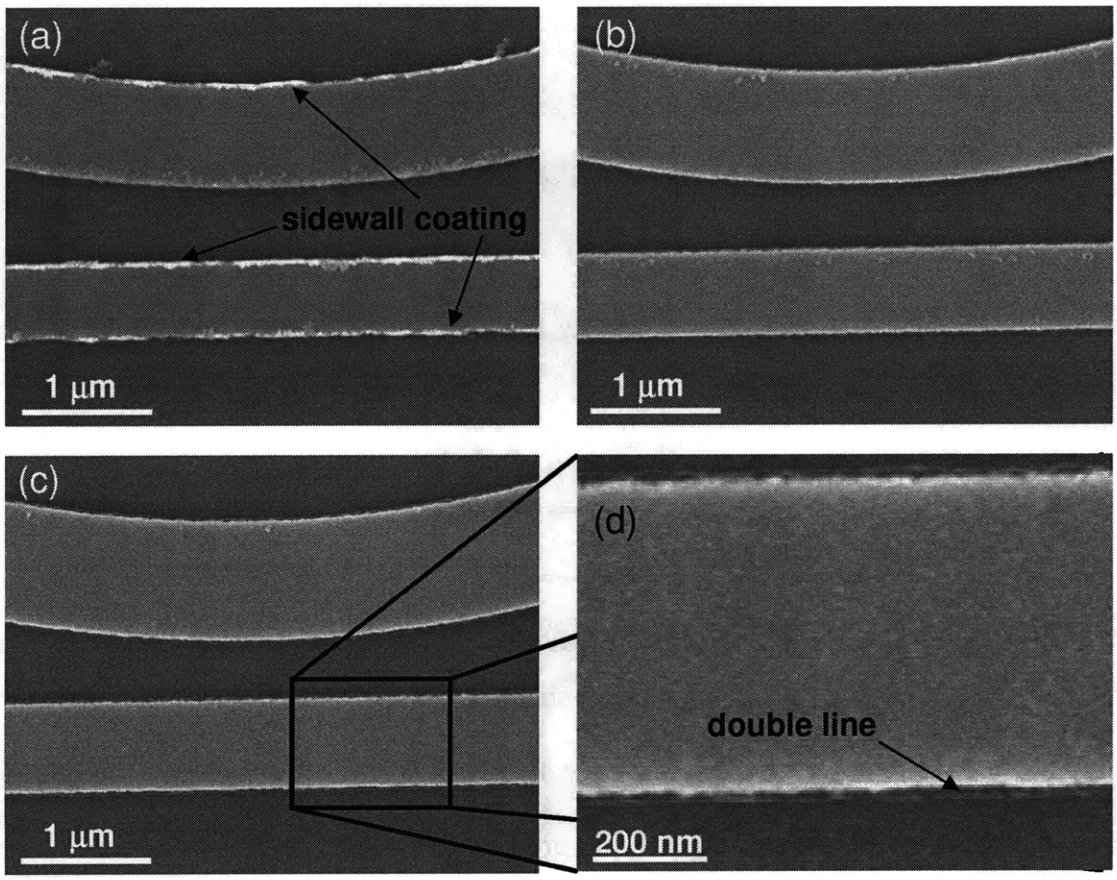


Fig. 3.8: Scanning-electron micrographs of Ni on SiN_x after lift-off for various exposure doses. (a) An under-exposed sample results in a thin coating of metal on the resist sidewalls that remains after lift-off. (b) Optimal exposure dose resulting in minimal sidewall roughness. (c) An over-exposed sample resulting in a thin secondary Ni line at the edges. (d) Zoom-in of an over-exposed sample clearly showing the double line.

etch process until it is completely sputtered away, adding to the sidewall roughness. With an optimally exposed dose the PMMA sidewalls are completely vertical or have a very slight undercut. In this case no metal is deposited on the PMMA sidewalls, resulting in a hardmask that has the same roughness as the PMMA resist. As one increases the dose even further the over exposed regime is entered. In this regime the PMMA profile has a significant undercut of a few nanometers. During evaporation the metal that hits the SiN_x surface has enough surface mobility to diffuse into this undercut area. This

creates a secondary thin mask that is seen in the SEM image as a faint double line (Fig. 3.8d). This thin secondary hardmask will sputter away during the etch process, once again increasing the sidewall roughness. If the dose is increased even further the coupling gap between the waveguide and the microring will fuse due to proximity effects, ruining the filter. The range of doses that fall between the under-exposed and over-exposed regimes makes up the exposure window. For PMMA, this window is quite large, $^{+}$/-20%. Using the optimal dose the sidewall roughness of the SiN_x microrings and waveguides is measured to have a variance of ~3.0 nm^2,

For the Si-based photonic devices, fabricated using HSQ resist, another range of doses were tested. Once again the results could be divided into five regimes: incomplete crosslinking, under exposed, optimum dose, over exposed and fused gaps (Fig. 3.9). When the crosslinking is incomplete the HSQ is unable to withstand the developer. The under exposed regime is characterized by moderately rough edges. The optimal dose has

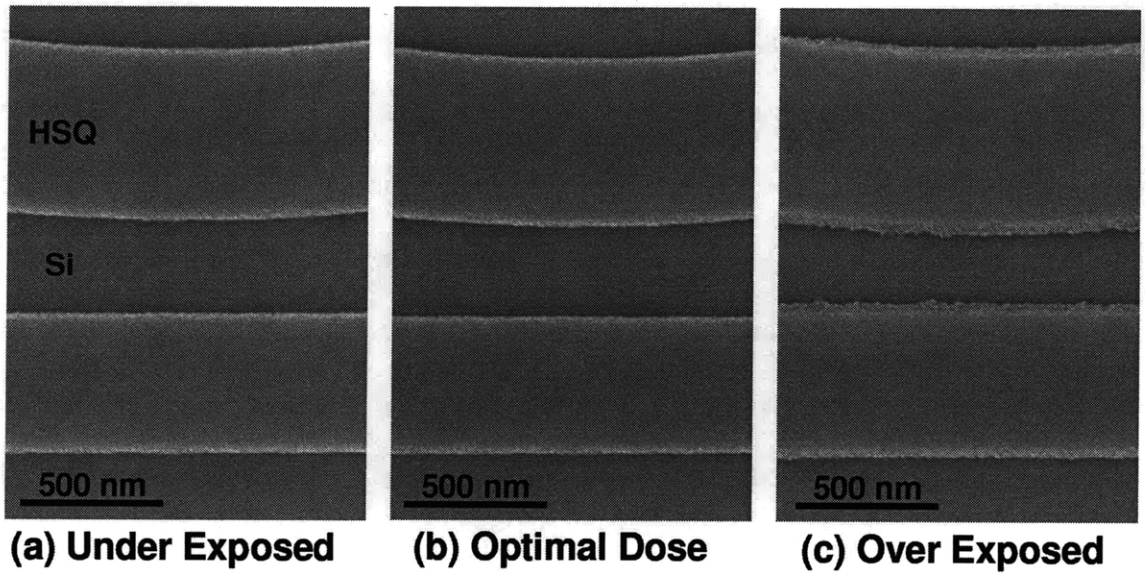


Fig. 3.9: Top-view scanning-electron micrographs of HSQ on Si after development for various exposure doses. (a) An under-exposed sample results in slightly rough sidewalls. (b) Optimal exposure dose resulting in minimal sidewall roughness. (c) An over-exposed sample resulting in a large footing and roughness

extremely smooth edges with a measured roughness variance of 1.8 nm^2. As the dose is increased into the over exposed regime a significant footing develops at the bottom of the HSQ features. This footing has an extremely high roughness as seen in Fig 3.9c. Once again if the dose is increased too much the coupling gap between the ring and waveguide will fuse. Although the sidewall roughness at the optimal dose achievable with HSQ is lower than for PMMA, the exposure window is also smaller, $^{+}$/-8%, but still acceptable.

3.4.2 Absolute Dimensional Control and Pattern Fidelity

Since the exposure dose is optimized to reduce sidewall roughness, not for replicating absolute dimension of the design, it is important to pre-bias all of the dimensions so that they are correct at the end of fabrication. This places a high level of importance on how well one can measure the dimensions of the straight (bus) waveguide width, the microring waveguide, and the coupling gaps. Typically, measurements performed using an SEM can obtain a measurement accuracy of only 5%, which, for the near-micron-size features of the microring resonators, is substantial. In an SEBL system one can calibrate the deflection of the electron-beam to the movement of the interferometric stage. This can theoretically improve the accuracy of SEM measurements to below 1 nm, but in practice the accuracy is limited to ~5 nm due mechanical vibrations. Using this method, all of the critical features of each microring-filter design were measured after a test fabrication run and then biased appropriately in the final layout to achieve the correct dimensions. After biasing, the critical dimensions are no more than 6 nm off from the design as seen in Table 3.2.

Table 3.2 Dimensional Accuracy of Filter Parameters

	SiN_x filter, air clad			SiN_x filter, oxide clad			Si filter, oxide clad		
	Bias	Measured	Error	Bias	Measured	Error	Bias	Measured	Error
Ring width (nm)	-30	897	-3	-36	802	+2	-72	602	+2
Bus width (nm)	-30	700	0	-42	602	+2	-72	501	+1
Gap, bus-ring (nm)	0	166	+4	0	508	-2	0	340	-2
Gap, ring-ring (nm)	-6	394	+4	-12	926	-4	-6	703	-5

In addition to making sure that the absolute dimensions of the microring are accurate it is also important to make sure that the overall shape of the microring filter is correct. This has two key components, one is that the overall shape of the microring be as close to circular as possible, and second is that both microrings in the same filter be identical or at least have identical resonant frequencies. To ensure circular shape of the microring it is important to optimize the SEBL writing strategy. This was first done by Tymon Barwicz and is outlined in detail in his thesis [27]. I feel it is important to briefly explain it again here because of how critical it is to the fabrication of high quality microring-resonator filters.

The first optimization is the scan speed. In a vector scan SEBL system a beam blanker controls when the beam is on and off. The beam will be blanked and driven to a point near the starting point of the vector to be scanned. Once the beam position reaches the starting point of the vector it is unblanked and scanned continuously to the end point, exposing the resist along the vector. When the beam has reached the ending point the blanker is reactivated halting the exposure of the resist. With this method any timing error in the blanking and unblanking of the beam will result in a positional error in the exposure. By slowing down the writing speed the same timing error in the beam blanker

will result in a smaller positional error in the exposed feature. There are multiple ways to decrease the scan speed in the Raith 150 system, including decreasing the beam current (smaller aperture) and increasing the spacing between vector scans.

The second optimization is the scan algorithm. In the Raith 150 it is possible to expose a given feature using an area, a point or a line scan. When using an area scan to expose a microring the pattern generator of the Raith 150 will split up the microring shape into a series of boxes and write each one using a raster scan. This results in the majority of the beginnings and endings of each scan, where most placement errors take place, to be located at the edges of the microring, the place of most concern. The point scan method, where the beam exposes the ring on a point by point basis is not practical since there is a finite settling time before and after each point. Given that each ring contains approximately 1 million points this quickly adds up. The line scan is ideal for circular structures because it allows one to have both the beginning and ending of each scan inside the exposed pattern, thereby decreasing the effect of beam-placement errors on the microring shape. By writing a group of concentric circles using these line scans it is possible to exposes a circle with a desired width. Also, by randomizing the beginning

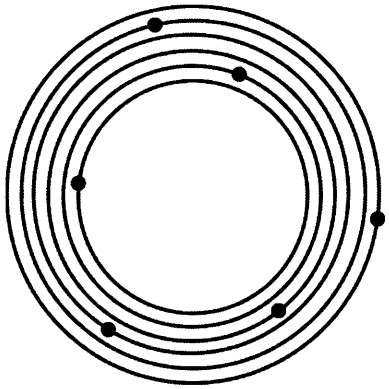


Fig. 3.10: Schematic demonstrating the optimum SEBL writing strategy for a microring resonator.

and ending points of the exposed concentric circles it is possible to distribute the deviation in the effective dose due to placement errors over the circumference of the microring, lessening their overall effect. This ideal writing strategy for the microring is sketched in Fig. 3.10, where the dots represent the starting and stopping points of each circular scan.

Another component of the SEBL write is matching the resonant frequencies of the two microrings of the same filter. In the layout the two microrings are identical and, due to symmetry, proximity effects should shift the resonant frequencies the same for both rings. However, a repeatable frequency mismatch between the two rings is always observed. Experiments showed that this repeatable mismatch was dependant of the location of the microrings in the 100 μm X 100 μm write field (Fig. 3.11). The cause of this is the intrafield distortion of the SEBL address grid. Clearly, the address grid that makes up the writing field is not a perfect Cartesian grid. These intrafield distortions are caused by imperfections in the electron optics and the digital-to-analog converters. In SEBL systems such as the Raith 150, these distortions can result in absolute beam-placement errors as high as 20 nm. How the distortion changes the microring varies with location in the write field, resulting in a location-dependent frequency mismatch between the two microrings. This frequency mismatch can be either measured empirically or simulated using a map of the intrafield distortion [28]. Once known, the mismatch can be compensated by predistorting the microrings in some manner to counteract the effects of the intrafield distortion.

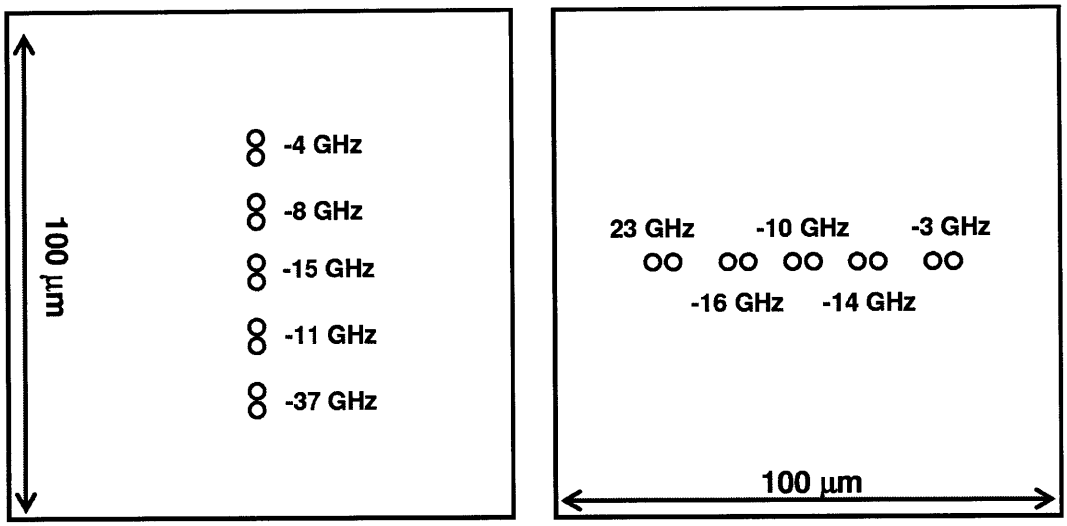


Fig. 3.11: The repeatable resonant frequency mismatch between the two rings of a second-order filter displaced by integrals of 12 microns along the y-axis (a) and by 12 microns along the x-axis (b). The actual filters are 4 times larger than what is shown here and each filter is fabricated in its own field. The variance of the frequency mismatch at a given location was less than 8 GHz.

3.5 CONCLUSION

The CHF_3 to O_2 ratio used during RIE for SiN_x microring resonators was optimized to achieve smooth vertical sidewalls. For the fabrication of Si microring resonators the process was changed to eliminate the metal hardmask which caused excess loss from silicide formation. The exposure dose for each filter design and resist was optimized to produce minimal sidewall roughness, which was measured to be of 3.0 and 1.8 nm^2 for the SiN_x and Si filters, respectively. To ensure dimensional accuracy all critical dimensions were measured using the SEBL system, calibrated with the interferometric stage, and then biased in the layout to reduce errors below 6 nm. The SEBL writing strategy was also optimized to achieve the high level pattern fidelity required for the microring resonator filters.

Chapter 4

Lithographic Resonant Frequency Control of Microring Resonators

4.1 INTRODUCTION

The greatest challenge in fabricating HIC microring-resonator filter banks is achieving accurate spacing between resonant frequencies. The resonant frequency of a microring filter is defined by the optical path length of the microring (shown previously in Eq. 2.5). The optical path length can be broken down into two components; the physical path length of the microring (i.e. the circumference $2\pi R$) and the effective index of refraction (n_{eff}). It is possible to control the physical path length and n_{eff} by changing the dimension of the microring in the lithographic layout. However, this is limited by the discrete step size of the SEBL address grid, which is 6 nm for the optimal microring-resonator writing strategy. For high performance (small channel spacing) filter banks, comprised of HIC microring filters, this discrete step size would result in frequency shifts that are too large.

Parts of this chapter are featured in:

C.W. Holzwarth, T. Barwicz, M.A. Popović, P.T. Rakich, E.P. Ippen, F.X. Kärtner, and Henry I. Smith, "Accurate resonant frequency spacing of microring filters without postfabrication trimming," J. Vac. Sci. Technol. B, vol. 24, no. 6, pp 3244-3247 (2006).

C.W. Holzwarth, R. Amatya, M. Dahlem, A. Khilo, F.X. Kärtner, E.P. Ippen, R.J. Ram, and Henry I. Smith, "Fabrication strategies for filter banks based on microring resonators," J. Vac. Sci. Technol. B, vol. 26, no. 6, pp 2164-2167 (2008).

There are two ways to change the physical path length of a microring resonator in the lithographic layout. The first way is to simply increase the radius of the microring resonator by ΔR, which will increase the physical path length by $2\pi\Delta R$ (Fig. 4.1a). Since the minimum address grid step size is 6 nm the minimum change in optical path length using this method is 2π*6 nm or 37.68 nm. The resulting frequency shifts from this minimum change in radius for the three microring-resonator filter designs are shown in Table 4.1. These frequency shifts are all larger than the channel spacing desired in a high-performance filter bank. Another way to change the physical path length is to add a small straight section to the microring, forming a racetrack structure (Fig. 4.1b). The length of this straight section can be changed by ΔL, which will increase the path length of the microring by $2\Delta L$. This results in a minimum change in the physical path length of 12 nm, producing a much smaller frequency shift than changing the radius of the microring (Table 4.1). This method, however, is not optimal because adding the straight section increases the internal loss of the microring due to the modal mismatch between the resonant modes in the curved and straight sections of the ring. For resonant structures this small loss due to modal mismatch adds up very quickly making this approach unsuitable.

Table 4.1 Resonant Frequency Dependence on Dimensional Changes

	SiN_x air-clad	SiN_x oxide-clad	Si oxide-clad
ΔR = 6 nm	106 GHz	87 GHz	104 GHz
ΔL = 6 nm	34 GHz	28 GHz	33 GHz
ΔW = 12 nm	396 GHz	300 GHz	480 GHz

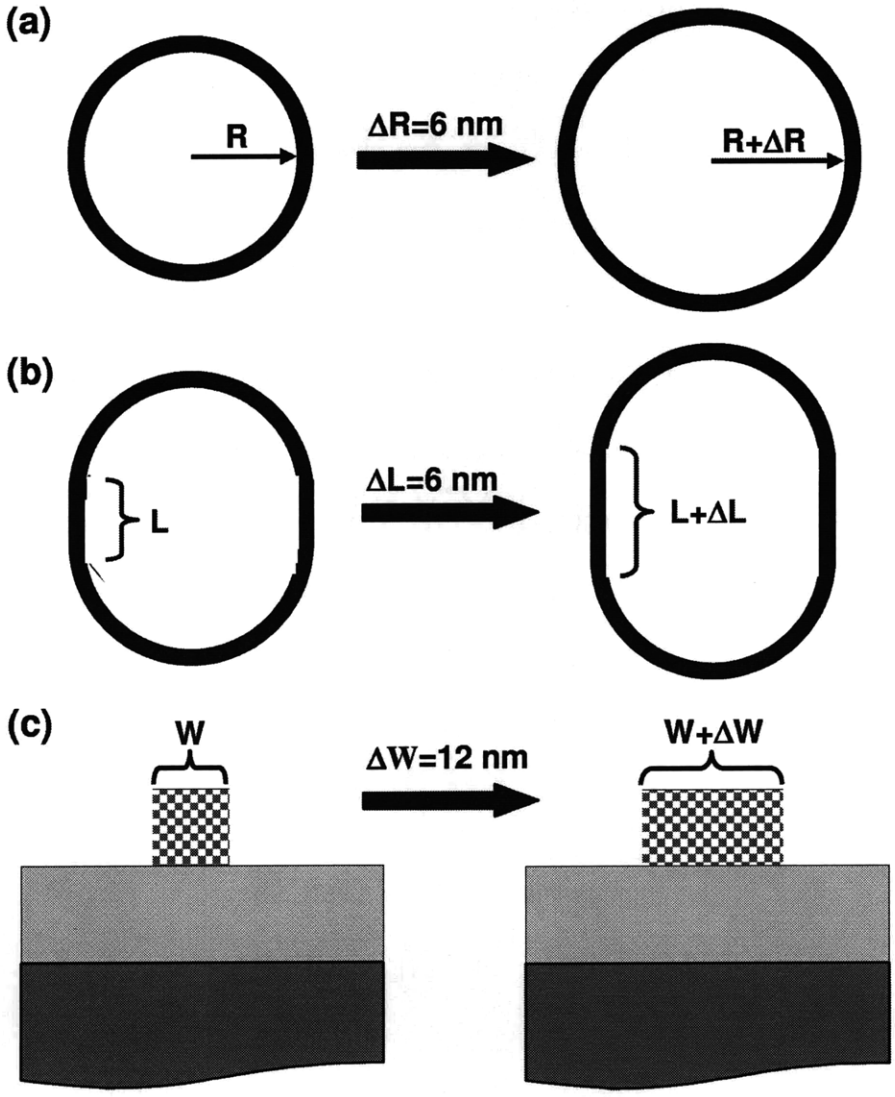


Fig. 4.1 Diagram showing how one can change the physical path length by increasing (a) the radius or (b) adding a length to a straight section. (c) It is also possible to increase n_{eff} by changing the microring waveguide width.

Although not as straight forward as changing the physical path length, it is also possible to change n_{eff} in the lithographic layout. This is done by increasing the microring waveguide width. One way to think of n_{eff} is a weighted average of the refractive index of the mode in the core and cladding materials. By increasing the width of the microring waveguide, more of the mode is confined in the high-index core, increasing n_{eff} (Fig. 4.1c). The writing strategy for the microring uses single-pixel lines

that are spaced by 12 nm each. This means that the minimum amount the width of the microring can be changed is 12 nm, resulting in the frequency shifts listed in Table 4.1. These frequency shifts are all quite large, demonstrating how sensitive the resonant frequency is to changes in the average waveguide width.

Clearly, to achieve the desired resonant-frequency spacing one needs to control the dimensions of the microrings on a scale much finer than the address grid of the SEBL system. To ensure 1 GHz channel-spacing precision it is necessary to control the dimension on the tens of picometer scale, orders of magnitude finer than the discrete address grid of the SEBL system. Another parameter that is adjustable in SEBL, is the exposure dose of each microring. By controlling the exposure dose one can control the resonant frequency of the microring filters in a way that is no longer limited by the discrete SEBL address grid.

4.2 DOSE MODULATION

One of the advantages of the serial writing process of SEBL is that it is possible to control the exposure dose (charge incident per unit area) of individual features in the layout. Assuming constant current in the electron-beam, the dose can be accurately controlled via adjusting the dwell time at the address-grid points. By adjusting the exposure dose it is possible to change the width of a feature on a scale that is orders of magnitude smaller than the address grid of the SEBL.

The point-spread function of an electron beam is not a delta or top-hat function, typically it is modeled as a double Gaussian, with the narrow Gaussian simulating the

incoming beam and the wider Gaussian is the backscattered electrons. To better fit empirical data, a tail function, represented by a polynomial in logarithmic space, is added to the point-spread function, smoothing out the double Gaussian. The point-spread function of the Raith 150 system has been previously measured and is shown in Fig 4.2 [27]. By performing a convolution of the point-spread function with the microring layout it is possible to calculate the effective exposure dose as a function of position. Once the effective exposure dose profile is known one can use resist development models to find how changes in exposure dose can change the width of the microring waveguide. This information can then be used to calculate the resonant frequency dependence on exposure dose. Two models used in this thesis for simulating the development of resists are the binary model and string propagation method.

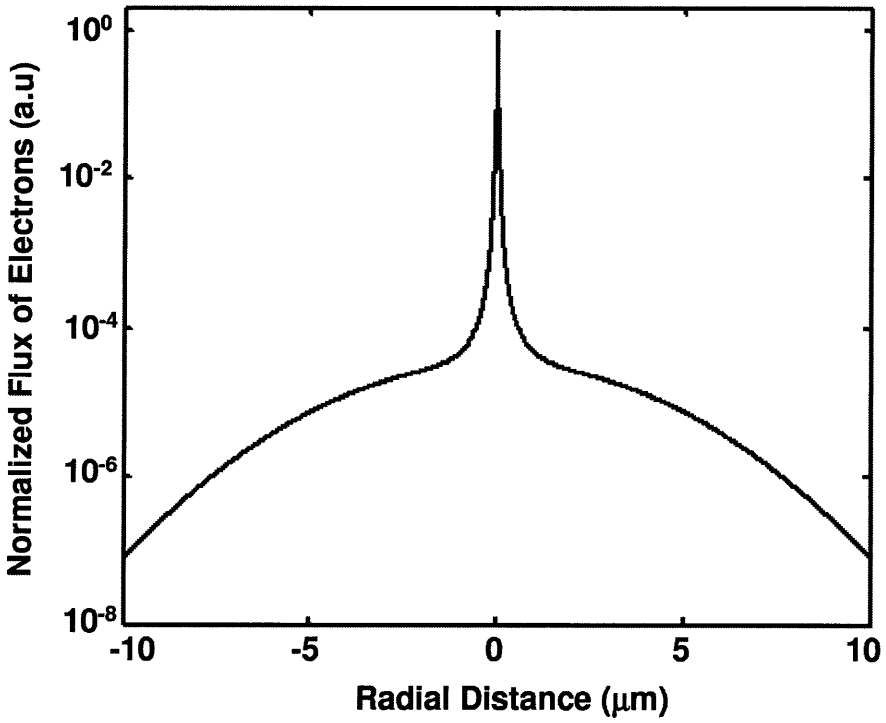


Fig. 4.2 Normalized plot of the electron-beam point-spread function of the Raith 150 system.

4.2.1 Binary Model

The binary development model is the most simplistic, but for many resists it will give accurate results. This model assumes that if a positive resist receives a dose above a threshold level it will be developed (dissolved by the developer) and will remain undeveloped for doses below the threshold. For a negative resist the opposite will be true.

For this model, in addition to calculating the effective dose as a function of location by performing a convolution of the point-spread function and the exposed layout, it is also necessary to determine the threshold dose. This can be done by measuring the width of an exposed pattern and finding the dose that intersects the corresponding cross-sectional width of the effective-dose profile.

Once the threshold dose is known it is possible to repeat the convolution for different exposure doses and calculate the change in width of the feature (Fig 4.3). For microring-resonator filters the resonant frequency shift depends on the average change in the ring-waveguide width. The change in waveguide width will be different at different radial locations along the microring due to the different contribution of proximity effects from the bus waveguide and neighboring microrings. To find the average change in waveguide width, the change in waveguide width is simulated for every 30 degrees around the microring and then fitted with a polynomial function. The polynomial is then averaged over the circumference of the ring to give the average change in ring waveguide and then the resulting change in resonant frequency is calculated. Fig. 4.4 shows the simulated change in resonant frequency versus change in exposure dose for the oxide-clad SiN_x and Si filter designs calculated using the binary model.

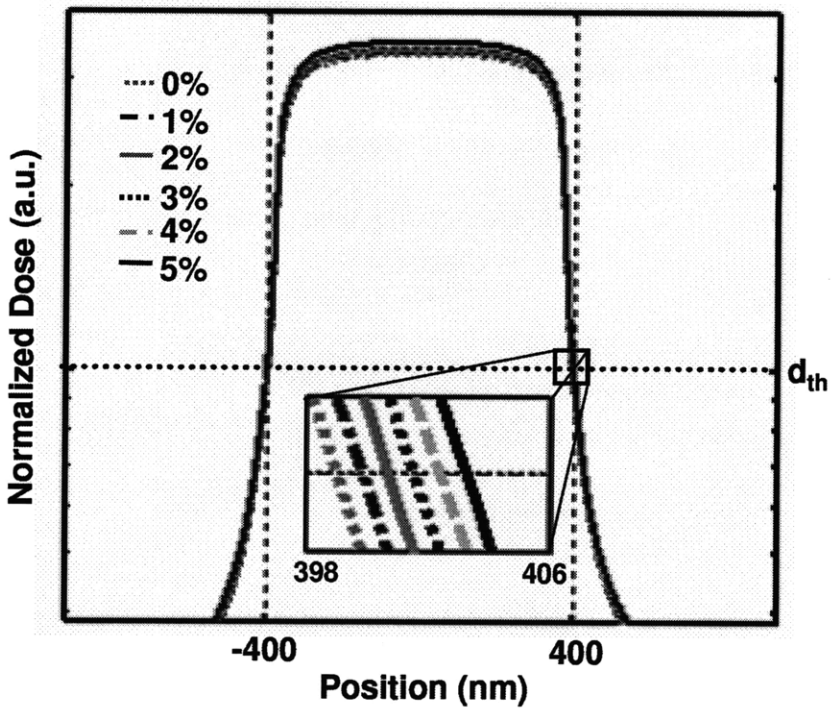


Fig. 4.3 Plot of the effective dose profile of an 800 nm wide microring waveguide.

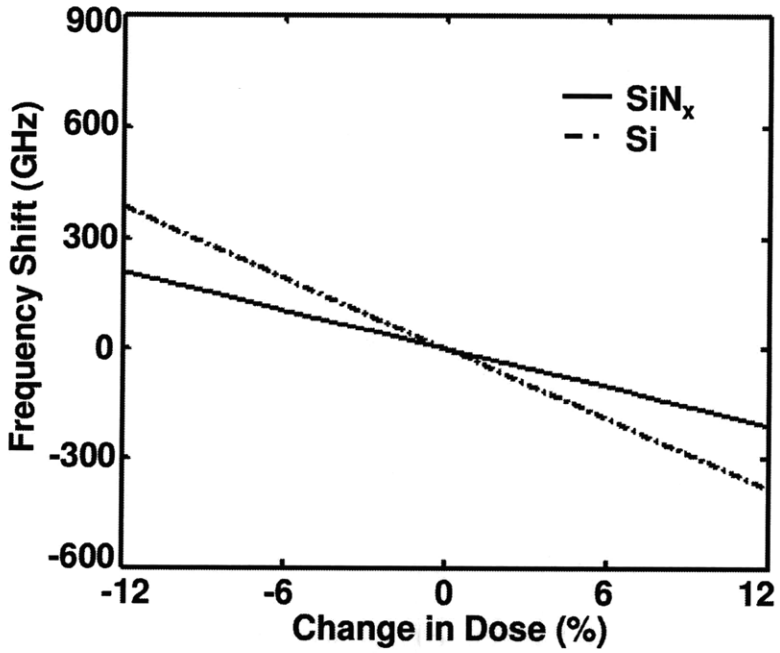


Fig. 4.4 The resonate frequency dependence on exposure dose for the oxide-clad SiN_x and Si filter designs found using the binary resist development model.

The major assumption in this development model is that the resist is binary, i.e. has infinite contrast. In reality all resists have finite contrast, meaning that the development rate is a continuous function of exposure dose. This assumption makes it so that the binary model is very good at simulating high contrast resist but breaks down for low contrast and chemically amplified resists. PMMA is a high contrast resist so the binary model is adequate but HSQ has significantly lower contrast. This means that to simulate the resonant frequency dependence of the Si filters fabricated using HSQ it is best to use a more rigorous development model.

4.2.2 String Propagation Method

Another way to model resist development is the string propagation method [29]. This method is more rigorous then the binary model since it takes into account material properties of the resist and the developer used. The string propagation method first calculates the distribution of the local resist etch-rates for the exposed feature. Next, a string of points, joined by straight-line segments, is plotted on the surface of the resist. As time proceeds by Δt, each point will propagate by a distance Δx, determined by the local etch rate of the resist. The direction of propagation is along the angle bisector of the two adjoining line segments as shown in Fig. 4.5. This is repeated for n iterations until $n*\Delta t$ equals the total development time. By making Δt small and, therefore n large, it is possible to simulate the width of the exposed microring waveguide very accurately. The main assumption for this simulation is that etching of the resist by the developer only

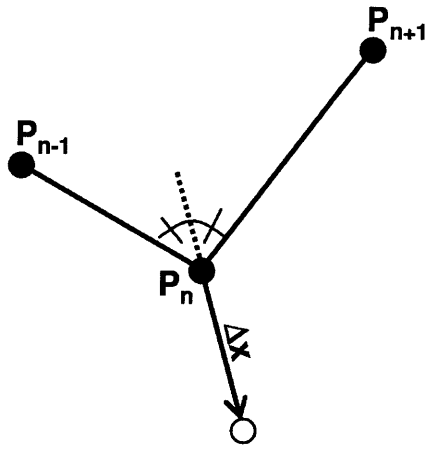


Fig. 4.5 Diagram showing how the string-propagation resist-development model works. Each point propagates Δx (local etch rate times Δt) in the direction of the angle bisector formed by the string segments connecting adjacent points.

occurs at the time-varying location of the string boundary. This assumption is valid for both PMMA and exposed HSQ.

Before employing this simulation the resist etch-rate distribution for the exposed feature must be calculated. This is done by first finding the rate of etching of the resist by the developer as a function of electron-dose. An array of 0.8 μm X 40 μm and 0.6 μm X 40 μm lines were exposed in PMMA and HSQ, respectively, using a wide range of doses. These samples were then developed in their respective developers for the standard development time, 60 s for PMMA and 120 s for HSQ. After development the thickness of the resist remaining was measured using a profilometer. This experiment was then repeated using half the development time. Using this data one can find the resist etch rate as a function of exposure dose. This method assumes that the exposure dose is constant throughout the thickness of the resist, which is valid for thin resists and high accelerating

voltages. By combining this data with the effective dose profiles it is possible to get the local etch-rate distribution profile for the exposed microrings.

Using the string-propagation method, with a Δt of 10 ms and an initial string segment length of 50 pm, the average width of the ring waveguide for various exposure doses was calculated. This data was used to find the resonant-frequency dependency on exposure dose for the oxide-clad SiN_x and Si filter designs. The results from these simulations are compared to the results obtained using the binary model in Fig 4.6. It can be seen that for PMMA, a high contrast resist, the results from the two simulations agree quite well. On the other hand for HSQ, a lower contrast resist, there is a significant difference between the two simulations. The results obtained using the string propagation method should be more accurate for HSQ since this method takes into account its low contrast by using the local resist etch-rate distribution.

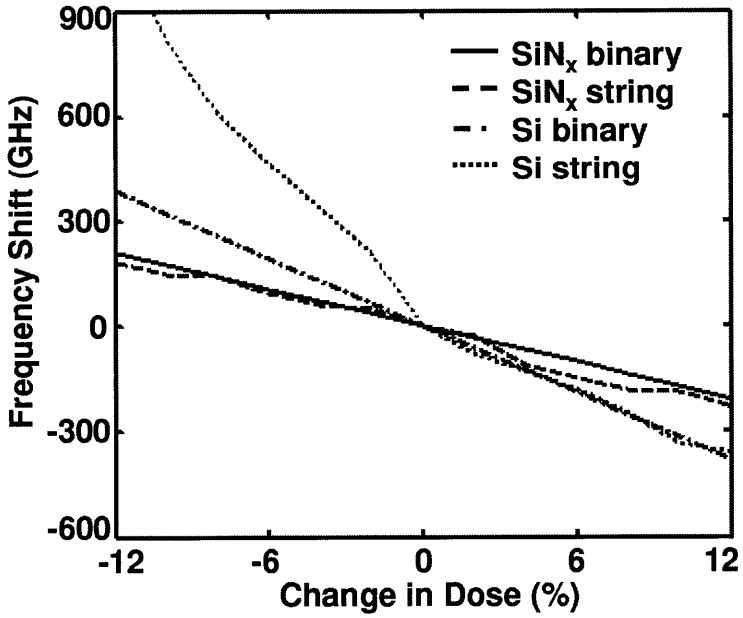


Fig. 4.6 Comparison of the frequency dependence on exposure dose using the two different resist development models.

4.3 CALIBRATION EXPERIMENTS

To confirm the simulated results for the resonant-frequency dependence on changes in the microring radius and exposure dose, empirical calibration experiments were performed. The design of these calibration experiments is critical in order to eliminate frequency shifts due to external factors. These external factors, which include variations in the core thickness, long-term drift in the electron-beam current, and temperature fluctuations during measurement, are capable of causing systematic errors that can not be factored out by using a large sampling population. For example, if the thickness of the core layer increases from one side of the wafer to the other by a few nanometers, and one writes the calibration experiment for changes in dose from top to bottom on the wafer; the results of the resonant frequency dependence will be a sum of the dependence on exposure dose and core thickness.

To factor out these external factors the calibration experiment was set up as is shown in Fig. 4.7. In this setup, each through-port has two filters on it located in close proximity (~100μm) to each other. One filter is a first-order filter and is used as a reference filter, where all parameters are kept constant in the electron-beam layout. The other filter is the second-order filter that is being calibrated, where either the radius or the exposure dose is changed slightly. For calculating the resonant frequency shifts the resonant frequency of the second-order filter is normalized to the resonant frequency of the reference filter. Since the calibration filter and reference filter are written close to each other in distance and time, the drift of the core thickness and electron-beam current are negligible. Any frequency shifts due to these effects will happen to the reference and

calibration filter equally, therefore not changing their relative frequencies. Similarly, since the through responses of the reference and calibration filters are tested at the same time their temperature is the same. If the temperature of the chip drifts a few degrees during the testing of the first calibration filters to the last the absolute difference in their frequency shifts will change but their relative difference compared to their reference filter will not. Therefore, by normalizing the resonant frequencies of the calibration filters to their respective reference filters it is, presumably, possible to remove the systematic errors in the calibration experiment. The results from these experiments for all of the filter designs are summarized in Table 4.2.

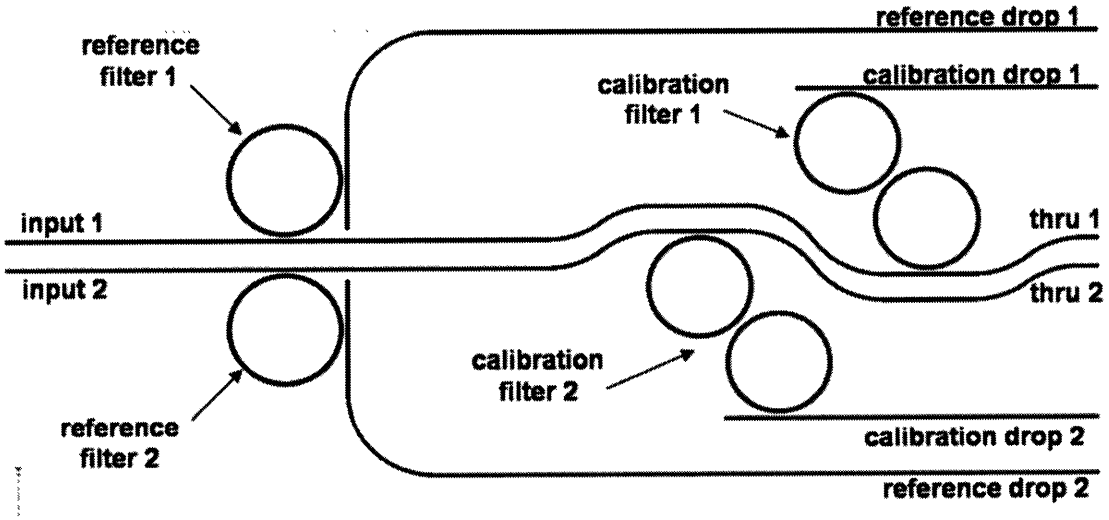


Fig. 4.7 Layout used for frequency-calibration experiments. The parameters used to write the reference filters are kept the same while the exposure dose or the radius of the calibration filter is changed.

Table 4.2 Frequency Dependence on Radius and Dose from Experiments

	SiN_x air-clad	SiN_x oxide-clad	Si oxide-clad
Dependence on radius	17.3 GHz/nm	14.8 GHz/nm	16.2 GHz/nm
Dependence on dose	17 GHz/%	14 GHz/%	64 GHz/%

The results for the frequency dependence on changes in the input radius for the oxide-clad SiN_x design is shown in Fig. 4.8 and compared to the simulated results. There are two reasons for the difference in simulated and calibration dependences. The first is intrafield distortion of the SEBL address grid, causing the inputted radius change of 6 nm to differ from the exact change in radius. The second reason, which affects the SiN_x filter only, is that the index of refraction varies slightly from batch to batch and wafer to wafer. The index used in the simulation was 2.20 and the actual index of the wafers used in that calibration experiments were between 2.17 and 2.21.

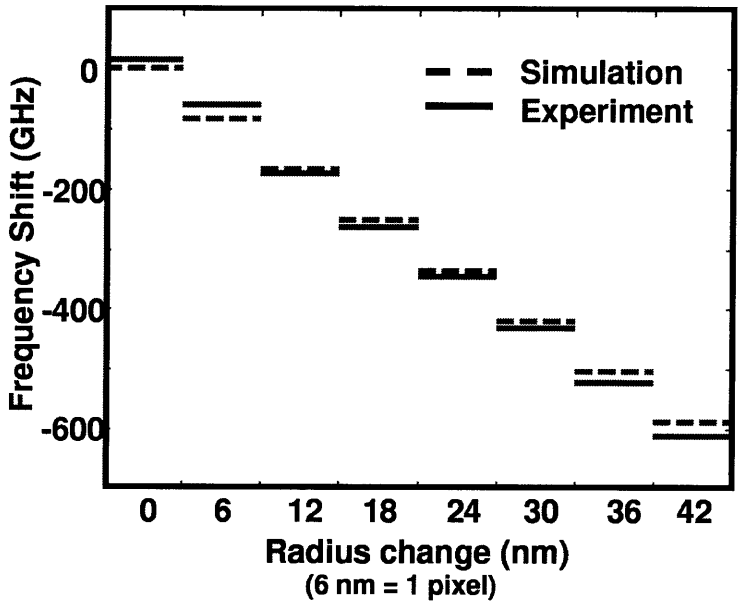


Fig. 4.8 Frequency dependence on changes in radius from the calibration experiment and simulations for the oxide-clad SiN_x filters.

Fig. 4.9(a) and (b) shows the frequency dependence on dose for each filter design compared to predictions using the binary model and string-propagation method, respectively. The graphs show that it is possible to make continuous frequency shifts by changing the electron-beam dose; one is not constrained by the discrete address grid. Also, the calibration experiment using PMMA matches up very nicely with the results

from the binary simulation, but the calibration using HSQ resist does not. This is what was expected since the binary model works well for high contrast resists like PMMA, but starts to break down for lower-contrast resists such as HSQ. The more rigorous string-propagation model, which is able to take contrast into account, predicts the frequency dependence for HSQ much better.

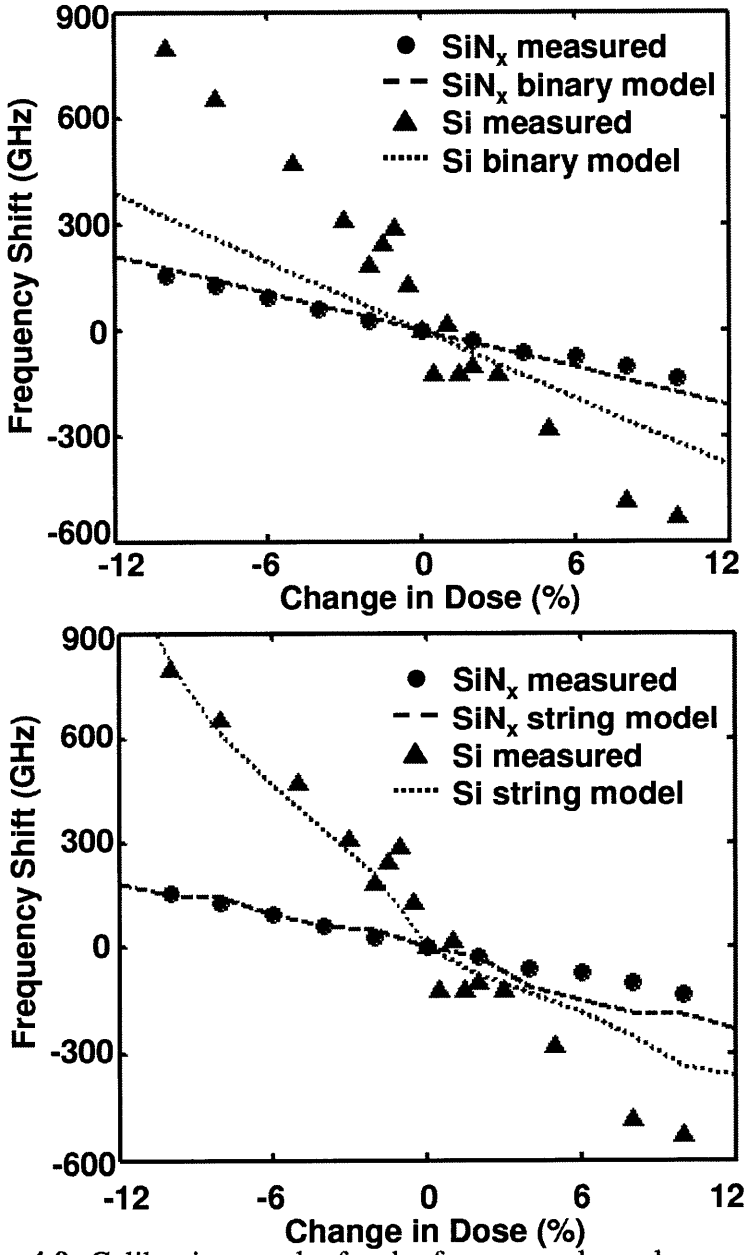


Fig. 4.9 Calibration results for the frequency dependence on exposure dose for the oxide-clad SiN_x and Si filters compared to the simulation results using the (a) binary model and (b) string propagation method.

It is important to note that there are limitations when varying the dose to control the resonant frequency of the microring. If the dose is varied by too much the resist will be either over exposed or under exposed, deteriorating the performance of the microring resonator. For best results, it is ideal to make large frequency shifts by changing the radius of the microring and then fine tune the frequency shifts by slightly changing the exposure dose. This makes it possible to achieve any desired frequency shift for any of these filter designs without having to deviate by more than 6% from the optimal exposure dose. Since the radius affects the physical path length and dose affects n_{eff} they can be treated as independent and added.

The standard deviation from the fitted frequency-dependence on dose for the SiN_x and Si filters was 8 GHz and 100 GHz, respectively. This variation comes from two main sources. The first source is short-term fluctuations of the electron-beam current. Although the calibration experiment is designed to cancel out long-term current drift it can not eliminated short-term fluctuations that can occur between the writing of the reference filter and the calibration filter. For this time scale, fluctuations on the order of 0.5% are possible. This can explain the 8 GHz standard deviation in the measured SiN_x filters and 32 GHz of the 100 GHz standard deviation of the Si filters. The second source is variation in the waveguide core thickness that occurs over the short distance between the reference filter and calibration filter. The SiN_x filter design is relatively insensitive to small changes of height and the LPCVD method used to deposit this film produces films with highly uniform thicknesses, so this source does not contribute significantly to the standard deviation of the SiN_x filters. On the other hand, the Si-filter design is extremely sensitive to changes in height, ~400 GHz/nm, and the fabrication process used to create

SOI wafers does not produce films with extremely uniform thickness. The SOI wafers used for these experiments have a 3-sigma height deviation of 15 nm over the 150 mm wafer. To explain the rest of the frequency standard deviation, the thickness of the Si would need to vary only 0.2 nm (approximately the lattice spacing of Si) over the 100 μm between the reference filter and the calibration filter. This would appear to be possible.

4.4 SCALE-UP

The fabrication technique described relies on SEBL to create the filter bank devices, which is a slow serial process. The low throughput of this process would make it suitable only for low level production of high-value chips, most likely for defense application. To truly transfer this method into mass production products, such as multicore processors, a path to scale-up needs to be found. In this section, four paths to scale-up are identified and explained, showing the possibility of using this technique to aid the mass production of filter banks. These methods utilize standard projection, nanoimprint, or maskless optical lithography to scale-up the process.

The clearest rout to scale-up is using standard projection lithography since this is the preferred lithography method for the mass manufacturing of integrated circuits. Projection lithography uses a mask that is designed to consistently reproduce the features. The projection masks are made using an SEBL systems so it may be possible to use the dose modulation technique to make slight changes in the dimensions of all the microrings on the optical mask. (Masks are generally made using projection electron-beam lithography rather than the SEBL described here. So dose modulation may not be

possible.) However, whatever slight changes are made should be replicated during the projection-lithography step. As an added benefit, the features on the mask are demagnified by 4X when exposing the photoresist. This means that if the average microring waveguide width had to be controlled to 25 pm it would only have to be controlled to 100 pm on the mask. A second way to use projection lithography is to add in dummy structures in the mask near the microring filters. By controlling the size of these dummy structures it would be possible to control the proximity effects, or added dose, that each microring sees. This method although feasible would require complex simulations since proximity effects in optical lithography depend on phase and intensity.

A third possible rout to scale-up is using nanoimprint lithography. Although not commonly used for integrated circuits it has been proven to precisely replicate fine features over a large scale [30]. In this method the SEBL dose modulation technique can be used to create the master imprint template, which will then be replicated through nanoimprint thousands of time, spreading out the cost of the template over many chips. An added advantage of using this method is that if there are frequency errors in the fabricated filter banks they can be measured and the master template can be altered using a focused-ion beam, to correct for dimensional errors. There are currently a few companies developing nanoimprint tools that are suitable for large-scale chip manufacturing [30,31].

A fourth possible rout to scale-up is using zone-plate array lithography (ZPAL) to fabricate the filter banks. ZPAL is a maskless optical lithography tool that uses an array of 1000 Freznel zone plates to focus individually modulated beamlits of light [32]. Since each beamlit can be individually modulated the exposure dose can be controlled precisely

for each microring filter. The number of zone-plates allows for massive parallelizing of the exposure, reducing the exposure time greatly. This is ideal for mid-volume production since there is no high-cost mask or template that must be amortized over a large number of chips. Parallelism allows for much faster production than single-beam serial methods such as SEBL.

4.5 CONCLUSION

We have shown that it is possible to precisely shift the resonant frequency of microring-resonator filters by making dimensional changes in the layout and by changing the electron-beam exposure dose. The resonant frequency shifts due to dimensional changes in the layout are limited to relatively large discrete shifts due to the finite size of the SEBL address grid. We have shown that this limitation can be overcome by varying the electron-beam dose in order to change the average ring waveguide width with a precision on the tens of picometer scale. Using a binary resist model it is possible to simulate the resonant frequency dependence on dose for high-contrast resists, such as PMMA. For low-contrast resist, such as HSQ, the more rigorous string-propagation method is used to simulate the resonant frequency dependence on dose. These simulations agreed well with data from calibration experiments. Also, due to the small exposure dose window it is best to make large frequency shifts by changing the radius of the microring and then fine tune the shift by slightly changing the exposure dose. We have also described possible routes for scaling-up this technique for high-volume manufacturing.

Chapter 5

Postfabrication Tuning

5.1 INTRODUCTION

To fabricate a filter bank with channel spacings that are accurate to within 1 GHz requires dimensional control of a few tens of picometers. Due to stochastic variations during processing this is not possible for a large number of channels, or many filter banks. Even if fabrication was perfect, the channel spacing can still change due to localized temperature fluctuations, which can be significant in some devices. Ideally, one would have a means to tune the resonant frequency of each microring after fabrication, to correct for any fabrication errors, temperature gradients and fluctuations. It is important that whatever tuning method is used not significantly affect any other property of the microring-resonator-filter response, including the drop loss and 3 dB bandwidth.

Methods for tuning the resonant frequency can be either dynamic or static. Dynamic tuning refers to methods that are completely reversible and can be changed relatively quickly. Examples of dynamic tuning include carrier injection, evanescent field perturbation, compression, and thermal tuning. For the carrier injection method a PIN junction must be fabricated were the ring waveguide is the intrinsic center region. By biasing the junction it is possible to change the carrier density in the ring waveguide,

slightly changing the refraction index [10]. The problem with this method is that the loss of the filter increases with carrier concentration. The method of evanescent field perturbation works by bringing a dielectric probe into close proximity of the microring, slightly changing the effective index. This can be done with an external probe or an integrated MEMS structure. The major problem with this method is that it requires the probe to be in very close proximity to the microring where van der waals forces can be significant, possibly attracting the probe to the ring [33]. If contact is made it can require significant force to remove the dielectric probe. It is also possible to change the resonant frequency by compressing the microring. This tuning method is, however, very inefficient since it takes a relatively large force to compress the ceramic and semiconductor materials typically used for the microring core [33]. Thermal tuning, takes advantage of the temperature dependence of the refractive index. The usefulness of this method depends on the thermal efficiency and crosstalk of integrated microheaters.

One key characteristic of all the dynamic tuning methods is that they consume power when in operation. Static tuning methods, on the other hand, are irreversible and therefore only require energy for initially tuning. The two major forms of static tuning change the refractive index of the low-index cladding layer. The most common way is to use a polymer as the cladding material that has a refractive index that is sensitive to UV light [34]. One can then locally expose the polymer, near each ring, with the dose of UV radiation needed to tune the resonant frequency. One disadvantage of this method is that UV light is typically used for optical lithography so any further lithography processing steps could change the resonant frequency of the filters. An alternative is to use HSQ as the overcladding material and then locally expose it with an electron beam. When HSQ

is exposed by an electron beam it undergoes chemical and structural changes that increase the refractive index.

5.2 DYNAMIC TUNING WITH MICROHEATERS

For the microring resonator filter banks in this project thermal tuning with resistive microheaters was used as the dynamic tuning method. Thermal tuning shifts the resonant frequency via the thermo-optic coefficient ($\Delta n/\Delta T$), which is $2.4*10^{-4}$, $4.0*10^{-5}$, and $1.5*10^{-5}$ K^{-1} for Si, SiN_x, and SiO_2, respectively The figures of merit for tuning with microheaters are the tuning efficiency, optical loss, tuning range and crosstalk. To increase the tuning efficiency, and lower the crosstalk it is desirable to place the heater as close as possible to the microring resonator. Since the heater is made from a conductive material there will be excess loss due to optical absorption if the evanescent field of the resonant mode couples to it. This would decrease the intrinsic quality factor for the microring, as seen in Fig. 5.1. Therefore, when choosing the distance the microheater is above the microring, a compromise between tuning efficiency and optical loss must be made.

The maximum range over which the heater can tune the resonant frequency, sets a limit on the maximum fabrication errors that can be tolerated. Ideally, one would like to be able to tune the resonant frequency over the entire FSR of the microring. However, the range is limited by the maximum temperature of the heater before failure. The two modes of failure are oxidation and electro-migration. Oxidation can be prevented by capping the microheater with an oxygen diffusion barrier. It is important that this

diffusion barrier have a low thermal conductivity so as not to increase the thermal crosstalk between heaters. Preferably, heaters should perform independently of one another. If the heaters are covered by an oxygen barrier layer that has a high thermal conductivity the barrier layer will spread the heat over a large area, increasing the thermal crosstalk between heaters. By choosing the right material combination for the barrier layer it is possible to prevent oxidation while maintaining low crosstalk.

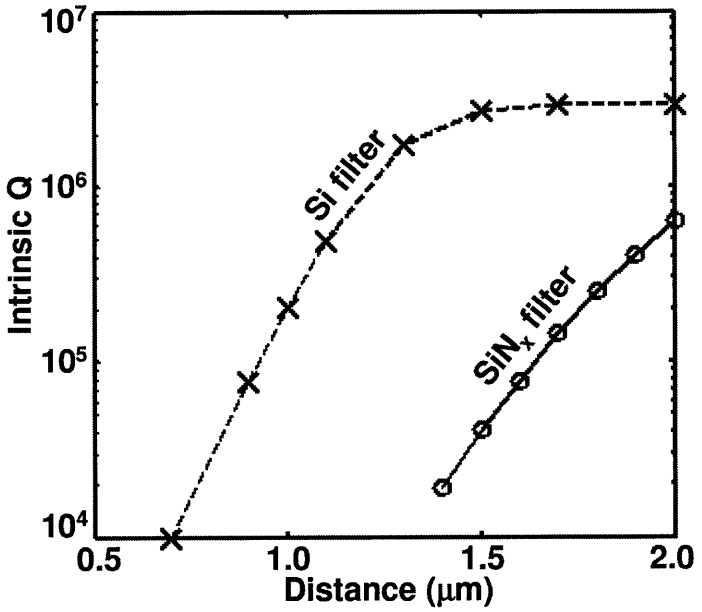


Fig. 5.1. The effects on the internal quality factor for the SiN_x and Si filter designs with Ti as a function of at distance measured from the bottom of the microring waveguide. Propagation loss in the core material is ignored in these calculations.

5.2.1 Heater Fabrication

After the photonic structures are overclad, using the optimized HSQ process described in Chapter 7, the sample is ready for heater fabrication. One of the key benefits of using HSQ to overclad the photonic structures is that it produces a planar surface so

step coverage is not a concern. The microheaters pattern is defined using contact lithography. First NR-9, a chemically-amplified dyed resist, is spun onto the overclad sample and baked on a hotplate at 150°C for 60s. Next, the microheater features on the mask are aligned to the microring filters on the sample. The sample is then brought into intimate contact with the mask, as evidenced by the disappearance of the Newton interference rings. The resist is then exposed with 400 nm light with an energy dose of ~1 mJ/cm^2. The sample is then baked at 80°C for 30 min in a convection oven. Next, the resist is developed in RD6, a commercial TMAH-based developer, for 30 s followed by a 60 s dip and thorough rinse in DI water. Then 100 nm of Ti and 10 nm of Au are deposited on the sample using e-beam evaporation. The sample is then immersed in RR5, a solvent-based resist remover, at 70°C, lifting off the unwanted metal, leaving only the microheaters and electrical leads. This process is repeated to form metal pads consisting of 10 nm Ti and 100 nm Au so that the sample can be wire bonded to a printed-circuit board, allowing the possibility of powering many microheaters at the same time (Fig. 5.2). This is necessary since a single filter bank may have as many as 40 heaters, which would be virtually impossible to power simultaneously using only probes.

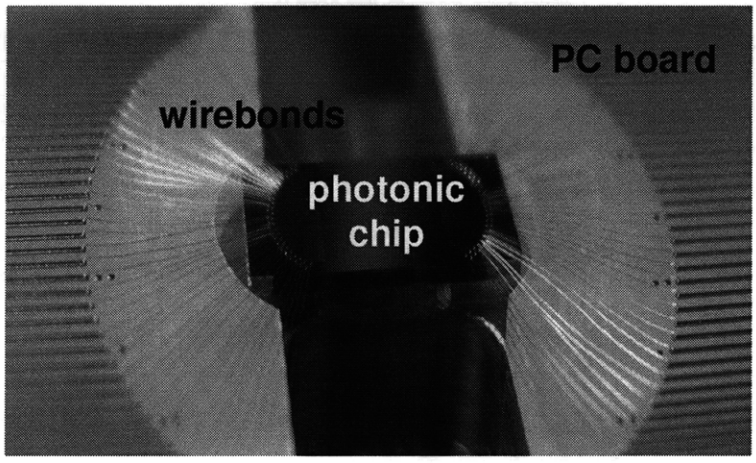


Fig. 5.2. Wirebonded photonic chip with 92 electrical connections.

Titanium is chosen for the microheater material because of its relatively high electrical resistance. This enables the width of the lines of the resistive heaters to be of the order of 1 μm. The only problem with titanium is that it reacts readily with oxygen, making it imperative to install a good oxygen diffusion barrier. A 10 nm gold cap was placed above the titanium heater but this alone is not enough to prevent oxidation. When looking for oxygen diffusion barriers for this application it important to have low oxygen diffusion and low thermal conductivity. To achieve this, a bilayer of 100 nm of SiO_2 and 50 nm of Si_3N_4, deposited by sputtering, was used. The SiO_2 was placed above the microheaters to limit thermal conductance, but since oxygen diffuses relatively quickly through SiO_2, a second layer of Si_3N_4, which has low diffusion of oxygen, was used. Si_3N_4 could not be used by itself because of its relatively high thermal conductivity.

5.2.2 Tuning Performance

The efficiency of the thermal tuning was calculated by measuring how far the resonate frequency of the microring shifts for a given input power. For the oxide-clad SiN_x filters a heater design that is optimized for tuning efficiency, shown in the inset of Fig 5.3, was used [35]. From the tuning data it is found that this heater has a tuning efficiency of 80 μW/GHz, slightly worse than the theoretical efficiency of 60 μW/GHz. The main reason for the slight difference between the measured and theoretical efficiencies is that the fabricated heater was misaligned with respect to the filter by ~2 μm. This increased the power necessary for a given frequency shift by 33%.

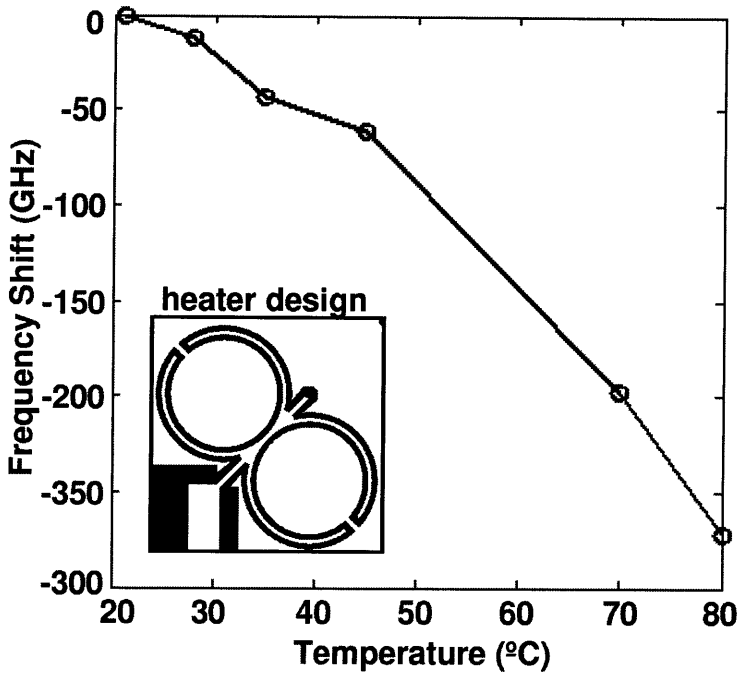


Fig. 5.3. Frequency shift of a second-order SiN_x filter for a given change in heater temperature. (inset) layout of microring heater design optimized for efficiency.

For the Si filters a heater design, optimized for maximum tuning range, was used (inset of Fig. 5.4) [36]. This heater design heats an area significantly larger than the microring, reducing its efficiency, but increasing the tuning range of the filter for a given maximum heater temperature. It also makes the tuning performance less sensitive to alignment errors. Using this heater design it is possible to tune a Si microring resonator over a range of 2.3 THz, which is larger than its 1.6 THz FSR (Fig 5.4). Although the heater was not optimized for tuning efficiency it still outperformed the SiN_x heater with an efficiency of 17 μW/GHz. This better performance is attributed mainly to the fact that the thermo-optic coefficient of Si is 5 times larger than that of SiN_x, and the required distance between the heater and microring is significantly smaller. With a Si heater

design optimized for efficiency, it should be possible to achieve a tuning efficiency of better than 10 μW/GHz.

The thermal crosstalk of the Si heaters design was also measured. For rings located in the same filter the crosstalk between heaters was 3%, and the crosstalk between heaters on neighboring filters, located 100 μm apart, was negligible.

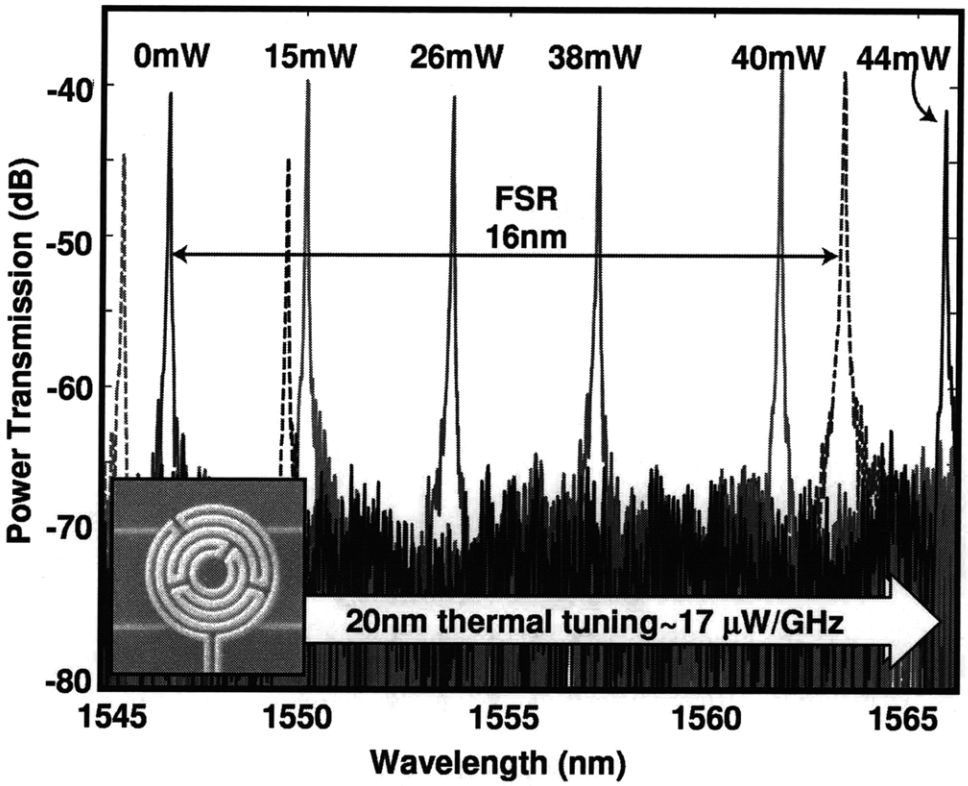


Fig. 5.4. Transmission response of first-order Si filter demonstrating tuning over 20 nm (2.3 THz). (inset) Micrograph of integrated microheater optimized for maximum tuning range.

5.3 STATIC TUNING WITH ELECTRON-BEAM CURING

In addition to dynamic tuning it is desirable to also have a method of statically tuning the resonant frequency of an individual microring. Static tuning does not require any power to maintain the resonant-frequency shift. Previous efforts for static tuning have focused

on using a UV sensitive polymer as the overcladding material, and exposing it to UV radiation to cause a change in the refractive index [34]. Since a significant portion of the resonant mode propagates in the cladding material outside the core, this results in a resonant-frequency shift. Although this method works it is not viable for CMOS-compatible integrated photonics. One problem is that organic polymers are generally not allowed in a CMOS process flow. Another is that UV light is used during optical lithography which could result in unwanted shifts in the resonant frequency during additional lithography steps.

An alternative method presented here is to use HSQ as the overcladding material and locally cure it with an electron beam. When HSQ ($HSiO_{3/2}$) is subjected to electron-beam irradiation Si-H bonds are broken, resulting in a change in density and transformation from a cage-like to a network structure. (Diagrams of these structures are shown in Fig. 7.1). Since the refractive index depends on molecular composition and free volume, these reactions should cause a change in the refractive index. Simulations using a 2D cylindrical mode solver have been performed to find how the resonance frequency of the Si filter depends on the refractive index of the overcladding material, for overcladding thicknesses of 110 nm and 1 000 nm (Fig. 5.5). It is seen here that just a small change in the refractive index of the overcladding material can cause significant shifts in the resonant frequency

For HSQ films prepared using a prebake of 150°C and 200°C for 2 min on consecutive hotplates it is possible to change the index of refraction from 1.38 to 1.40 with an electron-beam dose of 1.2 mC/cm^2 [37}. Based on the simulation this will result. in a resonant frequency shift of ~300 GHz. Using doses higher than 10 mC/cm^2 at

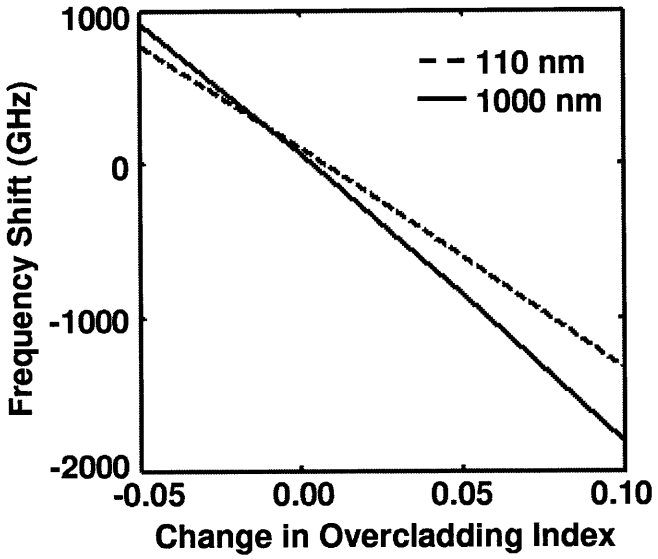


Fig. 5.5. Simulated frequency shifts for given change in overcladding refractive index for Si filters with 110 nm and 1000 nm thick overcladding layer.

elevated temperatures it is possible to form Si-rich films that can have refractive indices as high as 1.62 [38].

To experimentally find the resonant frequency dependence on the exposure dose used to cure the HSQ overcladding, a layout consisting of many sets of two first-order microring-resonator filters was used. The two filters, one a reference and one a calibration filter, have slightly different radii and share the same through port. The fabricated test structures were then overclad with 110 nm of HSQ and baked at 90°C to remove the solvent. The resonant frequencies of all the filters were then measured. Next, the HSQ overcladding of the calibration filter was electron-beam cured using a dose ranging from 0.1 to 5 mC/cm^2. The resonant frequencies of all the filters were measured again and, by comparing the change in resonant frequency difference between the calibration and reference filters on the same through port, before and after electron-beam curing, it is possible to calculate the resonance-frequency shift. This is shown in Fig. 5.6

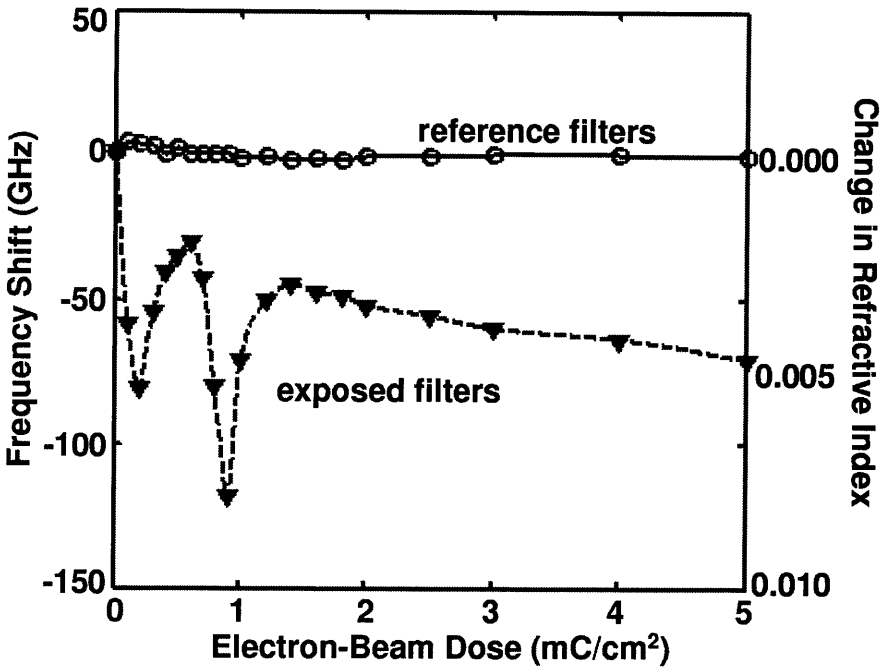


Fig. 5.6. Change in resonance frequency of microring filter after electron-beam curing 110 nm thick HSQ overcladding with different doses. Reference filters receive no dose and the frequency shift of the exposed filter is normalized to the reference filter.

as a function of the electron-beam dose. The overall trend is a decrease in the resonant frequency, which corresponds to an increase in the index of refraction of the HSQ film. Below 1400 $\mu C/cm^2$ the resonant frequency fluctuate quite rapidly. This is due to chemical reactions and structural changes that occur at lower doses. First at the lowest doses the main reaction is Si-H scissions causing densification of the caged oligomer film. As the dose is increased further, more Si-H bonds are broken causing a transformation from the cage oligomer to the network structure. The network structure has more free volume than the caged oligomer, resulting in an increased resonant frequency. As the exposure dose is increased further the network structure slowly converts to SiO_2, increasing the refractive index and therefore resulting in a decrease in the resonant frequency. As this reaction progresses further, Si starts to leave the film in the form of SiH_4, resulting in a decrease in the films density and a corresponding increase

in the resonant frequency. For electron-beam doses above 1400 $\mu C/cm^2$ all chemical reactions have already gone to completion and the linear decrease in the resonant frequency is attributed to densification of the network structure.

For statically tuning the resonant frequency of a microring resonator it is best to operate in the linear regime at high curing doses. For the range of doses used it was found that the weighted Q of the microrings, 7 750, did not change significantly, showing that this method does not dramatically increase the loss of the microring. Ideally, this method would be combined with thermal tuning, i.e., statically tuning with electron-beam curing all large resonant frequency errors and then thermally tuning smaller errors.

5.4 CONCLUSION

Due to the high level of dimensional accuracy needed to fabricate microring-resonator filter banks with a resonant frequency spacing accuracy better than 1 GHz, postfabrication tuning is required. We have demonstrated two types of tuning, dynamic tuning with integrated microheaters and static tuning using electron-beam curing of HSQ. Using integrated microheaters tuning efficiencies of 80 μW/GHz and 17 μW/GHz were achieved for the SiN_x and Si filters, respectively. Also, the crosstalk between heaters for different rings of the same filter was measured to be 3% and the crosstalk between heaters for neighboring filters was negligible. Using electron-beam curing of HSQ to change the index-of refraction for the overcladding materials it is possible to statically tune the resonate frequency. This method has the advantage of requiring no power to maintain the frequency shift.

Chapter 6

Microring-Resonator Filter Banks

6.1 INTRODUCTION

To maximize the value of integrating photonics with electronics, wavelength-division multiplexing (WDM), (transporting several optical signals through a single waveguide on several different wavelengths) is typically used [12]. This creates the need for filters to separate the signals (demultiplex) and combine the signals (multiplex). Currently, in discrete-component photonic systems this is done with arrayed-waveguide gratings, the large size of which greatly limits their integratability. The WDM filtering functions can be achieved using a bank of microring-resonator filters that have resonant frequencies corresponding to each of the several wavelengths. In HIC material systems, such as silicon-on-insulator, these microring resonators can have radii as small as 1.5 μm, making them ideal for integration [13].

The figures of merit when analyzing the performance of a microring-resonator filter bank are the number of channels, crosstalk between channels, optical loss, and

Parts of this chapter were featured in:

C.W. Holzwarth, A. Khilo, M. Dahlem, M.A. Popović, F.X. Kärtner, E.P. Ippen, and Henry I. Smith, "Device Architecture and Precision Nanofabrication of Microring- Resonator Filter Banks for Integrated Photonic Systems," Submitted to J. Nanosci. Nanotechnol., (2009)

frequency-spacing accuracy before and after postfabrication trimming. The first part of this chapter focuses on the architecture of microring-resonator filter banks, with the goal of maximizing performance while limiting fabrication challenges. This includes choosing the optimal filter design and core material. In the second part of this chapter the measured results of fabricated SiN_x- and Si-core microring-resonator filter banks are presented and discussed.

6.2 DEVICE ARCHITECTURE

The four most important characteristics of the microring-resonator filter design for a filter bank are the FSR, 3 dB bandwidth, internal quality factor, drop-loss, and roll-off. The FSR, or frequency spacing between resonances of the same microring, defines the maximum frequency range that can be used by a filter bank. The 3 dB bandwidth of the filter is the width of a single channel. It also defines the theoretical maximum channel density, since for even a perfect box filter response (infinite roll-off) the channel spacing can never be less than the 3 dB bandwidth. The drop loss of the filter is the sum of the power that is not filtered out of the waveguide and is lost during the filtering operation. This determines the efficiency of the filter bank and, for most applications, should be less than 3 dB. The 3 dB bandwidth and the drop-loss are related by the internal quality factor (Q_{int}). Q_{int} of a microring resonator is a measure of the rate of energy dissipation in the ring, normalized to the resonant frequency. Q_{int} is inversely proportional to the intrinsic loss of the microring due to material absorption, sidewall roughness, and bending loss. The minimum 3 dB bandwidth achievable with less than

3 dB of drop loss is twice the resonant frequency divided by Q_{int}. The last important feature is the filter's roll-off, i.e., how quickly the filter response's power is reduced outside the 3 dB bandwidth. The roll-off of the filter ultimately defines the minimum channel spacing of the filter bank needed to achieve the required level of crosstalk.

6.2.1 Filter Design

To maximize the performance of a filter bank, it is necessary to maximize the number of channels that fit into one FSR while maintaining minimal crosstalk. To do this, it is desirable to decrease the filter's bandwidth and increase the filter's order (i.e., the number of series-coupled rings) to take advantage of the sharper roll-off. For most application less than -30 dB crosstalk between adjacent channels is required. This, in turn, implies a minimum channel spacing of ~21, ~3, and ~2 times the filter's 3 dB bandwidth for first, second and third-order filters, respectively. The channel density increase when switching from first- to second-order filters is quite large (7x) and the increase in fabrication challenge is minimal. On the other hand, the increase in channel density, from second- to third-order filters is much smaller (1.5x). This increase in channel density becomes exponential less as the order is increased, with the channel density of an infinite-order filter being ~2 times the density of third-order filters.

As the order is increased in HIC microring filters the fabrication challenges increase dramatically due to coupling-induced frequency shifts (CIFS) and proximity effects. The resonant frequency of an uncoupled and a coupled microring resonator with the exact same dimension have different resonant frequencies due to CIFS. This occurs

because the coupling through the evanescent field changes the proximate environment of the field, locally modifying the effective index of refraction, resulting in a frequency shift. In first-order and second-order microring filters this is not a problem since the coupling environment for each ring is identical. For third- and higher-order filters the coupling environment is not the same for all rings, as illustrated in Fig. 6.1. Dimensionally identical rings will not have identical resonant frequencies due to different CIFS contributions. Similarly, proximity effects during SEBL when writing microrings or waveguides in close proximity can cause dimensional changes and, therefore shift

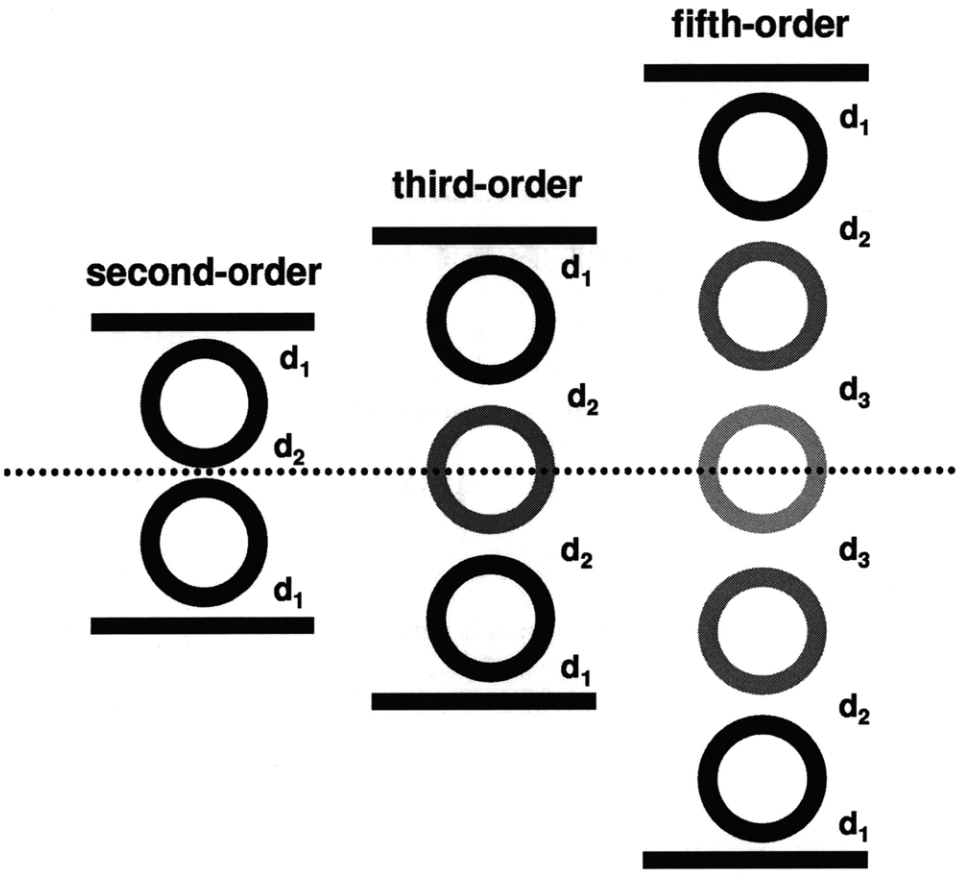


Fig. 6.1. Schematic of second-, third-, and fifth-order microring resonator filters. Although all rings have the same dimensions their frequencies are different due to CIFS and proximity effects shown by different shading. d_n in the figure represent different coupling gaps.

the resonant frequency of each microring. For first- and second-order filters one can design the layout with geometric symmetry about every microring so that the SEBL proximity effects are identical for each microring. This is not possible for third- and higher-order microring filters (Fig. 6.1). Therefore, to maximize the roll-off with a minimal increase in fabrication challenges, second-order filters are the logical choice for filter banks.

6.2.2 Material Selection

Choosing second-order filters for the filter bank fixes the minimum channel spacing required to achieve less than -30 dB crosstalk to about 3 times the 3 dB bandwidth of the filters. Thus, to increase the number of channels in the filter bank the 3 dB bandwidth of the filters must be reduced and/or the FSR increased. As mentioned previously, the minimum bandwidth of a microring filter is limited by Q_{int}, and to keep

Table 6.1 Material and Filter Bank Properties for Selected CMOS Materials

Material	Index of Refraction	Index Contrast[1]	Thermo-Optic Coeff. ($*10^{-5}$ K^{-1})	Propagation Loss (dB/cm)	Maximum FSR (THZ)	Maximum Channels
SiO_2	1.44	0%	1.5	<0.01	0	0
SiON	1.44-1.98	0-23%	1.5-2	0.1	0-1.0	~30
Si_3N_4	1.98	23%	2	~1.0	1.0	~30
SiN_x	2.19	28%	4	7.5	2.2	~30
a-Si	~3.73	43%	~24	0.5[2]	5.5	>128
poly-Si	~3.5	41%	~24	4.0[2]	5.5	>128
SOI	3.48	41%	24	2.0	5.5	>128

[1] Index contrast calculated assuming SiO_2 cladding
[2] Best reported in literature, typical values range from 10-100 dB/cm

the drop loss below 3 dB the bandwidth must be at least twice this minimum. Table 6.1 lists the material properties and resulting filter-bank properties for some common CMOS-compatible materials. Of these materials, both SiN_x and crystalline Si appear to be most suitable for filter bank application.

For microring resonators with a SiN_x core and oxide cladding, and a Q_{int} of ~50 000 (propagation loss of ~7.5 dB/cm), it is possible to have a FSR of 2.2 THz (2.5 THz if air-clad) and a bandwidth of 25 GHz, resulting in a filter bank with a maximum of 29 channels. The higher index contrast of oxide-clad Si microrings allows for a much larger FSR of >5.0 THz. Also, due to the lower intrinsic loss of Si microrings, (Q_{int} of 200 000 and larger are routinely reported [39, 40]) bandwidths smaller than 5 GHz are theoretically achievable, resulting in a maximum of >332 channels. This improvement by switching from SiN_x to Si comes at price since the resonant frequency of Si microrings is a factor of 1.5-10 times more sensitive to changes in the microring waveguide dimensions, depending on the exact design.

The height of the waveguide is defined by the thickness of the top silicon layer of the silicon-on-insulator (SOI) substrate. This thickness can be controlled with oxidative thinning and measured very accurately with an ellipsometer. The microring-waveguide width, however, is defined during fabrication, and is much harder to control and measure at the required sub-nm level. To minimize the frequency sensitivity to microring-waveguide width, a design was chosen that called for heights to widths of 105 X 600 nm and 105 X 500 nm for the microring and straight waveguides, respectively. For these cross sections, the frequency sensitivity to average ring-waveguide width, 40 GHz/nm, is 2.5 times less than for a typical Si-waveguide cross section and only 1.6 times more

sensitive than for the SiN_x design used. Choosing this cross section reduces slightly the achievable FSR to 3.5 THz, due to increased bend radiation loss, but still theoretically allows for over 128 channels within a single FSR. For the ultra-fast ADC system the filter FSR has to be larger than 2.0 THz, the spectral width of the femtosecond laser pulse, and the desired number of channels is only 20. This is possible to achieve using the SiN_x and Si second-order microring designs previously described in chapter 3.

6.2.3 Counter-Propagating-Mode Design

Another way to increase the performance of a filter bank is to use the 2 contra-propagating modes of each filter. At a given resonant frequency a single microring resonator supports two resonant modes; one propagating clockwise and the other propagating counter-clockwise. Back reflections from sidewall roughness can allow these two modes to couple, causing the resonant peak to split [41]. However, efforts to reduce surface roughness can eliminate such problematic back reflections in HIC microrings, eliminating any coupling between the two modes. This means that through clever design it is possible to take advantage of the contra-propagating modes and multiplex/demultiplex two signals at the same time. This has been demonstrated already in an arrayed-waveguide-grating demultiplexer for a polarization-diversity scheme, eliminating the need for two identical demultiplexers for each polarization [42].

Fig. 6.2 compares a double-filter bank using one mode and a single filter bank making use of the contra-propagating mode. The functionality of these designs is exactly the same, in the respect that they can multiplex/demultiplex two twenty-channel signals

at the same time. There are three main benefits of the contra-propagating mode design. The first is that the footprint of the filter bank is decreased by a factor of two, which is important for integrated applications. The second is that when using two separate filter banks there is always going to be some fabrication differences, causing the resonate frequencies of one filter bank to not align exactly with the other. This is not the case for the contra-propagating mode design since the signals use the same filter bank, resulting in the resonant frequencies being exactly aligned. The third benefit is that simply by reducing the number of rings needed by a factor of two reduces the amount of power, on average, that is needed to tune and maintain the filters at the correct resonant frequencies.

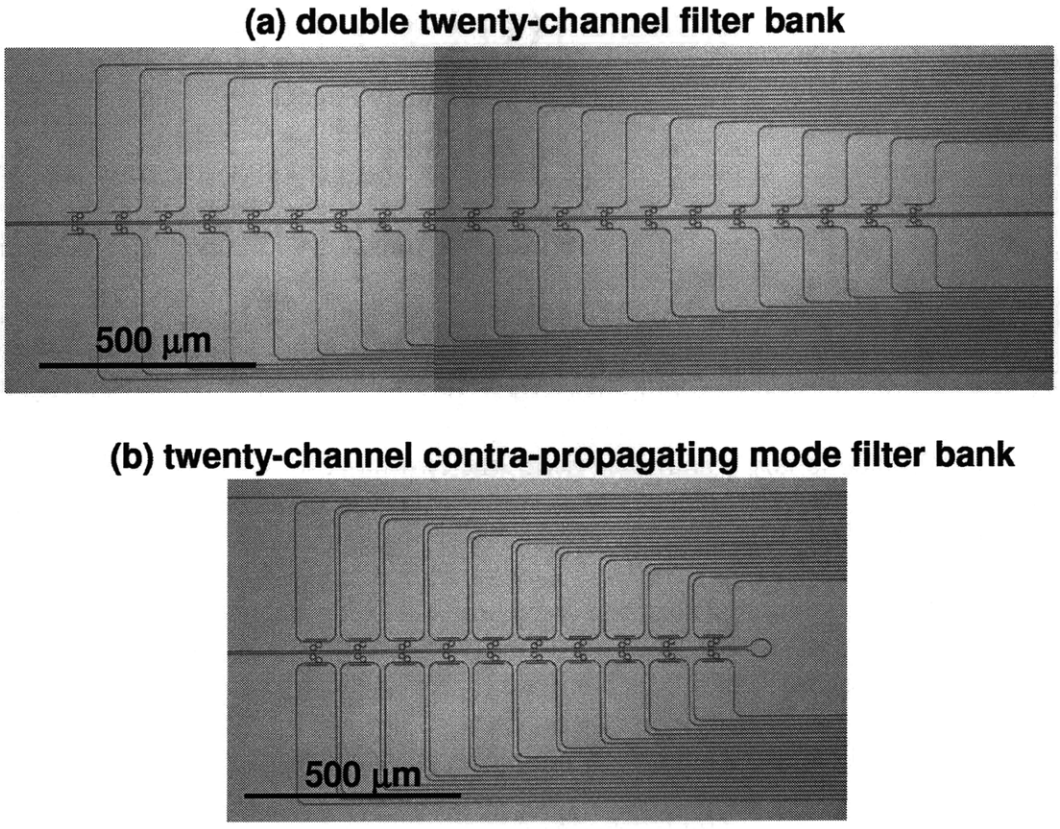


Fig. 6.2. Top-view optical micrograph of a (a) double twenty-channel filter bank and (b) twenty-channel contra-propagating mode filter bank. Both filters are capable of multiplexing/demultiplexing two twenty-channel signals simultaneously.

For the contra-propagating design to work, the crosstalk between the two modes due to back reflections in the microring must be less than -30 dB. A simple experiment using a first-order Si microring resonator was performed to measure the crosstalk between the two modes, as well as to check that the resonances of both modes are identical (Fig. 6.3a). The measured transmission response for both modes shows that they have identical resonant frequencies and bandwidths (Fig. 6.3b). However, the

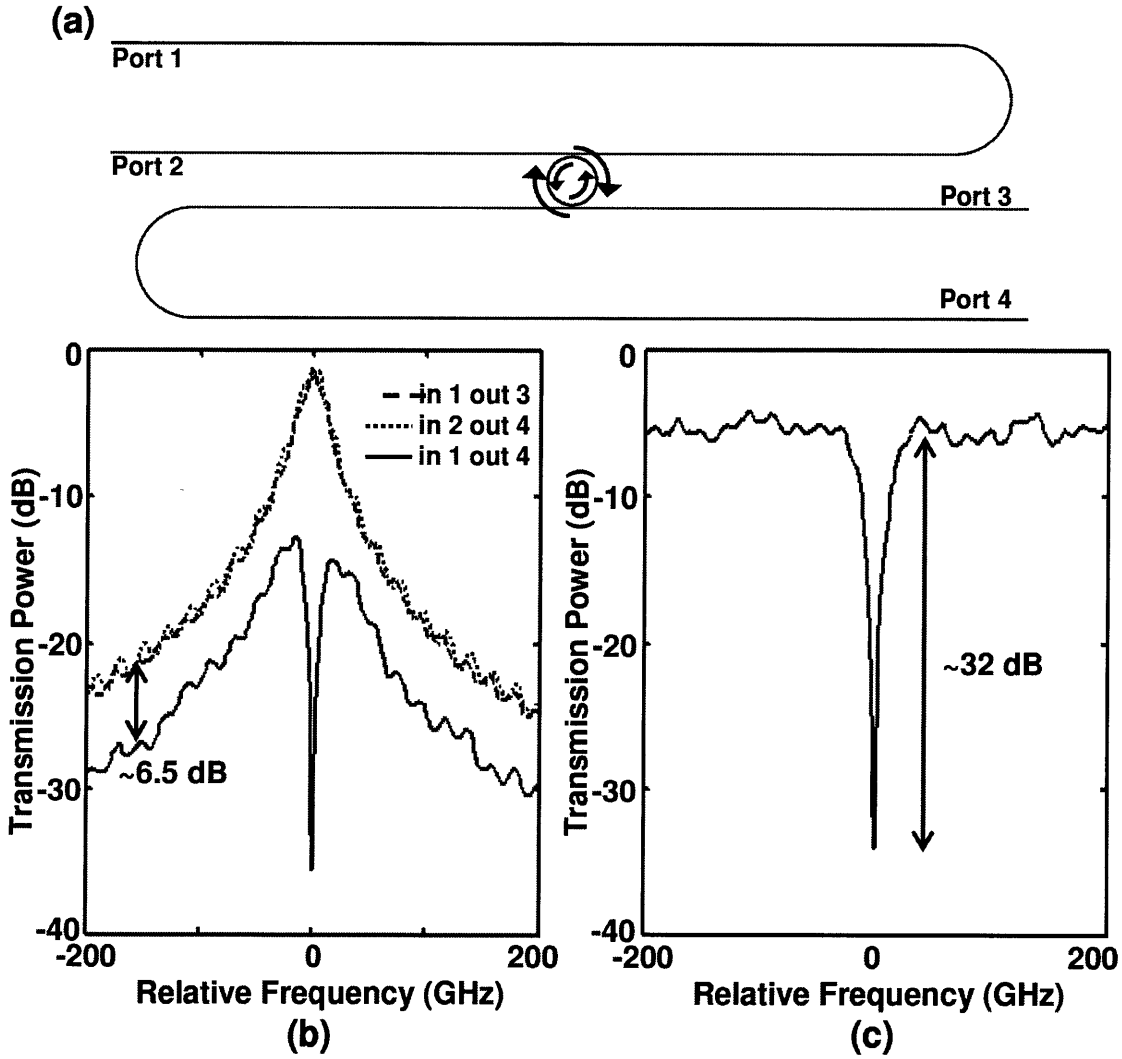


Fig. 6.3. (a) layout of first-order microring-resonator filter. (b) Transmission response of both propagating modes and crosstalk. (c) Plot of the crosstalk with the drop factored out, demonstrating ~32 dB extinction at the resonant frequency.

crosstalk is measured to be -6.5 dB, much higher than expected. Looking more closely at the crosstalk it is seen that it is the sum of the drop and through response of the filter, not what would be expected if it was due to coupling between the two contra-propagating modes in the ring. There are two ways that this sum can occur. The first is that some of the light that travels past the filter, but is not dropped, reflects off the end facet and then travels back towards the microring where part of it gets dropped and measured as crosstalk. The second way is that some of the light that gets dropped by the filter reflects off the output end facet and travels back past the ring, yielding a through response, that is then measured as crosstalk. This can be eliminated by reducing the reflections at the end facets, by adding horizontal couplers and using index-matching fluid. By subtracting the filters drop response from the measured crosstalk all that is left is the through response and the crosstalk of the contra-propagating modes (Fig 6.3c). Since this through response has 32 dB extinction at the resonant frequency, the crosstalk between the counter propagating modes must be less than -32 dB.

6.3 SiN_x FILTER BANKS

Using the SiN_x material as a core, three filter banks were fabricated using the process and designs described in chapter 3. The first filter bank was fabricated using the 50 GHz 3dB-bandwidth air-clad filter design; it contains eight channels. The second filter bank consisted of two identical twenty-channel filter banks side-by-side using the 25 GHz-bandwidth oxide-clad design. The third filter bank consisted of only two channels but demonstrated the possibility of using thermal trimming to correct resonant frequency

errors. The resonant-frequency spacings were achieved by making calibrated changes in microring radius and electron-beam exposure dose, as is discussed in detail in chapter 4.

6.3.1 Eight-Channel Filter Bank

Fig. 6.4 shows the measured transmission response of the eight-channel filter bank. The target channel spacing and 3 dB bandwidth for this filter back were 150 GHz and 50 GHz, respectively. To achieve this resonant frequency spacing, the radius was increased by 6 nm (1 address-grid point) and the exposure dose was increased by 3.9% from one microring filter to the next. The actual average channel spacing of the fabricated filter bank was 159 GHz, 6% larger than the targeted spacing. This offset is

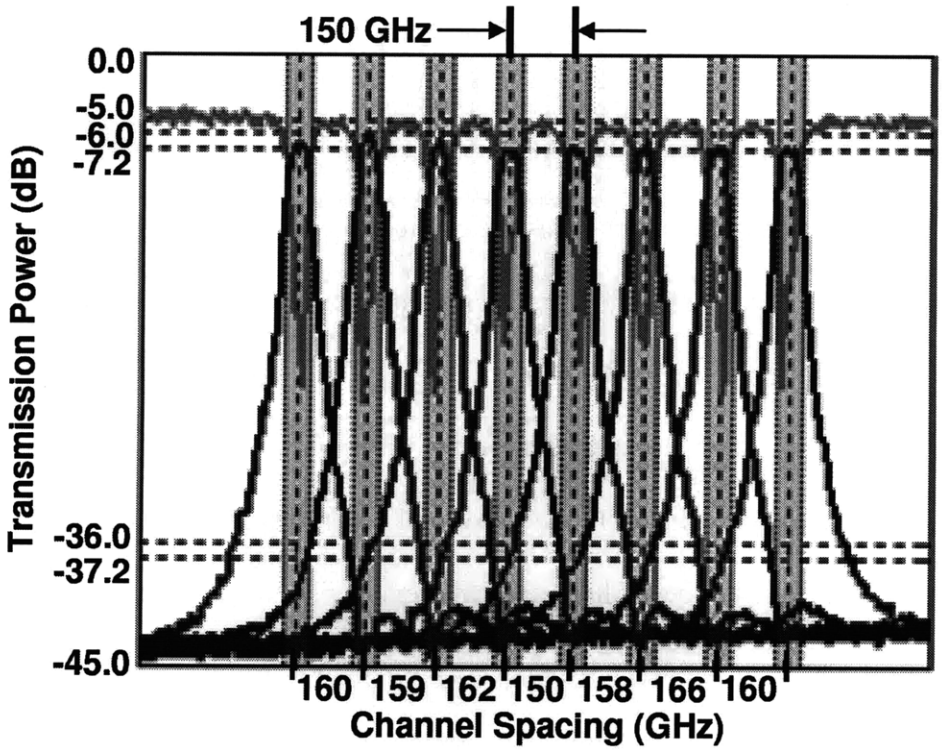


Fig. 6.4. Transmission response of eight-channel filter bank comprised of the air-clad SiN_x filter design.

due to a difference of 0.8 GHz/nm between the resonance-frequency dependence on specified radius at calibration and what was actually seen in the filter banks. This is within the error of the calibration experiment, which is calculated to be ~1.0 GHz/nm. The calibration of the resonant frequency dependence on dose was found to be even more accurate. The average change in microring-waveguide width due to dose is measured to be 0.34 nm per 1% increase in dose compared to 0.35 nm measured at calibration. This means that the change in average ring waveguide width per percent exposure dose increase varied by only 10 pm between the calibration experiment and the filter bank fabrication. This demonstrates that the technique of dose modulation, after empirical calibration, has the accuracy needed to fabricate filter banks based on HIC microring resonators with channel spacings that are not limited by the SEBL system's discrete address grid.

Controlling the exposure dose was also successful in correcting for the resonant frequency mismatch in the second-order filters caused by intrafield distortions. Although the filter design is symmetric, small distortions in the SEBL address grid cause the two microring to have slightly different resonant frequencies. Without using the electron-beam dose to compensate for this effect the filters would have a frequency mismatch of 8 GHz, which is equivalent to an average ring waveguide width difference of 0.24 nm (240 pm) between the two rings. In the fabricated filter banks the frequency mismatch is random in nature with the best filters having average ring waveguide widths that match within 23 pm. The reason that the average ring-waveguide-width mismatch is not 23 pm in all filters is due to uncontrollable, but very small, process variations. These process

variations resulted in a standard deviation of the average ring waveguide width of 0.12 nm (120 pm).

The 46.6 GHz bandwidth measured in the individual filters of the filter banks is very close to the designed 50 GHz bandwidth. The bandwidth is determined mainly by the coupling strength between the bus and ring waveguides, which is very sensitive to the filter's dimensions at the coupling region. Therefore, this small difference between the designed and measured bandwidths suggests that the dimensions of the fabricated filters are very close to the design values. Using the Raith 150 in scanning-electron-microscopy mode, absolute dimensions of the filters were measured, with 5 nm absolute accuracy, and compared to the targeted dimensions. The ring waveguide, bus waveguide, and bus-to-ring coupling gap widths were measured to be 897, 700, and 166 nm, respectively. All of these measurements are within the 5 nm measurement error to their designed dimensions, demonstrating the high level of absolute dimensional control achieved in the fabricated filters.

The low drop loss of 1.5±0.5 dB measured in the filter banks is much better than the system requirement of 3 dB. The major source of this loss is the propagation loss in the ring waveguide. From the internal quality factor (Q_{int}) of 53 000, measured in large, weakly coupled rings, the propagation loss is calculated to be 7.7 dB/cm, due mainly to absorption in the SiN_x. The SiN_x absorption loss was measured in an independent experiment employing shallow-etched ridge-waveguide paperclip structures to be 8±2 dB/cm. Accounting for the difference in modal overlap between the ridge waveguides and the rectangular waveguides employed in the filters, the propagation loss expected due to material absorption alone is 6±2 dB/cm

6.3.2 Twenty-Channel Dual Filter Bank

Fig. 6.5 shows the measured transmission response of a double twenty-channel filter bank using the oxide-clad SiN_x design. The target channel spacing and bandwidth were 80 GHz and 25 GHz, respectively. The average channel spacing was measured to be 83 GHz, just 3.8% higher than expected. This corresponded to a dimensional precision on the average microring waveguide width of 75 pm. The reason for this slight increase in channel spacing is attributed mainly to a frequency shift caused by the increased proximity effects as more and more drop-ports are added. This can be eliminated in future filter banks by modifying the layout. The bandwidth of these filters was measured to be 42 GHz, much larger than the 25 GHz target. The increase in bandwidth was due to two causes. The first is that on average there was a 20 GHz

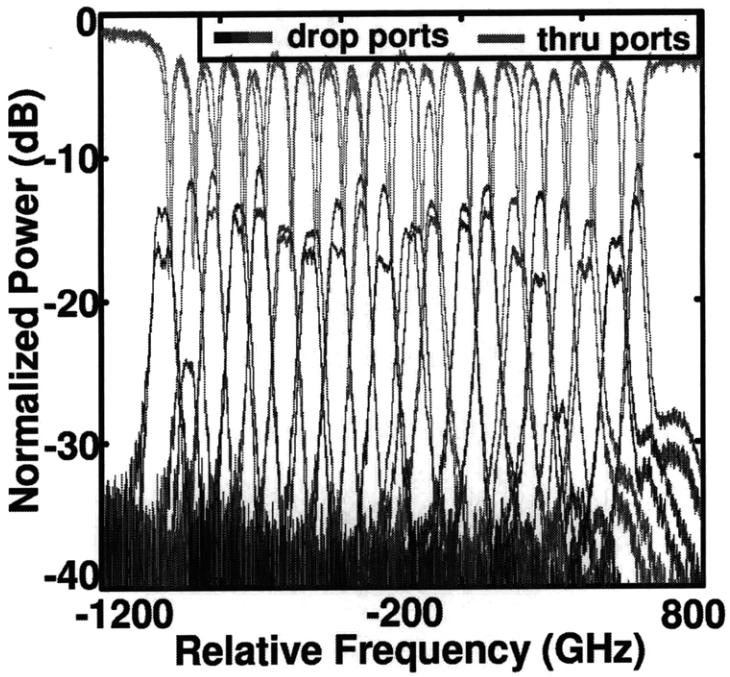


Fig. 6.5. Transmission response of a double twenty-channel filter bank comprised of the oxide-clad SiN_x filter design.

frequency mismatch between the two rings of each filter. This was not due to intrafield distortion, which was measured during the calibration experiments to be 18 GHz and 60 GHz for the top and bottom filter banks, respectively. The explanation of this mismatch is, once again, the proximity effects from the large number of drop ports. This is further supported by the fact that the mismatch in the first filter of both filter banks is very small but gets larger, on average, as more drop ports are added. The second reason for the increase in bandwidth is a much larger propagation loss than expected. This reduced Q_{int}, limited the minimum bandwidth of the filter and increased the drop loss. This higher than expected propagation loss is caused by increased material absorption in the SiN_x. The optical quality of the SiN_x film can vary significant from batch to batch.

The average drop loss of the filters in the filter bank was measured to be 12 dB with a deviation as high as 8 dB. The reason the deviation was much higher than what was seen in the eight-channel filter banks is that as the bandwidth is reduced the filter shape, drop-loss and bandwidth, become much more sensitive to small frequency mismatches between the two rings in the same filter. So, even though the variance of frequency mismatches stayed about the same as for the fabricated eight-channel filter banks, the smaller bandwidth makes them more noticeable. This demonstrates the importance of removing these frequency mismatches by some postfabrication tuning method as one goes to smaller bandwidth filters

Another important parameter measured for these two filters banks is how well their transmission responses match each other. The average channel frequency mismatch is measured to be 0.9 GHz (23 pm) with a standard deviation of 8 GHz (200 pm). This demonstrates that there are no systematic differences between the resonant frequencies of

the two filter banks that are fabricated in close proximity. The standard deviation of the frequency error between the two filters corresponds to a dimensional variation of 200 pm, which is very close to what is expected from small random process variations like those seen in the fabricated eight-channel filter banks. It is expected however, that for filter banks fabricated far from each other in time and distance, that there will be a systematic shift in their transmission response, but not in channel spacing, due to a combination of changes in the thickness of the core material and long term drift in the electron-beam current. This is evident in the experimental results.

6.3.3 Thermally Corrected Filter Bank

After fabrication of the filter bank, any errors in the resonant frequency of each microring can be corrected using thermal tuning. The refractive indices of SiN_x and Si change slightly with temperature. Therefore, by heating a microring it is possible to change its resonant frequency by changing n_{eff}. In Fig 6.6, the transmission response of a two-channel filter bank is shown, before and after thermal tuning. Before thermal tuning one of the filters has a drop loss of 13 dB due to a frequency mismatch of 63 GHz between the two rings, the other filter has a drop loss of 8 dB and a frequency mismatch of only 5 GHz. After thermal tuning, the frequency mismatch for each filter is reduced to less than 1 GHz and the drop loss is 8 dB for both filters. The thermal crosstalk between the individual heaters for each ring of the same filter is only 3%, and the crosstalk between heaters for different filters is less than 0.1%. In addition to correcting for the frequency mismatch between two rings of the same filter, thermal tuning can also be used

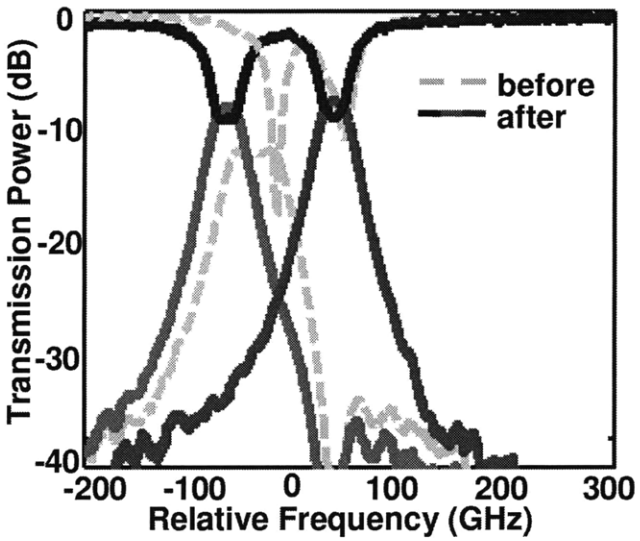


Fig. 6.6. Transmission response of a two-channel SiN_x filter bank before and after using thermal tuning, reducing frequency errors to less than 1 GHz.

to correct for any errors present in the frequency spacing by heating both rings of the filter the same amount. The tuning efficiency of the SiN_x filters is 80 μW/GHz and the tuning efficiency for the Si filters should be a factor of 10 times less. The amount of power needed to correct all of the frequency errors in the measured twenty-channel dual filter bank in Fig. 6.5 is only 0.09 W, compared to the 2.4 W that would be needed if no effort was made to control the resonant-frequency spacing during fabrication.

6.4 Si FILTER BANKS

Fig. 6.7 shows the measured transmission response of a twenty-channel Si filter bank. The average frequency spacing is 105 GHz with a standard deviation of 70 GHz. This frequency spacing is much larger than the target spacing of 80 GHz, but still small enough to allow for all 20 channels to fit into one FSR. The larger than expected channel spacing is likely caused by changes in the Si core thickness. To explain the increase in

channel spacing the thickness of the Si core would have to change by 1.2 nm over the 2 mm length of the filter bank. Since the standard deviation of the Si thickness is 5 nm, this appears reasonable. The 70 GHz standard deviation of the frequency spacing is slightly less than the 100 GHz that was measured during the Si calibration run and is attributed to variations in the electron-beam current, the core thickness, or other stochastic process variations.

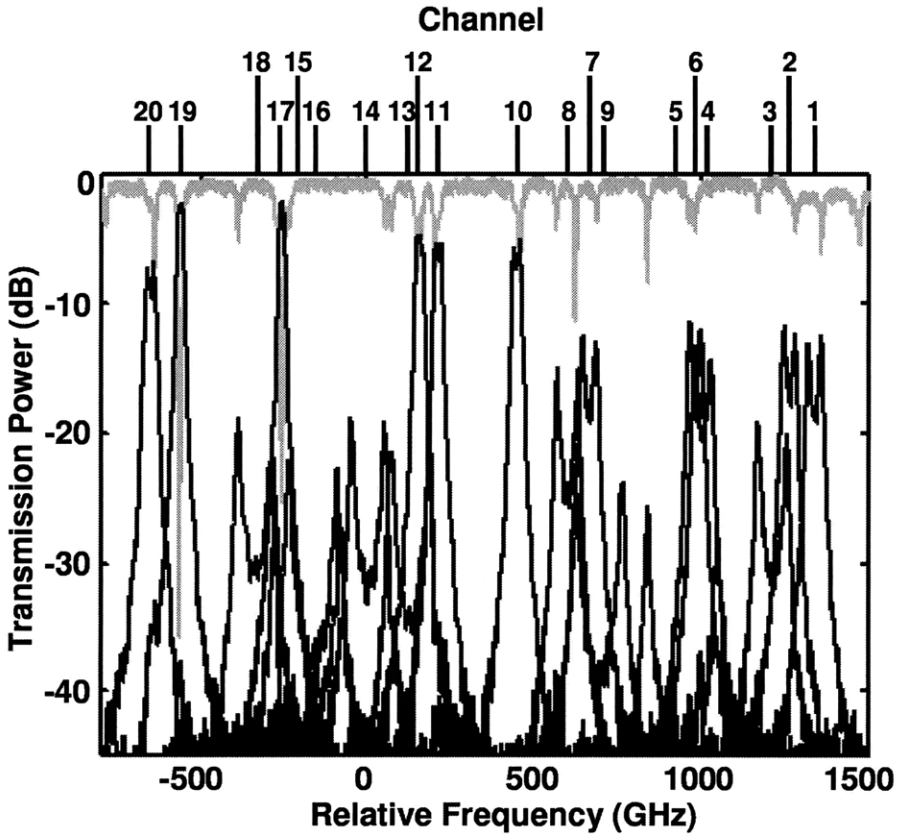


Fig. 6.7. Transmission response of a twenty-channel Si filter bank with an average channel spacing of 105 GHz. The channel numbers are listed above the graph.

The drop loss in this filter banks is seen to range from 1.5 to 35 dB. This drop loss variation correlates with the frequency mismatch between two rings of the same filter, and can be largely eliminated with thermal tuning. This should reduce the drop

loss to ~1.5 dB/cm for all of the channels, much less than the 8 dB measured in the SiN_x filters. This drop loss is still higher than what was measured during the calibration experiments, but can easily be explained by the slightly increased loss in the rings from optical absorption by the titanium heaters.

Fig. 6.8 shows the transmission response of channels 19 and 20 of the twenty-channel Si filter bank. The frequency spacing between these two channels is 88 GHz. The frequency mismatch between the two rings is 0.4 GHz and 20.9 GHz for channel 19 and 20, respectively. The bandwidth of the frequency-matched filter (channel 19) is measured to be 21 GHz and the crosstalk, for 80 GHz spaced channels, is < -35 GHz.

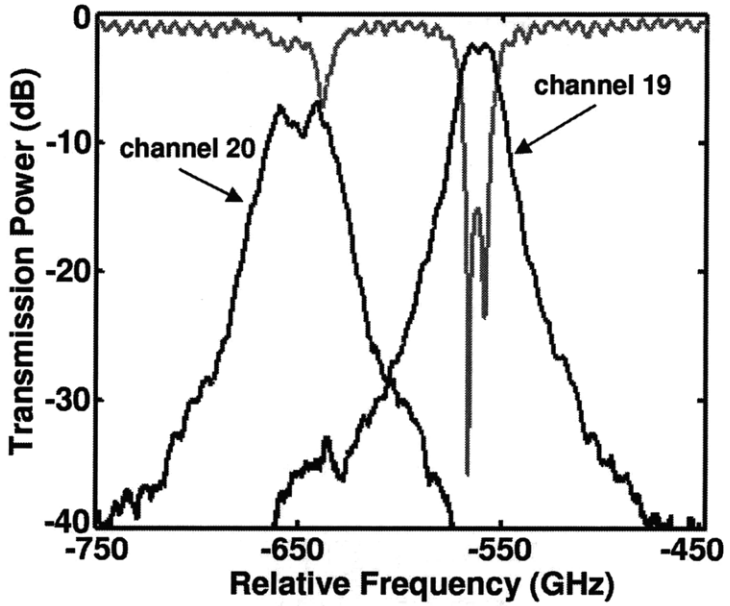


Fig. 6.8. Transmission response for channel 19 and 20 of the twenty-channel Si filter bank. The frequencies of the two rings in channel 19 are matched to 0.4 GHz representing what each channel will look like after thermal tuning.

After thermal tuning to correct for all frequency errors in the twenty-channel filter bank all channels will look similar to channel 19. This will result in a filter bank that meets all the requirements for the proposed electronic-photonic analog-to-digital converter. Assuming a tuning efficiency of 10 μW/GHz this will require 0.11 W, only slightly more

power than the SiN_x filter bank. If a channel spacing of 100 GHz is acceptable, the power consumption can be reduced to 0.064 W.

6.5 CONCLUSION

For high-performance filter banks second-order microring filters were used, balancing the tradeoffs between channel density and fabrication challenges. This fixed the channel density at three times the filter bandwidth. Therefore, to increase the number of channels one must either increase the FSR or decrease the bandwidth. Two CMOS-compatible materials, which allow for a FSR greater than 2.0 THz, are SiN_x and Si. Using these materials two-, eight-, and twenty-channel filter banks were fabricated. The frequency control was better for SiN_x filter banks due to the lower dimensional sensitivities. The best SiN_x filter banks had an average channel-spacing error of only 3 GHz, corresponding to control of the average ring waveguide width of 75 pm However, when moving to smaller bandwidths, the material absorption of the SiN_x resulted in a high drop loss, of 8 dB. By switching to Si, this drop loss was reduced to 1.5 dB, but at the price of larger frequency errors. Fortunately, the tuning efficiency for the Si filter was better than for SiN_x, making the total power to correct for all frequency errors approximately the same for the twenty-channel SiN_x and Si filter banks.

PART II

Supporting Technologies for Integration

Chapter 7

Hydrogen Silsesquioxane Overcladding

7.1 INTRODUCTION

In HIC photonic devices the majority of the emphasis is put on the high-index core material, usually treating the low-index cladding material(s) somewhat as just an afterthought. This is not the best approach because the cladding material serves many purposes beyond just providing the index contrast needed to help guide the optical mode. For single-mode HIC photonic structures a large fraction of the optical mode, sometimes more than 50%, travels outside the core in the cladding material. Hence, it is important that the cladding materials have low optical loss. The cladding also protects the photonic devices from the outside environment. For example, if a microring resonator is left unclad, dust particles that land on the device or changes in the chemical composition of the atmosphere can cause the resonant frequency to shift. The latter effect has, in fact, been exploited to make chemical sensors [43]. It is also important that the cladding material be uniform and fill all gaps between photonic devices. This is especially

Parts of this chapter were featured in:

C.W. Holzwarth, T. Barwicz, Henry I. Smith, "Optimization of hydrogen silsesquioxane films for photonic applications," J. Vac. Sci. Technol. B, vol. 25, no. 6, pp 2658-2661 (2007).

important for microring-resonators filters where incomplete filling of the sub-micron coupling gaps can result in excess loss, due to scattering in the coupling region, and changes in the coupling coefficient, which alters the shape of the filter transmission response. Also, since the cladding material is what separates the heaters from the microrings it is important that the thermal conductance and thermal stability be as high as possible (Fig. 7.1).

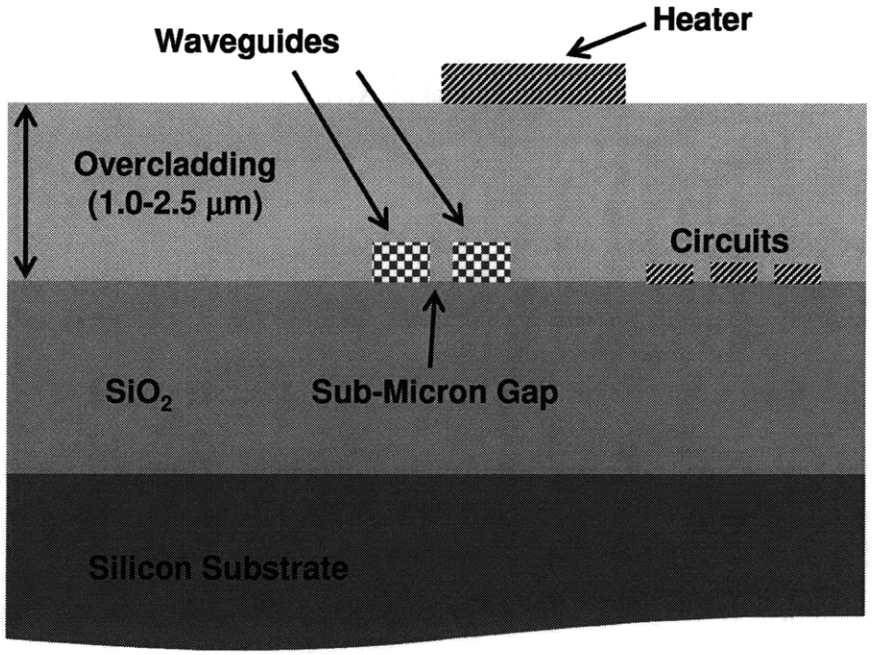


Fig. 7.1: Cross-sectional diagram illustrating the need for the low-index overcladding layer to fill-in sub-micron gaps, to separate the metal heater from the waveguide, to planarize the top surface and to provide thermal conductivity from heaters to the photonic structures.

The logical choice for a cladding material in EPIC is SiO_2 because it has a low index of refraction, low optical loss, and it is CMOS compatible. However, SiO_2 can have very different properties depending how it is grown or deposited. The highest quality oxide is formed through thermal oxidation of crystalline silicon. This is typically how the lower cladding is formed, and then the core material is deposited on top of it or,

in the case of SOI wafers, two thermally-oxidized wafers are bonded and then one of them is cut using smart-cut technology [44]. Thermal oxidation, however, is not an option for the overcladding layer because there is no silicon source for the oxide. The other options for depositing oxide include PECVD with various source gasses, LPCVD, sputtering and evaporation. Most of these options either form low quality oxides containing pin-holes, pores, and Si-H bonds, or they have difficulty filling in high-aspect-ratio gaps. Tetraethyl orthosilicate (TEOS) deposition is one method that is capable of meeting these requirements, but it requires expensive equipment and must be optimized for gap filling.

A cheaper and simpler alternative to TEOS is to use hydrogen silsesquioxane (HSQ), a spin-on glass, to form the overclading oxide layer. HSQ is a non-organic polymer with a chemical composition of $[HSiO_{3/2}]_n$. It was developed as a spin-on low-k dielectric, but it also functions as a negative electron-beam lithography resist. It is also well know to have excellent gap-filling and self-planarization properties making it a promising candidate for an overclading material [45]. However, an HSQ film prepared using the standard thermal annealing recipe results in a film that contains Si-H bonds, is about 21-24% porous, has reduced thermal conductivity, and is under high tensile stress, limiting the maximum thickness to less than 1.2 μm. By optimizing the annealing process it is possible to eliminate these problems and fully convert HSQ so that it has essentially the same optical properties as thermally-grown SiO_2, while retaining the excellent gap-filling and planarization properties.

7.2 CONVERTING HSQ TO SiO_2

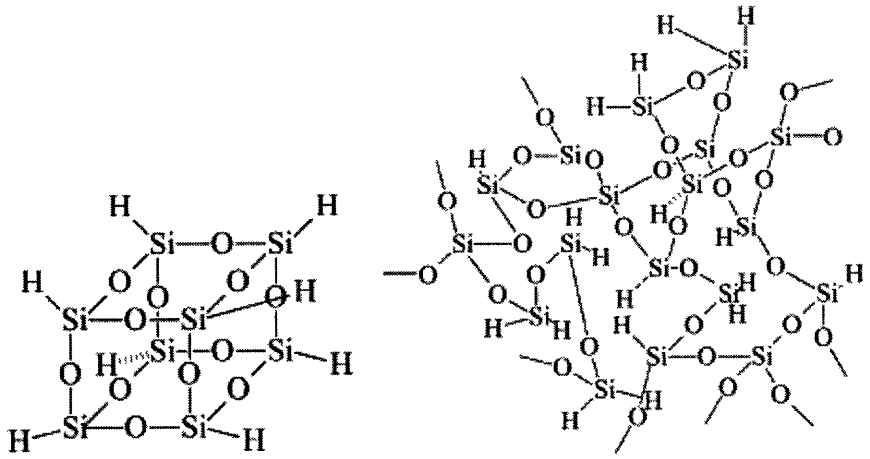
The subject of converting HSQ to SiO_2 has been touched on in many journal articles, most of the time with the objective of improving the etch resistance of HSQ after SEBL [46, 47, 48]. The methods used include O_2 plasma treatments and thermal annealing at high temperatures in either N_2 or O_2 atmospheres. Treating the films with an O_2 plasma in only effective in converting the first few nanometers from the surface into SiO_2, which although successful for improving the etch resistance of HSQ it is not helpful when one is trying to convert thick films of HSQ into SiO_2. Previous efforts using high temperature thermal anneals involved thin films, less than 200 nm, and therefore were not concerned with stress in the film. The stress, however, is critical for photonic applications because the overcladdings thickness must be 1.0-2.5 μm, depending on the exact design. Also, the confirmation that these HSQ films were in fact converted to SiO_2 is incomplete. Usually only the change in Si-H bonds was measured and it was assumed that once these bonds are completely removed the film is SiO_2. This is a faulty assumption that does not give information about the stoichiometry or porosity of the film.

7.2.1 Thermal Annealing

Since we were concerned with achieving thick SiO_2 films (> 1 μm) for the overcladding we placed our efforts on optimizing the thermal-annealing process. The optimized annealing process must be successful in removing the tensile stress, porosity, and Si-H bond content of the film, while achieving the same index of refraction as

thermally-grown SiO_2 and maintaining the excellent gap-filling and planarization properties.

HSQ is commercially available from Dow Corning and comes in the form of a cage oligomer $[HSiO_{3/2}]_n$ in a 4-methylpentan-2-one solution (Fig. 7.2a). This solution is spun onto a wafer to form a thin film. The standard thermal cure for HSQ consists of three consecutive 1 min hot plate bakes at 150, 200, and 350°C and then a final 1 hr anneal at 400°C in a N_2 atmosphere [49]. Each part of this curing process has a very



(a) **(b)**

Fig. 7.2: Bonding structure of HSQ in the (a) cage oligomer form and (b) a network structure.

specific role. The first hot plate bake at 150°C is responsible for removing the solvent from the thin film. The second bake at 200°C allows the HSQ oligomers to flow, filling in gaps and creating a planar surface. In the third bake at 350°C there is an exchange of Si-O and Si-H bonds between neighboring oligomers causing the HSQ oligomers to start forming a network structure, following the chemical Eqs. 7.1-3, providing some mechanic stability.

$$2HSiO_{3/2} \rightarrow H_2SiO + SiO_2 \quad \textbf{7.1}$$

$$H_2SiO + HSiO_{3/2} \rightarrow SiO_2 + H_3SiO_{1/2} \quad \textbf{7.2}$$

$$H_3SiO_{1/2} + HSiO_{3/2} \rightarrow SiO_2 + SiH_4 \quad \textbf{7.3}$$

The final anneal at 400°C in a N_2 atmosphere completes the formation of this network structure resulting in the evolution of SiH_4 and H_2 (Eq 7.4-5) and marked by an increase in porosity and slight reduction in refractive index. The final HSQ film is the network structure shown in Fig. 7.2b containing up to 15 at% hydrogen and having a porosity near 24%.

$$4\,HSiO_{3/2} \rightarrow 3SiO_2 + SiH_4 \quad \textbf{7.4}$$

$$SiH_4 \rightarrow Si + 2H_2 \quad \textbf{7.5}$$

For optimizing the annealing process it was decided to not change the first two hotplate steps since they are responsible for removing the solvent, filling in gaps, and planarizing the surface, things that are needed for the overcladding. It was also quickly evident the third hot plate anneal should not be changed, since without this step most films cracked prior to the final anneal, demonstrating that the mechanical stability provided by this step is essential. This means that only the final annealing step should be modified to create a film with the desired properties. The four major variables that are controlled in this final annealing step are the ambient gas, temperature, anneal time and ramp speed.

The two ambient gasses explored were N_2 and O_2. At temperatures above 350°C oxidation of Si-H can occur, increasing the incorporation of SiO_2 bonds in the film and removing hydrogen in the form of H_2O (Eq. 7.6). This results in an increase in the refractive index of the film and a more SiO_2-like structure, but at the same time

increasing the stress of the film. On the other hand, when annealed in a N_2 atmosphere hydrogen is removed from the film as SiH_4 and H_2 (Eq. 7.4-5) and the stress in the film is significantly less [50]. Since we want both a SiO_2 structure and a low stress film it was initially unclear which ambient would be better.

$$2HSiO_{3/2} + O_2 \rightarrow H_2O + SiO_2 \qquad \textbf{7.6}$$

For the experiments a quartz tube furnace and rapid-thermal processing (RTP) were used. These tools allowed testing of anneal temperatures between 400°C and 1150°C. It has been reported that pores in HSQ films start to collapse at temperature greater than 435°C and complete removal of Si-H bonds occurs at temperatures above 650°C, suggesting an anneal temperature above 650°C should be used [52]. Once again there is a trade off with stress since it has been shown that the stress in the film also increases as the anneal temperature increases. By using the RTP tool it is also possible to test the properties of films that are annealed for a very short period of time ~1 min. compared to the 1 hr anneal time used in the quartz-tube-furnace anneals. Also RTP allowed us to ramp to the anneal temperature very quickly, 50°C/s, compared to the slow ramp rate of a quartz furnace, ~10°C/min. This allowed us to bypass stress states that occur as the temperature is ramped up to the final anneal temperature.

For the experiments blanket HSQ films of various thicknesses were prepared by spin coating FOx-25 onto a silicon substrate using spin speeds of 1000, 2000, and 5000 rpm. After spin coating, all samples were heated on three consecutive hot plates at 150, 200, and 350°C for 1 min each. One set of samples was set aside after the three hot-plate bakes as the first control sample. Another set of samples was subjected to the standard final cure of 1 h at 400°C in a N_2 atmosphere and set aside as the second control

sample. The rest of the sample sets were subjected to anneals in either a quartz tube furnace or a RTP tool, using either an N_2 or O_2 atmosphere. After annealing, samples were inspected under an optical microscope for the presence of microcracks to qualitatively check the stress. The thickness and refractive index of uncracked samples were measured using a Sopra spectroscopic ellipsometer over a wavelength range of 0.4–1.8 μm. This data was used to determine the film shrinkage, chromatic dispersion, and the refractive index at 1550 nm for each annealing process. Fourier transform infrared (FTIR) measurements were also performed to check for the presences of Si-H bonds and the structure of the Si-O bonds.

7.2.2 Measured Material Properties

Table 7.1 shows the results of the refractive index at 1550 nm and the film shrinkage for each anneal. It is important to note that all films annealed in the quartz furnace above 800°C cracked and their data is not shown. From this data it is seen that as the film shrinkage increases the refractive index increases. At lower temperature, 400°C, the pores are not able to collapse so the changes are attributed to the removal of Si-H bonds and the formation of the network structure. The amount of shrinkage increases when a longer anneal time is used and when annealed in an O_2 atmosphere. This is expected since at the lower temperatures the reactions to remove the hydrogen and form the network structure is slow and the presence of O_2 is known to act as a catalyst for the reaction. At higher temperatures the increase in refractive index and decrease in thickness are due to the removal of hydrogen from the film and the collapsing of the pore

structure. All films annealed above 800°C showed shrinkage of at least 21% signaling the complete removal of the pores. For samples annealed at temperatures above 1000°C the shrinkage is higher for samples annealed in N_2 than samples annealed in O_2, the opposite of what is found at low temperatures. The reason for this is that when annealed in N_2 the majority of the hydrogen is removed as SiH_4 and H_2 compared to H_2O for

Table 7.1 Refractive Index and Film Shrinkage Results for HSQ Films

Temperature	Furnace	Time[a]	Ambient	Refractive index (1550 nm)	Shrinkage
350°C	Hotplate	1 min	Air	1.361	0%
400°C	Tube	1hr	N_2	1.370	3.6%
400°C	Tube	1 hr	O_2	1.386	7.9%
400°C	Tube	12 hr	N_2	1.414	11.3%
650°C	Tube	1 hr	N_2	1.432	19.4%
800°C	Tube	1 hr	O_2	1.419	21.7%
1000°C	RTP	1 min	N_2	1.521	32.4%
1000°C	RTP	1 min	O_2	1.439	23.4%
1150°C	RTP	1 min	N_2	1.585	37.9%
1150°C	RTP	1 min	N_2, O_2[b]	1.451	30.0%
1150°C	RTP	1 min	O_2	1.442	23.7%

[a] Time does not include ramp to anneal temperature
[b] Ramp performed in N_2, anneal performed in O_2

samples annealed in O_2. This means that in addition to the pores collapsing some of the Si is also removed in the N_2 samples. Also, without the presence of O_2, no additional oxygen can be incorporated into the film to correct the stoichiometry, resulting in the formation of a silicon-rich oxide. This is confirmed by comparing the wavelength-dependency of the refractive indices of the samples annealed in N_2 at 1150°C with those annealed in the presence of O_2 (Fig. 7.3). The refractive index of the films annealed in N_2 have a much higher chromatic dispersion than the sample annealed in O_2, which is characteristic of silicon-rich oxides [53]. These silicon-rich oxides are undesirable for

photonic overcladdings as they often show higher optical loss, in part from the presence of silicon nanoclusters [54]. The sample annealed at 1150°C in O_2 has the same chromatic dispersion and refractive index as thermal SiO_2. To prevent the formation of silicon-rich oxides the optimal final anneal must be performed in an O_2 atmosphere.

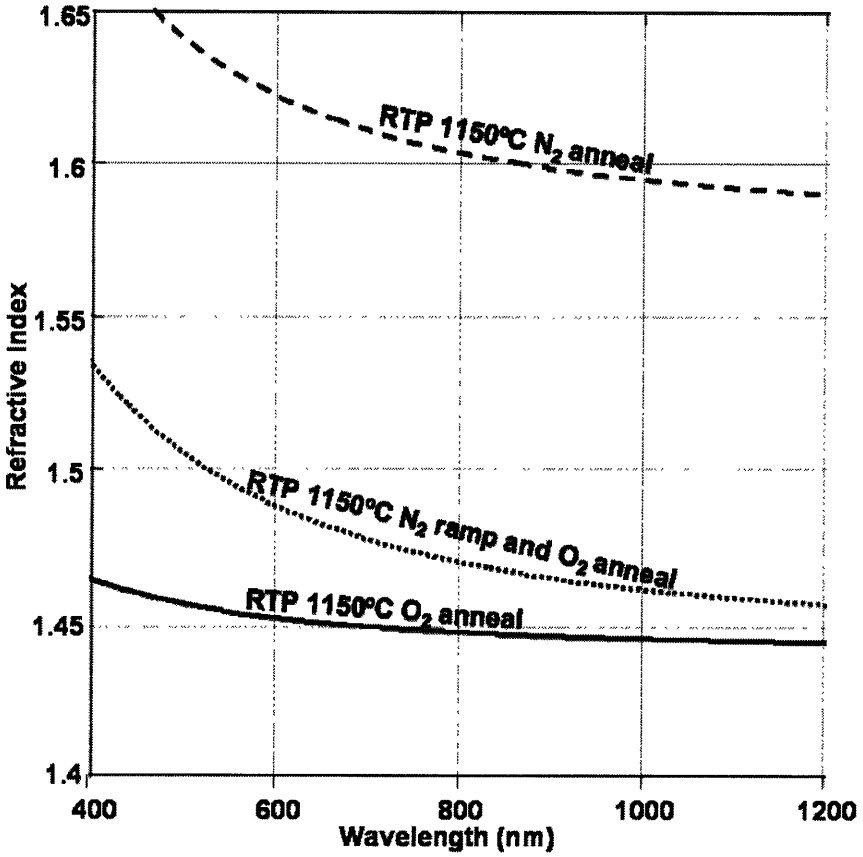


Fig. 7.3: Reactive index versus wavelength for the three different RTP anneals at 1150°C. The two samples annealed with N_2 present have higher chromatic dispersion.

The FTIR spectra for select HSQ annealing recipes are shown in Fig. 7.4. All peaks are normalized to a film thickness of 1 μm and the spectra offset for easy comparison. The important peaks in the spectra are the Si–H stretching peak at 2250 cm^{-1}, the three Si–O–Si (SiO_2) peaks at 1090 cm^{-1}, 800 cm^{-1}, and 450 cm^{-1}, and the multiple peaks from 800–900 cm^{-1} that are characteristic of suboxides (Si–O–H) [55, 56].

From the spectra it is seen that for all samples annealed above 650°C the Si–H and suboxide peaks are completely removed, therefore, all bonded hydrogen is removed, as is consistent with previous published results. The FTIR data also show that the Si–O–Si stretching peak gets larger in intensity and narrower as the anneal temperature is increased and the ambient is changed to O_2, suggesting that the HSQ film is being converted to SiO_2 via a combination of pyrolysis and oxidation. For the sample annealed at the highest temperature in an O_2 atmosphere the FTIR spectrum is identical to that of thermal SiO_2.

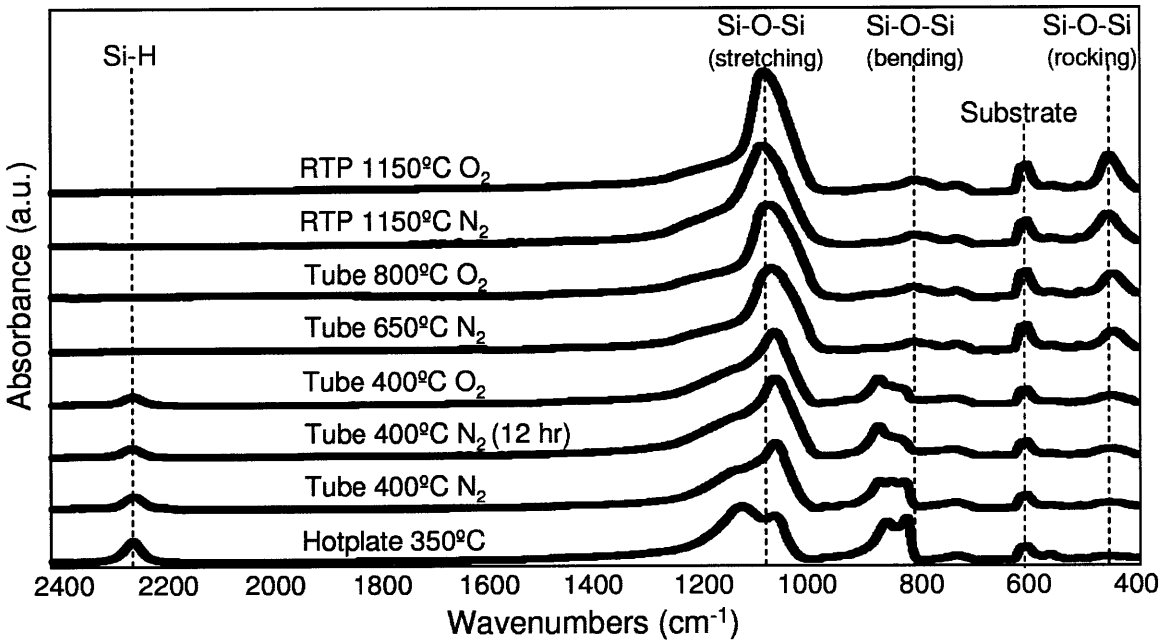


Fig. 7.4: FTIR spectra of HSQ films for selected final anneals. The spectra have been offset and all normalized to a film thickness of 1 μm for easy comparison.

7.2.3 Creating Thick Layers

The maximum thickness of HSQ films is limited by tensile stress. This tensile stress can form during the anneal and as the samples cools down to room temperature.

During the anneal, tensile stress develops from film shrinkage and the transformation of H-Si-O to Si-O-Si bonds [50]. Also, during cool down, stress can form from the coefficient of thermal expansion (CTE) mismatch between the annealed HSQ film and the Si substrate. The CTE of HSQ has been found to correlate with the Si-H to Si-O bond ratio [51]. When this ratio is over 0.2 the CTE of the film is between 10 and 20 ppm/°C, significantly higher than the CTE of Si, 2.6 ppm/°C, causing tensile stress to increase when the sample is cooled down to room temperature. Once the ratio falls below 0.2 the CTE decreases dramatically, and is approximately 1 ppm/°C, similar to the CTE of SiO_2, when all Si-H bonds are removed. Therefore, for anneals above 650°C, containing no Si-H bonds, the CTE mismatch between the HSQ and Si substrate can be ignored, leaving only the tensile stress formed by film shrinkage and the transformation of the bond network during the anneal. This stress starts to form at 350°C and 360°C for films annealed in O_2 and N_2, respectively [50].

Of all the anneals measured none, of them achieved a single layer thickness of 2.0 μm. In fact, most of them cracked due to stress at thickness less than 1 μm, as seen in Table 7.2. To achieve the 2.0 μm thickness needed for the overcladding layer one must resort to a multilayer film. The problem with this is that if the tensile stress is still present in the first layer the addition of the stress in the second layer will cause the film to crack. To qualitatively determine if the stress is still present after the anneal, a second layer of HSQ was added and the sample subjected to the same final anneal. The only samples that did not crack were samples that had been processed by RTP at temperatures above 1000°C in either a N_2 or O_2 atmosphere. For these samples it was possible to add a third and fourth layer, reaching the desired overcladding thickness of 2.0 μm, without the

film cracking (Fig. 7.5). This temperature corresponds to the temperature at which it is known that stress can be relaxed in thermal oxides through viscous flow, which is what is thought to be occurring in the HSQ films [57].

Table 7.2 HSQ Film Thickness First Observed to Crack

Temperature	Furnace	Time	Ambient	First Thicknesses Observed to Crack (μm)[a]	
				Single layer	Multiple layers
350°C	Hotplate	1 min	Air	1.20	1.20
400°C	Tube	1 hr	N_2	1.15	1.37
400°C	Tube	1hr	O_2	1.10	1.24
400°C	Tube	12 hr	N_2	0.93	1.16
650°C	Tube	1 hr	N_2	0.85	1.06
800°C	Tube	1 hr	O_2	0.82	0.99
1000°C	RTP	1 min	N_2	0.88	>2.0 (No Cracks)
1000°C	RTP	1 min	O_2	0.96	>2.0 (No Cracks)
1150°C	RTP	1 min	N_2	0.74	>2.0 (No Cracks)
1150°C	RTP	1 min	N_2, O_2	0.78	>2.0 (No Cracks)
1150°C	RTP	1 min	O_2	0.92	>2.5 (No Cracks)

[a] Thickest sample that showed no cracks typically ~20% thinner

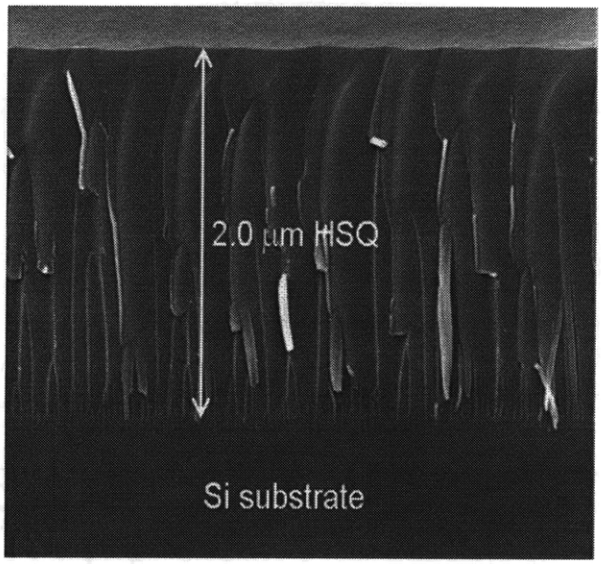


Fig. 7.5: Scanning-electron micrograph of the cross-section of a 2.0 μm thick HSQ film made using multiple layers and the optimized anneal process.

Knowing this, it was of interest to understand why the films annealed in the quartz tube furnace at 1000°C cracked since stress is annealed out at temperatures above 1000°C. The main difference in the two experiments was the time the samples spend between 350°C, where tensile stress starts to form, and 1000°C, where the stress can relaxed out. For the quartz-tube furnace the ramp rate was approximately 10°C/min while the ramp rate used in the RTP experiments was 50°C/s. This resulted in the samples being between the temperature of 350°C and 1000°C for 40 min and 13 s for the quartz and RTP anneals, respectively. (The samples were loaded into the quartz furnace at 600°C.) This led us to speculate that the films in the quartz tube furnace were cracking due to stress before they reached the temperature at which the stress can be annealed out. To confirm this we tried various ramping rates for the RTP anneals and found that as the ramping rate was decreased the maximum single-layer thickness of the film, achievable without cracking, was also reduced. This means that by using the quick ramp rates, attainable through RTP, it is possible to heat the sample to 1000°C before the stress builds up to the critical value needed to crack the film.

Therefore, the optimal anneal includes a quick ramp rate of ~50°C/s using the RTP tool. It is also necessary to heat the sample above 1000°C in order for the tensile stress in the film to relax, enabling multilayer films. Also, to avoid the formation of sub-oxides the annealing step must be performed in an O_2 atmosphere. Elsewhere in this thesis the optimized anneal refers to annealing the HSQ film at 1150°C for 60s in an O_2 atmosphere using RTP with a ramp rate of 50°C/s.

7.2.4 *Gap-Filling, Planarization, and Optical loss*

Beyond the experiments described above, using blanket films, it was important to confirm that the desirable planarization and gap filling properties of HSQ were retained in this optimized annealing process. This was done by overcladding high-aspect-ratio gaps using HSQ, cured with the optimized process. As seen in Fig. 7.6, the surface of the 2 μm thick HSQ is completely planar above the patterned structures. Figure 7.6 also shows that gaps with an aspect ratio greater than 6:1 are completely filled in with HSQ. To test the compositional uniformity in the filled gaps, a 10 min decorative etch in a 0.12% HF solution was performed on the exposed cross section, as shown in Fig. 7.7b. The HSQ in the gaps and at the outside vertical edges of the patterned structure is removed, whereas the rest of the annealed HSQ overcladding and thermal oxide undercladding remains. This indicates that the HSQ in close proximity to vertical edges of the pattern structure has not fully converted to SiO_2. This suggests that lateral

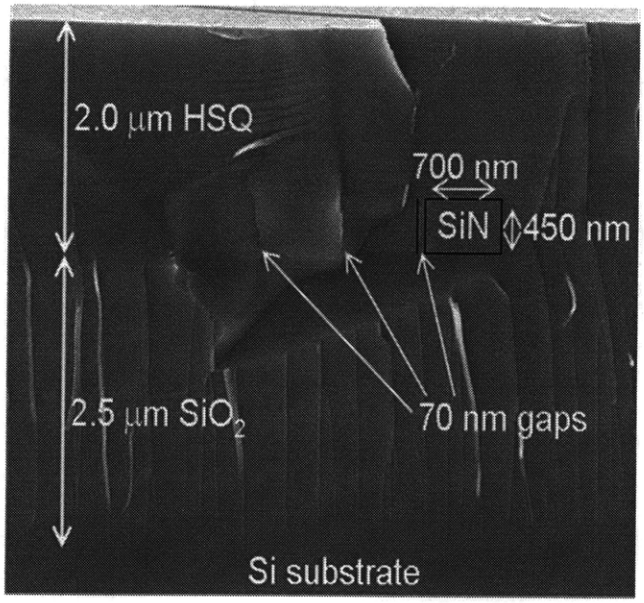


Fig. 7.6: Scanning-electron micrograph showing the planarization and gap-filling capabilities of the optimized anneal.

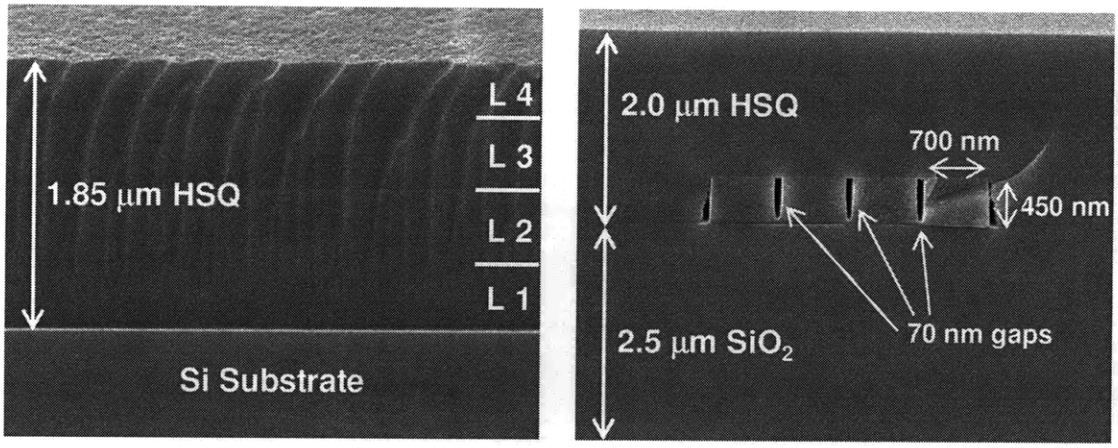


Fig. 7.7: Scanning-electron micrograph showing the cross-section of (a) a blanket film after a 10 min decretive etch in 1% HF and (b) an overclad photonic structure after a 10 min decretive etch in 0.12% HF.

confinement prevents the process of oxidation and/or densification from going to completion. This has also been reported in HSQ films formed using the standard annealing process and is not a major hindrance for most photonic structures as long as it does not cause excess loss [38].

To verify the optical loss of HSQ cured with the optimized anneal, a weakly-coupled large-radius microring resonators was fabricated in stoichiometric Si_3N_4, with a 2 μm overcladding of optimized HSQ. The reasons for choosing this photonic device are that the filling-in of the small coupling gaps between the bus and ring waveguides is critical for proper performance. Over 50% of the mode is outside the core material, and by measuring the Q of a weakly coupled microring it is possible to calculate the propagation loss (Appendix A). By measuring the Q of the microring, one can determine if nonuniformities in the cured HSQ cause any increased optical absorption. The transmission spectrum of the drop port for this microring had a measured 3 dB bandwidth of 0.8 GHz, corresponding to a Q of 240 000 and propagation loss of 1.5 dB/cm (Fig.

7.8). This is consistent with the best published data for Si_3N_4 microrings fabricated using TEOS as the overcladding material [43]. This demonstrates that HSQ can be used as an alternative to TEOS for overcladding photonic structures without adversely affecting device performance.

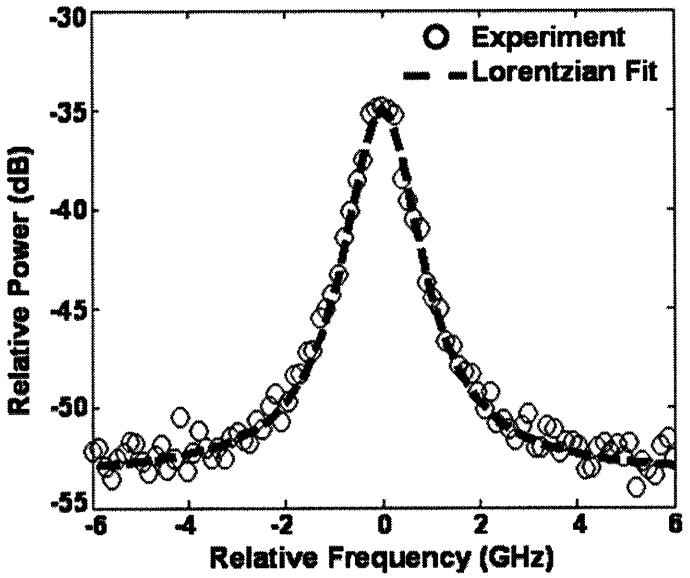


Fig. 7.8: Measured transmission response of a weakly-coupled Si_3N_4 microring resonator filter with a Q of 240 000.

7.3 CONCLUSION

In conclusion, we have presented an anneal process that optimizes the properties of HSQ for photonic overcladding applications. The optimized final step of the anneal consists of heating the sample to over 1000°C in an O_2 atmosphere with a ramp rate of 50°C/s, using RTP. This anneal is successful in removing the Si–H bonds, collapsing the pores, and removing the tensile stress, enabling thick films to be formed through multiple spins. We also demonstrated that the excellent planarization and gap-filling properties of HSQ are retained after this annealing process. As a proof of principle, a weakly-coupled Si_3N_4

microring resonator overclad with optimized HSQ was fabricated and tested. The measured Q of 240 000 is the same as the highest reported value found in the literature for a microring with the same core material and TEOS overcladding.

Chapter 8

Localized Substrate Removal

8.1 INTRODUCTION

Almost all research in CMOS-compatible HIC photonics, including all work mentioned so far in this thesis, starts with a silicon wafer as the substrate, with a thick (>2 μm) layer of SiO_2 and a high-index core material on top of it (Fig. 8.1a). This thick layer of SiO_2 between the substrate and the high-index core material is necessary to prevent the optical mode carried in the waveguide from "tunneling" (leaking) into the high-index silicon substrate. However, for high-performance electronics, such as processors, this thick layer of SiO_2 is not allowed due to the ever increasing need for the silicon substrate to transfer the heat away from the electronics. In order to integrate photonics monolithically with high performance Si circuitry one must eliminated this thick SiO_2 layer and work completely within the constraints of commercial CMOS process flows, utilizing the given material layers, thicknesses, processing steps and tools. Any additional fabrication steps must be performed as post-processing steps that meet the backend-processing thermal budget requirement of no steps above 400°C. This is no easy task, but the potential of photonic interconnects to break the energy-efficiency and bandwidth-density bottlenecks in scaled CMOS processor cores make it worth the effort.

Parts of this chapter were featured in:

C. W. Holzwarth, J. S. Orcutt, H. Li, M. A. Popovic, V. Stojanovic, J. L. Hoyt, R. J. Ram, and H. I. Smith, "Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk Si CMOS Processes," in *Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferenc,e* (2008).

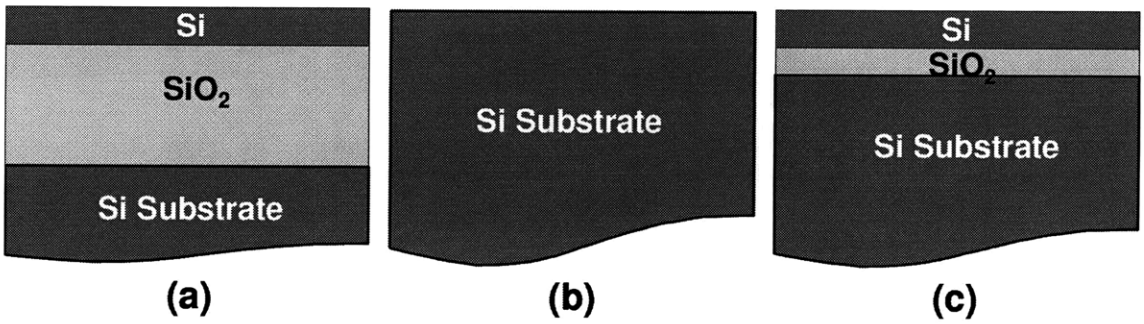


Fig. 8.1: Cross-section diagram of the common starting wafer for (a) photonics, (b) bulk VLSI, and (c) SOI-based VLSI.

Integration of photonics with processor cores requires an understanding of the basics of the CMOS flow. CMOS can be divided into two categories, bulk and SOI, depending on whether the starting substrate is a bulk silicon wafer or a SOI wafer with a thin buried-oxide layer (Fig. 8.1b,c). The majority of the industry is still using bulk CMOS, and that is what will be discussed in the remaining of this chapter (it is important to note that everything discussed can very easily be applied to SOI CMOS as well). In bulk CMOS, transistors are formed using the bulk Si substrate as the source, drain and channel, and a deposited polysilicon layer as the gate. This polysilicon is also used as local interconnect resistors in the transistor level. The transistors are electrically isolated via a thin layer of SiO_2, called the shallow-trench-isolation layer (STI). Above this are multiple layers of metal interconnects, etch stops, and dielectrics that can total more than 6 μm in thickness (Fig. 8.2).

The bulk CMOS process flow, thus permits the deposition of polysilicon above the STI where it can be patterned to form photonic structures (Fig. 8.3a) [58]. However, this STI layer is typically <400 nm in thickness, not nearly thick enough to prevent the optical mode from tunneling into the Si substrate. In fact, the polysilicon waveguide will have a loss on the order of 1000 dB/cm from power leakage into the substrate alone. If it is possible to remove only the Si substrate that is proximate to the photonic structures, without affecting the rest of the circuits, it would be possible to seamlessly integrate photonics and electronics (Fig 8.3b) [59].

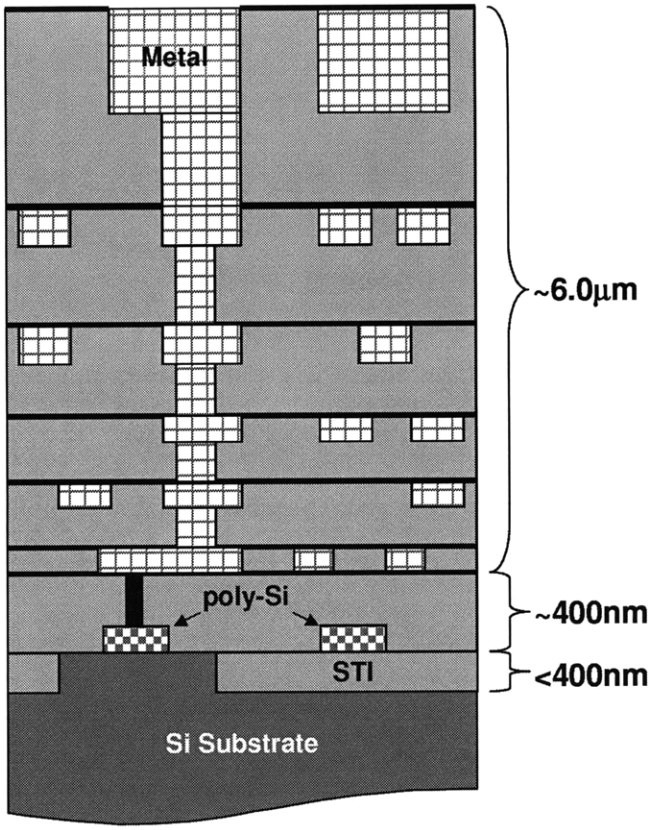


Fig. 8.2: Cross-sectional diagram of a high-performance bulk CMOS chip, including 6 layers of metallization.

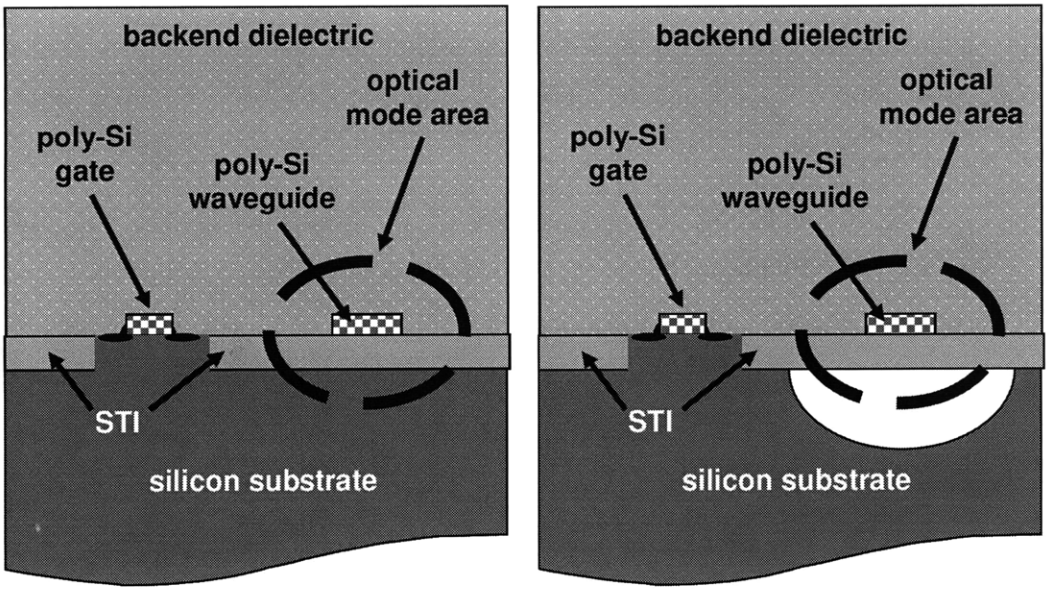


Fig 8.3: (a) diagram showing the integration of photonics using the poly-Si gate material deposited above STI as the core. (b) Diagram showing the localized removal of the Si substrate to prevent loss via leakage into the substrate.

8.2 LOCALIZED SUBSTRATE REMOVAL

In general there are three possible ways to locally remove the substrate below the photonics devices, as are depicted in Fig. 8.4. The first method requires an isotropic etch of the substrate starting from the backside. This method has the disadvantage of having to be aligned to the front surface from the backside, and requires removing a large portion of the substrate due to the thickness of the wafer and isotropic nature of the etch. The second method consists of an anisotropic etch from the backside, such as deep-reactive-ion etching. This method still has the disadvantage requiring alignment from the backside, but it removes less of the substrate. The third method combines both and an anisotropic etch to open up holes in the STI, dielectric and interconnect stack and an isotropic etch to locally remove the substrate by undercutting the photonic structures. This method has the advantage of being aligned from the front side and removing the least amount of the substrate. These advantages make it the most likely route for integrating photonics, at the transistor level, in a standard CMOS process flow.

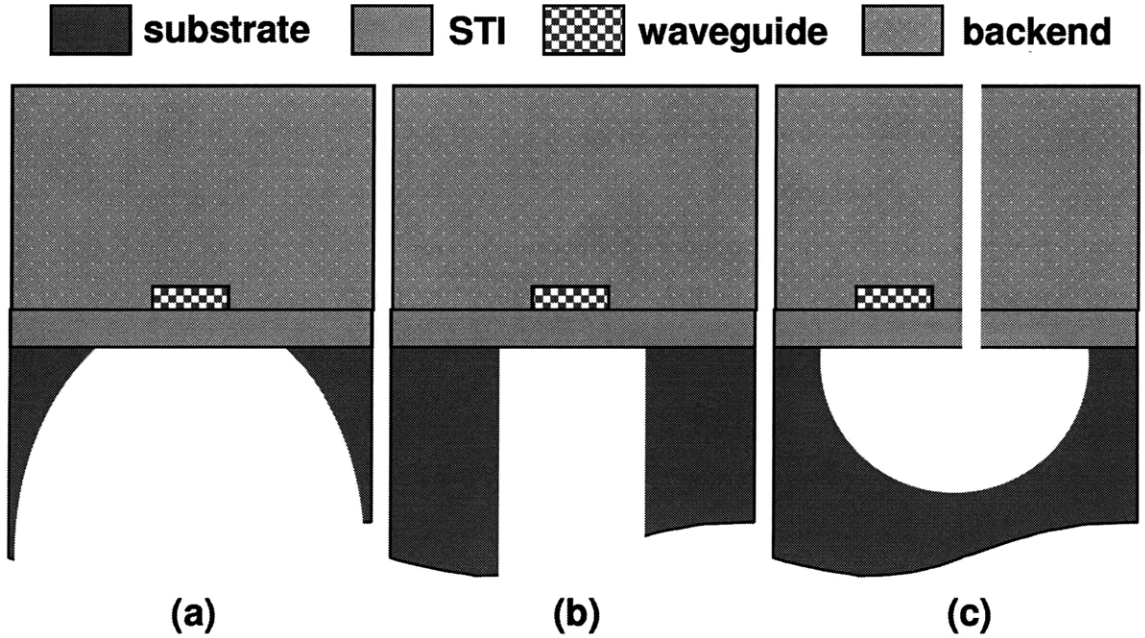


Fig. 8.4: Localized substrate removal using (a) an isotropic etch from the back side, (b) an anisotropic etch from the backside, and (c) using a combination of an anisotropic and an isotropic etch from the front side.

The two key requirements of the top-side method is first an anisotropic etch capable of etching through the entire dielectric stack, and second an isotropic etch that can remove the desired amount of silicon under the photonic structures. The top-side dielectric stack consists of layers of SiN, SiON, SiC, and SiO_2, all of which can be etched using RIE with CF_4 gas. The isotropic Si etch is a bit more complicated for two reasons. First, the etchant must be able to easily travel through etch holes to the silicon substrate, and the etch products must be able to escape from these holes. Secondly, all wet processing must be avoided to prevent the structure from collapsing due to surface tension during drying. One isotropic etchant that meets these requirements is XeF_2 gas.

8.2.1 XeF_2 Etching

XeF_2 is a unique dry etch in that it requires no plasma and it is completely isotropic. It is also very selective, with selectivity ratios as high as 1000:1 for $Si:SiO_2$ [60]. The way that XeF_2 etches silicon is depicted in Fig. 8.5. First the XeF_2 gas is introduced into a vacuum chamber containing a silicon sample. The XeF_2 molecules absorb on the surface of the silicon where they dissociates into Xe and 2F. The fluorine atoms are highly reactive and will combine with the Si atoms at the surface to form SiF_4. The unreacted Xe and etch product of SiF_4 are then desorbed from the surface. This is a spontaneous, exothermic reaction so heat is also produced as a result of the reaction. The Si etch rate is inversely proportional to temperature, with the etch typically performed at room temperature

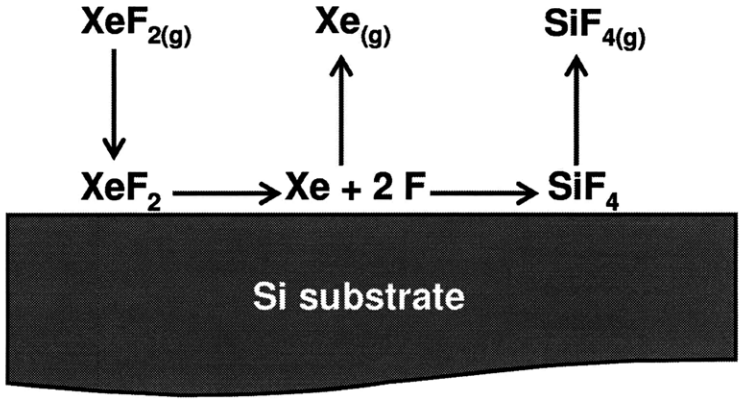


Fig. 8.5: Chemical reaction for etching Si with XeF_2 gas.

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XeF_2 etching tools typically consist of three chambers (Fig. 8.6). The first chamber contains the solid source of XeF_2 which has an equilibrium vapor pressure of 4.5 Torr. The second chamber is the expansion chamber; connected to both the first chamber and the third chamber. The valve between the first chamber and second is opened and closed quickly to allow the XeF_2 vapor to expand into it. The purpose of the second chamber is to supply a constant source of XeF_2 to the third chamber that is not affected by the history of the solid source. The third chamber contains the silicon sample to be etched. Once the expansion chamber is filled with XeF_2 gas and the valve connecting the first and second chambers closed, the valve connecting the expansion chamber and the third chamber is opened for a set time, typically 3-10 s. This allows XeF_2 gas to expand into the sample chamber and the etching to begin. The pressure of the XeF_2 during the etch is ~3 Torr, enabling very fast etching rates of 1-10 μm/min.

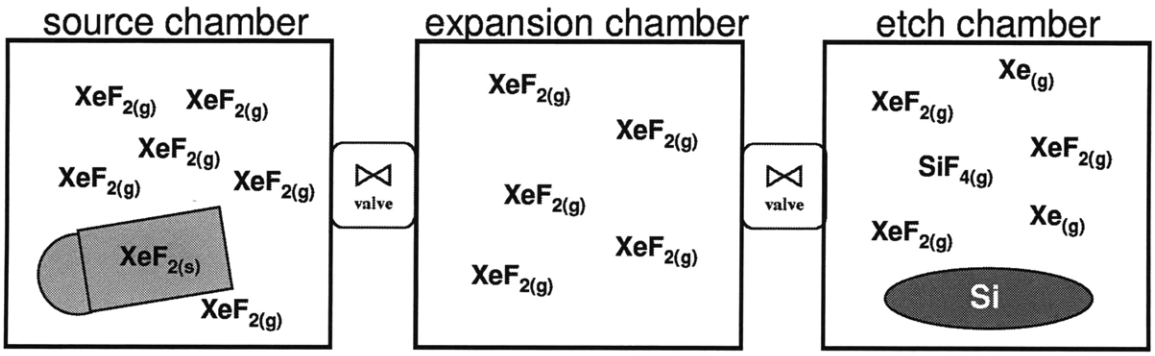

Fig. 8.6: Schematic of a three chamber XeF_2 etch system

To achieve large undercuts a pump-etch-pump technique is used. This technique, illustrated in Fig. 8.7, begins by placing the sample in a vacuum chamber and pumping down to a low pressure. The XeF_2 is then allowed to expand into the chamber where it starts to etch any exposed silicon surfaces. After a given period of time, typically 60s or less, the chamber is pumped back down to a low pressure removing the reaction products of Xe and SiF_4 and creating vacuum in the undercut feature. During this time the sample is also able to transfer the heat, produced from the chemical reaction, away from the sample. The XeF_2 is again allowed to expand into the chamber and continue etching all exposed Si. This cycle is repeated until the desired amount of Si is removed.

Since the etch rate of XeF_2 is very quick it is sometime desirable to slow it down. There are two ways to do this. The first is to increase the temperature of the substrate. The etch rate is inversely proportional to temperature since the time XeF_2 is absorbed on the surface of the Si reduces substantially at increased temperatures decreasing the probability of dissociation into Xe and F atoms. The second way is to decrease the size of the window of exposed silicon. As the window size is decreased it becomes harder for the reactants to fill the void and for the vacuum to remove the reaction products. Using the aperture size affect it is possible to achieve different etch rates at different locations on the sample by adjusting the window opening appropriately.

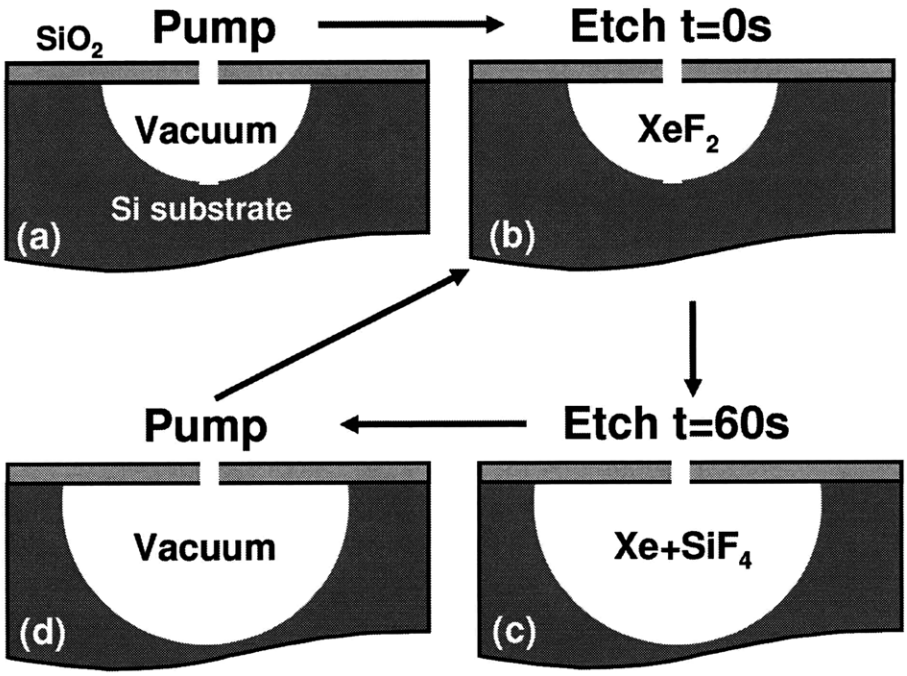

Fig. 8.7: Demonstration on how a pump-etch-pump technique is capable of achieving a large undercut using vacuum to remove the etch products.

8.2.2 Fabrication Process

The feasibility of this localized substrate removal process was tested using an extreme situation. The fabrication started with a silicon wafer with 50 nm of thermally grown SiO_2 and an 80 nm thick layer of polysilicon. This starting film was donated by Texas Instruments and the polysilicon was deposited using the same process as they use for

depositing the gate layer of the transistors. The 50 nm of SiO_2 is much thinner than the STI layer in the upcoming technology nodes and the 80 nm of polysilicon is about the same thickness as the transistor gate. Paperclip waveguide structures, for loss measurements (Appendix A), were then patterned using a positive photoresist and contact lithography. The pattern was transferred into the polysilicon layer using a Cl_2 based RIE process, taking great care to not etch through the 50 nm of thermal SiO_2. The photoresist was then striped and a 500 nm thick protective layer of SiO_2 was deposited using PECVD. Half of the samples were annealed at 800°C for an hour to close up any pinholes in this layers, the other half were left unannealed. This SiO_2 layer is used to protect the polysilicon waveguide from being etch by the XeF_2 gas and simulate the dielectric layers used in a CMOS process. Holes were then patterned next to the waveguides using a positive photoresist and contact lithography. The holes were then transferred into the 500 nm PECVD and 50 nm thermally grown SiO_2 layers exposing the silicon substrate beneath. The photoresist was then stripped with acetone before performing the XeF_2 etch.

The XeF_2 etch cycle was set up with a 60 s etch time with a 30 s pump down between etches. The sample was placed into the chamber and etched for 5 cycles (5 min total etching) and then examined with an optical microscope. Under the optical microscope it is possible to see how much of the substrate had been removed due to the differences in index of refraction of air and SiO_2. The sample was then placed back into the XeF_2 etching tool, etched for another 5 cycles, and viewed under the optical microscope to see how far the etch had progressed. This was repeated until the substrate in close proximity to the waveguides had been completely removed, as seen in Fig. 8.8. This required a total of 30 cycles. The sample was then cleaved to expose the end facets of the polysilicon waveguides for optical testing.

Three key observations were made during this fabrication. First, the polysilicon waveguides were slowly etched by the XeF_2 in the samples that were not annealed at 800°C. This demonstrated that XeF_2 can travel though pinholes in the PECVD oxide layer only a few nanometers in diameter. This was not a problem in the samples that were annealed. The second observation is that as the undercut increased the etch rate decreased. The pump-etch-pump technique should not allow this to happen since the

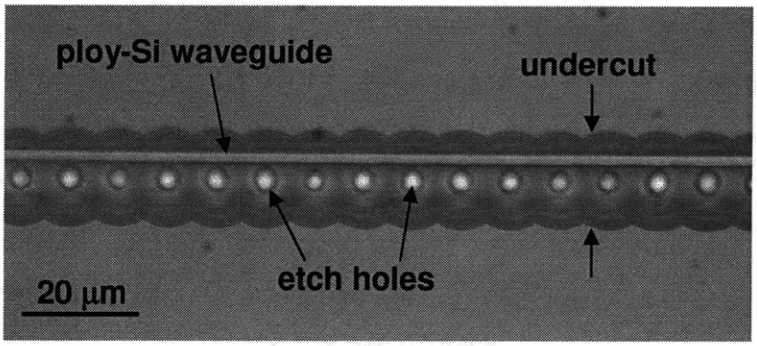

Fig. 8.8: Top-view optical micrograph of undercut poly-Si waveguide.

reaction products are pumped out and the new reactants diffuse in. Also, the surface area of the exposed silicon grows by the square of the etch radius, and the volume of the void, which is representative of the amount of reactants, grows by the cube of the etch radius, therefore this is not as simple as a decrease in reactant species. The proposed reason for reduced etch rate is that as the etch front progresses the volume of silicon being etched for a given amount of undercut is increasing, resulting in a higher temperature during the etch, reducing the etch rate. The final observation is that even after creating a large void under the waveguides the film still remains quite stable. Even after cleaving and for long curved structures, the waveguide does not collapse, as is shown in Fig 8.9.

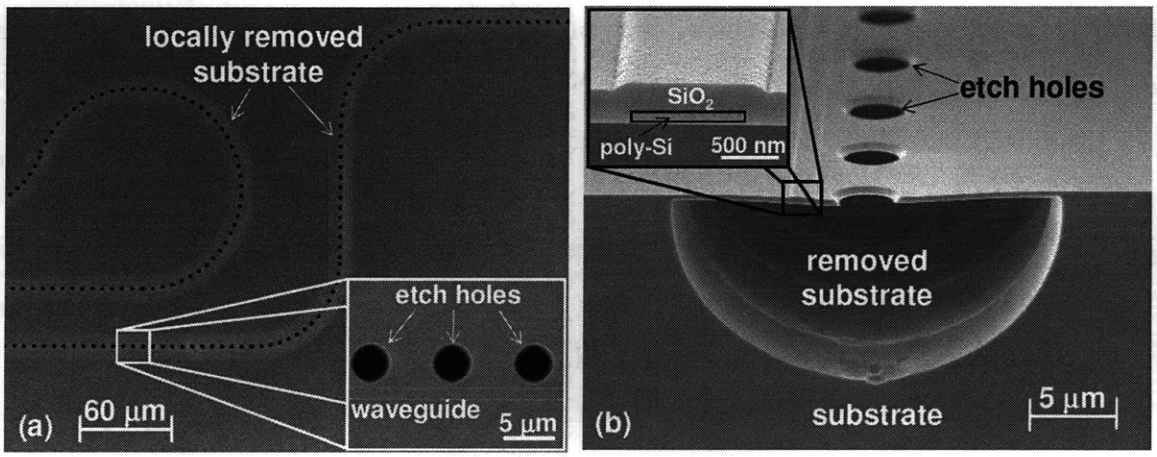

Fig. 8.9: (a) Top-view scanning-electron micrograph of undercut curved poly-Si waveguide. Inset shows zoom-in of etch holes and waveguide. (b) Cross-section scanning-electron micrograph of waveguide with locally removed substrate. Inset shows a zoom-in of poly-Si waveguide.

8.2.3 Measured Poly-Silicon Loss

After the samples were cleaved, broadband transmission measurements of the paperclip structures were taken over the wavelength range 1260 nm to 1620 nm. From these measurements it was possible to calculate the propagation loss (Appendix A), the results of which are shown in Fig. 8.10. The error bounds on these measurements are quite large due to the low number of lengths measured and the large coupling variations between each waveguide. The coupling variation is thought to be larger than normal mainly because the locally removed substrate causes the cleaving of the end facets to be less uniform. The cleave follows the crystal plane of the substrate so where the substrate is removed there is no cleave propagation guide. The highest loss of ~17 dB/cm was measured at the shortest wavelength, and the lowest loss of ~10 dB/cm was measured at longer wavelengths, with a small peak in the loss located close to 1510 nm. The small peak in loss is due to N-H and Si-H bonds in the PECVD SiO_2 layer.

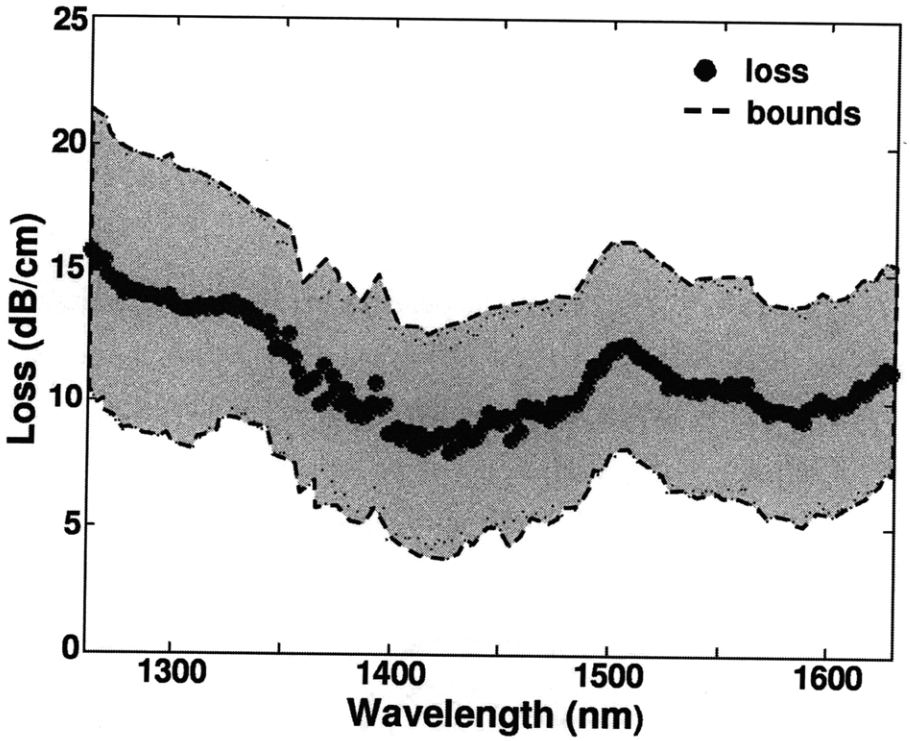

Fig. 8.10: Measured propagation loss versus wavelength for poly-Si waveguides with locally removed substrate.

These loss measurements are two orders of magnitude lower than the 1000 dB/cm expected if the substrate had not been locally removed. Note that the loss increases substantially at shorter wavelengths. The reason for this is two fold. First, the confinement of the optical mode in the polysilicon waveguide is higher at shorter wavelengths. Assuming that the majority of the loss is caused by absorption in the polysilicon this would imply that if the optical absorption is constant with wavelength the propagation loss is proportional to the confinement factor. In addition to this, the optical absorption is also thought to be higher at the shorter wavelengths. The optical absorption in polysilicon can be broken down into two sources. One is optical absorption due to mid-band gap states which are present in polysilicon due to the dangling Si bonds at grain boundaries. The other is optical absorption from above-band gap states. The bang gap of crystalline silicon is 1.1 eV, which means that the optical absorption for wavelengths below 1130 nm will be substantial. In going from crystalline silicon to polysilicon the band gap edge is blurred so that the absorption no longer has a sharp transition at 1130 nm but instead there is an absorption tail that can extends out to longer wavelengths.

8.3 CREATING WAVEGUIDES IN A CMOS LINE

Although the initial experiment demonstrated that the localized substrate removal method worked and that the polysilicon has low enough loss for testing devices, there is still much that needs to be worked out to transition this process to an actual CMOS chip. First and foremost is to make the waveguide-fabrication flow fit in seamlessly with the CMOS fabrication flow. Also, the CF_4 RIE step must be able to etch though all the materials in the dielectric stack to reach the Si surface. There are also questions about how wide of an area of the substrate can be locally removed before stress in the dielectric stack becomes a problem.

8.3.1 Transparent Fabrication

The most difficult aspect of this challenge is to make the process flow completely transparent, that is that the set of process steps are the same for a chip containing photonic structures and one with only electronics. This is important since it would enable companies to simply submit their mask layouts to any Si foundry and have their devices fabricated without the need for a specialized fabrication line, greatly reducing the cost. As mentioned earlier, the first step for creating the waveguide is to deposit and pattern the polysilicon gate layer above the STI layer. Although this polysilicon is doped in later steps either P or N-type there is a dopant blocking layer that can be used to prevent this. Also, normally the top surface of the polysilicon is silicided to provide good electrical contact, but there is also a silicide block layer that can be used to prevent this from happening to the waveguide. Once the waveguide is fabricated it is important to keep all metallization layer at least 1 μm away. This requires a block of metal layers 1 and 2 above the photonic structures. These metal layers have to be manually designed so that they meet the metal-fill requirements of chemical-mechanical polishing (CMP) while maintaining a minimum distance from the photonic components.

Although metal layers 3 through 5 are far enough away from the photonic structures as to not cause optical absorption, care must be taken to leave a metal-free area in order to couple the light into the photonic structures through vertical couplers. Also, metal-free areas must be formed in order to etch holes through to the silicon substrate. Once again, it is important to meet the mandatory metal fill requirements for CMP. It is also advantageous to place metal structures around the etch holes to help in alignment of the post-processing etch holes. If the alignment to the open etch hole area is poor the metal around the etch hole will act as a mask during the RIE etch steps. This is important since the lithography step for opening up the etch vias is done as a post-processing step where the alignment will very likely be worse than what is used in the actual CMOS line.

8.3.2 Post-Processing

This post-processing localized substrate-removal technique was tested on actual ICs to test its feasibility. The ICs were manufactured by Texas Instruments in their 65 nm-node CMOS manufacturing line. Although fabricated as part of a 300 mm wafer we received the chips after they had already been diced into 2 mm squares. When spinning resist onto chips this small a significant portion of the chip is taken up by the edge bead, formed at the edge of the chip. This edge bead, which can be tens of microns thick, posed a significant challenge since contact lithography was going to be used to define the etch holes. This problem was overcome by sticking the chip on a bigger wafer and placing tape around the chip that was the same thickness as the chip. This, in effect, made the resist not sense the effect of the chip's edge, eliminating the edge bead.

An 8 μm-thick layer of resist was spun on the chip using this method and then contact lithography was used to define the etch hole pattern. An RIE step was then performed using CF_4 gas and a 250 V bias to etch through the dielectric stack. This etch takes a total of 2 hours but is broken up into 5 min steps with a 5 min break between each etch. The reason for this is that the sample heats up during the etch, which can cause the photoresist to burn making it very difficult to remove.

Once the etch holes have reached the surface of the silicon substrate the resist is removed with acetone. The chip is than placed on a piece of tape and the sides of the chip are coated with photoresist. This is done to prevent the XeF_2 from etching the substrate form the bottom or edges, the only exposed silicon is now at the bottom of the etch holes. The chip was than placed in the XeF_2 etch chamber and etched for 5 cycles of 1 min. After the 5 cycles the sample was viewed under the optical microscope to see how much of the substrate had been removed. Fig. 8.11 shows the etch front as it undercuts some of the photonic structures on the chip during the XeF_2 etch. Undercuts with diameters as large as 80 μm were produced without any noticeable effects of stress in the dielectric stack. Once the substrate has been locally removed from under the entire photonic structure the etching is stopped and the chip is now ready for optical testing.

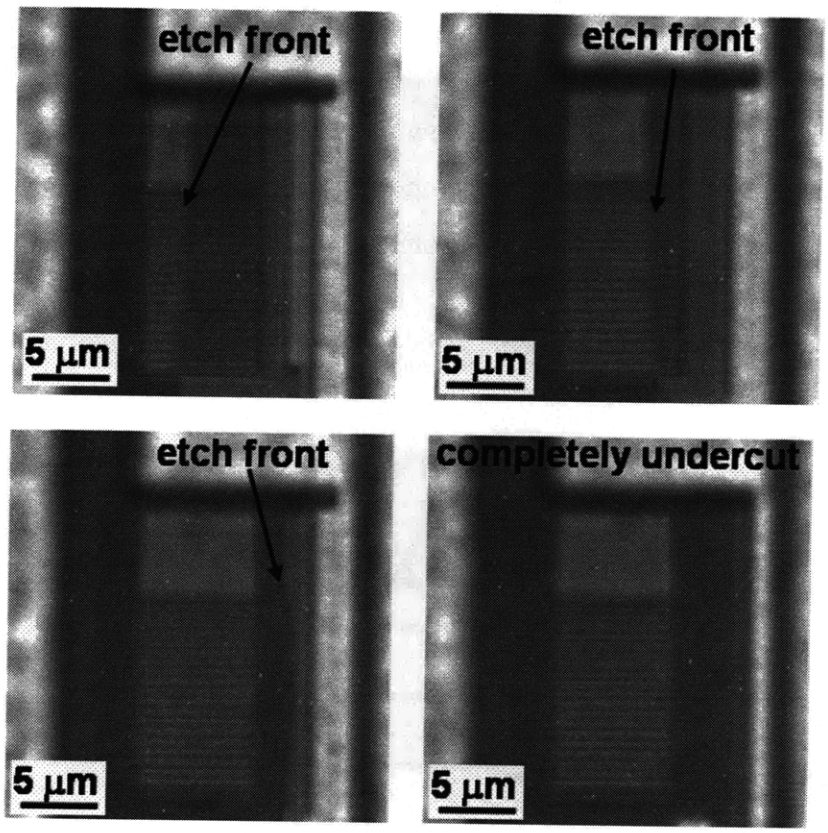

Fig. 8.11: Top-view optical micrograph of Si undercut etch front propagating under a vertical coupler. Each image is take after 5 min of additional XeF_2 etching.

After a certain time during XeF_2 etching a secondary etch front was noticeable. This usually occurred after 20-25 etch cycles. It is thought that this etch front is the XeF_2 slowly etching the thin TaN layer used as a copper barrier. It is known that XeF_2 can etch Ta at a very slow rate. This is not a problem if a different material is used for the copper barrier layer of if fewer than 25 cycles are needed to complete the full release. This would limit the localized substrate removal area to having a radius of approximately 30 µm.

8.4 CONCLUSION

We have demonstrated that it is possible to fabricated HIC photonic structures on the STI of conventional CMOS substrates by locally removing the Si substrate. This can be done as a back-end compatible post-fabrication process using XeF_2 gas. Using this process we

fabricated polysilicon waveguides with a measured propagation loss ~10 dB/cm, two orders of magnitude lower than the ~1000 dB/cm of loss expected if the substrate was not locally removed. We also demonstrated how this post-fabrication process can be used on integrated circuits, fabricated in a commercial CMOS line, enabling transparent integration of photonics with CMOS electronics.

Chapter 9

Conclusion

9.1 SUMMARY OF ACCOMPLISHMENTS

In this work, novel nanofabrication techniques for electronic-photonic integrated circuits (EPIC) were developed and characterized. This included ways to precisely control the resonant frequency spacing of microring resonator filters, enabling the fabrication of the high-performance filter banks needed for many EPIC systems. Also, supporting technologies for integration were developed including an optimized annealing process for HSQ and a localized substrate-removal method. The latter enabling the transparent integration of photonics with CMOS electronics.

The most advanced microring-resonator filter banks were fabricated, using SEBL, which enabled control in the average ring-waveguide width on a scale two orders of magnitude smaller than the SEBL address grid. This was achieved by using the electron-beam dose to precisely control the width of the ring waveguide on the tens of picometer scale. The average channel spacing of the best fabricated filter banks was within 3 GHz of the target. A dynamic postfabrication tuning method, using integrated microheaters to reduce the frequency errors in a fabricated filter bank to less than 1 GHz, was demonstrated. A static tuning method, consisting of electron-beam curing the HSQ overcladding was presented as a means to correct frequency errors without requiring constant power. This full complement of frequency control enables the fabrication of efficient, high-performance microring-resonator filter banks.

An optimized annealing process for HSQ, a spin-on glass, was developed to form a high quality overcladding material for high-index-contrast photonics. The optimized anneal consisted of heating the HSQ film in a rapid thermal processing tool to a temperature above 1000°C in an O_2 atmosphere. Using this method it was possible to

achieve a film thickness of 2.0 μm that had essentially the same optical properties as thermal SiO_2 with excellent gap-filling and planarization properties.

To enable the seamless integration of photonics with CMOS electronics a postfabrication method of localized substrate removal was demonstrated. This process relies on using RIE to etch through the backend dielectric stack, and using XeF_2 gas to locally remove the silicon substrate proximate to the photonic structures. This enables the fabrication of photonics without a thick SiO_2 undercladding layer, which is not allowed in high performance electronics due to thermal constraints. Using this technique it was demonstrated that waveguides with a propagation loss of ~10 dB/cm can be fabricated using the gate polysilicon, deposited on 50 nm of SiO_2, as the core.

9.2 FUTURE WORK

Of the work presented here I see three main areas that are in need of further research. The first is developing a way to scale-up this process so that it does not rely on the slow serial process of SEBL. The second is further exploration of static tuning of the microrings with electron-beam curing. The third is the fabrication of low-loss photonic devices in a commercial CMOS line utilizing the localized substrate removal postfabrication technique.

A few methods of process scale-up were presented in section 4.4. The two that I believe are of the most interest to academic research are nanoimprint lithography and zone-plate-array-lithography (ZPAL). Using the SEBL techniques described in this thesis it should be possible to make a nanoimprint template for microring-resonator filter banks. Since nanoimprint lithography is always described as capable of accurately replicating features on the imprint template, it should be able to replicate the resonant frequency spacing of the filter bank. Also, by measuring the resonant frequency spacing of filter banks fabricated using nanoimprint, it will be possible to confirm how well the dimensions are replicated. The advantage of using ZPAL to scale up this process is that it would demonstrate how new maskless lithography tools help address some of the unique fabrication challenges of photonic devices. ZPAL might not out perform projection lithography in minimum feature size, but it may be able to make superior filter

banks by taking advantage of its ability to adjust the exposure dose for each microring individually.

The work presented here on static tuning of the resonant frequency by electron-beam curing of the HSQ overcladding only scratches the surface of the potential of this method. Two aspects that need to be explored further are; how the thermal annealing history of the HSQ affects the electron-beam dose needed for the desired tuning and, are there any other types of overcladding materials for which this method could be used. I believe that this could make a good masters project for an interested student.

The post-processing method of localized substrate removal makes it possible to fabricate low-loss photonics in a commercial CMOS process. It has, however, been very difficult to do this for three main reasons. One is that there is much secrecy in the actual CMOS fabrication flow, preventing an outside researcher from knowing all the details that may effect photonic device performance. The second is the long research cycle. It can take 6 months to a year from the time of design of the chip to its actual delivery, making it a very slow process to debug. The final reason is that the area on a wafer in a CMOS process flow is very expensive and the sample size typically received is only 2 mm X 2 mm. This small size makes every part of the fabrication process more difficult due to handling challenges and edge effects. For progress in this area to be made at an acceptable rate, I believe the research needs to be an equal collaboration between a CMOS foundry and academic researchers. This in itself can be a challenge due the "openness" of university research and the proprietary nature of industry. However, the recent surge in fab-less and fab-lite IC companies have put pressure on CMOS foundries to be more open with their processing details, possibly laying the ground work for university collaboration.

Appendix A

Loss Measurement Methods

When fabricating photonic devices one question that always needs to be answered is, what is the propagation loss? Propagation loss can be very difficult to measure. Over the course of my thesis work I have employed three different methods for measuring the propagation loss. Each method has its own advantages and disadvantages, making it important to have structures in every fabricated layout that can be used for each method

The first loss measurement method is cut-back. In this method, one measures the transmitted power through different lengths of waveguides. By plotting this data as power (dB) versus length (cm) the slope will equal the propagation loss. One problem with this method is that for each length the sample must be cleaved. The randomness of the cleaving will result in a significant coupling-loss variation which will add to the error of the measurement. To avoid this problem, one can use so-called "paperclip" structures, shown in Fig. A.1, to measure different lengths without having to recleave the sample. In the paperclip structures the length of the straight section is different for each paperclip, but the length of curved sections is kept the same. A few disadvantages of using the cut-back method is that it does not work well for samples with very high or very low propagation loss. If the loss is too high (> 50 dB/cm), it will not be

possible to get power through long enough lengths to get accurate loss data. When the loss is too low (< 2 dB/cm), the end-facet coupling variation will dominated the measurement.

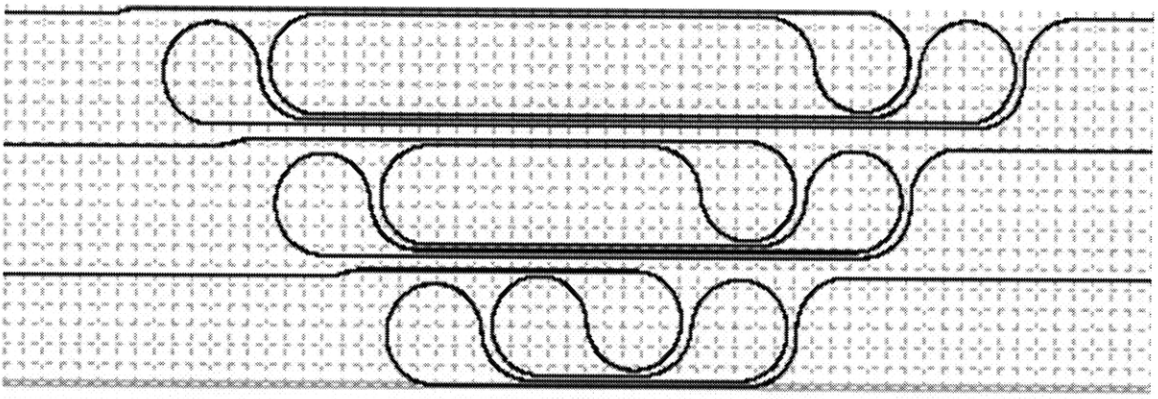

Fig. A.1 Layout of a paperclip structures with three different lengths.

A second method for measuring the propagation loss is to measure the Q factor of a weakly-coupled large-radius microring-resonator filter. For weakly-coupled filters with a drop-loss greater than 15 dB the Q factor is dominated by the propagation loss. Using Eq. A.1, where n_g is the group index and λ is the resonant wavelength in meters, the propagation loss can be calculated from the Q factor. The main advantage of this method is that it is possible to get a very accurate loss measurement from just one device. The disadvantage, however, is that one gets a loss measurement at the resonant frequency making it hard to determine how loss varies with wavelength.

$$\text{Loss (dB/cm)} = \frac{(0.2*\pi*n_g)}{(\text{Ln}(10)*\lambda*Q)} \qquad \textbf{A.1}$$

A third method for measuring the propagation loss is to image the surface of a waveguide during operation with an infrared camera. The infrared camera will pick up light that is scattered from the waveguide, which is proportional to the total power of

light in the waveguide (Fig. A.2). By plotting the intensity of light as a function of position in the image, and fitting it with an exponential decay function the exponent will be proportional to the propagation loss of the waveguide. The advantage of this method is that it is possible to get a loss measurement with only one straight waveguide. The main disadvantage is that there has to be significant light scattered from the waveguide for the camera to pick up. This method is best suited for measuring very high propagation losses.

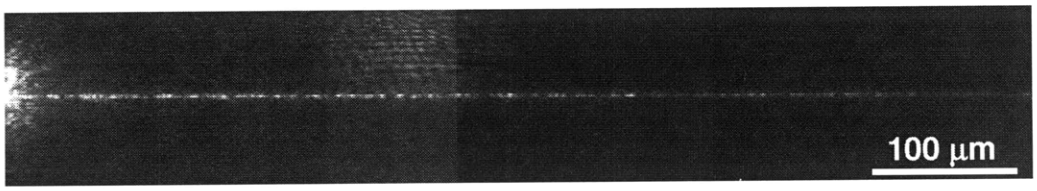

Fig. A.2 Image take with an IR camera of light scattered off a waveguide. By measuring the exponential decay of the intensity it was found that the loss of this waveguide was 140 dB/cm.

The best method to use for measuring propagation loss depends on the magnitude of loss and the dominate loss mechanism. Therefore, it is advisable to fabricate during every fabrication run a full compliment of loss structures including; paperclips, weakly-coupled microrings, and straight waveguides.

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