Reliability of GaN High Electron Mobility Transistors on Silicon Substrates

by

Sefa Demirtas

B.S. Electrical and Electronics Engineering, Bogazici University, 2007

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of

Master of Science in Electrical Engineering

at the
Massachusetts Institute of Technology

June 2009

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ABSTRACT

GaN High Electron Mobility Transistors are promising devices for high power and high frequency applications such as cellular base stations, radar and wireless network systems, due to the high bandgap and high breakdown field of GaN. However, their reliability is the main hindrance to the deployment of these transistors in a wide scale. In this study, we have investigated the reliability of GaN HEMTs grown on Si substrates. The large lattice and thermal mismatch between GaN and Si adds an additional reliability concern as compared to conventional substrates such as SiC and sapphire. We have performed systematic electrical stress experiments to understand the physics of degradation in these devices. Relevant device parameters are recorded continuously during these stress tests by a benign characterization suite. We conclude from these experiments that high voltage stress conditions are more effective in degrading the device than high current conditions. High voltage stress is found to impact the device in two different ways. The first is increased trapping in the large number of traps in the highly mismatched device structure even before any stress. The second is through the converse piezoelectric effect discussed by *Joh et al.* for GaN-on-SiC devices. We also have found evidence that these two mechanisms are connected. We have used UV illumination to enhance detrapping and shown that trapped electrons screen the electric field in the device and increase the critical voltage at which gate current degrades.

Thesis supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

Acknowledgements

First of all, I would like to thank my advisor Jesus A. del Alamo for letting me work with him and benefit from his endless knowledge, valuable experience and best teaching style. His clear way of thinking has taught me much more than what I would get by just reading, experimenting and studying. He was always encouraging by showing trust in me and my work. I would not have acquired so much confidence and knowledge without having his spectacular guidance.

My work would be impossible without our collaborator Nitronex Corporation. Their devices were the heart of this research and they generously provided me with them. I also had a very fruitful summer internship at Nitronex Corporation and had the chance to spend a beautiful summer with great people in North Carolina.

I feel very lucky for collaborating with fascinating team members in my project. I would like to acknowledge the great help I received from Jungwoo Joh from my very first day at MIT. He was always very patient with me as his "apprentice", teaching everything from how to screw the probes gently to how to run his sophisticated codes that made it possible for my research to "go". I would also like to thank Alejandro Ojeda for working with Jungwoo on the characterization suite that I used throughout this work and thus providing me with very valuable tools for my research.

I always had the feeling that I was surrounded with "extremely" fun people! My former officemate, Niamh Waldron, had solved how things at MIT run before I came and she was very willing to teach that to me. My current officemates Donghyun Jin and Tae-Woo Kim are not only teaching me Korean but also purging any stress fragment out of my office by their cheerful laughters filling the corridors of the sixth floor. I will always remember the friendliness of my groupmates Usha Gogineni, Ling Xia, Yoshihiro Ikura and Dae-Hyun Kim. I am glad to see always smiling faces of the "sixth floor residents" Melissa, Steve, Nicole, Omair, Will, Bin, Han, Leo and all others.

I would like to express gratitude toward my friends Saban and Huseyin, who have not left me alone after undergrad and followed me to Boston for many more years of true friendship. I appreciate the great company I received from my fellows Ozan and Halil, and their support at my hard times. Orcun, Ilke, Baris, Burak, Yunus, Burkay and all others in Boston and back in Turkey – I always enjoyed your cheerful friendship.

I would like to thank my dearest family for always loving me and supporting me with whatever I do. It is a great feeling to know that no matter how I mess things up; they will be there for me. I am really lucky to have them, I love them and I wish the best for them.

Not only this work would be impossible but anything in the world would be unbearable without the warmth of my precious love, Selda. She has the ability to support me overseas and make me smile at my hardest times. I am the luckiest guy in the world to have met her and will be grateful all my life for the treasure I found years ago.

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Chapter 1 : Introduction

1.1. Introduction to GaN HEMTs

Gallium Nitride is a semiconductor with a bandgap of 3.4 eV. An offshoot of such a wide bandgap is a high breakdown field of 3 MV/cm. It is also this bandgap that enables blue, green and white LEDs to be manufactured by using GaN as well as a blue-light semiconductor laser. The high breakdown field is of great importance in transistors since this enables operation at high power without the onset of breakdown induced at high voltage [1]. GaN is also known to be a polar and piezoelectric material because of its non-centrosymmetric crystal structure as is the case of most nitride semiconductors [2]. One of the ways that researchers have explored to manipulate these aspects of GaN structure is to build High Electron Mobility Transistors (HEMT) with AlGaN/GaN heterojunctions.

Figure 1-1 shows one such transistor [3]. HEMTs make use of heterojunctions to achieve separation of carriers from their source and thus decrease scattering during conduction. A further advantage of heterojunctions is the confinement of carriers to a relatively narrow and deep quantum well formed by the discontinuity of the conduction bands of the two neighboring semiconductors (in this case GaN and AlGaN). The source of 2DEG populating this well in most materials is doping in the wide bandgap material. This often serves also as barrier to confine electrons to the channel. In the AlGaN/GaN system, there is no need for doping because the

spontaneous polarization difference between these two materials readily induces considerable charge at the heterojunction. The piezoelectric effect adds more to this charge because of the tensile strain in the AlGaN barrier which has a smaller lattice constant than GaN. The overall result is a 2DEG density in excess of $2x10^{13}$ cm^{-2} and currents of 1000 mA/mm without doping [4].

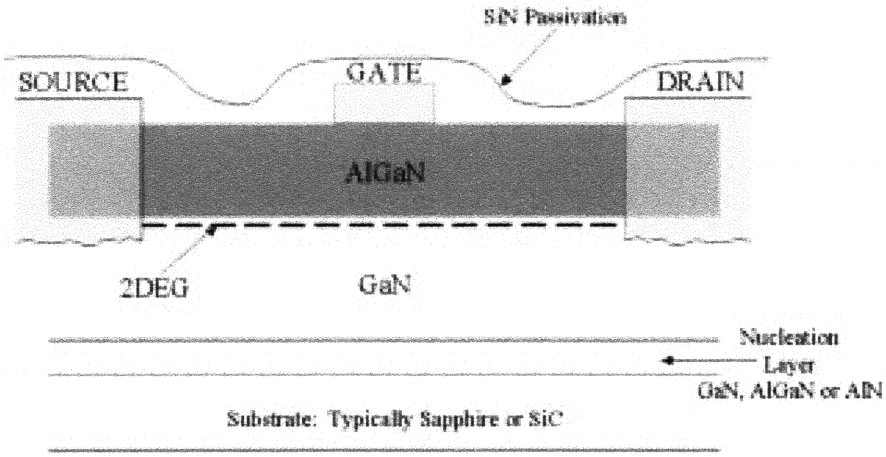


Figure 1-1: A HEMT structure that uses an AlGaN/GaN heterojunction [3]

GaN HEMTs can provide very high power and amplification because of high breakdown fields and high current delivery capabilities as described above. They are also suitable for very high frequency and high temperature applications. Not many semiconductors have these properties and none has all at once other than GaN. Thus, GaN HEMTs have a very promising potential of use in military applications, radar and satellite communication links, cellular base stations and many other "harsh" operating environments [1].

State-of-the-art GaN HEMT transistors have shown breakdown voltages up to 1.3 kV with very low ON resistances [5]. Power densities obtained from GaN HEMTs are also increasing over time. There have been reports of a pulsed output power density of 10.2 W/mm at 2.14 GHz when biased at 60 V on Si substrates [6]. More recently, 13.7 W/mm have been attained at 30 GHz for the same bias condition but on SiC substrates [7].

1.2. Silicon as a substrate

GaN HEMTs still suffer the lack of an inexpensive native substrate with a matched lattice constant and thermal expansion coefficient. The search for a different substrate other than GaN stems from the fact that GaN ingots are very difficult to make due to the high melting temperature and high N_2 equilibrium pressure at high temperatures [8]. As a result, several materials are being investigated and fewer of them have been commercialized including GaN itself, silicon carbide, sapphire, diamond, aluminum nitride and silicon [9].

The greatest competition as potential substrates for GaN HEMTs is between SiC, sapphire and more recently Si. SiC has a relatively good lattice match with GaN and a very good thermal conductivity, however it is an expensive choice and the substrate size is limited. Sapphire substrates, on the other hand, are more economical than SiC substrates, yet they exhibit poor thermal conductivity. Silicon substrates are extremely advantageous in terms of cost and availability in large diameters. Moreover Si is a very well characterized material for which many processing tools have been developed. However, large lattice and thermal mismatch between GaN and Si is problematic. Table 1-1 shows the lattice mismatch between GaN and different substrates as well as values of thermal expansion coefficients. There is signicant amount of research going into overcoming such disadvantages of Si and utilizing its large availability and low cost.

Table 1-1: Lattice mismatch of different substrates with GaN and their thermal expansion coefficients

Material	Percent Lattice Mismatch with GaN	Thermal Expansion Coefficient ($x10^{-6}$ /^{0}K)
GaN	0%	5.59 [9]
6H-SiC	3.5% [10]	4.50 [11]
Sapphire	16.1% [10]	8.1 [12]
Si	16% [13]	3.6 [12]

1.3. Motivation

GaN HEMTs have already shown reliability issues even when grown on relatively well matched SiC substrates such as decrease in drain current and increase in gate leakage current, drain and source resistances. Although Si is a very attractive alternative to SiC as a substrate, with greater

lattice and thermal mismatch, GaN layers grown on Si substrates tend to have many more dislocations. Threading dislocation densities on the order of 10^8 cm^{-2} have been observed in GaN-on-SiC and GaN-on-sapphire devices whereas they amount to 5-7x10^9 cm^{-2} for GaN-on-Si [14]. This brings additional concerns to the reliability of GaN HEMTs fabricated on Si substrates. There are studies addressing the reliability of GaN HEMTs on other substrates. However, to the best of our knowledge, no explicit reliability tests have been conducted to understand the physics of degradation in GaN-on-Si devices. In this thesis, we aim to understand the unique physical mechanisms underlying the degradation of GaN HEMTs on Si substrates through several reliability tests.

The most attractive aspect of GaN HEMTs is their ability to work at very high temperatures and high frequencies while still delivering very high power. This requires that high current levels are established and maintained at these levels for reliable operation. However sustained bias conditions often result in a decrease of drain current, which in turn decreases the output power performance of these devices. Figure 1-2 shows a drain current degradation experiment on GaN-on-Si HEMTs where V_{DS} = 28 V and I_D = 2.3 A on devices with a gate length of 0.7 um and gate width of 36 mm [15]. It is clear that substantial degradation can occur under prolonged stress and the degradation is thermally activated. However, we will not investigate the effect of temperature on degradation in this study.

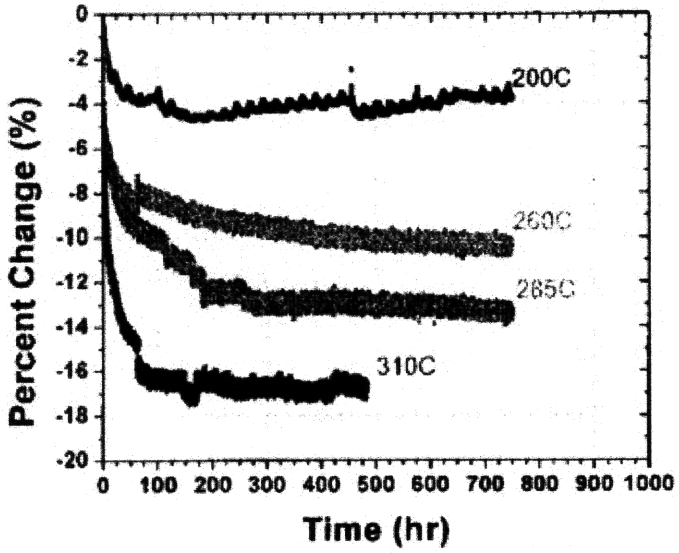


Figure 1-2: Current degradation in GaN HEMTs on Si over time at sustained DC bias conditions (V_{DS}=28V, Id=2.3A) and for different temperatures [15].

1.4 Previous Work

GaN HEMT performance degradation has been observed mostly in the forms of maximum drain current decrease, RF power slump [16-18], transconductance decrease and drain resistance increase [19, 20]. Although these changes take place during regular operation of GaN HEMTs, accelerated stress methods have been widely used by several authors to quickly determine reliability issues related to these devices. This usually helps to identify degradation mechanisms and observe changes in devices as GaN HEMTs normally degrade within a few hours of device operation under harsh conditions [21].

One of the degradation mechanisms that have been referred mostly is hot electron related degradation [22-24]. Braga et al. discussed that hot electrons overcome potential barriers associated with the heterojunction, spread to the barrier and bulk regions where they are captured by traps [25]. On the other hand, Vetury et al. have shown evidence that surface states charged with electrons could decrease the drain current significantly by acting as a virtual gate as shown in Figure 1-3 [26].

Surface passivation is believed to decrease trapping at the surface states which are due to the abrupt interruption of the crystal structure. Koley et al. have shown that the surface potential indeed decreases by increased electron trapping at these states [27]. Kim et al. compared degradation of devices with unpassivated surfaces to those passivated with SiN as in Figure 1-1 and observed that gate lag is removed by SiN passivation [22]. However, after a hot electron stress under high stress voltages, gate lag was observed even in the passivated device, which was attributed to a possible change in the trap density after stress [19, 28]. Kim et al. have also shown that SiN passivation improves reliability in this manner better than SiO_2 passivation [22]. Besides surface passivation, researchers have observed that a thin GaN cap layer on top of the AlGaN barrier improves stability by controlling the so called polarization-induced surface charges [29].

The effect of temperature on reliability has also been studied. Elevated temperature life-tests at high current conditions have revealed that the drain current and the transconductance decrease noticeably above 195^0C as well as the channel ON-resistance although the gate diode characteristics remained more or less the same [30]. The authors argue that the increase in channel on-resistance at these high temperatures is not due to hot electron effects because of the negative temperature coefficient of this degradation mechanism. No ohmic metal or gate metal interdiffusion into the epitaxial layers is observed after elevated temperature stress.

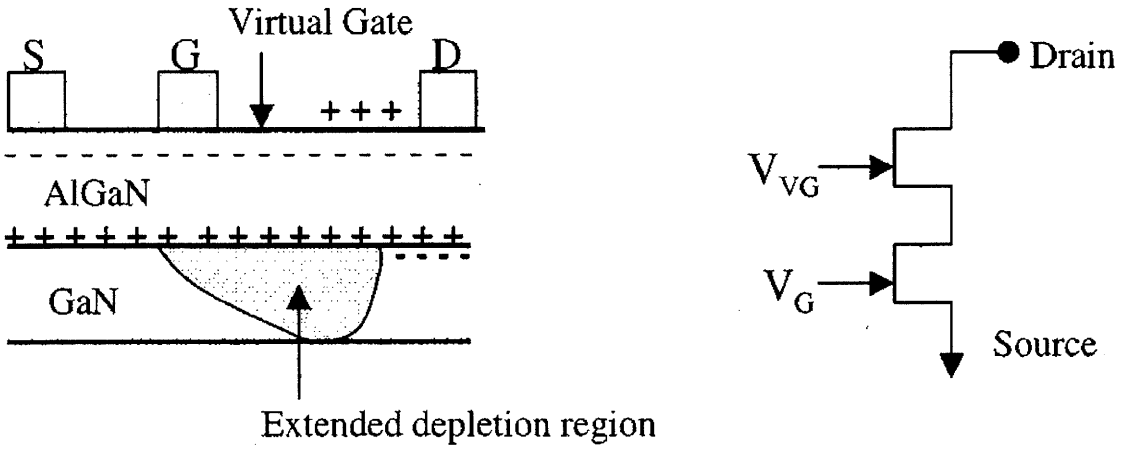


Figure 1-3: The virtual gate effect produced by the electrons trapped at surface states [26].

Most recently, Joh et al. have observed a degradation mechanism that does not appear to be caused by hot electrons, where devices stressed under high current but low voltage conditions show less degradation than low current high voltage stress conditions [20, 21]. Their experiments reveal that high voltage stress is the main reason for device degradation, which shows itself as permanently increased gate leakage current by several orders of magnitude [31] along with decrease in drain current and increase in parasitic resistances. They have postulated that converse piezoelectric effect causes defects to form on the drain edge of the gate under high electric fields. Focusing on gate leakage current as an indicator of degradation is justified by Inoue et al. as they have recorded longer lifetimes for their transistors which have less gate leakage to start with [32].

To date, reliability studies have rarely focused on the substrate; hence not much literature about GaN-on-Si reliability has been published. Jia et al. have proposed using patterned Si substrates to grow AlGaN/GaN heterojunctions to avoid the cracks and increased dislocations [33] whereas others have used sophisticated transition layers to account for the large mismatch between GaN and Si [34-36]. However, none of these has tried to compare reliability and physics behind the degradation of GaN-on-Si devices to those on conventional substrates. In this work, we are trying to address additional reliability concerns due to using a highly mismatched Si substrate and in fact most of our results show similarities to those reported in [21].

1.5 Outline of Thesis

In this study, we have focused on accelerated DC stress conditions that will help us identify the physics of degradation mechanisms of GaN HEMTs on Si substrates. Since enhanced trapping behavior is observed, we will also try to distinguish permanent degradation from simple trapping-detrapping processes.

In Chapter 2, we will describe the standard devices that were tested, the stressing schemes and the figures of merit that are monitored by our characterization suite. The experimental tools will be explained and the pre- and post stress evaluation methods for our devices will be described.

Chapter 3 will mainly focus on the observations made in fresh devices and the results of different stress experiments as described in Chapter 2. Results for GaN-on-Si devices will be compared to GaN-on-SiC devices where applicable. Strong evidence of trapping behavior will be presented and enhanced detrapping under UV light will be studied.

Chapter 4 will discuss the degradation mechanisms observed in GaN-on-Si HEMTs and more experiment results that conclude our discussions will be presented. Chapter 5 will conclude our study.

Chapter 2 : Experimental Procedures and Evaluation

2.1 Introduction

This chapter describes the experimental techniques followed in this research. First, structure of devices used in this study will be explained. Different experimental procedures will be introduced to help identify different aspects of the degradation observed in GaN-on-Si HEMTs. The figures of merit that are monitored to identify degradation are described along with a current transient analysis that helps the evaluation of degradation before, during and after the stress tests.

2.2 Test Devices

The devices used in this project are fabricated by Nitronex Corporation. Figure 2-1 shows a standard device [37]. A high resistivity silicon (111) substrate is used to host an intrinsic GaN buffer of 0.8 μm in thickness. The heterojunction is formed between this GaN buffer and an 18 nm thick AlGaN barrier layer. The conduction band discontinuity between AlGaN and GaN confines the 2DEG induced by polarization in the channel just below the channel-barrier interface. There is 15 Å thick GaN cap layer on the AlGaN barrier layer. The Al composition of the barrier level (x) is 0.26. The sheet carrier density (n_s) and the carrier mobility (μ) obtained within this channel are 8.5×10^{12} cm^{-2} and 1500 $cm^2/V\text{-}s$, respectively. A source field plate is utilized to decrease the peak electric field in the structure. The gate to source spacing (d_{gs}) is 1

μm whereas the gate to drain spacing (d_{gd}) is 3 μm. Gate length (L_g) is 0.5 μm and the gate width is 2x25 μm.

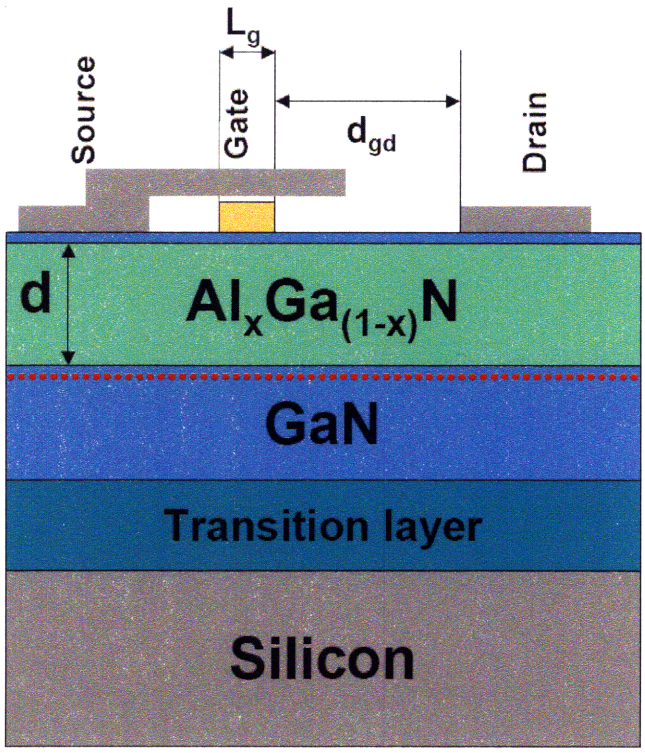


Figure 2-1: Standard devices used in this project [37]

Figure 2-2 shows a cross-sectional scanning electron micrograph of the transition (and the nucleation) layer between the Si substrate and the GaN buffer [37]. The purpose of this transition layer is to mitigate stress due to thermal expansion coefficient mismatch between the substrate and the buffer. On the other hand, the nucleation layer alleviates the lattice mismatch between these two structures. The silicon substrate is thinned to 150 μm to enhance heat conduction.

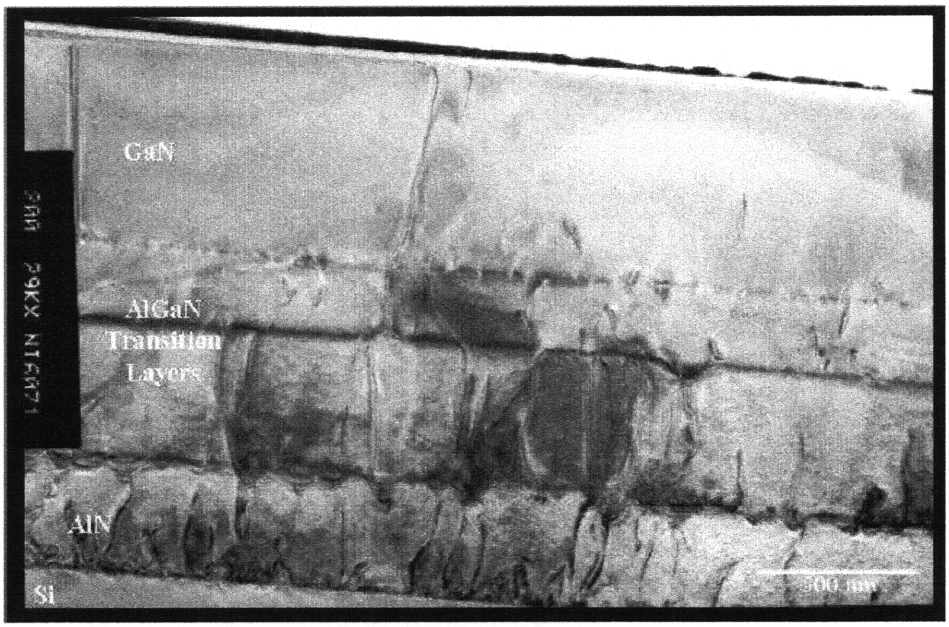


Figure 2-2: Cross-sectional scanning electron micrograph of the transition and the nucleation layers [37]

2.3 Experimental Tools

This project took place at Microsystems Technology Laboratories at MIT. We used two semiconductor parameter analyzers (SPA) interchangeably, namely HP4155 and B1500 to stress the devices and do all the measurements. Although it was possible to take measurements manually, we utilized the characterization suite that was also used in [21, 38]. This characterization suite runs from a computer and controls the semiconductor parameter analyzer through a GPIB connection. Custom stress tests could be designed and interrupted as frequently as desired to monitor the figures of merit (FOM) of the devices. The FOMs will be described in Section 2.4 and the stressing schemes that were mostly utilized in this project will be introduced in Section 2.5.

The devices were mounted on a metal chuck in a Cascade probe station and were probed using two RF probes from GGB Industries. The chuck temperature is controllable by means of a temperature controller in the range of -60^0C to 200^0C.

2.4 Figures of Merit

The characterization suite involves a benign set of measurements that allows us to monitor the device characteristics during the experiment. In our approach, the electrical stress is interrupted at predefined intervals, and the characterization suite performs a variety of measurements to extract figures of merit that characterize the device. Finally the stress conditions are resumed. We repeat this cycle with some frequency until the end of the test. The monitored figures of merit are described in Table 2-1. In [21], it is shown that measuring these figures of merit by using this benign characterization suite has indeed negligible effect on devices.

Table 2-1: Device parameters monitored during characterization

FOM	Description
I_{GOFF}	Gate leakage current. Measured at V_{GS}=-5 V and V_{DS}=0.1 V.
I_{DMAX}	Maximum drain current. Measured at V_{GS}=2 V and V_{DS}=5 V.
R_D	Drain resistance. Measured as V_{DS}/I_{DS} when I_G=-I_D=20 mA/mm (that is, I_S=0).
R_S	Source resistance. Measured as V_{DS}/I_{DS} when I_G=20 mA/mm and I_D=0 (that is, I_S=-I_G).
V_T	Threshold voltage. Defined as V_T=V_{GS}-0.5V_{DS} when I_D=1 mA/mm and V_{DS}=0.1 V.
SS	Subthreshold swing. Measured at I_D=1 mA/mm and V_{DS}=0.1 V.

The measurement of maximum drain current at V_{GS}=2 V results in turning on the gate diode. Since the voltage on the drain side is still 3 V higher than the gate voltage, the forward current flows mostly to the source. Therefore the drain current measurement is still reliable, however increasing the gate voltage beyond 2 V to increase the channel charge may result in excessive heating due to the strongly ON gate diode and this was not performed.

2.5 Electrical Stressing Schemes

In our study, we have followed the approach of [21] and focused mostly on short term degradation of GaN HEMTs as they usually degrade within a few hours. Since DC stress is easier to apply, results are easier to analyze and the physical degradation mechanisms are identified more effectively in this simple setup. Because of this, we have used DC stress conditions throughout our study. However, a clever choice of stressing bias conditions should be made to yield meaningful results as described here. These are illustrated in Figure 2-3.

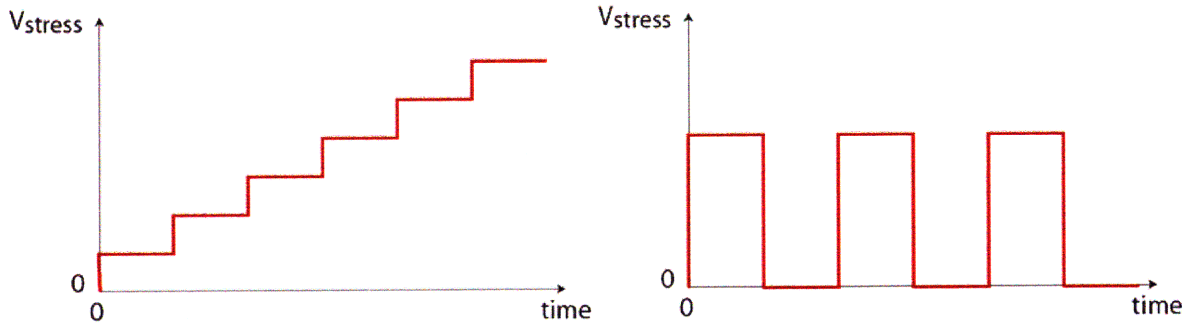


Figure 2-3: Stress schemes used in this study- left: step stress, right: stress-recovery [21].

2.5.1 Step-Stress Experiments

The first type of stress scheme is the step-stress mode. Although we use many constant voltage and constant current stress tests, step stress tests are useful as they sweep through various stages of stress and allow us to observe the changes in FOMs more effectively. This also reduces the stress time considerably because stepping the stress corresponds to the case where stress is held constant at lower values for a longer period. This is a productive method as many conditions can be studied in a single experiment. This is illustrated in the left of Figure 2-3.

2.5.2 Stress-Recovery Experiments

The stress is applied to and then removed from the devices for predefined time periods; however the characterization suite continues to take measurements of FOMs. This test is useful to figure out the behavior of FOMs under constant stress and compare it to the recovery period where no stress is applied. This idea is illustrated in the right of Figure 2-3. This stressing scheme helped evaluating trap dynamics in the device.

2.6 Stress Biasing Schemes

Vds=0 V stress: The gate voltage is held at negative values (down to -80 V) as the drain to source voltage is kept as 0 V. This stress scheme is designed to stress both the drain and source sides of the gate because the voltage difference between gate-source and gate-drain terminals is the same. The channel is almost completely depleted beyond V_{GS} = -5 V, therefore there is

negligible drain current. The stress is due to the high electric field built on both sides of the gate. The reverse current flowing through the gate is composed of the current coming from the drain and that from the source. These currents are on the order of few microamperes per millimeter, hence there is negligible power dissipation in this stress mode. The use of this bias scheme in a step-stress experiment is illustrated in Figure 2-4a.

OFF-State stress: The drain voltage is held at high voltages (up to 80 V) as the gate voltage is kept constant at a negative enough value (usually -5 V) to assure the channel is depleted. This stress method is supposed to stress mostly the drain side of the gate as this side is experiencing the increase in the stressing voltage whereas the gate to source voltage is constant. Similar to the V_{DS} = 0 V stress case described above; there is a reverse diode current through the gate. However, this comes mostly from the drain side as $|V_{GS}|$ is usually very small compared to $|V_{GD}|$. The stress is due to the high electric field built on the drain side of the gate. There is negligible power dissipation as in the V_{DS} = 0 V stress because the OFF state current is on the order of a few microamperes per millimeter. The use of this bias scheme for step-stress experiments is illustrated in Figure 2-4b.

High-Power State stress: The gate voltage is adjusted to maintain a high and constant stressing current as the drain voltage is held at high voltages (up to 60 V). This stress method is designed to stress the channel with hot electrons as well as the drain side of the gate with the high voltage. The use of this bias scheme in step-stress experiments is described in Figure 2-4c. Although we often utilized this step-stress scheme, the high power dissipation caused the channel temperature to increase and complicate the outcomes of the experiments. Calculation of channel temperature is essential if only this stress scheme is used. However we have adapted a technique where we compare the results of high power step stress to constant voltage experiments. In this new scheme, the current is stepped so that the power dissipation is the same for both experiments. Hence, differences observed in the two stressing schemes will not be due to temperature as the channel will have the same temperature in both cases.

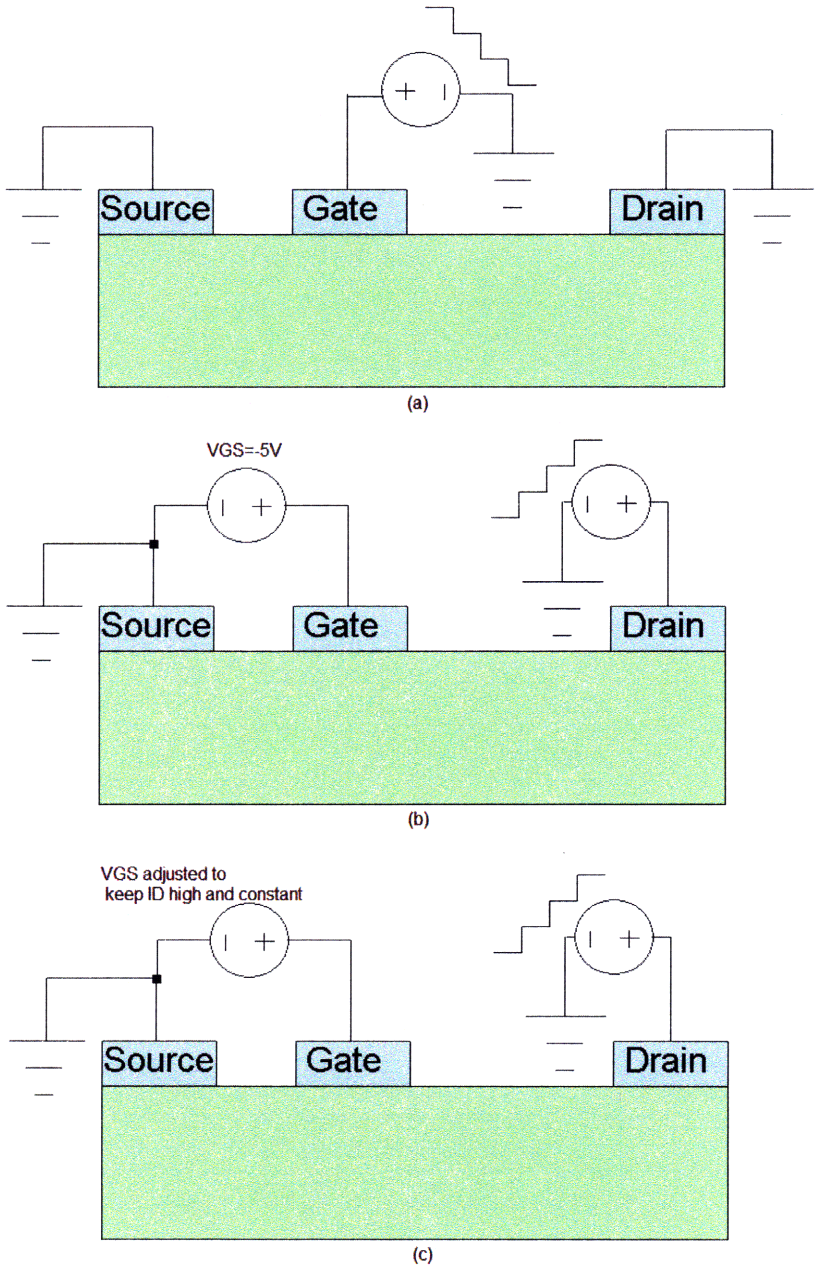


Figure 2-4: Different step-stress configurations: (a) V_{DS} = 0 V step-stress; (b) OFF State step-stress; (c) High Power State step-stress.

2.7 Evaluation of Trap Density

As it will be clearer in the following chapters, stress-recovery type experiments show strong trapping behavior in the test devices. After removing the stress, the recovery period starts but not

all the figures of merit can reach their original values before the stress right away, if they ever do. They rather show a transient behavior and sometimes this process can be very sluggish.

This type of behavior suggests that traps might be affecting the change in FOMs over time. However, the amount of this sluggishness is generally observed to have increased after degrading devices in some sort of stress scheme probably due to the fact that new traps are produced during the experiment. This also increases the current collapse. This observation leads to the idea that current collapse can be a tool to study trap concentrations.

For this analysis, usually a very short pulse is applied to the gate of the device and as a representative of other parameters, the drain current in the linear regime is monitored since it usually has the characteristic transient behavior like most other parameters. We call this figure as I_{Dlin} and measure it at V_{GS}=1 V and V_{DS}=0.5 V to ensure operation in the linear regime.

We introduced such pulses during stress experiments as well and measured the collapse in I_{DMAX} to have a sense of increased trap concentrations introduced by the stress. We applied negative gate voltage pulses where the amplitudes of the pulses were stepped to reach deeper traps as shown in Figure 2-5. This method is called step diagnostics and will be discussed in detail in the next chapter.

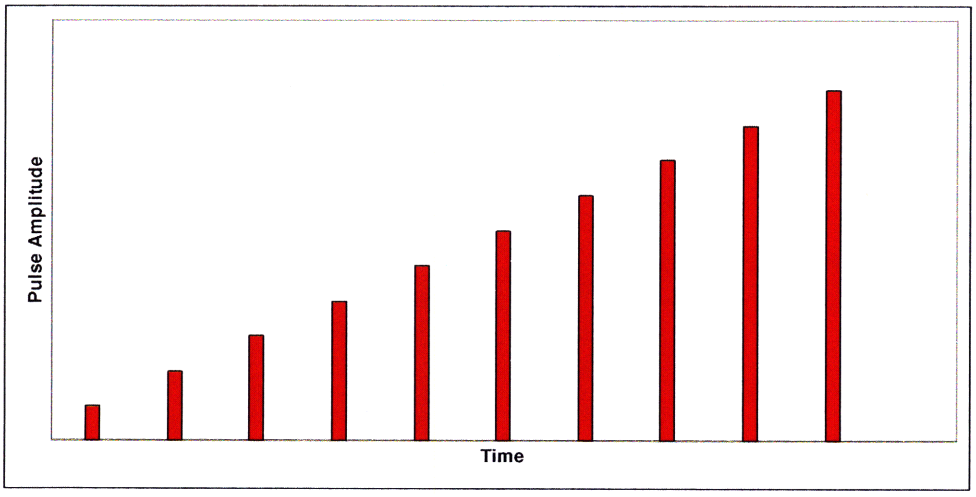


Figure 2-5: Stepped amplitude for the gate pulses used for measuring current collapse in the devices.

2.8 Summary

In this chapter, we described the devices that were used to perform our reliability studies. We also described the device figures of merit that were monitored during a stress test. Finally different stress experiments and bias conditions that were used in our study were introduced. These different sets of stressing schemes helped us to create degradation in selected ways. The characterization suite provided us with insights into the possible origins of degradation, as described in the following chapters.

Chapter 3 : Electrical Degradation of GaN HEMTs on Silicon

3.1 Introduction

In this chapter, we will start discussing the effect of traps in fresh GaN-on-Si HEMTs. Studying traps is essential as the large mismatch between GaN and Si has the potential to increase the number of traps. These traps may not only affect the device performance but also alter the consequences of stress and impact degradation mechanism. After that, the results of several stress experiments, as described in the previous chapter, will be shown. Key degradation phenomena will be presented for several figures of merit of the devices. The difference between physical degradation and trapping will be studied and the chapter will be concluded by other observations made in GaN-on-Si devices.

3.2 Traps in Fresh Devices

Silicon substrates are not well-matched substrates for GaN HEMTs in terms of lattice and thermal constants, therefore the devices are expected to have more dislocations and associated traps than devices on SiC substrates. This is true even before any degradation is introduced to the device. In our experiments we monitor I_{Dlin}, which is the drain current at V_{DS}=0.5 V and V_{GS}=1 V. Figure 3-1 compares normalized current (I_{Dlin}) transients observed in virgin GaN-on-Si and GaN-on-SiC devices after a one second pulse of -10V at the gate when V_{DS} = 0 V. The purpose

of such a short pulse is to "pump" electrons into the traps which get negatively charged and hence suppress the 2DEG in the channel, causing a sudden decrease in drain current. As time goes on, these electrons will be detrapped from these states allowing the current to "recover" to its original value before the pulse. Our experiments show a higher current collapse and a slower recovery in devices on a Si substrate when compared to devices on a SiC substrate. Clearly this shows that the higher mismatch between the GaN heterostructure and the Si substrate causes more traps than on a SiC substrate. Moreover, both transients have very slow components with time constants larger than 100 seconds, which means that some of these traps are very deep.

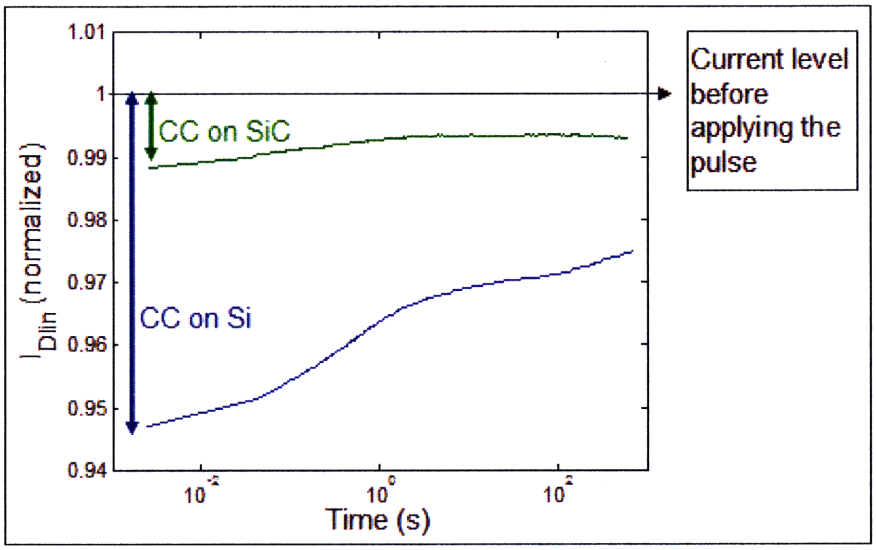


Figure 3-1: Comparison of current transients in GaN-on-Si and GaN-on-SiC HEMTs after the application of one second pulse of value -10 V at the gate when V_{DS} = 0 V.

3.3 Degradation in High Power Step Stress

GaN HEMTs are usually deployed in high power high frequency applications such as base stations and radar applications. Hence, the reliability of GaN HEMTs should account for prolonged or accelerated high power conditions. In Figure 1-2, we already referred to constant high-power stress experiments at different temperatures. In that figure, it is clear that for low channel temperatures, current degradation is minor and stress should be sustained for very long times to result in observable amount of degradation. This hinders understanding of degradation mechanisms in these devices by discarding the possibility to run experiments under different conditions in reasonable test times.

We have adapted a power sweep method where we stress devices starting from low values of power to higher values by stepping either the current or the voltage. This fast sweep of power yields not only more information than a constant stress test but also important hints about which of stressing current or voltage is the more dominant agent for degrading the device. The problem with this method is that as the power consumption increases during the stress, the finite thermal resistance from the channel to the base plate will cause an increase in channel temperature.

We have isolated the effect of temperature on device degradation to some extent in stepped power tests by designing two different schemes where the power dissipation in both cases is approximately the same at each step. In the first experiment, V_{DS} is kept constant at 22 V and I_D is stepped from 50 mA/mm to 600 mA/mm by a 50 mA/mm increase every 10 minutes. In the second experiment, I_D is kept constant at 180 mA/mm and V_{DS} is stepped from 6 V to 72 V by a 6 V increase every 10 minutes. These are illustrated in Figures 3-2 and 3-3 respectively. The power dissipation measured at each step of these experiments is shown in Figure 3-4. Each experiment consists of twelve equally long power stress periods and the difference between the power curves from both experiments is designed to be minimal to ensure that the two devices have the same temperature history at a point in time. This will enable us to attribute any differences in the degradation patterns to the bias conditions, not temperature change.

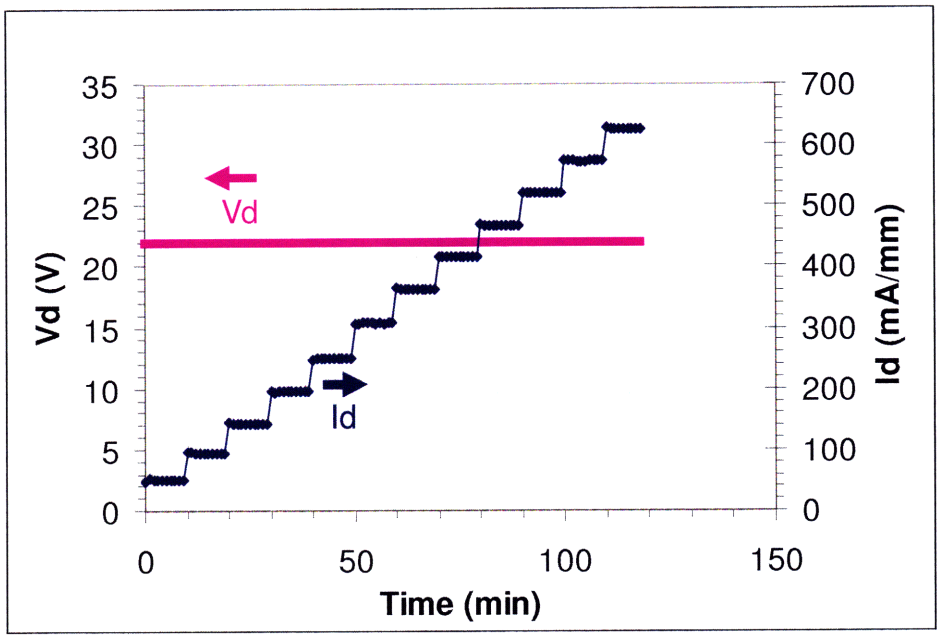


Figure 3-2: Stress bias conditions for the first type of experiment where the current is stepped. Voltage is kept constant at 22 V.

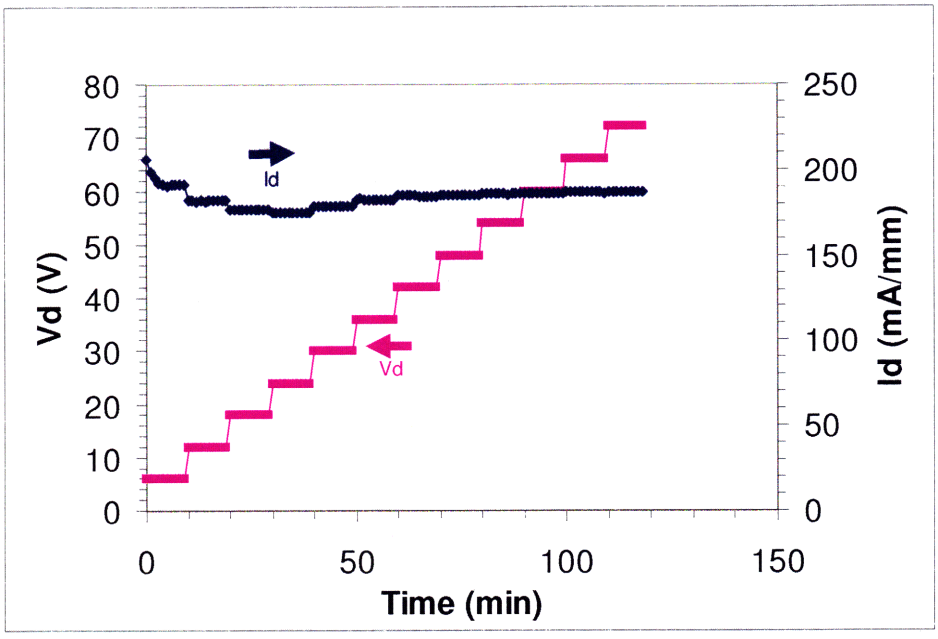


Figure 3-3: Stress bias conditions for the second type of experiment where the voltage is stepped. Current is maintained to be constant at 180 mA/mm to the best extent by adjusting the gate voltage.

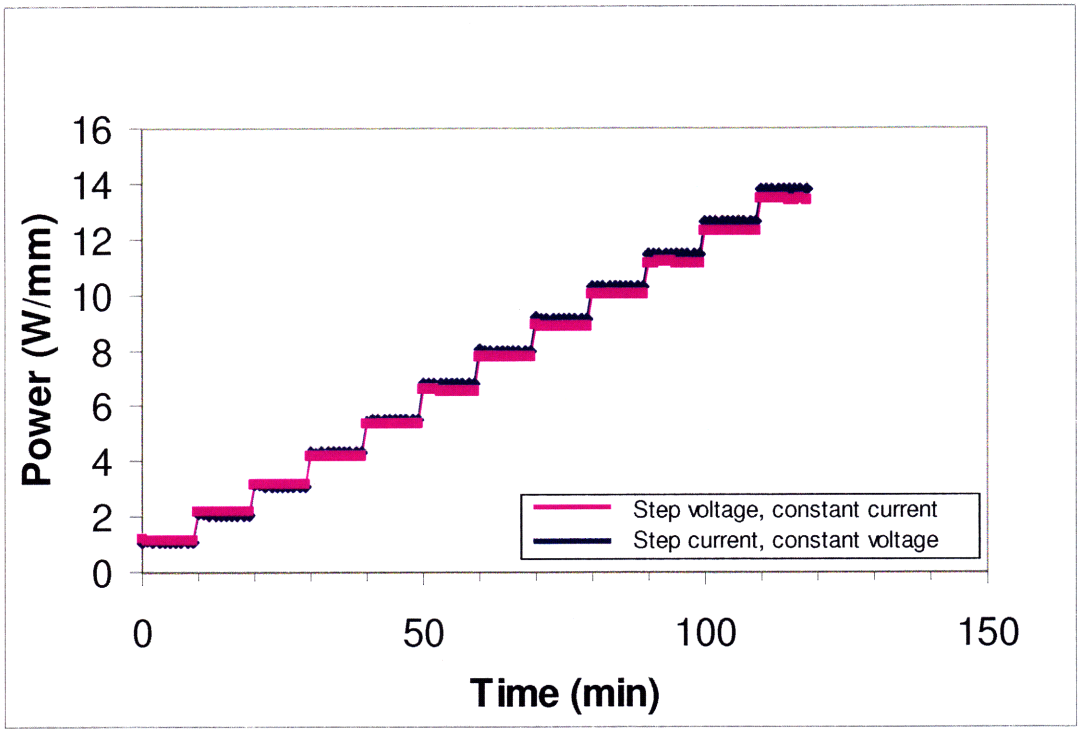


Figure 3-4: Power dissipation in two different step stress tests of Figs. 3-2 and 3-3. The duration of each step is the same and the difference between two curves is maintained to be as low as possible to ensure that two devices experienced the same temperature history up to any given time.

The devices parameters showed a significantly different degradation behavior in the two experiments. Figure 3-5 shows the change in normalized I_{DMAX} in the two experiments. There are two striking features in this figure. First, stepping the stress voltage is clearly reflected on the measurement of I_{DMAX} by the staircase shape of the curve whereas the degradation is much smoother for the case of step current. Second and probably more important, the degradation in I_{DMAX} is twice as big in the case where voltage is stepped. The maximum drain current decreased to 90% of its original value during the step current test whereas it decreased to 80% in the step voltage test.

The changes in R_D and R_S over time in these experiments are shown in Figure 3-6. Although source resistances did not degrade much in either of the experiments, drain resistance increase is 28% in the case of step voltage whereas the increase is just 10% for the case of step current.

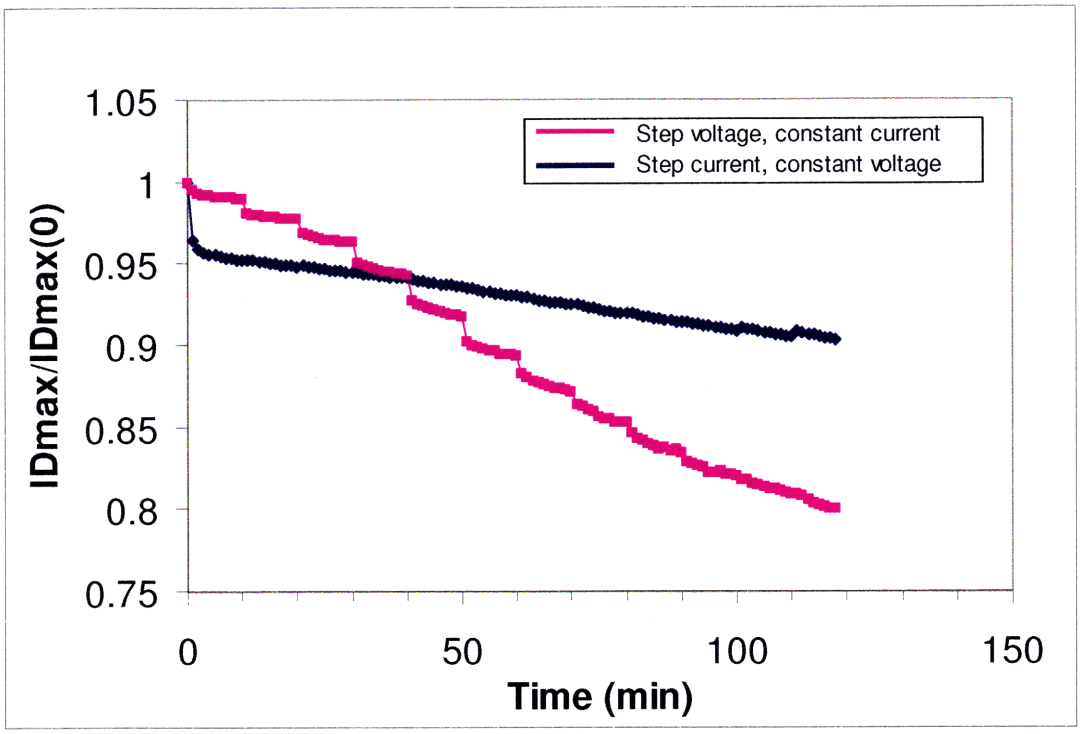


Figure 3-5: in I_{DMAX} in step current and step voltage experiments of Figures 3-2 and 3-3.

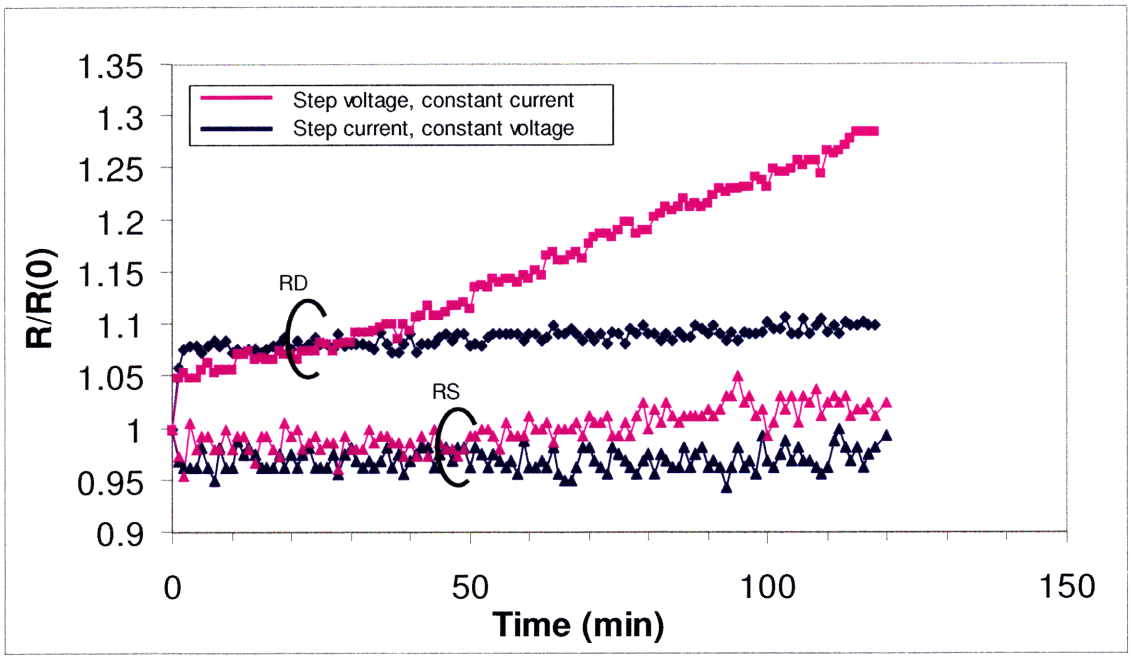


Figure 3-6: Increase in R_D and R_S in step current and step voltage experiments of Figs. 3-2 and 3-3.

Higher degradation observed in I_{DMAX} and R_D for the case where the stress voltage is higher is in agreement with the degradation observed in threshold voltage (V_T) and subthreshold swing (SS). This is illustrated in Figures 3-7 and 3-8, respectively, where degradation in both is larger for the step voltage experiment. Since all the figures of merit usually degrade with stress and this is more emphasized with higher voltage, it can be concluded that high voltage is more important in degrading the devices than high current. This observation leads to the fact that experiments that only investigate the effect of voltage will yield valuable information and performing low power stress tests with negligible currents will not only clarify the results but also remove the effect of temperature completely.

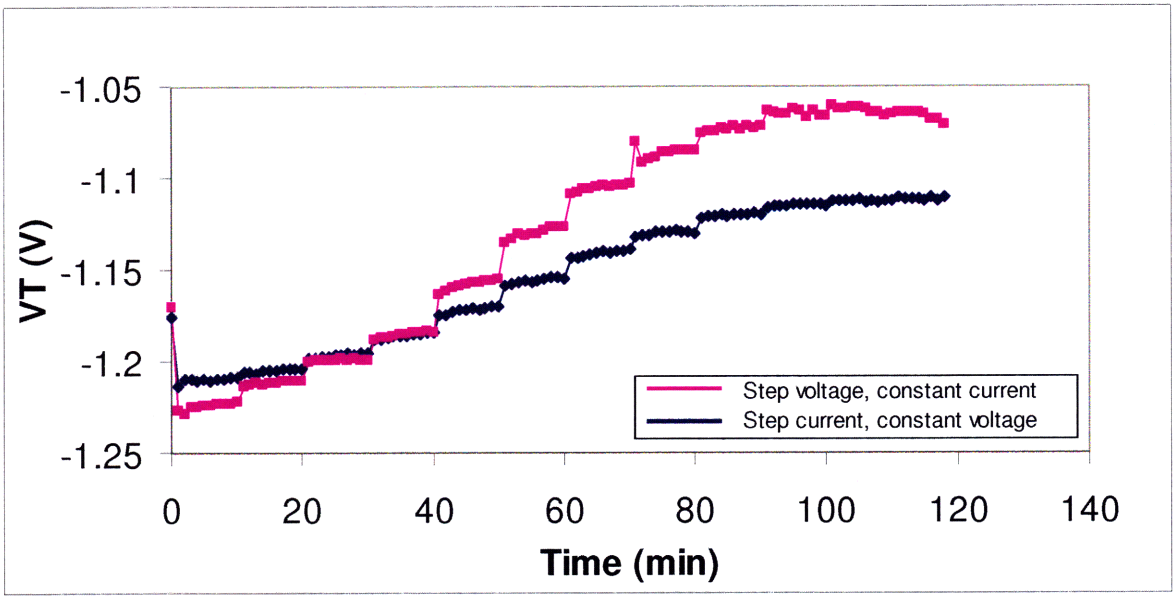


Figure 3-7: Increase in V_T in step current and step voltage experiments of Figs. 3-2 and 3-3.

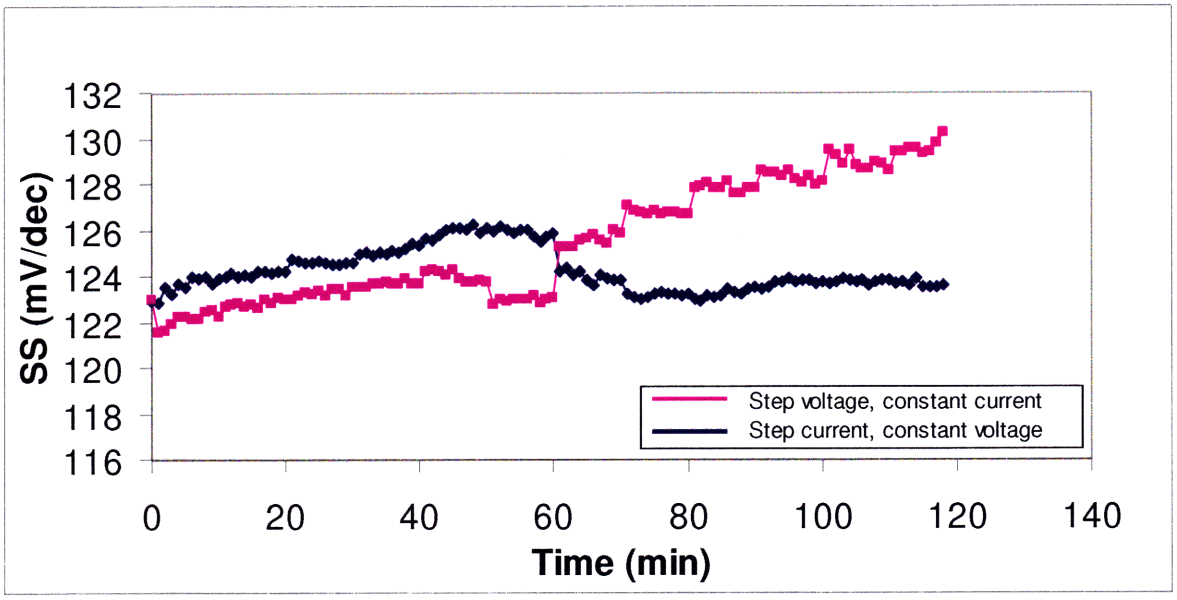


Figure 3-8: Increase in SS in step current and step voltage experiments of Figs. 3-2 and 3-3.

An interesting observation is illustrated in Figure 3-9. The gate leakage current (I_{GOFF}) was $4.6x10^{-3}$ mA/mm when the device was fresh and it decreases as the voltage is increased in the step voltage experiment. A relatively constant gate leakage is observed in the step current experiment. This may give the wrong impression that gate leakage current does not degrade as the cases where it degrades by several orders of magnitude will be shown later. We attribute the effect observed here to trapping in the AlGaN barrier as described in [31]. The trapped electrons occupy the states between gate and channel which constitute the path for I_{GOFF}; hence the leakage decreases as the drain voltage increases up to a certain point. For the case of stressing with step current, weaker trapping behavior is observed where finally the increased temperature may have enhanced detrapping and I_{GOFF} starts increasing again.

If the change in I_{GOFF} can be explained by trapping and not a physical degradation mechanism, it is important to ask the same question for the other figures of merit. Are the observed changes simply consequences of trapping in different layers of the device rather than a permanent degradation? We will have an answer to this in the following sections, but the fact that high voltage is more effective in changing the device characteristics than high current remains

unchanged. The highest drain current I_{DMAX} (measured at V_D=5 V) is usually on the order of 800 mA/mm and in this specific experiment introduced here, the stress current has reached 600 mA/mm without introducing much degradation. It is almost impossible to increase the current beyond this value in our case where V_D=22 V due to self heating of the device. In short, maximum achievable current under these conditions has not introduced as much degradation to the device as the high voltage has introduced.

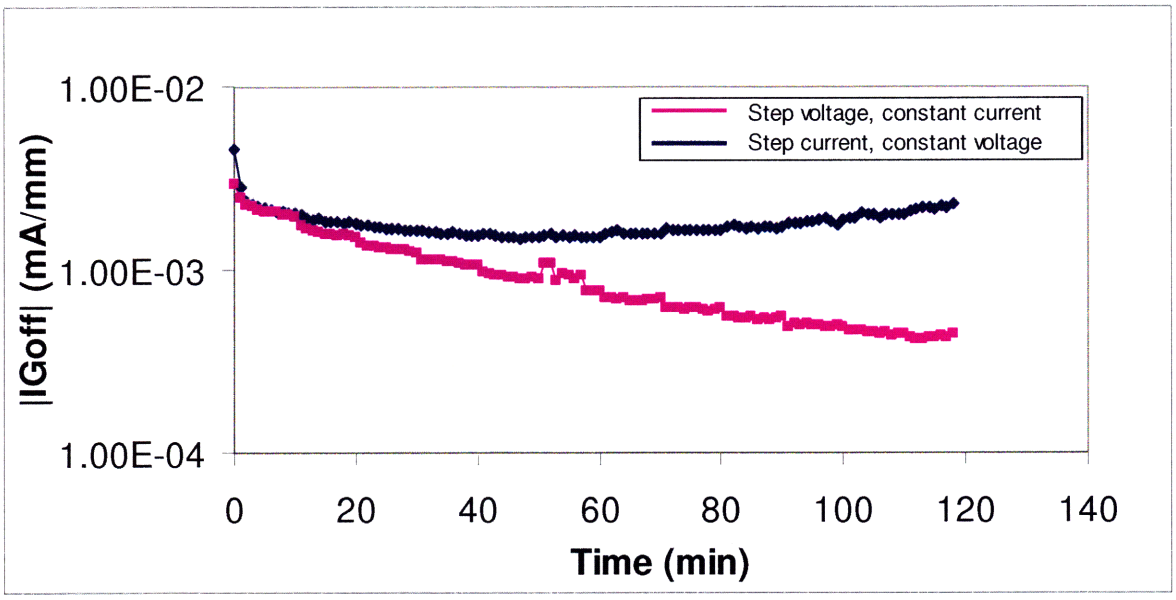


Figure 3-9: Change in I_{GOFF} in step current and step voltage experiments of Figs. 3-2 and 3-3.

3.4 Stress-recovery tests

As a result of the discussion in the previous section, we performed a stress-recovery type experiment on our devices to see if the changes observed in the device parameters can be explained by just trapping. If this is the case, device parameters should recover during the periods where stress is removed. Figure 3-10 shows a stress-recovery experiment where the device experienced OFF-state stress conditions during the stress periods thereby eliminating the effect of current and the resulting temperature increase. The gate voltage was fixed at V_G = -7 V and the drain voltage was fixed at V_{DS} = 50 V. The experiment consisted of three cycles and in each cycle; a two-hour stress period was followed by a two-hour recovery period.

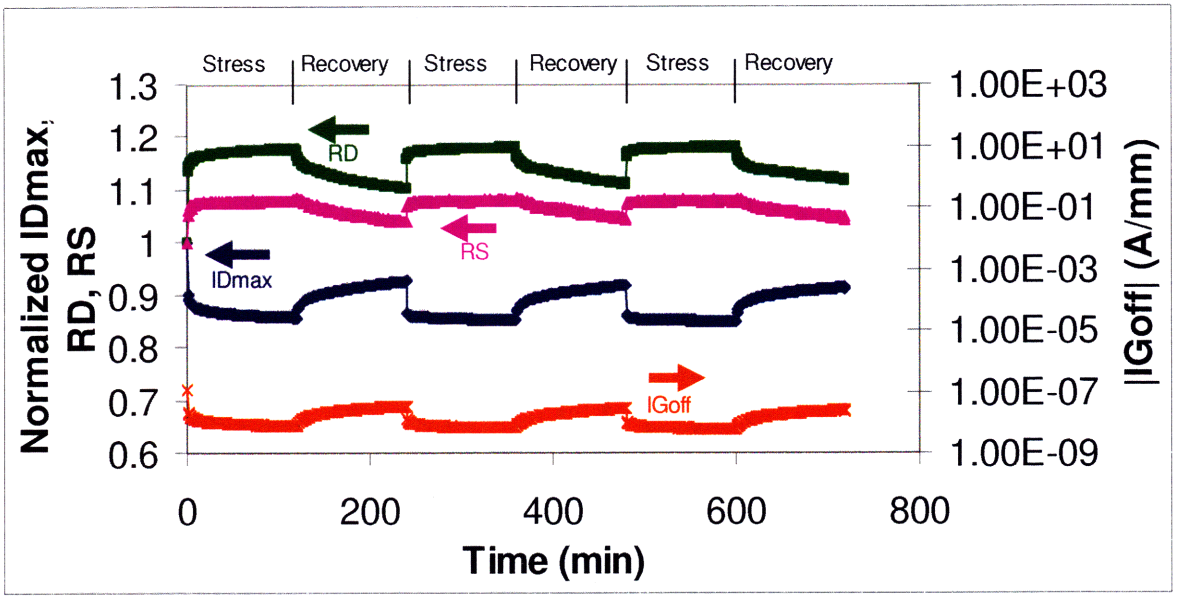


Figure 3-10: A stress recovery experiment with OFF state stress conditions. During stress, V_G=-7 V and V_{DS} = 50 V. During recovery, all the voltages were set to 0 V.

Although the stress is constant in each cycle, the parameters shown in Figure 3-10 keep degrading in that stress period. The word "degrading" should be used in a careful manner here because once the recovery period starts, all the parameters start recovering toward their unstressed values. I_{DMAX} drops to 85% of its original value at the end of the first stress period. However the fact that it reaches to 93% at the end of the first recovery period proves that this decrease was not all permanent, rather it was recoverable to some extent. Two hours of recovery is obviously not enough to recover fully and the shapes of curves suggest that more detrapping was going on when the stress was set again. The slow recovery behavior indicates that very deep trap levels are at play unlike the GaN-on-SiC devices, where such detrapping is usually faster [21]. In addition to the conclusion that there are more traps in GaN-on-Si devices from Section 3.2, slower recovery points to the fact that some of these traps are located much deeper in the bandgap.

The behavior of I_{GOFF} is consistent with the discussion at the end of the previous section, where trapping between gate and channel was considered to be the reason behind gate leakage current decrease during stress. As the electrons are allowed to detrap during the recovery period, I_{GOFF} also increases and evolves towards its original value before the onset of stress. The stress voltage

is not high enough to introduce permanent increase in I_{GOFF} as such cases will be shown later. R_D and I_{DMAX} are degrading during the stress and recovering relatively slowly. Additionally, R_S is showing a similar behavior though in a much less prominent fashion. This was not the case in the experiments described in Section 3.3. In those experiments, gate voltage was held high enough (from -1.0 V to +1.7 V) to allow appreciable current to flow through the channel. This is an interesting point to note as application of V_{DS} = 50 V has affected the source side of the device more than V_{DS} = 72 V because the gate voltage was slightly more negative in the former case. This observation suggests that more attention should be paid to the gate voltage.

Another stress-recovery test with V_{DS} = 0 V type stress was performed to investigate the observation made for the effect of gate voltage. In this case, the gate voltage was kept constant at V_G = -40 V during the stress phase. The test consisted of 3 cycles and each cycle had a three hour stress period followed by a three hour recovery period. It is interesting to see the immediate effect of gate voltage in this experiment on R_S, which has stayed unchanged during the high power stress and relatively unchanged during the OFF state stress described above. It follows a very similar pattern to resistance of the drain side of the device, which has always been subject to high voltage either applied to the drain or the gate. Although the current through the channel is the same on both sides of the gate, the source resistance has been relatively unaffected if the voltage across gate and source junctions is not high. This observation proves once again the fact that stress field is more effective in changing the device characteristics than stress current.

Although I_{DMAX}, R_D and R_S behave more or less in an expected way in Figure 3-11 when compared to Figure 3-10, there is a significant discrepancy in I_{GOFF}. It follows the behavior of I_{DMAX} in Figure 3-10 and increases during recovery where electrons are detrapped. On the other hand, it behaves in a less predictable manner in Figure 3-11. This requires investigating the effect of gate voltage more carefully through a step-stress test and this will be done in Section 3.5.

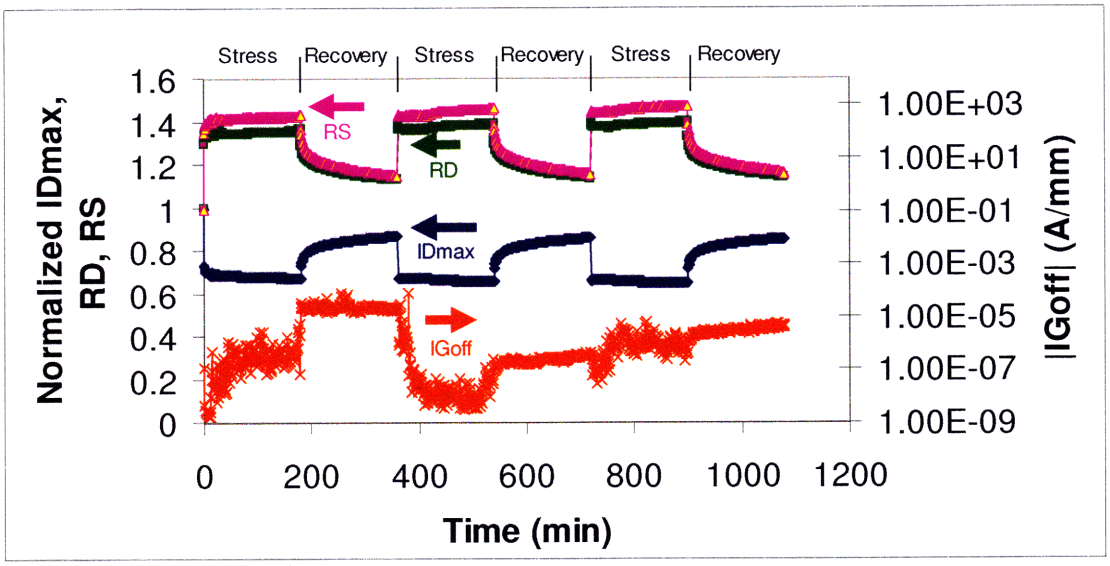


Figure 3-11: A stress recovery experiment with V_{DS} = 0 V stress conditions. During stress, V_G = -40 V and V_{DS} = 0 V. During recovery, all the voltages were set to 0 V.

3.5 V_{DS} = 0 V Step-Stress Tests

We have already investigated the effect of V_{DS} = 0 V type stress on GaN-on-Si devices in the previous section, however stepping the gate voltage could reveal some important information. The unpredictable behavior of I_{GOFF} when a high voltage is applied at the gate requires a careful study of this stress scheme. We designed an experiment where the gate voltage was stepped from -5V to -60V by 1V every 10 seconds. Meanwhile, the drain voltage was kept at 0 V so that both sides of the gate would experience a high electric field.

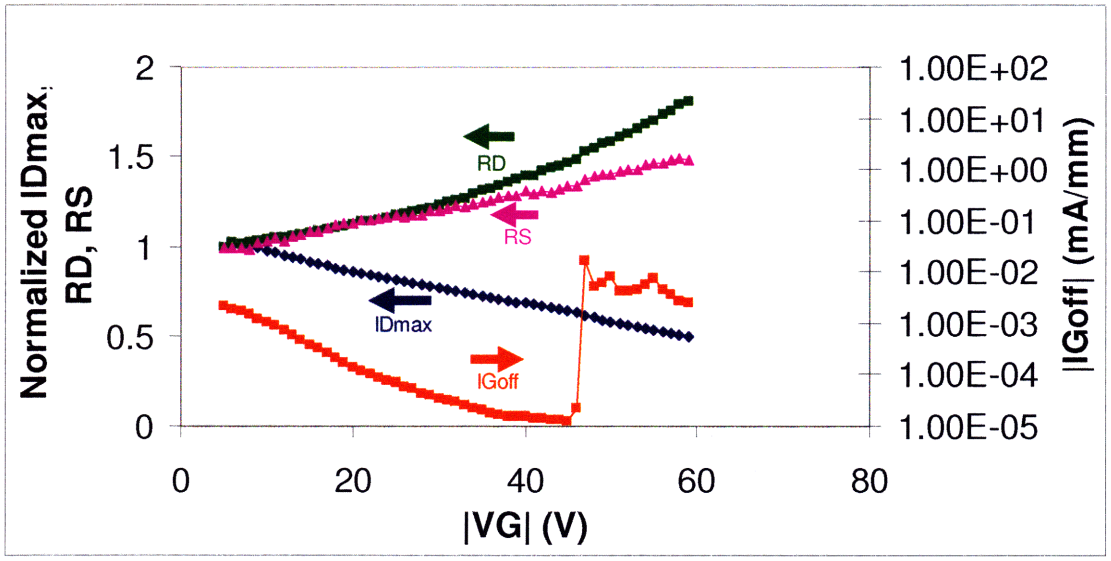


Figure 3-12: V_{DS}=0V step stress experiment. V_G is stepped from -5V to -60V by 1V every 10 seconds.

The results are shown in Fig. 3-12. There are very important observations in this figure. First, we observe almost two orders of magnitude decrease in gate leakage current down to V_G = -45V similar to those observed in Figures 3-9 and 3-10 during stress. However, increasing the stress voltage beyond this value results in a sudden increase in I_{GOFF}. Other figures of merit degrade in an expected way but they do not exhibit an obvious acceleration in degradation at this critical voltage. Hence we refer to the voltage where I_{GOFF} increases by several orders of magnitude as a critical voltage for gate leakage current degradation, V_{CRIT}. This observation is very similar to the discussion in [21], where such increase in current degradation was attributed to the inverse piezoelectric effect in AlGaN/GaN system. The triggering effect of this mechanism is the vertical fields due to the voltage applied at the gate. Since the field is more or less symmetrical on both sides of the gate, the impact of stress is comparable on the drain and the source side of the device. It is important to note that none of the effects can be attributed to current or temperature since the channel is OFF at all voltages applied.

The degradation mechanism through the converse piezoelectric effect implies degradation in the OFF state step stress as well. This is indeed the case in the set of GaN-on-SiC devices that were used in [21]. However, it was concluded that V_{DS} = 0 V step stress is a more severe stress condition than OFF-state step stress because the mechanical strain induced on the source side adds to that induced on the drain side. Critical degradation was still observed in I_{GOFF}, however,

this happened at a relatively higher voltage than V_{DS} = 0 V step stress. We have performed similar OFF-state step stress experiments on GaN-on-Si devices. Figure 3-13 shows the parameters measured during this test. Stress current was held at 10mA/mm and V_{DS} was stepped from 5 V to 60 V by 5 V steps every one hour. For this specific device and stress condition, no critical I_{GOFF} degradation was observed. Moreover, the degradation in I_{DMAX} and R_D is less compared to the V_{DS} = 0 V test of Figure 3-12 and no degradation was observed for R_S. We will see in Section 3.8 that different devices will show critical I_{GOFF} degradation in the OFF state step-stress and the repeatability of results under the same conditions for different devices will be discussed.

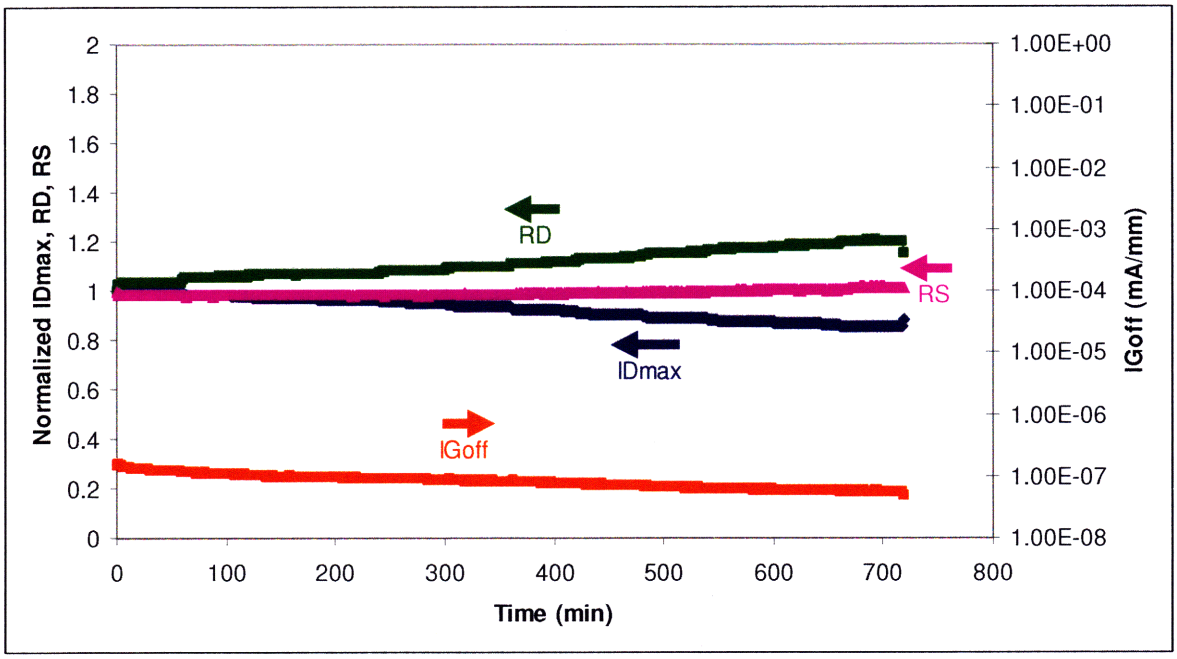


Figure 3-13: OFF state step stress experiment. V_{DS} is stepped from 5 V to 60 V by 5 V every one hour.

A distinction should be made at this point. We previously made the warning that the word "degradation" should be used with care. The figures of merit may seem to be degrading but in the previous section, we realized that this degradation is recoverable to some extent. The behavior of all the displayed figures of merit in Figure 3-12 are similar to that was attributed to the effect of trapping, except the sudden increase observed in I_{GOFF}. Moreover, this increase is found to be non-recoverable. This raises the question that what portion of the degradation is recoverable and what is a good way to assess the real degradation in the device. This is the

question that we are going to find an answer in Section 3.7, but we should first introduce the UV illumination as an effective means of detrapping most of the charged traps in Section 3.6.

3.6 Enhanced detrapping under UV light

GaN has a band gap of 3.4 eV. This corresponds to energy of a photon in the ultraviolet range which has a wavelength of 365 nm. AlGaN has a wider band gap that increases with AlN composition. This corresponds to a wavelength deeper in the ultraviolet spectrum. Since we are concerned about the increased number of traps in the AlGaN/GaN heterostructure built on Si substrates, it is helpful to investigate the behavior of such traps under UV light.

The first step is to observe the impact of UV on the main device figures of merit used in this study. Figure 3-14 shows the effect of UV light on I_{DMAX}, R_D, R_S and I_{GOFF} in a simple characterization experiment where these parameters are continuously characterized for one hour without applying any kind of stress. The wavelength of the light coincides with the band gap of GaN and is 365 nm. In the first 20 minutes, the device was characterized in the dark. We observe a slight degradation in the figures of merit as even the characterization suite itself can cause some trapping. Turning on the UV light causes not only a recovery from this trapping but also an overshoot probably due to emptying the traps that were originally occupied in the device before starting the characterization. The UV light was turned off in the last 20 minutes. The figures of merit approach their values before the light was turned on in this period due to retrapping. It is obvious from this experiment that UV light alone does not change the I_{DMAX}, R_D and R_S by more than 10% in a fresh device. However, I_{GOFF} has increased by about 40% because the detrapping has more significant consequences on this figure of merit as the leakage current is caused by electrons using unoccupied trap levels as a path from the gate to the channel. Any further change caused by UV during stress or recovery experiments can be attributed to enhanced detrapping under UV.

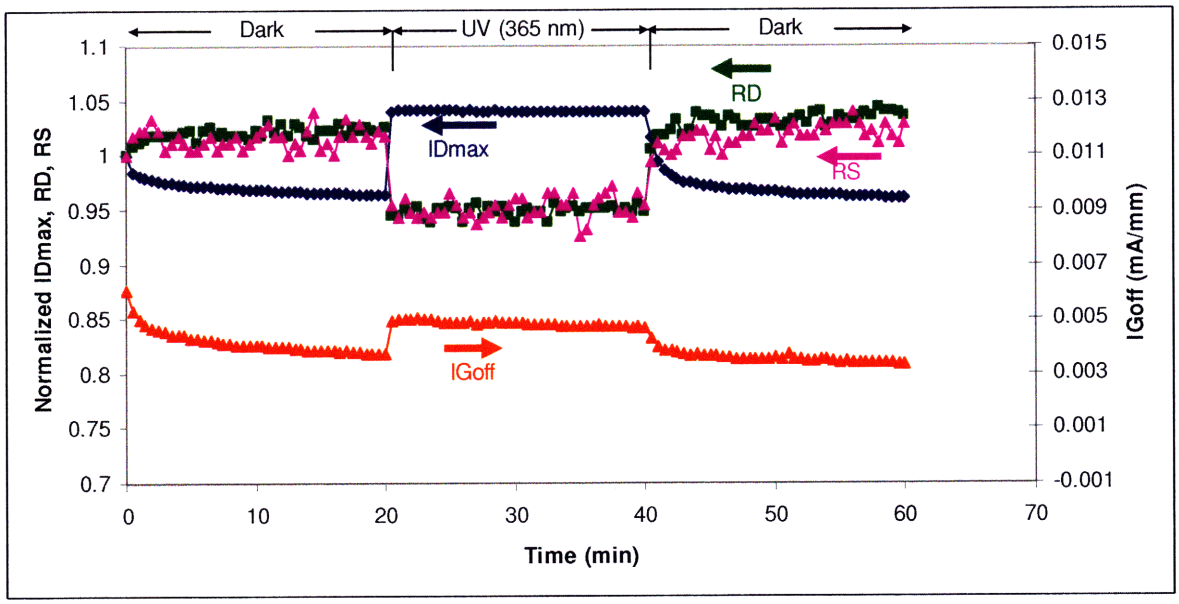


Figure 3-14: Characterization of the device in the dark and under UV light (365 nm). No stress is applied to the device during this experiment.

Figure 3-15 shows the change in the parameters of a GaN-on-Si device in another experiment that focuses on the effect of UV light. There are 5 phases in this experiment. Each phase lasts 15 minutes and the characterization suite is run every 30 seconds. In the first phase, no stress is applied on the fresh device and the values of I_{DMAX}, R_D, R_S and I_{GOFF} are recorded over a period of time. The data suggests that no significant degradation is introduced by the characterization suite for this specific device unlike the case in Figure 3-14. In the second phase, V_{DS} = 0 V type constant stress is applied to the device where the gate voltage was held at -30 V. This voltage is below the critical voltage for I_{GOFF} degradation and is expected to introduce trapping but not gate current degradation. At the end of this phase, R_D and R_S both degrade by 34% and I_{DMAX} by 30%. I_{GOFF} behaves in an expected way and decreases due to trapping. However, as the stress is removed during the recovery period in Phase 3, all the figures of merit exhibit a transient behavior trying to recover to their original values. This is rather a slow recovery period and the parameters seem they have already saturated before reaching their original values. This is indeed the case and we have observed that this recovery period takes a few days if not weeks unless there is external interference to enhance it. The slow recovery could be explained by detrapping from deep traps as discussed before.

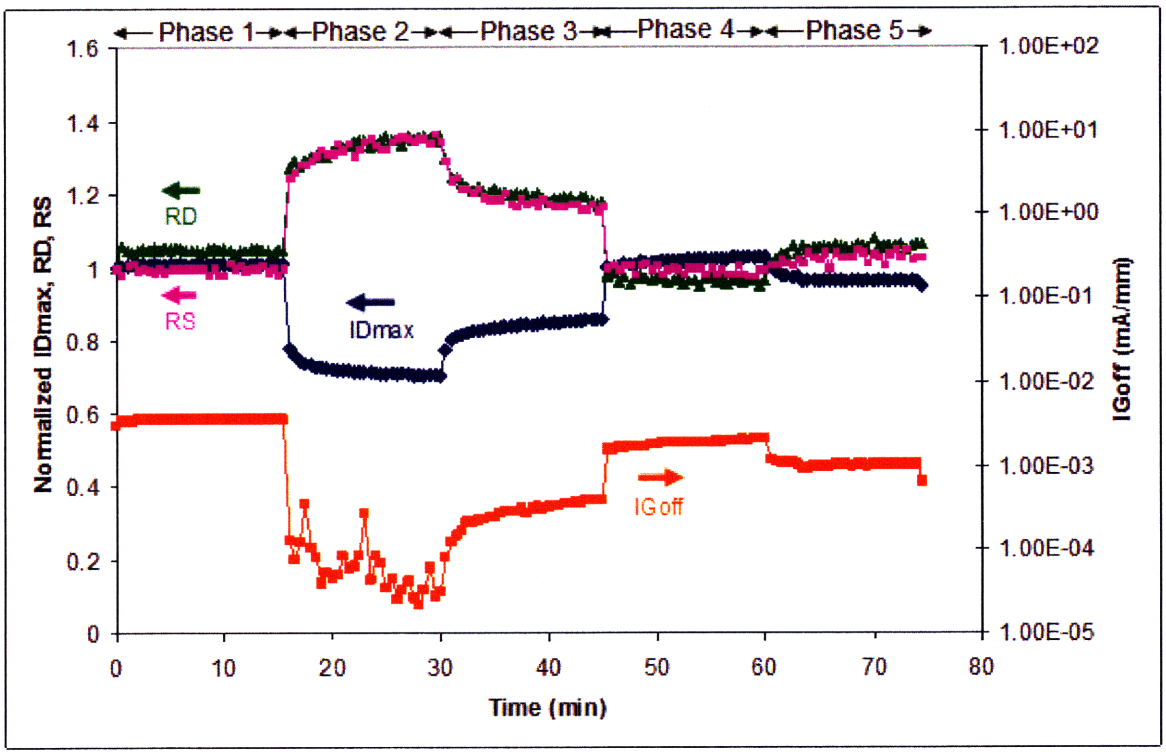


Figure 3-15: The behavior of parameters in a five-phase experiment. Phase 1: No stress in the dark. Phase 2: V_{DS}=0 V constant stress with V_G=-30 V. Phase 3: Recovery in the dark. Phase 4: Enhanced recovery under UV light (365 nm). Phase 5: Recovery in the dark.

Phase 4 represents the interval where we introduced UV illumination on the recovering device. The parameters recovered almost instantaneously under UV light as expected. However, some of the figures of merit overshot their original values similar to the experiment shown in Figure 3-14. In Phase 5, the UV light was turned off; hence the parameters changed reflecting slightly more trapping, as shown above.

The recovery under UV light is interesting. At the end of Phase 3, I_{DMAX} could only recover to 86% of its original value. However, it reached 96% of its original value due to the enhanced trapping under UV light. UV has been rather successful in detrapping electrons from the relatively deep traps that exist in this device.

With this understanding, it is interesting to compare step stress experiments in the dark and under UV illumination. Characterization is always done a few seconds after terminating the stress for that cycle due to technical constraints; hence the parameters are measured after some detrapping

during this short period. Figure 3-16 compares I_{DMAX} values recorded from two GaN-on-Si devices that are on the same reticle and neighbors to each other. The reason that they are taken from the same reticle and next to each other is to eliminate as much as possible the effects of process variations. Both devices were stressed in a V_{DS} = 0 V scheme where V_{GS} is stepped down to -70 V. In this figure, I_{DMAX} starts from a slightly larger value for the sample measured under UV illumination and remains higher throughout the stress. The first measurement point was taken under UV as well, which also is boosted because of emptying of the traps that were occupied by electrons in the fresh device. The fact that there is a downward slope observed for the I_{DMAX} of the illuminated sample means that trapping is still effective even under UV light. The changes in R_D and R_S in these experiments are shown in Figure 3-17. They are lower for the case of UV illumination as expected.

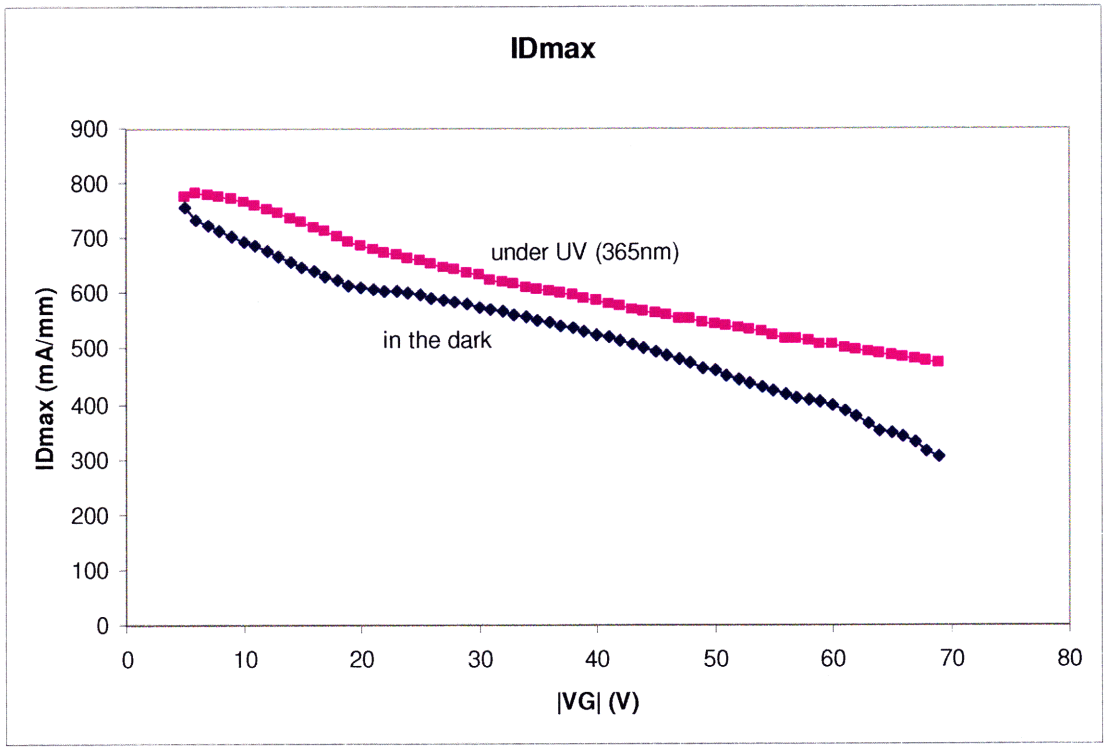


Figure 3-16: Comparison of I_{DMAX} in neighboring devices where one of them is stressed under UV and the other remained in the dark during stress. They are both stressed in a V_{DS}=0V step stress experiment where V_G was stepped from -5V to -70V.

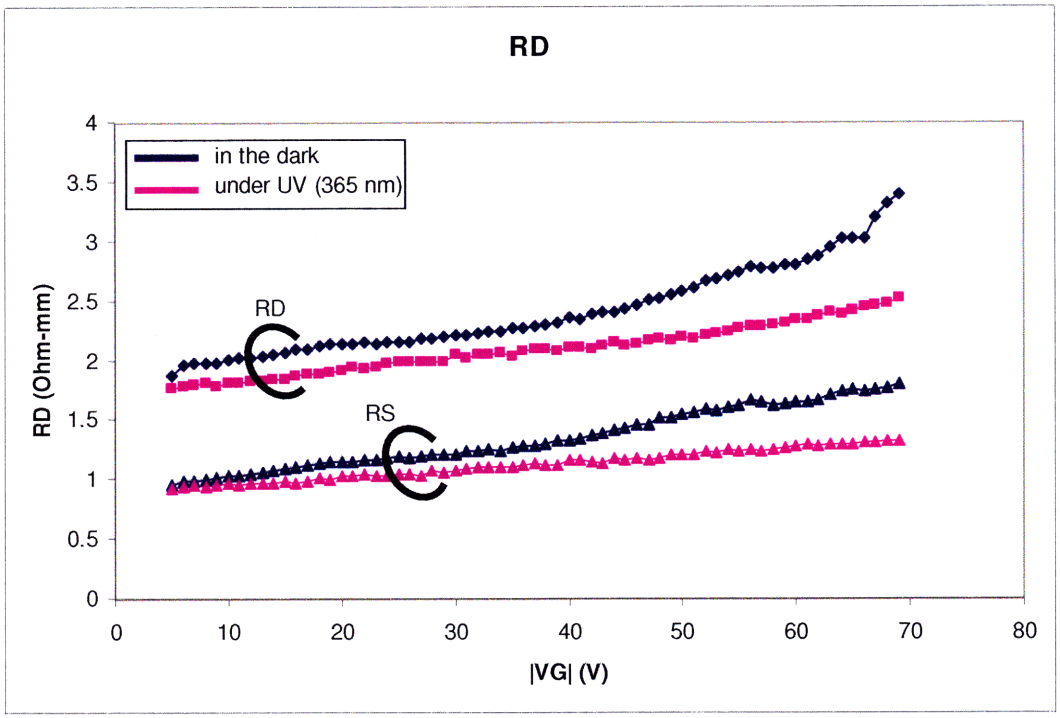


Figure 3-17: Comparison of RD in neighboring devices where one of them is illuminated under UV and the other remained in the dark. This is the same experiment as in Figure 3-16.

A similar observation is made for the threshold voltage (V_T) and subthreshold swing (SS). These are illustrated in Figure 3-18 and 3-19, respectively. Probably the most striking difference between stressing in the dark and under UV light is faced by the threshold voltage. V_T stays almost constant at a much lower value under UV illumination whereas it starts at a higher value and increases up to high stress voltages in the dark. The flat pattern observed under UV is a clear indication that UV has been effective to empty the traps under the gate that are populated by the increasing stress at least by the time the measurement was taken. The same discussion is valid for the subthreshold swing and it does not increase significantly under UV illumination.

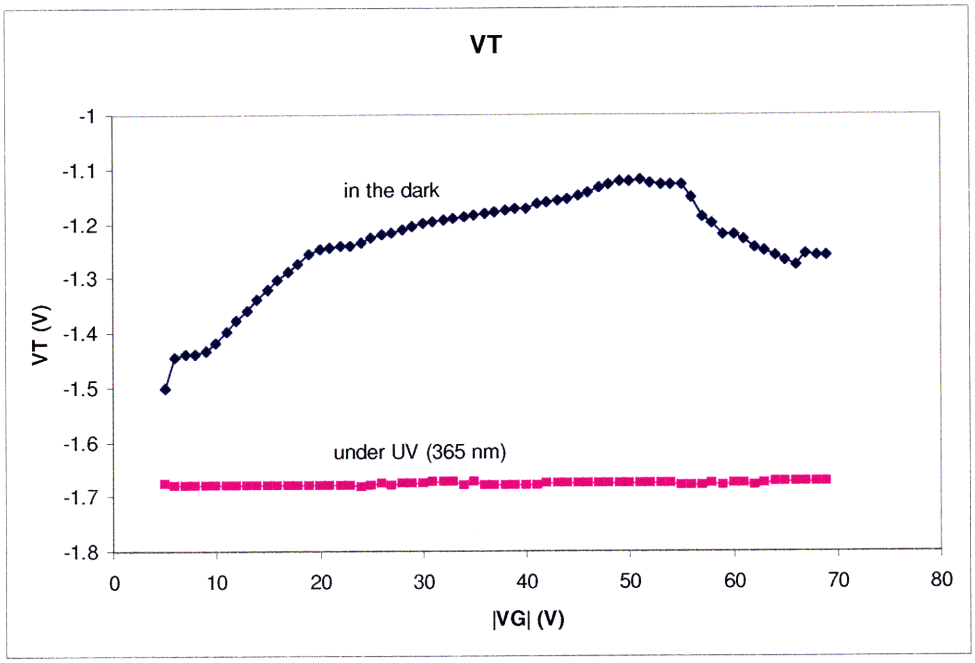


Figure 3-18: Comparison of V_T in neighboring devices where one of them is illuminated under UV and the other remained in the dark. This is the same experiment as in Figure 3-16.

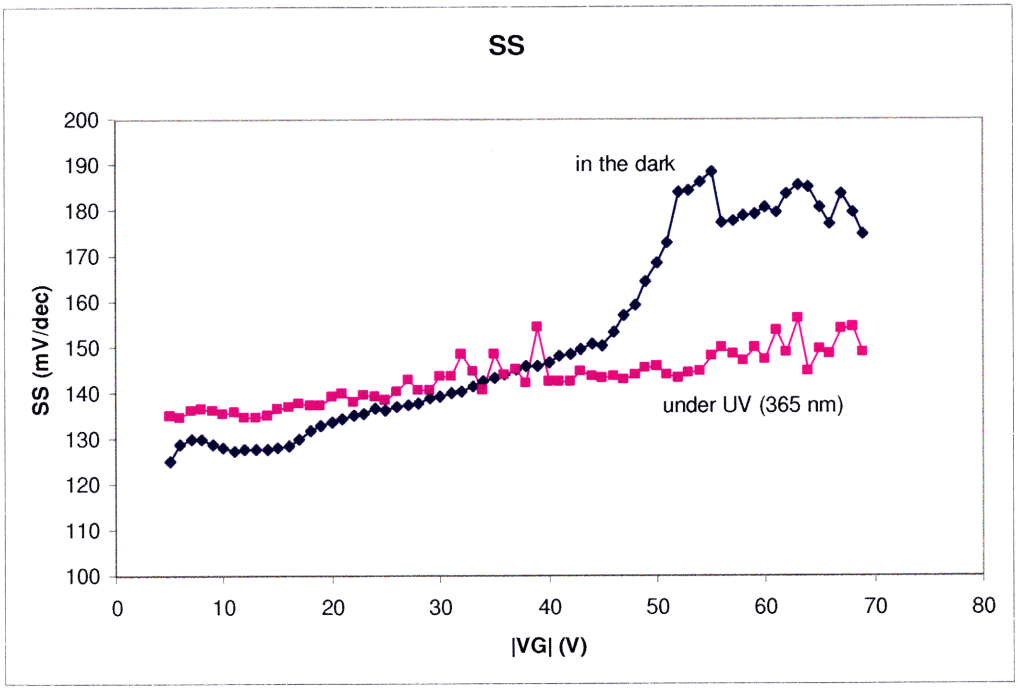


Figure 3-19: Comparison of SS in neighboring devices where one of them is illuminated under UV and the other remained in the dark. This is the same experiment as in Figure 3-16.

Figure 3-20 shows the comparison of I_{GOFF} for both the sample that is illuminated with UV and the one that remained in the dark. At the first measurement point, we observed a higher gate leakage due to less trapping. The most dramatic impact of UV is seen in the lower critical voltage for I_{GOFF} degradation. It is important to establish whether this difference arises from the devices themselves. This will be discussed in Section 3.8.

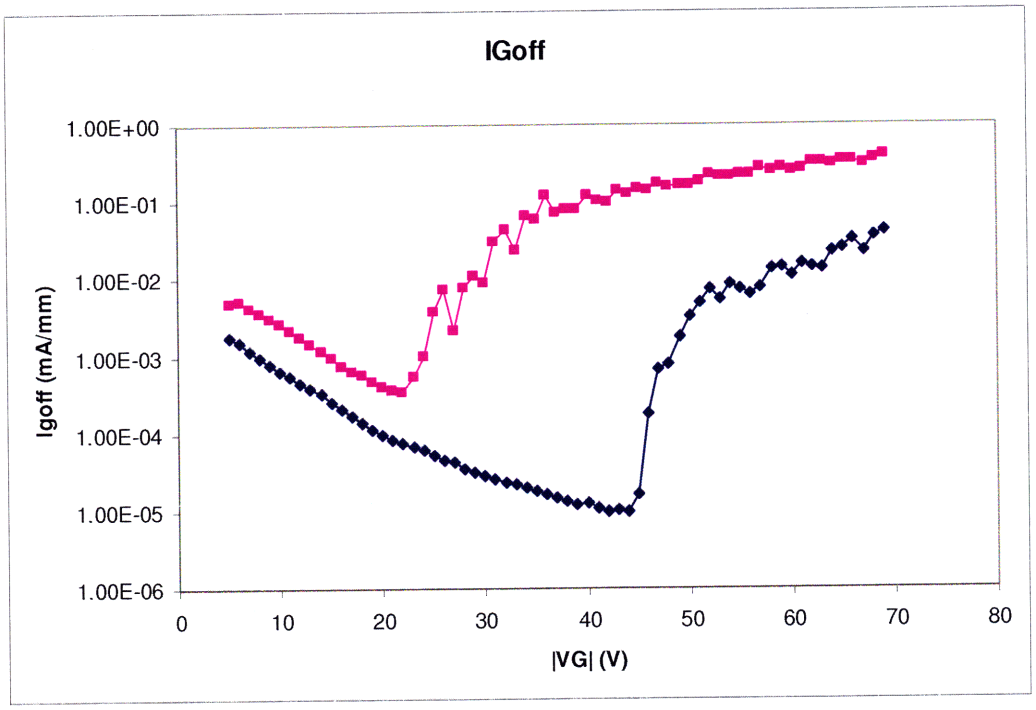


Figure 3-20: Comparison of I_{GOFF} in neighboring devices where one of them is illuminated under UV and the other remained in the dark. This is the same experiment as in Figure 3-16.

The data presented in this section indicates that UV light has been successful to enhance detrapping during characterization where the electrical stress is interrupted. This means that UV can be used as a tool to enhance detrapping and bring the traps in the device to the same charged conditions as before applying a stress much faster than just waiting in the dark. Further discussion is needed to conclude that UV light is also effective for detrapping when the stress conditions are persistent. This is done in the next chapter.

3.7 Degradation versus Trapping

In Chapter 2, we introduced current collapse and current transient measurements as a way to assess the amount of traps in fresh devices. This can also be used as a measure of increased trapping by comparing the values before and after a specific stress test. We will reserve the word "degradation" for I_{DMAX} for two cases from now on. In the first case, the device will be assumed "physically degraded" if I_{DMAX} cannot reach its original value by enhanced detrapping under UV light and waiting for long enough to detrap all the electrons from trap levels. The second indication of physical degradation is an increase in the number of traps.

An effective tool to evaluate degradation through the observation of a decrease in I_{DMAX} and the amount of trapping is an electron-injecting pulse when all the traps in the device are emptied. The value of current before the application of a pulse is referred to as the uncollapsed value of the current. The value recorded right after the pulse is referred to as the collapsed value of the current. As a result, current collapse (CC) is the difference between these two levels of current. Our definition of physical degradation above is now transformed to two simple observations: decrease in uncollapsed current value and/or an increase in current collapse because this will indicate that more traps are created and populated with electrons thereby suppressing the 2DEG to a greater extent.

In Figure 3-12, we showed a classical V_{DS} = 0 V step-stress experiment. We have observed that all the figures of merit except I_{GOFF} degraded in the same way throughout the experiment whereas I_{GOFF} decreased until V_{CRIT} = 45 V and then exhibited a sudden increase at this voltage. In the stress recovery tests of Figures 3-10 and 3-11, we observed that the FOMs can recover to some extent when the stress is removed. This was the strongest indication that at least some of the degradation observed was due to trapping. Moreover, the amount of trapping seems to increase as the stressing voltage V_G becomes more negative. This suggests a trapping mechanism in the device which depends on the stress voltage and higher stress is required to populate traps at different levels and locations. Our pulses to evaluate these traps should also be consistent with this mechanism. On the other hand, we need to make sure that our pulse diagnosis does not introduce more traps in the device as that would make the effects of actual stress indistinguishable from that of the diagnostic tool.

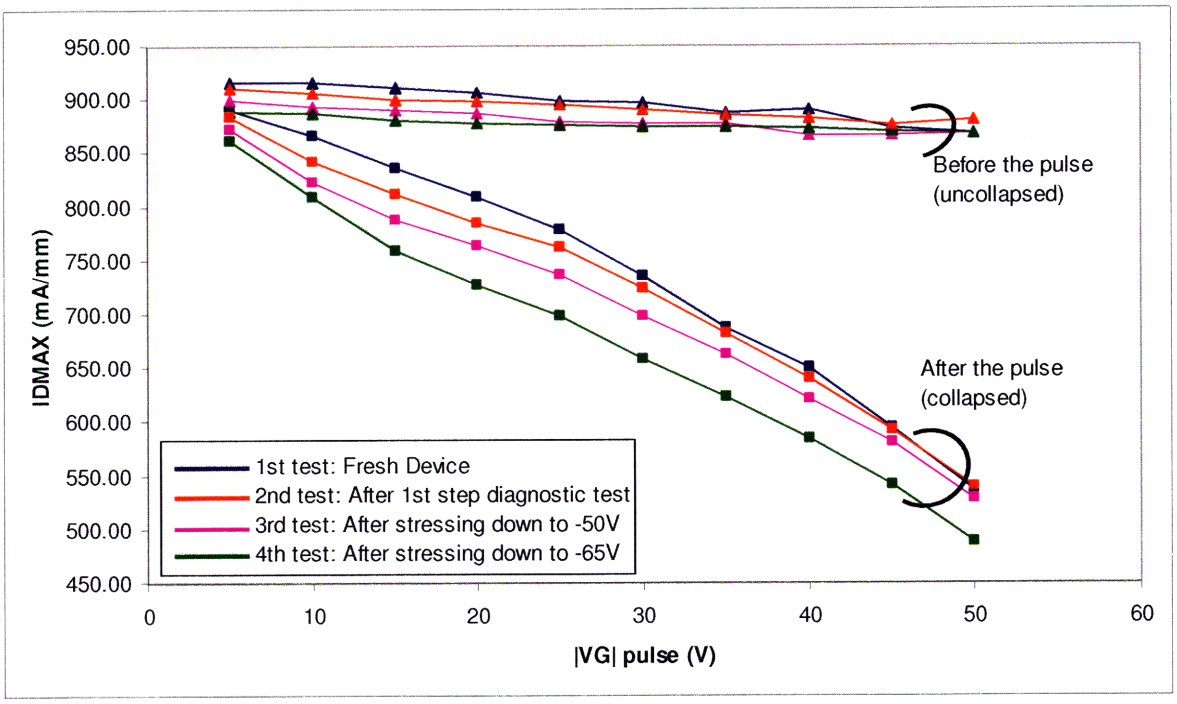


Figure 3-21: I_{DMAX} values before and after the application of pulses with stepped magnitude in 4 step diagnostic tests on the same device. The pulses are applied at the gate of the device at V_{DS} = 0 V condition and their values are stepped from -5 V to -50 V by -5 V steps.

We have adapted a step diagnostic method where the amplitude of the pulse is stepped from low values to high values to mimic the way that step-stress voltage populates traps at different levels and locations. The pulse duration has been limited to one second to ensure minimal damage by the diagnostic pulses. Figure 3-21 shows step diagnostic experiments performed on the same device. In these experiments, pulses with amplitudes stepped from -5 V to -50 V by -5 V steps are applied to the gate and the values of I_{DMAX} were measured right before the pulses and 6 ms after applying them, which is the measurement limitation of our B1500 tool. Before each pulse, the device was treated by UV light (365 nm) for 10 minutes and was allowed to rest in the dark for another 10 minutes to empty the traps as much as possible and allow the extra carriers generated to disappear before the next measurement. Even in this case, we observed a slight decrease in the uncollapsed I_{DMAX} values. This can be explained by very deep traps existing in the device. This was confirmed through the fact that although uncollapsed I_{DMAX} decreased by 49 mA/mm at the end of the first step diagnostic experiment on the fresh device, it recovered to a

level only 6 mA/mm less than the original level after 3 hours of UV treatment and overnight recovery in the dark. Hence we conclude that step diagnostic tests do not introduce physical degradation in the form of decrease in uncollapsed I_{DMAX}.

To show that the step diagnostic pulses are indeed benign, we need to show that current collapse does not increase after performing them as well. Figure 3-22 shows the current collapse values corresponding to each pulse width in the same step diagnostic experiments as in Figure 3-21. For the first two experiments where no stress was introduced yet, the current collapse is almost the same except for a small discrepancy in low voltage range. This difference for low voltages can be explained by a small increase in number of traps that are "reachable" by lower voltage pulses, however close current collapse values in general for the first two experiments suggest that step diagnostic tool remains as a potentially strong tool to study traps without introducing damage.

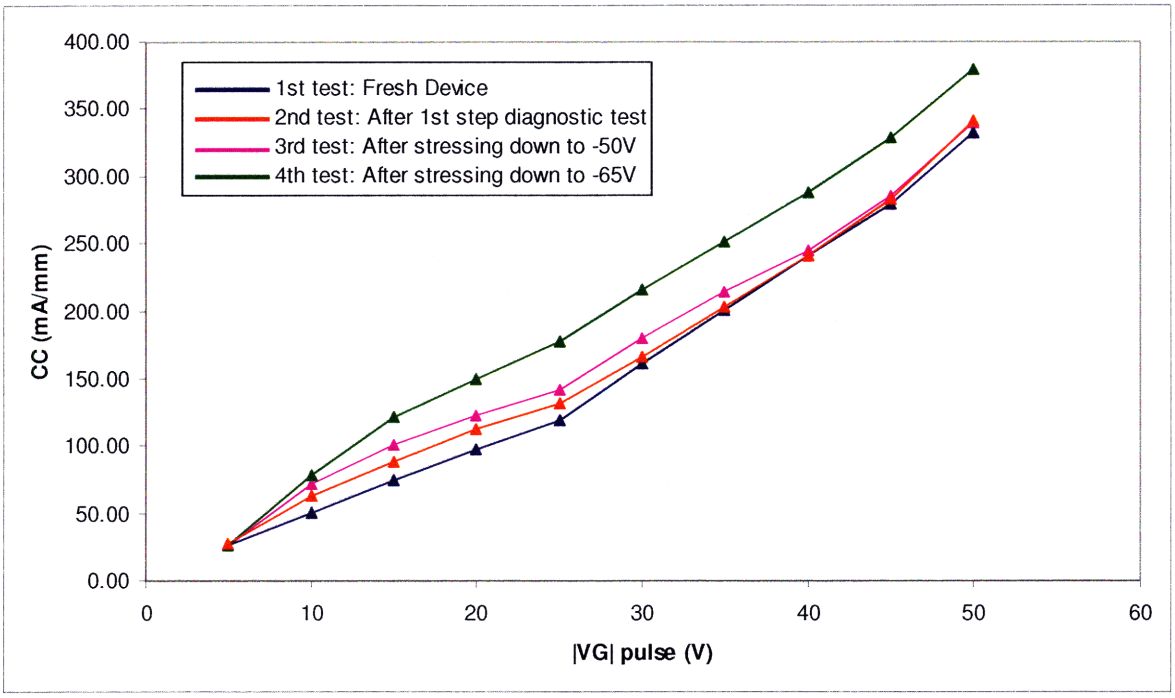


Figure 3-22: Current collapse values corresponding to pulses with different amplitudes in the same step diagnostic tests as in Figure 3-21.

We are now in a position to study how various stress conditions affect the device characteristics as we have a tool to assess degradation. Figures 3-21 and 3-22 already show the step diagnostic test results obtained after two V_{DS} = 0 V step-stress experiments. The changes in I_{DMAX} and I_{GOFF}

during these stress tests are shown in Figure 3-23. In the first experiment, V_G is stepped from -5 V to -50 V by 1 V steps, where V_{CRIT} for this device is not reached. In the second stress test, V_G was stepped down to -65 V, where I_{GOFF} went through a critical degradation at -54 V. The gate voltage was stepped every 60 seconds in the first experiment and every 90 seconds in the second experiment. I_{DMAX} values were not recorded with the characterization suite in these specific experiments where the measurement can take a few seconds and important detrapping information could be lost, instead they were measured manually 6 ms after the stress is interrupted to get a sensible comparison with the step diagnostic data. The fact that I_{GOFF} and I_{DMAX} are slightly lower in the second stress test indicates that although the sample was treated with UV light and allowed to recover for a long time, there are still deep traps which remained charged with electrons.

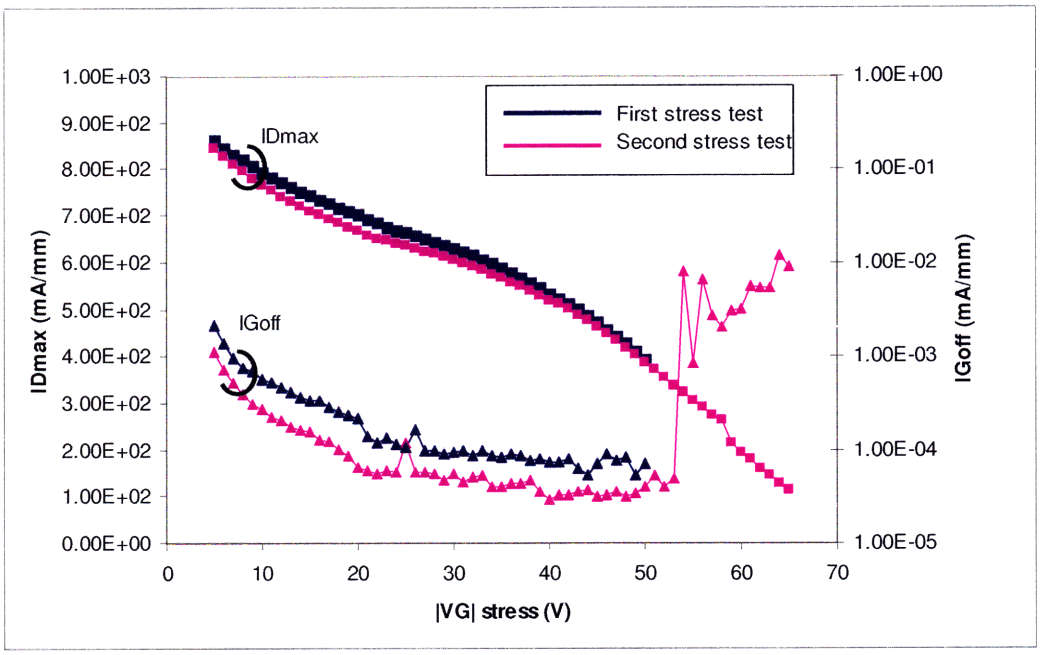


Figure 3-23: I_{DMAX} and I_{GOFF} change in the same device in two different V_{DS} = 0 V step stress experiments. In the first stress experiment, V_G was stepped from -5 V to -50 V whereas in the second experiment, it was stepped down to -65 V.

Before performing any step diagnostic or step stress experiment, the device was treated under UV light for 3 hours and allowed to recover overnight in the dark as discussed before to bring the device back to a reproducible state as mush as possible. It is seen in Figure 3-23 that I_{DMAX} collapsed to 114 mA/mm after stepping V_G down to -65V. However, Figure 3-22 shows the step

diagnostic test performed after this stress test, where uncollapsed I_{DMAX} value recovered back to 889 mA/mm after UV treatment. This is very close to the value in the fresh device. We already concluded that current collapse observed after a step diagnostic test was completely recoverable. This last observation suggests that current collapse during stress is mostly due to trapping and is also recoverable to a great extent by UV treatment and overnight recovery in the dark even after stressing the device beyond V_{CRIT}.

In Figure 3-22, it is clear that stressing down to V_{GS} = -50 V (below the critical voltage) has increased current collapse slightly for lower amplitude pulses just like the benign step diagnostic pulses. However stressing beyond the critical voltage has obviously increased current collapse for the whole range of pulse amplitudes used in these experiments by 40 mA/mm. This clearly shows that I_{GOFF} degradation at the critical voltage is the main indication of physical degradation in the device and it should be distinguished from change in parameters due to simple trapping.

It is interesting to compare the I_{DMAX} values in a step diagnostic experiment and a following stress experiment. I_{DMAX} values recorded in the second step diagnostic experiment of Figure 3-21 is shown in Figure 3-24 again. They are compared to I_{DMAX} values measured during the V_{DS} = 0 V step-stress experiment right after, where V_{GS} was stepped down to -50 V. The current collapse observed after one second pulses is obviously comparable to the collapse observed during the stress test itself, where each stress cycle lasted for one minute. In fact, this data shows that 50-70% of the current collapse occurs in the first second of the stress for this range of stress voltages. Moreover, stressing the device beyond V_{CRIT} after this test increased current collapse by 40 mA/mm for the whole range of voltages as we previously discussed. This increase due to permanent physical degradation is minor compared to the collapse observed even in the first second of the stress. This shows that stressing the device beyond the critical voltage and introducing permanent physical damage has increased the number of traps in the device, however this increase is very small as compared to the number of traps in the fresh device for this specific case.

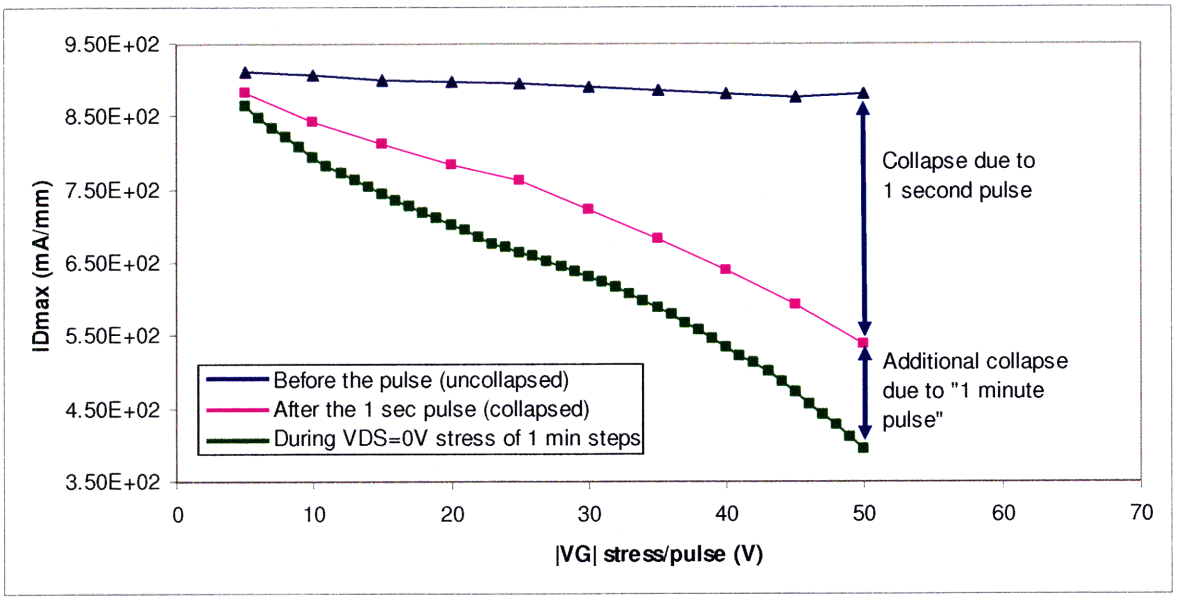


Figure 3-24: I_{DMAX} values recorded in a step diagnostic experiment are compared to those recorded in the following V_{DS} = 0 V step-stress test. These experiments were already discussed in Figures 3-21 to 3-23.

3.8 Other observations in GaN-on-Si HEMTs

3.8.1 Wide range of V_{CRIT}

In GaN on SiC devices, the critical voltage is found to be relatively well matched in devices within the same reticle within about 1 V [21]. Even from reticle to reticle on the same wafer, the difference tends to be within 10 V. This is usually not the case for GaN-on-Si devices. Figure 3-25 shows I_{GOFF} recorded from 6 devices from two different reticles on the same wafer. Curves with the same colors represent devices from the same reticle. The stress condition is the same for all devices and is a V_{DS} = 0 V step-stress type where V_{GS} is stepped from -5 V to -70 V by 1 V steps every 30 seconds. Although the devices are nominally identical and the stress conditions are identical, V_{CRIT} shows a wide range not only among different reticles of the same wafer but also within the same reticle.

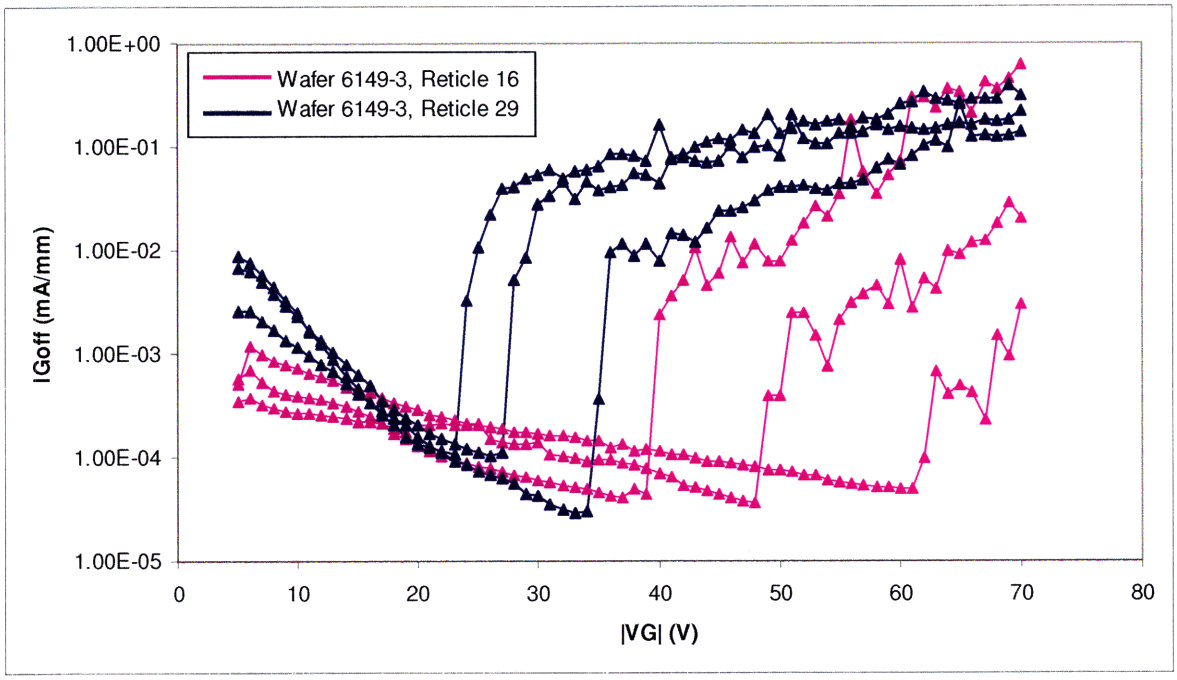


Figure 3-25: Wide range of critical voltages for I_{GOFF} degradation (V_{CRIT}) for identical V_{DS}=0V step stress experiments. Data for 6 GaN-on-Si devices are shown. Same colors represent devices from the same reticle.

Figure 3-28 shows OFF-state step-stress experiments where V_{GS} was kept constant at -5 V (below V_T) and V_{DS} was stepped from 5 V to high voltages (1V/step every 30 seconds) until all the devices experienced critical I_{GOFF} degradation. Similar to Figure 3-26, six devices from two reticles are compared and they are shown in separate viewgraphs for better illustration purposes. These experiments also show that V_{CRIT} can vary significantly throughout a wafer as well as in a single reticle as opposed to the case of GaN-on-SiC devices used in [21].

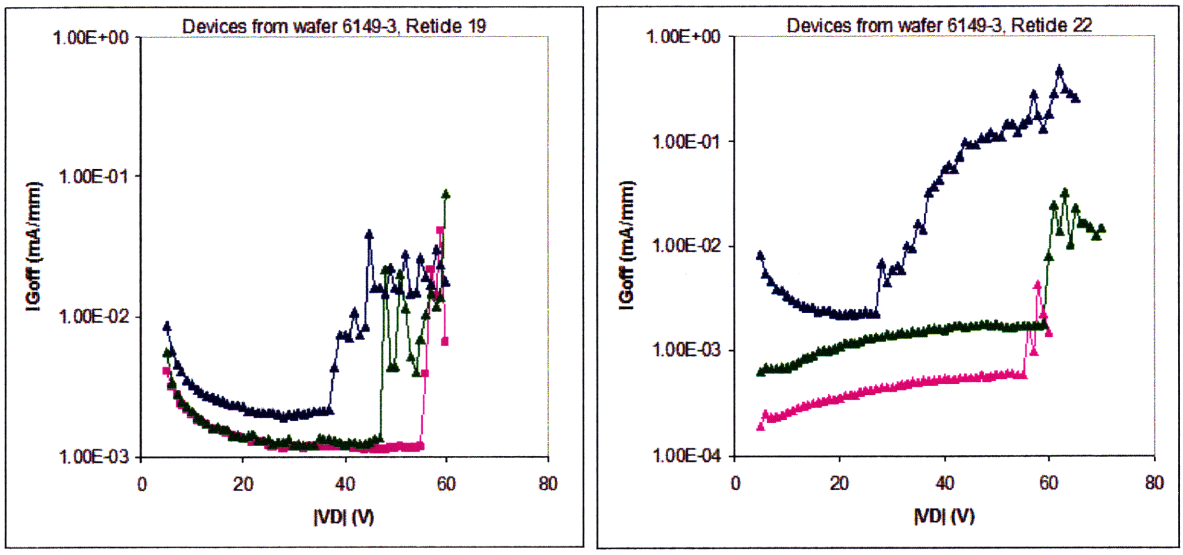


Figure 3-26: Wide range of critical voltages for IGOFF degradation (V_{CRIT}) for identical OFF state step stress experiments. Data for 6 GaN-on-Si devices are shown. I_{GOFF} values for devices from the same reticle are plotted on the same viewgraphs.

3.8.2 High V_T

Threshold voltage is known to be dependent on the barrier thickness and Al composition of the barrier layer. In Chapter 2, we have described the AlGaN/GaN heterostructure of our GaN-on-Si devices with barrier thickness of 18 nm and AlN composition (x) of 0.26. Although GaN-on-SiC devices used by [21] have similar parameters for the heterostructure (thickness of 16 nm and x=0.28), the threshold voltages exhibit a large difference as shown in Figure 3-27. In this figure, the changes of threshold voltages in identical V_{DS}=0 V step stress conditions are shown where V_G was stepped from -10 V to -70 V. Threshold voltage for the device on Si substrate starts from around -1.33 V and increases up to -0.92 V as the electrical stress is increased. On the other hand, V_T for GaN-on-SiC device changes from -3.34 V to -2.93 V.

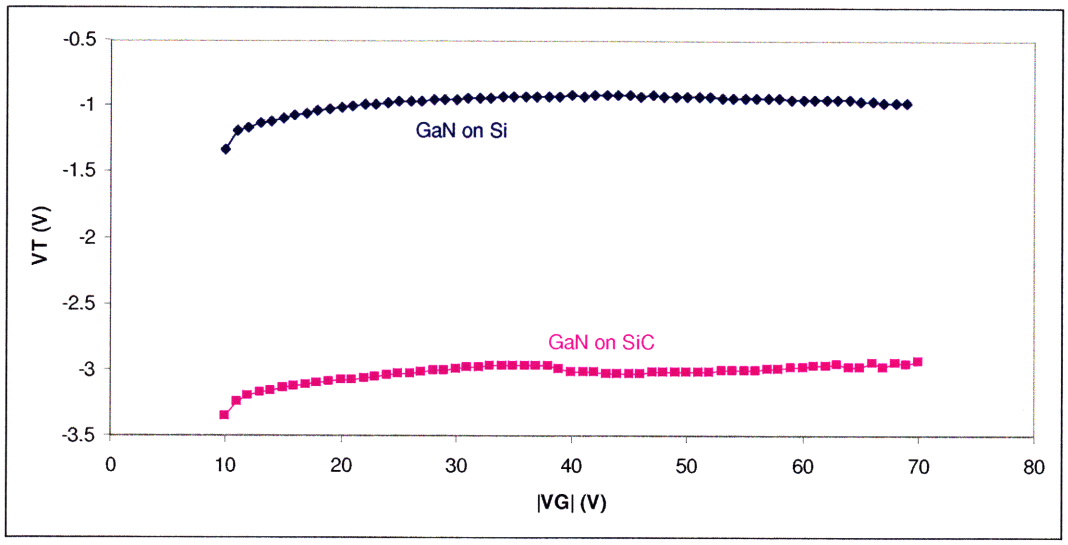


Figure 3-27: Threshold voltages for GaN-on-Si and GaN-on-SiC devices in identical V_{DS}=0V step stress tests. V_T is more positive for devices on Si substrates although the barrier layers have similar thicknesses and Al compositions.

3.9 Summary

We have shown that GaN-on-Si devices have more traps than GaN-on-SiC devices even before any stress is introduced. This is illustrated by using current collapse and current transient measurements right after a pulse which charges these traps and showing that more current collapse occurs in devices on Si substrates.

High power step-stress experiments where current and voltage is stepped separately revealed the fact that voltage is more effective in degrading device parameters. The effect of temperature in these experiments was eliminated by sweeping the same power levels at each step of the stress tests.

Step-stress experiments were performed to show that degradation can be recovered to some extent when the stress is removed. This indicates that trapping is an important phenomenon in these devices and that more trapping takes place under high voltages. V_{DS}=0 V step-stress tests proved to degrade device parameters more than OFF-state step-stress experiments. This is consistent with the discussion in [21] where the reason for physical degradation was described as

the converse piezoelectric effect in GaN triggered by high electric fields. We have also obtained consistent observations of I_{GOFF} undergoing a sudden and non-recoverable increase by several orders at a critical voltage.

Enhanced detrapping under UV light is introduced and this was utilized to study the traps by means of step diagnostic pulses applied at the gate of the device. Pulse magnitude was stepped to mimic the increased electrical stress during the step stress experiments. Before each pulse, the traps were emptied and using UV light proved to be efficient in decreasing the detrapping time. The study of traps using step diagnostic tests showed that the current collapse observed in I_{DMAX} during stress tests is mostly due to trapping and only a slight increase in the number of traps is introduced by stressing the device beyond the critical voltage.

Finally, a wide range of critical voltages for GaN-on-Si devices have been observed even in devices that are closely located side by side.

Chapter 4 : Discussion

4.1 Introduction

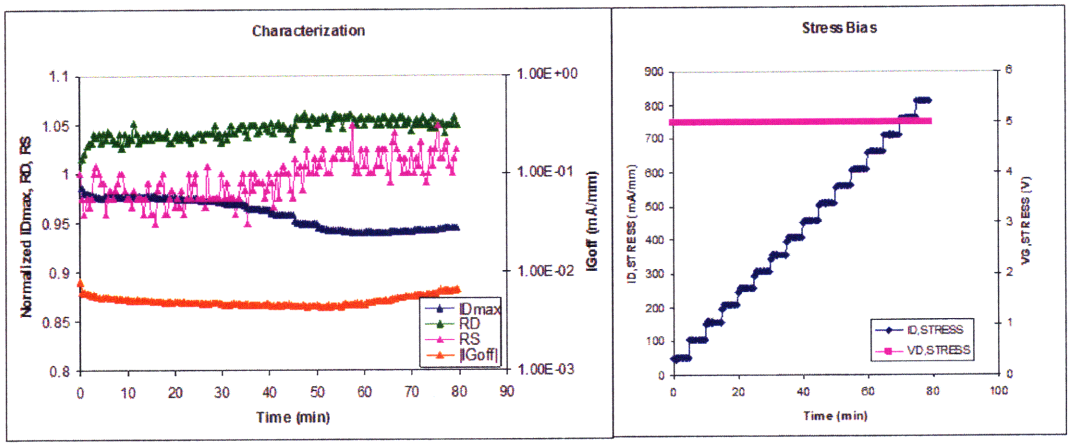
In the previous chapter, we have studied the degradation of GaN-on-Si HEMTs in several step stress experiments as well as stress-recovery experiments. We performed experiments where I_{GOFF} experienced several orders of magnitude of increase beyond a critical voltage and this was consistent with the observation in [21]. We also concluded that trapping is very effective in degrading device parameters and this was shown experimentally for I_{DMAX}. We also showed that UV light enhances detrapping and helps device parameters recover very fast during the characterization periods where the stress is interrupted. In this chapter, we will begin by explaining a possible trapping mechanism under high voltage bias. The permanent physical degradation mechanism will be discussed. After that, we will show that UV is also effective in enhancing detrapping to some extent during stress. The consequences of this effect will be discussed by presenting experimental data comparing similar stress tests in the dark and under illumination with UV light and visible microscope light.

4.2 Trapping as a degradation mechanism

In Section 3.3, it was shown that higher voltages are more effective than high currents in the degradation of GaN HEMTs. Later in Section 3.7, step diagnostic experiments were performed to understand to the first order what portion of this degradation is due to trapping in the traps that are already in the fresh device. This was done by application of negative voltage pulses at the gate of the device with increasing amplitude. The duration of these pulses were kept at 1 second to minimize any "damage" and this damage was proved to be minimal as discussed in Figure 3-21. In Figure 3-24, it was shown that most of the current collapse occurs in the first second of the stress, hence the diagnostic pulses proved to be an effective tool to qualitatively study the nature of traps.

The observation that source resistance R_S did not degrade during high power stress experiments supports the idea that the electric field is more effective in causing trapping in the device. In that case, the drain side of the gate experiences the high voltage difference as $|V_{GS}|$ is usually close to 0 V. The current is the same on both sides; however this current does not affect R_S as much as R_D. These observations could also be attributed to hot electron effects as discussed in [22-25] due to the fact that the electrons are hotter when they are traversing the drain side of the gate and cause more damage.

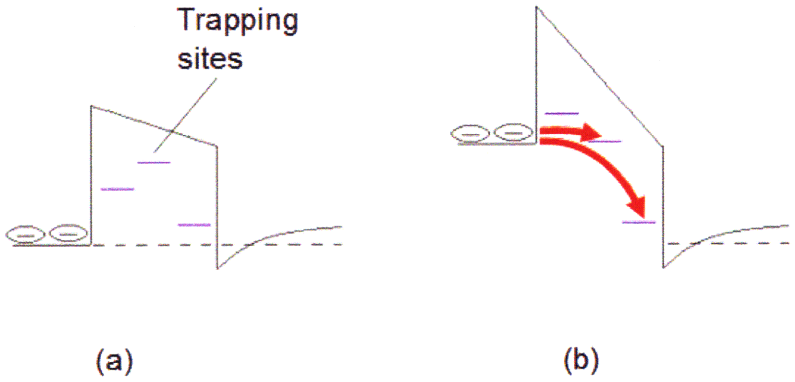
In order to test this, we have designed ON state experiments. Figure 4-1a shows that there is almost no degradation in R_S and only 5% degradation in R_D and I_{DMAX} when V_{DS} = 5 V and I_D is stepped from 50 mA/mm to 800 mA/mm. These stress bias conditions are described in Figure 4-1b. 800 mA/mm is almost the maximum current that these devices can provide and still the degradation in I_{DMAX} and R_D is minimal. Moreover, no critical degradation for I_{GOFF} is observed. This clearly shows that hot electrons might be responsible for degradation only to some extent, but large amounts of degradation cannot be explained by just this mechanism.



(a) (b)

Figure 4-1: ON state step stress experiment: (a) the parameters measured by the characterization suite and (b) the stress bias conditions where V_{DS}= 5 V and constant and I_D is stepped from 50 mA/mm to 800 mA/mm by 50 mA/mm steps every 5 minutes.

One possible explanation how trapping is enhanced by the electric field is illustrated in Figure 4-2. The application of a negative gate voltage increases the electric field across the AlGaN barrier layer which has many trapping sites due to the defects associated with the lattice and thermal mismatch of GaN and Si. This also decreases the effective barrier height for the electrons to reach these trap centers. This explains how even one second of a large voltage pulse applied at the gate can result in significant trapping. Some of these trap levels are geographically deep from the surface and once the electrons get trapped in them, the recovery period exhibits a slow transient behavior with very long time constants.



(a) (b)

Figure 4-2: Trapping enhanced by large electric fields due to negative voltage applied at the gate. (a) shows the case before the application of the negative bias and (b) shows the change in the band diagram after the bias qualitatively.

In Figure 3-15, the degradation in I_{DMAX}, R_D, R_S and I_{GOFF} was proved to be mostly due to trapping and hence recoverable. However, they did not reach their original values before the stress exactly. On the other hand, we previously showed in Section 3.6 that UV has the biggest recovery efficiency in V_T and SS. Figure 4-3 displays the change in these parameters during the same test as in Figure 3-15. In this experiment, the first phase was just characterization in the dark to see the original values of the parameters. In the second phase, device was stressed at V_{DS} = 0 V constant stress condition with V_G = -30 V. In the third phase, the device was allowed to recover in the dark and the UV light was turned on to enhance detrapping during Phase 4. They both reach their original values in the fresh device in Phase 5, where the UV light was turned off during recovery again. During the illumination, V_T dropped below the value in the fresh device probably due to emptying the traps already occupied before the application of any stress or the extra carriers generated by light excitation. The effect of this excitation on SS is seen as an increase during Phase 4.

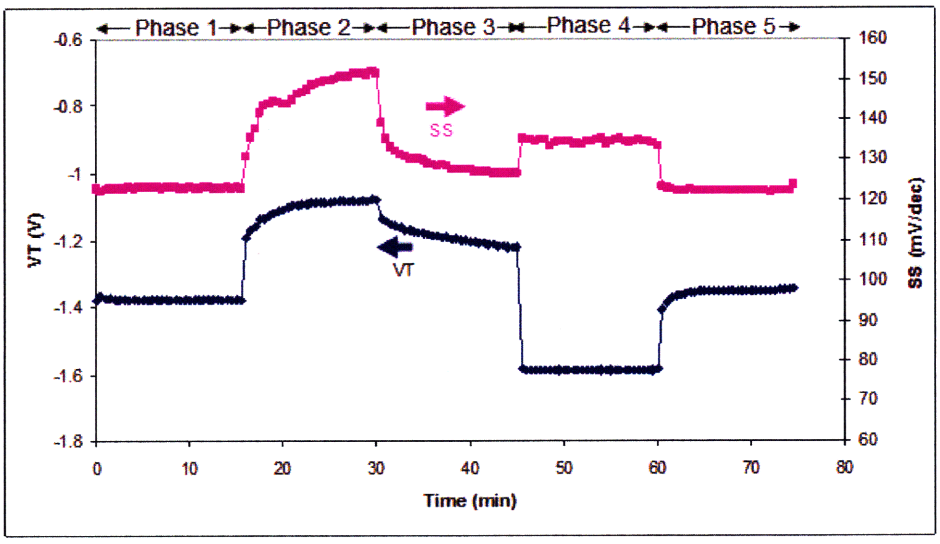


Figure 4-3: Change in V_T and SS during the same test as in Figure 3-14.

Figure 4-4 shows the drain current in the subthreshold regime under UV illumination with 365 nm wavelength and in the dark. It is clear that when the UV is on, V_T is shifted to more negative values and subthreshold swing gets worse. However, this does not prevent these parameters from maintaining their original values after the light is turned off because of enhanced detrapping. Below V_G = -2 V, the flat nature of the I_D curve for UV suggests that there is a photocurrent on

the order of 100 nA. This corresponds to 2 μA/mm of current for our devices with gate width of 50 μm. Clearly, the photocurrent is only a minor component of the drain current that flows in these devices under normal operating conditions. The same conclusion can be made for gate leakage current as seen in Figure 4-5. Here, the gate current under UV illumination is almost the same as that in the dark in the range of gate voltages where I_G is minimal and hence any increase in current due to the photocurrent is expected to be clearly observed.

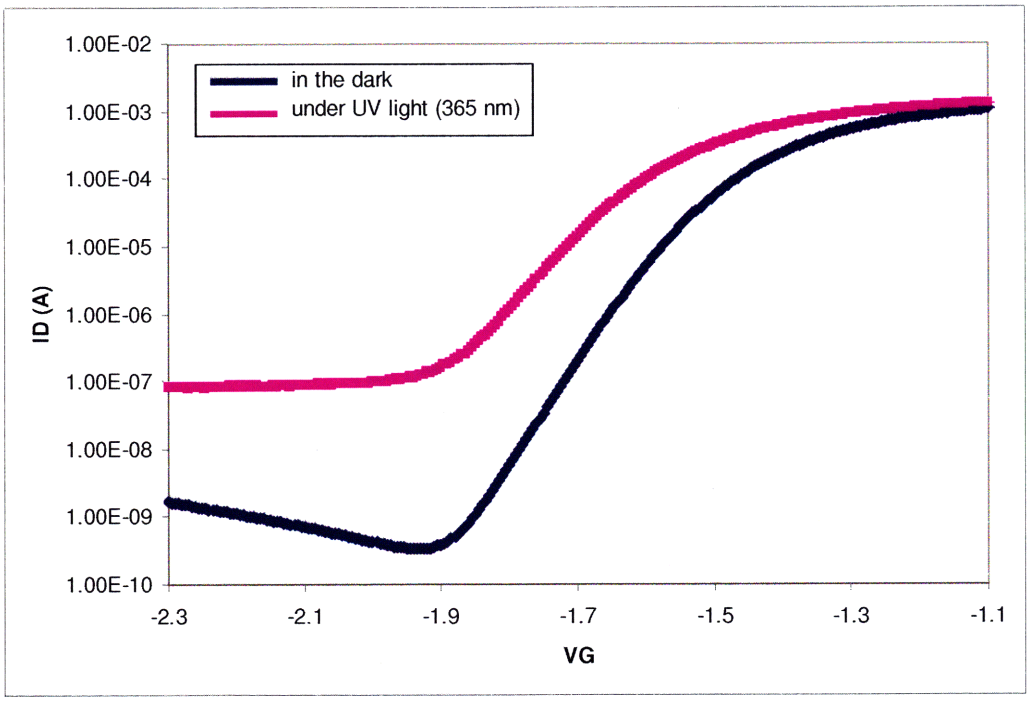


Figure 4-4: Drain current in the subthreshold regime for both under UV illumination with 365 nm wavelength and in the dark.

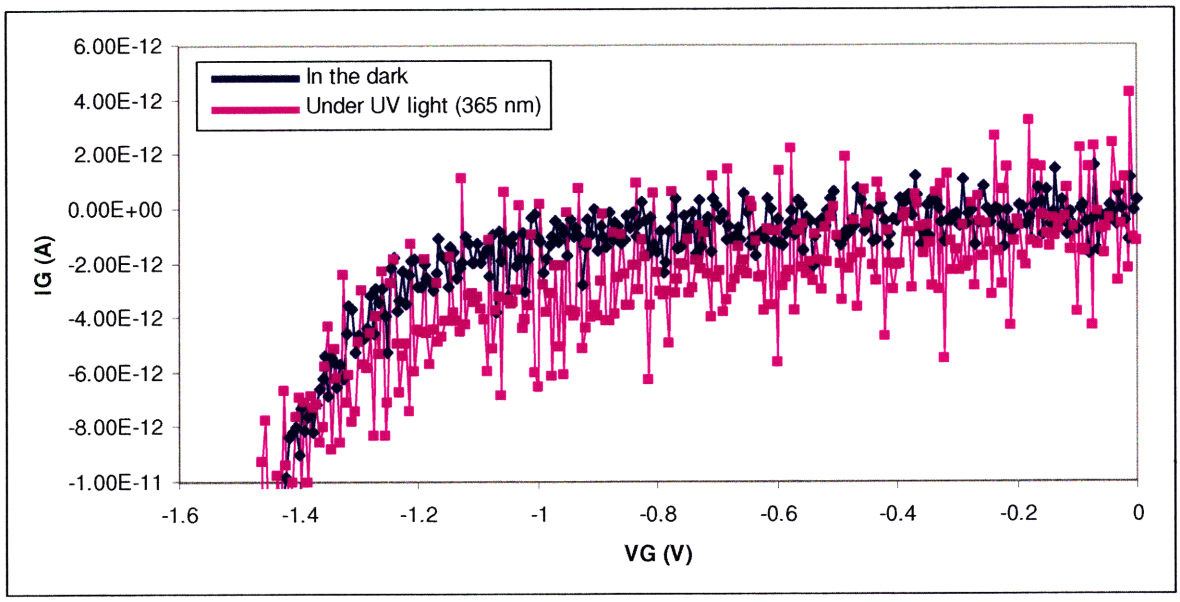


Figure 4-5: Gate current in the dark and under UV illumination in the gate voltage range where I_G is minimal to see if there is any increase caused by the photocurrent.

4.3 Critical Degradation in I_{GOFF}

We have investigated the recovery of parameters when the device is stressed below the critical voltage. In this stress regime, I_{GOFF} degradation is also recoverable. On the other hand, we have observed that all the figures of merit except I_{GOFF} can still recover when the device is stressed beyond V_{CRIT}. However, I_{GOFF} does not go down once it is critically degraded. Figure 4-6 illustrates this case by comparing two V_{DS} = 0 V step-stress experiments on the same device. In the first stress experiment, the device was fresh and V_G was stepped from -10 V to -70 V by 1 V steps every minute. I_{GOFF} exhibited a critical degradation at V_G = -62 V. The device was allowed to rest in the dark for 45 days and the same experiment was repeated. Although I_{DMAX} had recovered up to the same level as in the fresh case, it showed a small discrepancy at low voltages due to the extra traps related to the defects created during the first stress. This was not the case for I_{GOFF} and it remained at the same degraded value reached at the end of the first stress experiment. This is an obviously different behavior from the case where the change in I_{GOFF} was recoverable in the experiment shown in Figure 3-15 as the stress bias voltage was below V_{CRIT}. This is consistent with the discussion in Section 3.7, where we concluded that stressing the

device beyond V_{CRIT} introduces permanent physical degradation by just looking at the current collapse increase in this stress regime.

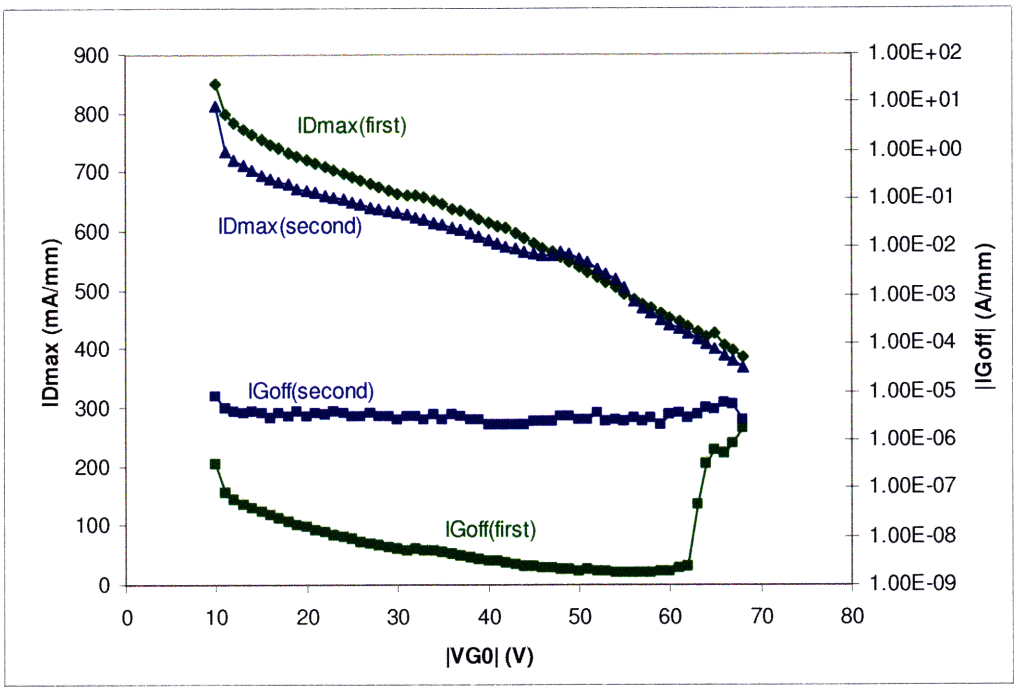


Figure 4-6: Two identical V_{DS} = 0 V step stress experiments on the same device. In the first experiment, the device was fresh but I_{GOFF} went through a critical degradation at V_G = -62 V. I_{DMAX} recovered mostly after waiting for 45 days, however I_{GOFF} degradation was permanent.

We already discussed that for our devices, hot electron type degradation is not as effective in the previous section. On the other hand, all of our observations are consistent with the hypothesis that converse piezoelectric effect degrades the device at some critical voltage because of the high electric fields in the device [21]. The tensile strain in the AlGaN barrier due to the lattice mismatch with the GaN buffer is increased through the converse piezoelectric effect triggered by high electric fields. Permanent physical degradation occurs at a critical voltage when the total strain accumulates the critical elastic energy for defects to occur. From this observation, we distinguish two separate degradation mechanisms for our GaN-on-Si devices caused by high voltages: enhanced trapping and permanent physical degradation along with increased number of traps due to the converse piezoelectric effect as described in [21].

The reason why critical degradation causes a permanent gate current increase is discussed in [31]. The traps between gate and the channel constitute a path for gate leakage current by providing "steps" for electrons to travel from the gate to the channel. This is consistent with our observation of I_{GOFF} decrease in Figure 3-12 until the critical voltage of -45 V is reached. The path for I_{GOFF} starts getting "clogged" as these traps get populated by electrons. Once the critical voltage is reached, more defects are created between the gate and the channel and the traps associated with these defects constitute more paths for I_{GOFF} in a permanent manner.

4.4 Enhanced Detrapping During Stress

In Section 3.6, we showed that UV light enhances the detrapping of electrons from trapping centers when the stress is removed. Figures 3-15 to 3-20 show the parameters measured by the characterization suite when the stress is interrupted temporarily during stress tests. One would expect that UV light also enhances detrapping when the stress conditions are applied. One possible way to investigate this is to focus on the gate current at stress bias conditions, namely $I_{G,STRESS}$. For negative gate bias voltages, the stress current flows through the gate by the same mechanism as I_{GOFF}. Hence $I_{G,STRESS}$ is a good representative of I_{GOFF} and the trapping can be qualitatively observed by focusing on this parameter. As detrapping is enhanced, more traps are available to provide a current path for either I_{GOFF} or $I_{G,STRESS}$.

Figure 4-7 shows how illumination effects $I_{G,STRESS}$ during a V_{DS} = 0 V type stress experiment. During stress, V_G is kept constant at -25 V. This is below the critical voltage to avoid adding additional traps and complicating the observations. The experiment has five phases. During the first phase, the device was stressed in the dark. During the second phase, the sample was illuminated by visible microscope light during the stress. In the third phase, the visible light was turned off. The effect of UV light was investigated in Phase 4 and the device was stressed in the dark again in the last phase. The initial fast drop from 0.14 mA/mm to 0.03 mA/mm is due to trapping and it is clear that almost all of this happens in the first minute. There is still some trapping that cannot be completely removed by UV as seen from the transient behavior in Phase 4, however the increased $I_{G,STRESS}$ during UV illumination clearly shows that UV light has been successful in producing some detrapping during stress. Some of this increase in $I_{G,STRESS}$ can be

attributed to photocurrent, however, we previously discussed in Figure 4-5 that photocurrent associated with I_G during UV illumination is negligible.

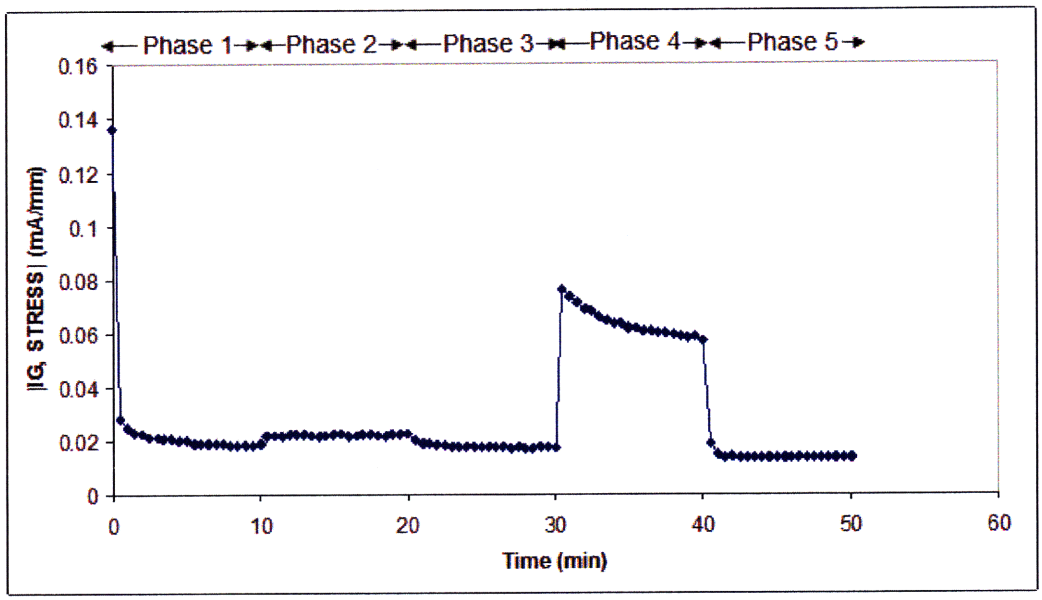


Figure 4-7: The change of gate bias current $I_{G,STRESS}$ during a V_{DS} = 0 V stress with constant V_G = -25 V. The device was stressed in the dark during Phase 1, Phase 3 and Phase 5. It was illuminated with microscope light in Phase 2 and UV (365 nm) in Phase 4.

4.5 Effect of UV on V_{CRIT}

In Figure 3-12, I_{GOFF} decrease down to the point where V_{CRIT} is reached was attributed to trapping, however although the voltage is steadily increased, the decrease in I_{GOFF} tends to get slower. This is mostly due to less number of empty traps that are available for new electrons to be trapped as time goes on. This explains the transient behavior observed in $I_{G,STRESS}$ during UV illumination because this means UV has made some of the traps available for retrapping by emptying them in the first place. On the other hand, we also attribute this decrease in the trapping rate to the fact that the trapped electrons cause a decrease in the sheet carrier concentration. This causes the electric field to be more spread out but the peak field to be reduced at the same stress voltages.

We showed in the previous section that UV light can enhance detrapping during the stress as well as during recovery. According to our hypothesis of field screening by trapped electrons,

using UV light during stress experiments will keep the traps less charged and decrease screening against the electric field. This means lower stress voltages under UV illumination will have the same effect on our devices as the case when the device is stressed in the dark. One observable implication of this effect would be a shift if V_{CRIT} to lower values in V_{DS} = 0 V step stress experiments when devices are stressed under UV light.

In the discussion of Figure 3-20, we pointed out the fact that one of the two neighboring samples which were stressed under UV light experienced critical I_{GOFF} degradation at a lower voltage than the other sample stressed in the dark. This is consistent with our hypothesis; however we also mentioned in Section 3.8 that devices even in the same reticle can show a wide range of critical voltages. We need to repeat many such controlled experiments to make a safe statistical statement that illumination under UV light decreases V_{CRIT}.

Figure 4-8 shows the result of such a set of experiments. We tested 15 pairs of devices from 5 different reticles on the same wafer. Each pair had two neighboring devices in the same reticle to eliminate any structural differences as much as possible. We stressed one of the neighbors in the dark in a V_{DS} = 0 V step-stress experiment where V_G was stepped beyond the critical voltage by 1 V every 30 seconds. The other device in the pair was stressed under the same bias conditions but under UV illumination (365 nm). The critical voltages recorded for samples stressed under UV are plotted against those recorded for the ones stressed in the dark. Ideally if all the samples were stressed in the dark, one would expect all the data points to be evenly scattered around y=x line. However under UV illumination, all the measurement data points except one outlier lie below the y=x line. We argue that the change of V_{CRIT} caused by UV should be more emphasized for high critical voltages. The data points were fit by imposing the fact that UV light cannot decrease V_{CRIT} below 0 V, i.e. the lines intersect at V_{CRIT} = 0 V. For this stress configuration, the slope of the fitted line is 0.76. This is a quite big deviation from the ideal slope of 1 and agrees with out hypothesis.

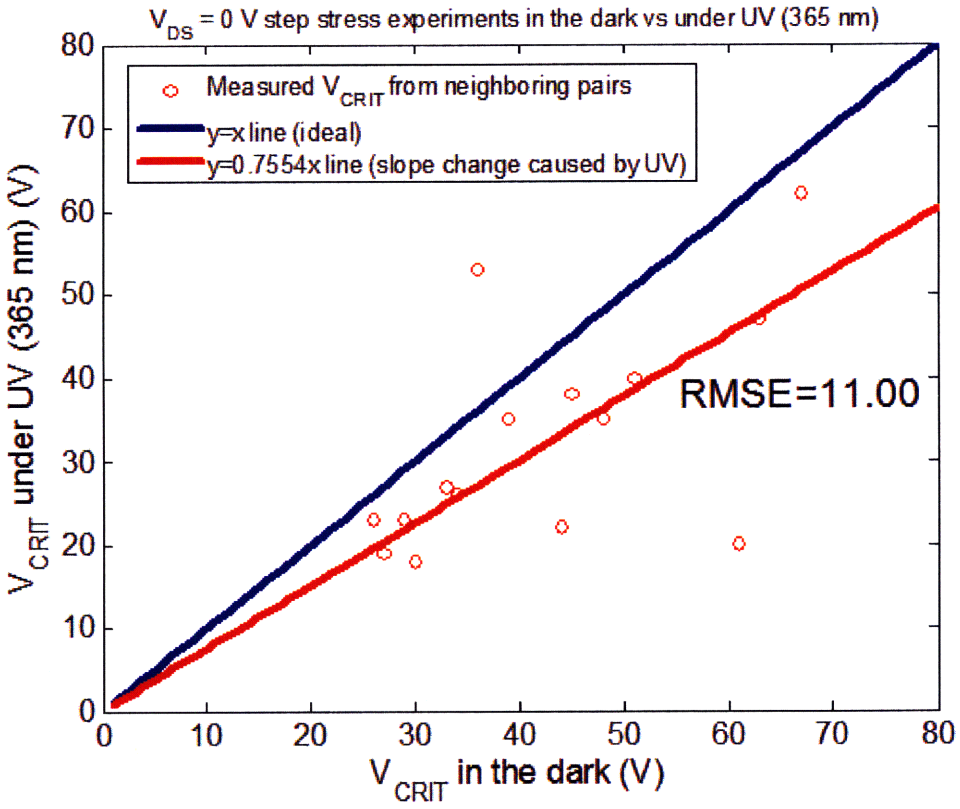


Figure 4-8: The effect of UV light (365 nm) on V_{CRIT} for V_{DS} = 0 V step stress tests. Each circle represents a comparison of V_{CRIT} from neighboring devices, one of which was stressed under UV light and the other in the dark. The slope of the fitted line is changed from 1 to 0.76 by UV illumination.

As a further proof of our hypothesis, we performed the same experiments under visible light. Another 15 pairs of devices were stressed and their critical voltages when stressed under microscope light were compared to those when stressed in the dark. We previously concluded when discussing Figure 4-6 that microscope light did not enhance detrapping much. The result should be very close to what one would expect from comparing samples only in the dark, i.e. the data points should be scattered randomly and evenly around y=x line. This is indeed the case in Figure 4-8 as seen from the perfect match of the ideal line and the fitted data. The slope of the fitted line is 0.99 and it is very close to the ideal slope of 1 as expected.

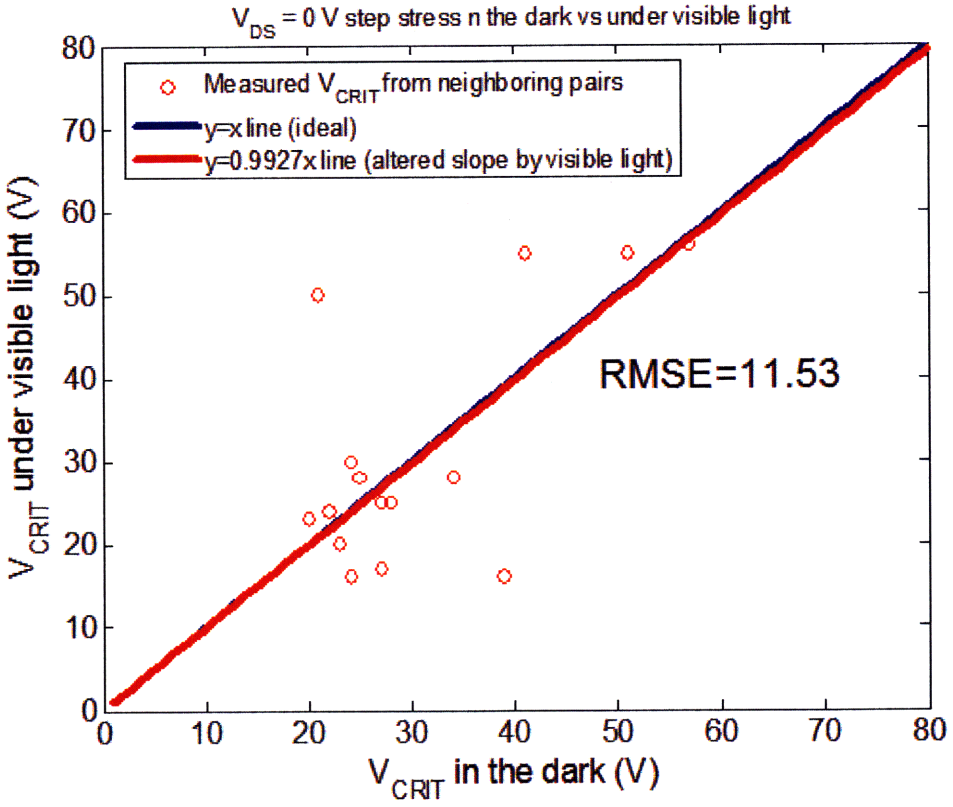


Figure 4-9: The effect of visible light on V_{CRIT} for V_{DS} = 0 V step stress tests. Each circle represents a comparison of V_{CRIT} from neighboring devices, one of which was stressed under visible light and the other in the dark. The change in the slope of the fitted line by visible light is negligible (from 1 to 0.99).

Once we have a consistent set of data for V_{DS}=0 V step-stress experiments, we move forward to check our hypothesis for OFF-state step-stress conditions as well. Figure 4-9 displays a similar comparison as in Figure 4-7, but for an OFF-state step-stress scheme. In these tests, V_D was stepped from 5 V up to high values beyond V_{CRIT} and V_G was kept constant at -5 V to pinch the channel off. There are two outliers in this data set, but the slope of the fitted line changed to 0.75 from the ideal value of 1. Along with other experiments discussed here, the results support our hypothesis of field screening caused by trapped electrons during high voltage stress conditions.

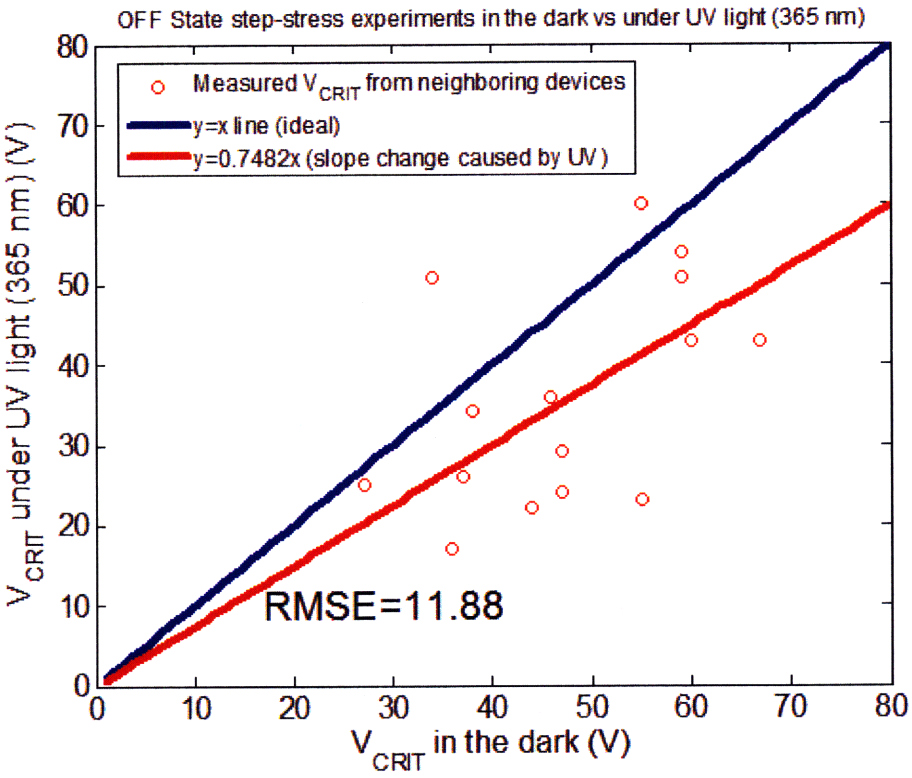


Figure 4-10: The effect of UV light (365 nm) on V_{CRIT} for OFF state step stress tests. Each circle represents a comparison of V_{CRIT} from neighboring devices, one of which was stressed under UV light and the other in the dark. The slope of the fitted line is changed from 1 to 0.75 by UV illumination.

4.6 Summary

In this chapter, we have qualitatively discussed how trapping is enhanced when the electric field across the AlGaN barrier is enlarged through high voltage bias. We have concluded that physically deep traps from the surface can also get charged and these cause slow recovery behavior in the device parameters when the stress is removed. The increased number of traps in GaN-on-Si devices due to the large mismatch between GaN and Si plays an important role in this picture. We showed that hot-electron effects are not as effective in degrading the device as the case of high-voltage stress.

Besides trapping, there is another degradation mechanism observed in our devices, namely the converse piezoelectric effect proposed by [21]. According to this mechanism, high electric fields in the device cause mechanical strain that is added to the tensile strain due to the AlGaN/GaN

mismatch. This added strain causes formation of new defects and hence permanent degradation at a critical voltage where the elastic energy hits a critical value. This shows itself through a several orders of increase in the gate leakage current. Our observations in V_{DS} = 0 V and OFF-state step-stress tests are consistent with this hypothesis.

Finally, we showed that UV light illumination enhances detrapping during the stress by looking at its effect on the gate bias current during stress, namely $I_{G,STRESS}$. Visible microscope light did not have a significant effect on this current and was concluded to be not successful in detrapping during stress. For the UV experiments, we proposed a hypothesis where the trapped electrons decrease the sheet charge density which causes the electric field in the device to spread out and the peak field to be reduced. This means that higher peak electric field values will be obtained for the same stress voltages if detrapping could be enhanced such as by UV illumination. One consequence of this effect is lower critical voltages for gate current degradation. We have successfully shown for V_{DS} = 0 V and OFF state step stress tests that UV illumination shifts V_{CRIT} to lower voltages by keeping the traps relatively uncharged during the electrical stress. For the case of visible light where no enhanced detrapping was observed, the critical voltage did not show any change based on statistical data.

Chapter 5 : Conclusion

5.1 Summary of Key Findings

Reliability of GaN HEMTs has been the main concern in their deployment in high power and high frequency applications. Reliability studies have been made but to the best of our knowledge, no explicit reliability study was conducted for GaN HEMTs grown on Si substrates. The importance of Si as a substrate is mainly due to its low cost, availability in large diameters and well-known electrical characteristics. In this thesis, we presented results of different electrical reliability experiments as well as evaluation tools for GaN-on-Si HEMTs and the results were compared to SiC where applicable.

The main concern about using Si as a substrate is the larger lattice and thermal mismatch compared to other substrates such as SiC and sapphire. As a result, greater number of dislocations and defects occur in the device structure acting as trapping centers even in fresh devices. This places additional concerns on the reliability of GaN-on-Si HEMTs. We performed electrical stress tests on the devices that we obtained from our collaborator Nitronex Corporation. Among these are step-stress and stress-recovery experiments as followed in [21] and [38].

During the stress experiments, a benign characterization suite used in [21] was utilized to monitor the device parameters I_{DMAX}, I_{GOFF}, R_D, R_S, V_T and SS by interrupting the stress temporarily at a predetermined frequency. Step-stress tests were highly productive as they enabled us to examine the change in these parameters in several stress conditions in a single experiment. Stress-recovery experiments helped identifying the trapping behavior observed frequently in our devices as the device parameters recovered to some extent during the intervals the stress was removed.

High power step-stress experiments were performed to see the general degradation behavior in GaN-on-Si HEMTs. Since the thermal resistance of the substrate is finite, the channel temperature increases during these high power tests. To eliminate the effect of temperature in the comparison of high voltage and high current step stress tests, the experiments were designed so that the power consumption in both experiments were the same at each step. These experiments yielded the conclusion that high current stress is secondary to the effect of high voltage stress as device parameters exhibited a larger degradation under high voltage. These experiments suggested that current could be eliminated from the picture to eliminate the effect of temperature as well.

OFF state and V_{DS}=0 V stress experiments are such experiments where there is negligible current and power consumption in the device. Stress-recovery tests with these stress schemes showed that degradation is due to trapping to some extent as transient behavior in parameters towards their original values was observed in recovery periods. The slow recovery suggested that deep traps are at play. Although all other parameters showed similar recovery behavior in both V_{DS} = 0 V and OFF state stress-recovery tests, I_{GOFF} behaved in a relatively unpredictable manner when the gate voltage is very negative. This suggested that more careful experiments regarding the gate voltage be carried out.

V_{DS} = 0 V step-stress experiments shone some light on the behavior of I_{GOFF}. Despite the fact that all other figures of merit degraded in the same fashion throughout the whole step-stress experiment, I_{GOFF} first decreased with the increasing amplitude of the gate voltage up to a critical voltage V_{CRIT} where it suddenly experienced an increase by several orders of magnitude. After

this observation, we divided the stress regimes into two regions: stress below the critical voltage for I_{GOFF} degradation and stress beyond V_{CRIT}. The main motivation was the observation that I_{GOFF} degradation was recoverable in stress-recovery tests only if the stress voltage is below the critical voltage.

The main reason for degradation was identified as trapping and recoverable to some extent for stress conditions below V_{CRIT}. As a result of slow recovery transients, we looked for methods to enhance detrapping and get the recovery transients faster. UV illumination during the recovery periods was realized to be an effective tool for detrapping. The capability to empty the traps in an efficient way led us to study the traps in devices during several step-stress tests by the help of stepped-amplitude pulses. The physical degradation in the device was defined as either or both of reduction in I_{DMAX} level and increase in current collapse observed after the application of a pulse at the gate with specific amplitude. It was shown that the pulses used in the so called step diagnostic tests were benign as they did not introduce any reduction in the uncollapsed I_{DMAX} values or a significant increase in the current collapse. They were used in the evaluation of devices when the devices were fresh, when they were stressed down to just below V_{CRIT} and when they were stressed beyond V_{CRIT}. I_{DMAX} was always recoverable almost to the values before any stress. The current collapse seemed to increase only slightly and only for lower voltage conditions when the stress was halted before reaching the critical voltage. However, stressing the device beyond V_{CRIT} resulted in an obvious increase in the current collapse experiments and obvious physical degradation was identified for this case. The most important result of these experiments was obtained when comparing the I_{DMAX} during a stress experiment and the I_{DMAX} recorded right after the application of step diagnostic pulses. In this comparison, it was obvious that high voltage stress enhances trapping and most of the trapping occurs in the first second of the stress.

Although V_{CRIT} is an important figure for a device and for a specific test scheme, we did not observe very consistent critical voltage values recorded for devices for the same stress conditions even on the same wafer and in the same reticle. This observation invoked the need for repeating many experiments for devices in close proximity to make a statistical comparison of critical voltages under different environmental conditions such as UV illumination.

We discussed that step stress experiments under low voltage high current conditions are not as effective as high voltage stress. This led us to the conclusion that hot electron related effects as discussed in [22-25] are minor as compared to the effect of high voltage on our devices. High voltage was found to enhance trapping in the device.

The other important effect of high voltage stress was the critical degradation observed in I_{GOFF}. This observation is consistent with the degradation mechanism related to the converse piezoelectric effect in GaN as discussed in [21]. The vertical field due to high voltage stress adds more strain on the tensile strain of the AlGaN barrier due to the mismatch with GaN buffer. When the field gets as high as to increase the elastic energy beyond a critical value, more defects are formed in the barrier between the gate and the channel serving as additional current paths for gate leakage. This is a permanent degradation. Although other figures of merit recover under UV illumination even when the device is stressed beyond V_{CRIT}, I_{GOFF} stays at its degraded level.

Effect of UV light was investigated on the gate bias current, namely $I_{G,STRESS}$ during a constant stress test in V_{DS}=0 V scheme. The current flow mechanism for I_{GOFF} and $I_{G,STRESS}$ is similar and the same effect during enhanced detrapping was observed under UV. They both increase under UV illumination which means that detrapping is enhanced. On the other hand, no increase in $I_{G,STRESS}$ was observed under visible microscope light, so we concluded that visible light is not effective in enhanced detrapping during stress conditions.

We proposed a mechanism where trapped electrons in the device suppress the sheet carrier density and cause the electric field distribution to spread out and the peak field value to decrease. As we already identified UV illumination as a way to keep these traps relatively uncharged, we expected to see a decrease in V_{CRIT} when the devices are stressed under UV illumination because this would mean higher electric field values would be achieved at lower stress voltages. This was indeed the case for V_{DS} = 0 V and OFF-state step-stress tests. However, we did not observe any such decrease in V_{CRIT} when the devices were stressed under visible light. This is consistent with our hypothesis as visible light was previously concluded to be ineffective to keep the traps uncharged during the stress.

Although Si has been a very attractive alternative to SiC as a substrate, our observations in increased trapping due to larger lattice and thermal mismatch suggests that concerns about reliability cannot be disregarded. We have shown cases where I_{DMAX} instantaneously decreased to half after application of very short pulses with amplitudes as large as 50 V. Moreover, although the slump is recoverable to some extent in a few seconds following the pulse, there are very slow components in this transient behavior. Exhaustive treatment under UV light during the recovery should be applied before the current reaches its original value. This means that even a short glitch with high amplitude during regular operation of HEMT could cause a power collapse with a slow recovery behavior. The situation could get even more questionable if this is not a glitch but a rather prolonged stress condition such as a deeply OFF state or highly ON state.

The degradation patterns observed in GaN-on-Si HEMTs are similar to SiC. The change of parameters during the step-stress and stress-recovery experiments utilized in this study shows a good correlation with the GaN-on-SiC devices tested in [21] under similar conditions. The converse piezoelectric effect seems to affect both types of devices in a similar way. This is good news as such a well-characterized and economically advantageous substrate yields similar degradation patterns as SiC, however the consequences of higher rates of trapping and slower recovery are not desirable as described above. To avoid increased trapping and slow recovery behavior, studies that focus on decreasing the threading dislocation density and related traps could be done as in [33-36].

5.2 Suggestions for Further Work

Although we have results in agreement with converse piezoelectric effect as a degradation mechanism, the bigger concern for GaN-on-Si HEMTs seems to be the degradation caused by increased trapping. We have investigated the behavior of these traps under a few stress bias conditions and pulsing schemes, however we have not performed detailed studies to understand the exact nature and location of these traps. We have mostly focused on $V_{DS} = 0$ V and OFF-state step-stress conditions as they degrade the device parameters in the fastest and harshest way. We have used step diagnostic pulses only in the V_{DS}=0 V scheme, where the pulse is applied at the

gate. The way the devices are stressed and evaluated can be diversified to understand the nature and physical location of these traps better. ON and OFF state pulses can help understand the nature of traps on the drain side of the gate and in the buffer better than the methods used in this thesis.

The effect of temperature on the device parameters has not been investigated. It would be interesting to perform stress experiments at different temperatures and see the effect of temperature on the critical voltage where I_{GOFF} degrades permanently. Since trapping is a main degradation mechanism, focusing on the effect of temperature on trapping and detrapping phenomena will give invaluable insight in the physics of the degradation. We have done preliminary experiments where we observed a shift of detrapping time constants to lower values as the temperature is increased, however we did not present the data in this thesis.

We have also started doing detrapping experiments under different wavelengths in the UV range. The effect of wavelength on the recovery curves as well as the shift in V_{CRIT} values are worth focusing on in further research. Results for only visible light and 365 nm UV light are reported in this thesis; however similar observations supporting our hypothesis of field screening by trapped electrons are made under 254 nm UV light. Moreover, the transient behavior during illumination shows that there is trapping going on even under UV light. The dynamics of this process is worth understanding to draw a better picture of and support our hypothesis.

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