XXI. COMPUTER RESEARCH

Prof. J. B. Dennis
N. Kerllenevich
R. A. Saunders
G. Y-C. Wang

A. EXPANDED INSTRUCTION CODE FOR THE TX-0 COMPUTER

The capability of the TX-0 computer has been enlarged through the addition of an index register and appropriate new instruction codes. The new system organization of the TX-0 is shown in Fig. XXI-1. The unique operate instruction of the TX-0 has been given more flexibility as shown in Charts 1 and 2. The set of addressable instructions has been enlarged from the original three to the twenty-three shown in Chart 3.

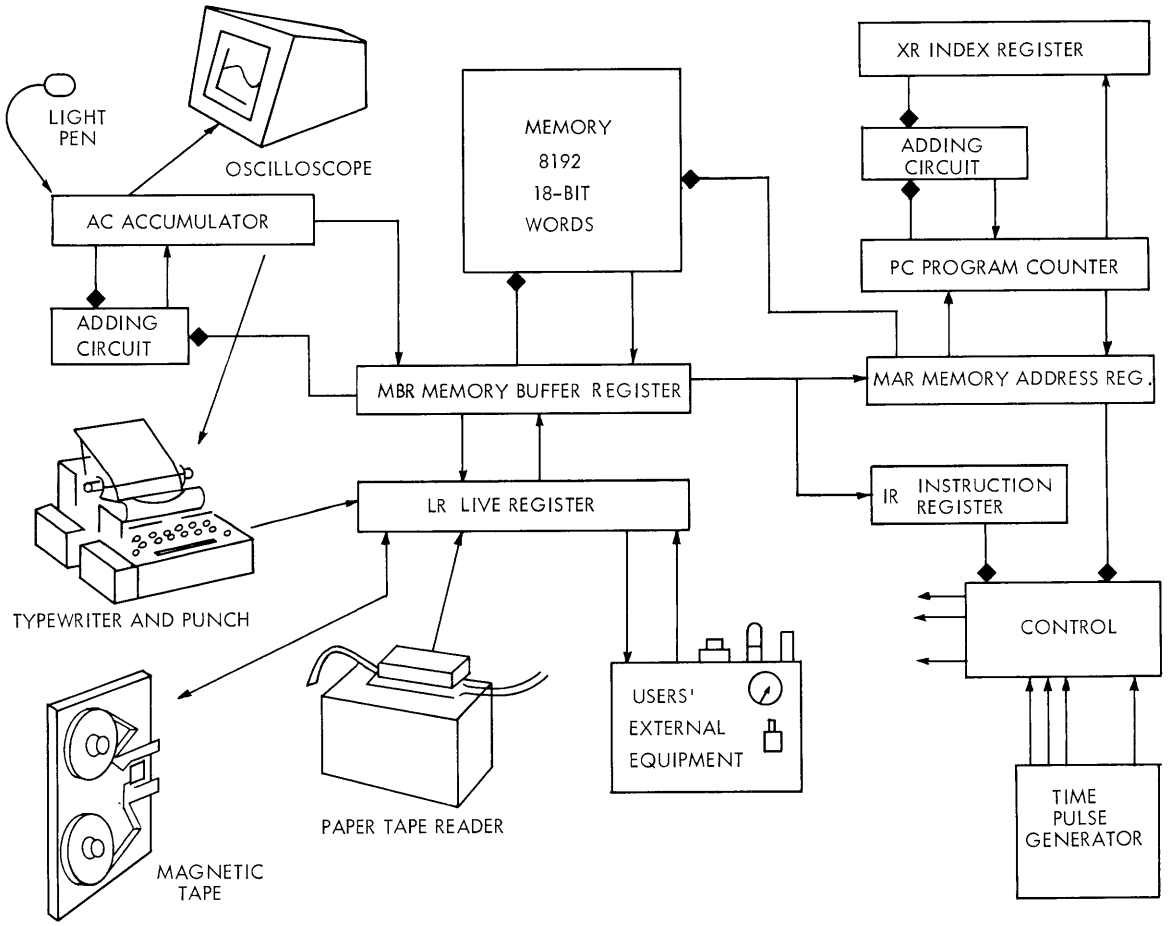


Fig. XXI-1. TX-0 system organization.

Notation

AC: ACcumulator

LR: Live Register

PC: Program Counter

MBR: Memory Buffer Register

C(AC): "Contents of AC"

$\rightarrow$: "Replaces"

$-x$ or $\overline{x}$: Complement of x

$\wedge$: Intersect; and; logical product

$\vee$: Union; inclusive or; logical sum

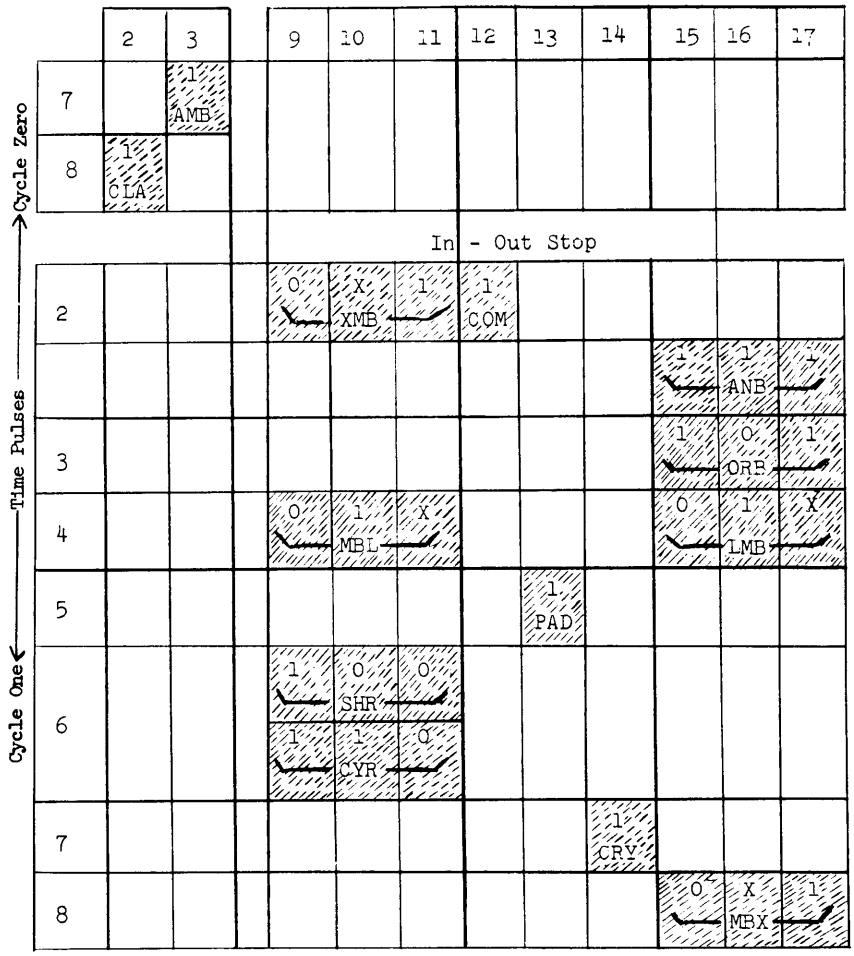
$\oplus$: Partial add; inequivalence; exclusive or

mod n: Modulo n; $y = x \bmod n$ means $x = kn + y$ for some integer k, $0 \leq k \leq n - 1$.

x	y	$x \wedge y$	$x \vee y$	$x \oplus y$	$\overline{x}$ or $-x$
0	0	0	0	0	1
0	1	0	1	1	1
1	0	0	1	1	0
1	1	1	1	0	0

Addition in the Accumulator is 18-bit, ones complement. Index addition is 14-bit, ones complement.

Chart 1. TX-0 Operate Instruction Micro Orders



Instruction bits 0 and 1 must be one for all operate instructions. The bit combinations associated with the symbols cause the corresponding actions in Chart 3 to occur in the time sequence indicated above. Bits 4 through 8 of operate instructions are used for in-out functions.

Chart 2. TX-0 Operate Instruction Micro Orders

MNEMONIC	ACTION	SYMBOLIC DESCRIPTION
CLA	CLear AC	$0 \rightarrow C(AC)$
AMB	transfer AC contents to MBR	$C(AC) \rightarrow C(MBR)$
XMB	transfer XR contents to MBR	$C(XR)$ bits 5-17 $\rightarrow C(MBR)$ bits 5-17. $C(XR)$ bit $4 \rightarrow C(MBR)$ bits 0-4.
MBL	transfer MBR contents to LR	$C(MBR) \rightarrow C(LR)$
LMB	transfer LR contents to MBR. Note: LMB and MBL, if used simultaneously, interchange C(LR) and C(MBR).	$C(LR) \rightarrow C(MBR)$
MBX	transfer MBR contents to XR	$C(MBR)_{5-17} \rightarrow C(XR)_{5-17}$ $C(MBR)_0 \rightarrow C(XR)_4$
CYR	CYcle AC contents Right one binary position. (AC bit 17 goes to AC bit 0)	$C(AC)_i \rightarrow C(AC)_j$ $i = 0, 1, \ldots, 17$ $j = (i+1) \bmod 18$
SHR	SHift AC contents Right one binary position (AC bit 0 is unchanged, bit 17 is lost)	$C(AC)_i \rightarrow C(AC)_{i+1}$, $i = 0, 1, 2, \ldots 16$
ANB	ANd (logical product) LR into MBR.	$C(LR) \wedge C(MBR) \rightarrow C(MBR)$
ORB	OR (logical sum) LR contents into MBR.	$C(LR) \vee C(MBR) \rightarrow C(MBR)$
COM	COMplement AC	$-C(AC) \rightarrow C(AC)$
PAD	Partial ADd MBR to AC (for each MBR one, complement the corresponding AC bit.)	$C(MBR) \oplus C(AC) \rightarrow C(AC)$
CRY	A CarRY digit is a ONE if in the next least significant digit, either AC = 0 and MBR = 1, or AC = 1 and carry digit = 1. The carry digits so determined are partial added to the AC by CRY. PAD and CRY used together give a full one's complement addition of C(MBR) to C(AC).	$CRY[C(AC), C(MBR)] = C(AC) \oplus C \rightarrow AC.$ $C_i = [C(MBR)_j \wedge \overline{C(AC)_j}]$ $\vee [C_j \wedge C(AC)_j]$ $i = 0, 1, \ldots, 17$ $j = (i+1) \bmod 18.$ $CRY[C(AC) \oplus C(MBR), C(MBR)]$ $= C(AC) + C(MBR)$

Chart 3. TX-0 Addressable Instructions

(A) STORE CLASS

MNEMONIC	OCTAL VALUE	OPERATION	SYMBOLIC DESCRIPTION
STO y	000000 + y	Store	C(AC)→C(y)
Place the contents of AC in register y. The previous contents of y are destroyed. Contents of AC remain unchanged.			
STX y	020000 + y	Store AC, Indexed	C(AC)→C(y+C(XR)) 2 cycles
SXA y	040000 + y	Store Index in Address	$C(XR)_{5-17} \rightarrow C(y)_{5-17}$
Store the digits of the index register in the address portion of register y. The sign of XR is ignored. The contents of XR are unchanged. Bits 0 through 4 of register y are unchanged.			
ADO y	060000 + y	Add One	C(y) + 1→C(AC) →C(y)
Add One to the contents of memory register y and leave the results in the accumulator and register y.			
SLR y	100000 + y	Store Live Register	C(LR)→C(y)
The contents of LR are placed in register y. The previous contents of y are destroyed. Contents of LR are unchanged.			
SLX y	120000 + y	Store LR, Indexed	C(LR)→C(y+C(XR))
STZ y	140000 + y	Store Zero	0→C(y)
Clear register y to plus zero.			

(B) ADD CLASS

MNEMONIC	OCTAL VALUE	OPERATION	SYMBOLIC DESCRIPTION
ADD y	200000 + y	Add	$C(y) + C(AC) \rightarrow C(AC)$
Add the contents of register y to AC. Contents of y are unchanged.			
ADX y	220000 + y	Add, indexed.	$C(y+C(XR)) + C(AC) \rightarrow C(AC)$
LDX y	240000 + y	Load Index	$C(y)_{5-17} \rightarrow C(XR)_{5-17}$ $C(y)_0 \rightarrow C(XR)_4$
Load the index register from bit 0 and bits 5 through 17 of register y. The contents of y are unchanged.			
AUX y	260000 + y	Augment Index	$C(y)_{0,5-17} + C(XR) \rightarrow C(XR)$
The contents of memory register y are added to XR. The fourteen bit number added consists of bit 0 and bits 5 through 17 of register y. Addition is ones' complement on 14 bit numbers.			
LLR y	300000 + y	Load Live Register	$C(y) \rightarrow C(LR)$
The contents of register y replace the previous contents of LR. Contents of y are unchanged. Previous contents of LR are destroyed.			
LLX y	320000 + y	Load LR, Indexed	$C(y+C(XR)) \rightarrow C(LR)$
LDA y	340000 + y	Load Accumulator	$C(y) \rightarrow C(AC)$
The contents of register y replace the previous contents of the AC. Contents of y are unchanged. Previous contents of the AC are destroyed.			
LAX y	360000 + y	Load Accumulator, Indexed	$C(y+C(XR)) \rightarrow C(AC)$

(C) TRANSFER CLASS

MNEMONIC	OCTAL VALUE	OPERATION	CONDITIONS AND SYMBOLIC DESCRIPTION	
			$y \rightarrow C(PC)$	$C(PC)+1 \rightarrow C(PC)$
TRN y	400000 + y	Transfer on Negative AC	$C(AC)_0 = 1$	$C(AC)_0 = 0$
If the AC bit 0 is a one, take next instruction from register y. Otherwise, take next instruction in sequence.				
TZE y	420000 + y	Transfer on Zero	$C(AC) = +0$ or $C(AC) = -0$	$C(AC) \neq +0$, and $C(AC) \neq -0$
If the contents of the accumulator are either plus zero or minus zero, the next instruction is taken from register y. If the accumulator contents are not plus or minus zero, the next instruction in sequence will be executed.				
TSX y	440000 + y	Transfer and Set Index	Always; $C(PC) \rightarrow C(XR)_{5-17}$ $0 \rightarrow C(XR)_4$	Never
The next instruction is taken from register y and the address of the register following the TSX instruction is placed in the index register.				
TIX y	460000	Transfer and Index	$C(XR) \neq +0$ and $C(XR) \neq -0$	$C(XR) = +0$ or $C(XR) = -0$
If the index register contains plus or minus zero, perform the next instruction in sequence without changing the contents of the index register. If the index register contains a non-zero positive number, its contents are reduced by one and the next instruction is taken from register y. If the index register contains a non-zero negative number, its contents are increased by one and the next instruction is taken from register y. A zero result will have the same sign as the initial contents of the index register.			If $C(XR)_4 = 1$, $C(XR)+1 \rightarrow C(XR)$; If $C(XR)_4 = 0$, $-[-C(XR)+1] \rightarrow C(XR)$	

MNEMONIC	OCTAL VALUE	OPERATION	CONDITIONS AND SYMBOLIC DESCRIPTION	
			y→C(PC) Timing: 1 cycle	C(PC)+1→C(PC) Timing: 2 cycles
TRA y	500000 + y	Transfer	Always	Never
The next instruction is taken from register y.				
TRX y	520000 + y	Transfer, Indexed.	Always y+C(XR)→C(PC)	Never
TLV y	540000 + y	Transfer on external Level	External level = 0 volts	External level = -3 volts
This instruction provides a means of testing an external condition, provided said condition can provide a 0 or -3 volt level at the in-out panel connection labeled TLV.				
TPL y	560000 + y	Transfer on Positive Live Register	$C(LR)_0 = 0$	$C(LR)_0 = 1$
If LR sign is positive, take the next instruction from register y; otherwise, take the next sequential instruction.				

J. B. Dennis