Mechanism and Assessment of Spin Transfer Torque (STT) Based Memory

by

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ABSTRACT

When a sufficient current density passes through the MTJ, the spin-polarized current will exert a spin transfer torque to switch the magnetization of the free layer. This is the fundamental of the novel write mechanism in STT-RAM, current-induced magnetization switching. It allows STT-RAM to have a smaller cell size and write current than MRAM, and also capable of what MRAM promises: fast, dense, and non-volatile.

A technological assessment was conducted to verify the claims of STT-RAM by understanding the physical principles behind it. A comparison of performance parameters in various memory technologies was also made. STT-RAM scores well in all aspect except in the size of the memory cell. The high current density ($>10^6$ A/cm^2) sets the lower limit of the size of the driving transistor and ultimately the cost of manufacturing STT-RAM. Cost models were presented to estimate the cost of a STT-RAM based on a three mask levels fabrication process. Although much effort has been put into reducing the switching current density, there are still no easy solutions to the problem. Research and development of STT-RAM must show success in a very near future or else STT-RAM will follow the step of its predecessor, MRAM: surviving in the niche market.

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PART I   THE TECHNOLOGY

1.   Introduction

The ability to manipulate spin degree of freedom of conduction electrons, in addition to charge, inspired an exciting new field of spintronics [1]. Spintronics, a joint word of spin and electronics, was founded after giant magnetoresistance (GMR) effect had been discovered [2]. GMR is the change of resistance that depends on the relative orientation of the magnetization of two ferromagnetic (FM) layers. It was not surprising that these GMR structures have been widely used as an element in the read head of hard disk drive [3]. Nevertheless, a higher magnetoresistance response is still demanded to further expand the application of GMR. This eventually led to another big step in spintronics, the discovery of magnetic tunnel junction (MTJ). MTJ exhibits the behavior of tunneling magnetoresistance (TMR) with a much higher MR ratio than the GMR structure.

The development of spintronics coincides with the changing period of semiconductor memories. In this information era, the demand for information storage is ever increasing but the devices that hold the memories become even more compact. Moreover, cost effectiveness permits only little change on the existing complementary metal oxide silicon (CMOS) processing for a new memory technology [4]. Combining these two traits, an embedded and more CMOS-compatible memory is more preferable. However, the most important factor that triggers the search for a new memory technology is the inherent scalability issue in the current memory technologies (beyond 40 nm for DRAM [5] and beyond 22 nm for NAND flash [6]). Therefore, the reason for implementing MTJ as the magnetic element in a magnetic memory device, or better known as magnetic random access memory (MRAM), becomes obvious. MRAM is said to be capable of speed of static random access memory (SRAM), the density of dynamic random access memory (DRAM), the non-volatility benefits of flash, and the unlimited endurance [7]. (SRAM is the fastest memory in the market and DRAM has reasonable capacity without comprising the speed.) In other words, MRAM will be the universal memory. However, after years of effort, the intrinsic disadvantages of MRAM, such as large cell size and high write current, greatly forbids it to be widely commercialized [7].

Although spin transfer torque (STT) is initially regarded as the cause of noise in recording technology [8], researchers found that it can be manipulated for producing a current-induced magnetization

switching memory device. This immediately solves the high write current and scaling issue in MRAM. Although applications of STT effect are not limited to only memory devices (for example, spin-torque diode [9] and nano-oscillator [10]), a STT based random access memory (STT-RAM) is more vital for the reasons discussed above. Therefore, a technological assessment on STT-RAM is crucial, especially when the technology is not commercially available. This thesis will first discuss the necessary physics and mechanism of GMR and TMR. It is important to understand some of the basis that is similar with STT-RAM. In chapter two, the process of current-induced magnetization switching is examined. The current will cause the electrons to precess around the local magnetization that ultimately causes magnetization switching at a given condition, namely sufficient switching current density. The switching current density depends on several parameters, which is either material or geometrical effect. The switching speed then depends on the switching current density. Together with other conducting elements, MTJ forms the basic configuration of a STT-RAM memory cell. The read and write mechanisms will be discussed as well. In the final section of chapter two, the memory cell size is shown to be directly related to the switching current density. The following of the thesis will switch its focus to evaluate the market and implementation of STT-RAM. Comparison among the memory technologies is included because it is crucial to judge the standpoint of STT-RAM. Then, the application and memory market share that are associated to STT-RAM is explored. The size of the market allows us to determine whether STT-RAM should be invested at the beginning. The influence of failed-to-deliver MRAM on STT-RAM is also investigated. The fabrication process will be discussed in chapter four. This will include the estimation of the fabrication cost using two different methods. Search on STT-RAM related patents will reveal whether the value of fabricating a STT-RAM is all taken. From here, the business model to venture into the STT-RAM market as well as the decision to pursue STT-RAM or otherwise is made.

1.1.   Giant Magnetoresistance (GMR)

Before furthering the discussion of GMR effect, it is important to understand some of the spin nomenclatures since there are often confusion between the direction of spin and magnetization. In metals, electron spin is opposite in direction with magnetic moment [11]. Majority-spin or spin-up electrons are electrons with moment parallel (spin antiparallel) to the magnetization of the ferromagnetic (FM) layer, while minority-spin or spin-down electrons are electrons with moment

antiparallel (spin parallel) to the magnetization. When a current is said to be spin-polarized, it means most of the electrons are either spin-up or spin-down.
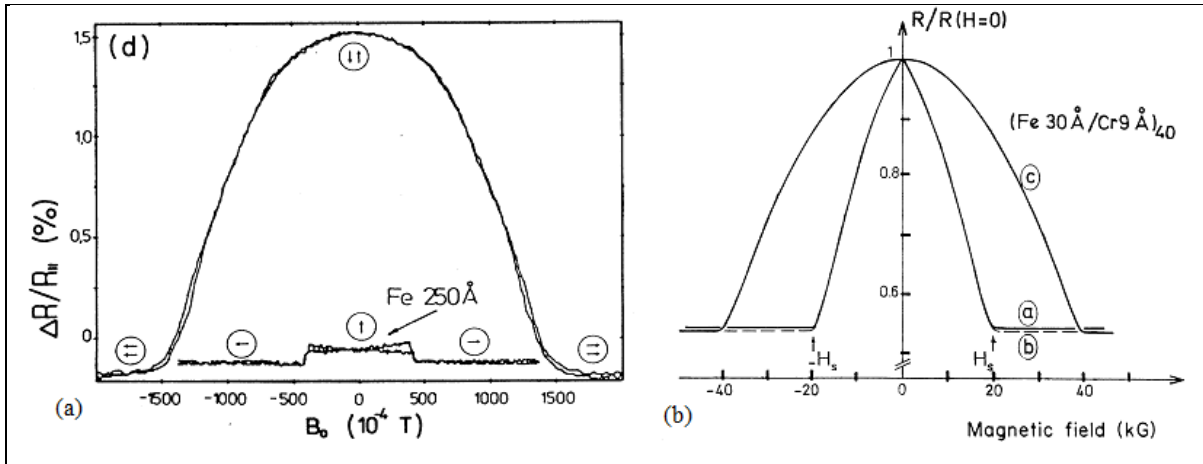
Figure 1 The first two demonstration of GMR effect. The horizontal and vertical axes are the applied magnetic field and MR ratio, respectively. (a) The larger curve the GMR effect. (b) The field is in-plane with the current in a and b, but perpendicular in c. Taken from [12,13].

The simplest structure for the observation of GMR effect consists of two FM layers sandwiching a spacer layer [2]. FM materials show magnetism during the presence of an external magnetic field and the magnetism vanishes if the field is taken away. Typical FM materials are iron (Fe), nickel (Ni), cobalt (Co) and their alloys, with or without other addition: permalloy (NiFe), CoFeB, CoFe, and so on. The spacer layer in a GMR structure is made of nonmagnetic (NM) metals, such as copper (Cu). GMR effect is first observed in two configurations: Fe|Cr|Fe trilayer [12] and Fe|Cr super lattice [13]. Chromium (Cr), an antiferromagnetic (AFM) material, is used in the above mentioned configurations. AFM materials have spin ordering that can be visualize as the following figure:
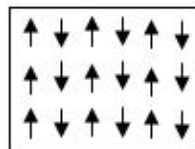

Figure 2 Spin ordering of AFM materials below Neel temperature. Cr, FeMn and NiO are commonly used antiferromagnetic materials.

The individual thickness of the multilayers that displayed GMR effect must be comparable to the mean free path of electrons or less [2], typically a few nanometers [10]. When a current pass through the trilayer, the resistance (R_{AP}) of the trilayer becomes high if the relative magnetizations of the two FM layers are in antiparallel; the resistance (R_P) is low if the magnetizations are in parallel. This phenomenon is called the GMR effect. One of the two FM layers has its magnetization fixed (referred as the fixed or pinned layer) while the magnetization of the other FM layer is free to rotate (free layer). The FM|NM|FM layered structure soon became the foundation for the continuous development of this field.

The key mechanism of GMR effect is spin dependent scattering. Mott [14] first proposed the two-current model to explain this phenomenon. In this model, there are two independent conducting channels, which means that the spin-up and spin-down electrons have different scattering probability [15,16]. This is because the d-bands in FM materials are spin-split, thus k the densities of states are different for both spin-up and spin-down electrons [15]. The unoccupied d-states will act as scattering centers, since they are situated near the Fermi surface in transition metals. The result is spin-up electrons will scatter less than spin-down electrons. A better GMR effect means a higher MR ratio and MR ratio is defined by

$$\frac{(R_{AP} - R_P)}{R_P} = \frac{\Delta R}{R_P}.$$

(1)
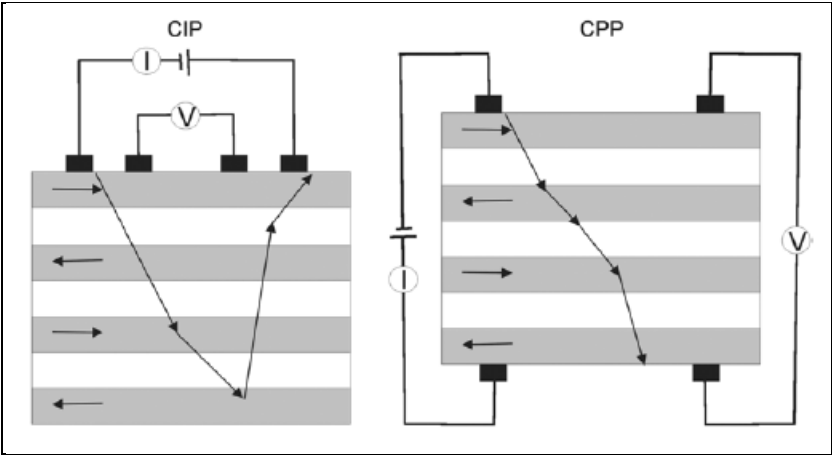
Figure 3 Left: CIP-GMR. Right: CPP-GMR. The arrows represent the movement of electrons. Taken from [16].

There are two versions of GMR structures: current-in-plane (CIP) and current-perpendicular-to-plane (CPP) (Figure 3). The name of CIP indicates the flow of current is along the plane of multilayer, whereas the direction of current is normal to the plane of multilayer in CPP structure. In a CIP structure, it is important that the mean free path is longer than the total thickness of the layers. In the contrary, spin diffusion length is more important in the case of CPP structure. Spin diffusion length is the distance of the electrons travelled without spin flipping (spin is conserved).

1.1.1. Spin accumulation in CPP-GMR

Valet and Fert in 1993 [17] pointed out that in CPP geometry, the net spin transport across the FM|NM|FM structure causes spin accumulation in the area near the interface, in contrast to CIP geometry. Therefore, spin accumulation effect is the key difference between CIP and CPP geometry.

Consider an antiparallel magnetizations, the electrons will be spin-polarized by the fixed layer, which the case of more majority-spin electrons than minority-spin electrons is assumed. At the far right of the FM|NM interface, the number of spin-up and spin-down electrons are equal due to spin flipping. Consequently, at the first FM|NM interface, more spin-up electrons will flip their spins, causing an accumulation of spin-up electrons in the area near the interface [2]. Spin-up electrons injected into the NM layer will reduce to a minimum, but not zero since the thickness of FM layer is thin. The spin-up electrons again accumulates at the second NM|FM interface because the majority-spin electrons became minority-spin electrons that will get scattered in the second FM layer.

In summary, spin accumulation and spin flip scattering changes the electric field and thus induces potential drops at the interfaces. The extra potential drop will introduce interface resistance, which helps to enhance the MR ratio when compared to a CIP geometry. All the discussions above are valid in the limit of t_F, $t_N \ll l_{sd}$ and $\lambda < l_{sd}$, where t_F, t_N, λ and l_{sd} is thickness of FM layer, thickness of NM layer, mean free path and spin diffusion length, respectively. This discussion is also applicable to parallel magnetizations configuration. The result can further be generalized to include both bulk and interface spin dependent scattering. This theory is later extended to any multilayered structures including spin valves with synthetic free layers, laminated free and pinned layers, and dual spin valves [18]. This consideration also includes spin flipping in all layers.

1.2.   Tunneling Magnetoresistance (TMR)

The main difference between TMR and GMR is TMR uses a magnetic tunnel junction (MTJ) structure. MTJ is very similar to GMR structure, with the exception of the metallic spacer layer is replaced by an insulating layer. The insulating layer is also known as tunnel barrier; the materials are usually Al_2O_3 or MgO. MTJ has a CPP geometry, which means the current flows in the direction normal to the plane of multilayer. Therefore, the theories that applied to CPP geometry also applies to MTJ, in some extent.
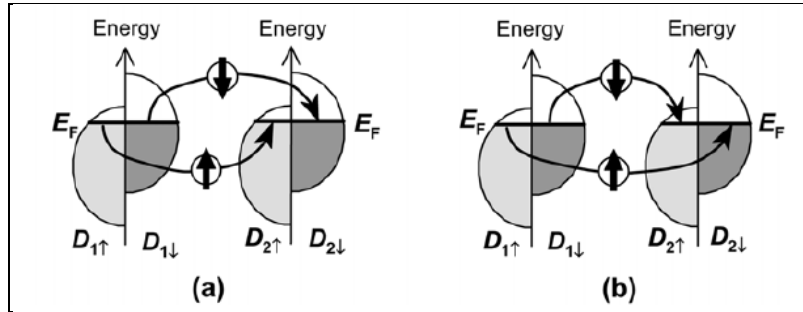
Figure 4 Illustration of TMR effect using band structure. Adapted from [19].

Julliere in 1975 first observed the TMR effect using Fe|Ge|Co structure with germanium (Ge) as the insulating barrier (10-15 nm) [20]. In Julliere's work, the MR ratio (or conductance ratio in Julliere's work but it is equivalent) is given as

$$\frac{2P_1P_2}{1 - P_1P_2}.$$

$$(2)$$

P_1 and P_2 are the spin polarization of the FM materials (P_α), which is defined as

$$\frac{D_{\alpha\uparrow} - D_{\alpha\downarrow}}{D_{\alpha\uparrow} + D_{\alpha\downarrow}}; \ \alpha = 1,2$$

$$(3)$$

with α=1 (2) refers to the first (second) FM layer. $D_{\alpha\uparrow}$ and $D_{\alpha\downarrow}$ denote the density of states at Fermi energy (E_F) for the majority-spin and minority-spin electrons, respectively. In other words, P_α value depends on the tunneling density of states of electrons. In parallel magnetizations, electrons in FM

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layer will find more empty states to tunnel through the barrier than in antiparallel magnetizations (Figure 4). The MR ratio calculated using experimental P values fits well to the experimental MR ratio [19]. However, the theoretical P values derived from band calculations using Julliere's model does not agree with experimental P values. Nevertheless, one important point can still be taken from this model: better spin polarization of FM materials will increase the MR ratio.

A more complicated model involves the transmission of Bloch states. Various Bloch states can tunnel incoherently through the amorphous barrier, such as Al_2O_3 [19]. With crystalline MgO barrier [19], the decay rates for all other Bloch states are high except for one that tunnels coherently. This is due to the matching of Bloch states of the FM layer and the insulating barrier. This remaining Bloch state has net spin polarization of 100%; therefore, MgO-MTJ has higher MR ratio than Al-O-MTJ. For further reading, please refer to [21,22].
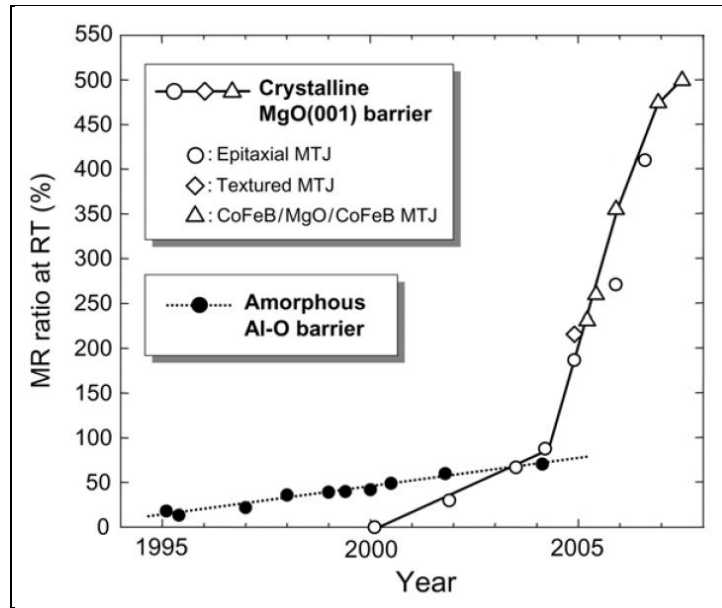
Figure 5 Improvement on MR ratio of different MTJ configuration at room temperature. Adapted from [19].

The highest MR ratio of amorphous Al-O MTJ is around 70% at room temperature [2,19]. Experimental work of MgO-based MTJ does not demonstrate MR ratio which is significantly higher than Al-O-based MTJ until 2004 [23]. In this work, Parkin et al. presented CoFe|MgO-MTJ of MR ratio over 200% at room temperature. The trend of increment of the MR ratio in MTJ over the years is shown in Figure 5. The highest MR ratio obtainable to date is 604% at room temperature [24].

Another point to note, the MR ratio of MTJ generally decreases with increasing magnitude of biasing voltage, but the bias dependence of STT in MTJ is still inconclusive and in research [25,26].

1.3. GMR, TMR and STT

The voltage output of GMR and MTJ structure is proportional to the MR ratio and the current density:

$$\Delta V = (k)(J)(\Delta R)(A).$$

(4)

J is the current density; ΔR is the resistance change when the magnetizations switch from parallel to antiparallel or the opposite (see section 1.1); A is the area involved that the current flows perpendicularly through it; and k is the efficiency. ΔR and A is commonly written together as the resistance change-area product (ΔRA), and always corresponds to MR ratio. Therefore, it can be seen that high MR ratio is required to have a readable voltage output. CIP-GMR, CPP-GMR and TMR devices has MR ratio in increasing order.

As the size decreases, the performance of CIP-GMR structure degrades due to edge effect, since the electrical contacts are connected to the side of the CIP-GMR structure [8,27]. CPP geometry, including CPP-GMR and MTJ structure, does not have this problem as the leads are connected on the top and bottom. This provides a much better geometry for inspection of spin injection and spin accumulation, the underlying concepts that leads to STT. Moreover, CPP geometry has higher MR ratio than CIP-GMR because averagely more electrons travel from one end to the other (refer to Figure 3) [2]. As mentioned earlier, STT, at first, is sort of a side effect of the current density when dealing GMR or TMR effect, but the manipulation of STT eventually leads to current-induced magnetization switching, which helps to solve scaling difficulties and high current write current found in magnetic random access memory (MRAM).

2. Current-induced Magnetization Switching

2.1. Overview

It is the net spin transport (also resulted spin accumulation, as discussed in section 1.1.1) found in CPP geometry that ultimately gives rise to STT. STT then becomes the fundamental principle that lies behind current-induced magnetization switching or reversal. This effect is first predicted independently by Slonczewski [28] and Berger [29] in 1996 and experimentally shown [30-32] with point contact or nanopillar geometry [10]. Various aspects of the current-induced magnetization switching and STT, including the spin precession and switching current density, are discussed here.

2.2. The process

Consider a trilayer of fixed and free FM layers separated by a NM spacer layer (Figure 6) [33]. The magnetization of the fixed layer is assumed to be pinned (in real case, it is pinned by an AFM layer) and will not be flipped by any current density. Moreover, there is an angle θ between the magnetizations of two FM layers for current switching purpose. When the incoming spin orientation is collinear with the magnetization of the FM layer (θ=0 or π), there will be no torque exerted [34]. Since spin transfer torque is crucial in switching the magnetization of the free layer, therefore non-collinearity between fixed and free layers is necessary.
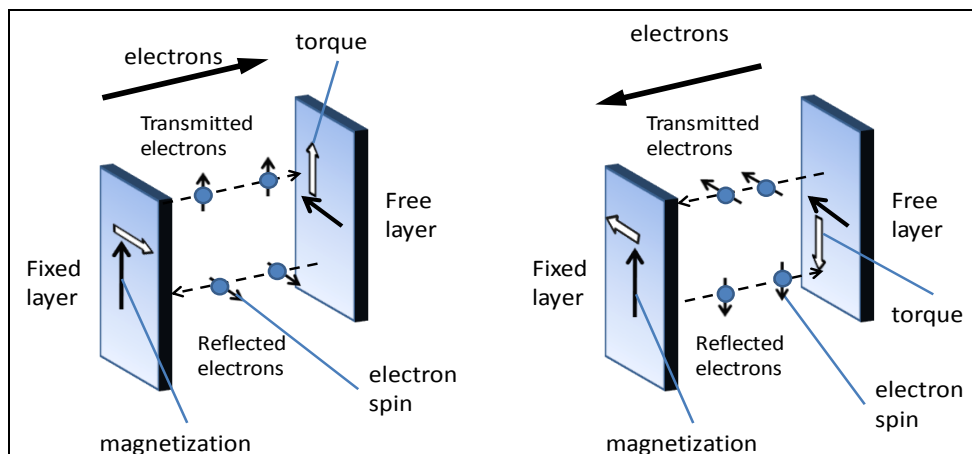
Figure 6 The direction of the magnetizations and spins of the electrons. The arrows show the direction of corresponding terms. The spacer layer is located between the fixed and free layer. The spacer layer is hidden and its thickness is exaggerated for visualization purpose.

Electrons always move in the opposite direction of the current. When current flows from the free to fixed layer, the s-band electrons [2] will be spin-polarized in the direction of the magnetization of the fixed layer. This is the first spin filtering event: majority-spin electrons, with respect to the fixed layer, are able to pass through the spacer layer. The minority-spin electrons accumulate in the FM layer.

The second spin filtering event happens in the free layer. When the electrons reach the free layer, s-d exchange interaction occurs [2]. The electrons will align themselves along the magnetization of the free layer. Therefore, the spin will start to precess around the magnetization of the free layer. Since the precession is averaged over all electrons, transverse components of spin angular momentum become zero since the electrons are out of phase [35]. Due to conservation of spin angular momentum, the transverse components of the electron spins will be absorbed and transferred to magnetization of the free layer. Therefore, the same interaction also exerts a torque on the magnetization of free layer, making the magnetization tends to align towards the magnetization of the fixed layer. This torque effect is commonly known as spin transfer torque (STT). Although the minority-spin electrons, with respect to the free layer, will be reflected back to the fixed layer, the magnetization of the fixed layer will not change because this torque is not strong enough. If the current density is high enough, that is more than critical switching current (usually around 10^7 A/cm^2), the torque applied by the spin of electrons can switch the magnetization of the free layer [34].

Similar situation happens when the electrons move from the free layer to the fixed layer with one exception. The torque exerted by the electrons that precess around the magnetization of the fixed layer are insufficient to switch the magnetization. The minority-spin electrons, with respect to the fixed layer, are reflected back to the free layer. These electrons apply torque that enough to switch the magnetization of the free layer antiparallel to the fixed layer. The strength of the torque is normally expressed as the magnitude of current density.

2.3.   Switching current density

The critical current density required to cause magnetization reversal at zero temperature using macrospin approximation is given as [8,36-38]

$$J_{c0} = \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha}{\eta}\right)(M_S t_F)\left(\pm H_{ext} + H_K + 2\pi M_S - \frac{H_{K\perp}}{2}\right)$$

(5)

or equivalently in terms of current,

$$I_{c0} = \left(\frac{2e}{\hbar}\right)\left(\frac{\alpha}{\eta}\right)(M_S A t_F)\left(\pm H_{ext} + H_K + 2\pi M_S - \frac{H_{K\perp}}{2}\right)$$

(6)

where e, α, η, M_S, t_F, A, H_{ext}, H_K, and $H_{K\perp}$ is the electron charge, damping constant, spin transfer efficiency, saturation magnetization of the free layer, thickness of the free layer, area of the free layer normal to the plane of the films, externally applied magnetic field, in-plane uniaxial anisotropy field and out-of-plane (perpendicular) anisotropy field of the free layer, respectively. The perpendicular anisotropy can be induced by interfacial anisotropy, strain field or crystalline anisotropy [36]. η is a function of current polarity, polarization, and the relative angle between fixed and free layer. The saturation magnetization arises from the demagnetizing field of the thin film geometry [39]. The $2\pi M_S$ term (around thousands of Oersteds) is large compared to the H_K term (hundreds of Oersteds) and thus becomes the dominating factor in determining the switching current density.

Equation (6) provides insight on the means to reduce the critical current density, which its motivation will be made clear in section 2.6.3. Therefore, the critical current density can be reduced by using materials with low M_S and high η [37]. For example, CoFeB with low M_S [40] and high η MgO-MTJ as described in section 1.2 is favored. Moreover, a material with a perpendicular anisotropy ($H_{K\perp}$), such as Co/Ni and Co/Pt, can be utilized to minimize the switching current density by reducing the effect of $2\pi M_S$ term [39,41]. As seen in equation (6), I_{c0} can also be reduced by making the size of the free layer smaller (A·t_F). However, reducing the area has a more significant effect since the thickness of the free layer is already on the order of few nanometers as compared to typical value of area (50 x 150 nm^2).

$$J_c = J_{c0} \left(1 - \frac{k_B T}{K_u V} \ln \frac{t_p}{\tau_0} \right)$$

(7)

At a given temperature T, the critical current decreases to the expression above. k_B, K_u, V, t_p, and τ_0 is the Boltzmann constant, anisotropic constant, activation volume of free layer, current pulse width, and inverse of the attempt frequency (typical around 1 ns), respectively [7,37,40]. For a 10-year thermal stability, $K_u V$ must be over 40 times of $k_B T$ [40].

Reported by Diao et al. [37], the average critical current density for an AlO_x-MTJ is about 6×10^6 A/cm^2 (MR ratio= 45%, cell size= 127 nm × 148 nm, pulse width= 30 ms, room temperature). For a MgO–MTJ, the critical switching current density is reduced to 2.2×10^6 A/cm^2 (MR ratio=155%, cell size= 125 nm x 220 nm). The critical current density can be further reduced by structural modification. For example, a dual MTJ configuration, with two MgO barriers, can have critical switching current density as low as 1.1×10^6 A/cm^2.

If the electrons flow from the free to fixed layer, approximately 50% higher critical current is needed to switch the magnetization [8]. This is because when the electrons move from free to fixed layer, the magnetization switching is obtained by the reflection of minority-spin electrons, as opposed to the case when the electrons travel from fixed to free layer, which the magnetization switching is induced by direct spin transfer of the majority-spin electrons. This can be overcome by using a dual MTJ configuration.
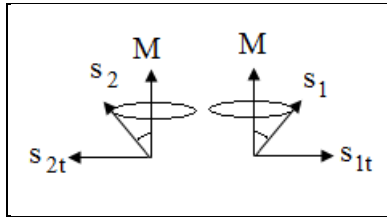
2.4.   Precession of spin around local magnetization

Provided the spin orientation is non-collinear with the magnetization of free layer, the spin of electrons will try to align with this local magnetization by precessing around it when the electrons move through the free layer (Figure 7). In FM materials, the exchange interaction is strong, and it causes the electrons to move a few atomic lengths for one period of precession. The FM layer discussed here is typically ten times the atomic length, thus the electrons will be out of phase. Since the electrons have different initial conditions, transverse components of spin angular momentum of all electrons average to zero [25,33]. The energy loss in this process can be described by the Landau-

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Lifshitz-Gilbert equation (see equation (8)) [34]. As described earlier, this loss of spin angular momentum will be absorbed by the magnetization of the free layer due to conservation of angular momentum and causes the magnetization to precess around the moment of spin. This is the initial step for complete magnetization reversal of the free layer.

$$\frac{\partial \mathbf{M}}{\partial t} = -\gamma \mathbf{M} \times \mathbf{H_{eff}} + \frac{\alpha}{\mathbf{M_s}} \mathbf{M} \times \frac{\partial \mathbf{M}}{\partial t}$$

(8)

Figure 7 Two different electrons with spin s₁ and s₂ that precess around the local magnetization M. In this example, both precessions are out of phase by π. The subscript t indicates the transverse component of the spin.

Consider the case for magnetic reversal of free magnetic layer with magnetization antiparallel to the fixed magnetic layer, and the current is applied such that STT acts against magnetic damping (Figure 8) [34]. The magnitude of STT depends on the magnitude of the current density applied. If the current density is small, the magnetization of the free layer spirals back to the direction of the magnetization of the fixed layer due to magnetic damping [34]. (The magnetization of the fixed layer can be regarded as the moment of the spin since the electrons are spin-polarized by the fixed layer.) However, if the current density exceeds a certain critical value, the magnetic damping becomes negative and the magnetization of the free layer spirals away from the fixed layer. In such case, two possible scenarios might result. The first possibility, if the magnetic damping increases with the precession angle faster than the STT, stable precession will proceed. For the second possibility, the precession angle will keep increasing and the magnetization will ultimately reverse or switch. Although the above discussion is done without magnetic anisotropic, it still hold true for thin film geometry, as in the case of GMR or MTJ.
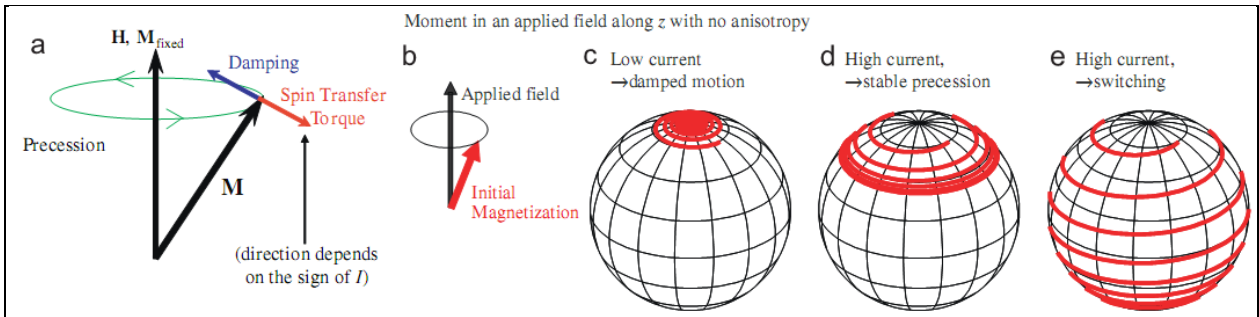
Figure 8 (a) Direction of STT, damping, M (magnetization of free layer), and M$_{fixed}$ (magnetization of fixed layer, along z-direction). (b) Magnetic configuration for case c to e. (c) M spirals back to z-direction. (d) Stable precession. (e) Magnetization reversal. Adapted from [34].

2.5.   Switching speed

The switching speed depends on the duration and amplitude of the current pulse [8]. If the current density J>J$_{c0}$, complete magnetization reversal by precessional switching occurs as discussed in section 2.4 [37]. The switching speed corresponding to this operation mode is around 5-20 ns at room temperature [8]. If J<J$_{c0}$, the magnetization still can be reversed by assistance of thermal excitations but the switching speed is slow. Therefore, there is tradeoff between switching speed and magnitude of current density.

In summary, the magnetization switching is a thermally activated process for long current pulse, whereas precessional switching occurs for very short current pulse (Figure 9) [37]. In between these two regions, there is an intermediate region called dynamic reversal. This region corresponds to the operating speed of a practical STT-RAM (3-10 ns [40]).
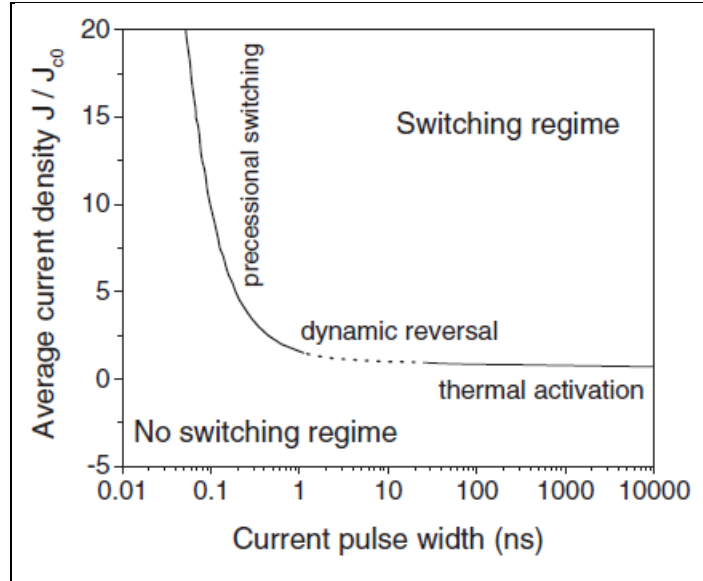
Figure 9 Three switching modes: thermal activation, dynamic reversal, and precessional switching. The parameters are taken as α = 0.02, H$_K$ = 500 Oe and 4πM$_S$ = 18 kOe. Taken from [37].
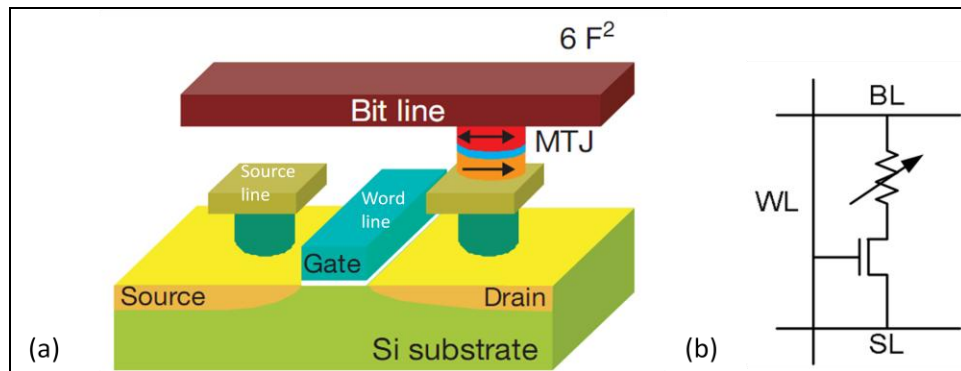
2.6.   STT-RAM

Although there is another form of STT based memory device, namely racetrack memory [42], which utilizes the movement of domain wall induced by STT, STT-RAM is closer to commercialization and more mature in terms of research work done. STT-RAM not only has the same advantages as MRAM, which is fast write and read time (in order of tens of nanoseconds), unlimited endurance, non-volatility, low power and high tolerance to radiation and operational temperature [10,43], it also has added value of ease of scaling down and smaller write current as compared to MRAM (more in section 3.6.1).

Let us first compare the two CPP geometries. CPP-GMR structure can reach a high current density required for STT easier than MTJ, due to the low resistance in metallic layer. On the other hand, MTJ has higher MR ratio and can have much better impedance matching (higher resistance, several kΩ [44]) with the complementary metal oxide semiconductor (CMOS) electronics [34]. This compatibility allows fast sensing and reading of MTJ by the CMOS circuitry [8,44]. Therefore, it is often to see that STT-RAMs nowadays are based on MgO-MTJ (highest MR ratio, see section 1.2) as the magnetic element, which is the unit for storing information. In the following sections, the basic design of STT-

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RAM memory cell, the writing and reading mechanism, and the restriction on CMOS circuitry will be discussed.

## 2.6.1. Basic design of STT-RAM

Figure 10 (a) Basic structure of a STT-RAM cell (b) The equivalent schematic diagram. Adapted from [45,46].

The basic structure for a typical STT-RAM memory cell is depicted in Figure 10 (a). It has one transistor (NMOS transistor [47]) connected in series with the MTJ; interconnects connected to the MTJ (bit line); interconnects of the source of transistor (source line); and interconnects of the gate (word line) [45]. One memory cell corresponds to one bit; multiple cell arrays construct a memory storage device. End-tapered and elongated shape MgO-MTJs are the most widely used memory element in STT-RAM [7]; however, a practical MTJ is more complicated, that is it has more layers, than shown in Figure 10 (a). The transistor is used to provide the switching current density to the MTJ and used to select (address) a particular memory cell [7,8,48]. A memory device that is based on STT effect is of random access type, thus it is normally referred as STT-RAM (also known as spin-RAM, SpRAM, and so on). In STT-RAM, the current density is the crucial parameter for writing a bit, not current [8].

2.6.2. Read and write mechanisms

The reading mechanism of STT-RAM is similar to GMR or TMR effect. Parallel magnetizations configuration has lower resistance, and thus a lower voltage output (voltage is proportional to resistance), corresponding to a '0' state (Figure 11). Antiparallel configuration has higher resistance or voltage output, giving a '1' state. During the read operation, the word line is selected and a voltage is applied to the bit line such that a current density of magnitude less than the switching current density is supplied.
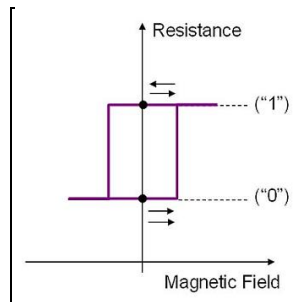
Figure 11 Schematic drawing of memory states in STT-RAM. The arrows represent the relative orientation of the magnetizations of the fixed and free layers. Taken from [7].

The writing mechanism in STT-RAM follows the current-induced magnetization switching as discussed in section 2.2. Consider the case when a current density larger than the critical current density flows from the free to fixed layer (electrons in opposite direction, Figure 12). The spin of the electrons will reverse the magnetization of the free layer, making it parallel with the magnetization of the fixed layer. This is a '0' state because parallel magnetization has low resistance. If the current flows from the fixed to free layer, the magnetizations will be antiparallel. This corresponds to a '1' state. '1' and '0' constitutes the binary states for storing information. During the write operation, a bit is selected by selecting the word line. Then, either the bit line or the source line of a selected column is positively biased [48]. The magnetization of the free layer can be made either parallel or antiparallel, with respect to the fixed layer, by changing the current direction: either from source line to bit line or vice versa.
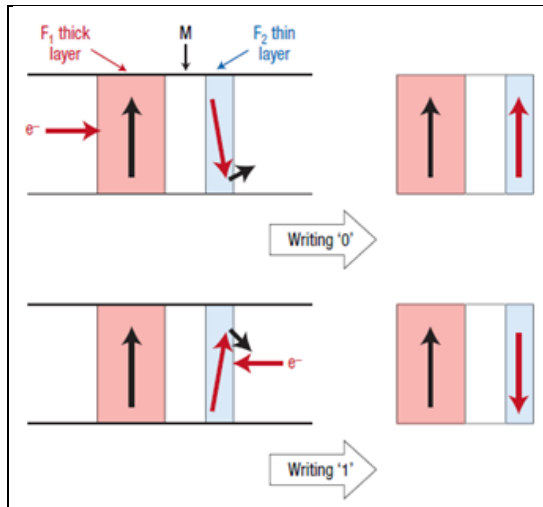
Figure 12 Writing '1' and '0' in STT-RAM. F_1 and F_2 are the fixed and free layer, respectively. Taken from [2].

2.6.3. Cell size and limitation of CMOS transistor
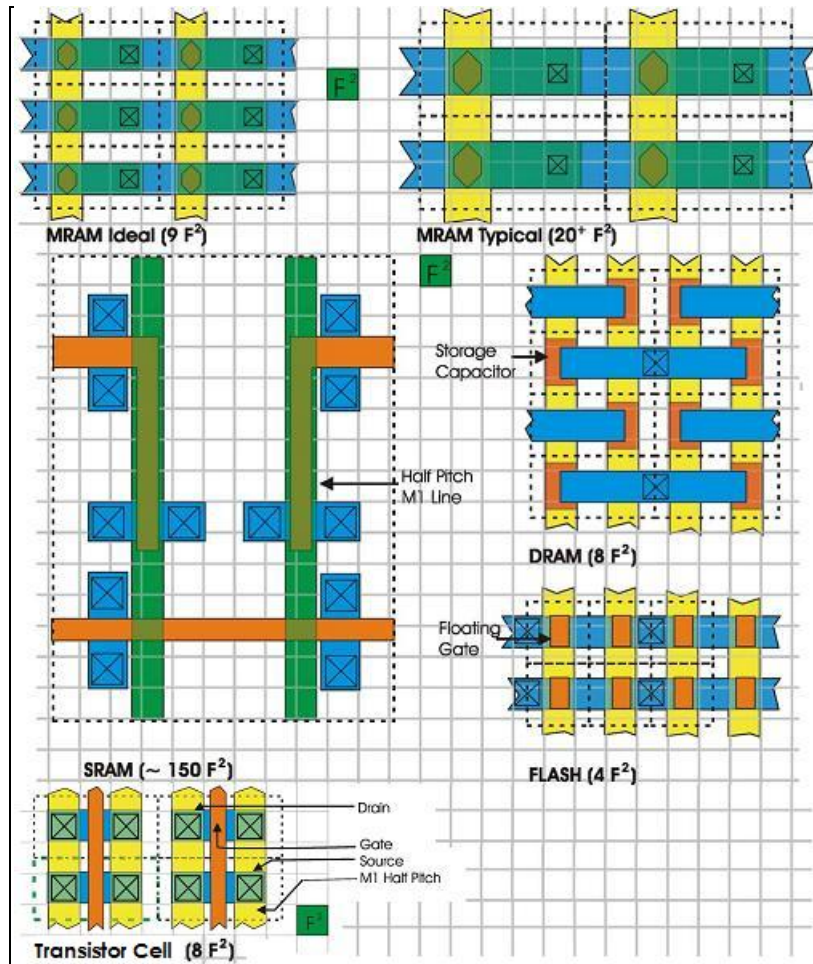
Figure 13 Cell size for different memory technologies, including transistor cell. Adapted from [49].

Since this thesis focuses on a memory technology, it is inevitably that the term "memory cell size" will be often repeated throughout the thesis. Therefore, it is good to have a pictorial idea about memory design. Figure 13 shows the memory cell size for various memory technologies. A typical transistor cell occupies an area of $8F^2$, where F is the minimum lithographic feature size used in the fabrication [49]. SRAM has the largest cell size among the mature memory technologies while flash cell size is the smallest. MRAM has memory cell consists of one MTJ and one transistor; the transistor sets the minimum cell size of MRAM to $8F^2$. In fact, most MTJ has cylindrical shape and have a typical cell size of $20F^2$ to $30F^2$ to accommodate this variation. Figure 14 shows how the memory cell size has evolves over the years.

Figure 14 Memory cell size over the years. Adapted from [49].

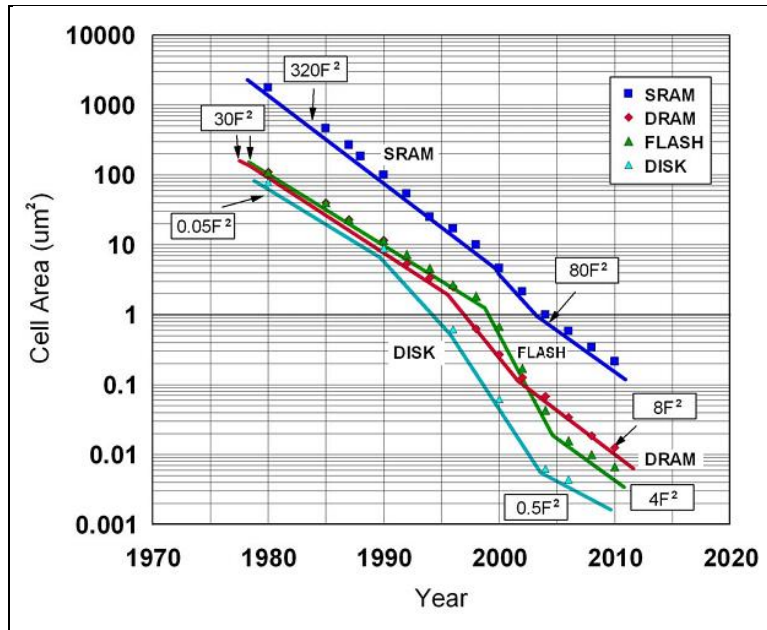The transistors in STT-RAM are provided by the CMOS wafer and are used to drive the MTJ. Careful selection of the gate width of the transistors is needed because the minimum STT-RAM cell size is set by the transistor, similar to the MRAM memory cell as discussed previously. According to ITRS 2007 edition [50], the saturation current of the transistor is about 500 μA/μm (transistors used for high performance logic can reach until 1 mA/μm but low power is preferred for memory applications). Therefore, a MTJ with area of 50 x 100 nm^2 needs a typical switching current density of $4x10^6$ A/cm^2. This translates to a gate width of 400 nm. It can be seen that the gate width is four times the largest dimension of MTJ, which means the memory cell size is limited by transistor size instead of the magnetic element (MTJ). This eventually increases the cell size and thus the cost per bit. Even with switching current density of 10^6 A/cm^2, a gate width of 100 nm is still needed. Therefore, the motivation of reducing the critical switching current to less than 10^6 A/cm^2 is to reduce the transistor size. The ultimate goal of STT-RAM is to achieve switching current density 0.5×10^6 A/cm^2 [46]. However, there is no great improvement on reducing the switching current density in recent years as the lowest current density reported is still similar to what we had in year 2005 (2×10^6 to 3×10^6 A/cm^2 [40]). Depending on the operating mode of the transistor, different saturation current could be obtained, but all still depending on the ratio of gate width to gate length [45].

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On the other hand, the voltage across MTJ is either limited by the voltage provided by CMOS circuitry (MOS transistor) or the breakdown voltage of the MTJ itself (Figure 15). Similar to the treatment of ΔV in section 1.3, the voltage across the MTJ is proportional to the resistance-area (RA) product, and thus current will be inversely proportional to the RA product. Therefore, a lower RA product is desired. Typical RA values are 1 $\Omega \cdot \mu m^2$ and 0.1 $\Omega \cdot \mu m^2$ for MTJ and CPP-GMR, respectively. RA product is different from ΔRA, as R is the overall resistance of the multilayer structure. However, it could not be too low, as the MR ratio will reduce [7] and it is limited by impedance matching issue as mentioned earlier.
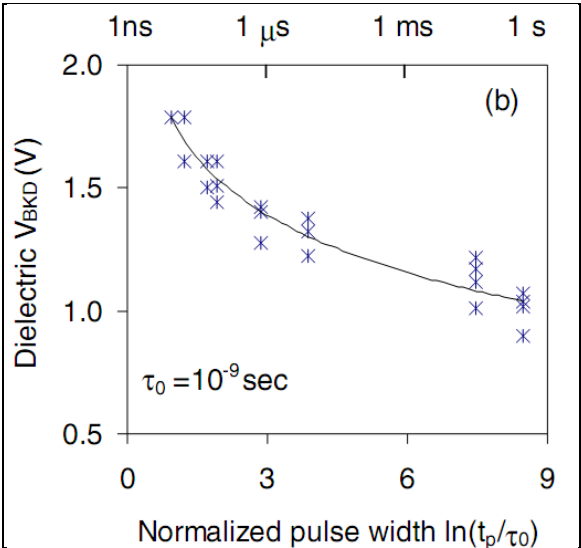

Figure 15 Breakdown characteristic of MgO-MTJ as function of current pulse width. Taken from [37].

PART II   THE BUSINESS

3.   Market Analysis

In the second part, a market survey on different memory technologies is done. The advantages and shortcomings of these technologies will be explored according to their categories. Next, the potential applications and markets of STT-RAM are overviewed. Before implementing a new technology, an evaluation of patents of prior art is a must. From the patents and literatures, the fabrication process can be estimated and further used as the basis for cost modeling. The purpose of cost modeling is to provide insight into the price and cost of STT-RAM. From the consideration of cost and the technological aspects of STT-RAM, suitable business plan can be deployed or put a hold on to venturing further into the field.

3.1.   Overview

A typical processor in personal computer can easily achieve operation speed up to 3 GHz to date. This translates to speed of less than 1 ns but it is hard to achieve such fast operation speed with a large-capacity memory [51]. Memory hierarchy provides a workaround solution to this problem (Figure 16). A small-capacity and fast memory deals with the data that the processor needs frequently, whereas large-capacity memory stores the total program. For example, in a computer, level 1 (L1) cache is SRAM and located on the same chip as the processor. L1 cache typically has capacity of few tens of kilobytes but have access time of less than 10 ns. DRAM is at lower hierarchy and thus has a higher capacity, a few GB, but it is slower. For the above reason, different memory technologies have their shares in the market to cater different needs. The most prominent ones are SRAM, DRAM, and flash. If a universal memory exists to replace different memories in the memory hierarchy system, this will result in a very lucrative business. Many researchers and memory makers like to compare FeRAM, PCRAM, and STT-RAM, with some refer STT-RAM as a variant of MRAM, as a candidate for universal memory.
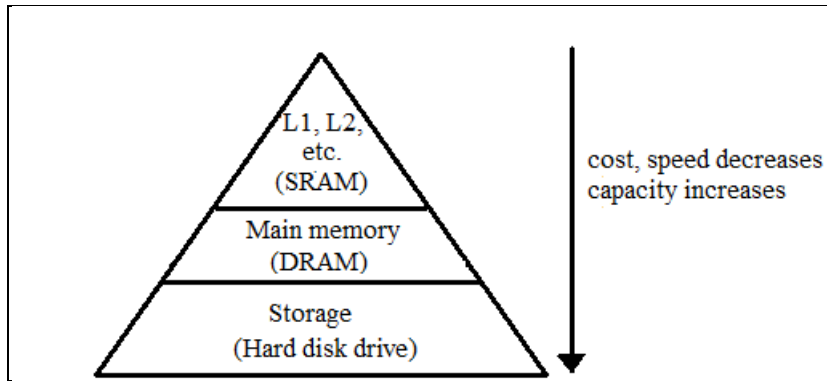
Figure 16 Schematic representation of the memory hierarchy.

3.2. Comparison of memory technologies

There are many memory technologies that are either existing in the market (DRAM, SRAM and flash), available in small market (FeRAM [6,52] and MRAM [53]), in advanced research and development stage (PCRAM and STT-RAM), or still in embryonic research state (RRAM, racetrack). The typical performance and fabrication parameters of these memory technologies except the embryonic ones are presented in Table 1. There are few properties that are important for memories: non-volatility (does not need constant refresh or continuous power supply for keeping information); density (relates to memory cell size and ultimately cost of production); speed (reading and writing time); endurance (must be at least 10^{15} cycles); and reading and writing current (energy needed for reading and writing).

	Standalone								Embedded		
	SRAM	DRAM	NOR Flash	NAND Flash	MRAM	STT-RAM	PCRAM	FeRAM	eSRAM	eDRAM	eNOR
Cell Size (F^2)	80-120	6	6-11	4	25-40	8-25	4-4.8	16-22	100	16	50
Bits/Cell	1	1	2-4	2-3	1	1	1-2	1			
Access time (ns)	2-100	6-40	70	10^4	3-30	10-20	50	50			
Write time (ns)	2-100	6-40	2.5×10^4	10^5	3-30	3-30	100	50			
Write/Erase current (μA)	1	100	10^3	10^4	$>10^3$	>100					
Write energy/bit (pJ)	2	2	160	65	50	2	100	2	Same as standalone specifications.		
Read endurance	10^{15}	10^{15}	10^{15}	10^{15}	10^{15}	10^{15}	10^{15}	10^8-10^{14}			
Write endurance	10^{15}	10^{15}	10^5	10^5	10^{15}	10^{15}	10^{12}	10^8-10^{14}			
Volatility (Data retention in years)	V	V	NV (10-20)	NV (5-20)	NV (>10)	NV (>10)	NV (>10)	NV (10)			
Standby current (μA)	20	100	0	0	0	0	0	0			
Compatibility										eSRAM	eSRAM
Additional masks	0/1	5/8	4/6	N/A	3	3	2-4	2-4	0/1	5/8	11

Table 1 Comparison among memory technologies. F is the minimum metal line width in the memory cell (also referred as minimum feature size); V and NV means volatile and non-volatile, respectively. Adapted from [43,50,54].

STT-RAM has the advantages of non-volatile, theoretically unlimited endurance, fast, high density, and low read and write energy requirement. The immediate rival technologies of STT-RAM are PCRAM and FeRAM. However, these two technologies also have their disadvantages, which will be discussed later. The focus of this assessment will focus on competitiveness of STT-RAM, in terms of cost and density, compared to the other technologies, especially existing ones. This is essential since the acceptance of a new technology in a specific market mostly depends on the price, unless the technology brings significant impact in changing human behavior. This is not the case for a new

memory technology, at least for now. There are also demand to replace the existing memories because the scalability difficulties beyond 30 nm for DRAM and flash memories [55].

3.3. Existing memory technologies

3.3.1. Static RAM (SRAM)
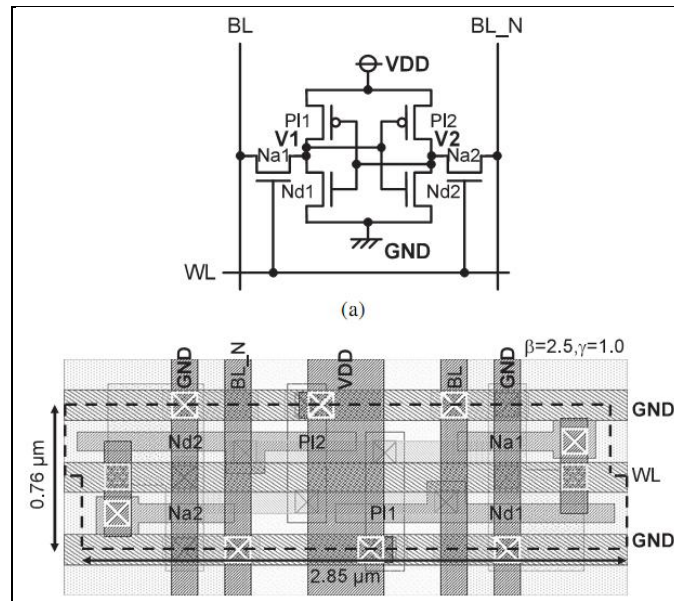
Figure 17 (a) Schematic layout of a typical 6T-SRAM memory cell. (b) Actual layout of SRAM using 90 nm design rule. Pl1 and Pl2 are load transistors, Na1 and Na2 are access transistor, Nd1 and Nd2 are driver transistor. WL and BL are word line and bit line, respectively; VDD is the voltage supplied to SRAM. Taken from [56].

The most conventional design for SRAM incorporates six transistors (Figure 17) [56]. The load and driver transistors form a pair of inverters and are cross-coupled, which means one of the output of the inverters is the input of another. These four transistors could hold stable data states of '1' or '0', which is the basic of information storage in memory. During the read operation, both bit lines are pre-charge to logical '1' and the word line is then turn on [51]. If the bit (charge) is stored at V1 ("0" at V2, see Figure 17), BL_N will discharge through Na2 but BL will stay high. For write operation, the desired state is written by charging both the bit lines to the desired state ('0' or '1'). The write operation is complete after the word line is turned on. When the word line is not turned on, a sufficient voltage is required to switch on the inverters, such that the inverters could hold the states at differential voltage levels. This is specified as the standby current. Therefore, the standby current

(20 µA) plays a more important role than the write current (1 µA) when it comes to consideration of power consumption. Performance wise, SRAM is the fastest memory of all memory available [46]. However, it requires continuous power supply for data retention, that is volatile, and it has very low density, due to the relative large cell size. Since density relates directly to cost, therefore SRAM has a very high cost per bit. As the transistor dimensions scale-down, the leakage current increases and thus increases the standby power consumption.

3.3.2. Dynamic RAM (DRAM)

DRAM uses single transistor-capacitor pair (1T1C) to store one bit (Figure 18) [57]. The capacitor stores the charge which defines the data states and the transistor controls the access to the capacitor [51]. To write to DRAM memory cell, the bit lines are either charged with a logical state '1' or '0' and then the state is transferred to the capacitor, by either charging or discharging [58]. On the other hand, for read operation, the bit lines are charged to midway between the high ('1') and low voltage ('0') level [57]. After the transistor is turned on by putting high voltage on word lines, the capacitors connect to the bit lines. The sense amplifiers are used to detect the change on bit lines induced by the discharging of the capacitor. Eventually, the bit lines will be pulled towards '1' or '0' logical level, depending on the initial state of the capacitor. The reading process is destructive since discharging of capacitor is involved [59]. Therefore a refresh process follows after readout. Moreover, the charge in the capacitor will eventually disappear and needs constant refresh to maintain the data state. DRAM performs fairly well in terms of cell size ($6F^2$) and speed (in the range of tens of nanoseconds). However, it is volatile and needs a periodic refresh current [46].
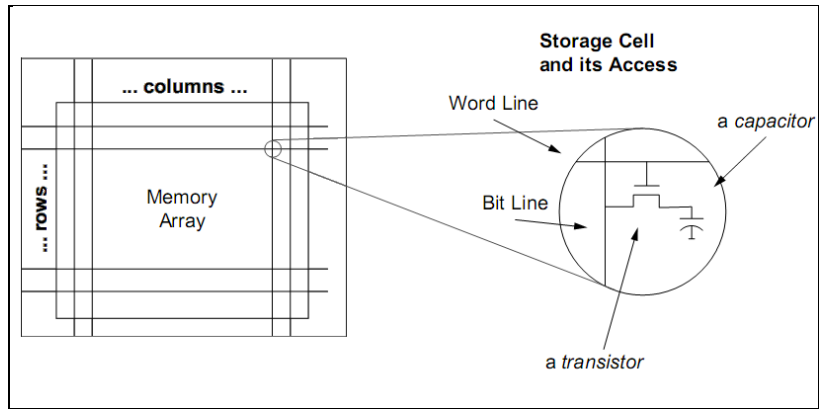
Figure 18 : A schematic drawing of the memory cell of DRAM. Adapted from [57].

3.3.3. Flash memory
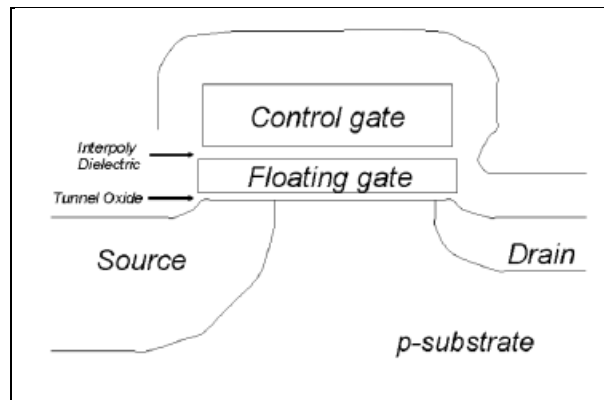
Figure 19 Schematic drawing of a flash memory cell. Taken from [60].

Flash memory cell uses one floating gate transistor. The presence (absence) of charge in the floating gate shifts (restores) the threshold voltage of the transistor, allowing it to have two states [6]. The one-transistor configuration allows flash to have the highest density and even achieves multi bits per cell. Multi bits technology reduces the effective cell size, which mean a smaller cell size per bit.

There are two types of flash memory architecture in industry standard: NOR and NAND flash [60]. The NOR flash has faster access but larger cell size, and thus used majorly for code storage, whereas NAND flash is mainly used for data storage since it has longer access and higher programming voltage [61]. Each cell in NOR configuration is directly connected to word lines and bit lines of the memory

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array, while NAND memory are arranged in series within a small block [6]. Therefore, NAND flash is not truly random access [62]. In NOR flash, programming (writing) is done using channel hot electron injection (CHEI). High voltage, 4 to 6 V and 8 to 11 V, is biased to the drain and the gate, respectively while source is grounded. Hot electrons flow in the cell and have sufficient energy to tunnel across the oxide layer into the floating gate. The speed of writing using the mechanism is on the order of microseconds or more.

On the contrary, Fowler-Nordheim (FN) tunneling is used to program a NAND flash. Voltage of about 20 V is applied to the gate while source and drain are grounded. Although FN programming is slower than CHEI programming, FN tunneling allows many cells to be written at once since the energy requirement of FN tunneling is very small (<1 nA). The erasing procedure in both NAND and NOR flash uses FN tunneling. A negative voltage is applied to the gate and the voltage pushes out the electrons. The read time for NAND flash (25 μs) is slower than NOR flash since NAND is read block-by-block [6].

Flash memory has slow write speed and low endurance (10^5 write cycles). It also requires the internal voltage of at least 10 volts for write operations [46], consuming high write energy. Besides the intrinsic disadvantages, flash also encounter difficulties when scaling down to 30 nm [4]. NAND flash suffers from several issues. Capacitive coupling between floating gates will occur if word line shrinks to 40 nm or less [4,6]. This will create unwanted interference and disturbs the memory cell threshold voltage. Reducing the thickness of the floating gate can overcome this problem but it leads to loss of coupling between floating gate and control gate (Figure 19). The solution could be implementation of high k interpoly dielectrics. The reduction in number of electrons also causes the threshold voltage to be easily disturbed [4]. All these issues suggest a replacement of flash is needed quickly.
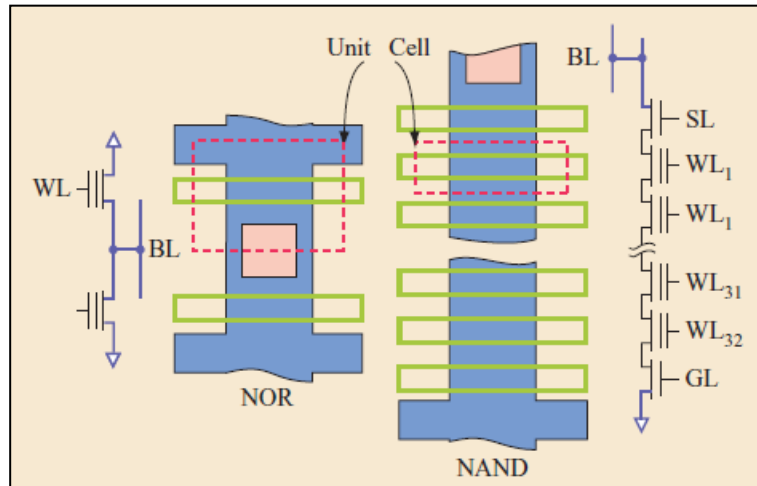
Figure 20 Schematic circuit layout of NOR and NAND flash memory cell (BL – bit line; GL – ground select line; SL – select line; and WL – word line.) Taken from [6].

3.4. New memory products
3.4.1. Ferroelectric RAM (FeRAM)

Similar to DRAM, the memory cell of FeRAM contains one transistor and one capacitor (1T1C), except the capacitor is made of ferroelectric material (Figure 21). A ferroelectric capacitor is created by sandwiching ferroelectric material, such as $Pb(Zr_xTi_{1-x})O$ (PZT); $SrBi_2Ta_2O_9$ (SBT); or $Bi_{4-x}LA_xTi_3O_{12}$ (BLT), between two metal electrodes (Figure 22) [6,51]. The two data states at zero voltage are result from electrical hysteresis behavior of ferroelectric material, the electric equivalent of ferromagnetic material (Figure 23). The two polarization states in a ferroelectric capacitor can be visualized as charges accumulate at either side of a normal capacitor plate.
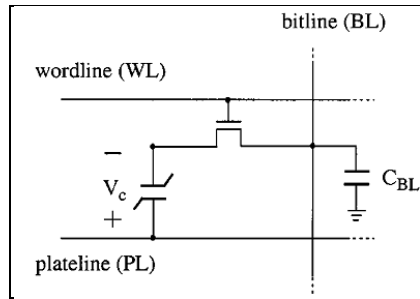
Figure 21 Schematic drawing of the FeRAM memory cell incorporating one transistor and one ferroelectric capacitor with V_c. C_{BL} is the parasitic capacitance of the bit line. Taken from [63].

The read operation of FeRAM is destructive. During the read operation, a word line is selected to switch on the transistor, allowing the capacitor to connect to the bit line [62,63]. Regardless of the initial state of the ferroelectric capacitor, a voltage is then applied to the plate line. If the capacitor switches, that is one polarization state changes to another, an extra switching charges flows to the bit line. Therefore, the bit line will give different voltage level depending on the initial state of the ferroelectric capacitor. The differentiation of '1' and '0' is done by sense amplifiers similar in DRAM case. For writing, the bit line is driven to a logical '1' state (V_{DD}) to write '1' to the memory cell. Otherwise, the bit line is driven to 0 V to write '0' state [63]. A shorter voltage pulse is applied to the plate line during this writing operation. This reading and writing mechanism leads to low endurance of FeRAM ($<10^{15}$ cycles). The write current needed depends on the voltage needed to switch the electric polarization state.

FeRAM have been around for sometime but still suffer from scalability issue [61]. Despite many years of effort, FeRAM cell size ($16F^2$) still remain larger than DRAM and NAND flash cell size [6,51]. There are also fatigue, imprint, and retention issues in FeRAM that addresses reduction of remnant polarization with each read or write cycle, preference to continue staying at one polarization state, and loss of polarization over time, respectively [6]. FeRAM also possesses some processing difficulties, such as as high processing temperature and degradation by presence of hydrogen. Nevertheless, FeRAM have been used for embedded application since its cell size is comparable to other embedded memory technologies and have better performance in terms of write endurance (compared to embedded NOR) and non-volatility (compared to embedded DRAM and SRAM) [6,51]. FeRAM also find its place in radiation resistance application, such as aerospace industry [4].
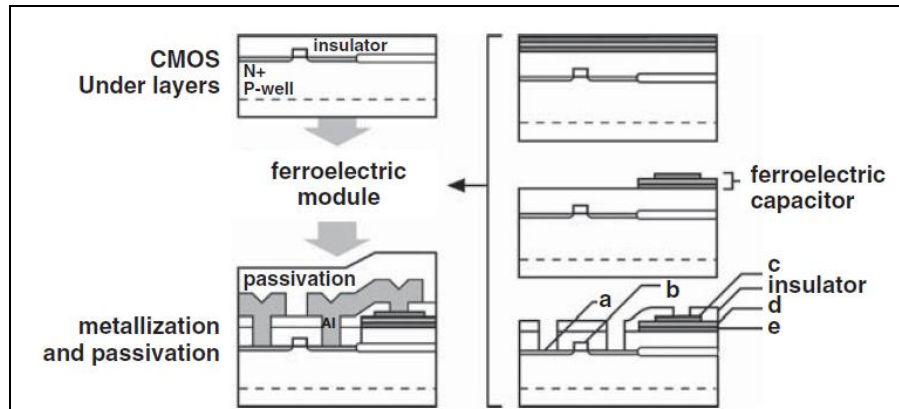
Figure 22 Typical integration of ferroelectric capacitor into the CMOS process. (a – bit line, b – gate of the pass transistor; the ferroelectric capacitor comprises of: c – top electrode, d- ferroelectric material, and e – bottom electrode). Taken from [62].
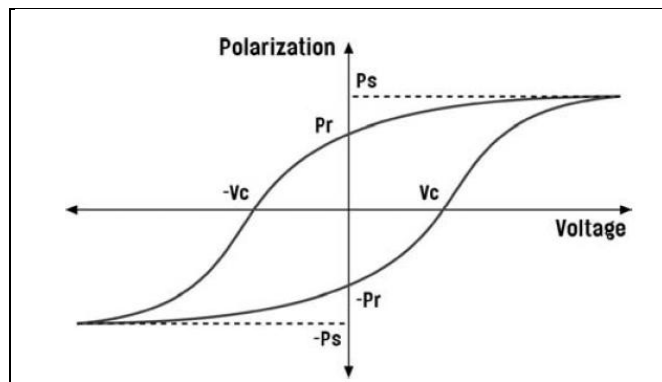
Figure 23 Hysteresis loop for a ferroelectric material: polarization (charge) versus voltage. Ps is the saturation polarization, Pr is the remnant polarization and Vc is the coercive voltage. Taken from [62].

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3.5.   Memories in development
3.5.1.   Phase Change RAM (PCRAM)
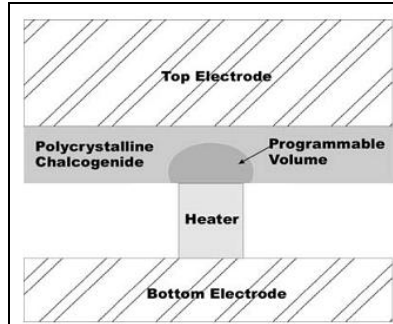
Figure 24 Cross section of a simplified PCRAM memory cell. Taken from [64].

PCRAM basically is a one transistor and one resistor (1T1R) technology. The resistor is a material that can switch between an amorphous phase and a crystalline phase in a thermally induced reversible process [4]. In crystalline state, the material has much lower resistance as compared to amorphous state. This large resistance difference easily allows PCRAM to operate in multi bits [6]. This material is normally chalcogenide alloys and the most commonly used one is $Ge_2Sb_2Te_5$ (GST) due to its large amorphous to crystalline resistance ratio and fast crystallization speed [65].The SET operation involves heating of material below the melting temperature (or above the melting temperature and then allow slow cooling down) until the material is fully crystallize [6]. This operation determines the write speed of PCRAM [6] because it is the slowest process and it ranges from 50 to 150 ns [65]. On the other hand, large electrical current is applied for tens of nanoseconds and cut off rapidly (less than a few nanoseconds) to quench the phase change material to amorphous phase in the RESET operation [6,65]. The RESET operation determines the current or power requirement since the melting temperature is much higher than crystallization temperature (Figure 25).

Since larger access devices (transistors) are needed to supply higher RESET current, many efforts are focus on reducing the RESET current to minimize the overall cell size [65]. This either requires one of the dimensions of PCRAM to be scaled less than the current lithography capability [65] or reducing the contact area between phase change material and the heater [62]. The focus is on the latter and there is no inherent limitation in future scaling down, at least to the extent of thermal proximity effect is not an issue [65]. However, write endurance is the biggest problem in PCRAM. After a number of cycles of phase switching (10^{12}), the PCRAM fails [65]. The failures include physical

disconnection of phase change material from the electrodes and occurrence of phase segregation in the phase change material. Phase segregation could cause resistance level drift and hard-to-form amorphous state. Despite the limitations, PCRAM holds good aspect in scaling and it is also radiation hard [4].
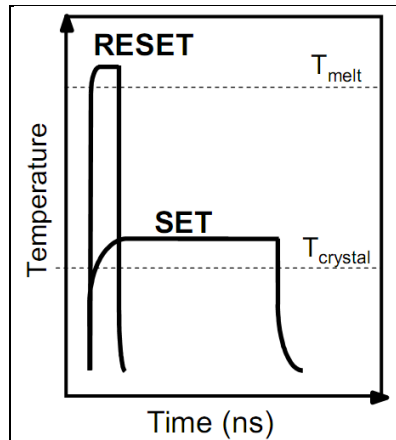
Figure 25 Temperature profile needed to change the phase of PCRAM. Taken from [65].

3.5.2.   Other memory technologies

Resistive RAM (RRAM) relates to manipulation of resistance change at different voltage level [6]. Materials such as NiO and TiO_x form a conductive oxygen vacancy or defect path when an electric field is applied. On the other hand, conductive bridge RAM (CBRAM; programmable metallization cell (PMC); or solid electrolyte) involves growth of conductive filament by means of oxidizing metal ions in the electrolytes between two metal electrodes. Polymeric or organic semiconductors are used in organic memories, whereas racetrack memory utilizes the movement of magnetic domain wall by STT effect [6]. There are also improvements on the existing technologies, such as silicon-oxide-nitride-oxide-silicon (SONOS) and nanocrystal, to promote better charge trapping in flash devices. In conclusion, there are many memory technologies that are either in research or development. The discussion of competing technology is limited to those which have in state of advanced development, with at least a prototype available in the literature.

3.6. Magnetic Memories

3.6.1. Magnetic RAM (MRAM)
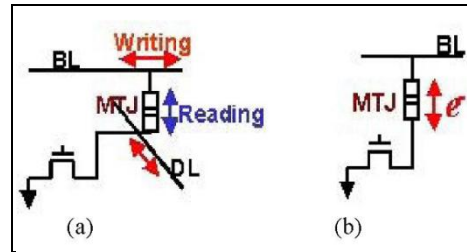
Figure 26 Schematic drawing of (a) MRAM memory cell and (b) STT-RAM memory cell. Taken from [66].

In this thesis, MRAM refers to field-induced magnetization switching magnetic memory, as opposed to current-induced switching in STT-RAM. Similar to STT-RAM, a typical MRAM memory cell consists of a MTJ (specifically MgO-MTJ) and a transistor (Figure 26). The read operation is similar to STT-RAM, a current passes through the MTJ and the resultant resistivity level is measured. For the write mechanism, one current passes through the bit line (I_{Easy}) while another current (I_{Hard}) flows through the digit line (some refers it as word line [7]). A large current will induce a high magnetic field. The combination of these two magnetic fields will able to switch the magnetization of the free layer (Figure 27). The limitations of MTJ-MRAM include high write current, half-select issue, shape dependence of magnetic element (MTJ), and large cell size [4]. First of all, the requirement of two conducting lines, to induce magnetic fields, increases the overall memory cell size. Besides that, the shape variation of the magnetic element (MTJ) can result in formation of multiple domains and distort the switching field threshold [67]. At high density, the magnetic field can perturb adjacent cell to switch undesirably and causes half-select issue [6]. This problem is solved using toggle mode MRAM, which its free layer is replaced by synthetic antiferromagnetic (SAF) structure [7]. SAF structure consists of two ferromagnetic layer antiferromagnetically coupled through a thin NM spacer layer, which is usually Ruthenium (Ru) [68]. However, even with toggle MRAM, large write current is needed to switch magnetization (on order of 10 mA). Scaling down actually increases the write current needed. Moreover, since resistance also increases with smaller area, ohmic loss will dominate the power consumption. On the good side, MRAM is fast, non-volatile, has infinite endurance, and also radiation resistant [4,7]. The appearance of STT-RAM revives the promises of MRAM since the switching current in STT-RAM reduces when the technology scales down [6]. This is due to the switching parameter in STT-RAM is determined by switching current density rather than

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switching current. Nevertheless, despite the difference in the underlying physics, STT-RAM is often regarded as one of the variants of MRAM because both MRAM and STT-RAM are magnetic memories and have similar design.
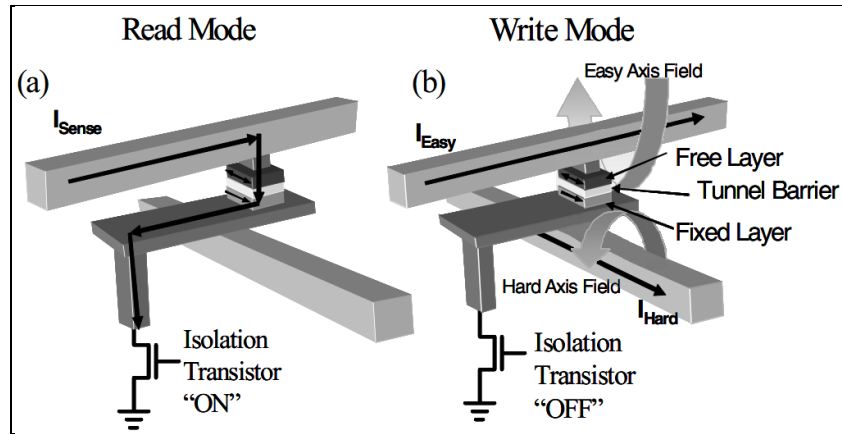
Figure 27 Read and write operation of a MTJ MRAM. Adapted from [69].

3.6.2.   Spin Transfer Torque RAM (STT-RAM)

The details of STT-RAM are discussed in section 2.6. To date, there are two publicly announced prototypes of STT-RAM memory chip, which are demonstrated by Sony and Hitachi [48,70]. The highest density reported is the 2 Mb memory chip from Hitachi (Figure 28), manufactured using 0.2 µm CMOS logic process and uses a write current of 200 µA. It has a cell size and chip size of 1.6 x 1.6 μm^2 and 5.32 x 2.50 mm^2, respectively. This prototype also confirmed 10^9 endurance cycles with no degradation [71].

Process	0.2 um CMOS
Power Supply	1.8 V
Memory Cell size	1.6 um x 1.6 um
Write	200 uA/cell, 100ns
Read	40 ns
Chip Module size	5.32 mm x 2.50 mm
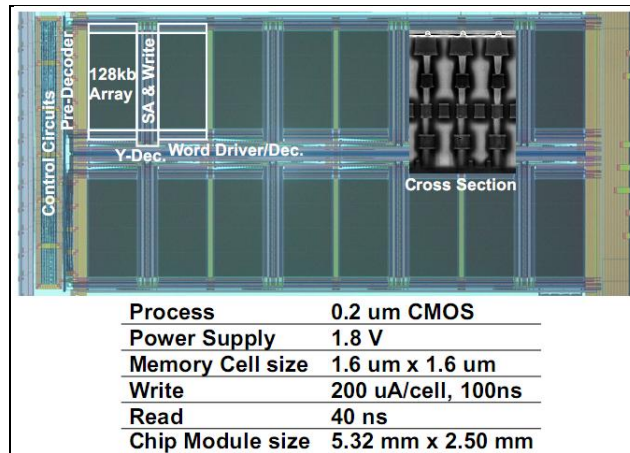
Figure 28 2Mb SPRAM by Hitachi. Taken from [72].

3.7. Application

One of the motivations in developing STT-based device is to reduce the high switching current needed in MRAM. Therefore, the applications of STT effect are very closely related to the field of memory. Since STT-RAM has similar working principles as MRAM, all the applications of MRAM can be equally well catered using STT-RAM, but with a higher density (translates to lower cost). Despite the obvious application of becoming a standalone memory to replace existing memory technologies, a few more examples are listed in the following [73,74]. The first and most likely application is as embedded memory, which is a memory design that has memory built on the same chip as the processor. The memory cell size for embedded applications is normally bigger using the combination of embedded SRAM, DRAM or flash [75]. Speed and non-volatility are the main concerns for embedded applications instead of the cell size. Flash are well known to be slower than DRAM and SRAM, whereas DRAM needs a constant current to refresh its information. SRAM also needs a continuous power supply, besides having problem in providing high density if it is used in small dimension applications, such as mobile phones and portable multimedia players. STT-RAM eliminates all the disadvantages and retains the advantages of each memory mentioned above.

Secondly, STT-RAM is suitable in fast and continuous updates condition. This includes microcontrollers and robotics with data feedback in factory; printers systems that handles large amount of users; and large data communication systems. Thirdly, STT-RAM can be used in high

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reliability condition, such as health care electronics, power management systems, and server storage. Finally, STT-RAM is extreme temperature and environment condition tolerant. This will be particularly useful in transportation, such as automobile controls and feedback; and in military uses, such as missiles and spacecraft (which requires high resistance to radiation damage).

3.8. Present memory market

The total estimated market for memory chip is about $50 billion to $60 billion annually (Figure 29). Recession starts in late 2007 and severely affected the semiconductor industry today. The oversupply in the memory market also plays an important role in bringing down the price of memory [76] and eventually leads to loss. Therefore, the decrease in memory market share of year 2009 in Figure 29 reflects the reality of recession.

STT-RAM is most expected to replace DRAM, SRAM and NOR flash, which accounts for about 80% of the total memory market. Assuming a market penetration of 1%, the estimated revenue is around $400 million. The market share is expected to grow slowly for the first few years for a new technology, thus the total revenue for the first few years will probably less than a few billion dollars. If wide implementation of STT-RAM is supported by major memory makers in the world, the market penetration could rise to 50% or even completely replacing DRAM, SRAM and NOR flash. This will give ultimate revenue of around $20 billion to $40 billion.

One of the exciting opportunities for STT-RAM is the embedded memory market. Figure 30 shows the breakdown of the memory revenue in mobile phone industry. It is expected that the penetration of this market will be easier because of advantages in cell size, endurance and speed dominate. The memory revenue for this part will be around $7 billion excluding NAND flash. STT-RAM could be sold into further end of the supply chain as standalone memory chip or into earlier implementation as part of integrated circuit. Therefore, the immediate intended customers will be memory module makers or the manufacturers of mobile phone and portable multimedia players. The selling channels could be either direct channel or via electronics wholesale distributors.
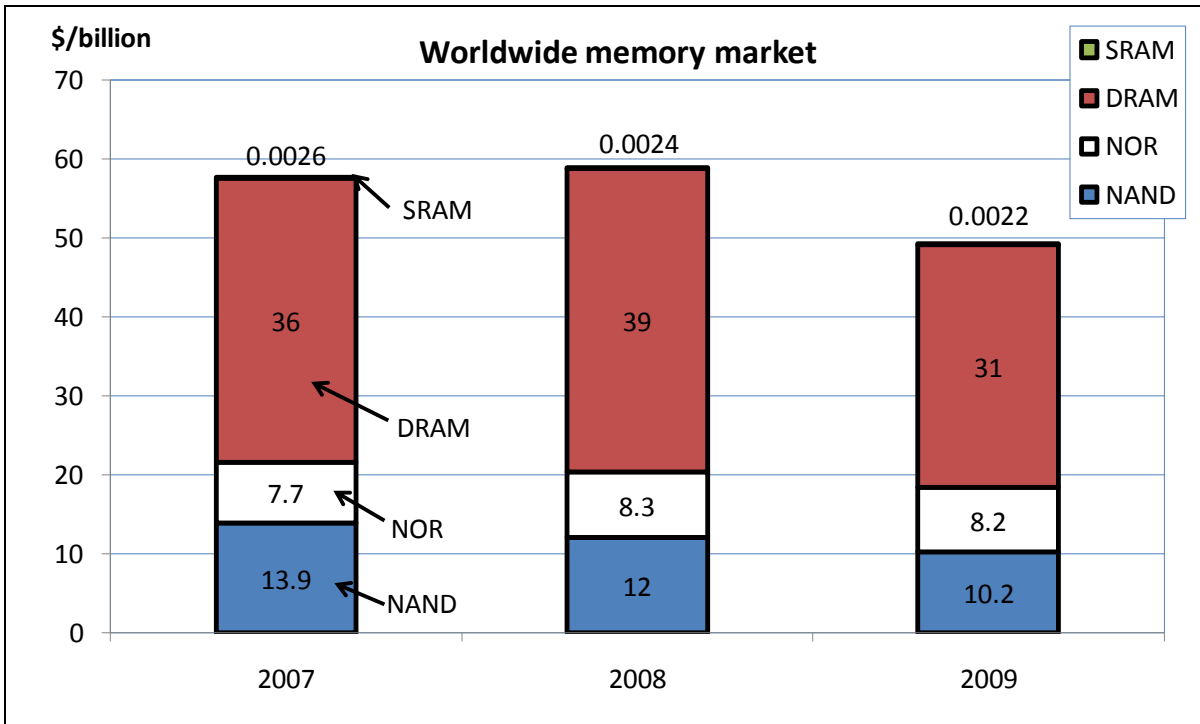
Figure 29 Breakdown of memory market, with estimation and forecast. The numbers shown are the corresponding values. Adapted from [75,77,78].
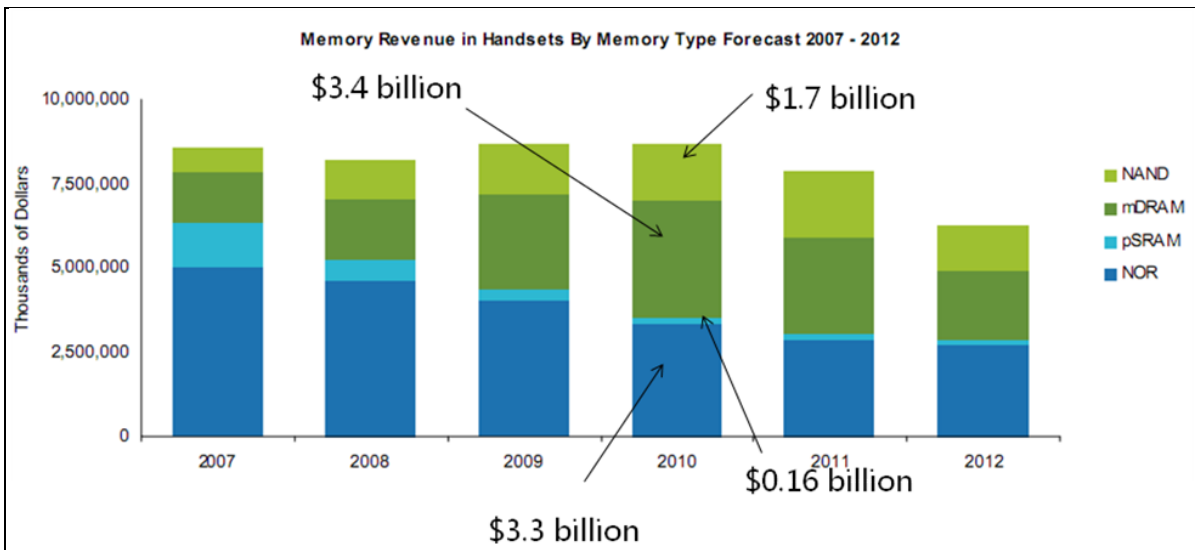
Figure 30 Memory revenue in mobile phone markets. pSRAM is one type of DRAM that mimics the operation of SRAM. Taken from [79].

The pricing of different existing memories is obtained by surveying various sources from the internet [80-84], and it is given in Table 2.

Technology	Price ($/Gb)
NAND flash	0.10-0.40
NOR flash	15
DRAM	0.60-2
SRAM	1000-2000

Table 2 Price of different memory technologies to date. Adapted from [80-84].

Many companies, especially those who worked in developing MRAM before, are researching and developing STT-RAM. These companies includes but not limited to Everspin (Everspin Technologies is a spin-off company that handles the business of MRAM by Freescale [85]), Grandis, Hynix, IBM-TDK, Samsung, Toshiba, Hitachi, Qimonda, Siemens, and Altis. [86,87]. Among all these companies, Grandis appears to be the most popular. Although Grandis has made many announcements related to STT-RAM [88], such as opening of first 300 mm MTJ fabrication facility dedicated to STT-RAM and joint development with Hynix, no product or prototype has been available publicly. Recently, the co-founder of Grandis has started up Avalanche Technology and plan to fabricate standalone STT-RAM at 65 nm [86].

4.   Implementations

4.1.   Evaluation of patents

Evaluation of patents allows us to understand the latest advancement in a specific technology because publications in this form guarantee the inventors a 20 years of monopoly from the date of application [89]. This is especially true when there lays a great business opportunity behind the inventions, such as STT-RAM. In a patent, the most important part is the claim of the invention. Claim number one is the broadest claim in the patent. Each subsequent claim narrows down the uniqueness and the real features of the invention. The narrower claims also protect the patents if claim number one is deemed invalid (too broad). The description is given to educate the readers about the invention in exchange for the claims granted to the inventor(s).

This section will only examine patents that are already issued because patent applications might be deemed invalid. To further restrict the scope of this section, only United States patents are examined. Therefore, it is assumed that United States (US) patents represent the overall technology trend. The search on issued patents using US classification related to magnetic memory gives more than 3000 patents in the database of United States Patent and Trademark Office [90]. To further understand the distribution of STT-RAM related patents, the patent search is conducted using manipulation of keywords and then manual reviewing using Free Patents Online website [91]. There are a few points to note before going to the result. It is hard to differentiate STT-RAM patents from MRAM sometimes since the difference is small (see section 3.6.1) and the intention of filing a patent is to make the invention has the widest claim possible; for example, [92]. The keyword is mainly based on assignee name (usually are companies) and further restricted by specific terms to reduce the unrelated patents. The best effort has been made to include most of the institution that have been issued STT-RAM related patents. Since there are many ways to describe an invention, this keywords combination will inevitably eliminate some of the related patents; however, it is common to all cases and thus still gives relative number of patents among the assignees. In some rare cases, the same patent that shared by different assignees could be accounted twice. The relevance point system, provided by Free Patents Online, is used to further filter the search result. STT-RAM is a very specific technology and many broad patents could have already covered a design of STT-RAM. Therefore, patents with relevance point more than 500 (out of 1000) are considered and the total amount is 94. With the above points in mind, the search reveals that Grandis, Inc. is dominating the STT-RAM patents realm with 46 patents (Figure 31).
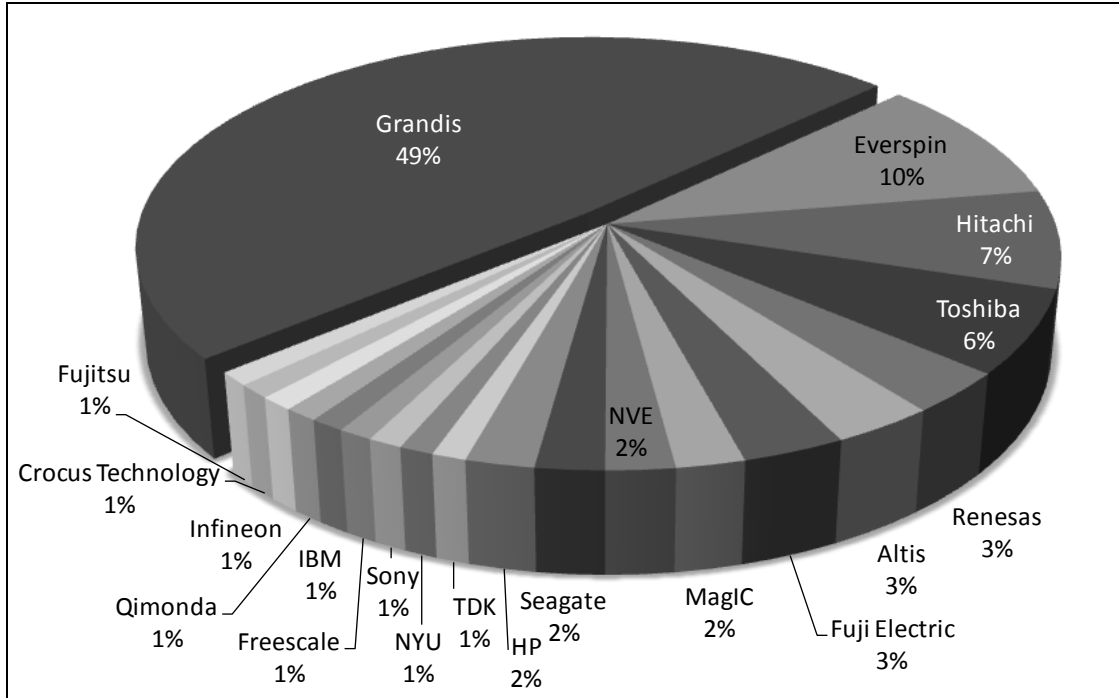
Figure 31 Distribution of patents with relevance points more than 500. NYU and HP is New York University and Hewlett-Packard, respectively.

Further examination of some patents reveals that the patents mainly involve three categories. The first one involves new structure of magnetic element, which is normally still MTJ but with different arrangement of layers [38,93-96]. The claims will also include the memory design by using plurality of the magnetic element mentioned. The second category describes the design of the magnetic memory array, which includes bit lines and word lines, in detail [97,98]. Finally, the third category of patents discuss only the fabrication of a new magnetic element (MTJ) [99,100]. Therefore, to secure a unique invention for fabrication of STT-RAM, at least two levels of patents are needed, one for the magnetic element and another one for the design of the circuit.

As mentioned above, the patents reflect the technological trend of an invention. Much effort has been put into reducing the switching current density for the motivation discussed in section 2.6.3. Referring to equation (5) or (6) in section 2.3, one of the way to reduce the switching current density is to introduce a free layer with perpendicular anisotropy as described in the patent numbered 7531882 [101]. This new free layer has perpendicular anisotropy energy with value more than 20% of the in-plane anisotropy energy, but less than 100%. This allows the magnetization of the free layer to stay in-plane when in equilibrium but able to offset the $2\pi M_S$ term. Another invention

introduces a keeper layer that is adjacent to the free layer [38]. The keeper layer itself has perpendicular anisotropy and is coupled magnetostatically to the free layer, effectively negates the surface anisotropy ($2\pi M_S$). Besides that, the switching current density can also be reduced by increasing the spin transfer efficiency. This can be done using a spin diffusion layer that has a very short spin diffusion length (less than 10 nm) next to the free layer [94] because it can confine the spin dependent current in the MTJ to increase the STT in the free layer. Similar result is observed in a STT-RAM magnetic cell combining both GMR and MTJ structure but with only one free layer [95]. The free layer experienced two STT and the switching current is thus reduced. Moreover, the surface anisotropy can be reduced directly by using a ferromagnetic material with a low saturation magnetization (M_S) [96]. Unfortunately, the patents do not disclosed the value of the achievable switching current density with the inventions they presented.

4.2. Fabrication steps
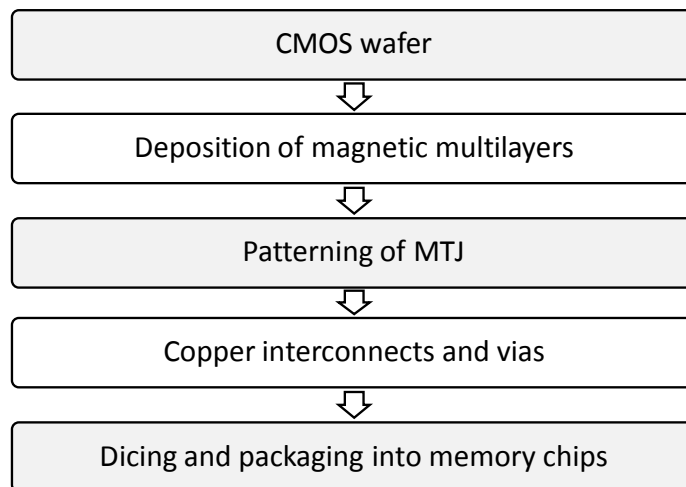
Figure 32 Simplified fabrication steps for a STT-RAM.

The fabrication steps of STT-RAM are identical to MRAM because only the metal lines for inducing one of the magnetic fields are removed in STT-RAM. Similar with MRAM, the starting step can begin at the back-end of a CMOS wafer (Figure 33) [102].
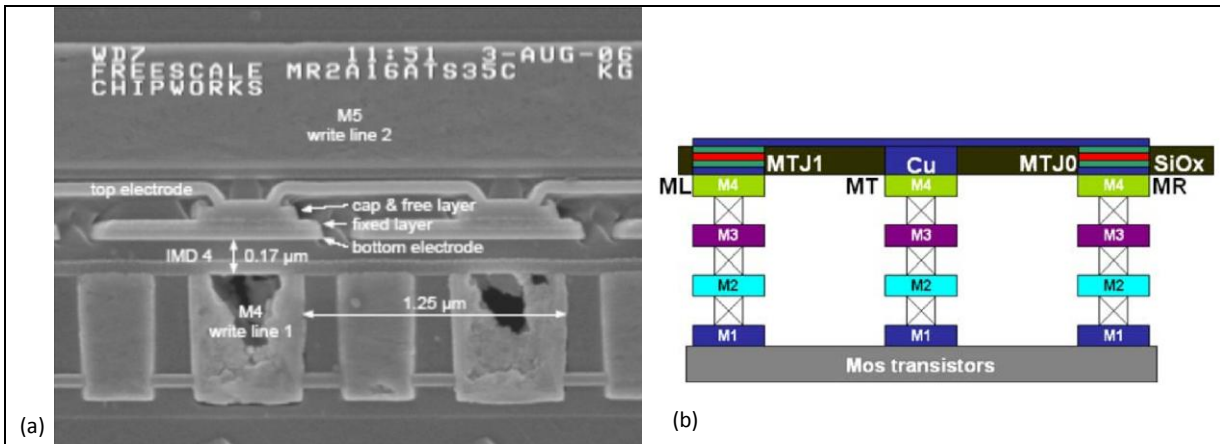
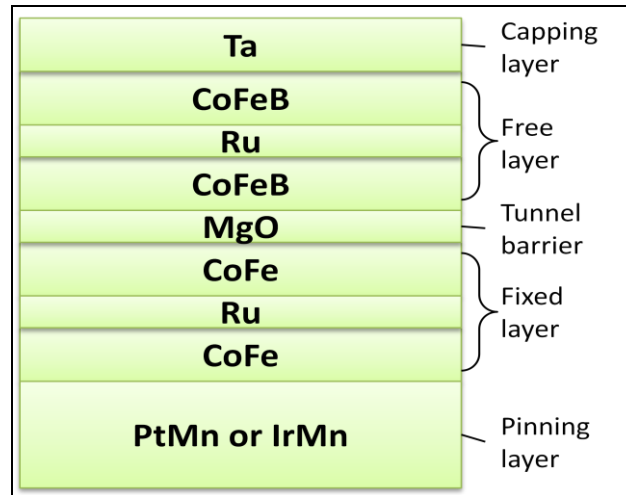**Figure 33 (a) Cross sectional view of Freescale MR2A16ATS35C 4Mb RAM. (b) Schematic view of MTJ on top of CMOS circuit in a STT-RAM. Adapted from [44,102].**

The fabrication process described here is an approximation to the exact process as it is believed that the actual process is far more complicated for an industry-standard STT-RAM. In summary, three additional mask levels are required to integrate the MTJ to form STT-RAM: one for patterning the MTJ, and another two to form local interconnects and via to the interconnects, respectively [103]. According to the structure of a MRAM product from Freescale (Figure 33) [102], the MTJ is located between metal lines. M4 is the metal line from the CMOS wafer and M5 is the metal line deposited after the MTJ is integrated to the CMOS wafer.

Detailed fabrication process in [104,105] is used to estimate the MTJ integration in STT-RAM. First, the magnetic and nonmagnetic layers are deposited in a desired sequence onto the whole CMOS wafer by direct current (dc) magnetron sputtering, whereas the insulating tunnel barrier (MgO) is deposited by radio frequency (rf) magnetron sputtering. In a practical device, synthetic antiferromagnetic (SAF, see section 3.6.1) structure is normally used as the fixed and free layer. The advantage of SAF structure is its less sensitivity to the magnetostatic stray field created by other layer [2,106]. A pinning layer is used to fix the magnetization of the fixed layer and render the fixed layer undisturbed by STT from free layer, whereas capping layer is used to protect the MTJ stack and it has influence on the TMR effect [19]. An example of a MTJ stack is shown in Figure 34. The final MgO layer is obtained by depositing MgO on an Mg seed layer (0.4 nm) to acquire low RA product.

Ta — Capping layer

CoFeB

Ru — Free layer

CoFeB

MgO — Tunnel barrier

CoFe

Ru — Fixed layer

CoFe

PtMn or IrMn — Pinning layer

Figure 34 An example of a practical MTJ.

The multilayers are later annealed at 280 °C for two hours and the patterning of MTJ follows next. (Before patterning the MTJ, a test of MR ratio and RA product could be done on the wafer by using equipment such as CIPTech [107].) A negative photoresist mask is patterned using lithography and further trimmed. The photoresist together with a conducting hard mask (Ta, TaN or TiN) situated below are put on top of the multilayers. The hard mask can be later used as the capping layer. Reactive ion etching (RIE) is used to etch through the hard mask to pattern the multilayers into desired MTJ shape. This etching process should stop in the MgO barrier to avoid shorting and inhomogeneous current flow. The resist is striped off after the etching process. The patterned structures are then encapsulated with dielectric and further planarized by chemical mechanical polish (CMP). The CMP process eliminates any protruding features and prepares the wafer for damascene copper wiring. Next, a second photoresist mask is prepared to define the trench. The trench is etched using RIE into the dielectrics using the previous conducting hard mask for self-alignment. The depth of the trench is enough to expose the conducting hard mask. After a cleaning step, a wiring liner film is deposited along with a copper seed layer. The trench is subsequently filled with copper electroplating. A final CMP process is used to planarize the surface. The overall process and final product are shown in Figure 35.
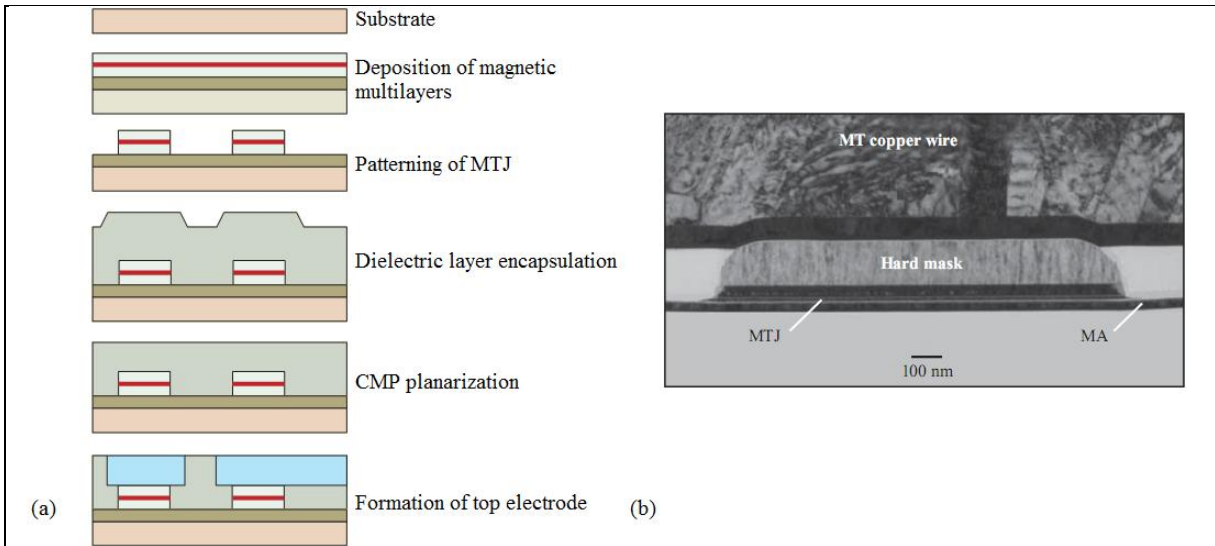
Figure 35 (a) Schematic fabrication process of MTJ. (b) TEM cross section of the finished MTJ device. MA is the bottom electrode. The dimension of this MTJ is larger than the process described. Adapted from [105].

The third photoresist mask is used to create vias necessary for connecting the transistors from the CMOS base to the MTJ above (Cu above MT in Figure 33). At the end, the wafer is diced and packaged into desired size to constitute a memory chip.

4.3.   Cost estimation

4.3.1.   Dependence of parameters

The cost of fabricating a STT-RAM is closely related to technological parameters associated with it, such as switching current density and the size of MTJ and transistor. Here, a simple model is established to examine the effect of this dependency. The area of a STT-RAM memory cell (A_{cell}) is determined by both the area of the MTJ (A_{MTJ}) and the driving transistor,

$$A_{cell} = k_1 A_{MTJ} + k_2 \left(L_g\right)^2$$

(9)

where L_g is the gate width of the driving transistor, k_1 and k_2 are proportional constants that decides the effect of the area of MTJ and driving transistor in a memory cell, respectively. The effect of the elongated shape of MTJ is considered and absorbed into the constant k_1, whereas the saturation current of the transistor per gate width ($I_{sat/g}$) is around 500μA/μm [50]. Therefore, the required gate width depends on the switching current (I_c) of the MTJ,

$$L_g = \frac{I_c}{I_{sat/g}} \text{ and } I_c = J_c A_{MTJ}$$

(10)

where J_c is the switching current density of the MTJ. Substituting equations (10) into equation (9), we obtained

$$A_{cell} = k_1 A_{MTJ} + k_2 \left(\frac{J_c A_{MTJ}}{I_{sat/g}} \right)^2$$

(11)

The cost per bit can be expressed as

$$C_{bit} = \frac{C_{wafer}}{N_{cell}} = \frac{C_{wafer}}{N_{bit}}$$

(12)

where C_{bit}, C_{wafer}, N_{cell} and N_{bit} is cost per bit, cost per wafer, number of cells per wafer, and number of bits per wafer, respectively. At high volume manufacturing, the complexity of a fabrication process often dominates the total cost of a wafer. Since the number of masks levels determines the total fabrication steps, the cost per wafer increases for each addition of mask levels. Therefore, the cost per wafer is assumed to have the following expression:

$$C_{wafer} = C_{wm} (N_{mask}).$$

(13)

C_{wm} is the cost per mask level per wafer and N_{mask} is the number of mask levels for that memory technology. The number of bits per wafer can be obtained by dividing the area of cell with area of the whole wafer (A_{wafer}), namely

$$N_{bit} = f\left(\frac{A_{wafer}}{A_{cell}}\right).$$

(14)

f is the utilization efficiency and has value between 0 and 1. It measures how much area in a chip is occupied by memory elements (MTJ for the case of STT-RAM); 1-f is the area occupied by other logic that needed for the memory to function. Substituting equations (13), (14) into (12) with (11), the cost per bit for a STT-RAM can be expressed as

$$\begin{aligned} C_{bit} &= \frac{C_{wafer}}{N_{bit}} \\ &= \frac{(C_{wm})(N_{mask})(A_{cell})}{(f)(A_{wafer})} \\ &= \frac{(C_{wm})(N_{mask})}{(f)(A_{wafer})}\left[k_1 A_{MTJ} + k_2\left(\frac{J_c A_{MTJ}}{I_{sat/g}}\right)^2\right] \end{aligned}$$

(15)

Examination of equation (15) reveals that cost per bit can be reduced if the switching current density and area of MTJ decreases. This expression is used to calculate the cost per bit for a typical STT-RAM with some values from [37] (Table 3).

A_{MTJ}	125 nm × 220 nm
$I_{sat/g}$	500μA/μm
J_c	2.2×10^6 A·cm^{-2}

Table 3 Values for the parameters in a STT-RAM. Taken from [37].

Assuming $k_1=k_2=16$, f=0.5, and 200 mm wafer ($A_{wafer}=$ 0.0314 m^2), the cost per bit can be simplified to

$$C_{bit} = (1.52 \times 10^{-9})(C_{wm})(N_{mask})$$

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Assuming a $500 CMOS wafer needs around 20 mask levels and the cost per mask level per wafer is roughly the same for different memory technologies, C_{wm} is given a value of $2.5. The number of mask levels for a STT-RAM is 23 (3 additional mask levels on a CMOS wafer). Therefore, the cost for a STT-RAM using the above parameters is $87.4/G b. The accuracy of estimating the cost relies heavily on the accuracy of the value of C_{wm}.

To compare between two memory technologies, a simple expression can be written by making certain assumptions: the cost per mask level per wafer and the utilization efficiency is the same for different memory technologies. Hence, for same wafer area, the cost per bit for specific memory technology is

$$C'_{bit} = \left(\frac{N'_{mask}}{N_{mask}}\right) \left(\frac{A'_{cell}}{A_{cell}}\right)(C_{bit})$$

(16)

where the primed terms refer to the parameters of one technology and the unprimed terms refer to the other. Since the base mask levels are around the same (approximately 20), the memory cell size have more impact on the cost per bit for a memory technology.

4.3.2. Bottom-up cost model

It is often very difficult to estimate the cost using bottom-up method since many specialized knowledge are needed. However, the method still can give a rough idea about the order of magnitude of the cost, if it obeys certain assumptions. In the case of STT-RAM, some important assumptions are mentioned here. First, the STT-RAM prototype from Hitachi (section 3.6.2 [72]) is used as the basis of this cost modeling (0.4 μm feature size (F); cell size of 2.56 μm^2 (16F^2); chip size of 13.3 mm^2; 2 Mb per chip; and have sixteen 128 kb arrays with size of 0.328 mm^2 each). Hence, the amount of chip per wafer is 1700 after considering 80% yield and 90% usable wafer area. Second, the multilayer used in this cost model is shown in Figure 36, which is based on a description from a patent with slight modification to ease calculation [95]. Third, the number of equipments is estimated using the fabrication process described in section 4.2, the final cost is very much dependent on the equipments used and thus is one of the main factor that limits the accuracy of this cost model. In this

case, one equipment, with usable lifetime of five years, is dedicated to each fabrication step to avoid possible contamination, which is also shown in Figure 36. The fabrication process starts with a 200 mm CMOS wafer and it costs $500 per wafer. Fourth, the equipment can only process one wafer at a time and the cycle time is two wafers per hour. Finally, the overhead and maintenance costs are equal to 5% (excluding overhead) and 15 % of all other costs, respectively, and are included to cover indirect costs, such as consumables.

(a)		(b) Equipments/materials	Quantity
Ta (3 nm) — Capping layer		Lithography	3
CoFeB (2 nm) — Free layer		Dc/rf magnetron sputterer	5
Ta (0.6 nm)		Electroplating	2
CoFeB (2 nm) — Tunnel barrier		Etching	3
MgO (0.6 nm)		Chemical mechanical polisher	2
CoFeB (5 nm) — Fixed layer		Testing	5
Ru (0.8 nm)		Mask	3
CoFeB (5 nm)			
PtMn (10 nm) — Pinning layer			
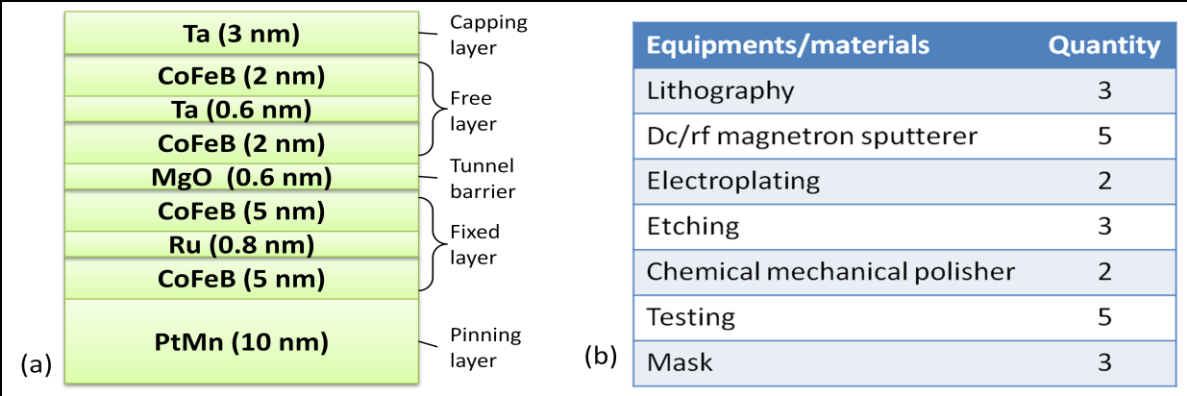
Figure 36 (a) Multilayers and (b) equipments and materials used in the bottom-up cost modeling.

Figure 37 Variation of cost per chip as production volume scales up.

As expected from a memory business, the fixed cost dominates the total cost (Figure 37). Fixed cost includes equipments, masks, building rental, clean room, maintenance, and overhead costs. On the other hand, variable cost consists of materials, labor, and electricity costs. As the production volume

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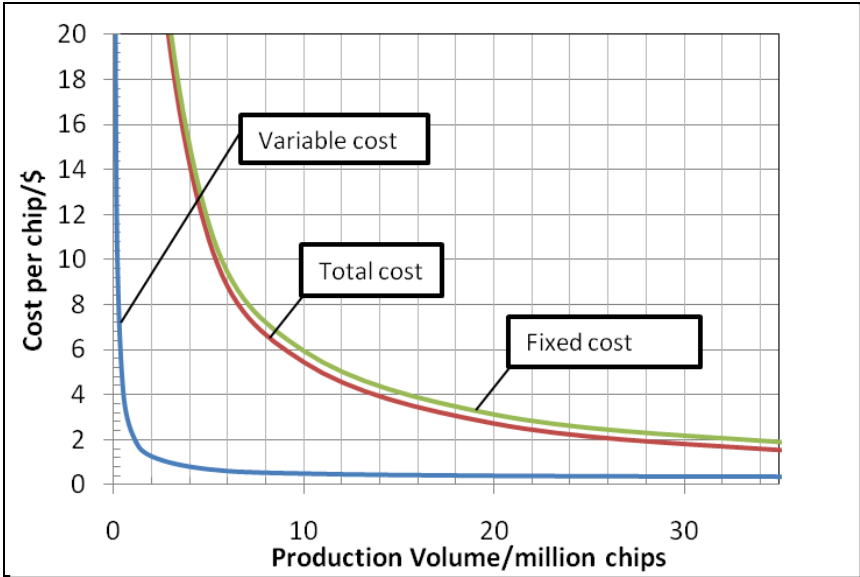scales up while the production capacity (around 35 million chips or 16000 wafers in Figure 37) remains the same, the cost per chip reduces rapidly until it saturates to a value near $2 per chip. Even if we expand the capacity (1X corresponds to around 16000 wafers annually), the cost per chip does not deviate far from $2 (Figure 38). When considering the expansion of production capacity, the production volume is set to equals to the production capacity, in other words, the factory is running at its maximum utilization ratio.
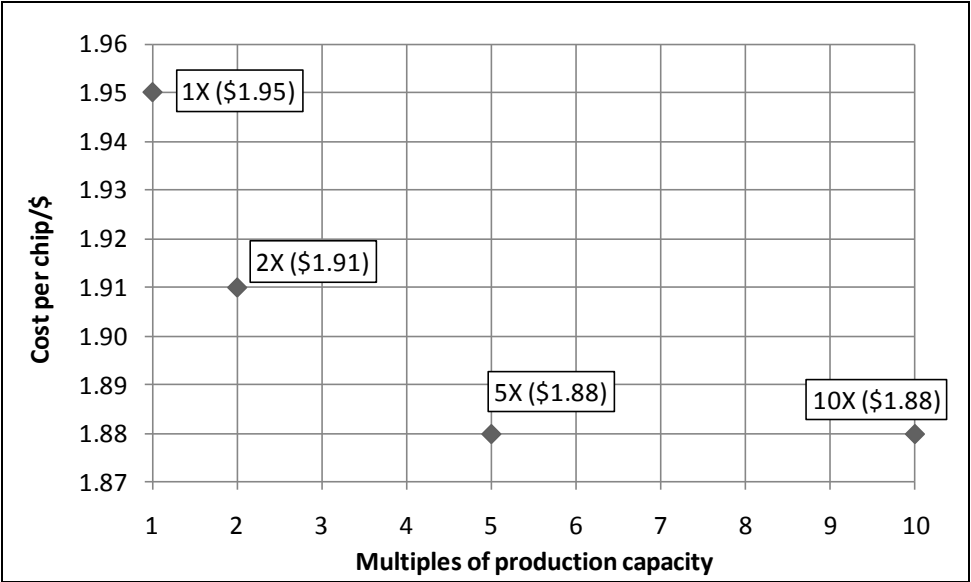
Figure 38 Effect of expanding production capacity at maximum factory utilization ratio.

The production volume is first set to be low (1,000 wafers per month), and the cost per chip is $2.51, corresponding to $1255/Gb. If the volume is increased to 10,000 wafers per month (the capacity scales up to ten times as well), the cost per chip drops slightly to $2.41, which means $1205/Gb. The distributions of costs for these two cases are shown in Figure 39 and are similar in overall. These numbers suggest that fabrication using 0.4 μm is expensive and hard to replace DRAM that only costs a few dollars per Gb. To investigate the effect of scalability of the cell size on the cost, the same memory chip architecture is used and the cost to shift to a smaller feature size is assumed to be the negligible as compared to the effect of decreasing cell size. For a same cell size of $16F^2$ but with feature size of 90 nm, the same array size can have more bits in it and the chip now has 40 Mb of memory capacity. The cost of this 40 Mb chip becomes $60/Gb if the production volume is 10,000 wafers per month. For an ultimate cell size for STT-RAM ($6F^2$) and F=32 nm, this gives around $2.82/Gb. Scaling down (reducing F) decreases the area of the memory cell in whole and thus is

necessary to reduce the selling price of STT-RAM to be comparable to DRAM price range. Another way of reducing the cost per bit is by introducing more effective memory cell design; for example, reducing $16F^2$ to $6F^2$.
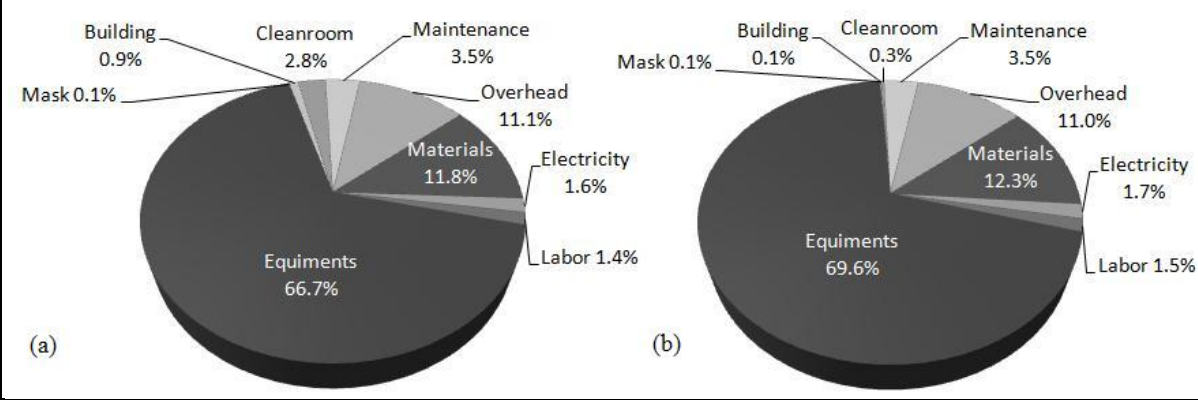
Figure 39 Distribution of cost for a STT-RAM for (a) 1,000 wafers per month and (b) 10,000 wafers per month.

4.3.3. Relative cost model

The relative cost model is based on the arguments in section 4.3.1 and provides another perspective on the cost of STT-RAM. The first comparison is made between the demonstrated STT-RAM technology and a mature memory technology, DRAM. DRAM needs 5 additional mask levels and cell area (or cell size) of 0.015 μm^2 ($6F^2$; F=50 nm; year 2009 [50]), whereas the additional mask levels and cell size for STT-RAM is 3 and 2.56 μm^2 ($16F^2$; F=400 nm, according to the prototype of Hitachi [70]), respectively. Using equation (16) in section 4.3.1 and the cost of DRAM assumed at $1.58/Gb [108], the cost of STT-RAM is about $248/Gb.

The second comparison is with a memory technology that has almost the same technological maturity with STT-RAM, the MRAM. The Freescale 4Mb MRAM is priced at $15 per chip or $3750/Gb [109]. The cell size of this MRAM is 1.55 μm^2 ($48F^2$; F=180 nm [110]), whereas the cell size of STT-RAM is as mentioned previously. Both MRAM and STT-RAM need the same additional mask layers. Using equation (16), the price is about $6194/Gb. The cost of STT-RAM could be several times less than the selling price because the profit margin is generally large for new technology, as a

high price is normally set to test the market response. This is also hinted when Freescale reduces the price of the same MRAM from \$25 to \$15 after one year of introduction [109].

4.3.4. Comparison between two models

The two cost models discussed above have ignore the effect of yield, throughput and testing procedures on different memory technologies. These parameters might be very different from one memory technology to another. However, these cost models are useful to provide an idea on the cost range of STT-RAM. Comparing both models, the bottom-up and relative cost models gives a cost of \$1205/Gb and \$248/Gb, respectively for the Hitachi prototype mentioned. The difference could possibly arise from the following reason. The comparison with the mature DRAM gives the cost of STT-RAM that is after optimization, especially in its fabrication process. On the other hand, the bottom-up model was based on current fabrication process. Nevertheless, these two models give an idea on the cost range of STT-RAM using the technology described. These two cost models also reemphasis the impact of area of memory cell on the cost per bit of STT-RAM.

4.4. Business model
4.4.1. Patents-licensing

Using the operating revenue of Grandis, Inc. in year 2006 (\$2.6 million) as an example, the estimated revenue for a patents-licensing company is less than \$10 million per year [111]. Although the profit is small compared to the total memory market size, but this involves a relative light investment at the starting point. The main risk of this business plan is the existence of large amount of patents in the industry. It might be hard to start up a new company with important technology that other companies cannot do without. Moreover, the competitors are developing their own version of STT-RAM. Even if the start-up company has some crucial patents, this business plan will fail if other companies catch up with a better solution. Therefore, start-up companies could license their patents to other companies for the first few years after STT-RAM is commercialized, but soon they need to fabricate their own memory chips either by outsourcing to foundries or seek co-operations from major memory chips makers.

4.4.2. Fabless company

If a company designs the STT-RAM and the fabrication is handed over to foundries (semiconductor fabrication plants), it is expected that portion of the profit will be divided to the foundries as well. The estimated revenue is $400 million for a market penetration of 1% according to section 3.8. The profit depends on the first setting of the price and also the market penetration. However, the condition for this model to be successful is the company must have adequate patents to fabricate the whole STT-RAM. Licensing missing key patents from other companies will still be feasible if the missing patents are not the main values of the whole STT-RAM. Foundries might not able to produce MTJ in large scale and optimized way could also be one of the risks involved.

4.4.3. Full fabrication

A full fabrication facility is estimated to involve first year investment of $130 million and subsequently $51 million yearly as calculated using the bottom-up cost model. A good strategy is starting the fabrication process with a CMOS wafer; this helps to avoid potential patent conflicts and loss due to unsalable of products: by stocking CMOS wafers and only produce as needed [102]. Considering the situation listed in section 3.8, the break-even point (cost equals to revenue) might happen within the first few years, heavily dependent on the market penetration and the initial pricing (or initial profit margin). However, big semiconductor or memory players, such as Intel, Toshiba, SanDisk, Hynix, Samsung, and so on will mostly likely have the "influence" advantage (reducing the price of and improving the existing memory to buy time for their own version of STT-RAM to emerge) since they are in other memory business as well. On the other hand, giant fabless companies can give pressures to the foundries to reduce the cost of fabrication for their own product since they are the main customers of the foundries. Eventually, it depends on how well the company can protect their intellectual properties and how to maintain advantages in terms of technology ahead of other competitors.

5.   Conclusion
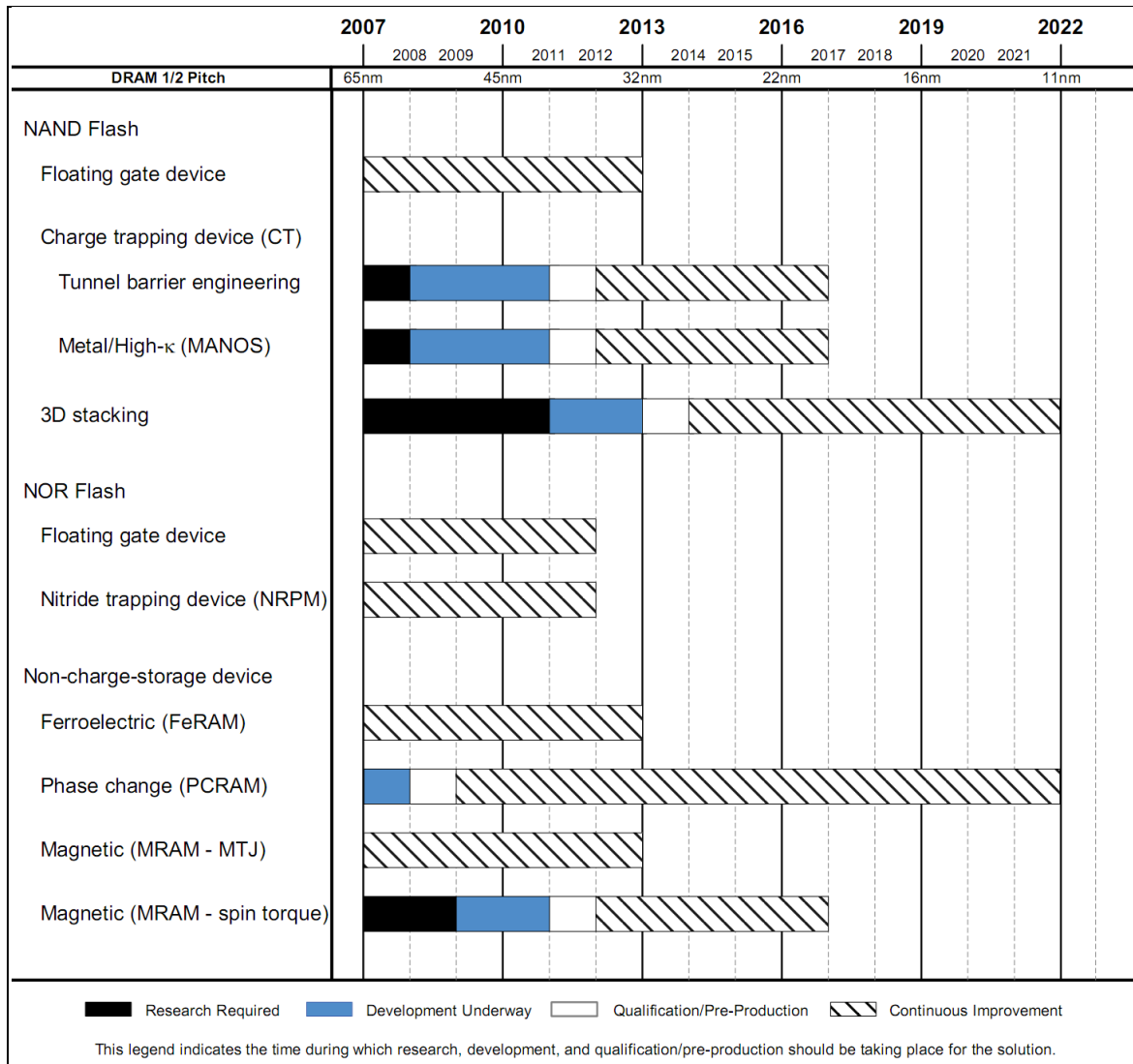
Figure 40 Timeline planned for different memory technologies. Taken from [50].

STT-RAM provides a solution for overcoming the high write current in MRAM, the first and most important technological barrier of magnetic memory. However, STT-RAM is still limited by the minimum gate width of the transistors that can be used. Therefore, the second-major technological barrier is the size reduction of the transistor, which could be done either by the scaling down of critical switching current of the magnetic element or increasing the saturation current per gate width for the MOS transistor. It would probably need another few years to overcome this technological barrier if it is possible. Meanwhile, the existing technologies will not stop developing and are

expected to scale-down. Let assume the industry overcame the second-major barrier, the wide acceptance of STT-RAM still depends on the cost, which are determined by the willingness of main memory providers to scale-up STT-RAM for high volume manufacturing. All these indications biased to a focus on research and development for a few more years rather than entering the market right now. Within few years (predictably to be by year 2012, see Figure 40 [50]), the promises of STT-RAM as massive replacement of existing technologies will be made clear. Otherwise, it would be expected that STT-RAM to take only small portion of the total memory market, or in other words, becoming a niche market technology.

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22spin+transfer%22+OR+ACLM%2F%22spin+injection%22%29+OR+%28ABST%2F%22spin+tor
que%22+OR+ABST%2F%22spin+momentum%22+OR+ABST%2F%22spin+transfer%22+OR+ABS
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%22+NOT+ACLM%2F%22probes%22+NOT+ACLM%2F%22GMR+sensor%22+NOT+ACLM%2F%2
2EMR+sensor%22+NOT+ACLM%2F%22nuclear+magnetic+resonance%22+NOT+ACLM%2F%22
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