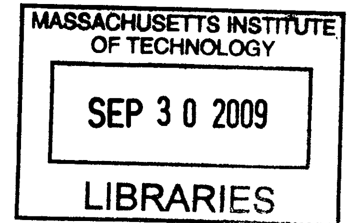
Physics of Electrical Degradation in GaN High Electron Mobility Transistors

by

Jungwoo Joh

B.S., Electrical Engineering
Seoul National University, 2002
S.M., Electrical Engineering and Computer Science
Massachusetts Institute of Technology, 2007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Author ______________________________
Department of Electrical Engineering and Computer Science
August 20, 2009

Certified by ______________________________
Jesús A. del Alamo
Professor of Electrical Engineering
Thesis Supervisor

Accepted by ______________________________
Terry P. Orlando
Professor of Electrical Engineering
Chairman, Department Committee on Graduate Students

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ABSTRACT

The deployment of GaN high electron mobility transistors (HEMT) in RF power applications is currently bottlenecked by their limited reliability. Obtaining the required reliability is a difficult issue due to the high voltage of operation. In order to improve reliability, it is essential to develop detailed physical understanding of the fundamental degradation mechanisms. In this thesis, we investigate the physical mechanisms behind the electrical degradation of GaN HEMTs by performing systematic stress experiments on devices provided by our industrial collaborators. These devices are electrically stressed under various bias conditions while regularly characterized by a benign characterization suite. We observe that electrical stress beyond a critical voltage results in an increase in drain resistance, a decrease in maximum drain current, and a sharp increase in reverse gate current. We show that this mode of degradation is driven by electric field and that current is less relevant. Behind this degradation is trap formation that occurs at the critical voltage. To understand this, we have developed a new trap-analysis methodology. It is found that under stress, the density of traps increases in the AlGaN barrier layer in the proximity to the gate edge on the drain side of the device. We show that this degradation is enhanced under mechanical uniaxial tensile strain that is externally applied to the device. From our experiments, we propose a degradation mechanism of defect formation through the inverse piezoelectric. In this mechanism, high vertical electric field at the gate edge under high voltage increases tensile stress in the AlGaN layer due to piezoelectricity of the material. When the elastic energy in the crystal exceeds a critical value, crystallographic defects are formed. These defects trap electrons and reduce drain current as well as provide leakage paths and increase gate current. We theoretically validate the plausibility of this hypothesis and provide a model for the critical voltage that agrees with experimental observations. Unlike conventional wisdom, hot electrons do not appear to be the direct cause of electrical degradation in the devices that we study. Our studies suggest several possibilities to improving the electrical reliability of GaN HEMTs.

Thesis supervisor: Jesús A. del Alamo
Title: Professor of Electrical Engineering

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Chapter 1. Introduction

1.1. Introduction to GaN HEMT

GaN high electron mobility transistors (HEMTs) have great potential for high voltage switching and high power RF power applications due to a variety of unique material properties of GaN. As a result of the high band-gap (3.4 eV) and subsequent high breakdown electric field (>3×10^6 V/cm) of GaN [1], GaN based devices can handle very high voltage. For example, GaN-based devices have demonstrated a very high breakdown voltage of 8300 V [2]. In addition, strong piezoelectric effect and spontaneous polarization in III-nitride result in a high sheet carrier density (>10^{13} cm^{-2}) in AlGaN/GaN heterostructure without conventional doping [3-4]. As a result, high current density can be easily achieved in GaN HEMTs. The combination of high voltage capability and high current density makes GaN HEMTs an ideal candidate for high power applications. In addition, due to large conduction band discontinuity between AlGaN and GaN, AlGaN/GaN structure shows high electron mobility (>1500 cm^2/Vs) and high electron saturation velocity (2.5×10^7 cm/s) [1]. This enables a high frequency and high power operation, and an f_T of 180 GHz has been demonstrated with a 30 nm gate length device [5].

Due to these outstanding material properties of GaN, the AlGaN/GaN HEMTs have shown extraordinary performance at wide range of frequency in RF power applications: output power density of 40 W/mm at 4 GHz [6] and 13.7 W/mm at 30 GHz [7] has been demonstrated. Also, a power density of 2.1 W/mm has been demonstrated at 80.5 GHz [8]. These power densities are an order of magnitude higher than conventional technologies

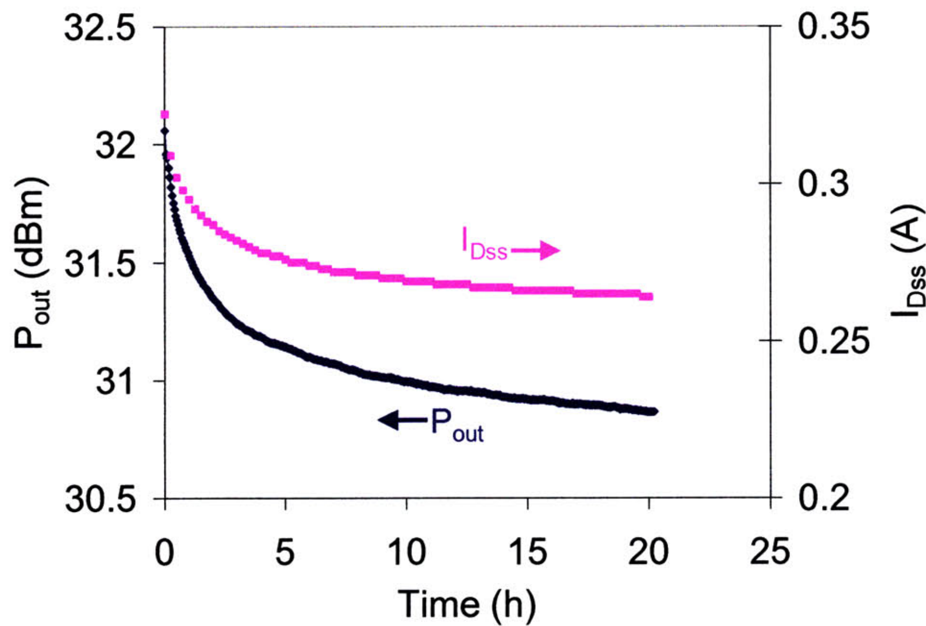

Figure 1-1. Change in P_{out} and I_{DSS} in an RF life test. The stress condition is V_{DS}=40 V and P_{in}=23 dBm.

based on GaAs or InP. This outstanding performance makes these devices of great interest for high-power, high-frequency applications such as WiMAX or WLAN base stations as well as for high voltage switching applications in power electronics.

1.2. Motivation

One of the greatest impediments today preventing the wide deployment of GaN HEMT technology is its limited electrical reliability. Although the reliability of GaN HEMTs has been improving over the last few years [9], these devices still suffer from a variety of degradation mechanisms [10-13]. As a result, GaN HEMTs have yet to demonstrate solid RF and DC reliability. For example, Figure 1-1 shows the degradation in RF and DC device performance parameters in an RF life test. This experiment has been done in the course of this work. The device is stressed at a target operation bias point of 40 V. It can be seen that the output power density P_{out} as well as I_{DSS} degrade relatively fast during the first 20 hours

of RF operation. This is a serious problem especially for applications, such as satellite communications, where extremely good reliability is required. As mentioned above, these devices are targeted for high-power and high-voltage applications. Also, due to the high band-gap of GaN, these devices are expected to be used for high temperature operation. Because of the extreme environments in which these devices will be used, solid reliability is especially difficult to achieve.

In order to achieve solid reliability, detailed understanding of the physical mechanisms behind device degradation is crucial. This entails understanding what stress conditions (current, voltage, temperature, environment) cause degradation, what device performance parameters (I_D, R_D, or V_T) degrade and how, and the role of device design (device geometry, heterostructure). In addition, because there is usually a trade-off between performance and reliability, by understanding the physics of degradation, the device structure and the heterostructure can be designed to achieve optimized performance and reliability. Also, understanding of physical degradation mechanism is important for evaluating device reliability. Normally, device reliability is evaluated in terms of life time that is extracted from stress tests where high temperature and/or harsher bias condition are used to accelerate the degradation. With a good understanding of the physical mechanism of degradation, acceleration parameters such as temperature and voltage for stress tests can be correctly determined for accurate prediction of device life time. Otherwise, degradation mechanisms that are irrelevant to real device degradation under normal operation condition can be activated in the life test, and predicted life time from that life test may not represent the device life time under normal operation condition.

To date, several mechanisms have been proposed to explain GaN HEMT degradation. The prevailing hypotheses are hot-electron induced trap formation [14-15], hot electron trapping at the surface [16], and crystallographic defect formation through the inverse piezoelectric effect [10]. However, understanding of device degradation is still limited, and more detailed understanding of these mechanisms as well as finding new mechanisms that have

not been identified is necessary. In addition, new measurement techniques to study various phenomena in GaN HEMTs should be developed in order to understand these degradation mechanisms in greater depth. In this thesis, we investigate detailed physical degradation mechanisms of millimeter-wave RF GaN HEMT through various device characterization techniques in order to shed light on solutions to improving device reliability.

1.3. Background

In this section, previous studies on GaN reliability in the literature are introduced. First, we summarize the most significant reports about degradation in GaN HEMTs. We give more details about what appear to be the two major degradation mechanisms – hot electron effects and defect formation through the inverse piezoelectric effect. Finally, two related phenomena, trapping effects and current collapse, are discussed.

1.3.1. Reliability studies

The electrical degradation of GaN HEMTs has been investigated by many authors. As mentioned above, a reduction in drain current and output power is one of the most serious problems in RF power applications, and this has been widely observed in various stress experiments [13, 17-22]. Although a few studies have tried to understand the origin of RF output power degradation [18, 23], in most cases, DC stress tests were performed to identify physical degradation mechanisms. The degradation in drain current is usually accompanied by an increase in drain resistance, while source resistance is relatively unaffected by electrical stress [10, 17, 24]. In addition, transconductance degradation is also observed [13, 15, 17, 25]. Although positive shift of threshold voltage has been observed in some cases [11, 17-18, 24], no systematic and consistent picture has emerged about the changes in the threshold voltage of the device.

In many cases, after electrical stress, increased trapping behavior has been observed [10-11, 13-15]. This increased trapping effect worsens RF to DC dispersion, and thus RF output power can significantly degrade without apparent degradation in DC characteristics. In some cases, reduced drain current recovers to some extent, but it immediately decreases to the previously degraded value once the stress is resumed [10, 26]. This is an evidence of trap creation during the stress. Also, degradation in gate current has been reported after high voltage stress tests [17, 22, 27-30]. In these cases, a large increase in reverse gate leakage due to degradation of the Schottky gate has been observed. No recovery in I_G degradation was observed. An excessive increase in gate current can degrade the RF performance such as PAE and gain [9]. Although Schottky characteristics can degrade under high voltage stress, the Schottky gate characteristics have been found to be generally stable during thermal stress [9, 15, 31-32]. Unlike GaAs devices where gate sinking is one of the important degradation mechanisms, no gate sinking has been reported in GaN HEMTs [31-33]. In addition, no obvious ohmic contact degradation has been found after long term thermal stress [15, 31] or even after device degradation in high voltage stress tests [19, 24, 33].

Although there have been some studies on the effect of long term stress [15], most of the reliability studies have focused on degradation mechanisms that affect devices in a relatively short period of time, as GaN HEMTs normally degrade within a few hours of device operation at high voltage and temperature. A few industry groups have reported their DC and RF life test results [9, 18, 34-38]. Although stressing conditions, failure criteria, or existence of pre burn-in tests are all different among these reports, the predicted mean time to failure (MTTF) at 300 C of junction temperature was around 150 hours. The activation energy of the MTTF was generally between 1.05 and 2 eV (although Coffie et al. have reported a negative activation energy of -0.15 eV [37]).

1.3.2. Hot electron effects

In previous studies on Si MOSFET, Si LDMOS, and InP and GaAs HEMT, hot-electron induced degradation has been found to be one of the primary device degradation mechanisms [39-44]. In these devices, under high drain voltage, electrons in the channel can be accelerated to gain enough energy to overcome the energy barrier and reach the surface, barrier, interface between gate metal and semiconductor, or passivation and semiconductor in the gate-drain gap. These electrons can be trapped or create traps in these regions and degrade the performance of the device by shifting the threshold voltage, increasing the drain resistance, reducing the maximum drain current, and worsening trapping behavior. In this type of degradation mechanism, there is a correlation between the degradation and $1/(V_{DS}-V_{DSsat})$ [39, 42-43] or gate current that is produced by impact ionization [41, 43]. In the early stage of degradation, hot-electron trapping can be reversible, but it becomes irreversible as degradation advances [44].

Following this body of work, many studies on GaN HEMT reliability have focused on hot electron effects and suggested that hot electrons are at the center of device degradation. Hot-electron induced degradation is particularly of concern because the typical drain bias during operation in a GaN HEMT is expected to be much higher than in conventional device technologies. So far, prevailing hypotheses are hot-electron induced trap formation [15] and hot electron trapping at the surface between gate and drain [17, 24]. However, unlike GaAs or InP based HEMTs, no obvious degradation due to impact ionization has been reported. In fact, impact ionization itself seems less important in GaN HEMTs under typical operating conditions [13], presumably due to the high bandgap of GaN.

Kim et al. have attributed device degradation in high-voltage and high-current stress conditions to hot electron trapping [16-17]. They observed that degradation in P_{out} and I_D are associated with an increase in drain series resistance and suggested that this is caused by an increase of channel depletion due to electron trapping at the surface region between

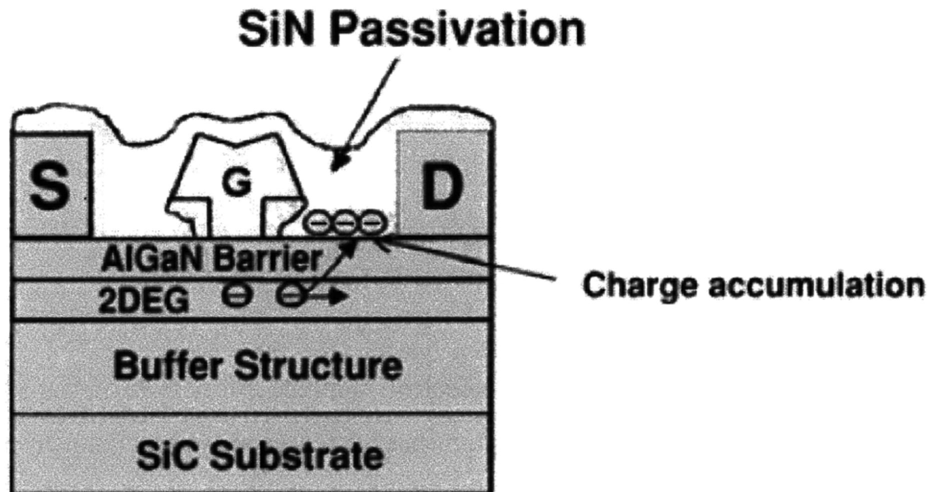

Figure 1-2. Degradation mechanism in AlGaN/GaN HEMT under high stress condition [16].

gate and drain [16]. As shown in Figure 1-2, hot electrons can gain enough energy to escape the channel and get trapped at the surface. These electrons form a so called virtual gate [45]. In [24, 46], Valizadeh et al. have suggested that degradation both during DC and RF stress is related to hot electron trapping at the surface in the drain extrinsic region. This hot electron trapping at the surface is more pronounced in unpassivated devices. Many authors have reported that SiN passivation largely alleviates this problem and improves reliability [14, 17, 19, 47-48]. They also proposed that in RF stress, hot electrons can be also trapped under the gate metal due to the randomizing effect of RF signal, resulting in a threshold voltage change.

Sozza et al. have proposed that it is not only hot electron trapping but also hot electron induced trap generation at the surface region between gate and drain that is the origin of device degradation [15]. They have shown that frequency dependent g_m dispersion after a long term hot-electron type of stress test (V_{DS}=25 V and P_d=6 W/mm). Because the activation energy of the trap after device degradation was the same as that of a fresh device, they have postulated that the same types of traps in a fresh device are increased during electrical stress. Because degradation in OFF-state was smaller than that in ON-state, they have attributed this increase in trap density to hot electron effects. Similarly, Mittereder et

al. have observed that current collapse increases after a bias stress test [14]. The current collapse is a temporary decrease of drain current after applying high voltage to the device, which is a widely observed trapping effect in GaN HEMT. They have measured absorption spectrum of trapped carriers, and they concluded that the same types of traps are involved in the current collapse after the device degradation [14]. The impact of device degradation on the trapping effects is discussed in more detail in Section 1.3.4.

However, the detailed mechanism for hot-electron induced formation of traps is still not well known, and few solutions to this problem have been proposed to date. In most of the papers that suggest hot electrons as the main cause of the degradation, little experimental or theoretical modeling of the phenomena is provided in detail. For example, to the best of our knowledge, clear signature of hot-electron effect such as correlation between degradation and $1/(V_{DS}-V_{DSsat})$ has not been reported in GaN HEMT degradation. In fact, there are a few evidences that show hot electron effects are not the sole dominant degradation mechanisms in GaN HEMTs. Stressing a device in OFF-state can significantly degrade the device [11, 17, 49]. Although hot electrons from the gate electrode can exist in the OFF-state, these are not the kind described above (hot electrons from the channel). Also, it has been found that significant amount of trapping can be induced by high electric field without any hot electrons [50]. Moreover, the fact that degradation is usually thermally activated with a high activation energy (>1 eV) implies that hot electron related effects are not the only degradation mechanisms in GaN HEMTs.

1.3.3. Inverse piezoelectric effects

After extensive stress experiments performed in our previous studies, we concluded that the main mechanism of device degradation observed in our experiments is inconsistent with hot electron effects [26]. Based on our experimental results, we proposed a new hypothesis that crystallographic defect formation through the inverse piezoelectric effect is a major cause of degradation in the GaN HEMT that we tested [10, 26].

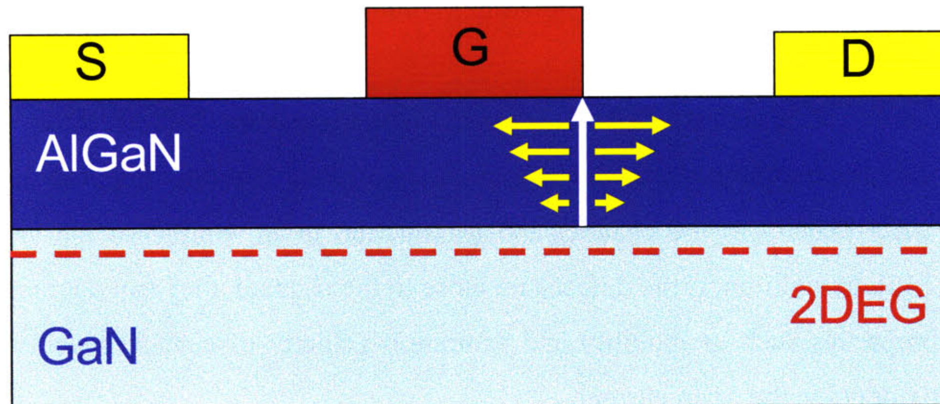

Figure 1-3. Inverse piezoelectric effect at the gate edge in the drain side of GaN HEMT. The vertical and horizontal arrows represent vertical electric field and mechanical stress, respectively.

GaN and AlN, as a result AlGaN also, are strong piezoelectric materials. In fact, it is this strong piezoelectricity that makes it possible to achieve high carrier density ($>10^{13}/cm^2$) without doping any layer in an AlGaN/GaN heterostructure. However, piezoelectricity also works in a reverse way: under an electric field, a piezoelectric material gets mechanically stressed either in compressive or tensile way depending on the direction of the electric field. This is called the inverse (or converse) piezoelectric effect. In normal operating bias conditions where high V_{DG} is applied, the vertical electric field at the drain-side gate edge in the AlGaN barrier layer can be high enough to produce significant amount of tensile stress in this region. This is shown in Figure 1-3. Because of lattice mismatch between AlGaN and GaN, the AlGaN barrier layer is already under tensile strain even in the absence of an electric field, and a certain amount of elastic energy is stored in it. The tensile stress that is caused by the electric field through the inverse piezoelectric effect adds on top of this initial stress due to lattice mismatch. As a result, elastic energy density in AlGaN layer increases. If the total elastic energy density in this area exceeds a critical value, crystallographic defects such as dislocations or cracks can be formed. In previous studies, XTEM analysis has confirmed the existence of prominent crystallographic defects after high voltage stress [20, 51]. It was also found that the defects are much more pronounced on the drain side than that on source side. In fact, in many cases the source side was not

damaged at all. Chowdhury et al. have shown that the amount of the defect in the drain side correlates well with the amount of degradation in drain current during the stress tests [51].

In this model, the generated defects behave as trapping sites for electrons, and they therefore increase trapping effects such as current collapse. Electron trapping results in a reduced carrier density in the channel and a reduction in I_D, similar to the virtual gate formation [45]. In addition, if the defects are close to the channel, they can degrade electron transport properties such as mobility and saturation velocity of channel electrons, which permanently degrade the drain current.

In this thesis, extending our previous research [26], the inverse piezoelectric effect driven degradation mechanism is investigated in greater detail. More evidence that supports this hypothesis is provided. Also, a theoretical model on this degradation mechanism is presented.

1.3.4. Trapping effect in GaN HEMT

It has been reported that GaN HEMTs suffer from prominent trapping effects [52]. As mentioned above, the so-called "current collapse" – a recoverable temporary reduction in drain current after the application of high voltage – is one of these trapping effects. It is widely believed that under high voltage, surface states between the gate and the drain trap electrons that tunnel from the gate metal [45, 50, 53]. As mentioned above, hot electrons from the channel can also be trapped at the surface [16]. These trapped electrons at the surface or AlGaN barrier changes electrostatics such that they deplete the channel carrier in the extrinsic drain resulting in a reduction of the drain current [45]. Koley et al. have measured the surface potential in the extrinsic region by Kelvin probe technique, and they found that applying high voltage accumulates negative change on the surface [50]. They have postulated that trapped electrons come from the gate and are not hot electrons from the channel because no current was flowing in the channel during the high voltage

application in their experiment. Although trapping at the surface or inside the AlGaN barrier layer is believed to be dominant, it has also been postulated that electron trapping in the GaN buffer can cause current collapse [52]. This type of current collapse was not observed in devices on conducting buffer layer [52]. Another hypothesis is that the current collapse is caused by a reduction of tensile strain in the extrinsic device under negative gate bias [54].

It has been widely observed that trapping in GaN HEMTs has a slow nature. Although fast component exists [55-56], the recovery time from the current collapse is generally long (>100 s or even a few days) [10, 45, 50]. This means that detrapping of trapped electrons is generally very slow. SiN passivation is known to reduce various trapping-related problems [14, 48, 50]. This is due to a decreased trap density by passivating surface states as well as by making surface states inaccessible to electrons that tunnel from the gate [45]. However, a detailed mechanism of how surface passivation reduces trapping effects is still not clear. Although there has been an effort to make dispersion-free devices by using a special cap structure [57], sometimes even without passivation [58], surface passivation is seen to be essential to alleviate trapping effects and improve device reliability in most devices.

Although the current collapse is seen as a performance limiting factor because it results in limited RF performance compared to DC performance, it is also one of the most serious reliability problems. With various methods such as DLTS, gate-lag measurement, and frequency dependent g_m dispersion, it has been widely seen that trapping effects increase after device degradation [10, 13-14, 17-18, 25, 48, 59]. This increased trapping changes the performance of the device, and thus its reliability. As trapping effects are important in understanding device degradation mechanisms, in this thesis, we study the detailed nature of the trap dynamics in GaN HEMT devices. For this, we develop a new methodology to analyze trapping and detrapping behavior in GaN HEMT. We try to identify physical location, energy level, and trapping/detrapping time constants of the traps that exist in fresh devices as well as the traps that are produced during device stressing in various conditions.

1.4. Project goal and thesis outline

This thesis presents an extension of our previous research [10, 26]. In this thesis, we carry out a systematic study to understand the detailed physical origin of electrical degradation in GaN HEMTs. While our previous work mostly focused on reliability experiments in simple stress conditions in order to find a high-level picture of device degradation mechanisms [26], in this thesis, we investigate electrical degradation of GaN HEMTs at a greater detail. This includes stress parameters that have not been considered, for example mechanical strain; figures of merit that were not previously discussed, such as gate current; degradation of DC and RF figures of merit in RF reliability experiments; and detailed analysis of trapping behavior. In particular, the piezoelectric effect induced defect formation mechanism is discussed in greater depth. This includes an extensive discussion on the critical voltage and the development of a physical model for degradation.

With a systematic approach, we look for a more complete picture of fundamental mechanisms underlying the device failure. For this, new characterization techniques are developed. Upon finding out the physical mechanisms, we attempt to identify process and device design changes to improve electrical reliability of GaN HEMTs.

This thesis is organized as follows: In chapter 2, GaN HEMT devices that are used in this study are briefly described. The MIT reliability test chip is also introduced. Following, the description of experimental setup and characterization methods as well as stress schemes is discussed.

In chapter 3, the main experimental results are presented. Following the summary of our previous work, the degradation of the gate current under various stress conditions is presented. Then, the dependence of the critical voltage for device degradation on various parameters is extensively discussed. Finally, the impact of external mechanical strain on device reliability is shown. In chapter 4, the physics of the inverse piezoelectric effect is

discussed in detail. A simple theoretical model is presented and compared with experimental results.

In chapter 5, a detailed analysis in trapping behavior before and after electrical stress is discussed. Results from trapping and detrapping experiment under a variety of conditions are shown. We look for detailed nature of traps in terms of the trapping/detrapping time constant, activation energy, and physical location. Also, in order to show that the physical mechanism that we find is relevant to real RF performance degradation, RF and DC reliability experiments are compared. Finally, the conclusions of this research are presented in chapter 6. Based on our conclusion, device design guidelines to improve reliability are suggested .This chapter also includes recommendations for further research.

Chapter 2. Experimental

2.1. Introduction

This chapter starts with an introduction of the GaN HEMTs that are investigated in this work. The MIT reliability test chip that has been designed in the course of this research is described. Finally, the experimental setup, a device characterization suite and various characterization techniques, and different stress test schemes and stress conditions examined in this work are presented.

2.2. Devices and MIT reliability test chip

Figure 2-1 shows a schematic cross section of a GaN HEMT for this study [35]. These devices are fabricated by our industrial collaborators, TriQuint Semiconductor under their own design rules. The AlGaN/GaN heterostructure is grown on a SiC substrate. GaN buffer and active channel layer is followed by AlGaN barrier layer below which 2-D electron gas is confined. Between the surface and the AlGaN layer, there is a thin GaN cap layer. Typical thickness and Al composition in the AlGaN layer is 16 nm and 28%, respectively although these values slightly change from wafer to wafer. Source and drain ohmic contacts are formed by thermal annealing, and the surface is passivated by a PECVD SiN layer. The Pt/Au based Schottky gate has an integrated T-shaped field-plate, and some devices have incorporated a second field plate that is connected to the source [9].

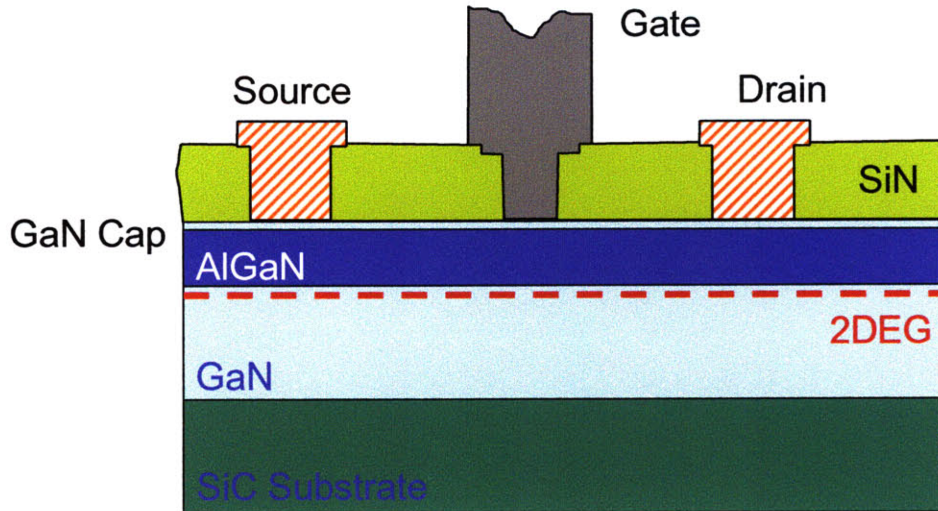

Figure 2-1. Schematic cross section of a GaN HEMT.

Standard devices that are investigated in most of our reliability experiments have 0.25 um gate length. In order to prevent oscillations that are typically seen in large devices and obtain reliable measurement data, these standard devices have relatively small gate width of 2x25 um. Source to drain spacing is 4 um, with the gate centered in between. A typical unstressed TriQuint device with 4x100 um gate width has a current-gain cut-off frequency f_T around 40 GHz, and I_{Dmax} is about 1.2 A/mm. The output power is about 9.8 W/mm, and PAE is 55 % at 10 GHz when the device is biased at 40 V [35].

In order to carry out a systematic study of reliability, a reliability test chip was designed (Figure 2-2) [26]. The major flat of the wafer is the $\{10\underline{1}0\}$ plane, and the gate fingers of the devices are parallel to the $<11\underline{2}0>$ direction. Each chip is about 10 mm^2 in size and contains 5 standard devices that are described above. Most devices are finished before via process. These devices sit side by side, enabling fair comparison for different stress experiments on multiple devices. In addition to standard devices, there are other HEMTs with different geometries in this chip:

- Gate length: standard, 2x, 5x, 10x, and 20x of standard device
- Gate width: 2x12.5 um, 2x25 um, 2x50 um, and 2x100 um

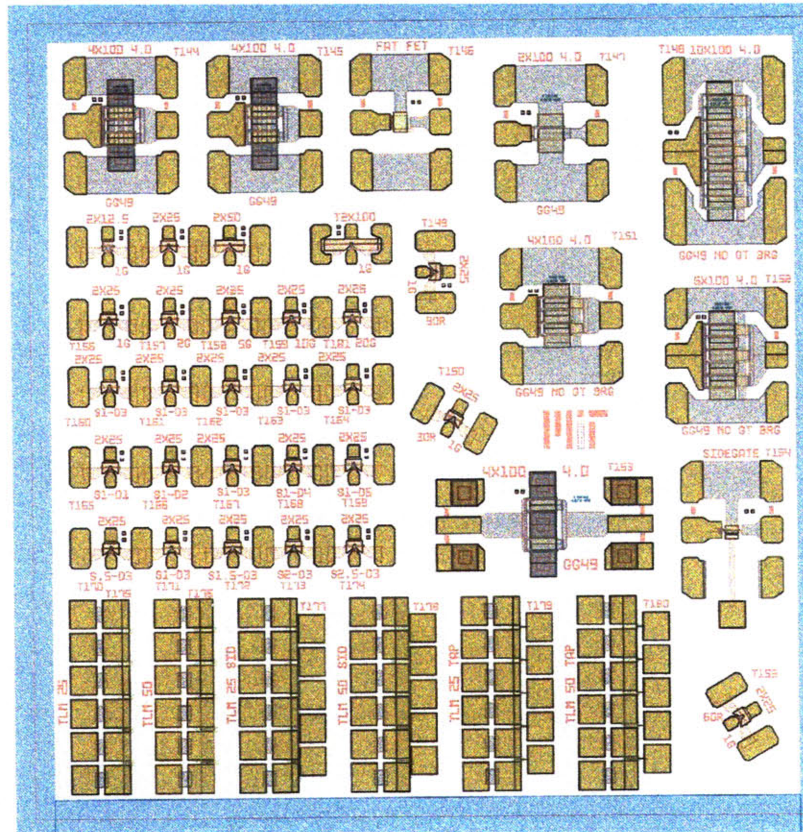

Figure 2-2. MIT reliability test chip.

- Number of fingers with 100 um unit finger width: 2, 4, 6, and 10
- Gate to drain gap: 1, 2, 3, 4, and 5 um
- Source to gate gap: 0.5, 1, 1.5, 2, and 2.5 um
- Gate orientations with respect to the major flat: 0, 30°, 60°, 90°
- HEMT with a side-gate: to probe the hole current due to impact ionization
- FATFET: a long gate length FET to measure Hall mobility
- Microstrip: 4x100 um

In addition, the reliability test chip also includes different types of Transmission-Line Method (TLM):

- Standard TLMs: W=25 um, 50 um. L = 3, 7, 11, 15, 19 um
- Tapped TLMs: W=25 um, 50 um. L = 3, 7, 11, 15, 19 um. A tap is used to monitor the voltage at the midpoint of TLM.
- Sidegate TLMs: W=25 um, 50 um. L = 3, 7, 11, 15, 19 um. A side gate is used to probe the hole current due to impact ionization.

With these variations in HEMTs and TLMs, we can investigate the effect of various design aspects on reliability. Also, we can find out where the degradation takes place, what the key signature of degradation is, and what the key dependencies (current, voltage, etc) of degradation are. This test chip is incorporated in the regular process development mask used in TriQuint Semiconductor. 41 of these chips are fabricated in every wafer that they produce. Chips from different wafers are cut out and sent to MIT for this study.

2.3. Reliability test experiment

The same approach as in the previous work [26] is also adopted to analyze the device degradation. More details of stress methods and characterization techniques are presented below, but general procedure of a stress experiment is as follows: First, we fully characterize a device before stressing it. This full characterization includes complete I-V characteristics over a certain range: output, transfer, gate, and subthreshold. From these measurements, a variety of device parameters are extracted. Then, we stress the device in a certain stress scheme, and once in a while (typically every 1 or 2 minutes), we stop stressing the device and run a coarse device characterization which extracts a few important figures of merit such as such as V_T, I_{Dmax}, R_S, R_D, and I_{Goff}. Both of these full and coarse characterizations are proven to be benign enough not to change the device characteristics or degrade the device for repeated measurements [26]. After the short characterization, we resume stressing, and this stress-characterization cycle repeats. Finally, after the stress test or in some experiments at some of the important points during the stress experiment, for example once every 30 minutes, full characterization is again performed. In this way, we can track how the device performance parameters as well as device characteristics changes as the device is stressed. In some cases, special characterization such as trapping and detrapping analysis is performed during the course of the experiment.

2.3.1. Experimental setup

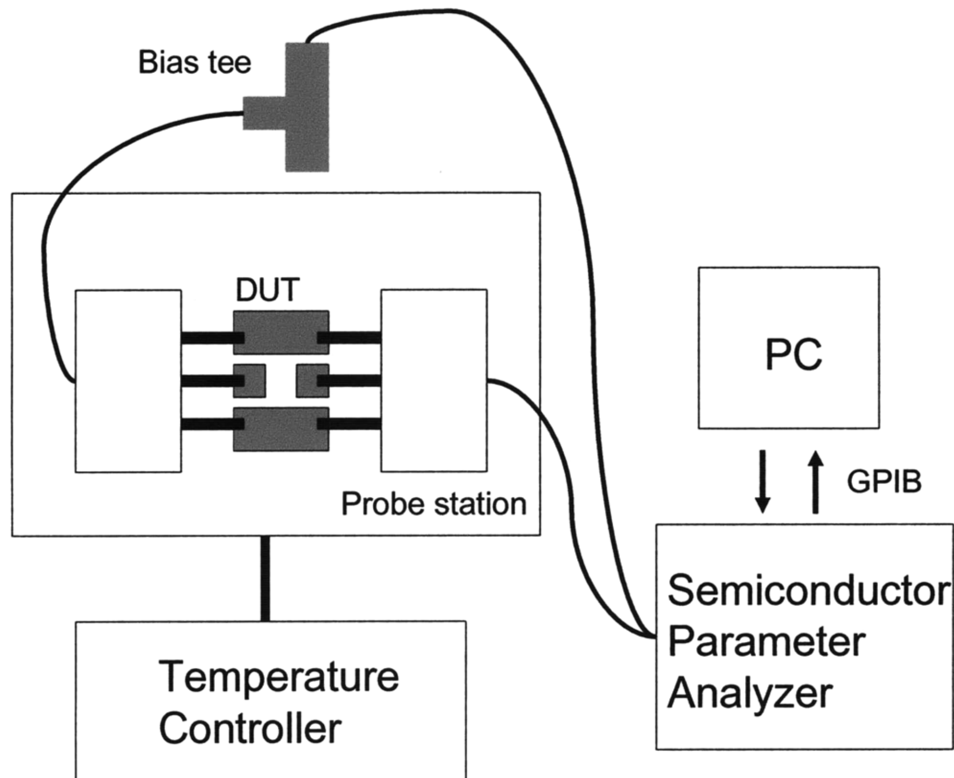

Figure 2-3. A schematic diagram of the experimental setup.

The experimental setup for DC stress experiments is similar to our previous work [26]. A schematic diagram of the experimental setup is shown in Figure 2-3. It consists of a semiconductor parameter analyzer and a Cascade Microtech probe station. Two different parameter analyzers are used: HP4155 semiconductor parameter analyzer with a HP41501A high power expander unit and Agilent B1500A semiconductor parameter analyzer. The maximum current capability is 1 A for both instruments. The temperature of the base plate of the probe station is controlled by a Temptronic TP03000 ThermoCheck system. This temperature controller unit regulates the base plate temperature from -60°C to 200°C. An enclosed gas chamber enables performing measurements with the device under nitrogen and under controlled illumination conditions. Because of a high gain and high current of the device that we test, in most cases, we use Picoprobe GSG 125 um microwave

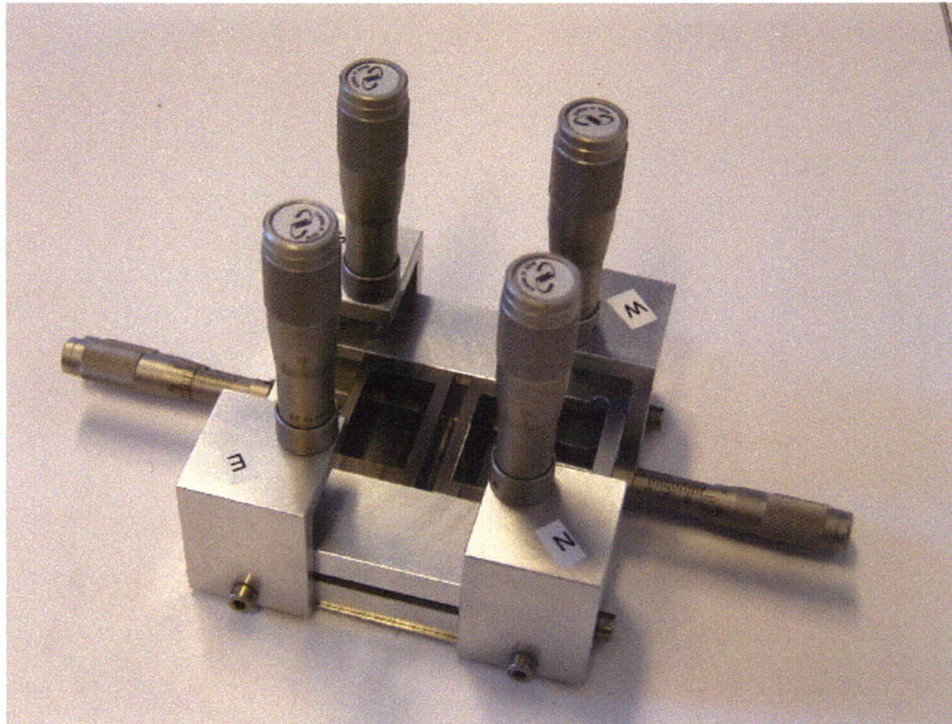

Figure 2-4. A jig used for applying external mechanical strain during stress experiments.

probes with a bias tee installed in the gate side in order to avoid any oscillations that may occur during the measurements. The parameter analyzer is controlled by a Windows OS PC through a GPIB connection. Some experiments are performed in air or under the microscope light illumination.

For the stress tests under external mechanical strain (Chapter 3), experiments have been performed on a jig that is designed in our group (designed and assembled by Ling Xia). This jig is shown in Figure 2-4. This device consists of 4 micrometers that apply vertical stress to bend a semiconductor chip. Two sets of jaws apply forces from the top and the bottom of the chip. The location of these jaws is controlled by 4 horizontal micrometers. Depending on the relative location of the jaws, compressive and tensile strain can be applied. This jig is placed on the probe station, and the device is measured through DC probes in this type of experiments.

The RF reliability experiments in this thesis have been performed in the RF reliability test lab in TriQuint Semiconductor, Richardson, TX. For RF experiments, a single stage 4x100 um MMIC amplifier chip is mounted on an RF fixture and wire-bonded to be connected to a life test system. The system consists of simple DC supplies, an RF source unit, and a temperature controller. All these instruments are controlled by a Windows based PC through GPIB. A brief version of device characterization suite is incorporated into the RF stress test system to measure important DC figures of merit. Equipment limitations preclude a more extensive device characterization during RF stress experiments.

Unless specified, all of our experiments are done at room temperature, with the device inside a dark chamber with nitrogen gas injected into it.

2.3.2. Device characterization

One of the keys to examine physical degradation mechanisms is a detailed characterization of the device under stress test. In our stress experiments, a device characterization suite automatically measures various device parameters before, during, and after the stress tests. The characterization suite has been upgraded from the previous version [26]. Also, a new version of the characterization suite was implemented for the new semiconductor parameter analyzer (Agilent B1500A). This new version is written in Microsoft Visual C++. Due to a faster response of Agilent B1500A, the coarse device characterization that extracts a few important figures of merit takes less than 10 seconds, and the full device characterization takes less than 30 seconds. Both short and full characterizations are proven not to degrade device characteristics in a significant way. We have previously confirmed that 100 executions of the full characterization do not change any of the electrical parameters that are extracted by more than 2% [26]. The key figures of merit that the characterization suite extracts include I_{Dmax}, R_S, R_D, I_{Goff}, and V_T. These parameters have been selected to provide a view of the impact of stress in the different regions of the device. The definition of key figures of merit is summarized in Table 2-1 although they are sometimes fine-tuned for

Parameter	Definition
I_{Dmax}	Drain current at V_{DS}=5 V and V_{GS}=2 V
R_S	Source resistance measured with I_G=20 mA/mm
R_D	Drain resistance measured with I_G=20 mA/mm
V_T	V_{GS}-0.5V_{DS} when I_D=1 mA/mm at V_{DS}=0.1 V
SS	Sub-threshold slope at V_{DS}=0.1 V and I_D=1 mA/mm
g_{mpk}	Peak transconductance dI_D/dV_{GS} at V_{DS}=5 V
V_{Gpk}	Gate voltage where g_m is maximum at V_{DS}=5 V
V_{Gon}	Gate voltage where I_D=1 uA/mm
I_{Goff}	Gate current at V_{GS}=-5 V and V_{DS}=0.1 V
I_{Gon}	Gate current at V_{GS}=0.5 V and V_{DS}=0.1 V
I_{Dss}	Drain current at V_{DS}=5 V and V_{GS}=0 V

Table 2-1. Definition of device parameters measured by the characterization suite.

different devices or technologies. More detailed information about the definitions of these figures of merit and their measurement details can be found in [26].

As discussed in Section 1.3.4, the current collapse is one of the critical issues in GaN HEMT reliability. Therefore, it is important to characterize current collapse during the course of stress experiments. Traditionally, current collapse has been measured with a pulsed I-V setup in the sub-microsecond range. Not only does this technique require special equipment, but it is also time consuming and hard to implement as part of an automated device characterization suite or life test experiment.

In order to measure current collapse and trap density during stress experiments more efficiently, a simple diagnostic pulse technique was developed [26, 60]. In this technique, we first bring the device under test to its fully detrapped condition. Normally, microscope light illumination for 30 seconds fully detraps trapped electrons caused by electrical stress. After turning off the light, we wait for 30 seconds to resolve a non-equilibrium state that light illumination may have introduced. Then, we measure I_{Dmax} which is the uncollapsed value at this point. After that, we apply a diagnostic pulse. A typical pulsing condition is V_{DS}=0 and V_{GS}=-10 V with 1 second of pulse width. We have proven that this diagnostic pulse does not introduce any degradation in the device but it produces current collapse

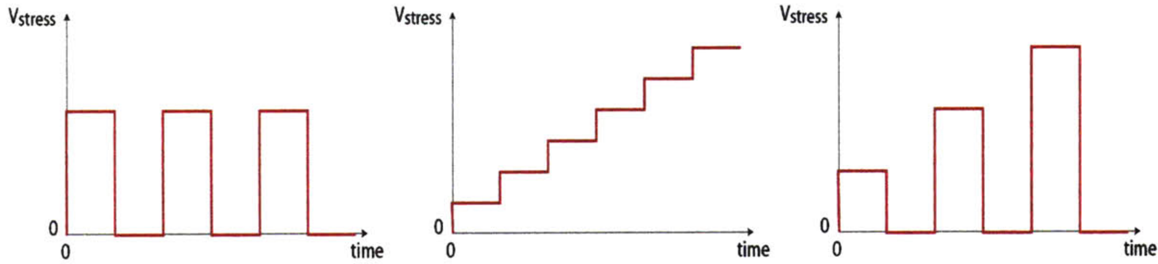

Figure 2-5. Conceptual stress schemes: (from left to right) stress-recovery, step-stress, and step-stress-recovery.

through electron trapping. Right after removing the pulse, I_{Dmax} is again measured. This is the collapsed I_{Dmax}. By comparing the collapsed and uncollapsed I_{Dmax}, the current collapse can be evaluated. Because of the sizable time gap between the removal of the diagnostic pulse and the subsequent I_{Dmax} measurement, the current collapse measured through this technique is usually smaller than the current collapse measurement with a pulsed I-V system. Nevertheless, this technique is found to provide a good sense of trapping behavior in GaN HEMTs because of the slow nature of trapping in GaN HEMTs [60].

The detailed nature of the traps was investigated thorough a current transient technique that we have developed in the course of this study. We have studied trapping transient as well as detrapping transient after current collapse being introduced by various pulsing conditions. This current transient is measured through B1500A's current sampling mode with pre-biasing. The transient response is analyzed by obtaining the time constant spectrum of the transient signal. With the time constant spectrum, we can identify different trapping and detrapping processes under various conditions. More details of this technique are described in Section 5.2.4.

2.4. Stress methodology

In this work, we have performed DC and RF reliability experiments. For DC experiments, several special stress schemes as well as constant bias stress tests are exploited as in our

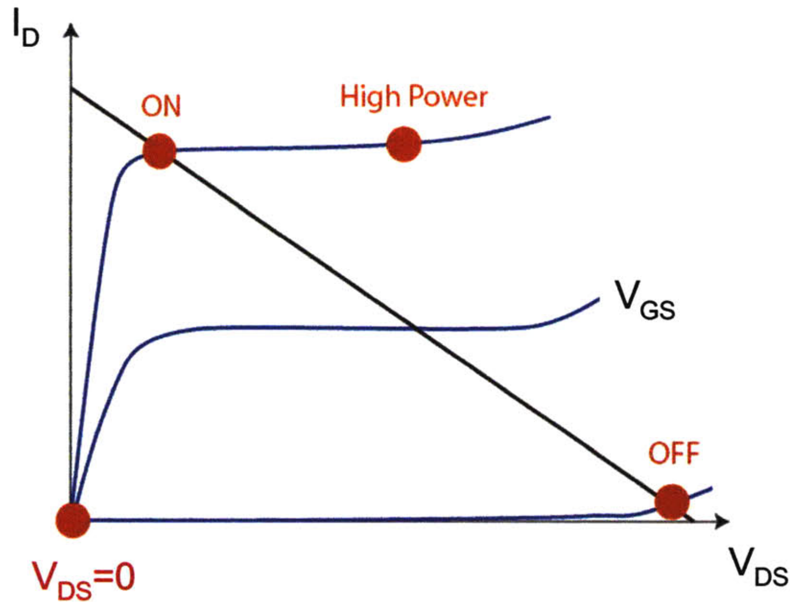

Figure 2-6. Stress bias points: High Power, ON state, OFF state, and V_{DS}=0 conditions.

previous study [26]. These are graphically described in Figure 2-5. *Stress-recovery*-type experiments show how a device degrades and also how it recovers from degradation. In this type of experiment, an electrical stress is applied in the stress phase, and this stress is removed in the recovery phase while the device is characterized periodically (Figure 2-5 left). This type of experiment is especially useful to understand trapping dynamics. As shown in previous studies [26, 61-62], a *step-stress* scheme is a powerful tool to maximize productivity in stress experiments. In this type of test, a stress parameter such as voltage or current is stepped up from a lower value to higher values. The effect of the stress parameter over a wide range of values in a single device can be examined (Figure 2-5 middle). From this type of experiment, we obtain great insight into physical mechanisms especially when we investigate the critical behavior in Section 3.3. Finally, *step-stress-recovery* experiments are carried out (Figure 2-5 right). Usually in this type of tests, we perform the trap-diagnostic characterization at the end of the recovery phase. From this, we can examine when trap formation takes place.

We have studied various stress bias conditions for DC stress: *high-power state* (high V_{DS}, high I_D), *ON-state* (low V_{DS}, high I_D), and *OFF-state* (high V_{DS}, low I_D). In high power condition, we try to simulate the RF power amplifying operation in a more severe way. We have also investigated both ends of the load line, ON-state and OFF-state in order to find the most stressful point during RF operation. In addition, we have focused on the *V_{DS}=0 state* in which negative gate voltage is applied. In this condition, we can stress both sides of the device simultaneously with a high electric field but without any channel current. These conditions are summarized in Figure 2-6 where a typical RF power load line is shown.

Considering the stress time, most of the stress experiments in this thesis are short-term (within a few hours) since GaN-based HEMTs are known to degrade in relatively short period of time. In fact, we observe significant degradation even within an hour of stress. Especially, the step-stress experiment is productive in reducing the stress time. In addition, medium-term stress experiments (on the order of one or two days) have also been performed in order to investigate phenomena which take place in a relatively longer period of time. For RF experiments, some long-term experiments (on the order of several days) have been also performed.

2.5. Summary

In this chapter, we have introduced the GaN HEMT device technology, the MIT reliability test chip, and the stress experiment setup used in this work. In order to measure device degradation efficiently, we have developed a characterization suite that automatically extracts important figures of merit during the stress experiments. In addition, we have introduced two methods to study trapping behavior in GaN HEMTs. Finally, we have described stress test methodologies that were used in this study. The stress conditions for DC and RF stress experiments have been introduced. In the following chapter, experimental results of reliability experiments are presented, and device degradation phenomena are discussed.

Chapter 3. Experimental results

In the previous chapter, we have described the experimental setup, characterization methodology, and stress schemes for studying degradation mechanisms of GaN HEMTs. In this chapter, we present experimental results of various stress tests. First, general results of degradation phenomena from previous work are summarized. On top of the previous findings, degradation in gate current under forward and reverse bias stress are investigated. Then, the critical voltage at which degradation of GaN HEMTs starts to occur is discussed in detail. Various dependences of the critical voltage are examined. Finally, the impact of external mechanical strain on electrical reliability is investigated.

3.1. Summary of key findings from previous work

In previous works, we have carried out a systematic study of the electrical reliability of GaN HEMTs [10, 26]. Under various stress conditions, we confirm that electrical stress results in an increase in R_D and a decrease in I_{Dmax}. Under regular bias condition, R_S changes negligibly. We find that degradation in the OFF-state is comparable to that in the high-power state and that almost no degradation takes place in the ON-state with low voltage. This result suggests that it is not current but mostly electric field that drives electrical degradation. Current appears to be a mild accelerating factor, but it is not clear whether its role is through supplying hot electrons or increasing junction temperature. From the experiments on TLMs, we also confirm that ohmic contacts are not significantly degraded during device operation with high current.

Step-stress experiments in the V_{DS}=0 state reveal a clear onset for I_{Dmax} and series resistance degradation, which we define as the critical voltage (V_{crit}) for degradation. This critical voltage is found to be higher under ordinary bias conditions, high-power state and OFF-state. Also, stress experiments in V_{DS}=0 state confirm that a device can be severely degraded without the effect of hot electrons as we see significant degradation in the V_{DS}=0 state despite negligible current. This result supports our hypothesis that the electric field matters the most in device degradation. This is also inconsistent with the widely believed hot-electron involved mechanisms.

In stress-recovery experiments, we observe strong trapping behavior. By incorporating diagnostic voltage pulses, we confirm that traps are created during device stress. Some of the electrons that are trapped in these traps get detrapped when the device is put at rest, but they get immediately retrapped if the device is again stressed. Trapping behavior can be seen in other stress-recovery experiments in which detrapping is enhanced in the recovery period by light illumination, by applying positive gate voltage, and at higher temperatures.

In many of our experiments, a hot electron mechanism acting alone is inconsistent with our observations. This finding coupled with observations that the electric field is more relevant to device degradation made us postulate an inverse piezoelectric effect related mechanism. We hypothesized that defect formation through the inverse piezoelectric effect and subsequent electron trapping is the main cause of the decrease in sheet carrier concentration. This gives rise to increase in R_D and decrease in I_{Dmax}, eventually resulting in a loss in output power. V_{DS}=0 step stress experiments on different gate length devices and comparison between devices with reduced strain in the AlGaN barrier and the baseline structure support our hypothesis experimentally.

3.2. Gate current degradation

The majority of previous studies on GaN HEMT reliability in the literature, including our own, have mostly focused on P_{out}, I_D, and R_D degradation [10, 15, 17, 20-21, 25]. Although gate current degradation is often also observed in stress tests [17, 22, 27-30], it has not received much attention. In RF power applications, gate current degradation is important because it decreases gain, PAE, and output power by increasing feedback between input and output of the amplifier. In this section, we investigate I_G degradation during electrical stress and show that for reverse bias stress it is caused by the same degradation mechanism that causes degradation in drain current and access resistance. In forward bias stress, Schottky contact degradation takes place due to high current and high temperature.

3.2.1. Gate current degradation under reverse bias

First, we investigate the gate current degradation under reverse bias stress. For this, we perform a step stress experiment in the V_{DS}=0 state. In this experiment, V_{GS} is stepped from -10 V to -50 V in 1 V steps. At each step, the device is stressed for 1 minute. The stress voltage and stress current are plotted in Figure 3-1(left). Figure 3-1 (right) also shows the change in I_{Dmax}, R_S, R_D, and I_{Goff} as a function of stress voltage. As previously found, significant degradation in I_{Dmax}, R_S,

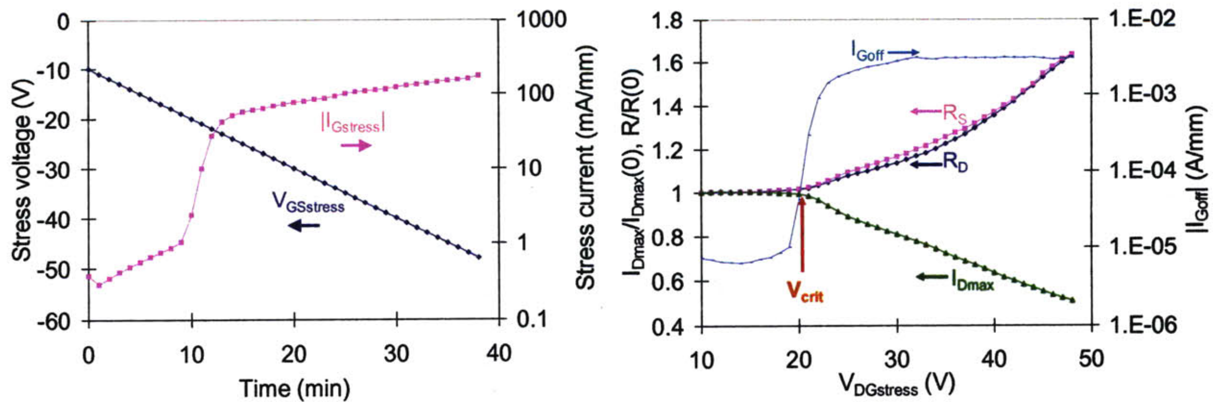

Figure 3-1. Stress condition (left) and the change in I_{Dmax}, R_S, R_D, and I_{Goff} (right) in a V_{DS}=0 step stress experiment at room temperature. V_{GS} is stepped from -10 V to -50 V in a 1 V step. At each step, the device is stressed for 1 minute.

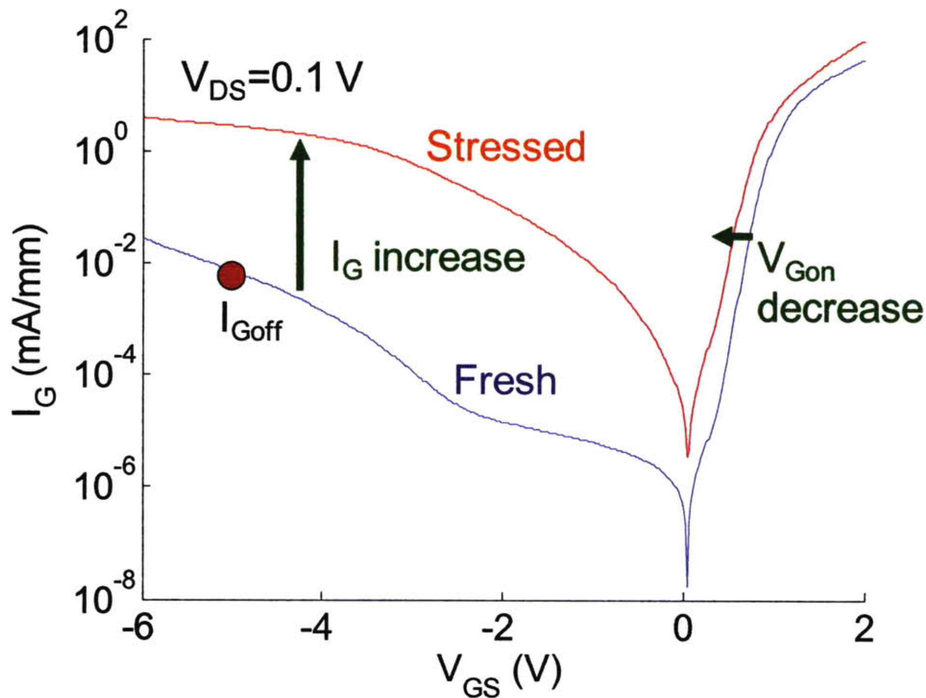

Figure 3-2. Gate current characteristics at V_{DS}=0.1 V before and after the experiment of Figure 3-1.

and R_D suddenly occurs beyond a critical voltage V_{crit}. At this same V_{crit} current collapse is found to increase [10]. The impact of device degradation on trapping behavior is discussed in greater depth in Section 5.2. Interestingly, there is also a sharp increase in I_{Goff} of several orders of magnitude at around V_{crit}. Note that this degradation in I_G takes place in a short time (<5 minutes) and is not recoverable. It is important to realize that the bias current that flows through the device during the stress (Figure 3-1 left) is initially small (~0.3 mA/mm), and there is therefore negligible self heating or hot-electron production. Around V_{crit}, this current increases, but by the time I_{Goff} has increased by two orders of magnitude, $I_{Gstress}$ is still below 10 mA/mm. As a result, it is difficult to attribute the sudden degradation that takes place around V_{crit} to hot-electron production or self heating. In addition, in our previous study, we have seen that the stress current at the critical voltage can be several orders of magnitude different [26]. This confirms that this mode of degradation is driven by voltage or electric field and not current.

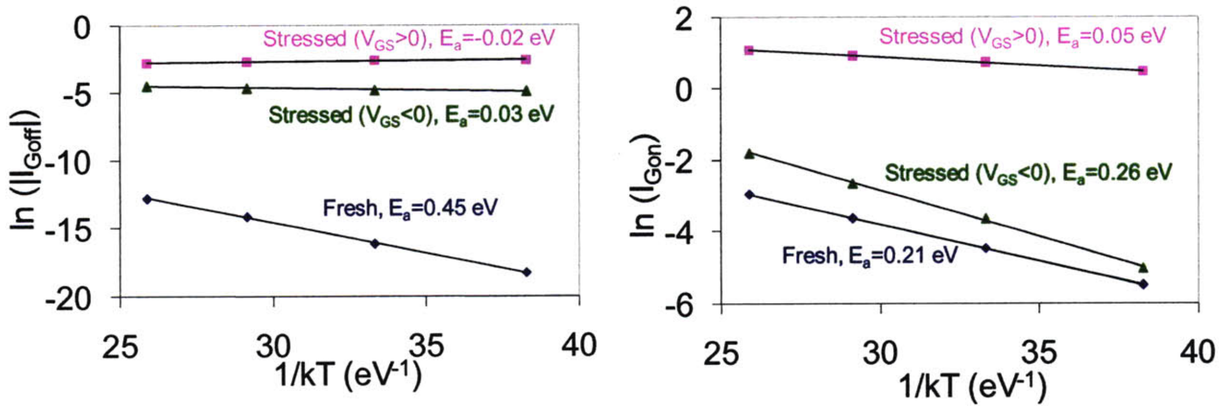

Figure 3-3. Temperature dependence of I_{Goff} (left) and I_{Gon} (right) for a fresh device and degraded devices in the V_{DS}=0 state with a reverse and a forward bias stress.

Figure 3-2 shows I_G-V_{GS} characteristics before and after the stress experiment of Figure 3-1. The reverse leakage current increases by several orders of magnitude, and the forward turn-on voltage V_{Gon} decreases, which suggests a lowering of effective Schottky barrier height. In fact, the activation energy of I_{Goff} significantly decreases from 0.45 eV to 0.03 eV (Figure 3-3). However, the ideality factor in the forward branch (about 2) as well as the activation energy for I_{Gon} (I_G @ V_{DS}=0.1 and V_{GS}=0.5 V) are relatively unchanged.

In a separate step-stress test in the OFF-state, where only the gate to drain region is under high voltage, we find that it is the fraction of the gate current flowing into the drain that is enhanced, indicating that I_G degradation is associated with high fields at the gate edge. Figure 3-4 summarizes the result of the experiment. In this experiment, V_{DS} is stepped from 5 to 45 V while V_{GS} was kept constant at -5 V. It can be seen that I_{Dmax} and R_D start to degrade beyond a critical voltage around V_{DG}=35 V while R_S remains almost unchanged. At around the same voltage, I_{Goff} sharply increases. In this figure, we also plot the two components of I_{Goff}: current from gate to drain, I_{GDoff}, and from gate to source, I_{GSoff} (this current is obtained as the difference between I_{Goff} and I_{GDoff} and is therefore quite noisy). As it can be seen, it is the gate-to-drain component of I_{Goff} that is degraded, and I_{GSoff} is unaffected. This is consistent with the increase in R_D but not in R_S, which indicates that the drain side of the device is degraded, but the source side remains almost

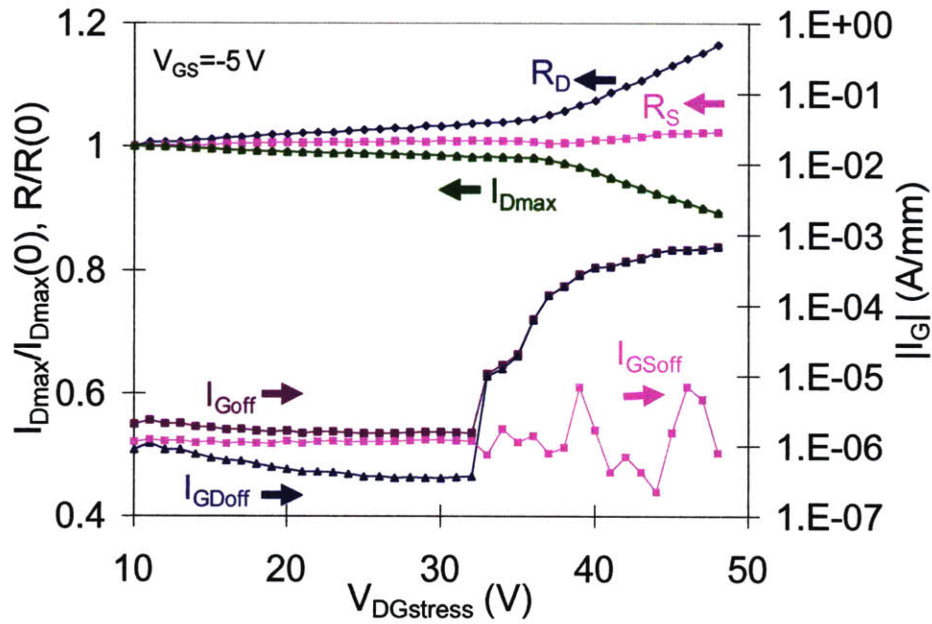

Figure 3-4. Change in I_{Dmax}, R_D, R_S, and I_{Goff} in an OFF-state step-stress experiment (V_{GS}=-5 V). V_{DS} is step-stressed from 5 to 45 V. The two components of I_{Goff} (I_{GDoff} and I_{GSoff}) are also plotted.

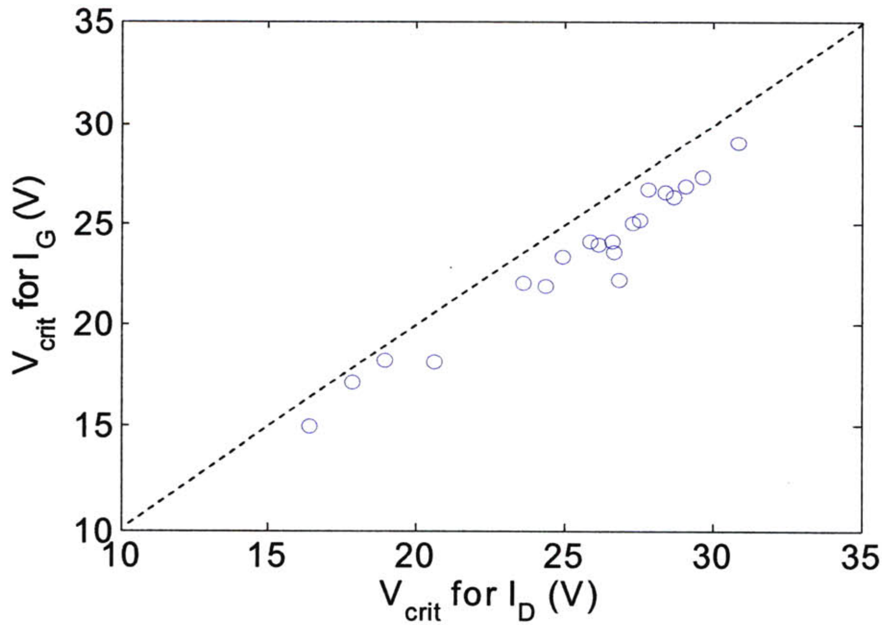

Figure 3-5. Correlation between critical voltage V_{crit} for I_D and I_G degradation. The devices are step-stressed in the V_{DS}=0 state from V_{GS}=-15 V to -45 V in 1 V steps (30 sec/step).

intact. It suggests that a leakage path is formed in the drain side of the device where a high electric field is present. Incidentally, it can be seen in this figure that V_{crit} in the OFF-state is significantly higher than the value of V_{crit} observed under V_{DS}=0 stress [26]. This is addressed more specifically in Section 3.3.1.

In both of the experiments above, there is a correlation between the degradation in drain current and gate current: I_{Dmax} and I_{Goff} start to degrade around the same critical voltage. This suggests that degradation in I_D and I_G have a common physical origin. In order to statistically confirm this, we have performed V_{DS}=0 step stress experiments on 23 devices across a wafer. Figure 3-5 shows V_{crit} for I_D and I_G degradation for 23 devices on the same wafer. V_{crit} for I_D is defined as V_{DG} at which I_{Dmax} becomes 95 % of its initial value, and V_{crit} for I_G is defined as V_{DG} at which a sharp increase in I_{Goff} occurs. This graph shows that there is indeed a close correlation between the onset of I_D degradation and the sudden increase in I_G. This close correlation confirms a common physical origin. Also of interest in Figure 3-5 is to note the broad distribution in V_{crit} across a single wafer. We observe this in other wafers with different device structures. This broad distribution implies a connection between degradation and some slow changing local wafer or epilayer attribute. In our experiments we consistently find that adjoining devices show very well matched values of V_{crit} with a difference that is typically smaller than 1 V.

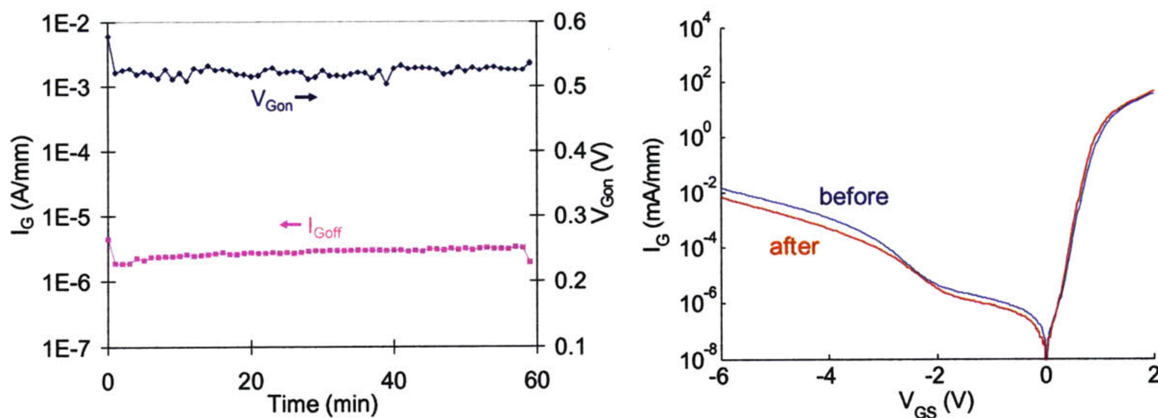

Figure 3-6. Left: time evolution of I_{Goff} and V_{Gon} during a constant stress test in high power condition (V_{DS}=25 V and $I_{Dstress}$=800 mA/mm). Right: change in I_G-V_{GS} characteristics before and after the stress experiment.

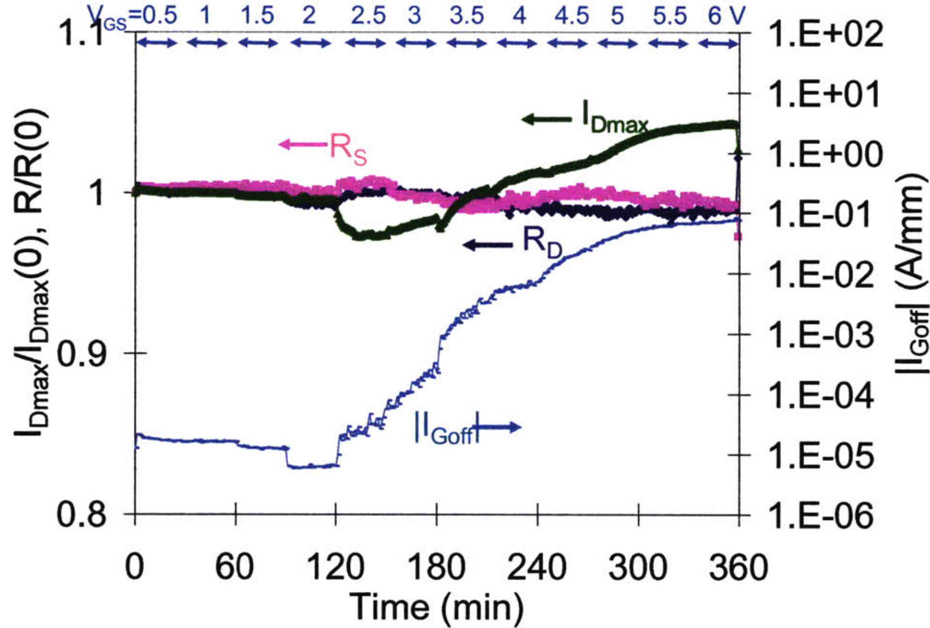

Figure 3-7. Time evolution of I_{Dmax}, R_S, R_D, and I_{Goff} in a V_{DS}=0 step-stress experiment with positive gate bias. V_{GS} is stepped from 0.5 V to 6 V in 0.5 V steps. The device is stressed for 30 minutes at each step.

As discussed in Section 1.3.2, hot electron effects are found to degrade device performance in a variety of devices. In order to investigate the possible role of hot electron effects on I_G degradation under large gate reverse bias in our devices, we have carried out a constant stress experiment in the high power condition, where hot electron effects can be seen most effectively. In this experiment, V_{DS} is set to be 25 V, which is below the critical voltage for I_D degradation [26]. As shown in Figure 3-6, no obvious degradation in gate current characteristics can be seen after 1 hour of stress in spite of the very high current (800 mA/mm). This result suggests that hot electrons are unlikely to be responsible for the gate current degradation in reverse bias stress. The role of hot electrons is discussed in more detail in Section 3.3.2.

3.2.2. Gate current degradation under forward bias

We have also investigated the effect of *forward* gate bias on I_G degradation. This is relevant in RF power applications as V_{GS} can swing rather positive under high input power drive. In order to understand the impact of positive gate bias, we have performed a V_{DS}=0 step stress experiment

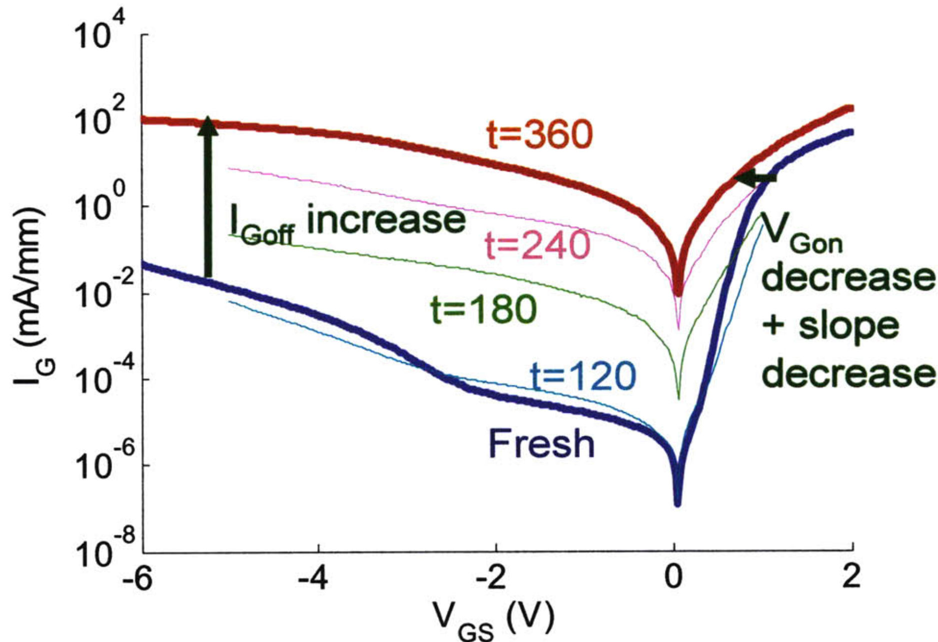

Figure 3-8. Change in the gate current characteristics at V_{DS}=0.1 V in the experiment of Figure 3-7.

with positive V_{GS}. In this experiment, V_{GS} is stepped from 0.5 V to 6 V in 0.5 V steps. The device is stressed for 30 minutes at each step. In Figure 3-7, we show that I_{Goff} starts to increase at around V_{GS}=2.5 V, where the stress gate current $I_{Gstress}$ becomes about 150 mA/mm. This gate current degradation is also irrecoverable. However, unlike for negative V_{GS} stress, in spite of the large increase in gate current, there is negligible degradation in I_{Dmax}, R_D, and R_S, and we did not see an increase in current collapse after the stress. In addition, I_{Goff} degradation is rather gradual but reaching a value of 50 mA/mm at 5 V when $I_{Gstress}$ became 2 A/mm. It thus seems that the degradation mechanism in the forward bias regime is different from that in the reverse bias regime.

Figure 3-8 shows the evolution of the gate current characteristics in this experiment. A reduction in V_{Gon} along with ideality factor degradation suggests that for high forward gate bias Schottky contact degrades severely due to the large gate current. This is different from the change after the reverse bias stress where the Schottky behavior is preserved in spite of a large increase in the reverse leakage current (Figure 3-2). After the degradation, the activation energy of I_{Goff} as well

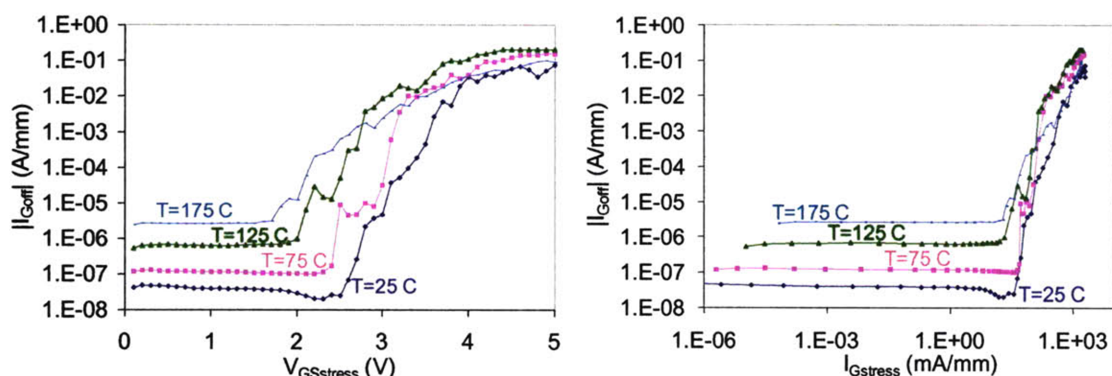

Figure 3-9. Change in I_{Goff} as a function of stress voltage (left) and stress current (right) in V_{DS}=0 step stress experiments at different temperature.

as I_{Gon} became essentially zero (Figure 3-3). This indicates that the Schottky contact is heavily degraded, showing almost ohmic behavior.

Unlike the reverse bias stress, stress current appears to be important for I_G degradation under positive gate bias. Figure 3-9 shows the change in I_{Goff} in V_{DS}=0 step stress experiments with V_{GS}>0 at different temperature. First, it seems that there is similar critical voltage beyond which the gate current degrades, and this critical voltage is thermally activated (Figure 3-9 left). However, if we plot the change in I_{Goff} as a function of the stress current (Figure 3-9 right), the degradation seems to start at around the same critical current around 50 mA/mm. This is again different from the gate current degradation mechanism in reverse bias stress in that current itself does not degrade I_G in the reverse bias stress. In the forward regime, the current appears to be the main degradation driver.

3.2.3. Casual relationship

Since I_G and I_D degradation are closely related, an interesting question arises: is I_G a cause of I_D degradation or vice versa? In order to investigate this problem, we further analyze the data in the experiment of Figure 3-5. First, we do not find any strong correlation between V_{crit} and the stress gate current at V_{crit} (Figure 3-10a). As mentioned in Section 3.2.1, we observe larger variation in

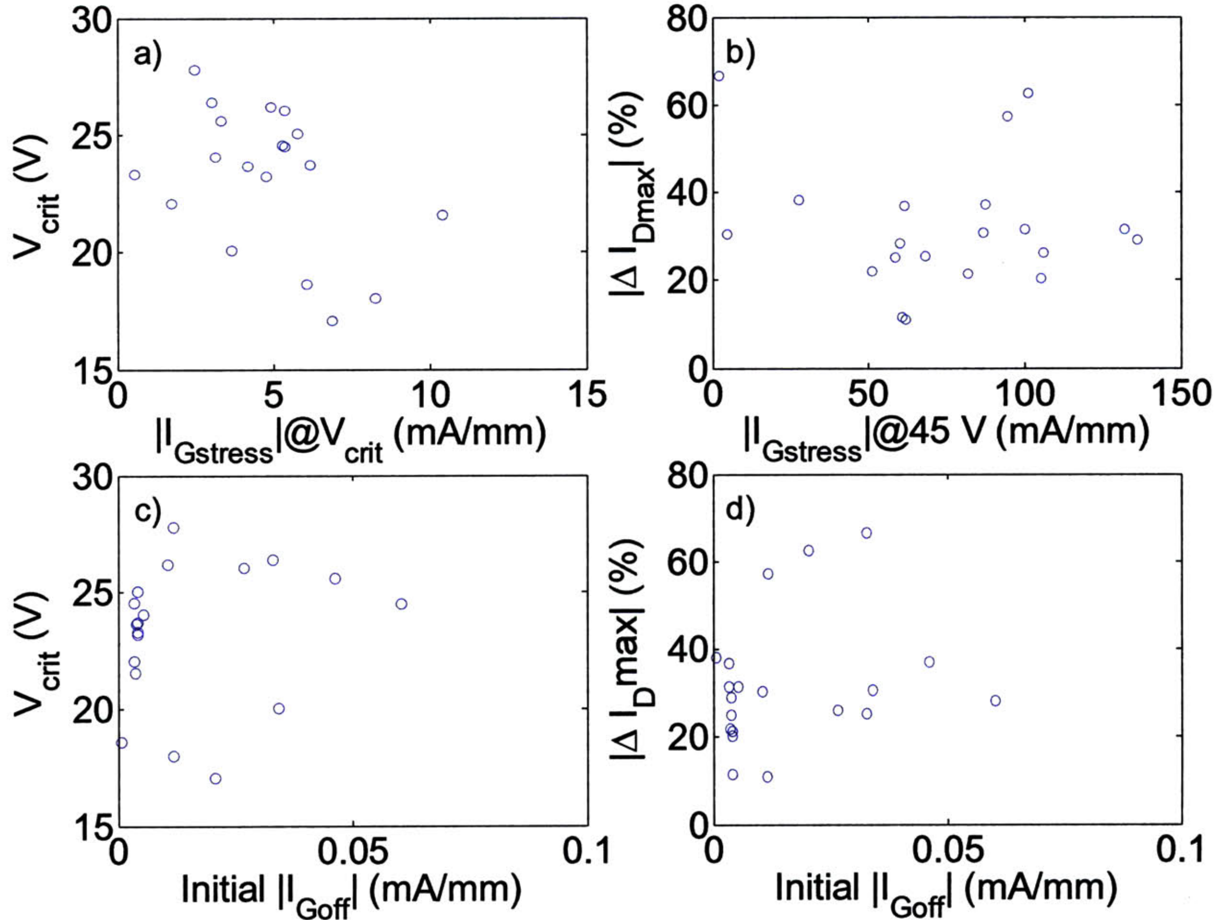

Figure 3-10. Correlation between gate current and degradation in V_{DS}=0 step-stress experiments of Figure 3-5: (a) V_{crit} and $I_{Gstress}$ at V_{crit}; (b) total I_{Dmax} reduction and $I_{Gstress}$ at 45 V; (c) V_{crit} and initial I_{Goff}; (d) I_{Dmax} degradation and initial I_{Goff}.

$I_{Gstress}$ across many different wafers with similar results. In addition, no correlation is found between the total drain current loss after $V_{DGstress}$=45 V and the final stress gate current at this voltage (Figure 3-10b). These two sets of data confirm that the stress current is not a direct cause of degradation in reverse bias stress. Also, we find that the initial gate current is not a predictor of degradation measured by V_{crit} (Figure 3-10c) or the total loss in I_{Dmax} (Figure 3-10d). All of these results indicate that the gate current itself is not a direct cause of device degradation. On the contrary, a large increase in the gate current is a result of degradation when a device is stressed beyond the critical voltage as discussed in Section 3.2.1. More evidences of this are provided in Section 5.2.

3.3. Critical voltage

As we see in Section 3.2.1, device degradation shows a critical behavior. For moderate voltages, there is little change in any of the parameters of the device. Suddenly, over a narrow range of voltage around the critical voltage, the gate current increases by nearly three orders of magnitude and I_{Dmax}, R_S and R_D start to degrade. We observe this peculiar signature for sudden degradation in nearly every device that we have studied under these conditions across many wafers, runs and manufacturers provided that the stress voltage is high enough. This is what we believe is the unique signature of the defect formation mechanism through the inverse piezoelectric effect [10, 12, 26].

In some devices, the critical behavior in I_D and series resistance degradation is somewhat weaker that what has been shown in the previous sections. One such example is shown in Figure 3-11. It can be seen that I_{Dmax} decreases below the critical voltage to some extent. However, this decrease in I_{Dmax} is found to be recoverable and related to temporary carrier trapping. This indicates that this particular device had more traps to begin with, and I_{Dmax} decreased below V_{crit} due to trapping to those pre-existing traps in the device. Beyond the critical voltage, the degradation in I_{Dmax} is accelerated. This is due to trap formation that takes place beyond the critical voltage [10]. In addition, some degree of permanent degradation in I_{Dmax} takes place beyond V_{crit} (not shown here). More detailed discussion on trapping behavior and permanent degradation are presented in Section 5.2.

On the other hand, critical behavior in I_G degradation is found to be sharp and clear in almost all step-stress experiments. As mentioned above, the increase in I_G is accompanied by an increase in trap density [29, 63], and it can be interpreted as a real degradation that involves some physical change in the device. More evidences of this are also shown in 5.2. Because of this clearness in I_G degradation, we mostly focus on I_{Goff} to identify the critical voltage in this section.

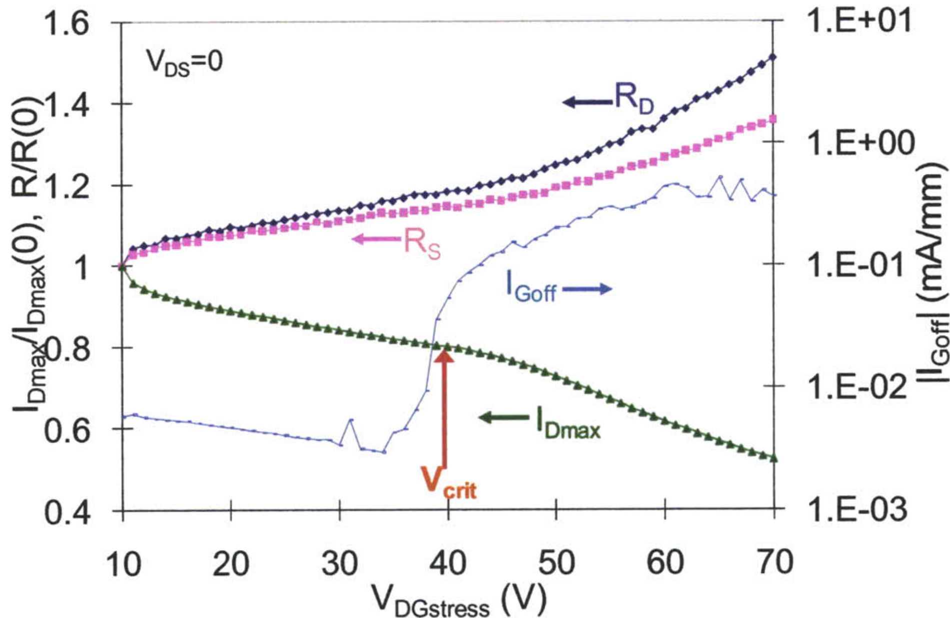

Figure 3-11. Change in I_{Dmax}, R_S, R_D, and I_{Goff} in a V_{DS}=0 step stress experiment at room temperature. V_{GS} is stepped from -10 V to -70 V in a 1 V step. At each step, the device is stressed for 1 minute.

3.3.1. V_{GS} dependence

In Section 3.2.1, we show that the critical voltage in the OFF-state is higher than that in the V_{DS}=0 state. In principle, this difference in critical voltage could result from different values of V_{GS} or different levels of stress current. We have studied both possibilities. First, we investigate the impact of V_{GS}, by step-stressing V_{DS} with V_{GS} fixed at different values. The results are shown in Figure 3-12 with the data for the V_{DS}=0 state as reference (in this case, V_{GS}=-V_{DG}). As one can see, V_{DGcrit} increases as $|V_{GS}|$ decreases. This change in V_{DGcrit} does not result from a change in stress current. For V_{GS}=-10 and -15 V, the stress current was less than 1 mA/mm up to V_{DGcrit}. Even for V_{GS}=-5 V, the stress current was 115 mA/mm at V_{DGcrit}.

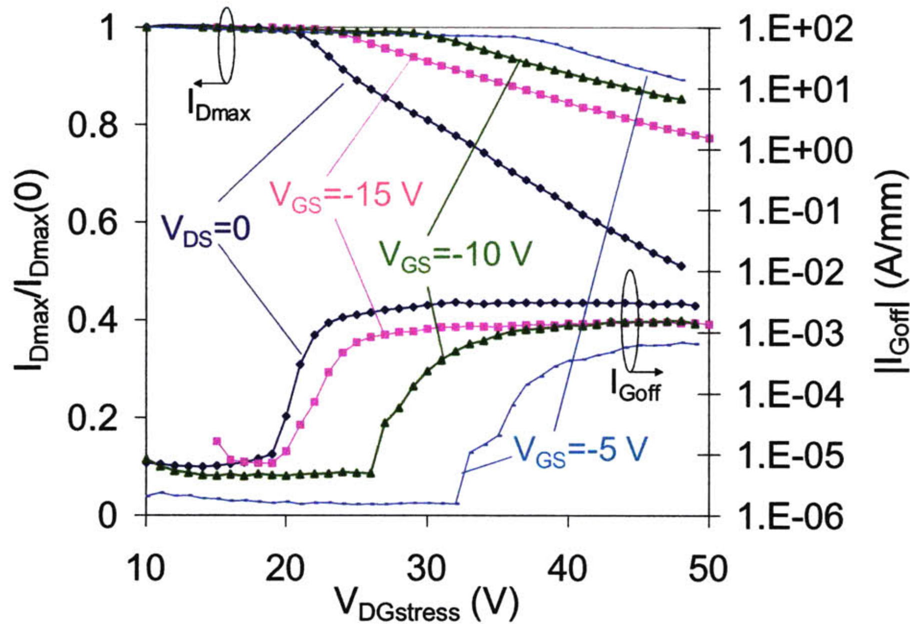

Figure 3-12. Change in I_{Dmax} and I_{Goff} in OFF-state step stress experiments with different V_{GS}. A result of V_{DS}=0 step-stress is also shown. For the OFF state, V_{GS}=-5, -10, and -15 V are investigated. For V_{DS}=0 state, V_{GS}=-V_{DG}. V_{DGcrit} increases as $|V_{GS}|$ decreases.

This is understandable in the context of an inverse piezoelectric effect driven mechanism. In short gate length devices, V_{GS} is known to affect the field on the drain side of the device [64]. A high absolute value of V_{GS} does actually change the field distribution on the drain side and in this way enhances elastic energy density and reduces the critical voltage for degradation. This is examined in more detail with a theoretical model in Chapter 4.

3.3.2. I_D dependence

In Section 3.2.1, we show that high drain current is not a cause of gate current degradation. Further confirmation of the relatively unimportant role of current comes from step-stress experiments in the high-power state with current as a parameter. In Figure 3-13 (left), we can see that the stress current has little impact on V_{DGcrit} for I_{Dmax} except for a softening of the corner at high current (>0.7 A/mm). This soft degradation – decrease in I_{Dmax} below V_{crit} – has been previously observed in the high power state [26].

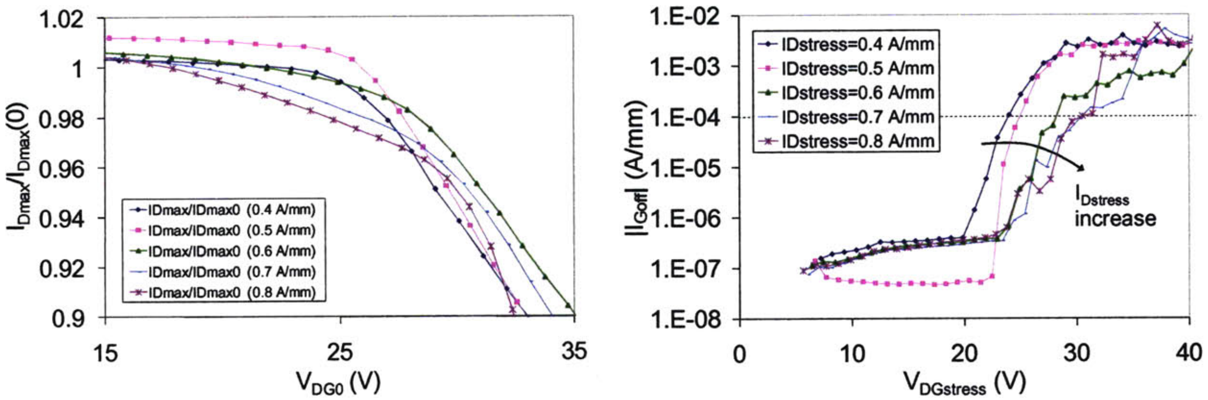

Figure 3-13. Change in I_{Dmax} (left) and $|I_{Goff}|$ (right) in high-power step-stress experiments at different stress currents. V_{DS} is stepped from 5 to 40 V in 1 V step (1 min/step).

As mentioned earlier, I_{Goff} is a better indicator for the critical voltage. In fact, we find that V_{crit} for I_{Goff} shows a *negative* dependence on stress current (Figure 3-13, right). This confirms that current by itself is not a main driver of the type of degradation that is taking place at V_{crit}. This result is clearly inconsistent with hot electron related degradation mechanisms because hot electron production is proportional to the drain current under the same V_{DG}. The critical voltage shows the opposite dependency.

3.3.3. Temperature dependence

In order to understand the impact of temperature on V_{crit}, we have carried out V_{DS}=0 step-stress experiments at different base plate temperatures. Because of negligible self-heating in the V_{DS}=0 state stressing, the device temperature is the same as the base plate temperature. In this experiment, the stress voltage $V_{DGstress}$ is stepped from 10 V to 50 V. Figure 3-14 shows the change in I_{Dmax} and I_{Goff} as a function of $V_{DGstress}$ (only up to 25 V for graphical purposes). As it can be seen, V_{DGcrit} is reduced as the temperature increases. Also, the onset of degradation in I_{Dmax} becomes somehow softer at higher temperatures. This suggests that the soft degradation in I_{Dmax} that takes place in high power state (Figure 3-13) may be due to high channel temperature.

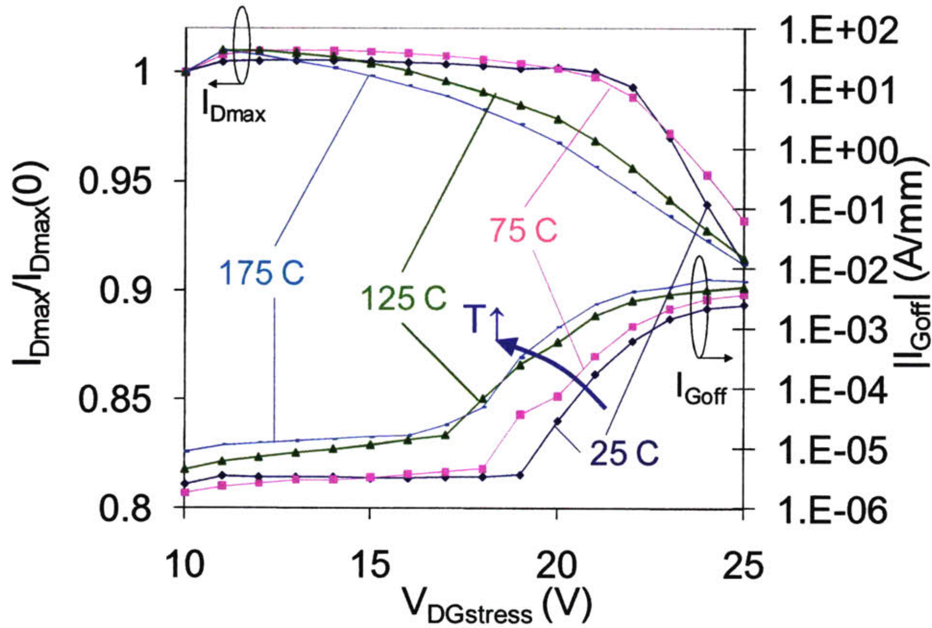

Figure 3-14. Change in I_{Dmax} and I_{Goff} in V_{DS}=0 step stress experiments at different ambient temperatures. V_{DG} is stepped from 10 V to 50 V in 1 V step.

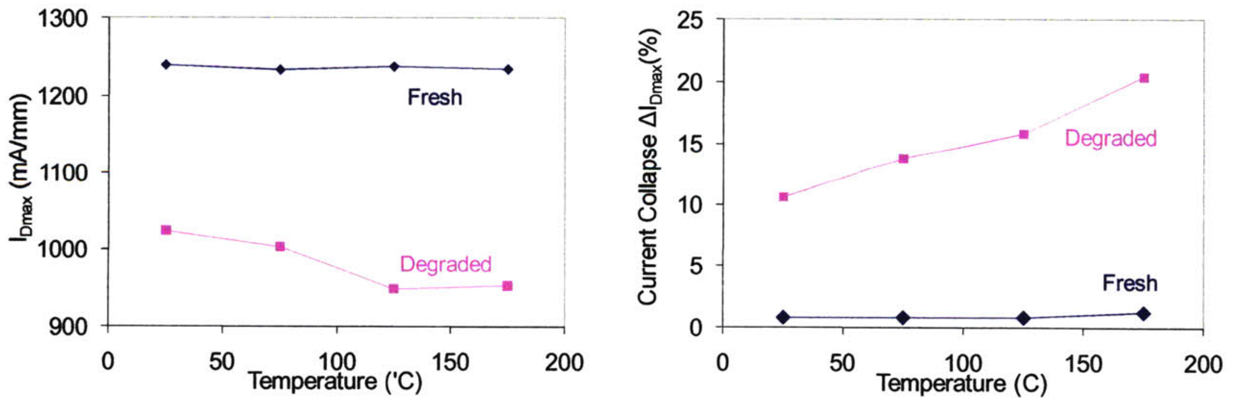

Figure 3-15. I_{Dmax} (left) and the current collapse (right) before and after the V_{DS}=0 step stress experiments in Figure 3-14.

At the end of these experiments, we observe larger degradation in I_{Dmax} at higher stress temperature (Figure 3-15 left). This figure also shows the current collapse before and after the experiments of Figure 3-14. The current collapse was evaluated by applying a 1 second V_{GS}=-10 V diagnostic pulse as described in Section 2.3.2. While fresh devices show negligible current

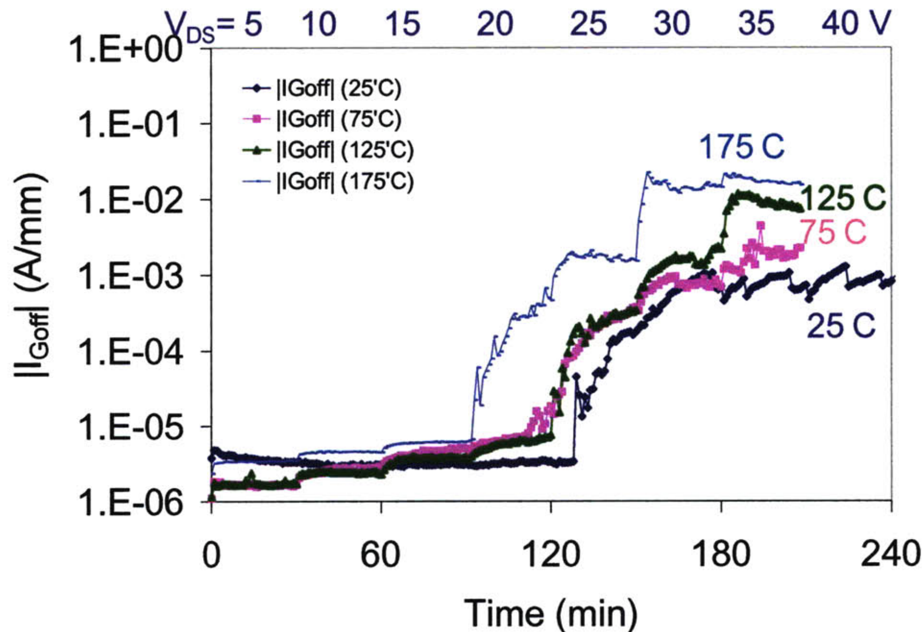

Figure 3-16. Time evolution of I_{Goff} in OFF-state step-stress experiments at different ambient temperatures. V_{DS} is stepped from 5 to 40 V in 5 V steps with I_D fixed at 20 mA/mm.

collapse (~1%), after the step-stress experiments it becomes significantly larger particularly for the devices stressed at higher temperature. This shows that more traps are produced during stress experiments at higher temperatures.

We observe similar behavior in the OFF-state step-stress experiments. In these experiments, V_{DS} is stepped from 5 to 40 V in 5 V steps while I_D was set to 20 mA/mm. The constant current ensures the same amount of power dissipation and thus temperature increase. As shown in Figure 3-16, at higher temperatures, a large increase in I_{Goff} occurs at lower voltages. These results are somehow inconsistent with hot-electron related degradation mechanisms which are expected to be mitigated at higher temperatures. This is because there should be less number of hot electrons at high temperature at given V_{DG} and I_D due to more frequent electron scattering. However, this result does not completely rule out the hot electron hypotheses because the mechanism by which hot electrons degrade the device can be thermally activated with a high activation energy. In that case, larger degradation can occur in spite of fewer hot electrons.

3.3.4. Other dependencies

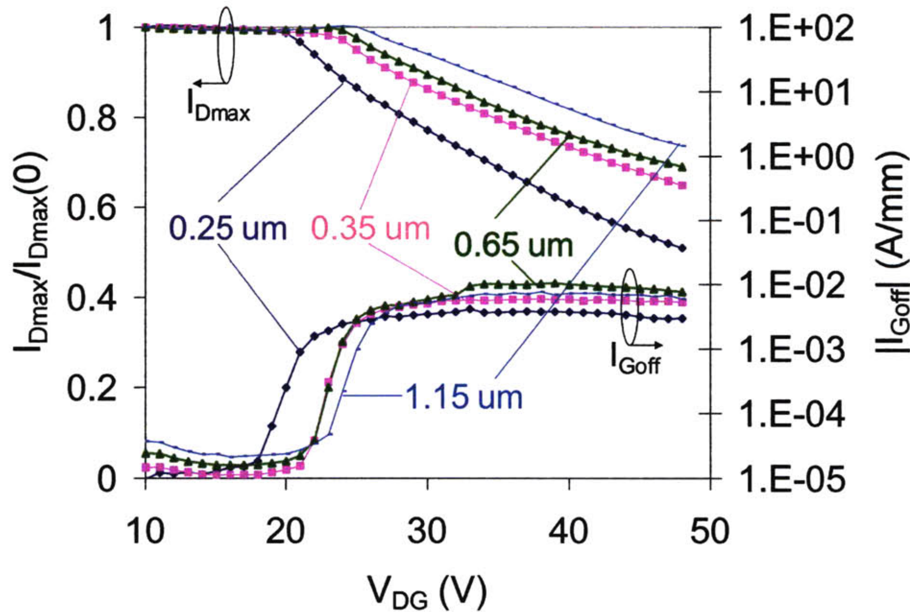

Figure 3-17. Change in I_{Dmax} and I_{Goff} in V_{DS}=0 state step-stress experiments for different gate length devices. As the gate length increases, the critical voltage increases.

We have investigated the dependency of V_{crit} on other variables. First, we confirm the gate length dependence of V_{DGcrit} in V_{DS}=0 state that we observed previously [26]. Figure 3-17 clearly shows that V_{DGcrit} for both I_{Dmax} and I_{Goff} decreases as L_G decreases with stress in the V_{DS}=0 state. This result is also inconsistent with a hot electron related hypothesis [15-16]. First, no hot electrons are produced from the channel current because V_{DS} is zero. Also, to the first order, the electrostatics in the extrinsic portion of the device must be the same regardless of the value of L_G if the gate-drain gap length does not change, as is the case in these devices. Therefore, at a given bias point, the hot electron production from the gate leakage current should be about the same in all these devices. In contrast with this, we do not observe any clear dependence of degradation on L_G in the OFF state and the high power state. In our hypothesis, in the V_{DS}=0 state, longer gate length devices bring the two high-field points at both ends of the gate further apart, resulting in an overall lower elastic energy density in the AlGaN layer near the gate edge. This is discussed in more detail in Section 4.3.5.

We have also studied the impact of device orientation on the critical voltage. For this, we have performed V_{DS}=0 step stress experiments on devices that are rotated 0, 30, 60, and 90 degrees on the wafer. In these devices, we do not find any difference in V_{crit}. Also, we do not observe any differences in different environment such as air and dry nitrogen.

3.4. Impact of strain

At the heart of the inverse piezoelectric effect hypothesis for I_D and I_G degradation is excessive elastic energy in the AlGaN barrier. This can be tested through electrical stress experiments under additional tensile *mechanical* strain. In our model, additional tensile mechanical strain should enhance degradation since it adds on top of the initial tensile stress of the AlGaN barrier plus that introduced by the electric field through the inverse piezoelectric effect. In the following sections, we show that adding tensile mechanical strain enhances device degradation.

3.4.1. Experimental setup

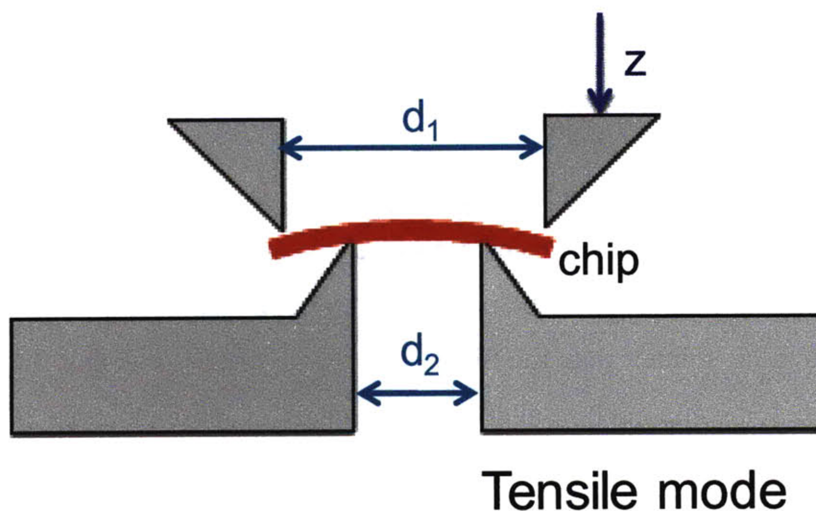

Figure 3-18. A schematic diagram of the jig to apply tensile stress on a chip.

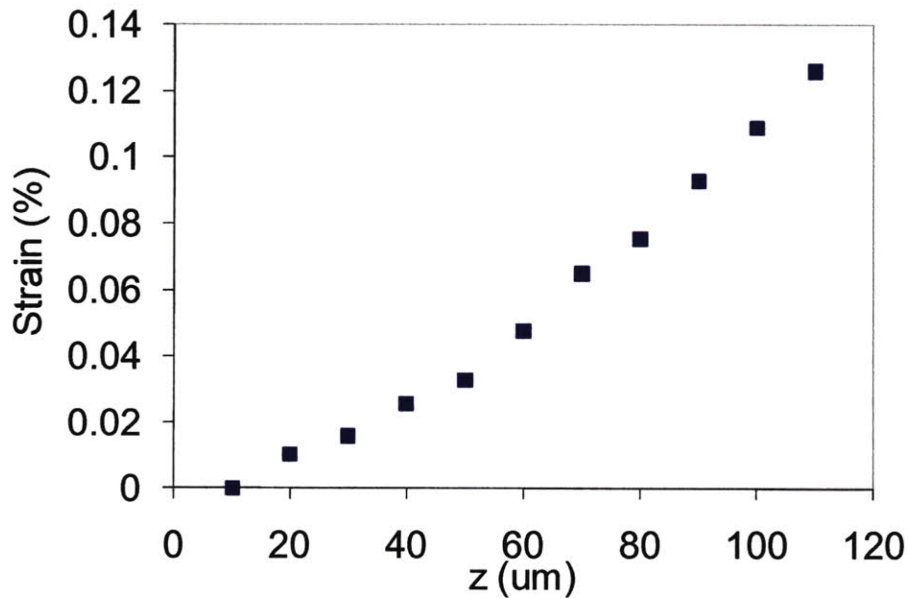

Figure 3-19. Measured strain of a 425 um GaN chip as a function of vertical displacement of micrometers of the jig in Figure 2-4. d_1=4.3 mm and d_2=1.3 mm.

In order to carry out stress experiments under mechanical strain, we use the jig that is introduced in Section 2.3.1. Through this apparatus, we can apply uniaxial mechanical strain on a chip by bending it, as shown in Figure 3-18. The level of bending and applied strain can be controlled by the vertical displacement z of four vertical micrometers that move two upper jaws of the jig up and down. To the first order, the strain on the chip surface is determined by the distance between two upper and two lower jaws (d_1 and d_2), the vertical displacement of the upper jaws (z), and the thickness of the chip.

We first calibrate the strain applied by the jig with a laser reflection system. This system measures the amount of bowing of the chip surface. The strain at the chip surface is calculated from the curvature of the chip surface and the thickness of the chip. Because the AlGaN/GaN heterostructure is much thinner than the SiC substrate, we can assume that this level of strain is applied to the whole heterostructure although the impact of mesa isolation is not clear. Figure 3-19 shows the measured strain as a function of vertical displacement of the micrometers of the jig. It can be seen that the applied strain is almost linear to z. Since we have used the same values

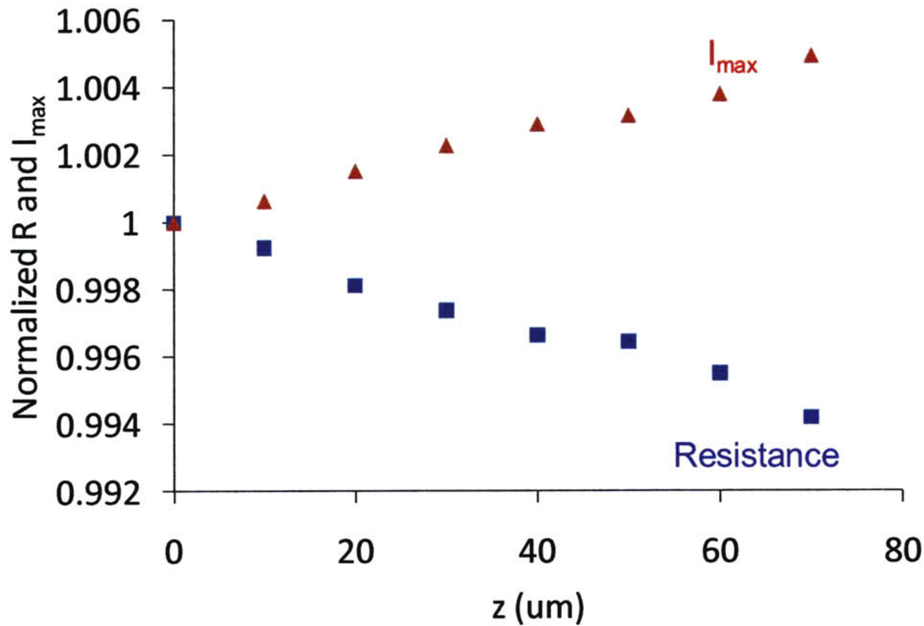

Figure 3-20. Change in sheet resistance and I_{max} as a function of vertical displacement z of the jig.

for d_1 and d_2, we estimated the applied strain from this data and the reading of z from the micrometers.

We have also tested whether the heterostructure and the device are indeed strained by bending the chip. For this, we measure the resistance and the maximum current I_{max} of a TLM structure with L=19 um under mechanical tensile strain. The strain is applied parallel to the channel direction. In Figure 3-20, it can be seen that both I_{max} and the sheet resistance of the TLM consistently change linearly with z, and the change at z=70 um is about 0.5-0.6%. Although these changes can be due to the change in electron mobility and saturation velocity under applied strain, it is more likely to be due to an increase in sheet carrier density. The sheet carrier density n_s of 2D electron gas (2DEG) in AlGaN/GaN heterostructure is a function of polarization-induced charge at AlGaN/GaN interface [3-4]. This polarization-induced charge consists of the net spontaneous polarization and piezoelectric effect induced polarization due to strain in AlGaN layer. By bending the chip, strain in both AlGaN and GaN layer increases, and this results in additional piezoelectric polarization at the top of the GaN layer and the bottom of the AlGaN layer. Although the signs of these two piezoelectric polarization charges are different, net

positive charge is induced at the AlGaN/GaN interface under tensile strain due to higher piezoelectric coefficient of AlGaN compared to GaN [3, 65]. With the reported values of material property in [3, 65], the estimated increase in sheet carrier density is about 0.9% at z=70 um that corresponds to 0.06% of strain. This is quite larger than the value that we experimentally obtain. This discrepancy can be due to inaccuracy in the piezoelectric coefficient in the literature (e.g. e_{31} ranges from 0.30 to 0.55 C/m^2 [3, 65-67]). Also, the actual strain in the device can be reduced due to mesa isolation [68]. In any case, the fact that we observe the change in sheet carrier density indicates that strain is applied to the AlGaN barrier layer at least to some extent although the strain applied to the AlGaN may be lower than the strain applied to the chip.

We verify that by itself, the level of strain applied to the chip does not damage the devices. This is confirmed by applying 0.07% of tensile strain on a chip for 24 hours. We find no significant change in electrical characteristics in a device on this chip. At this time, when using small chips, our apparatus limits us to introducing tensile strain only. In our experiments, strain is applied parallel to the channel direction (perpendicular to gate finger).

3.4.2. Critical voltage

First, we have investigated the impact of mechanical strain on the critical voltage. Figure 3-21 shows change in I_{Goff} in typical V_{DS}=0 step-stress experiments under combined electrical and mechanical stress. It can be seen that applying tensile strain of 0.076% reduces the critical voltage by about 2 V. We also observe a similar reduction of V_{crit} under mechanical strain in OFF-state step-stress experiments (Figure 3-22). In these experiments, we studied 5 pairs of identical devices that are located side by side on the same chip. As mentioned earlier, devices that are located side by side shows well matched critical voltage. In all cases the device under tensile mechanical strain exhibits a lower value of V_{crit} of around 1 to 3 V. The changes observed in V_{crit} upon the application of mechanical strain are relatively small but systematic.

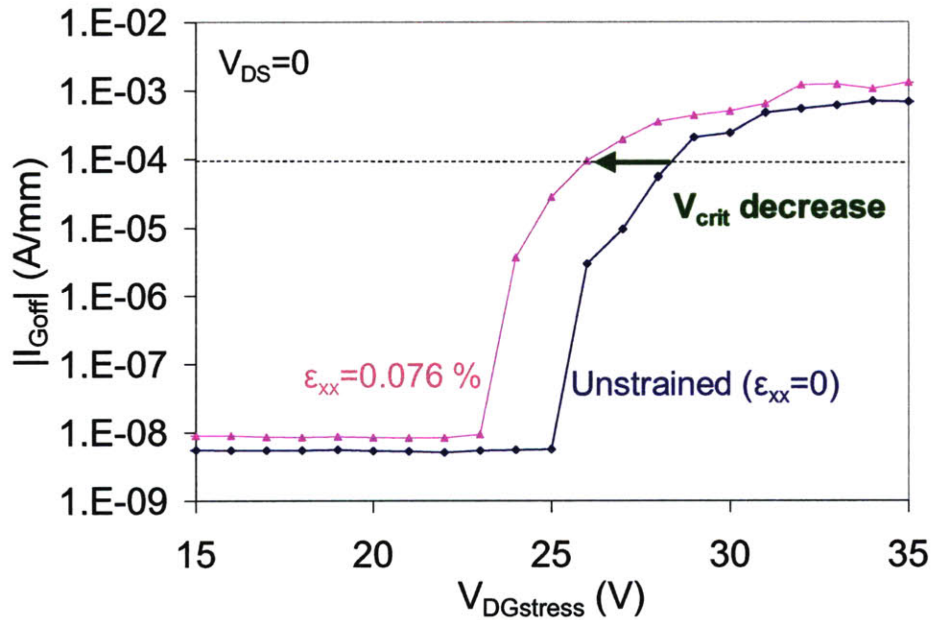

Figure 3-21. Change in I_{Goff} in V_{DS}=0 state step stress experiments. V_{GS} is stepped from -10 V to -40 V in a 1 V step (10 sec/step). V_{crit} is about 2 V lower for the devices that are stressed under 0.076% uniaxial mechanical strain.

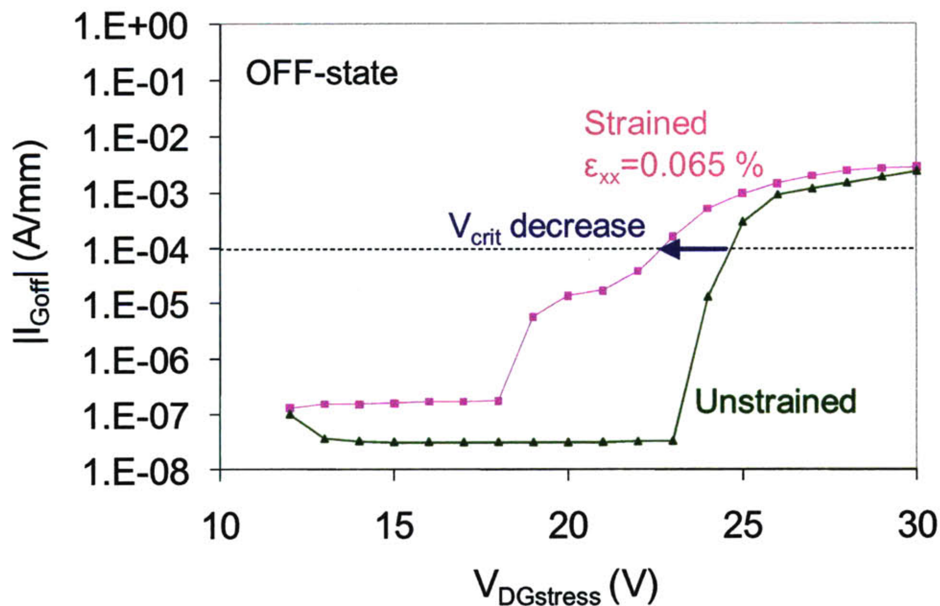

Figure 3-22. Change in I_{Goff} in OFF-state step stress experiments. V_{DS} was stepped from 5 V to 40 V in a 1 V step (10 sec/step) while V_{GS} is kept constant at -7 V. V_{crit} is about 2 V lower for the devices that are stressed under 0.065% uniaxial mechanical strain.

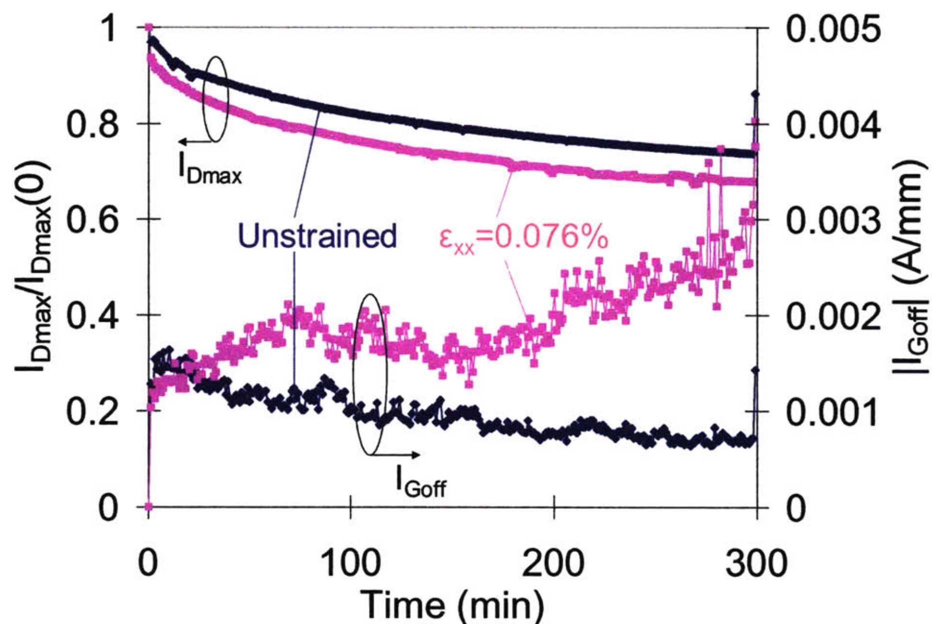

Figure 3-23. Time evolution of I_{Dmax} and I_{Goff} in OFF-state stress experiments. The devices are stressed at V_{GS}=-7 V and V_{DS}=35 V. The device stressed under tensile mechanical strain shows larger degradation in both I_D and I_G.

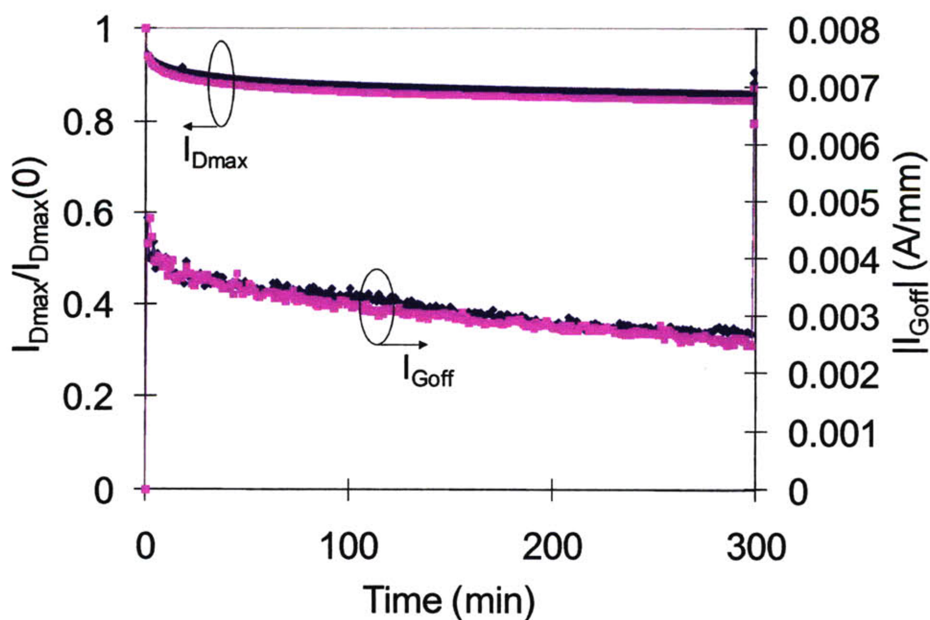

Figure 3-24. Change in I_{Dmax} and I_{Goff} of OFF-state stress experiments on two matched devices. The devices are stressed at V_{GS}=-7 V and V_{DS}=35 V.

3.4.3. Constant stress

We have also investigated the impact of strain on long term reliability. For this, we have performed OFF-state stress experiments at constant electrical stress with and without additional mechanical strain. These experiments are also performed on matched devices that are placed side by side on a chip. The stress bias is V_{GS}=-7 V and V_{DS}=35 V, which is beyond the critical voltage in the OFF-state. Figure 3-23 shows the time evolution of I_{Dmax} and I_{Goff} for two conditions. It can be seen that I_{Dmax} degrades 15% more under tensile strain of 0.076%. Also, I_{Goff} degrades about 3 times more under tensile strain, compared to the unstrained device. This result confirms that I_D and I_G degradation are enhanced by applying mechanical strain. In order to show the degree of matching that can be obtained in devices that are sitting side by side on the same die, we have performed the same experiment on another set of devices, both without applying external strain. The result of this experiment is plotted in Figure 3-24, where both I_{Dmax} and I_{Goff} degrade almost the same amount. Therefore, the result in Figure 3-22 significantly shows the impact of tensile strain on long term reliability.

3.4.4. Step strain test

Further confirmation of the impact of strain is obtained through a step-strain experiment in the OFF-state. In this experiment, the stress bias is fixed at V_{GS}=-7 V and V_{DS}=30 V. This electrical bias is close to the critical voltage. The time evolution of I_{Goff} in this experiment is shown in Figure 3-25. After degradation in I_{Goff} is saturated (at t=133 min), we apply 0.065% of external mechanical strain. As shown in Figure 3-25, degradation in I_{Goff} is enhanced as additional mechanical strain is applied. At t=197 min, the tensile strain is increased to 0.076%, and I_{Goff} slightly increases. Another device that is stressed under the same electrical conditions but without strain shows no increase in I_{Goff} after the initial increase as shown in Figure 3-25.

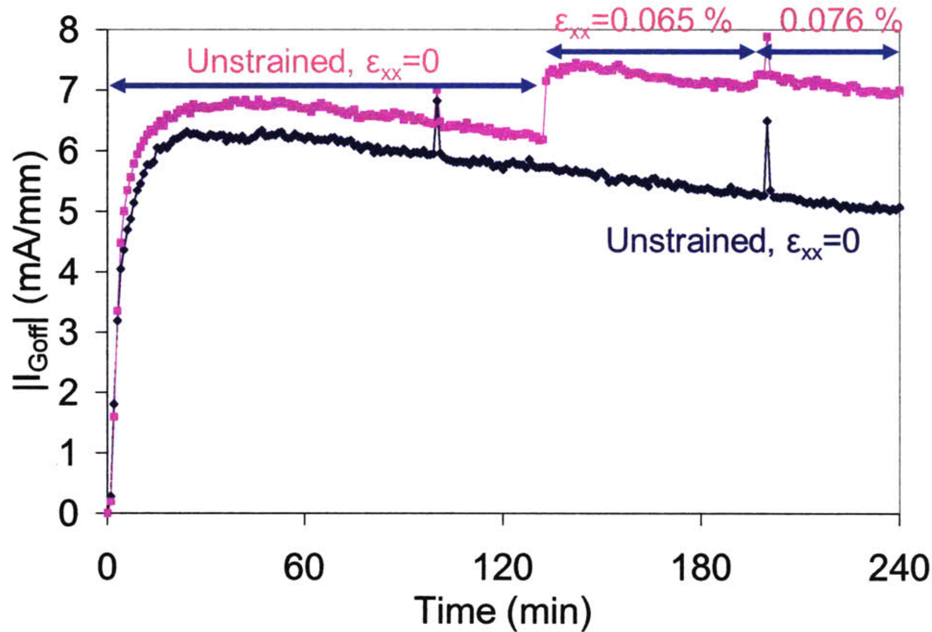

Figure 3-25. Time evolution of I_{Goff} in OFF-state stress experiments. Stress bias is V_{GS}=-7 V and V_{DS}=30 V. One device is stressed without mechanical strain. For the other device, uniaxial mechanical tensile strain ε_{xx}=0.065 and 0.076% is applied at t=133 and 197 min. Applying mechanical strain enhances I_G degradation.

All these experiments show that external tensile mechanical stress exacerbates device degradation. This is consistent with our inverse piezoelectric effect hypothesis for electrical degradation of both I_G and I_D and are difficult to explain through hot-electron type degradation mechanisms. Although we have not performed any experiments under compressive strain, it is expected that degradation is mitigated under compressive strain since it has the opposite effect to tensile strain.

3.5. Summary

In this chapter, we show various aspects of electrical device degradation in GaN HEMTs from stress experiments. First, we have investigated gate current degradation. We find that the application of a large positive gate bias severely degrades the Schottky contact due to large

current. However, under positive gate voltage, no degradation is observed in I_D as well as series resistance of the device. For high reverse gate bias, we find that I_G degradation occurs simultaneously with I_D degradation. Both degradations appear to have a common origin and take place beyond a critical voltage. This type of degradation is driven by electric field. In spite of the strong correlation between I_D and I_G degradation, initial level of gate current as well as the gate current at stress condition is not found to be a cause of degradation. Degradation in gate current in both forward and reverse bias is not recoverable.

We have investigated the dependence of the critical voltage on different parameters. First, we have seen that V_{crit} is higher in the OFF state than in the V_{DS}=0 state. This is found to be due to a V_{GS} dependence of V_{crit}. As the magnitude of V_{GS} increases, this modifies the electric field distribution in the drain side of the device, resulting in higher elastic energy near the drain side of the gate edge. As a result, V_{crit} decreases. On the other hand, the drain current is found to not be an accelerating factor in the degradation process associated with the critical voltage. It was found that V_{crit} is slightly increased under higher stress drain current. Also, V_{crit} is reduced, and larger degradation is observed at higher temperature. These results show that this type of degradation process is not related to hot-electron mechanisms.

Based on the inverse piezoelectric effect hypothesis, we have studied the impact of mechanical strain on device degradation. We have shown that under additional tensile mechanical stress, the critical voltage is reduced in both V_{DS}=0 and OFF-state step stress; there is larger degradation both in I_D and I_G in constant electrical stress; and degradation in I_G is enhanced as the external strain is stepped up. These results clearly show that additional tensile strain affects device degradation and support the hypothesis that the defect formation through the inverse piezoelectric effect plays a major role in device degradation in GaN HEMTs. In the next chapter, we propose a model for the inverse piezoelectric mechanism and discuss experimental results in more detail.

Chapter 4. Physics of electrical degradation

In the previous chapter, we have shown that our experimental results are consistent with the inverse piezoelectric effect induced defect formation mechanism. In order to improve reliability of GaN HEMTs, it is important to understand and model this degradation process. In this chapter, we present a theoretical background of this degradation mechanism and propose a simple model for the critical voltage of degradation in GaN HEMTs. We show that our model is consistent with experimental observations of V_{crit} in devices with different geometries and stress conditions.

4.1. Mechanism of defect formation by inverse piezoelectric effect

In Section 1.3.3, we have introduced the inverse piezoelectric effect driven defect formation mechanism. The built-in lattice mismatch between the AlGaN barrier layer and the GaN buffer in GaN HEMTs results in substantial in-plane tensile stress and stored elastic energy in the AlGaN. Due to the strong piezoelectric nature of GaN and AlN, this stress increases upon applying a high vertical electric field through the AlGaN layer under high V_{DG}. As a result, the stored elastic energy in the AlGaN barrier close to the gate edge, where the electric field is the highest, increases. If the elastic energy exceeds a critical value, crystallographic defects can be produced in the AlGaN (where the initial stress and field are the highest). Some of these defects can behave as electrical traps, and trapping behavior is enhanced as a result. If these traps get filled with electrons, it modifies the electrostatics of the channel which gets depleted. This degrades I_{Dmax} and R_D. These

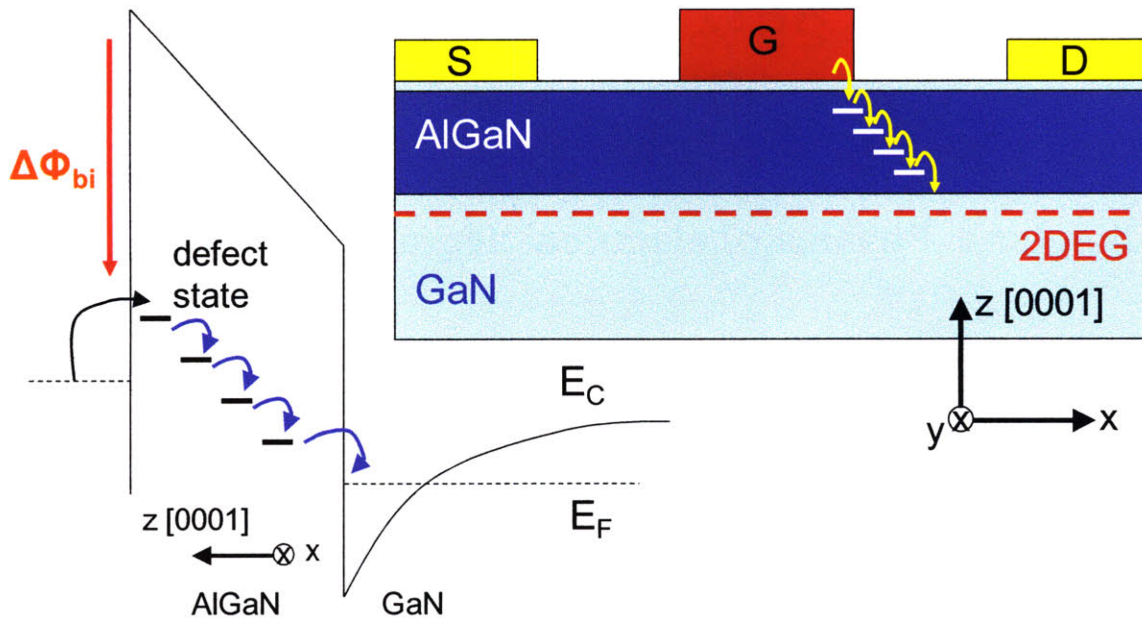

Figure 4-1. Conceptual I_G degradation mechanism for reverse bias stress. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path across the AlGaN barrier. The axis definition is also shown.

generated defects not only degrade I_D and R_D by trapping but also provide additional leakage paths and aid electron tunneling between gate and channel through the AlGaN barrier. As shown in 3.2, the generated defects in AlGaN effectively lower the Schottky barrier height of the gate and increase the gate leakage current. A pictorial view of the role of traps in gate current degradation after an OFF state stress is shown in Figure 4-1. Moreover, carrier transport properties can also degrade due to enhanced scattering especially when these defects propagate to the AlGaN/GaN interface. This gives rise to permanent degradation in drain current. As mentioned in Chapter 1, pits and cracks at the drain side of the gate edge are observed in TEM images after stress tests [9, 20]. Since these crystallographic defects are found after stressing devices for a short period of time (sometimes less than an hour), they appear to be created at least partly due the inverse piezoelectric effect, not from chemical or electrochemical processes that take long time. These kinds of significant defects, when excessive, locally relax strain in AlGaN, which reduces the piezoelectric induced charge and thus decreases sheet carrier density in 2DEG. This also results in permanent degradation in drain current.

The fact that the electric field in the AlGaN barrier is a function of V_{DG} implies existence of a critical voltage, V_{crit}, that marks the onset of this degradation process. This is because this degradation process is not likely to occur before the elastic energy density reaches its critical value. As shown in stress experiments in Chapter 3, at a certain voltage, an irreversible sudden rise in gate current takes place, and I_D and series resistance starts to degrade. In the next few sections, we propose a simple procedure to estimate the critical voltage for a given heterostructure and device design.

4.2. Theory

In this section, we first examine fundamental physics behind the inverse piezoelectric effect driven degradation mechanism. Our goal is to express the elastic energy density at any point in the device as a function of the electric field at that point. The definition of the axes with respect to a typical device structure is shown in Figure 4-1. In this definition, the vertical direction (heterostructure growth direction, or [0001] direction or c-axis of Ga-face Wurtzite crystal) is called z direction. The channel direction is on x axis.

4.2.1. Stress and strain induced by the inverse piezoelectric effect

First, we start with the governing equations and boundary conditions of the problem that we try to solve. The constitutive equations mathematically describe the piezoelectric effect and the inverse piezoelectric effect. The piezoelectric constitutive law in stress-charge form is:

$$\mathbf{D} = \mathbf{e} \cdot \mathbf{S} + \boldsymbol{\varepsilon}_{\mathbf{S}} \cdot \mathbf{E} \tag{4-1}$$

$$\mathbf{T} = \mathbf{c}_{\mathbf{E}} \cdot \mathbf{S} - \mathbf{e}^{t} \cdot \mathbf{E} \tag{4-2}$$

where **D**, **T**, **S**, and **E** are electric displacement, stress, strain, and electric field tensors/vectors, respectively. For proportionality constants, **e** is a third-rank piezoelectric coefficient tensor (superscript t in Equation (4-2) denotes the inverse process or transpose in the matrix form); ε_S is a second-ranked electric permittivity tensor for constant (preferably zero [69-70]) strain; and $\mathbf{c_E}$ is a fourth-ranked stiffness coefficient tensor for constant (preferably zero [69-70]) electric field. Equation (4-1) and (4-2) represents the piezoelectric effect and the inverse effect, respectively. In Voigt notation (xx→1, yy→2, zz→3, yz→4, zx→5, xy→6), $\mathbf{c_E}$ and **e** in GaN and AlGaN can be written in a simple matrix form [71]:

$$\mathbf{c_E} = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & (C_{11}-C_{12})/2 \end{bmatrix} \tag{4-3}$$

$$\mathbf{e} = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{bmatrix} \tag{4-4}$$

In the AlGaN-GaN system where an AlGaN layer is grown pseudomorphically on a GaN buffer, planar strain in the AlGaN is assumed to be fixed by a thick GaN layer, and it is given by the lattice mismatch between AlGaN and GaN (pseudomorphic boundary condition) [67, 72]:

$$S_1 = S_2 = \frac{a_{GaN} - a_{AlGaN}}{a_{AlGaN}} = S_{10} \tag{4-5}$$

In addition, we assume a free surface where all normal components of the stress are zero [67, 73]:

$$T_3 = T_4 = T_5 = 0 \quad (4\text{-}6)$$

It is assumed that no sheer stress is applied in x-y plane, and thus T_6=S_6=0. It is straightforward to solve Equation (4-2) for electric field **E** with these boundary conditions, and we can express planar stress, vertical strain, and sheer strain at any point as a function of electric field. These results are summarized below:

$$S_3 = -2\frac{C_{13}}{C_{33}}S_1 + \frac{e_{33}}{C_{33}}E_3 \quad (4\text{-}7)$$

$$S_4 = \frac{e_{15}}{C_{44}}E_2 \quad (4\text{-}8)$$

$$S_5 = \frac{e_{15}}{C_{44}}E_1 \quad (4\text{-}9)$$

$$\begin{aligned} T_1 = T_2 &= C_{11}S_1 + C_{12}S_2 + C_{13}S_3 - e_{31}E_3 \\ &= (C_{11} + C_{12} - 2\frac{C_{13}^{\ 2}}{C_{33}})S_1 + (\frac{C_{13}e_{33}}{C_{33}} - e_{31})E_3 \end{aligned} \quad (4\text{-}10)$$

Here, E_1=E_x, E_2=E_y, and E_3=E_z. As it can be seen in Equations (4-7), the vertical normal strain S_3 is changed by the vertical electric field. Without any electric field, S_3 is negative, meaning compressive strain as expected. Under normal bias condition where a reverse bias is applied between the gate and the drain, electric field directs from 2DEG to surface, thus E_3>0. As a result, the magnitude of S_3 decreases under electrical bias. Due to a high aspect ratio of a gate finger, in most regions except the edge of the gate finger, the electric field that is parallel to the gate finger, E_2, is negligible, and as a result S_4 is almost zero (Equation (4-8)). On the other hand, sheer strain in x-z plane, S_5, is introduced when horizontal field (E_1) is present, as can be seen in Equation (4-9). In particular, Equation (4-10) shows that vertical electric field changes planar stress T_1 or T_2 by $\Delta T = (\frac{C_{13}e_{33}}{C_{33}} - e_{31})E_3$.

Since e_{31}<0 and e_{33}>0, T_1 and T_2 increase under typical direction of E_3 (>0). This increase

in planar stress gives rise to an increase in the elastic energy in AlGaN barrier layer where high vertical electric field is present. This is explained in the next section.

4.2.2. Elastic energy

The differential of the elastic energy at a point, dW, can be expressed as:

$$dW = T_1 dS_1 + T_2 dS_2 + T_3 dS_3 + T_4 dS_4 + T_5 dS_5 + T_6 dS_6 \tag{4-11}$$

In this equation, only the first two terms are non-zero since T's are zero for the other terms due to boundary conditions in Equation (4-6). Therefore, the change in vertical strain (S_3) in Equation (4-7) does not directly affect the elastic energy. Also, sheer strain S_5 that is produced due to horizontal electric field does not contribute to the elastic energy since $T_5=0$. As a result, the change in elastic energy in AlGaN is only due to the vertical electric field that modifies T_1 and T_2 as shown in Equation (4-10), not due to the horizontal field. Since we have obtained formulas for non-zero T's in Equation (4-10), it is more convenient and obvious to express the elastic energy density as a function of T's [74]:

$$W = \sum_{i,j} \frac{1}{2} s_{ij} T_i T_j \tag{4-12}$$

Here, s_{ij}'s are matrix elements of compliance tensor **s** which is the inverse of the stiffness coefficient tensor $\mathbf{c_E}$. After simplifying, the elastic energy density can be expressed as following:

$$W = \frac{1}{2} s_{11} T_1^2 + \frac{1}{2} s_{22} T_2^2 + s_{12} T_1 T_2 = \frac{C_{33}}{C_{11}C_{33} - 2C_{13}^2 + C_{12}C_{33}} T_1^2 \tag{4-13}$$

The last equality holds for $T_1 = T_2$ as is the case in Equation (4-10). It can be seen that the elastic energy quadradically increases with T_1. By plugging Equation (4-10) into (4-13), we

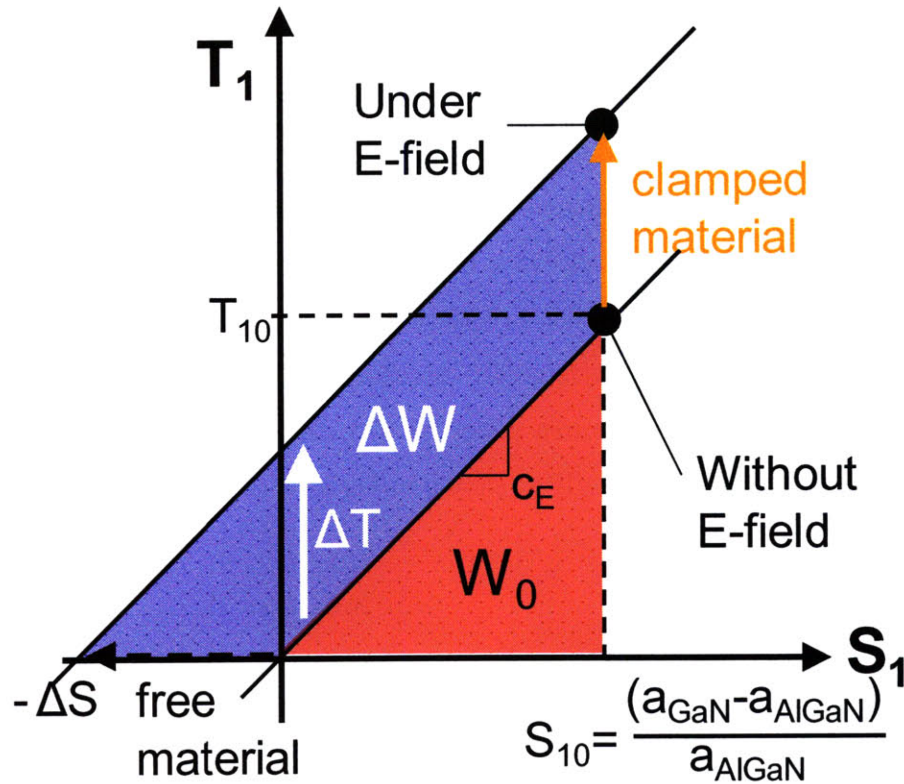

Figure 4-2. Change in stress-strain relationship and elastic energy in AlGaN barrier under vertical electric field.

can obtain a relationship between the elastic energy density W and the vertical electric field E_3, which is super-linear.

The result in Equation (4-13) can be graphically understood in Figure 4-2. It plots the relationship between planar stress (T_1) and planar strain (S_1) in x direction in the AlGaN layer with and without vertical electric field. Although we plot the T-S relation here as if it were in 1-D, it should be noted that the actually *T-S* relationship has a 3-dimentional nature. Therefore, it does not capture, for example, the cross terms in Equation (4-12). However, we present it to conceptually show how *W* increases quadradically with the planar stress, as can be seen in Equation (4-13). As mentioned above, under the E-field, the linear *T-S* relationship is shifted by ΔT, the additional stress introduced by the inverse piezoelectric effect. Because the AlGaN barrier is clamped on the GaN buffer, S_1 remains fixed at S_{10},

	C_{11}	C_{12}	C_{13}	C_{33}	C_{44}	e_{13}	e_{33}	e_{15}
GaN	350	110	103	405	105	-0.49	0.73	-0.30
AlN	350	110	108	373	105	-0.60	1.46	-0.48

Table 4-1. Material parameters used in the calculation [3, 65-67]. Units for C's and e's are GPa and C/m^2, respectively.

the value given by the lattice mismatch between AlGaN and GaN (Equation (4-5)). If the AlGaN layer were free-standing (all T=0), it would become compressively strained under this E-field ($S_1= -\Delta S$), as it can be seen in Figure 4-2 and Equation (4-10). This means that the strain in the clamped AlGaN effectively increases to $S_{10}+\Delta S$. In this figure, the elastic energy stored in the AlGaN is the area under the T-S curve. Since the T-S curve shifts by ΔT, the elastic energy increases by ΔW as shown in Figure 4-2.

4.3. Model for the critical voltage

Our model for V_{crit} is based on the calculation of elastic energy stored in the AlGaN layer of a GaN HEMT and its modification under electrical bias. First, we calculate stress, strain, and elastic energy in AlGaN as a function of the electric field. This calculation is based on the equations derived in Section 4.2. Then, from electrostatics simulations, we compute the electric field at every point in the device under a given bias condition. Finally, from these results, we calculate the elastic energy density at every point in the device. By comparing the elastic energy density to the critical elastic energy derived from epitaxial growth studies [75], the critical voltage can be derived.

We have modeled a GaN HEMT with 16 nm thick $Al_xGa_{1-x}N$ with x=0.28, which is a close match to our experimental devices. The material parameters used in this calculation are summarized in Table 4-1 [3, 65-67]. For AlGaN, we linearly interpolate values between GaN and AlN.

4.3.1. Critical elastic energy

In growing a thin strained layer on a substrate, it is known that the strained material starts to relax its strain by forming defects beyond critical thickness [75-76]. This is because formation of defects such as cracks is energetically favored over maintaining large mechanical stress and subsequent elastic energy stored in the material. Therefore, the maximum elastic energy that can be stored in the AlGaN barrier layer without any formation of defect can be estimated from the critical thickness data for AlGaN growth on GaN. From the data of critical thickness below which AlGaN layer can be pseudomorphically grown on GaN without having cracks or defects, the critical elastic energy density can be estimated:

$$W_{crit} = E_Y h_{crit} S_1^2 \qquad (4\text{-}14)$$

, where E_Y and h are Young's modulus and the critical thickness of the film, respectively. Young's modulus can be computed from Table 4-1. From the critical thickness data in [75], the estimated critical elastic energy density is between 0.35 and 0.58 J/m^2. This value is later compared to the elastic energy density under electrical bias.

4.3.2. Stress, strain, and elastic energy under electric field

We first calculate the impact of electric field on stress, strain, and elastic energy density at a certain point in the AlGaN barrier. For this, we evaluate the equations in Section 4.1. The change in some of these parameters in the AlGaN layer as a function of vertical electric field is computed for our structure and plotted in Figure 4-3 and Figure 4-4. As mentioned earlier, under a positive vertical field, the planar stress in the AlGaN (T_1=T_2) is increased, which increases the elastic energy. As shown in Figure 4-4, the change in elastic energy density can be as high as 50% of its original value at high electric field. The vertical strain

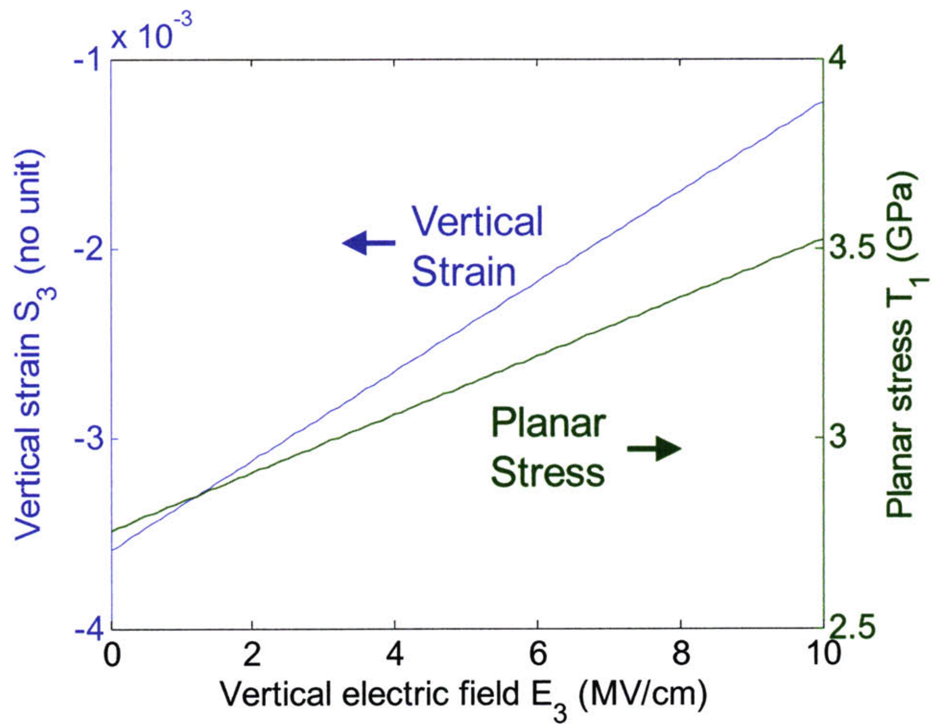

Figure 4-3. Vertical normal strain S_3 and planar stress T_1 ($=T_2$) as a function of vertical electric field in the AlGaN layer.

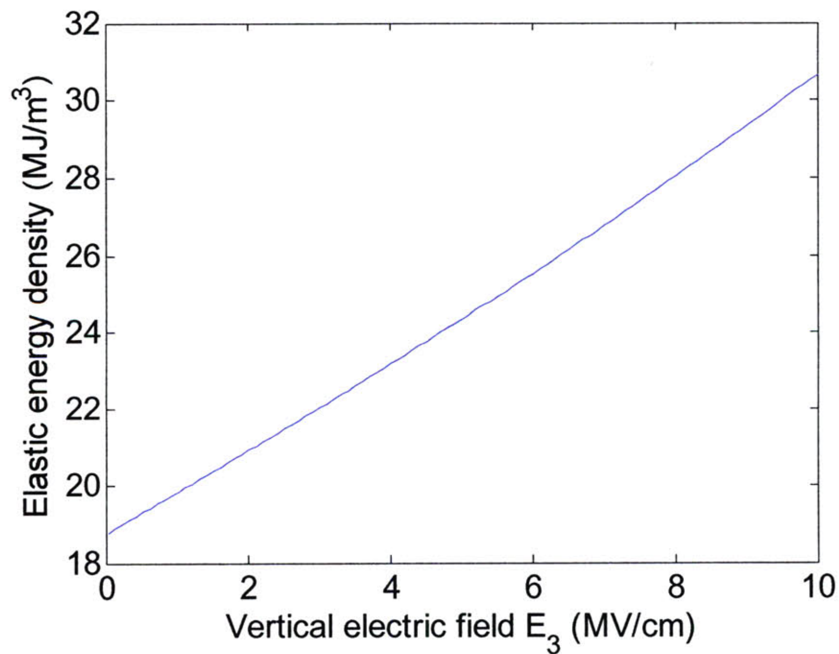

Figure 4-4. Elastic energy density as a function of vertical electric field in the AlGaN layer.

(S_3) is reduced in magnitude (Figure 4-3), but this does not directly affect the elastic energy as mentioned above.

4.3.3. Electrostatics simulation

The electrostatics at various bias points are computed with Silvaco Atlas. The device structure that we simulate matches that used in our experiments. From this simulation result, horizontal and vertical electric field distribution in the device is extracted. The 2D field distribution is the basis for computation of mechanical stress and stored elastic energy across the structure, as described above. Strictly speaking, this problem should be solved in a coupled way since the variables in Equation (1) and (2) are all coupled. As a result, a fully electromechanically coupled calculation is desirable [67, 72]. However, the discrepancy between a fully coupled model and uncoupled model was found to be rather small,

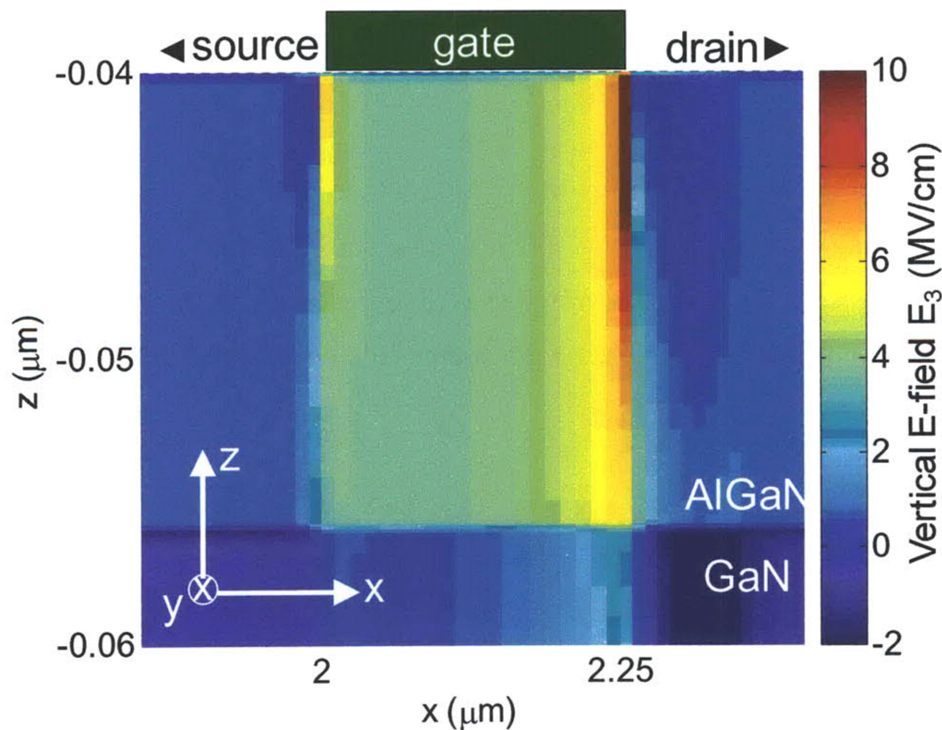

Figure 4-5. Vertical electric field profile under the 0.25 um gate in the OFF state at V_{GS}=-5 V and V_{DS}=33 V.

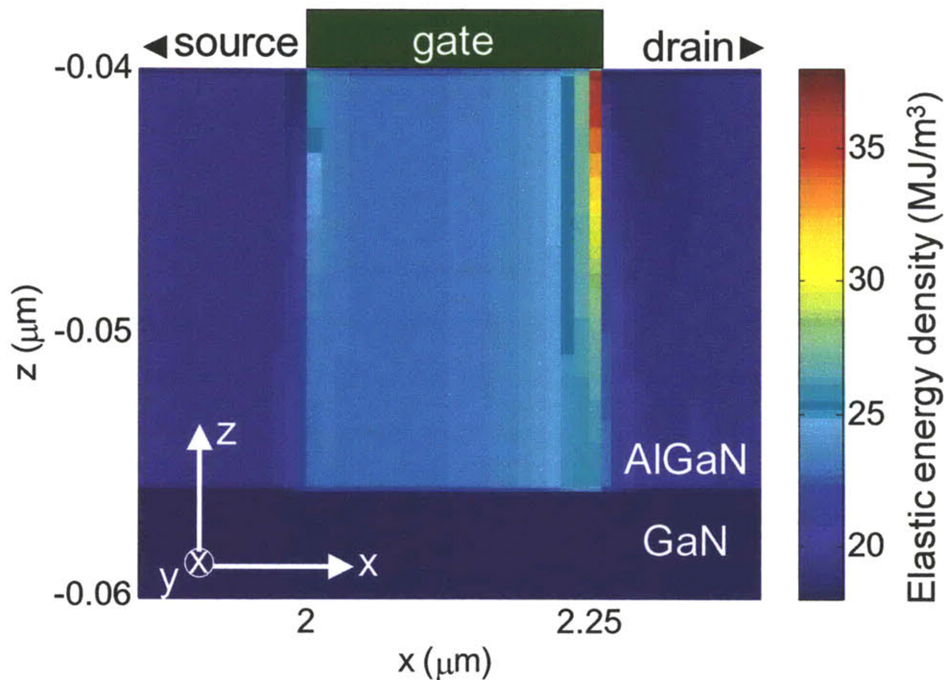

Figure 4-6. Calculated elastic energy density in AlGaN and GaN layer of a GaN HEMT in the OFF state at V_{GS}=-5 V and V_{DS}=33 V.

especially when 2DEG is present [67]. Therefore, in this calculation, mechanical and electrical parts are treated separately.

The vertical electric field distribution in the AlGaN layer for a bias condition typical of the onset of degradation in the OFF-state [12] is shown in Figure 4-5. As it can be seen, the electric field peaks at the drain side of the gate edge and decreases towards the channel and also towards the center of the gate. At the source side edge of the gate, a smaller peak is present.

4.3.4. Elastic energy density under bias

Combining the electric field distribution in Figure 4-5 and relationship between elastic energy density and E-field in Figure 4-4, the elastic energy density at every point in the AlGaN layer under electrical bias is calculated. Figure 4-6 shows the distribution of elastic

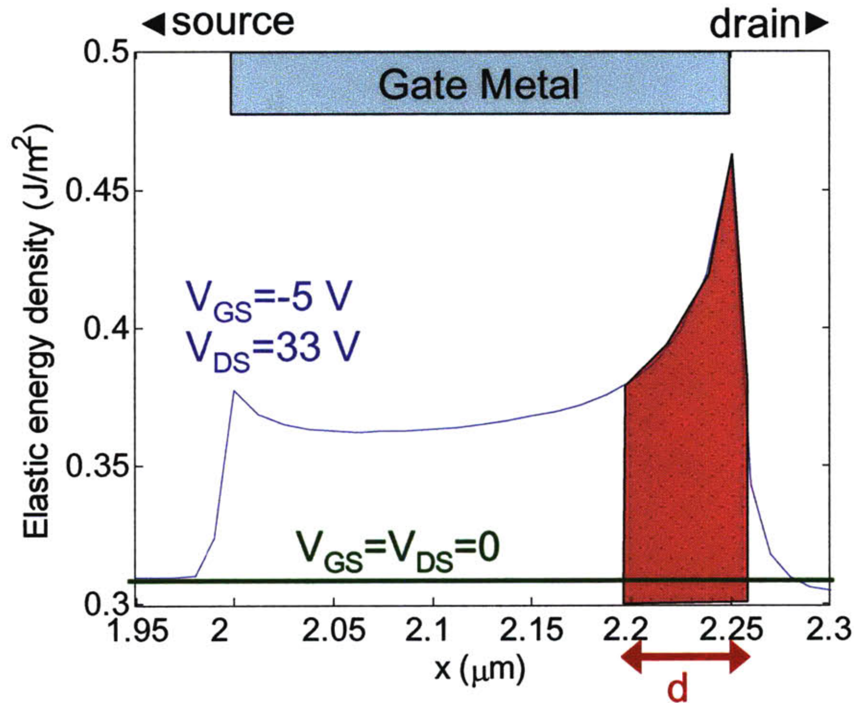

Figure 4-7. Elastic energy per unit area under the gate area in the Off state at V_{GS}=-5 V and V_{DS}=33 V as well as at rest with V_{GS}=V_{DS}=0 V.

energy density under the same bias condition as in Figure 4-5. It can be seen that the elastic energy density peak right under the gate edge on the drain side of the device. A smaller peak is present under the gate edge at the source side of the device.

4.3.5. Calculation of the critical voltage

From the elastic energy density distribution, we can compute the critical voltage. It is known that cracking in a stressed material is determined by the critical elastic energy *per unit area* [77]. We then integrate the volume elastic energy density along the z direction to obtain an *areal* elastic energy density. In Figure 4-7, the elastic energy density profile under the gate at the same bias point as in Figure 4-5 (blue line), as well as at zero bias (green line), are shown. The peak elastic energy density at the drain-side gate edge markedly increases from 0.31 J/m^2 to 0.46 J/m^2 at the critical voltage.

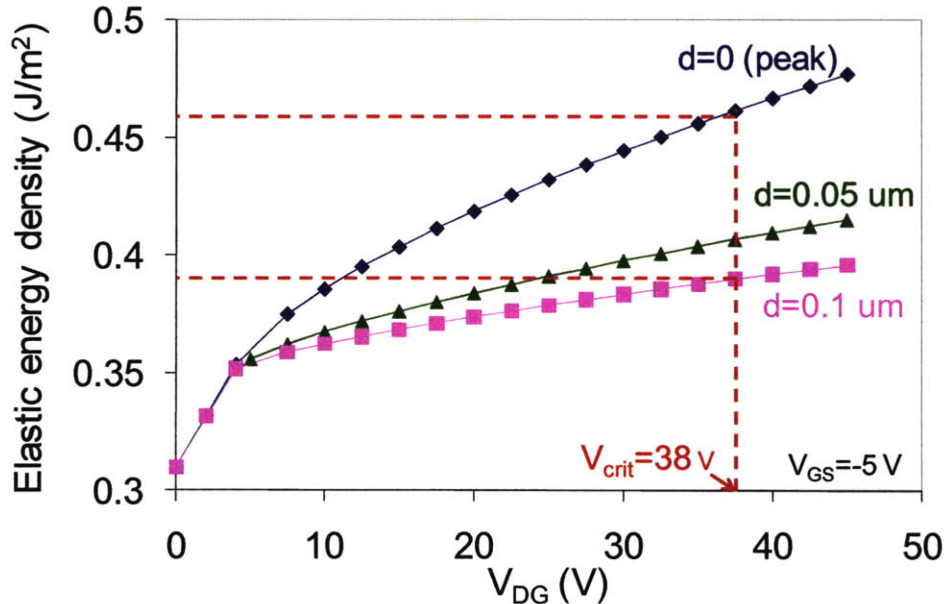

Figure 4-8. Average elastic energy density around the gate edge (drain side) as a function of V_{DG} in the OFF-state step stress (V_{GS}=-5 V) for different averaging length d=0, 0.05, and 0.1 um.

The peak density at one point is not physically very meaningful since it highly depends on grid discretization and assumptions about gate edge rounding. Instead, an average density around the gate edge over a certain averaging length, d, (Figure 4-7) is likely to determine the onset of degradation. The change in the average elastic energy density at the gate corner as a function of V_{DG} for different values of the averaging length d is plotted in Figure 4-8. At the experimental value of V_{crit}, the elastic energy density ranges from 0.39 to 0.46 J/m^2, depending on d. This is comparable to the elastic energy density that we estimate for the bias condition at V_{crit}. However, there is a caveat that, as it can be seen in Figure 4-7, the elastic energy density is highly non-uniform under electrical bias, whereas it should be relatively uniform during growth. As a result, it may not be completely appropriate to compare these values. For example, there might be other parameters such as the gradient of the elastic energy density that also plays an important role in defect or crack formation. Nevertheless, this result is enough to show that the change in the elastic energy density due

to the inverse piezoelectric effect at V_{crit} can be large enough, at least in order of magnitude, to introduce crystallographic defects and perhaps partially relax the strain in the AlGaN layer.

4.3.6. Comparison to experiments

In this section, we compare the model with various experimental results. In particular, dependence of the critical voltage on V_{GS} and gate length are discussed.

4.3.6.1. V_{GS} dependence of V_{crit}

As mentioned in Section 3.3.1, it is found that under OFF-state stress, V_{crit} was much higher than under V_{DS}=0 stress [26]. In Section 3.3.1, we ascribe this to V_{GS} dependence of V_{crit}. In order to understand this with our model, we first compare the elastic energy density in the OFF state and the V_{DS}=0 state. Figure 4-9 shows the elastic energy density profile at experimentally determined V_{crit} in the V_{DS}=0 state and the OFF state. In the OFF state, the peak elastic energy density is higher at the drain side gate edge due to higher V_{DG}, but it becomes lower towards the center of the gate because of lower elastic energy density at the source side. Because, experimentally, both conditions represent the onset of degradation, a certain property should be the same. With that said, it makes sense that the average elastic energy density around the gate corner determines the onset of degradation, as discussed in the previous section. In order to test this hypothesis, we examine the impact of averaging length d (Figure 4-7) on the computed V_{crit}.

As shown in Figure 4-10, the averaging length impacts the prediction of the critical voltage. Here, we use different values of W_{crit} for different d's in order to match the experimental data for the V_{DS}=0 state. However, W_{crit} is within the range that we obtain from the growth experiment. As it can be seen in Figure 4-10, by using peak value (d=0), the model does not

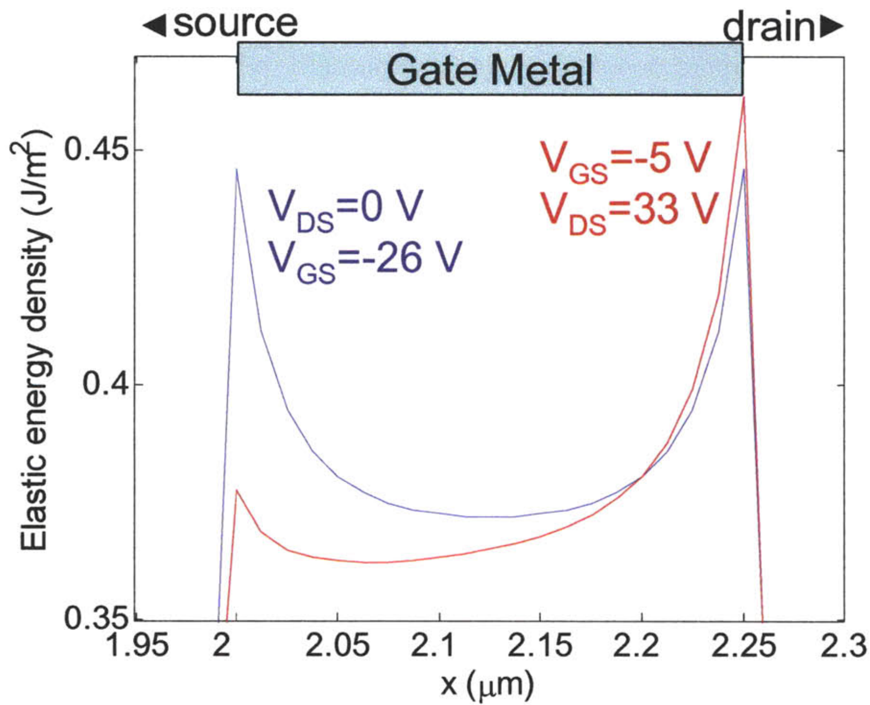

Figure 4-9. Elastic energy density profile at critical voltage for V_{DS}=0 condition (V_{GS}=-26 V) and OFF-state (V_{GS}=-5 and V_{DS}=33 V).

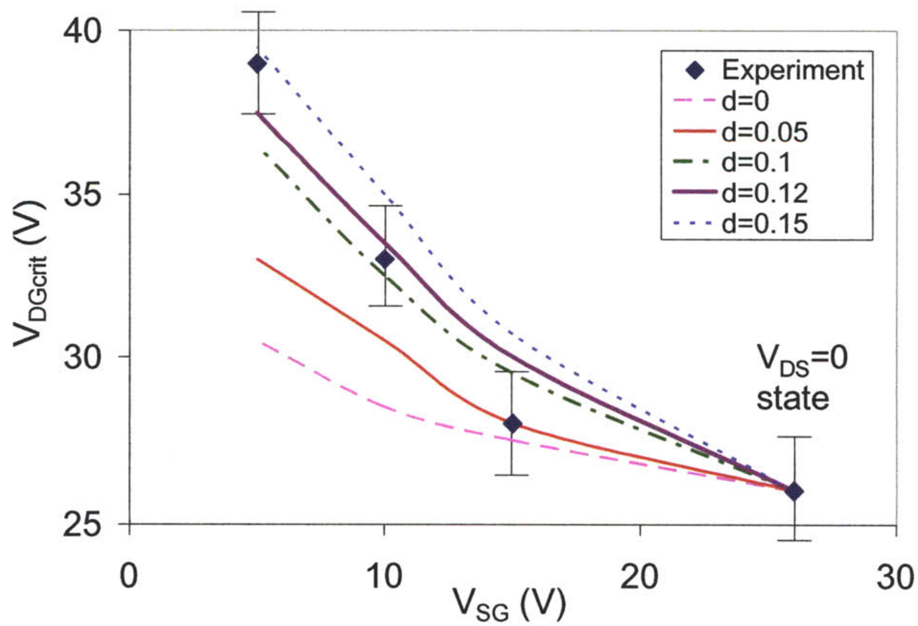

Figure 4-10. Calculated critical voltage as a function of V_{SG} of stress bias for various averaging lengths d (Figure 4-7). Data from experiments are also shown.

correctly predict the large increase in V_{crit} under small $|V_{GS}|$. The model predicts both V_{GS} dependency relatively well with d=0.1~0.12 um.

4.3.6.2. L_G dependence of V_{crit}

In section 3.3.4, we observe that in the V_{DS}=0 state V_{crit} increases with gate length while in the OFF-state, the L_G dependence is negligible (not shown). This is also tested through our model. Figure 4-11 shows calculation of elastic energy density for two devices with different gate lengths at the experimentally determined value of V_{crit}. Similar to above, in the long channel device, the peak density is larger due to high V_{DG}, but it decays faster towards the center of the gate because of a larger separation between the two peak points at the edges of the gate. Again, this result clearly shows that the average of the elastic energy density around the gate edge, and not the peak value, should determine the onset of degradation.

We also find that the model predicts the L_G dependence of V_{crit} well for d=0.1~0.12 um, as shown in Figure 4-12. Note that the estimation with the peak elastic energy density (d=0) shows large discrepancy between the model and the experimental data. The model also correctly predicts that experimentally observed weak dependence of V_{crit} on L_G under OFF-state stress (Figure 4-12).

4.4. Summary

In this chapter, we have built a model for the defect formation mechanism through the inverse piezoelectric effect that is postulated in this thesis. We have done this by modeling the critical voltage for the onset of this degradation process. The model is based on a computation of the elastic energy density in the AlGaN barrier. First, we presented the detailed physics of how the inverse piezoelectric effect changes strain, stress, and elastic

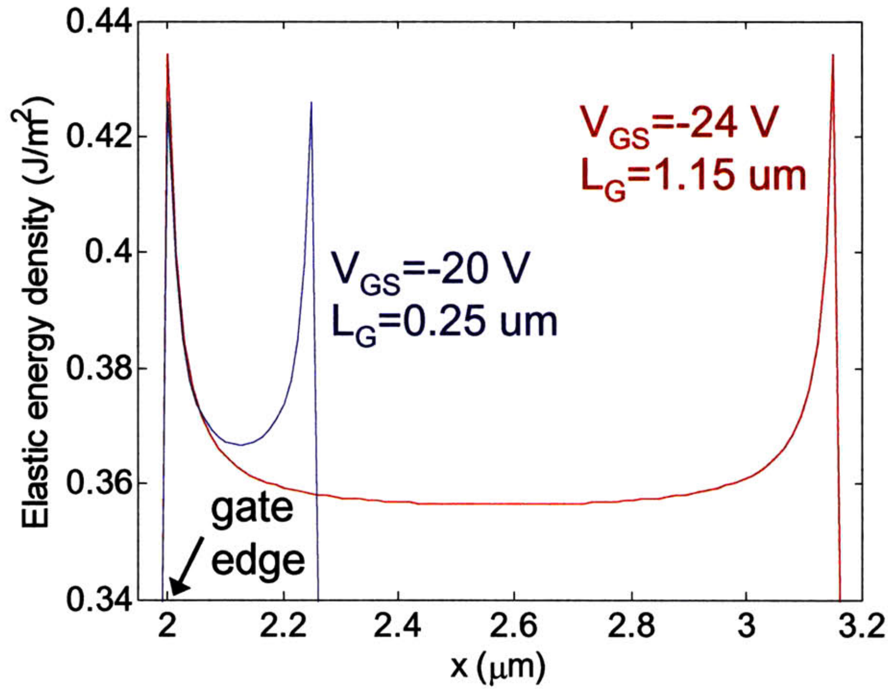

Figure 4-11. Elastic energy density profile at critical voltage in the V_{DS}=0 state for a short (0.25 um, V_{crit}=-20 V) and a long (1.15 um, V_{crit}=-24 V) gate length device.

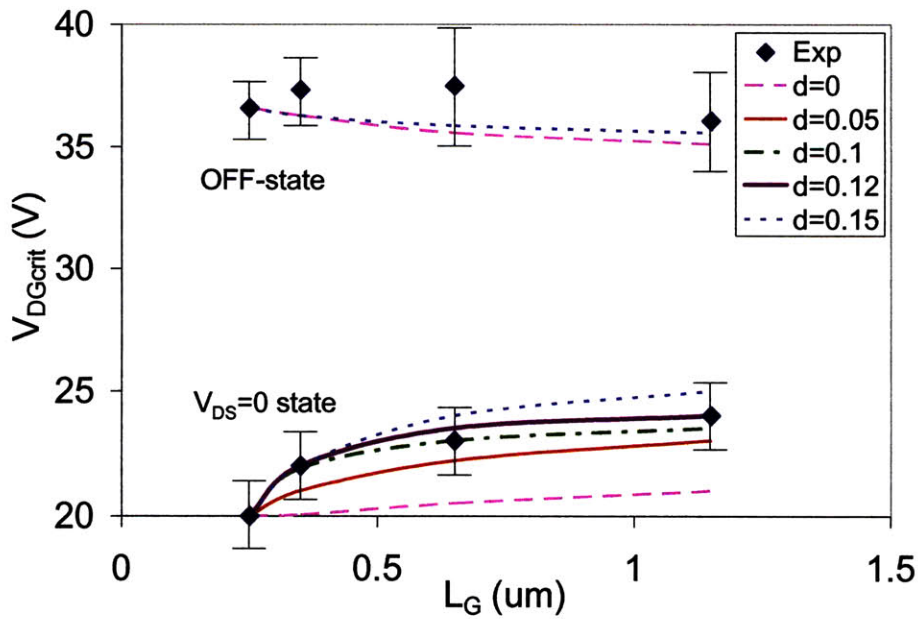

Figure 4-12. Calculated critical voltage as a function of L_G for various averaging lengths d (Figure 4-7) in the V_{DS}=0 state and the OFF=state. Data from experiments are also shown.

energy density under an electric field. Based on this understanding, we have computed the elastic energy density in the AlGaN layer under electrical bias. This was accomplished by electric field calculation through electrostatics simulations. By comparing the computed elastic energy density to its critical value, the critical voltage was estimated. The model matches experimental results under a variety of conditions. This result validates the plausibility of the inverse piezoelectric effect hypothesis.

Chapter 5. Discussion

5.1. Introduction

In this chapter, two important issues in reliability of GaN HEMT are discussed before concluding this thesis. As it is discussed in Section 1.3.4, one of the most deleterious effects of electrical degradation is an increase in carrier trapping and subsequent current collapse [10-11, 14-15]. To date, a detailed understanding of the nature, location and trapping/detrapping time constants of these traps is not completely available. In the first part of this chapter, we try to understand degradation that is caused by trapping effects. For this, we first separate permanent degradation that is not related to trapping from trapping-related degradation. Then, the trapping and detrapping characteristics of GaN HEMTs are examined. In particular a new current transient analysis methodology is presented to comprehensively understand detailed trapping nature. Through this technique, the change in trapping behavior in the course of various stress tests is investigated.

The other part of this chapter is on understanding DC and RF reliability of GaN HEMTs. So far, we have focused on various aspects of degradation in DC stress tests. However, since the main application of GaN HEMTs is RF power amplifier, it is the RF reliability that eventually matters. To understand RF reliability, we perform RF stress experiments and investigate the change in various DC and RF performance figures of merit. Also, we study how RF performance changes under DC stress and verify that our previous findings in DC experiments are relevant to RF reliability in GaN HEMTs.

5.2. Trapping behavior

In this section, we discuss trapping behavior in GaN HEMTs in detail. First, we try to separate permanent degradation from trapping-related degradation. Then, it is shown that both gate current and drain current degradation are caused by the same traps that are generated during the electrical stress. In order to understand the detailed nature of these traps, a new method to analyze trapping and detrapping behavior is developed. Through this method, we identify different trapping and detrapping characteristics in terms of time constant, activation energy, and physical location in fresh and degraded devices. In particular, the impact of electrical degradation during OFF-state step-stress and long term stress both in OFF-state and in high-power state on trapping behavior is studied in detail.

5.2.1. Permanent vs. trapping-related degradation

As mentioned in Chapter 1, degradation in drain current consists of two parts: non-recoverable degradation and recoverable degradation. This can be seen in stress-recovery experiments where decrease in I_{Dmax} or increase in series resistance partially recovers when stress is removed [10, 26]. This recoverable degradation was attributed to detrapping of trapped electrons. In order to clearly understand this, we have performed a stress-recovery test in the V_{DS}=0 state. As shown in Figure 5-1, after stressing the device at V_{GS}=-30 V (this is beyond the critical voltage for this device) for 30 minutes, I_{Dmax} decreases by 28%.. After the stress is removed, I_{Dmax} partially recovers due to detrapping over the following 30 mins. After 88 days of room temperature storage, we find that I_{Dmax} recovers up to 87% of its original value. At this point, we try to detrap more trapped electrons, if any, by shining microscope light and UV light, or heating the device, but I_{Dmax} does not increase any further. Thus, it seems that part of I_{Dmax} degradation is unrecoverable, for example, due to degradation in transport property such as electron mobility and saturation velocity, or an increase in resistance due to the formation of a crack, for example. Although we cannot completely rule out a possibility of trapping with extremely long or even almost infinite

detrapping time constant, and also the trap creation itself is permanent, the unrecoverable and recoverable part of degradation are defined as permanent and trap-related degradation, respectively, throughout this thesis. It should be noted that trap-related degradation may result from trap formation that can be permanent degradation. According to our definition, in this experiment, out of the 28% of I_{Dmax} drop at the end of the 30 min stress period, 13% is due to permanent degradation, while the remaining 15% is trapping-related degradation. Separately, we have found that in our devices, regardless of the amount of degradation, shining microscope light efficiently brings the device to a fully recovered state within about 0.5% in 30 seconds. This is consistent with our notion that the recoverable part of degradation is due to carrier trapping. We use this simple procedure to fully empty traps and in this manner separate permanent and trapping-related degradation from the total degradation.

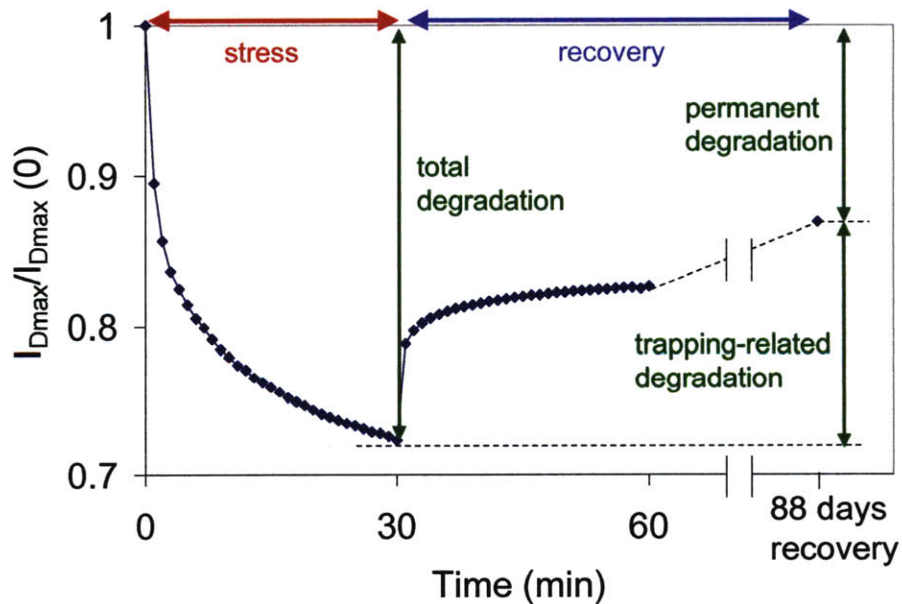

Figure 5-1. Time evolution of normalized I_{Dmax} in a $V_{DS}=0$ stress-recovery experiment at room temperature. The stress condition is $V_{DS}=0$ and $V_{GS}=-30$ V. After the first 30 minutes, the stress is removed while I_{Dmax} is periodically measured. The last data point is measured after 88 days of recovery.

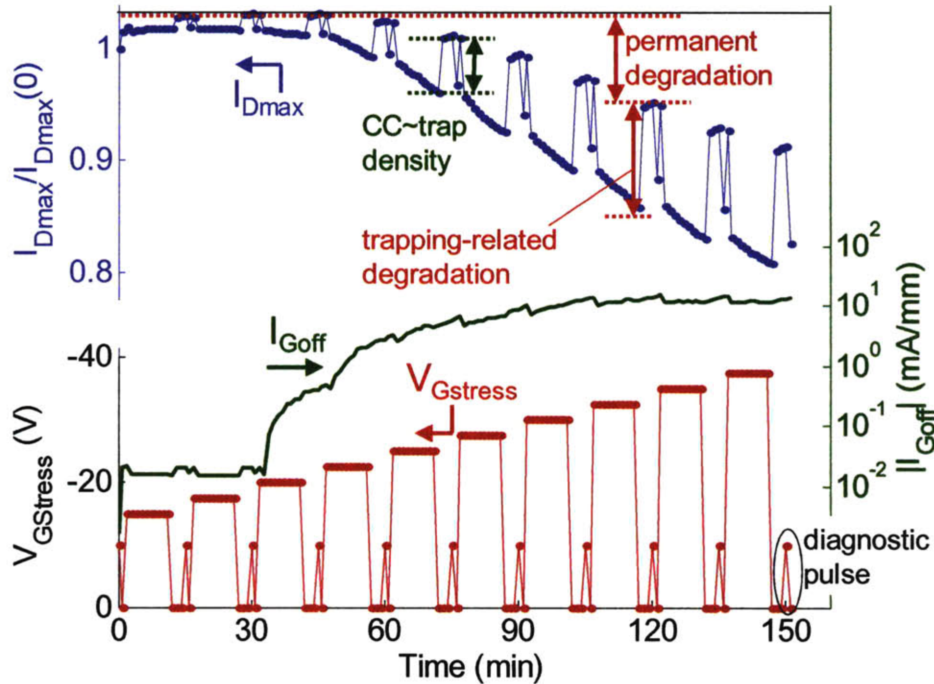

Figure 5-2. Time evolution of I_{Dmax}, I_{Goff}, and stress voltage in a step-stress-recovery experiment in V_{DS}=0 state. For the stress period, V_{GS} is step stressed from -15 V to -37.5 V in 2.5 V step. A 10-minute stress period is followed by a 5-minute recovery period. At the end of the recovery period, a 1-s V_{GS}=-10 V pulse is applied to measure current collapse.

In order to further understand this issue, we have performed a step-stress-recovery experiment in the V_{DS}=0 state. In this experiment, we interrupt the electrical stress by inserting a recovery phase that contains a diagnostic pulse designed to measure current collapse and in this way sample trap concentration [10, 26]. As shown in Figure 5-2, we step-stress V_{GS} from -15 V to -37.5 V in 2.5 V step while V_{DS} is maintained at 0 V. In each step, the device is stressed for 10 minutes followed by a 5-minute recovery period without stress. Towards the end of the recovery phase, we insert a 1-second V_{GS}=-10 V and V_{DS}=0 V diagnostic pulse. This experiment is performed under microscope light. This ensures that during the recovery period, electrons that have been trapped during the stress period are fully detrapped in a short amount of time.

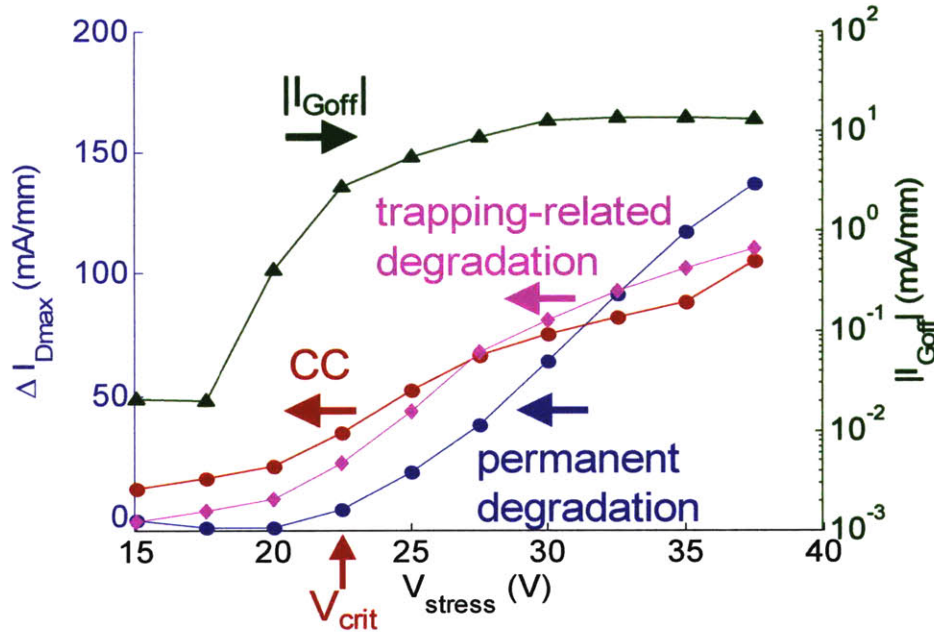

Figure 5-3. Change in permanent and trapping-related I_{Dmax} degradation, current collapse, and I_{Goff} in the experiment of Figure 5-2. All figures of merit start to sharply increase beyond a critical voltage V_{crit}.

Figure 5-2 also shows the evolution of I_{Goff} and I_{Dmax} during this experiment. As shown in Chapter 3, I_{Goff} start to sharply degrade at a critical voltage V_{crit}, which is around -20 V for this device. I_{Dmax} also starts to degrade at around the same critical voltage. In the recovery period, I_{Dmax} quickly recovers and saturates. However, I_{Dmax} shows permanent degradation once the device is heavily degraded beyond V_{crit}. The trapping behavior is clearly manifested in the response to the -10 V diagnostic pulses. Immediately after the pulse, there is a temporary drop in I_{Dmax}, or current collapse. The magnitude of the current collapse provides a sense of the trap density that is increased as a result of electrical stress. Although the increase in current collapse might be due to a change in the access to pre-existing traps in a fresh device, we ascribe it to the increase in the number of traps. This also sharply increases beyond the critical voltage.

The critical behavior in permanent and trapping-related drain current degradation, gate current increase, and current collapse vs. stress voltage is summarized in Figure 5-3. All three degradation phenomena increase sharply at about the same critical voltage. This result

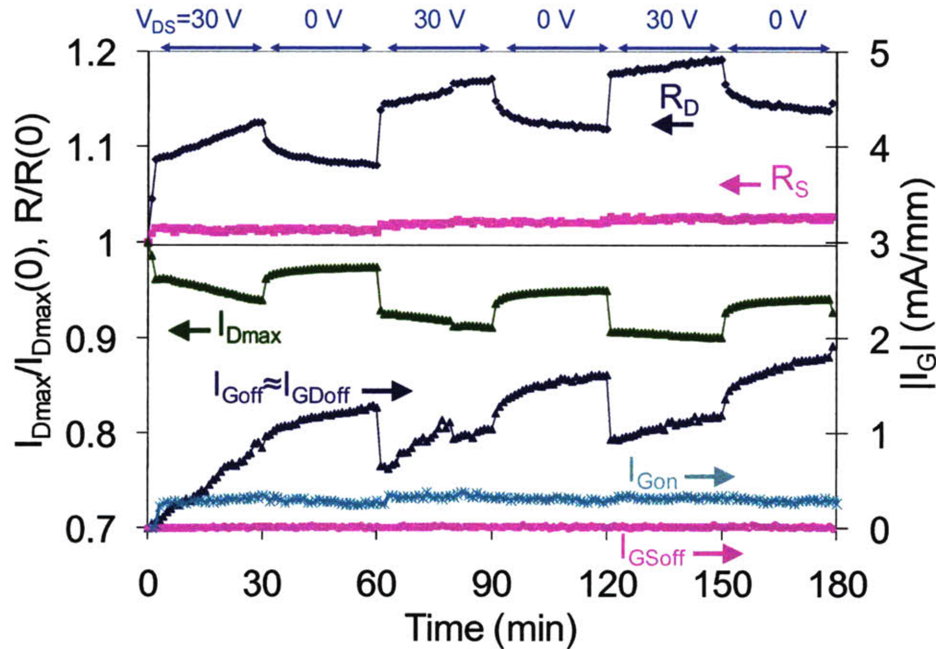

Figure 5-4. Time evolution of I_{Dmax}, R_D, R_S, I_{Goff}, I_{GDoff}, I_{GSoff}, and I_{Gon} in a stress-recovery experiment in the OFF-state. The stressing condition is V_{DS}=30 V and I_D=20 mA/mm. A 30-minute stress period is followed by a 30-minute recovery period. I_{GSoff} is constant below 0.01 mA/mm throughout the experiment.

strongly suggests that permanent I_D degradation, the increase in trapping behavior (current collapse), and the gate current degradation all result from a common physical origin. This is discussed in the next section.

5.2.2. Common trapping behavior in I_D and I_G

In Section 4.1, from the close correlation between I_G and I_D degradation, we have postulated that defects that are produced as a result of device degradation not only trap electrons and reduce the drain current but also provide leakage paths and enhance gate current conduction. In this section, this hypothesis is examined in more detail.

In order to understand impact of the generated traps on the gate current and their location in the device, we have performed a stress-recovery experiment in the OFF-state [10]. This

stresses the drain side of the device while leaving the source side largely unaffected. The result of this experiment is shown in Figure 5-4. In this experiment, the device is first stressed at V_{DS}=30 V and I_D=20 mA/mm for 30 minutes. Following the stress period is a 30-minute recovery period. This 1-hour cycle is repeated three times. For this device, the stress voltage is just above V_{crit}, and both I_D and I_G degraded rather slowly as a result. During the stress period, I_{Dmax} decreases and it partially recovers during the recovery period. As soon as the stress is reapplied (e.g., at t=60 min), I_{Dmax} immediately returns to its degraded value. This clearly shows trap-formation and subsequent trapping and detrapping nature of I_D degradation [26]. Although R_D shows degradation and the same trapping nature as I_{Dmax}, R_S remains unchanged.

Considering the gate current, I_{Goff} largely increases during the stress periods. This indicates trap-formation as shown in the previous experiment. Interestingly, I_{Goff} follows the same detrapping and re-trapping signature as I_{Dmax} shows: it increases during the recovery period and returns to its last value under stress immediately after the stress resumes. This suggests that the same traps are involved in both I_D and I_G degradation. This result is consistent with our hypothesis in the following sense: traps that are produced during the stress period provide leakage paths for the gate current. As a result, I_{Goff} largely increases. During the recovery period, some of these traps are emptied, which can be seen from partial increase in I_{Dmax}. These empty traps participate in more gate current conduction, and I_{Goff} is enhanced. After the stress is reapplied, electrons are immediately retrapped, which not only decreases I_{Dmax} instantaneously but also partially blocks the gate conduction path. As a result, I_{Goff} also decreases. Also of interest is the fact that I_{Gon} does not exhibit any trapping behavior. This is consistent with the fact that the activation energy of the forward gate current is unchanged as a result of stress (Section 3.2). These results also provide a hint for gate conduction mechanisms: In reverse bias, due to relatively large Schottky barrier height, tunneling which is presumably assisted by traps is dominant. On the other hand, in forward bias, thermionic emission from the channel to the gate is dominant, which is not affected by trapping.

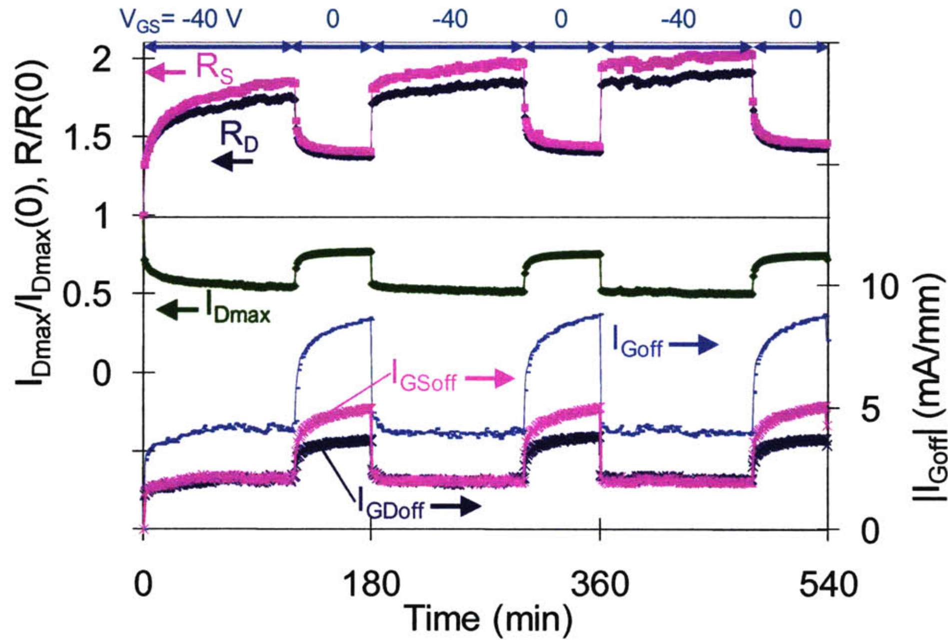

Figure 5-5. Time evolution of I_{Dmax}, R_D, R_S, I_{Goff}, I_{GDoff}, and I_{GSoff} in a stress-recovery experiment in the V_{DS}=0 state. The stressing condition is V_{GS}=-40 V. A 120-minute stress period is followed by a 60-minute recovery period.

In addition, as we have seen in Section 3.2.1, only I_{GDoff} in I_{Goff} shows degradation and trapping behavior, and I_{GSoff} is unchanged throughout the experiment and remained below 0.01 mA/mm (Figure 5-4). This again shows that degradation in I_G results from increased conduction from gate to drain, which suggests that the produced traps are localized in the drain side [51]. This is consistent with the fact that only R_D, not R_S, degrades and that only R_D shows trapping behavior (Figure 5-4). In a similar experiment in V_{DS}=0 state where the device is symmetrically stressed, both I_{GDoff} and I_{GSoff} as well as both R_D and R_S show degradation and trapping behavior (Figure 5-5).

In order for the produced traps to participate in gate current conduction, they should be close enough to the gate in the AlGaN barrier layer. In fact, crystallographic defects such as cracks and pits were found at the gate edge in the drain side, and those defects correlated well with I_D degradation [51]. Our results strongly suggest that the same defects appear to

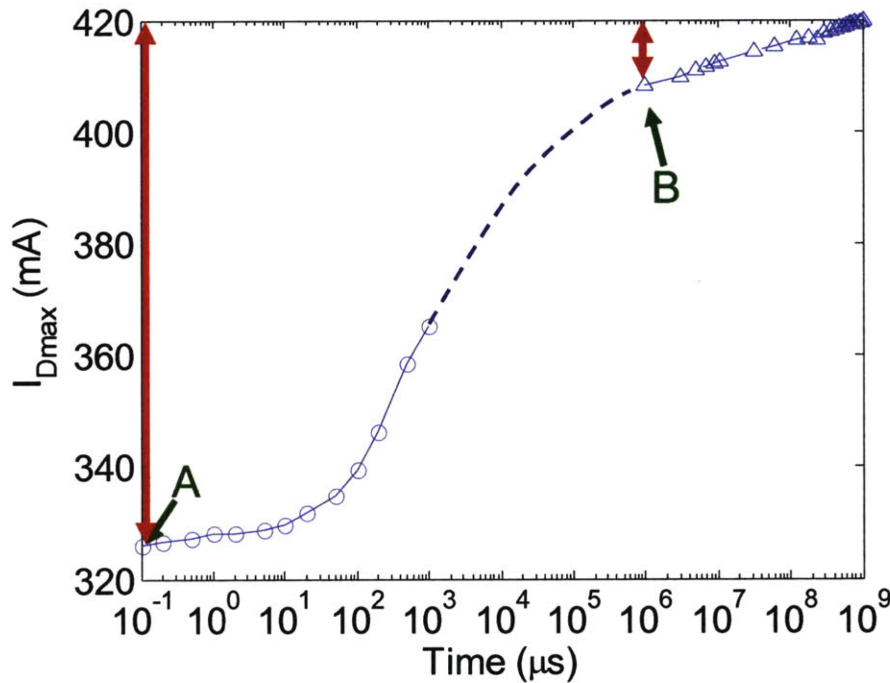

Figure 5-6. Recovery transient of I_{Dmax} after removing a bias of V_{DS}=35 V and V_{GS}=-5 V. The circle data points are measured with the pulsed I-V setup, and the triangle data points are measured with the DC setup. Points A and B are the collapsed I_{Dmax} that is measured from the pulsed current collapse and DC current collapse techniques, respectively.

be responsible for I_G degradation. Therefore, degradation in the reverse bias gate leakage current is perhaps one of the most sensitive signatures of trap formation in GaN HEMTs under electrical stress.

5.2.3. Recovery from current collapse

In Section 5.2.1, we have shown that the decrease in drain current is partially recoverable through electron detrapping with time. In GaN HEMTs, a wide range of detrapping times have been reported [45, 50, 52, 55-56]. In general, slow recovery in the order of minutes from current collapse is observed [26, 50]. In order to better understand how fast I_D recovers from a current collapseevent, we have measured the time evolution of I_{Dmax} recovery from its collapsed value at room temperature. Figure 5-6 shows the I_{Dmax} transient of a 4x100 um device following the removal of a high voltage bias (V_{DS}=35 V, V_{GS}=-5 V).

The original (uncollapsed) value of I_{Dmax} for this device is 420 mA. In this experiment, a high voltage is used to emphasize current collapse. From 0.1 us to 1 ms, I_{Dmax} is measured with a specialized pulsed I-V setup (Accent DIVA system), while from 1 s on, measurements are taken with the DC setup. Point A denotes the maximum current collapse that we can observe with this pulsed I-V system. Point B is where the value of the collapsed I_{Dmax} is measured with the DC technique that is described in Section 2.3.2. Previously, it was shown that the current collapse measurements at A and B are well correlated [60]. As shown in Figure 5-6, the recovery is almost negligible up to 100 us, and I_{Dmax} starts to slowly recover beyond that point. Even after 1 s, the recovery is not complete. From this, we confirm that taking measurements even a few seconds after current collapse is enough to observe it and evaluate it. Also, we observe that detrapping takes place over a very wide range of time from 0.1 ms to 1000 s. This motivated us to find a better method to analyze these kinds of detrapping processes and to do this in a way that can be integrated in the middle of our electrical stress experiments. This is discussed in the next section.

5.2.4. Trap analysis methodology

There are various methods to investigate trapping behavior in semiconductor material. However, these conventional methods are sometimes not suitable for studying actual semiconductor devices since the small dimension of the device makes these measurements difficult or almost impossible. One good example is a conventional deep-level transient spectroscopy (DLTS) technique [78]. Since the original technique relies on capacitance measurement, it is usually difficult to apply it to highly scaled transistors with a small gate length due to the unreliable measurement of small capacitance in a short time.

In order to overcome these difficulties, several techniques that involve current measurement have been developed to understand trapping behavior in actual transistor devices. Also for GaN HEMTs, measurement of drain current transients has been a popular and powerful technique. The gate lag and drain lag measurement [52, 55-56] and drain current DLTS

technique [79] are good examples of current transient-based technique. Also, frequency dependent transconductance measurement and low frequency noise measurement have been utilized to study trapping behavior [15, 24, 46].

In this thesis, we have developed a new methodology to study trapping behavior in GaN HEMT. This technique is integrated in the middle of stress experiments to analyze the change in trapping behavior during device degradation. This method consists of current transient measurement and its analysis to obtain time constant spectrum of the trapping and detrapping transients. The current transient is measured through the sampling mode of Agilent B1500A. In trapping experiments, certain bias voltages are applied to induce trapping, and the drain and/or gate current are sampled at certain points in a logarithmic time scale to monitor the amount of trapping. In most cases, only drain current is measured. For detrapping experiments, a trapping pulse is applied before measuring the current transient to induce current collapse. This allows us to measure a recovery transient right after removing the stimulus pulse with different bias conditions and pulse widths. In B1500A, the pulse is applied by setting pre-bias with certain duration. In principle, I_{Dmax} is the most suitable parameter to monitor the current collapse and subsequent detrapping behavior since it is directly related to device performance. However, we find that a measurement of I_{Dmax} over an extended period of time induces significant amount of trapping due to relatively high voltage. Moreover, because of large self-heating at I_{Dmax} condition (~6 W/mm), it is difficult to accurately determine the temperature which is very important in understanding detrapping. Thus, we instead measure drain current in the linear regime, I_{Dlin} (V_{GS}=1, V_{DS}=0.5 V), to monitor the recovery from the current collapse. We have experimentally confirmed that the transients of I_{Dmax} and I_{Dlin} are closely correlated. In fact, measuring I_{Dlin} is essentially identical to measuring R_{DS} (=R_S+R_{CH}+R_D), and we have already shown that I_{Dmax} and the series resistance shows the same trapping and detrapping behavior (Figure 5-4). Therefore, I_{Dlin} can represent the overall level of trapping in the device. In our system, the minimum time resolution is about 2 ms. Thus, the very first measurement of I_{Dlin} is performed 2 ms after removal of the stimulus pulse, and any

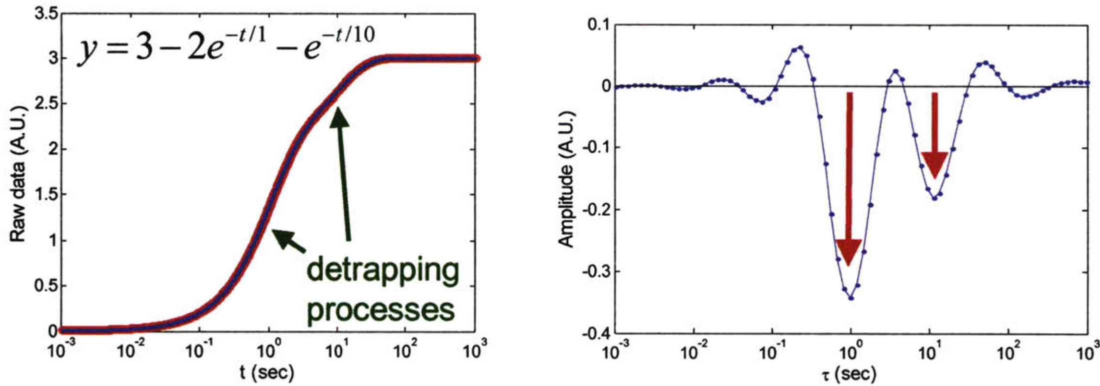

Figure 5-7. An example of the time constant analysis methodology. Left: time domain signal of an artificial current transient (red: data, blue: fitted curve). Right: time constant spectrum extracted from the fitting of the time domain signal.

information on the current collapse and its recovery before t=2 ms cannot be obtained. As it can be seen in Figure 5-6, this corresponds to about 40% of the current collapse that we can measure with a specialized pulsed I-V system at room temperature. However, by lowering the temperature, we are able to obtain significant information because thermally activated detrapping process becomes slower at lower temperature.

The trapping and detrapping transient data, $I_{data}(t)$, is analyzed by fitting them to a sum of pure exponentials in least mean-square fashion. The underlying assumption is that current transient consists of many trapping and detrapping processes and each of these processes exponentially decays over time. This assumption makes sense especially for a detrapping process because a process of recovery from a non-equilibrium state whose decay rate is proportional to the population of the state follows an exponential dependence on time. The fitting function can be expressed as:

$$I=\sum a_i \exp(-t/\tau_i)+I_\infty \quad (1)$$

For this fitting, we use 100 exponentials with time constants, τ_i, that are equally spaced logarithmically in time. Positive (negative) values of a_i correspond to trapping (detrapping) processes. Our measurement and analysis are carried out in the 10^{-3} to 10^{3} s range.

In order to show how this methodology works, we apply our fitting algorithm to an artificial data set. This is illustrated in Figure 5-7. The time domain signal in this example consists of two pure exponential recovery components with time constants of 1 and 10 s. The amplitude of the two components is 2 and 1, respectively. As it can be seen in the time constant spectrum (Figure 5-7 right) that is evaluated by the fitting the time domain data to Equation (1), this method clearly identifies two components with correct time constants that are 1 decade apart. Also, the amplitudes of the two peaks in the spectrum are proportional to those in the original data. Although two delta function-like peaks at 1 and 10 s would be ideal representation of this transient in time constant domain, the two peaks that we obtained have finite widths. Also, a few small ripples are shown around the two peaks. These non-idealities are caused by two reasons: First, we used finite number (100 in this example and throughout this chapter) of exponential components for fitting in Equation (1). Using more exponentials can reduce the width of the peaks. Second, the basis functions – decaying exponential – in Equation (1) are not orthogonal to one another. This is why we cannot do a simpler analysis, for example something similar to Fourier transform, and need a least mean square fitting. In principle, this fitting is a linear optimization problem. However, in order to prevent a possible over-fitting that makes the time constant spectrum extremely noisy, a few constraints such as lower and upper bound or smoothness in the spectrum are added. Due to these constraints, this problem mathematically turns into a non-linear optimization, and it takes quite long time to solve it. As a result, the number of exponential is limited to 100 to obtain good enough results to analyze trapping and detrapping process in our experiments and also to compute it in a reasonable amount of time.

Our methodology has several advantages over conventional trap analysis methods. First, by using a double pulse where both drain and gate voltage can be simultaneously pulsed between two arbitrary bias points, we can induce various state of trapping. In other words, we can apply various kinds of bias condition for the pulse to introduce different states of

trapping before jumping to I_{Dlin} condition to measure the detrapping transient. As discussed in Section 1.3.4, there are several sources and locations in trapping in GaN HEMT. As a result, our ability to stimulate different trapping processes by changing condition of the trapping pulse is useful for detailed physical understanding of the nature of trapping. Second, we obtain the *time constant spectrum* that shows trapping and detrapping processes in a current transient data set over a wide range of time as a whole. This can be especially powerful when multiple processes with similar time constants are present in a mixed way. As shown in the example in Figure 5-7, when a single or only a few processes are present, we can also obtain the exact time constant and relative amplitude of different processes just as in the DLTS method.

5.2.5. Trapping and detrapping behavior of a fresh device

Transient experiments in fresh and degraded devices are performed at temperatures between -60 to 130 C. First, the trapping and detrapping behavior at various bias conditions of a fresh device are investigated in order to understand pre-existing trapping behavior without any device degradation. In order not to degrade the device during the experiments, the maximum voltage is kept below 10 V in all cases. After each experiment, the initial condition of the device is completely recovered by shining microscope light for 30 s. All the experiments in this section have been performed on the same device.

5.2.5.1. Trapping behavior in a fresh device

First, we study the trapping behavior of a fresh device. To obtain trapping transient, we bias the device in the ON-state (V_{GS}=1, V_{DS}=2 to 8 V) while monitoring I_D. A typical I_D transient at V_{DS}=6 V at 30 C is shown in Figure 5-8. The corresponding time constant spectrum is also shown. As it can be seen, I_D decreases over time. This reduction in I_D is fully recoverable after microscope light illumination, suggesting it is solely due to

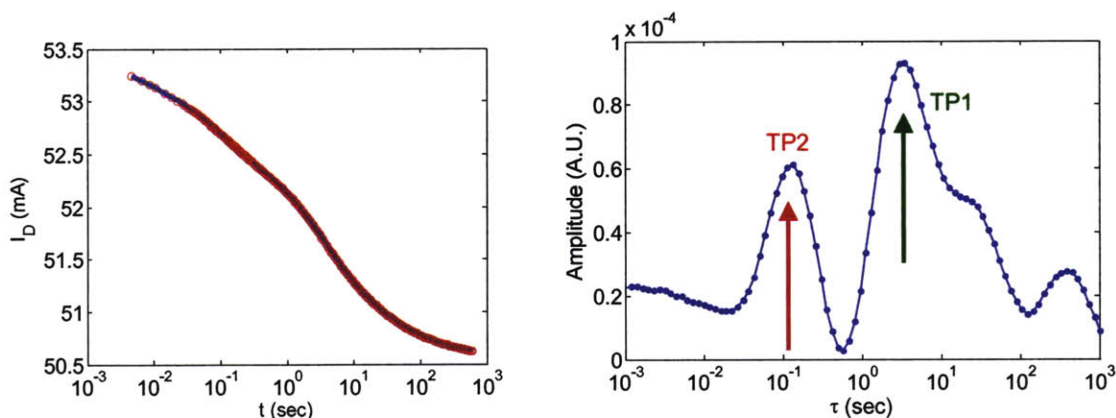

Figure 5-8. Trapping transient of I_D (left) and the corresponding time constant spectrum (right) of a fresh device in the ON state (V_{GS}=1 V, V_{DS}=6 V) at 30 C. No pulse is applied before the transient measurement. Two major trapping processes, TP1 and TP2, can be identified.

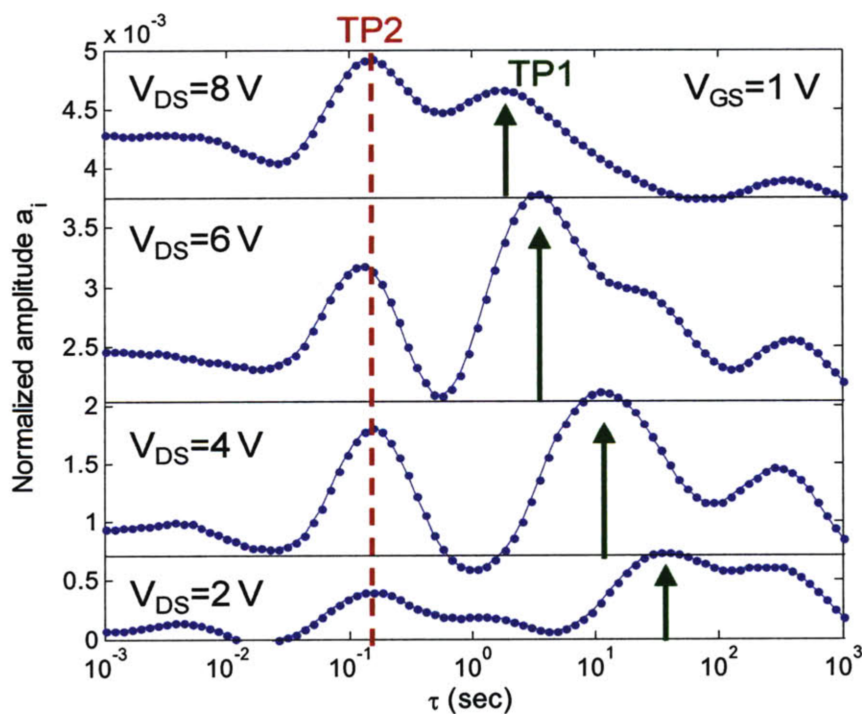

Figure 5-9. Time constant spectrum for trapping transient in the ON-state with V_{GS}=1 and different V_{DS}=2-8 V. TP1 is affected by V_{DS}, whereas TP2 is not.

temporary trapping. In the time constant spectrum, two major trapping processes, which we label TP1 and TP2, can be identified. At this temperature, the time constants of these processes are about 3 and 0.1 s, respectively. In similar experiments in which different values of V_{DS} is applied, we find that the time constant of TP2 does not change although its amplitude increases with V_{DS} (Figure 5-9). On the other hand, the time constant of TP1 reduces at higher V_{DS}. This can result from either higher temperature due to high power dissipation or higher electric field at high V_{DS}. This is discussed below.

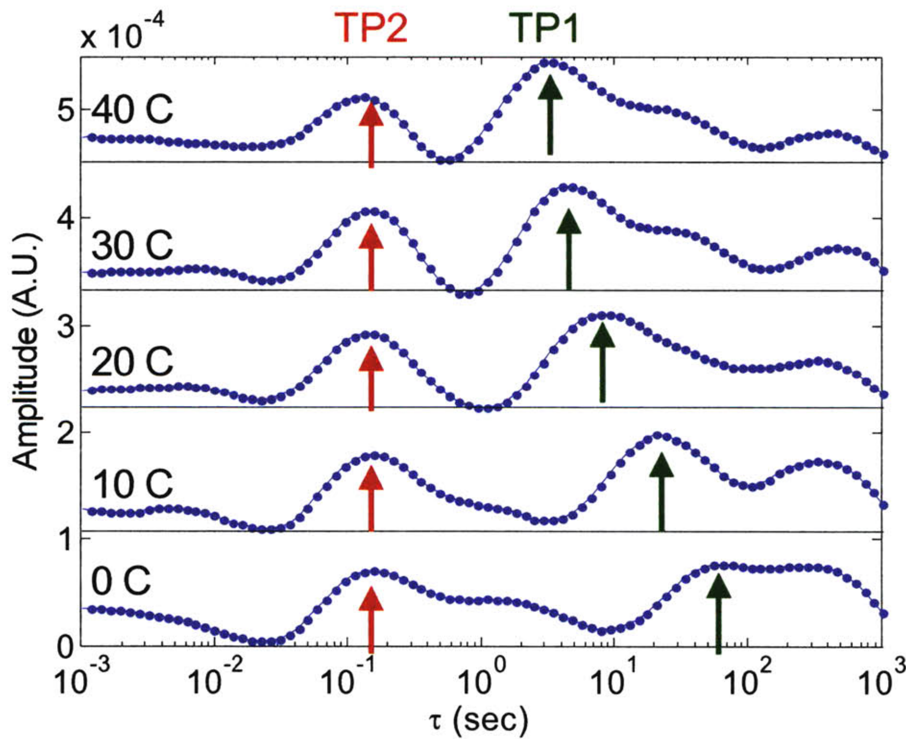

Figure 5-10. Time constant spectrum for trapping transient in the ON-state with V_{GS}=1 and V_{DS}=6 V (Figure 5-8) at different temperatures. The temperature is changed from 0 to 40 C. TP1 is affected by temperature, whereas TP2 is not.

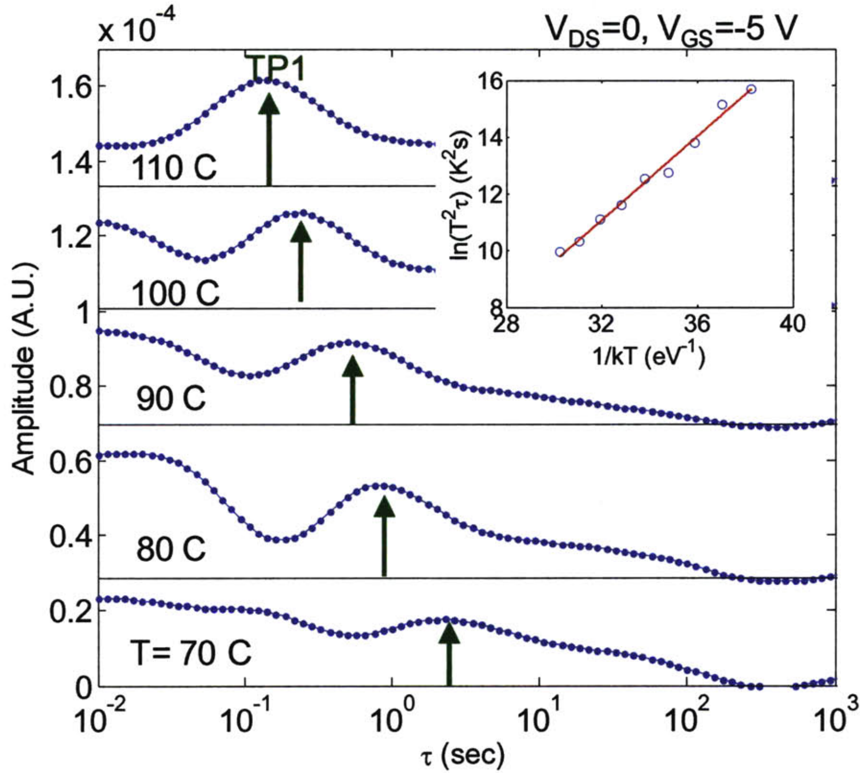

Figure 5-11. Time constant spectrum for trapping transient of I_G in the V_{DS}=0 state with V_{GS}=-5 V at different temperatures (70 to 110 C). In the inset, Arrhenius plot of the time constant is shown (E_a=0.74 eV).

In order to understand the temperature dependence of the trapping behavior in ON-state, we have performed the same experiment as in Figure 5-8 at different temperatures. Figure 5-10 shows the time constant spectrum of those trapping transients. We find that the time constant for TP1 is thermally activated, while that of TP2 is insensitive to temperature. This suggests that in trapping process TP1, electrons have to overcome an energy barrier. From the time constant of TP1 at different temperatures and voltages, its activation energy is estimated to be between 0.62 and 0.90 eV. The relatively large variation in E_a is mainly due to uncertainty in the device temperature. In the ON-state, the temperature in the device can increase significantly due to high power dissipation. Although the channel temperature can be calculated or measured through various methods [80-82], it is difficult to precisely estimate the temperature at the exact region where this trapping occurs. As a result, experiments where no self-heating occurs are preferred to extract E_a.

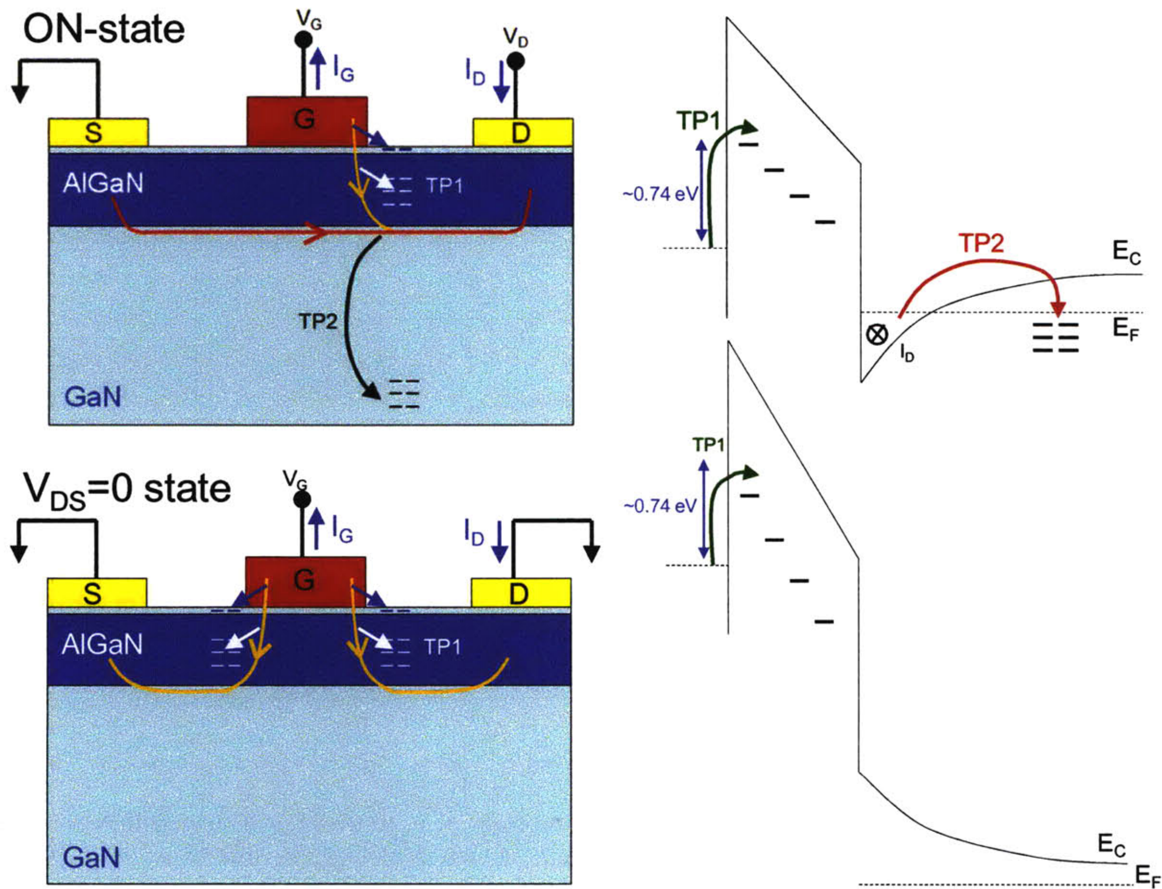

Figure 5-12. A conceptual schematic diagram of trapping behavior in the ON-state and V_{DS}=0 state. Corresponding band diagram is also shown.

A similar trapping experiments are performed in the V_{DS}=0 state where device self heating is negligible. In this case, a negative gate bias of -5 V is applied, and I_G is monitored over time because the channel current is zero. The time constant spectra in these experiments are shown in Figure 5-11. Also in this experiment, we observe a temperature dependent process. The time constant of this process is close to that of TP1 in the ON-state with V_{DG}=5 V, considering the self-heating in the ON-state. Also, the activation of the time constant is 0.74 eV, which is within the range of E_a that we observe in the ON-state experiments. This suggests that this process in the V_{DS}=0 state is the same process as TP1 in the ON-state. Interestingly, the time constant as well as E_a of TP1 in the V_{DS}=0 state does not change for different V_{GS} values. Thus, it seems that V_{DS} dependence of time constant of TP1 in the ON-state is due to temperature.

Unlike the ON-state, in the V_{DS}=0 state, we do not observe a TP2-like process that is temperature independent. Since all trapping in the V_{DS}=0 state should results from gate leakage current, we conclude that TP1 is associated with electron injection from the gate and trapping either inside the AlGaN barrier or at the surface. However, as one can see in Figure 5-11, where quite broad range of trapping processes also exists, TP1 is not the only trapping process that occurs in the V_{DS}=0 state. On the other hand, since TP2 appears only when channel current is present, it appears to be trapping of channel electrons. This process takes place in the channel or buffer. The fact that TP2 is observed at as low a voltage as V_{DG}=1 V suggests that it may not be hot-electron trapping at the surface or inside the AlGaN. A pictorial view of these trapping processes TP1 and TP2 is shown in Figure 5-12.

5.2.5.2. Detrapping behavior in a fresh device

We also examined recovery processes from a current collapse event in the same device. Figure 5-13 shows a detrapping transient of I_{Dlin} and the corresponding time constant spectrum at -20 C right after current collapse is induced by applying a 1 s long V_{DS}=0 state pulse (V_{GS}=-10 V). As one can see, at 2 ms, the V_{DS}=0 pulse introduced current collapse of about 1.3% in I_{Dlin}. Up to around 1 s, the collapsed drain current does not recover. Then the current collapse is mostly recovered in a well defined detrapping process, marked as DP1, with a time constant τ~4 s. As shown in Figure 5-14, this time constant depends on temperature and is thermally activated with a very well defined activation energy E_a=0.57 eV. A trap at around this energy level is widely observed in DLTS or other transient analyses [15, 79]. Since in the V_{DS}=0 condition we know that trapping only occurs in the AlGaN barrier or at the surface (TP1 in Figure 5-12), it is reasonable to conclude that detrapping process DP1 is a reverse process of these trapping processes, including TP1. This is schematically shown in Figure 5-15. Interestingly, the sum of activation energies of TP1 (0.74 eV) and DP1 (0.57 eV) is close to the Schottky barrier height (1.27 eV) [83]. This suggests that this trap is inside AlGaN barrier.

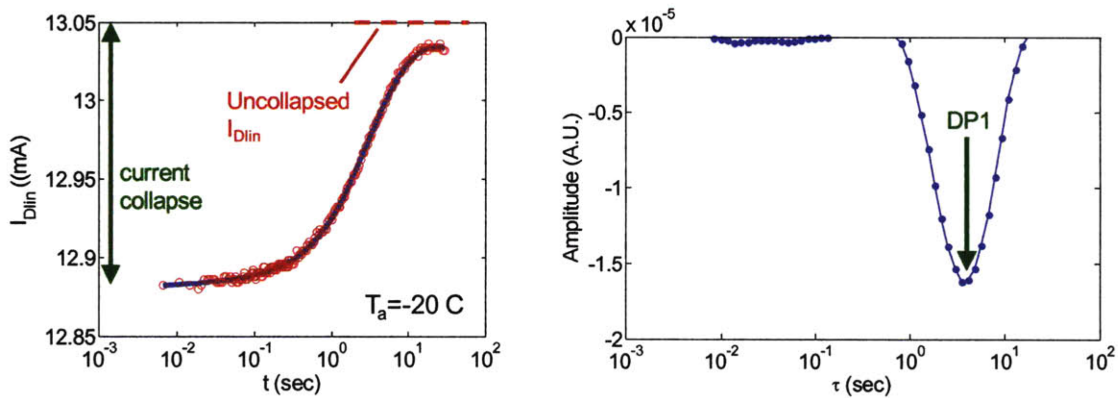

Figure 5-13. Recovery transient of I_{Dlin} (left) and time constant spectrum (right) at -20 C after applying a 1 s V_{DS}=0 and V_{GS}=-10 V pulse.

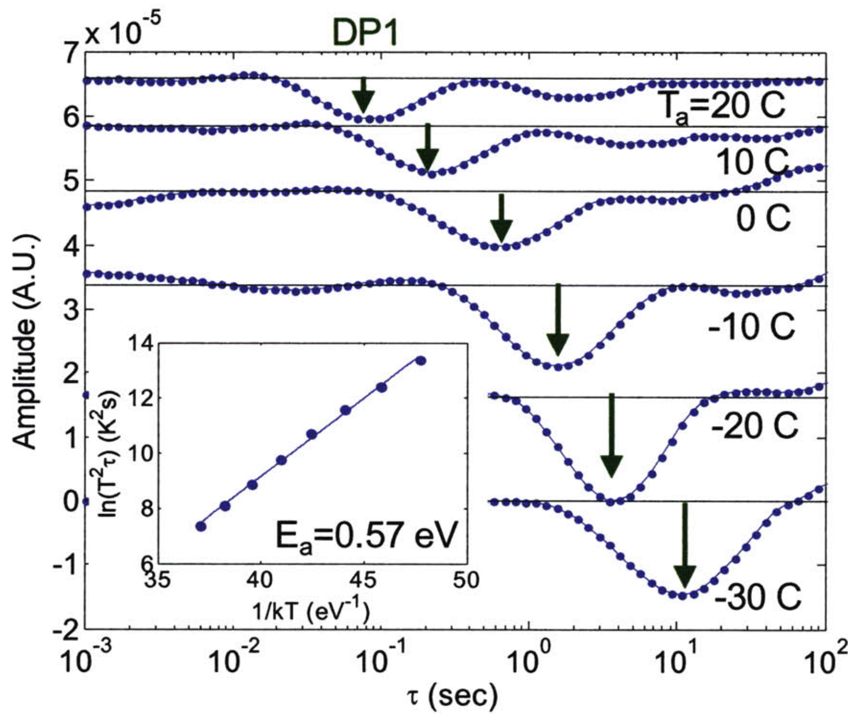

Figure 5-14. Time constant spectra of detrapping transient after a 1s V_{DS}=0 and V_{GS}=-10 V pulse for T=-30 to 20 C (inset: Time constant of DP1 as a function of temperature. E_a=0.57 eV).

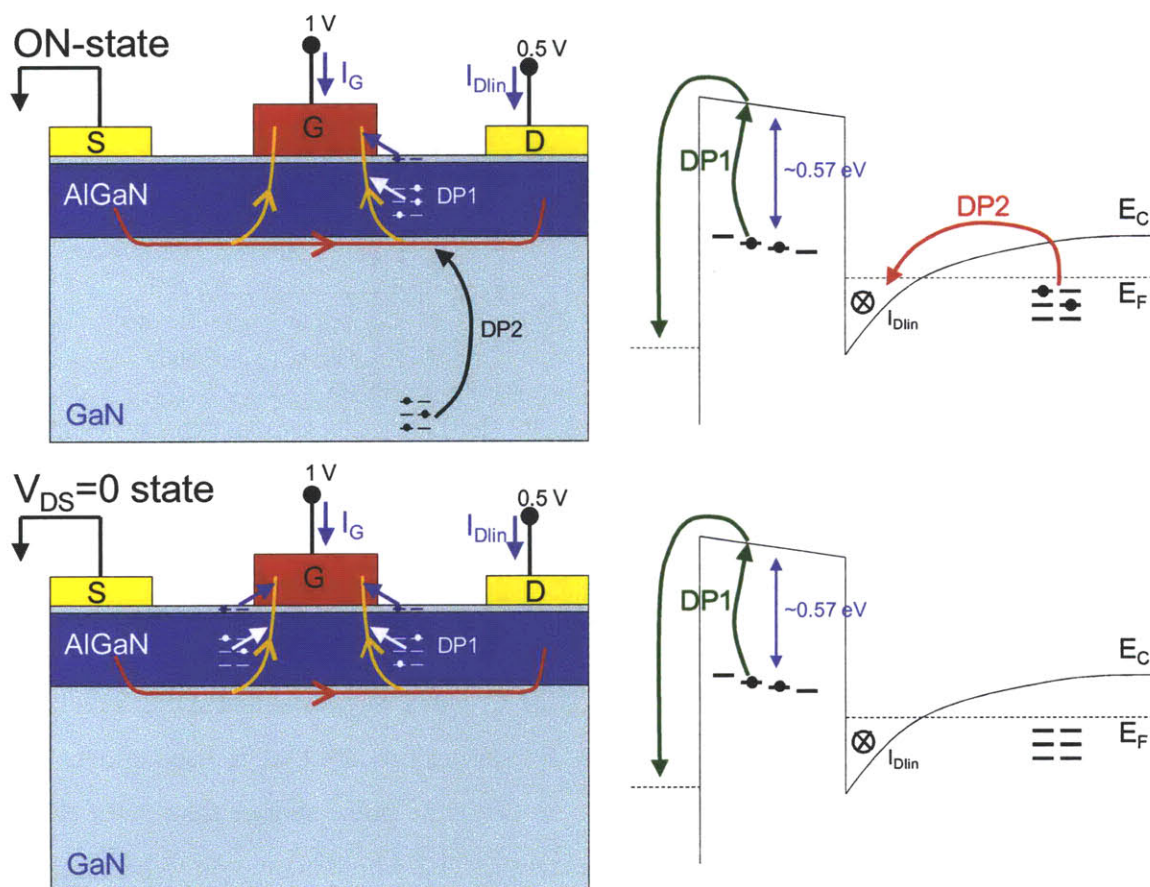

Figure 5-15. A conceptual schematic diagram of detrapping behavior after the current collapse induced by an ON-state and V_{DS}=0 state. Corresponding band diagram is also shown.

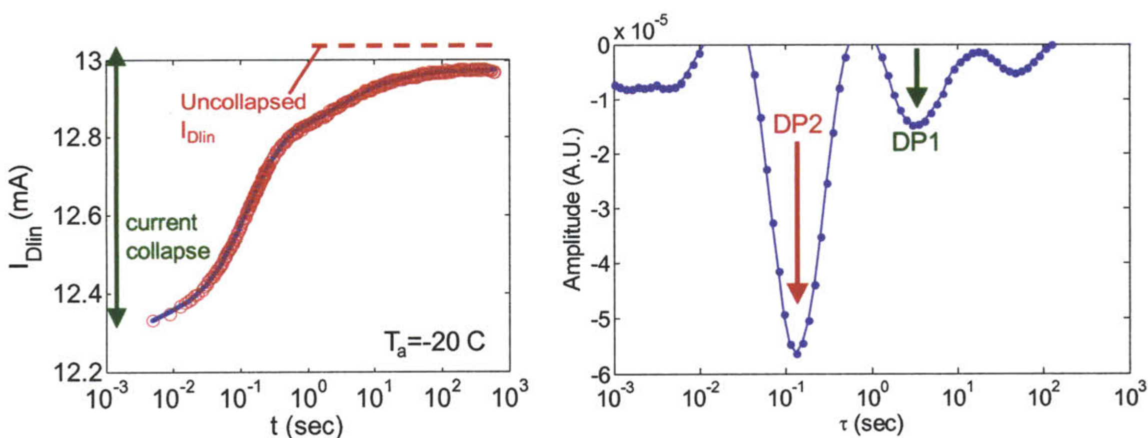

Figure 5-16. Time evolution of I_{Dlin} (left) and time constant spectrum (right) at -20 C for 10 minutes after applying 1 second V_{DS}=10 and V_{GS}=0 V pulse.

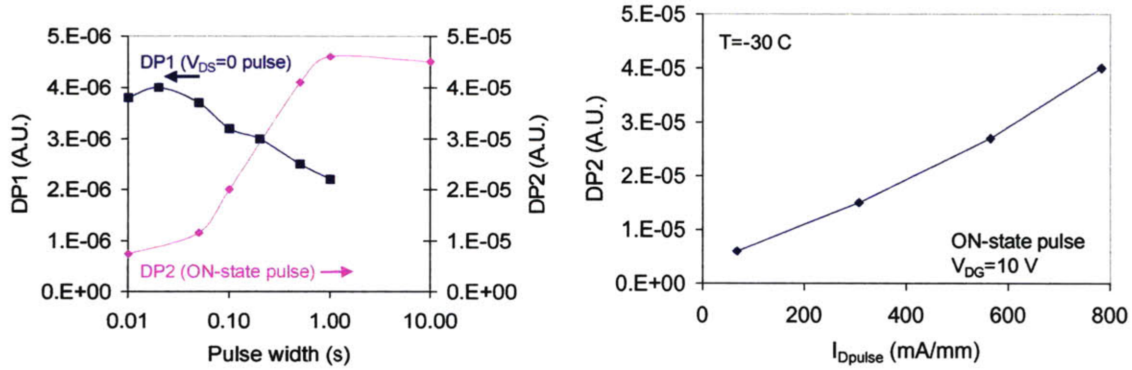

Figure 5-17. Pulse width dependence of DP1 and DP2 (left) and pulse current dependence of DP2 (right) at 30 C.

Current collapse induced by an ON-state pulse (1 s, V_{GS}=0 V, V_{DS}=10 V), during which high drain current flows, involves an additional detrapping process, DP2, with time constant τ~0.1 s (Figure 5-16). Unlike DP1, the time constant of DP2 is found to be temperature independent between -30 and 100 C. This suggests that DP2 involves a bottleneck transport process in series with a detrapping process that is itself much faster than 0.1 s. DP2 is found to be negligible for an ON state pulse shorter than 0.1 s (Figure 5-17). In fact, this coincides with the time constant of TP2 which is thought to be a trapping of channel electrons in the buffer or channel area (Section 5.2.5.1). On the other hand, DP1 does not show this kind of threshold in pulse width. Also in Figure 5-17, it can be seen that the magnitude of DP2 scales with the current level of the trapping pulse at constant V_{DG}=10 V. This is consistent with the previous finding that in the V_{DS}=0 state, both TP2 and DP2 are not present as the channel current is zero. Also, the time constant of DP2 is always exactly the same as that of TP2 observed in the ON-state trapping process. All of these results strongly suggest that DP2 and TP2 are inverse processes of each other and that both are related to buffer trapping/detrapping of channel electrons (Figure 5-12 and Figure 5-15). The time constant (~0.1 s) is the RC charging/discharging time [84] or transit time that it takes for an electron to reach the traps deep in the buffer. In fact, Binari et al. ascribed the current collapse induced by a high current and high V_{DS} pulse to trapping in the buffer [52]. A pictorial diagram of DP2 process is shown in Figure 5-15.

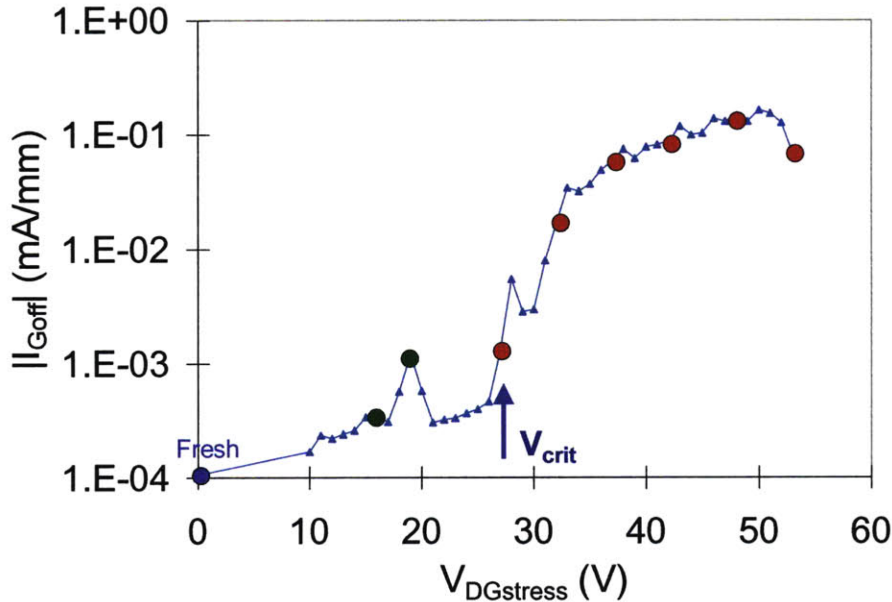

Figure 5-18. Change in I_{Goff} in an OFF-state step stress (V_{GS}=-5, V_{DS}=5~48 V). The points when transient analyses are performed are marked with solid circles. Note different colors are used to represent different level of degradation (blue: fresh, green: below V_{crit}, red: beyond V_{crit}). The same colors are used in Figure 5-19 and Figure 5-20.

5.2.6. Trapping and detrapping behavior of a degraded device

With the understanding of trapping and detrapping phenomena in a fresh GaN HEMT, we investigate the impact of electrical degradation on trapping phenomena in this section.

5.2.6.1. OFF-state step stress

In Section 5.2.1, we have shown that trap density and subsequent trapping effects increase when a device is stressed beyond the critical voltage. The trap density is found to sharply increase beyond V_{crit}. In those experiments, trapping is accessed through current collapse which is measured through a simple DC technique. We have studied this critical behavior in trapping through the trapping transient analysis method. For this, we step-stress a device in the OFF-state (V_{GS}=-5 V, V_{DS}=5-48 V in 1 V step, 1 min/step) at 100 C. The change in

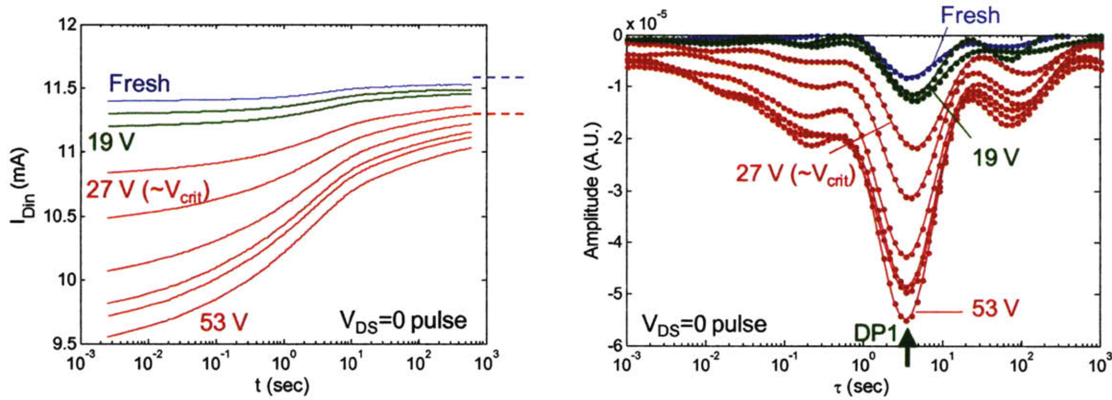

Figure 5-19. I_{Dlin} detrapping transient (left) and time constant spectrum (right) after current collapse introduced by a 1 s V_{DS}=0 and V_{GS}=-10 V pulse at -20 C. The uncollapsed levels of I_{Dlin} before and after the stress experiment are marked with dashed lines. The transient characteristics are measured for the points marked with circles in Figure 5-18.

I_{Goff} is shown in Figure 5-18. As discussed in Section 5.2.2, I_{Goff} is a sensitive indicator of device degradation. It can be seen that I_{Goff} increases by more than 2 orders of magnitude beyond the critical voltage V_{DGcrit}~27 V.

Trapping/detrapping analyses are performed before, during, and after the stress experiment. The points at which this analysis is carried out are indicated through colored circles in Figure 5-18. In Figure 5-19, I_{Dlin} transient and the corresponding time constant spectrum after a 1 s V_{DS}=0 pulse with V_{GS}=-10 V are shown. Uncollapsed I_{Dlin} level (dashed lines on top right of Figure 5-19 (left) show those levels before and after the stress experiment) decreased after stressing as a result of permanent degradation. In the I_{Dlin} transient, it can be seen that current collapse increase sharply for stress beyond the critical voltage. Also, in the time constant spectrum, DP1 is sharply enhanced and traps with a broad range of time constants are introduced beyond V_{crit}. In addition, after the stress, slow traps (τ>10 min) are produced, which can be seen from the difference between the uncollapsed I_{Dlin} and its value after 10 minutes of recovery from the current collapse. Although I_{Dlin} keeps recovering, the transient measurements are stopped at 10 minutes.

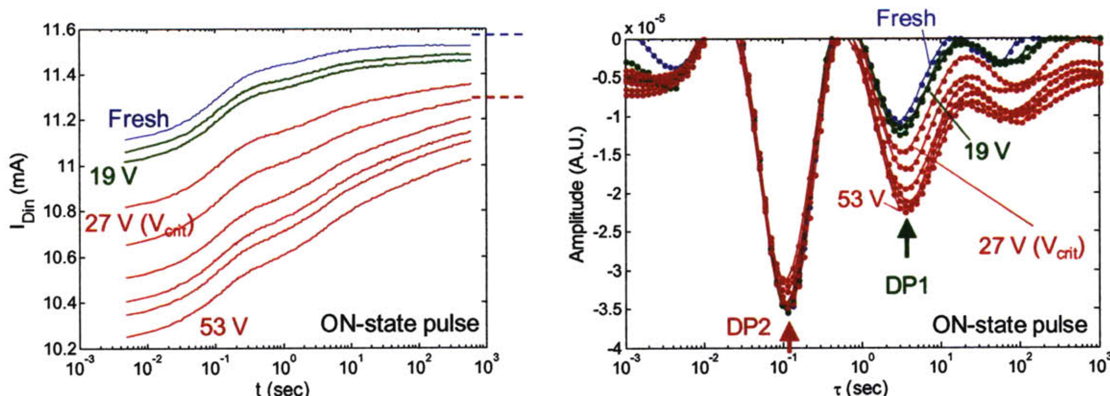

Figure 5-20. I_{Dlin} detrapping transient (left) and the time constant spectrum after current collapse introduced by a 1 s ON-state (V_{DS}=10 and V_{GS}=0 V) pulse at -20 C. The transient characteristics are measured for the points marked with circles in Figure 5-18.

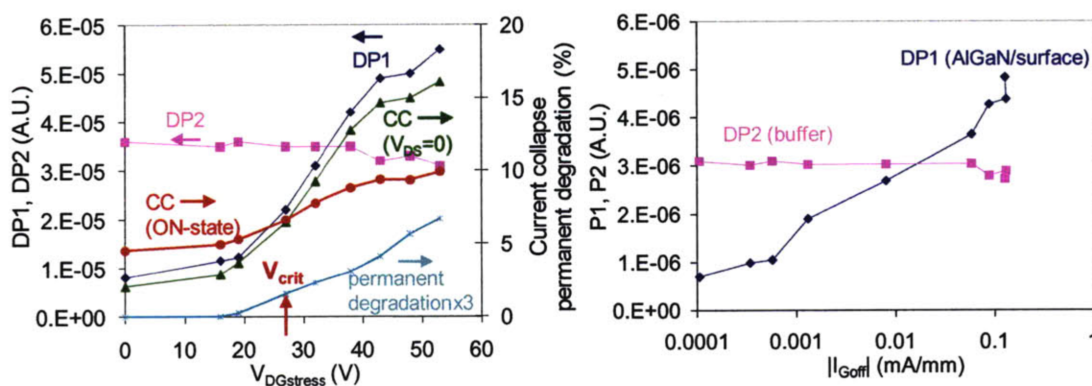

Figure 5-21. Left: change in DP1, DP2, and current collapse due to V_{DS}=0 and ON-state pulse, and permanent degradation in I_{Dlin} as a function of the stress V_{DS} in the experiment of Figure 5-18. Right: correlation between I_{Goff} degradation and trapping processes.

A similar trend is observed for detrapping after a 1 s ON-state pulse (V_{GS}=0 and V_{DS}=10 V). This result is shown in Figure 5-20. However, unlike DP1, DP2 does not increase at all after stressing. This shows that no damage is introduced in the buffer layer. The results of this experiment are summarized in Figure 5-21. First, the current collapse induced by the V_{DS}=0 pulse as well as DP1 increases more than 3 times beyond V_{crit}. The current collapse induced by the ON-state pulse also increases, but this increase is mostly due to the increase in DP1 as shown in Figure 5-20 (right) and DP2 does not show any change. A critical behavior is also evident in the magnitude of permanent degradation that is measured by the

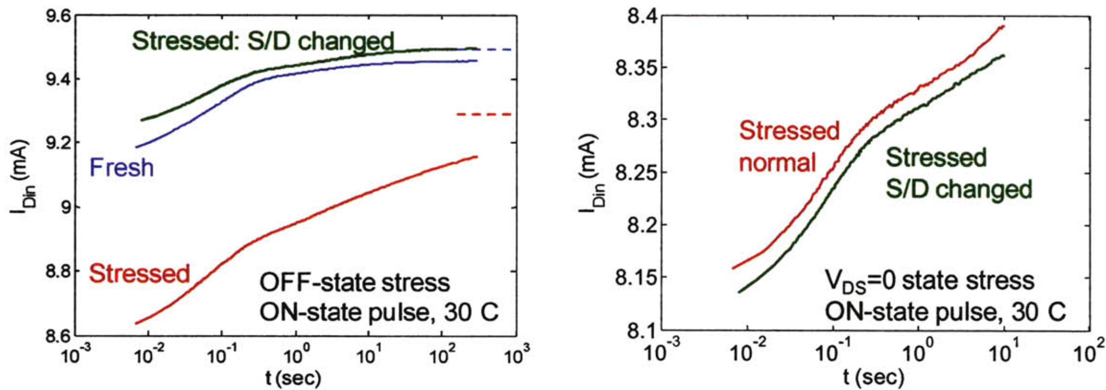

Figure 5-22. I_{Dlin} detrapping transient of a degraded device after current collapse introduced by 1 s V_{DS}=10 and V_{GS}=0 V (normal) and V_{SD}==10 and V_{GD}=0 V (S/D changed) pulses at 30 C. The devices are degraded in the OFF-state (left) and V_{DS}=0 state (right).

uncollapsed value of I_{Dlin}. All of these observations are consistent with the result in Section 5.2.1. It can be also seen that degradation in trapping behavior (DP1) and I_{Goff} degradation are well correlated (Figure 5-21 (right)) [11]. This confirms that degradation in reverse leakage current is indeed a sensitive signature of device degradation.

In order to establish the location of the traps that are created during the OFF-state stress, we measure the transient after an identical ON-state pulse with the source and the drain switched (V_{SG}=10 V, V_{DG}=0 V). During this pulse, a high electric field is applied in the source-gate region, and traps in that region are filled by the (reversed) ON-state pulse. Since in this pulse V_{DG}=0, trapping is unlikely to occur in the drain side. As shown in Figure 5-22 (left), we find that the current transient and the amount of current collapse are almost unchanged from the unstressed state when the source and the drain side are exchanged. On the other hand, for the normal direction ON-state pulse, the current collapse is largely increased. This indicates that the source side of the device is intact, and the generated traps are mostly localized in the gate to drain region. This result confirms our finding in Section 5.2.2, where we have shown that only R_D and I_{GDoff} show degradation and trapping behavior after the OFF-state stress. In contrast, as shown in Figure 5-22 (right), a device that is symmetrically stressed in the V_{DS}=0 state do not show a significant difference when the source and the drain are exchanged. All of these results are consistent

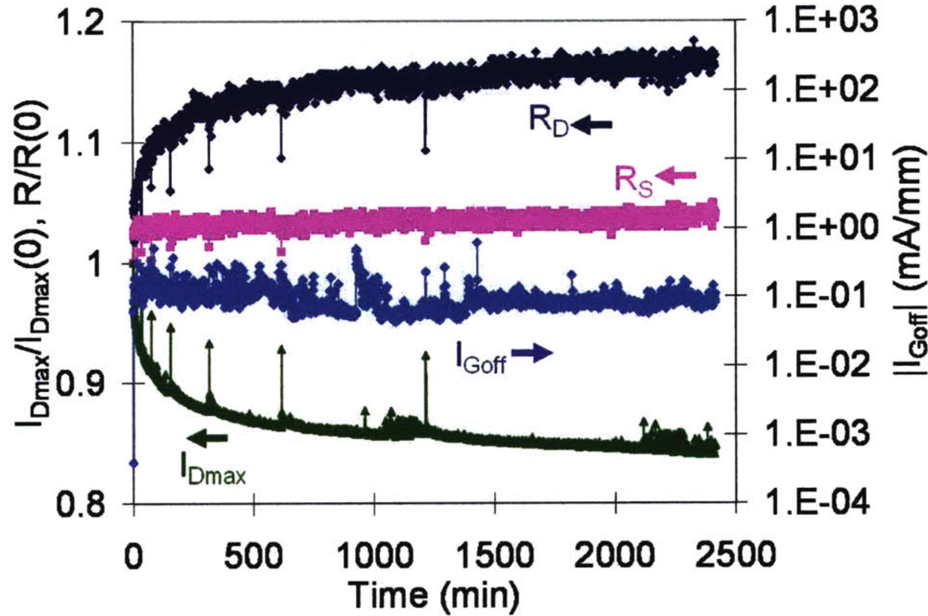

Figure 5-23. Time evolution of I_{Dmax}, R_D, R_S, and I_{Goff} in OFF-state stress. The stress condition is V_{GS}=-5 and V_{DS}=40 V at 100 C. These figures of merit are measured at 100 C.

with our hypothesis that the inverse piezoelectric effect introduces deep states by producing crystallographic defects under the high-field edge of the gate.

5.2.6.2. Long-term stress

In the previous section, we have shown that both trapping-related and permanent degradation sharply increase at V_{crit}. Although the voltage is the most important degradation driver, it is not clear how fast this degradation occurs beyond V_{crit}. In order to understand the time component of trapping-related and permanent degradation, we have performed a constant-stress experiment in the OFF state. The stress condition for this experiment is V_{GS}=-5 and V_{DS}=40 V at 100 C. At the beginning of the experiment and at several points during the experiment, the trapping dynamics as well as the permanent degradation are characterized at 30 C by the drain current transient method. These are measured after stopping the stress at certain points and shining microscope light to detrap

electrons. Figure 5-23 summarizes the result of the experiment. Since the stress condition is beyoud V_{crit}, I_{Goff} sharply increases in the first few minutes and then remains almost unchanged. As the stress proceeds, I_{Dmax} decreases and R_D increases, while R_S remains relatively unchanged.

As shown in detrapping transients and their time-constant spectrum after a 1 s V_{DS}=0 pulse with V_{GS}=-10 V (Figure 5-24), trapping-related degradation sharply increases in the early stages of the experiment and then the increase slows down. The current collapse increases up to around 300 min but not much beyond. We also observe an increase in DP1 that saturates around the same time. As we have seen in the step-stress experiments, DP2 does not change throughout the experiment (not shown).

The change in current collapse and permanent degradation measured from uncollapsed I_{Dlin} are summarized in Figure 5-25. It can be seen that the increase in current collapse evaluated at t=2 ms tends to saturates in 300 min (Figure 5-25 left). On the other hand, the density of very slow traps (detrapping time constant > 10 min) keeps increasing (Figure 5-25 right). However, the contribution of these slow traps to current collapse is relatively small. In addition, permanent degradation keeps increasing throughout the experiment. This is somewhat different from the previous observation in short-term step-stress experiments where the increase in trapping density and permanent degradation are closely correlated. At this point, it is not clear whether there is a separate mechanism for permanent degradation that takes place in a long time scale. Another possibility is that electrons are permanently trapped (or cannot be detrapped in a short time even under light illumination) at the traps that are produced during the early stage of the experiment.

We have also performed a similar experiment at 150 C (not shown). In that experiment, we observe the same trend with faster saturation in the trap increase but larger current collapse. Also, more permanent degradation takes place (9% in 20 hours). This shows that this degradation process is thermally activated.

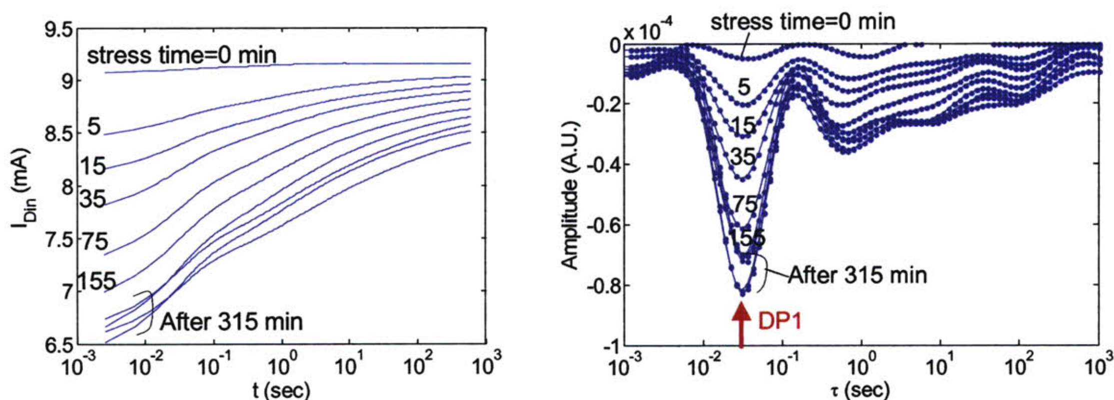

Figure 5-24. Evolution of detrapping transients of I_{Dlin} (left) and corresponding time constant spectrum (right) after applying V_{DS}=0 pulse (V_{GS}=-10 V, 1 s) at 30 C in the experiment in Figure 5-23.

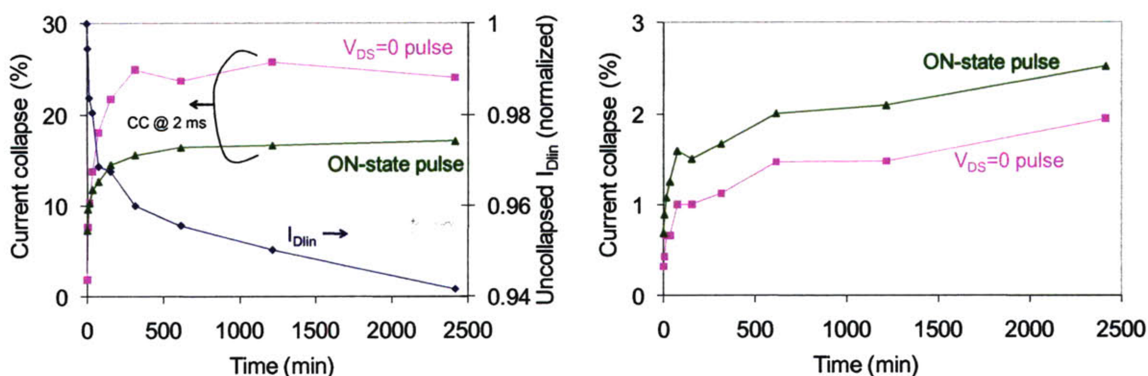

Figure 5-25. Change in permanent degradation in I_{Dlin} and current collapse after applying a V_{DS}=0 pulse (1 s V_{DS}=0 and V_{GS}=-10 V) and an ON-state pulse (1 s V_{DS}=10 and V_{GS}=0 V) at 30 C for the experiment in Figure 5-23. The current collapse is evaluated 2 ms (left) and 10 min (right) after applying the pulse.

In order to understand the possible role of hot-electrons in trapping-related and permanent degradation, we have performed a similar experiment in the high-power state. The stress condition is V_{GS}=0 and V_{DS}=40 V at room temperature. During the stress, the drain current is around 750 mA/mm. This large current and high voltage produces a large amount of hot electrons. The overall result is shown in Figure 5-26. In general, we obtain similar results as in Figure 5-23. However, in spite of a very high channel temperature of 235 C that we

estimate from the method in [81], degradation in I_{Goff} is smaller than that during the OFF-state at base plate temperature of 100 C (Figure 5-23).

The change in current collapse and permanent degradation in this experiment are summarized in Figure 5-27. From the decrease in uncollapsed I_{Dlin}, it can be seen that the permanent degradation in the high-power state is much larger than in the OFF-state. Considering trapping-related degradation, the increase in current collapse due to a $V_{DS}=0$ pulse is much smaller, and the increase in DP1 is negligible (not shown) compared to the OFF-state, which suggests much less defect formation in the AlGaN or surface region in the high-power state. This is consistent with the smaller increase in I_{Goff}. On the other hand, the increase in current collapse due to ON-state pulse is comparable to that during the OFF-state. However, this increase during the high-power state is solely due to formation of relatively long time constant (>1 s) traps, not an increase in DP1 as in the OFF-state. It can be also seen that formation of very slow traps (τ>10 min) occurs at a lower rate than in the OFF-state (Figure 5-27 right). This weaker and slower trap formation in high-power stress may partially results from lower electric field due to high current. Also, the average temperature as opposed to the peak channel temperature in the device seems to be important in trap formation as we have shown in Section 3.3.3 that larger current collapse is introduced after stressing at higher temperature. In spite of higher peak channel temperature during the high-power state stress, the temperature decreases fast from the hot area [85], and thus average temperature is lower than the previous OFF-state experiment where the whole device is at 100 C. On the other hand, the larger permanent degradation and the sizable increase in current collapse for the ON-state pulse that are seen in the high-power state stress test appears to be due to hot-electron related degradation, since they are not as evident in the OFF-state experiment.

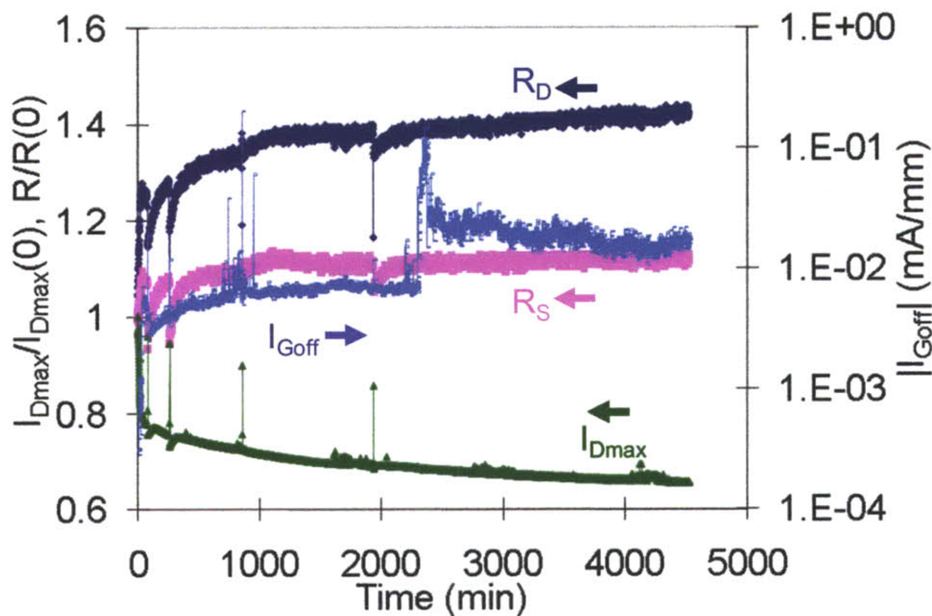

Figure 5-26. Time evolution of I_{Dmax}, R_D, R_S, and I_{Goff} in high-power state stress. The stress condition is V_{GS}=0 and V_{DS}=40 V ($I_{Dstress}$~750 mA/mm) at room temperature.

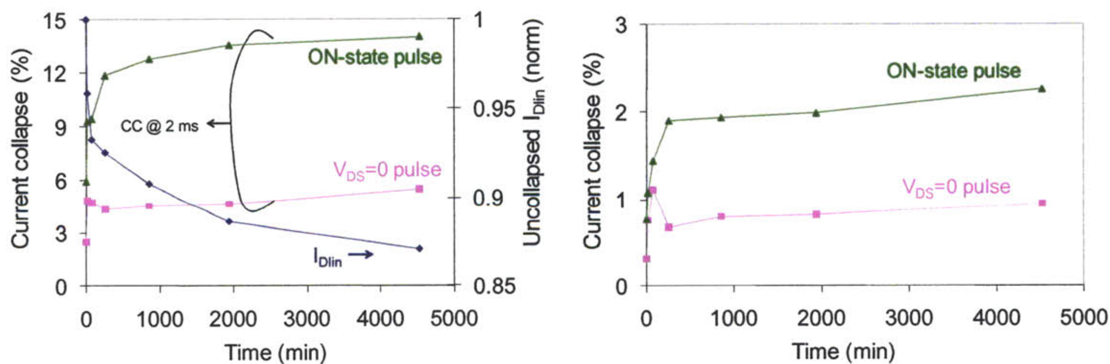

Figure 5-27. Change in permanent degradation in I_{Dlin} and current collapse after applying a V_{DS}=0 pulse (1 s V_{DS}=0 and V_{GS}=-10 V) and an ON-state pulse (1 s V_{DS}=10 and V_{GS}=0 V) at 30 C in a high-power stress test. The current collapse is evaluated 2 ms (left) and 10 min (right) after applying the pulse.

5.3. Degradation under DC and RF stress

So far, we have studied degradation mechanisms in GaN HEMTs through DC stress tests. However, in principle, what eventually matters in the end is the reliability during RF operation. Because of this, thermally accelerated RF life tests (RFLT) are widely accepted as the most reliable way to evaluate reliability and device lifetime of RF amplifiers in the field. However, RF life tests require a rather complicated setup, and an accurate and controlled device channel temperature is sometimes very difficult to achieve. This is especially the case for high-power density technologies such as GaN HEMT or high-voltage GaAs PHEMT. This is because: a) large self-heating, b) uncertainty in RF power levels at the device plane, and c) changes in load lines with temperature. Also, in terms of understanding the physics of degradation, RFLT is somewhat cumbersome because change in RF output power can result from many different reasons. However, this can be complemented by introducing detailed device characterization in the middle of the RF stress experiments.

In order to overcome the complexities in RFLT, DC life tests (DCLT) are often preferred due to their simplicity [9]. In addition, better insight of failure mechanisms can be obtained by monitoring changes in multiple DC parameters such as I_{Dmax} and V_T during DC stress tests as we have seen in this thesis. Though simple to implement, DC life tests have several limitations. This is because DC life tests at most can only hope to emulate the DC conditions of the RF amplifier and not the impact of RF swing. As a result, the choice of stress bias conditions is not obvious, and sometimes they can be immune to certain types of degradation (e.g. RF breakdown degradation) that could be present only under RF conditions.

Then, an important question arises: are various modes of degradation that we have identified in DC experiments really relevant to RF degradation? In order to answer this question, it is of great importance to understand the relationship between DC degradation

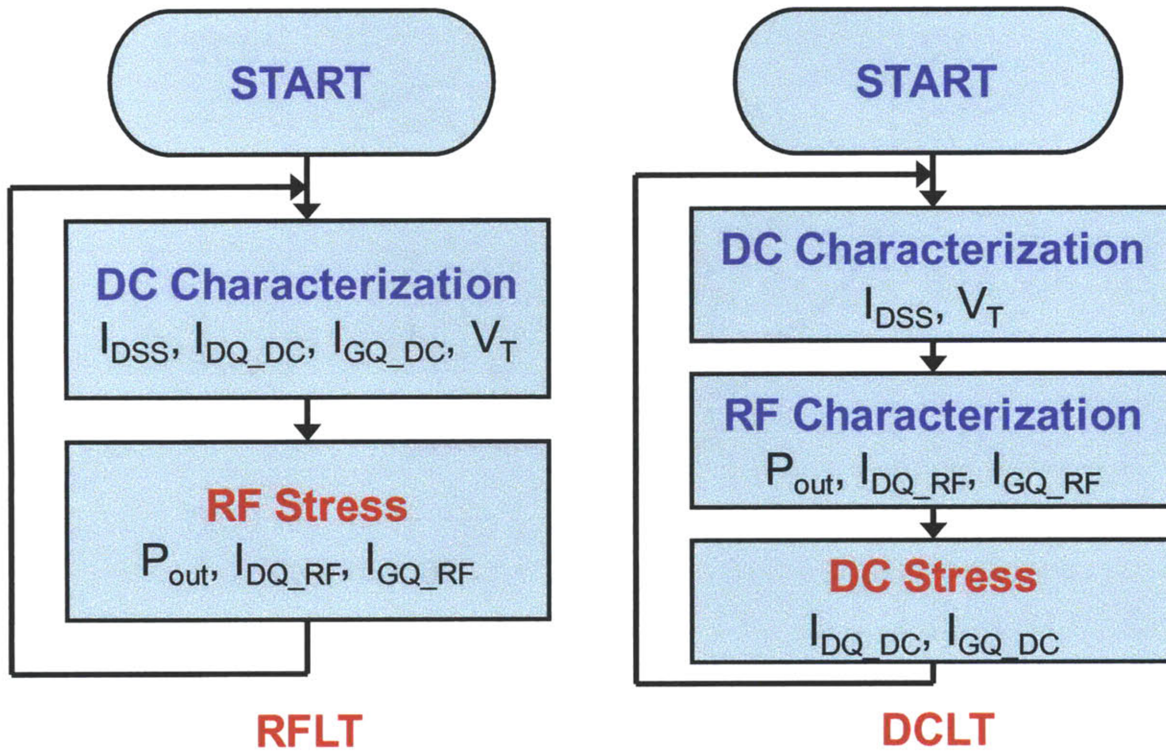

Figure 5-28. Flow charts of RF life test (left) and DC life test (right) where complementary DC and RF figures of merit are characterized.

parameters during DCLT and RF power degradation during RFLT [18]. This can be partially achieved by introducing RF characterization in the DCLTs.

In this section, we study the correlation between the degradation of DC and RF figures of merit during DCLT and RFLT. For this, we perform RFLT and DCLT in a special purpose RF life test system with the device mounted on an RF test fixture. During the course of both types of life tests, we monitor both RF and DC parameters. This allows us to map the correlation between DC parameter measurements in DCLT experiments and RF parameter measurements in RFLT experiments. The procedures of these experiments are shown in Figure 5-28. For this study, we use 4x100 um GaN single stage amplifiers [9].

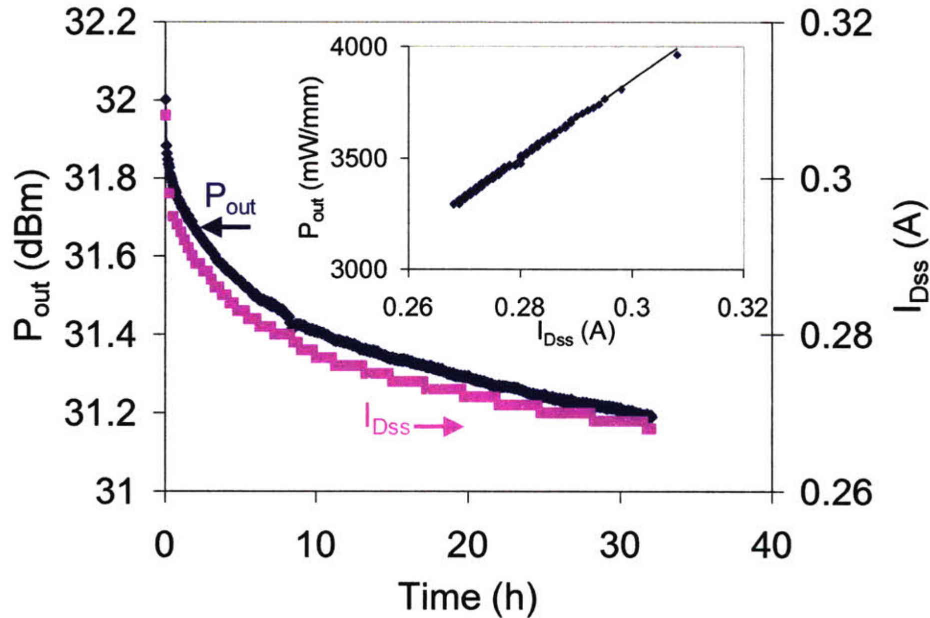

Figure 5-29. Time evolution of output power and I_{DSS} in an RF life test. Correlation between output power and I_{DSS} is shown in inset.

5.3.1. RF stress test

First, we have performed RF life tests while monitoring several DC and RF parameters during the stress test (Figure 5-28 left). The stressing condition is V_{DS}=40 V with P_{in}=23 dBm (2-3 dB compression) at elevated base plate temperature. V_{GS} is initially set to yield I_{DQ}=50 mA/mm and is then kept constant throughout the experiment. During the RF stress, several RF parameters are measured: P_{out}, I_{DQ_RF}, and I_{GQ_RF} (I_D and I_G at quiescent bias condition under RF input). The RF stress is removed every 15 minutes, and several DC parameters are evaluated including I_{DQ_DC} and I_{GQ_DC} (I_D and I_G at quiescent bias condition without RF input), I_{DSS} (I_D at V_{DS}=5 V and V_{GS}=0 V; I_{Dmax} may be a better choice, but due to instrumental limitation, we measure I_{DSS}, which is close to I_{Dmax}), and V_T.

Figure 5-29 shows the change in P_{out} and I_{DSS} in the RFLT experiment. As it can be seen, P_{out} as well as I_{DSS} decrease over time. We find that the decrease in I_{DSS} correlates very well with the decrease in P_{out} (Figure 5-29 inset). While degradation in I_{DSS} shows good

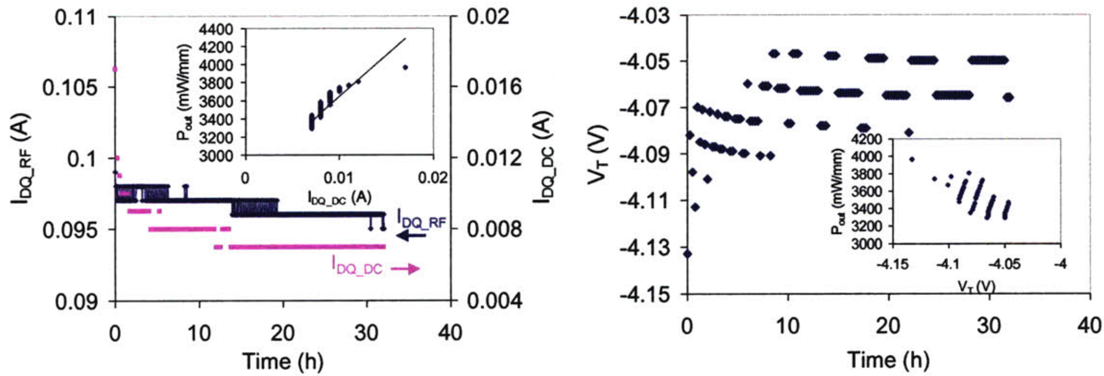

Figure 5-30. Left: change in I_{DQ} (under RF and without RF) in the RFLT in Figure 5-29. Correlation between output power and I_{DQ_DC} is shown in inset. Right: change in V_T in the same experiment. The inset shows correlation between P_{out} and V_T.

correlation with that in P_{out}, I_{DQ} (both under RF and without RF) shows a weaker correlation (Figure 5-30 left). It can be seen that I_{DQ_DC} drops very fast at the beginning and remains unchanged after about 12 hours of stress. In the inset, one can see a poorer correlation between I_{DQ_DC} and P_{out}. Other DC parameters also did not show any significant correlation with P_{out}. In particular, V_T shifts only +0.08 V in this experiment, which shows no significant gate sinking or gate metal diffusion (Figure 5-30 right).

The strong correlation between I_{DSS} and P_{out} degradation and the lack of correlation between other DC parameters such as I_{DQ_DC} or V_T and P_{out} degradation suggest that I_{DSS} degradation is the main component in RF output power degradation of saturated single stage GaN amplifiers. This strong and linear correlation shows that RF breakdown voltage degradation is not an important factor in P_{out} degradation. In industry, it is a usual practice to perform DC life tests under constant V_{DS} and I_D (though often times, at constant V_{GS} instead of constant I_D) and at a constant base plate or channel temperature. In many cases, only I_{DQ} (I_D at stressing V_{DS} and V_{GS}) is monitored to evaluate degradation although it is generally preferred to monitor additional electrical parameters such as I_{Dmax}, I_{DSS}, or V_T. Failure time is defined as the time it takes for one or more of these parameters to degrade by a certain amount (e.g. 10% degradation in I_{DQ}). Our result here suggests that using

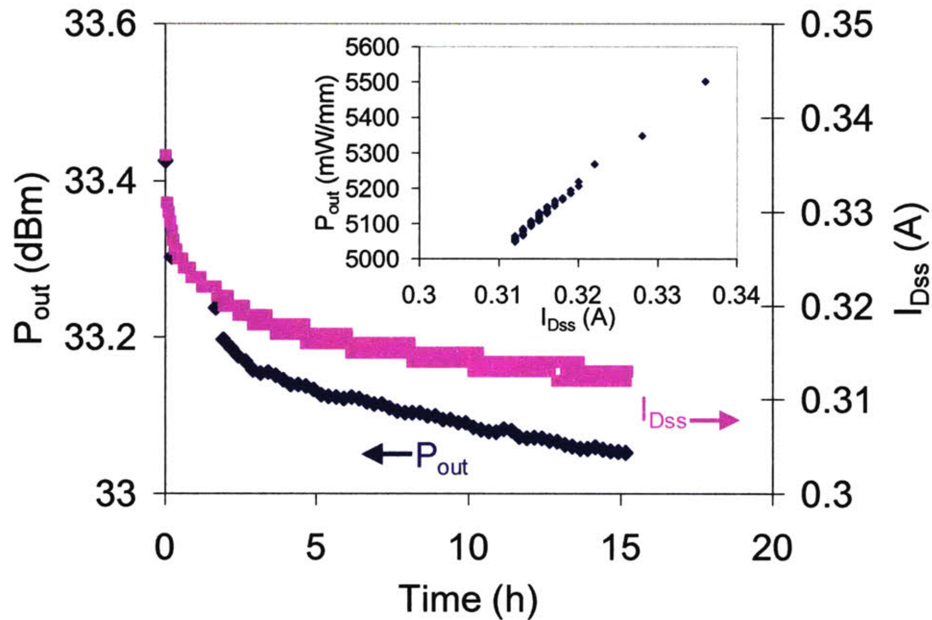

Figure 5-31. Change in I_{DSS} and P_{out} in a DC life test. The correlation between I_{DSS} and P_{out} is shown in the inset.

I_{DQ_DC} to establish failure criteria in DCLT might not be suitable in the estimation of a meaningful device life time.

5.3.2. DC stress test

In order to understand how DCLT results correspond to actual RF performance degradation, we have performed DC life tests where we have evaluated the device through DC and RF figures of merit (Figure 5-28 right). As in our RFLT experiments, we stop the DC stress every 15 minutes and extract the same DC parameters. In addition, we also characterize the devices for RF and extracted their RF output power and I_{GQ_RF} and I_{DQ_RF}. During RF characterization, an input power of 23 dBm and V_{DS}=40 V are applied. In order to maintain the channel temperature the same as that in the RFLT, V_{GS} is initially set to keep I_{DQ}=175 mA/mm with V_{DS}=40 V. The base plate temperature is identical as in the RFLT experiments. By measuring RF output power, we can correlate DC degradation in DCLT with RF performance.

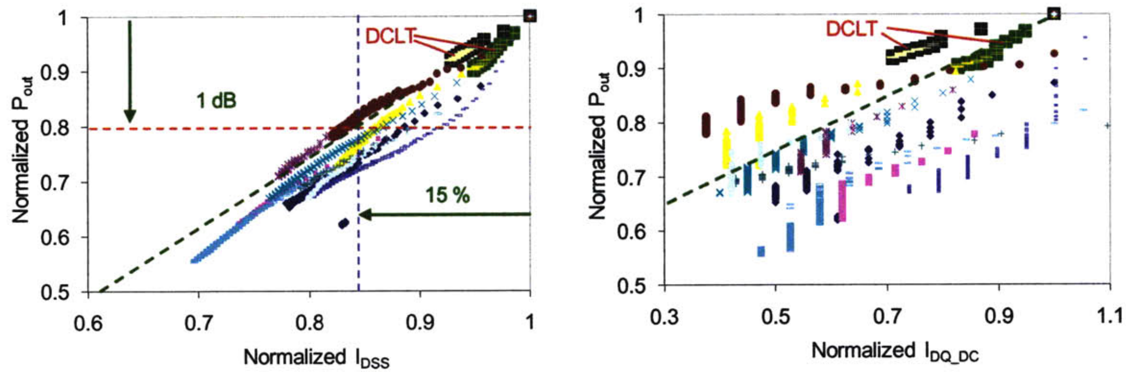

Figure 5-32. Correlation between P_{out} and I_{DSS} (left) and between P_{out} and I_{DQ_DC} (right) in 10 RFLT and 2 DCLT experiments.

Figure 5-31 shows the change in P_{out} and I_{DSS} in this experiment. Again, we find a good correlation between degradation of P_{out} and that of I_{DSS} during DCLT (Figure 5-31 inset). As in the RFLT, degradation in other DC parameters (I_{DQ_DC} or V_T) does not correlate well with P_{out} degradation (not shown). This suggests that the degradation in I_{DSS} (or I_{Dmax}) that we observe in our DC experiments is in fact a good predictor of degradation in RF performance and that, for the conditions that we have examined, it is not I_{DQ_DC} but I_{DSS} (or ultimately I_{Dmax}) that needs to be monitored with highest priority during DCLTs. I_{DQ_DC} change is more sensitive to V_T changes especially when it is much lower than I_{Dmax}. As shown in Figure 5-30, the V_T change does not correlate with P_{out} degradation.

To understand and quantify how good the correlations between P_{out} and DC parameters are, we perform the same RFLT experiment as in Figure 5-29 on 10 identical GaN amplifiers and two DCLT experiments as in Figure 5-31. P_{out} vs. I_{DSS} and P_{out} vs. I_{DQ_DC} correlations in these experiments are shown in Figure 5-32. It can be seen that for all devices, P_{out} vs. I_{DSS} correlation is almost linear and very tight with a consistent slope, whereas P_{out} vs. I_{DQ_DC} correlation is much weaker and scattered. It should be noted that correlation between I_{DSS} and P_{out} in DCLT is consistent with that in RFLT although the level of degradation is much smaller as discussed below. Other DC parameters also show a poor correlation with P_{out}.

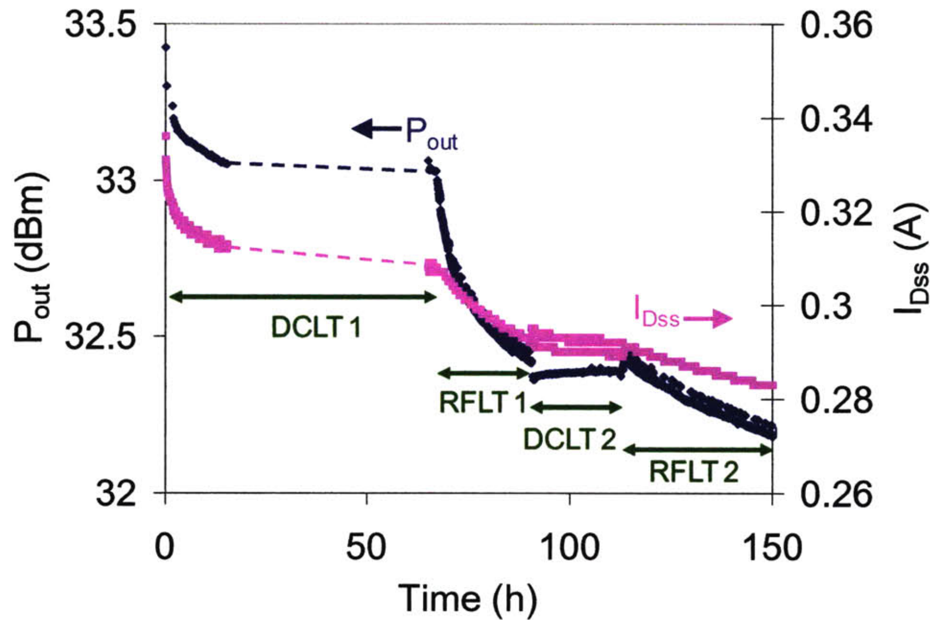

Figure 5-33. Change in P_{out} and I_{DSS} in a stress experiment. For t=0 to 65 hr, DC stress is applied (for t=15 to 67 hr, the data is not recorded). For t=67 to 90 hr, RF stress is applied. After that, another DC and RF stress cycle is performed.

We have calculated the sensitivity of a change in P_{out} to a change in I_{DSS}, $(\Delta P_{out}/P_{out}(t=0))/(\Delta I_{DSS}/I_{DSS}(t=0))$. The average is 1.34, which means that 1% change in I_{DSS} corresponds to 1.34% change in P_{out} (or 15% I_{DSS} drop to 1 dB drop in P_{out}). The standard deviation of this sensitivity among 10 devices in RFLT is 12% of the mean value. For I_{DQ_DC}, the average is 0.49 with standard deviation of 26%. These statistics confirm that I_{DSS} tracks P_{out} change much better than I_{DQ_DC}. These results strongly suggest that rather than degradation in I_{DQ_DC}, degradation in I_{DSS} (or I_{Dmax} depending on the load line) is the parameter to focus on when calculating the device life time. As mentioned earlier, this poor correlation in I_{DQ_DC} arises from changes in V_T which does not significantly impact P_{out}.

In order to study whether RF stress degrades the device similarly to DC stress, we have performed combinations of DC stressing and RF stressing on the same device. A typical experiment is shown in Figure 5-33. In this case, the device is stressed first in DC and then

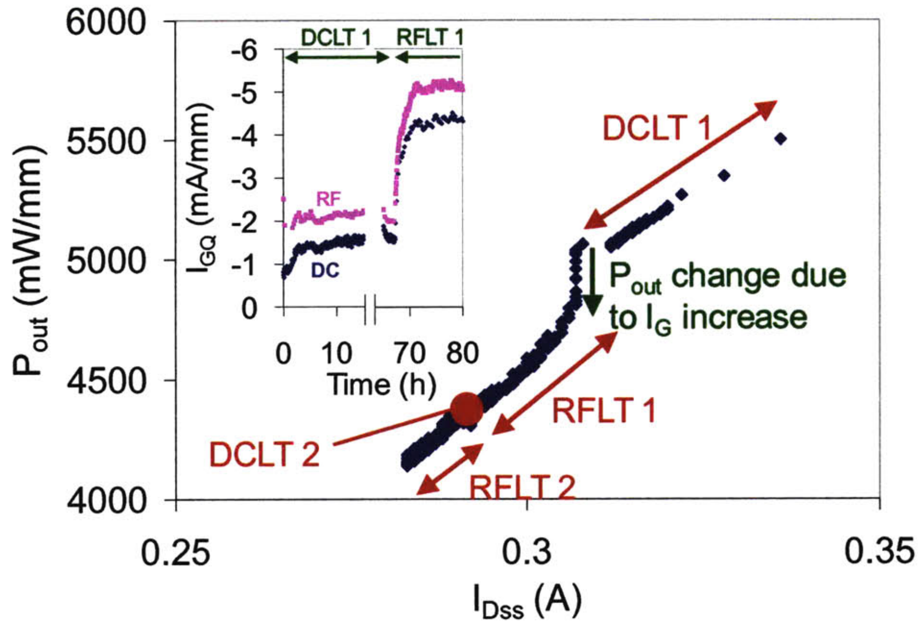

Figure 5-34. Correlation between P_{out} and I_{DSS} in the experiment in Figure 5-34. Inset: Change in I_{GQ} (under RF and without RF) during the stress test.

RF. This cycle is repeated twice. First, we performe the DCLT experiment with the same condition as in Figure 5-31 for 67 hours (marked as DCLT 1 in Figure 5-33; for t=15 to 67 hr, the data is not recorded, but the device is stressed at the set conditions). At this point, we turn on the RF input with P_{in}=23 dBm without changing V_{GS}. This RF stress (RFLT 1) continues until t=90 hr. After RF 1, we stress the device in the same DC condition as before for 22 hours (DCLT 2). Finally, we stress under RF conditions again for 35 hours (RFLT 2). We monitor both RF and DC figures of merit as above.

During DCLT1, the degradation in P_{out} and I_{DSS} almost saturates. During RFLT1, RF stress with the same V_{DS} and T_{CH} degrades the device much more than DC stress does. There is no additional degradation when RF stress is stopped and DC stress is resumed (DCLT 2). However, once the RF input is reapplied, the amplifier starts to degrade again (RFLT 2). This clearly shows that RF stress is a more harsh condition than DC stress in spite of the same V_{DQ} and T_{CH}.

We also find a good correlation between degradation of P_{out} and that of I_{DSS} during DCLT and subsequent RFLT (Figure 5-34). One can see a linear correlation for DCLT 1. Interestingly, P_{out} drops with little change in I_{DSS} upon starting RF stress (indicated with an arrow in Figure 5-34) and then there is a good linear correlation afterwards (RFLT 1-RFLT 2). This sharp P_{out} decrease seems to be related to a large I_G increase after applying RF power (inset of Figure 5-34). This occurs for both the gate current under RF (I_{GQ_RF}) and without RF (I_{GQ_DC}). In our experiments, we observe additional P_{out} degradation during RFLT beyond what DCLT produces the moment I_{GQ} exceeds ~2.5 mA/mm [9]. Beyond a certain threshold, the gate current can decrease the gain and PAE by enhancing forward feedback between input and output stage of the amplifier. Also, a large gate current can degrade the input matching, thus decreasing the output power.

The larger degradation that we observe during RF stress presumably arises from the high instantaneous V_{DS} that is present in RF especially when the device is under high compression. This can be twice as larger than V_{DQ}. This suggests that the maximum instantaneous value of V_{DG} has a large impact in device degradation. In consequence, great care has to be taken when evaluating the life time of GaN HEMT amplifiers based on the DCLT experiments.

5.4. Summary

In this chapter, we have investigated trapping behavior and RF degradation in GaN HEMTs. First, we have separated permanent degradation and trapping-related degradation. We find that both types of degradation sharply increase beyond the critical voltage. We identify that the increase in traps beyond V_{crit} is the main cause of degradation in both I_D and I_G. After an OFF-state stress, these traps are formed at the drain side edge of the gate and provide a leakage path from the gate.

For a detailed characterization of traps, we have developed a trapping analysis methodology to investigate traps in GaN HEMTs. In fresh devices, we identify several traps located above the channel, in the AlGaN or at the surface, and in the buffer. We find that after electrical degradation beyond the critical voltage, the concentration of traps above the channel increase in a marked way, and their time constant spectrum broadens. These traps are generated in the high field region of the device [12]. However, buffer trapping is unaffected by electrical stress. These results are consistent with our hypothesis that traps are produced in the AlGaN barrier layer through the inverse piezoelectric effect.

We have also applied this technique during long term experiments in the OFF-state and high-power state. In the OFF-state, we find that increase in trap density saturates in the early stage of the stress while permanent degradation keeps growing throughout the stress test. In the high-power state, trapping-related degradation is much smaller than in the OFF-state in spite of much higher channel temperature. However, more permanent degradation is observed, which might be related to hot-electron induced degradation. Our methodology can be used for further understanding of trapping behavior and electrical degradation in GaN HEMTs.

We have addressed correlation between DC and RF reliability. We have performed DCLT and RFLT experiments while monitoring complimentary DC and RF figures of merit. We find that a decrease in the DC figure of merit I_{DSS} is an excellent predictor for P_{out} degradation, but that I_{DQ} under DC or RF is not. Due to larger voltage swing under RF input with high compression, RF stress can degrade GaN HEMTs much more than DC stress does even at a same V_{DS} and T_{ch}. In particular, an excessive gate current degradation can seriously impact P_{out}. These results shows that our previous findings in DC stress experiments are in fact relevant to RF reliability of GaN HEMTs.

Chapter 6. Conclusion

6.1. Summary

In this thesis, we have investigated the physics of electrical degradation in GaN high electron mobility transistors. This work is a follow-up to our previous research on investigating various fundamental degradation mechanisms that take place under an electrical stress [10, 26]. In particular, we focus on the inverse piezoelectric effect hypothesis that we proposed in previous work [26]. We investigate more detailed aspects of this degradation mechanism and provide more experimental and theoretical evidence that supports this hypothesis. For the present work, various characterization techniques have been developed. The device characterization suite has been updated to extract more figures of merit in a shorter time. A subset version of the characterization suite has been implemented in an RF life test setup in order to examine the change in various DC parameters during RF life tests. We have also developed a trapping analysis methodology to comprehensively investigate trapping effects in GaN HEMTs.

Through these characterization techniques, we perform a variety of electrical stress experiments. The devices are stressed in different stress schemes such as step-stress, stress-recovery, or step-stress-recovery experiments. In this work, we first focus on degradation in gate current, which was not clearly understood in the previous study. In our experiments, degradation in gate current is found to be a key indicator of degradation. We examine the degradation in gate current characteristics both under forward bias stress and reverse bias stress. Under forward bias stress, the Schottky gate characteristics severely degrade when

the forward gate current exceeds a certain threshold. After the degradation, gate current in both reverse bias (I_{Goff}) and forward bias (I_{Gon}) largely increases. Also, measurements of I_{Goff} and I_{Gon} at different temperature reveal that the activation energy of both I_{Goff} and I_{Gon} becomes almost zero, suggesting an Ohmic-like behavior in gate current characteristics.

On the other hand, I_G degradation under the reverse bias stress is driven by voltage, or electric field. After high-voltage stress in reverse bias, the reverse bias gate current increases several orders of magnitude, and the turn-on voltage in the forward regime shows a small negative shift. Also, the activation energy of I_{Goff} is significantly reduced, whereas that of I_{Gon} appears to be unchanged. This indicates that the effective Schottky barrier height decreases for reverse gate leakage current while it changes little for the forward bias regime.

The degradation in I_{Goff} under reverse bias stress also shows a different critical behavior than under forward bias stress. In step-stress experiments in both the OFF-state and the V_{DS}=0 state, I_{Goff} sharply increases around a critical voltage (V_{crit}) at which degradation in I_D and series resistance also starts to occur. Also, through a diagnostic pulse test, it is shown that traps are created beyond V_{crit}. In a stress-recovery experiment in the OFF-state, degradation in I_G and I_D follows a common trapping behavior, suggesting that the same traps that are produced beyond V_{crit} result in both I_D and I_G degradation. The fact that only R_D and the component of I_{Goff} that flows towards the drain side show trapping behavior demonstrates that these traps are localized in the drain side of the device. The onset of this mode of degradation occurs at lower voltage for lower stress current and also for higher temperature, suggesting that hot-electron effects are not a main cause of it.

From all these results, we have hypothesized that defect formation through the inverse piezoelectric effect is responsible for both I_D and I_G degradation. In our hypothesis, these produced traps not only trap electrons to deplete the channel and thus decrease I_D, but also provides a conduction path from gate to channel and thus increase the gate leakage current.

In spite of the close correlation and seemingly common origin in I_G and I_D degradation, the gate current itself is found not to be a direct cause of the physical degradation.

Our inverse piezoelectric effect hypothesis is tested through stress experiments with additional mechanical stress applied on a device. For these experiments, a specially designed jig is used to apply uniaxial tensile mechanical strain to a chip. In our hypothesis, this additional tensile strain increases the elastic energy in the AlGaN layer and expedites the degradation process. In fact, we confirm that additional tensile strain aggravates degradation in various ways. First, in step-stress experiments in the V_{DS}=0 state and the OFF-state, the critical voltage decreases under external strain. Also, under long-term constant bias stress in the OFF-state, total degradation in I_G and I_D is significantly larger under tensile strain. Finally, in a step-strain experiment in which the level of strain is increased during the experiment, I_{Goff} degradation is enhanced according to the increase in tensile strain. These experiments clearly show that tensile strain or elastic energy in the AlGaN affects degradation, and they are consistent with our hypothesis.

Trapping and detrapping behavior in GaN HEMTs has been also extensively investigated. It is found that I_D degradation consists of permanent and trapping-related components. In our definition, permanent degradation refers to non-recoverable decrease in I_D. On the other hand, the trapping-related degradation refers to the decrease in I_D that is recovered over a long period of time. In our experiments, no matter how heavily a device is degraded, light illumination for 30 seconds effectively detraps almost all the trapped electrons. This allows permanent degradation to be separated from trapping-related degradation. Detailed trapping characteristics have been studied through a new experimental technique that we have developed.

In a fresh device, applying a V_{DS}=0 state pulse induces trapping above the channel, inside the AlGaN layer and/or at surface. This induces trapping in a well-distinguished trap state characterized by a detrapping time constant that is thermally activated with E_a=0.57 eV. On

the other hand, applying an ON-state pulse induces trapping in the buffer region, in addition to the trapping that occurs above the channel as for the $V_{DS}=0$ pulse. This buffer trapping process seems to involve a bottleneck transit process that is temperature independent. As a result, the trapping and detrapping time constants for this trap are the same and are not thermally activated.

We have embedded this new methodology for trap studies in stress experiments. In an OFF-state step-stress, permanent degradation, current collapse, and traps above the channel all start to significantly increase at the critical voltage where I_{Goff} sharply degrades. The increase in permanent degradation beyond V_{crit} makes sense in the framework of our hypothesis in that generated defects that are close to the AlGaN/GaN interface can degrade carrier transport properties and thus permanently decrease I_D. Also, local strain relaxation that may occur due to crack formation could be responsible for reducing the sheet carrier density underneath. In this experiment, a close correlation between I_{Goff} and an increase in current collapse is observed, which confirms that I_G degradation is a sensitive signature of physical damage in the device.

In a long-term stress test in the OFF-state, this trap formation occurs in the early stages of stress and saturates while permanent degradation keeps increasing. It is found that the trap formation process is thermally activated in that it saturates faster and larger current collapse is produced after stress at higher temperature. On the other hand, a long term stress test in high-power state reveals much less trapping-related degradation in spite of higher channel temperature. However, larger permanent degradation occurs during the high-power stress, which could be related to a hot-electron mechanism.

Finally, we have studied the correlation between DC and RF reliability. During RF life tests, the change in DC characteristics has been studied in an effort to understand which DC parameters are affected by RF power degradation. It is found that I_{DSS} correlates well with P_{out} degradation, and other DC parameters show poor correlations. This is confirmed in a

DC life test in which RF characterization is performed. In this DC experiment, a decrease in I_{DSS} also shows a good correlation with P_{out} degradation. These results suggest that the decrease in I_{DSS} (or, at a more fundamental level, I_{Dmax}) is the main cause of RF performance degradation. We have also performed an experiment where DC and RF stresses are alternated. In this experiment, at the same stress bias point, RF stress is found to produce larger degradation than DC stress, suggesting that high electric field that is reached for the peak of the RF waveform produces more damage than the bias point itself. Also, we have found that excessive degradation in I_G can additionally decrease RF output power. This shows the importance of I_G degradation itself. From these experiments, we confirm that our findings are in fact relevant to RF reliability of GaN HEMTs.

From a theoretical point of view, we have tried to understand the detailed physics of the degradation mechanism that is postulated in this work and proposed a model for estimation of the critical voltage. In an AlGaN/GaN HEMT where the AlGaN layer is pseudomorphically grown on a GaN buffer, the AlGaN layer exhibits a large tensile stress, and therefore a certain amount of elastic energy is stored in the AlGaN. Under electrical bias, high vertical electric field through the AlGaN layer increases the tensile stress in AlGaN, and the elastic energy density also increases accordingly. Based on the physics, the change in strain, stress, and elastic energy as a function of applied electric field has been first evaluated. Once the electric field distribution is computed in an electrostatics simulation, the elastic energy density at every point in AlGaN can be calculated. This value is compared to the critical elastic energy density that can be deduced from material growth study data, and the critical voltage is estimated.

We have tested this model against two sets of experimental data that shows different dependencies of V_{crit}. First, we find that V_{crit} decreases as $|V_{GS}|$ increases in OFF-state step-stress experiments. Also, V_{crit} under V_{DS}=0 condition is lower than that in the OFF-state. In addition, V_{crit} decreases as the gate length decreases, but this only in the V_{DS}=0 state. In order to explain these experimental results with our model, it is found that an average

elastic energy density near the drain side of the gate corner determines the onset of degradation. With an averaging length of around 0.1 um, our model predicts all these dependencies correctly.

6.2. Suggestion for improving reliability

The physical understanding of the electrical degradation mechanism that involves the inverse piezoelectric effect suggests several solutions to its mitigation or elimination. As is often the case, these approaches normally entail drawbacks, and most often there is a trade-off between performance and reliability.

Since the degradation mechanism that we postulate occurs when the elastic energy density stored in the AlGaN layer under the gate edge increases beyond its critical value, one of the most efficient ways to increase the critical voltage should be to minimize the initial elastic energy density in the AlGaN barrier. This allows for a larger increase in elastic energy density under electrical stress. This can be accomplished by using a thinner AlGaN barrier or by using AlGaN with lower AlN composition. In fact, evidence of the impact of initial elastic energy on reliability is widely seen in the literature. Lee et al. show a good correlation between RF reliability and AlGaN thickness [21]. In their RF life tests, devices with a thinner AlGaN barrier degrade much slowly. Gotthold et al. show that sheet resistance dramatically degrades after epitaxial growth of AlGaN/GaN layers for high Al composition [86]. In this case, structures with thicker AlGaN layer degrade faster. For lower Al composition, this degradation is not observed. They find micro-cracks through AFM in degraded samples. Also, localized strain relaxation in AlGaN is observed through XRD. Valizadeh et al. also observe more degradation in higher Al mole fraction devices in that a larger threshold voltage shift, more gate leakage current increase, and significant change in LFN signal occur [46]. Coffie et al. show that degradation in gate leakage current can be mitigated by eliminating the AlN spacer layer [27]. Because the AlN spacer is

highly strained, its removal results in much reduced elastic energy in the structure. Also in our previous study, introducing an AlGaN buffer layer, which decrease strain in the AlGaN barrier layer, improves both DC and RF reliability [10]. Finally, using AlGaN buffer instead of GaN buffer is found to improve both DC and RF reliability [10]. In this case, strain in AlGaN barrier layer is reduced due to smaller lattice mismatch. However, for most of these solutions, sheet carrier density decreases and output power performance of the device is degraded. Nevertheless, reducing Al composition seems to be more efficient than reducing the AlGaN thickness because the initial elastic energy changes quadratically with the Al composition, whereas it changes linearly with the thickness. In contrast, sheet carrier density is affected linearly by both parameters, to the first order.

A second path to mitigation should be mechanically strengthening the AlGaN barrier. This can prevent or retard crack formation in the AlGaN layer. This can be accomplished through a GaN cap or by SiN passivation. The GaN cap is found to partially or sometimes completely prevent degradation in sheet resistance that is mentioned above [86]. It presumably holds the AlGaN layer below mechanically and mitigates crack formation. Also, as shown in [51], formation of pits in GaN cap layer sometimes precedes the crack formation in AlGaN. If the cracks are more critical than the pits, a thicker GaN cap can slow down the degradation process. As a result, the critical voltage can be improved or defect formation process can be retarded by GaN cap. Although role of SiN passivation in reliability is generally to inactivate traps and reduce trapping effects, it is also found that SiN layer deposited in situ during heterostructure growth also mitigates strain relaxation and crack formation in the AlGaN layer significantly [30, 87].

Yet another path for mitigation should consist of minimizing the electric field across the AlGaN barrier at the gate edge. For a given voltage, this should reduce the increase in elastic energy by the inverse piezoelectric effect. This can be accomplished through field plates [20]. Engineering of the gate edge such as in a recessed device also ought to help. A reduction in sheet carrier concentration in the drain should also ameliorate the situation by

reducing the peak field. However, it can be generally difficult to reduce the vertical electric field across the AlGaN barrier. Nevertheless, reducing the electric field is also helpful to mitigate any other degradation processes such as hot-electron related mechanisms, and therefore it is always a good solution to improving reliability.

6.3. Suggestion for future work

Although we have extensively investigated the physics of electrical degradation in GaN HEMTs, there are still many issues that need to be clearly understood in order to improve reliability of these devices. In this section, we suggest some of the most relevant ones for future research.

As we have presented in this thesis, our experimental results are largely consistent with the inverse piezoelectric effect induced defect formation mechanism. Nevertheless, a few more experiments can be performed to further understand and support our hypothesis. First, the impact of compressive strain on device reliability needs to be investigated. In our experimental setup, we were unable to apply compressive strain due to small size of the chips. We expect to see the opposite effect of what we have observed in the tensile strain experiments presented in this thesis. In addition, it would be interesting to study reliability of other types of GaN devices that are less likely to be affected by the inverse piezoelectric effect. These include N-face GaN/AlGaN HEMT where no high vertical electric field is present across the AlGaN layer, or InAlN/GaN HEMT where InAlN barrier is lattice matched to GaN and therefore the initial elastic energy density in InAlN is essentially zero. In these devices, we expect that the unique signature of this particular mechanism such as the critical voltage is not observed or observed at much higher voltage although other degradation mechanisms are presumably likely to dominate. Also, impact of substrate residual stress as well as stress from SiN passivation layer would be interesting topics to study.

In theoretical point of view, our model that is presented in Chapter 4 is still in a preliminary stage and needs to be extended. For this, further understanding of the mechanism is still required. For example, the model does not include any temperature dependence although it is almost certain that this kind of defect formation process in crystal is thermally activated. In fact, we observe the temperature dependence of V_{crit} in our experiments. Also, in our model, we do not consider time dependence. As we present in Section 5.2.6, this degradation evolves with time although it can occur in a short period of time when stress voltage is high enough. Therefore, this model needs to be enhanced in order to explain these kinds of dependencies.

Extending the model requires more detailed understanding of mechanisms of micro-crack formation. For instance, it has been sometimes observed that only small pits in GaN cap layer is formed without any evidence of cracks in the AlGaN for lightly degraded devices [51]. However, it is not clear whether this pit formation initiates the crack formation or they are totally independent mechanisms. Also, although it seems that these cracks and pits are continuous along the gate finger when the device is heavily degraded [9], it is not clear whether these cracks are simultaneously created or a small crack is first produced locally and then propagates across the gate. In fact, it has been found that gate current degradation produces discrete bright spots in light emission experiment [29]. Density of these hot spots increases as degradation proceeds. Thus, it would be interesting to correlate these hot spots with crystallographic defects. In order to answer these issues, a certain level of understanding in material science seems to be required.

Also, although the inverse piezoelectric effect mechanism appears to be dominant in our experiments on our devices, we believe other degradation mechanisms can occur concurrently. In particular, for devices in which the device structure and the heterostructure are designed to mitigate the inverse piezoelectric effect mechanism, other mechanisms may show up and be dominant. Therefore, other mechanisms need to be identified and

understood. One such mechanism is the hot-electron effect. As it has been observed by many authors [13, 15-16, 24], including our observation in Section 5.2.6, hot-electrons obviously play important roles in device degradation although their impact is not as clear as in conventional devices. Also, investigation on impact ionization that also produces holes would be interesting as it is found to be a major reliability problem in other III-V devices. In understanding these degradation mechanisms, it is of great importance to investigate the role of channel temperature in reliability [88], which we somehow lack in this thesis.

In addition, RF reliability has to be eventually understood much better. Although we have dealt with some RF experiments in this thesis, there are a lot of RF experiments that would be interesting. As preliminarily shown in this thesis, RF stress can degrade a device more severely due to high instantaneous voltage. In order to better understand RF reliability, more detailed DC and RF characterization needs to be employed in the RF stress tests. Also, various stress conditions such as step-stress and stress-recovery types of experiments would be interesting to examine for RF experiments. Because trapping effects are important in RF characteristics, more thorough understanding of traps that are present in an unstressed device as well as traps that are generated during the stress is necessary beyond what we have explored in this thesis. This comprehensive understanding of physics of degradation should help fundamentally improving overall RF reliability of GaN HEMTs.

Finally, we need to develop a good way to estimate life time of the device. Estimation of device life time is essential for deployment of a new technology. For this, detailed understanding of which stress parameters accelerates degradation to what extent is required. Although we have found that voltage and temperature are two main accelerating factors, qualitative understanding is still lacking. Statistical approach in experiments and also theoretical modeling as mentioned above would help understanding this.

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