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Massachusetts Institute of Technology

Gate-Recessed InAlN/GaN HEMTs on SiC Substrate With Al$_2$O$_3$ Passivation

Jinwook W. Chung, Omair I. Saadat, Jose M. Tirado, Xiang Gao, Shiping Guo, and Tomás Palacios, *Member, IEEE*

Abstract—We studied submicrometer ($L_G = 0.15-0.25$ μm) gate-recessed InAlN/AlN/GaN high-electron mobility transistors (HEMTs) on SiC substrates with 25-nm Al$_2$O$_3$ passivation. The combination of a low-damage gate-recess technology and the low sheet resistance of the InAlN/AlN/GaN structure resulted in HEMTs with a maximum dc output current density of $I_{\rm DS,max} = 1.5$ A/mm and a record peak extrinsic transconductance of $g_{m,\rm ext} = 675$ mS/mm. The thin Al$_2$O$_3$ passivation improved the sheet resistance and the transconductance of these devices by 15% and 25%, respectively, at the same time that it effectively suppressed current collapse.

Index Terms—Al$_2$O$_3$ passivation, GaN, gate recess, high-electron mobility transistor (HEMT), high transconductance, InAlN, SiC substrate.

I. INTRODUCTION

FOR SOLID-STATE power amplifiers, AlGaN/GaN high-electron mobility transistors (HEMTs) have become one of the most important options. These devices have already demonstrated outstanding performance, including output power densities in excess of 32 W/mm at 4 GHz [1] and more than 10 W/mm at 40 GHz [2]. However, several important challenges need to be overcome to increase the performance of these devices even further, including long-term device reliability, minimization of short-channel effects in deeply scaled devices, and reduction of the parasitic capacitances introduced by Si$_x$N$_y$ passivation layers. InAlN/GaN HEMTs have the potential to overcome all these challenges.

Several authors have related the poor reliability of AlGaN/GaN devices to lattice defects introduced by the stress resulting from highly mismatched AlGaN/GaN heterojunctions [3], [4]. In$_{0.17}$Al$_{0.83}$N can be grown lattice matched to GaN [5], thus reducing the defect density due to stress in the barrier layer. In addition, the InAlN barrier normally has higher polarization than the standard AlGaN barrier, which results in higher output current density and power density. DC output current densities of 2.3 A/mm have already been reported with 13-nm-thick In$_{0.19}$Al$_{0.81}$N ($n_s = 2.5 \times 10^{13}$ cm^{-2}, 1170 cm^2/V · s) [6]. In addition, the thickness of the InAlN barrier can be reduced below 10 nm without a significant degradation of the 2-D electron gas density ($n_s = 1.7 \times 10^{13}$ cm^{-2}) [5]. The combination of large current densities and thin barrier layers is very attractive for high-frequency operation as it reduces short-channel effects in transistors with gate lengths below 100 nm.

Surface passivation is another important challenge in high-frequency nitride transistors. Si$_x$N$_y$ passivation has commonly been used to mitigate current collapse in AlGaN/GaN and InAlN/GaN transistors [6]; however, the large thickness normally required for the Si$_x$N$_y$ passivation (>100 nm) significantly degrades the high-frequency operation of the device by increasing total gate capacitances [7]. Therefore, for future high-frequency devices, a new surface passivation scheme needs to be developed with thinner layers.

In this letter, we demonstrate submicrometer gate-recessed InAlN/GaN HEMTs on SiC substrates with a novel 25-nm Al$_2$O$_3$ passivation. The low-damage gate recess allowed a reduction in the gate-to-channel distance down to 3 nm and a record transconductance of 675 mS/mm in 0.15-μm gate-length HEMTs. The thin Al$_2$O$_3$ passivation effectively removed dispersion and improved transport properties in the channel. No current collapse was observed under 200-ns gate-pulse measurements.

II. DEVICE FABRICATION

Fig. 1 shows a schematic cross section of one of the InAlN/GaN HEMTs fabricated in this letter. The InAlN/GaN transistor structures were grown on SiC substrates by metal–organic chemical vapor deposition at IQE RF LLC. In these samples, the InAlN barrier had a total thickness of 7 nm and an Al composition of 81%. A 1-nm AlN interlayer between the GaN channel and the InAlN barrier is used to improve the surface morphology and to increase the electron mobility in the channel by reducing the alloy-related interface roughness and scattering [5]. A total charge density of 1.7×10^{13}/cm^2, an electron mobility of 1060 cm^2/V · s, and a sheet resistance of 325 Ω/square were measured for unpassivated samples using van der Pauw structures at room temperature.

The InAlN/GaN HEMTs were fabricated by first depositing a Ti/Al/Ni/Au metal stack for the ohmic contacts followed by annealing at 870 °C for 30 s in a N$_2$ atmosphere. The source-to-drain distance was 2 μm in all the devices. Then, mesaisolation was performed with a Cl$_2$/BCl$_3$ plasma. Electron-beam lithography was used to define a T-shaped gate, using a trilayer resist
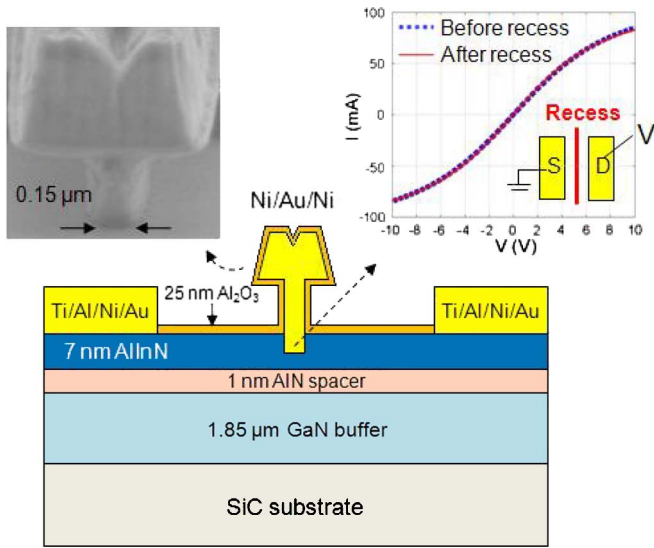
Fig. 1. Schematic cross section of an InAlN/GaN HEMT used in this letter. The left inset shows a scanning electron micrograph of the cross section of a 0.15-μm-length T-shape gate. The right inset shows the current between source and drain contacts after the gate recess. No degradation was observed.

stack made of PMMA/Copolymer/PMMA. For the gate recess, a low-power electron cyclotron resonance reactive ion etching with Cl_2/BCl_3 gas mixture was used. To minimize the damage induced by ion bombardment, radio-frequency (RF) bias was kept low ($\sim$75 V) while ECR power was set to achieve an etch rate of 1 nm/min ($\sim$100 W). The recess depth was 4 nm as measured by an atomic force microscope. The thickness of the remaining InAlN barrier layer was 3 nm. We did not observe any degradation in the source-to-drain current after the recess, and no postannealing step was performed. After the gate recess, a Ni/Au/Ni metal stack was deposited for the gate contact. Devices with gate lengths (L_G) in the 0.15–0.25-μm range were confirmed by a scanning electron microscope. Finally, the devices were passivated with 25 nm of an Al_2O_3 layer ($\varepsilon_r = 10.8$ [8]) deposited by atomic layer deposition with a Cambridge Nanotech Savannah reactor.

III. RESULTS AND DISCUSSION

The effect of the Al_2O_3 passivation on the electron transport of InAlN/GaN HEMTs was evaluated by transfer length measurements. Although the contact resistance (R_c) did not vary (0.3 $\Omega \cdot$ mm), the sheet resistance (R_{sh}) was reduced by 15%, from 325 to 275 Ω/square, after the Al_2O_3 deposition. The same improvement in R_{sh} has been observed in AlGaN/GaN heterostructures [8]. This improvement has been attributed to the increased channel charge density induced by the change in the surface potential due to the high-κ dielectric passivation. Fig. 2 shows the dc characteristics of a typical InAlN/GaN HEMT with a gate length of 0.15 μm. The maximum drain current ($I_{DS,max}$) at $V_{GS} = 2$ V and the peak extrinsic transconductance ($g_{m,ext}$) at $V_{DS} = 5$ V simultaneously increased by 25% after the Al_2O_3 passivation. Owing to this improvement as well as the low-damage gate recess, 0.15-μm-gate-length devices exhibited a high $I_{DS,max}$ of 1.5 A/mm with a record $g_{m,ext}$ of 675 mS/mm. For comparison, the highest
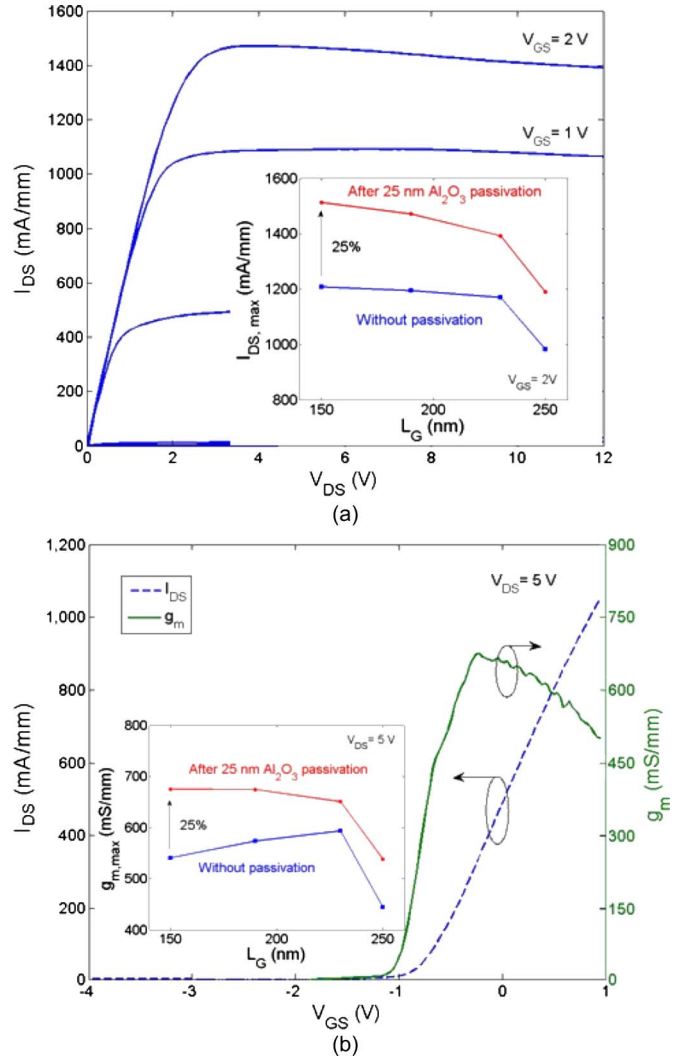

Fig. 2. (a) DC current–voltage characteristics of an InAlN/GaN HEMT ($L_G = 0.15$ μm, $W_G = 25$ μm) with a high maximum output current of 1.5 A/mm. (b) Corresponding transfer curve showing a record peak extrinsic transconductance of 675 mS/mm. The insets show the improvement in (a) $I_{DS,max}$ and (b) $g_{m,max}$ by the Al_2O_3 passivation in submicrometer gate devices.

transconductance reported so far in any nitride semiconductor was 635 mS/mm (with $I_{DS,max} = 1.4$ A/mm) in deep-recessed AlGaN/GaN HEMTs [9]. The combination of high current density and transconductance in a single InAlN/GaN HEMT is very promising particularly for high-frequency high-power applications. The gate recess increased the transconductance of the 0.15-μm device from 420 mS/mm (7-nm barrier) to 675 mS/mm (3-nm barrier), and the threshold voltage (V_T) shifted from −3 to −0.8 V. The reduction of barrier thickness increases gate leakage current ($I_G = 0.4$ mA/mm at $I_{DS,max}$). To minimize the gate leakage and to allow an even more aggressive gate recess, we are developing high-κ gate dielectrics [8].

Current collapse in the fabricated devices was characterized by pulsed I–V measurements. A 200-ns pulse was applied to the gate, while a load resistance of 100 Ω was connected between the drain contact and the drain bias. During the measurement, the drain bias was swept from 0 to 20 V, and the
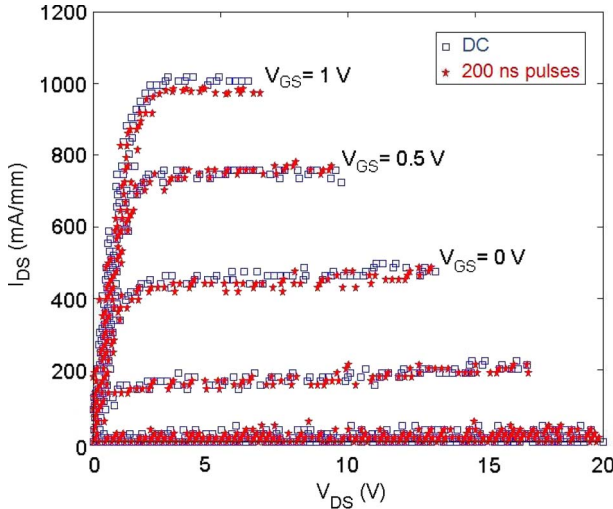
Fig. 3.   DC and pulsed $I-V$ characteristics of InAlN/GaN HEMTs with 25-nm Al_2O_3 passivation. Very limited dispersion was observed under a 200-ns gate pulse and a 100-Ω load line.
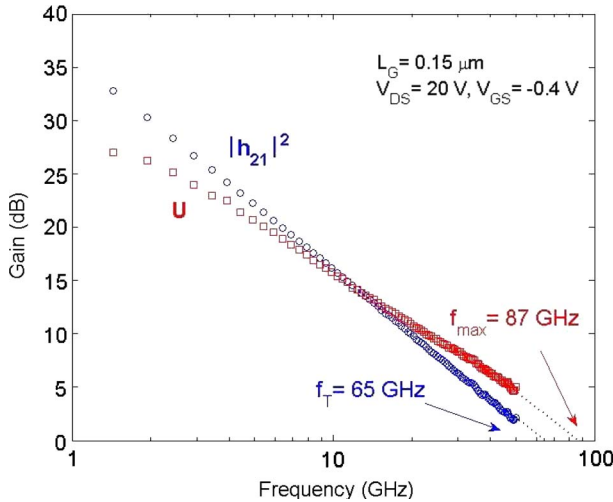

Fig. 4.   RF performance of the 0.15-μm-gate-length HEMT showing $f_T =$ 65 GHz and $f_{max} = 87$ GHz.

gate electrode was pulsed from its quiescent value at pinch-off condition, typically -3 V. The transistors showed no current dispersion after the Al_2O_3 passivation (Fig. 3), which demonstrates the ability of the thin Al_2O_3 layer to effectively passivate the surface states located in the gate-drain access region.

The high-frequency performance of these devices was characterized from 0.45 to 50 GHz using an Agilent Technologies N5230A network analyzer, calibrated with a short-open-load-through calibration standard. On-wafer open and short patterns were used to subtract the effect of parasitic pad capacitances and inductances from the measured S-parameters. Fig. 4 shows the plot of $|h_{21}|^2$ and Mason's unilateral gain U against frequency for the 0.15-μm-gate-length device at $V_{DS} = 20$ V and $V_{GS} = -0.4$ V. A unity current gain cutoff frequency (f_T) of 65 GHz and a power gain cutoff frequency (f_{max}) of 87 GHz were obtained by extrapolating measured data with a slope of -20 dB/dec using a least square fit. Small-signal parameters were extracted from the measured S-parameters following

the method described in [10], and we found that both the gate capacitances ($C_{gs} + C_{gd}$) and the intrinsic transconductance ($g_{m,i}$) were simultaneously increased by 30%–40% by the Al_2O_3 passivation, while their overall effect on f_T and f_{max} ($\sim g_m/(C_{gs} + C_{gd})$) was constant. Simulations of the parasitic capacitances introduced by Si_xN_y and Al_2O_3 passivations show a 20% lower capacitance in the new Al_2O_3 passivation than that in the conventional Si_xN_y passivation due to the lower thickness required for the Al_2O_3 layer (25 versus ~ 100 nm). Thin Al_2O_3 passivation layers are therefore promising candidates for high-frequency devices where the gate capacitances need to be minimized. The lower-than-expected f_T/f_{max} values obtained in this letter are mainly due to a significant reduction of the intrinsic transconductance at high frequencies (> 1 GHz). The study of the origin of this transconductance dispersion between dc and RF measurements is part of our ongoing work.

IV. CONCLUSION

We have investigated submicrometer gate-recessed InAlN/GaN HEMTs on SiC substrates with a thin Al_2O_3 passivation. Owing to the new Al_2O_3 passivation and the low-damage gate recess, devices with a high output current density and record peak transconductance were achieved. The overall device performance demonstrates the great potential of InAlN/GaN HEMTs as a very promising alternative to AlGaN/GaN HEMTs.

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